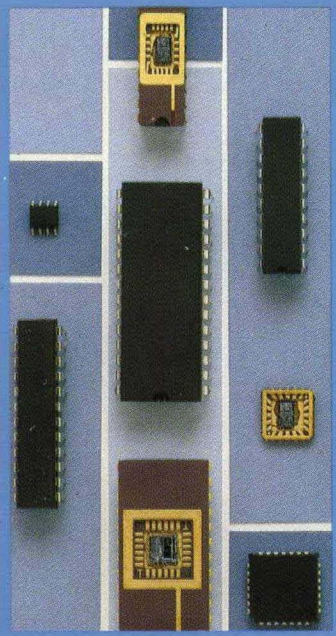
ANALOG DEVICES

1989/90



DATA CONVERSION PRODUCTS DATABOOK

D/A CONVERTERS
A/D CONVERTERS
V/F & F/V CONVERTERS
SYNCHRO & RESOLVER CONVERTERS
SAMPLE/TRACK-HOLD AMPLIFIERS
CMOS SWITCHES & MULTIPLEXERS
VOLTAGE REFERENCES
DATA ACQUISITION SUBSYSTEMS
MICROCOMPUTER I/O BOARDS
APPLICATION SPECIFIC ICS
POWER SUPPLIES
COMPONENT TEST SYSTEMS

DATA CONVERSION PRODUCTS DATABOOK 1989/90

ANALOG DEVICES

How to Find Product Data in This Databook

THIS VOLUME

Contains Data Sheets, Selection Guides and a wealth of background information on signal conversion and a wide variety of components for analog signal processing.

It is one member of a three-volume, 2,800-page set of Databooks describing and specifying Linear, Conversion and DSP products from Analog Devices, Inc., in IC, hybrid and assembled form for measurement, control and real-world signal processing.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Volume-Section-Page location of data sheets bound into this volume.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), add our "AD" prefix and look it up in the index.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your function in the list on the opposite page or in the Table of Contents on pages 1–5 through 1–10. Turn directly to the appropriate Section. You will find a functional Selection Guide at the beginning of the Section. The Selection Guides (and the "Orientation" that usually accompanies them) will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria.

IF YOU CAN'T FIND IT HERE . . . ASK!

If it's not a signal conversion product, it's probably in one of the two sister volumes, the *Linear Products Databook* or the *DSP Products Databook*. If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or phoning (617)-329-4700, Extension 3392.

See Worldwide Service Directory on pages 15–9 and 15–10 at the back of this volume for our sales office phone numbers.

Contents of Other Databooks

LINEAR PRODUCTS DATABOOK

Operational Amplifiers
Comparators
Instrumentation Amplifiers
Isolation Amplifiers
Analog Multipliers/Dividers
Log/Antilog Amplifiers
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Special Function Components
Temperature Transducers
Signal Conditioning Components & Subsystems
Digital Panel Instruments
Application Specific ICs
Power Supplies
Component Test Systems

DSP PRODUCTS DATABOOK

DSP Processors
Microcoded Support Components
Floating-Point Components
Fixed-Point Components

1989/90 DATA CONVERSION PRODUCTS DATABOOK

ANALOG DEVICES

DATA CONVERSION PRODUCTS DATABOOK
July 1989

Products in this book may be covered by one or more of the following patents. Additional patents are pending.

U.S.:
RE29,619, RE29,992, RE30,586, RE31,850, DES. 233,909, 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,268,759, 4,270,118, 4,286,225, 4,309,693, 4,313,083, 4,323,795, 4,338,591, 4,349,811, 4,363,024, 4,374,314, 4,383,222, 4,395,647, 4,399,345, 4,400,689, 4,400,690, 4,427,973, 4,439,724, 4,460,891, 4,475,103, 4,475,169, 4,476,538, 4,481,708, 4,484,149, 4,485,372, 4,491,825, 4,511,413, 4,521,764, 4,543,560, 4,543,561, 4,547,766, 4,547,961, 4,556,870, 4,558,242, 4,562,400, 4,565,000, 4,586,019, 4,586,155, 4,590,456, 4,596,976, 4,601,760, 4,604,532, 4,608,541, 4,622,512, 4,626,769, 4,639,683, 4,644,253, 4,646,056, 4,646,238, 4,678,936, 4,684,922, 4,685,200, 4,694,276, 4,697,151, 4,703,283, 4,707,682, 4,709,167, 4,717,883, 4,722,910, 4,742,331, 4,751,455, 4,752,900 4,761,636, 4,769,564, 4,771,011, 4,774,685, 4,791,551, 4,800,524, 4,808,908, 4,811,296, 4,814,767

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Sweden:
7603320-8

General Information
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Analog Devices designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes – and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SO, LCC, PLCC), and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. More than twenty years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high-performance mixed-signal ASICs.

MAJOR PROGRESS

Since publication of our *1988 Data Conversion Products Databook*, more than 40 significant new data conversion products have been introduced; they run the gamut from brand new product categories and technologies to new standard products (with improvements in price, performance or design) to augmented second-source products. They are all classified and summarized in this Volume, along with existing products that are desirable for use in new designs.

Major new data conversion products include hybrid and monolithic products with high levels of performance and integration, complete and fully guaranteed specifications, and attractive price. For high-speed A/D conversion, these include: the AD9005 (12 bit, 10 MSPS), AD9006 and AD9016 (6 bit, 500 MSPS) with direct and demultiplexed 1:2 output, AD9011 (8 bit, 100 MSPS), AD9028 (8 bit, 300 MSPS) also with direct and demultiplexed 1:2 output, and the AD9048 (8 bit, 20 MSPS). High-speed D/A conversion is available with the AD9712 and AD9713 DACs, providing 100 MSPS and 80 MSPS update rates, respectively.

A variety of speed, functionality, and resolution combinations are available from the AD7769 dual 8-bit ADC and DAC I/O port, the AD7237 and AD7247 dual 12-bit DAC (8+4- or 12-bit parallel data loading), AD662 12-bit single-supply DAC, the AD7840 14-bit DAC (serial or parallel data loading), the AD7772 12-bit, 10 μs serial output ADC, and the AD7871 and AD7872 14-bit ADCs (serial only or serial/parallel data interface). Higher performance is achieved with the AD1679 and AD1779 14-bit, 100 KSPS ADCs with byte-wide and fully parallel interface, the AD1377 16-bit, 10 μs ADC, the AD1362 16-channel, 10 μs ADC, the AD1334 ADC with 4 channels of simultaneous or independent sampling (well-suited for DSP applications), and the AD1330 which provides A/D conversions at 100 KSPS with 18-bit dynamic range and 12 bits of resolution in a floating-point output format.

Digital audio needs are met with the optimized AD1856 (16 bit) and AD1860 (18 bit) DACs, both of which minimize the need for external components; video applications are served by the ADV453, ADV471, ADV476, and ADV478 video DACs plus internal RAM which provide a variety of color resolution, pixel density, and color palette choices. Conversion support circuitry includes the monolithic AD684 quadruple sample/hold amplifier for simultaneous sampling, and the AD1154 and AD386 16-bit sample or track/hold devices. Switching and routing of wide-band signals is facilitated by the AD9300 4-channel video multiplexer.

THE 1989/90 DATA CONVERSION PRODUCTS DATABOOK

This Volume provides complete technical data on Analog Devices "data conversion" products – designed to process, condition and otherwise operate between *analog signals* and *digital signals*. One of a set of three volumes, it is accompanied by the *DSP Products Databook*, dedicated to products for high-performance digital signal-processing (i.e., *digital-to-digital*), and the *Linear Products Databook*, which covers products involved in spanning the interface *between analog signals and analog results.*

The product data in this book is intended primarily for the majority of users who are concerned with new designs. For this reason, those existing and available products that offer little if any unique advantage over newer products in future designs are included in the Index and their data sheets are available from us separately – but they aren't published in this book.

This book includes:

- Comprehensive data sheets on more than 193 significant product families:
- Orientation material and selection guides for rapid product finding;
- A representative list of available Analog Devices technical publications on real-world analog and digital signal-processing;
- Worldwide Service Directory; and
- Product Index to all three volumes.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for precision measurement and control. Besides tutorial material and comprehensive data sheets, including a large amount in our Databooks, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several free serial publications; for example, *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch* is a quarterly newsletter that brings its reader up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to Databook catalogs – and general short-form selection guides, – we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 15-6 to 15-8 at the back of the book.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Service Directory, as of the publication date, appears on pages 15-9 and 15-10 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is the Companywide Quality Improvement Process (QIP). In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 for ICs in the U.S. and Ireland and MIL-STD-1772 for hybrids. More than 25 of our products – both proprietary and second-source – have qualified for JAN part numbers; others are in the process. A larger number of products – including many of the newer ones just starting the JAN qualification process – are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts (the 1987 issue contains data on nearly 150 available product families). A newsletter, *Analog Briefings*, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, they are often suffixed "/+" and are available from stock.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in the Index, turn to page 15-4 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 15-5 you will find a guide to substitutions (where possible) for products no longer available.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

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D/A Converters
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Selection Guide
Digital-to-Analog Converters

VOLTAGE OUTPUT DACs

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Voltage Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page	Comments
AD557	**8**	**0.8**	**8, µP**	**Int**	**N, P**	**C**	**2–43**	**Lowest Cost 8-Bit DACPORT™. Single +5 V Supply**
AD7569	**8**	**1**	**8, µP**	**Int**	**E, N, P, Q**	**C, I, M**	**3–237**	**CMOS, Complete 8-Bit DAC/ADC/SHA/Reference**
AD558	**8**	**3**	**8, µP**	**Int**	**D, E, N, P**	**C, M**	**2–47**	**10 V Out DACPORT. Single or Dual Supply**
AD7224	**8**	**7**	**8, µP**	**2–12.5 V, Ext**	**E, N, P, Q**	**C, I, M**	**2–189**	**CMOS, Low Cost 8-Bit DAC**
HDD-1206	**12**	**2**	**12**	**Int**	**M, W**	**C, M**	**2–459**	**Deglitched Voltage Output**
***AD662**	**12**	**3**	**12, µp**	**2.56 V, Int**	**N, Q**	**C, I, M**	**2–95**	**Complete 12-Bit DACPORT™. Single +5 V Supply**
AD DAC80-V	12	3	12	6.3 V, Int	D	C	2–411	Improved Industry Standard
AD DAC85-V	12	3	12	6.3 V, Int	D	I, M	2–411	Improved Industry Standard
AD DAC87-V	12	3	12	6.3 V, Int	D	I, M	2–411	Improved Industry Standard
AD667	**12**	**3**	**4/8/12, µP**	**10 V, Int**	**D, E, N, P**	**C, I, M**	**2–123**	**Highest Accuracy Complete 12-Bit DAC**
AD767	**12**	**3**	**12, µP**	**10 V, Int**	**D, N**	**C, I, M**	**2–135**	**Fastest Interface Complete 12-Bit DAC**
***AD7848**	**12**	**4**	**12, µP**	**3 V, Int**	**E, N, P, Q**	**C, I, M**	**2–371**	**CMOS, Complete 12-Bit DAC with DSP Interface**
AD7845	**12**	**5**	**12, µP**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**2–345**	**CMOS, 12-Bit Multiplying DAC with Output Amplifier**
AD7245	**12**	**10**	**12, µP**	**5 V, Int**	**E, N, P, Q**	**C, I, M**	**2–221**	**CMOS, 12-Bit Complete DAC, Parallel Load**
AD7248	**12**	**10**	**8, µP**	**5 V, Int**	**E, N, P, Q**	**C, I, M**	**2–221**	**CMOS, 12-Bit Complete DAC, Byte Load**
***AD7840**	**14**	**4**	**14/Serial, µP**	**3 V, Int**	**E, N, P, Q**	**C, I, M**	**2–329**	**CMOS, 14-Bit Complete DAC, Parallel or Serial Load**
***AD1856**	**16**	**1.5**	**Serial, µP**	**Int**	**N**	**C**	**2–161**	**16-Bit PCM Audio DAC**
AD569	**16**	**3**	**8/16, µP**	**±5 V, Ext (M)**	**D, N**	**I, M**	**2–83**	**Monolithic, 16-Bit Monotonic DAC**
AD DAC71-V	16	5	16	6.3 V, Int	D, H	C	2–407	High Resolution 16-Bit DAC
AD DAC72-V	16	5	16	6.3 V, Int	D, H	C, I	2–407	High Resolution 16-Bit DAC
***AD7846**	**16**	**6**	**16, µP**	**Ext (M)**	**D, E, N, P**	**C, I, M**	**2–357**	**CMOS, 16-Bit Multiplying DAC with Readback Capability**
AD1145	**16**	**6**	**8/16/Serial, µP**	**3–6 V, Ext**	**G, PLLCC[4]**	**C**	**2–149**	
DAC1136	**16**	**8**	**16**	**6 V, Int**	**Module**	**I**	**2–453**	**High Resolution and Accuracy**
AD1147	**16**	**20**	**16, µP**	**10 V, Int**	**D**	**I**	**2–155**	**8-Bit Latched Input DAC for Offset and Gain Adjust**
AD1148	**16**	**20**	**16, µP**	**10 V, Int**	**D**	**I**	**2–155**	**Separate 8-Bit Bus for Offset and Gain Adjust DACs**
***AD1860**	**18**	**1.5**	**Serial, µP**	**Int**	**N**	**C**	**2–171**	**18-Bit PCM Audio DAC**
DAC1138	**18**	**10**	**18**	**6 V, Int**	**Module**	**C**	**2–453**	**High Resolution and Accuracy**
AD1139	**18**	**40**	**8, µP**	**–10 V, Int**	**D**	**C**	**2–143**	**True 18-Bit Accuracy**

DACPORT is a trademark of Analog Devices, Inc.

CURRENT OUTPUT DACs

Model	Res Bits	Settling Time µs typ	Bus Interface Bits[1]	Reference Volt Int/Ext (M)[2]	Package Options[3]	Temp Range[4]	Page	Comments
AD9768	**8**	**0.005**	**8, µP**	**−1.26 V, Int**	**D, E**	**C, M**	**2–403**	**Ultrahigh Speed, ECL Compatible, 20 mA Output Current**
AD7524	**8**	**0.1**	**8, µP**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**2–235**	**CMOS, Low Cost, 8-Bit Multiplying DAC with Latch**
AD561	**10**	**0.25**	**10**	**Int**	**D, N**	**C, M**	**2–55**	**Industry Standard 10-Bit DAC, JAN Part Available**
AD7533	**10**	**0.6**	**10**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**2–245**	**CMOS, Low Cost 10-Bit Multiplying DAC**
AD568	**12**	**0.035**	**12**	**Int**	**Q**	**C, M**	**2–71**	**Highest Accuracy 12-Bit Ultrahigh Speed DAC**
HDS-1250	**12**	**0.035**	**12**	**Int**	**D, M**	**C, M**	**2–477**	**Ultrahigh Speed 12-Bit DAC**
AD668	**12**	**0.05**	**12**	**Ext (M)**	**Q**	**C, M**	**2–131**	**Multiplying 12-Bit Ultrahigh Speed DAC**
HDM-1210	**12**	**0.085**	**12**	**Int**	**D**	**I, M**	**2–471**	**Ultrahigh Speed 12-Bit Multiplying DAC**
AD565A	**12**	**0.25**	**12**	**10 V, Int**	**D**	**C, I, M**	**2–63**	**Industry Workhorse High Speed DAC. JAN Part Available**
AD DAC80-I	12	0.3	12	6.3 V, Int	D	C	2–411	Industry Standard, High Speed DAC
AD DAC85-I	12	0.3	12	6.3 V, Int	D	I, M	2–411	Improved Industry Standard
AD DAC87-I	12	0.3	12	6.3 V, Int	D	I, M	2–411	Improved Industry Standard
AD566A	**12**	**0.35**	**12**	**10 V, Ext**	**D**	**C, M**	**2–63**	**High Speed DAC**
AD7541A	**12**	**0.6**	**12**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**2–275**	**CMOS, 12-Bit Multiplying DAC**
AD7548	**12**	**1**	**8, µP**	**Ext (M)**	**E, N, P, Q**	**C, I, M**	**2–305**	**CMOS, Byte Load 12-Bit DAC, Specified with Single and Dual Supplies**
AD562	12	1.5	12	Ext	D	C, I, M	2–59	Industry Standard, JAN Part Available
AD563	12	1.5	12	2.5 V, Int	D	C, M	2–59	Industry Standard
AD7542	**12**	**2.0**	**4, µP**	**Ext (M)**	**D, E, N, P**	**C, I, M**	**2–281**	**CMOS, Nibble Load 12-Bit Multiplying DAC**
AD7543	**12**	**2.0**	**Serial, µP**	**Ext (M)**	**D, E, N, P, Q**	**C, I, M**	**2–289**	**CMOS, Serial Load 12-Bit Multiplying DAC**
AD7545	12	2.0	12, µP	Ext (M)	E, N, P, Q	C, I, M	2–293	CMOS, Parallel Load 12-Bit Multiplying DAC
AD7545A	12	1.0	12, µP	Ext (M)	E, N, P, Q	C, I, M	2–297	CMOS, Improved AD7545
AD7534	**14**	**1.5**	**8, µP**	**Ext (M)**	**D, N, P**	**C, I, M**	**2–251**	**CMOS, Byte Load**
AD7535	**14**	**1.5**	**8/14, µP**	**Ext (M)**	**D, E, N, P**	**C, I, M**	**2–255**	**CMOS, Parallel or Byte Load**
AD7536	**14**	**1.5**	**8/14, µP**	**Ext (M)**	**D, E, N, P**	**C, I, M**	**2–259**	**CMOS, Parallel or Byte Load, Bipolar Output**
AD7538	**14**	**1.5**	**14, µP**	**Ext (M)**	**N, Q**	**C, I, M**	**2–267**	**CMOS, Parallel Load**
***AD1856**	**16**	**0.35**	**Serial, µP**	**Int**	**N**	**C**	**2–161**	**16-Bit PCM Audio DAC**
AD DAC71-I	16	1	16	6.3 V, Int	D, H	C	2–407	High Resolution 16-Bit DAC
AD DAC72-I	16	1	16	6.3 V, Int	D, H	C, I	2–407	High Resolution 16-Bit DAC
***AD1860**	**18**	**0.35**	**Serial, µP**	**Int**	**N**	**C**	**2–171**	**18-Bit PCM Audio DAC**

[1]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; W–Ceramic/Glass Dual-In-Line, Non-Hermetic; Z–Ceramic Leaded Chip Carrier.
[4]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
[5]PLLCC = Plastic Leadless Chip Carrier.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

Selection Guide
Digital-to-Analog Converters

VIDEO DACs

Model	Res Bits	Update Rate MHz min	Settling Time ns max	Reference Voltage Int/Ext[1]	Package Options[2]	Temp Range[3]	Page	Comments
AD9702	4	125	5	Ext	D, W	I	2–391	RGB Output, TTL or ECL Interface
*ADV476	6	66, 50, 35			N	C	2-431	CMOS, Triple 6-Bit Color Palette RAM-DAC
*ADV471	6	80, 50, 35			P	C	2–441	CMOS, Triple 6-Bit Color Palette RAM-DAC
AD9703	8	300	6	Int	D, W	I, M	2–395	Synchronous Composite Functions, Designed for High Resolution Screens, 300 MHz Update Rate
AD9701	8	225	8	Int	E, Q	I, M	2–385	Low Power, Low Glitch Impulse, Synchronous Composite Functions, 250 MHz Update Rate
HDG-0805	8	150	9	Int	D, W	I, M	2–463	−5.2 V Power Supply
AD9700	8	100	12	Ext	D, W	I, M	2–379	Single −5.2 V Power Supply, On-Chip Reference
*ADV478	8	80, 50, 35			P	C	2–441	CMOS, Triple 8-Bit Color Palette RAM-DAC
*ADV453	8	66, 40			N, P	C	2–421	CMOS, Triple 8-Bit Color Palette RAM-DAC
HDG-0807	8	50	14	Int	D, W	I	2–467	TTL-Compatible Inputs
*AD9713	12	80	25	−1.2 V, Int	N, P	C	2–399	TTL Compatible Inputs, Low Glitch Energy
*AD9712	12	100	25	−1.2 V, Int	N, P	C	2–399	ECL Compatible Inputs, Low Glitch Energy

LOGDACs™

Model	Res dB	Full Scale Range dB	Accuracy dB	Package Options[2]	Temp Range[3]	Page	Comments
AD7111	0.375	88.5	0.17	E, N, Q	C, I, M	C2–183	Low Distortion

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MULTIPLE DACs

Model	Res Bits	Out Mode V/I	Settling Time µs typ	Bus Interface Bits[4]	Reference Volt Int/Ext[1]	# DACs	Package Options[2]	Temp Range[3]	Page	Comments
***AD7669**	**8**	**V**	**1**	**8, µP**	**Int**	**2**	**N, P**	**C, I, M**	**3–237**	**CMOS, Complete 8-Bit Dual DAC/ADC/SHA/Reference**
***AD7769**	**8**	**V**	**2.5**	**8, µP**	**Ext**	**2**	**N, P**	**C, I**	**3–329**	**CMOS, Complete 8-Bit Dual DAC/ 2-Channel ADC**
AD7225	**8**	**V**	**5**	**8, µP**	**2–12.5 V, Ext**	**4**	**E, N, P, Q**	**C, I, M**	**2–193**	**CMOS, Separate Reference for Each DAC**
AD7228	**8**	**V**	**5**	**8, µP**	**2–10 V, Ext**	**8**	**E, N, P, Q**	**C, I, M**	**2–205**	**CMOS, Specified with Single and Dual Supplies, Skinny 20-Pin Package**
AD7226	**8**	**V**	**7**	**8, µP**	**2–12.5 V, Ext**	**4**	**E, N, P, Q, R**	**C, I, M**	**2–199**	**CMOS, No User Trims, Specified with Single and Dual Supplies**
AD392	**12**	**V**	**4**	**12, µP**	**Int**	**4**	**M**	**C**	**2–21**	**Fast Bus Access Time (<40ns), Data Readback Capability**
AD390	**12**	**V**	**8**	**12, µP**	**+10 V, Int**	**4**	**D**	**C, M**	**2–13**	**Factory Trimmed Gain and Offset**
***AD7237**	**12**	**V**	**10**	**8, µP**	**+5 V, Int**	**2**	**N, P, Q**	**C, I, M**	**2–213**	**CMOS, Complete 12-Bit Dual, Byte Load**
***AD7247**	**12**	**V**	**10**	**12, µP**	**+5 V, Int**	**2**	**N, P, Q**	**C, I, M**	**2–213**	**CMOS, Complete 12-Bit Dual, Parallel Load**
AD664	**12**	**V**	**10**	**12, µP**	**±14.5 V, Ext (M)**	**4**	**D, E, N, P**	**C, I, M**	**2–103**	**Readback, Reset, Low Power Quad DAC**
AD394	**12**	**V**	**15**	**12, µP**	**±11 V, Ext (M)**	**4**	**D**	**C, M**	**2–27**	**Four Independent Reference Inputs, Precision Amps for Bipolar Output**
AD395	**12**	**V**	**15**	**12, µP**	**±11 V, Ext (M)**	**4**	**D**	**C, M**	**2–27**	**Four Independent Reference Inputs, Precision Amps for Unipolar Output**
AD396	**14**	**V**	**15**	**8, µP**	**±11 V, Ext (M)**	**4**	**D**	**C, M**	**2–35**	**Four Independent Reference Inputs, Bipolar Output, Simultaneous Update**
AD7528	**8**	**I**	**0.2**	**8, µP**	**Ext (M)**	**2**	**E, N, P, Q, R**	**C, I, M**	**2–241**	**CMOS, +5 V to +15 V Operation, TTL Compatible at V_{DD} = 5 V**
AD7628	8	I	0.35	8, µP	Ext (M)	2	E, N, P, Q	C, I, M	2–325	CMOS, +12 V to +15 V Operation, TTL Compatible at V_{DD} = 12 V to 15 V
AD7537	12	I	1.5	8, µP	Ext (M)	2	E, N, P, Q	C, I, M	2–263	CMOS, Byte Load, Double Buffered
AD7547	12	I	1.5	12, µP	Ext (M)	2	E, N, P, Q	C, I, M	2–301	CMOS, Parallel Load
AD7549	12	I	1.5	4, µP	Ext (M)	2	D, E, N, P	C, I, M	2–317	CMOS, Nibble Load, Double Buffered

[1]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[2]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC); W–Ceramic/Glass Dual-In-Line, Non-Hermetic.
[3]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
[4]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

Orientation
Digital-to-Analog Converters

FACTORS IN CHOOSING A D/A CONVERTER

In this catalog there are listed some 57 different families of digital-to-analog converters (DACs). If one were to consider all the variations, there would be several times that number to choose among. The reason for so many different types is the number of degrees of freedom in selection – technological, functional, performance and package. Complete information on converters may be found in the 700-page book, *Analog-Digital Conversion Handbook*, published by Prentice-Hall, Inc.

FUNCTIONAL CHARACTERISTICS

The basic structure of all conventional D/A converters involves a network of precision resistors, a set of switches and some form of level-shifting to adapt the switch drives to the specified logic levels. In addition, the device may contain output-conditioning circuitry, an output amplifier, a reference amplifier, an on-board reference, on-board buffer registers (single- or dual-rank), configuration conditioning and even high-voltage isolation.

Basic DAC

This form which supplies a current, and consequently a small voltage across its internal impedance or an external low-impedance load, is used principally for high speed, for example, the 10ns HDM-1210. Basic current-output DACs, such as the AD565A, are inherently fast, but additional elements (such as an output op amp), furnished by the user to meet overall system specs, slow down the conversion. Some popular CMOS IC devices, such as the AD7543 and the AD7524, are quite simple (and correspondingly low in cost), but they usually require a buffering op amp.

While the basic DAC function is almost always linear, there are exceptions. For example, the AD7111 LOGDAC, which has linear two-quadrant analog response, has a digitally controlled exponential gain function, i.e., 0.375dB per bit; thus its gain at the input code 1000 0000 (binary 128) is -48dB (48×0.375), and the analog output swing for 10V p-p input is 0.04 p-pV_{IN} to $\exp -\left(\frac{0.375N}{20}\right)$.

Output Conditioning

The analog quantity that is the "output" of a DAC, representing the input digital data may be a "gain" (multiplying DAC), a current and/or a voltage. In order to obtain a substantial voltage output at low impedance, an op amp is required. It is often provided by the DAC itself (whether monolithic, modular or hybrid), but many permit the user to choose an external op amp that will meet the particular needs of the application in stability, speed and cost.

Almost all types of DACs provide one or more feedback resistors; they are matched to, and thermally track, resistances in the network so that an external op amp, if used, will not require an external feedback resistor that might introduce tracking errors. If more than one feedback resistor is provided, a choice of analog output voltage ranges becomes available, e.g., 0 – 5V full-scale or 0 – 10V full-scale. If bipolar output-voltage ranges are specified, a bipolar-offset resistor is provided to subtract a half-scale value from the current flowing through the op amp summing point; it is usually derived from the DAC's reference (or analog) input to avoid additional tracking error. Multiplying DACs use an internal or external op amp for bipolar offset.

In order to avoid difficulties, the user must pay special attention to the specified output polarity, its relationship to the reference (if external) and to the input digital code. This can be especially tricky if the output is bipolar and the input requires a complementary (negative-true) digital coding. Another such case is where a current-output DAC, specified for a particular output-voltage polarity when used with an inverting op amp, is used in a mode that develops an output voltage passively (without the op amp) across an external resistive load. In addition to polarity, in this case, the user should be aware of the output-compliance constraint and the specified resistive component of output impedance.

Reference Input

The reference may be specified as external or internal, fixed or variable, single polarity or bipolar. If internal, it may be permanently connected (as in the AD561) or optionally connectible (as in the AD565A). If the DAC is a 4-quadrant multiplying type, the reference (or "analog input") is external, variable and bipolar (e.g., AD7533, AD7541, AD7541A, etc.). The user should check a converter's specifications to determine whether the full-scale accuracy specifications are overall or subdivided into a converter-gain spec and a reference spec.

Digital Data

There a number of ways in which converters differ in regard to the input data: first, the *coding* must be appropriate (binary, offset-binary, twos complement, BCD, arbitrary, etc.), and its sense should be understood (positive-true, negative-true). The *resolution* (number of bits) must be sufficient; in addition, the specifications must be checked to ascertain that the 2^n distinct binary input codes will not only be accepted, but that also they will (if necessary) correspond to 2^n output values in a monotonic progression at any temperature in the operating range with sufficient accuracy. Analog Devices offers DACs with resolutions of 8, 10, 12, 14, 16 and 18 bits. The *data levels* accepted by the converter must be checked (TTL, ECL, low-voltage CMOS, high-voltage CMOS), as must the input loading imposed by the converter and the supply conditions under which the converter will respond to the data. Check the data notation (is the MSB Bit 1 or Bit (n-1)?) – misinterpretation can lead to connecting the data bits in backward order.

If *buffer registers* are desired, the converter should have an appropriate buffer configuration (for example, the AD558 and AD7226 have a set of TTL buffers; the AD667 and AD7224 have two ranks of buffering).

Controls

If the DAC has external digital controls – for example, register strobes – their drive levels, digital sense (true or false), loading and timing must be considered. The function and use of configuration controls (where present), such as serial/parallel, short-cycle or chip-select decoding, should be understood, and the appropriate ways of disabling them when not needed should be employed.

Many DACs are specifically designed to interface directly to the bus of the computer or microprocessor. These DACs provide the necessary control and handshake lines, as well as the data bit buffers, to minimize and often eliminate the interface circuitry

required. The bus timing should be studied with respect to the timing provided by the DAC interface, especially as the processor performs a data-write cycle to the DAC. Systems with higher speed clocks require either shorter DAC strobe times (such as the AD767) or the use of processor-wait states when the DAC is addressed. DACs for video applications, such as the AD9701, provide special control lines unique to CRT applications (e.g. blanking, sync and reference level display).

STATIC AND DYNAMIC PERFORMANCE SPECIFICATIONS

All DACs are specified using terms such as accuracy, linearity, offset, defined and explained below. These static, or "dc," parameters are necessary and sufficient for many applications; they may not be sufficient for others, such as those in digital signal processing, adaptive filtering, or waveform generation. Dynamic, ac specifications define how the DAC performs using parameters such as signal-to-noise ratio (SNR), intermodulation distortion (IMD) and total harmonic distortion (THD). These specifications characterize the performance of the DAC output in applications where the envelope of output changes and output timing errors are critical.

POWER SUPPLIES

Appropriate power supplies should be made available considering the logic levels and analog output signals to be employed into the system. The appropriate degree of power-supply stability to meet the accuracy specs should be employed. In many cases separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals while ensuring that a connection between the grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

SPECIFICATIONS AND TERMS

Definitions of the performance specifications and related information are provided on the next few pages in alphabetical order.

Accuracy, Absolute
Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Sources of error include gain (calibration) error, zero error, linearity errors and noise. Error is usually commensurate with resolution, i.e., less than $2^{-(n+1)}$, or "1/2LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01% of each ideal value.

Absolute accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

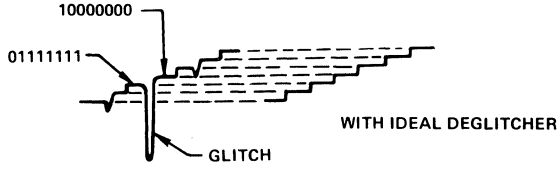
Accuracy, Relative
Relative accuracy error, expressed in %, ppm or fractions of 1LSB is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range) after the full-scale range (FSR) has been calibrated. Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative accuracy error of a linear DAC can be interpreted as a measure of nonlinearity (*see Linearity*).

Compliance-Voltage Range
For a current-output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

Common-Mode Rejection (CMR)
The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually a logarithmic expression representing a "common-mode rejection ratio" e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 10^6:1 means that a 1V common-mode voltage passes through the device as though it were a differential input signal of 1 microvolt.

Common-Mode Voltage
An undesirable signal picked up in a circuit by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

Deglitcher
As the input code to a DAC is increased or decreased by small changes, it passes through what is known as major and minor transitions. The most major transition is at half-scale when the DAC switches around the MSB and all switches change state, i.e., 0111 1111 to 1000 0000. If, at major transitions, the switches are faster (or slower) to switch off than on, this means that for a short time the D/A will give a zero (or full-scale) output and then return to the required 1LSB above the previous reading. Such large transient spikes which differ widely in amplitude and are extremely difficult to filter out are commonly known as "glitches," hence, a deglitcher is a device which removes these glitches or reduces them to a set of small, uniform pulses. It normally consists of a fast sample-hold circuit which holds the output constant until the switches reach equilibrium. Glitch energy is smallest in fast-switching DACs driven by fast logic gates that have little time skew between 0-1 and 1-0 transitions.



Feedthrough
Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplying DAC. It is variously specified in %, ppm, fractions of 1LSB or fractions of 1 volt with a given set of inputs at a specified frequency.

Four-Quadrant
In a multiplying DAC, "four quadrant" refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign.

Gain
The "gain" of a converter is that analog scale-factor setting that provides the nominal conversion relationship, e.g., 10V span for a full-scale code change in a fixed-reference converter. For fixed-reference converters where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain- and zero-adjustment are discussed under *Zero*.

Harmonic Distortion (and Total Harmonic Distortion)
The DAC is driven by the digitized representation of a sine wave. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included such as second through fifth:

$$\text{THD} = 20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4 and V_5 are the rms amplitudes of the individual harmonics.

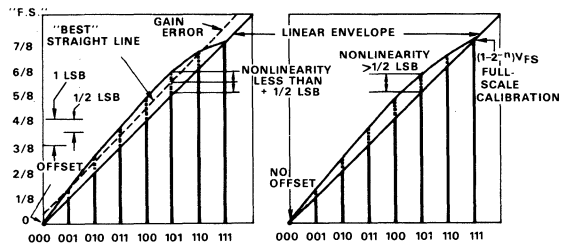
Intermodulation Distortion
The DAC is driven by the digitized representation of two combined sine waves of frequencies f_a and f_b. As with any imperfectly linear device, distortion products (of order m+n) are produced at sum and difference frequencies of $mf_a \pm nf_b$ where m, n = 0, 1, 2, 3, ... Intermodulation terms are those for which m or n is not equal to zero. The second order terms include $(f_a + f_b)$ and $(f_a - f_b)$ and the third order terms are $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$. IMD is defined as:

$$\text{IMD} = 20 \log \frac{\text{(rms sum of the sum and difference distortion products)}}{\text{rms amplitude of the fundamental}}$$

Least-Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost digit is the LSB. Its analog weight, relative to full scale is 2^{-n} where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n-bit converter.

Linearity
Linearity error of a converter (also *integral nonlinearity*, see *Linearity, Differential*), expressed in %, ppm of full-scale range or (sub)multiples of 1LSB, is a deviation of the analog values in a plot of the measured conversion relationship from a straight line. The straight line can be either a "best straight line" determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristics from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (sometimes referred to as "end-point" linearity). End-point linearity error is similar to *relative accuracy* error.

For multiplying D/A converters, the *analog* linearity error, at a specified digital code, is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.



a. ½LSB Nonlinearity Achieved By Arbitrary Location of "Best Straight Line".

b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of a.

Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More Conservative Specification.

Linearity, Differential
Any two adjacent digital codes should result in measured output values that are exactly 1LSB apart (2^{-n} of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called *differential nonlinearity* expressed in (sub)multiples of 1LSB. It is an important specification because a differential linearity error greater than 1LSB can lead to nonmonotonic response in a D/A converter and missed codes in an A/D converter (see *Differential Linearity* in the A/D converter section for an illustration).

Monotonic
A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a *differential nonlinearity* specification since differential nonlinearity less than 1LSB is a sufficient condition for monotonic behavior.

Most-Significant Bit (MSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the leftmost "1" is the MSB with a weight of 2^{n-1}, or 8LSBs. Its analog weight, relative to a DAC's full-scale span, is 1/2. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits.

Multiplying DAC
A multiplying DAC differs from a fixed-reference DAC in being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the "reference" (i.e., analog input) voltage and the fractional equivalent of the digital input number (see also *four-quadrant*).

Noise, Peak and rms
Internally generated random noise is not a major factor in D/A converters, except at extreme resolutions (e.g., DAC1138) and dynamic ranges (AD7111). Random noise is characterized by rms specifications for a given bandwidth or as a spectral density (current or voltage per root hertz); if the distribution is Gaussian, the probability of peak-to-peak values exceeding 7x the rms value is less than 0.1%.

Of much greater importance in DACs is interference in the form of high-amplitude low-energy (hence low-rms) spikes appearing at the DAC's output caused by coupling of digital signals in a surprising variety of ways; they include coupling via stray capacitance, via power supplies, via inadequate ground systems, via feedthrough and by glitch generation. Their presence underscores the necessity for maximum application of the designer's art, including layout, shielding, guarding, grounding, bypassing and deglitching.

Offset
For almost all bipolar converters (e.g., ± 10-volt output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used and the output is offset by half full scale (1MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference because the 1/2 scale offset cancels the weight of the MSB at zero, independently of the amplitude of both.

Power-Supply Sensitivity
The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (of fractions of 1LSB) for a 1% dc change in the power supply, e.g., $0.05\%/1\%\Delta V_S$). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed ± 1/2LSB for a 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit processing. All analog values within a given range of output (of a DAC) are represented by the same digital code usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of ± 1/2LSB due to limited resolution, in addition to the actual conversion errors. For applications in which discrete output levels are desired (e.g., digitally controlled power supplies or digitally controlled gains), this consideration is not relevant.

Resolution
An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a *resolution* of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span. However, a nonlinear device, such as the AD7111 LOGDAC, has a logarithmic gain resolution of 0.375/88.5dB = 1:256dB which corresponds to a gain increment of 4.25%/step or 26,600:1.

Settling Time
The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually ± 1/2LSB) of the final value. Typical prescribed changes are full scale, 1MSB and 1LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op amp circuit.

Signal-to-Noise Ratio
Signal-to-Noise Ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by:

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for an ideal 8-bit converter, SNR = 50dB.

Slew Rate (or Slewing Rate)
Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration such as limited current to charge a capacitor. Amplifiers with slew rate of a few V/μs are common and moderate in cost. Slew rates greater than about 75 volts/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

Stability
Stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficient").

Staircase
A voltage or current increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot) generated by applying a pulse train to a counter and the output of the counter to the input of a DAC.

A very simple A/D converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1LSB, the count is stopped and the code corresponding to the count is the digital output.

Switching Time
In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10% – 90%) but does not include settling time, e.g., to <1/2LSB.

Temperature Coefficients

In general, temperature instabilities are expressed as %/°C, ppm/°C, as fractions of 1LSB/°C or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar) and *zero*.

Gain Tempco: Two factors principally affect converter gain stability with temperature.

a) In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of an AD581L is generally less than 5ppm/°C.
b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters (e.g. AD566K/T). High resolution converters require much better tempcos for accuracy commensurate with the resolution.

Linearity Tempco: Sensitivity of linearity ("integral" and/or differential linearity) to temperature (in % FSR/°C or ppm FSR/°C) over the specified range. Monotonic behavior is achieved if the differential nonlinearity is less than 1LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range and/or implied by a statement that the device is monotonic over the specified temperature range.

Offset Tempco: The temperature coefficient of the all-DAC-switches-off (minus full scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors:

a) The tempco of the reference source
b) The voltage zero-stability of the output amplifier
c) The tracking capability of the bipolar-offset resistors and the gain resistors

Unipolar Zero Tempco (in % FSR/°C or ppm FSR/°C): The temperature stability of a unipolar fixed-reference DAC is principally affected by current leakage (current-output DAC) and offset voltage and bias current of the output op amp (voltage-output DAC).

Total Unadjusted Error

Total unadjusted error is a comprehensive specification which includes internal voltage reference error, relative accuracy, gain and offset errors.

Zero- and Gain-Adjustment Principles

The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for F.S.$(1 - 2^{-n})$ with all bits on. The "zero" of an offset-binary bipolar DAC is set to $-$F.S. with all bits off, and the gain is set for $+$F.S.$(1 - 2^{-(n-1)})$ with all bits on. The data sheet instructions should be followed.

ANALOG DEVICES

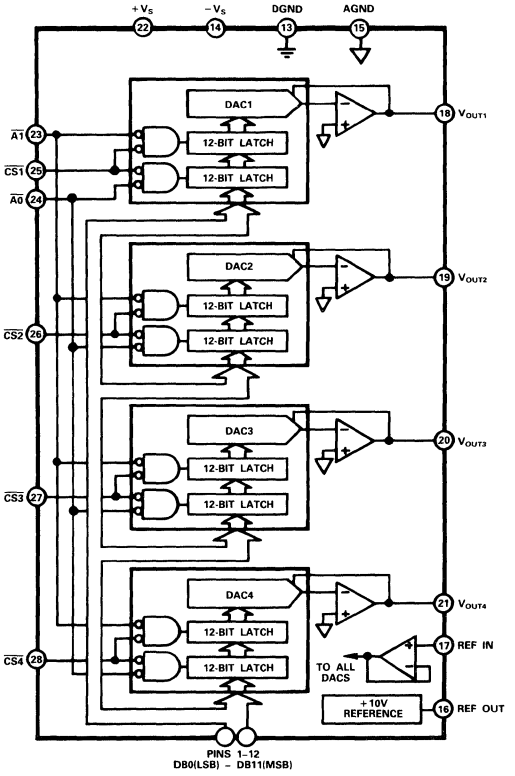
Quad 12-Bit Microprocessor-Compatible D/A Converter

AD390*

FEATURES

Four Complete 12-Bit DACs in One IC Package
Linearity Error ±1/2LSB T_{min} – T_{max} (AD390K, T)
Factory-Trimmed Gain and Offset
Buffered Voltage Output
Monotonicity Guaranteed Over Full Temperature Range
Double-Buffered Data Latches
Includes Reference and Buffer
Fast Settling: 8μs max to ±1/2LSB

AD390 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD390 contains four 12-bit high speed voltage-output digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit DAC chip which reduces chip count and provides high reliability. The AD390 is ideal for systems requiring digital control of many analog voltages where board space is at a premium. Such applications include automatic test equipment, process controllers, and vector-scan displays.

The AD390 is laser-trimmed to ±1/2LSB max nonlinearity (AD390KD, TD) and absolute accuracy of ±0.05 percent of full scale. The high initial accuracy is made possible by the use of thin-film scaling resistors on the monolithic DAC chips. The internal buried zener voltage reference provides excellent temperature drift characteristics (20ppm/°C) and an initial tolerance of ±0.03% maximum. The internal reference buffer allows a single common reference to be used for multiple AD390 devices in large systems.

The individual DACs are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control inputs and the $\overline{A0}$ and $\overline{A1}$ lines. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be simultaneously updated.

The AD390 outputs are calibrated for a ±10V output range with positive-true offset binary input coding. A 0 to +10V version is available on special order.

The AD390 is packaged in a 28-lead ceramic package and is specified for operation over the 0 to +70°C and −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD390 offers a dramatic reduction in printed circuit board space requirements in systems using multiple DACs.
2. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
3. The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±1/2LSB is 8 microseconds maximum.
4. An internal 10 volt reference is available or an external reference can be used. With an external reference, the AD390 gain TC is ±5ppm/°C maximum.
5. The proprietary monolithic DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
6. The 28-pin double-width hybrid package provides extremely high functional density. No external components or adjustments are required to provide the complete function.
7. The AD390SD and AD390TD feature guaranteed accuracy and linearity over the −55°C to +125°C temperature range.

***Covered by patent numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486 and other patents pending.**

SPECIFICATIONS (T_A = +25°C, V_S = ±15V unless otherwise specified)

Model	AD390JD/SD			AD390KD/TD			Units
	Min	Typ	Max	Min	Typ	Max	
DATA INPUTS (Pins 1-12 and 23-28)[1]							
Except Pin 24 TTL or 5 Volt CMOS							
Input Voltage							
Bit ON (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
Bit OFF (Logic "0")			+0.8			+0.8	V
Input Current (Pin 24 is 3× Larger)							
Bit ON (Logic "1")		500	1200		500	1200	μA
Bit OFF (Logic "0")		150	400		150	400	μA
RESOLUTION			12			12	Bits
OUTPUT[2]							
Voltage Range[3]			±10			±10	V
Current			5			5	mA
Settling Time (to ±½LSB)		4	8		4	8	μs
ACCURACY							
Gain Error (w/ext. 10.000V reference)		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Linearity Error		±1/4	±3/4		±1/8	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
TEMPERATURE DRIFT							
Gain (internal reference)			±40			±20	ppm/°C
(external reference)			±10			±5	ppm/°C
Zero			±10			±5	ppm/°C
Linearity Error $T_{min}-T_{max}$		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
CROSS TALK[5]		0.1			0.1		LSB
REFERENCE OUTPUT							
Voltage (without load)	9.997	10.000	10.003	9.997	10.000	10.003	V
Current (available for external use)	2.5	3.5		2.5	3.5		mA
REFERENCE INPUT							
Input Resistance		10^{10}			10^{10}		Ω
Voltage Range	5		11	5		11	V
POWER REQUIREMENTS							
Voltage[6]	±13.5	±15	±16.5	±13.5	±15	±16.5	V
Current							
$+V_S$		12	20		12	20	mA
$-V_S$		−75	−90		−75	−90	mA
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]Timing specifications appear in Table II.

[2]The AD390 outputs are guaranteed stable for load capacitances up to 300pF.

[3] ± 10V range is standard. A 0 to 10V version is also available. To order, use the following part numbers:

AD50207-1	J Grade
AD50207-2	K Grade
AD50207-3	S Grade
AD50207-4	T Grade
AD50207-7	S/883B Grade
AD50207-8	T/883B Grade

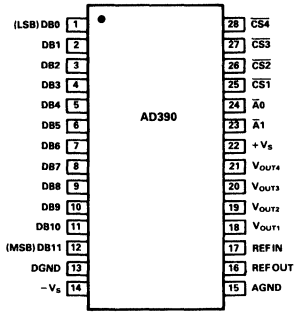
[4]FSR means Full Scale Range and is equal to 20V for a ± 10V range.

[5]Crosstalk is defined as the change in any one output as a result of any other output being driven from − 10V to + 10V into a 2kΩ load.

[6]The AD390 can be used with supply voltage as low as ± 11.4V, Figure 10.

Specifications subject to change without notice.

PIN CONFIGURATION
TOP VIEW



ABSOLUTE MAXIMUM RATINGS

$+V_S$ to DGND . . . . . 0 to +18V
$-V_S$ to DGND . . . . . 0 to −18V
Digital Inputs (Pins 1-12, 23-28) to DGND . . . −10 to +7V
Ref In to DGND . . . . . $\pm V_S$
AGND to DGND . . . . . ±0.6V
Analog Outputs (Pins 16, 18-21)
. . . . . Indefinite Short to AGND or DGND
Momentary Short to $\pm V_S$

ORDERING GUIDE

Model	Temperature Range	Gain Error 25°C	Linearity Error $T_{min}-T_{max}$	Package Option*
AD390JD	0 to +70°C	±4LSB	±3/4LSB	DH-28
AD390KD	0 to +70°C	±2LSB	±1/2LSB	DH-28
AD390SD	−55°C to +125°C	±4LSB	±3/4LSB	DH-28
AD390TD	−55°C to +125°C	±2LSB	±1/2LSB	DH-28

*See Section 14 for package outline information.

Digital Circuit Details

DATA AND CONTROL SIGNAL FORMAT

The AD390 accepts 12-bit parallel data in response to control signals $\overline{CS1}$-$\overline{CS4}$, $\overline{A0}$ and $\overline{A1}$ The input registers are double-buffered, allowing any register to be updated independently of the others. As detailed in Table I, the four chip select lines are used to address the DAC register of interest. It is permissible to have more than one chip select active at any time. The first rank register of a given DAC is loaded by bringing the appropriate chip select and $\overline{A0}$ both low. The second rank register of any DAC can then be loaded by bringing the appropriate chip select $\overline{A1}$ both low. If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincident with $\overline{A1}$ low, all four DAC outputs will be updated to the value in the corresponding first rank register. All control inputs are level-triggered and may be hard-wired low to render any register (or group of registers) transparent.

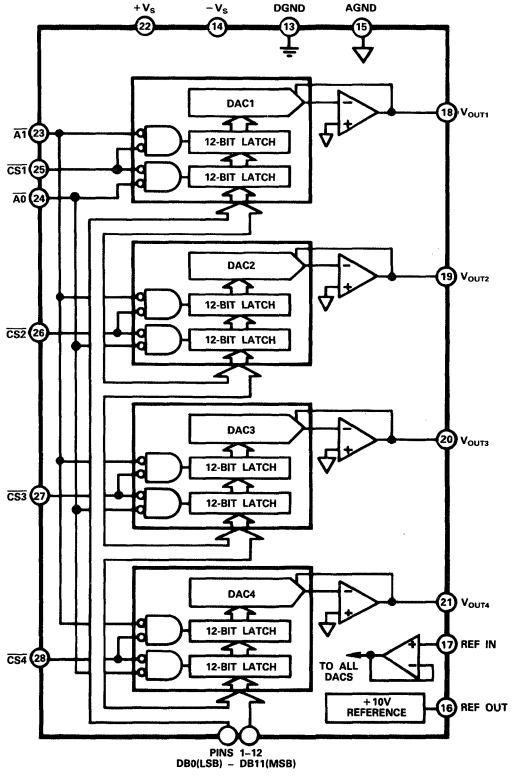


Figure 1. AD390 Functional Block Diagram

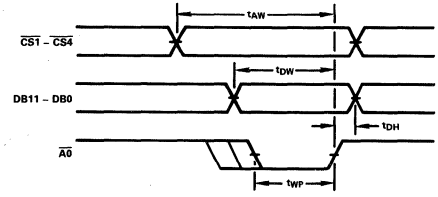
$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{A1}$	$\overline{A0}$	Operation
1	1	1	1	X	X	No Operation
X	X	X	X	1	1	No Operation
0	1	1	1	1	0	Enable 1st rank of DAC 1
1	0	1	1	1	0	Enable 1st rank of DAC 2
1	1	0	1	1	0	Enable 1st rank of DAC 3
1	1	1	0	1	0	Enable 1st rank of DAC 4
0	1	1	1	0	1	Load DAC 1 second rank from first rank
1	0	1	1	0	1	Load DAC 2 second rank from first rank
1	1	0	1	0	1	Load DAC 3 second rank from first rank
1	1	1	0	0	1	Load DAC 4 second rank from first rank
0	0	0	0	0	0	All latches transparent

Table I. AD390 Truth Table

TIMING

The AD390 control signal timing is fairly straightforward. $\overline{A0}$, $\overline{A1}$ and $\overline{CS1}$-$\overline{CS4}$ must be concurrently valid for at least 100ns for a desired operation to occur. When loading data from a bus into the first rank register, the data inputs must be stable for at least 50ns before any control signal returns high. Data can change immediately after the control signals are inactive. When loading the second rank registers from the first rank, it is possible to exercise the chip select inputs at the same time as $\overline{A1}$. DAC settling time is measured from the falling edge of whichever control signal last becomes valid.

WRITE CYCLE #1
(Load First Rank from Data Bus; $\overline{A1}$ = 1)



WRITE CYCLE #2
(Load Second Rank from First Rank; $\overline{A0}$ = 1)

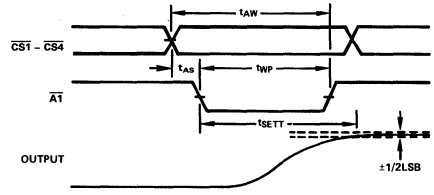


Figure 2. Timing Diagrams

Symbol	Parameter	Min	Typ	Max	Units
t_{AW}	$\overline{CS1}$-4 Valid before $\overline{A0}$ Rising Edge	100			ns
t_{WP}	$\overline{A0}$, $\overline{A1}$ Low Time	100			ns
t_{DW}	DB11-DB0 valid before $\overline{A0}$ Rising Edge	50			ns
t_{DH}	DB11-DB0 valid after $\overline{A0}$ Rising Edge	10			ns
t_{AS}	$\overline{CS1}$-4 valid before $\overline{A1}$ Low	0			ns
t_{SETT}	Output Voltage Settling Time		4	8	µs

Table II. AD390 Timing Specifications

INTERFACING THE AD390 TO MICROPROCESSORS

The AD390 control logic provides simple interface to microprocessors. The latches are fast enough to operate with even the fastest processors.

16-Bit Processors

The AD390 is a 12-bit resolution DAC system and is easily interfaced to 16-bit wide data buses. Several possible addressing configurations exist.

In the circuit of Figure 3, the AD390 second rank registers are made transparent by hard-wiring $\overline{A1}$ low. A system $\overline{WR}$ signal is used to drive the $\overline{A0}$ control input and a 74LS138 decoder driven from the least significant address bits provides the active-low $\overline{CS1}$ through $\overline{CS4}$ signals. In this circuit, only one DAC at a time may be updated. If simultaneous update of all four DACs is required, a slightly different addressing scheme is used. The circuit shown in Figure 4 allows selection of either register of any DAC at the expense of larger memory space requirements. In this circuit, address lines A0 through A3 each select a single DAC of the four contained in the AD390. The use of a separate address line for each DAC allows several DACs to be accessed

simultaneously. The address lines are gated by the simultaneous occurrence of a system $\overline{WR}$ and the appropriately decoded base address. Selection of first rank or second rank register for any DAC is done by using two additional address bits. The AD390 thus occupies a block of 64 memory word locations but offers considerable flexibility in DAC updating.

In this addressing scheme, the A5 and A4 lines divide the 64 locations into 4 blocks. When both A5 and A4 are high, no operation occurs. When A5 and A4 are both low, data written into any one of the DACs (selected by A3-A0) will immediately update that analog output. In the address block where A4 is low and A5 is high, data is written into the first rank register of the selected DAC (or DACs). When A5 is low and A4 is high, data previously written into the first rank register of the selected DAC is transferred to the second rank register, which updates the analog output. It is particularly useful to perform a $\overline{WR}$ operation with A5 low, A4 high, and A3 through A0 all low (base address plus 32) since this action will cause all four DAC outputs to be simultaneously updated to the values previously written into the first rank registers.

In both addressing schemes shown, A0 represents the least significant *word address* bit. In most 16-bit systems this will be the A1 address line. Data may reside in either the 12MSBs (left-justified) or the lower 12 bits (right-justified). Left justification is useful when the data word represents a binary fraction of full scale, while right-justified data usually represents an integer value between 0 and 4095.

8-Bit Processors

Since the AD390 is designed to accept data in 12-bit words, an external latch is required in order to interface with 8-bit buses. Thus each DAC in the AD390 occupies 2 memory locations. The choice of data format is similar to the choice in the 16-bit bus interface. The data can either be right-justified (one byte contains the 8LSBs and another the 4MSBs in the bottom half of the byte) or left-justified (where one byte contains the 8MSBs and another the 4LSBs in the top half of the byte). The addressing scheme illustrated in Figure 6 allows 12-bit data to be sent to the first rank register of any DAC in a right-justified format. The first rank register of DAC occupies two memory locations–a write to the even (A0 low) address stores the 4MSBs of the DAC data in a 74LS173 quad latch. When the 8LSBs are written to the odd address (A0 = 1), the eight bits present on the data bus and the four bits held in the 74LS173 are strobed into the first rank register of the selected DAC. Address bits A1 through A4 select the DAC to be addressed, while A6 and A5 enable either the first or second rank register (or both) as in the 16-bit interface of Figure 4.

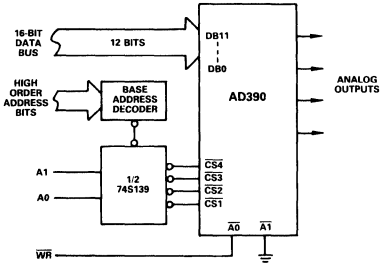


Figure 3. AD390–16-Bit Bus Interface

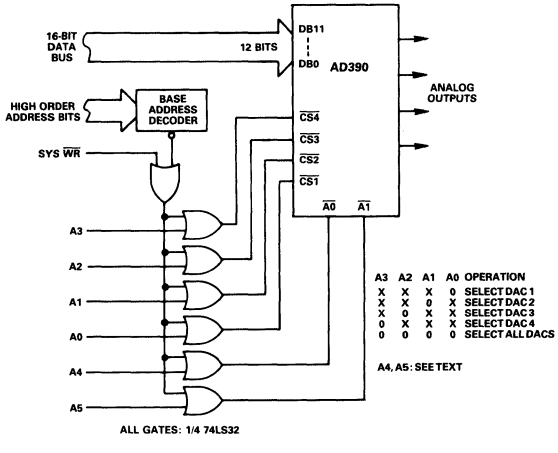
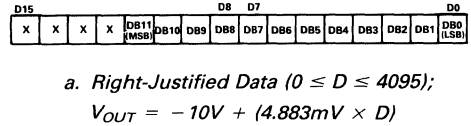
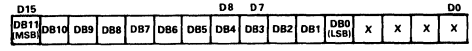


Figure 4. Alternate 16-Bit Bus Interface



a. Right-Justified Data ($0 \leq D \leq 4095$); $V_{OUT} = -10V + (4.883mV \times D)$



b. Left-Justified Data $\left(0 \leq D \leq \frac{65520}{65536}\right)$; $V_{OUT} = -10V + (20V \times D)$

Figure 5. 12-Bit Data Formats for 16-Bit Bus

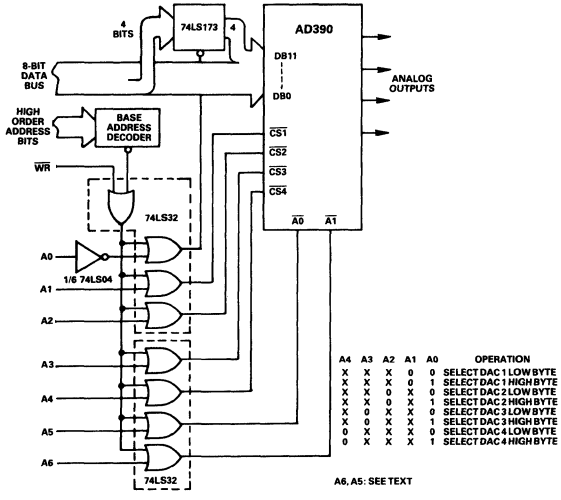


Figure 6. AD390–8-Bit Bus Interface Connections

Analog Circuit Details

REFERENCE CONNECTIONS

The AD390 is equipped with a precision internal reference voltage of 10.00 volts, trimmed to within ±3 millivolts. This reference is available for external use and can typically supply up to 3.5 milliamps of output current. In normal operation, this reference is connected to pin 17 (REF IN), which establishes the ±10 volt output scale. The internal reference is sufficiently accurate for most applications, however, if a master system reference is available, or if a range other than ±10V (±10.24V, for example) is desired, an external reference may be used. It is recommended that the reference used with the AD390 be at least 5 volts and at most 11 volts to preserve specified linearity.

Digital Input Code	Analog Output Voltage	
0000 0000 0000	−10.000V	− Full Scale
0100 0000 0000	−5.000V	− 1/2 Scale
1000 0000 0000	0.000V	Zero
1000 0000 0001	+4.88mV	+1LSB
1100 0000 0000	+5.000V	+ 1/2 Scale
1111 1111 1111	+9.9951V	+ Full Scale − 1LSB

Table III. AD390 Analog Output vs. Digital Input (±V Scale)

GROUNDING RULES

The AD390 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (pin 13) and AGND (pin 15). The DGND pin is the return for the supply currents of the AD390, and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the digital circuitry which drives the AD390.

Pin 15, AGND, is the high quality analog ground connection. This pin should serve as the reference point for all analog circuitry which follows the AD390. It is recommended that any analog signal path carrying significant currents have its own return connection to pin 15 as shown in Figure 7.

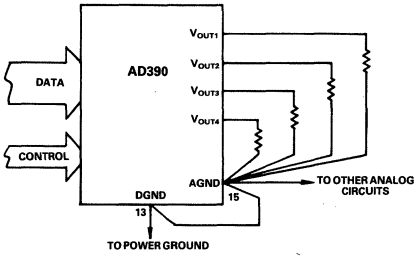


Figure 7. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the AD390 outputs are accurately developed between the output pin and pin 15 (AGND), delivering these signals to remote loads can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD390 packages are used. Figure 8 illustrates the parasitic impedances which influence output accuracy.

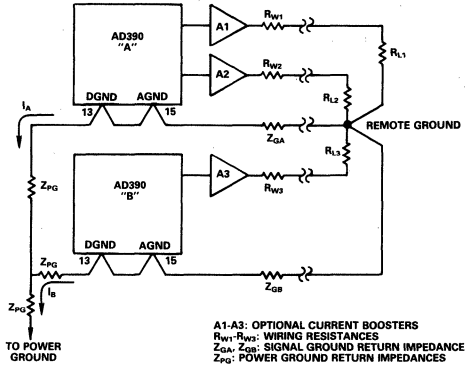


Figure 8. Grounding Errors in Multiple-AD390 Systems

An output buffer configured as a subtractor as shown in Figure 9 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances is eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote ground directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

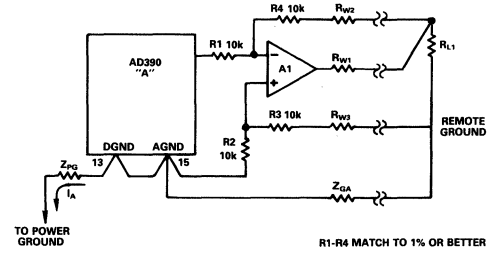


Figure 9. Use of Subtractor Amplifier to Preserve Accuracy

POWER SUPPLY DECOUPLING

The power supplies used with the AD390 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD390 supply pins and the load ground (ideally the AGND pin). If an output booster is used, its supplies should also be decoupled to the load ground.

OPERATION FROM ±12 VOLT SUPPLIES

The AD390 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4V swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 4 millivolts per LSB). The required 8.192V reference can be derived from a precision, low TC divider from the internal +10.000V reference. The only restriction is that the total load resistance presented to the +10.000V reference output must be at least 10kΩ for −55°C to +125°C temperature range 12 volt applications. Figure 10 shows a suggested circuit to set up a ±8.192V output range. Multiple AD390 units can share the same resistive divider-generated reference since the REF IN terminal is very high impedance.

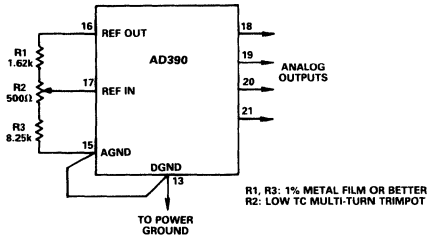


Figure 10. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

IMPROVING FULL-SCALE STABILITY

In large systems using multiple AD390s, it may be desirable for all devices to share a common reference. While it is possible to use the reference output for one device to provide a reference for all devices, use of an external precision reference can greatly improve system accuracy and temperature stability. The external reference should be at least +5V and at most +11V to preserve DAC linearity.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ±1ppm/°C, compared with the 10 to 20ppm/°C drift of the AD390 internal reference. The combination of the AD2710LN and AD390KD shown in Figure 11 will yield a multiple-DAC system with maximum full-scale drift of ±6ppm/°C and excellent tracking.

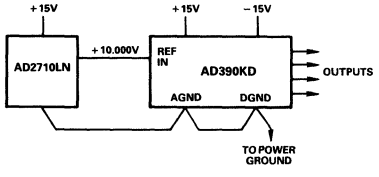
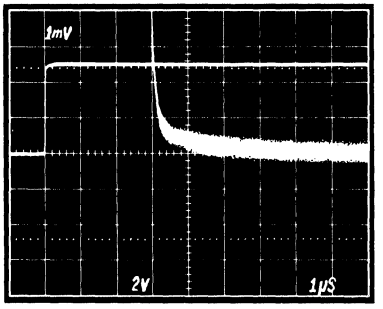


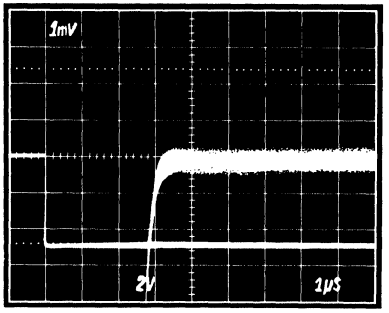
Figure 11. Low Drift AD390 Configuration

OUTPUT CURRENT BOOSTING

The output amplifiers used in the AD390 are capable of supplying a ±10 volt swing into a resistive load of 2kΩ or greater. Stability is guaranteed for load capacitance up to 300pF. Larger load capacitance may cause severe overshoot and possible oscillation. The settling characteristic of the AD390 output amplifier is shown in Figure 12.



a. All Bits OFF-to-ON



b. All Bits ON-to-OFF

Figure 12. AD390 Settling Characteristic

In many applications, including automatic test equipment, the load presented to the AD390 may be less than 2kΩ or include large capacitance. In such cases, it is advisable to use a buffer amplifier capable of delivering rated output to the most severe load anticipated. The AD382, for example, can supply ±10V into a 200Ω load and the AD3554 is suitable for load resistances down to 100Ω. In applications where errors due to output boosting must be minimized, the composite amplifier shown in Figure 13 provides excellent dc stability as well as 100mA output drive capability.

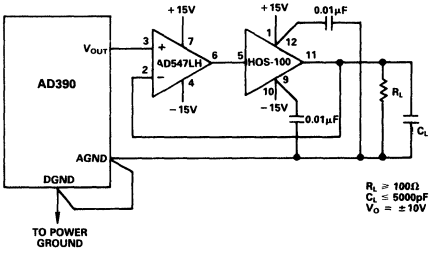


Figure 13. Composite Amplifier for Increased Output Drive

APPLICATIONS

The functional density of the AD390 permits complex analog functions to be produced under digital control, where board space requirements would otherwise be prohibitive. Multiple-output plotters, multi-channel displays and complex waveform generation and multiple programmable voltage sources can all be implemented with the AD390 in a fraction of the space which would be needed if separate DACs were used.

PROGRAMMABLE WINDOW COMPARATOR

The AD390 can be used to perform limit testing of responses to digitally-controlled input signals. For example, two DACs may be used to generate software-controlled test conditions for a component or circuit. The response to these input conditions can either be completely converted from analog to digital or simply tested against high and low limits generated by the two remaining DACs in the AD390.

In the circuit of Figure 14 two AD311 voltage comparators are used with an AD390 to test the output of a 5 volt power supply regulator. The AD390 V_{OUT1} output (through an appropriate current booster) drives the input to the regulator to simulate variations in input voltage. The output of the regulator is applied to comparators 1 and 2, with their outputs wire-ORed with LED indicators as shown. The test limits for each comparator are programmed by the AD390 V_{OUT2} and V_{OUT3} outputs. When the output of the device under test is within the limits, both comparators are off and D1 lights. If the output is above or below the limits, either D4 or D5 lights.

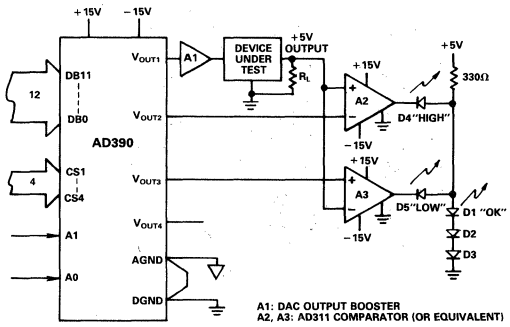


Figure 14. Programmable Window Comparator Used In Power Supply Testing

USING THE AD390 FOR ANALOG-TO-DIGITAL CONVERSION

Many systems require both analog output and analog input capability. While complete integrated circuit analog-to-digital converters (such as the AD574A) are readily available, the AD390 can be used as the precision analog section of an ADC if some external logic is available. Several types of analog-to-digital converters can be built with a DAC, comparator, and control logic, including staircase, tracking, and successive-approximation types. In systems which include a microprocessor, only a comparator must be added to the AD390 to accomplish the ADC function since the processor can perform the required digital operations under software control. A suitable circuit is shown in Figure 15. The AD311 comparator compares the unknown input voltage to one of the AD390 outputs for the analog-to-digital conversion, while the other three outputs are used as normal DACs. The diode clamp shown limits the voltage swing at the comparator input and improves conversion speed. With careful layout, a new comparison can be performed in less than 10 microseconds, resulting in 12-bit successive approximation conversion in under 120 microseconds. The benefit of the AD390 in this application is that one ADC and three DACs can be implemented with only two IC packages (the AD390 and the comparator).

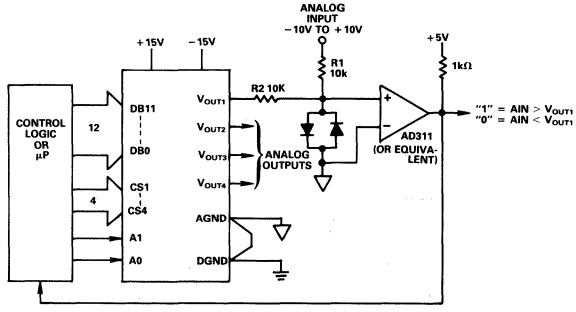


Figure 15. Using One AD390 Output for A/D Conversion

ANALOG DEVICES

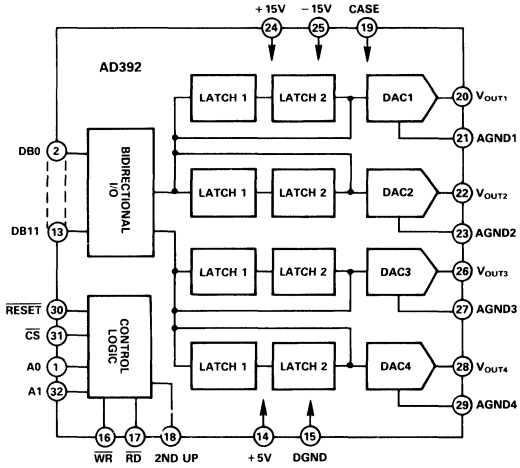
Complete Quad 12-Bit D/A Converter with Readback

AD392

FEATURES

- **Data Readback Capability**
- **Four Complete, Voltage Output, 12-Bit DACs in One 32-Pin Hermetic Package**
- **Fast Bus Access: 40ns max, T_{min}-T_{max}**
- **Asynchronous Reset to Zero Volts**
- **Minimum of Two TTL Load Drive (Readback Mode)**
- **Double-Buffered Data Latches**
- **Monotonicity Guaranteed T_{min}-T_{max}**
- **Linearity Error ±1/2LSB**
- **Low Digital-to-Analog Feedthrough, 2nV·sec typ**
- **Factory Trimmed Gain and Offset**
- **Low Cost**

AD392 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD392 is a quad 12-bit, high speed, voltage output digital-to-analog converter with readback in a 32-pin hermetically sealed package. The design is based on a custom IC interface to complete 12-bit DAC chips which reduces chip count and provides high reliability. The AD392 is ideal for systems requiring digital control of many analog voltages and for the monitoring of these analog voltages especially where board space is a premium. Such applications include ATE, robotics, process controllers and precision filters.

Featuring maximum access time of 40ns, the AD392 is capable of interfacing to the fastest of microprocessors. The readback capability provides a diagnostic check between the data sent from the microprocessor and the actual data received and transferred to the DAC. When $\overline{\text{RESET}}$ is low, all four DACs are simultaneously set to (bipolar) zero providing a known starting point.

The AD392 is laser-trimmed to ±1/2LSB integral linearity and ±1LSB max differential linearity at +25°C. Monotonicity is guaranteed over the full operating temperature range. The high initial accuracy and stability over temperature are made possible by the use of precision thin-film resistors.

The individual DAC registers are accessed by the address lines A0 and A1 and control lines $\overline{\text{CS}}$ and 2ND UP. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be simultaneously updated.

The AD392 outputs are calibrated for a ±10V output range with positive true offset binary input coding.

The AD392 is packaged in a 32-lead metal platform DIP and is hermetically sealed. The AD392 is specified for operation over the 0 to +70°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD392 is packaged in a 32-pin DIP and is a complete solution to space constraint multiple DAC applications.
2. Readback capability provides system monitor of DAC output useful in ATE, robotics or any closed-loop system.
3. Fast bus access time of 40ns maximum allows for fast system updating compatible with high speed microprocessing.
4. Simultaneous reset to zero volts output is extremely useful for system calibration or simply when all DAC outputs must initially start at zero volts.
5. Readback drive capability of two TTL loads virtually eliminates the need to buffer.
6. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors.
7. Monolithic DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
8. Low digital-to-analog feedthrough (2nV·sec typ) is maintained to assure DAC accuracy.

SPECIFICATIONS (V_{CC} = +15V, V_{EE} = −15V, V_{DD} = +5V, T_A +25°C, unless otherwise specified)

Parameter	AD392 Min	AD392 Typ	AD392 Max	Units	Comments
DATA INPUTS (Pins 1-13, 16-18, 30-32)					
TTL Compatible					
Input Voltage					
Bit ON (Logic "1")	+2.0		$+V_{DD}$	V	V_{DD} = 5.25V
Bit OFF (Logic "0")	DGND		+0.8	V	V_{DD} = 4.75V
Input Current					
+25°C	−2		+2	μA	V_{IN} = V_{DD} or GND
T_{min} to T_{max}	−20		+20	μA	V_{IN} = V_{DD} or GND
RESOLUTION			12	Bits	
OUTPUT					
Bidirectional Outputs (Pins 2-13)					
Voltage Output Low (I_{OL} = +4.0mA)	0		+0.4	V	
Voltage Output High (I_{OH} = −4.0mA)	+2.4		V_{DD}	V	
Tristate Output Leakage					
T_{min} to T_{max}	−20		+20	μA	See Note 1
DAC Output Voltage Range		±10		V	
Current Range	−5		+5	mA	
Short Circuit Current			+40	mA	
STATIC ACCURACY					
Gain Error	−0.1	±0.05	+0.1	% of FSR	
Offset	−0.05	±0.025	+0.05	% of FSR	
Bipolar Zero		±0.025		% of FSR	
Integral Linearity Error	−0.5	±0.25	+0.5	LSB	
Differential Linearity Error	−1	±0.5	+1	LSB	
TEMPERATURE PERFORMANCE					
Gain Drift	−25	±20	+25	ppm FSR/°C	
Offset Drift	−25	±20	+25	ppm FSR/°C	
Integral Linearity Error					
T_{min} to T_{max}	−1		+1	LSB	
Differential Linearity Error	–Monotonicity Guaranteed Over Full Temperature Range–				
AC ANALOG PERFORMANCE					
Settling Time (to ± 1/2LSB)					
Change All Register Inputs					
From +5V to 0V/0V to +5V			4	μs	See Note 2
For LSB Change		1	2	μs	
Slew		10		V/μs	
Digital-to-Analog Glitch Impulse		2		nV-sec	See Note 3
Crosstalk		0.1		LSB	See Note 4
POWER REQUIREMENTS					
$+V_{CC}$, $-V_{EE}$	±13.5		±16.5	V	
$+V_{DD}$	+4.5		+5.5	V	
Current (All Digital Inputs DGND or $+V_{DD}$ ONLY, No Load)					
I_{CC}		26	44	mA	
I_{EE}		62	82	mA	
I_{DD}		7.2	13	mA	
Power Dissipation		1356	1955	mW	See Note 5
POWER SUPPLY GAIN SENSITIVITY					
$+V_{CC}$, V_{DD}, $-V_{EE}$			0.002	%FS/%V_S	See Note 6
TEMPERATURE RANGE					
Operating (Full Specifications)	0		+70	°C	
Storage	−65		+150	°C	

NOTES
[1] V_{OUT} = V_{DD} or DGND.
[2] Referenced to trailing rising edge of $\overline{WR}$.
[3] Digital-to-Analog Glitch Impulse: This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. Specified as the area of the glitch in nV-secs.
[4] Crosstalk is defined as the change in any one output as a result of any other output being driven from −10V to +10V into a 2kΩ load.
[5] θ_{JC} approximately 10°C/W.
[6] $+V_{CC}$, $+V_{DD}$, $-V_{EE}$ are ±10%.

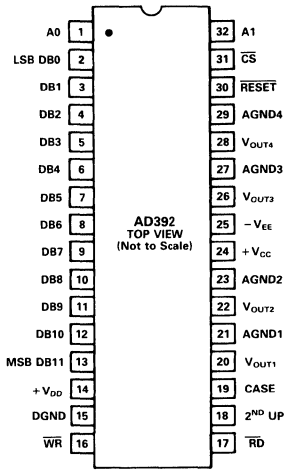
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_{CC}$ to AGND (Any DAC) . . . . . 0 to +18V
$-V_{EE}$ to AGND (Any DAC) . . . . . 0 to −18V
$+V_{DD}$ to DGND . . . . . −0.3V to +7V
Digital Inputs to DGND
(Pins 1-13, 16-18, 30-32) . . . . . −0.3V to +7V
Analog Outputs (Pins 20, 22, 26, 28)
Short Circuit Duration . . . . . Indefinite
($+V_{CC}$, $-V_{EE}$ or AGND)
Storage Temperature . . . . . −65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stess rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}	Package Option*
AD392JV	0 to +70°C	±4LSB	±1LSB	DH-32A

*See Section 14 for package outline information.

Theory of Operation

The AD392 is a quad 12-bit digital-to-analog converter with readback capability. The analog portion of the AD392 includes four bipolar process digital-to-analog converters. Each DAC contains current steering switches and a resistor ladder network which is laser-wafer trimmed for 12-bit accuracy. A precision output amplifier for voltage out operation and an internal highly stable voltage reference are all integrated on a single chip. The DAC is fixed to run in bipolar, 20V span analog output mode as shown in Table I.

Data Input			Analog Output	Analog Output Voltage	
1111	1111	1111	$+1\cdot(V_{REFIN})\left\{\frac{2047}{2048}\right\}$	+9.9951V	+Full Scale − 1LSB
1100	0000	0000	$+1\cdot(V_{REFIN})\left\{\frac{1024}{2048}\right\}$	+5.000V	+1/2 Scale
1000	0000	0001	$+1\cdot(V_{REFIN})\left\{\frac{1}{2048}\right\}$	+4.88mV	+1LSB
1000	0000	0000	$+1\cdot(V_{REFIN})\left\{\frac{0}{2048}\right\}$	+0.000V	Zero
0111	1111	1111	$-1\cdot(V_{REFIN})\left\{\frac{1}{2048}\right\}$	−4.88mV	−1LSB
0100	0000	0000	$-1\cdot(V_{REFIN})\left\{\frac{1024}{2048}\right\}$	−5.000V	−1/2 Scale
0000	0000	0000	$-1\cdot(V_{REFIN})\left\{\frac{2048}{2048}\right\}$	−10.000V	−Full Scale

Table I. AD392 Bipolar Code Table.

The digital portion of the AD392 includes the readback function, control logic and registers all integrated on a custom IC. Data can be latched into any one of the first rank registers by selecting the correct combination of address lines (A0 and A1) and $\overline{CS}$. The second rank registers are controlled by the 2ND UP control line. Use of the 2ND UP line enables the DACs to be updated simultaneously. The digital word can be readback from the second rank registers by asserting the correct address lines, 2ND UP and $\overline{RD}$ command. The $\overline{RD}$ and $\overline{WR}$ commands control the bidirectional I/O port. The AD392 features a $\overline{RESET}$ command for simultaneous update of all DACs to 0 volts out. This is useful for easy system calibration.

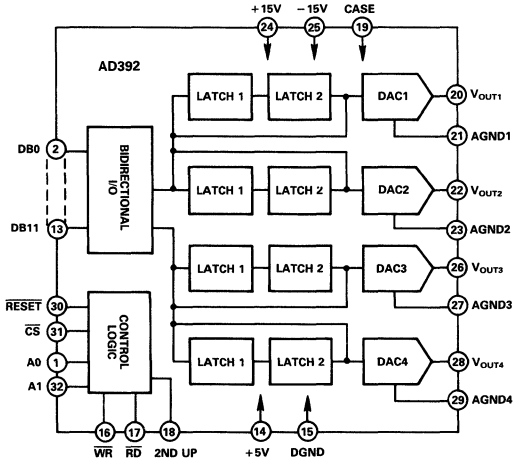


Figure 1. AD392 Block Diagram

DATA AND CONTROL SIGNAL FORMAT

The double buffered registers of the AD392 are addressed by the $\overline{CS}$, A1 and A0 lines. Each rank of registers is 12 bits wide and is presented in a straight offset binary notation. The first rank of registers are loaded sequentially, with valid $\overline{CS}$, A1, A0 on the trailing rising edge of $\overline{WR}$. The second rank of registers, on the other hand, are loaded simultaneously with the data which is in their corresponding first rank registers, with a valid $\overline{CS}$ and positive pulse of the 2ND UP command. (Note: All second rank registers can be made transparent by tieing the 2ND UP line to a Logic "1".) The data loaded into the second rank registers represents the actual digital code which is on the input of the individual DACs. This data can be read back through the data port, with valid $\overline{CS}$, A1 and A0, by taking the $\overline{RD}$ line to a Logic "0". The AD392 also features an asyncronous reset to zero volts for all four DACs by applying a negative pulse to the $\overline{RESET}$ line. Executing a reset replaces the contents of both ranks of registers with the bipolar zero code (MSB equals Logic "1", all other bits equal Logic "0".)

$\overline{CS}$	A1	A0	$\overline{WR}$	$\overline{RD}$	$\overline{RESET}$	2ND Up	Output
1	X	X	X	X	1	X	Chip Read/Write Disable
X	X	X	X	X	0	X	MSBs Go to 1, All Others Go to 0
0	X	X	X	X	1	1	All 2ND Rank Latches Transparent
0	X	X	X	X	1	0	All 2ND Rank Latches Latched
0	0	0	1	0	1	X	Read Back DAC1 2ND Rank
0	0	0	⌐	1	1	X	Write to 1ST Rank DAC1
0	0	1	1	0	1	X	Read Back DAC2 2ND Rank
0	0	1	⌐	1	1	X	Write to 1ST Rank DAC2
0	1	0	1	0	1	X	Read Back DAC3 2ND Rank
0	1	0	⌐	1	1	X	Write to 1ST Rank DAC3
0	1	1	1	0	1	X	Read Back DAC4 2ND Rank
0	1	1	⌐	1	1	X	Write to 1ST Rank DAC4

Symbols: X = Don't Care
1 = Logic High
0 = Logic Low
⌐ = Positive Trailing Edge Triggered

Table II. AD392 Truth Table

TIMING

The timing diagrams (Figures 2 and 3) illustrate the precise relationship between control signals, address signals and the data. The address lines ($\overline{CS}$, A1, A0) as well as the data (D0-D11) must be valid a minimum of 15ns before a $\overline{WR}$ is executed, and the data must remain valid a minimum of 15ns after the $\overline{WR}$ has been executed. Minimum pulse width for the $\overline{WR}$, 2ND UP and $\overline{RESET}$ commands is 15ns. Similarly, the address lines ($\overline{CS}$, A1, A0) must be valid a minimum of 15ns before a $\overline{RD}$ is executed. Data will be valid a maximum of 40ns after $\overline{RD}$ goes low. (Note: This is a MAXIMUM and, therefore, data should be off the bus just before $\overline{RD}$ goes low to avoid bus contention problems, i.e., damage to the device, data bus oscillations which may result in latching erroneous data in the registers.) Data will be off the bus a maximum of 30ns after $\overline{RD}$ goes high. (Note: This is a MAXIMUM and, therefore, the data read should be completed just before $\overline{RD}$ goes high to avoid reading erroneous data.) DAC settling time is measured from the trailing rising edge of the $\overline{WR}$ signal.

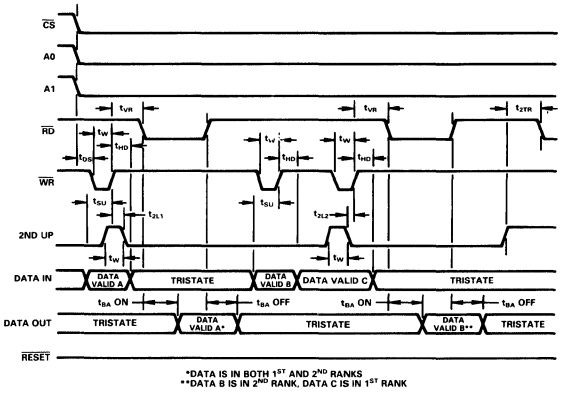


Figure 2. AD392 Write/Read Cycle Timing Diagram

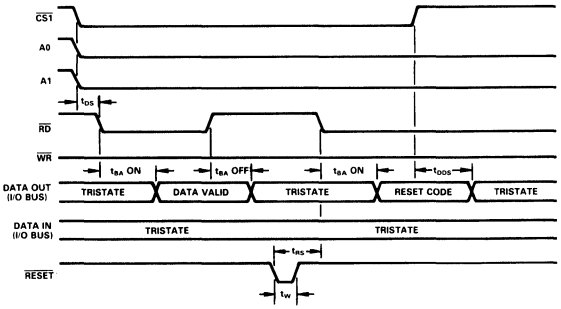


Figure 3. AD392 Read Cycle Timing Diagram

Symbol	Parameter	Min	Max	Unit
t_{DS}	Device Select	15		ns
t_W	Write/Update/Reset Pulse Width	15		ns
t_{SU}	Data Setup Time	15		ns
t_{HD}	Data Hold Time	15		ns
t_{RS}	Reset Valid for Read		35	ns
t_{VR}	Read Valid After Write	30		ns
t_{DDS}	Device De-Select (from Read Data to Tristate		40	ns
t_{BA} On	Bus Access On Time		40	ns
t_{BA} Off	Bus Access Off Time		30	ns
t_{2L1}	Minimum Latch Delay after Write/	10		ns
t_{2L2}	Minimum Latch Delay after Next Write/	5		ns
t_{2TR}	2ND Rank Transparent for Valid Read	25		ns
t_{2TD}	2ND Rank Transparent to DAC Port Outputs		40	ns
t_R, t_F	Data Rise, Fall Times	0	5	ns

NOTES

Timing between pulses measured at 50% points.

Bus access on time measured from 50% point of read going low to active high (2.4) or active low (0.4) (see Figures 4 and 5).

Bus access off time measured from 50% point of read going high to point at which voltage trails away from active high or low under standard tristate load conditions (see Figure 6).

Table III. AC Charactertics: $V_{DD} = 5.0V \pm 10\%$; $0 \leq T_A \leq +70°C$; $V_{IN} = V_{DD}$ or DGND

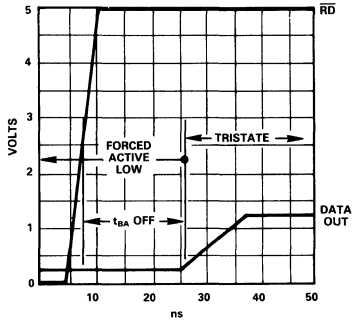


Figure 4. Typical Bus Access Off Time (t_{BA} Off)

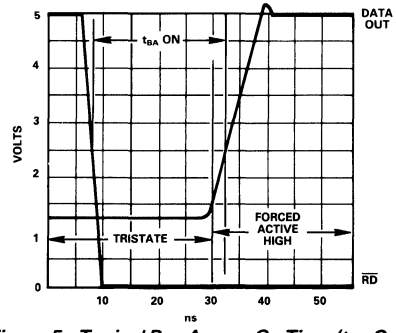


Figure 5. Typical Bus Access On Time (t_{BA} On)

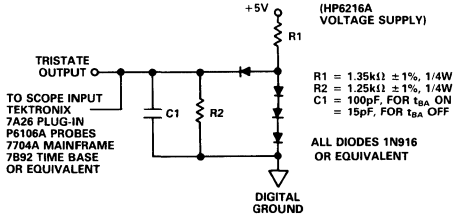


Figure 6. Standard Tristate Load Circuit

SETTLING TIME

The output amplifiers used in the AD392 are capable of supplying a ±10 volt swing into a resistive load of 2kΩ or greater. The settling characteristics of the output amplifier is shown in Figure 7. The test setup used to determine settling time is shown in Figure 8.

POWER SUPPLY DECOUPLING

The power supplies used with the AD392 should be well filtered and regulated. Internally the $+V_{CC}$ and $-V_{EE}$ supplies are independently decoupled about each DAC with 0.039μF chip capacitors to their corresponding AGND. Therefore, if the grounding scheme of Figure 9 is used, it should be sufficient to place a 4.7μF tantalum electrolytic capacitor across the $+V_{CC}$ and $-V_{EE}$ supplies. Decoupling the $+V_{DD}$ supply to DGND should be done in the same manner, however, using a parallel combination of 0.047μF ceramic and a 4.7μF tantalum electrolytic capacitor.

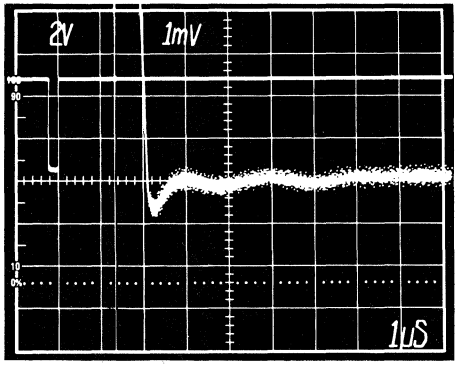


Figure 7. AD392 V_O Settling 20V Step

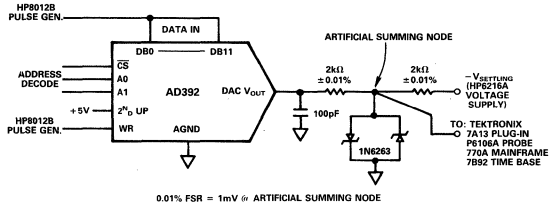


Figure 8. AD392 V_O Settling Time Circuit

GROUNDING RULES

The AD392 has been designed with four independent DAC analog grounds and a separate digital ground return pin. The analog ground pins are not only the reference points for the individual voltage outputs, they also serve as the return path for the switched DAC bit input currents. These rapidly switching currents may be as large as several milliamps for each DAC and, therefore, should be returned to a low impedance node to avoid code dependent linearity errors, digital-to-analog feed-through and crosstalk between DAC outputs. It is recommended that all four DAC analog grounds and the digital ground be tied together at the package for optimal performance. $+V_{CC}$ and $-V_{EE}$ grounds can be tied together back at the system supply and brought up to the AD392 together, whereas the $+V_{DD}$ ground is tied to the other grounds at the package and not back at the system supply. This configuration is recommended because the DAC bit input currents are sourced from the $+V_{DD}$ supply and should return by the shortest possible path and not down the analog return (see Figure 9 for details.).

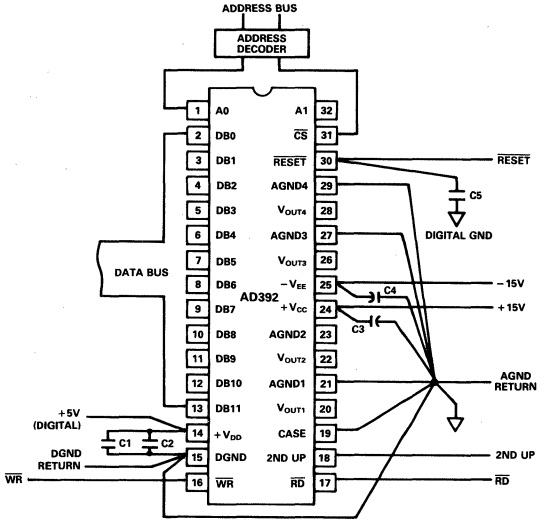


Figure 9. AD392 Recommended Circuit Schematic

CIRCUIT DETAILS

The following two suggestions are intended to aid the user in the normal operation of the AD392:

1. *Bus Termination*: The bidirectional tristateable port of the AD392 (as well as the digital inputs) should not be allowed to "float". These functions are provided by a custom CMOS integrated circuit having an input control circuit which is essentially the common gate contact of a pair of P and N channel MOS devices connected in series between the $+V_{DD}$ and DGND supply lines. An unterminated bus allows the gate potential to float to a point where both channels are partially "on" creating an ohmic path across the supply. Therefore, to avoid excessive supply current drain and possible reflections of the digital signal the bus should be terminated in its characteristic impedance to DGND.
2. *Digital Signal Integrity and the $\overline{\text{RESET}}$ line*: The AD392 has been designed to respond to extremely fast data rates and as a result must operate with a "clean" bus to ensure that valid data is being transmitted (i.e., transients on the bus that cross thresholds with sufficient duration, 5ns-10ns, may cause data to become invalid just before a $\overline{\text{WR}}$ command). If the $\overline{\text{RESET}}$ line is not connected to this "clean" bus (i.e., connected to some sort of power on reset circuitry), then it is recommended that this line be decoupled with a minimum of 1000pf capacitor to avoid an unwanted asynchronous zero volt reset on all four DACs. If this signal is not used, it should be tied to $+V_{DD}$ at the package.

ANALOG DEVICES

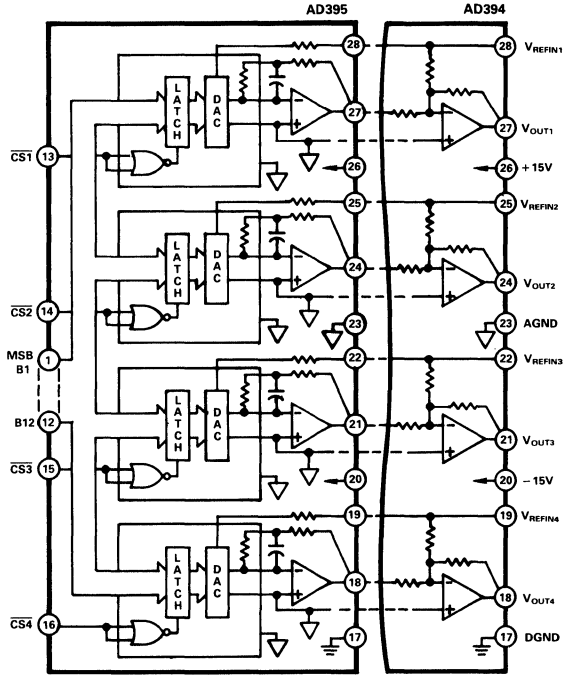
μP-Compatible Multiplying Quad 12-Bit D/A Converters

AD394/AD395

FEATURES

- **Four Complete 12-Bit CMOS DACs with Buffer Registers**
- **Linearity Error ±1/2LSB T_{min}-T_{max} (AD394, AD395K,T)**
- **Factory-Trimmed Gain and Offset**
- **Precision Output Amplifiers for V_{OUT}**
- **Full Four Quadrant Multiplication per DAC**
- **Monotonicity Guaranteed Over Full Temperature Range**
- **Fast Settling: 15μs Max to ±1/2LSB**
- **Available to MIL-STD-883 (See ADI Military Catalog)**

AD394/AD395 FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD394 and AD395 contain four 12-bit, high-speed, low power, voltage output multiplying digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit CMOS DAC chip which reduces chip count and provides high reliability. The AD394 and AD395 both are ideal for systems requiring digital control of many analog voltages where board space is at a premium and low power consumption a necessity. Such applications include automatic test equipment, process controllers, and vector stroke displays.

Both the AD394 and the AD395 are laser-trimmed to ±1/2LSB max differential and integral linearity (AD394, AD395K,T) and full scale accuracy of ±0.05 percent at 25°C. The high initial accuracy is made possible by the use of precision laser trimmed thin-film scaling resistors.

The individual DAC registers are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control pins. These control signals allow any combination of the DAC select matrix to occur (see Table III). Once selected, the DAC is loaded with a single 12-bit wide word. The 12-bit parallel digital input interfaces to most 12- and 16-bit bus systems.

The AD394 outputs (V_{REFIN} = +10V) provide a ±10V bipolar output range with positive-true offset binary input coding. The AD395 outputs (V_{REFIN} = −10V) provide a 0V to +10V unipolar output range with straight binary input coding.

Both the AD394 and the AD395 are packaged in a 28-lead ceramic package and are available for operation over the 0 to +70°C and −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD394, AD395 offer a dramatic reduction in printed circuit board space in systems using multiple DACs.
2. The use of CMOS DACs provides low power consumption.
3. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
4. The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±1/2LSB is 15 microseconds maximum.
5. Maximum gain TC of 5ppm/°C is achievable by both the AD394 and the AD395.
6. The monolithic CMOS DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
7. The 28-pin double-width hybrid package provides extremely high functional density.
8. Two or four quadrant multiplication can be achieved simply by applying the appropriate input voltage signal to the selected DAC's reference (V_{REFIN}).
9. Both the AD394S,TD and AD395S,TD feature guaranteed accuracy and linearity over the −55°C to +125°C temperature range.

SPECIFICATIONS (T_A = +25°C, V_{REFIN} = 10V, V_S = ±15V unless otherwise specified)

Model	AD394JD/SD[1] AD395JD/SD			AD394KD/TD[1] AD395KD/TD			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Pins 1-16)[2]							
TTL or 5 Volt CMOS Compatible							
Input Voltage							
Bit ON (Logic "1")	+2.4		+5.5	+2.4		+5.5	V
Bit OFF (Logic "0")	0		+0.8	0		+0.8	V
Input Current		±4	±40		±4	±40	μA
RESOLUTION			12			12	Bits
OUTPUT							
Voltage Range[3]							
AD394		$\pm V_{REFIN}$			$\pm V_{REFIN}$		V
AD395		0V to $-(V_{REFIN})$			0V to $-(V_{REFIN})$		V
Current	5			5			mA
STATIC ACCURACY							
Gain Error		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Bipolar Zero (AD394)		±0.025			±0.012		% of FSR
Integral Linearity Error[5]		±1/4	±3/4		±1/8	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
TEMPERATURE PERFORMANCE							
Gain Drift			±10			±5	ppm FSR/°C
Offset Drift			±10			±5	ppm FSR/°C
Integral Linearity Error[5]							
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE INPUTS							
Input Resistance	5		25	5		25	kΩ
Voltage Range	−11		+11	−11		+11	V
DYNAMIC PERFORMANCE							
Settling Time (to ±1/2LSB)							
V_{REFIN} = +10V, Change All Digital							
Inputs from +5.0V to 0V		10	15		10	15	μs
V_{REFIN} = 0 to 5V Step,							
All Digital Inputs = 0V		10	15		10	15	μs
Reference Feedthrough Error[6]							
AD395		5			5		mV p-p
AD394		See Figure 1			See Figure 1		
Digital-to-Analog Glitch Impulse[7]		250			250		nV-sec
Crosstalk							
Digital Input (Static)[8]		0.1			0.1		LSB
Reference[9]		2.0			2.0		mV p-p
POWER REQUIREMENTS							
Supply Voltage[10]	±13.5		±16.5	±13.5		±16.5	V
Current (All Digital Inputs 0V or +5V)							
$+V_S$		20	22		20	22	mA
$-V_S$		18	28		18	28	mA
Power Dissipation		570	750		570	750	mW
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]AD394 and AD395 S and T grades are available to MIL-STD-883, Method 5008, Class B. See Analog Devices Military Catalog (1987) for proper part number and detail specification.

[2]Timing specifications appear in Table IV and Figure 5.

[3]Code tables and graphs appear on Theory of Operation page.

[4]FSR means Full Scale Range and is equal to 20V for a ±10V bipolar range and 10V for 0 to 10V unipolar range.

[5]Integral nonlinearity is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function.

[6]For AD395 (unipolar), DAC register loaded with 0000 0000 0000, V_{REFIN} = 20V p-p, 10kHz sinewave. For AD394 (bipolar), V_{REFIN} = 20V p-p, 60 and 400Hz.

[7]This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVs and is measured with V_{REFIN} = AGND.

[8]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2kΩ load by means of varying the digital input code.

[9]Reference crosstalk is defined as the change in any one output as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} @10kHz into a 2kΩ load by means of varying the amplitude of the reference signal.

[10]The AD394 and the AD395 can be used with supply voltages as low as ±11.4V, Figure 10.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to DGND . . . . . −0.3V to +17V
$-V_S$ to DGND . . . . . +0.3V to −17V
Digital Inputs (Pins 1-16) to DGND . . . . . −0.3V to +7V
V_{REFIN} to DGND . . . . . ±25V
AGND to DGND . . . . . ±0.6V
Analog Outputs (Pins 18, 21, 24, 27)
. . . . . Indefinite Short to AGND or DGND
Momentary Short to $\pm V_S$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

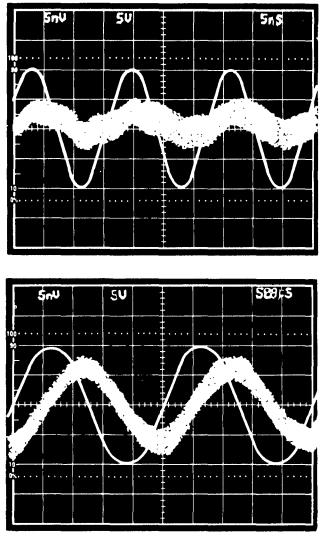


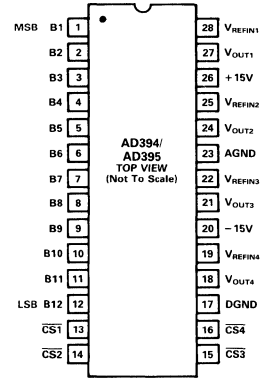
Figure 1. AD394 Feedthrough V_{REFIN} = 60Hz (top photo) and 400Hz (bottom photo) Sinewave. Digital code is set at 1000 000 0000.
SCALE: Reference Input 5V/DIV (Thin Trace)
Feedthrough Output 5mV/DIV
TIME: Top Photo 5ms/DIV
Bottom Photo 500µs/DIV

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD394, AD395, with the inherent reliability of integrated circuit construction, were designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protect the chips from hazardous environments. To further insure reliability, the AD394, AD395 are both fully compliant to MIL-STD-883 Class B, Method 5008.

Consult Analog Devices Military Catalog for proper ordering part number and detail specification.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}	Package Option*
AD394JD	0 to +70°C	±4LSB	±3/4LSB	DH-28A
AD395JD	0 to +70°C	±4LSB	±3/4LSB	DH-28A
AD394KD	0 to +70°C	±2LSB	±1/2LSB	DH-28A
AD395KD	0 to +70°C	±2LSB	±1/2LSB	DH-28A
AD394SD	−55°C to +125°C	±4LSB	±3/4LSB	DH-28A
AD395SD	−55°C to +125°C	±4LSB	±3/4LSB	DH-28A
AD394TD	−55°C to +125°C	±2LSB	±1/2LSB	DH-28A
AD395TD	−55°C to +125°C	±2LSB	±1/2LSB	DH-28A

*See Section 14 for package outline information.

Theory of Operation

The AD394 quad DAC provides four-quadrant multiplication. It is a hybrid IC comprised of four monolithic 12-bit CMOS multiplying DACs and eight precision output amplifiers. Each of the four independent-buffered channels has an independent reference input capable of accepting a separate dc or an ac signal for multiplying or for function generation applications. The CMOS DACs act as digitally programmable attenuators when used with a varying input signal or, if used with a fixed dc reference, the DAC would act as a standard bipolar output DAC. In addition, each DAC has a 12-bit wide data latch to buffer the converter when connected to a microprocessor data bus.

The AD395 quad DAC provides two-quadrant multiplication and is comprised of four 12-bit CMOS multiplying DACs and four precision output amplifiers. The two-quadrant-multiplication function arises from a straight-binary digital input multiplied by a bipolar analog input which results in two-quadrant multiplication. The AD395 can also operate as a standard unipolar DAC when a fixed dc reference is applied to V_{REFIN}.

MULTIPLYING MODE

The figures below show the transfer function for each model. The diagrams indicate an area over which many different combinations of the reference input and digital input can result in a particular analog output voltage. The highlighted transfer line in each diagram indicates the transfer function if a fixed reference is at the input. The digital codes above each diagram indicate the mid and endpoints of each function. The relationship between the reference input (V_{REFIN}) the digital input code and the analog output is given in Tables I and II below. Note that the reference input signal sets the slope of the transfer function (and determines the full scale output at code 111 . . 111) while the digital input selects the horizontal position in each diagram.

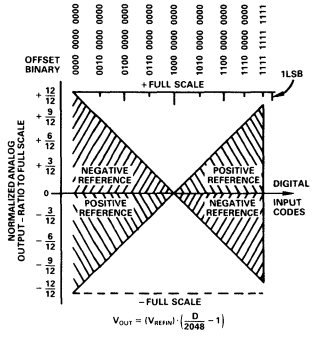


Figure 2. AD394 as a Four-Quadrant Multiplier of Reference Input and Digital Input

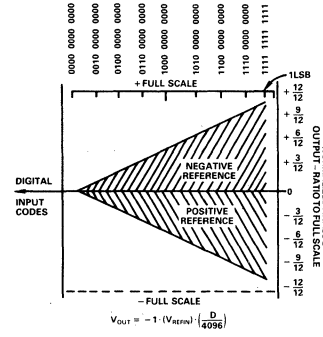


Figure 3. AD395 as a Two-Quadrant Multiplier of Reference Input and Digital Input

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$+1 \cdot (V_{REFIN}) \left\{\frac{2047}{2048}\right\}$	+9.9951V	+FULL SCALE − 1LSB
1100	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	+5.000V	+1/2 SCALE
1000	0000	0001	$+1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	+4.88mV	+1LSB
1000	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{0}{2048}\right\}$	+0.000V	ZERO
0111	1111	1111	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	−4.88mV	−1LSB
0100	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	−5.000V	−1/2 SCALE
0000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{2048}{2048}\right\}$	−10.000V	−FULL SCALE

Table I. AD394 Bipolar Code Table

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$-1 \cdot (V_{REFIN}) \left\{\frac{4095}{4096}\right\}$	−9.9976V	−FULL SCALE − 1LSB
1000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{2048}{4096}\right\}$	−5.000V	−1/2 SCALE
0000	0000	0001	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{4096}\right\}$	−2.44mV	−1LSB
0000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{0}{4096}\right\}$	0.000V	ZERO

Table II. AD395 Unipolar Code Table

DATA AND CONTROL SIGNAL FORMAT

The AD394 and AD395 accept 12-bit parallel data in response to control signals $\overline{CS1}$-$\overline{CS4}$. As detailed in Table III, the four chip select lines are used to address the DAC register of interest. It is permissible to have more than one chip select active at any time. If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincident, all four DAC outputs will be updated to the value located on the data bus. All control inputs are level-triggered and may be hard-wired low to render any register (or group of registers) transparent.

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Bus
1	0	1	1	Load DAC 2 From Data Bus
1	1	0	1	Load DAC 3 From Data Bus
1	1	1	0	Load DAC 4 From Data Bus
0	0	0	0	All DACs Simultaneously Loaded

Table III. DAC Select Matrix

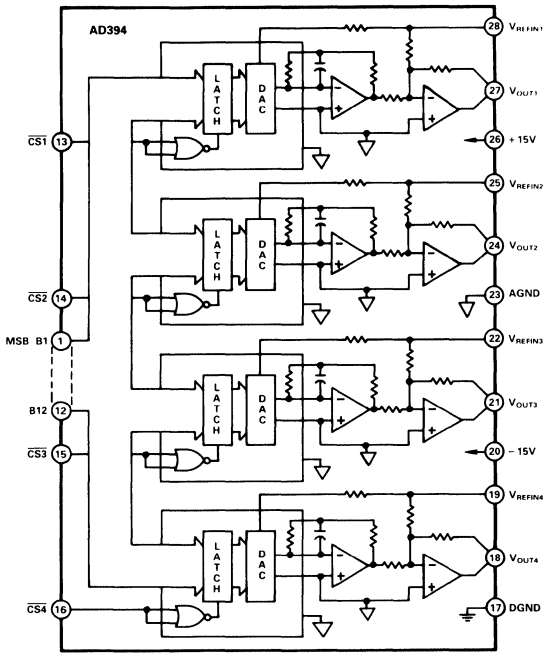


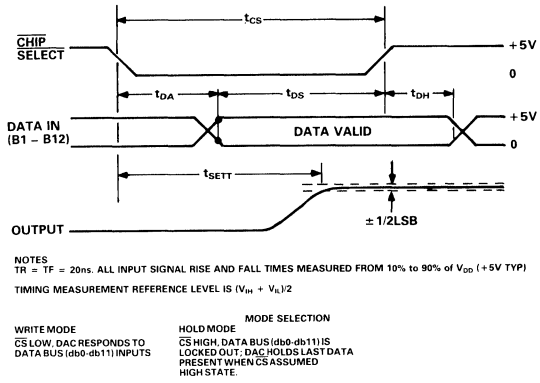
Figure 4. AD394 (Bipolar) Functional Block Diagram

TIMING

The AD394, AD395 control signal timing is very straightforward. $\overline{CS1}$-$\overline{CS4}$ must maintain a minimum pulsewidth of at least 380ns for a desired operation to occur. When loading data from a bus into a 12-bit wide data latch, the data must be stable for at least 210ns before returning CS to a high state. When the $\overline{CS}$ is low, the data latch is transparent allowing the data at the input to propagate through to the DAC. Data can change immediately after the chip select returns high. DAC settling time is measured from the falling edge of the active chip select.

Symbol	Parameter	T_{min} to T_{max}	Units
t_{CS}	Chip Select Pulse Width	380	ns min
t_{DA}	Data Access Time	0	ns min
t_{DS}	Data Set-Up Time	210	ns min
t_{DH}	Data Hold Time	10	ns min

Table IV. AD394, AD395 Timing Specifications



NOTES
TR = TF = 20ns. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% to 90% of V_{DD} (+5V TYP)

TIMING MEASUREMENT REFERENCE LEVEL IS $(V_{IH} + V_{IL})/2$

MODE SELECTION

WRITE MODE	HOLD MODE
$\overline{CS}$ LOW, DAC RESPONDS TO DATA BUS (db0-db11) INPUTS	$\overline{CS}$ HIGH, DATA BUS (db0-db11) IS LOCKED OUT; DAC HOLDS LAST DATA PRESENT WHEN CS ASSUMED HIGH STATE.

Figure 5. Timing Diagram

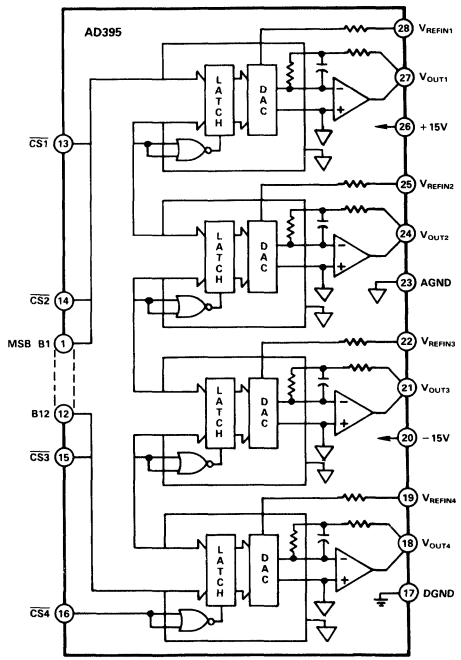


Figure 6. AD395 (Unipolar) Functional Block Diagram

Analog Circuit Details

GROUNDING RULES

The AD394 and AD395 include two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (pin 17) and AGND (pin 23). The DGND pin is the return for the supply currents of the AD394, AD395 and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the circuitry which drives the digital inputs.

Pin 23, AGND, is the high-quality analog ground connection. This pin should serve as the reference point for all analog circuitry associated with the AD394, AD395. It is recommended that any analog signal path carrying significant currents have its own return connection to pin 23 as shown in Figure 7.

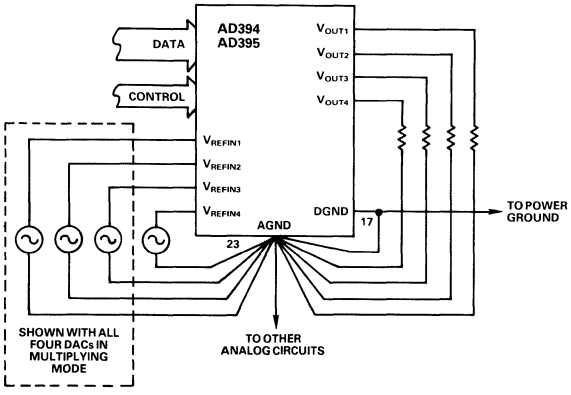


Figure 7. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the DAC outputs are accurately developed between the output pin and pin 23 (AGND), delivering these signals to remote loads can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD394, AD395 packages are used. Figure 8 illustrates the parasitic impedances which influence output accuracy.

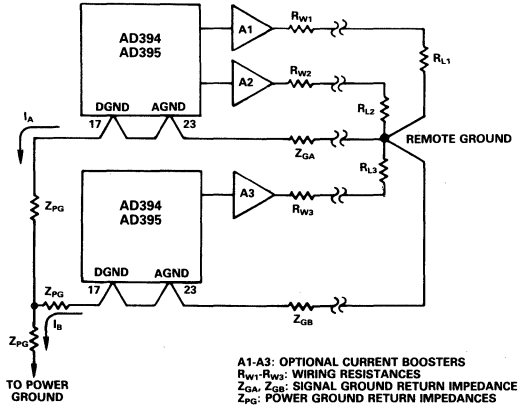


Figure 8. Grounding Errors in Multiple-AD394, AD395 Systems

An output buffer configured as a subtractor as shown in Figure 9 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances is eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote ground directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

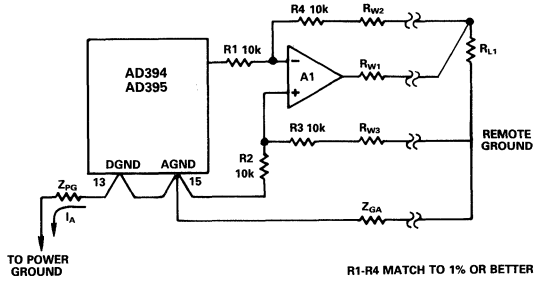


Figure 9. Use of Subtractor Amplifier to Preserve Accuracy

OPERATION FROM ±12 VOLT SUPPLIES

The AD394, AD395 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4V swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 4 millivolts per LSB).

Figure 10 shows a suggested circuit to set up a ±8.192V output range. To help prevent poor gain drift due to possible mismatch between R_{IN} and $R_{THEVENIN}$ of divider network it is recommended to buffer the potentiometer wiper voltage with an OP-07.

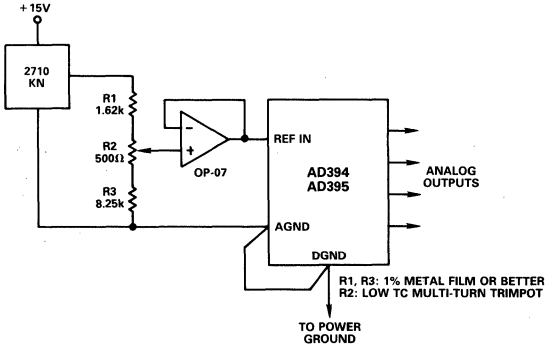


Figure 10. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

POWER SUPPLY DECOUPLING

The power supplies used with the AD394, AD395 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD394 supply pins and the AGND pin. If an output booster is used, its supplies should also be decoupled to the load ground.

IMPROVING FULL-SCALE STABILITY

In large systems using multiple DACs, it may be desirable for all devices to share a common reference. A precision reference can greatly improve system accuracy and temperature stability.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ±1ppm/°C. The combination of the AD2710LN and AD394, AD395 shown in Figure 11 will yield a multiple-DAC system with maximum full-scale drift of ±6ppm/°C and excellent tracking.

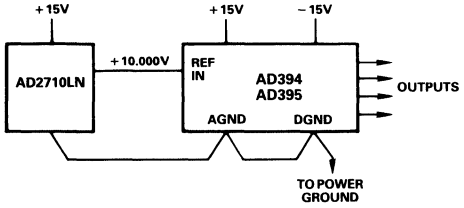


Figure 11. Low Drift AD394, AD395 Configuration

Applications

INTERFACING THE AD394, AD395 TO MICROPROCESSORS

The AD394, AD395 control logic provides simple interface to microprocessors. The individual latches allow for multi-DAC interfacing to a single data bus.

16-BIT PROCESSORS

The AD394, AD395 are 12-bit resolution DAC systems and are easily interfaced to 16-bit wide data buses. Several possible addressing configurations exist.

In the circuit of Figure 12, a system write signal is used to control the decoded address lines and a 74LS139 decoder driven from the least significant address bits provides the active-low $\overline{CS1}$ through $\overline{CS4}$ signals. In the circuit of Figure 12, address lines A0 and A1 each select a single DAC of the four contained in the AD394 or AD395. The use of a separate address line for each DAC allows several DACs to be accessed simultaneously. The address lines are gated by the simultaneous occurrence of a system $\overline{WR}$ and the appropriately decoded base address.

In the addressing scheme shown, A0 represents the least significant word address bit. Data may reside in either the 12MSBs (left-justified) or the 12LSBs (right-justified). Left justification is useful when the data word represents a binary fraction of full scale, while right-justified data usually represents an integer value between 0 and 4095.

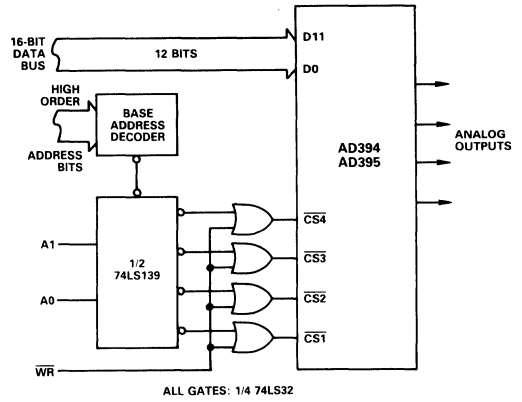
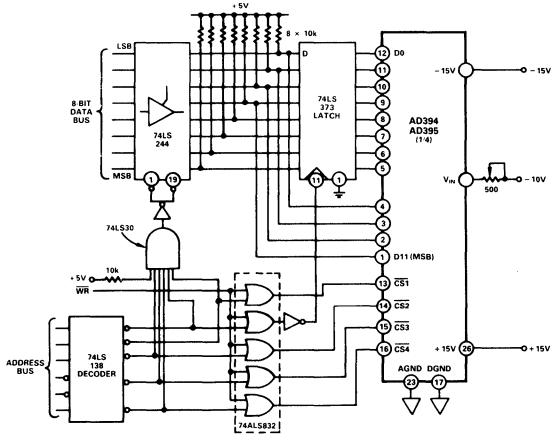


Figure 12. AD394, AD395 16-Bit Bus Interface

8-BIT PROCESSORS

The circuit of Figure 13 shows the general principles for connecting the AD394 or the AD395 to an 8-bit data bus. The 74LS244 buffers the data bus; its outputs are enabled when the DAC address appears on the address bus. The first byte sent to the DAC is loaded to the 74LS373 octal latch and, when the second byte is sent to the DAC, it is combined with the first byte to create a 12-bit word. The connections shown are for right-hand justified data. $\overline{CS}$ and $\overline{WR}$ inputs to the DAC are also gated, and when active, the DAC is loaded. Pull-up resistors at the output of the 74LS244 buffer ensure that the inputs to the DAC do not float at an ill-defined level when the DAC is not being addressed. This method of connecting 12-bit DACs to an 8-bit data bus is most cost effective when multiple DACs are utilized for 8-bit data bus applications.



NOTE:
UNUSED HEX INVERTER INPUTS SHOULD BE TIED LOW. ALL OTHER GATE INPUTS SHOWN SHOULD BE TIED HIGH TO +5V THROUGH A 10kΩ RESISTOR.

Figure 13. AD394, AD395 8-Bit Data Bus Interface

Applications

The functional density of the AD394 and AD395 permits complex analog functions to be produced under digital control, where board space requirements would otherwise be prohibitive. Multiple-output plotters, multi-channel displays and complex waveform generation and multiple programmable voltage sources can all be implemented with the AD394 or AD395 in a fraction of the space which would be needed if separate DACs were used.

USING THE AD394 FOR ANALOG-TO-DIGITAL CONVERSION

Many systems require both analog output and analog input capability. While complete integrated circuit analog-to-digital converters (such as the AD574A) are readily available, the AD394 can be used as the precision analog section of an ADC if some external logic is available. Several types of analog-to-digital converters can be built with a DAC, comparator, and control logic, including staircase, tracking, and successive-approximation types. In systems which include a microprocessor, only a comparator must be added to the AD394 to accomplish the ADC function since the processor can perform the required digital operations under software control. A suitable circuit is shown in Figure 14. The AD311 comparator compares the unknown input voltage to one of the AD394 outputs for the analog-to-digital conversion, while the other three outputs are used as normal DACs. The diode clamp shown limits the voltage swing at the

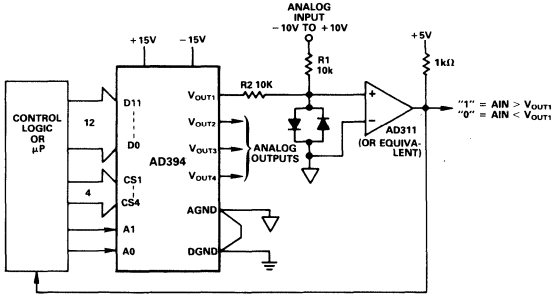


Figure 14. Using One AD394 Output for A/D Conversion

comparator input and improves conversion speed. With careful layout, a new comparison can be performed in less than 15 microseconds, resulting in 12-bit successive approximation conversion in under 180 microseconds. The benefit of the AD394 in this application is that one ADC and three DACs can be implemented with only two IC packages (the AD394 and the comparator).

PROGRAMMABLE WINDOW COMPARATOR

The AD395 can be used to perform limit testing of responses to digitally-controlled input signals. For example, two DACs may be used to generate software-controlled test conditions for a component or circuit. The response to these input conditions can either be completely converted from analog to digital or simply tested against high and low limits generated by the two remaining DACs in the AD395.

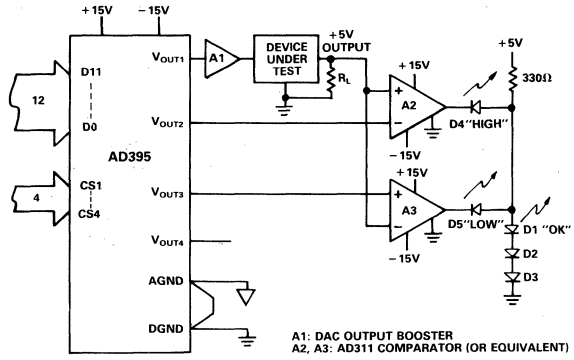


Figure 15. Programmable Window Comparator Used in Power-Supply Testing

In the circuit of Figure 15, two AD311 voltage comparators are used within AD395 to test the output of a 5 volt power-supply regulator. The AD395 V_{OUT1} output (through an appropriate current booster) drives the input to the regulator to simulate variations in input voltage. The output of the regulator is applied to comparators 1 and 2, with their outputs wire-ORed with LED indicators as shown. The test limits for each comparator are programmed by the AD395 V_{OUT2} and V_{OUT3} outputs. When the output of the device under test is within the limits, both comparators are off and D1 lights. If the output is above or below the limits, either D4 or D5 lights.

AD395 AS A MULTIPLIER AND ATTENUATOR

So far, it has been assumed that the reference voltage V_{REFIN} is fixed. In fact, V_{REFIN} can be any voltage within the range ($-11V < V_{REFIN} < +11V$). It can be negative, positive, sinusoidal or whatever the user prefers. This leads to the name "Multiplying D/A Converters" because the output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the V_{REFIN} terminal.

$$V_{OUT} = -1 \cdot (V_{REFIN}) \cdot \frac{D}{(4096)} \qquad (0<D<4095)$$

D is the fractional binary value of the digital word applied to the converter. The AD395 multiplies the digital input value by the analog input voltage at V_{REFIN} for any value of V_{REFIN} up to 22V p-p. This in itself is a powerful tool. Any applications requiring precision multiplication with minimal zero offset and very low distortion should consider the AD395 as a candidate. One popular use for AD395 is as a audio frequency attenuator. The audio signal is applied to the V_{REFIN} input and the attenuation code is applied to the DAC; the output voltage is the product of the two – an attenuated version of the input. The maximum attenuation range obtainable utilizing 12-bits is 4096:1 or 72db.

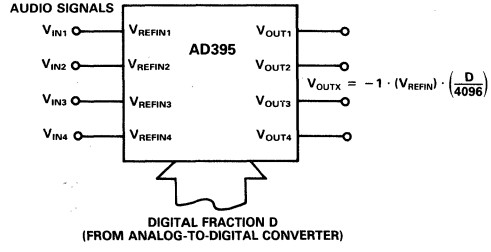


Figure 16. AD395 as a Multiplier or Attenuator

ANALOG DEVICES

μP-Compatible Multiplying Quad 14-Bit D/A Converter

AD396

FEATURES

Four, Pre-Trimmed, 14-Bit CMOS DACs
Double Buffered for Simultaneous Update
Precision Output Amplifiers for Voltage Out
Full Four Quadrant Multiplication – Independently Pinned Out DAC Reference
Monotonicity Guaranteed Over Full MIL Temp. Range
Low Power – 780mW Max
Small 28 Lead, Hermetic Double DIP Package
MIL-STD-883 Processing Available

PRODUCT DESCRIPTION

The AD396 is a high-speed microprocessor compatible Quad 14-bit digital-to-analog converter. The AD396 contains four 14-bit, low power multiplying digital-to-analog converters followed by precision voltage output amplifiers all in a compact 28-pin hybrid package. The design is based on a proprietary latched 14-bit CMOS DAC chip which reduces chip count and provides high reliability.

The AD396 (K, T) is laser-trimmed to ±1LSB max differential and integral linearity, and to full-scale accuracy of ±0.05 percent at 25°C. The high initial accuracy is made possible by the use of precision laser trimmed thin-film scaling resistors.

The individual DAC registers are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control pins. These control signals allow any combination of the DAC select matrix to occur (see Table III). Once selected, the DAC is loaded with right-justified data in two bytes from an 8-bit data bus. Standard Chip Select and Memory Write logic is used to access the DACs. Address lines A0, and A1, control internal register loading and transfer.

The AD396 outputs (V_{REF} = +10V) provide a ±10V bipolar output range with positive-true offset binary input coding.

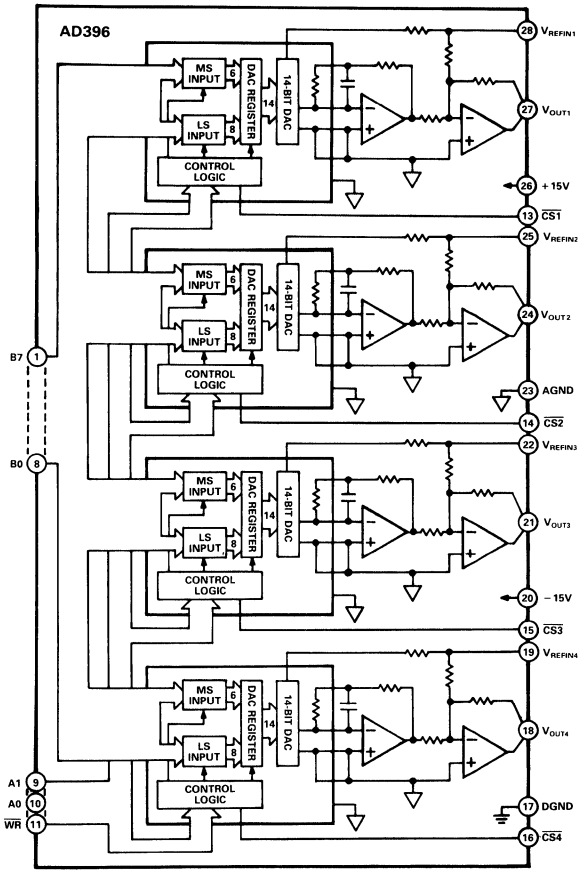
The AD396 is packaged in a 28-lead ceramic DIP package and is available for operation over the 0 to +70°C and −55°C to +125°C temperature range.

The AD396 is for systems requiring digital control of many analog voltages where board space is at a premium and low power consumption a necessity. Such applications include automatic test equipment, process controllers, and vector stroke displays.

PRODUCT HIGHLIGHTS

1. The AD396 offers a dramatic reduction in printed circuit board space in systems using multiple DACs.
2. The use of CMOS DACs provides low power consumption.
3. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
4. The output voltage is trimmed to a full-scale accuracy of ±0.05%. Settling time to ±1/2LSB is 15 microseconds maximum.
5. Maximum gain TC of 5ppm/°C is achievable by the AD396.

AD396 FUNCTIONAL BLOCK DIAGRAM



6. The monolithic CMOS DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
7. The 28-pin double-width hybrid package provides extremely high functional density.
8. Four quadrant multiplication can be achieved simply by applying the appropriate input voltage signal to the selected DACs reference (V_{REFIN}).
9. The AD396S, T features guaranteed accuracy and linearity over the −55°C to +125°C temperature range.
10. MIL-STD-883 processing is available. See Analog Devices Military Data Sheet for further information.
11. Protection against power supply surges is included within the AD396.

SPECIFICATIONS (T_A = +25°C, V_{REFIN} = 10V, V_S = ±15V unless otherwise specified)

Model	AD396JD/SD[1]			AD396KD/TD[1]			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS (Pins 1-16)[2]							
TTL or 5 Volt CMOS Compatible							
Input Voltage							
Bit ON (Logic "1")	+2.4		+5.5	+2.4		+5.5	V
Bit OFF (Logic "0")	0		+0.8	0		+0.8	V
Input Current		±4	±40		±4	±40	μA
RESOLUTION			14			14	Bits
OUTPUT							
Voltage Range[3]		$\pm V_{REFIN}$			$\pm V_{REFIN}$		V
Current	5			5			mA
STATIC ACCURACY							
Gain Error		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Bipolar Zero		±0.025			±0.012		% of FSR
Integral Linearity Error[5]		±1	±2		±1/2	±1	LSB
Differential Linearity Error		±1/2	±1		±1/2	±1	LSB
TEMPERATURE PERFORMANCE							
Gain Drift			±10			±5	ppm FSR/°C
Offset Drift			±10			±5	ppm FSR/°C
Integral Linearity Error[5]							
0 to +70°C		±1	±2		±1/2	±1	LSB
−55°C to +125°C		±2	±4		±1	±2	LSB
Differential Linearity Error	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE INPUTS							
Input Resistance	5		25	5		25	kΩ
Voltage Range	−11		+11	−11		+11	V
DYNAMIC PERFORMANCE							
Settling Time (to ±1/2LSB)							
V_{REFIN} = +10V, Change All Digital							
Inputs from +5.0V to 0V		10	15		10	15	μs
V_{REFIN} = 0 to 5V Step,							
All Digital Inputs = 0V		10	15		10	15	μs
Reference Feedthrough Error[6]		5			5		mV p-p
Digital-to-Analog Glitch Impulse[7]		250			250		nV·sec
Crosstalk							
Digital Input (Static)[8]		1/2			1/2		LSB
Reference[9]		4.0			4.0		mV p-p
POWER REQUIREMENTS							
Supply Voltage[10]	±13.5		±16.5	±13.5		±16.5	V
Current (All Digital Inputs 0V or +5V)							
$+V_S$		20	22		20	22	mA
$-V_S$		18	28		18	28	mA
Power Dissipation		570	780		570	780	mW
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES
[1]AD396S and T grades are available to MIL-STD-883, Method 5008, Class B.
[2]Timing specifications appear in Table IV and Figure 3.
[3]Code tables and graphs appear on Theory of Operation page.
[4]FSR means Full Scale Range and is equal to 20V for a ±10V bipolar range.
[5]Integral nonlinearity is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function.
[6]For AD396 (bipolar), DAC register loaded with 00 0000 0000 0000, V_{REFIN} = 20V p-p, 60 and 400Hz.
[7]This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVs and is measured with V_{REFIN} = AGND.
[8]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2kΩ load by means of varying the digital input code.
[9]Reference crosstalk is defined as the change in any one output as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} @10kHz into a 2kΩ load by means of varying the amplitude of the reference signal.
[10]The AD396 can be used with supply voltages as low as ±11.4V, Figure 7.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to DGND . . . . . −0.3V to +17V
$-V_S$ to DGND . . . . . +0.3V to −17V
Digital Inputs (Pins 1-16) to DGND . . . . . −0.3V to +7V
V_{REFIN} to DGND . . . . . ±25V
AGND to DGND . . . . . +0.3V to $+V_S$
Analog Outputs (Pins 18, 21, 24, 27)
. . . . . Indefinite Short to AGND or DGND
Momentary Short to $\pm V_S$

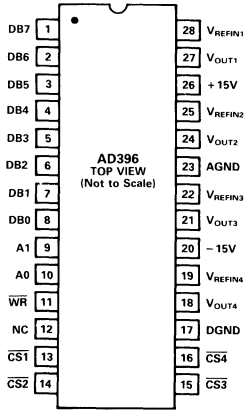
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



PIN	FUNCTION	DESCRIPTION
1	DB7	DATA BIT 7
2	DB6	DATA BIT 6
3	DB5	DATA BIT 5/DATA BIT 13 (DAC MSB)
4	DB4	DATA BIT 5/DATA BIT 12
5	DB3	DATA BIT 3/DATA BIT 11
6	DB2	DATA BIT 2/DATA BIT 10
7	DB1	DATA BIT 1/DATA BIT 9
8	DB0	DATA BIT 0/DATA BIT 8
9	A1	ADDRESS LINE 0
10	A0	ADDRESS LINE 1
11	$\overline{WR}$	WRITE INPUT. ACTIVE LOW
12	NC	NO CONNECTION
13	$\overline{CS1}$	CHIP SELECT DAC 1. ACTIVE LOW
14	$\overline{CS2}$	CHIP SELECT DAC 2. ACTIVE LOW
15	$\overline{CS3}$	CHIP SELECT DAC 3. ACTIVE LOW
16	$\overline{CS4}$	CHIP SELECT DAC 4. ACTIVE LOW
17	DGND	DIGITAL GROUND
18	V_{OUT4}	DAC 4 VOLTAGE OUTPUT
19	V_{REFIN4}	DAC 4 REFERENCE INPUT
20	−15V	−15V SUPPLY INPUT
21	V_{OUT3}	DAC 3 VOLTAGE OUTPUT
22	V_{REFIN3}	DAC 3 REFERENCE INPUT
23	AGND	ANALOG GROUND
24	V_{OUT2}	DAC 2 VOLTAGE OUTPUT
25	V_{REFIN2}	DAC 2 REFERENCE INPUT
26	+15V	+15V SUPPLY INPUT
27	V_{OUT1}	DAC 1 VOLTAGE OUTPUT
28	V_{REFIN1}	DAC 1 REFERENCE INPUT

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD396 with the inherent reliability of intergrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protect the chips from hazardous environments. To further insure reliabilty, the AD396S,T/883B are fully compliant to MIL-STD-883 Class B, Method 5008. See Analog Devices Military Data Sheet for further information.

ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}	Package Option*
AD396JD	0 to +70°C	±16LSB	±2LSB	DH-28A
AD396KD	0 to +70°C	± 8LSB	±1LSB	DH-28A
AD396SD	−55°C to +125°C	±16LSB	±2LSB	DH-28A
AD396TD	−55°C to +125°C	± 8LSB	±1LSB	DH-28A

*See Section 14 for package outline information.

Theory of Operation

The AD396 quad DAC provides four-quadrant multiplication. It is a hybrid comprised of four monolithic 14-bit CMOS multiplying DACs and eight precision output amplifiers. Each of the four independent-buffered channels has an independent reference input capable of accepting a separate dc or ac signal for multiplying or for function generation applications. The CMOS DACs act as digitally programmable attenuators when used with a varying input signal or, if used with a fixed dc reference, the DAC would act as a standard bipolar output DAC. In addition, each DAC has data latches to buffer the converter when connected to a microprocessor data bus.

MULTIPLYING MODE

Figure 1 shows the transfer function for the AD396. The diagram indicates an area over which many different combinations of the reference input and digital input can result in a particular analog output voltage. The highlighted transfer line in the diagram indicates the transfer function for a fixed reference at the input. The digital codes above the diagram indicates the mid and endpoints of the function. The relationship between the reference input (V_{REFIN}), the digital input code, and the analog output is given in Table I below. Note that the reference input signal sets the slope of the transfer function (and determines the full-scale output at code 111..111) while the digital input selects the horizontal position in each diagram.

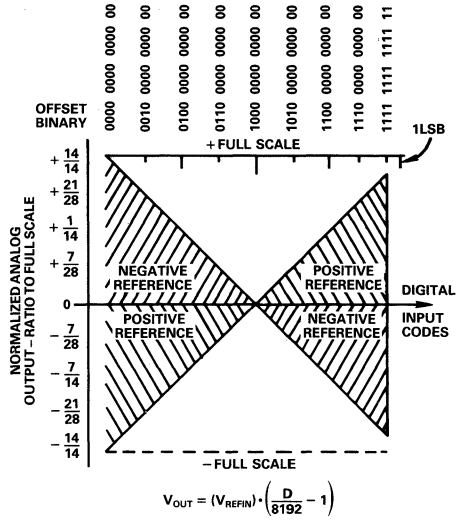


Figure 1. AD396 as a Four-Quadrant Multiplier of Reference Input and Digital Input

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111 11	$+1 \cdot (V_{REFIN}) \left\{\frac{8191}{8192}\right\}$	+9.9988V	+FULL SCALE – 1LSB
1100	0000	0000 00	$+1 \cdot (V_{REFIN}) \left\{\frac{4096}{8192}\right\}$	+5.000V	+1/2 SCALE
1000	0000	0000 01	$+1 \cdot (V_{REFIN}) \left\{\frac{1}{8192}\right\}$	+1.22mV	+1LSB
1000	0000	0000 00	$+1 \cdot (V_{REFIN}) \left\{\frac{0}{8192}\right\}$	+0.000V	ZERO
0111	1111	1111 11	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{8192}\right\}$	–1.22mV	–1LSB
0100	0000	0000 00	$-1 \cdot (V_{REFIN}) \left\{\frac{4096}{8192}\right\}$	–5.000V	–1/2 SCALE
0000	0000	0000 00	$-1 \cdot (V_{REFIN}) \left\{\frac{8192}{8192}\right\}$	–10.000V	–FULL SCALE

Table I. AD396 Bipolar Code Table

DATA AND CONTROL SIGNAL FORMAT

The AD396 accepts 14-bit data by loading two separate input registers off an 8-bit data bus, and then loading the internal DAC register. The LS (least significant) register is loaded with the bottom 8-bits of the 14-bit word by selecting the appropriate address lines (see Table II). The MS (most significant) register is loaded with the top 6-bits in a similar manner. The $\overline{CS}$ and $\overline{WR}$ line must also be asserted to load the registers. The internal DAC register can then be loaded with the 14-bit data word. The appropriate DAC or DACs are selected by asserting $\overline{CS1}$-$\overline{CS4}$ (see Table III). If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincidentally, all four DAC outputs will be updated to the value located in the DAC register. When $A_1 = 0$ and $A_0 = 0$ all DAC registers are transparent so by placing all 0s or 1s on the data inputs the user can load the DACs to zero or full scale in one write operation. This provides simple system calibration.

$\overline{WR}$	$\overline{CS}$	A1	A0	Function
X	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers.

Table II. Truth Table

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Register
1	0	1	1	Load DAC 2 From Data Register
1	1	0	1	Load DAC 3 From Data Register
1	1	1	0	Load DAC 4 From Data Register
0	0	0	0	All DACs Simultaneously Loaded

Table III. DAC Select Matrix

TIMING

The AD396 timing is shown in Figure 3, and has a few restrictions as stated in Table IV. $\overline{WR}$ must maintain a minimum pulse width of 240ns for desired operation to occur. When loading data in from the data bus, data must be stable for at least 180ns before returning $\overline{WR}$ to a high state. The Data must be held constant for at least 30ns after $\overline{WR}$ goes high to assure latching of valid data. DAC settling time is measured from the falling edge of the $\overline{WR}$ command.

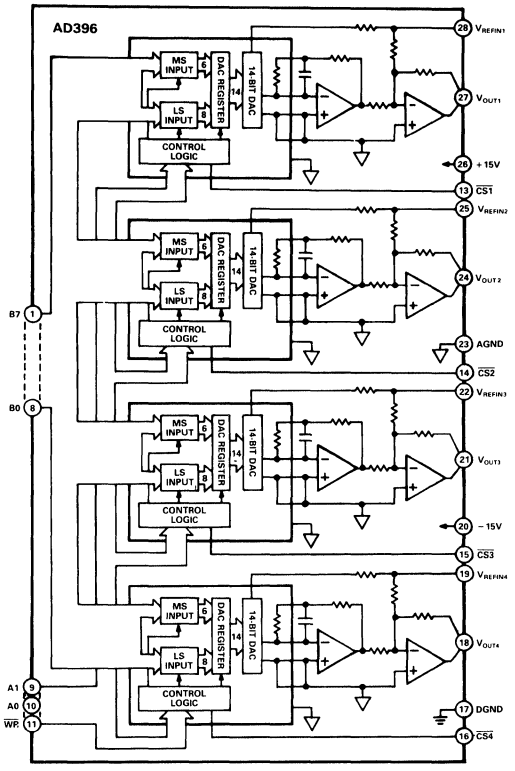
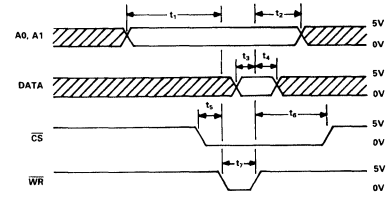


Figure 2. AD396 Block Diagram



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 3. AD396 Timing Diagram

($V_{CC} = +15V$, $V_{EE} = -15V$, $V_{REF} = +10V$)

Parameter	Limit at $T_A = 25°C$	Limit at $T_A = 0$ to $+70°C$ $T_A = -25°C$ to $+85°C$	Limit at $T_A = -55°C$ to $+125°C$	Units	Test Conditions/Comments
t_1	0	0	0	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	140	70	180	ns min	Data Setup Time
t_4	20	20	30	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select to Write Setup Time
t_6	0	0	0	ns min	Chip Select to Write Hold Time
t_7	170	200	240	ns min	Write Pulse Width

Table IV. Timing Characteristics

GROUNDING RULES

The AD396 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (Pin 17) and AGND (Pin 23). The DGND pin is the return for the supply currents of the AD396 and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the circuitry which drives the digital inputs.

Pin 23, AGND, is the high-quality analog ground connection. This pin should serve as the reference point for all analog circuitry associated with the AD396. It is recommended that any analog signal path carrying significant currents have its own return connection to Pin 23 as shown in Figure 4.

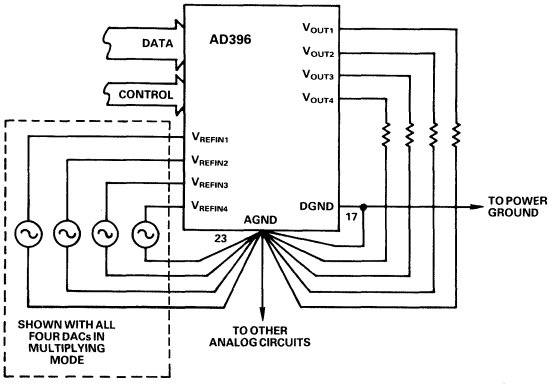


Figure 4. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the DAC outputs are accurately developed between the output pin and Pin 23 (AGND), delivering these signals to remote loads can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD396 packages are used. Figure 5 illustrates the parasitic impedances which influence output accuracy.

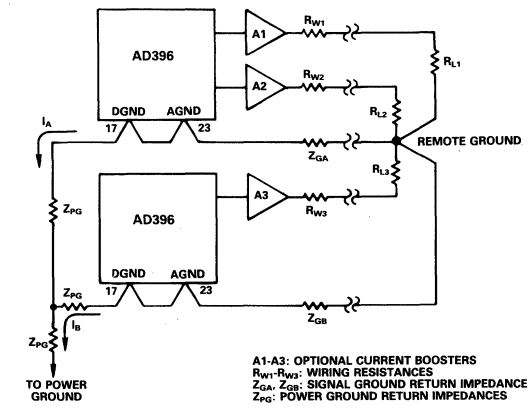


Figure 5. Grounding Errors in Multiple-AD396 Systems

An ouput buffer configured as a subtractor as shown in Figure 6 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances is eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote gound directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

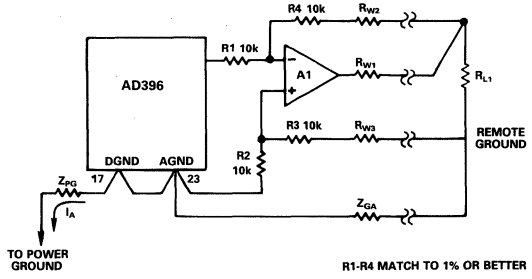


Figure 6. Use of Subtractor Amplifier to Preserve Accuracy

OPERATION FROM ±12V SUPPLIES

The AD396 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4 swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 1 millivolt per LSB).

Figure 7 shows a suggested circuit to set up a ±8.192V output range. To help prevent poor gain drift due to possible mismatch between R_{IN} and $R_{THEVENIN}$ of the divider network it is recommended to buffer the potentiometer wiper voltage with an OP-07.

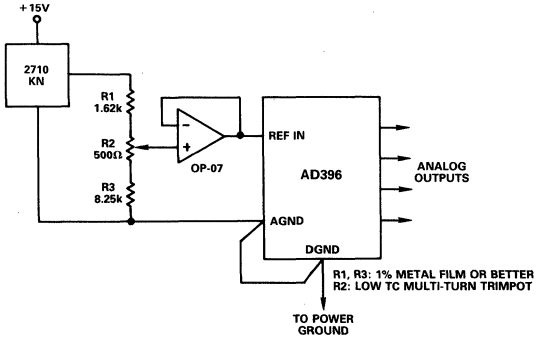


Figure 7. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

POWER SUPPLY DECOUPLING

The power supplies used with the AD396 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD396 supply pins and the AGND pin. If an output booster is used, its supplies should also be decoupled to the load ground.

IMPROVING FULL-SCALE STABILITY

In large systems using multiple DACs, it may be desirable for all devices to share a common reference. A precision reference can greatly improve system accuracy and temperature stability.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ± 1ppm/°C. The combination of the AD2710LN and AD396 shown in Figure 8 will yield a multiple-DAC system with maximum full-scale drift of ± 6ppm/°C and excellent tracking.

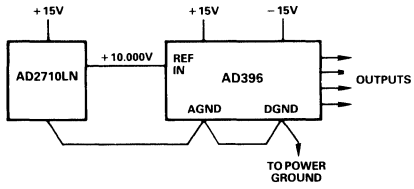


Figure 8. Low Drift AD396 Configuration

Applications

USING THE AD396 IN AUTOMATIC TEST EQUIPMENT

Most Automatic Test Equipment requires multiple accurate analog voltage thresholds which must be under microprocessor control. The AD396 is useful in such an application where space is at a premium and accuracy is essential.

The circuit in Figure 9 demonstrates how the AD396 is used to set up four different voltage thresholds (1 threshold per DAC).

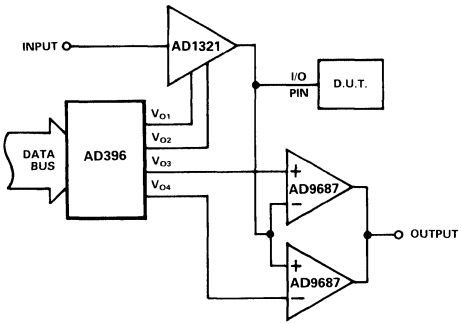


Figure 9. AD396 in ATE Systems

A fixed reference is used for the V_{REFIN} input of each of the multiplying DACs. The digital code corresponding to the desired voltage output is put on the bus, and the $\overline{\text{CHIP SELECT}}$ for the proper DAC is asserted. Two of the four DACs are used to set logic thresholds on the AD345 pindriver. The AD345 pindriver will then accurately test the logic thresholds on an I/O pin of the DUT (Device Under Test). The pindriver tests the pin by driving the pin to the proper logic thresholds set by the DACs. The response from the I/O pin will then enter the AD9687 dual comparator. The other two DACs are used to set the voltage threshold for either a Logic HI (2.2V-5.0V) or a Logic LO (0V-0.8V). This is done by placing the upper voltage limit on the positive terminal of the higher comparator, and the lower voltage limit on the negative terminal of the lower comparator. The response can then be accurately tested if it is either a Logic HI or LO by looking if the output value of the pin falls within the designated window.

THE AD396 IN SYNCHRO-TO-DIGITAL CONVERTERS

The AD396 is useful in navigation systems where a Synchro-to-Digital Converter is needed. The Synchro-to-Digital Converter is used to measure angular position and is needed to measure pitch in the x-y-z axes and roll in the x-y-z axes. An S-D converter has three inputs and two converters are needed for this application. Each S-D converter uses two multiplying DACs and the accuracy of the S-D converter depends on the accuracy of the multiplying DAC.

The outputs of the transformer are Vsinwt(sinθ) and Vsinwt(cosθ). These two outputs are applied to the V_{REF} inputs of the DACs whose digital input words are proportional to the sine and cosine of angle θ as shown in Figure 10. The output of the cosine multiplier is given by Vsinwt(sinθ)(cosϕ), and the output of the sine multiplier is given by Vsinwt(cosθ)(sinϕ). These signals are subtracted by the error amplifier to give the error signal which is:

$$Vsinwt(\sin\theta\cos\phi - \cos\theta\sin\phi) = Vsinwt(\sin\theta - \phi)$$

This error signal is demodulated by the phase sensitive detector which utilizes the system reference voltage and a dc error signal proportional to sin(θ-ϕ) is produced. The dc error signal is fed back via an integrator and V.C.O. to drive the up-down counter until the error signal is nulled. The contents of the up-down counter give a binary representation of the angular position. For more information on synchro-to-digital conversion the reader is referred to Analog Devices Synchro & Resolver Conversion Handbook.

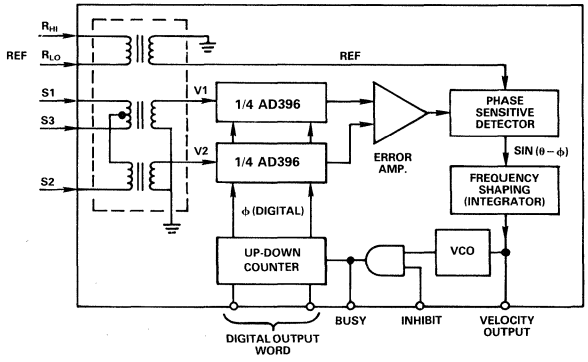


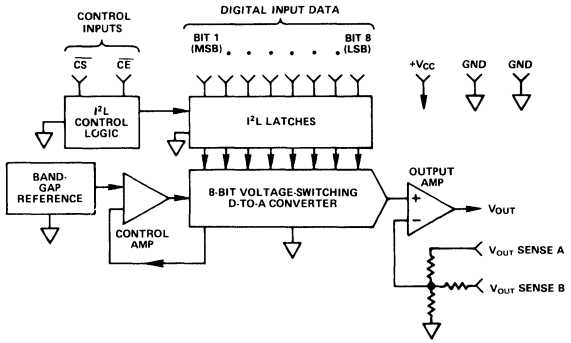
Figure 10. A Tracking Synchro-to-Digital Converter

DACPORT Low-Cost Complete µP-Compatible 8-Bit DAC

AD557

FEATURES
Complete 8-Bit DAC
Voltage Output – 0 to 2.56V
Internal Precision Band-Gap Reference
Single-Supply Operation: +5V (±10%)
Full Microprocessor Interface
Fast: 1µs Voltage Settling to ±1/2LSB
Low Power: 75mW
No User Trims Required
Guaranteed Monotonic Over Temperature
All Errors Specified T_{min} to T_{max}
Small 16-Pin DIP or 20-Pin PLCC Package
Low Cost

AD557 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD557 DACPORT™ is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The low cost and versatility of the AD557 DACPORT are the result of continued development in monolithic bipolar technologies.

The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while laser-wafer trimming of these thin-film resistors permits absolute calibration at the factory to within ±2.5LSB; thus, no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD557 is available in two package configurations. The AD557JN is packaged in a 16-pin plastic, 0.3"-wide DIP. For surface mount applications, the AD557JP is packaged in a 20-pin JEDEC standard PLCC. Both versions are specified over the operating temperature range of 0 to +70°C.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD557 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The AD557 is designed and specified to operate from a single +4.5V to +5.5V power supply.
5. Low digital input currents, 100µA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible.
6. The single-chip, low power I^2L design of the AD557 is inherently more reliable than hybrid multichip or conventional single-chip bipolar designs.

SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +5V unless otherwise specified)

Model	AD557J Min	Typ	Max	Units
RESOLUTION			8	Bits
RELATIVE ACCURACY[1]				
0 to +70°C		±1/2	1	LSB
OUTPUT				
Ranges		0 to +2.56		V
Current Source	+5			mA
Sink		Internal Passive Pull-Down to Ground[2]		
OUTPUT SETTLING TIME[3]		0.8	1.5	µs
FULL SCALE ACCURACY[4]				
@25°C		±1.5	±2.5	LSB
T_{min} to T_{max}		±2.5	±4.0	LSB
ZERO ERROR				
@25°C			±1	LSB
T_{min} to T_{max}			±3	LSB
MONOTONICITY[5]				
T_{min} to T_{max}		**Guaranteed**		
DIGITAL INPUTS				
T_{min} to T_{max}				
Input Current			**±100**	µA
Data Inputs, Voltage				
Bit On – Logic "1"	2.0			V
Bit On – Logic "0"	0		0.8	V
Control Inputs, Voltage				
On – Logic "1"	2.0			V
On – Logic "0"	0		0.8	V
Input Capacitance		4		pF
TIMING[6]				
t_W Strobe Pulse Width	225			ns
T_{min} to T_{max}	**300**			ns
t_{DH} Data Hold Time	10			ns
T_{min} to T_{max}	**10**			ns
t_{DS} Data Setup Time	225			ns
T_{min} to T_{max}	**300**			ns
POWER SUPPLY				
Operating Voltage Range (V_{CC})				
2.56 Volt Range	+4.5		+5.5	V
Current (I_{CC})		15	**25**	mA
Rejection Ratio			**0.03**	%/%
POWER DISSIPATION, V_{CC} = 5V		75	125	mW
OPERATING TEMPERATURE RANGE	0		+70	°C

NOTES

[1]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See "Measuring Offset Error" on AD558 data sheet.

[2]Passive pull-down resistance is 2kΩ.

[3]Settling time is specified for a positive-going full-scale step to ± 1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[4]The full-scale output voltage is 2.55V and is guaranteed with a +5V supply.

[5]A monotonic converter has a maximum differential linearity error of ± 1LSB.

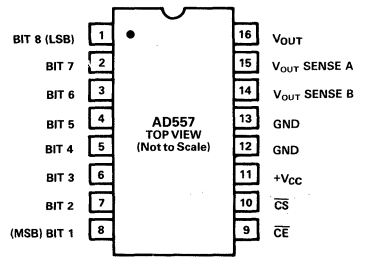
[6]See Figure 7.

Specifications shown in **boldface** are tested on all production units at final electrical test.

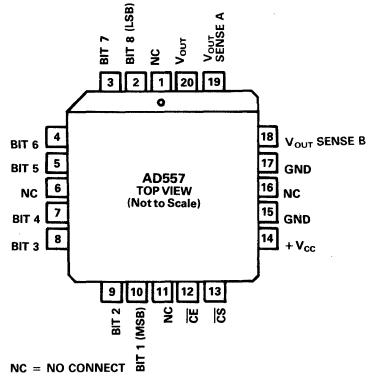
Specifications subject to change without notice.

PIN CONFIGURATIONS

DIP



PLCC



NC = NO CONNECT

AD557 ORDERING GUIDE

Model	Package Options*	Temperature
AD557JN	Plastic (N-16)	0 to +70°C
AD557JP	PLCC (P-20A)	0 to +70°C

*See Section 14 for package outline information.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground . . . . . 0V to +18V
Digital Inputs (Pins 1-10) . . . . . 0 to +7.0V
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range
N/P (Plastic) Packages . . . . . −25°C to +100°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

Thermal Resistance
Junction to Ambient/Junction to Case
N/P (Plastic) Packages . . . . . 140/55°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CIRCUIT DESCRIPTION

The AD557 consists of four major functional blocks fabricated on a single monolithic chip (see Figure 1). The main D/A converter section uses eight equally weighted laser-trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0mV to 400mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

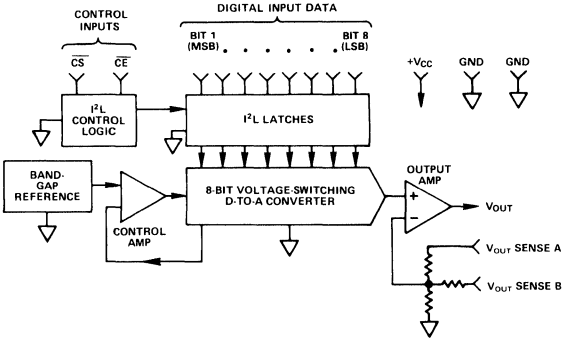


Figure 1. Functional Block Diagram

The high-speed output buffer amplifier is operated in the noninverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin film laser trimmed to match and track the DAC resistors and to assure precise initial calibration of the output range, 0V to 2.56V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply.

The internal precision voltage reference is of the patented band-gap type. This design produces a reference voltage of 1.2V and thus, unlike 6.3V temperature-compensated zeners, may be operated from a single, low-voltage logic power supply. The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low power, small geometry and high speed are advantages of the I^2L design as applied to this section. I^2L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a µP or data bus, wiring $\overline{CS}$ and $\overline{CE}$ to ground renders the latches "transparent" for direct DAC access.

Digital Input Code			Output
Binary	Hexadecimal	Decimal	Voltage
0000 0000	00	0	0
0000 0001	01	1	0.010V
0000 0010	02	2	0.020V
0000 1111	0F	15	0.150V
0001 0000	10	16	0.160V
0111 1111	7F	127	1.270V
1000 0000	80	128	1.280V
1100 0000	C0	192	1.920V
1111 1111	FF	255	2.55V

CONNECTING THE AD557

The AD557 has been configured for low cost and ease of application. All reference, output amplifier and logic connections are made internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. The only connection decision to be made by the user is whether the output range desired is unipolar or bipolar. Clean circuit board layout is facilitated by isolating all digital bit inputs on one side of the package; analog outputs are on the opposite side.

UNIPOLAR 0 TO +2.56V OUTPUT RANGE

Figure 2 shows the configuration for the 0 to +2.56V full-scale output range. Because of its precise factory calibration, the AD557 is intended to be operated without user trims for gain and offset; therefore, no provisions have been made for such user trims. If a small increase in scale is required, however, it may be accomplished by slightly altering the effective gain of the output buffer. A resistor in series with V_{OUT} SENSE will increase the output range. Note that decreasing the scale by putting a resistor in series with GND will not work properly due to the code-dependent currents in GND. Adjusting offset by injecting dc at GND is not recommended for the same reason.

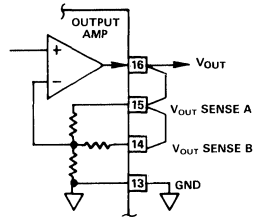


Figure 2. 0 to 2.56V Output Range

BIPOLAR −1.28V TO +1.28V OUTPUT RANGE

The AD557 was designed for operation from a single power supply and is thus capable of providing only a unipolar 0 to +2.56V output range. If a negative supply is available, bipolar output ranges may be achieved by suitable output offsetting and scaling. Figure 3 shows how a ±1.28V output range may be achieved when a −5V power supply is available. The offset is provided by the AD589 precision 1.2V reference which will operate from a +5V supply. The AD711 output amplifier can provide the necessary ±1.28V output swing from ±5V supplies. Coding is complementary offset binary.

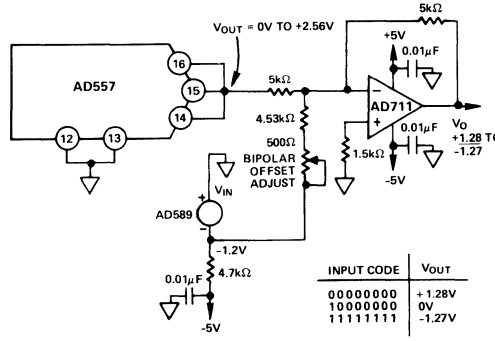


Figure 3. Bipolar Operation of AD557 from ±5V Supplies

Applications

GROUNDING AND BYPASSING

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD557 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD557 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 4 shows how the ground connections should be made.

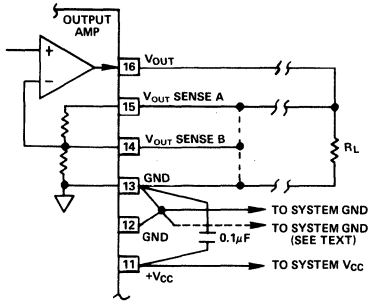


Figure 4. Recommended Grounding and Bypassing

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD557, it is recommended that common ground tie-points should be provided at *each* such device. If only one system ground can be connected directly to the AD557, it is recommended that analog common be selected.

USING A "FALSE" GROUND

Many applications, such as disk drives, require servo control voltages that swing on either side of a "false" ground. This ground is usually created by dividing the +12V supply equally and calling the midpoint voltage "ground."

Figure 5 shows an easy and inexpensive way to implement this. The AD586 is used to provide a stable 5V reference from the system's +12V supply. The op amp shown likewise operates from a single (+12V) supply available in the system. The resulting output at the V_{OUT} node is ±2.5V around the "false" ground point of 5V. AD557 input code vs. V_{OUT} is shown in Figure 6.

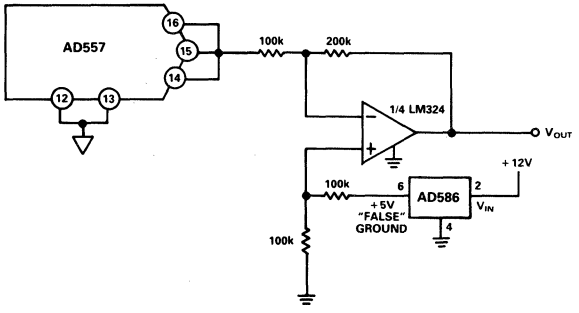


Figure 5. Level Shifting the AD557 Output Around a "False" Ground

TIMING AND CONTROL

The AD557 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) inputs. $\overline{CE}$ and $\overline{CS}$ are internally "NORed" so that the latches transmit input data to the DAC section when both $\overline{CE}$ and $\overline{CS}$ are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either $\overline{CE}$ or $\overline{CS}$ go to Logic "1," the input data is latched into the registers and held until both $\overline{CE}$ and $\overline{CS}$ return to "0." (Unused $\overline{CE}$ or $\overline{CS}$ inputs should be tied to ground.) The truth table is given in Table I. The logic function is also shown in Figure 6.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	∫	0	0	latching
1	∫	0	1	latching
0	0	∫	0	latching
1	0	∫	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
∫ = Logic Threshold at Positive-Going Transition

Table I. AD557 Control Logic Truth Table

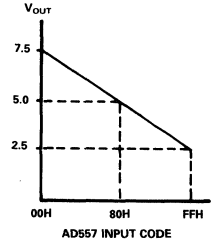


Figure 6. AD557 Input Code vs. Level Shifted Output in "False" Ground Configuration

In a level-triggered latch such as that used in the AD557, there is an interaction between the data setup and hold times and the width of the enable pulse. In an effort to reduce the time required to test all possible combinations in production, the AD557 is tested with $T_{DS} = T_W = 225ns$ at 25°C and 300ns at T_{min} and T_{max}, with $T_{DH} = 10ns$ at all temperatures. Failure to comply with these specifications may result in data not being latched properly.

Figure 7 shows the timing for the data and control signals, $\overline{CE}$ and $\overline{CS}$ are identical in timing as well as in function.

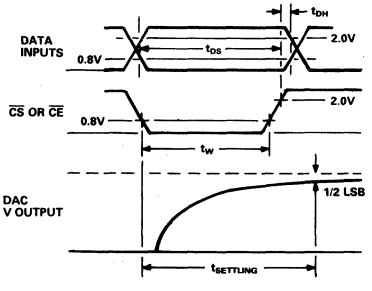


Figure 7. AD557 Timing

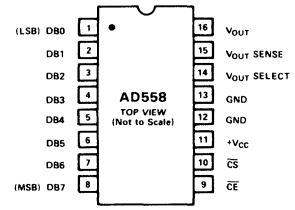
DACPORT Low-Cost Complete µP-Compatible 8-Bit DAC

AD558*

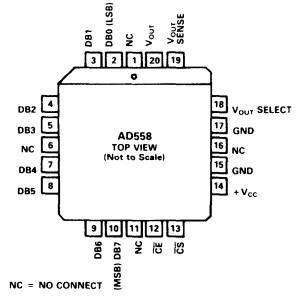
FEATURES

Complete 8-Bit DAC
Voltage Output – 2 Calibrated Ranges
Internal Precision Band-Gap Reference
Single-Supply Operation: +5V to +15V
Full Microprocessor Interface
Fast: 1µs Voltage Settling to ±1/2LSB
Low Power: 75mW
No User Trims
Guaranteed Monotonic Over Temperature
All Errors Specified T_{min} to T_{max}
Small 16-Pin DIP, 20-Pin PLCC and LCC Packages
Single Laser-Wafer-Trimmed Chip for Hybrids
Low Cost

AD558 PIN CONFIGURATION (DIP)



AD558 PIN CONFIGURATION (PLCC AND LCC)



PRODUCT DESCRIPTION

The AD558 DACPORT™ is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD558 is available in four performance grades. The AD558J and K are specified for use over the 0 to +70°C temperature range, while the AD558S and T grades are specified for -55°C to +125°C operation. The "J" and "K" grades are available either in 16-pin plastic (N) or hermetic ceramic (D) DIPS. They are also available in 20-pin JEDEC standard PLCC packages. The "S" and "T" grades are available in 16-pin hermetic ceramic DIP packages and 20-pin LCC packages.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD558 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The voltage-switching structure of the AD558 DAC section along with a high-speed output amplifier and laser-trimmed resistors give the user a choice of 0V to +2.56V or 0V to +10V output ranges, selectable by pin-strapping. Circuitry is internally compensated for minimum settling time on both ranges; typically settling to ±1/2LSB for a full-scale 2.55 volt step in 800ns.
5. The AD558 is designed and specified to operate from a single +4.5V to +16.5V power supply.
6. Low digital input currents, 100µA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible over the entire operating V_{CC} range.

(continued further)

SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +5V to +15V unless otherwise specified)

Model	AD558J			AD558K			AD558S[1]			AD558T[1]			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			8			8			8			8	Bits
RELATIVE ACCURACY[2]													
0 to +70°C			±1/2			±1/4			±1/2			±1/4	LSB
−55°C to +125°C									±3/4			±3/8	LSB
OUTPUT													
Ranges[3]		0 to +2.56			0 to +2.56			0 to +2.56			0 to +2.56		V
		0 to +10			0 to +10			0 to +10			0 to +10		V
Current Source	+5			+5			+5			+5			mA
Sink		Internal Passive Pull-Down to Ground[4]			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground		
OUTPUT SETTLING TIME[5]													
0 to 2.56 Volt Range		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	µs
0 to 10 Volt Range[4]		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	µs
FULL SCALE ACCURACY[6]													
@25°C			±1.5			±0.5			±1.5			±0.5	LSB
T_{min} to T_{max}			±2.5			±1			±2.5			±1	LSB
ZERO ERROR													
@25°C			±1			±1/2			±1			±1/2	LSB
T_{min} to T_{max}			±2			±1			±2			±1	LSB
MONOTONICITY[7]													
T_{min} to T_{max}		**Guaranteed**			**Guaranteed**			**Guaranteed**			**Guaranteed**		
DIGITAL INPUTS													
T_{min} to T_{max}													
Input Current			±100			±100			±100			100	µA
Data Inputs, Voltage													
Bit On – Logic "1"	2.0			2.0			2.0			2.0			V
Bit On – Logic "0"	0		0.8	0			0			0			V
Control Inputs, Voltage													
On – Logic "1"	2.0			2.0			2.0			2.0			V
On – Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
Input Capacitance		4			4			4			4		pF
TIMING[8]													
t_W Strobe Pulse Width	200			200			200			200			ns
T_{min} to T_{max}	**270**			**270**			**270**			**270**			ns
t_{DH} Data Hold Time	10			10			10			10			ns
T_{min} to T_{max}	**10**			**10**			**10**			**10**			ns
t_{DS} Data Set-Up Time	200			200			200			200			ns
T_{min} to T_{max}	**270**			**270**			**270**			**270**			ns
POWER SUPPLY													
Operating Voltage Range (V_{CC})													
2.56 Volt Range	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	V
10 Volt Range	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	V
Current (I_{CC})		15	25		15	25		15	25		15	25	mA
Rejection Ratio			**0.03**			**0.03**			**0.03**			**0.03**	%/%
POWER DISSIPATION, V_{CC} = 5V		75	125		75	125		75	125		75	125	mW
V_{CC} = 15V		225	375		225	375		225	375		225	375	mW
OPERATING TEMPERATURE RANGE	0		+70	0		+70	−55		+125	−55		+125	°C

NOTES

[1]The AD558 S & T grades are available processed and screened to MIL-STD-883 Class B. Consult Analog Devices' Military Databook for details.

[2]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See "Measuring Offset Error".

[3]Operation of the 0 to 10 volt output range requires a minimum supply voltage of +11.4 volts.

[4]Passive pull-down resistance is 2kΩ for 2.56 volt range, 10kΩ for 10 volt range.

[5]Settling time is specified for a positive-going full-scale step to ± 1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[6]The full range output voltage for the 2.56 range is 2.55V and is guaranteed with a +5V supply, for the 10V range, it is 9.960V guaranteed with a +15V supply.

[7]A monotonic converter has a maximum differential linearity error of ±1LSB.

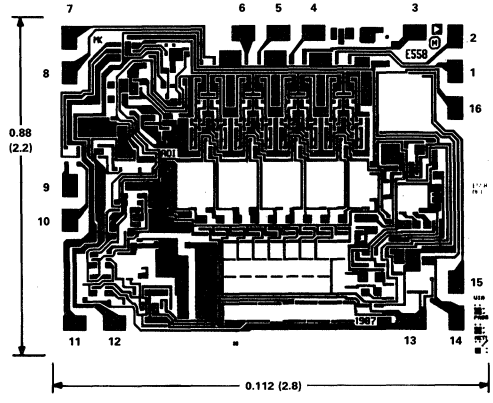
[8]See Figure 7.

Specifications shown in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

AD558 METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Ground . . . . . 0V to +18V
Digital Inputs (Pins 1-10) . . . . . 0 to +7.0V
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range
N/P (Plastic) Packages . . . . . −25°C to +100°C
D/E (Ceramic) Package . . . . . −55°C to +150°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C
Thermal Resistance
Junction to Ambient/Junction to Case
D/E (Ceramic) Package . . . . . 100/30°C/W
N/P (Plastic) Packages . . . . . 140/55°C/W

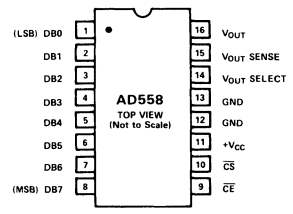


Figure 1a. AD558 Pin Configuration (DIP)

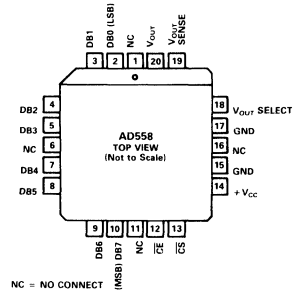


Figure 1b. AD558 Pin Configuration (PLCC and LCC)

AD558 ORDERING GUIDE

Model	Package Options*	Temperature	Relative Accuracy Error Max T_{min} to T_{max}	Full-Scale Error, Max T_{min} to T_{max}
AD558JN	Plastic (N-16)	0 to +70°C	±1/2LSB	±2.5LSB
AD558JP	PLCC (P-20A)	0 to +70°C	±1/2LSB	±2.5LSB
AD558JD	TO-116 (D-16)	0 to +70°C	±1/2LSB	±2.5LSB
AD558KN	Plastic (N-16)	0 to +70°C	±1/4LSB	±1LSB
AD558KP	PLCC (P-20A)	0 to +70°C	±1/4LSB	±1LSB
AD558KD	TO-116 (D-16)	0 to +70°C	±1/4LSB	±1LSB
AD558SD	TO-116 (D-16)	−55°C to +125°C	±3/4LSB	±2.5LSB
AD558SE	LCC (E-20)	−55°C to +125°C	±3/4LSB	±2.5LSB
AD558TD	TO-116 (D-16)	−55°C to +125°C	±3/8LSB	±1LSB
AD558TE	LCC (E-20)	−55°C to +125°C	±3/8LSB	±1LSB

*See Section 14 for package outline information.

(continued from features page)

7. The single-chip, low power I^2L design of the AD558 is inherently more reliable than hybrid multi-chip or conventional single-chip bipolar designs. The AD558S and T grades which are specified over the -55°C to +125°C temperature range, are available processed to MIL-STD-883, Class B.
8. All AD558 grades are available in chip form with guaranteed specifications from +25°C to T_{max}. MIL-STD-883, Class B visual inspection is standard on Analog Devices bipolar chips. Contact the factory for additional chip information.

CIRCUIT DESCRIPTION

The AD558 consists of four major functional blocks, fabricated on a single monolithic chip (see Figure 2). The main D to A converter section uses eight equally-weighted laser-trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0mV to 400mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

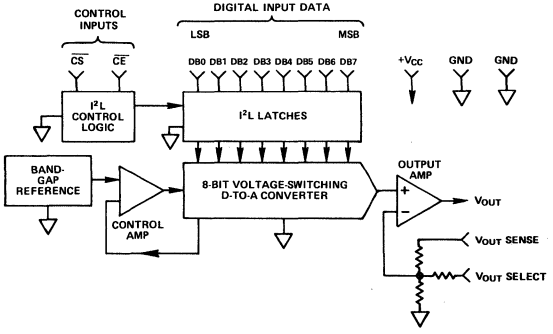


Figure 2. AD558 Functional Block Diagram

The high-speed output buffer amplifier is operated in the non-inverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin-film laser-trimmed to match and track the DAC resistors and to assure precise initial calibration of the two output ranges, 0V to 2.56V and 0V to 10V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply.

The internal precision voltage reference is of the patented band-gap type. This design produces a reference voltage of 1.2 volts and thus, unlike 6.3 volt temperature-compensated zeners, may be operated from a single, low-voltage logic power supply. The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low-power, small geometry and high-speed are advantages of the I^2L design as applied to this section. I^2L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a μP or data bus, wiring $\overline{CS}$ and $\overline{CE}$ to ground renders the latches "transparent" for direct DAC access.

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD558, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further ensure reliability, military-temperature range AD558 grades S and T are available screened to MIL-STD-883. For more complete data sheet information consult the Analog Devices' Military Databook.

CHIP AVAILABILITY

The AD558 is available in laser-trimmed, passivated chip form. AD558J and AD558T chips are available. Consult the factory for details.

Digital Input Code			Output Voltage	
Binary	**Hexadecimal**	**Decimal**	**2.56V Range**	**10.00V Range**
0000 0000	00	0	0	0
0000 0001	01	1	0.010V	0.039V
0000 0010	02	2	0.020V	0.078V
0000 1111	0F	15	0.150V	0.586V
0001 0000	10	16	0.160V	0.625V
0111 1111	7F	127	1.270V	4.961V
1000 0000	80	128	1.280V	5.000V
1100 0000	C0	192	1.920V	7.500V
1111 1111	FF	255	2.55V	9.961V

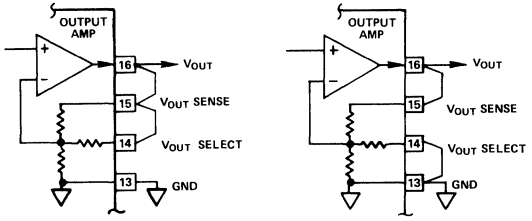
Input Logic Coding

CONNECTING THE AD558

The AD558 has been configured for ease of application. All reference, output amplifier and logic connections are made internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. The only connection decision that must be made by the user is a single jumper to select output voltage range. Clean circuit-board layout is facilitated by isolating all digital bit inputs on one side of the package; analog outputs are on the opposite side.

Figure 3 shows the two alternative output range connections. The 0V to 2.56V range may be selected for use with any power supply between +4.5V and +16.5V. The 0V to 10V range requires a power supply of +11.4V to +16.5V.

Because of its precise factory calibration, the AD558 is intended to be operated without user trims for gain and offset; therefore no provisions have been made for such user-trims. If a small increase in scale is required, however, it may be accomplished by slightly altering the effective gain of the output buffer. A resistor in series with V_{OUT} SENSE will increase the output range.



a. 0V to 2.56V Output Range *b. 0V to 10V Output Range*

Figure 3. Connection Diagrams

For example if a 0V to 10.24V output range is desired (40mV = 1LSB), a nominal resistance of 850Ω is required. It must be remembered that, although the internal resistors all ratio-match and track, the *absolute* tolerance of these resistors is typically ±20% and the *absolute* TC is typically -50ppm/°C (0 to -100ppm/°C). That must be considered when re-scaling is performed. Figure 4 shows the recommended circuitry for a full-scale output range of 10.24 volts. Internal resistance values shown are nominal.

NOTE: Decreasing the scale by putting a resistor in series with GND will not work properly due to the code-dependent currents in GND. Adjusting offset by injecting dc at GND is not recommended for the same reason.

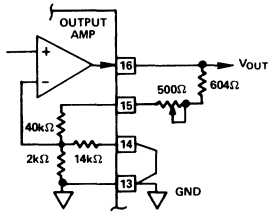


Figure 4. 10.24V Full-Scale Connection

GROUNDING AND BYPASSING*

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD558 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD558 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 5 shows how the ground connections should be made.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD558, it is recommended that common ground tie-points should be provided at *each* such device. If only one system ground can be connected directly to the AD558, it is recommended that analog common be selected.

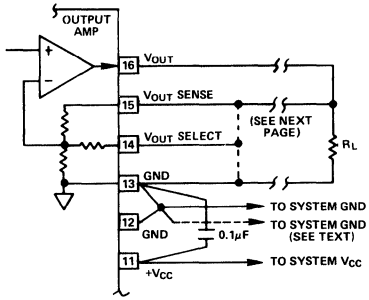


Figure 5. Recommended Grounding and Bypassing

POWER SUPPLY CONSIDERATIONS

The AD558 is designed to operate from a single positive power supply voltage. Specified performance is achieved for any supply voltage between +4.5V and +16.5V. This makes the AD558 ideal for battery-operated, portable, automotive or digital main-frame applications.

The only consideration in selecting a supply voltage is that, in order to be able to use the 0V to 10V output range, the power supply voltage must be between +11.4V and +16.5V. If, however, the 0V to 2.56V range is to be used, power consumption will be minimized by utilizing the lowest available supply voltage (above +4.5V).

TIMING AND CONTROL

The AD558 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) inputs. $\overline{CE}$ and $\overline{CS}$ are internally "NORed" so that the latches transmit input data to the DAC section when both $\overline{CE}$ and $\overline{CS}$ are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either $\overline{CE}$ or $\overline{CS}$ go to Logic "1", the input data is latched into the registers

*For additional insight, "An IC Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right For A Change", is available at no charge from any Analog Devices Sales Office.

and held until both $\overline{CE}$ and $\overline{CS}$ return to "0". (Unused $\overline{CE}$ or $\overline{CS}$ inputs should be tied to ground.) The truth table is given in Table I. The logic function is also shown in Figure 6.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	↓	0	0	latching
1	↓	0	1	latching
0	0	↓	0	latching
1	0	↓	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
↓ = Logic Threshold at Positive-Going Transition

Table I. AD558 Control Logic Truth Table

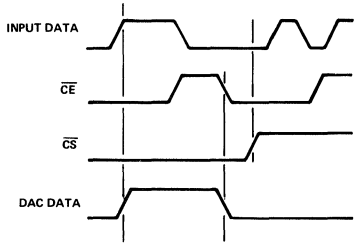


Figure 6. AD558 Control Logic Function

In a level-triggered latch such as that in the AD558 there is an interaction between data setup and hold times and the width of the enable pulse. In an effort to reduce the time required to test all possible combinations in production, the AD558 is tested with $t_{DS} = t_W = 200ns$ at 25°C and 270ns at T_{min} and T_{max}, with $t_{DH} = 10ns$ at all temperatures. Failure to comply with these specifications may result in data not being latched properly.

Figure 7 shows the timing for the data and control signals; $\overline{CE}$ and $\overline{CS}$ are identical in timing as well as in function.

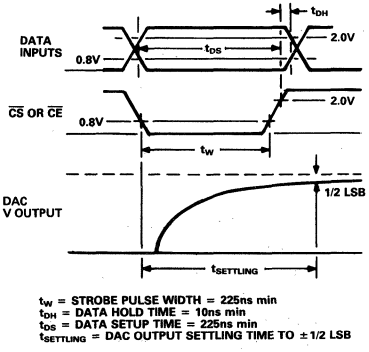
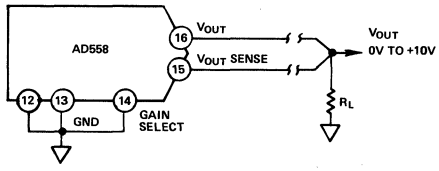


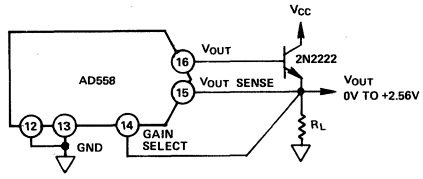
Figure 7. AD558 Timing

USE OF V_{OUT} SENSE

Separate access to the feedback resistor of the output amplifier allows additional application versatility. Figure 8a shows how I X R drops in long lines to remote loads may be cancelled by putting the drops "inside the loop." Figure 8b shows how the separate sense may be used to provide a higher output current by feeding back around a simple current booster.



a. Compensation for I x R Drops in Output Lines



b. Output Current Booster

Figure 8. Use of V_{OUT} Sense

OPTIMIZING SETTLING TIME

In order to provide single-supply operation and zero-based output voltage ranges, the AD558 output stage has a passive "pull-down" to ground. As a result, settling time for negative-going output steps may be longer than for positive-going output steps. The relative difference depends on load resistance and capacitance. If a negative power supply is available, the negative-going settling time may be improved by adding a pull-down resistor from the output to the negative supply as shown in Figure 9. The value of the resistor should be such that, at zero voltage out, current through that resistor is 0.5mA max.

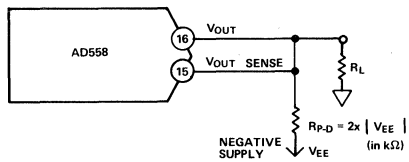


Figure 9. Improved Settling Time

BIPOLAR OUTPUT RANGES

The AD558 was designed for operation from a single power supply and is thus capable of providing only unipolar (0V to +2.56 and 0V to 10V) output ranges. If a negative supply is available, bipolar output ranges may be achieved by suitable output offsetting and scaling. Figure 10 shows how a ±1.28 volt output range may be achieved when a −5 volt power supply is available. The offset is provided by the AD589 precision 1.2 volt reference which will operate from a +5 volt supply. The AD544 output amplifier can provide the necessary ±1.28 volt output swing from ±5 volt supplies. Coding is complementary offset binary.

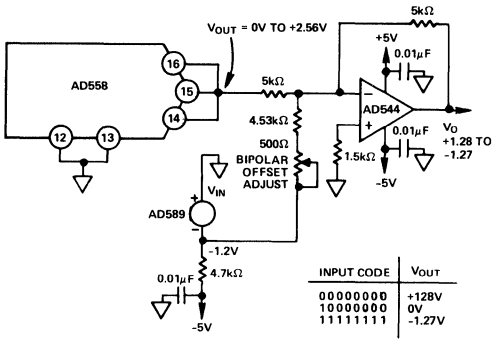


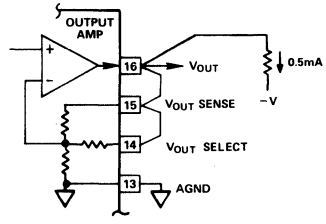
Figure 10. Bipolar Operation of AD558 from ±5V Supplies

MEASURING OFFSET ERROR

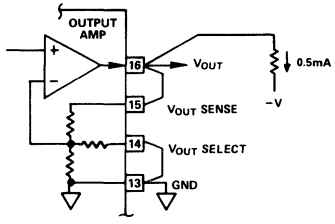
One of the most commonly specified end-point errors associated with real-world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volts. There are some DACs, like the AD558 where offset errors may be present but not observable at the zero scale, because of other circuit limitations (such as zero coinciding with single-supply ground) so that a nonzero output at zero code cannot be read as the offset error. Factors like this make testing the AD558 a little more complicated.

By adding a pulldown resistor from the output to a negative supply as shown in Figure 11, we can now read offset errors at zero code that may not have been observable due to circuit limitations. The value of the resistor should be such that, at zero voltage out, current through the resistor is 0.5mA max.



a. 0V to 2.56V Output Range

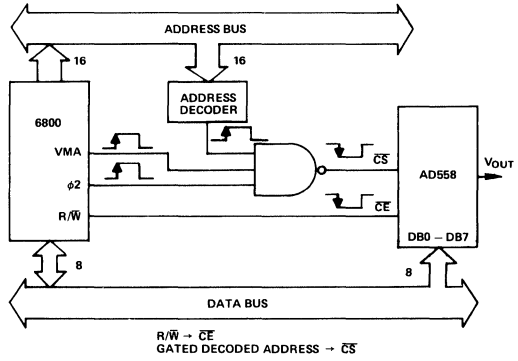


b. 0V to 10V Output Range

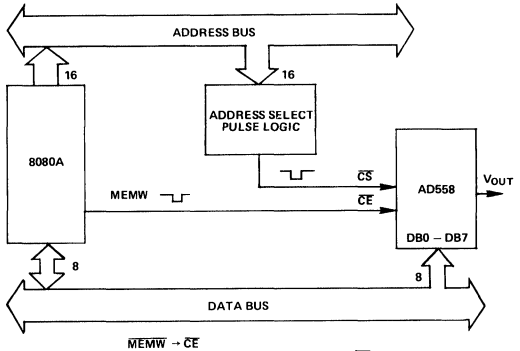
Figure 11. Offset Connection Diagrams

INTERFACING THE AD558 TO MICROPROCESSOR DATA BUSES

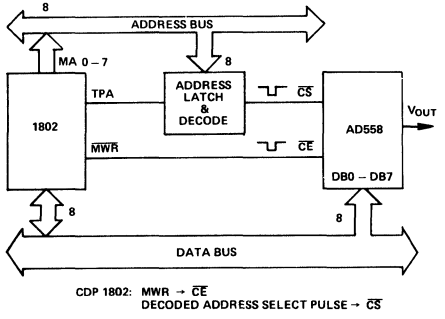
The AD558 is configured to act like a "write only" location in memory that may be made to coincide with a read only memory location or with a RAM location. The latter case allows data previously written into the DAC to be read back later via the RAM. Address decoding is partially complete for either ROM or RAM. Figure 12 shows interfaces for three popular microprocessor systems.



a. 6800/AD558 Interface



b. 8080A/AD558 Interface



c. 1802/AD558 Interface

Figure 12. Interfacing the AD558 to Microprocessors

AD558 Performance (typical @ +25°C, V_{CC} ± +5V to +15V unless otherwise noted)

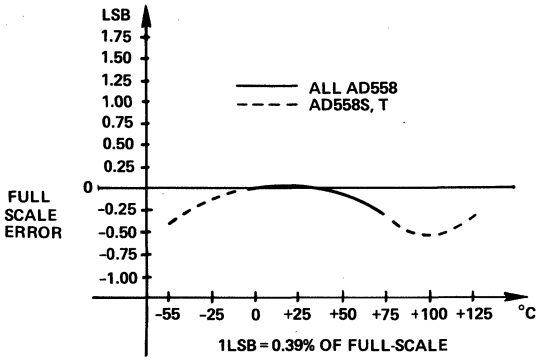


Figure 13. Full-Scale Accuracy vs. Temperature Performance of AD558

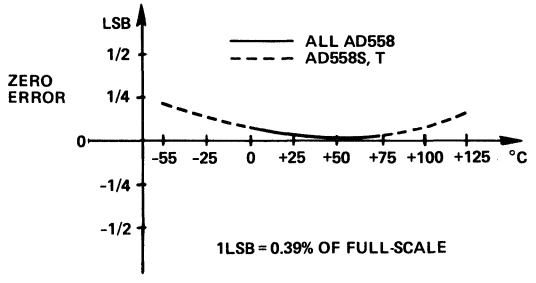


Figure 14. Zero Drift vs. Temperature Performance of AD558

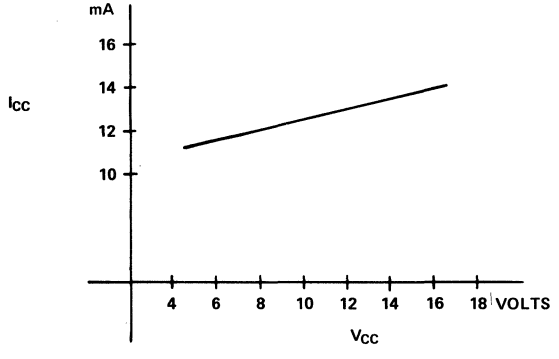


Figure 15. Quiescent Current vs. Power Supply Voltage for AD558

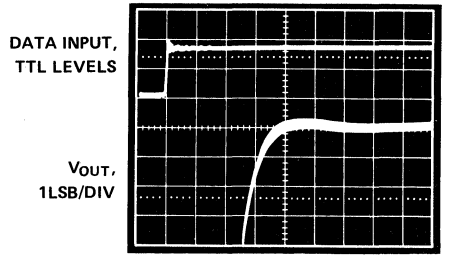


Figure 16. AD558 Settling Characteristic Detail 0V to 2.56V Output Range Full-Scale Step

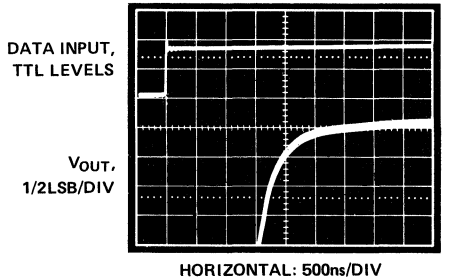


Figure 17. AD558 Settling Characteristic Detail 0V to 10V Output Range Full-Scale Step

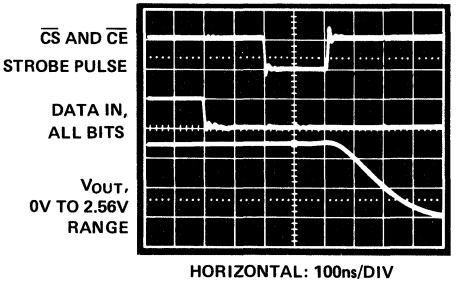


Figure 18. AD558 Logic Timing

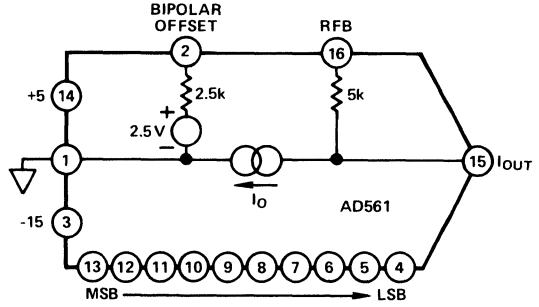
Low Cost 10-Bit Monolithic D/A Converter

AD561*

FEATURES
- **Complete Current Output Converter**
- **High Stability Buried Zener Reference**
- **Laser Trimmed to High Accuracy (1/4LSB Max Error, AD561K, T)**
- **Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges**
- **Fast Settling – 250ns to 1/2LSB**
- **Guaranteed Monotonicity Over Full Operating Temperature Range**
- **TTL/DTL and CMOS Compatible (Positive True Logic)**
- **Single Chip Monolithic Construction**
- **Available in Chip Form**

AD561 FUNCTIONAL BLOCK DIAGRAM

TO-116



PRODUCT DESCRIPTION

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of ±1/4LSB max for the K and T versions, and 1/2LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15ppm/°C; the T.C. is tested and guaranteed to 30ppm/°C max for the K and T versions, 60ppm/°C max for the S, and 80ppm/°C for the J.

The AD561 is available in four performance grades. The AD561J and K are specified for use over the 0 to +70°C temperature range and are available in either a 16-pin hermetically-sealed ceramic DIP or a 16-pin molded plastic DIP. The AD561S and T grades are specified for the -55°C to +125°C range and are available in the ceramic package.

PRODUCT HIGHLIGHTS

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4LSB max relative accuracy and 1/2LSB max differential nonlinearity. The low T.C. R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting V_{CC} to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25μA.
3. The high speed current steering switches are designed to settle in less than 250ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 to 5μs range.
4. The AD561 has an output voltage compliance range from -2 to +10 volts, thus allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40MΩ open collector output impedance results in negligible errors due to output leakage currents.

SPECIFICATIONS ($T_A = +25°C$, $V_{CC} = +5V$, $V_{EE} = -15V$, unless otherwise specified)

MODEL	AD561J MIN	AD561J TYP	AD561J MAX	AD561K MIN	AD561K TYP	AD561K MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			*			V
Bit OFF Logic "0"			+0.8			*	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V							
Bit ON Logic "1"	70% V_{CC}			*			V
Bit OFF Logic "0"			30% V_{CC}			*	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+5	+100		*	*	nA
Bit OFF Logic "0"		-5	-25		*	*	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	*	*	*	mA
Bipolar	±0.75	±1.0	±1.2	*	*	*	mA
Resistance (Exclusive of Application Resistors)		40M			*		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		*	*	% of F.S.
Capacitance		25			*		pF
Compliance Voltage	-2	-3	+10	*	*	*	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			*		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		8	10		*	*	mA
V_{EE}, -10.8V dc to -16.5V dc		12	16		*	*	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		*	*	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		*	*	ppm of F.S./%
TEMPERATURE RANGE							
Operating		0 to +70			*	*	°C
Storage ("D" Package)		-65 to +150			*	*	°C
("N" Package)		-25 to +85			*	*	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	80		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT		0 to +10			*		V
RANGES		-5 to +5			*		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			*		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			*		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			*		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			*		% of F.S.

NOTES
*Specifications same as AD561J specs.
Specifications subject to change without notice.

MODEL	AD561S MIN	AD561S TYP	AD561S MAX	AD561T MIN	AD561T TYP	AD561T MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			**			V
Bit OFF Logic "0"			+0.8			**	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V							
Bit ON Logic "1"	70% V_{CC}			**			V
Bit OFF Logic "0"			30% V_{CC}			**	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+20	+100		**	**	nA
Bit OFF Logic "0"		-25	-100		**	**	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	**	**	**	mA
Bipolar	±0.75	±1.0	±1.2	**	**	**	mA
Resistance (Exclusive of Application Resistors)		40M			**		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		**	**	% of F.S.
Capacitance		25			**		pF
Compliance Voltage	-2	-3	+10	**	**	**	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			**		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		6	10		**	**	mA
V_{EE}, -10.8V dc to -16.5V dc		11	16		**	**	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		**	**	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		**	**	ppm of F.S./%
TEMPERATURE RANGE							
Operating		-55 to +125			**	**	°C
Storage		-65 to +150			**	**	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	60		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT RANGES		0 to +10 -5 to +5			** **		V V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			**		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			**		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			**		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			**		% of F.S.

NOTES
**Specifications same as AD561S specs.
Specifications subject to change without notice.

CIRCUIT DESCRIPTION

A simplified schematic with the essential circuit features of the AD561 is shown in Figure 1. The voltage reference, CR1, is a buried zener (or subsurface breakdown diode). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long term stability and lower noise are the major benefits the buried zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so that the positive supply can be allowed to go as low as 4.5 volts. The temperature coefficient of each diode is determined individually; this data is then used to laser trim a compensating circuit to balance the overall T.C. to zero. The typical resulting T.C. is 0 to ±15ppm/°C.

The negative reference level is inverted and scaled by A_1 to give a +2.5 volt reference (which can be driven by the low positive supply). The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the 2.5kΩ bipolar offset resistor.

The 2.5kΩ scaling resistor and control amplifier A_2 then force a 1mA reference current to flow through reference transistor Q1, which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since Q_1 and Q_2 have equal emitter areas and have equal 5kΩ emitter resistors, Q_2 also carries 1mA. The ladder voltage drop constrains Q_7 (with area 4A) to carry only 0.5mA; Q_8 carries 0.25mA, etc.

The first four significant bit cells are scaled exactly in emitter area to match Q_1 for optimum V_{BE} and V_{BE} drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18mV V_{BE} difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is done by forcing 120μA through the 150Ω interbase resistors. These resistors and the R-2R ladder resistors are actively laser-trimmed at the wafer level to bring total device accuracy to better than 1/4LSB. Sufficient ratio accuracy in the last two bits is obtained by simple emitter area ratio such that it is unnecessary to use additional area for ladder resistors. The current in Q_{16} is added to the ladder to balance it properly but is not switched to the output; thus full scale is 1023/1024 x 2mA.

The switching cell of Q_3, Q_4, Q_5 and Q_6 serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, thus minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface) is applied to one side of each cell.

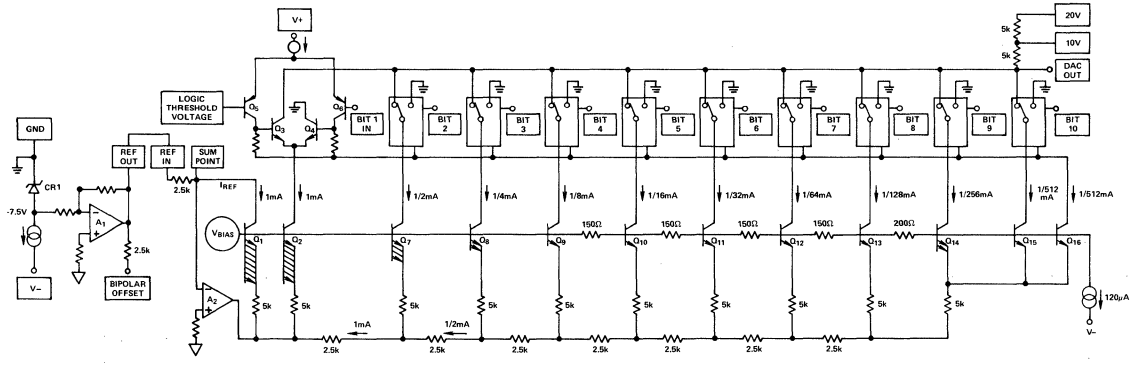


Figure 1. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

PIN CONFIGURATION
TOP VIEW

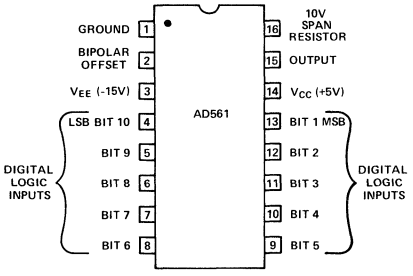


Figure 2.

AD561 ORDERING GUIDE

MODEL	TEMP RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PACKAGE OPTIONS*
AD561JD	0 to +70°C	±½LSB max	80ppm max	D-16
AD561JN	0 to +70°C	±½LSB max	80ppm max	N-16
AD561KD	0 to +70°C	±¼LSB max	30ppm max	D-16
AD561KN	0 to +70°C	±¼LSB max	30ppm max	N-16
AD561SD	-55 to +125°C	±½LSB max	60ppm max	D-16
AD561TD	-55 to +125°C	±¼LSB max	30ppm max	D-16

*See Section 14 for package outline information.

AD562/AD563*

FEATURES

True 12-Bit Accuracy
Guaranteed Monotonicity Over Full Temperature Range
Hermetic 24-Pin DIP
TTL/DTL and CMOS Compatibility
Positive True Logic

PRODUCT DESCRIPTION

The AD562/AD563 are monolithic 12-bit digital-to-analog converters consisting of especially designed precision bipolar switches and control amplifiers and compatible high stability silicon chromium thin film resistors. The AD563 also includes its own internal voltage reference.

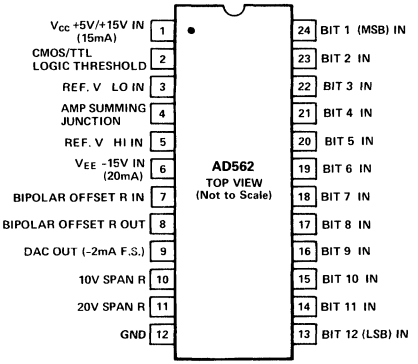
A unique combination of advanced circuit design, high stability SiCr thin film resistor processing and laser trimming technology provide the AD562/AD563 with true 12-bit accuracy. The maximum error at +25°C is limited to ±½LSB on all versions and monotonicity is guaranteed over the full operating temperature range.

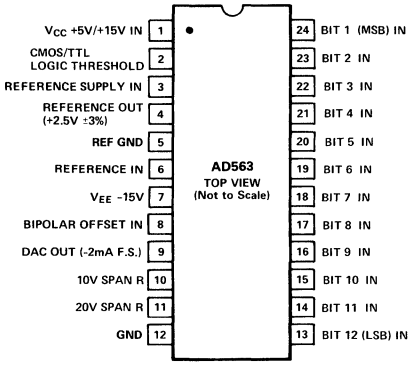
The AD562 and AD563 are recommended for high accuracy 12-bit D/A converter applications where true 12-bit performance is required, but low cost and small size are considerations. Both devices are also ideal for use in constructing A/D conversion systems and as building blocks for higher resolution D/A systems. J and K versions are specified for operation over the 0 to +70°C temperature range, the S and T for operation over the extended temperature range, -55°C to +125°C. All are packaged in a 24-pin, hermetically sealed, ceramic, dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD562 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, the AD563 is recommended with its internal low drift voltage reference.
2. True 12-bit resolution is achieved with guaranteed monotonicity over the full operating temperature range. Voltage outputs are easily implemented by using an external operational amplifier and the AD562/AD563s internally provided feedback resistors.
3. The devices incorporate a newly developed and fully differential, non-saturating precision current switching cell structure which provides increased immunity to supply voltage variation and also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation.

AD562, AD563 PIN CONFIGURATIONS





4. The thin film resistor network contains gain, range, and bipolar offset resistors so that various output voltage ranges can be programmed by changing connections to the device terminal leads. Thin film resistors are laser trimmed while the device is powered to accurately calibrate all scale factors. The scale factors are dependent upon the tracking coefficient (<±2ppm/°C) of these resistors, rather than upon their absolute temperature coefficients.
5. TTL or CMOS input can be accommodated for supply voltages from +5V to +15V.
6. Positive true logic eliminates the need for additional inverter components.

***Covered by Patent Nos. 3,961,326; 4,141,004; 3,747,088; RE 28,633; 3,803,590; 4,020,486; the AD563 is also covered by 4,213,806; 4,136,349.**

SPECIFICATIONS (T_A = +25°C, unless otherwise specified)

MODEL	AD562KD/BIN AD562KD/BCD	AD562AD/BIN AD562AD/BCD	AD562SD/BIN AD562SD/BCD
DATA INPUTS (positive True, Binary (BCD) and Offset Binary (BCD))			
TTL, V_{CC} = +5V, Pin 2 Open Circuit			
Bit ON Logic "1"	+2.0V	*	*
Bit OFF Logic "0"	+0.8V max	*	*
CMOS, 4.75 ≤ V_{CC} ≤ 15.8, Pin 2 Tied to Pin 1			
Bit ON Logic "1"	70%V_{CC} min	*	*
Bit OFF Logic "0"	30%V_{CC} max	*	*
Logic Current (Each Bit)			
Bit ON Logic "1"	+20nA typ, +100nA max	*	*
Bit OFF Logic "0"	−50μA typ, −100μA max	*	*
OUTPUT			
Current			
Unipolar	−1.6mA min, −2.0mA typ, −2.4mA max	*	*
Bipolar	±0.8mA min, ±1.0mA typ, ±1.2mA max	*	*
Resistance (Exclusive of Span Resistors)	5.3kΩ min, 6.6kΩ typ, 7.9kΩ max	*	*
Unipolar Zero (All Bits OFF)	0.01% of F.S. typ, 0.05% of F.S. max	*	*
Capacitance	33pF typ	*	*
Compliance Voltage	−1.5V to +10V typ	*	*
RESOLUTION			
Binary	12 Bits	*	*
BCD	3 Digits	*	*
ACCURACY (Error Relative to Full Scale)			
Binary	±1/2LSB max	*	±1/4LSB max
BCD	±1/2LSB max	*	±1/10LSB max
DIFFERENTIAL NONLINEARITY	±1/2LSB max	*	*
SETTLING TIME TO 1/2LSB All Bits ON-to-OFF or OFF-to-ON	1.5μs typ	*	*
POWER REQUIREMENTS			
V_{CC}, +4.75 to +15.8V dc	15mA typ, 18mA max	*	*
V_{EE}, −15V dc ±5%	20mA typ, 25mA max	*	*
POWER SUPPLY GAIN SENSITIVITY			
V_{CC} @ +5V dc	2ppm of F.S./% max	*	*
V_{CC} @ +15V dc	2ppm of F.S./% max	*	*
V_{EE} @ −15V dc	6ppm of F.S./% max	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C typ	−25°C to +85°C	−55°C to +125°C
Storage	−65°C to +150°C typ	*	*
TEMPERATURE COEFFICIENT			
Unipolar Zero	2ppm of F.S./°C max	*	*
Bipolar Zero	4ppm of F.S./°C max	*	*
Gain	5ppm of F.S./°C max	*	*
Differential Nonlinearity	2ppm of F.S./°C	*	1ppm of F.S./°C
MONOTONICITY	Guaranteed Over Full Operating Temperature Range	*	*
EXTERNAL ADJUSTMENTS[1]			
Gain Error with Fixed 50Ω Resistor	±0.2% of F.S. typ	*	*
Bipolar Zero Error with Fixed 50Ω Resistor	±0.1% of F.S. typ	*	*
Gain Adjustment Range	±0.25% of F.S. typ	*	*
Binary Bipolar Zero Adjustments Range	±0.25% of F.S. typ	*	*
BCD Bipolar Offset Adjustment Range	±0.17% of F.S. typ	*	*
PROGRAMMABLE OUTPUT RANGES	0 to +5V typ	*	*
	−2.5V to +2.5V typ	*	*
	0V to +10V typ	*	*
	−5V to +5V typ	*	*
	−10V to +10V typ	*	*
REFERENCE INPUT			
Input Impedance	20kΩ typ	*	*

*Specifications same as AD562KD. **Specifications same as AD563KD. ***Specifications same as AD563JD. [1]Device calibrated with internal reference.
Specifications subject to change without notice.

AD563JD/BIN AD563JD/BCD	AD563KD/BIN AD563KD/BCD	AD563SD/BIN AD563SD/BCD	AD563TD/BIN AD563TD/BCD
• •	• •	• •	• •
• •	• •	• •	• •
• •	• •	• •	• •
• • • • •	• • • • •	• • • • •	• • • • •
• •	• •	• •	• •
• •	±1/4LSB ±1/4LSB	•• ••	•• ••
•	•	•	•
•	•	•	•
15mA typ, 20mA max •	••• •	••• •	••• •
3ppm of F.S./% typ, 10ppm of F.S./% max 3ppm of F.S./% typ, 10ppm of F.S./% max 14ppm of F.S./% typ, 25ppm of F.S./% max	••• ••• •••	••• ••• •••	••• ••• •••
• •	• •	-55°C to +125°C •	-55°C to +125°C •
With Internal Reference 1ppm of F.S./°C typ, 2ppm of F.S./°C max 10ppm of F.S./°C max 50ppm of F.S./°C max •	 ••• ••• 20ppm of F.S./°C max •	 ••• ••• 30ppm of F.S./°C max •	 ••• ••• 10ppm of F.S./°C max •
•	•	•	•
With Fixed 10Ω Resistor ±0.2% of F.S. typ	•••	•••	•••
• •	• •	• •	• •
•	•	•	•
•	•	•	•
• • • • •	• • • • •	• • • • •	• • • • •
5kΩ typ	•••	•••	•••

THE AD562/AD563 OFFERS TRUE 12-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

Accuracy: Analog Devices defines accuracy as the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) *for any bit combination.* The AD563, for example, is laser trimmed to ¼LSB (0.006% of F.S.) maximum error at +25°C for K, S and T versions . . . ½LSB for the J version.

Monotonicity: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD562/AD563 are monotonic over their full operating temperature range.

Differential Nonlinearity: Monotonic behavior requires that the differential nonlinearity error be <1LSB both at 25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a one LSB change in digital input code. For example, for a 10V full-scale output, a change of one LSB in the digital input code should result in a 2.4mV change in the analog output (10V x 1/4096 = 2.4mV). If in actual use, however, a one LSB change in the input code results in a change of 1.3mV in analog output, the differential nonlinearity would be 1.1mV, or 0.011% of F.S. The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1ppm/°C) of error. The resulting error could then be as much as 0.006% + 0.01% = 0.016% of F.S. (1LSB represents 0.024% of F.S.). All versions of the AD563 are 100% tested to be monotonic over the full operating temperature range.

UNIPOLAR DAC's

STEP I . . . OUTPUT RANGE

Determine the output range required. For +10V F.S., connect the external operational amplifier output to Pin 10 and leave Pin 11 unconnected. For +5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

STEP II . . . ZERO ADJUST

Turn all bits OFF and adjust R_1 until op amp output is 0 volts.

STEP III . . . GAIN ADJUST

Turn all bits ON for binary DAC's (bits 1, 4, 5, 8, 9 and 12 ON for BCD DAC's). Adjust R_2 until op amp output is:

BINARY	BCD
4.9988V for +5V Range	4.9950 for +5V Range
9.9976 for +10V Range	9.9900 for +10V Range

BIPOLAR DAC's

STEP I . . . OUTPUT RANGE

Determine the output range required. For ±10V F.S., connect the external op amp output to Pin 11 and leave Pin 10 unconnected. For ±5V F.S., connect the external op amp output to Pin 10 and leave Pin 11 unconnected. For ±2.5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

STEP II . . . OFFSET ADJUST

Turn all bits OFF and adjust R_3 until op amp output is:

-2.5000V for ±2.5V Range
-5.0000V for ±5V Range
-10.0000V for ±10V Range

STEP III . . . GAIN ADJUST (Bipolar Zero)

Turn bit 1 ON for Binary DAC's (bits 2 and 4 ON for BCD DAC's). Adjust R_2 until op amp output is 0 volts.

ORDERING GUIDE

MODEL	INPUT CODE	TEMP. RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PACKAGE OPTION*
AD562KD/BIN	Binary	0 to +70°C	±1/2LSB max	5ppm max	D-24
AD562KD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	5ppm max	D-24
AD562AD/BIN	Binary	-25°C to +85°C	±1/2LSBmax	5ppm max	D-24
AD562AD/BCD	Binary Coded Decimal	-25°C to +85°C	±1/2LSB max	5ppm max	D-24
AD562SD/BIN	Binary	-55°C to +125°C	±1/4LSB max	5ppm max	D-24
AD562SD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/10LSB max	5ppm max	D-24
AD563JD/BIN	Binary	0 to +70°C	±1/2LSB max	50ppm max	D-24
AD563JD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	50ppm max	D-24
AD563KD/BIN	Binary	0 to +70°C	±1/4LSB max	20ppm max	D-24
AD563KD/BCD	Binary Coded Decimal	0 to +70°C	±1/4LSB max	20ppm max	D-24
AD563SD/BIN	Binary	-55°C to +125°C	±1/4LSB max	30ppm max	D-24
AD563SD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/4LSB max	30ppm max	D-24
AD563TD/BIN	Binary	-55°C to +125°C	±1/4LSB max	10ppm max	D-24
AD563TD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/4LSB max	10ppm max	D-24

*See Section 14 for package outline information.

ANALOG DEVICES

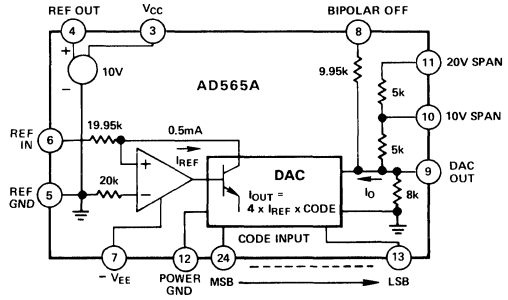
High-Speed 12-Bit Monolithic D/A Converters

AD565A*/AD566A*

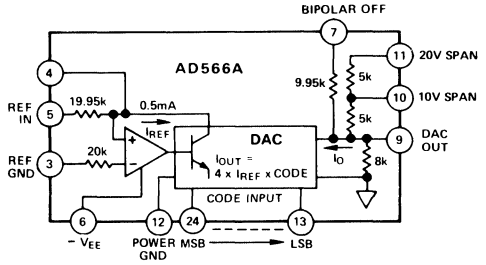
FEATURES

- Single Chip Construction
- Very High-Speed Settling to 1/2LSB
  - AD565A: 250ns max
  - AD566A: 350ns max
- Full-Scale Switching Time: 30ns
- Guaranteed for Operation with ±12V Supplies: AD565A with -12V Supply: AD566A
- Linearity Guaranteed Over Temperature: 1/2LSB max (K, T Grades)
- Monotonicity Guaranteed Over Temperature
- Low Power: AD566A = 180mW max; AD565A = 225mW max
- Use with On-Board High-Stability Reference (AD565A) or with External Reference (AD566A)
- Low Cost

AD565A FUNCTIONAL BLOCK DIAGRAM



AD566A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD565A and AD566A are fast 12-bit digital-to-analog converters which incorporate the latest advances in analog circuit design to achieve high speeds at low cost.

The AD565A and AD566A use 12 precision, high-speed bipolar current-steering switches, control amplifier and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The AD565A also includes a buried zener reference that features low-noise, long-term stability and temperature drift characteristics comparable to the best discrete reference diodes.

The combination of performance and flexibility in the AD565A and AD566A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565A and AD566A have a 10-90% full-scale transition time less than 35ns and settle to within ±1/2LSB in 250ns max (350ns for AD566A). Both are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD565A and AD566A the ideal choice for high-speed display drivers as well as fast analog-to-digital converters.

The laser trimming process which provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A resulting in a typical full-scale gain TC of 10 ppm/°C. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

***Covered by Patent Nos.: 3,803,590; RE 28,633; 4,213,806; 4,136,349; 4,020,486; 3,747,088.**

AD565A and AD566A are available in four performance grades. The J and K are specified for use over the 0 to +70°C temperature range while the S and T grades are specified for the -55°C to +125°C range. All are packaged in a 24-pin, hermetically sealed, ceramic, dual-in-line package.

PRODUCT HIGHLIGHTS

1. The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The devices incorporate a newly developed, fully differential, nonsaturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562/3 with very fast switching times and an optimally-damped settling characteristic.
3. The devices also contain SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +15V, V_{EE} = −15V, unless otherwise specified)

MODEL	AD565AJ MIN	AD565AJ TYP	AD565AJ MAX	AD565AK MIN	AD565AK TYP	AD565AK MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S. Range
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

NOTES

[1] The digital inputs are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc.

[3] For operation at elevated temperatures the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

Specifications subject to change without notice.

MODEL	AD565AS MIN	AD565AS TYP	AD565AS MAX	AD565AT MIN	AD565AT TYP	AD565AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	**+2.0**		**+5.5**	**+2.0**		**+5.5**	V
Bit OFF Logic "0"			**+0.8**			**+0.8**	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	**+300**		+120	**+300**	μA
Bit OFF Logic "0"		+35	**+100**		+35	**+100**	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	**-1.6**	-2.0	**-2.4**	**-1.6**	-2.0	**-2.4**	mA
Bipolar (all bits on or off)	**±0.8**	±1.0	**±1.2**	**±0.8**	±1.0	**±1.2**	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	**0.05**		0.01	**0.05**	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	**0.15**		0.05	**0.1**	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	**±1/2**		±1/8	**±1/4**	LSB
		(0.006)	**(0.012)**		(0.003)	**(0.006)**	% of F.S. Range
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	**MONOTONICITY GUARANTEED**			**MONOTONICITY GUARANTEED**			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	**2**		1	**2**	ppm/°C
Bipolar Zero		5	**10**		5	**10**	ppm/°C
Gain (Full Scale)		15	**30**		10	**15**	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		**250**	**400**		**250**	**400**	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	**5**		3	**5**	mA
V_{EE}, -11.4 to -16.5V dc		-12	**-18**		-12	**-18**	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	**10**		3	**10**	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	**25**		15	**25**	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGES (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω							
Resistor for R2 (Figure 2)		±0.1	**±0.25**		±0.1	**±0.25**	% of F.S. Range
Bipolar Zero Error with Fixed							
50Ω Resistor for R1 (Figure 3)		±0.05	**±0.15**		±0.05	**±0.1**	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	**9.90**	10.00	10.10	**9.90**	10.00	**10.10**	V
Current (available for external loads)[3]	**1.5**	2.5		**1.5**	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

SPECIFICATIONS (T_A = +25°C, V_{EE} = −15V, unless otherwise specified)

MODEL	AD566AJ MIN	AD566AJ TYP	AD566AJ MAX	AD566AK MIN	AD566AK TYP	AD566AK MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.R.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		3	5	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, −11.4 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = −11.4 to −16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%–90%	5mA/μs
90%–10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.
CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

NOTES
[1] The digital input levels are guaranteed but not tested over the temperature range.
[2] The power supply gain sensitivity is tested in reference to a V_{EE} of −15V dc.
Specifications subject to change without notice.

MODEL	AD566AS MIN	AD566AS TYP	AD566AS MAX	AD566AT MIN	AD566AT TYP	AD566AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	**+2.0**		**+5.5**	**+2.0**		**+5.5**	V
Bit OFF Logic "0"	**0**		**+0.8**	0		**+0.8**	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	**+300**		+120	**+300**	μA
Bit OFF Logic "0"		+35	**+100**		+35	**+100**	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	**-1.6**	-2.0	**-2.4**	**-1.6**	-2.0	**-2.4**	mA
Bipolar (all bits on or off)	**±0.8**	±1.0	**±1.2**	**±0.8**	±1.0	**±1.2**	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	**0.05**		0.01	**0.05**	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	**0.15**		0.05	**0.1**	% of F.S.R
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	**±1/2**		±1/8	**±1/4**	LSB
		(0.006)	**(0.012)**		(0.003)	**(0.006)**	% of F.S.R.
T_{min} to T_{max}		±1/2	**±3/4**		±1/4	**±1/2**	LSB
		(0.012)	**(0.018)**		(0.006)	**(0.012)**	% of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	**±3/4**		±1/4	**±1/2**	LSB
T_{min} to T_{max}	**MONOTONICITY GUARANTEED**			**MONOTONICITY GUARANTEED**			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	**2**		1	**2**	ppm/°C
Bipolar Zero		5	**10**		5	**10**	ppm/°C
Gain (Full Scale)		7	**10**		3	**5**	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits On-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -11.4 to -16.5V dc		-12	**-18**		-12	**-18**	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = -11.4 to -16.5V dc		15	**25**		15	**25**	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor R2 (Figure 3)		±0.1	**±0.25**		±0.1	**±0.25**	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	**±0.15**		±0.05	**±0.1**	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	**300**		180	**300**	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%-90%	5mA/μs
90%-10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.

CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

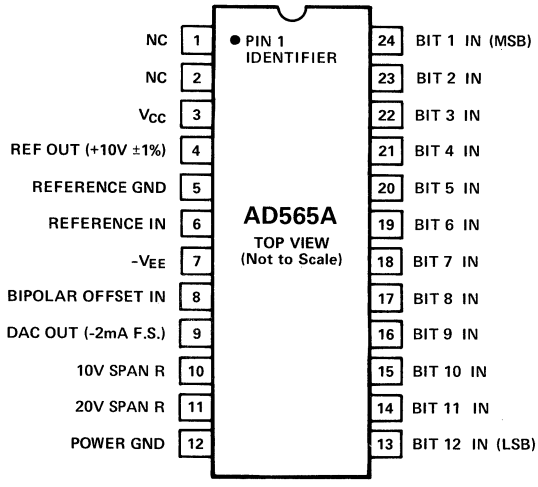
Specifications subject to change without notice.

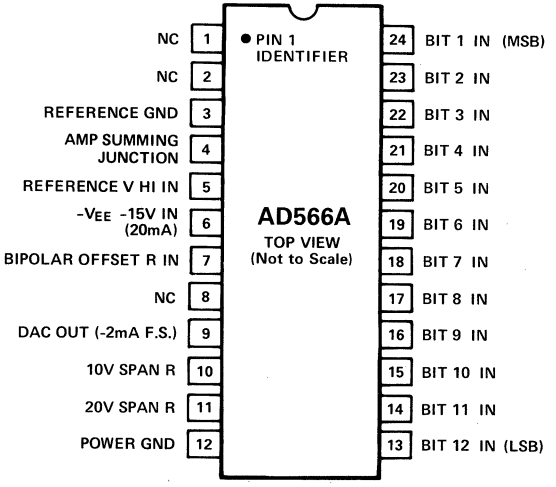
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground (AD565A) . . . . . 0V to −18V
Voltage on DAC Output (Pin 9) . . . . . −3V to +12V
Digital Inputs (Pins 13 to 24) to
Power Ground . . . . . −1.0V to +7.0V
Ref in to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref out (AD565A) . . . . . Indefinite Short to Power Ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

PIN DESIGNATIONS





AD565A ORDERING GUIDE

Model	Package Option*	Temp. Range	Linearity Error Max @ 25°C	Max Gain T.C. (ppm of F.S./°C)
AD565AJD/BIN	Ceramic (D-24)	0 to +70°C	±1/2LSB	50
AD565AKD/BIN	Ceramic (D-24)	0 to +70°C	±1/4LSB	20
AD565ASD/BIN	Ceramic (D-24)	−55°C to +125°C	±1/2LSB	30
AD565ATD/BIN	Ceramic (D-24)	−55°C to 1125°C	±1/4LSB	15

*See Section 14 for package outline information.

AD566A ORDERING GUIDE

Model	Package Option*	Temp. Range	Linearity Error Max @ +25°C	Max Gain T.C. (ppm of F.S./°C)
AD566AJD/BIN	Ceramic (D-24)	0 to +70°C	±1/2LSB	10
AD566AKD/BIN	Ceramic (D-24)	0 to +70°C	±1/4LSB	3
AD566ASD/BIN	Ceramic (D-24)	−55°C to +125°C	±1/2LSB	10
AD566ATD/BIN	Ceramic (D-24)	−55°C to +125°C	±1/4LSB	3

*See Section 14 for package outline information.

GROUNDING RULES

The AD565A and AD566A bring out separate reference and power grounds to allow optimum connections for low noise and high-speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 1. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 2. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 3.

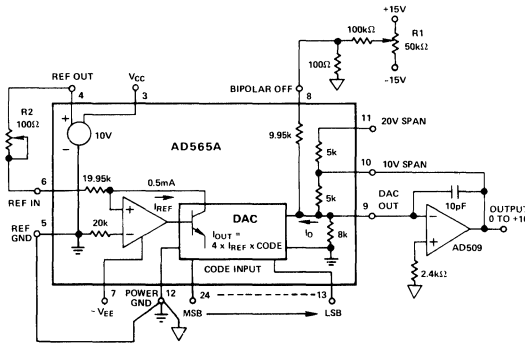


Figure 1. 0 to +10V Unipolar Voltage Output

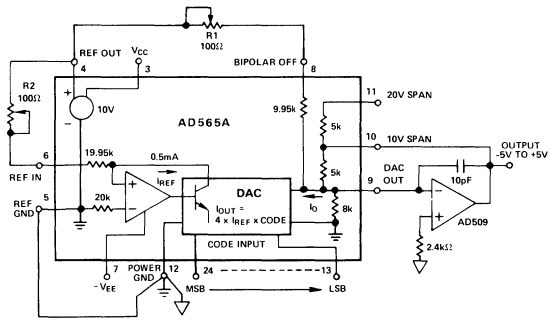


Figure 2. ±5V Bipolar Voltage Output

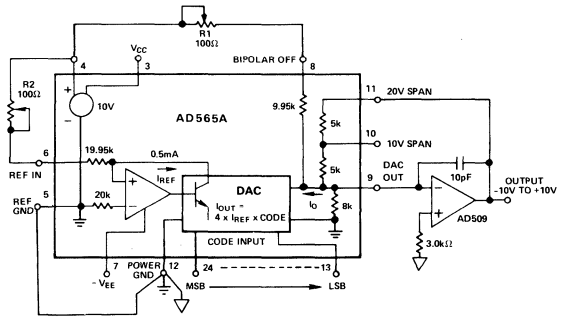


Figure 3. ±10V Voltage Output

CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 5. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 output volts.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 6. OTHER VOLTAGE RANGES

The AD566A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 6.

DIGITAL INPUT MSB LSB	Straight Binary	Offset Binary	Two's Compl.*
000000000000	Zero	-Full Scale	Zero
011111111111	Mid Scale -1LSB	Zero -1LSB	+FS -1LSB
100000000000	+1/2 FS	Zero	-FS
111111111111	+FS -1LSB	+ Full Scale -1LSB	Zero -1LSB

*Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

Table I. Digital Input Codes

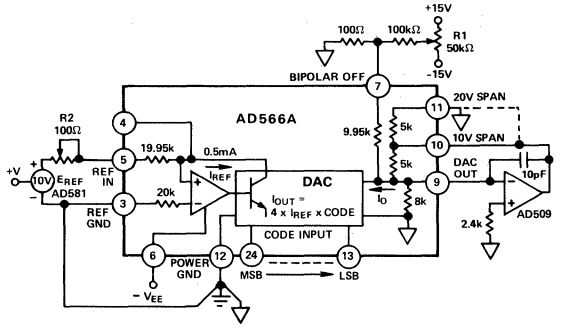


Figure 4. 0 to +10V Unipolar Voltage Output

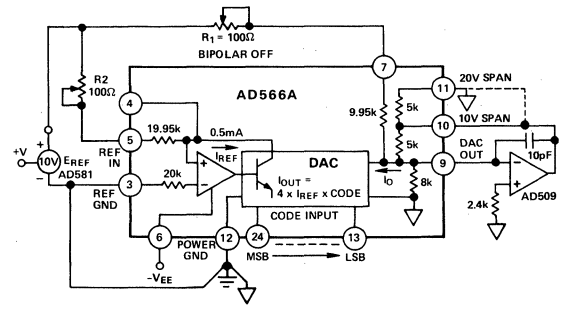
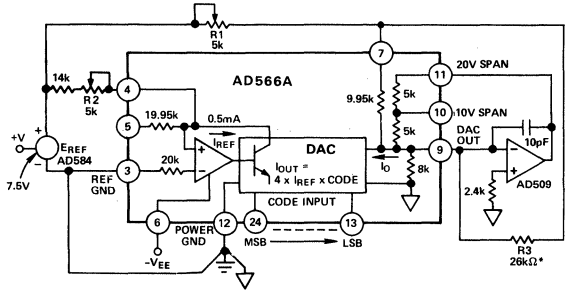


Figure 5. ±5V Bipolar Voltage Output



*THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISH A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPLAINED ON PREVIOUS PAGE.

Figure 6. ±10V Voltage Output

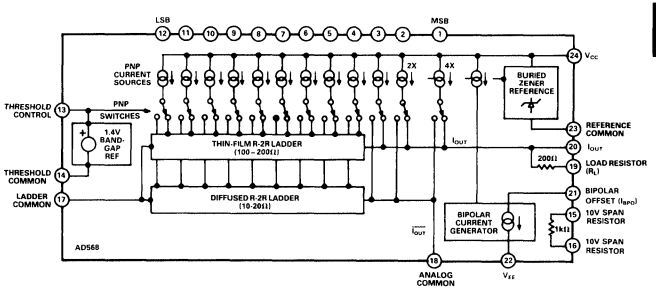
12-Bit Ultrahigh Speed Monolithic D/A Converter

AD568

FEATURES

- **Ultrahigh Speed: Current Settling to 1LSB in 35ns**
- **High Stability Buried Zener Reference on Chip**
- **Monotonicity Guaranteed Over Temperature**
- **10.24mA Full-Scale Output Suitable for Video Applications**
- **Integral and Differential Linearity Guaranteed Over Temperature**
- **0.3" "Skinny DIP" Packaging**
- **Variable Threshold Allows TTL and CMOS Interface**

AD568 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD568 is an ultrahigh-speed, 12-bit digital-to-analog converter (DAC) settling to 0.025% in 35ns. The monolithic device is fabricated using Analog Devices' Complementary Bipolar (CB) Process. This is a proprietary process featuring high-speed NPN and PNP devices on the same chip without the use of dielectric isolation or multichip hybrid techniques. The high speed of the AD568 is maintained by keeping impedance levels low enough to minimize the effects of parasitic circuit capacitances.

The DAC consists of 16 current sources configured to deliver a 10.24mA full-scale current. Multiple matched current sources and thin-film ladder techniques are combined to produce bit weighting. The DAC's output is a 10.24mA full scale (FS) for current output applications or a 1.024V FS unbuffered voltage output. Additionally, a 10.24V FS buffered output may be generated using an onboard 1kΩ span resistor with an external op amp. Bipolar ranges are accomplished by pin strapping.

Laser wafer trimming insures full 12-bit linearity. All grades of the AD568 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100Ω ± 1.0%. The gain temperature coefficient of the voltage output is 30ppm/°C max (K).

The AD568 is available in three performance grades. The AD568JQ and KQ are available in 24-pin cerdip (0.3") packages and are specified for operation from 0 to +70°C. The AD568SQ features operation from −55°C to +125°C and is also packaged in the hermetic 0.3" cerdip.

PRODUCT HIGHLIGHTS

1. The ultrafast settling time of the AD568 allows leading edge performance in waveform generation, graphics display and high-speed A/D conversion applications.
2. Pin strapping provides a variety of voltage and current output ranges for application versatility. Tight control of the absolute output current reduces trim requirements in externally-scaled applications.
3. Matched on-chip resistors can be used for precision scaling in high-speed A/D conversion circuits.
4. The digital inputs are compatible with TTL and +5V CMOS logic families.
5. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.

SPECIFICATIONS (@ T_A = +25°C, V_{CC}, V_{EE} = ±15V unless otherwise noted)

Model	AD568J			AD568K			AD568S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	12			12			12			Bits
ACCURACY[1]										
Linearity	−1/2		+1/2	−1/4		+1/4	−1/2		+1/2	LSB
T_{min} to T_{max}	−3/4		+3/4	−1/2		+1/2	−3/4		+3/4	LSB
Differential Nonlinearity	−1		+1	−1/2		+1/2	−1		+1	LSB
T_{min} to T_{max}	−1		+1	−1		+1	−1		−1	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE									
Unipolar Offset	−0.2		+0.2	*		*	*		*	% of FSR
Bipolar Offset	−1.0		+1.0	*		*	*		*	% of FSR
Bipolar Zero	−0.2		+0.2	*		*	*		*	% of FSR
Gain Error	−1.0		+1.0	*		*	*		*	% ofFSR
TEMPERATURE COEFFICIENTS[2]										
Unipolar Offset	−5		+5	−3		+3	−5		+5	ppm of FSR/°C
Bipolar Offset	−30		+30	−20		+20	−30		+30	ppm of FSR/°C
Bipolar Zero	−15		+15	*		*	*		*	ppm of FSR/°C
Gain Drift	−50		+50	−30		+30	−50		+50	ppm of FSR/°C
Gain Drift (I_{OUT})	−150		+150	*		*	*		*	ppm of FSR/°C
DATA INPUTS										
Logic Levels (T_{min} to T_{max})										
V_{IH}	2.0		7.0	*		*	*		*	V
V_{IL}	0.0		0.8	*		*	*		*	V
Logic Currents (T_{min} to T_{max})										
I_{IH}	−10	0	+10	*	*	*	*	*	*	µA
I_{IL}	−0.5	−60	−100	*	*	*	*	−100	−200	µA
V_{TH} Pin Voltage		1.4			*			*		V
CODING	BINARY, OFFSET BINARY									
CURRENT OUTPUT RANGES	0 to 10.24, ±5.12									mA
VOLTAGE OUTPUT RANGES	0 to 1.024, ±0.512									V
COMPLIANCE VOLTAGE	−2		+1.2	*		*	*		*	V
OUTPUT RESISTANCE										
Exclusive of R_L	160	200	240		*			*		Ω
Inclusive of R_L	99	100	101		*			*		Ω
SETTLING TIME										
Current to										
±0.025%		35			*			*		ns to 0.025% of FSR
±0.1%		23			*			*		ns to 0.1% of FSR
Voltage										
50Ω Load[3], 0.512V p-p,										
to 0.025%		37			*			*		ns to 0.025% of FSR
to 0.1%		25			*			*		ns to 0.1% of FSR
to 1%		18			*			*		ns to 1% of FSR
75Ω Load[3], 0.768V p-p,										
to 0.025%		40			*			*		ns to 0.025% of FSR
to 0.1%		25			*			*		ns to 0.1% of FSR
to 1%		20			*			*		ns to 1% of FSR
100Ω (Internal R_L)[3], 1.024V p-p,										
to 0.025%		50			*			*		ns to 0.025% of FSR
to 0.1%		38			*			*		ns to 0.1% of FSR
to 1%		24			*			*		ns to 1% of FSR
Glitch Impulse[4]		350			*			*		pV-sec
Peak Amplitude		15			*			*		% of FSR
FULL-SCALE TRANSITION[5]										
10% to 90% Rise Time		11			*			*		ns
90% to 10% Fall Time		11			*			*		ns
POWER REQUIREMENTS										
+13.5V to +16.5V		27	32		*	*		*	*	mA
−13.5V to −16.5V		−7	−8		*	*		*	*	mA
Power Dissipation		525	625		*	*		*	*	mW
PSRR			0.05			*			*	% of FSR/V
TEMPERATURE RANGE										
Rated Specification[2]	0		70	0		70	−55		+125	°C
Storage	−65		+150	*		*	*		*	°C

NOTES
*Same as AD568J.
[1]Measured in I_{OUT} mode.
[2]Measured in V_{OUT} mode, unless otherwise specified. See text for further information.
[3]Total Resistance. Refer to Figure 3.
[4]At the major carry, driven by HCMOS logic. See text for further explanation.
[5]Measured in V_{OUT} mode.
Specifications shown in boldface are tested on all production units at final electrical test.
Specifications subject to change without notice.

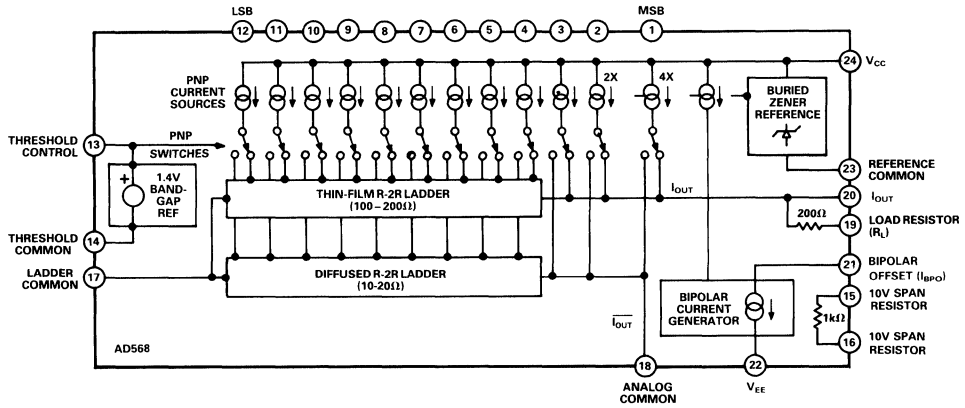


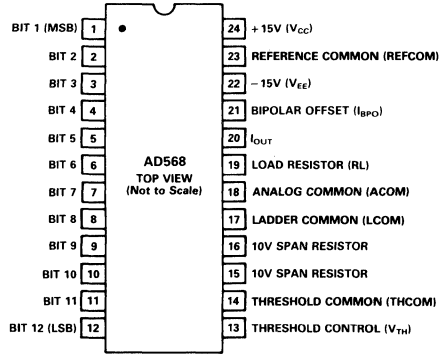
Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to REFCOM . . . . . 0V to +18V
V_{EE} to REFCOM . . . . . 0V to −18V
REFCOM to LCOM . . . . . +100mV to −10V
ACOM to LCOM . . . . . ±100mV
THCOM to LCOM . . . . . ±500mV
SPANs to LCOM . . . . . ±12V
I_{BPO} to LCOM . . . . . ±5V
I_{OUT} to LCOM . . . . . −5V to V_{TH}
Digital Inputs to THCOM . . . . . −500mV to +7.0V
Voltage Across Span Resistor 12V
V_{TH} to THCOM . . . . . −0.7V to +1.4V
Logic Threshold Control Input Current 5mA
Power Dissipation 1000mW
Storage Temperature Range
Q (Cerdip) Package . . . . . −65°C to +150°C
Junction Temperature . . . . . 175°C
Thermal Resistance
θ_{ja} . . . . . 75°C/W
θ_{jc} . . . . . 25°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD568 PIN CONFIGURATION



ORDERING GUIDE

Model	Package Option*	Temperature Range °C	Linearity Error Max. @ 25°C	Voltage Gain T.C. Max ppm/°C
AD568JQ	24-Lead Cerdip (Q-24)	0 to +70	±1/2	±50
AD568KQ	24-Lead Cerdip (Q-24)	0 to +70	±1/4	±30
AD568SQ	24-Lead Cerdip (Q-24)	−55 to +125	±1/2	±50

*See Section 14 for package outline information.

Definitions

LINEARITY ERROR (also called INTEGRAL NON-LINEARITY OR INL): Analog Devices defines linearity error as the maximum deviation of the actual analog output from the ideal output (a straight line drawn from 0 to FS − 1LSB) for any bit combination expressed in multiples of 1LSB. The AD568 is laser trimmed to 1/4LSB (0.006% of FS) maximum linearity error at +25°C for the K version and 1/2LSB for the J and S versions.

DIFFERENTIAL LINEARITY ERROR (also called DIFFERENTIAL NONLINEARITY or DNL): DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases.

UNIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (0V or 0mA) when the inputs are set to all 0s is called unipolar offset error.

BIPOLAR OFFSET ERROR: The deviation of the analog output from the ideal (negative half-scale) when the inputs are set to all 0s is called bipolar offset error.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal half-scale output of 0V (or 0mA) for bipolar mode when only the MSB is on (100.....00) is called bipolar zero error.

GAIN ERROR: The difference between the ideal and actual output span of FS − 1LSB, expressed in % of FS, or LSB, when all bits are on.

GLITCH IMPULSE: Asymmetrical switching times in a DAC give rise to undesired output transients which are quantified by their glitch impulse. It is specified as the net area of the glitch in nV-sec or pA-sec.

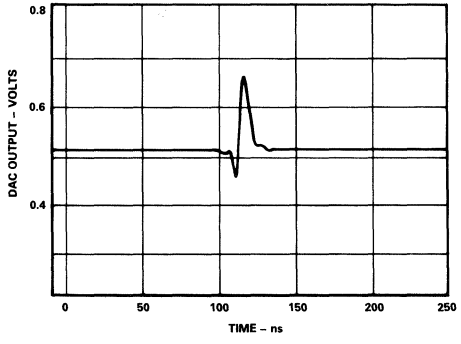


Figure 2. AD568 Glitch Impulse

COMPLIANCE VOLTAGE: The range of allowable voltage at the output of a current-output DAC which will not degrade the accuracy of the output current.

SETTLING TIME: The time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

Connecting the AD568

UNBUFFERED VOLTAGE OUTPUT

Unipolar Configuration

Figure 3 shows the AD568 configured to provide a unipolar 0 to +1.024V output range. In this mode, the bipolar offset terminal, Pin 21, should be grounded if not used for offset trimming.

The nominal output impedance of the AD568 with Pin 19 grounded has been trimmed to 100Ω, ±1%. Other output impedances can be generated with an external resistor, R_{EXT}, between Pins 19 and 20. An R_{EXT} equalling 300Ω will yield a total output resistance of 75Ω, while an R_{EXT} of 100Ω will provide 50Ω of output resistance. Note that since the full-scale output current of the DAC remains 10.24mA, changing the load impedance changes the unbuffered output voltage accordingly. Settling time and full-scale range characteristics for these load impedances are provided in the specifications table.

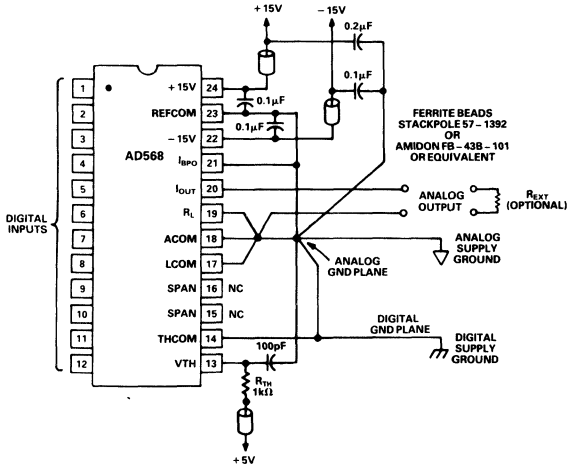


Figure 3. Unipolar Output Unbuffered 0 to +1.024V

Bipolar Configuration

Figure 4 shows the connection scheme used to provide a bipolar output voltage range of 1.024V. The bipolar offset (−0.512V) occurs when all bits are OFF (00 . . . 00), bipolar zero (0V)

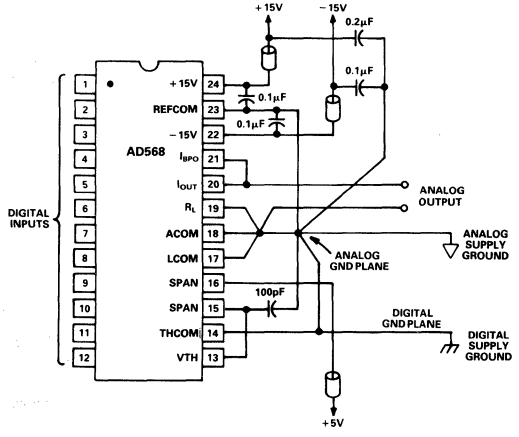


Figure 4. Bipolar Output Unbuffered ±0.512V

occurs when the MSB is ON with all other bits OFF (10 . . . 00), and full-scale minus 1LSB (0.51175V) is generated when all bits are ON (11 . . . 11). Figure 5 shows an optional bipolar mode with a 2.048V range. The scale factor in this mode will not be as accurate as the configuration shown in Figure 4, because the laser-trimmed resistor R_L is not used.

Figure 4 also demonstrates how the internal span resistor may be used to bias the V_{TH} pin (Pin 13) from a 5V supply. This eliminates the requirement for an external R_{TH} in applications that do not require the precision span resistor.

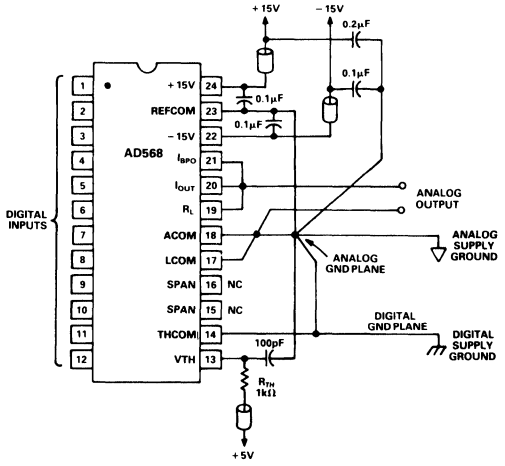


Figure 5. Bipolar Output Unbuffered ± 1.024V

Optional Gain and Zero Adjustment

The gain and offset are laser trimmed to minimize their effects on circuit performance. However, in some applications, it may be desirable to externally reduce these errors further. In those cases, the following procedures are suggested.

UNIPOLAR MODE: (Refer to Figure 6)

Step 1 – Set all bits (BIT 1–BIT 12) to Logic "0" (OFF) – note the output voltage. This is the offset error.

Step 2 – Set all bits to Logic "1" (ON). Adjust the gain trim resistor so that the output voltage is equal to the desired full scale minus 1LSB plus the offset error measured in step 1.

Step 3 – Reset all bits to Logic "0" (OFF). Adjust the offset trim resistor for 0V output.

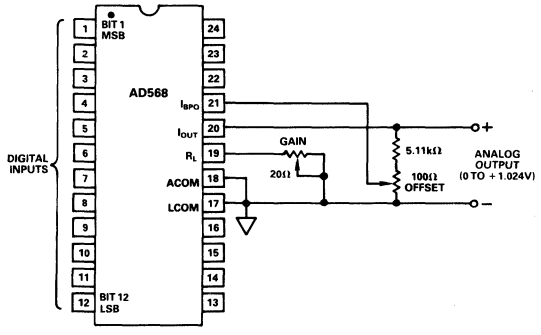


Figure 6. Unbuffered Unipolar Gain and Zero Adjust

BIPOLAR MODE (Refer to Figure 7)

Step 1 – Set bits to offset binary "zero" (10 . . . 00). Adjust the zero resistor to produce 0V at the DAC output. This removes the bipolar zero error.

Step 2 – Set all bits to Logic "1" (ON). Adjust gain trim resistor so the output voltage is equal to the desired full-scale minus 1LSB.

Step 3 – (Optional) If precise trimming of the bipolar offset is preferred to trimming of bipolar zero: set all bits to Logic "0" (OFF). Trim the zero resistor to produce the desired negative full scale at the DAC output.

Note: this may slightly compromise the bipolar zero trim.

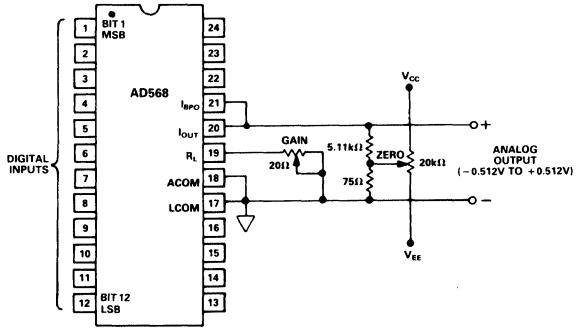


Figure 7. Bipolar Unbuffered Gain and Zero Adjust

BUFFERED VOLTAGE OUTPUT

For full-scale outputs of greater than 1V, some type of external buffer amplifier is required. The AD840 fills this requirement perfectly, settling to 0.025% from a 10V full-scale step in less than 100ns.

A 1kΩ span resistor has been provided on chip for use as a feedback resistor in buffered applications. Using R_{SPAN} (Pins 15, 16) introduces a 100mW code-dependent power source onto the chip which may generate a slight degradation in linearity. Maximum linearity performance can be realized by using an external span resistor.

Unipolar Inverting Configuration

Figure 8 shows the connections for producing a − 10.24V full-scale swing. This configuration uses the AD568 in the current output mode into a summing junction at the inverting input terminal of the external op amp. With the load resistor R_L grounded, the DAC has an output impedance of 100Ω. This produces a noise gain of 11 from the noninverting terminal of the op amp, and hence, satisfies the stability criterion of the AD840 (stable at a gain of 10). The addition of a 5pF compensation capacitor across the 1kΩ feedback resistor produces optimal settling. Lower noise gain can be achieved by connecting R_L to I_{OUT}, increasing the DAC output impedance to approximately 200Ω, and reducing the noise gain to 6 (illustrated in Figure 9). While the output in this configuration will feature improved noise performance, it is somewhat less stable and may suffer from ringing. The compensation capacitance should be increased to 7pF to maintain stability at this reduced gain.

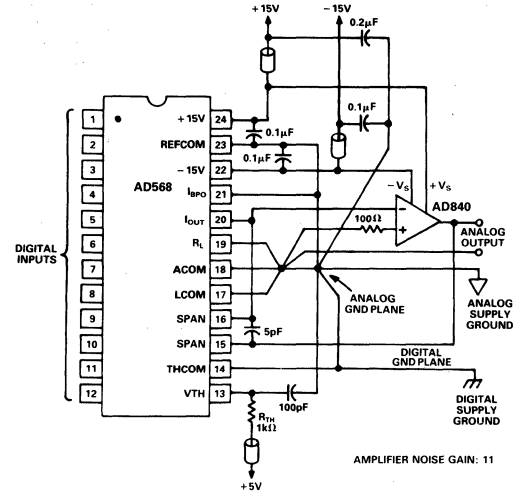


Figure 8. Unipolar Output Buffered 0 to −10.24V

Bipolar Inverting Configuration

Figure 9 illustrates the implementation of a +5.12V to −5.12V bipolar range, achieved by connecting the bipolar offset current, I_{BPO}, to the summing junction of the external amplifier. Note that since the amplifier is providing an inversion, the full-scale output voltage is −5.12V, while the bipolar offset voltage (all bits OFF) is +5.12V at the amplifier output.

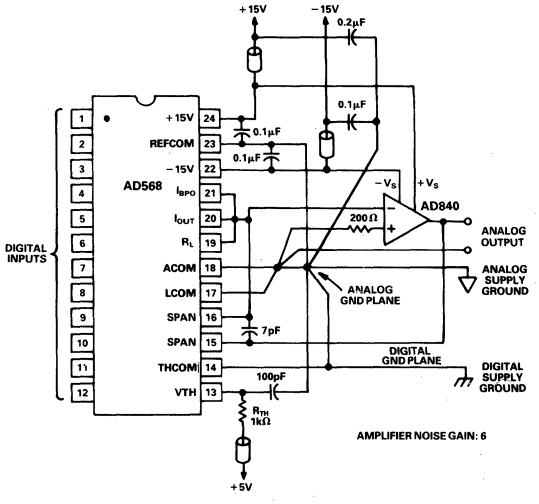


Figure 9. Bipolar Output Buffered ±5.12V

Noninverting Configuration

If a positive full-scale output voltage is required, it can be implemented using the AD568 in the unbuffered voltage output mode followed by the AD840 in a noninverting configuration (Figure 10). The noise gain of this topology is 10, requiring only 5pF across the feedback resistor to optimize settling.

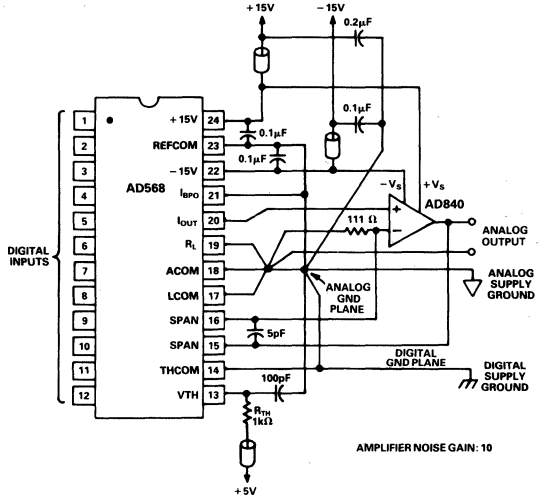


Figure 10. Unipolar Output Buffered 0 to +10.24V

Guidelines for Using the AD568

The designer who seeks to combine high speed with high precision faces a challenging design environment. Where tens of milliamperes are involved, fractions of an ohm of misplaced impedance can generate several LSBs of error. Increasing bandwidths make formerly negligible parasitic capacitances and inductances significant. As system performance reaches and exceeds that of the measurement equipment, time-honored test methods may no longer be trustworthy. The DAC's placement on the boundary between the analog and digital domains introduces additional concerns. Proper RF techniques must be used in board design, device selection, supply bypassing, grounding, and measurement if optimal performance is to be realized. The AD568 has been configured to be relatively easy to use, even in some of the more treacherous applications. The device characteristics shown in this datasheet are readily achievable if proper attention is paid to the details. Since a solid understanding of the circuit involved is one of the designer's best weapons against the difficulties of RF design, the following sections provide illustrations, explanations, examples, and suggestions to facilitate successful design with the AD568.

Current Output vs. Voltage Output

As indicated in Figures 3 through 10, the AD568 has been designed to operate in several different modes depending on the external circuit configuration. While these modes may be categorized by many different schemes, one of the most important distinctions to be made is whether the DAC is to be used to generate an output voltage or an output current. In the current output mode, the DAC output (Pin 20) is tied to some type of summing junction, and the current flowing from the DAC into this summing junction is sensed (e.g., Figures 8 and 9). In this mode, the DAC output scale is insensitive to whether the load resistor, R_L, is shorted (Pin 19 connected to Pin 20), or grounded (Pin 19 connected to Pin 18). However, this does affect the output impedance of the DAC current and may have a significant impact on the noise gain of the external circuitry. In the voltage output mode, the DAC's output current flows through its own internal impedance (perhaps in parallel with an external impedance) to generate a voltage, as in Figures 3, 4, 5, and 10. In this

case, the DAC output scale is directly dependent on the load impedance. The temperature coefficient of the AD568's internal reference is trimmed in such a way that the drift of the DAC output in the voltage output mode is centered on zero. The current output of the DAC will have an additional drift factor corresponding to the absolute temperature coefficient of the internal thin-film resistors. This additional drift may be removed by judicious placement of the 1kΩ span resistor in the signal path. For example, in Figures 8 and 9, the current flowing from the DAC into the summing junction could suffer from as much as 150ppm/°C of thermal drift. However, since this current flows through the internal span resistor (Pins 15 and 16) which has a temperature coefficient that matches the DAC ladder resistors, this drift factor is compensated and the buffered voltage at the amplifier output will be within specified limits for the voltage output mode.

Output Voltage Compliance

The AD568 has a typical output compliance range of +1.2V to −2.0V (with respect to the LCOM Pin). The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, as shown in Figure 11, there is an equivalent output impedance of 200Ω in parallel with 15pF at the output terminal which produces an equivalent error current if the voltage deviates from the ladder common. This is a linear effect which does not change with input code. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance. The positive compliance limit is not affected by the positive power supply, but is a function of output current and the logic threshold voltage at V_{TH}, Pin 13.

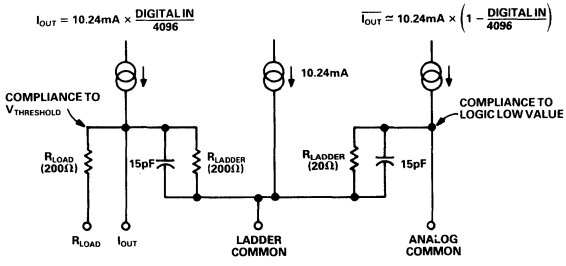


Figure 11. Equivalent Output

Digital Input Considerations

The AD568 uses a standard positive true straight binary code for unipolar outputs (all 1s full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full scale; with 111 . . . 11, the output will go to positive full scale less 1LSB; and with 100 . . 00 (only the MSB on), the output will go to zero.

The threshold of the digital inputs is set at 1.4V and does not vary with supply voltage. This is provided by a bandgap reference generator, which requires approximately 3mA of bias current achieved by tying R_{TH} to any $+V_L$ supply where

$$R_{TH} = \left(\frac{+V_L - 1.4V}{3mA}\right).$$

The input lines operate with small input currents to easily achieve interface with unbuffered CMOS logic. The digital input signals to the DAC should be isolated from the analog output as much as possible. To minimize undershoot, ringing, and possible digital feedthrough noise, the interconnect distances to the DAC inputs should be kept as short as possible. Termination resistors may improve performance if the digital lines become too long. The digital input should be free from large glitches and ringing and have maximum 10% to 90% rise and fall times of 5ns. Figure 12 shows the equivalent digital input circuit of the AD568.

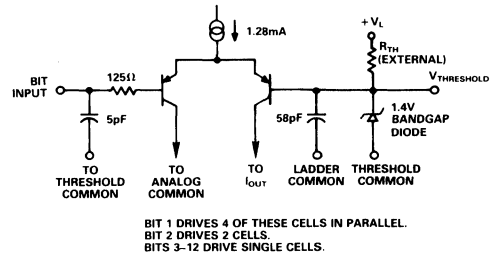


Figure 12. Equivalent Digital Input

Due to the high-speed nature of the AD568, it is recommended that high-speed logic families such as Schottky TTL, high-speed CMOS, or the new lines of FAST* TTL be used exclusively. Table I shows how DAC performance can vary depending on the driving logic used. As this table indicates, STTL, HCMOS, and FAST represent the most viable families for driving the AD568.

DAC PERFORMANCE VS. DRIVE LOGIC[1]

Logic Family	10-90% DAC Rise Time[2]	DAC SETTLING TIME[2,3] 1%	0.1%	0.025%	Glitch[4] Impulse	Maximum Glitch Excursion
TTL	11ns	18ns	34ns	50ns	2.5nV-s	240mV
LSTTL	11ns	28ns	46ns	80ns	950pV-s	160mV
STTL	9.5ns	16ns	33ns	50ns	850pV-s	150mV
HCMOS	11ns	24ns	38ns	50ns	350pV-s	115mV
FAST*	12ns	16ns	36ns	42ns	1.0nV-s	250mV

[1]All values typical, taken in test fixture diagrammed in Figure 13.
[2]Measurements are made for a 1V full-scale step into 100ΩDAC load resistance.
[3]Settling time is measured from the time the digital input crosses the threshold voltage (1.4V) to when the output is within the specified range of its final value.
[4]The worst case glitch impulse, measured on the major carry. DAC full scale is 1V.

Table I.

The variations in settling times can be attributed to differences in the rise time and current driving capabilities of the various families. Differences in the glitch impulse are predominantly dependent upon the variation in data skew. Variations in these specs occur not only between logic families, but also between different gates and latches within the same family. When selecting a gate to drive the AD568 logic input, pay particular attention to the propagation delay time specs: t_{PLH} and t_{PHL}. Selecting the smallest delays possible will help to minimize the settling time, while selection of gates where t_{PLH} and t_{PHL} are closely matched to one another will minimize the glitch impulse resulting from data skew. Of the common latches, the 74374 octal flip-flop provides the best performance in this area for many of the logic families mentioned above.

***FAST is a registered trademark of Fairchild Camera and Instrumentation Corporation.**

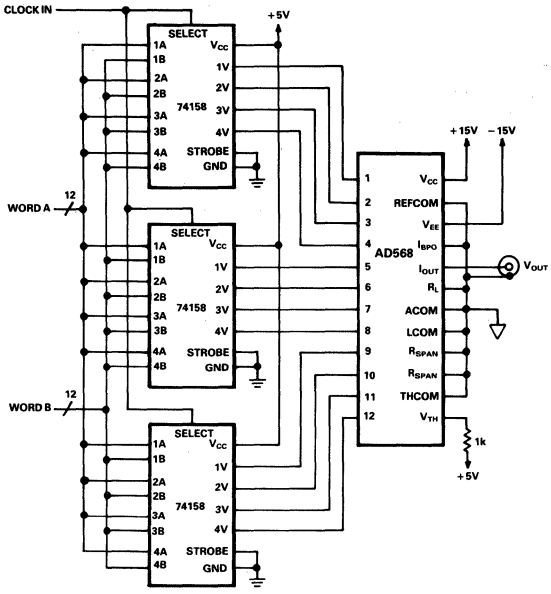


Figure 13. Test Setup for Glitch Impulse and Settling Time Measurements

Settling Time Considerations

As can be seen from Table I and the specifications page, the settling time of the AD568 is application dependent. The fastest settling is achieved in the current-output mode, since the voltage-output mode requires the output capacitance to be charged to the appropriate voltage. The DAC's relatively large output current helps to minimize this effect, but settling-time sensitive applications should avoid any unnecessary parasitic capacitance at the output node of voltage output configurations. Direct measurement of the fine scale DAC settling time, even in the voltage output mode, is extremely tricky: analog scope front ends are generally incapable of recovering from overdrive quickly enough to give an accurate settling representation. The plot shown in Figure 14 was obtained using Data Precision's 640 16-bit sampling head, which features the quick overdrive recovery characteristic of sampling approaches combined with high accuracy and relatively small thermal tail.

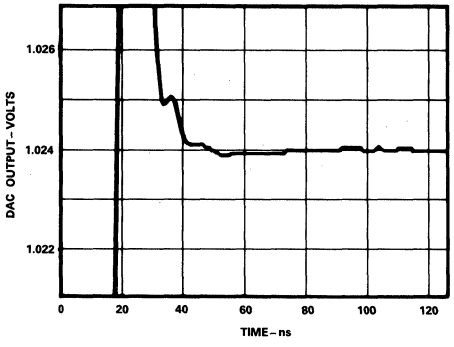


Figure 14. Zero to Full-Scale Settling

Glitch Considerations

In many high-speed DAC applications, glitch performance is a critical specification. In a conventional DAC architecture such as the AD568 there are two basic glitch mechanisms: data skew and digital feedthrough. A thorough understanding of these sources can help the user to minimize glitch in any application.

DIGITAL FEEDTHROUGH – As with any converter product, a high-speed digital-to-analog converter is forced to exist on the frontier between the noisy environment of high-speed digital logic and the sensitive analog domain. The problems of this interfacing are particularly acute when demands of high speed (greater than 10MHz switching times) and high precision (12 bits or more) are combined. No amount of design effort can perfectly isolate the analog portions of a DAC from the spectral components of a digital input signal with a 2ns risetime. Inevitably, once this digital signal is brought onto the chip, some of its higher frequency components will find their way to the sensitive analog nodes, producing a digital feedthrough glitch. To minimize the exposure to this effect, the AD568 has intentionally omitted the on-board latches that have been included in many slower DACs. This not only reduces the overall level of digital activity on chip, it also avoids bringing a latch clock pulse on board, whose opposite edge inevitably produces a substantial glitch, even when the DAC is not supposed to be changing codes. Another path for digital noise to find its way onto a converter chip is through the reference input pin. The completely internal reference featured in the AD568 eliminates this noise input, providing a greater degree of signal integrity in the analog portions of the chip.

DATA SKEW – The AD568, like many of its slower predecessors, essentially uses each digital input line to switch a separate, weighted current to either the output (I_{OUT}) or some other node (ANALOG COM). If the input bits are not changed simultaneously, or if the different DAC bits switch at different speeds, then the DAC output current will momentarily take on some incorrect value. This effect is particularly troublesome at the "carry points", where the DAC output is to change by only one LSB, but several of the larger current sources must be switched to realize this change. Data skew can allow the DAC output to move a substantial amount towards full scale or zero (depending upon the direction of the skew) when only a small transition is desired. Great care was taken in the design and layout of the AD568 to ensure that switching times of the DAC switches are symmetrical and that the length of the input data lines are short and well matched. The glitch-sensitive user should be equally diligent about minimizing the data skew at the AD568's inputs, particularly for the 4 or 5 most significant bits. This can be achieved by using the proper logic family and gate to drive the DAC, and keeping the interconnect lines between the logic outputs and the DAC inputs as short and as well matched as possible, particularly for the most significant bits. The top 6 bits should be driven from the same latch chip if latches are used.

Glitch Reduction Schemes

BIT-DESKEWING – Even carefully laid-out boards using the proper driving logic may suffer from some degree of data-skew induced glitch. One common approach to reducing this effect is to add some appropriate capacitance (usually several pF) to each of the 2 or 3 most significant bits. The exact value of each capacitor for a given application should be determined experimentally, as it will be dependent on circuit board layout and the type of driving logic used. Table II presents a few examples of how the glitch impulse may be reduced through passive deskewing.

BIT DELAY GLITCH REDUCTION EXAMPLES[1]

Logic Family	Gate	Uncompensated Glitch	Compensation Used	Compensated Glitch
HCMOS	74157	350pV-s	C2 = 5pF	250pV-s
STTL	74158	850pV-s	R1 = 50Ω, C1 = 7pF	600pV-s

NOTE
[1]Measurements were made using a modified version of the fixture shown in Figure 13, with resistors and capacitors placed as shown in Figure 15. Resistance and capacitance values were set to zero except as noted.

Table II.

As Figure 15 indicates, in some cases it may prove useful to place a few hundred ohms of series resistance in the input line to enhance the delay effect. This approach also helps to reduce some of the digital feedthrough glitch, as the higher frequency spectral components are being filtered out of the most significant bits' digital inputs.

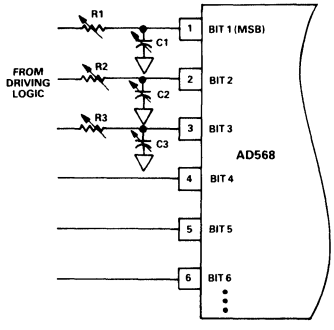


Figure 15. R-C Bit Deskewing Scheme

THRESHOLD SHIFT – It is also possible to reduce the data skew by shifting the level of logic voltage threshold, V_{TH} (Pin 13). This can be readily accomplished by inserting some resistance between the THRESHOLD COM pin (Pin 14) and ground, as in Figure 16. To generate threshold voltages below 1.4V, Pin 13 may be directly driven with a voltage source, leaving Pin 14 tied to the ground plane. As Note 2 in Table III indicates, lowering the threshold voltage may reduce output voltage compliance below the specified limits, which may be of concern in an unbuffered voltage output topology.

Table III shows the glitch reduction achieved by shifting the threshold voltage for HCMOS, STTL, and FAST logic.

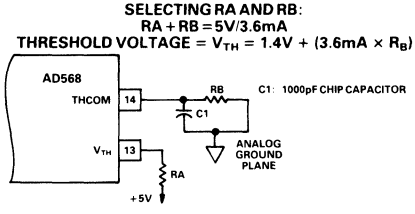


Figure 16. Positive Threshold Voltage Shift

THRESHOLD SHIFT FOR GLITCH IMPROVEMENT[1]

Logic Family	Gate	Uncompensated Glitch	Modified Threshold[2]	Resulting Glitch
HCMOS	74HC158	350pV-s	1.7V	150pV-s
STTL	74S158	850pV-s	1.0V	200pV-s
FAST	74F158	1000pV-s	1.3V	480pV-s

NOTES
[1]Measurements made on a modified version of the circuit shown in Figure 13, with a 1V full scale.
[2]Use care in any scheme that lowers the threshold voltage since the output voltage compliance of the DAC is sensitive to this voltage. If the DAC is to be operated in the voltage output mode, it is strongly suggested that the threshold voltage be set at least 200mV above the output voltage full scale.

Table III.

Deglitching

Some applications may prove so sensitive to glitch impulse that reduction of glitch impulse by an order of magnitude or more is required. In order to realize glitch impulses this low, some sort of sample-and-hold amplifier (SHA)-based deglitching scheme must be used.

There are high-speed SHAs available with specifications sufficient to deglitch the AD568, however most are hybrid in design at costs which can be prohibitive. A high performance, low cost alternative shown in Figure 17 is a discrete SHA utilizing a high-speed monolithic op amp and high-speed DMOS FET switches.

This SHA circuit uses the inverting integrator architecture. The AD841 operational amplifier used (300MHz gain bandwidth product) is fabricated on the same high-speed process as the AD568. The time constant formed by the 200Ω resistor and the 100pF capacitor determines the acquisition time and also band limits the output signal to eliminate slew induced distortion.

A discrete drive circuit is used to achieve the best performance from the SD5000 quad DMOS switch. This switch driving cell is composed of MPS571 RF npn transistors and an MC10124 TTL to ECL translator. Using this technique provides both high speed and highly symmetrical drive signals for the SD5000 switches. The switches are arranged in a single-throw double-pole (SPDT) configuration. The 360pF "flyback" capacitor is switched to the op amp summing junction during the hold mode to keep switching transients from feeding to the output. This capacitor is grounded during sample mode to minimize its effect on acquisition time.

Circuit layout for a high speed SHA is almost as critical as the design itself. Figure 17 shows a recommended layout of the deglitching cell for a double sided printed circuit board. The layout is very compact with care taken that all critical signal paths are short.

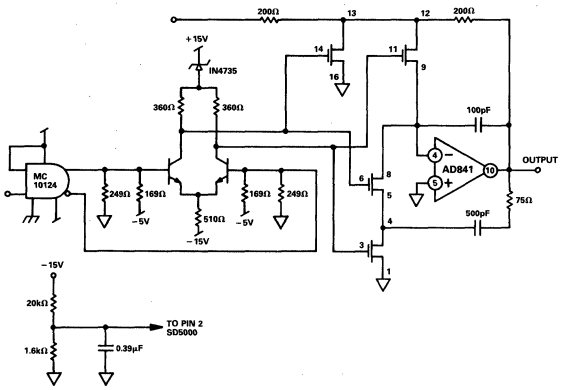


Figure 17. High Performance Deglitcher

Grounding Rules

The AD568 brings out separate reference, output, and digital power grounds. This allows for optimum management of signal ground currents for low noise and high-speed settling performance. The separate ground returns are provided to minimize changes in current flow in the analog signal paths. In this way, logic return currents are not summed into the same return path with the analog signals.

It is important to understand which supply and signal currents are flowing in which grounds so that they may be returned to the proper power supply in the best possible way.

The majority of the current that flows into the V_{CC} supply (Pin 24) flows out (depending on the DAC input code) either the ANALOG COMMON (Pin 18), the LADDER COMMON (Pin 17), and/or I_{OUT} (Pin 20).

The current in the LADDER COMMON is configured to be code independent when the output current is being summed into a virtual ground. If I_{OUT} is operated into its own output impedance (or in any unbuffered voltage output mode) the current in LADDER COMMON will become partially code dependent.

The current in the ANALOG COMMON (Pin 18) is an approximate complement of the current in I_{OUT}, i.e., zero when the DAC is at full scale and approximately 10mA at zero input code.

A relatively constant current (not code dependent) flows out the REFERENCE COMMON (Pin 23).

The current flowing out of the V_{EE} supply (Pin 22) comes from a combination of reference ground and BIPOLAR OFFSET (Pin 21). The plus and minus 15V supplies are decoupled to the REFERENCE COMMON.

The ground side of the load resistor R_L, ANALOG COMMON and LADDER COMMON should be tied together as close to the package pins as possible. The analog output voltage is then referred to this node and thus it becomes the "high quality" ground for the AD568. The REFERENCE COMMON (and Bipolar offset when not used), should also be connected to this node.

All of the current that flows into the V_{TH} terminal (Pin 13) from the resistor tied to the 5V logic supply (or other convenient positive supply) flows out the THRESHOLD COMMON (Pin 14). This ground pin should be returned directly to the digital ground plane on its own individual line.

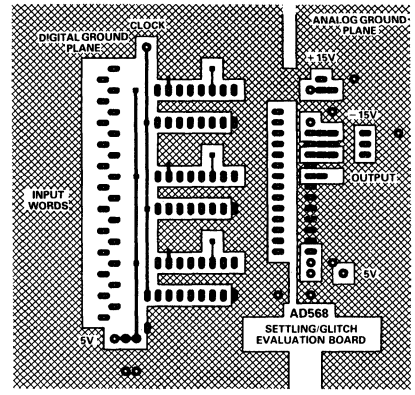
The +5V logic supply should be decoupled to the THRESHOLD COMMON.

Because the V_{TH} pin is connected directly to the DAC switches it should be decoupled to the analog output signal common.

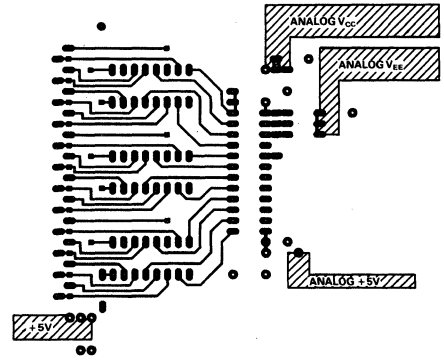
In order to preserve proper operation of the DAC switches, the digital and analog grounds need to eventually be tied together. This connection between the ground planes should be made within 1/2" of the DAC.

The Use of Ground and Power Planes

If used properly, ground planes can perform a myriad of functions on high-speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from one another, with the analog ground plane covering analog signal traces and the digital ground plane confined to areas covering digital interconnect.



Component Side



Foil Side

Figure 18. Printed Circuit Board Layout

The two ground planes should be connected at or near the DAC. Care should be taken to insure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC and any clock lines. On the analog side, this includes the DAC output signal as well as the supply feeders. The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual function of providing a low series impedance power supply to the part as well as providing some "free" capacitive decoupling to the appropriate ground plane. Figure 18 illustrates the PC board used for the circuit shown in Figure 13. This design was constructed on a simple two-layer board and illustrates many of the points discussed above. If more layers of interconnect are available, even better results are possible.

Using The Right Bypass Capacitors

Probably the most important external components associated with any high-speed design are the capacitors used to bypass the power supplies. Both selection and placement of these capacitors can be critical and, to a large extent, dependent upon the specifics of the system configurations. The dominant consideration in selection of bypass capacitors for the AD568 is minimization of series resistance and inductance. Many capacitors will begin to look inductive at 20MHz and above, the very frequencies we are most interested in bypassing. Ceramic and film-type capacitors generally feature lower series inductance than tantalum or electrolytic types. A few general rules are of universal use when approaching the problem of bypassing:

Bypass capacitors should be installed on the printed circuit board with the shortest possible leads consistent with reliable construction. This helps to minimize series inductance in the leads. Chip capacitors are optimal in this respect.

Some series inductance between the DAC supply pins and the power supply plane often helps to filter out high-frequency power supply noise. This inductance can be generated using a small ferrite bead.

High-Speed Interconnect and Routing

It is essential that care be taken in the signal and power ground circuits to avoid inducing extraneous voltage drops in the signal ground paths. It is suggested that all connections be short and direct, and as physically close to the package as possible, so that the length of any conduction path shared by external components will be minimized. When runs exceed an inch or so in length, some type of termination resistor may be required. The necessity and value of this resistor will be dependent upon the logic family used.

For maximum ac performance, the DAC should be mounted directly to the circuit board; sockets should not be used as they introduce unwanted capacitive coupling between adjacent pins of the device.

Applications

1μs, 12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

The AD568's unique combination of high speed and true 12-bit accuracy can be used to construct a 12-bit SAR-type A/D converter with a sub-μs conversion time. Figure 19 shows the configuration used for this application. A negative analog input voltage is converted into current and brought into a summing junction with the DAC current. This summing junction is bidirectionally clamped with two Shottky diodes to limit its voltage excursion from ground. This voltage is differentially amplified and passed to a high-speed comparator. The comparator output is latched and fed back to the successive approximation register, which is then clocked to generate the next set of codes for the DAC.

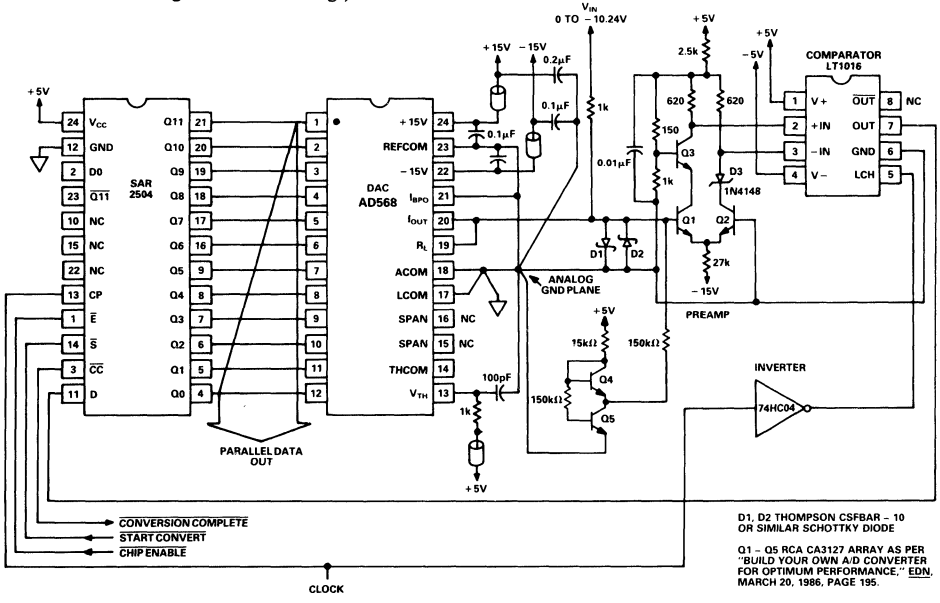


Figure 19. AD568 1μs Successive Approximation A/D Application

Circuit Details

Figure 20 shows an approximate timing budget for the A/D converter. If 12 cycles are to be completed in 1μs, approximately 80ns is allowed for each cycle. Since the Shottky diodes clamp the voltage of the summing junction, the DAC settling time approaches the current-settling value of 35ns, and hence uses up less than half the timing budget.

To maintain simplicity, a simple clock is used that runs at a constant rate throughout the conversion, with a duty cycle of approximately 90%. If absolute speed is worth the additional complexity, the clock frequency can be increased as the conversion progresses since the DAC must settle from increasingly smaller steps.

When seeking a cycle time of less than 100ns, the delays generated by the older generation SAR registers become problematic. Newer, higher speed SAR logic chips are becoming available in the classic 2504 pinout that cuts the logic overhead in half. One example of this is Zyrel's ZR2504.

Finding a comparator capable of keeping up with this DAC arrangement is fairly difficult: it must respond to an overdrive of 250μV (1LSB) in less than 25ns. Since no inexpensive comparator exists with these specs, special arrangements must be made. The LT1016 comparator provides relatively quick response, but requires at least 5mV of overdrive to maintain this speed. A discrete preamplifier may be used to amplify the summing junction voltage to sufficiently overdrive the comparator. Care must be exercised in the layout of the preamp/comparator block to avoid introducing comparator instability with the preamp's additional gain.

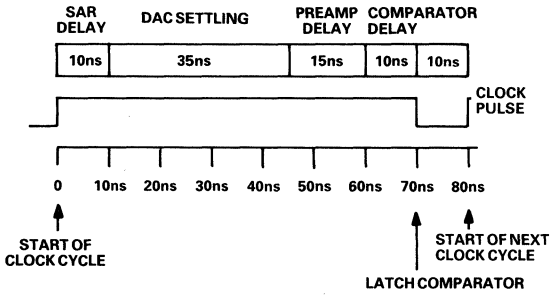


Figure 20. Typical Clock Cycle for a 1μs SAR A/D Converter

HIGH-SPEED MULTIPLYING DAC

A powerful use for the AD568 is found in multiplying applications, where the DAC controls the amplitude of a high-speed signal. Specifically, using the AD568 as the control voltage input signal for the AD539 60MHz analog multiplier and AD5539 wide-band op amp, a high-speed multiplying DAC can be built.

In the application shown in Figure 21, the AD568 is used in a buffered voltage output mode to generate the input to the AD539's control channel. The speed of the AD568 allows oversampling of the control signal waveform voltage, thereby providing increased spectral purity of the amplitude envelope that modulates the analog input channels.

The AD568 is configured in the unbuffered unipolar output mode. The internal 200Ω load resistor creates the 0-1V FS output signal, which is buffered and amplified to a 0-3V range suitable for the control channel of the AD539.

A 500Ω input impedance exists at Pin 1, the input channel. To provide a buffer for the 0-1V output signal from the AD568 looking into the impedance and to achieve the full-scale range, the AD841, high-speed, fast settling op amp is included. The gain of 3 is achieved with a 2kΩ resistor configured in follower mode with a 1kΩ pot and 500Ω resistor. A 20kΩ pot with connections to Pins 3, 4 and 12 is provided for offset trim.

The AD539 can accept two separate input signals, each with a nominal full-scale voltage range of ±2V. Each signal can then be simultaneously controlled by the AD568 signal at the common input channel, V_X. The current outputs from the two signal channels, Pins 11 and 14, applied to the AD5539 in a subtracting configuration, provide the voltage output signal:

$$V_{OUT} = \frac{D}{4096} \times \frac{V_{Y1} - V_{Y2}}{2V} \quad (0 \leq D \leq 4095)$$

For applications where only a single channel is involved, channel 2, V_{Y2}, is tied to ground. This provides:

$$V_{OUT} = \frac{D}{4096} \times \frac{V_{Y1}}{2V} \quad (0 \leq D \leq 4095)$$

Some AD539 circuit details: The control amplifier compensation capacitor for Pin 2, C_C, must have a minimum value of 3000pF to provide circuit stability. For improved bandwidth and feedthrough, the feedthrough capacitor between Pins 1 and 2 should be 5-20% of C_C. A Schottky diode at Pin 2 can improve recovery time from small negative values of V_X. Lead lengths along the path of the high-speed signal from AD568 should be kept at a minimum.

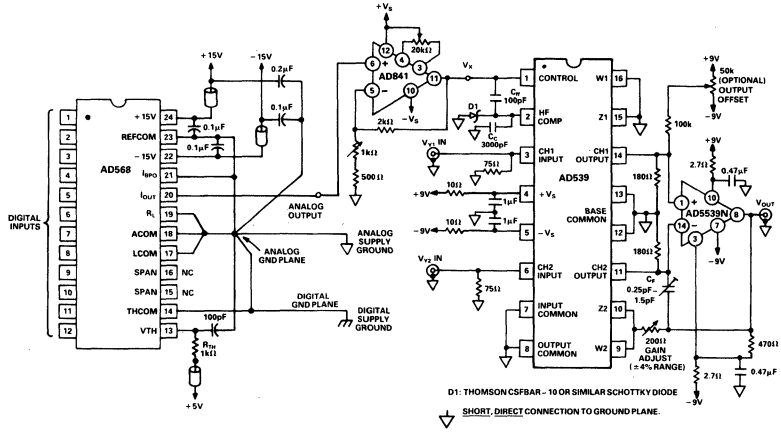


Figure 21. Wideband Digitally Controlled Multiplier

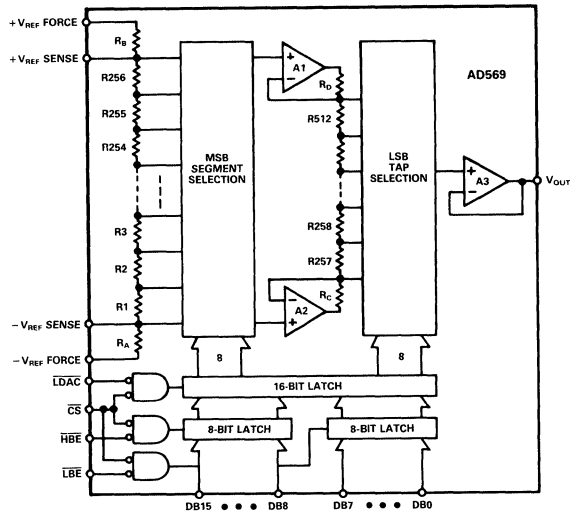
16-Bit Monotonic Voltage Output D/A

AD569

FEATURES
Guaranteed 16-Bit Monotonicity
Monolithic BiMOS II Construction
±0.01% Typical Nonlinearity
8- and 16-Bit Bus Compatibility
3μs Settling to 16-Bits
Low Drift
Low Power
Low Noise

APPLICATIONS
Robotics
Closed-Loop Positioning
High-Resolution ADCs
Microprocessor-Based Process Control

AD569 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD569 is a monolithic 16-bit digital-to-analog converter (DAC) manufactured in Analog Devices' BiMOS II process. BiMOS II allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry. The AD569 chip includes two resistor strings, selector switches, decoding logic, buffer amplifiers, and double-buffered input latches.

The AD569's voltage-segmented architecture insures 16-bit monotonicity over time and temperature. Integral nonlinearity is maintained at ±0.01%, while differential nonlinearity is ±0.0004%. The on-chip, high-speed buffer amplifiers provide a voltage output settling time of 3μs to within ±0.001% for a full-scale step.

The reference input voltage which determines the output range can be either unipolar or bipolar. Nominal reference range is ±5V and separate reference force and sense connections are provided for high accuracy applications. The AD569 can operate with an ac reference in multiplying applications.

Data may be loaded into the AD569's input latches from 8- and 16-bit buses. The double-buffered structure simplifies 8-bit bus interfacing and allows multiple DACs to be loaded asynchronously and updated simultaneously. Four TTL/LSTTL/5V CMOS-compatible signals control the latches: $\overline{CS}$, $\overline{LBE}$, $\overline{HBE}$, and $\overline{LDAC}$.

The AD569 is available in five grades: J and K versions are specified from 0 to +70°C and are packaged in a 28-pin plastic DIP and 28-pin PLCC package; AD and BD versions are specified from −25°C to +85°C and are packaged in a 28-pin ceramic DIP. The SD version, also in a 28-pin ceramic DIP, is specified from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Monotonicity to 16 bits is insured by the AD569's voltage-segmented architecture.
2. The output range is ratiometric to an external reference or ac signal. Gain error and gain drift of the AD569 are negligible.
3. The AD569's versatile data input structure allows loading from 8- and 16-bit buses.
4. The on-chip output buffer amplifier can supply ±5V into a 1kΩ load, and can drive capacitive loads of up to 1000pF.
5. Kelvin connections to the reference inputs preserve the gain and offset accuracy of the transfer function in the presence of wiring resistances and ground currents.

SPECIFICATIONS (T_A = +25°C, $+V_S$ = +12V, $-V_S$ = −12V, $+V_{REF}$ = +5V, $-V_{REF}$ = −5V, unless otherwise noted)

Model	AD569JN/AD			AD569KN/BD			AD569SD			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION			16			16			16	Bits
LOGIC INPUTS										
V_{IH} (Logic "1")	2.0		5.5	2.0		5.5	2.0		5.5	Volts
V_{IL} (Logic "0")	0		0.8	0		0.8	0		0.8	Volts
I_{IH} (V_{IH} = 5.5V)			10			10			10	μA
I_{IL} (V_{IL} = 0V)			10			10			10	μA
TRANSFER FUNCTION CHARACTERISTICS										
Integral Nonlinearity		±0.02	**±0.04**		±0.01	**±0.024**			**±0.04**	%FSR[1]
T_{min} to T_{max}		±0.02	**±0.04**		±0.020	**±0.024**			**±0.04**	%FSR
Differential Nonlinearity		±1/2	**±1**		±1/4	**±1/2**			**±1**	LSB
T_{min} to T_{max}		±1/2	**±1**		±1/2	**±1**			**±1**	LSB
Unipolar Offset[2]			**±500**			**±350**			**±500**	μV
T_{min} to T_{max}			**±750**			**±450**			**±750**	μV
Bipolar Offset[2]			**±500**			**±350**			**±500**	μV
T_{min} to T_{max}			**±750**			**±450**			**±750**	μV
Full Scale Error[2]			**±350**			**±350**			**±350**	μV
T_{min} to T_{max}			**±450**			**±450**			**±450**	μV
Bipolar Zero[2]			**±0.04**			**±0.024**			**±0.04**	%FSR
T_{min} to T_{max}			**±0.04**			**±0.024**			**±0.04**	%FSR
REFERENCE INPUT										
$+V_{REF}$ Range[3]	−5		+5	−5		+5	−5		+5	Volts
$-V_{REF}$ Range[3]	−5		+5	−5		+5	−5		+5	Volts
Resistance	15	20	25	15	20	25	15	20	25	kΩ[4]
OUTPUT CHARACTERISTICS										
Voltage	−5		+5	−5		+5	−5		+5	Volts
Capacitive Load			1000			1000			1000	pF
Resistive Load	1			1			1			kΩ
Short Circuit Current		10			10			10		mA
POWER SUPPLIES										
Voltage										
$+V_S$	**+10.8**	+12	**+13.2**	**+10.8**	+12	**+13.2**	**+10.8**	+12	**+13.2**	Volts
$-V_S$	**−10.8**	−12	**−13.2**	**−10.8**	−12	**−13.2**	**−10.8**	−12	**−13.2**	Volts
Current										
$+I_S$		+9	**+13**		+9	**+13**		+9	**+13**	mA
$-I_S$		−9	**−13**		−9	**−13**		−9	**−13**	mA
Power Supply Sensitivity[5]										
$+10.8V \leq +V_S \leq +13.2V$		±0.5	**±2**		±0.5	**±2**		±0.5	**±2**	ppm/%
$-10.8V \geq -V_S \geq -13.2V$		±1	**±3**		±1	**±3**		±1	**±3**	ppm/%
TEMPERATURE RANGE										
Specified										
JN, KN, JP, KP	0		+70	0		+70				°C
AD, BD	−25		+85	−25		+85				°C
SD							−55		+125	°C
Storage										
JN, KN, JP, KP	−65		+150	−65		+150				°C
AD, BD, SD	−65		+150	−65		+150	−65		+150	°C

NOTES
[1]FSR stands for Full-Scale Range, and is 10V for a −5 to +5V span.
[2]Refer to Definitions section.
[3]For operation with supplies other than ±12V, refer to the Power Supply and Reference Voltage Range Section.
[4]Measured between $+V_{REF}$ Force and $-V_{REF}$ Force.
[5]Sensitivity of Full-Scale Error due to changes in $+V_S$ and sensitivity of Offset to changes in $-V_S$.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance Only and are not subject to test.
$+V_S = +12V$; $-V_S = -12V$; $+V_{REF} = +5V$; $-V_{REF} = -5V$ except where stated.

Parameter	Limit	Units	Test Conditions/Comments
Output Voltage Settling	5	μs max	No Load Applied
(Time to ±0.001% FS	3	μs typ	(DAC output measured from falling edge of $\overline{LDAC}$.)
For FS Step)	6	μs max	V_{OUT} Load = 1kΩ, C_{LOAD} = 1000pF.
	4	μs typ	(DAC output measured from falling edge of $\overline{LDAC}$.)
Digital-to-Analog Glitch Impulse	500	nV-sec typ	Measured with V_{REF} = 0V. DAC registers alternatively loaded with input codes of 8000_H and $0FFF_H$ (worst-case transition). Load = 1kΩ.
Multiplying Feedthrough	−100	dB max	$+V_{REF}$ = 1V rms 10kHz sine wave, $-V_{REF}$ = 0V
Output Noise Voltage Density (1kHz-1MHz)	40	nV/$\sqrt{Hz}$ typ	Measured between V_{OUT} and $-V_{REF}$

TIMING CHARACTERISTICS ($+V_S = +12V$, $-V_S = -12V$, T_{min} to T_{max})

Parameter	Limit	Units	Test Conditions/Comments
Case A[1]			150ns Pulse on $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$
t_{WC}	70	ns min	$\overline{CS}$ Pulse Width
t_{SC}	60	ns min	$\overline{CS}$ Data Setup Time
t_{HC}	0	ns min	$\overline{CS}$ Data Hold Time
Case B[2]			100ns Pulse on $\overline{CS}$
t_{WB}	60	ns min	$\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SB}	30	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HB}	20	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Hold Time
t_{WD}	70	ns min	$\overline{LDAC}$ Pulse Width
Case C[3]			100ns Pulse on $\overline{CS}$
t_{WS}	70	ns min	$\overline{LDAC}$ & $\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SS}	30	ns min	$\overline{LDAC}$ & $\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HS}	10	ns min	$\overline{LDAC}$ & $\overline{HBE}$, $\overline{LBE}$ Data Hold Time

NOTES
[1]Write strobe applied to $\overline{CS}$ as shown in Figure 20a. Address decoding defines which register(s) data is strobed into (see Figure 1).
[2]Write strobe applied to $\overline{HBE}$ and/or $\overline{LBE}$ as in Figure 19 or applied to $\overline{LDAC}$ separately. DAC base address applied to $\overline{CS}$ (see Figure 1).
[3]Write strobe applied to $\overline{LDAC}$ and either $\overline{HBE}$ or $\overline{LBE}$ for synchronous load of 16-bit DAC register with one of the 8-bit first-rank registers as shown in Figure 20b (see Figure 2).

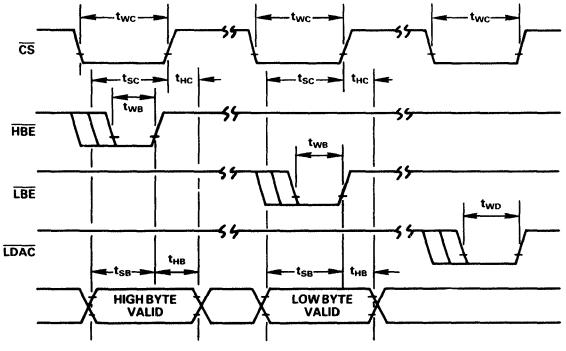


Figure 1. AD569 Timing Diagram

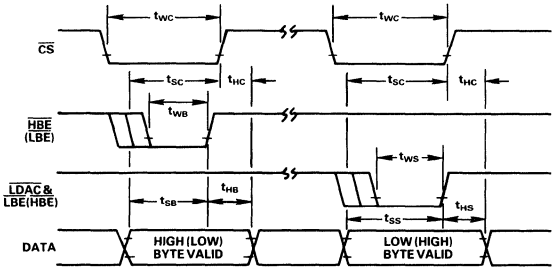


Figure 2. Timing for Synchronous Load of DAC Register

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

$+V_S$ (Pin 1) to GND (Pin 18) . . . . . +18V, −0.3V
$-V_S$ (Pin 28) to GND (Pin 18) . . . . . −18V, +0.3V
$+V_S$ (Pin 1) to $-V_S$ (Pin 28) . . . . . +26.4V, −0.3V
Digital Inputs
(Pins 4-14, 19-27) to GND (Pin 18) . . . . . $+V_S$, −0.3V
$+V_{REF}$ Force (Pin 3) to $+V_{REF}$ Sense (Pin 2) . . . . ±16.5V
$-V_{REF}$ Force (Pin 15) to $-V_{REF}$ Sense (Pin 16) . . . ±16.5V
V_{REF} Force (Pins 3, 15) to GND (Pin 18) . . . . . $\pm V_S$
V_{REF} Sense (Pins 2, 16) to GND (Pin 18) . . . . . $\pm V_S$
V_{OUT} (Pin 17) . . . . . Indefinite Short to GND
Momentary Short to $+V_S$, $-V_S$
Power Dissipation (Any Package) 1000mW
Operating Temperature Range
Commercial Plastic (JN, KN Versions) . . . . . 0 to +70°C
Industrial Ceramic (AD, BD Versions) . . −25°C to +85°C
Extended Ceramic (SD Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

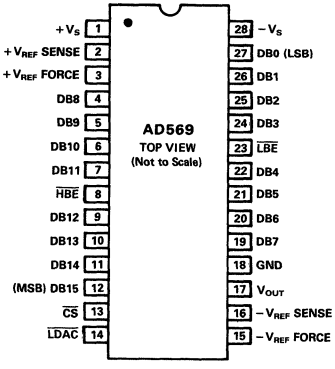
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

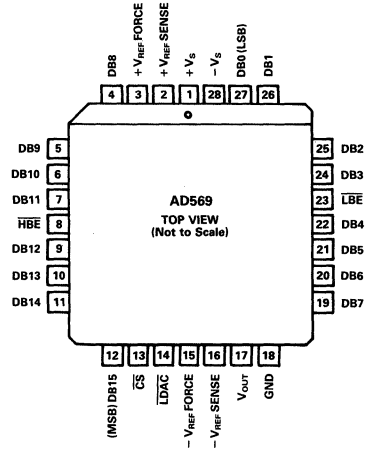
ESD SENSITIVITY

The AD569 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low-energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD569 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

PIN DESIGNATIONS





ORDERING INFORMATION

Integral Nonlinearity		Differential Nonlinearity		Temperature Range and Package Options*		
+25°C	T_{min}–T_{max}	+25°C	T_{min}–T_{max}	Plastic (N-28) 0 to +70°C	Ceramic (D-28) −25°C to +85°	Ceramic (D-28) −55°C to +125°C
±0.04%	±0.04%	±1LSB	±1LSB	AD569JN, JP	AD569AD	AD569SD
±0.024%	±0.024%	±1/2LSB	±1LSB	AD569KN, KP	AD569BD	–

*See Section 14 for package outline information.

FUNCTIONAL DESCRIPTION

The AD569 consists of two resistor strings, each of which is divided into 256 equal segments (see Figure 3). The 8MSBs of the digital input word select one of the 256 segments on the first string. The taps at the top and bottom of the selected segment are connected to the inputs of the two buffer amplifiers A1 and A2. These amplifiers exhibit extremely high CMRR and low bias current, and thus accurately preserve the voltages at the top and bottom of the segment. The buffered voltages from the segment endpoints are applied across the second resistor string, where the 8LSBs of the digital input word select one of the 256 taps. Output amplifier A3 buffers this voltage and delivers it to the output.

Buffer amplifiers A1 and A2 leap-frog up the first string to preserve monotonicity at the segment boundaries. For example, when increasing the digital code from $00FF_H$ to 0100_H, (the first segment boundary), A1 remains connected to the same tap on the first resistor, while A2 jumps over it and is connected to the tap which becomes the top of the next segment. This design guarantees monotonicity even if the amplifiers have offset voltages. In fact, amplifier offset only contributes to integral linearity error.

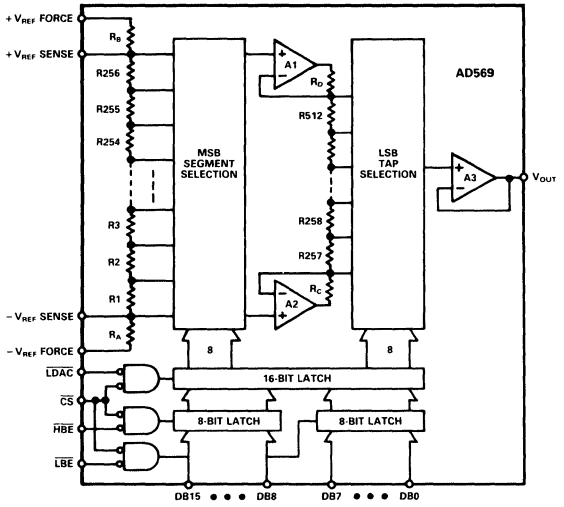


Figure 3. AD569 Block Diagram

CAUTION

It is generally considered good engineering practice to avoid inserting integrated circuits into powered-up sockets. This guideline is especially important with the AD569. An empty, powered-up socket configures external buffer amplifiers in an open-loop mode, forcing their outputs to be at the positive or negative rail. This condition may result in a large current surge between the reference force and sense terminals. This current surge may permanently damage the AD569.

ANALOG CIRCUIT DETAILS

Definitions

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal output (a straight line drawn from 0 to FS-1LSB) for any bit combination. The AD569's linearity is primarily limited by resistor uniformity in the first divider (upper byte of 16-bit input). The plot in Figure 4 shows the AD569's typical linearity error across the entire output range to be within ±0.01% of full scale. At 25°C the maximum linearity error for the AD569JN, AD and SD grades is specified to be ±0.04%, and ±0.024% for the KN and BD versions.

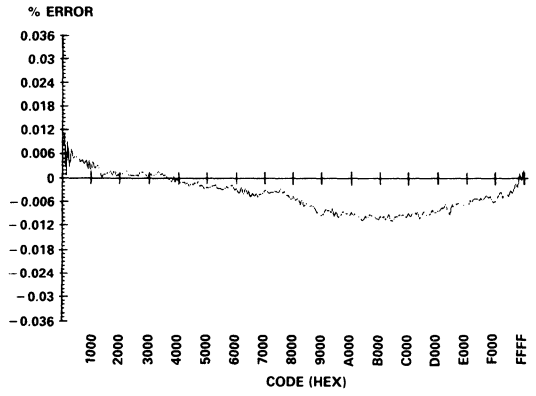


Figure 4. Typical Linearity

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs. All versions of the AD569 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: DNL is the measure of the change in the analog output, normalized to full scale, associated with a 1LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be less than 1LSB over the temperature range of interest. For example, for a ±5V output range, a change of 1LSB in digital input code should result in a 152μV change in the analog output (1LSB = 10V/65,536). If the change is actually 38μV, however, the differential linearity error would be −114μV, or −3/4LSB. By leapfrogging the buffer amplifier taps on the first divider, a typical AD569 keeps DNL within ±38μV (±1/4LSB) around each of the 256 segment boundaries defined by the upper byte of the input word (see Figure 5). Within the second divider, DNL also typically remains less than ±38μV as shown in Figure 6. Since the second divider is independent of absolute voltage, DNL is the same within the rest of the 256 segments.

OFFSET ERROR: The difference between the actual analog output and the ideal output ($-V_{REF}$), with the inputs loaded with all zeros is called the offset error. For the AD569, Unipolar Offset is specified with 0V applied to $-V_{REF}$ and Bipolar Offset is specified with −5V applied to $-V_{REF}$. Either offset is trimmed by adjusting the voltage applied to the $-V_{REF}$ terminals.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal half-scale output of 0.0000V when the inputs are loaded with 8000_H is called the Bipolar Zero Error. For the AD569, it is specified with ±5V applied to the reference terminals.

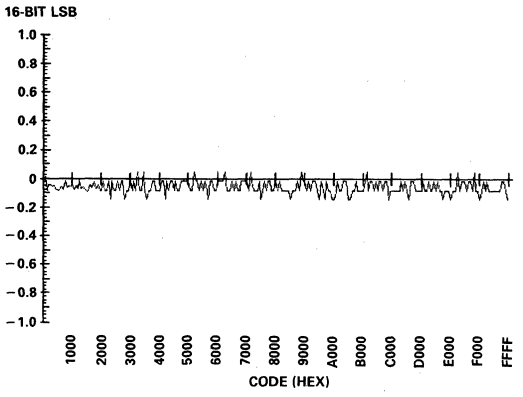
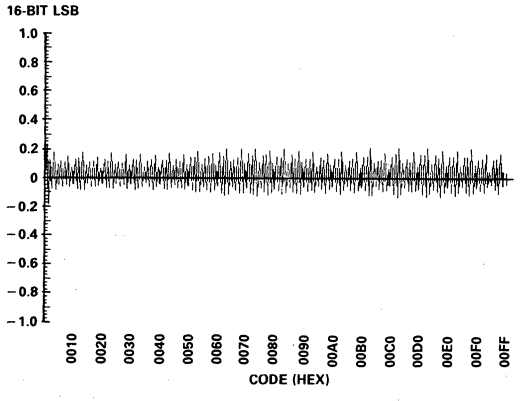
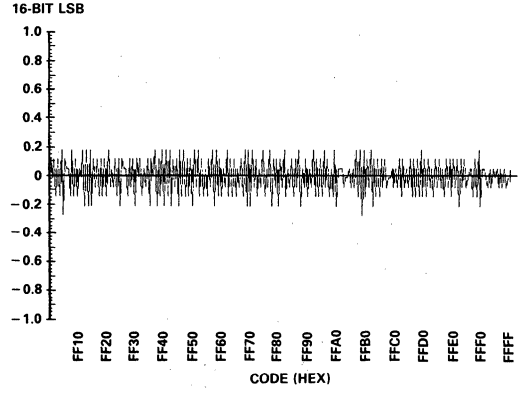


Figure 5. Typical DNL at Segment Boundary Transitions



a. Segment 1



b. Segment 256

Figure 6. Typical DNL Within Segments

MULTIPLYING FEEDTHROUGH ERROR: This is the error due to capacitive feedthrough from the reference to the output with the input registers loaded with all zeroes.

FULL-SCALE ERROR: The AD569's voltage dividing architecture gives rise to a fixed full-scale error which is independent of the reference voltage. This error is trimmed by adjusting the voltage applied to the $+V_{REF}$ terminals.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The charge injected into the analog output when a new input is latched into the DAC register gives rise to the Digital-to-Analog Glitch Impulse. Glitches can be due to either time skews between the input bits or charge injection from the internal switches. Glitch Impulse for the AD569 is mainly due to charge injection, and is measured with the reference connections tied to ground. It is specified as the area of the glitch in nV-secs.

TOTAL ERROR: The worst-case Total Error is the sum of the fixed full-scale and offset errors and the linearity error.

POWER SUPPLY AND REFERENCE VOLTAGE RANGES

The AD569 is specified for operation with ±12 volt power supplies. With ±10% power supply tolerances, the maximum reference voltage range is ±5 volts. Reference voltages up to ±6 volts can be used but linearity will degrade if the supplies approach their lower limits of ±10.8 volts (12 volts – 10%).

If ±12 volt power supplies are unavailable in the system, several alternative schemes may be used to obtain the needed supply voltages. For example, in a system with ±15V supplies, a single Zener diode can be used to reduce one of the supplies to 9 volts with the remaining one left at 15 volts. Figure 7a illustrates this scheme. A 1N753A or equivalent diode is an appropriate choice for the task. Asymmetrical power supplies can be used since the AD569's output is referenced to $-V_{REF}$ only and thus floats relative to logic ground (GND, Pin 18). Assuming a worst-case ±1.5 volt tolerance on both supplies (10% of 15 volts), the maximum reference voltage ranges would be +6 and −2 volts for $+V_S = +15V$ and $-V_S = -9V$, and +2 to −8 volts for $+V_S = 9V$ and $-V_S = -15V$.

Alternately, two 3V Zener diodes or voltage regulators can be used to drop each ±15 volt supply to ±12 volts, respectively. In Figure 7b, 1N746A diodes are a good choice for this task.

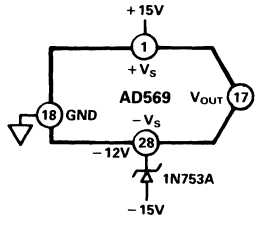
A third method may be used if both ±15 volt and ±5 volt supplies are available. Figure 7c shows this approach. A combination of $+V_S = +15V$ and $-V_S = -5V$ can support a reference range of 0 to 6 volts, while supplies of $+V_S = +5V$ and $-V_S = -15V$ can support a reference range of 0 to −8 volts. Again, 10% power supply tolerances are assumed.

NOTE: Operation with $+V_S = +5V$ alters the input latches' operating conditions causing minimum write pulse widths to extend to 1μs or more. Control signals $\overline{CS}$, $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$ should, therefore, be tied low to render the latches transparent.

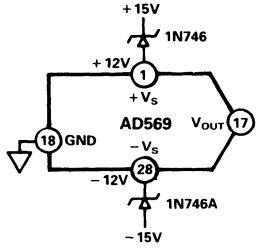
No timing problems exist with operation at $+V_S = 9V$ and $-V_S = -15V$. However, 10% tolerances on these supplies generate a worst-case condition at $-V_S = -16.5V$ and $+V_S = +7.5V$ (assuming $+V_S$ is derived from a +15V supply). Under these conditions, write pulse widths can stretch to 200ns with similar degradation of data setup and hold times. However, ±0.75V tolerances (±5%) yield minimal effects on digital timing with write pulse widths remaining below 100ns.

Finally, Figure 7d illustrates the use of the combination of an AD588 and AD569 in a system with ±15 volt supplies. As shown, the AD588 is connected to provide ±5V to the reference inputs of the AD569. It is doing double-duty by simultaneously regulating the supply voltages for the AD569 through the use of the level shifting zeners and transistors. This scheme utilizes the capability of the outputs of the AD588 to source as well as sink current. Two other benefits are realized by using this approach. The first is that the AD569 is no longer directly connected to the system power supplies. Output sensitivity to variations in those supplies is, therefore, eliminated. The second benefit is

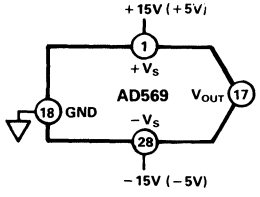
that, should a zener diode fail (a short circuit would be the most likely failure), the supply voltage decreases. This differs from the situation where the diode is used as a series regulator. In that case, a failure would place the unregulated supply voltage on the AD569 terminal.



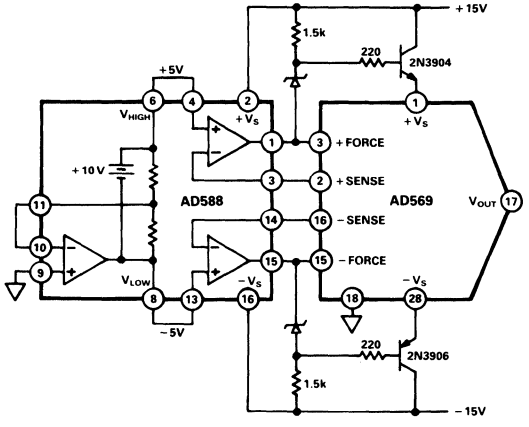
a. Zener Regulates Negative Supply



b. Diodes Regulate Both Supplies



c. Use of ±15V and ±5V Supplies



d. AD588 Produces References and Supply Voltages

Figure 7. Power Supply Options

ANALOG CIRCUIT CONNECTIONS

The AD569 is intended for use in applications where high resolution and stability are critical. Designed as a multiplying D/A converter, the AD569 may be used with a fixed dc reference or an ac reference. V_{REF} may be any voltage or combination of voltages at $+V_{FORCE}$ and $-V_{FORCE}$ that remain within the bounds set for reference voltages as discussed in the power supply range section. Since the AD569 is a multiplying D/A converter, its output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the reference terminal. The transfer function is $V_{OUT} = D \cdot V_{REF}$ where D is the fractional binary value of the digital word applied to the converter using offset-binary coding. Therefore, the output will range from $-V_{REF}$ for a digital input code of all zeros (0000_H) to $+V_{REF}$ for an input code of all ones ($FFFF_H$).

For applications where absolute accuracy is not critical, the simple reference connection in Figure 8 can be used. Using only the reference force inputs, this configuration maintains linearity and 16-bit monotonicity, but introduces small, fixed offset and gain errors. These errors are due to the voltage drops across resistors R_A and R_B shown in Figure 9. With a 10V reference voltage, the gain and offset errors will range from 80 to 100mV. Resistors R_A and R_B were included in the first resistor string to avoid degraded linearity due to uneven current densities at the string's endpoints. Similarly, linearity would degrade if the reference voltage were connected across the reference sense terminals. Note that the resistance between the force and sense terminals cannot be measured with an ohmmeter; the layout of the thin-film resistor string adds approximately 4kΩ of resistance (R_S) at the sense tap.

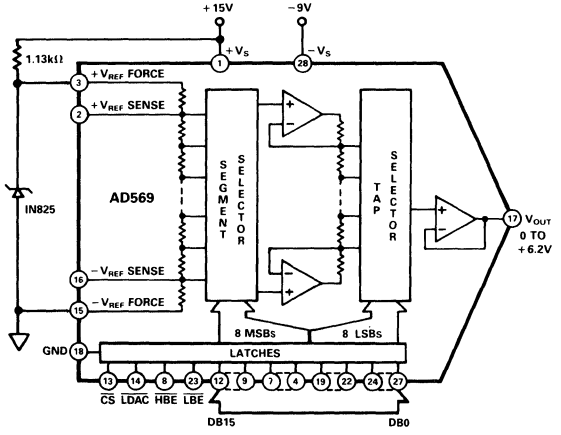


Figure 8. Simple Reference Connection

For those applications in which precision references and high accuracy are critical, buffer amplifiers are used at $+V_{REF}$ and $-V_{REF}$ as shown in Figure 10 to force the voltage across resistors R1 to R256. This insures that any errors induced by currents flowing through the resistances of the package pins, bond wires, aluminum interconnections, as well as R_A and R_B are minimized. Suitable amplifiers are the AD517, AD OP-07, AD OP-27, or the dual amplifier, the AD712. Errors will arise, however, as the buffer amplifiers' bias currents flow through R_S (4kΩ). If the bias currents produce such errors, resistance can be inserted at the noninverting terminal (R_{BC}) of the buffer amplifiers to compensate for the errors.

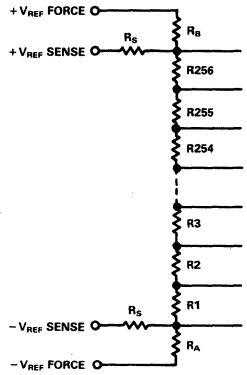


Figure 9. MSB Resistor Divider

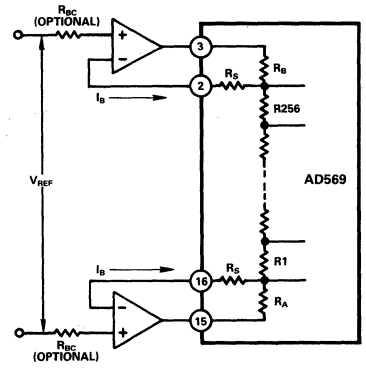


Figure 10. Reference Buffer Amplifier Connections

Figures 11, 12, and 13 show reference configurations for various output ranges. As shown in Figure 11, the pin-programmable AD588 can be connected to provides tracking ±5V outputs with 1-3ppm/°C temperature stability. Buffer amplifiers are included for direct connection to the AD569. The optional gain and balance adjust trimmers allow bipolar offset and full-scale errors to be nulled. In Figure 12, the low-cost AD586 provides +5V reference. A dual op amp, the AD712, buffers the reference input terminals preserving the absolute accuracy of the AD569. The optional noise-reduction capacitor and gain adjust trimmer allow further elimination of errors. The low-cost AD584 offers 2.5V, 5V, 7.5V, and 10V options and can be connected for ±5V tracking outputs as shown in Figure 13. Again, an AD712 is used to buffer the reference input terminals.

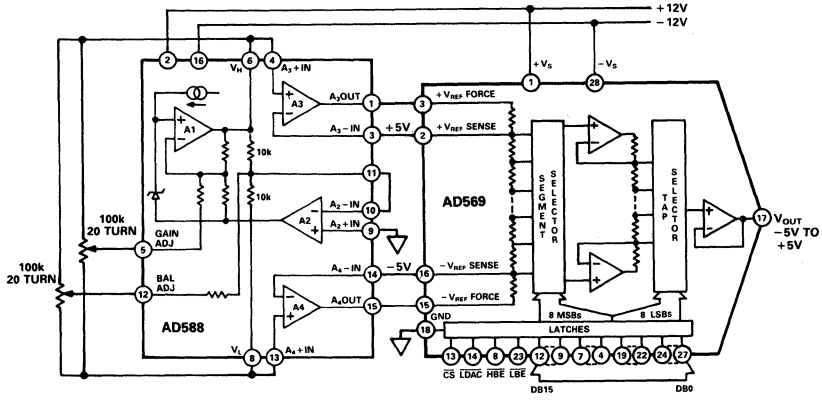


Figure 11. Ultralow Drift ±5V Tracking Reference

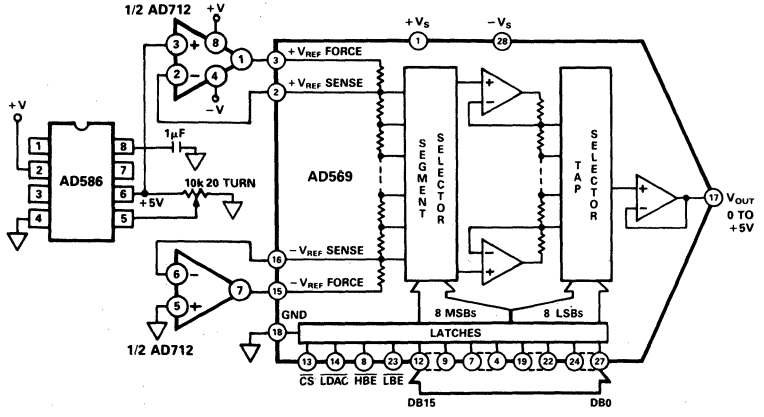


Figure 12. Low-Cost ±5V Reference

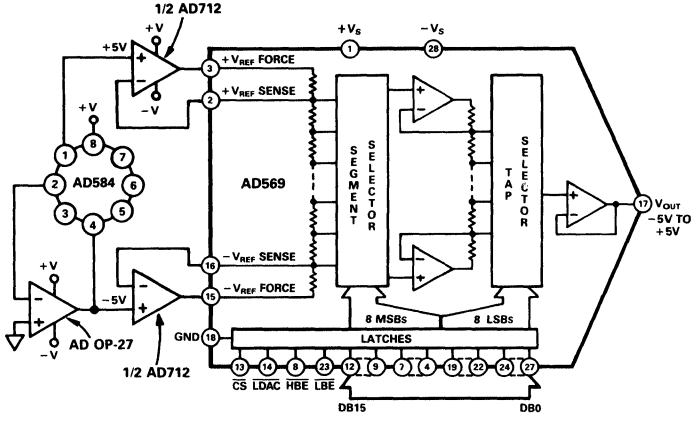
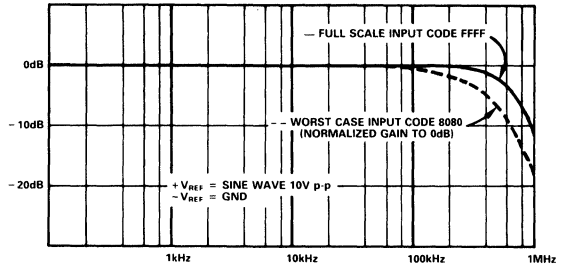


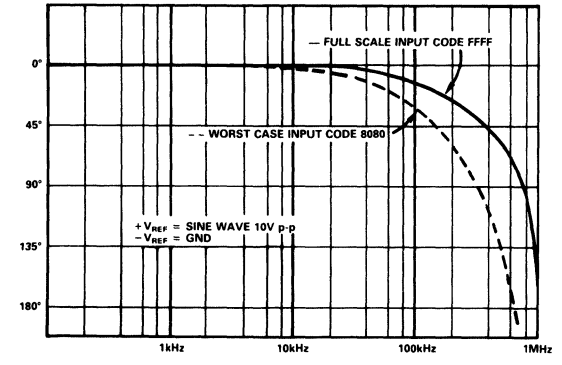
Figure 13. Low-Cost ±5V Tracking Reference

MULTIPLYING PERFORMANCE

Figure 14 illustrates the gain and phase characteristics of the AD569 when operated in the multiplying mode. Full-power bandwidth is shown in Figure 14a and the corresponding phase shift is shown in Figure 14b. Performance is plotted for both a full-scale input of $FFFF_H$ and an input of 8080_H. An input represents worst-case conditions because it places the buffer taps at the midpoints of both dividers. Figure 15 illustrates the AD569's ability to resolve 16-bits (where 1LSB is 96dB below full scale) while keeping the noise floor below −130dB with an ac reference of 1V rms at 200Hz.

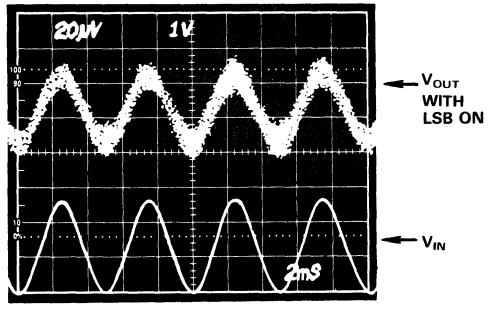


a. Bandwidth

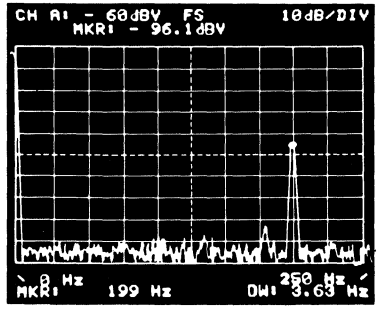


b. Phase Shift

Figure 14. Full Power Multiplying Performance



a. Time Domain



b. Frequency Domain

Figure 15. Multiplying Mode Performance (Input Code 0001_H)

Multiplying feedthrough is due to capacitive coupling between the reference inputs and the output. As shown in Figure 16, under worst-case conditions (hex input code 0000), feedthrough remains below −100dB at ac reference frequencies up to 10kHz.

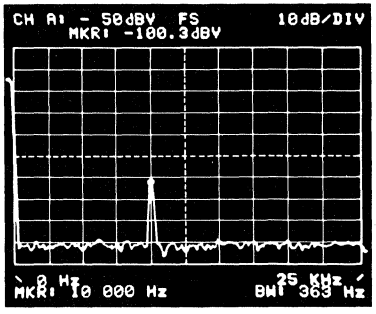


Figure 16. Multiplying Feedthrough

BYPASSING AND GROUNDING RULES

It is generally considered good engineering practice to use bypass capacitors on the device supply voltage pins and to insert small valued resistors in the supply lines to provide a measure of decoupling between various circuits in a system. For the AD569, bypass capacitors of at least 4.7μF and series resistors of 10Ω are recommended. The supply voltage pins should be decoupled to Pin 18.

NOISE

In high-resolution systems, noise is often the limiting factor. A 16-bit DAC with a 10 volt span has an LSB size of 152μV (−96dB). Therefore, the noise floor must remain below this level in the frequency ranges of interest. The AD569's noise spectral density is shown in Figures 17 and 18. The lowband noise spectrum in Figure 17 shows the 1/f corner frequency at 1.2kHz and Figure 18 shows the wideband noise to be below 40nV/$\sqrt{Hz}$.

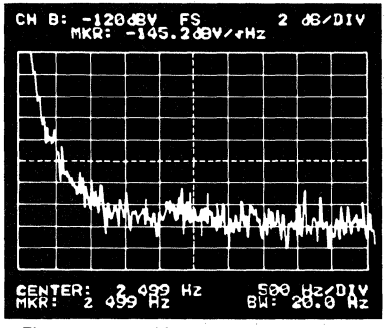


Figure 17. Lowband Noise Spectrum

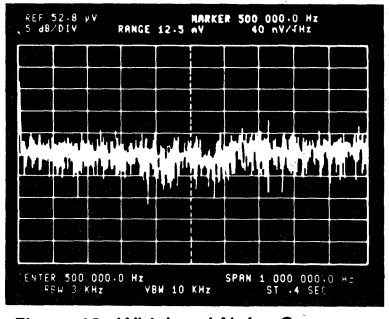


Figure 18. Wideband Noise Spectrum

DIGITAL CIRCUIT CONNECTIONS

The AD569's truth table appears in Table I. The High Byte Enable ($\overline{HBE}$) and Low Byte Enable ($\overline{LBE}$) inputs load the upper and lower bytes of the 16-bit input when Chip Select ($\overline{CS}$) is valid (low). A similar strobe to Load DAC ($\overline{LDAC}$) loads the 16-bit input into the DAC register and completes the DAC update. The DAC register can either be loaded with a separate write cycle or synchronously with either of the 8-bit registers in the first rank. A simultaneous update of several AD569s can be achieved by controlling their $\overline{LDAC}$ inputs with a single control signal.

$\overline{CS}$	$\overline{HBE}$	$\overline{LBE}$	$\overline{LDAC}$	OPERATION
1	X	X	X	No Operation
X	1	1	1	No Operation
0	0	1	1	Enable 8MSBs of First Rank
0	1	0	1	Enable 8LSBs of First Rank
0	1	1	0	Enable 16-Bit DAC Register
0	0	0	0	All Latches Transparent

Table I. AD569 Truth Table

All four control inputs latches are level-triggered and active low. When the DAC register is loaded directly from a bus, the data at the digital inputs will be reflected in the output any time $\overline{CS}$, $\overline{LDAC}$, $\overline{LBE}$ and $\overline{HBE}$ are low. Should this not be the desired case, bring $\overline{LDAC}$ (or $\overline{HBE}$ or $\overline{LBE}$) high before changing the data. Alternately, use a second write cycle to transfer the data to the DAC register or delay the write strobe pulse until the appropriate data is valid. Be sure to observe the appropriate data setup and hold times (see Timing Characteristics).

Whenever possible, the write strobe signal should be applied to $\overline{HBE}$ and $\overline{LBE}$ with the AD569's decoded address applied to $\overline{CS}$. A minimum pulse width of 60ns at $\overline{HBE}$ and $\overline{LBE}$ allows the AD569 to interface to the fastest microprocessors. Actually, data can be latched with narrower pulses, but the data setup and hold times must be lengthened.

16-Bit Microprocessor Interfaces

Since 16-bit microprocessors supply the AD569's complete 16-bit input in one write cycle, the DAC register is often unnecessary. If so, it should be made transparent by grounding $\overline{LDAC}$. The DAC's decoded address should be applied to $\overline{CS}$, with the write strobe applied to $\overline{HBE}$ and $\overline{LBE}$ as shown in the 68000 interface in Figure 19.

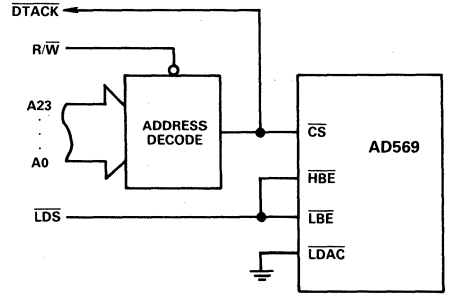
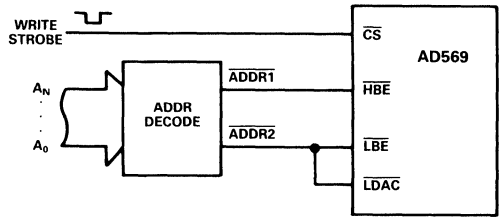
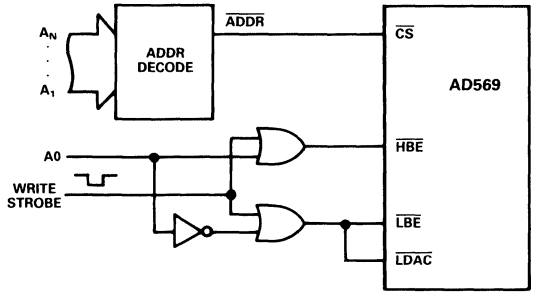


Figure 19. AD569/68000 Interface



a. Simple Interface



b. Fast Interface

Figure 20. 8-Bit Microprocessor Interface

8-Bit Microprocessor Interfaces

Since 8-bit microprocessors require two write cycles to provide the AD569's 16-bit input, the DAC register must be utilized. It is most often loaded as the second byte enters the first rank of latches. This synchronous load method, shown in Figure 20, requires $\overline{LDAC}$ to be tied to either $\overline{LBE}$ or $\overline{HBE}$, depending upon the byte loading sequence. In either case, the propagation delay through the first rank gives rise to longer timing requirements as shown in Figure 2. If the DAC register ($\overline{LDAC}$) is controlled separately using a third write cycle, the minimum write pulse on $\overline{LDAC}$ is 70ns, as shown in Figure 1.

Two basic methods exist for interfacing the AD569 to an 8-bit microprocessor's address and control buses. In either case, at least one address line is needed to differentiate between the upper and lower bytes of the first rank ($\overline{HBE}$ and $\overline{LBE}$). The simplest method involves applying the two addresses directly to $\overline{HBE}$ and $\overline{LBE}$ and strobing the data using $\overline{CS}$ as shown in Figure 20a. However, the minimum pulse width on $\overline{CS}$ is 70ns with a minimum data setup time of 60ns. If operation with a shorter pulse width is required, the base address should be applied to $\overline{CS}$ with an address line gated with the strobe signal to supply the $\overline{HBE}$ and $\overline{LBE}$ inputs (see Figure 20b). However, since the write pulse sees a propagation delay, the data still must remain valid at least 20ns after the rising edge of the delayed write pulse.

OUTPUT SETTLING

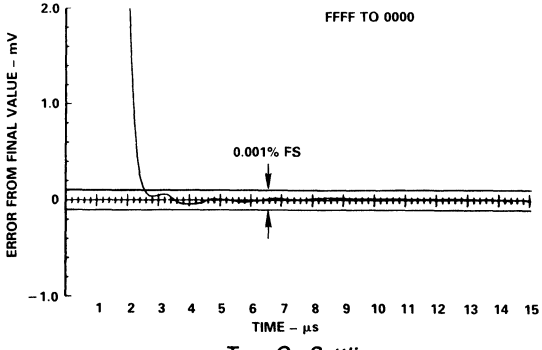
The AD569's output buffer amplifier typically settles to within ±0.001% FS of its final value in 3μs for a 10V step. Figure 21 shows settling for negative and positive full-scale steps with no load applied. Capable of sourcing or sinking 5mA, the output buffer can also drive loads of 1kΩ and 1000pF without loss of stability. Typical settling to 0.001% under these worst-case conditions is 4μs, and is guaranteed to be a maximum of 6μs. The plots of Figure 21 were generated using the settling test procedure developed specifically for the AD569.

Subranging 16-Bit ADC

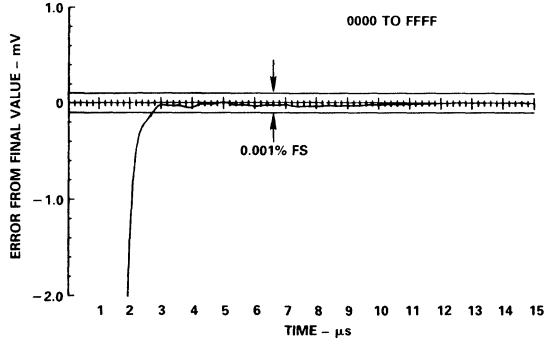
The subranging ADC shown in Figure 22 completes a conversion in less than 20μs, including the sample-hold amplifier's sample time. The sample-hold amplifier is allocated 5μs to settle to 16 bits.

Before the first flash, the analog input signal is routed through the AD630 at a gain of +1. The lower AD7820 quantizes the signal to the 8-bit level within 1.4μs, and the 8-bit result is routed to the AD569 via a digital latch which holds the 8-bit word for the AD569 and the output logic.

The AD569's reference polarity is reversed so that a full-scale output is −5V and zero scale is 0V, thereby subtracting an 8-bit approximation from the original sampled signal. The residue from the analog subtraction is then quantized by the second 8-bit flash conversion to recover the 8LSBs. Even though only the AD569's upper 8MSBs are used, the AD569's accuracy defines the A/D converter's overall accuracy. Any errors are directly reflected in the output.



a. Turn-On Settling



b. Turn-Off Settling

Figure 21. Full-Scale Output Settling

Preceding the second flash, the residue signal must be amplified by a factor of 256. The OP-37 provides a gain of 25.6 and the AD630 provides another gain of 10. In this case, the AD630 acts as a gain element as well as a channel control switch. The second flash conversion yields a 9-bit word. This provides one extra bit of overlap for digital correction of any errors that occurred in the first flash. The correction bit is digitally added to the first flash before the entire 16-bit output is strobed into the output register.

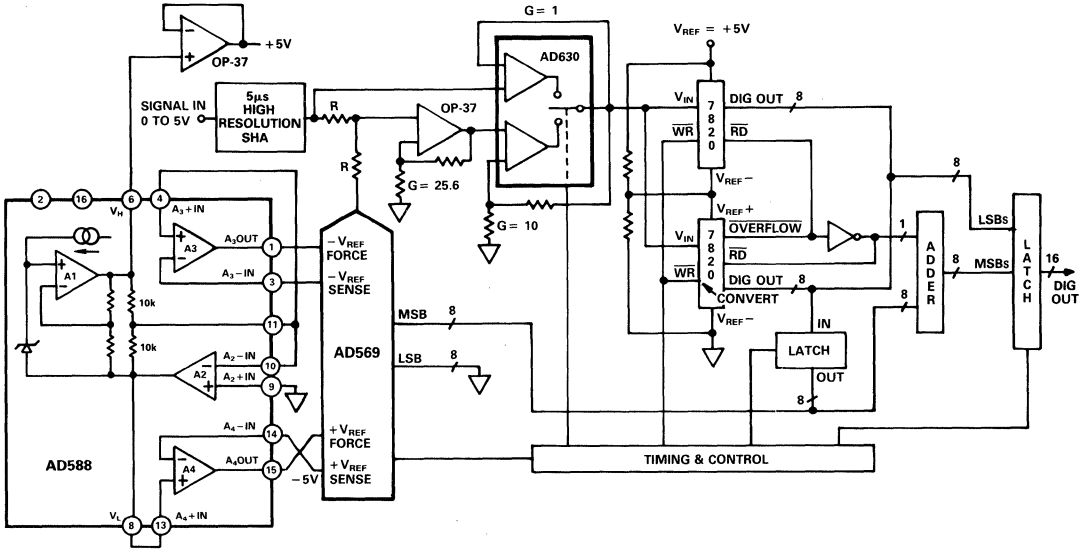


Figure 22. 16-Bit Subranging ADC

ANALOG DEVICES

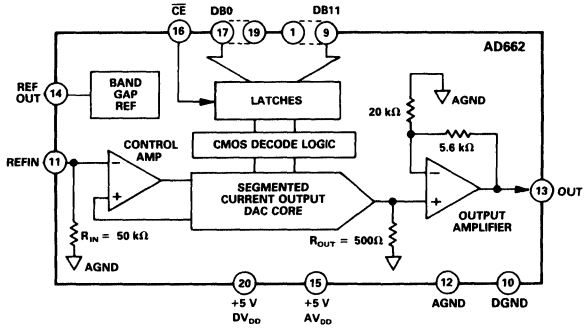
Single Supply 12-Bit DACPORT

AD662

FEATURES

Complete 12-Bit D/A Function
On-Chip Output Amplifier
Internal High Stability Voltage Reference
Single +5 V Operation
Settling Time: 3 μs to 1/2 LSB
Monotonicity Guaranteed Over Temperature
Fast Digital Interface
Low Power Consumption: 55 mW
TTL/5 V CMOS Compatible Logic Inputs
20-Pin Cerdip and Plastic Packages

AD662 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD662 DACPORT™ is a complete 12-bit voltage output DAC specified to operate on a single +5 V power supply. The converter combines 1023 individual current sources and a 2-bit binary weighted DAC, high stability voltage reference, and an on-chip output amplifier to achieve 12-bit resolution and monotonicity over temperature.

Microprocessor compatibility is accomplished with an on-chip data latch, allowing a direct interface between the AD662 and a 16-bit digital bus. The latch responds to write pulses as short as 35 ns, for easy use with the fastest available microprocessors.

Functional completeness of the 12-bit DACPORT provides designers of single supply systems with a complete interface solution that was previously unavailable.

The AD662 is available in two performance grades over commercial, industrial, and military temperature ranges. The device is available in 20-pin plastic and cerdip packages. The AD662J, A, and S grades provide 4 LSB integral nonlinearity (INL), while the K, B, and, T grades provide 2 LSB INL, over temperature.

PRODUCT HIGHLIGHTS

1. The AD662 is a complete voltage output DAC with a voltage reference, an output amplifier, and digital latches on a single chip.
2. Device performance is optimized for single +5 V supply operation.
3. The output amplifier is capable of driving to within 3 mV of ground.
4. The data latch responds to write pulse widths as short as 35 ns, assuring direct interface with the industry's fastest microprocessors.
5. Output settling time is 3 μs to within 1/2 LSB of the final value.
6. Low power consumption of the device, 55 mW, makes it ideal for applications that are power constrained such as portable or battery-operated equipment.

DACPORT is a trademark of Analog Devices, Inc.

SPECIFICATIONS (@ $T_A = T_{min}$ to T_{max}, $DV_{DD} = AV_{DD} = 5$ V, unless otherwise specified)[1]

Parameter	AD662J/A/S Min	AD662J/A/S Typ	AD662J/A/S Max	AD662K/B/T Min	AD662K/B/T Typ	AD662K/B/T Max	Units
RESOLUTION			12			12	Bits
TRANSFER CHARACTERSTICS							
Accuracy							
Integral Nonlinearity	**−4**		**+4**	**−2**		**+2**	LSB
Differential Nonlinearity	**−1**	±1/2	**+1**	**−1**	±1/2	**+1**	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION RANGE						
Gain Error[2]	**−0.25**		**+0.25**	**−0.25**		**+0.25**	% of FS
Zero Error[2]	**−3.2**	±2	**+3.2**	**−3.2**	±2	**+3.2**	mV
TEMPERATURE COEFFICIENT							
Gain Error	**−60**	**±30**	**+60**	**−30**	±15	**+30**	ppm of FS/°C
Zero Error	**−10**		**+10**	**−10**		**+10**	μV/°C
DIGITAL INPUTS							
Logic Levels							
V_{IH}	+2.0		DV_{DD}	+2.0		DV_{DD}	V
V_{IL}	0		+0.8	0		+0.8	V
I_{IH}	**−1**		**+1**	**−1**		**+1**	μA
I_{IL}	**−1**		**+1**	**−1**		**+1**	μA
Data Setup Time t_{DS}	25			25			ns
Data Hold Time t_{DH}	0			0			ns
Write Pulse Width t_{PW}	35			35			ns
ANALOG OUTPUT							
Range	**0**		**+2.56**	**0**		**+2.56**	V
Output Current	−5		+5	−5		+5	mA
Output Impedance							
Source		0.05	0.1		0.05	0.1	Ω
Sink		0.1	0.2		0.1	0.2	Ω
Sink from V_{OUT} <50 mV[2]		10			10		Ω
Short Circuit Current							
to GND			+50			+50	mA
to V_{DD}	−50			−50			mA
SETTLING TIME							
To 0.01%							
(<1/2 LSB, R_L = 1 kΩ, C_L = 470 pF)							
Full Scale Change (0 to FS)		3.0			3.0		μs
FS to Code 40 (25 mV)[2]		3.0			3.0		μs
FS to Code 12 (7.5 mV)[2]		5.5			5.5		μs
FS to Zero[2]		8.6			8.6		μs
LSB Change (Midscale)[2]		2.0			2.0		μs
LSB Change (Not Midscale)[2]		1.0			1.0		μs
REFIN INPUT IMPEDANCE		50			50		kΩ
POWER SUPPLY SENSITIVITY							
PSRR[2]	**−400**	100	**+400**	**−400**	100	**+400**	ppm of FS/V
POWER SUPPLY REQUIREMENTS							
Operating Voltage Range	4.5	5.0	**5.5**	4.5	5.0	**5.5**	V
Supply Current		11	**13.5**		11	**13.5**	mA
Power Consumption		55	68		55	68	mW
TEMPERATURE RANGE							
Specified Range (J, K)	0		70	0		70	°C
Specified Range (A, B)	−40		+85	−40		+85	°C
Specified Range (S, T)	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES
[1]Specified for AV_{DD} tied to DV_{DD}.
[2]This parameter is specified for +25°C operation only.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested at+25°C on all production units at final electrial test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

AV_{DD} and DV_{DD} to AGND and DGND . . . . . −0.3 V to +7 V
Digital Inputs to DGND . . . . . −0.3 V to DV_{DD}+0.3 V
REFIN to AGND . . . . . −0.3 V to AV_{DD}+0.3 V
V_{OUT} to AGND . . . . . −0.3 V to AV_{DD}
REFOUT to AGND . . . . . −0.3 V to AV_{DD}
AV_{DD} to DV_{DD} . . . . . ±1V
AGND to DGND . . . . . −0.3 V to +0.3 V
Power Dissipation . . . . . 500 mW
Storage Temperature Range
N Package (Plastic) . . . . . −25°C to +100°C
Q Package (Cerdip) . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

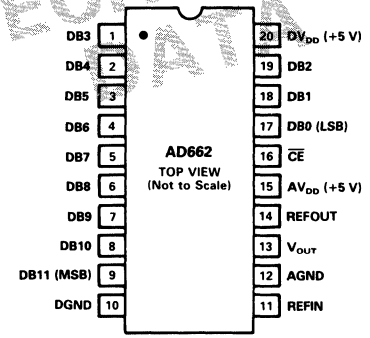
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Binary	Hexadecimal	Decimal	Output (V)
0000 0000 0000	000	0	0
0000 0000 0001	001	1	0.000625
0000 0000 0010	002	2	0.001250
0000 0000 1111	00F	15	0.009375
0000 0001 0000	010	16	0.010000
0000 1111 1111	0FF	255	0.159375
0001 0000 0000	100	256	0.160000
0001 1111 1111	1FF	511	0.319375
0010 0000 0000	200	512	0.320000
0011 1111 1111	3FF	1023	0.639375
0100 0000 0000	400	1024	0.640000
0111 1111 1111	7FF	2047	1.279375
1000 0000 0000	800	2048	1.280000
1100 0000 0000	C00	3072	1.920000
1111 1111 1111	FFF	4095	2.559375

Table I. Output Voltage vs. Input Code

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



AD662 Pin Configuration

ORDERING GUIDE

Model	Package	Temperature Range °C	Linearity Error Max T_{min} to T_{max}	Gain TC Max ppm/°C	Package Options*
AD662JN	Plastic DIP	0 to +70	±4 LSB	60	N-20
AD662KN	Plastic DIP	0 to +70	±2 LSB	30	N-20
AD662AQ	Cerdip	−40 to +85	±4 LSB	60	Q-20
AD662BQ	Cerdip	−40 to +85	±2 LSB	30	Q-20
AD662SQ	Cerdip	−55 to +125	±4 LSB	60	Q-20
AD662TQ	Cerdip	−55 to +125	±2 LSB	30	Q-20

*See Section 14 for package outline information.

Definitions

LINEARITY ERROR (also called INTEGRAL NONLINEARITY or INL): Analog Devices defines linearity error as the maximum deviation of the actual analog output from the ideal output (a straight line drawn from 0 to FS) for any bit combination expressed in multiples or fractions of 1 LSB. The AD662 requires no trimming to achieve 2 LSB (0.048% of FS) maximum INL at +25°C for the K, B, and T versions and 4 LSB for the J, A, and S versions.

DIFFERENTIAL LINEARITY ERROR (also called DIFFERENTIAL NONLINEARITY or DNL): DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code. Monotonic behavior requires that the differential linearity error not exceed 1 LSB in the negative direction.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases.

ZERO ERROR: Zero error is the difference between the actual DAC output with respect to analog ground and zero when all bits are set to 0, expressed in % of FS, mV or LSBs.

GAIN ERROR: The DAC's gain error is the difference between the ideal and actual outputs of FS − 1 LSB, expressed in % of FS, mV or LSB, when all bits are on.

SETTLING TIME: Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. Figure 1 exhibits the AD662's settling time characteristics from zero to full scale. See the section Output Considerations for more details.

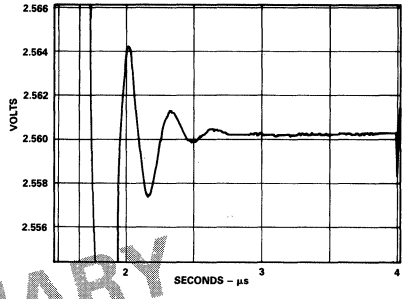


Figure 1. Code 0 to Full Scale Settling Time

Circuit Description

The AD662 consists of four functional blocks as shown in the AD662 functional block diagram on the previous page. These blocks are a 12-bit current output DAC, a bandgap reference, an output amplifier, and digital decode logic. The top 10 bits of the current output DAC are realized by 1023 identical current source segments. An additional 2-bit binary current source DAC creates the lower 2 bits. As the input code increases, the current sources turn on sequentially. The inherently monotonic current output flows from the DAC through the resistor, R_{OUT}, and appears as an unbuffered voltage output at an input terminal of the output amplifier. The internal bandgap reference circuit produces a temperature stable 2.0 V reference when the REFOUT pin is externally connected to the REFIN pin. The unbuffered full scale value is set equal to the voltage input at REFIN by the control amplifier. Therefore, when utilizing the internal 2.0 V reference, the voltage at the top terminal of R_{OUT} swings from 0 to 2.0 V. The output amplifier then takes the unbuffered output from the current-output DAC and amplifies it by a factor of 1.28 to provide a low impedance voltage output which ranges from 0 to 2.56 V.

An advanced 2.0 µm BiCMOS process provides the low power, high speed and high density implementation of the digital interface. This interface consists of TTL/CMOS converters, 12-bit data latch, and decode logic. All digital inputs are TTL compatible. The level triggered latches have an active low $\overline{CE}$ as the control signal, allowing a direct interface with industry standard microprocessors and digital signal processors. Hard-wiring $\overline{CE}$ low renders the latches "transparent" for direct DAC access.

INTERNAL/EXTERNAL REFERENCE

The AD662 has an internal bandgap reference circuit that is laser trimmed to produce a temperature stable 2 V reference when REFIN is externally connected to REFOUT. The full scale trim of the device is performed with the internal reference. The reference is intended only for this purpose and not for driving any external load. To insure the specified performance of the device, when using the internal reference, it is recommended to add an external decoupling capacitor of at least 1 µF as shown in Figure 2.

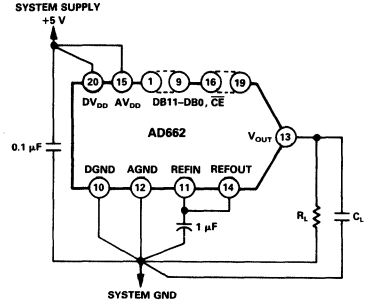


Figure 2. Internal Reference Configuration

The REFIN/REFOUT configuration demonstrates that the AD662 can operate with either the on-chip reference or an external reference. The external reference can be used to set a different full scale value to further improve temperature stability, or to reduce 1/f noise contribution from the reference. A user has to simply apply an external voltage reference to REFIN. REFOUT may be either open or connected to REFIN. When REFOUT is left open, the input impedance at REFIN is the specified value of 50 kΩ, typical. The output impedance of REFOUT is 12 kΩ, typical. Consequently, when REFIN and REFOUT are connected, the input impedance of REFIN becomes 9.0 kΩ, typical. Figure 3 exhibits a scheme to achieve a programmable full scale output between 1.58 V and 2.56 V. It is not recommended to reduce the full scale voltage any further than 1.58 V because the output noise will exceed an LSB level.

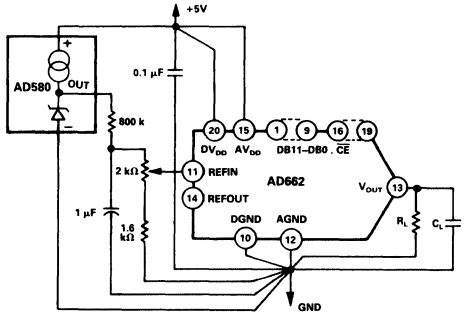


Figure 3. External Reference Configuration

TIMING AND CONTROL

The AD662 has a 12-bit latch that simplifies interface to a 12-bit (or wider) data bus. The latch is controlled by the Chip Enable ($\overline{CE}$) input. If the application does not involve a data bus, wiring $\overline{CE}$ low allows direct operation of the DAC.

The data latch is level triggered and acquires data from the data bus during the time period when $\overline{CE}$ is low. When $\overline{CE}$ goes high, the data is latched into the register and held until $\overline{CE}$ returns low. The minimum time required for the data to be present on the bus before $\overline{CE}$ returns high is called the data setup time (t_{DS}) as seen in Figure 4. The data hold time(t_{DH}) is the amount of time that the data has to remain on the bus after $\overline{CE}$ goes high. The AD662 is specified for t_{DS} = 25 ns and t_{DH} = 0 ns for minimum $\overline{CE}$ pulse width (t_{PW}) of 35 ns, allowing direct interface with the fastest microprocessors and controllers.

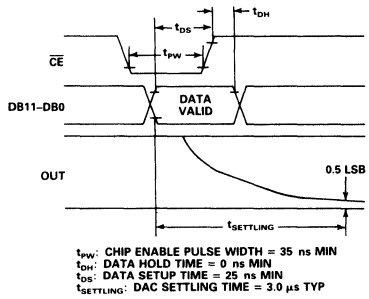


Figure 4. Timing Diagram

OUTPUT CONSIDERATIONS

The AD662 has an internal output amplifier which provides the specified low impedance output. The amplifier drives the output down to the zero offset value from ground when the input code is 000H. The output maintains its specified linearity for all the codes from 000H to FFFH when the output sources up to 5 mA of output current. When the output sinks current for input codes below 048H, however, the output impedance increases up to 10 Ω typical. This output impedance determines the lowest possible output level for a given sink current. The transfer curve will be nonlinear at this level and stay flat for inputs below it. This situtuation is illustrated in Figure 5. For example, the output stays at about 50 mV for input codes between 000H and 050H when the output is sinking 5 mA.

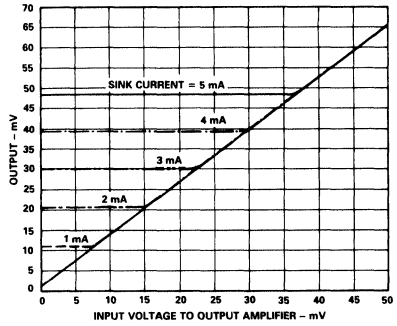


Figure 5. Output Voltage for Sink Current of 0 to 5 mA

The settling time from 0 to full scale is 3 µs. However, the settling time of the DAC from full scale towards 0 will increase for final values below approximately 25 mV (Code 40). For a system which requires 3 µs settling for all the code transitions, it is recommended to disregard the codes below 40 and to refer the output to a pseudoground at 25 mV above AGND. Figure 6 illustrates the settling time for the AD662 from 0 to full scale and then from full scale back to 0. Figures 1 and 7 are enlargements of the respective settling times circled in Figure 6.

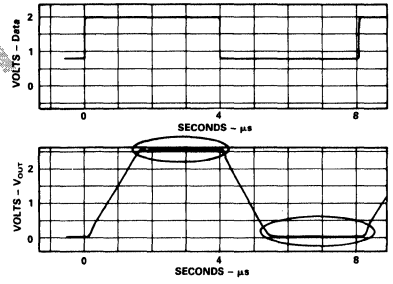


Figure 6. Settling Time

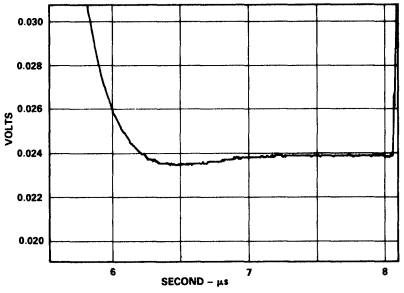


Figure 7. Full Scale to Code 40 Settling Time

When the internal reference is used, it is highly recommended to filter the internal reference output by adding an external capacitor of at least 1 µF from REFIN (= REFOUT) to AGND. Otherwise, noise from the reference will dominate the total output noise and will exceed an LSB level. The total output noise is largest at full scale because the DAC core has the

maximum number of current sources connected to its output. The measured output white noise is 68 nV/$\sqrt{Hz}$. The corner frequency for 1/f noise is approximately 15 kHz. The output amplifier has its −3 dB frequency at about 1 MHz. This data results in a total output noise of about 79 μV rms from 0.1 Hz at full scale. Figure 8 illustrates the output noise versus frequency with a 1 μF cap from REFIN and REFOUT to AGND.

The output of the AD662 is protected against short circuits to ground and the supply. However, short circuits to another 5 V supply through resistances in the 30 Ω to 120 Ω range may cause device damage and should be avoided.

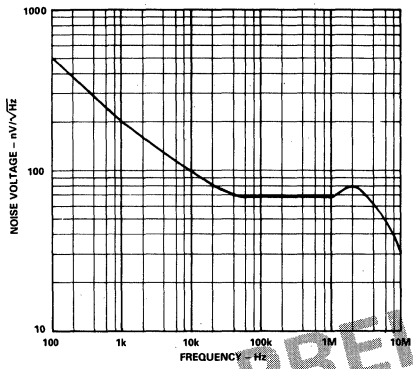


Figure 8. Output Noise vs. Frequency

GROUNDING RULES

The AD662 has two ground connections, digital ground (DGND) at Pin 10 and analog ground (AGND) at Pin 12. The AGND pin is the "high quality" ground reference point for the device. Any external loads or external reference should be referred to this ground. In order to minimize a voltage drop across Pin 12 and the reference point, care should be taken to provide a system reference point as close to Pin 12 as possible. Note that the AD662 typically has 10 mA analog ground current and a 0.1 Ω series resistance between AGND, Pin 12, and the system reference point would result in an additional offset of 1 mV (equivalent to 1.6 LSBs). The digital ground returns current from the digital portion of the device and should be tied to the analog ground at one point, usually the device power ground. This should be as close to the device as possible in order to avoid a differential voltage across these two ground pins. Differential voltage across two ground pins will degrade the accuracy of the device. Figures 2 and 9 illustrate connections for proper operation of the device.

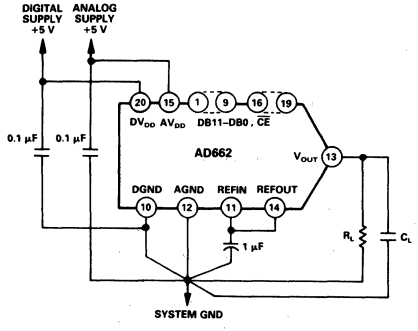


Figure 9. Output Configuration Using Two Supplies

POWER SUPPLY AND DECOUPLING

The AD662 has two power supply pins, digital V_{DD} at Pin 20 and analog V_{DD} at Pin 15. Specified device performance is achieved for a supply voltage between 4.5 V and 5.5 V at both pins. The AD662 is designed to operate from a single power supply, although it has two supply pins. Figure 2 shows this configuration. The two supply pins should be tied at one point to the single system supply and should be decoupled to one system ground point. Figure 10 is the measured PSRR of the output at full scale when the analog and digital V_{DD}s are tied together.

When it is impractical or uneconomical to provide a quiet single system supply, the user can use two system supplies as shown in Figure 9. The analog V_{DD} at Pin 15 should be the "high quality" supply in this case. Decoupling capacitors should be used on both supply pins. They should be located as near as possible to the device. The digital V_{DD} should be bypassed to the digital ground pin and likewise for analog V_{DD} and ground.

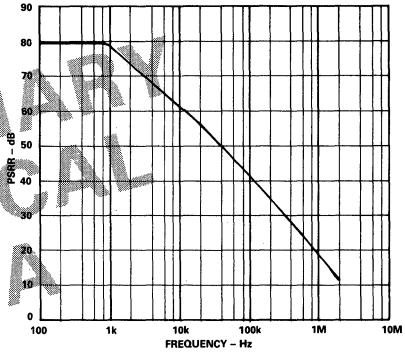


Figure 10. PSRR vs. Frequency

BIPOLAR OPERATION

The AD662 was designed for operation from a single +5 V supply and is capable of providing a unipolar output range. When a negative supply is available in a system, bipolar output ranges can be achieved by properly offsetting and scaling the output. Figure 11 shows an example of this application and Figure 12 is a photo of its settling time characteristics. The precision voltage reference, AD589, provides the offset and determines the bipolar zero level. The BiFET amplifier, AD711, provides the buff-

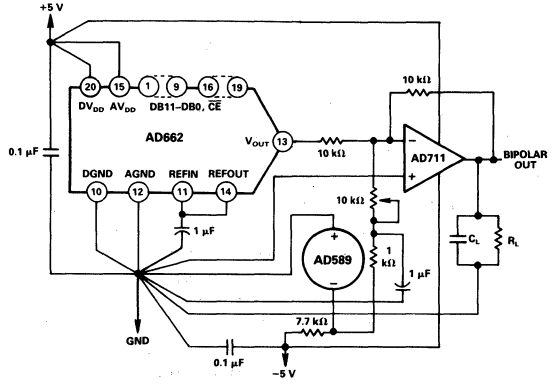


Figure 11. Bipolar Buffered Output ±1.28 V

ered output. In the case of the circuit shown in Figure 11, the bipolar signal range is ±1.28 V. If we adjust the bipolar zero with the 10 kΩ potentiometer to be 0 V, the input code, FFFH, will produce a nominal −1.2794 V and 000H will give +1.28 V.

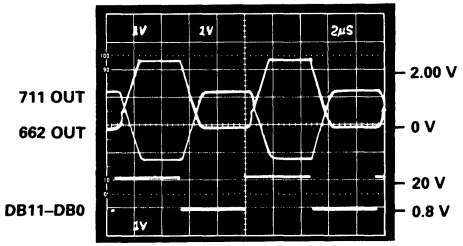


Figure 12. Settling Time Characteristics

Applications

MICROPROCESSOR INTERFACE

The high speed digital interface of the AD662 facilitates its use with a wide variety of microprocessors and microcontrollers. The 12-bit single buffered input register accepts 12-bit parallel load data from processors such as the ADSP-2101, TMS320 series, 80386, and microcontrollers such as the 8096. Several illustrative examples follow.

ADSP-2100 – AD662 INTERFACE

Figure 13 demonstrates the AD662 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digitial signal processor supports the AD662 interface with one hardware wait state.

ADSP-2100A starts a data memory write operation by providing the converter's memory mapped address on the DMA bus. The decoded address generates $\overline{CE}$ for the converter. $\overline{CE}$, together with some glue logic and latches, is used to force the ADSP-2100A into a one cycle wait state by generating DMACK. The write operation to the AD662 is thus started and completed within two processor cycles (160 ns). At clock speeds of 6 MHz, no wait states are necessary.

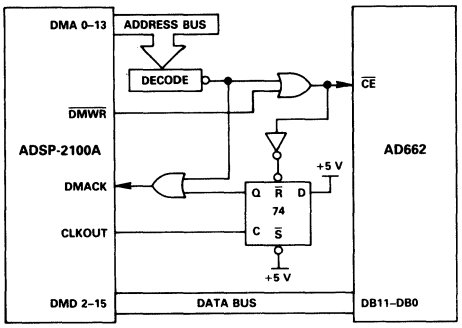


Figure 13. AD662 Interface to ADSP-2100A

ADSP-2101 or ADSP-2102 – AD662 INTERFACE

Figure 14 demonstrates the AD662 interfaced to an ADSP-2101/ADSP-2102. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor supports the AD662 interface with one software wait state.

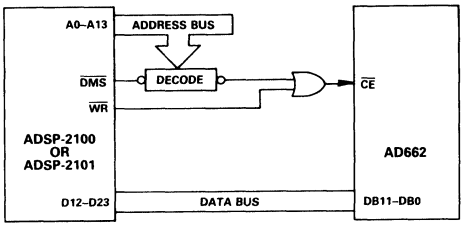


Figure 14. AD662 Interface to ADSP-2101/ADSP-2102

ADSP-2101/ADSP-2102 starts the data memory write operation by providing the converter's memory mapped address on its address bus and by asserting DMS. The decoded address generates $\overline{CE}$ for the converter. This allows the converter's 12-bit input latch to be loaded with the value on the data bus. The write operation to the AD662 is extended by a software wait state and completed within two processor cycles (160 ns).

TMS320C25 – AD662 INTERFACE

Figure 15 illustrates the AD662 interface to a TMS320C25 digital signal processor using the I/O port capability. The $\overline{IS}$ signal distinguishes the I/O address space from the local program/data memory space is used to enable 74F138 decoder. The decoded port address is then gated with the R/$\overline{W}$ and $\overline{STRB}$ to provide the AD662 $\overline{CE}$. As shown, this interface will support a 40 MHz processor without wait states.

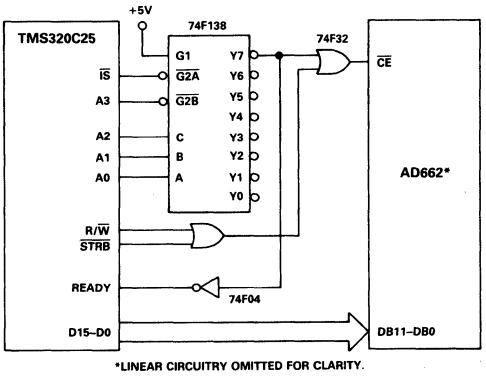


Figure 15. AD662 Interface to TMS32C25

80386 – AD662 INTERFACE

The AD662 interface to the 80386 microprocessor is shown in Figure 16. The processor's $\overline{WR}$ signal is gated with a decoded address to provide $\overline{CE}$ for the AD662. As $\overline{WR}$ returns high, valid data is latched into the DAC.

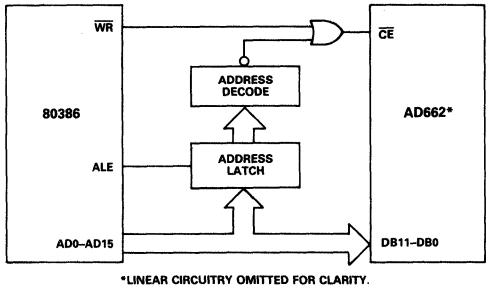


Figure 16. 80386 – AD662 Interface

8096 – AD662 INTERFACE

The circuit of Figure 17 shows the interface between the 8096 16-bit microcontroller and the AD662. In this application, the 8096 external bus width is programmed via the chip configuration register to operate as a standard 16-bit multiplexed address/data bus. A write cycle to the DAC outputs the low order address/data to Port 3 and the high order to Port 4. The ALE signal then latches the address which is decoded and gated with $\overline{WR}$ to control the AD662 $\overline{CE}$. Data is latched into the DAC on the rising edge of $\overline{WR}$ updating the analog output. The cycle is now complete.

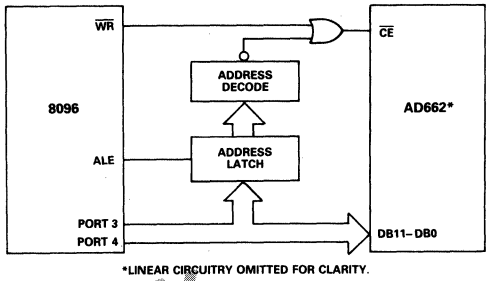


Figure 17. 8096 – AD662 Interface

Bipolar Around +5 V

A popular use for the AD662 can be found in disk drive and other +12 V supply applications. The AD662 can be easily applied to create a bipolar swing around +5 V in a +12 V system by properly offsetting and scaling its output. Figure 18 illustrates a circuit which has an output swing of ±2 V around a bipolar zero point of +5 V. A high precision voltage reference, AD689, creates +8.192 V from the +12 V system supply. This output is resistively divided to produce a temperature-stable bipolar zero point at +5 V. The AD847 acts as a buffer for this voltage and drives the AD662. The output amplifier AD711 provides the proper scaling and offsetting. Gain and bipolar zero of the output are trimmed by 10 kΩ and 5 kΩ potentiometer, respectively. To trim the gain, the output of the AD711 is measured at input code 800H (to be +5V, ideally) first. Then the gain is trimmed at code 000H to achieve an ouput of +2 V plus the measured value at code 800H. The bipolar zero can then be trimmed by adjusting the output to +5 V for an input code of 800H. The 2 pF capacitor cancels a parasitic capacitance at the negative input terminal of AD711 and improves its settling characteristics. This capacitance value should be properly chosen for a given circuit board. The scope photo, Figure 19, shows settling characteristics of this circuit with the outputs of AD662 and AD711 on the same scale.

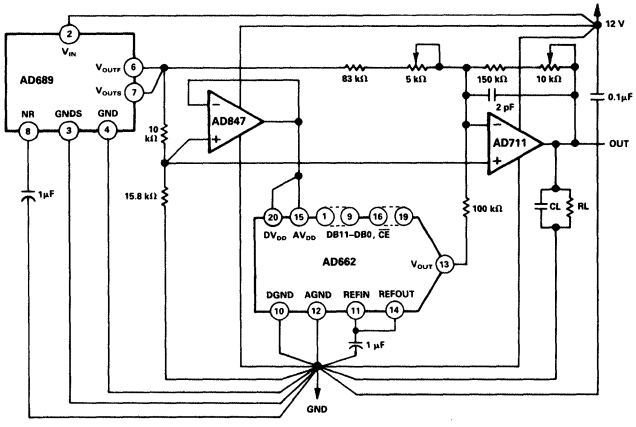


Figure 18. Bipolar Output of ±2 V Around 5 V

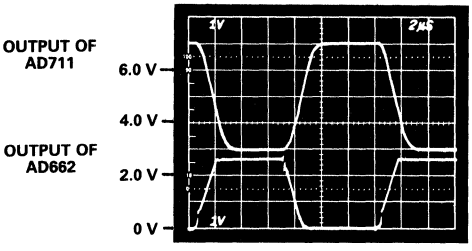


Figure 19. Bipolar Output Settling Characteristics

ANALOG DEVICES

Monolithic 12-Bit Quad DAC

AD664

FEATURES
- Four Complete Voltage Output DACs
- Data Register Readback Feature
- "Reset to Zero" Override
- Multiplying Operation
- Double-Buffered Latches
- Surface Mount and DIP Packages

APPLICATIONS
- Automatic Test Equipment
- Robotics
- Process Control
- Disk Drives
- Instrumentation
- Avionics

PRODUCT DESCRIPTION

The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port.

The I/O port accomodates 4-, 8- or 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response by the outputs to the input data.

The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, with a gain of one or two times the reference voltage. All DACs are operated from a single external reference.

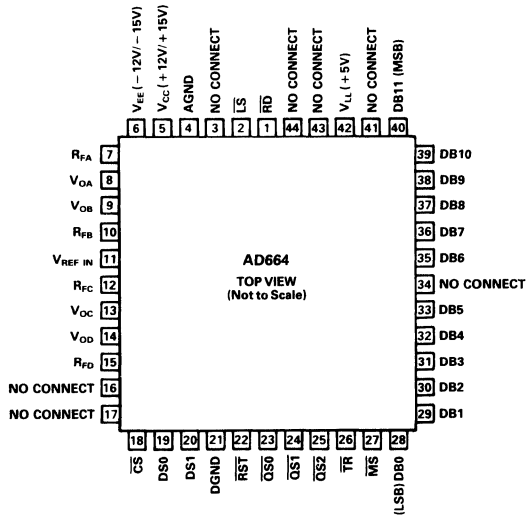
The functional completeness of the AD664 results from the combination of Analog Devices' BiMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

PRODUCT HIGHLIGHTS

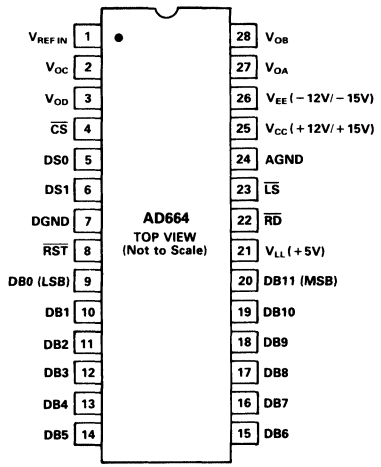
1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit D/A function available.
2. The output range of each DAC is fully and independently programmable.
3. Readback capability allows verification of contents of the internal data registers.
4. The asynchronous RESET control returns all D/A outputs to zero volts.
5. DAC-to-DAC matching performance is specified and tested.

AD664 PIN CONFIGURATIONS

44-Pin Package



28-Pin DIP Package



6. Linearity error is specified to be 1/2LSB at room temperature and 1LSB maximum.
7. DAC performance is guaranteed to be monotonic over the full operating temperature range.
8. Readback buffers have tristate outputs.
9. Multiplying-mode operation allows use with fixed or variable, positive or negative external references.

SPECIFICATIONS (V_{LL} = +5V, V_{CC} = +15V, V_{EE} = −15V, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

Model	AD664BD/BE/TD/TE Min	Typ	Max	Units
RESOLUTION		12	12	Bits
ANALOG OUTPUT				
Voltage Range[1]				
UNI Versions	0		V_{CC} − 2.0*	Volts
BIP Versions	V_{EE} + 2.0*		V_{CC} − 2.0*	Volts
Output Current	5			mA
Load Resistance		2		kΩ
Load Capacitance			500	pF
Short-Circuit Current		25	40	mA
ACCURACY				
Gain Error	−5	±2	5	LSB
Unipolar Offset	−1	±1/4	1	LSB
Bipolar Zero[2]	−2	±1/2	2	LSB
Linearity Error[3]	−1/2	±0.25	1/2	LSB
Linearity T_{min} to T_{max}	−3/4	±1/2	3/4	LSB
Differential Linearity	−1/2		1/2	LSB
Differential Linearity T_{min} to T_{max}	Monotonic @ All Temperatures			
Gain Error Drift				
Unipolar 0 to +10V mode	−10	±5	10	ppm of FSR[4]/°C
Bipolar −5V to +5V mode	−10	±5	10	ppm of FSR/°C
Bipolar −10V to +10V mode	−10	±5	10	ppm of FSR/°C
Unipolar Offset Drift				
Unipolar 0 to +10V mode	−2	±1	2	ppm of FSR/°C
Bipolar Zero Drift				
Bipolar −5V to +5V mode	−10	±5	10	ppm of FSR/°C
Bipolar −10V to +10V mode	−10	±5	10	ppm of FSR/°C
REFERENCE INPUT				
Input Resistance	1.3		2.6	kΩ
Voltage Range[5]	V_{EE} + 2.0*		V_{CC} − 2.0*	Volts
POWER REQUIREMENTS				
V_{LL}	4.5	5.0	5.5	Volts
I_{LL}		0.1	1	mA
V_{CC}/V_{EE}	±11.4		±16.5	Volts
I_{CC}		12	15	mA
I_{EE}		15	19	mA
Total Power		400	525	mW
ANALOG GROUND CURRENT[6]	−600	±400	+600	µA
MATCHING PERFORMANCE				
Gain[7]	−4	±2	4	LSB
Offset[8]	−1	±1/4	1	LSB
Bipolar Zero[9]	−2	±1	2	LSB
Linearity[10]	−1	±1/2	1	LSB
CROSSTALK				
Analog			−90	dB
Digital			−60	dB
DYNAMIC PERFORMANCE (R_L = 2kΩ, C_L = 500pF)				
Settling Time to ±1/2LSB				
Off←Bits→On, GAIN = 1, V_{REF} = 10		8	10	µs
Settling Time to ±1/2LSB				
−10←V_{REF}→10V, GAIN = 1, Bits On		10		µs
Glitch Impulse			500	nV-sec
MULTIPLYING MODE PERFORMANCE				
Reference Feedthrough @ 1kHz		−75		dB
Reference −3dB Bandwidth		70		kHz
POWER SUPPLY GAIN SENSITIVITY				
11.4V←V_{CC}→16.5V		±2	±5	ppm/%
−16.5V←V_{EE}→−11.4V		±2	±5	ppm/%
4.5V←V_{LL}→5.5V		±2	±5	ppm/%
DIGITAL INPUTS				
V_{IH}	2.0			Volts
V_{IL}	0		0.8	Volts
Data Inputs				
I_{IH} @ V_{IN} = V_{LL}	−10	±1	10	µA
I_{IL} @ V_{IN} = DGND	−10	±1	10	µA
$\overline{CS}$/DS0/DS1/$\overline{RST}$/$\overline{RD}$/$\overline{LS}$				
I_{IH} @ V_{IN} = V_{LL}	−10	±1	10	µA
I_{IL} @ V_{IN} = DGND	−10	±1	10	µA

Model	AD664BD/BE/TD/TE Min	Typ	Max	Units
$\overline{MS}/\overline{TR}$[11]				
I_{IH} @ $V_{IN} = V_{LL}$	**−10**	5	**10**	µA
I_{IL} @ V_{IN} = DGND	**−150**	−85	**0**	µA
$\overline{QS0}/\overline{QS1}/\overline{QS2}$[11]				
I_{IH} @ $V_{IN} = V_{LL}$	**−10**	70	**120**	µA
I_{IL} @ V_{IN} = DGND	**−10**	±1	**10**	µA
DIGITAL OUTPUTS				
V_{OL}@1.6mA Sink			**0.4**	Volts
V_{OH}@0.5mA Source	**2.4**			Volts
DIGITAL TIMING (V_{IN} = 0.8, 2.4V)[12]				
Data Input Mode (Figure 10)				
$\overline{CS}$ Pulse Width t_{CW}	80			ns
Data Setup t_{DS}	0			ns
Data Hold t_{DH}	100			ns
Address Setup t_{AS}	0			ns
Address Hold t_{AH}	30			ns
$\overline{LS}$ Setup t_{LS}	0			ns
$\overline{LS}$ Hold t_{LH}	30			ns
Data Input Mode (Figure 9)				
Data Setup t_{DS}	0			ns
Data Hold t_{DH}	0			ns
$\overline{LS}$ Width t_{LW}	80			ns
$\overline{LS}$ Setup t_{LS}	0			ns
$\overline{CS}$ Hold t_{CH}	50			ns
Address Setup t_{AS}	0			ns
Address Hold t_{AH}	30			ns
Mode Select (Figure 16)				
$\overline{LS}$ Setup t_{LS}	20			ns
Address Setup t_{AS}	0			ns
Data Setup t_{DS}	0			ns
$\overline{LS}$ Width t_{LW}	80			ns
$\overline{CS}$ Hold t_{CH}	260			ns
Data Hold t_{DH}	0			ns
$\overline{MS}$ Hold t_{MH}	0			ns
Mode Select (Figure 17)				
$\overline{MS}$ Setup t_{MS}	20			ns
$\overline{MS}$ Hold t_{MH}	0			ns
$\overline{LS}$ Setup t_{LS}	0			ns
Data Setup t_{DS}	0			ns
$\overline{CS}$ Width t_W	80			ns
$\overline{LS}$ Hold t_{LH}	85			ns
Data Hold t_{DH}	100			ns
Readback Mode (Figures 20, 21)				
Address Setup t_{AS}	20			ns
Address Hold t_{AH}	30			ns
$\overline{RD}$ Setup t_{RS}	20			ns
$\overline{RD}$ Hold t_{RH}	30			ns
$\overline{MS}$ Setup t_{MS}	20			ns
$\overline{MS}$ Hold t_{MH}	30			ns
Data Access t_{DV}			240	ns
Data Release t_{DF}			75	ns
Address Hold t_{AH}	0			ns
Asynchronous Reset (Figure 23)				
Reset Width t_W	90			ns
TEMPERATURE RANGE				
KN/KP	**0**		**+70**	°C
BD/BE	**−40**		**+85**	°C
TD/TE	**−55**		**+125**	°C

NOTES
[1]A minimum power supply of ±12.0V is required for 0 to +10V and ±10V operation.
A minimum power supply of ±11.4V is required for −5V to +5V operation.
[2]Bipolar zero error is the difference from the ideal output (0 volts) and the actual output voltage with code 100 000 000 000 applied to the inputs.
[3]Linearity error is defined as the maximum deviation of the actual DAC output from the ideal output (a straight line drawn from 0 to F.S. −1LSB)
[4]FSR means Full-Scale Range and is 20V for ±10V range and 10V for ±5V range.
[5]A minimum power supply of ±12.0V is required for a 10V reference voltage.
[6]Analog Ground Current is input code dependent.
[7]Gain error matching is the largest difference in gain error between any two DACs in one package.
[8]Offset error matching is the largest difference in offset error between any two DACs in one package.
[9]Bipolar zero error matching is the largest difference in bipolar zero error between any two DACs in one package.
[10]Linearity error matching is the difference in the worst case linearity error betweeen any two DACs in one package.
[11]44-pin versions only.
[12]Timing specifications are relative to $\overline{CS}$.
*For V_{CC}<13V and V_{EE}<−13V. Voltage not to exceed 11V maximum.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades except where noted)

V_{LL} to DGND	0 to +7V
V_{CC} to DGND	0 to +18V
V_{EE} to DGND	−18V to 0V
Soldering	+300°C, 10sec
Power Dissipation	1000mW
AGND to DGND	−1V to +1V
Reference Input	−11V to +11V
V_{CC} to V_{EE}	0 to +36V
Digital Inputs	−0.3V to +7V
Analog Outputs	Indefinite Shorts to V_{CC}, V_{LL}, V_{EE} and GND

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

AD664 ORDERING GUIDE[1]

Model	Output Range	Temperature Range	Gain Error	Linearity Error	Package Options[2]
AD664BD-UNI	0 to V_{REF}	Ind	±5LSB	±0.5LSB	D-28
AD664BD-BIP	$-V_{REF}$ to V_{REF}	Ind	±5LSB	±0.5LSB	D-28
AD664TD-UNI/883B[3]	0 to V_{REF}	Mil	±5LSB	±0.5LSB	D-28
AD664TD-BIP/883B[3]	$-V_{REF}$ to V_{REF}	Mil	±5LSB	±0.5LSB	D-28
AD664BE	Programmable	Ind	±5LSB	±0.5LSB	E-44A
AD664TE/883B[3]	Programmable	Mil	±5LSB	±0.5LSB	E-44A

NOTES
[1]AD664KN and AD664KP commercial devices to be available soon.
[2]See Section 14 for package outline information.
[3]Consult Military Products Databook for complete specifications.

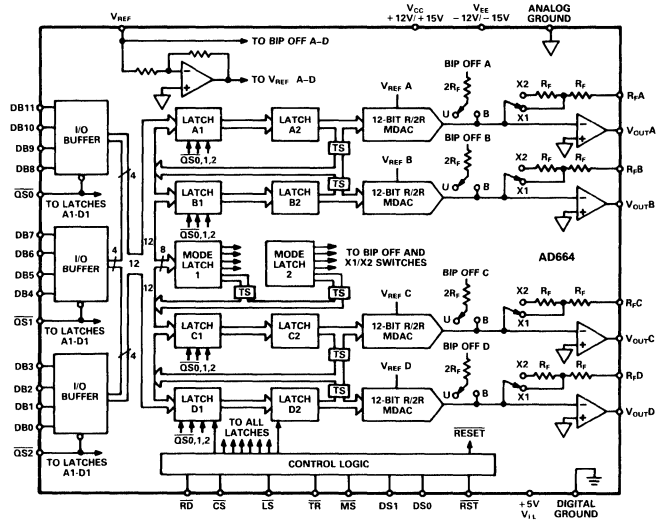


Figure 1a. 44-Pin Block Diagram

FUNCTIONAL DESCRIPTION

The AD664 combines four complete 12-bit voltage output D/A converters with a fast, flexible digital input/output port on one monolithic chip. It is available in two forms, a 44-pin version shown in Figure 1a and a 28-pin version shown in Figure 1b.

44-Pin Versions

Each DAC offers flexibility, accuracy and good dynamic performance. The R-2R structure is fabricated from thin-film resistors which are laser-trimmed to achieve 1/2LSB linearity and guaranteed monotonicity. The output amplifier combines the best features of the bipolar and MOS devices to achieve good dynamic performance and low offset. Settling time is under 10μs and each output can drive a 5mA, 500pF load. Short-circuit protection allows indefinite shorts to V_{LL}, V_{CC}, V_{EE} and GND. The output and span resistor pins are available separately. This feature allows a user to insert current-boosting elements to increase the drive capability of the system, as well as to overcome parasitics.

Digital circuitry is implemented in CMOS logic. The fast, low power, digital interface allows the AD664 to be interfaced with most microprocessors. Through this interface, the wide variety of features on each chip may be accessed. For example, the input data for each DAC is programmed by way of 4-, 8-, 12- or 16-bit words. The double-buffered input structure of this latch allows all four DACs to be updated simultaneously. A readback feature allows the internal registers to be read back through the same digital port, as either 4-, 8- or 12-bit words. When disabled, the readback drivers are placed in a high impedance (tristate) mode. A TRANSPARENT mode allows the input data to pass straight through both ranks of input registers and appear at the DAC with a minimum of delay. One D/A may be placed in the transparent mode at a time, or all four may be made transparent at once. The MODE SELECT feature allows the output range and mode of the DACs to be selected via the data bus inputs. An internal mode select register stores the selections. This register may also be read back to check its contents. A RESET-TO-ZERO feature allows all DACs to be reset to 0 volts out by strobing a single pin.

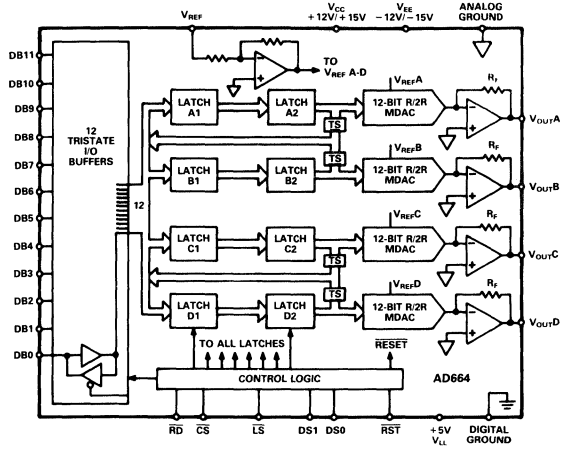


Figure 1b. 28-Pin Block Diagram

28-Pin Versions

The 28-pin versions are dedicated versions of the 44-pin AD664. Each offers a reduced set of features from those offered in the 44-pin version. This accommodates the reduced number of package pins available. Data is written and read with 12-bit words only. Output range and mode select functions are also not available in 28-pin versions. As an alternative, users specify either the UNI (unipolar, 0 to V_{REF}) models or the BIP (bipolar, $-V_{REF}$ to V_{REF}) models depending on the application requirements. Finally, the transparent mode is not available on the 28-pin versions.

	Mode = UNI	Mode = BIP
Gain = 1	000000000000 = 0V 100000000000 = $V_{REF}/2$ 111111111111 = V_{REF} − 1LSB	000000000000 = $-V_{REF}/2$ 100000000000 = 0V 111111111111 = $V_{REF}/2$ − 1LSB
Gain = 2	000000000000 = 0V 100000000000 = V_{REF} 111111111111 = $2 \times V_{REF}$ − 1LSB	000000000000 = $-V_{REF}$ 100000000000 = 0V 111111111111 = $+V_{REF}$ − 1LSB

Table I. Transfer Functions

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS − 1LSB) for any bit conbination. This is also referred to as relative accuracy. The AD664 is laser-trimmed to typically maintain linearity errors at less than ± 1/4LSB.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD664 are monotonic over their full operating temperature range.

DIFFERENTIAL LINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at 25°C as well as over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10V full-scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (V_{REF} = 10V, Gain = 1, 1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be −1.83mV, or −3/4LSB.

GAIN ERROR: DAC gain error is a measure of the difference between the output span of an ideal DAC and an actual device.

UNIPOLAR OFFSET ERROR: Unipolar offset error is the difference between the ideal output (0V) and the actual output of a DAC when the input is loaded with all "0s" and the MODE is unipolar.

BIPOLAR ZERO ERROR: Bipolar zero error is the difference between the ideal output (0V) and the actual output of a DAC when the input code is loaded with the MSB = "1" and the rest of the bits = "0" and the MODE is bipolar.

SETTLING TIME: Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

CROSSTALK: Crosstalk is the change in an output caused by a change in one or more of the other outputs. It is due to capacitive and thermal coupling between outputs.

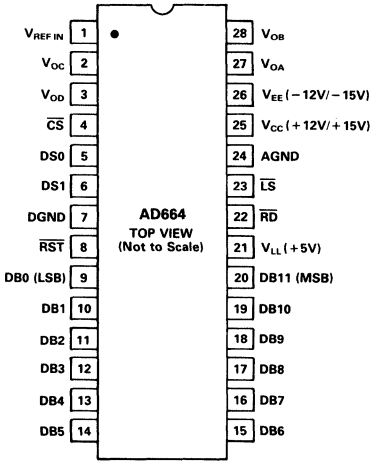
REFERENCE FEEDTHROUGH: The portion of an ac reference signal that appears at an output when all input bits are low. Feedthrough is due to capacitive coupling between the reference input and the output. It is specified in decibels at a particular frequency.

REFERENCE 3dB BANDWIDTH: The frequency of the ac reference input signal at which the amplitude of the full-scale output response falls 3dB from the ideal response.

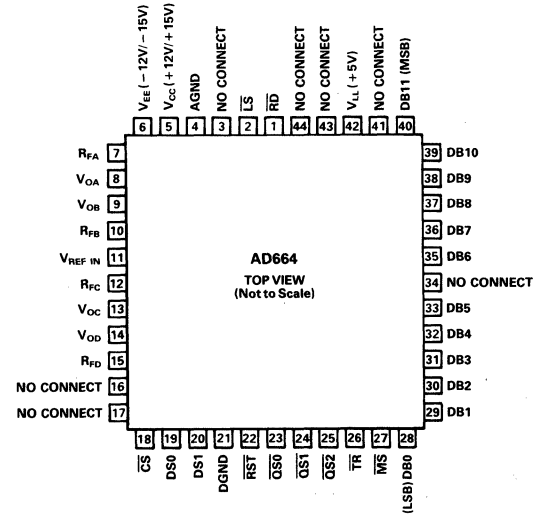
GLITCH IMPULSE: Glitch impulse is an undesired output voltage transient caused by asymmetrical switching times in the switches of a DAC. These transients are specified by their net area (in nV-sec) of the voltage vs. time characteristic.

PIN CONFIGURATIONS

28-Pin DIP Package



44-Pin Package



ANALOG CIRCUIT CONSIDERATIONS

Grounding Recommendations

The AD664 has two pins, designated ANALOG and DIGITAL ground. The analog ground pin is the "high quality" ground reference point for the device. A unique internal design has resulted in low analog ground current. This greatly simplifies management of ground current and the associated induced voltage drops. The analog ground pin should be connected to the analog ground point in the system. The external reference and any external loads should also be returned to analog ground.

The digital ground pin should be connected to the digital ground point in the circuit. This pin returns current from the logic portions of the AD664 circuitry to ground.

Analog and digital grounds should be connected at one point in the system. If there is a possibility that this connection be broken or otherwise disconnected, then two diodes should be connected between the analog and digital ground pins of the AD664 to limit the maximum ground voltage difference.

Power Supplies and Decoupling

The AD664 requires three power supplies for proper operation. V_{LL} powers the logic portions of the device and requires +5 volts. V_{CC} and V_{EE} power the remaining portions of the circuitry and require +12V to +15V and −12V to −15V, respectively. V_{CC} and V_{EE} must also be a minimum of two volts greater then the maximum reference and output voltages anticipated.

Decoupling capacitors should be used on all power supply pins. Good engineering practice dictates that the bypass capacitors be located as near as possible to the package pins. V_{LL} should be bypassed to digital ground. V_{CC} and V_{EE} should be decoupled to analog ground.

Driving the Reference Input

The reference input of the AD664 can have an impedance as low as 1.3kΩ. Therefore, the external reference voltage must be able to source up to 7.7mA of load current. Suitable choices include the 5V AD586, the 10V AD587 and the 8.192V AD689.

The architecture of the AD664 derives an inverted version of the reference voltage for some portions of the internal circuitry. This means that the power supplies must be at least 2V greater than both the external reference and the inverted external reference.

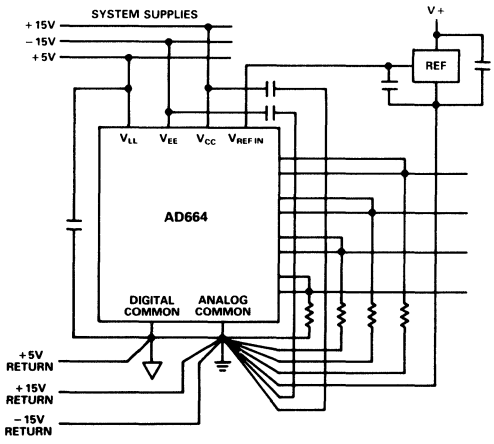


Figure 2. Recommended Circuit Schematic

Output Considerations

Each DAC output can source or sink 5mA of current to an external load. Short-circuit protection limits load current to a maximum load current of 40mA. Load capacitance of up to 500pF can be accomodated with no effect on stability. Should an application require additional output current, a current boosting element can be inserted into the output loop with no sacrifice in accuracy. Figure 3 details this method.

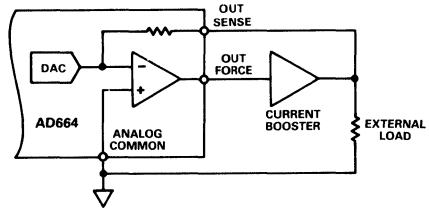


Figure 3. Current-Boosting Scheme

AD664 output voltage settling time is 10μs maximum. Figure 4 shows the output voltage settling time with a fixed 10V reference, gain = 1 and all bits switched from 1 to 0.

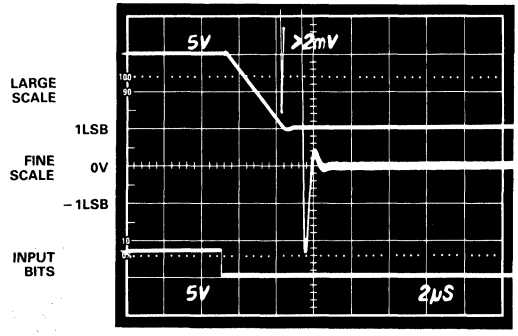


Figure 4. Settling Time; All Bits Switched from On to Off

Alternately, Figure 5 shows the settling characteristics when the reference is switched and the input bits remain fixed. In this case, all bits are "on", the gain is 1 and the reference is switched from −5V to +5V.

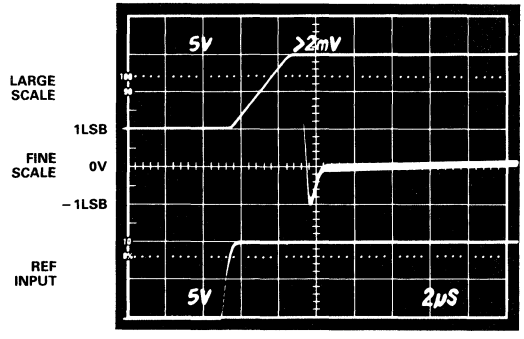


Figure 5. Settling Time; Input Bits Fixed, Reference Switched

Multiplying Mode Performance
Figure 6 illustrates the typical open-loop gain and phase performance of the output amplifiers of the AD664.

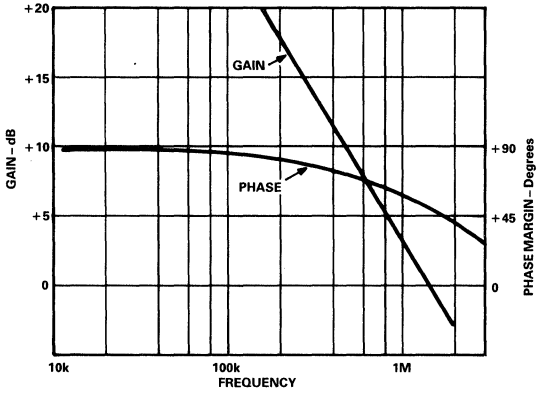


Figure 6. Gain and Phase Performance of AD664 Outputs

Crosstalk
Crosstalk is a spurious signal on one DAC output caused by a change in the output of one or more of the other DACs. Crosstalk can be induced by capacitive, thermal or load current induced feedthrough. Figure 7 shows typical crosstalk. DAC B is set to output 0 volts. The outputs of DAC A, C and D switch 2kΩ loads from 10V to 0V. The first disturbance in the output of DAC B is caused by digital feedthrough from the input data lows. The second disturbance is caused by analog feedthrough from the other DAC outputs.

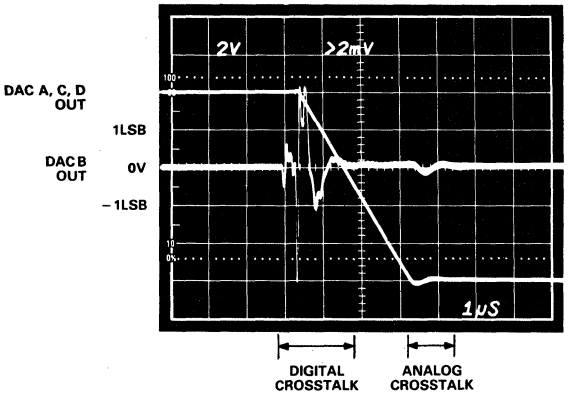


Figure 7. Output Crosstalk

Output Noise
Wideband output noise is shown in Figure 8. This measurement was made with a 7MHz noise bandwidth, gain = 1 and all bits on. The total rms noise is approximately one fifth the visual peak-to-peak noise.

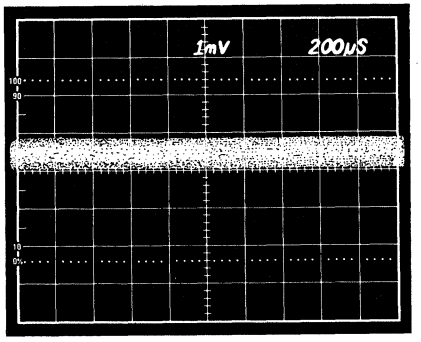


Figure 8. Typical Output Noise

As Table II shows, the AD664 makes a wide variety of operating modes available to the user. These modes are accessed or programmed through the high-speed digital port of the quad DAC. On-board registers program and store the DAC input codes and the DAC operating mode data. All registers are double-buffered to allow for simultaneous updating of all outputs. Register data may be read back to verify the respective contents. The digital port also allows transparent operation. Data from the input pins can be sent directly through both ranks of latches to the DAC.

Partial address decoding is performed by the DS0, DS1, $\overline{QS0}$, $\overline{QS1}$ and $\overline{QS2}$ address bits.

The $\overline{RST}$ pin provides a simple method to reset all output voltages to zero. Its advantages are speed and low software overhead.

INPUT DATA
In general, two types of data will be input to the registers of the AD664, input code data and mode select data. Input code data sets the DAC inputs while the mode select data sets the gain and range of each DAC.

The versatile I/O port of the AD664 allows many different types of data input schemes. For example, the input code for just one of the DACs may be loaded and the output may or may not be updated. Or, the input codes for all four DACs may be written, and the outputs may or may not be updated.

The same applies for MODE SELECTION. The mode of just one or many of the DACs may be rewritten and the user can choose to immediately update the outputs or wait until a later time to transfer the mode information to the outputs.

A user may also write both input code and mode information into their respective first ranks and then update all second ranks at once.

Finally, transparent operation allows data to be transferred from the inputs to the outputs. This feature is useful, for example, in a situation where one of the DACs is used in an A/D converter. The SAR register could be connected directly to a DAC by using the transparent mode of operation. Another use for this feature would be during system calibration where the endpoints of the transfer function of each DAC would be measured. For example, if the full-scale voltages of each DAC were to be measured, then by making all four DACs transparent and putting all "1s" on the input port, all four DACs would be at full-scale. This requires far less software overhead than loading each register individually.

The following sections detail the timing requirements for various data loading schemes.

Function	DS1,DS0	$\overline{LS}$	$\overline{MS}$	$\overline{TR}$	$\overline{QS0}$, $\overline{1}$, $\overline{2^1}$	$\overline{RD}$	$\overline{CS}$	$\overline{RST}$
Load 1st Rank (data)								
DACA	00	0	1	1	Select Quad	1	1→0	1
DACB	01	0	1	1	Select Quad	1	1→0	1
DACC	10	0	1	1	Select Quad	1	1→0	1
DACD	11	0	1	1	Select Quad	1	1→0	1
Load 2nd Rank (data)	XX	1	1	1	XXX	1	1→0	1
Readback 2nd Rank (data)	Select D/A	X	1	1	Select Quad	0	1→0	1
Reset	XX	X	X	X	XXX	X	X	0
Transparent[1]								
All DACs	XX	1	1	0	000	1	1→0	1
DACA	00	0	1	0	000	1	1→0	1
DACB	01	0	1	0	000	1	1→0	1
DACC	10	0	1	0	000	1	1→0	1
DACD	11	0	1	0	000	1	1→0	1
Mode Select[1,2]								
1st Rank	XX	0	0	1	00X	1	1→0	1
2nd Rank	XX	1	0	1	XXX	1	1→0	1
Readback Mode[1]	XX	X	0	1	00X	0	1→0	1

Notes: X = don't care.
[1]For 44-pin versions only
[2]For $\overline{MS}$, $\overline{TR}$, $\overline{LS}$ = 0, a $\overline{MS}$ 1st write occurs.

Table II. AD664 Digital Truth Table

Load and Update One DAC Output

In this first example, the object is simply to change the output of one of the four DACs on the AD664 chip. The procedure is to select the address bits that indicate the DAC to be programmed, pull LATCH SELECT($\overline{LS}$) low, pull CHIP SELECT($\overline{CS}$) low, release $\overline{LS}$ and then release $\overline{CS}$. When $\overline{CS}$ goes low, data enters the first rank of the input latch. As soon as $\overline{LS}$ goes high, the data is transferred into the second rank and produces the new output voltage. During this transfer, $\overline{MS}$, $\overline{TR}$, $\overline{RD}$ and $\overline{RST}$ should be held high.

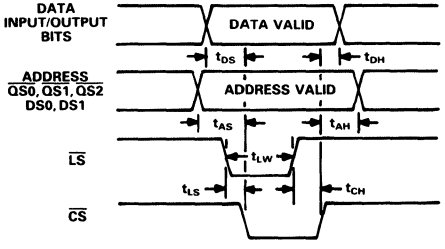


Figure 9. Update Output of a Single DAC

Preloading the First Rank of One DAC

In this case, the object is to load new data into the first rank of one of the DACs but *not* the output. As in the previous case, the address and data inputs are placed on the appropriate pins. $\overline{LS}$ is then brought to "0" and then $\overline{CS}$ is asserted. Note that in this situation, however, $\overline{CS}$ goes high before $\overline{LS}$ goes high. The input data is prevented from getting to the second rank and affecting the output voltage.

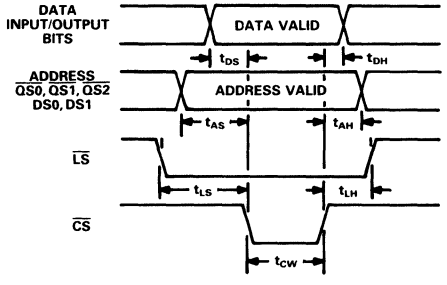


Figure 10. Preload First Rank of a DAC

This allows the user to "preload" the data to a DAC and strobe it into the output latch at some future time. The user could do this by reproducing the sequence of signals illustrated in the next section.

Update Second Rank of a DAC

Assuming that a new input code had previously been placed into the first rank of the input latches, the user can update the output of the DAC by simply pulling $\overline{CS}$ low while keeping $\overline{LS}$, $\overline{MS}$, $\overline{TR}$, $\overline{RD}$ and $\overline{RST}$ high. Address data is not needed in this case. In reality, all second ranks are being updated by this procedure, but only those which receive data different from that already there would manifest a change. Updating the second rank does not change the contents of the first rank.

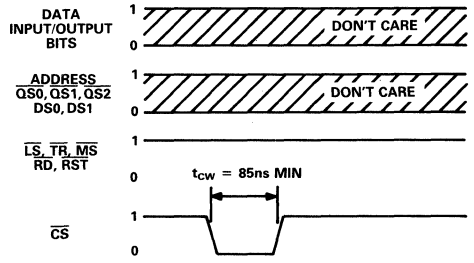


Figure 11. Update Second Rank of a DAC

The same options that exist for individual DAC input loading also exist for multiple DAC input loading. That is, the user can choose to update the first and second ranks of the registers *or* preload the first ranks and then update them at a future time.

Load and Update Multiple DAC Outputs

The following examples demonstrate two ways to update all DAC outputs. The first method involves doing all data transfers during one long $\overline{CS}$ low period. Note that in this case, shown in Figure 12, $\overline{LS}$ returns high before $\overline{CS}$ goes high. Data hold time, relative to an address change, is 70ns. This updates the outputs of all DACs simultaneously.

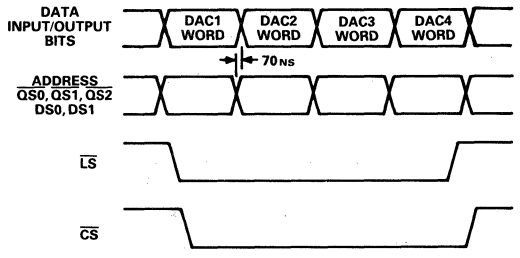


Figure 12. Update All DAC Outputs

The second method involves doing a $\overline{CS}$ assertion (low) and an $\overline{LS}$ toggle separately for each DAC. It is basically a series of preload operations (Figure 10). In this case, illustrated in Figure 13, two $\overline{LS}$ signals are shown. One, labelled $\overline{LS}$, goes high before $\overline{CS}$ returns high. This transfers the "new" input word to the DAC outputs sequentially. The second $\overline{LS}$ signal, labelled Alternate $\overline{LS}$, stays low until $\overline{CS}$ returns high. Using this sequence loads the first ranks with each "new" input word but doesn't update the DAC outputs. To then update all DAC outputs simultaneously would require the signals illustrated in Figure 11.

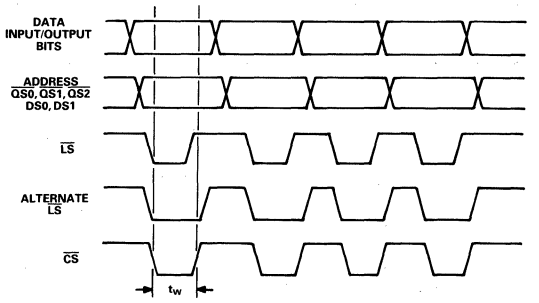


Figure 13. Load and Update Multiple DACs

Preload Multiple First Rank Registers

The first ranks of the DAC input registers may be preloaded with new input data without disturbing the second rank data. This is done by transferring the data into the first rank by bringing $\overline{CS}$ low while $\overline{LS}$ is low. But $\overline{CS}$ must return high before $\overline{LS}$. This prevents the data from the first rank from getting into the second rank. A simple second rank update cycle as shown in Figure 11 would move the "preloaded" information to the DACs.

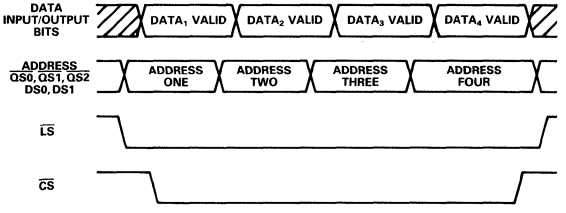


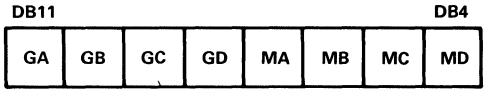
Figure 14. Preload First Rank Registers

Selecting Gain Range and Modes (44-Pin Versions)

The AD664's mode select feature allows a user to configure the gain ranges and output modes of each of the four DACs. On-board switches take the place of up to eight external relays that would normally be required to accomplish this task. The switches are programmed by the mode select word entered via the data I/O port. The mode select word is eight bits wide and occupies the topmost eight bits of the input word. The last four bits of the input word are "don't cares."

Figure 15 shows the format of the MODE SELECT word. The first four bits determine the gain range of the DAC. When set to be a gain of 1, the output of the DAC spans a voltage of 1 times the reference. When set to a gain of 2, the output of the DAC spans a voltage of 2 times the reference.

The next four bits determine the mode of the DAC. When set to UNIPOLAR, the output goes from 0 to REF or 0 to 2REF. When the BIPOLAR mode is selected, the output goes from −REF/2 to REF/2 or −REF to REF.



GX = "0", GAIN = 1
GX = "1", GAIN = 2
MX = "0", UNIPOLAR
MX = "1", BIPOLAR

Figure 15. Mode Select Word Format

Load and Update Mode of One DAC

In this next example, the object is to load new mode information for one of the DACs into the first rank of latches and then immediately update the second rank. This is done by putting the new mode information (8-bit word length) onto the databus. Then $\overline{MS}$ and $\overline{LS}$ are pulled low. Following that, $\overline{CS}$ is pulled low. This loads the mode information into the first rank of latches. $\overline{LS}$ is then brought high. This action updates the second rank of latches (and, therefore, the DAC outputs). The load cycle ends when $\overline{CS}$ is brought high.

In reality, this load cycle really updates the modes of all the DACs, but the effect is to only change the modes of those DACs whose mode select information has actually changed.

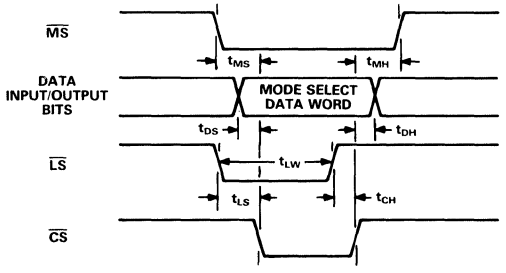


Figure 16. Load and Update Mode of One DAC

Preloading the Mode Select Register

Mode data can be written into the first rank of the mode select latch without changing the modes currently being used. This feature is useful when a user wants to preload new mode information in anticipation of strobing that in at a future time. Figure 17 illustrates the correct sequence of control signals to accomplish this task. (A second rank load requires $\overline{CS}$ = 320ns.)

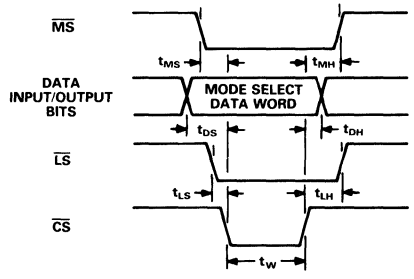


Figure 17. Preload Mode Select Register

Transparent Mode Operation (44-Pin Versions)

Transparent operation allows data from the inputs of the AD664 to be transferred into the DAC registers without the intervening step of being latched into the first rank of latches. Two modes of transparent operation exist, the "partially transparent" mode and a "fully transparent" mode. In the "partially transparent" mode, one of the DACs is transparent while the remaining three continue to use the data latched into their respective input registers. Both modes require a 12-bit wide input word!

The fully transparent mode is selected by asserting lows on $\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$, $\overline{TR}$ and $\overline{CS}$ while asserting highs on $\overline{LS}$, $\overline{MS}$ and $\overline{RD}$. Figure 18 illustrates the correct timing relationships for those signals. Address setup and $\overline{TR}$ setup times are 0ns minimum.

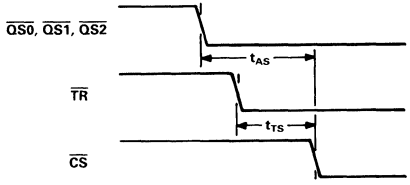


Figure 18. Fully Transparent Operation

The partially transparent mode of operation is achieved by setting $\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$, $\overline{LS}$ and $\overline{TR}$ low while $\overline{RD}$ and $\overline{MS}$ are high. The address of the transparent DAC is asserted on DS0 and DS1. Figure 19 illustrates the correct sequence of those signals. The required minimum setup times for $\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$, DS0, DS1, $\overline{TR}$ and $\overline{LS}$ are again 0ns.

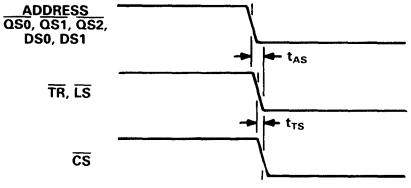


Figure 19. Partially Transparent Operation

OUTPUT DATA

Two types of outputs may be obtained from the internal data registers of the AD664 chip, mode select and DAC input code data. Readback data may be in the same forms in which it can be entered; 4-, 8-, and 12-bit wide words (12 bits only for 28-pin versions).

DAC Data Readback

DAC input code readback data is obtained by setting the address of the DAC (DS0, DS1) and Quads ($\overline{QS0}$, $\overline{QS1}$, $\overline{QS2}$) on the address pins and bringing the $\overline{RD}$ and $\overline{CS}$ pins low. The timing diagram for a DAC code readback operation appears in Figure 20.

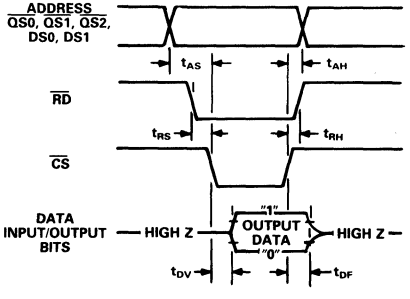


Figure 20. DAC Input Code Readback

Mode Data Readback

Mode data is read back in a similar fashion. By setting $\overline{MS}$, $\overline{QS0}$, $\overline{QS1}$, $\overline{RD}$ and $\overline{CS}$ low while setting $\overline{TR}$ and $\overline{RST}$ high, the mode select word is presented to the I/O port pins. Figure 21 shows the timing diagram for a readback of the mode select data register.

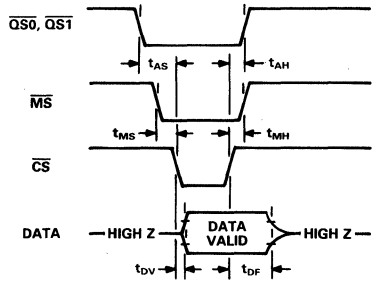


Figure 21. Mode Select Readback

OUTPUT LOADS

Readback timing is tested with the output loads shown in Figure 22.

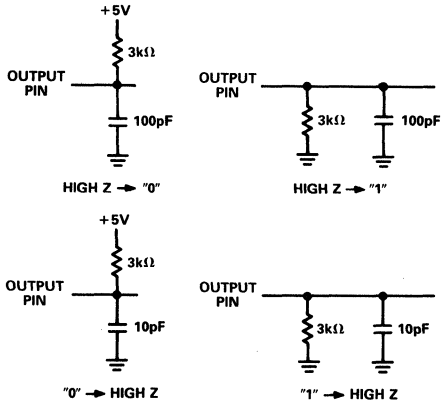


Figure 22. Output Loads

Asynchronous Reset Operation

The asynchronous reset signal shown in Figure 23 may be asserted at any time. A minimum pulse width (t_{RW}) of 90ns is required. The reset feature is designed to return all DAC outputs to 0 volts regardless of the mode or range selected. In the 44-pin versions, the modes are reset to unipolar 10V span (gain of 1), and the input codes are rewritten to be "0s." Previous DAC code and mode information is erased.

In the 28-pin versions of the AD664, the mode remains unchanged, the appropriate input code is rewritten to reset the output voltage to 0 volts. As in the 44-pin versions, the previous input data is erased.

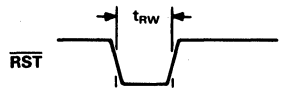


Figure 23. Asynchronous Reset Operation

At power-up, an AD664 may be activated in either the read or write modes. While, at the device level, this will not produce any problems, at the system level it may. Analog Devices recommends the addition of a simple power-on reset scheme to any system where the possibility of an unknown start-up state could be a problem. The simplest version of this scheme is illustrated in Figure 24.

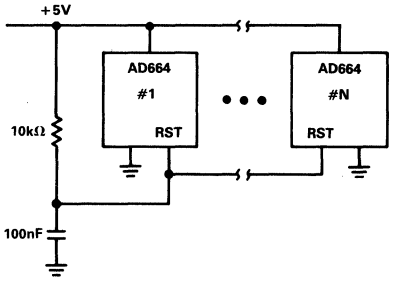


Figure 24. Power-On Reset

It is obvious from inspection that the scheme shown in Figure 24 is only appropriate for systems in which the $\overline{RST}$ pin is otherwise not used. Should the user wish to use the $\overline{RST}$ pin, an additional logic gate may be included to combine the power-on reset with the reset signal.

Interfacing the AD664 To Microprocessors

The AD664 is easy to interface with a wide variety of popular microprocessors. Common architectures include processors with dedicated 8-bit data and address buses, an 8-bit bus over which data and address are multiplexed, an 8-bit data and 16-bit address partially muxed, and separate 16-bit data and address buses.

AD664 addressing can be accomplished through either memory-mapped or I/O techniques. In memory-mapped schemes, the AD664 appears to the host microprocessor as RAM memory. Standard memory addressing techniques are used to select the AD664. In the I/O schemes, the AD664 is treated as an external I/O device by the host. Dedicated I/O pins are used to address the AD664.

MC6801 Interface

In Figures 25a-25d, we illustrate a few of the various methods that can be used to connect an AD664 to the popular MC6801 microprocessor. In each of these cases, the MC6801 is intended to be configured in its expanded, nonmultiplexed mode of operation. In this mode, the MC6801 can address 256 bytes of external memory over 8-bit data (Port 3) and 8-bit address (Port 4) buses. Eight general-purpose I/O lines (Port 1) are also available. On-board RAM and ROM provide program and data storage space.

In Figure 25a, the three least significant address bits (P40, P41 and P42) are employed to select the appropriate on-chip addresses for the various input registers of the AD664. Three I/O lines (P17, P16 and P15) are used to select various operating features of the the AD664. IOS and E(nable) are combined to produce an appropriate $\overline{CS}$ signal. This addressing scheme leaves the five most significant address bits and five I/O lines free for other tasks in the system.

Figure 25b shows another way to interface an AD664 to the MC6801. Here we've used the six least significant address lines to select AD664 features and registers. This is a purely memory-mapped scheme while the one illustrated in Figure 25a uses some memory-mapping as well as some dedicated I/O pins. In Figure 25b, two address lines and all eight I/O lines remain free for other system tasks.

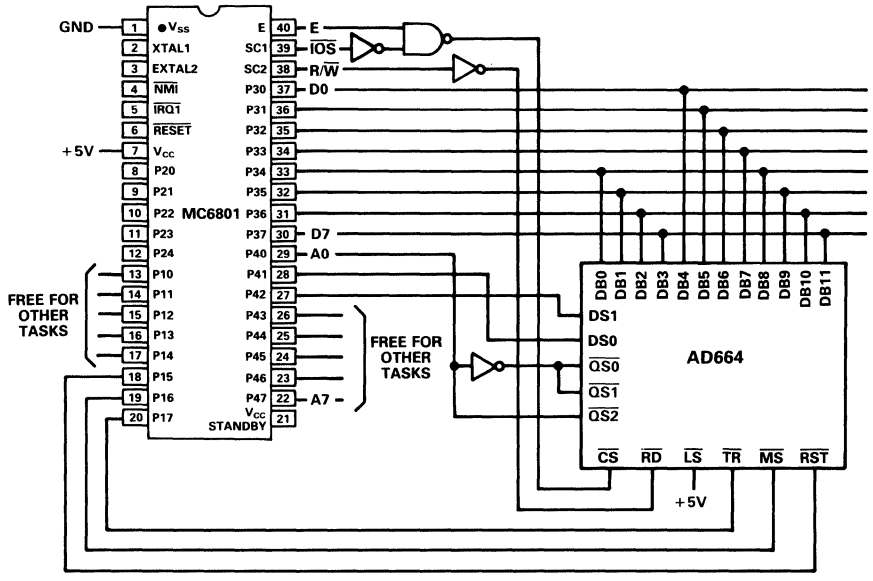


Figure 25a. Simple AD664 to MC6801 Interface

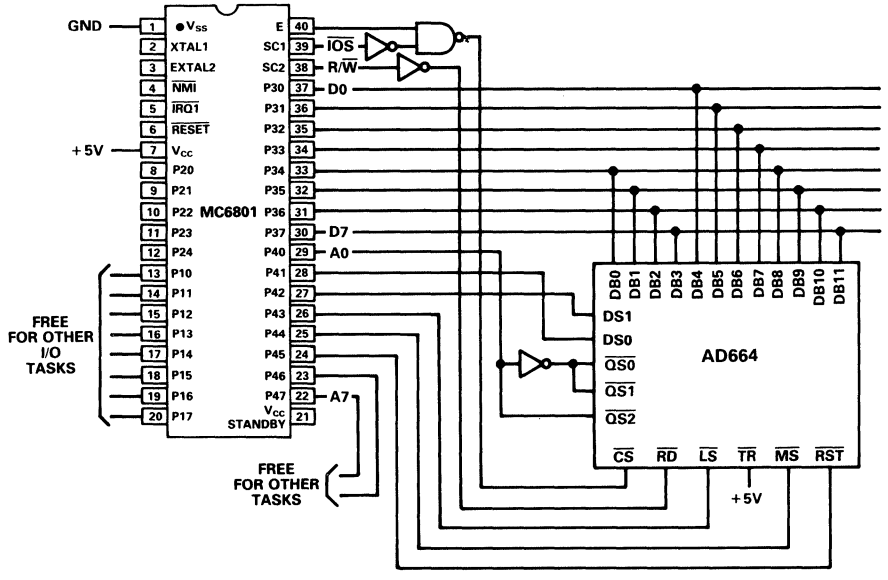


Figure 25b. Alternate AD664 to MC6801 Interface

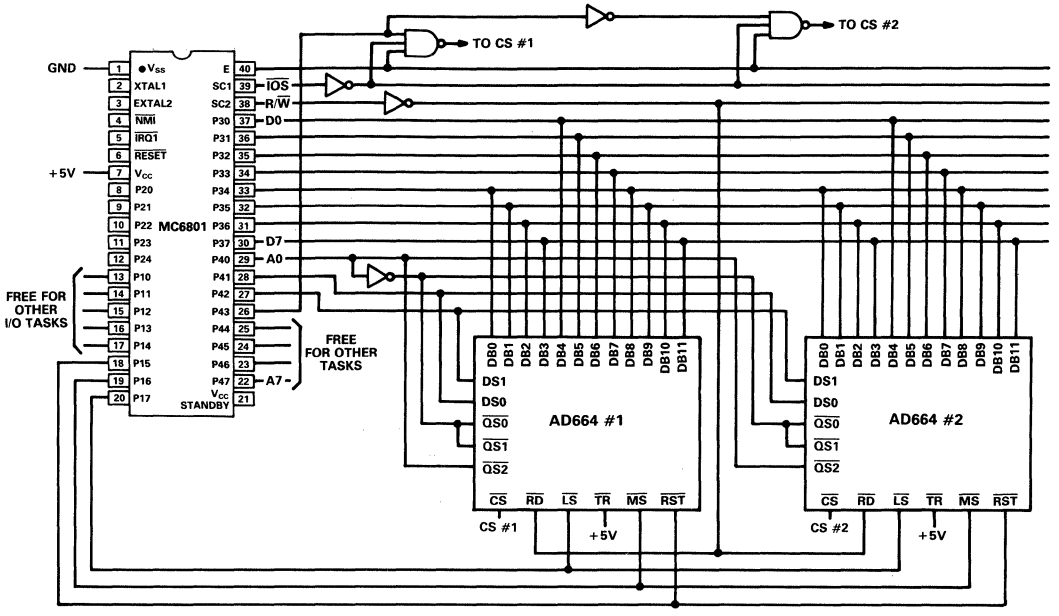


Figure 25c. Interfacing Two AD664s to an MC6801

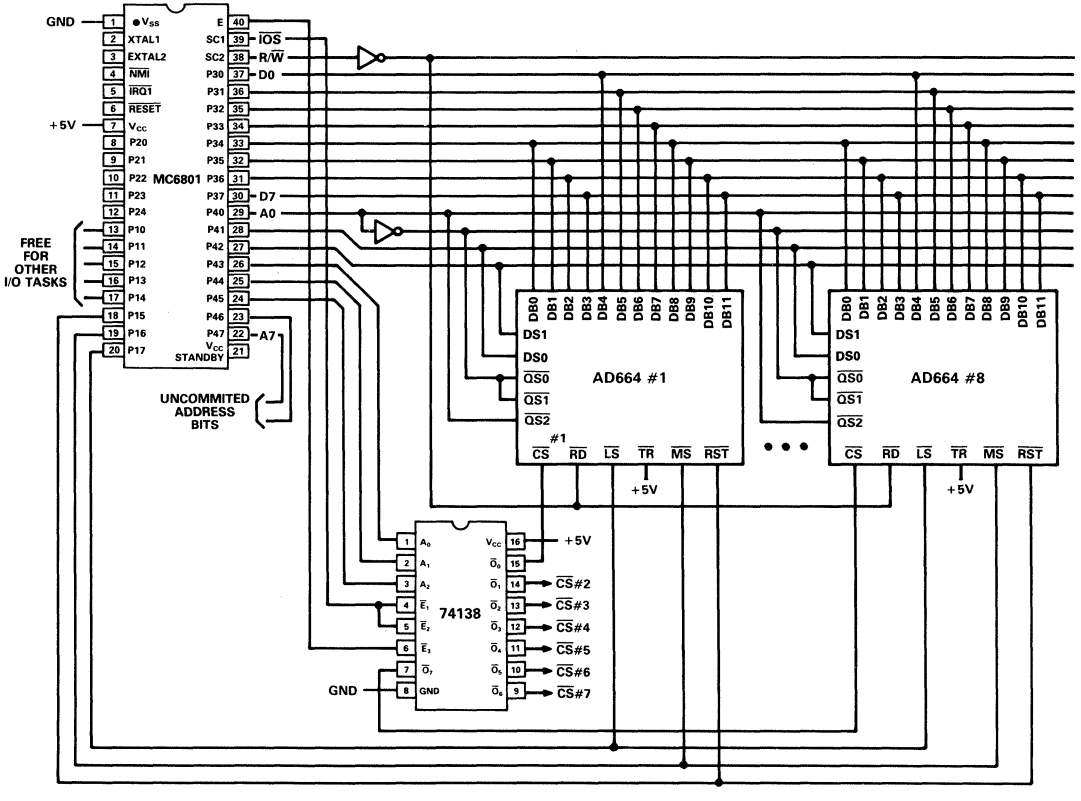


Figure 25d. Interfacing Eight AD664s to an MC6801

Expansion of the scheme employed in Figure 25a results in that shown in Figure 25c. Here, two AD664s are connected to an MC6801, providing a total of eight 12-bit, software programmable DACs. Again, the three least significant bits of address are used to select the on-chip registers of the AD664. IOS and E, as well as a fourth address bit, are decoded to provide the appropriate $\overline{CS}$ signals. Four address and five I/O lines remain uncommitted.

A slightly more sophisticated approach to system expansion is illustrated in Figure 25d. Here, a 74LS138 (1-of-8 decoder) is used to address one of the eight AD664s connected to the MC6801. The three least significant address bits are used to select on-chip register and DAC. The next three address bits are used to select the appropriate AD664. IOS and E gate the 74LS138 output.

The schemes in Figure 25 illustrate some of the trade-offs which a designer may make when configuring a system. For example, the designer may use I/O lines instead of address bits or vice versa. This decision may be influenced by other I/O tasks or system expansion requirements. He/she can also choose to implement only a subset of the features available. Perhaps the $\overline{RST}$ pin isn't really needed. Tying that input pin to V_{LOGIC} frees up another I/O or address bit. The same consideration applies to mode select. In all of these cases $\overline{TR}$ is shown tied to V_{LOGIC}, because the MC6801 cannot provide the 12-bit-wide input word required for the transparent mode. In situations where transparent operation isn't required, and mode select is also not needed, the designer may consider specifying the DIP version of the device (either the UNI or BIP version).

Each of the schemes illustrated in Figure 25 operates with an MC6801 at clock rates up to and including 1.5MHz. Similar schemes can be derived for other 8-bit microprocessors and microcontrollers such as the 8051/8086/8088/6502, etc. One such scheme developed for the 8051/AD664 is illustrated in Figure 26.

8051 Interface

Figure 26 shows the AD664 combined with an 8051 μcontroller chip. Three LSBs of address provide the quad and DAC select signals. Control signals from Port 1 select various operating modes such as readback, mode select and reset as well as providing the $\overline{LS}$ signal. Read and write signals from the 8051 are decoded to provide the $\overline{CS}$ signal.

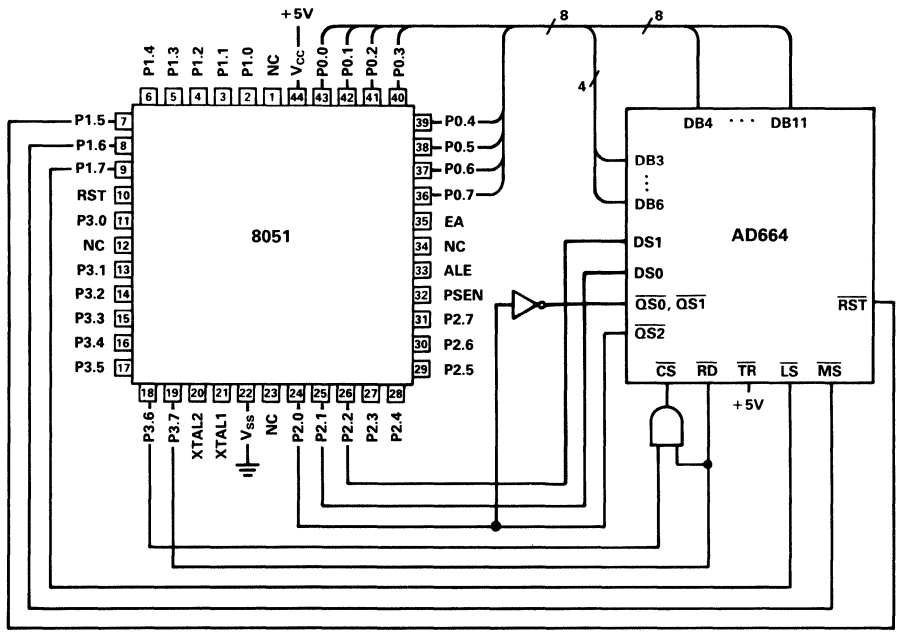


Figure 26. AD664 to 8051 Interface

IBM PC* Interface

Figure 27 illustrates a simple interface between an IBM PC and an AD664. The three least significant address bits are used to select the Quad and DAC. The next two address bits are used for $\overline{LS}$ and $\overline{MS}$. In this scheme, a 12-bit input word requires two load cycles, an 8-bit word and a 4-bit word. Another write is required to transfer the word or words previously written to the second rank. A 12-bit-wide word again requires at least two read cycles; one for the 8MSBs and four for the LSBs. The page select signal produces a $\overline{CS}$ strobe for any address from 300H to 31FH.

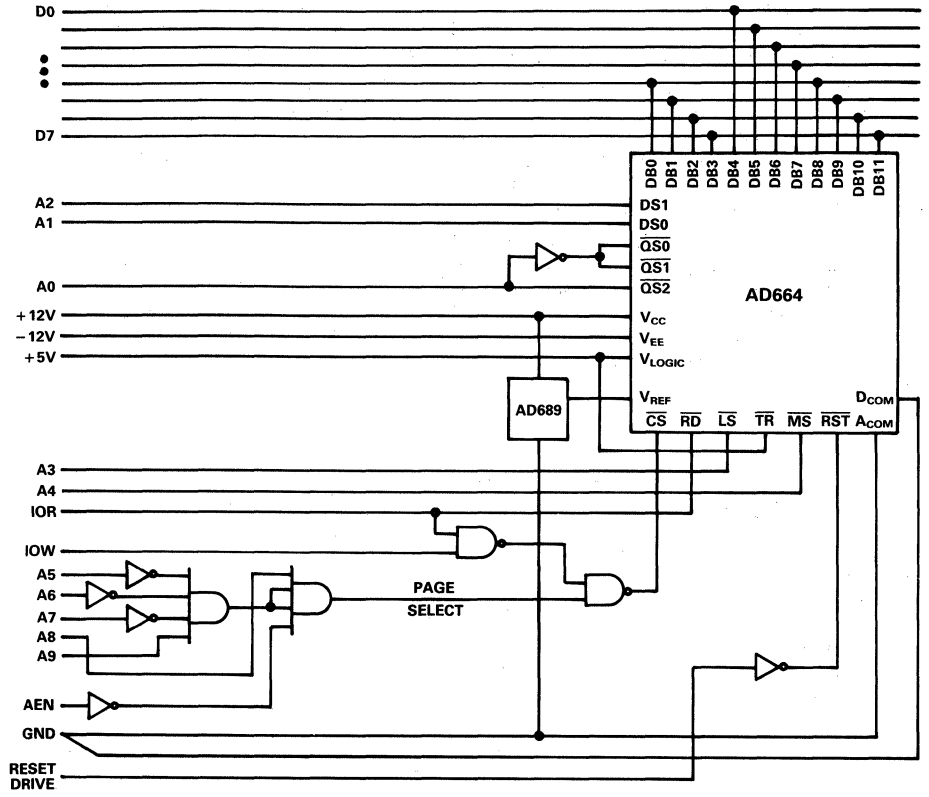


Figure 27. AD664 to IBM PC Interface

*IBM PC is a trademark of International Business Machines Corp.

Table III, shown below details the memory locations and addresses used by this interface.

HEX	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	REGISTER SELECTED
300	1	1	0	0	0	0	0	0	0	0	Illegal Address
301								0	0	1	Mode Select, 1st Rank
302								0	1	0	Illegal Address
303								0	1	1	Mode Select, 1st Rank
304								1	0	0	Illegal Address
305								1	0	1	Mode Select, 1st Rank
306								1	1	0	Illegal Address
307								1	1	1	Mode Select, 1st Rank
308							1	0	0	0	Mode Select, 2nd Rank
309								0	0	1	
30A								0	1	0	
30B								0	1	1	
30C								1	0	0	
30D								1	0	1	
30E								1	1	0	
30F								1	1	1	
310						1	0	0	0	0	DAC A, 4LSBs, 1st Rank
311								0	0	1	DAC A, 8MSBs, 1st Rank
312								0	1	0	DAC B, 4LSBs, 1st Rank
313								0	1	1	DAC B, 8MSBs, 1st Rank
314								1	0	0	DAC C, 4LSBs, 1st Rank
315								1	0	1	DAC C, 8MSBs, 1st Rank
316								1	1	0	DAC D, 4LSBs, 1st Rank
317								1	1	1	DAC D, 8MSBs, 1st Rank
318							1	0	0	0	2nd Rank
319								0	0	1	
31A								0	1	0	
31B								0	1	1	
31C								1	0	0	
31D								1	0	1	
31E								1	1	0	
31F								1	1	1	

Note: Shaded registers are readable.

Table III. IBM PC Memory Map

The following IBM PC Basic routine produces four output voltage ramps from one AD664. Line numbers 10 through 70 define the hardware addresses for the first and second ranks of DAC registers as well as the first and second ranks of the mode select register. Program variables are initialized in line numbers 110 through 130. Line number 170 writes "0s" out to the first rank and, then, the second rank of the mode select register.

Line numbers 200 through 320 calculate output voltages. Finally line numbers 410 through 450 update the first, then the second ranks of the DAC input registers. Hardware registers may be read with the "INP" instruction. For example, the contents of the DAC A register may be accessed with the following command: Line# A=INP(DACA).

```
  5  REM----AD664 LISSAJOUS PATTERNS----
 10  REM ---ASSIGN HARDWARE ADDRESSES---
 20  DACA = 785
 30  DACB = 787
 40  DACC = 789
 50  DACD = 791
 60  DAC2ND = 792
 70  MODE1 = 769 :MODE2 = 776
 80  REM
 90  REM
100  REM ---INITIALIZE VARIABLES---
110  X=0: Y1 = 128: Y2 = 64: Y3 = 32
120  CX = 1: CY1 = 1: CY2 = -1: CY3 = 1
130  FX = 9: FY1 = 5: FY2 = 13 : FY3 = 15
140  REM
150  REM
160  REM ---INITIALIZE MODES AND GAINS---
170  OUT MODE1,0: OUT MODE2,0
180  REM
190  REM
200  REM ---CALCULATE VARIABLES---
210   X  = X  + FX*CX
220   Y1 = Y1 + FY1*CY1
230   Y2 = Y2 + FY2*CY2
240   Y3 = Y3 + FY3*CY3
250  IF X > 255 THEN X = 255: CX = -1: GOTO 270
260  IF X < 0 THEN X = 0: CX = 1
270  IF Y1 > 255 THEN Y1 = 255: CY1 = -1: GOTO 290
280  IF Y1 < 0 THEN Y1 =0: CY1 = 1
290  IF Y2 > 255 THEN Y2 =255: CY2=-1: GOTO 310
300  IF Y2 < 0 THEN Y2 = 0: CY2=-1
310  IF Y3 > 255 THEN Y3 = 255: CY3=-1: GOTO 400
320  IF Y3 < 0 THEN Y3=0: CY3=1
330  REM
340  REM
400  REM ---SEND DAC DATA---
410  OUT DACA,X
420  OUT DACB,Y1
430  OUT DACC,Y2
440  OUT DACD,Y3
450  OUT DAC2ND,0
500  REM
510  REM
520  REM ---LOOP BACK---
530  GOTO 210
```

Simple AD664 to MC68000 Interface

Figure 28 shows an AD664 connected to an MC68000. In this memory-mapped I/O scheme, the "left-justified" data is written in one 12-bit input word. Four address bits are used to perform the on-chip D/A selection as well as the various operating features. The R/$\overline{W}$ signal controls the $\overline{RD}$ function and system reset controls $\overline{RST}$.

This scheme can be converted to write "right-justified" data by connecting the data inputs to DATA bits D0 through D11 respectively. Other options include controlling the $\overline{QS0}$, $\overline{QS1}$ and $\overline{QS2}$ pins with $\overline{UDS}$ and $\overline{LDS}$ to provide a way to write 8-bit input and read 8-bit output words.

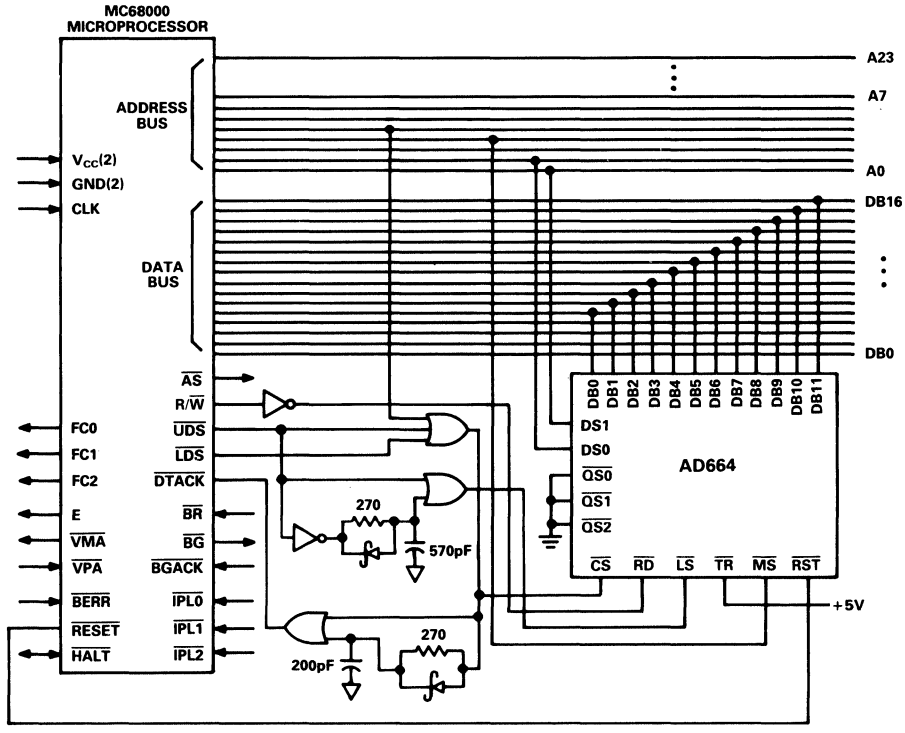


Figure 28. AD664 to MC68000 Interface

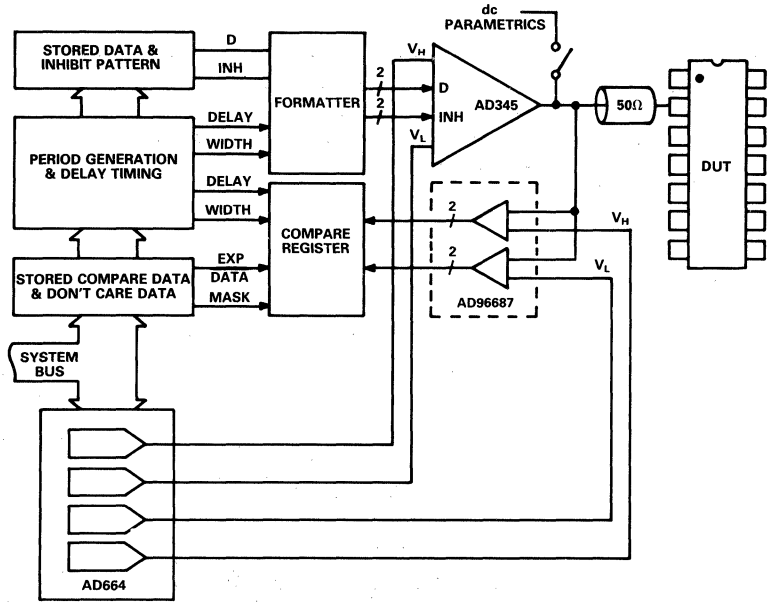


Figure 29. AD664 in a "Tester-Per-Pin" Architecture

APPLICATIONS OF THE AD664

"Tester-Per-Pin" ATE Architecture

Figure 29 Shows the AD664 used in a single channel of a digital test system. In this scheme, the AD664 supplies four individual output voltages. Two are provided to the V_{HIGH} and V_{LOW} inputs of the AD345 pin driver I.C. to set the digital output levels. Two others are routed to the inputs of the AD96687 dual comparator to supply reference levels of the readback features. This approach can be replicated to give as many channels of stimulus/readback as the tester has pins. The AD664 is a particularly appropriate choice for a large-scale system because the low power requirements (under 500mW) ease power supply and cooling requirements. Analog ground currents of 600μA or less make the ground current management task simpler. All DACs can be driven from the same system reference and will track over time and temperature. Finally, the small board area required by the AD664 (and AD345 and AD96687) allows a high functional density.

X-Y Plotters

Figure 30 is a block diagram of the control section of a microprocessor-controlled X-Y pen plotter. In this conceptual exercise, two of the DACs are used for the X-channel drive and two are used for the Y-channel drive. Each provides either the coarse or fine movement control for its respective channel. This approach offers increased resolution over some other approaches.

A designer can take advantage of the reset feature of the AD664 in the following manner. If the system is designed such that the "HOME" position of the pen (or galvanometer, beam, head or similar mechanism) results when the outputs of all of the DACs are at zero, then no system software is required to home the pen. A simple reset signal is sufficient.

Similarly, the transparent feature could be used to the same end. One code can be sent to all DACs at the same time to send the pen to the home position. Of course, this would require some software where the previous example would require only a single reset strobe signal!

Drawing scaling can be achieved by taking advantage of the AD664's software programmable gain settings. If, for example, an "A" size drawing is created with gain settings of 1, then a "C" size drawing can be created by simply resetting all DAC gains to 2 and redrawing the object. Conversely, a "C" size drawing created with gains of 2 can be reduced to "A" size simply by changing the gains to 1 and redrawing. The same principal applies for conversion from "B" size to "D" size or "D" size to "B" size. The multiplying capability of the AD664 provides another scaling option. Changing the reference voltage provides a proportional change in drawing size. Inverting the reference voltage would invert the drawing.

Swapping digital input data from the X channel to the Y channel would rotate the drawing 90 degrees.

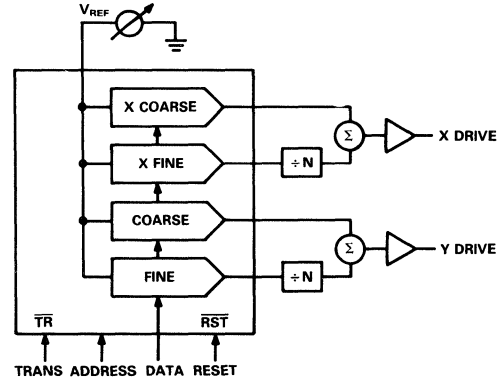


Figure 30. X-Y Plotter Block Diagram

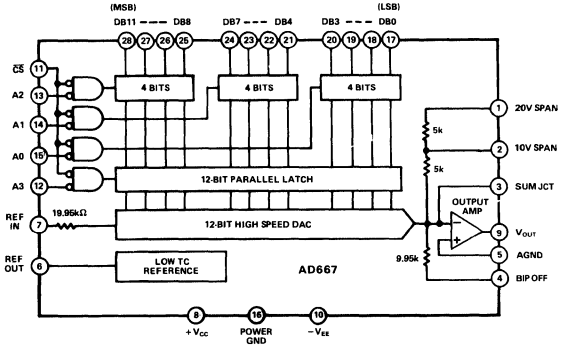
Microprocessor-Compatible 12-Bit D/A Converter

AD667*

FEATURES

- **Complete 12-Bit D/A Function**
  - **Double-Buffered Latch**
  - **On Chip Output Amplifier**
  - **High Stability Buried Zener Reference**
- **Single Chip Construction**
- **Monotonicity Guaranteed Over Temperature**
- **Linearity Guaranteed Over Temperature: 1/2LSB max**
- **Settling Time: 3μs max to 0.01%**
- **Guaranteed for Operation with ±12V or ±15V Supplies**
- **Low Power: 300mW Including Reference**
- **TTL/5V CMOS Compatible Logic Inputs**
- **Low Logic Input Currents**

AD667 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD667 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD667 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD667 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K, B grades) at 25°C and ±1/2LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity, is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD667 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 5ppm/°C.

***Covered by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.**

The AD667 is available in five performance grades. The AD667J and K are specified for use over the 0 to +70°C temperature range and are available in a 28-pin molded plastic DIP (N) or PLCC (P) package. The AD667S grade is specified for the −55°C to +125°C range and is available in the ceramic DIP (D) or LCC (E) package. The AD667A and B are specified for use over the −25°C to +85°C temperature range and are available in either a 28-pin hermetically sealed ceramic DIP (D) or LCC (E) package.

PRODUCT HIGHLIGHTS

1. The AD667 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried Zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current steering switch and on-board high speed output amplifier settle within 1/2LSB for a 10V full scale transition in 2.0μs when properly compensated.

SPECIFICATIONS (T_A = +25°C, ±12V. ±15V power supplies unless otherwise noted)

Model	AD667J Min	AD667J Typ	AD667J Max	AD667K Min	AD667K Typ	AD667K Max	Units
DIGITAL INPUTS							
Resolution			12			12	Bits
Logic Levels (TTL Compatible, T_{min}–T_{max})[1]							
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10	µA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2	LSB
$T_A = T_{min}$ to T_{max}		Monotonicity Guaranteed			Monotonicity Guaranteed		LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		±1	±2	LSB
Bipolar Zero[2]		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT							
Differential Linearity		±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR Change (2kΩ‖500pF load)							
with 10kΩ Feedback		3	4		3	4	µs
with 5kΩ Feedback		2	3		2	3	µs
For LSB Change		1			1		µs
Slew Rate	10			10			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			mA
Output Impedance (dc)		0.05			0.05		Ω
Short Circuit Current			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5V dc		5	10		5	10	ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			±12, ±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	V
Supply Current							
+11.4 to +16.5V dc		8	12		8	12	mA
−11.4 to −16.5V dc		20	25		20	25	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	−65		+125	−65		+125	°C

NOTES
[1]The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.
[2]Adjustable to zero.
[3]FSR means "Full Scale Range" and is 20V for ±10V range and 10V for the ±5V range.
[4]A minimum power supply of ±12.5V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TIMING SPECIFICATIONS

(All Models, T_A = 25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V)

Symbol	Parameter	Min	Typ	Max	
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

ABSOLUTE MAXIMUM RATINGS

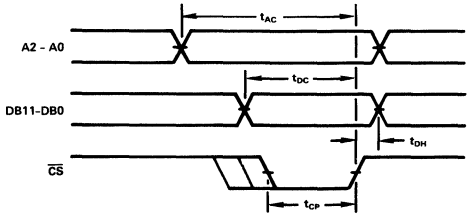
V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 11–15, 17–28)
to Power Ground . . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out, V_{OUT} (Pins 6, 9) . . Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

Model	AD667A Min	AD667A Typ	AD667A Max	AD667B Min	AD667B Typ	AD667B Max	AD667S Min	AD667S Typ	AD667S Max	Units
DIGITAL INPUTS										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible, $T_{min}-T_{max}$)[1]										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.7	V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10		3	10	μA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5		1	5	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4		±1/8	±1/2	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2		±1/4	±3/4	LSB
$T_A = T_{min}$ to T_{max}		Monotonicity Guaranteed			Monotonicity Guaranteed			Monotonicity Guaranteed		LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		±1	±2		±1	±2	LSB
Bipolar Zero[2]		±0.05	±0.1		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT										
Differential Linearity		±2			±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15		±15	±30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ±0.01% of FSR for										
FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY										
V_{CC} = +11.4 to +16.5V dc		5	10		5	10		5	10	ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	10		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±12, ±15			±12, ±15			±12, ±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	±11.4		±16.5	V
Supply Current										
+11.4 to +16.5V dc		8	12		8	12		8	12	mA
−11.4 to −16.5V dc		20	25		20	25		20	25	mA
TEMPERATURE RANGE										
Specification	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C

TIMING DIAGRAMS

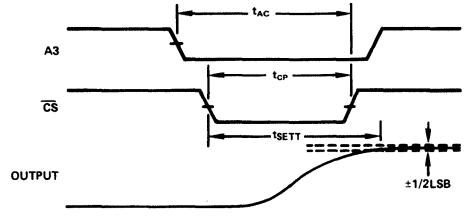
WRITE CYCLE #1

(Load First Rank from Data Bus; A3 = 1)

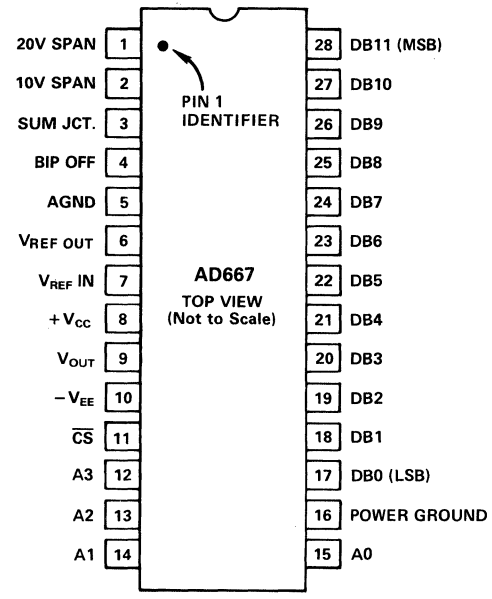


WRITE CYCLE #2

(Load Second Rank from First Rank; A2, A1, A0 = 1)

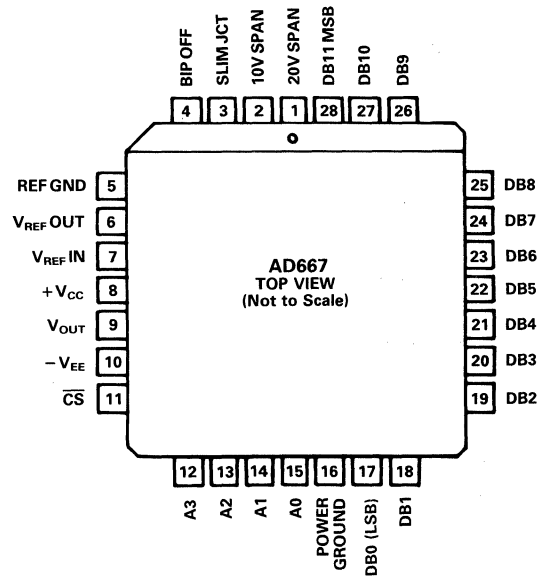


28-PIN DIP CONNECTIONS



*NOTE DIP PACKAGE PIN NUMBERS AND LCC CONTACT NUMBERS SERVE THE SAME FUNCTION.

PLCC, LCC PIN CONNECTIONS



ORDERING INFORMATION

Model	Package Options*	Temperature Range – °C	Linearity Error Max @ 25°C	Gain T.C. Max ppm/°C
AD667JN	Plastic DIP (N-28)	0 to +70	±1/2LSB	30
AD667JP	PLCC (P-28A)	0 to +70	±1/2LSB	30
AD667KN	Plastic DIP (N-28)	0 to +70	±1/4LSB	15
AD667KP	PLCC (P-28A)	0 to +70	±1/4LSB	15
AD667AD	Ceramic DIP (D-28)	−25 to +85	±1/2LSB	30
AD667AE	LCC (E-28A)	−25 to +85	±1/2LSB	30
AD667BD	Ceramic DIP (D-28)	−25 to +85	±1/4LSB	15
AD667BE	LCC (E-28A)	−25 to +85	±1/4LSB	15
AD667SD	Ceramic DIP (D-28)	−55 to +125	±1/2LSB	30
AD667SE	LCC (E-28A)	−55 to +125	±1/2LSB	30

*See Section 14 for package outline information.

THE AD667 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD667 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and B versions and 1/2LSB for the J, A and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD667 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be −1.83mV, or −3/4LSB. The AD667K and B grades have a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2 LSB.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD667 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V.

Gain and offset drift are minimized in the AD667 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table I.

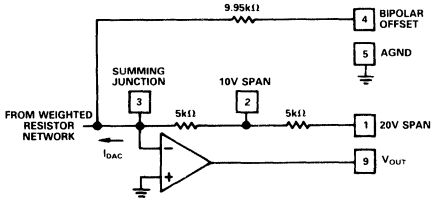


Figure 1. Output Amplifier Voltage Range Scaling Circuit

UNIPOLAR CONFIGURATION (Figure 2)

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar offset terminal, pin 4, should be grounded if not used for trimming.

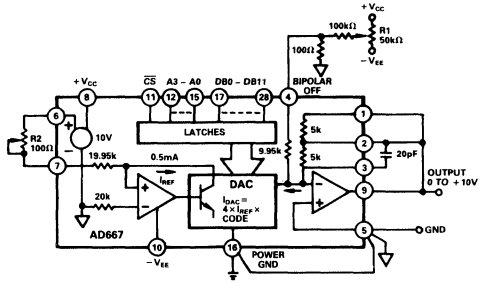


Figure 2. 0 to +10V Unipolar Voltage Output

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and pin 4 should be connected to pin 5.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.)

BIPOLAR CONFIGURATION (Figure 3)

This configuration will provide a bipolar output voltage from −5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give −5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

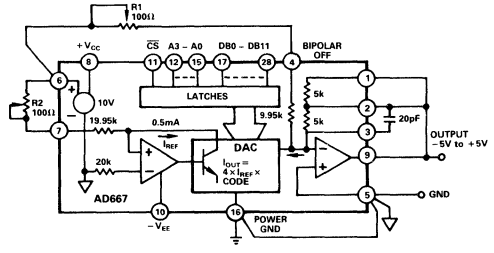


Figure 3. ±5V Bipolar Voltage Output

Output Range	Digital Input Codes	Connect Pin 9 to	Connect Pin 1 to	Connect Pin 2 to	Connect Pin 4 to
±10V	Offset Binary	1	9	NC	6 (through 50Ω fixed or 100Ω trim resistor)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (through 50Ω fixed or 100Ω trim resistor)
±2.5V	Offset Binary	2	3	9	6 (through 50Ω fixed or 100Ω trim resistor)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (or optional trim – See Figure 2)
0 to +5V	Straight Binary	2	3	9	5 (or optional trim – See Figure 2)

Table I. Output Voltage Range Connections

INTERNAL/EXTERNAL REFERENCE USE

The AD667 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD667 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale error and bipolar offset) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset). A minimum of 0.1mA is available for driving external loads. The AD667 reference output should be buffered with an external op amp if it is required to supply more than 0.1mA output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

If an external reference is used (10.000V, for example), additional trim range must be provided, since the internal reference has a tolerance of ±1%, and the AD667 full-scale and bipolar offset are both trimmed with the internal reference. The gain and offset trim resistors give about ±0.25% adjustment range, which is sufficient for the AD667 when used with the internal reference.

It is also possible to use external references other than 10 volts. The recommended range of reference voltage is from +8 to +11 volts, which allows both 8.192V and 10.24V ranges to be used. The AD667 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range in a particular application, a CMOS multiplying DAC is a better choice.

Reduced values of reference voltage will also permit the ±12 volt ±5% power supply requirement to be relaxed to ±12 volts ±10%.

It is not recommended that the AD667 be used with external feedback resistors to modify the scale factor. The internal resistors are trimmed to ratio-match and temperature-track the other resistors on the chip, even though their absolute tolerances are ±20%, and absolute temperature coefficients are approximately −50ppm/°C. If external resistors are used, a wide trim range (±20%) will be needed and temperature drift will be increased to reflect the mismatch between the temperature coefficients of the internal and external resistors.

Small resistors may be added to the feedback resistors in order to accomplish small modifications in the scaling. For example, if a 10.24V full-scale is desired, a 140Ω 1% low-TC metal-film resistor can be added in series with the internal (nominal) 5k feedback resistor, and the gain trim potentiometer (between pins 6 and 7) should be increased to 200Ω. In the bipolar mode, increase the value of the bipolar offset trim potentiometer also to 200Ω.

GROUNDING RULES

The AD667 brings out separate analog and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths.

The analog ground at pin 5 is the ground point for the output amplifier and is thus the "high quality" ground for the AD667; it should be connected directly to the analog reference point of the system. The power ground at pin 16 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

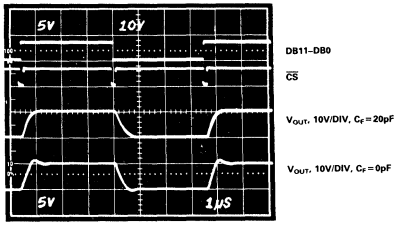
It is also important to apply decoupling capacitors properly on the power supplies for the AD667 and the output amplifier. The correct method for decoupling is to connect a capacitor from each power supply pin of the AD667 to the analog ground pin of the AD667. Any load driven by the output amplifier should also be referred to the analog ground pin.

OPTIMIZING SETTLING TIME

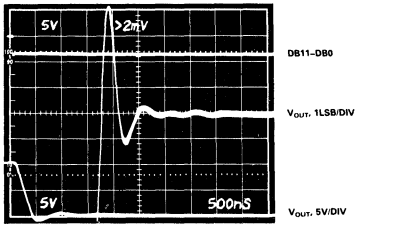
The dynamic performance of the AD667's output amplifier can be optimized by adding a small (20pF) capacitor across the feedback resistor. Figure 4 shows the improvement in both large-signal and small-signal settling for the 10V range. In Figure 4a, the top trace shows the data inputs (DB11–DB0 tied together), the second trace shows the CS pulse (A3–A0 tied low), and the lower two traces show the analog outputs for C_F = 0 and 20pF respectively.

Figures 4b and 4c show the settling time for the transition from all bits on to all bits off. Note that the settling time to ±1/2LSB for the 10V step is improved from 2.4 microseconds to 1.6 microseconds by the addition of the 20pF capacitor.

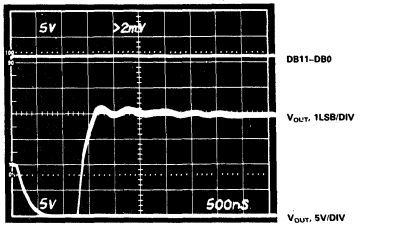
Figures 4d and 4e show the settling time for the transition from all bits off to all bits on. The improvement in settling time gained by adding C_C = 20pF is similar.



a. Large Scale Settling

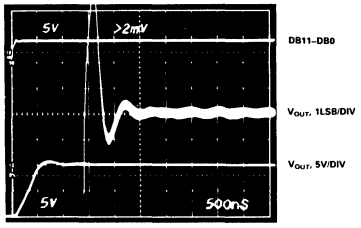


b. Fine-Scale Settling, C_F = 0pF

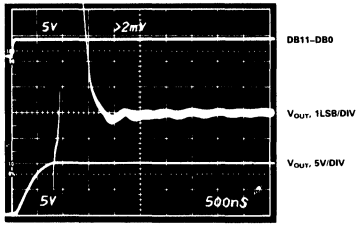


c. Fine-Scale Settling, C_F = 20pF

Figure 4. Settling Time Performance



d. Fine-Scale Settling, $C_F = 0pF$



e. Fine-Scale Settling, $C_F = 20pF$

Figure 4. Settling Time Performance (Continued)

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD667 consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers which can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 5 shows the block diagram of the AD667 logic section.

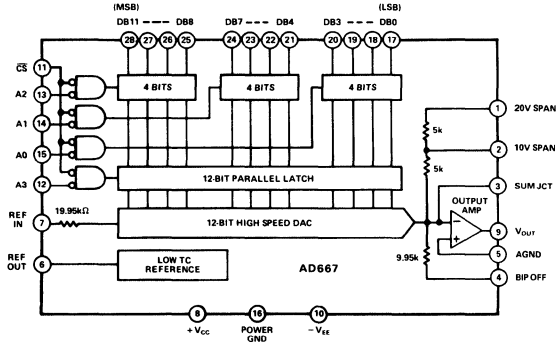


Figure 5. AD667 Block Diagram

The latches are controlled by the address inputs, A0-A3, and the $\overline{CS}$ input. All control inputs are active low, consistent with general practice in microprocessor systems. The four address lines each enable one of the four latches, as indicated in Table II.

All latches in the AD667 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. When any one of the control signals returns high, the data is latched.

It is permissible to enable more than one of the latches simultaneously. If a first rank latch is enabled coincident with the second rank latch, the data will reach the second rank correctly if the "WRITE CYCLE #1" timing specifications are met.

$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table II. AD667 Truth Table

INPUT CODING

The AD667 uses positive-true binary input coding. Logic "1" is represented by an input voltage greater than 2.0V and logic "0" is defined as an input voltage less than 0.8V.

Unipolar coding is straight binary, where all zeroes (000_H) on the data inputs yields a zero analog output and all ones (FFF_H) yields an analog output 1LSB below full scale.

Bipolar coding is offset binary, where an input code of 000_H yields a minus full-scale output, an input of FFF_H yields an output 1LSB below positive full scale, and zero occurs for an input code with only the MSB on (800_H).

The AD667 can be used with two's complement input coding if an inverter is used on the MSB (DB11).

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can thus interface with any type of 5 volt logic. The configuration of the input circuit is shown in Figure 6.

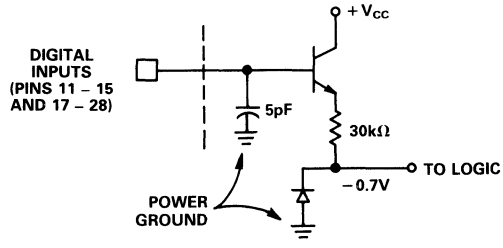


Figure 6. Equivalent Digital Input Circuit

The AD667 data and control inputs will float to a logic 0 if left open. It is recommended that any unused inputs be connected to power ground to improve noise immunity.

Fanout for the AD667 is 100 when used with a standard low power Schottky gate output device.

8-BIT MICROPROCESSOR INTERFACE

The AD667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats.

Whenever a 12-bit DAC is loaded from an 8-bit bus, two bytes are required. If the program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the 4 most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4
DB3	DB2	DB1	DB0	X	X	X	X

a. Left Justified

X	X	X	X	DB11	DB10	DB9	DB8
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

b. Right Justified

Figure 7. 12-Bit Data Formats for 8-Bit Systems

Figure 8 shows an addressing scheme for use with an AD667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the AD667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

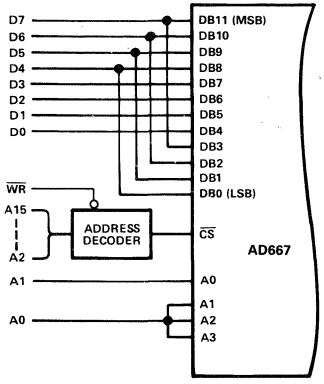


Figure 8. Left-Justified 8-Bit Bus Interface

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD667 still occupies two adjacent locations in the processor's memory map. In the circuit of Figure 9, location X01 loads the 8LSBs and location X10 loads the 4MSBs and updates the output.

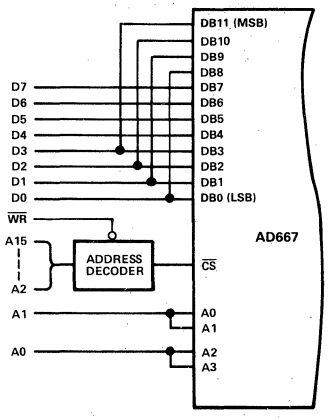


Figure 9. Right-Justified 8-Bit Bus Interface

USING THE AD667 WITH 12- AND 16-BIT BUSES

The AD667 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines (A0 through A3) are tied low, and the latch is enabled by $\overline{CS}$ going low. The AD667 thus occupies a single memory location.

This configuration uses the first and second rank registers simultaneously. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is low will cause activity at the AD667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

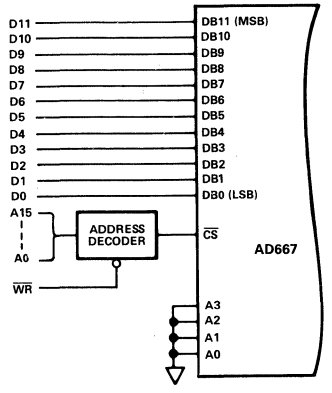


Figure 10. Connections for 12- and 16-Bit Bus Interface

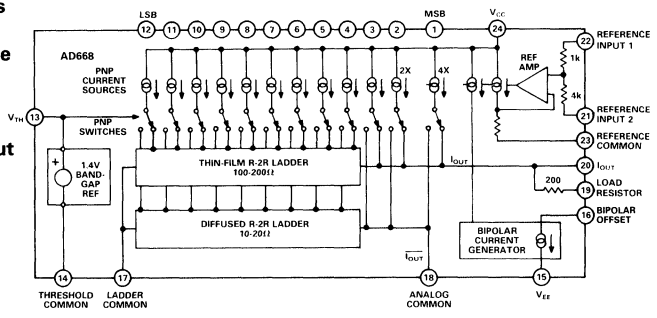
12-Bit Ultrahigh Speed Multiplying D/A Converter

AD668

FEATURES

- **Ultrahigh Speed: Current Settling to 1 LSB in 50 ns for a Full Scale Change in Digital Input. Voltage Settling to 1 LSB in 80 ns for a Full Scale Change in Analog Input**
- **25 MHz Reference Bandwidth**
- **Monotonicity Guaranteed over Temperature**
- **10.24 mA Current Output or 1.024 V Voltage Output**
- **Integral and Differential Linearity Guaranteed over Temperature**
- **0.3" "Skinny DIP" Packaging**

AD668 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD668 is an ultrahigh speed, 12-bit, multiplying digital-to-analog converter, providing outstanding accuracy and speed performance in responding to both analog and digital inputs. The AD668 provides a level of performance and functionality in a monolithic device that exceeds that of many contemporary hybrid devices. The part is fabricated using Analog Devices' Complementary Bipolar (CB) Process, which features high-speed NPN and PNP devices on the same chip without the use of dielectric isolation. The AD668's design capitalizes on this proprietary process in combination with standard low-impedance circuit techniques to provide its unique combination of speed and accuracy in a monolithic part.

The wideband reference input is buffered by a high gain, closed loop reference amplifier. The reference input is essentially a 1 V, high impedance input, but trimmed resistive dividers are provided to readily accommodate 5 V and 1.25 V references. The reference amplifier features an effective small signal bandwidth of 25 MHz, and an effective slew rate of 3% of full scale/ns.

Multiple matched current sources and thin film ladder techniques are combined to produce bit weighting. The output range can nominally be taken as a 10.24 mA current output or a 1.024 V voltage output. Varying the analog input can provide modulation of the DAC full scale from 10% to 120% of its nominal value. Bipolar outputs can be realized through pin-strapping to provide two quadrant operation without additional external circuitry.

Laser wafer trimming insures full 12-bit linearity and excellent gain accuracy. All grades of the AD668 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100 Ω ±1.0%.

The AD668 is available in three performance grades. The AD668JQ and KQ are available in 24-pin cerdip (0.3") packages and are specified for operation from 0 to +70°C. The AD668SQ features operation from −55°C to +125°C and is also packaged in the hermetic 0.3" cerdip.

PRODUCT HIGHLIGHTS

1. The fast settling time of the AD668 provides suitable performance for waveform generation, graphics display, and high-speed A/D conversion applications.
2. The high bandwidth reference channel allows high frequency modulation between analog and digital inputs.
3. The AD668's design is configured to allow wide variation of the analog input, from 10% to 120% of its nominal value.
4. The AD668's combination of high performance and tremendous flexibility makes it an ideal building block for a variety of high speed, high accuracy instrumentation applications.
5. The digital inputs are readily compatible with both TTL and 5 V CMOS logic families.
6. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.

SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +15 V, V_{EE} = −15 V, unless otherwise noted)

Model	AD668J Min	AD668J Typ	AD668J Max	AD668K Min	AD668K Typ	AD668K Max	AD668 Min	AD668 Typ	AD668 Max	Units
RESOLUTION	12			12			12			Bits
LSB WEIGHT (At Nominal FSR)										
Current		2.5			*			*		μA
Voltage (Current into R_L)		250			*			*		μV
ACCURACY[1]										
Linearity	−1/2		+1/2	−1/4		+1/4	−1/2		+1/2	LSB
T_{min} to T_{max}	−3/4		+3/4	−1/2		+1/2	−3/4		+3/4	LSB
Differential Linearity	−1		+1	−1/2		+1/2	−1		+1	LSB
T_{min} to T_{max}	−1		+1	−1/2		+1/2	−1		+1	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE									
Unipolar Offset (Digital)	−0.2		+0.2	*		*	*		*	% of FSR
Bipolar Offset	−1.0		+1.0	*		*	*		*	% of FSR
Bipolar Zero	−0.2		+0.2	*		*	*		*	% of FSR
Analog Offset	−0.5		+0.5	*		*	*		*	% of V_{NOM}
Gain Error	−1.0		+1.0	*		*	*		*	% of FSR
TEMPERATURE COEFFICIENTS[2]										
Unipolar Offset	−5		+5	*		*	*		*	ppm of FSR/°C
Bipolar Offset	−15		+15	*		*	*		*	ppm of FSR/°C
Bipolar Zero	−10		+10	*		*	*		*	ppm of FSR/°C
Analog Offset	−30		+30	*		*	*		*	ppm of V_{NOM}/°C
Gain Drift	−30		+30	*		*	*		*	ppm of FSR/°C
Gain Drift (I_{OUT})	−100		+100	*		*	*		*	ppm of FSR/°C
REFERENCE INPUT										
Input Resistance										
5.0 V		5			5			5		kΩ
1.25 V		5			5			5		kΩ
1.0 V		1			1			1		MΩ
Reference Range (T_{min} to T_{max})	10	100	120	10	100	120	10	100	120	% of V_{NOM}
DATA INPUT										
Logic Level (T_{min} to T_{max})										
V_{IH}	2.0		7.0	*		*	*		*	V
V_{IL}	0.0		0.8	*		*	*		*	V
Logic Currents (T_{min} to T_{max})										
I_{IH}	−10		+10	*		*	−10		+10	μA
I_{IL}	0	60	100	*		*	0	100	200	−μA
V_{TH} Pin Voltage		1.4			*			1.4		V
CODING	BINARY, OFFSET BINARY									
CURRENT OUTPUT RANGES				0 to 10.24, ±5.12						mA
VOLTAGE OUTPUT RANGES				0 to 1.024, ±0.512						V
OUTPUT COMPLIANCE	−2		+1.2	*		*	*		*	V
OUTPUT RESISTANCE										
Exclusive of R_L	160	200	240	*	*	*	*	*	*	Ω
Inclusive of R_L	99	100	101	*	*	*	*	*	*	Ω
REFERENCE AMPLIFIER										
Input Bias Current		1.5			*			*		μA
Slew Rate		3			*			*		% of FS/ns
Large Signal Bandwidth		20			*			*		MHz
Small Signal Bandwidth		25			*			*		MHz
Undervoltage Recovery Time										
V_{REF}/V_{NOM} to 0%		500			*			*		ns
V_{REF}/V_{NOM} to 1%		120			*			*		ns

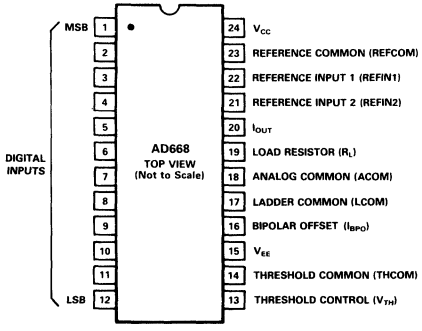
This information applies to a product under development. Its characteristics and specifications are subject to change without notice Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Model	AD668J Min	AD668J Typ	AD668J Max	AD668K Min	AD668K Typ	AD668K Max	AD668 Min	AD668 Typ	AD668 Max	Units
SETTLING TIME										
Analog (10% to 120% Step)										
to ±1%		60			*			*		ns to 1% of FSR
to ±0.1%		90			*			*		ns to 0.1% of FSR
to ±0.025%		120			*			*		ns to 0.025% of FSR
Digital										
Current to										
±1%		TBD			*			*		ns to 1% of FSR
±0.025%		50			*			*		ns to 0.025% of FSR
Voltage (100 Ω, Internal R_L)[3]										
to 1%		25			*			*		ns to 1% of FSR
to 0.01%		50			*			*		ns to 0.1% of FSR
0 to 0.025%		80			*			*		ns to 0.025% of FSR
Glitch Impulse[4]		350			*			*		pV-sec
Peak Amplitude		20			*			*		% of FSR
POWER REQUIREMENTS										
+10.8 V to +16.5 V		27	**32**			*			*	mA
−10.8 V to −16.5 V		7	**9**			*			*	−mA
Power Dissipation		510	615			*			*	mW
PSRR[5]			**0.05**			*			*	% of FSR/V
TEMPERATURE RANGE										
Rated Specification[2]	0		+70	*		*	−55		+125	°C
Storage	−65		+150	*		*	*		*	°C
PACKAGE OPTION[6]										
Cerdip (Q-24)		AD668JQ			AD668KQ			AD668SQ		

NOTES
[1]Measured in I_{OUT} mode. Specified at nominal full-scale reference.
[2]Measured in V_{OUT} mode, unless otherwise specified.
[3]Total resistance.
[4]At the major carry, driven by HCMOS logic.
[5]Measured at 15 V ±10% and 12 V ±10%.
[6]See Section 14 for package outline information.

*Same as AD668J.
Specifications shown in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The AD668 is designed to combine excellent performance with maximum flexibility. The functional block diagram and the simple transfer functions provided below will provide the user with a basic grasp of AD668's operation. Examples of typical circuit configurations are provided in the section APPLYING THE AD668. Subsequent sections contain more detailed information useful in optimizing DAC performance in high-speed, high resolution applications.

DAC Transfer Function

The AD668 may be used either in a current-output mode (with the DAC output connected to a virtual ground) or a voltage-output mode (DAC output connected to a resistive load.)

In current output mode:

Unipolar Mode

$$I_{OUT} = \frac{V_{IN}}{V_{NOM}} \times \frac{\text{DAC code}}{4096} \times 10.24\ \text{mA}$$

Bipolar Mode

$$I_{OUT} = \frac{V_{IN}}{V_{NOM}} \times \frac{\text{DAC code}}{4096} \times 10.24\ \text{mA} - \frac{V_{IN}}{V_{NOM}} \times 5.12\ \text{mA}$$

In voltage output mode:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

(for both unipolar and bipolar modes)

Where:

V_{IN} – the analog input voltage.

V_{NOM} – the nominal full scale of the reference voltage: 1 V, 1.25 V, or 5 V, determined by the wiring configuration of Pins 21 and 22. (See APPLYING THE AD668.)

DAC code – the numerical representation of the DAC's digital inputs; a number between 0 and 4095.

R_{LOAD} – the resistance of the DAC output node; the maximum this can be is 200 Ω (the internal DAC ladder resistance). The on-board load resistor (Pin 19) has been trimmed so that its parallel combination with the DAC ladder resistance is 100 Ω (±1%).

Bipolar mode – produces a bipolar analog output from the digital input by offsetting the normal output current with a precision current source. This offset is achieved by connecting Pin 16 to the DAC output. In the unipolar mode, Pin 16 should be grounded.

Operating Limits:

$$0.1 < \frac{V_{IN}}{V_{NOM}} < 1.2$$

$0 < V_{IN}/V_{NOM} < 0.1$ constitutes an undervoltage condition and is subject to the specified recovery time.

$1.2 < V_{IN}/V_{NOM}$ constitutes an overvoltage condition. This can saturate the DAC transistors, resulting in decreased response time and can, over extended time, damage the part through excessive power dissipation.

The small signal 3 dB bandwidth of the V_{IN} channel is 25 MHz. The large signal 3 dB bandwidth is approximately 20 MHz.

V_{OUT} is limited by the specified output compliance: −2 V to +1.2 V.

APPLYING THE AD668

The following are some typical circuit configurations for the AD668. These represent only a sample of possible implementations.

5 V REFIN, 1 V UNIPOLAR, UNBUFFERED VOLTAGE OUTPUT

Figure 1 shows a typical topology for generating an unbuffered voltage output. R_L (Pin 19) is grounded, producing a 100 Ω DAC output resistance that generates a 1.024 V output when the DAC current is at its full scale of 10.24 mA. The presence of low impedance loads will effect the output voltage swing directly: an external load of 300 Ω will yield a total output resistance of 75 Ω, and a full scale output of 0.768 V. An external 100 Ω will reduce the total output resistance to 50 Ω and the full scale voltage swing will drop to 0.512 V. Since the bipolar offset current is not used in this configuration, Pin 16 is connected to the analog ground plane.

The input divider has been connected to produce a 5 V full scale reference input by shorting REFIN1 to the analog ground plane and using REFIN2 as the reference input. With a 5 V nominal full scale, the 10% to 120% reference input range falls between 0.5 V and 6 V. The effective input resistance in this mode is 5 kΩ (±20%). The ratio of the input divider has been intentionally skewed by 50 Ω to provide an optional external fine trim for gain adjust. A trim range of ±1% is provided by the 100 Ω trimming potentiometer shown in Figure 1. If trimming is not desired, a 50 Ω resistor may be used in place of the potentiometer to produce the specified gain accuracy, or, if a +1% nominal gain error is tolerable, the resistor may be omitted altogether.

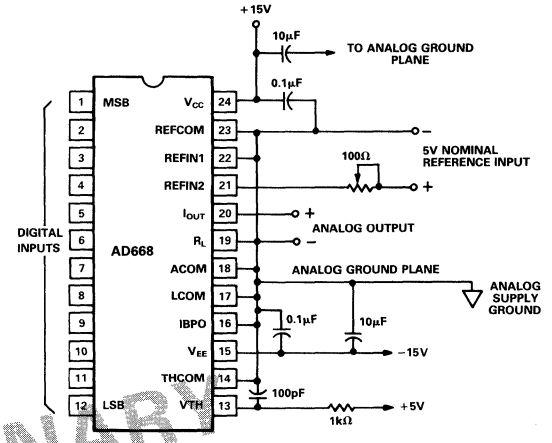


Figure 1. 5 V REFIN, 1 V Unipolar Unbuffered Voltage Output

5 V REFIN, 2 V BIPOLAR, UNBUFFERED VOLTAGE OUTPUT

Figure 2 demonstrates how a larger unbuffered voltage output swing can be realized. R_{LOAD} (Pin 19) is tied to the DAC output (Pin 20) to produce an output resistance of roughly 200 Ω. It should be noted that this impedance is not trimmed, and may vary by as much as 20%, but this can be compensated by adjusting the reference voltage. It is also important to note that limitations in the DAC output compliance would prohibit use of a 2 V unipolar output voltage swing.

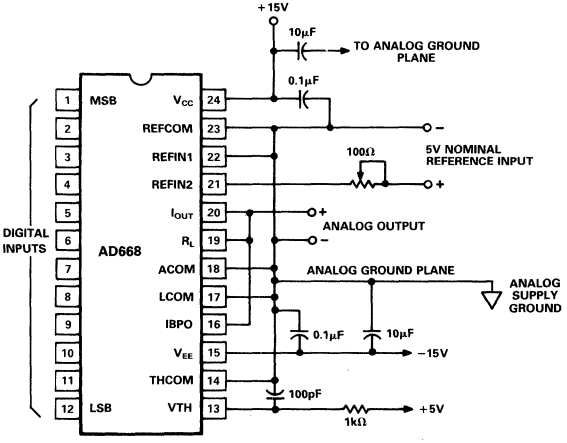


Figure 2. 5 V REFIN, −1 V to +1 V Unbuffered Bipolar Voltage Output

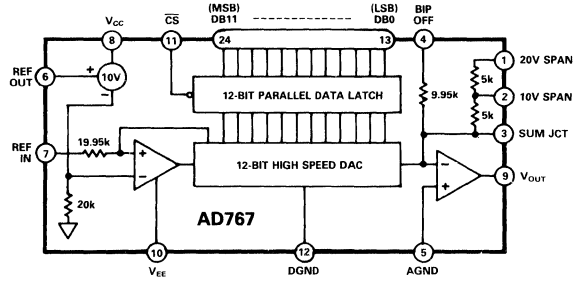
Microprocessor-Compatible 12-Bit D/A Converter

AD767*

FEATURES

- **Complete 12-Bit D/A Function**
  - **On-Chip Output Amplifier**
  - **High Stability Buried Zener Reference**
- **Fast 40ns Write Pulse**
- **0.3" Skinny DIP and PLCC Packages**
- **Single Chip Construction**
- **Monotonicity Guaranteed Over Temperature**
- **Settling Time: 3μs max to 1/2LSB**
- **Guaranteed for Operation with ±12V or ±15V Supplies**
- **TTL/5V CMOS Compatible Logic Inputs**

AD767 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD767 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener reference and input latch on a single chip. The converter uses 12 precision high-speed bipolar current steering switches and a laser-trimmed thin-film resistor network to provide high accuracy.

Microprocessor compatibility is achieved by the on-chip latch. The design of the input latch allows direct interface to 12-bit buses. The latch responds to strobe pulses as short as 40ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance of the AD767 result from a combination of advanced switch design, high-speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD767 is thus well suited for wide temperature range performance with ± 1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain T.C. is 5ppm/°C.

PRODUCT HIGHLIGHTS

1. The AD767 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The input latch responds to write pulse widths as short as 40ns assuring direct interface with the industry's fastest microprocessors.
3. The internal buried Zener reference is laser-trimmed to 10.00 volts with a ± 1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser trimmed for minimum full-scale and bipolar offset errors.
5. The precision high-speed current steering switches and on-board high-speed output amplifier settle within 1/2LSB for a 10V full-scale transition in 3.0μs when properly compensated.

***Covered by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.**

SPECIFICATIONS (T_A = +25°C, ±15 volt power supplies, Unipolar Mode, unless otherwise noted)

Model	AD767J/A/S[1]			AD767K/B			AD767A[2] Chips			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIGITAL INPUTS										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible, $T_{min}-T_{max}$)[3]										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0") J, K, A, B	0		+0.8	0		+0.8	0		+0.8	V
V_{IL} (Logic "0") S	0		+0.7							V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10		3	10	μA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5		1	5	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C		±1/2	±1		±1/8	±1/2		±1/2	±1	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±1		±1/4	±1/2		±1/2	±1	LSB
Differential Linearity Error @ +25°C		±1/2	±1		±1/4	±1		±1/2	±1	LSB
$T_A = T_{min}$ to T_{max}	Monotonicity Guaranteed			Monotonicity Guaranteed			Monotonicity Guaranteed			LSB
Gain Error[4]		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	% of FSR[5]
Unipolar Offset Error[4]		±1	±2		±1	±2		±1	±2	LSB
Bipolar Zero Error[4]		±0.05	±0.1		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT										
Gain T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15		±5	±30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10		±5	±10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ±0.01% of FSR for										
FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Ranges[6]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short-Circuit Current			40			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY										
V_{CC} = +11.4 to +16.5V dc		5	10		5	10		5	10	ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	10		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±12, ±15			±12, ±15			±12, ±15		V
Range[6]	±11.4		±16.5	±11.4		±16.5	±11.4		±16.5	V
Supply Current										
+11.4 to +16.5V dc		9	13		9	13		9	13	mA
−11.4 to −16.5V dc		18	23		18	23		18	23	mA
Total Power Consumption		400	600		400	600		400	600	mW
TEMPERATURE RANGE										
J/K	0		+70	0		+70				°C
A/B	−25		+85	−25		+85	−25		+85	°C
S	−55		+125	−55		+125				°C
Operating	−55		+125	−55		+125				°C
Storage (All Grades)	−65		+125	−65		+125	−65		+125	°C

NOTES

[1]AD767 "S" specifications shown for information only. Consult Analog Devices Military Databook or contact factory for a controlled specification sheet.

[2]AD767A Chips specifications are tested at +25°C and, when in boldface, at +85°C. They are typical at −25°C.

[3]The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.

[4]Adjustable to zero.

[5]FSR means "Full-Scale Range" and is 20V for ±10V range and 10V for the ±5V range.

[6]A minimum power supply of ±12.5V is required for a ±10V full-scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test (except per Notes 1 and 2). Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

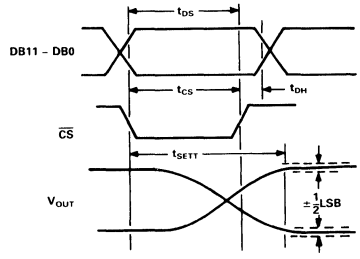
V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 11, 13–24)
to Power Ground . . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out, V_{OUT} (Pins 6, 9) . . Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

TIMING SPECIFICATIONS

(All Models, $T_A = 25°C$, $V_{CC} = +12V$ or $+15V$, $V_{EE} = -12V$ or $-15V$)

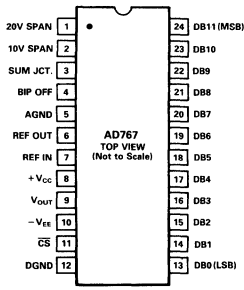


Symbol	Parameter	Min	Typ	Max	
t_{DS}	Data Valid to End of $\overline{CS}$	40	–	–	ns
	(−25°C to +85°C)	60	–	–	ns
	(−55°C to +125°C)	90	–	–	ns
t_{DH}	Data Hold Time	10	–	–	ns
	(−25°C to +85°C)	10	–	–	ns
	(−55°C to +125°C)	20	–	–	ns
t_{CS}	$\overline{CS}$ Pulse Width	40	–	–	ns
	(−25°C to +85°C)	60	–	–	ns
	(−55°C to +125°C)	90	–	–	ns
t_{SETT}	Output Voltage Settling Time*	–	2	4	µs

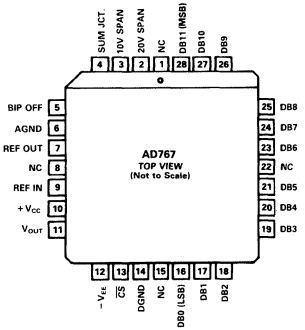
*t_{SETT} is measured referenced to the leading edge of t_{CS}. If $t_{CS} > t_{DS}$, then t_{SETT} is measured referenced to the beginning of Data Valid.

PIN CONFIGURATION

DIP



PLCC



AD767 ORDERING GUIDE

Model	Package Options*	Temperature Range °C	Linearity Error Max $T_{min}-T_{max}$	Gain T.C. Max ppm/°C
AD767JN	Plastic DIP (N-24)	0 to +70	±1LSB	30
AD767JP	PLCC (P-28A)	0 to +70	±1LSB	30
AD767KN	Plastic DIP (N-24)	0 to +70	±1/2LSB	15
AD767KP	PLCC (P-28A)	0 to +70	±1/2LSB	15
AD767AD	Ceramic DIP (D-24A)	−25 to +85	±1LSB	30
AD767BD	Ceramic DIP (D-24A)	−25 to +85	±1/2LSB	15
AD767SD/883B	Ceramic DIP (D-24A)	−55 to +125	±1LSB	30
AD767A Chips	N/A	−25 to +85	±1LSB	30

*See Section 14 for package outline information.

Analog Circuit Details

THE AD767 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. This is also referred to as relative accuracy. The AD767 is laser trimmed to typically maintain linearity errors at less than ±1/8LSB for the K and B versions and ±1/2LSB for the J, A and S versions. Linearity over temperature is also held to ±1/2LSB (K/B) or ±1LSB (J/A/S).

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD767 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C as well as over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full-scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be −1.83mV, or −3/4LSB.

GAIN ERROR: DAC gain error is a measure of the difference between an ideal DAC and the actual device's output span. All grades of the AD767 have a maximum gain error of 0.2% FS. However, if this is not sufficient, the error can easily be adjusted to zero (see Figures 2 and 3).

UNIPOLAR OFFSET ERROR: Unipolar offset error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured when the AD767 is configured for unipolar outputs. It is present for all codes and is measured with all "0s" in the DAC latches. This is easily adjustable to zero when required.

BIPOLAR ZERO ERROR: Bipolar zero errors result from errors produced by the DAC and output amplifier when the AD767 is configured for bipolar output. Again, as with unipolar offset and gain errors, this is easily adjusted to zero when required.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD767 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V.

Gain and offset drift are minimized in the AD767 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table I.

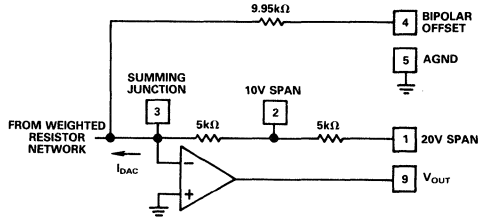


Figure 1. Output Amplifier Voltage Range Scaling Circuit

UNIPOLAR CONFIGURATION (Figure 2)

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar offset terminal, Pin 4, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and Pin 4 should be connected to Pin 5.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2 until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.)

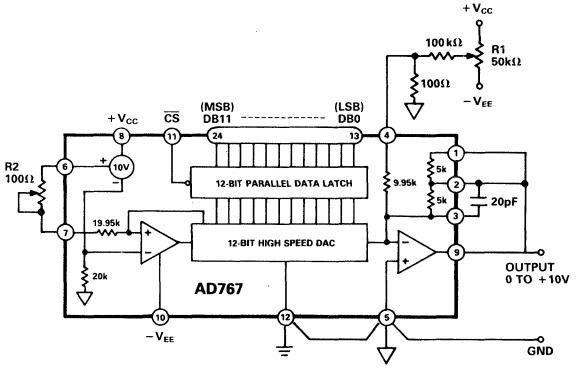


Figure 2. 0 to +10V Unipolar Voltage Output

Output Range	Digital Input Codes	Connect Pin 9 to	Connect Pin 1 to	Connect Pin 2 to	Connect Pin 4 to
±10V	Offset Binary	1	9	NC	6 (through 50Ω fixed or 100Ωtrim resistor)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (through 50Ω fixed or 100Ωtrim resistor)
±2.5V	Offset Binary	2	3	9	6 (through 50Ω fixed or 100Ωtrim resistor)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (or optional trim – See Figure 2)
0 to +5V	Straight Binary	2	3	9	5 (or optional trim – See Figure 2)

Table I. Output Voltage Range Connections

BIPOLAR CONFIGURATION (Figure 3)

This configuration will provide a bipolar output voltage from −5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1s).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give −5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

STEP III . . . BIPOLAR ZERO ADJUST (Optional)

In applications where an accurate zero output is required, set the MSB ON, all other bits OFF, and readjust R1 for zero volts output.

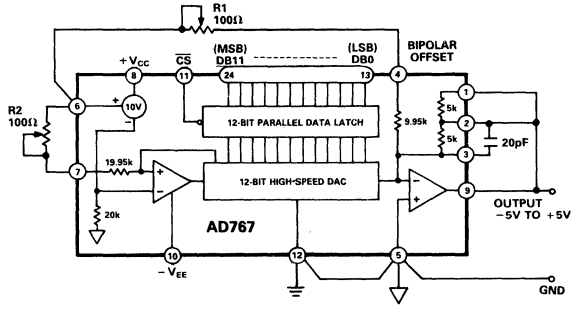


Figure 3. ±5V Bipolar Voltage Output

INTERNAL/EXTERNAL REFERENCE USE

The AD767 has an internal low-noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high-speed DAC and will give long-term stability equal or superior to the best discrete Zener reference diodes. The performance of the AD767 is specified with the internal reference driving the DAC since all trimming and testing (especially for full-scale error and bipolar offset) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset). A minimum of 0.1mA is available for driving external loads.

The AD767 reference output should be buffered with an external op amp if it is required to supply more than 0.1mA output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full-scale TC for a particular grade.

If an external reference is used (10.000V, for example), additional trim range must be provided, since the internal reference has a tolerance of ±1%, and the AD767 full-scale and bipolar offset are both trimmed with the internal reference. The gain and offset trim resistors give about ±0.25% adjustment range, which is sufficient for the AD767 when used with the internal reference.

It is also possible to use external references other than 10 volts. The recommended range of reference voltage is from +8 to +10.5 volts, which allows both 8.192V and 10.24V ranges to be used. The AD767 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range in a particular application, a CMOS multiplying DAC is a better choice.

Reduced values of reference voltage will also permit the ±12 volt ±5% power supply requirement to be relaxed to ±12 volts ±10%.

It is not recommended that the AD767 be used with external feedback resistors to modify the scale factor. The internal resistors are trimmed to ratio-match and temperature-track the other resistors on the chip, even though their absolute tolerances are ±20%, and absolute temperature coefficients are approximately −50ppm/°C. If external resistors are used, a wide trim range (±20%) will be needed and temperature drift will be increased to reflect the mismatch between the temperature coefficients of the internal and external resistors.

Small resistors may be added to the feedback resistors in order to accomplish small modifications in the scaling. For example, if a 10.24V full scale is desired, a 140Ω 1% low-TC metal-film resistor can be added in series with the internal (nominal) 5k feedback resistor, and the gain trim potentiometer (between Pins 6 and 7) should be increased to 200Ω. In the bipolar mode, increase the value of the bipolar offset trim potentiometer also to 200Ω.

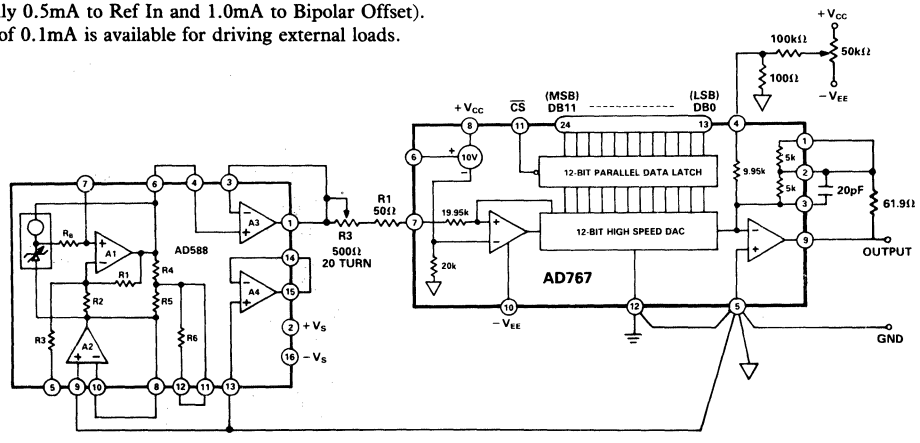


Figure 4. Using the AD767 with the AD588 High Precision Reference

USING THE AD767 WITH THE AD588 HIGH PRECISION VOLTAGE REFERENCE

The AD767 is specified for gain drift from 15ppm/°C to 30ppm/°C (depending on grade) using its internal 10 volt reference. Since the internal reference contributes the majority of this drift, an external high-precision voltage reference will greatly improve performance over temperature. As shown in Figure 4, the 10 volt output from the AD588 is used as the reference. With a 1.5ppm/°C output voltage drift the AD588 contributes less than 1/2LSB gain drift when used with the AD767 over the industrial temperature range. Using this combination may result in apparent increases in full-scale error due to the differences between the internal reference by which the device is laser trimmed and the external reference with which the device is actually applied. The AD767 internal reference is specified to be 10 volts ±100mV whereas the AD588 is specified as 10 volts ±1mV. This may result in up to 101mV of apparent full-scale error beyond the ±25mV specified AD767 gain error. The 500Ω potentiometer in series with the reference input allows adequate trim range to null this error.

GROUNDING RULES

The AD767 brings out separate analog and power grounds to allow optimum connections for low noise and high-speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths.

The analog ground at Pin 5 is the ground point for the output amplifier and is thus the "high quality" ground for the AD767; it should be connected directly to the analog reference point of the system. The power ground at Pin 12 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

It is also important to apply decoupling capacitors properly on the power supplies for the AD767. The correct method for decoupling is to connect a capacitor from each power supply pin of the AD767 to the analog ground pin of the AD767. Any load driven by the output amplifier should also be referred to the analog ground pin.

OPTIMIZING SETTLING TIME

The dynamic performance of the AD767's output amplifier can be optimized by adding a small (20pF) capacitor across the feedback resistor. Figure 5 shows the improvement in both large-signal and small-signal settling for the 10V range. In Figure 5a, the top trace shows the data inputs (DB11–DB0 tied together), the second trace shows the CS pulse, and the lower two traces show the analog outputs for C_F = 0 and 20pF respectively.

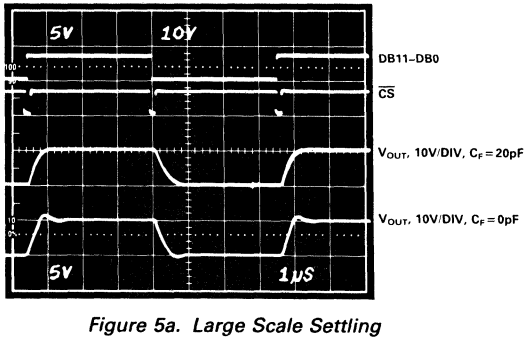


Figure 5a. Large Scale Settling

Figures 5b and 5c show the settling time for the transition from all bits on to all bits off. Note that the settling time to ±1/2LSB for the 10V step is improved from 2.4 microseconds to 1.6 microseconds by the addition of the 20pF capacitor.

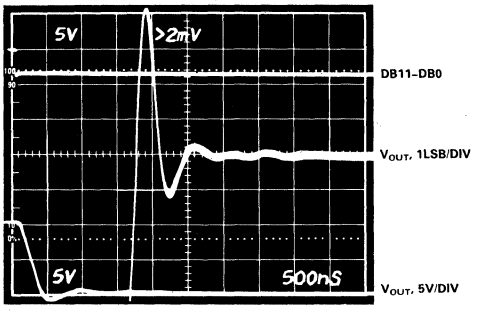


Figure 5b. Fine-Scale Settling, C_F = 0pF

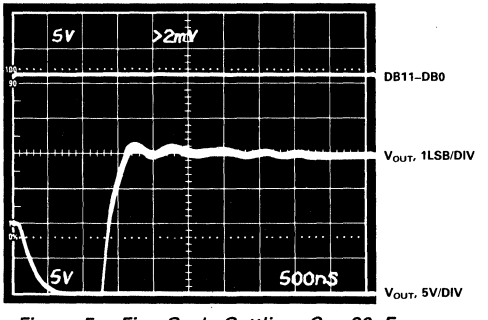


Figure 5c. Fine-Scale Settling, C_F = 20pF

Figures 5d and 5e show the settling time for the transition from all bits off to all bits on. The improvement in settling time gained by adding C_C = 20pF is similar.

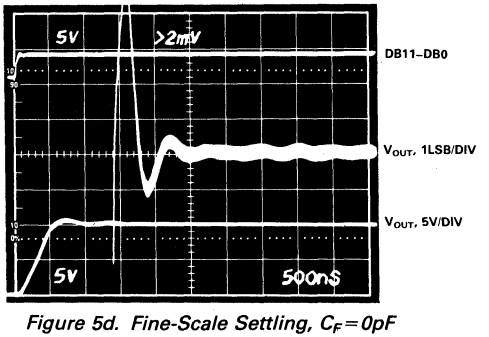


Figure 5d. Fine-Scale Settling, C_F = 0pF

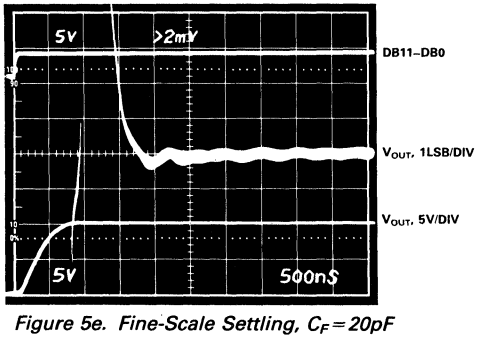


Figure 5e. Fine-Scale Settling, C_F = 20pF

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not change with supply voltage. Thus the AD767 digital interface may be driven with any of the popular types of 5 volt logic.

A good engineering practice is to connect unused inputs to power ground to improve noise immunity. Unconnected data and control inputs will float to logic 0 if left open.

The low digital input current of the AD767 eliminates the need for buffer/drivers required by many monolithic converters using bipolar technology. A single low-power Schottky gate, for example, will drive several AD767s when connected to a common bus.

INPUT CODING

The AD767 uses positive-true binary input coding. Logic "1" is represented by an input voltage greater than 2.0V, and logic "0" is defined as an input voltage less than 0.8V.

Unipolar coding is straight binary, where all zeroes (000_H) on the data inputs yields a zero analog output and all ones (FFF_H) yields an analog output 1LSB below full scale.

Bipolar coding is offset binary, where an input code of 000_H yields a minus full-scale output, an input of FFF_H yields an output 1LSB below positive full scale, and zero occurs for an input code with only the MSB on (800_H).

The AD767 can be used with twos complement input coding if an inverter is used on the MSB (DB11).

MICROPROCESSOR INTERFACE

The AD767, with its 40ns minimum $\overline{CS}$ pulse width, may be easily interfaced to any of today's high-speed microprocessors. The 12-bit single buffered input register will accept 12-bit parallel data from processors such as the 68000, 8086, TMS320 series, and the Analog Devices ADSP-2100. Several illustrative examples follow.

68000 – AD767 INTERFACE

Figure 6 illustrates the AD767 interface to a 68000 microprocessor. An active low decoded address is OR'ed with the processor's R/$\overline{W}$ signal to provide $\overline{CS}$ and latch data into the AD767. Later in the bus cycle the processor issues the upper ($\overline{UDS}$) and lower ($\overline{LDS}$) data strobes which are gated with the decoded address to provide $\overline{DTACK}$ and terminate the bus cycle. As shown, this interface will support a 12.5MHz 68000 system.

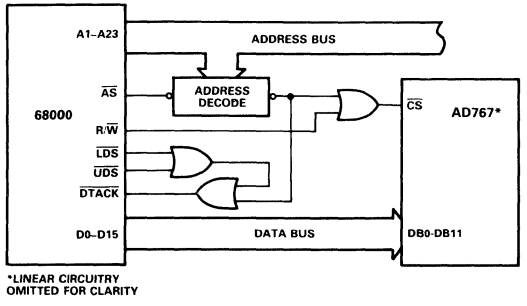


Figure 6. 68000 – AD767 Interface

8086 – AD767 INTERFACE

Interfacing the AD767 to the 8086 16-bit microprocessor requires a minimal amount of external components. A 10MHz 8086, for example, generates a 165ns low write pulse which may be gated with a decoded address to provide $\overline{CS}$ for the AD767. As $\overline{WR}$ returns high valid data is latched into the DAC. See Figure 7.

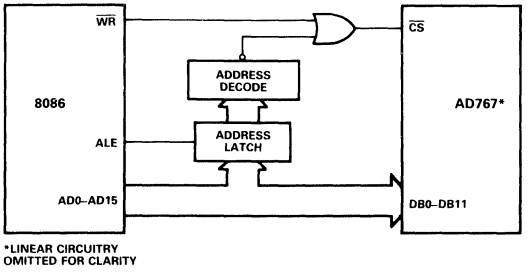


Figure 7. 8086 – AD767 Interface

TMS32010 – AD767 INTERFACE

The high-speed digital interface of the AD767 facilitates its use with the TMS32010 microprocessor at speeds up to 20MHz. In the three multiplexed LSBs of the address bus, PA2 – PA0 are decoded as a port address and OR'ed with the low write enable to generate $\overline{CS}$ for the DAC. A simple OUT xx,y instruction will output the data word stored in memory location xx to any one of eight port locations y.

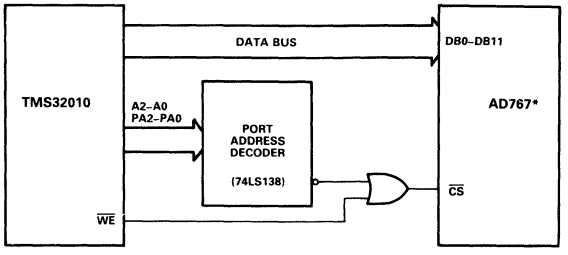


Figure 8. TMS32010 – AD767 Interface

TMS32020 – AD767 INTERFACE

Interfacing the AD767 to the TMS32020 microprocessor is easily achieved by using the TMS32020 I/O port capability. The $\overline{IS}$ signal distinguishes the I/O address space from the local program/data memory space and is used to enable a 74LS138 decoder. The decoded port address is then gated with the R/$\overline{W}$ and $\overline{STRB}$ signals to provide the AD767 $\overline{CS}$.

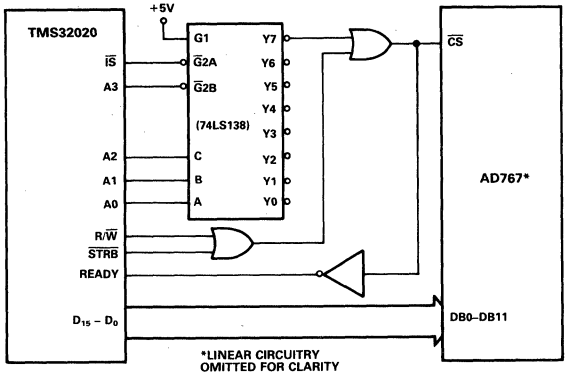


Figure 9. TMS32020 – AD767 Interface

ADSP-2100 – AD767 INTERFACE

The ADSP-2100 single chip DSP processor may be interfaced to the AD767 as shown in Figure 10. With a clock frequency of 32MHz, and instruction execution in a single 125ns cycle, the processor will support the AD767 interface with a single wait state.

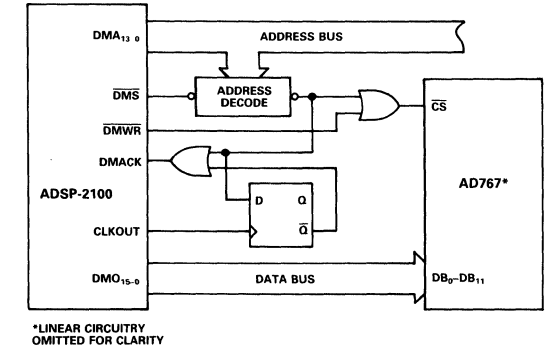


Figure 10. ADSP-2100 – AD767 Interface

At the beginning of the data memory access cycle the processor provides a 14-bit address on the DMA bus. The $\overline{DMS}$ signal is then asserted enabling a LOW address decode. Valid data is now placed on the data bus and $\overline{DMWR}$ is issued. $\overline{DMWR}$ is OR'ed with the LOW address decode to generate the AD767 $\overline{CS}$.

The LOW decoded address is also gated with the $\overline{Q}$ output of a D flip-flop to hold DMACK (Data Memory Acknowledge) LOW. This forces the processor into a wait state and extends the AD767 $\overline{CS}$ by 1 clock cycle. The rising edge of CLKOUT latches $\overline{Q}$ HIGH bringing DMACK HIGH. The cycle is now complete.

TMS320C25 – AD767 INTERFACE

Figure 11 illustrates the AD767 interface to a TMS320C25 digital signal processor. Due to the high-speed capability of the processor (40MHz), a single wait state is required and is easily generated using MSC. A 20MHz TMS320C25 however, does not require wait states and should be interfaced using the circuit shown in Figure 9.

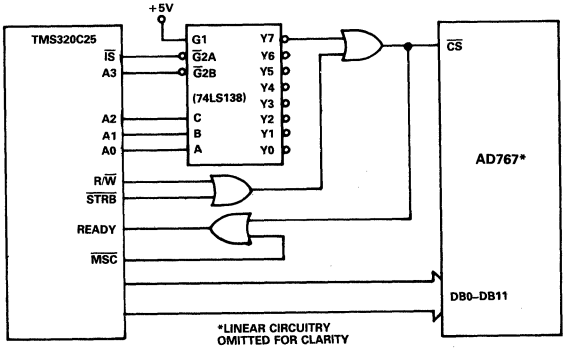


Figure 11. TMS320C25 – AD767 Interface

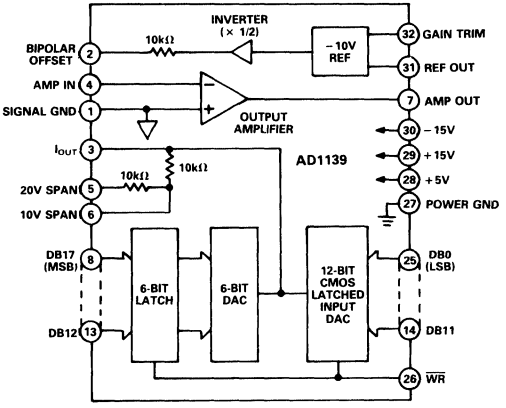
High Accuracy, 18-Bit Digital-to-Analog Converter

AD1139

FEATURES
- **18-Bit Resolution**
- **Low Nonlinearity**
  - **Differential: ±1/2LSB max**
  - **Integral: ±1/2LSB max**
- **High Stability**
  - **Differential TC: ±1ppm/°C max**
  - **Integral TC: ±1/2ppm/°C max**
  - **Gain TC (with Reference): ±4ppm/°C max**
- **Fast Settling**
  - **Full Scale: 40μs to ±0.00019%**
  - **LSB: 6μs to ±0.00019%**
- **Small Hermetic 32-Lead Triple DIP Package**
- **Low Cost**

APPLICATIONS
- **Automatic Test Equipment**
- **Scientific Instrumentation**
- **Beam Positioners**
- **Digital Audio**

AD1139 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD1139 is the first DAC offering 18-bit resolution (1 part in 262,144) and true 18-bit accuracy in a component size hybrid package. A proprietary bit switching technique provides high accuracy, speed and stability without compromising small size or low cost.

The AD1139 is a complete DAC with precision internal reference, latched data inputs and a quality output voltage amplifier. The analog output voltage ranges are pin programmable to +5V, +10V, ±5V and ±10V. Current output is also provided for use with external amplifiers. The internal precision −10V reference has a low ±3ppm/°C maximum temperature coefficient and is available for ratiometric applications.

The AD1139K is a true 18-bit accurate DAC with ±1/2LSB maximum differential and integral nonlinearity. The differential and integral nonlinearity temperature stability is guaranteed at ±1ppm/°C maximum and ±1/2ppm/°C maximum, respectively.

The AD1139 settles to within ±1/2LSB at 18 bits (±0.00019%) in 40μs for a full-scale step (10V). The glitch energy is a low 400mV × 500ns for a major carry, and wideband output noise is only 15μV.

The AD1139 operates from ±15V dc and +5V dc power supplies. Digital inputs are 5V CMOS compatible with binary input coding for unipolar output ranges and offset binary coding for bipolar ranges.

PRODUCT HIGHLIGHTS

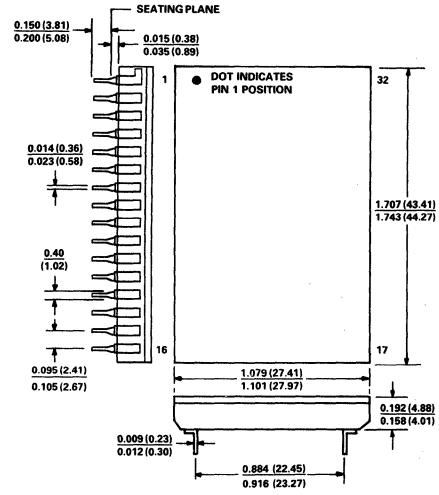
1. Eighteen-bit resolution with ±1/2LSB maximum differential and integral nonlinearity in a hermetic 32-lead triple DIP package.
2. Complete DAC with internal reference, stable low-noise output amplifier, latched DAC inputs, reference output and internal application resistors for programmable output voltage ranges.
3. Temperature compensated internal precision reference with ±0.1% maximum initial accuracy and ±3ppm/°C maximum tempco.
4. Four pin programmable output voltage ranges (+5V, +10V, ±5V, ±10V) and current output available (−1mA, ±0.5mA).
5. The 18-bit parallel input latch assists in microprocessor interface.
6. Accurate measurements of the DAC's output are unusually simple since the AD1139 does *not* suffer from code dependent ground current errors.
7. True analog output remote sense capability.

SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise specified)

Model	AD1139J	AD1139K
RESOLUTION	18 Bits	*
ACCURACY		
Differential Nonlinearity	±1LSB max	±1/2LSB max
	(= ±0.00038% max)	(= ±0.00019% max)
Integral Nonlinearity	±1LSB max	±1/2LSB max
	(= ±0.00038%max)	(= ±0.00019% max)
Monotonicity (18 Bits)	Guaranteed	*
Initial Errors[1]		
Unipolar Gain Error	±0.01%	*
Bipolar Gain Error	±0.02%	*
Offset Error	±0.01%	*
Bipolar Offset Error	±0.01%	*
STABILITY (ppm FSR[2]/°C)		
Differential Nonlinearity[3]	±1 max	±0.5 typ, ±1 max
Integral Nonlinearity[3]	±0.5 max	*
Gain (Including V_{REF})	±4 max	*
Offset		
Unipolar Mode	±1 max	*
Bipolar Mode	±1 max	*
STABILITY (Long Term, ppm FSR[2]/1000 hour)		
Differential Nonlinearity[4]	±0.5	*
Gain (Including V_{REF})	±15	*
Offset	±1	*
Bipolar Offset	±2	*
Reference Output Voltage	±15	*
WARMUP TIME (MINIMUM)	15 minutes	*
REFERENCE VOLTAGE (V_{REF})		
Output Voltage (@ 5 mA max)	−10V (±0.1% max)	*
Noise (BW = 0.1-10Hz)	20μV pk-pk	10μV pk-pk
Noise (BW = 100kHz)	50μV rms	*
Tempco	3ppm/°C max	*
DYNAMIC PERFORMANCE		
Settling Time to 1/2LSB (@ 18 Bits)[5]		
Voltage		
Unipolar (10V Step)	40μs	*
Bipolar (20V Step)	60μs	*
Unipolar (LSB Step)	6μs	*
Bipolar (LSB Step)	8μs	*
Slew Rate	2V/μs	*
Current[6]		
Full-Scale Step	10μs	*
LSB Step	6μs	*
Glitch Energy (Major Carry		
@ 20MHz Bandwidth 0-to-10V Range)	400mV (500ns Duration)	*
DIGITAL INPUTS (5V CMOS Compatible)		
V_{IL}	≤0.8V	*
V_{IH}	≥3.5V	*
Unipolar Code	Binary (BIN)	*
Bipolar Code	Offset Binary (OBN)	*
ANALOG OUTPUT		
Current[4]	−1mA, ±0.5mA	*
Voltage (Pin Programmable)	+5V, +10V, ±5V, ±10V	*
Noise (Includes V_{REF})		
BW = 0.1-10Hz (μV pk-pk)	2×FSR	1×FSR
BW = 100kHz (Unipolar)	15μV rms	*
BW = 100kHz (Bipolar)	45μV rms	*
VOLTAGE COMPLIANCE	±10mV	*
Source Resistance		
Unipolar	3.3kΩ	*
Bipolar	2.85kΩ	*
Source Capacitance	10pF	*
POWER SUPPLY REQUIREMENTS		
+5V dc (±5%)	100μA	*
±15V dc (±5%)	+25mA, −30mA	*
POWER SUPPLY REJECTION		
(±15V dc)		
Gain	±2.5ppm/%	*
Offset	±0.3ppm/%	*
Reference Output	±2.5ppm/%	*
(+5V dc)		
Differential Nonlinearity	±0.15ppm/%	*
TEMPERATURE RANGE		
Operating (Rated Performance)	0 to +70°C	*
Storage	−40°C to +85°C	

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

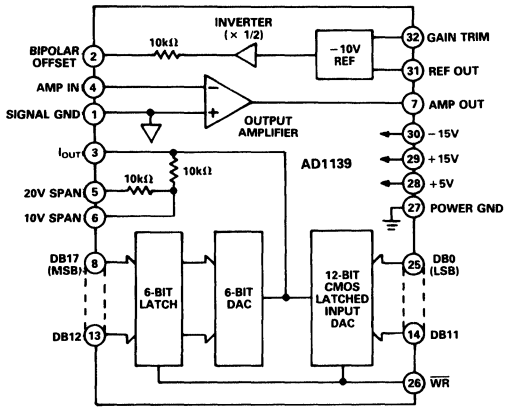


CAUTION: OBSERVE PROPER PLUG-IN POLARITY TO PREVENT DAMAGE TO CONVERTER

PIN DESIGNATIONS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	SIGNAL GND	32	GAIN TRIM
2	BIPOLAR OFFSET	31	REF OUT
3	I_{OUT}	30	−15V
4	AMP IN	29	+15V
5	20V SPAN	28	+5V
6	10V SPAN	27	POWER GND
7	AMP OUT	26	$\overline{WR}$
8	DB17 (MSB)	25	DB0 (LSB)
9	DB16	24	DB1
10	DB15	23	DB2
11	DB14	22	DB3
12	DB13	21	DB4
13	DB12	20	DB5
14	DB11	19	DB6
15	DB10	18	DB7
16	DB9	17	DB8

NOTES
*Specifications same as AD1139J.
[1]Initial Errors are adjustable to zero via external potentiometers (see Figure 1).
[2]FSR means Full-Scale Range.
[3]Temperature stability of linearity is guaranteed to a 1% AQL, Level II sampling plan per MIL-STD-105.
[4]See Figure 7 for typical long-term linearity stability vs. temperature. Also, see the BURN-IN section on page 6 for caution against preconditioning by the user.
[5]Figure 9 provides typical LSB and full-scale settling time to within 1/2LSB at 12- to 18-bit resolutions.
[6]Current Output Operation is structured for input to the summing junction of an amplifier.
Specifications subject to change without notice.



AD1139 Functional Block Diagram

ANALOG OUTPUT RANGE

The AD1139 is pin programmable to provide a variety of analog outputs, either current or voltage. A unipolar output current of 0 to −1mA is available at Pin 3 and can be offset by 0.5mA (connect Pin 2 to Pin 3) for a biolar output of ±0.5mA. Output voltage ranges (+5V, +10V, ±5V and ±10V) are available at Pin 7 by connecting the current output (Pin 3) to the amplifier input (Pin 4) and the appropriate internal feedback resistors to the amplifier output (Pin 7) as shown in Figure 1.

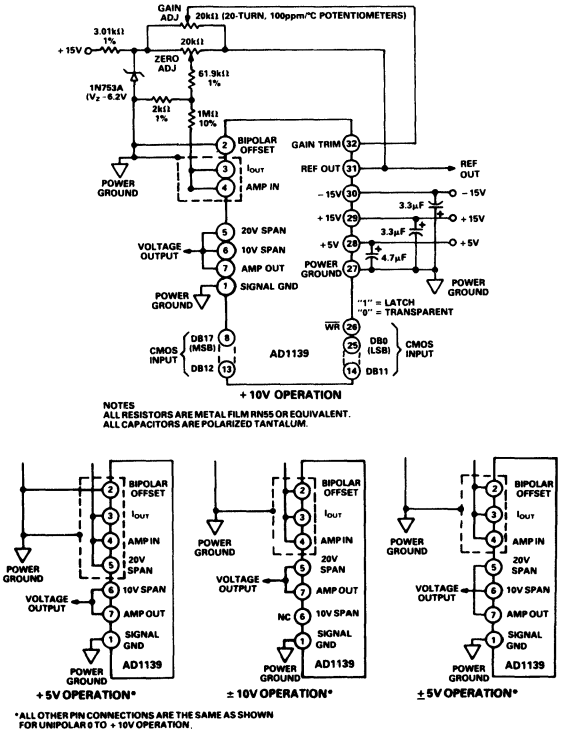


Figure 1. Output Voltage and Trim Configuration

OFFSET & GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 1. The offset adjust range is *plus 0.03% to minus 0.02% of full scale range* (wiper of potentiometer to REF OUT equals plus 0.03%). The gain adjust range is *plus 0.06% to minus 0.08% of full scale range* (wiper to REF OUT equals plus 0.06%). Measurement instruments used should be capable of resolving 1μV at plus full scale for the chosen output range and within 1μV of zero.

Procedure:

UNIPOLAR MODE

1. Apply a digital input of all "0s."
2. Adjust the offset potentiometer until a 0.000000V output is obtained.
3. Apply a digital input of all "1s."
4. Adjust the gain potentiometer until plus full-scale output is obtained (see Table I for exact value).

BIPOLAR MODE

1. Apply a digital input of 100 . . . . . 000.
2. Adjust the offset potentiometer until a 0.000000V output is obtained.
3. Apply a digital input of all "1s."
4. Adjust the gain potentiometer until plus full-scale output is obtained (see Table I for exact value).

	Code 000 00	Code 111 . . . 11	
Unipolar +5V	0.000000V	+4.999981V	
+10V	0.000000V	+9.999962V	
	Code 100 00	**Code 111 . . . .11**	**Code 000 . . . .00**
Bipolar ±5V	0.000000V	+4.999962V	− 5.000000V
±10V	0.000000V	+9.999924V	−10.000000V

Table I. Full-Scale and Offset Calibration Voltages

Symbol	Parameter	Requirement
t_{DS}	Data Setup Time	160ns min
t_{DH}	Data Hold Time	120ns min
t_{WR}	Write Pulse Width	200ns min

Table II. Timing Requirements

TIMING DIAGRAM & LATCH CONTROL

Timing requirements for the AD1139 are shown in Table II. The timing diagram is shown in Figure 2. The WRite line controls an 18-bit wide data input latch. This latch is transparent when the WRite line is LOW, allowing all bits to be accessed directly. When the WRite line is activated HIGH, the data present at the inputs is held in the latch and the appropriate analog voltage is seen at the output.

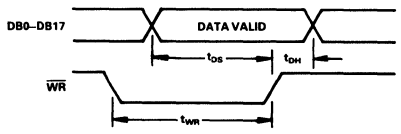


Figure 2. AD1139 Timing Diagram

GROUNDING & GUARDING

The current from measurement ground (Pin 1) is small and independent of the digital input code to the DAC. This greatly simplifies making error free analog measurements. Connect this high quality ground to the system's or application's high quality ground. Connect the DAC's power ground (Pin 27) to the system return, also connect the system's high quality ground to the system return. *It is most important that the measurement ground (Pin 1) and power ground (Pin 27) be connected externally for proper circuit operation.*

The current output pin (I_{OUT}, Pin 3) is sensitive to external noise sources, such as digital input lines. This pin and any components connected to this pin should be surrounded by a grounded guard as shown in Figure 3.

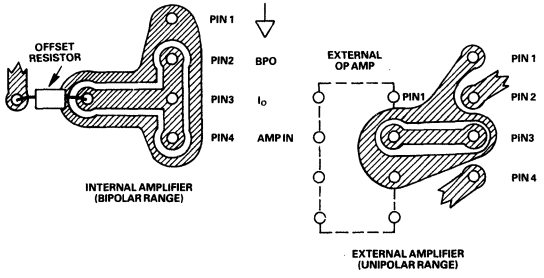


Figure 3. Guarding Recommendations

REMOTE SENSE APPLICATION

The AD1139's remote sense capability allows driving heavy loads or long cables without the usual, accompanying gain errors. By sensing at the load, as described in Figure 4, the load current will pass through the amplifier's output and the power ground, but not through the sense lines. The potential gain errors that would be induced by this load current are therefore minimized. The load should not exceed ± 10mA or 2 nanofarads to insure proper operation of the AD1139's internal output amplifier.

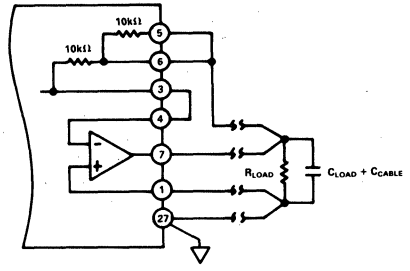


Figure 4. Remote Sensing

RATIOMETRIC DAC TESTING APPLICATION

The AD1139's highly stable reference output can be conveniently used in the testing of other high resolution DACs. Figure 5 describes how the REF OUT (Pin 31) is used as the external reference input to a device-under-test. The gain of the device-under-test will now accurately track the AD1139's gain and eliminate reference contribution to gain error.

When used as a reference DAC to test the integral and differential linearity of 14- and 16-bit DACs, the AD1139 provides a measurement capability with just 1/16LSB of uncertainty at 14 bits.

Gain and offset errors of the device-under-test (D.U.T.) may be accounted for in software. Once zeroed, the integral linearity error can be measured as the difference between the reference DAC (AD1139) and the D.U.T. as seen at the digital voltmeter.

The differential linearity error is then determined by incrementing or decrementing the D.U.T. digital input by 1LSB, and comparing the new output at the DVM with the previous output. The difference between these two measurements should be exactly one ideal LSB. The amount of disagreement from one ideal LSB is the differential linearity error.

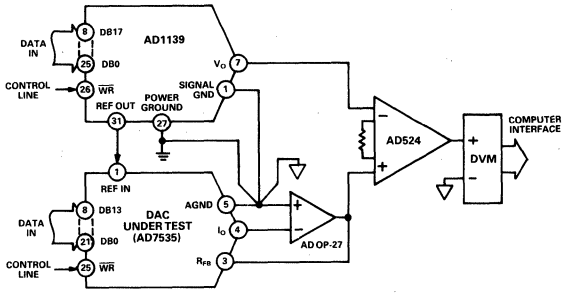


Figure 5. Ratiometric DAC Testing

IBM* PC INTERFACE

Figure 6 illustrates a typical IBM personal computer interface which uses three 8-bit external latches and two decoder chips. The three HCT374 latches are connected to the data bus (D0 through D7). The HCT138 decoder chip decodes the address bus and enables each latch, including the AD1139's internal DAC latch, to see the appropriate digital word. The HCT688 chip and the HCT138 decoder define the I/O address space where the four latches will reside. In the Figure 6 example, they reside in the address space as shown in Table III.

I/O Address	Selected Latch	Data Bits
380H	Low Byte	DB0–DB7
381H	Mid Byte	DB8–DB15
382H	High Byte	DB16, DB17
383H	AD1139 Latch	DB0–DB17

Table III. IBM Interface Address Locations

***IBM is a trademark of International Business Machines Corp.**

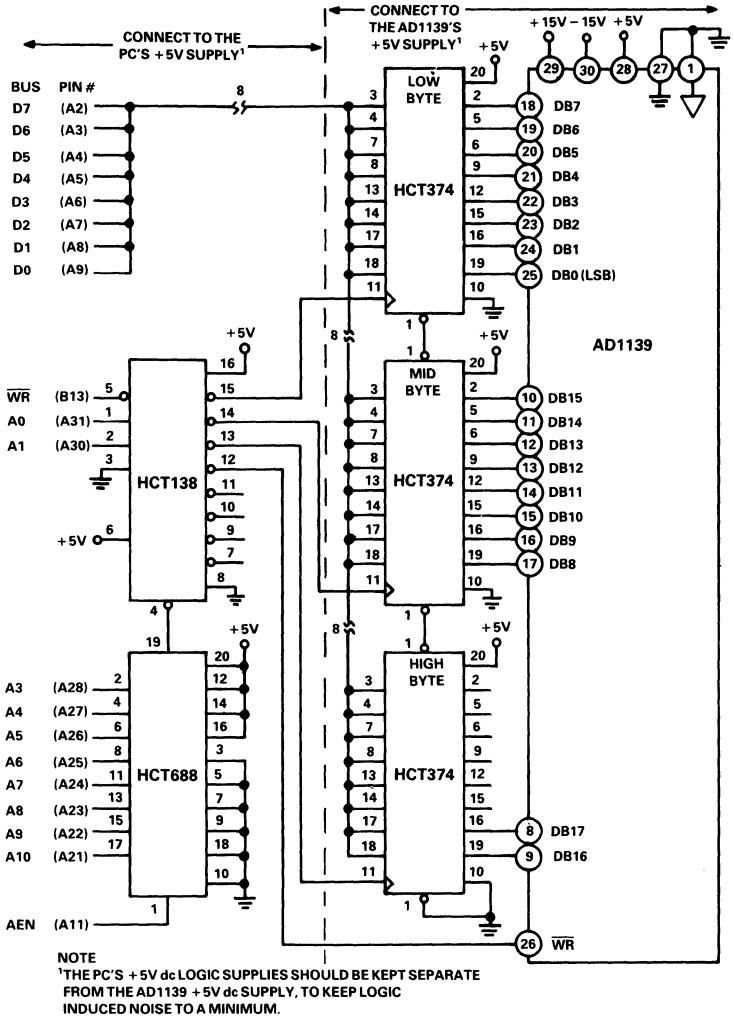


Figure 6. AD1139 to IBM PC Compatible Interface

LONG-TERM STABILITY VS. TEMPERATURE

Adjusting the linearity of any DAC after it is installed in the application is often difficult or impossible. It is preferable to maintain some specified accuracy over the useful working life of the product (commonly 5 to 10 years). Stable linearity performance over time can, therefore, be a very important parameter for the DAC.

Accelerated testing to determine the *expected linearity stability over time* can be accomplished by two different methods. Linearity is first measured at +25°C. The DAC is then operated at a fixed elevated temperature for an extended period of time. The DAC is then retested at +25°C, and the change in linearity error vs. time is calculated. The ARRHENIUS EQUATION (used in reliability calculations) can be used to determine what the acceleration factor is from +25°C to the elevated test temperature. Knowing the acceleration factor and the linearity error vs. time at the elevated temperature, one could calculate the expected long-term stability of linearity at nominal temperatures.

A second test method determines how long it will take for the linearity to shift by a specific error band (we chose ±2ppm for our example) at any specified temperature. The first step is to measure the linearity at a moderately elevated temperature (e.g., +85°C) and then monitor how long it takes at this temperature to reach the error band limit. The second step is to perform the same test at a much higher elevated temperature (e.g., +125°C). The two resulting time vs. temperature points are then plotted on semilog paper. A line drawn through the two points allows extrapolation to the length of time expected to reach the error band (±2ppm) at other temperatures, including +25°C.

Figure 7 shows how long it would take for the AD1139's linearity to drift ±2ppm (1/2LSB) at any operating temperature. The uppermost plot shows stability under storage conditions (no power), and the lower plot shows the AD1139's operating stability (under power). The *operating vs. storage* difference is due to the 10°C temperature rise when the AD1139 is powered.

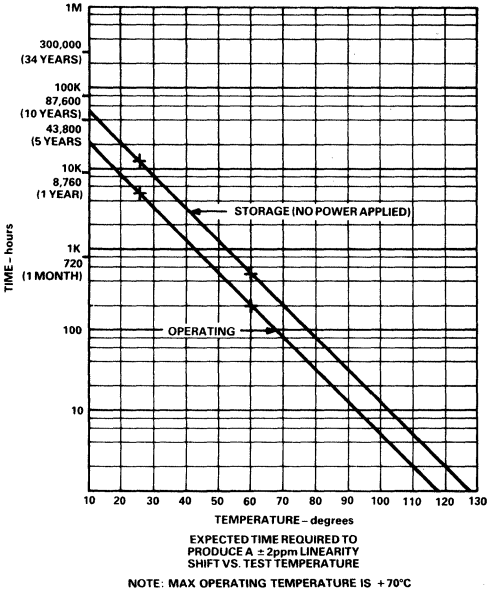


Figure 7. Nonlinearity vs. Time/Temperature

BURN-IN

All AD1139s undergo a 168 hour, powered burn-in @125°C, prior to laser trimming. This burn-in produces the optimum stability for the resistor network and eliminates infancy defects.

As shown in Figure 7, exposure to elevated temperatures produces an acceleration of the normal aging process. Preconditioning/burn-in employed by the user will lead to premature linearity shifts outside of the initial guaranteed specifications. The ADI warranty will not cover DACs that exhibit this type of *forced* premature specification degradation.

EXTERNAL AMPLIFIER FOR HIGH SPEED OR HIGH OUTPUT CURRENT

The AD1139's internal output amplifier is optimized for very low noise, dc stable applications with moderate settling time. Applications requiring higher speed or more output current can use an external amplifier, such as shown in Figure 8. The AD711 settles to within 16 bits in only 6μs for a unipolar full scale step. Other amplifiers may be chosen for differing tradeoffs. The noise gain seen by the output amplifier, depends on the output voltage range selected (see Table IV). The amplifier selected must be stable at the noise gain corresponding to the output range.

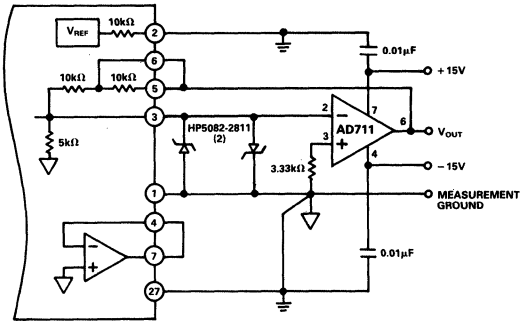


Figure 8. External Amplifier for High Speed

Output Voltage Range	Noise Gain
0 to +5V	2
0 to +10V	3
±5V	4
±10V	7

Table IV. Noise Gain vs. Output Voltage Range

SETTLING TIME

The LSB step and full-scale step typical settling times, to within ±1/2LSB at 18 bits, are shown in the Specification Table. Figure 9 graphically presents the typical settling times to within ±1/2LSB at resolutions from 12 to 18 bits.

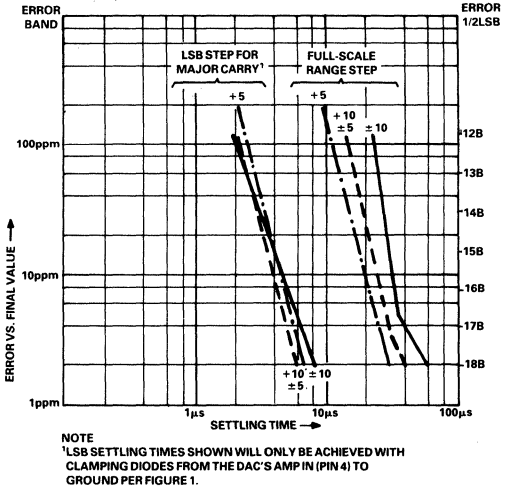


Figure 9. Settling Time vs. Resolution

ANALOG DEVICES

Low Cost 16-Bit Digital-to-Analog Converter

AD1145

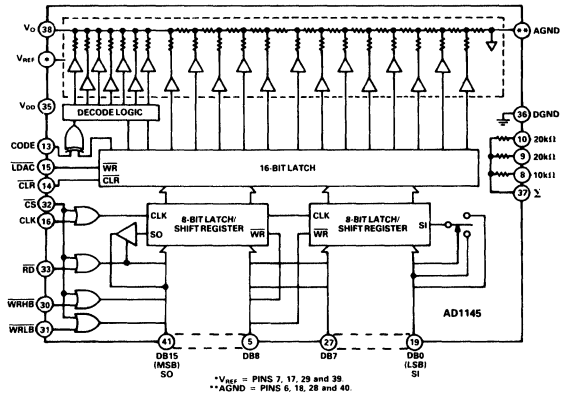
FEATURES

- 16-Bit Resolution
- Low Nonlinearity
  - Differential: ±3/4LSB max
  - Integral: ±1LSB max
- Relative Accuracy: ±0.003% max
- Fast Full-Scale Settling: 6μs to ±1/2LSB
- High Stability
  - Monotonic to 16 Bits: +15°C to +35°C
  - Offset TC: ±0.1ppm/°C max
  - Gain TC: ±0.1ppm/°C max
- Double Buffered Digital Input
- Parallel and Serial Data Input
- Single +5V Supply Operation
- Low Power Consumption: 2.5mW
- Small Size: 44-Pad Plastic LLCC
- Low Cost

APPLICATIONS

- Automatic Test Equipment
- Scientific Instrumentation
- Machine Control
- Digital Audio
- Robotics

AD1145 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD1145 is a double-buffered, 16-bit resolution DAC with ±3/4LSB maximum differential and ±1LSB maximum integral nonlinearity. Size comparable to the smallest monolithic DACs and high reliability are owed to its proprietary two-chip construction. A custom CMOS integrated circuit and laser-trimmed, thin-film resistor network provide 16-bit accuracy, excellent temperature stability and low power consumption.

The AD1145 offers an unparalleled combination of low cost, high accuracy, small size and convenient design-in features. The AD1145 directly interfaces with 8- and 16-bit microprocessors or can be used in stand-alone applications. Digital input coding is binary for unipolar output and offset binary or twos complement for bipolar output. Data can be written to the DAC in either a parallel or a serial mode. Serial data readback is available for error checking.

A clear line allows resetting the DAC output to zero volts on command. Power-up automatically resets the DAC output to zero volts following a power failure as required in machine control applications. All outputs may be simultaneously updated in a multiple DAC system.

Internal application resistors allow a wide variety of pin programmable output voltage ranges (+5V, +10V, −5V, −10V, ±5V and ±10V). The AD1145 may be operated off of a single +5V reference/supply, consuming only 2.5mW of power.

A 5 volt full-scale output step settles to within ±1/2LSB in just 6 microseconds. Wideband noise (100kHz) is only 50 microvolts peak-to-peak.

SPECIFICATIONS (typical @ +25°C, rated supplies unless otherwise specified)

Model	AD1145A/AG	AD1145B/BG
RESOLUTION	16 Bits	*
ACCURACY		
Differential Nonlinearity, max	±1LSB (= ±0.0015%)	±3/4LSB (= ±0.001%)
Integral Nonlinearity, max[1]	±1LSB (= ±0.0015%)	*
Relative Accuracy, max	±0.003%	*
Initial Errors		
Offset Error	±1/4LSB	*
Gain Error		
w/o Int. Application Resistors	±1/4LSB	*
w/Int. Application Resistors	±0.1%	*
STABILITY VS. TEMPERATURE		
Monotonicity, Guaranteed (Range °C)		
16 Bits	@ +25	+15 to +35
15 Bits	0 to +70	−40 to +85
14 Bits	−40 to +100	−40 to +100
Offset, max	±0.1ppm/°C	*
Gain, max	±0.1ppm/°C	*
STABILITY LONG TERM		
Differential Nonlinearity	±0.1ppm/1000 hours	*
Offset	±0.1ppm/1000 hours	*
Gain	±0.1ppm/1000 hours	*
DYNAMIC PERFORMANCE		
5V Full-Scale Settling Time (to ±1/2LSB)	6μs	*
LSB Settling Time	3μs	*
Glitch Energy (Major Carry @ BW = 20MHz)	800mV × 2μs	*
Total Harmonic Distortion	−98dB	*
ANALOG OUTPUT		
Nominal Voltage Output Range	+5V	*
Voltage Ranges (w/External Amplifier)[2]	−5V, −10V, +5V, +10V, ±5V, ±10V	*
Noise (BW = 0.1-10Hz)	5μV pk-pk	*
Noise (BW = 100kHz)	50μV pk-pk	*
Source Capacitance	18pF	*
Output Impedance	5kΩ	*
POWER SUPPLY REQUIREMENTS (V_{DD})		
w/CMOS Digital Inputs (V_{IN} = V_{DD} or GND)	+5V dc @ 10μA	*
w/TTL Digital Inputs (V_{IN} = 2.4V or 0.5V)	+5V dc @ 3mA	*
Range for Multiplying[3]	$V_{REF} - 0.3 \leq V_{DD} \leq V_{REF} + 0.6V$	*
Total Power @ +5V (Including Reference)		
w/CMOS Digital Inputs	2.5mW	*
w/TTL Digital Inputs	17.5mW	*
POWER SUPPLY SENSITIVITY		
Differential Nonlinearity	0.2ppm/%	*
Offset	10μV/V	*
Gain	10μV/V	*
EXTERNAL REFERENCE INPUT		
Nominal	+5V @ 500μA	*
Range[3]	+3.0V dc to +6.0V dc	*
Input Resistance	10kΩ	*
DIGITAL INPUTS		
V_{IL}	0.8V max @ 10μA max	*
V_{IH}	2.0V min @ 10μA max	*
Parallel & Serial (with Serial Readback)		
Unipolar Code	Binary	*
Bipolar Codes	Offset Binary, Twos Complement	*
TEMPERATURE RANGE		
Rated Performance	−40°C to +100°C	*
Storage	−55°C to +125°C	*
PACKAGE		
Surface Mount Device (AD1145A, B)	44-Pad Plastic Leadless Chip Carrier	*
Leaded Device (AD1145AG, BG)	44-Pin Grid Array	*

NOTES
[1]*Best Straight Line* linearity by manipulation of the gain and/or offset to equalize maximum positive and negative deviations.
[2]For custom voltage ranges use external resistors as shown in Figure 2d and 2e.
[3]V_{DD} must track V_{REF} within +0.6 and −0.3 volts. V_{DD} and V_{REF} can be tied together if the reference voltage is well buffered.
*Specifications same as AD1145A/AG.
Specifications subject to change without notice.

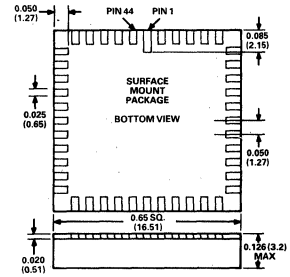
CAUTION: OBSERVE PROPER PLUG-IN POLARITY AND DO NOT PLUG INTO "LIVE" SOCKET – THE CONVERTER MAY BE DAMAGED.

ESDS CLASSIFICATION: MIL-STD-883, METHOD 3015, CATEGORY B

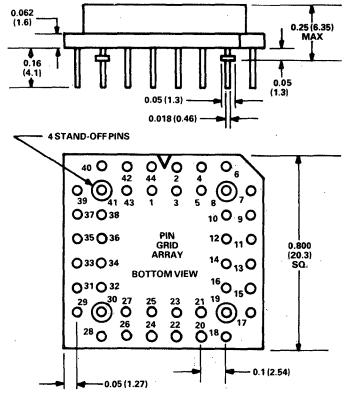
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

PLASTIC LEADLESS CHIP CARRIER*



44-PIN GRID ARRAY*



*PACKAGE NOTES:
A post assembly *water wash* cycle may trap water between the surface mount device and P.C. board. A drying period should be observed before operation (e.g., 65°C bake for 1 hour).
See Table VI for recommended sockets.

AD1145 PIN DESIGNATIONS

PIN	MNEMONIC	DESCRIPTION
1, 11, 12, 23, 34	NC	No Connection
2	DB11	Data Bit 11
3	DB10	Data Bit 10
4	DB9	Data Bit 9
5	DB8	Data Bit 8
6, 18, 28, 40	AGND	Analog Ground
7, 17, 29, 39	V_{REF}	Voltage Reference Input
8	10K	10kΩ Application Resistor
9, 10	20K	20kΩ Application Resistors
13	CODE	Selects Digital Input Code
14	$\overline{CLR}$	Clear, Active Low, Asynchronous
15	LDAC	Load DAC Register, Active Low Asynchronous
16	CLK	Clock, Rising Edge Triggered
19	DB0/SI	Data Bit 0 (LSB), Serial Input
20	DB1	Data Bit 1
21	DB2	Data Bit 2
22	DB3	Data Bit 3
24	DB4	Data Bit 4
25	DB5	Data Bit 5
26	DB6	Data Bit 6
27	DB7	Data Bit 7
30	$\overline{WRHB}$	Write High Byte, Active Low
31	$\overline{WRLB}$	Write Low Byte, Active Low
32	$\overline{CS}$	Chip Select, Active Low
33	$\overline{RD}$	Readback, Active Low
35	V_{DD}	Digital Power Supply
36	DGND	Digital Ground
37	Σ	Application Resistor Common
38	V_O	DAC Voltage Output
41	DB15/SO	Data Bit 15 (MSB), Serial Output
42	DB14	Data Bit 14
43	DB13	Data Bit 13
44	DB12	Data Bit 12

OUTPUT AMPLIFIER AND REFERENCE

The users choice of output amplifier and reference to complement the AD1145 will have a direct effect on the overall accuracy, speed and precision of the complete DAC circuit. The AD1145 can be optimized accordingly for a wide range of applications. Internal application resistors are provided to obtain output voltage ranges of 0 to 5V, 0 to 10V, 0 to −5V, 0 to −10V, ±5V, and ±10V. External resistors can be used for custom output voltage ranges as shown in Figure 2.

The AD1145's high impedance (5kΩ) voltage output must be buffered to drive a load since resistive loading at the output introduces a gain error (e.g., 50MΩ load resistance introduces a 0.01% gain error). Op amp bias current flows through the DAC output impedance to introduce an offset term (e.g., 100 nanoamps bias current introduces a 0.01% offset error).

In the noninverting mode the inputs of the operational amplifier swing between 0 and +5 volts. Therefore, to maintain 16-bit linearity the common-mode rejection ratio of the operational amplifier must be at least 96dB over a 5 volt range. Special consideration must be given to offset voltage, offset drift, bias current, bias drift, common-mode rejection, slew rate, and settling time when selecting an operational amplifier. High quality BiFET amplifiers, such as the AD711, are recommended.

The linearity and settling time for the AD1145 have a direct correlation to the output impedance and recovery time of the voltage reference. Therefore, a reference with a fast recovery time and low output impedance, such as the AD586, is recommended. When choosing a voltage reference, gain error and temperature drift must also be considered. A typical reference and output amplifier hookup is shown in Figure 1.

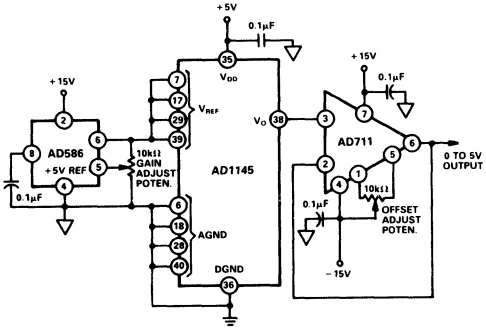


Figure 1. AD1145 Configured for a 0 to 5V Output with External Reference and Unity Gain Amplifier.

OFFSET AND GAIN CALIBRATION

The AD1145 has virtually no offset or gain errors of its own. When connected in a system, such as that shown in Figure 1, the system errors are nulled with external potentiometers. Offset error is nulled by adjusting the offset voltage of the output amplifier. Gain error is nulled by adjusting the output voltage of the external reference. The voltmeter used to measure the output must be capable of 1μV resolution. Offset adjustment should be done before gain adjustment.

UNIPOLAR MODE CALIBRATION

1. Apply a digital input of all "0"s.
2. Adjust the offset potentiometer until a 0.00000V output is obtained.
3. Apply a digital input of all "1"s.
4. Adjust the gain potentiometer until plus full-scale output is obtained. (see Table I for full-scale value).

BIPOLAR MODE CALIBRATION

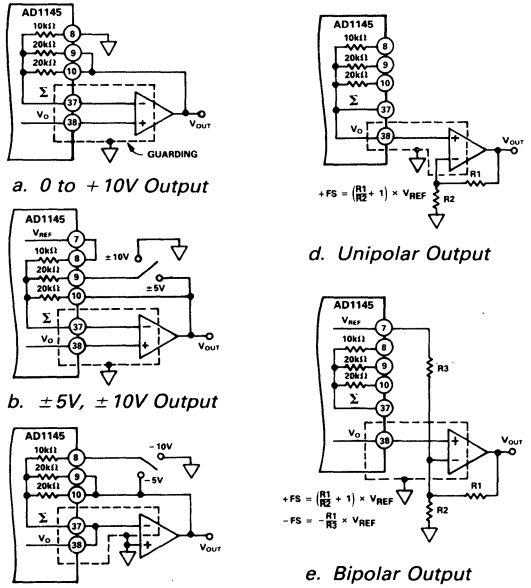
1. Apply a digital input of all "0"s (for offset binary coding) or 8000 Hex (for twos complement coding).
2. Adjust the offset potentiometer until minus full-scale output is obtained (see Table I for value).
3. Apply a digital input of all "1"s (for offset binary coding) or 7FFF Hex (for twos complement coding).
4. Adjust the gain potentiometer until plus full-scale output is obtained (see Table I for full-scale value).

Range	Input Code (Hex)		Output
Unipolar:			
0V to 5V	0000		0.00000V
	FFFF		4.999924V
0V to 10V	0000		0.00000V
	FFFF		9.999848V
	Offset	**Twos Comp**	
Bipolar:			
−5V to +5V	0000	8000	−5.00000V
	FFFF	7FFF	+4.999848V
−10V to +10V	0000	8000	−10.00000V
	FFFF	7FFF	+9.999695V

Table I. Offset and Gain Adjust

ANALOG OUTPUT RANGE

Figure 2 shows the required external amplifier connections for standard and custom output ranges. See Figure 1 for 0 to 5V.



a. 0 to +10V Output

b. ±5V, ±10V Output

c. 0 to −5V, −10V Output

d. Unipolar Output

e. Bipolar Output

Figure 2. Analog Output Range Configurations

TIMING DIAGRAM

The timing requirements of the AD1145 are shown in Table II. The timing diagrams for both serial and parallel input modes of operation as well as serial output operation are shown in Figure 3. The serial output mode enables the user to read back data written to the AD1145.

Symbol	Parameter	Requirement
t_{DS}	Data Setup Time	25ns
t_{DH}	Data Hold Time	10ns
t_{WR}	Write Pulse Width	25ns
t_{CWS}	Chip Select to Write Setup	0ns
t_{CWH}	Chip Select to Write Hold	0ns

Table II. Timing Requirements

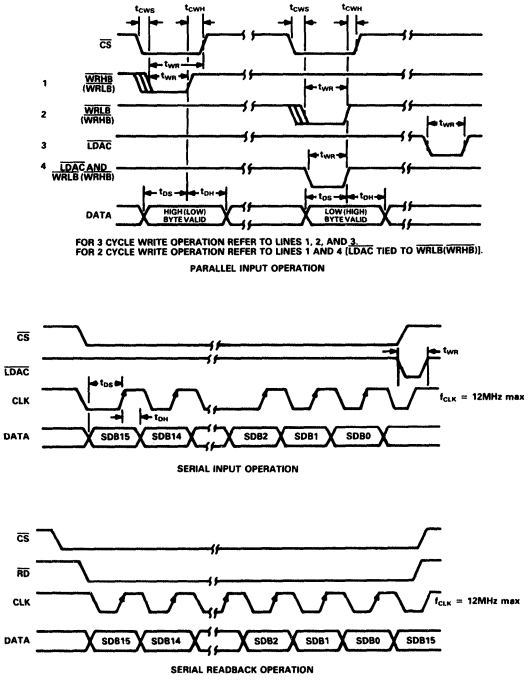


Figure 3. Timing Diagrams

The AD1145 has eight control lines. A brief description of each line follows:

$\overline{CS}$ is the Chip Select line and allows multiple AD1145s to share the same input bus. The desired DAC is selected with the $\overline{CS}$ line. A low on this line enables $\overline{WRLB}$, $\overline{WRHB}$, CLK, and $\overline{RD}$ of the selected DAC.

$\overline{WRLB}$ is the WRite line for the Low Byte input register. A low on this line makes the register transparent. A high level latches the input data into the register.

$\overline{WRHB}$ is the WRite line for the High Byte input register. Operation is the same as $\overline{WRLB}$.

$\overline{LDAC}$ is the Load line for the DAC register. A low on this line makes the DAC register transparent. A high level latches the data from the input registers into the DAC register. $\overline{LDAC}$ operates independently of $\overline{CS}$.

CLK is the line used to CLocK serial data into or out of the input registers. Data is moved on each positive transition of CLK. Note that CLK must be held high for parallel operation.

$\overline{RD}$ is the ReaD line. A low on this line enables the serial output function and also connects the serial output to the serial input.

$\overline{CLR}$ is the CLeaR line. A low on this line clears the DAC output to zero volts regardless of input coding. $\overline{CLR}$ operates independently of $\overline{CS}$.

CODE determines the input coding of the DAC. A low on this line inverts the MSB for twos complement coding. A high does not invert the MSB (for binary and OBN codes).

PARALLEL OPERATION

The AD1145 is fully compatible with either 8- or 16-bit microprocessor systems. In an 8-bit system, data may be loaded using either two or three instruction cycles, with either the high byte or the low byte being loaded first. Typical load sequences are (1) load high byte, load low byte, load DAC register, or (2) load high byte, load low byte and DAC register. With a 16-bit system, data may be loaded using either one, or two, instruction cycles, or the DAC may be operated with all of its registers transparent. Table III illustrates the AD1145's parallel operation as a function of its control lines. Note that CLK and $\overline{RD}$ must be held high for parallel operation.

$\overline{CLR}$	$\overline{CS}$	$\overline{WRLB}$	$\overline{WRHB}$	$\overline{LDAC}$	OPERATION
0	X	X	X	X	Reset DAC Output to Zero Volts.
1	0	0	0	0	Input and DAC Registers are Transparent.
1	0	0	0	1	Load High Byte and Low Byte Input Registers.
1	0	0	1	0	Load DAC Register from High Byte Register and Transparent Low Byte Inputs.
1	0	0	1	1	Load Low Byte Input Register.
1	0	1	0	0	Load DAC Register from Low Byte Register and Transparent High Byte Inputs.
1	0	1	0	1	Load High Byte Input Register.
1	0	1	1	0	Load DAC Register from Input Registers.
1	1	X	X	0	Load DAC Register from Input Registers.
1	1	X	X	1	No Operation.
1	X	1	1	1	No Operation.

Table III. Parallel Operation Truth Table

SERIAL OPERATION

In the serial mode, data is written from DB0/SI into the input register on each positive going transition of the clock. For error checking, data can also be readback from the input register to DB15/SO. The serial output is switched internally to the serial input in the readback mode so that the data is recirculated as it is read. In this way the data is restored after 16 clock cycles. The data in the DAC register and hence the DAC output voltage is unchanged during readback. Table IV shows the serial operation of the AD1145 as it relates to the status of the control lines.

INPUT CODING

The AD1145 accepts data in twos complement, offset binary, or straight binary formats. The code pin either *inverts* or *not inverts*

$\overline{CLR}$	$\overline{CS}$	CLK	$\overline{RD}$	$\overline{LDAC}$	OPERATION
0	x	x	x	x	Reset DAC Output to Zero Volts.
1	0	↑	1	1	Clock Serial Data from DB0/SI into Input Register.
1	0	↑	0	1	Clock Serial Data from Input Register out to DB15/SO.
1	x	x	x	0	Load DAC Register.
1	x	↓	x	1	No Operation.

Table IV. Serial Operation Truth Table

the MSB. If code is low, the MSB is inverted for twos complement coding. If code is high, the MSB is true for straight binary and offset binary coding. See Table V for further detail.

CLEAR LINE OPERATION

The clear line, in conjunction with the code line, resets the DAC output to zero volts. For straight binary operation CODE should be tied to $+V_{DD}$, the MSB will not be inverted, the DAC register gets reset to 0000H, and the AD1145's output is reset to zero volts. For twos complement operation, CODE is tied to DGND, the MSB is inverted, the DAC register is reset to 1/2 full scale, and the AD1145's output is reset to zero volts. For offset binary operation CODE is tied to $\overline{CLR}$. In this way the MSB is not inverted in normal operation but on CLEAR the MSB gets inverted, the DAC register is reset to 1/2 full scale, and the AD1145's output is reset to zero volts. Table V shows the clear operation as a function of CODE input.

CLR	CODE	OPERATION
0	0	BIPOLAR CLEAR (Twos Complement, Offset Binary)
0	1	UNIPOLAR CLEAR (Binary)
1	0	MSB INVERTED (Twos Complement)
1	1	MSB TRUE (Binary, Offset Binary)

Table V. Clear Operation Truth Table

POWER-UP RESET

In the event of a power failure, the DAC output is automatically reset to zero volts upon power-up. When CODE is high, the DAC is reset to zero for a unipolar clear. When CODE is low, the DAC is reset to 1/2 full scale for a bipolar clear (zero volt output).

GROUNDING AND GUARDING

The AD1145 is a precision D/A converter with 76μV LSB resolution at a FSR of 5V. Special care must be taken to insure proper layout, grounding, and guarding. Analog and digital grounds should be individually star pointed and then tied together at a single point near the measurement point. High-speed digital inputs should be kept separate from low level analog outputs. Power supplies should be locally bypassed around all high-speed components and at the power supply input to the printed circuit board. All high impedance nodes such as the DAC output and amplifier inputs are sensitive to interference from the digital input lines. They should be surrounded by low impedance guard tracks at all times. Figure 2 shows the proper guarding of the AD1145 depending on output configuration.

SINGLE SUPPLY OPERATION

The AD1145 can operate with V_{DD} connected to V_{REF}. If CMOS is used to drive the DAC inputs, the static current drawn from V_{DD} will be less than 10μA. If TTL is used to drive the DAC inputs, the static current draw will be increased to about 3mA depending on the digital input. Therefore, the reference must be well buffered to avoid code dependent errors when TTL inputs are used. Figure 4 shows the AD1145 operating from a single supply.

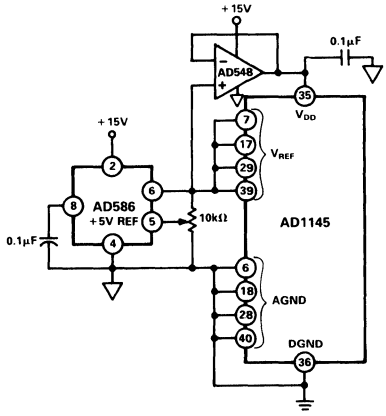


Figure 4. Single Supply Configuration

MULTIPLYING DAC OPERATION

The AD1145 operates as a two quadrant multiplying DAC over a limited voltage range. V_{REF} can vary between 3 and 6 volts. V_{DD} must track V_{REF} within +0.6 and −0.3 volts. Logic levels will vary with V_{DD}, with a logic low being less than $1/3V_{DD}$ and a logic high being greater than $2/3V_{DD}$. V_{DD} and V_{REF} may be tied together provided the reference voltage is well buffered.

A useful application of the multiplying feature is to set the reference voltage to 4.096 volts and configure the DAC as shown in Figure 2b for ±10V range. This provides a ±8.192 volt full-scale output for a bit weight of 0.25mV per LSB.

MULTIPLE DAC APPLICATION

The AD1145 is well suited for applications using multiple DACs sharing the same data bus, as in automated test equipment. Figure 5 shows a typical multiple DAC hookup. Note that the $\overline{WRLB}$, $\overline{WRHB}$, $\overline{LDAC}$, $\overline{RD}$, $\overline{CLR}$, and CLK lines from each DAC are tied together. A separate chip select ($\overline{CS}$) line is provided to individually select each DAC. Data can be written to one or all DACs by appropriate selection of the chip select lines. All DACs may be simultaneously updated by strobing the $\overline{LDAC}$ line. A separate CODE line is provided for each DAC so that they may be independently configured for unipolar and bipolar coding.

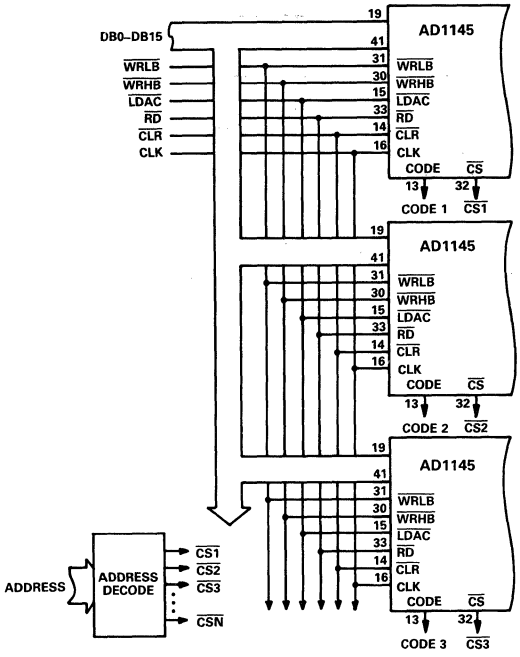


Figure 5. Multiple DAC Application

PARALLEL READBACK

Full parallel readback can be achieved by adding two 74ALS990 octal D-type read-back latch chips as shown in Figure 6. These latches also reduce digital feedthrough from the data bus; an important consideration in high accuracy systems.

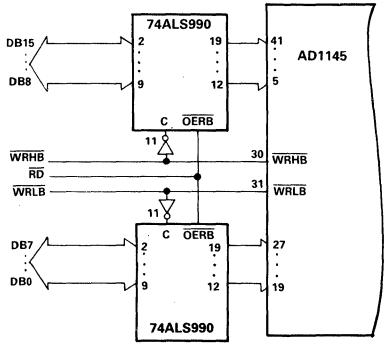


Figure 6. Parallel Readback

PACKAGE INFORMATION

The AD1145 is packaged in a 44-pad glass epoxy chip carrier. This package is ideal for automated surface mounting due to its excellent dimensional tolerances and planarity. As the package is made from the same material as printed circuit boards, it has the same temperature coefficient of expansion. This minimizes stress and maximizes product reliability. Standard JEDEC leadless chip carrier sockets such as those manufactured by Textool can be used for testing. For conventional through-hole mounting, the AD1145 is also available in a PGA package. See Table VI for recommended sockets.

Simple 8-Bit and 16-Bit Data Bus Connections

The AD1145 can be configured to directly connect to an 8-bit or 16-bit data bus. An 8-bit microprocessor requires at least two write cycles to supply 16 bits of input data. Utilizing the AD1145's high byte and low byte input registers, one byte at a time is loaded from the 8-bit bus. The 16-bit DAC register can be latched during or after the second byte write operation. Figure 7 shows a typical AD1145 connection to an 8-bit bus. Note that the three logic gates can be eliminated if two address lines are available.

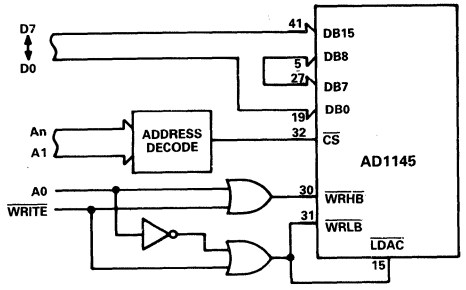


Figure 7. 8-Bit Microprocessor Interface

A 16-bit microprocessor supplies a complete 16-bit input in a single write cycle. This eliminates the requirement for the individual high byte and low byte input latches. Figure 8 shows a typical AD1145 connection to a 16-bit bus. The 16-bit DAC register is made transparent by grounding the $\overline{\text{LDAC}}$ line or can be strobed for full double buffering.

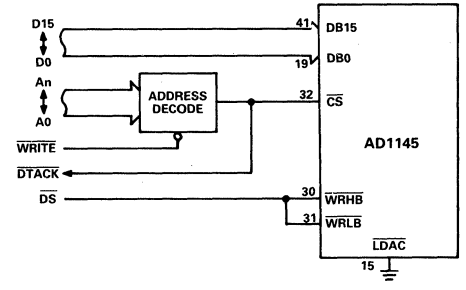


Figure 8. 16-Bit Microprocessor Interface

Package	Purpose	Manufacturer	Mfg. Part No.
PLLCC	Test	Textool	244-4961-000
PGA	Test	Amp	55280-4
PGA	Production	Advanced Interconnections	CS044-01TG
		Augat	PPS044-3A0802-L
		Samtec	MPAS–044-ZS-8

Table VI. Recommended Sockets

Microprocessor Compatible 16-Bit D/A Converters

AD1147/AD1148

FEATURES

Low Nonlinearity
- **Differential: ±0.00076% max**
- **Integral: ±0.00076% max**
- **Differential TC: ±1ppm/°C max**

Fast Settling
- **Full Scale: 20μs to ±0.00076%**
- **LSB: 3μs to ±0.00076%**

Low Power: 375mW Including Reference

Functionally Complete
- **Internal Reference, Output Voltage Amplifier, Input Latches and 8-Bit Latched Input DACs for Offset and Gain Correction.**

Full Four Quadrant Multiplying

Low Cost

APPLICATIONS

Automatic Test Equipment

Scientific Instrumentation

Beam Positioners

Robotics

Graphics Displays

GENERAL DESCRIPTION

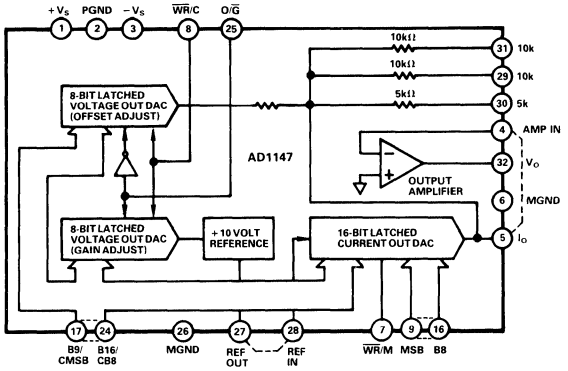
The AD1147 and AD1148 are 16-bit resolution, hybrid, latched input, digital-to-analog converters. Their two 8-bit latched input DACs allow direct offset and gain correction via microprocessor interface.

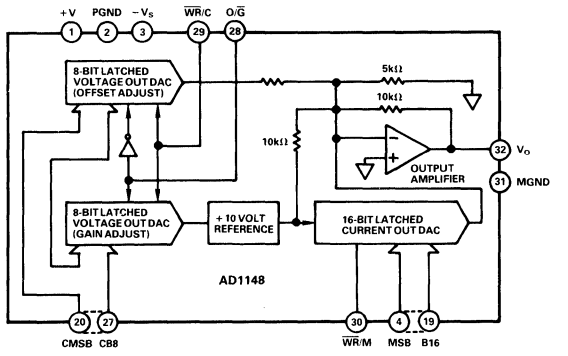
The AD1147 and AD1148 are constructed as hybrids in a compact 32-pin, triple wide dual-in-line package. Precision CMOS switches and a laser-trimmed thin-film resistor network are used to provide 16-bit accuracy and excellent temperature stability.

The Main (16-bit) DAC is loaded as a 16-bit word. The offset and gain correction DACs are each loaded as 8-bit words. The AD1147 multiplexes both correction DACs' inputs with the Main DAC's eight LSBs. This pin sharing allows for additional pin connections providing: external reference input, a current output and feedback resistors for voltage output ranges of 0 to +5V, 0 to +10V, ±5V and ±10V.

The AD1148 correction DACs' inputs are separate from the Main DAC's. The gain correction DAC's inputs are multiplexed with the offset DAC's 8-bit inputs. This allows for a separate 8-bit bus interface with the correction DACs – common in applications such as Automatic Test Equipment.

AD1147/AD1148 FUNCTIONAL BLOCK DIAGRAMS





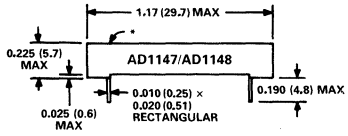
SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise specified)

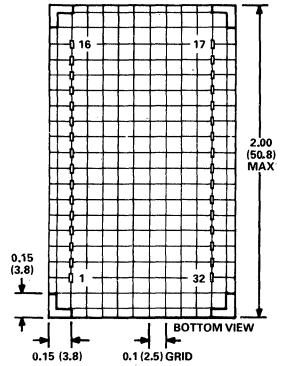
MODEL	AD1147	AD1148
RESOLUTION	16 Bits	*
ACCURACY		
Differential Nonlinearity	±0.00076% FSR[1] (max)	±0.00076% FSR[1] (typ), ±0.0015% FSR[1] (max)
Integral Nonlinearity	±0.00076% FSR[1] (max)	±0.00076% FSR[1] (typ), ±0.0015% FSR[1] (max)
Monotonic (16 Bits)	Guaranteed	*
Offset	Adjustable to Zero	*
Gain	Adjustable to Full Scale	*
STABILITY		
Differential Nonlinearity	±1ppm/°C (max)	*
Offset	±20μV/°C (max)	**
Bipolar Offset	±6ppm/°C (max)	*
Gain (Includes Int. Ref.)	±10ppm/°C (max)	*
STABILITY, Long-Term (ppm/1000 hr.)		
Differential Nonlinearity	±1ppm	*
Offset	±3ppm	**
Bipolar Offset	±3ppm	*
Gain	±12ppm	*
REFERENCE VOLTAGE		
Output Voltage	+10.00V, ±0.3% (max)	**
Output Current	2mA (max)	**
Ext. Ref Voltage Range[2]	−12V to +12V	**
Input Resistance	12kΩ	**
DYNAMIC PERFORMANCE		
Settling Time to ±0.00076%		
Voltage, Full-Scale Step	20μs	*
Voltage, LSB Step	3μs	*
Current	2μs	**
DIGITAL INPUT CODES	5 Volt CMOS/TTL Compatible	
Main DAC		
Unipolar	Binary (BIN)	**
Bipolar	Offset Binary (OBN)	*
Correction DACs	Binary (BIN)	*
ANALOG OUTPUT		
Voltage	+5V, +10V, ±5V, ±10V	±10V
Current	−2mA, ±1mA	**
Voltage Compliance	±500mV	**
Noise (100kHz BW)	60μV rms	*
POWER REQUIREMENTS		
Voltage (Rated Performance)	±15V (±5%)	*
Voltage (Operating)	±12.5V to ±17V	*
Supply Current Drain	±15mA (max)	*
Total Power @V_S = ±15V	375mW typ, 500mW max	*
POWER SUPPLY SENSITIVITY		
Offset	±10ppm/V	*
Gain	±10ppm/V	*
OFFSET ADJUSTMENT		
Range	±0.05% FSR	*
Resolution (@±10V)	1/4LSB	*
GAIN ADJUSTMENT		
Range (Unipolar/Bipolar)	±0.2% FSR[1]/±0.1% FSR[1]	NA/*
Resolution (Unipolar/Bipolar)	1LSB/1/2LSB	NA/*
TEMPERATURE RANGE		
Rated Performance	−25°C to +85°C	*
Storage Temperature	−40°C to +100°C	*
SIZE	2.00″ × 1.17″ × 0.225″ (all maximums) (50.8 × 29.7 × 5.7mm)	

NOTES
*Specifications same as AD1147.
**AD1148 does not provide pin connections to current output, reference input, reference output or the internal feedback resistors. Output voltage range is fixed at ±10V.
[1]FSR means Full-Scale Range.
[2]Rated performance is specified with +10V reference.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





* PIN 1 LOCATION IS IDENTIFIED BY A WHITE DOT ON THE TOP SURFACE.

AD1147 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	$+V_S$	32	V_O
2	PGND	31	10k
3	$-V_S$	30	5k
4	AMP IN	29	10k
5	I_O	28	REF IN
6	MGND	27	REF OUT
7	$\overline{WR}$/M	26	MGND
8	$\overline{WR}$/C	25	O/$\overline{G}$
9	MSB	24	B16/CB8
10	B2	23	B15/CB7
11	B3	22	B14/CB6
12	B4	21	B13/CB5
13	B5	20	B12/CB4
14	B6	19	B11/CB3
15	B7	18	B10/CB2
16	B8	17	B9/CMSB

AD1148 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	$+V_S$	32	V_O
2	PGND	31	MGND
3	$-V_S$	30	$\overline{WR}$/M
4	MSB	29	$\overline{WR}$/C
5	B2	28	O/$\overline{G}$
6	B3	27	CB8
7	B4	26	CB7
8	B5	25	CB6
9	B6	24	CB5
10	B7	23	CB4
11	B8	22	CB3
12	B9	21	CB2
13	B10	20	CMSB
14	B11	19	B16
15	B12	18	B15
16	B13	17	B14

ANALOG OUTPUT RANGE

The AD1148 is internally connected for ±10 volts output range.

The AD1147 is pin programmable to provide a variety of analog outputs, either current or voltage. A unipolar output current of 0 to −2mA is available at pin 5, and can be offset by 1mA (by connecting pin 28 to pin 29) for a bipolar output of ±1mA. Output voltage ranges (+5V, +10V, ±5V and ±10V) are available at pin 32 by connecting the current output (pin 5) to the amplifier input (pin 4) and the appropriate internal feedback resistors to the amplifier output (pin 32) as shown in Figure 1.

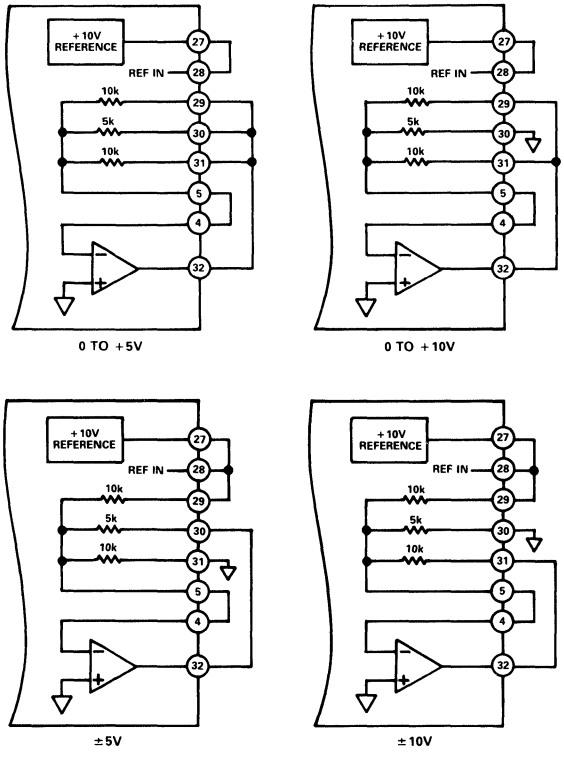


Figure 1. AD1147 Analog Output Range Pin Programming

TIMING DIAGRAM

The timing requirements for the models AD1147 and AD1148 are shown in Table I. The timing diagrams for the MAIN 16-bit DAC and the 8-bit Correction DACs are shown in Figure 2. The three control lines operate as follows:

$\overline{WR}$/M is the write line for the main DAC. The latches are transparent when the write line is low, and latched when the write line goes high.

$\overline{WR}$/C is the write line for the correction DACs. Operation is the same as above.

O/$\overline{G}$ selects between the offset correction DAC and the gain correction DAC. A high level on this pin selects the offset DAC. A low level selects the gain DAC.

SYMBOL	PARAMETER	REQUIREMENT
Main DAC		
t_{DS}	Data Setup Time	140ns min
t_{DH}	Data Hold Time	120ns min
t_{WR}	Write Pulse Width	250ns min
Correction DACs		
t_{CS}	O/$\overline{G}$ To Write Setup Time	200ns min
t_{CH}	O/$\overline{G}$ To Write Hold Time	20ns min
t_{DS}	Data Valid To Write Setup Time	110ns min
t_{DH}	Data Valid To Write Hold	0ns min
t_{WR}	Write Pulse Width	100ns min

Table I. Timing Requirements

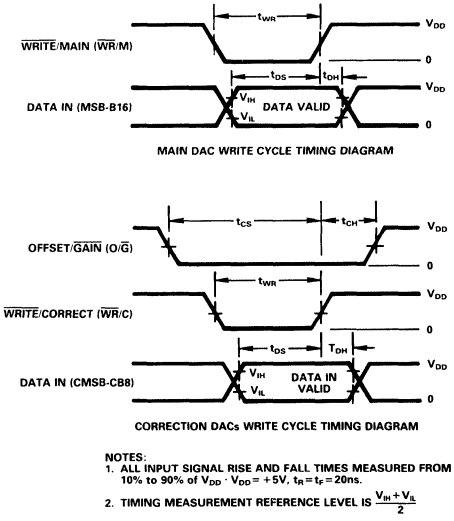


Figure 2. AD1147 and AD1148 Timing Diagrams

OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero using the two internal 8-bit calibration DAC's. There are three control lines used in the calibration sequence: $\overline{WR}$/M is the write line for the Main (16-bit) DAC – the latches are transparent when the write line is low, and latched when the write line goes high; $\overline{WR}$/C is the write line for the correction DACs and operates the same as $\overline{WR}$/M; O/$\overline{G}$ selects between the offset correction DAC and the gain correction DAC – a high level on this pin selects the offset DAC and a low level selects the gain DAC.

Offset and Gain calibrations are performed as follows:

1. With $\overline{WR}$/M low, set the digital inputs of the Main DAC to "000....00" (in unipolar mode) or "100....00" (in bipolar mode).
2. Set $\overline{WR}$/M high to latch the digital input into the Main DAC.
3. With $\overline{WR}$/C low and O/$\overline{G}$ high, adjust the digital inputs of the offset correction DAC until the Main DAC's output

voltage (pin V_O) is as close to 0.000000 volts as possible. Note that incrementing the digital input produces a more negative voltage output.

4. Set $\overline{WR}$/C high to latch the digital input into the offset correction DAC.
5. With $\overline{WR}$/M low, set the digital input of the Main DAC to "111....11".
6. Set $\overline{WR}$/M high to latch the digital input into the Main DAC.
7. With $\overline{WR}$/C low and O/$\overline{G}$ low, adjust the digital inputs of the gain correction DAC until the Main DAC's output voltage (pin V_O) is as close as possible to the positive full-scale voltage shown below in Table II. Note that incrementing the digital input produces a more negative voltage output.
8. Set $\overline{WR}$/C high to latch the digital input into the gain correction DAC.
9. Calibration is complete. Set $\overline{WR}$/M low and begin/resume normal digital-to-analog conversion via the Main DAC.

Output Voltage Range	Positive Full-Scale Voltage
0 to +5 volts	+4.999924 volts
0 to +10 volts	+9.999847 volts
±5 volts	+4.999847 volts
±10 volts	+9.999695 volts

Table II. Gain Calibration

GROUNDING AND GUARDING

The current from the measurement ground pin (MGND) is constant, independent of digital input, for ease of making measurements. This is the high quality ground for the AD1147 and AD1148. It should be connected to the high quality ground in the application. Power ground (PGND) should be connected to measurement ground (MGND) at the measurement point.

The current output pin (I_O) of the AD1147 is sensitive to interference from the digital input lines. It should be surrounded by a grounded guard at all times. When using the AD1147 in the voltage output mode, both the "I_O" and "AMP IN" pins should be guarded (see Figure 3).

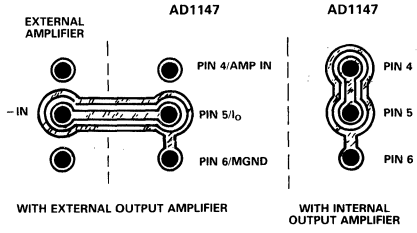


Figure 3. Typical Guarding Techniques

EXTERNAL AMPLIFIER FOR LOW DRIFT VOLTAGE OUTPUT OR HIGH OUTPUT CURRENT

The internal output amplifier of the AD1147 is designed for high-speed applications that require fast settling times. An external precision operational amplifier like the AD OP-07C can be applied when lower offset (less than 20μV/°C) is important (see Figure 4). Simply connect the current output (Pin 5) to the inverting input of the amplifier and connect the proper feedback resistors as shown in Figure 1. Be certain to keep the current output-amplifier's input connection short and surrounded by a grounded guard. To avoid degrading the gain drift performance of the DAC, always use the internal feedback resistors, since they are matched to the internal current weighting resistors of the DAC. It is also good practice to connect the negative input (Pin 4, AMP IN) of the unused internal output amplifier to its output (Pin 32, V_O).

The current drift of the AD1147 is typically 350pA/°C from +15°C to +35°C. When using the AD OP-07, the total offset drift of the output signal will typically be less than 2μV/°C.

As a second example, a high output current amplifier can be connected to the AD1147 to create a programmable power supply. The configuration is the same as shown for the AD OP-07C in Figure 4.

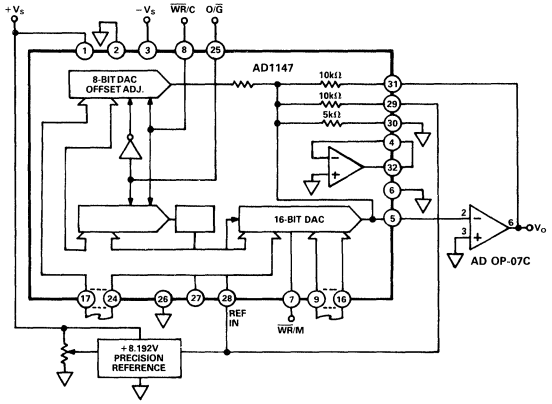


Figure 4. Precision DAC with ±8.192V F.S. Output Voltage

FULL FOUR-QUADRANT MULTIPLYING DAC

The AD1147 is a full four-quadrant multiplying DAC and can be used with references varying between +12 and −12 volts. Typical linearity vs. external reference voltage is shown in Figure 5. Output voltage ranges other than those provided can be obtained by connecting the appropriate reference voltage to "REF IN" (Pin 28), (see Figure 4). The DAC output voltage can be calculated as follows:

$$\text{UNIPOLAR } V_O = \frac{\text{DIGITAL INPUT}}{2^{16}} \times \frac{V_{REF}}{5k} \times R_{fb}$$

$$\text{BIPOLAR } V_O = \frac{\text{DIGITAL INPUT}}{2^{16}} \times \frac{V_{REF}}{5k} \times R_{fb} - \frac{V_{REF}}{10k}$$

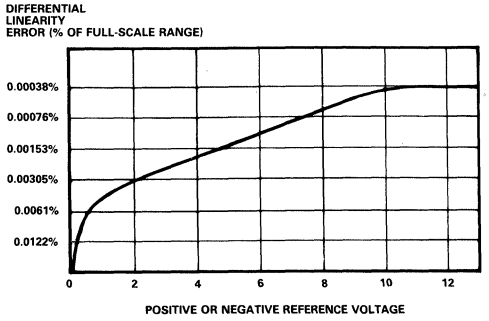


Figure 5. Typical Differential Linearity vs. External Reference Voltage

8-BIT MICROPROCESSOR INTERFACE

The AD1147/AD1148 can easily be operated with an 8-bit bus by the addition of an octal latch. The 16-bit Main DAC is loaded from the 8-bit bus as two 8-bit bytes. Figure 6 shows the configuration when using a 74HC573 octal latch.

The eight most significant bits are latched into the 74HC573 by setting the "latch enable" control line low. The eight least significant bits are then placed on the bus. Now all sixteen bits can be simultaneously latched into the Main DAC by setting $\overline{WR}$/M high.

The offset and gain correction DAC's are calibrated as they were for 16-bit microprocessor applications. See the "OFFSET AND GAIN CALIBRATION" section of this data sheet.

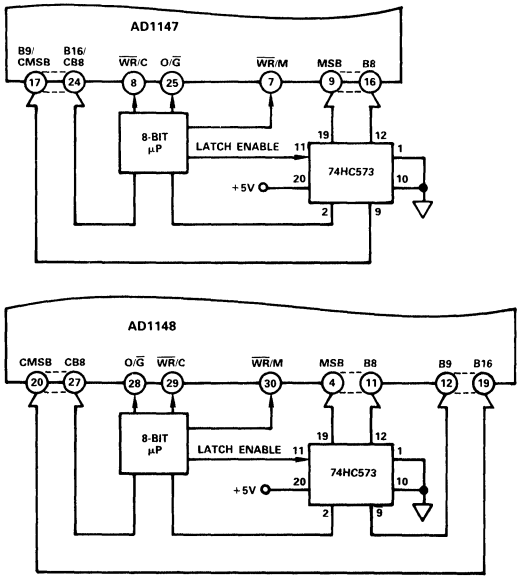


Figure 6. Connections for 8-Bit Bus Interface

AUTOMATIC TESTING OF 12-BIT ADC'S AND DAC'S

The AD1147 and AD1148 can be used as a reference DAC to automatically test the integral and differential linearity of 12-bit ADCs and DACs. An ideal reference DAC should be an order of magnitude more accurate than the devices to be tested. The AD1147 and AD1148 are sixteen times more accurate than the devices to be tested and therefore can be considered ideal.

The general test procedures for ADCs and DACs are shown below. Before actual testing proceeds, calibrate the offset and gain of the AD1147 or AD1148 (see "OFFSET AND GAIN CALIBRATION" section of this data sheet).

ADC TESTING (refer to Figures 7 and 8).

The differential nonlinearity of ADC's is the difference between the actual code widths of the analog input voltage vs. the ideal, one LSB, code widths of a perfect converter. A code width is the range of analog input voltage which produces the desired digital output word.

A code width can be measured by determining the analog input voltage at which the transition occurs from the code under test to its next lower digital output code and then differencing that analog value with the same determined for the transition from the code under test to its next higher digital output code.

Virtually all converters exhibit a degree of noise. This will necessitate an averaging technique to determine the analog input value for a code transition – where a reduction in analog input voltage produces a majority of the lower digital code decisions and an analog input increase produces a majority of the higher digital code decisions.

Begin testing by calibrating the offset and gain of the ADC under test per the manufacturer's instructions. Set the digital inputs of the reference DAC to the nominal value of the desired transition edge (produces an analog input to the device under test that is either 1/2LSB below or 1/2LSB above the ideal analog input for the code under test). Increment or decrement this digital input until the Device Under Test (D.U.T.) outputs the digital code below the transition 50% of the time and the digital code above the transition 50% of the time. Record this digital input and repeat the procedure for the next transition of the nominal code to be measured. Compare this second digital input with the recorded input. The difference between these two digital values is the width of the code being measured. A perfect code width is 16 counts of the reference DAC. Each count more, or less than 16, corresponds to a differential linearity error of 1/16LSB for the D.U.T. The arithmetic average of the two digital input values is the center of the code being tested. Each count of difference between this actual code center and the ideal, nominal code center represents an integral linearity error of 1/16LSB.

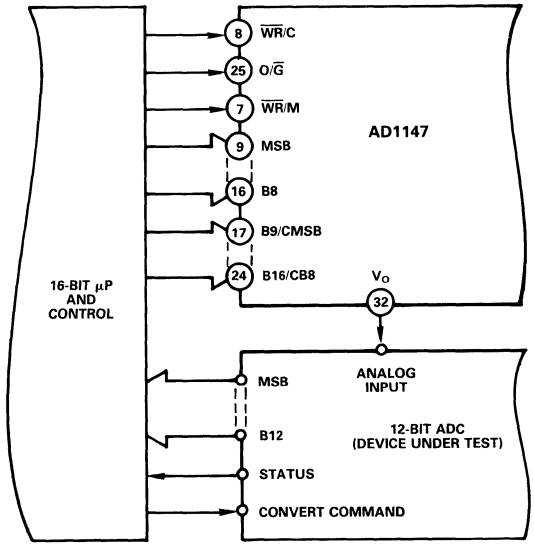


Figure 7. ADC Testing

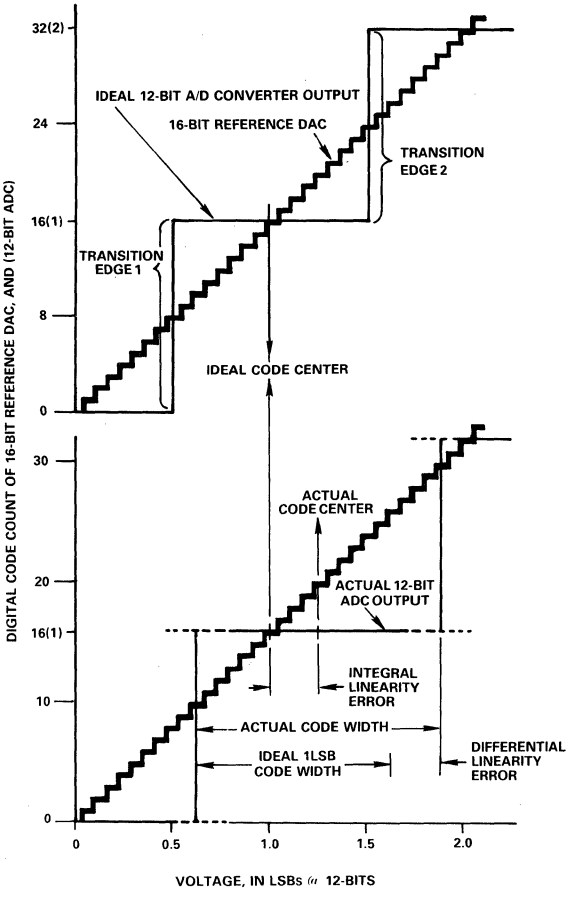


Figure 8. 12-Bit ADC Linearity Testing

DAC TESTING (refer to Figure 9).
To test 12-bit DACs begin with offset and gain calibration of the DAC under test per the manufacturer's instructions. Set the digital inputs of the reference DAC and the D.U.T. to the desired code. Latch this digital input into the reference DAC. The DACs' outputs are differenced and amplified by an AD524A instrumentation amplifier. The voltage error between the DACs is the integral linearity error.

Now null the meter and then increment or decrement the digital input to the D.U.T. only, by one LSB. The meter reading will correspond to the code width of the new digital input word. The deviation of this voltage from the ideal value of one LSB is the differential linearity error of the D.U.T.

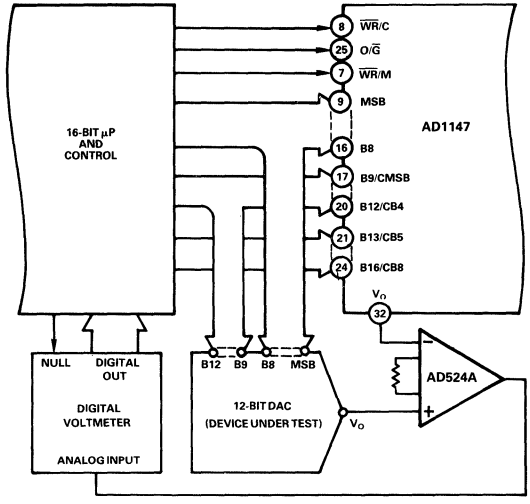


Figure 9. DAC Testing

ANALOG DEVICES

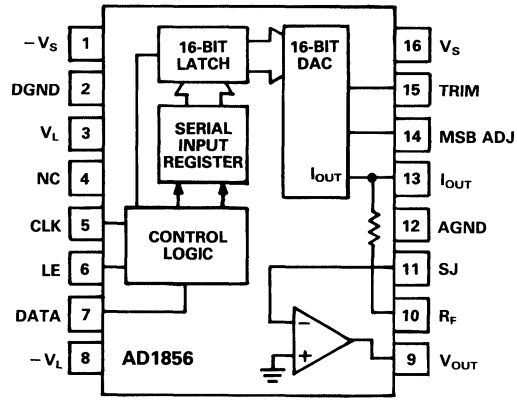
16-Bit PCM Audio DAC

AD1856

FEATURES
0.0025% THD
Fast Settling Permits 2×, 4× or 8× Oversampling
±3V Output
Optional Trim Allows Superlinear Performance
±5V to ±12V Operation
16-Pin Plastic DIP Package
Serial Input

APPLICATIONS
Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

AD1856 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1856 is a monolithic 16-bit PCM Audio DAC. Each device provides a voltage output amplifier, 16-bit DAC, 16-bit serial-to-parallel input register and voltage reference. The digital portion of the AD1856 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1856 is fabricated with bipolar and MOS devices as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reconstructions of low amplitude signals. Output glitch is also small contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3V signal at load currents up to 8mA. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 10MHz clock rate. This serial input port is compatible with popular digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4× and 8× sampling frequency.

The AD1856 can operate with ±5V to ±12V power supplies making it suitable for both the portable and home-use markets. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110mW typical with ±5V supplies and is a typical 300mW when ±12V supplies are used.

The AD1856 is packaged in a 16-pin plastic DIP and incorporates the industry-standard pinout. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 to ±13.2V.

PRODUCT HIGHLIGHTS

1. Total harmonic distortion is 100% tested.
2. MSB trim feature allows superlinear operation.
3. The AD1856 operates with ±5V to ±12V supplies.
4. Serial interface is compatible with digital filter chips.
5. 1.5μs settling time permits 2×, 4× and 8× oversampling.
6. No external components are required.
7. 96dB dynamic range.
8. ±3V or ±1mA output capability.
9. 16-bit resolution.
10. 2s complement serial input words.
11. Low cost.
12. 16-pin plastic DIP package.

SPECIFICATIONS (typical at T_A = +25°C and ±5V supplies unless otherwise noted)

Parameter		Min	Typ	Max	Units
RESOLUTION				**16**	Bits
DIGITAL INPUTS	V_{IH}	2.4		V_L	V
	V_{IL}	0		0.8	V
	I_{IH}, $V_{IH} = V_L$			**1.0**	μA
	I_{IL}, $V_{IL} = 0.4$			**−50**	μA
Clock Input Frequency		**10**			MHz
ACCURACY					
Gain Error			±2.0		%
Bipolar Zero Error			±30		mV
Differential Linearity Error			±0.001		% of FSR
Noise (rms, 20Hz to 20kHz) @ Bipolar Zero			6		μV
TOTAL HARMONIC DISTORTION					
0dB, 990.5Hz	AD1856N-K		0.002	**0.0025**	%
	AD1856N-J		0.002	**0.004**	%
	AD1856N		0.002	**0.008**	%
−20dB, 990.5Hz	AD1856N-K		0.018	**0.020**	%
	AD1856N-J		0.018	**0.040**	%
	AD1856N		0.018	**0.040**	%
−60dB, 990.5Hz	AD1856N-K		1.8	**2.0**	%
	AD1856N-J		1.8	**4.0**	%
	AD1856N		1.8	**4.0**	%
MONOTONICITY			15		Bits
DRIFT (0 to +70°C)					
Total Drift			±25		ppm of FSR/°C
Bipolar Zero Drift			±4		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)					
Voltage Output	6V Step		1.5		μs
	1LSB Step		1.0		μs
	Slew Rate		9		V/μs
Current Output	1mA Step 10Ω to 100Ω Load		350		ns
	1kΩ Load		350		ns
WARM-UP TIME		1			min
OUTPUT					
Voltage Output Configuration					
Bipolar Range			±3		V
Output Current		±8			mA
Output Impedance			0.1		Ω
Short Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Range (±30%)			1.0		mA
Output Impedance (±30%)			1.7		kΩ
POWER SUPPLY					
Voltage, $+V_L$ and $+V_S$		4.75	5	13.2	V
Voltage, $-V_L$ and $-V_S$		−13.2	−5	−4.75	V
Current, +I, V_L and V_S = +5V, 10MHz Clock			10	**17**	mA
Current, −I, $-V_L$ and $-V_S$ = −5V, 10MHz Clock			−25	**−35**	mA
Current, +I, V_L and V_S = +12V, 10MHz Clock			12		mA
Current, −I, $-V_L$ and $-V_S$ = −12V, 10MHz Clock			−27		mA
POWER DISSIPATION					
V_S and V_L = ±5V, 10MHz Clock			110	**260**	mW
V_S and V_L = ±12V, 10MHz Clock			300		mW
TEMPERATURE RANGE					
Specification		0		+70	°C
Operation		−25		+70	°C
Storage		−60		+100	°C

Specifications subject to change without notice.
Specifications shown in boldface are tested on all production units at final test.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . .0 to 13.2V
V_S to AGND . . . . . .0 to 13.2V
$-V_L$ to DGND. . . . . .−13.2 to 0V
$-V_S$ to AGND . . . . . .−13.2 to 0V
Digital Inputs to DGND . . . . . .−0.3 to V_L
AGND to DGND . . . . . .±0.3V
Short Circuit Protection . . . . . .Indefinite Short to Ground
Soldering . . . . . .+300°C, 10sec
Storage Temperature . . . . . .−60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Analog Negative Power Supply
2	DGND	Digital Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Data Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model	THD @ FS	Package Options*
AD1856N	0.008%	N-16
AD1856N-J	0.004%	N-16
AD1856N-K	0.0025%	N-16

*See Section 14 for package outline information.

Definition of Specifications

TOTAL HARMONIC DISTORTION

Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency. It is expressed in percent (%) or decibels (dB).

THD is a measure of the magnitude and distribution of linearity error and differential linearity error. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is the primary measure of dynamic performance.

DYNAMIC RANGE

Dynamic Range is the specification that indicates the ratio of the smallest signal the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dB). The theoretical dynamic range of an n-bit converter is approximately (6×n) dB. In the case of the 16-bit AD1856, that is 96dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise and quantization and other errors.

BIPOLAR ZERO ERROR

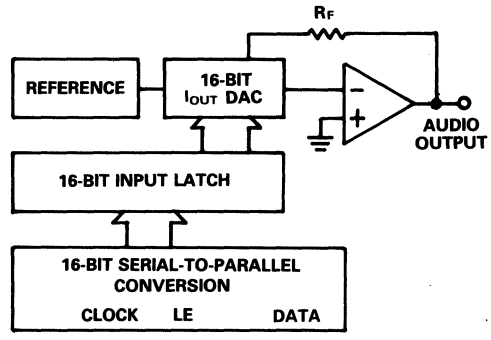
Bipolar Zero Error is the deviation in the actual analog output from the ideal output (0V) when the 2s complement input code representing half scale (all 0s) is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.



AD1856 Block Diagram

FUNCTIONAL DESCRIPTION

The AD1856 is a complete, monolithic 16-bit PCM audio DAC. No additional external components are required for operation. As shown in the block diagram, each chip contains a voltage reference, an output amplifier, a 16-bit DAC, a 16-bit input latch and a 16-bit serial-to-parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This circuitry produces an output voltage that is stable over time and temperature changes.

The 16-bit D/A converter uses a combination of segmented decoder and R-2R architectures to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error resulting in low output distortion.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew-rate and optimum settling time. When combined with the onboard feedback resistor, the output op amp can convert the output current of the AD1856 to a voltage output.

ANALOG CIRCUIT CONSIDERATIONS

GROUNDING RECOMMENDATIONS

The AD1856 has two pins, designated ANALOG and DIGITAL ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1856 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 1, the analog and digital grounds should be connected together at one point in the system.

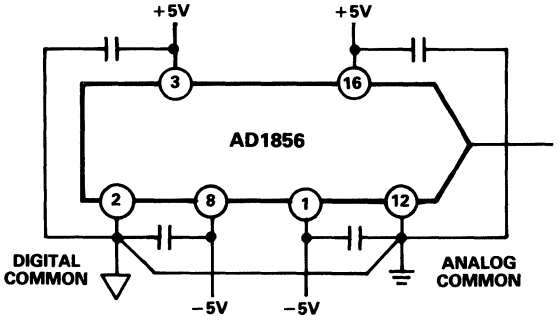


Figure 1. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1856 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from ±5V to ±12V.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to operate from ±5V to ±12V subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portions of the system, thus contributing to good performance. However,

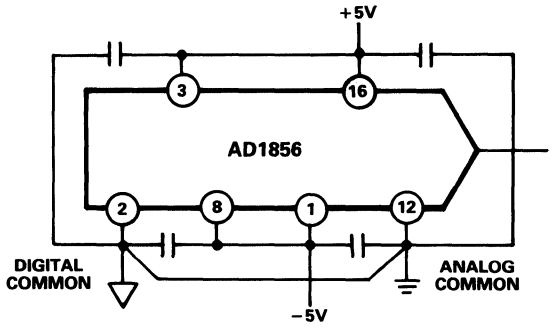


Figure 2. Alternate Recommended Schematic

four separate voltage supplies are not necessary for good circuit performance. For example, Figure 2 illustrates a system where only a single positive and a single negative supply are available. Given that these two supplies are within the range of ±5V to ±12V, they may be used to power the AD1856. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low-pass filters in the individual power supply leads.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

TOTAL HARMONIC DISTORTION

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

Analog Devices tests and grades all AD1856s on the basis of THD performance. A block diagram of the test setup is shown in Figure 3. In this test setup, a digital data stream, representing a 0db, −20dB or −60dB sine wave is sent to the device under test. The frequency of this waveform is 990.5Hz. Input data is sent to the AD1856 at a $4\times F_S$ rate (176.4kHz). The AD1856 under test produces an analog output signal with the on-board op amp.

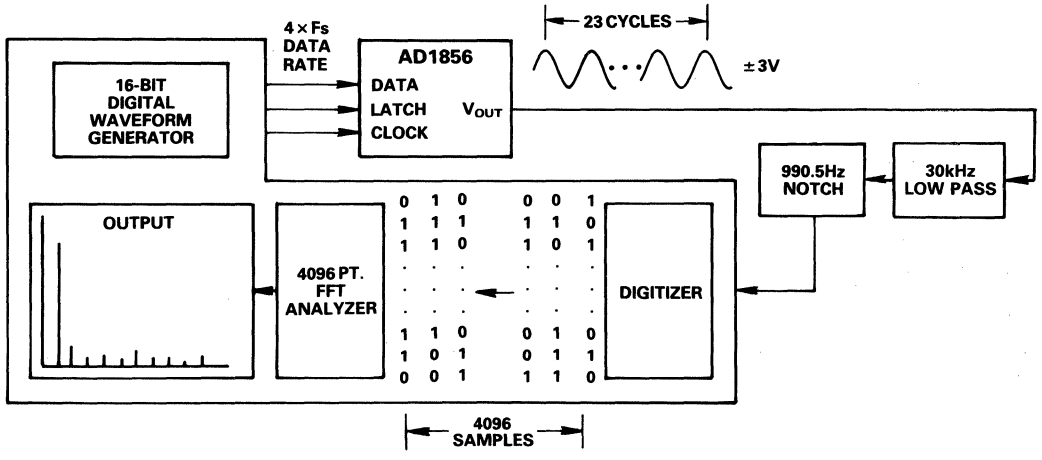


Figure 3. Block Diagram of Distortion Test Circuit

The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of sine wave. A 4096 point FFT is performed on the results of the test. Based on the first 9 harmonics of the fundamental 990.5Hz output wave, the total harmonic distortion of the device is calculated. Neither a deglitcher nor an MSB trim is used during the THD test.

The circuit design, layout and manufacturing techniques employed in the production of the AD1856 result in excellent THD performance. Figure 4 shows the typical unadjusted THD performance of the AD1856 for various amplitudes of a 1kHz output signal. As can be seen, the AD1856 offers excellent performance, even at amplitudes as low as −60dB. Figure 5 illustrates the typical THD vs. frequency performance.

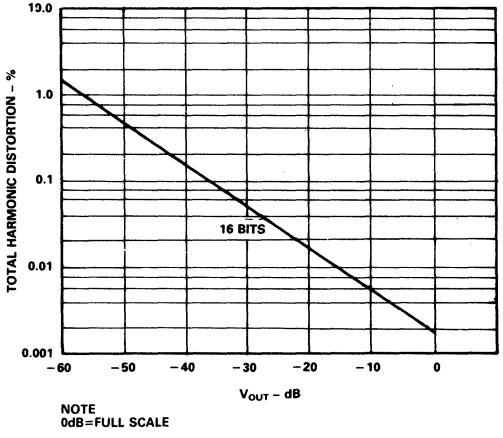


Figure 4. Typical Unadjusted THD vs. Amplitude

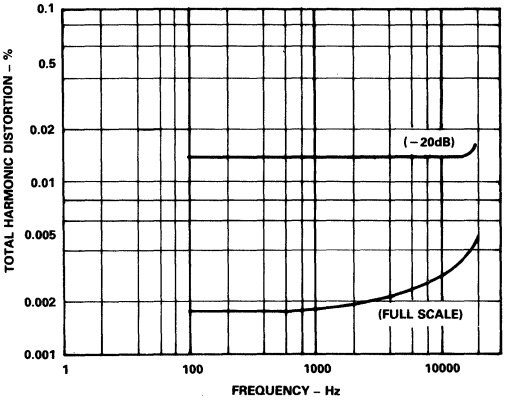


Figure 5. Typical THD vs. Frequency

OPTIONAL MSB ADJUSTMENT

Use of an optional adjustment circuit allows residual differential linearity error around midscale to be eliminated. These errors are especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases and THD increases.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 6 may be used. This circuit allows the differential linearity error at midscale to be zeroed out. However, no adjustments are required to meet data sheet specifications.

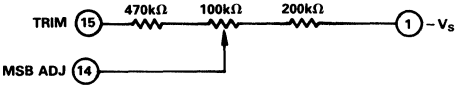


Figure 6. Optional THD Adjust Circuit

DIGITAL CIRCUIT CONSIDERATIONS

Input Data

Data is transmitted to the AD1856 in a bit stream composed of 16-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation: the Data, Clock and Latch Enable signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 16th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 7 illustrates the general signal requirements for data transfer for the AD1856.

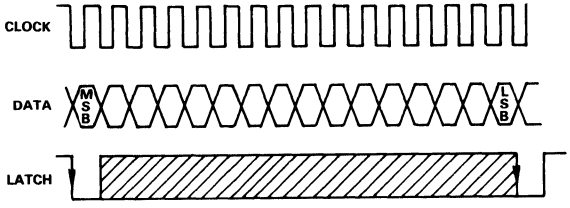


Figure 7. Signal Requirements of AD1856

Figure 8 provides the specific timing requirements that must be met in order for the data transfer to be accomplished properly.

The input pins of the AD1856 are both TTL and 5V CMOS compatible, independent of power supply voltages used.

The input requirements illustrated in Figures 7 and 8 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1856 input clock can run at a 10MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× oversampling reconstruction. The application section of this data sheet contains additional guides for using the AD1856 with various DSP filter chips available from Sony, NPC and Yamaha.

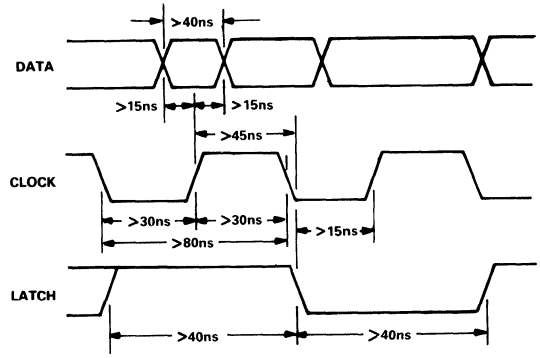


Figure 8. Timing Relationships of Input Signals

APPLICATIONS OF THE AD1856 PCM AUDIO DAC

The AD1856 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car and home compact disc player, digital audio-amplifier and DAT systems can all use the AD1856. Various circuit architectures are popular in these systems. They include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right) or even multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions including reproduction at the sample rate F_S (1×), at twice the sample rate(2×F_S), at four times the sample rate (4×F_S) and even at eight times the sample rate (8×F_S). F_S is 44.1kHz for CD and 48kHz for DAT applications.

One DAC per System

Figure 9 shows a circuit using one AD1856 per system to reproduce both stereo channels of a typical first generation digital

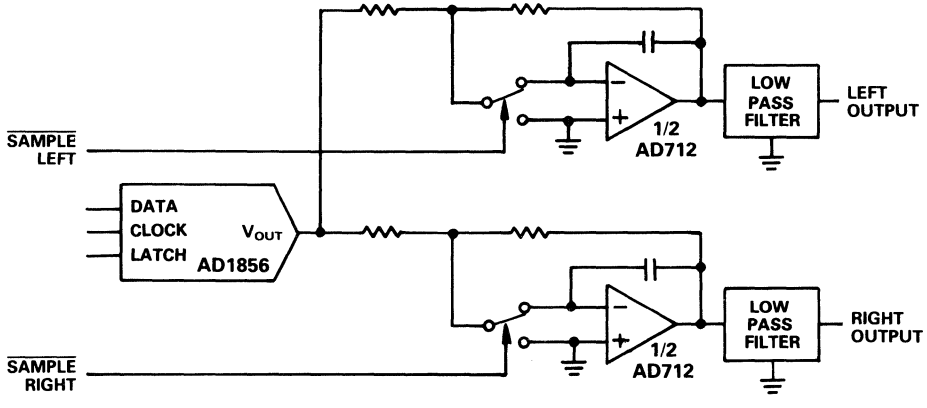


Figure 9. AD1856 in a One DAC per System Architecture

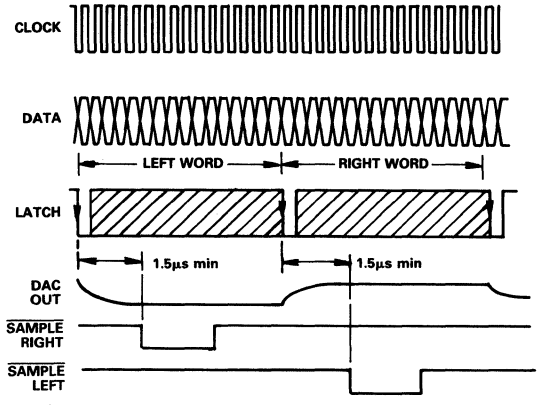


Figure 10. Control Signals for One DAC Circuit

audio system. The input data is fed to the AD1856 in a format which alternates between left channel data and right channel data. The output of the AD1856 is switched between the left channel and right channel output sample/hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1856. The timing diagram for the control signals for this circuit is shown in Figure 10.

The architecture illustrated in Figure 9 is suitable for low-end home or portable systems. However, its usefulness in mid- or high-end digital audio reproduction is limited by the phase delay which is introduced in the multiplexed output. This phase delay is due to the fact that the information contained in the input bit stream represents left and right channel audio sampled simultaneously but reconstructed alternately. One obvious solution to this problem may be arrived at by incorporating a third, noninverting SHA to delay the output of one channel to "catch up to" the other channel. This eliminates the phase shift by restoring simultaneous reproduction. This solution is illustrated in Figure 11.

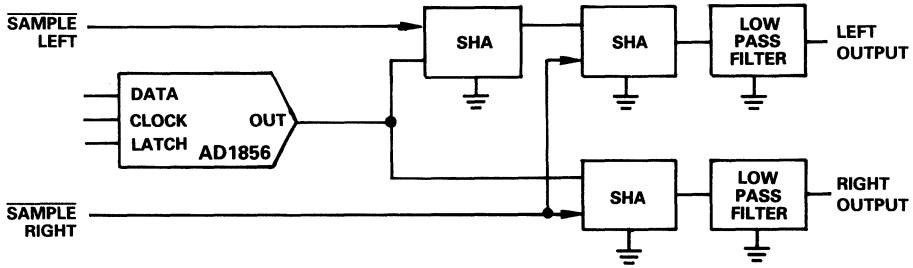


Figure 11. Third SHA Eliminates Phase Delay

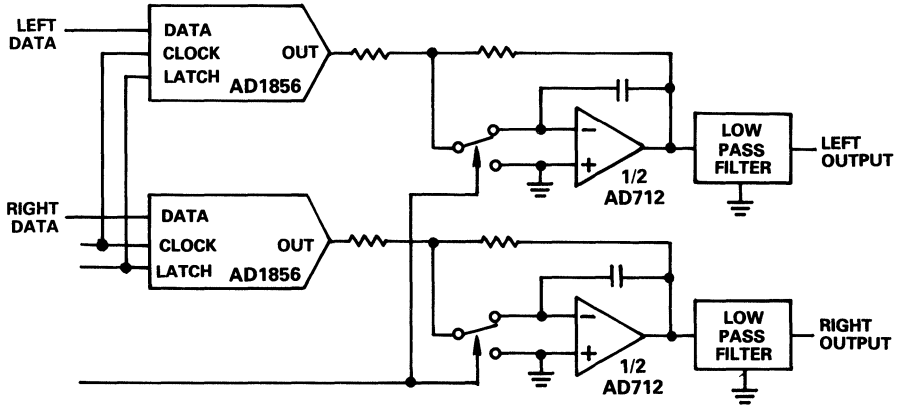


Figure 12. One DAC per Channel Architecture

One DAC per Channel

Another approach used to eliminate phase delay between left and right channels employs one DAC per channel. In this architecture, the input data bit streams for the left channel and the right channel are simultaneously sent and latched into each DAC. This "second generation" approach, shown in Figure 12, is suitable for higher performance digital-audio playback units.

Two DACs per Channel (Four DAC System)

Another architecture uses two DACs per channel. In this scheme, shown in Figure 13, each DAC reproduces one half of the output waveform. The advantage obtained is that midscale differential linearity error no longer effects the zero-crossing points of the waveforms. Its effects are shifted to the points where the output waveform crosses ±3/4 full scale. The result is that THD performance for low amplitude signals is greatly improved. Not shown in Figure 13 is a VLSI circuit required to separate the incoming data into the appropriate form required by each DAC.

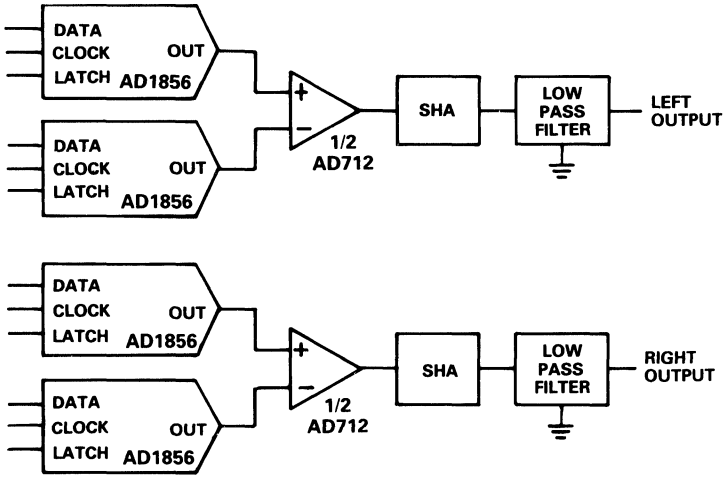


Figure 13. Two DACs per Channel Eliminate Midscale Distortion from the Zero-Crossing Points

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term which refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1kHz. Popular oversampling rates are 2× or 4× F_S yielding reconstruction rates of 88.2 and 176.4kHz, respectively.

Oversampling is used to ease the performance constraints of the low-pass filters which usually follow the reconstruction DAC. In any signal reconstructed from sampled data, unwanted frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency. When a 44.1kHz reconstruction frequency is used, the actual frequency band of interest is 20Hz to 20kHz, and the band of unwanted "image" frequency components extends from 44.1kHz to approximately 24kHz and from 44.1kHz to 64kHz.

These unwanted components must be removed with a low-pass filter of very high order. First generation digital audio systems often use low-pass filters of 9, 11 and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture and can produce distortion due to varying group delay characteristics.

When a 2× reconstruction frequency (88.2kHz) is used, the lowest unwanted frequency components now extend down to approximately 68kHz. A 4× rate (176.4kHz) has unwanted components extending down to approximately 156kHz. The filter response needed to remove these frequency components can now be less steep. This means that a lower order filter may be used resulting in less distortion at lower cost. Linear filters with 3 or 5 poles are adequate to do the job and are quite common in digital audio products employing oversampling techniques.

Oversampling techniques require that the serial input data stream run at the same integral multiple of the original data rate. So, while the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip which is located "upstream" from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Since the digital filters actually interpolate these additional reconstruction points, they have earned the name "interpolation filters."

The AD1856 is compatible with popular digital filter chips used in digital audio products such as the NPC SM5807, NPC SM5805, Yamaha YM3414, and Sony CXD1136.

DUAL DAC, 4× F_S OVERSAMPLING ARCHITECTURE

Figure 14 illustrates the use of an NPC digital filter chip with two AD1856 audio DACs. This scheme achieves four times oversampling reconstruction with a dedicated DAC per channel. In this example of a typical compact disc player application, the digital filter chip accepts serial input words from the digital decoder/processor at a 44.1kHz sample rate. Through the use of oversampling, the SM5807 transmits data to the two DACs at a 176.4kHz rate. The serial DAC input data is sent out of the DOUT pin to the serial inputs of the DACs. Left channel and right channel data are sent alternately down the same wire. The Left/Right Channel Output signal, $\overline{\text{LRCO}}$ and two logic gates demultiplex the data clock signals from BCKO. In this example, the BCKO rate is 192×F_S. However, a 196×F_S clock can be used if $\overline{\text{SCSL}}$ is wired to a logic zero. Finally, left and right channel deglitching signals are provided. At the user's option, these signals may be used to control external sample-hold amplifiers in order to obtain optimal performance.

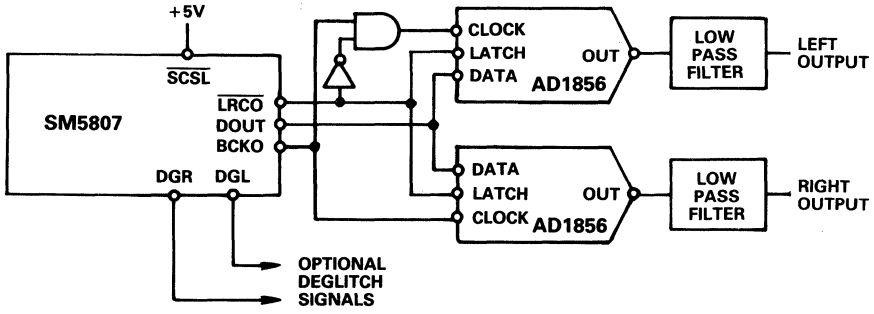


Figure 14. NPC SM5807 and AD1856 Interface

ACHIEVING 8× F_S OVERSAMPLING WITH AD1856S AND YAMAHA YM3414

Figure 15 illustrates the combination of a Yamaha YM3414 digital filter chip and two AD1856 audio DACs. In this scheme, the use of a 16.9344MHz clock allows an 8 times oversampling rate for extremely high performance. In addition, a lower-order low-pass filter may be used without sacrificing performance. The DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left and right channel output pins on the YM3414. As before, optional sample/hold signals are provided.

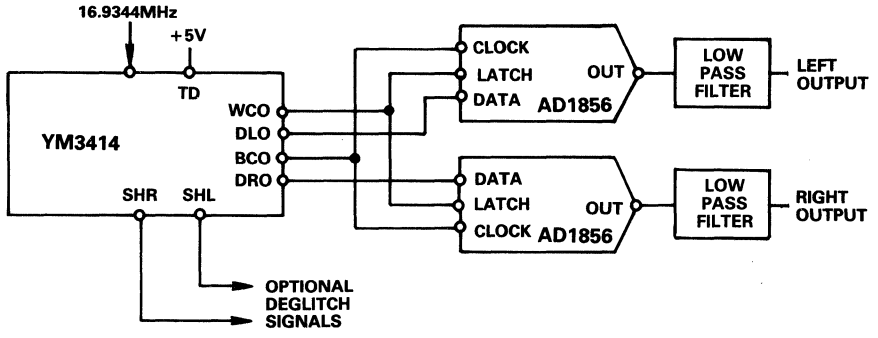


Figure 15. Yamaha YM3414 and AD1856 Interface

ANALOG DEVICES

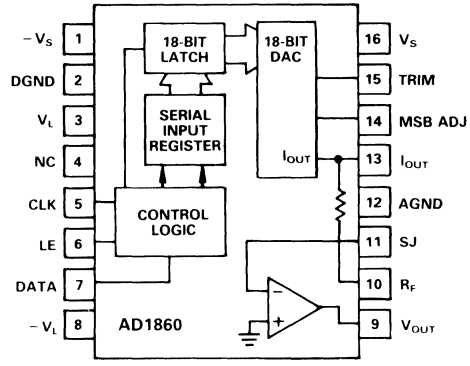
18-Bit PCM Audio DAC

AD1860

FEATURES
- 0.002% THD + Noise
- Fast Settling Permits 8× Oversampling
- ±3V Output
- Optional Trim Allows Superlinear Performance
- ±5V to ±12V Operation
- 16-Pin Plastic DIP and SOIC Packages
- Industry Standard Pinout
- 2s Complement, Serial Input

APPLICATIONS
- High End Compact Disc Players
- Digital Audio Amplifiers
- DAT Recorders and Players
- Synthesizers and Keyboards

AD1860 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1860 is a monolithic 18-bit PCM Audio DAC. Each device provides a voltage output amplifier, 18-bit DAC, 18-bit serial to parallel input register and voltage reference. The digital portion of the AD1860 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1860 is fabricated with bipolar and MOS devices as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reproductions of low amplitude signals. Output glitch is also small contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3V signal at load currents up to 8mA. When used in current output mode, the AD1860 provides a ±1mA output signal. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 12.5MHz data rate. This serial input port is compatible with second generation digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4× and 8× sampling frequencies.

The AD1860 can operate with ±5V to ±12V power supplies making it suitable for both the portable and home use markets. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110mW typical with ±5V supplies and is 225mW typical when +5V/−12V supplies are used.

The AD1860 is available in either a 16-pin plastic DIP or a 16-pin plastic SOIC surface mount package. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 to ±13.2V.

PRODUCT HIGHLIGHTS

1. 18-bit resolution provides 108dB dynamic range.
2. No external components are required.
3. Operates with ±5V to ±12V supplies.
4. 16-pin DIP or space saving SOIC package.
5. 110mW power dissipation.
6. 1.5μs settling time permits 2×, 4× and 8× oversampling.
7. ±3V or ±1mA output capability.
8. THD + Noise is 100% tested.

SPECIFICATIONS (T_A at +25°C and ±5V supplies unless otherwise noted)

	Min	Typ	Max	Units
RESOLUTION			**18**	Bits
DIGITAL INPUTS V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH}=V_L$			**1.0**	μA
I_{IL}, $V_{IL}=0.4$			**−10**	μA
Clock Input Frequency	**12.5**			MHz
ACCURACY				
Gain Error		±2.0		%
Midscale Output Voltage		±30		mV
Differential Linearity Error		±0.001		% of FSR
TOTAL HARMONIC DISTORTION + NOISE				
0dB, 990.5Hz AD1860N-K, R-K		0.002	**0.0025**	%
AD1860N-J, R-J		0.002	**0.004**	%
AD1860N, R		0.004	**0.008**	%
−20dB, 990.5Hz AD1860N-K, R-K		0.006	**0.020**	%
AD1860N-J, R-J		0.010	**0.020**	%
AD1860N, R		0.010	**0.040**	%
−60dB, 990.5Hz AD1860N-K, R-K		0.9	**2.0**	%
AD1860N-J, R-J		0.9	**2.0**	%
AD1860N, R		0.9	**4.0**	%
SIGNAL TO NOISE RATIO (A-Weight Filter)	**102**	108		dB
DRIFT (0 to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.0015% of FSR)				
Voltage Output, 6V Step		1.5		μs
1LSB Step		1.0		μs
Slew Rate		9		V/μs
Current Output 1mA Step 10Ω to 100Ω Load		350		ns
1kΩ Load		350		ns
MONOTONICITY		15		Bits
OUTPUT				
Voltage Output Configuration				
Bipolar Range	**±2.88**	±3.0	**±3.12**	V
Output Current	±8			mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage V_L and V_S	4.75		13.2	V
Voltage $-V_L$ and $-V_S$	−13.2		−4.75	V
Current +I, V_L and $V_S=5V$, 10MHz Clock		10.0	**13.0**	mA
−I, $-V_L$ and $-V_S=-5V$, 10MHz Clock		12.0	**−15.0**	mA
Current +I, V_L and $V_S=12V$, 10MHz Clock		10.5		mA
−I, $-V_L$ and $-V_S=-12V$, 10MHz Clock		13.5		mA
Current +I, V_L and $+V_S=+5V$, 10MHz Clock		10		mA
−I, $-V_L$ and $-V_S=-12V$, 10MHz Clock		14		mA
POWER DISSIPATION				
V_S and $V_L=\pm5V$, 10MHz Clock		110		mW
V_S and $V_L=\pm12V$, 10MHz Clock		300		mW
V_S and $V_L=+5V$, $-V_S$ and $-V_L=-12V$, 10MHz Clock		225		mW

	Min	Typ	Max	Units
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

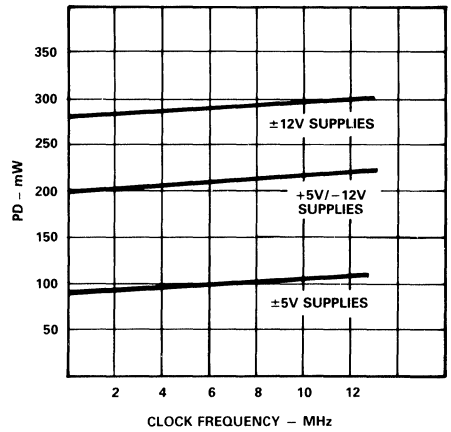
Specifications subject to change without notice.

TYPICAL PERFORMANCE

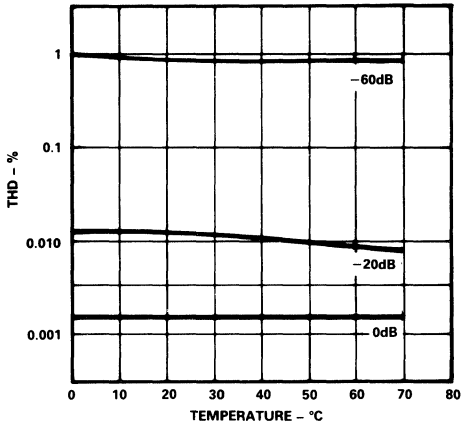
ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 13.2V
V_S to AGND . . . . . 0 to 13.2V
$-V_L$ to DGND . . . . . −13.2 to 0V
$-V_S$ to AGND . . . . . −13.2 to 0V
Digital Inputs to DGND . . . . . −0.3 to V_L
AGND to DGND . . . . . ± 0.3V
Short Circuit . . . . . .Indefinite Short to Ground
Soldering . . . . . +300°C, 10sec
Storage Temperature . . . . . −60°C to +100°C

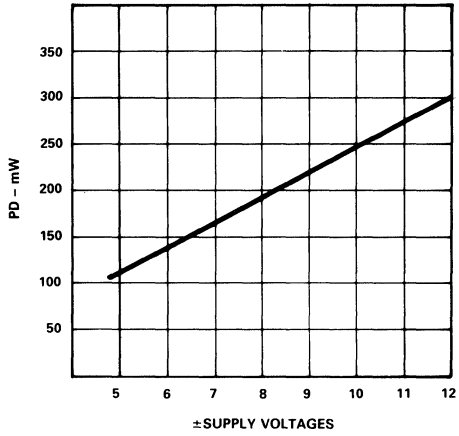
Note
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Power Dissipation vs. Clock Frequency



THD vs. Temperature



Power Dissipation vs. Supply Voltages

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN ASSIGNMENTS		
1	$-V_S$	Analog Negative Power Supply
2	DGND	Logic Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Data Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

ORDERING GUIDE

Model and Package Option*

DIP Package (N-16)	Surface Mount (R-16)	THD @ FS
AD1860N	AD1860R	0.008%
AD1860N-J	AD1860R-J	0.004%
AD1860N-K	AD1860R-K	0.0025%

*See Section 14 for package outline information.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is a primary measure of dynamic performance.

DYNAMIC RANGE

Dynamic Range is the specification that indicates the ratio of the smallest signal the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dBs). The theoretical dynamic range of an n-bit converter is (6×n) dB. In the case of the 18-bit AD1860, that is 108dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise and other errors.

MIDSCALE ERROR

Midscale Error, or bipolar zero error, is the deviation of the actual analog output from the ideal output (0V) when the 2s complement input code representing half scale is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

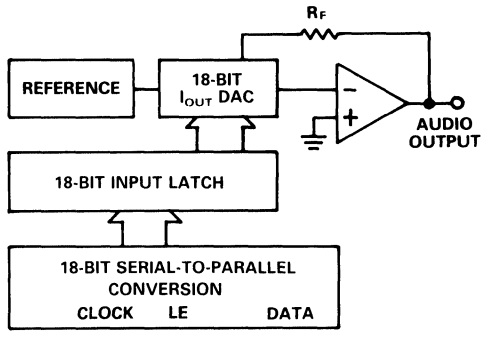
Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output with no signal present to the amplitude of the output when a full-scale output is present. This is measured with a standard A-Weight filter.



AD1860 Block Diagram

FUNCTIONAL DESCRIPTION

The AD1860 is a complete monolithic 18-bit PCM Audio DAC. No additional external components are required for operation. As shown in the block diagram, each chip contains a voltage reference, an output amplifier, an 18-bit DAC, an 18-bit input latch and an 18-bit serial to parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This combination of elements produces a reference voltage that is unaffected by changes in temperature and age. The DAC output voltage, which is derived from the reference voltage, is also unaffected by these environmental changes.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew rate and optimum settling time. When combined with the on chip feedback resistor, the output op amp converts the output current of the AD1860 to a voltage output.

The 18-bit D/A converter uses a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity error resulting in low output distortion.

The input register and serial to parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. This contributes to the overall low power dissipation of the AD1860.

Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1860 has two pins, designated Analog and Digital ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1860 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 1, the analog and digital grounds should be connected together at one point in the system.

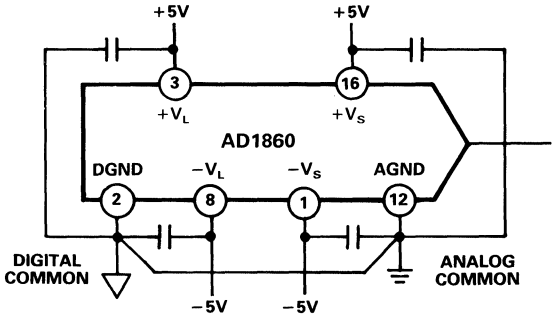


Figure 1. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1860 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from ±5V to ±12V.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to be operated from ±5V to ±12 V subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portion of the system, thus contributing to good performance. However, four separate voltage supplies are not necessary for good circuit performance. For example, Figure 2 illustrates a system where only a single positive and a single negative supply are available.

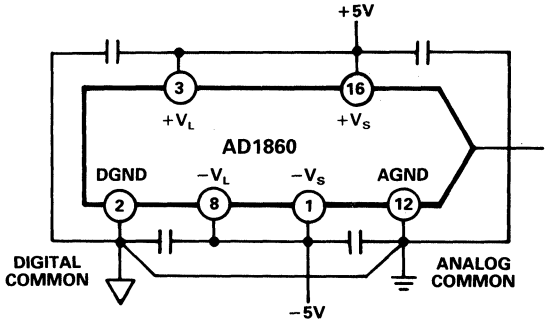


Figure 2. Typical Power Supply Sensitivity

Given that these two supplies are within the range of ±5V to ±12V, they may be used to power the AD1860. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low pass filters in the individual power supply leads.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

TOTAL HARMONIC DISTORTION + NOISE

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

By combining noise measurement with THD measurement, a THD+N specification is produced. This specification measures all undesirable signal produced by the DAC, including harmonic products of the test tone as well as noise.

Analog Devices tests and grades all AD1860s on the basis of THD+N performance. A block diagram of the test setup is shown in Figure 3. In this test setup, a digital data stream representing a 0dB, −20dB or −60dB sinewave is sent to the device under test. The frequency of this waveform in 990.5 Hz.

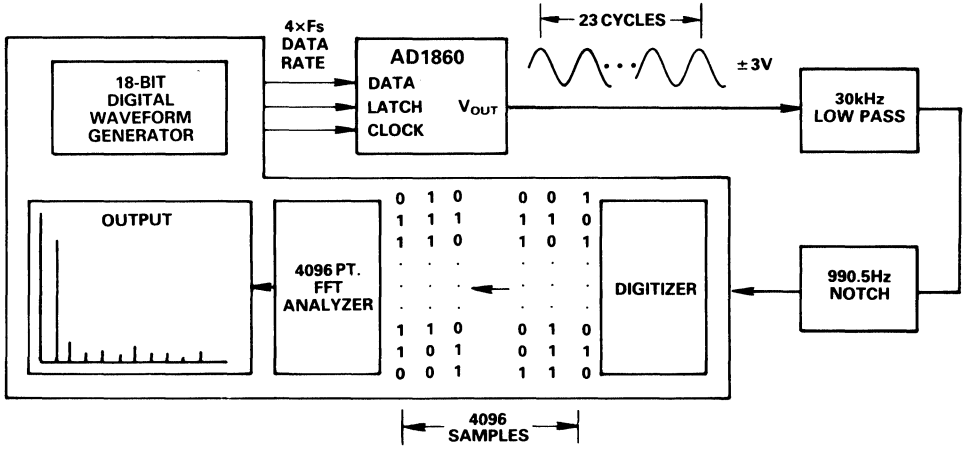


Figure 3. Block Diagram of DistortionTest Circuit

Input data is sent to the AD1860 at a $4\times F_S$ rate (176.4kHz). The AD1860 under test produces an output signal with its onboard op amp. The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sinewave. A 4096 point FFT is performed on the results of the test. Based on the harmonics of the fundamental 990.5Hz test tone and the noise components, the total harmonic distortion + noise of the device is calculated. Neither a deglitcher nor an MSB trim is used during this test.

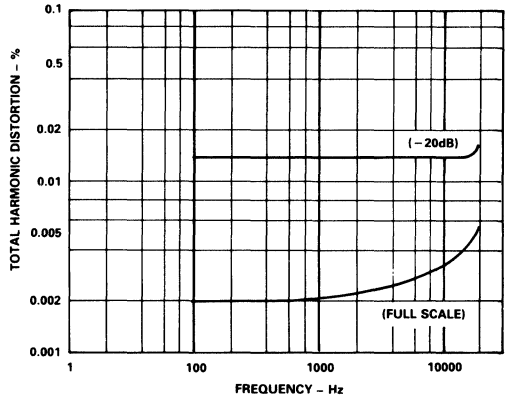


Figure 4. Typical THD vs Frequency

The circuit design, layout and manufacturing techniques employed in the production of the AD1860 result in excellent THD performance. Figure 4 shows the typical unadjusted THD performance of the AD1860 for various amplitudes and frequencies of output signals. As can be seen, the AD1860 offers excellent performance, even at low amplitudes.

OPTIONAL MSB ADJUSTMENT

Use of an optional adjust circuitry allows residual differential linearity error around midscale to be eliminated. This error is especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases, thereby increasing THD.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 5 may be used to improve performance.

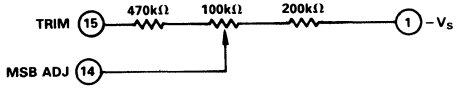


Figure 5. Optional THD Adjust Circuit

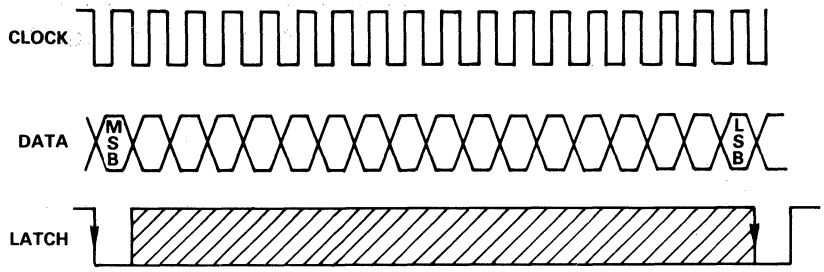


Figure 6. Signal Requirements for AD1860

DIGITAL CIRCUIT CONSIDERATIONS

Input Data

Data is transmitted to the AD1860 in a bit stream composed of 18-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 18th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 6 illustrates the general signal requirements for data transfer for the AD1860.

Timing

Figure 7 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1860 are both TTL and 5V CMOS compatible, independent of the power supplies used. The input requirements illustrated in Figures 6 and 7 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1860 input clock can run at a 12.5MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× oversampling reconstruction. The application section of this datasheet contains additional guides for using the AD1860 with various DSP filter chips available from Sony, NPC and Yamaha.

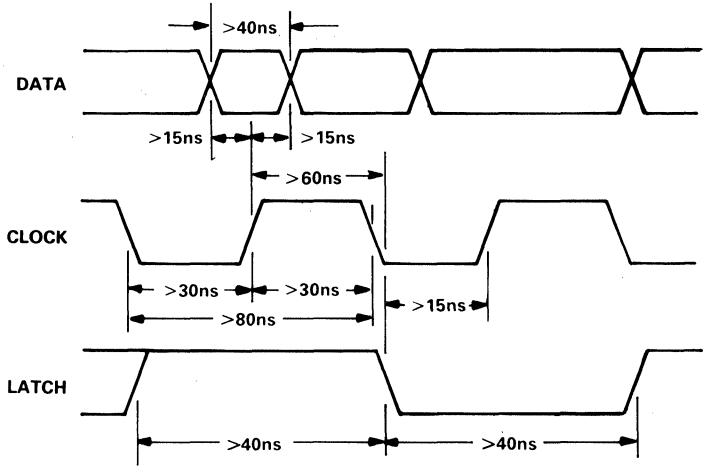


Figure 7. Timing Relationships of Input Signals

APPLICATIONS OF THE AD1860 PCM AUDIO DAC

The AD1860 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car and home compact disc player, digital audio amplifier and DAT schemes can all use the AD1860. Various circuit architectures are popular in these systems. They include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right) or multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions including reproduction at the sample rate F_S (1×), at twice the sample rate (2×F_S), at four times the sample rate (4×F_S) and even at eight times the sample rate (8×F_S). F_S is 44.1kHz for CD and 48kHz for DAT applications.

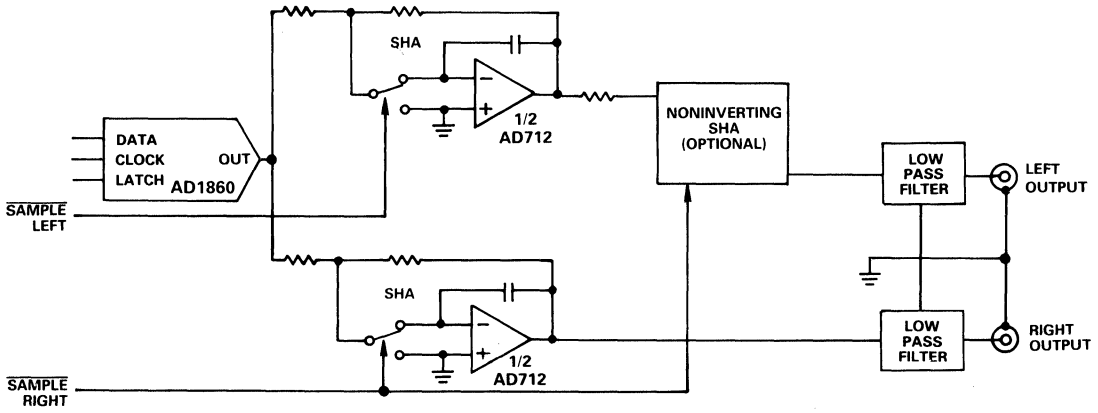


Figure 8. AD1860 in a One DAC per System Architecture

One DAC per System

Figure 8 shows a circuit using one AD1860 per system to reproduce both channels of a typical first generation stereo digital audio system. The input data is fed to the AD1860 in a format which alternates between left channel data and right channel data. The output of the AD1860 is switched between the left channel and right channel output sample/hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1860. The timing diag-am for the control signals for this circuit are shown in Figure 9.

However, when only two SHAs are used, the actual system performance is limited by the phase delay introduced by the demultiplexed format. This undesirable phase delay is caused by the fact that the data words presented to the inputs of the DAC represent samples taken at precisely the same point in time. But when reconstructed and demultiplexed by a single DAC, these same outputs occur at slightly different times.

By incorporating a noninverting SHA into the circuit, the phase delay can be eliminated. In Figure 8, the optional SHA ensures that the left channel output appears at the same time as the right channel output. This minor change to the circuit eliminates the artificially induced phase delay by restoring simultaneous outputs.

Following the outputs of the SHAs are low pass filters. These filters are required in any sampled data system to remove unwanted aliased components introduced by the sample and reconstruction operations.

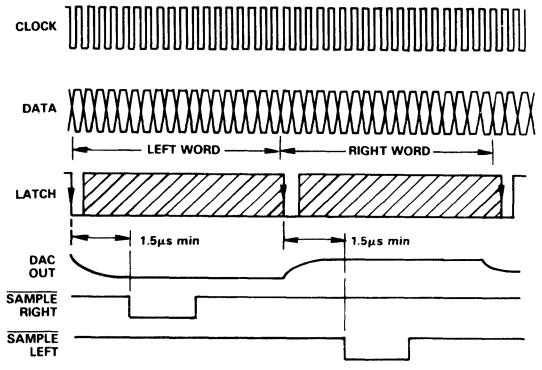


Figure 9. Control Signals for One DAC Circuit

One DAC per Channel

A second approach used to eliminate phase delay between left and right channels employs one DAC per channel. In this architecture, the input data bitstream for each channel is transmitted and then latched into the input register of each DAC. This "second generation" approach is illustrated in Figure 10. A standard implementation of a low pass filter is shown at the output of each DAC. An optional sample/hold amplifier could be connected between the DACs and the LPFs to deglitch the outputs. This is not required, however, to achieve the specified performance.

Two DACs per Channel

Another architecture uses two DACs per channel. In this scheme each DAC reproduces one half of the output waveform. The advantage obtained with this structure is that midscale differential linearity error no longer affects the zero crossing points of the waveforms. Its effects are shifted to the points where the output waveform crosses ±3/4 full scale. The result is that THD performance for low amplitude signals is greatly improved.

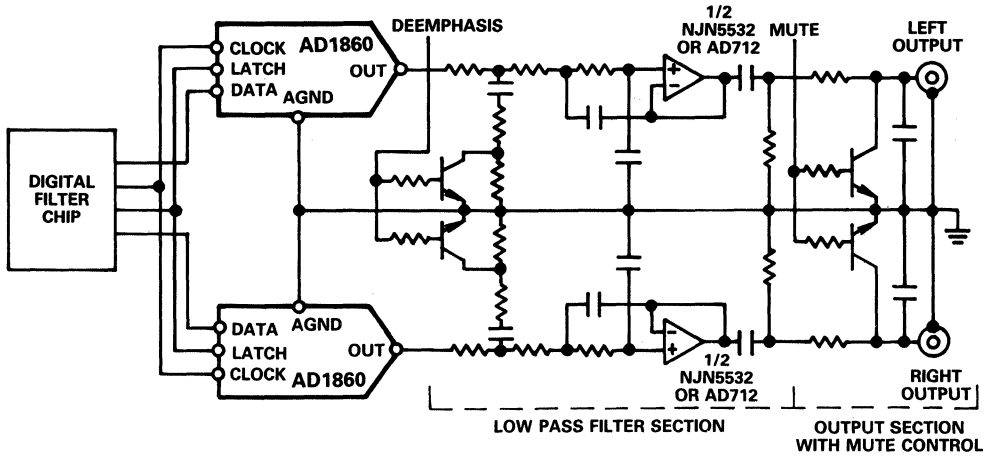


Figure 10. One DAC per Channel Architecture with LPF

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term which refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1kHz. Popular oversampling rates are 2× or 4×F_S, yielding reconstruction rates of 88.2 and 176.4kHz, respectively.

Oversampling is used to ease the performance constraints of the low pass filters which follow the reconstruction DAC. In any signal reconstructed from sampled data, unwanted frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency. When a 44.1kHz reconstruction frequency is used, the actual frequency band of interest is 20Hz to 20kHz, and the band of unwanted "image" frequency components extends from 44.1kHz to approximately 24kHz. These unwanted components must be removed with a low-pass filter of very high order. First generation digital audio systems often used low-pass filters of 9, 11 and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture and can produce distortion due to varying group delay characteristics.

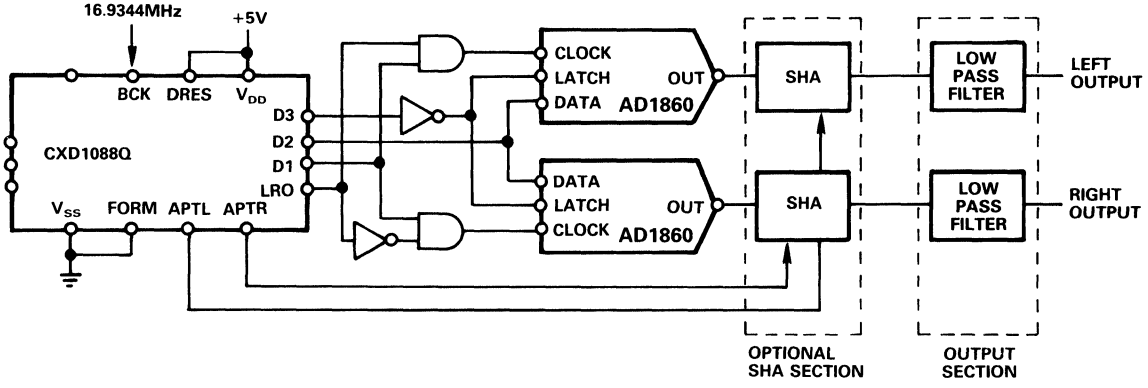
When a 2×reconstruction frequency (88.2kHz) is used, the lowest frequency components now extend down to approximately 68kHz. A 4×rate (176.4kHz) has unwanted components extending down to approximately 156kHz. The filter response needed to remove these frequency components can now be less steep. This means that a lower order filter may be used resulting in less distortion at lower cost. Linear filters with 3 or 5 poles, as shown in Figure 10, are adequate to do the job and are quite common in digital audio products employing oversampling techniques.

Oversampling techniques require the serial input data stream to run at the same integral multiple of the original data rate. So, while the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip (DSP) which is located "upstream" from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Since the digital filters actually interpolate these additional reconstruction points, they have earned the name "interpolation filters".

The AD1860 is compatible with popular digital filter chips used in digital audio products such as the Sony CXD1088, the Yamaha YM3434 and the NPC SM5813.

Figure 11 illustrates the combination of a second generation digital filter chip, the Sony CXD1088, and the AD1860 audio DAC. The digital filter chip provides 18-bit data words to the DACs at $4\times F_S$. Very high performance can be achieved.



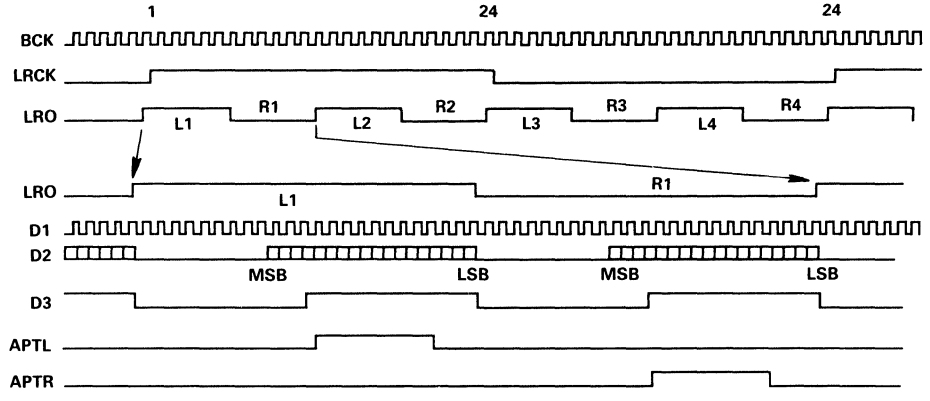


Figure 11. $4\times F_S$ with the CXD1088Q

Figure 12 illustrates the combination of a Yamaha YM3434 digital filter chip and two AD1860 audio DACs. This combination of components results in $8\times F_S$ oversampling reconstruction rates. This rate allows the use of lower order output low pass filters than would be required with lower oversampling rates, without sacrificing performance. In this high performance CD player application, the DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left and right channel output pins on the YM3434. This implementation does not require any external components to achieve the full 108dB dynamic range afforded by the 18-bit AD1860 audio DAC. As before, optional sample/hold signals are provided.

Figure 13 shows the schematic for $8\times F_S$ when two AD1860s are used with an NPC SM5813AP/APT digital filter chip. As can be seen, this application is very similar to the one shown in Figure 12. See Figure 10 for an example of a typical LPF.

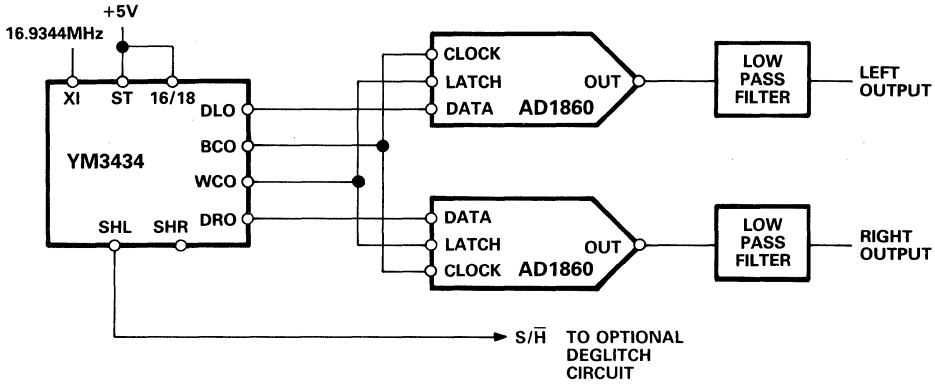


Figure 12. YM3434 and AD1860 Achieve $8\times F_S$

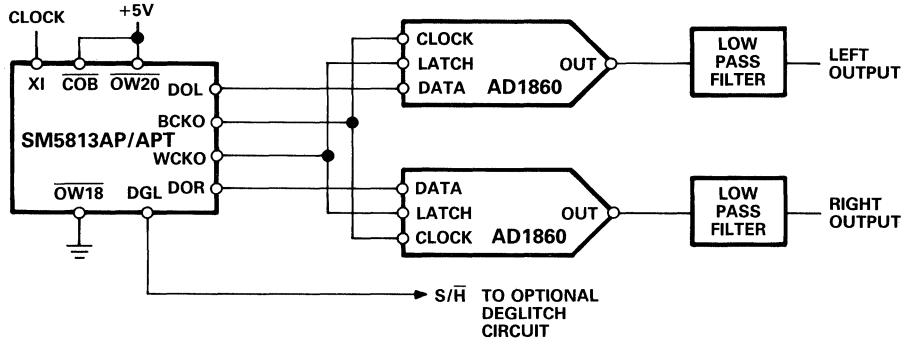


Figure 13. SM5813AP/APT and AD1860 Achieve $8\times F_S$

ANALOG DEVICES

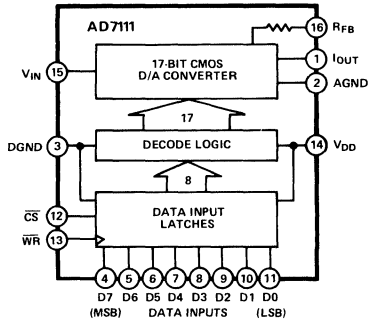
LOGDAC
CMOS Logarithmic D/A Converter

AD7111*

FEATURES
Dynamic Range: 88.5dB
Resolution: 0.375dB
On-Chip Data Latches
Full ±25V Input Range Multiplying DAC
Low Distortion
Single +5V Supply
Latch-Up Free (No Protection Schottky Required)

APPLICATIONS
Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators

AD7111 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The LOGDAC™ AD7111 is a CMOS multiplying D/A converter which can attenuate an analog input signal over the range 0 to −88.5dB in 0.375dB steps.

The degree of attenuation is determined by an 8-bit data word which is latched into on-chip data latches using microprocessor compatible control signals $\overline{CS}$ and $\overline{WR}$. Operating frequency range of the device is from dc to several hundred kHz.

The device is available in a standard 16-pin DIP and in a 20-terminal surface mount package.

*U.S. Patent No. 4521764
LOGDAC is a trademark of Analog Devices, Inc.

ORDERING INFORMATION[1, 2]

Specified Accuracy Range	Temperature Range and Package Options[3]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-16)	**Hermetic (Q-16)**	**Hermetic (Q-16)**
0 to 60dB	AD7111KN	AD7111BQ	AD7111TQ
0 to 72dB	AD7111LN	AD7111CQ	AD7111UQ
			LCCC[4] (E-20A)
0 to 60dB			AD7111TE
0 to 72dB			AD7111UE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]Analog Devices reserves to right to ship ceramic (package option D-16) packages in lieu of cerdip (package option Q-16) packages.
[3]See Section 14 for package outline information.
[4]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS (V_{DD} = +5V, V_{IN} = −10V dc, V_{PIN2} = V_{PIN1} = 0V output amplifier AD544 except where stated)

Parameter	AD7111L/C/U GRADES T_A = +25°C	AD7111L/C/U GRADES T_A = T_{min}, T_{max}	AD7111K/B/T GRADES T_A = +25°C	AD7111K/B/T GRADES T_A = T_{min}, T_{max}	Units	Conditions/Comments
NOMINAL RESOLUTION	0.375	0.375	0.375	0.375	dB	
ACCURACY RELATIVE TO 0dB ATTENUATION						
0.375dB Steps:						
Accuracy ⩽ ±0.17dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	Guaranteed attenuation ranges
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	for specified step sizes
0.75dB Steps:						
Accuracy ⩽ ±0.35dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5dB Steps:						
Accuracy ⩽ ±0.7dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	Full Range is from 0 to 88.5dB
3.0dB Steps:						
Accuracy ⩽ ±1.4dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
6.0dB Steps:						
Accuracy ⩽ ±2.7dB	0 to 72	0 to 60	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
GAIN ERROR	±0.1	±0.15	±0.15	±0.20	dB max	
V_{IN} INPUT RESISTANCE (PIN 15)	9/11/15	9/11/15	7/11/18	7/11/18	kΩ min/typ/max	
R_{FB} INPUT RESISTANCE (PIN 16)	9.3/11.5/15.7	9.3/11.5/15.7	7.3/11.5/18.8	7.3/11.5/18.8	kΩ min/typ/max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±10	±1	±10	μA max	Digital Inputs = V_{DD}
SWITCHING CHARACTERISTICS[1]						
t_{CS}	0	0	0	0	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	350	500	350	500	ns min	Write Pulse Width
t_{DS}	175	250	175	250	ns min	Data Valid to Write Setup Time
t_{DH}	10	10	10	10	ns min	Data Valid to Write Hold Time
t_{RFSH}	3	4.5	3	4.5	μs min	Refresh Time
POWER SUPPLY						
V_{DD}	+5	+5	+5	+5	V	
I_{DD}	1	4	1	4	mA max	Digital Inputs = V_{IH} or V_{IL}
	500	1000	500	1000	μA max	Digital Inputs = 0V or V_{DD}. See Figure 7.

NOTE
[1] Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.
V_{DD} = +5V, V_{IN} = −10V dc except where stated, V_{PIN1} = V_{PIN2} = 0V, output amplifier AD544 except where stated.

Parameter	AD7111L/C/U GRADES T_A = 25°C	AD7111L/C/U GRADES T_A = T_{min}, T_{max}	AD7111K/B/T GRADES T_A = +25°C	AD7111K/B/T GRADES T_A = T_{min}, T_{max}	Units	Conditions/Comments
DC Supply Rejection, ΔGain/ΔV_{DD}	0.001	0.005	0.001	0.005	dB per % max	ΔV_{DD} = ±10%, Input Code = 00000000
Propagation Delay	3.0	4.5	3.0	4.5	μs max	Full Scale Change Measured from $\overline{WR}$ going high, $\overline{CS}$ = 0V.
Digital to Analog Glitch Impulse	100	–	100	–	nV secs typ	Measured with ADLH0032CG as Output Amplifier for Input Code Transition 10000000 to 00000000. C1 of Figure 1 is 0pF
Output Capacitance, Pin 1	185	185	185	185	pF max	
Input Capacitance, Pin 15 and Pin 16	7	7	7	7	pF max	
Feedthrough at 1kHz	−94	−72	−92	−68	dB max	Feedthrough is also determined by circuit
Total Harmonic Distortion	−91	−91	−91	−91	dB typ	layout (see Figure 4).
Output Noise Voltage Density	70	70	70	70	nV/√Hz max	V_{IN} = 6V rms at 1kHz
Digital Input Capacitance	7	7	7	7	pF max	Includes AD544 Amplifier Noise

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (to DGND)	+7V
V_{IN} (to AGND)	+35V
Digital Input Voltage to DGND	−0.3V to V_{DD} +0.3V
Output Voltage (Pin 1) to AGND	−0.3V to V_{DD}
V_{REF} to AGND	±35V
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (K, L Versions)	0 to +70°C
Industrial (B, C Versions)	−25°C to +85°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: A measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

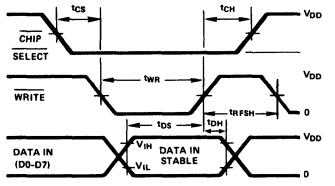
ACCURACY: The difference (measured in dB) between the ideal transfer function as listed in Table I and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL TO ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

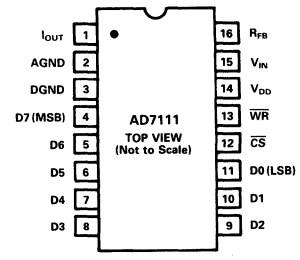
WRITE CYCLE TIMING DIAGRAM



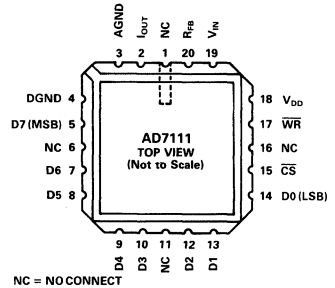
NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

PIN CONFIGURATIONS

DIP



LCCC



NC = NO CONNECT

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7111 consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital logic. The logic translates the 8-bit binary input into a 17-bit word which is used to drive the D/A converter. Input data on the D7–D0 bus is loaded into the input data latches using $\overline{CS}$ and $\overline{WR}$ control signals. The rising edge of $\overline{WR}$ latches the input data and initiates the internal data transfer to the decoder. A minimum time t_{RFSH}, the refresh time, is required for the data to propagate through the decoder before a new data write is attempted.

The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10\ \exp - \frac{0.375\ N}{20}$$

or

$$\left|\frac{V_O}{V_{IN}}\right| \text{ dB} = -0.375\ N$$

Where 0.375 is the step size (resolution) in dB and N is the input code in decimal for values 0 to 239. For $240 \leqslant N \leqslant 255$ the output is zero. Table I gives the output attenuation relative to 0dB for all possible input codes.

The graphs on the last page give a pictorial representation of the specified accuracy and monotonic ranges for all grades of the AD7111. High attenuation levels are specified with less accuracy than low attenuation levels. The range of monotonic behavior depends upon the attenuation step size used. For example, the AD7111L is guaranteed monotonic in 0.375dB steps from 0 to -54dB inclusive and in 0.75dB steps from 0 to -72dB inclusive. To achieve monotonic operation over the entire 88.5dB range it is necessary to select input codes so that the attenuation step size at any point is consistent with the step size guaranteed for monotonic operation at that point.

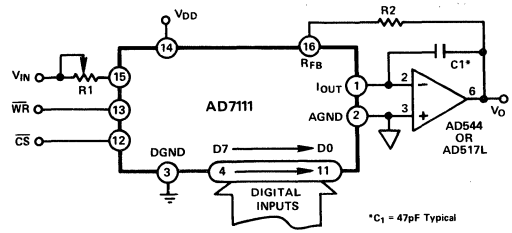


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7111 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, approximately doubles every 10°C—see Figure 11. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 60pF to 185pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A converters" which is available from Analog Devices, Publication Number G479—15—8/78.

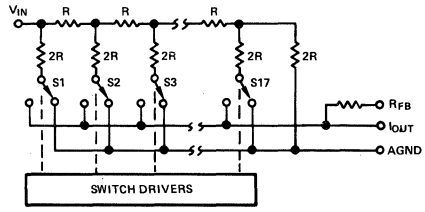
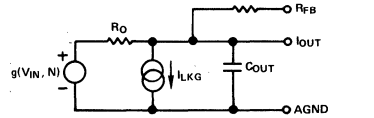


Figure 2. Simplified D/A Circuit of AD7111



g(VIN, N) IS THE THEVENIN EQUIVALENT VOLTAGE GENERATOR DUE TO THE INPUT VOLTAGE VIN. THE BINARY ATTENUATION FACTOR N AND THE TRANSFER FUNCTION OF THE R-2R LADDER.

Figure 3. Equivalent Analog Output Circuit of AD7111

D3-D0 / D7-D4	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.0	0.375	0.75	1.125	1.5	1.875	2.25	2.625	3.0	3.375	3.75	4.125	4.5	4.875	5.25	5.625
0001	6.0	6.375	6.75	7.125	7.5	7.875	8.25	8.625	9.0	9.375	9.75	10.125	10.5	10.875	11.25	11.625
0010	12.0	12.375	12.75	13.125	13.5	13.875	14.25	14.625	15.0	15.375	15.75	16.125	16.5	16.875	17.25	17.625
0011	18.0	18.375	18.75	19.125	19.5	19.875	20.25	20.625	21.0	21.375	21.75	22.125	22.5	22.875	23.25	23.625
0100	24.0	24.375	24.75	25.125	25.5	25.875	26.25	26.625	27.0	27.375	27.75	28.125	28.5	28.875	29.75	29.625
0101	30.0	30.375	30.75	31.125	31.5	31.875	32.25	32.625	33.0	33.375	33.75	34.125	34.5	34.875	35.25	35.625
0110	36.0	36.375	36.75	37.125	37.5	37.875	38.25	38.625	39.0	39.375	39.75	40.125	40.5	40.875	41.25	41.625
0111	42.0	42.375	42.75	43.125	43.5	43.875	44.25	44.625	45.0	45.375	45.75	46.125	46.5	46.875	47.25	47.625
1000	48.0	48.375	48.75	49.125	49.5	49.875	50.25	50.625	51.0	51.375	51.75	52.125	52.5	52.875	53.25	53.625
1001	54.0	54.375	54.75	55.125	55.5	55.875	56.25	56.625	57.0	57.375	57.75	58.125	58.5	58.875	59.25	59.625
1010	60.0	60.375	60.75	61.125	61.5	61.875	62.25	62.625	63.0	63.375	63.75	64.125	64.5	64.875	65.25	65.625
1011	66.0	66.375	66.75	67.125	67.5	67.875	68.25	68.625	69.0	69.375	69.75	70.125	70.5	70.875	71.25	71.625
1100	72.0	72.375	72.75	73.125	73.5	73.875	74.25	74.625	75.0	75.375	75.75	76.125	76.5	76.875	77.25	77.625
1101	78.0	78.375	78.75	79.125	79.5	79.875	80.25	80.625	81.0	81.375	81.75	82.125	82.5	82.875	83.25	83.625
1110	84.0	84.375	84.75	85.125	85.5	85.875	86.25	86.625	87.0	87.375	87.75	88.125	88.5	88.875	89.25	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

Table I. Ideal Attenuation in dB vs. Input Code

DYNAMIC PERFORMANCE

The dynamic performance of the AD7111 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7111 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.

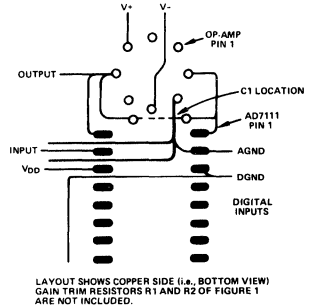


Figure 4. Suggested Layout for AD7111 and Op-Amp

It is recommended that when using the AD7111 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7111 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

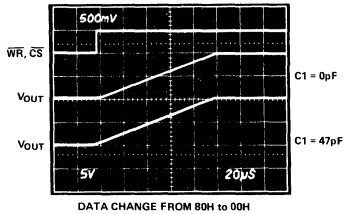


Figure 5. Response of AD7111 with AD517

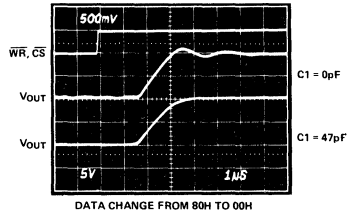


Figure 6. Response of AD7111 with AD544

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7111 has been designed to minimize these glitches as much as possible.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 12. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7111.

Feedthrough and absolute accuracy are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7111 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 11.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7111 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7111 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7111 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07) in dc applications. Amplifiers with higher offset voltage may cause audible "thumps" in ac applications due to dc output changes.

The AD7111 accuracy is specified and tested using only the internal feedback resistor. Any Gain Error (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7111 D/A converter circuit results in a constant attenuation error over the whole range. The AD7111 accuracy is specified relative to 0dB attenuation, hence "Gain" trim resistors—R1 and R2 in Figure 1—can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0dB attenuation) with input code 00000000. The accuracy and monotonic range specifications of the AD7111 are not affected in any way by this gain trim procedure. For the AD7111L/C/U grades, suitable values for R1 and R2 of Figure 1 are R1 = 500Ω, R2 = 180Ω; for the K/B/T grades suitable values are R1 = 1000Ω, R2 = 270Ω. For additional information on gain error the reader is referred to Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs" by Phil Burton available from Analog Devices Inc., Publication Number E630–10–6/81.

Typical Performance Characteristics

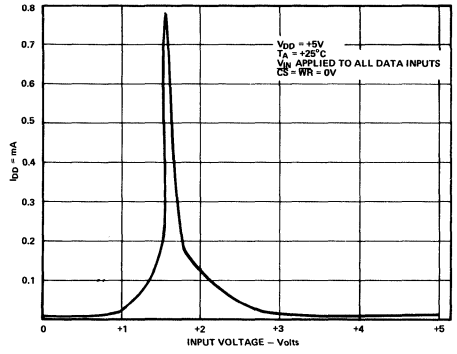


Figure 7. Typical Supply Current vs. Logic Input Level

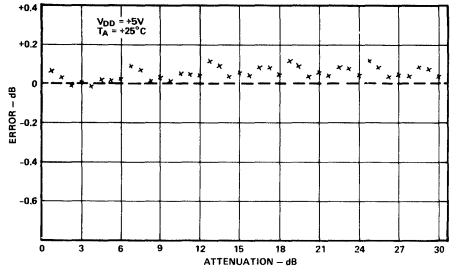


Figure 8. Typical Attenuation Error for 0.75dB Steps

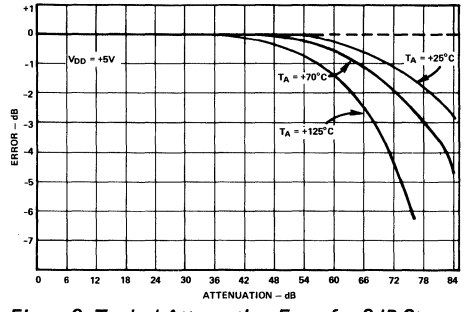


Figure 9. Typical Attenuation Error for 3dB Steps vs. Temperature

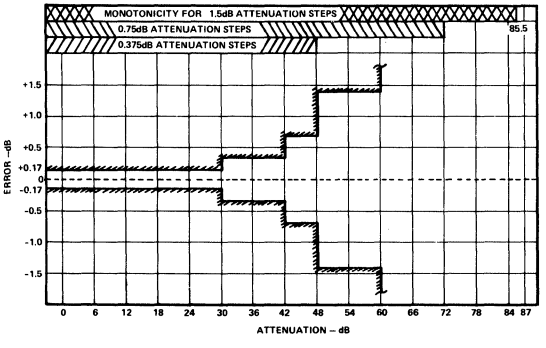


Figure 10. Accuracy Specification for K/B/T Grade Devices at T_A = +25°C

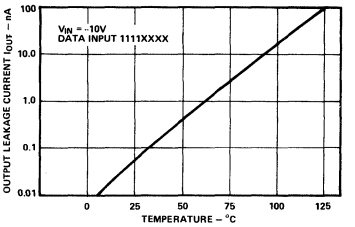


Figure 11. Output Leakage Current vs. Temperature

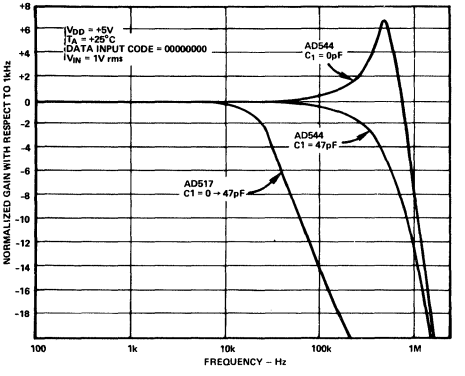


Figure 12. Frequency Response with AD544 and AD517 Amplifiers

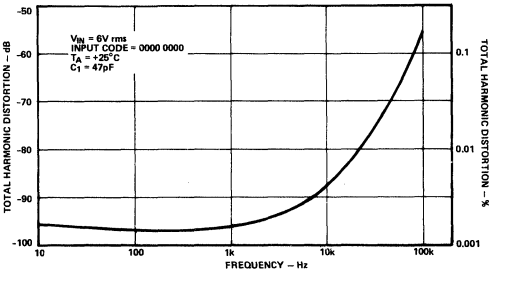


Figure 13. Distortion vs. Frequency Using AD544 Amplifier

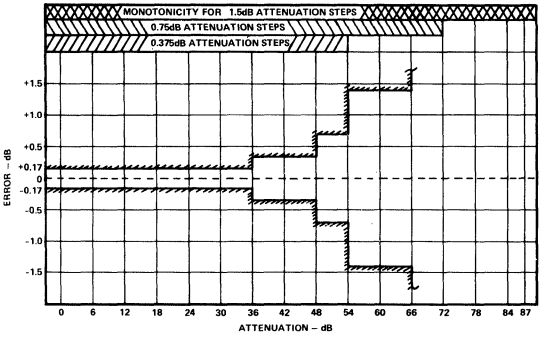


Figure 14. Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

ANALOG DEVICES

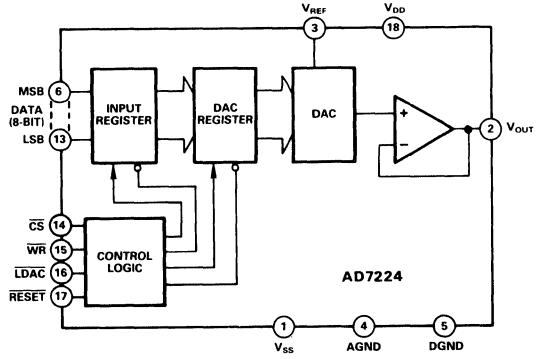
LC²MOS 8-Bit DAC with Output Amplifier

AD7224

FEATURES

8-Bit CMOS DAC with Output Amplifier
Operates with Single or Dual Supplies
Low Total Unadjusted Error:
Less than 1/2LSB Over Temperature
µP-Compatible with Double Buffered Input
Standard 18-Pin DIPs and 20-Terminal Surface Mount Packages

AD7224 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7224 is a precision 8-bit, voltage-output, digital-to-analog converter with output amplifier and double buffered interface logic on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The double buffered interface logic consists of two 8-bit registers–an input register and a DAC register. Only the data held in the DAC register determines the analog output of the converter. The double buffering allows simultaneous update in a system containing multiple AD7224's. Both registers may be made transparent under control of three external lines, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$. With both registers transparent, the $\overline{RESET}$ line functions like a zero override; a useful function for system calibration cycles. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. The output amplifier is capable of developing +10V across a 2kΩ load.

The AD7224 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC and Amplifier on CMOS Chip:
   The single-chip design of the 8-bit DAC and output amplifier is inherently more reliable than multi-chip designs. CMOS fabrication means low power consumption (35mW typical with single supply).
2. Low Total Unadjusted Error:
   The fabrication of the AD7224 on Analog Devices Linear Compatible CMOS (LC²MOS) process, coupled with a novel DAC switch-pair arrangement, enables an excellent total unadjusted error of less than 1LSB over the full operating temperature range.
3. Single or Dual Supply Operation:
   The voltage-mode configuration of the AD7224 allows operation from a single power supply rail. The part can also be operated with dual supplies giving enhanced performance for some parameters.
4. Versatile Interface Logic:
   The high speed logic allows direct interfacing to most microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7224 in multiple DAC systems. The part also features a zero override function.

ORDERING INFORMATION[1]

Total Unadjusted Error (LSB)	Temperature Range and Package Options[2,3]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-18)	**Hermetic DIP (Q-18)**	**Hermetic DIP (Q-18)**
±2	AD7224KN	AD7224BQ	AD7224TQ
±1	AD7224LN	AD7224CQ	AD7224UQ
	PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
±2	AD7224KP		AD7224TE
±1	AD7224LP		AD7224UE

NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Also available in SOIC package (AD7224KR-1).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4V to 16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} −4V)[1] unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	K, B, T Versions[2]	L, C, U Versions	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±1	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±3/2	±1	LSB max	
Full Scale Temperature Coefficient	±20	±20	ppm/°C max	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	±20	mV max	
Zero Code Error Temperature Coefficient	±50	±30	µV/°C typ	
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} −4)	2 to (V_{DD} −4)	V_{min} to V_{max}	
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1's.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]				
Positive Full Scale Change	5	5	µs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Negative Full Scale Change	7	7	µs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Digital Feedthrough	50	50	nV secs typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES				
V_{DD} Range	11.4/16.5	11.4/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	4.5/5.5	4.5/5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}				
@25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}				
@25°C	3	3	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	5	5	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]				
t_1				
@25°C	150	150	ns min	Chip Select/Load DAC Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_2				
@25°C	150	150	ns min	Write/Reset Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_3				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@25°C	90	90	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	100	100	ns min	
t_6				
@25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions; 0 to +70°C
B, C Versions; −25°C to +85°C
T, U Versions; −55°C to +125°C
[3]Sample Tested at 25°C by Product Assurance to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	K, B, T Versions[2]	L, C, U Versions	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT				
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1's.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2	2	V/μs min	
Voltage Output Settling Time[3]				
Positive Full Scale Change	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	20	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough[3]	50	50	nV secs typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	14.25/15.75	V_{min}/V_{max}	For Specified Performance
I_{DD}				
@25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V, +17V
V_{DD} to DGND . . . . . −0.3V, +17V
V_{DD} to V_{SS} . . . . . −0.3V, +24V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
V_{REF} to AGND . . . . . −0.3V, V_{DD}
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature
Commerical (K, L Versions) . . . . . 0 to +70°C
Industrial (B, C Versions) . . . . . −25°C to +85°C
Extended (T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTES
[1]The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$\overline{RESET}$	LDAC	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H	↓	L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L	↓	H	DAC Register Latched
L	X	X	X	Both Registers Loaded With All Zeros
↓	H	H	H	Both Register Latched With All Zeros and Output Remains at Zero
↓	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care.
All control inputs are level triggered.

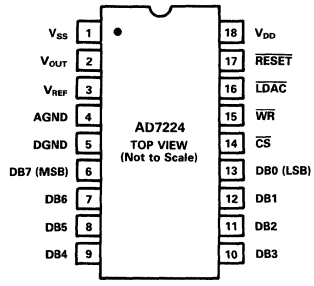
Table I. AD7224 Truth Table

CAUTION

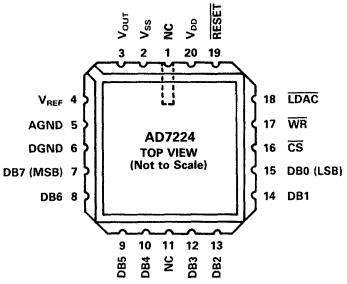
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP

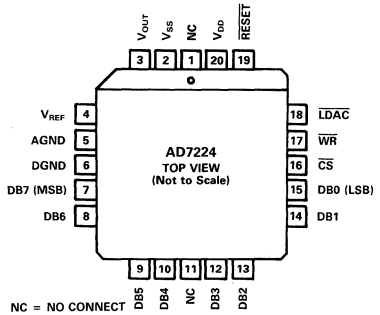


LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

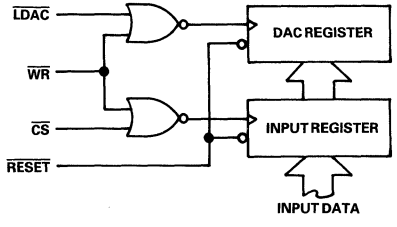
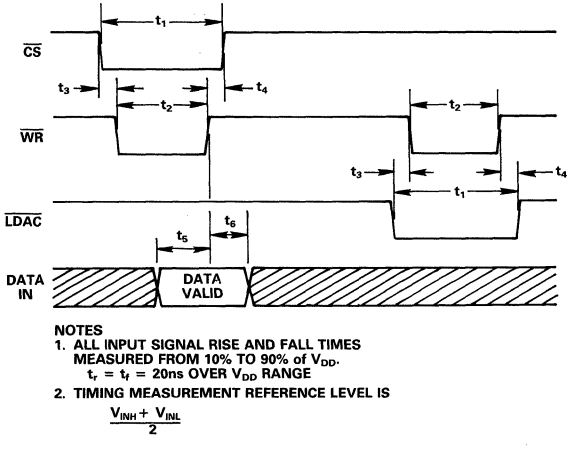


Figure 1. Input Control Logic



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% of V_{DD}.
   $t_r = t_f$ = 20ns OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS
   $\frac{V_{INH} + V_{INL}}{2}$

Figure 2. Write Cycle Timing Diagram

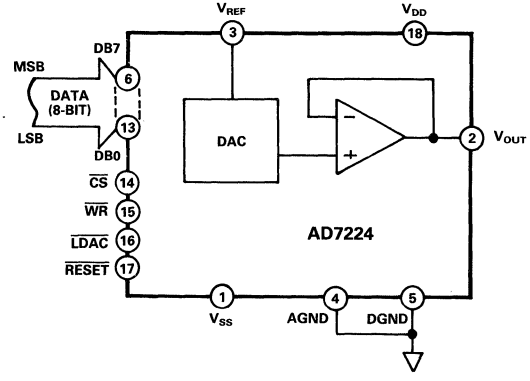


Figure 3. Unipolar Output Circuit

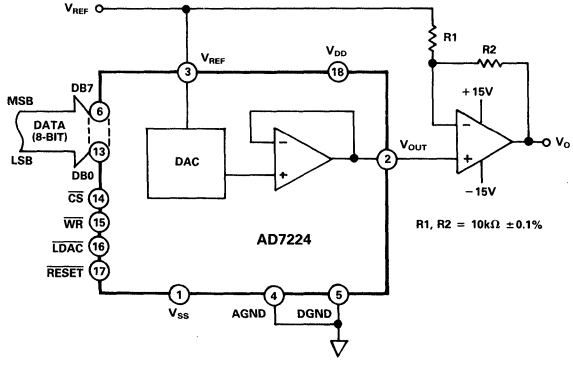


Figure 4. Bipolar Output Circuit

ANALOG DEVICES

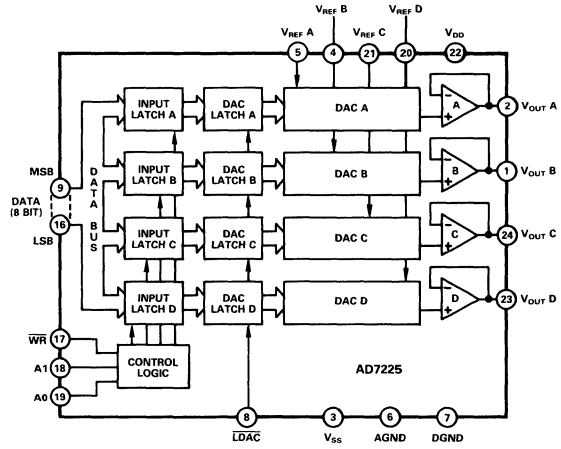
LC²MOS Quad 8-Bit DAC with Separate Reference Inputs

AD7225

FEATURES

Four 8-Bit DACs with Output Amplifiers
Separate Reference Input for Each DAC
µP Compatible with Double-Buffered Inputs
Simultaneous Update of All Four Outputs
Operates with Single or Dual Supplies
No User Trims Required
Skinny 24-Pin DIPs and 28-Terminal Surface Mount Packages

AD7225 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7225 contains four 8-bit voltage output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. Each D/A converter has a separate reference input terminal. No external trims are required to achieve full specified performance for the part.

The double-buffered interface logic consists of two 8-bit registers per channel–an input register and a DAC register. Control inputs A0 and A1 determine which input register is loaded when $\overline{WR}$ goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double-buffering allows simultaneous update of all four outputs under control of $\overline{LDAC}$. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7225 is fabricated on an all ion-implanted high-speed Linear Compatible CMOS (LC² MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuitry on the same chip.

PRODUCT HIGHLIGHTS

1. DACs and Amplifiers on CMOS Chip:
   The single-chip design of four 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one end of the package and all digital inputs at the other.
2. Single or Dual Supply Operation:
   The voltage-mode configuration of the AD7225 allows single supply operation. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Versatile Interface Logic:
   The AD7225 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. The double-buffered interface allows simultaneous update of the four outputs.
4. Separate Reference Input for Each DAC:
   The AD7225 offers great flexibility in dealing with input signals with a separate reference input provided for each DAC and each reference having variable input voltage capability.

ORDERING INFORMATION[1]

Total Unadjusted Error (LSB)	Temperature Range and Package Options[2]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-24)	**Hermetic DIP (Q-24)**	**Hermetic DIP (Q-24)**
±2	AD7225KN	AD7225BQ	AD7225TQ
±1	AD7225LN	AD7225CQ	AD7225UQ
	PLCC[3] (P-28A)		**LCCC[4] (E-28A)**
±2	AD7225KP		AD7225TE
±1	AD7225LP		AD7225UE

NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4V to 16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} −4V)[1] unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±1	±1/2	±1	±1/2	LSB max	
Full Scale Temp. Coeff.	±5	±5	±5	±5	ppm/°C typ	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error @ 25°C	±25	±15	±25	±15	mV max	
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Zero Code Error Temp Coeff.	±30	±30	±30	±30	µV/°C typ	
REFERENCE INPUT						
Voltage Range	2 to (V_{DD} −4)	2 to (V_{DD} −4)	2 to (V_{DD} −4)	2 to (V_{DD} −4)	V_{min} to V_{max}	
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[3]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1's.
Channel-to-Channel Isolation[3]	60	60	60	60	dB min	V_{REF} = 10V p-p Sine Wave @ 10kHz
AC Feedthrough[3]	−70	−70	−70	−70	dB max	V_{REF} = 10V p-p Sine Wave @ 10kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[3]	2.5	2.5	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]						
Positive Full Scale Change	5	5	5	5	µs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Negative Full Scale Change	5	5	5	5	µs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Digital Feedthrough[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Digital Crosstalk[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES						
V_{DD} Range	11.4/16.5	11.4/16.5	11.4/16.5	11.4/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	9	9	10	10	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions; 0 to +70°C
B, C Versions; −25°C to +85°C
T, U Versions; −55°C to +125°C
[3]Sample Tested at 25°C to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

SINGLE SUPPLY (V_{DD} = +15V ±5%, V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT						
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[3]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1's.
Channel-to-Channel Isolation	60	60	60	60	dB min	V_{REF} = 10V p-p Sine Wave @ 10kHz
AC Feedthrough[3,4]	−70	−70	−70	−70	dB max	V_{REF} = 10V p-p Sine Wave @ 10kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[3]	2	2	2	2	V/μs min	
Voltage Output Settling Time[3]						
Positive Full Scale Change	5	5	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	7	7	7	7	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough[3,4]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Digital Crosstalk[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES						
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V_{min}/V_{max}	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}

ABSOLUTE MAXIMUM RATINGS*

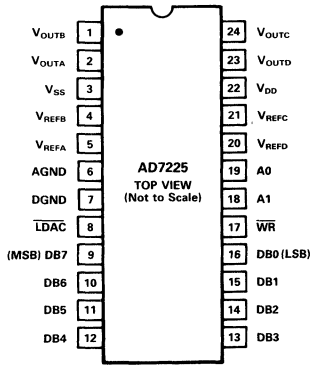
V_{DD} to AGND . . . . . −0.3V, +17V
V_{DD} to DGND . . . . . −0.3V, +17V
V_{DD} to V_{SS} . . . . . −0.3V, +24V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD}
V_{REF} to AGND . . . . . −0.3V, V_{DD}
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C 500mW
Derates above 75°C by 2.0mW/C
Operating Temperature
Commercial (K, L Versions) . . . . . 0 to +70°C
Industrial (B, C Versions) . . . . . −25°C to +85°C
Extended (T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTES
[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to AGND or V_{SS} is 50mA.

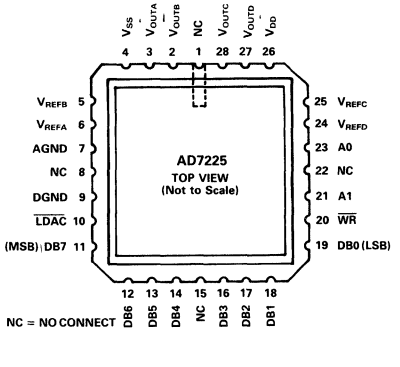
*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

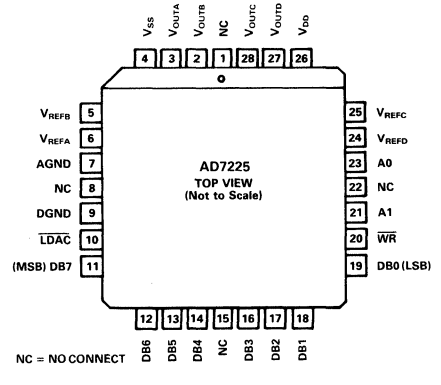
DIP



LCCC



PLCC



CIRCUIT INFORMATION

D/A SECTION

The AD7225 contains four, identical, 8-bit voltage-mode digital-to-analog converters. Each D/A converter has a separate reference input. The output voltages from the converters have the same polarity as the reference voltages, allowing single supply operation. A novel DAC switch pair arrangement on the AD7225 allows a reference voltage range from +2V to +12.5V on each reference input.

Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high-speed NMOS, single-pole, double-throw switches. The simplified circuit diagram for channel A is shown in Figure 1. Note that AGND is common to all four DACs.

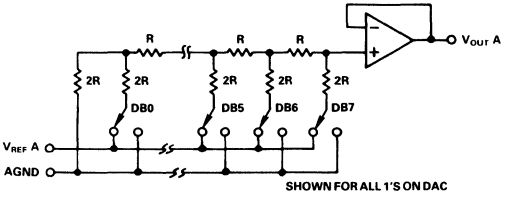


Figure 1. D/A Simplified Circuit Diagram

The input impedance at any of the reference inputs is code dependent and can vary from 11kΩ minimum to infinity. The lowest input impedance at any reference input occurs when that DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminals is also code dependent and typically varies from 15pF to 35pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUTX} = D_X \cdot V_{REFX}$$

where D_X is fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier.

OP-AMP SECTION

Each voltage mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is capable of developing +10V across a 2kΩ load and can drive capacitive loads of 3300pF.

The AD7225 can be operated single or dual supply; operating with dual supplies results in enhanced performance in some parameters which cannot be achieved with single supply operation. In single supply operation (V_{SS} = 0V = AGND) the sink capability of the amplifier, which is normally 400μA, is reduced as the output voltage nears AGND. The full sink capability of 400μA is maintained over the full output voltage range by tying V_{SS} to −5V. This is indicated in Figure 2.

Settling-time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling-time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS}.

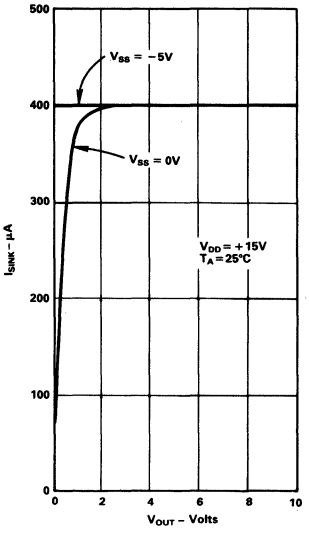


Figure 2. Variation of I_{SINK} with V_{OUT}

Additionally, the negative V_{SS} gives more headroom to the output amplifiers which results in better zero code performance and improved slew-rate at the output, than can be obtained in the single supply mode.

DIGITAL SECTION

The AD7225 digital inputs are compatible with either TTL or 5V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode between DGND and each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

The AD7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register will accept data from the input port. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{WR}$. Table I shows the addressing for the input registers on the AD7225.

Only the data held in the DAC register determines the analog output of the converter. The $\overline{LDAC}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ signal is level triggered and therefore the DAC

A1	A0	Selected Input Register
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Table I. AD7225 Addressing

registers may be made transparent by tying $\overline{LDAC}$ LOW (in this case the outputs of the converters will respond to the data held in their respective input latches). $\overline{LDAC}$ is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ is activated prior to the rising edge of $\overline{WR}$ (or $\overline{WR}$ occurs during $\overline{LDAC}$), then $\overline{LDAC}$ must stay LOW for t_6 or longer after $\overline{WR}$ goes HIGH to ensure correct data is latched through to the output. Table II shows the truth table for AD7225 operation. Figure 3 shows the input control logic for the part and the write cycle timing diagram is given in Figure 4.

$\overline{WR}$	$\overline{LDAC}$	Function
H	H	No Operation. Device not selected
L	H	Input Register of Selected DAC Transparent
↓	H	Input Register of Selected DAC Latched
H	L	All Four DAC Registers Transparent (i.e. Outputs respond to data held in respective input registers)
		Input Registers are Latched
H	↓	All Four DAC Registers Latched
L	L	DAC Registers and Selected Input Register Transparent
		Output follows Input Data for Selected Channel.

Table II. AD7225 Truth Table

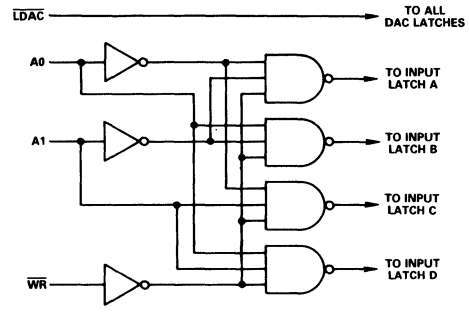


Figure 3. Input Control Logic

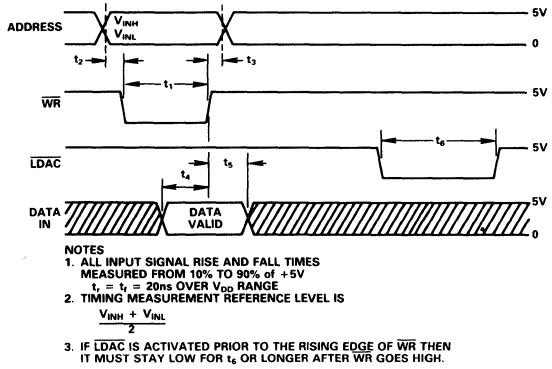


Figure 4. Write Cycle Timing Diagram

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for each channel of the AD7225, with the output voltage having the same positive polarity as V_{REF}. The AD7225 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 5. The voltage at any of the reference inputs must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table III.

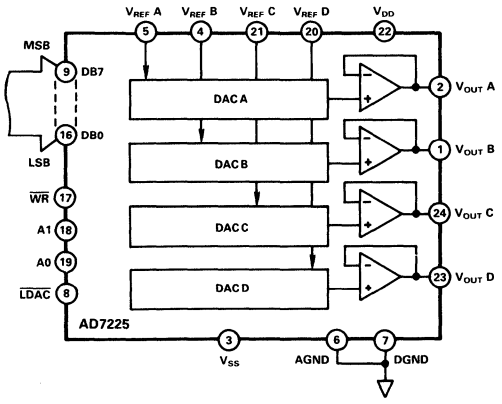


Figure 5. Unipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table III. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

Each of the DACs of the AD7225 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 6 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the AD7225. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_A V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_A - 1) \cdot V_{REF}$$

where D_A is a fractional representation of the digital word in latch A. ($0 \leq D_A \leq 255/256$)

Mismatch between R1 and R2 causes gain and offset errors and, therefore, these resistors must match and track over temperature. Once again the AD7225 can be operated in single supply or from positive/negative supplies. Table IV shows the digital code versus output voltage relationship for the circuit of Figure 6 with R1 = R2.

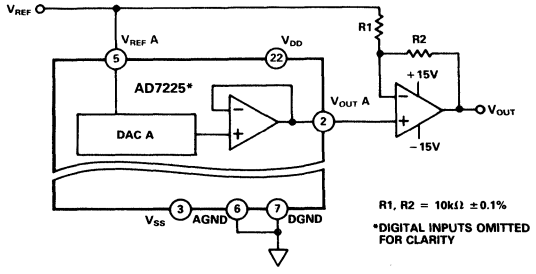


Figure 6. AD7225 Bipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table IV. Bipolar (Offset Binary) Code Table

AC REFERENCE SIGNAL

In some applications it may be desirable to have ac reference signals. The AD7225 has multiplying capability within the upper (V_{DD} – 4V) and lower (2V) limits of reference voltage when operated with dual supplies. Therefore ac signals need to be ac coupled and biased up before being applied to the reference inputs. Figure 7 shows a sine wave signal applied to V_{REF} A. For input signal frequencies up to 50kHz the output distortion typically remains less than 0.1%. The typical 3dB bandwidth figure for small signal inputs is 800kHz.

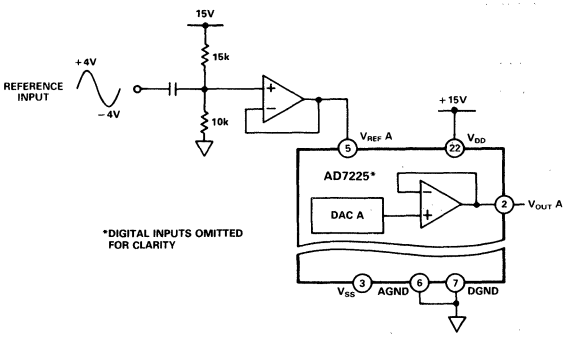


Figure 7. Applying an AC Signal to the AD7225

GROUND MANAGEMENT AND LAYOUT

Since the AD7225 contains four reference inputs which can be driven from ac sources (see AC REFERENCE SIGNAL section) careful layout and grounding is important to minimize analog crosstalk between the four channels. The dynamic performance of the four DACs depends upon the optimum choice of board layout. Figure 8 shows the relationship between input frequency and channel-to-channel isolation. Figure 9 shows a printed circuit board layout which is aimed at minimizing crosstalk and feed-through. The four input signals are screened by AGND. V_{REF} was limited to between 2V and 3.24V to avoid slew rate limiting effects from the output amplifier during measurements.

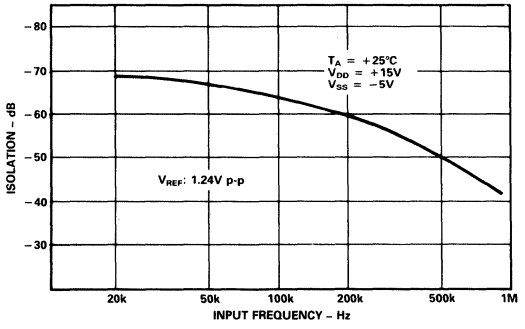


Figure 8. Channel-to-Channel Isolation

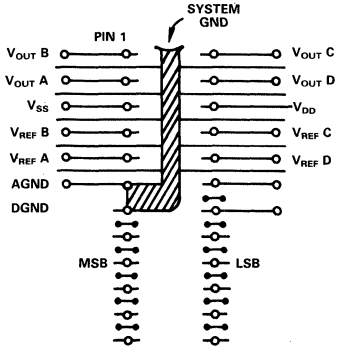


Figure 9. Suggested PCB Layout for AD7225. Layout Shows Component Side (Top View)

ANALOG DEVICES

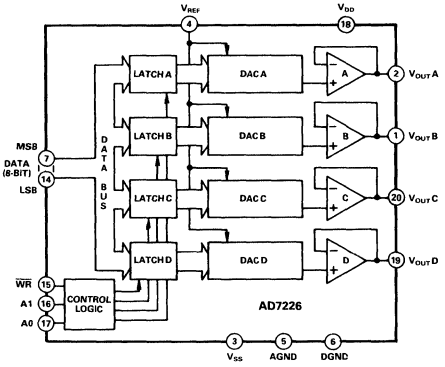
LC²MOS Quad 8-Bit D/A Converter

AD7226

FEATURES
- Four 8-Bit DACs with Output Amplifiers
- Skinny 20-Pin DIPs and 20-Terminal Surface Mount Packages
- Microprocessor Compatible
- TTL/CMOS Compatible
- No User Trims
- Single Supply Operation Possible

APPLICATIONS
- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters e.g., Gain/Offset

AD7226 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7226 contains four 8-bit voltage-output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the four D/A converters. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Control inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. The control logic is speed-compatible with most 8-bit microprocessors.

Each D/A converter includes an output buffer amplifier capable of driving up to 5mA of output current. The amplifiers' offsets are laser-trimmed during manufacture, thereby eliminating any requirement for offset nulling.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V with dual supplies. The part is also specified for single supply operation at a reference of +10V.

The AD7226 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC-to-DAC Matching:
   Since all four DACs are fabricated on the same chip at the same time, precise matching and tracking between the DACs is inherent.
2. Single Supply Operation:
   The voltage mode configuration of the DACs allows the AD7226 to be operated from a single power supply rail.
3. Microprocessor Compatibility:
   The AD7226 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered.
4. Small Size:
   Combining four DACs and four op-amps plus interface logic into either a small, 0.3" wide, 20-pin DIP or a 20-terminal surface mount package allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all the analog inputs and outputs at one end of the package and all the digital inputs at the other.

ORDERING INFORMATION[1]

Total Unadjusted Error (LSB)	Temperature Range and Package Options[2,3]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-20)	**Hermetic DIP (Q-20)**	**Hermetic DIP (Q-20)**
±2	AD7226KN	AD7226BQ	AD7226TQ
	PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
±2	AD7226KP		AD7226TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-87802.
[2]See Section 14 for package outline information.
[3]Also available in SOIC package (AD7226KR).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4V to 16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = 2V to (V_{DD} −4V)[1] unless otherwise stated). All specifications T_{MIN} to T_{MAX} unless otherwise noted.

Parameter	K, B, T Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error	±2	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±1 1/2	LSB max	
Full Scale Temperature Coefficient	±20	ppm/°C typ	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	mV max	
Zero Code Error Temperature Coefficient	±50	µV/°C typ	
REFERENCE INPUT			
Voltage Range	2 to (V_{DD} −4)	V_{MIN} to V_{MAX}	
Input Resistance	2	kΩ min	
Input Capacitance[3]	65	pF min	Occurs when each DAC loaded with all 0's.
	300	pF max	Occurs when each DAC loaded with all 1's.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[4]	2.5	V/µs min	
Voltage Output Settling Time[4]			
Positive Full Scale Change	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	7	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Crosstalk	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES			
V_{DD} Range	11.4/16.5	V_{MIN}/V_{MAX}	For Specified Performance
I_{DD}	13	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}.
I_{SS}	11	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}.
SWITCHING CHARACTERISTICS[4,5]			
Address to Write Setup Time, t_{AS}			
@25°C	0	ns min	
T_{MIN} to T_{MAX}	0	ns min	
Address to Write Hold Time, t_{AH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Data Valid to Write Setup Time, t_{DS}			
@25°C	90	ns min	
T_{MIN} to T_{MAX}	100	ns min	
Data Valid to Write Hold Time, t_{DH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Write Pulse Width, t_{WR}			
@25°C	150	ns min	
T_{MIN} to T_{MAX}	200	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K Version; 0 to +70°C
B Version; −25°C to +85°C
T Version; −55°C to +125°C
[3]Guaranteed by design. Not production tested.
[4]Sample Tested at 25°C to ensure compliance.
[5]Switching Characteristics apply for both single and dual supply operation.
Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated). All specifications T_{MIN} to T_{MAX} unless otherwise noted.

Parameter	K, B, T Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error	±2	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT			
Input Resistance	2	kΩ min	
Input Capacitance[3]	65	pF min	Occurs when each DAC loaded with all 0's.
	300	pF max	Occurs when each DAC loaded with all 1's.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[4]	2	V/μs min	
Voltage Output Settling Time[4]			
Positive Full Scale Change	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	μs max	Settling Time to ± 1/2LSB
Digital Crosstalk	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES			
V_{DD} Range	14.25 to 15.75	V_{MIN}/V_{MAX}	For Specified Performance
I_{DD}	13	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}

ABSOLUTE MAXIMUM RATINGS*

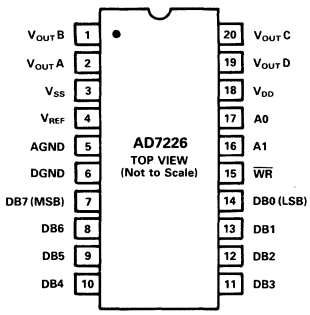
V_{DD} to AGND . . . . . −0.3V, +17V
V_{DD} to DGND . . . . . −0.3V, +17V
V_{SS} to AGND . . . . . −7V, V_{DD}
V_{SS} to DGND . . . . . −7V, V_{DD}
V_{DD} to V_{SS} . . . . . −0.3V, +24V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD}+0.3V
V_{REF} to AGND . . . . . −0.3V, V_{DD}
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C 500mW
Derates above 75°C by . . . . . 2.0mW/°C
Operating Temperature
Commerical (K Version) . . . . . 0 to +70°C
Industrial (B Version) . . . . . −25°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTES
[1]Outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60mA.

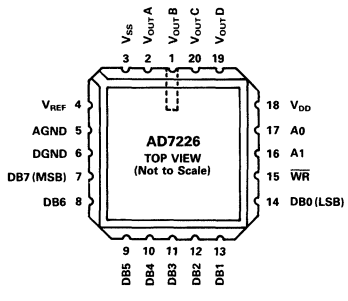
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

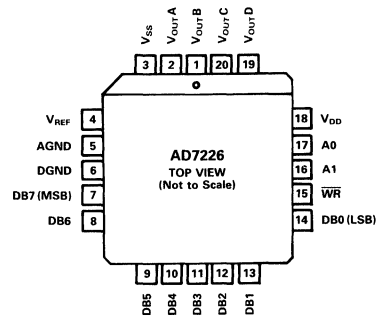
DIP



LCCC



PLCC



INTERFACE LOGIC INFORMATION

Address lines A0 and A1 select which DAC will accept data from the input port. Table I shows the selection table for the four DACs with Figure 1 showing the input control logic. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high the analog outputs remain at the value corresponding to the data held in their respective latches.

AD7226 Control Inputs			AD7226
$\overline{WR}$	A1	A0	Operation
H	X	X	No Operation Device Not Selected
L	L	L	DAC A Transparent
↑	L	L	DAC A Latched
L	L	H	DAC B Transparent
↑	L	H	DAC B Latched
L	H	L	DAC C Transparent
↑	H	L	DAC C Latched
L	H	H	DAC D Transparent
↑	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

Table I. AD7226 Truth Table

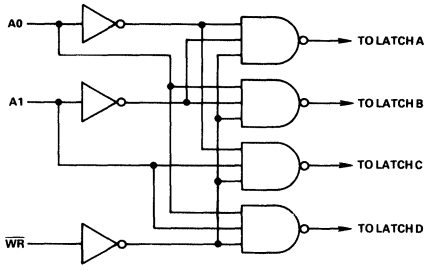


Figure 1. Input Control Logic

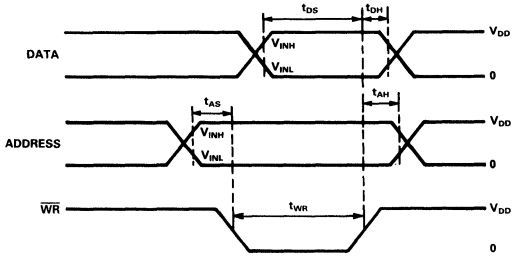


Figure 2. Write Cycle Timing Diagram

Unipolar Output Operation

This is the basic mode of operation for each channel of the AD7226, with the output voltages having the same positive polarity as $+V_{REF}$. The AD7226 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Note that the voltage at V_{REF} must never be negative with respect to DGND in order to prevent parasitic transistor turn-on. Connections for the unipolar output operation are shown in Figure 3.

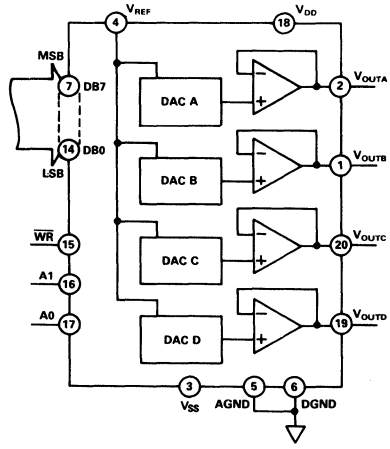


Figure 3. Unipolar Output Circuit

Bipolar Output Operation

Each of the DACs of the AD7226 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 4 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the AD7226. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_A V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_A - 1) \cdot V_{REF}$$

where D_A is a fractional representation of the digital word in latch A.

Mismatch between R1 and R2 causes gain and offset errors and therefore these resistors must match and track over temperature. Once again the AD7226 can be operated in single supply or from positive/negative supplies.

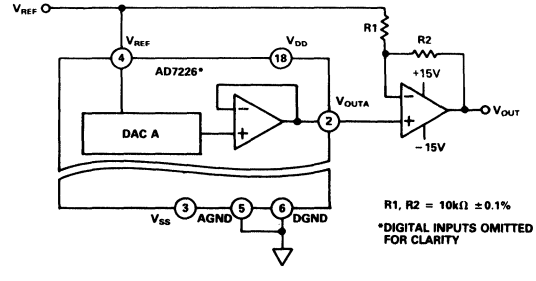


Figure 4. AD7226 Bipolar Output Circuit

GROUND MANAGEMENT

AC or transient voltages between AGND and DGND can cause noise at the analog output. This is especially true in microprocessor systems where digital noise is prevalent. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7226. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7226 AGND and DGND pins (IN914 or equivalent).

3-PHASE SINE WAVE

The circuit of Figure 5 shows an application of the AD7226 in the generation of 3-phase sine waves which can be used to control small 3-phase motors. The proper codes for synthesising a full sine wave are stored in EPROM, with the required phase-shift of 120° between the three D/A converter outputs being generated in software.

Data is loaded into the three D/A converters from the sine EPROM via the microprocessor or control logic. Three loops are generated in software with each D/A converter being loaded from a separate loop. The loops run through the look-up table producing successive triads of sinusoidal values with 120° separation which are loaded to the D/A converters producing 3 sine wave voltages 120° apart. A complete sine wave cycle is generated by stepping through the full look-up table. If a 256-element sine wave table is used then the resolution of the circuit will be 1.4° (360°/256). Figure 7 shows typical resulting waveforms. The sine waves can be smoothed by filtering the D/A converter outputs.

The fourth D/A converter of the AD7226, DAC D, may be used in a feedback configuration to provide a programmable reference voltage for itself and the other three converters. This configuration is shown in Figure 5. The relationship of V_{REF} to V_{IN} is dependent upon digital code and upon the ratio of R_F to R and is given by the formula

$$V_{REF} = \frac{(1 + G)}{(1 + G.D_D)} \cdot V_{IN}$$

where $G = R_F/R$

and D_D is a fractional representation of the digital word in latch D.

Alternatively, for a given V_{IN} and resistance ratio, the required value of D_D for a given value of V_{REF} can be determined from the expression

$$D_D = (1 + R/R_F) \cdot \frac{V_{IN}}{V_{REF}} - \frac{R}{R_F}$$

Figure 6 shows typical plots of V_{REF} versus digital code for three different values of R_F. With $V_{IN} = +2.5V$ and $R_F = 3R$ the peak-to-peak sine wave voltage from the converter outputs will vary between +2.5V and +10V over the digital input code range of 0 to 255.

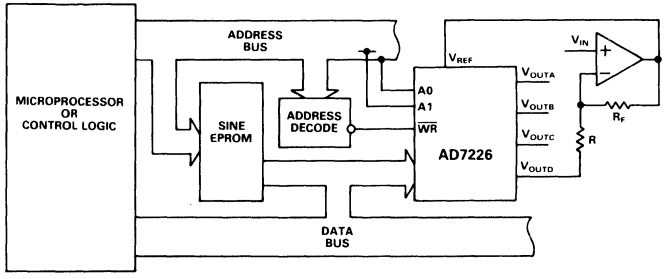


Figure 5. 3-Phase Sine Wave Generation Circuit

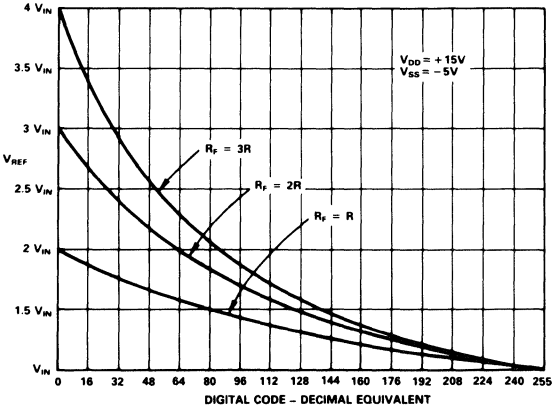


Figure 6. Variation of V_{REF} with Feedback Configuration

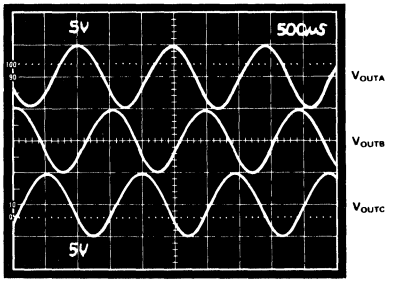


Figure 7. 3-Phase Sine Wave Output

STAIRCASE WINDOW COMPARATOR

In many test systems, it is important to be able to determine whether some parameter lies within defined limits. The staircase window comparator of Figure 8a is a circuit which can be used, for example, to measure the V_{OH} and V_{OL} thresholds of a TTL device under test. Upper and lower limits on both V_{OH} and V_{OL} can be programmably set using the AD7226. Each adjacent pair of comparators forms a window of programmable size. If V_{TEST} lies within a window then the output for that window will be high. With a reference of 2.56V applied to the V_{REF} input, the minimum window size is 10mV.

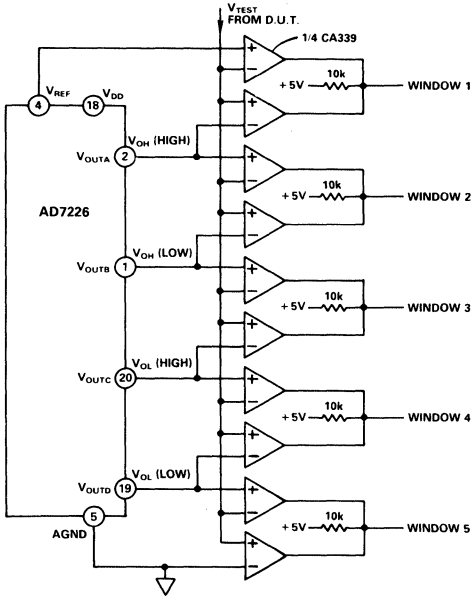


Figure 8a. Logic Level Measurement

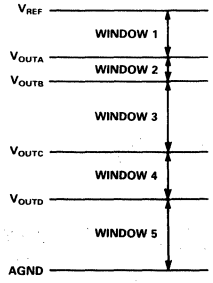


Figure 8b. Window Structure

The circuit can easily be adapted to allow for overlapping of windows as shown in Figure 9a. If the three outputs from this circuit are decoded then five different nonoverlapping programmable windows can again be defined.

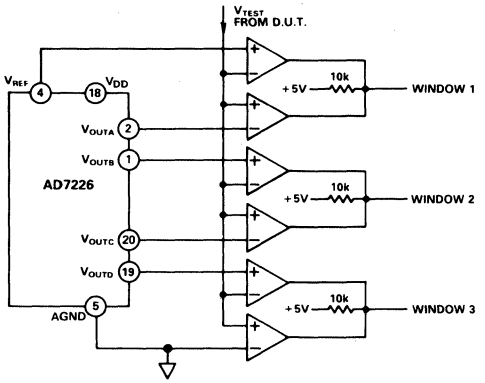


Figure 9a. Overlapping Windows

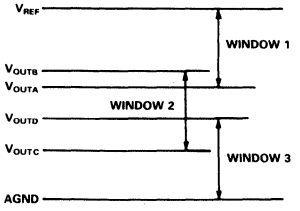


Figure 9b. Window Structure

OFFSET ADJUST

Figure 10 shows how the AD7226 can be used to provide programmable input offset voltage adjustment for the AD544 op amp. Each output of the AD7226 can be used to trim the input offset voltage on one AD544. The 620kΩ resistor tied to +10V provides a fixed bias current to one offset node. For symmetrical adjustment, this bias current should equal the current in the other offset node with the half-full scale code (i.e. 10000000) on the DAC. Changing the code on the DAC varies the bias current and hence provides offset adjust for the AD544. For example, the input offset voltage on the AD544J, which has a maximum of ±2mV, can be programmably trimmed to ±10μV.

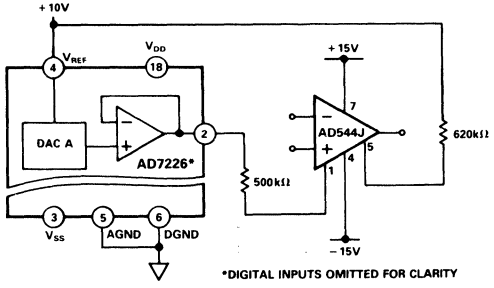


Figure 10. Offset Adjust for AD544

ANALOG DEVICES

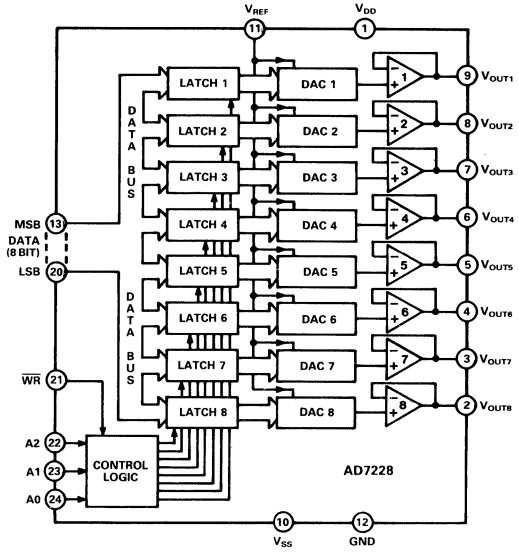
LC²MOS Octal 8-Bit DAC

AD7228

FEATURES

Eight 8-Bit DACs with Output Amplifiers
Operates with Single or Dual Supplies
µP Compatible (95ns $\overline{WR}$ pulse)
No User Trims Required
Skinny 20-Pin DIPs and 20-Terminal Surface Mount Packages

AD7228 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7228 contains eight 8-bit voltage-mode digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the eight D/A converters. Data is transferred into the data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Address inputs A0, A1 and A2 determine which latch is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 to +10V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7228 is fabricated on an all ion-implanted, high-speed, Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuits on the same chip.

PRODUCT HIGHLIGHTS

1. Eight DACs and Amplifiers in Small Package:
   The single-chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.
2. Single or Dual Supply Operation:
   The voltage-mode configuration of the DACs allows single supply operation of the AD7228. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Microprocessor Compatibility:
   The AD7228 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high-performance 8-bit microprocessors.

SPECIFICATIONS

DUAL SUPPLY (V_{DD} = 10.8V to 16.5V; V_{SS} = −5V ±10%; GND = 0V; V_{REF} = +2V to +10V[1]; R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	K, B Versions[2]	L, C Versions	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	V_{DD} = +15V ± 10%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error[4]	±1	±1/2	±1	±1/2	LSB max	Typical tempco is 5ppm/°C with V_{REF} = +10V
Zero Code Error						
@ 25°C	±25	±15	±25	±15	mV max	Typical tempco is 30μV/°C
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
REFERENCE INPUT						
Voltage Range[1]	2 to 10	2 to 10	2 to 10	2 to 10	V_{min} to V_{max}	
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
AC Feedthrough	−70	−70	−70	−70	dB typ	V_{REF} = 8V p-p Sine Wave @ 10kHz/
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[5]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/μs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full-Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. V_{REF} = +10V; $\overline{WR}$ = 0V
POWER SUPPLIES						
V_{DD} Range	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	
I_{SS}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°	14	14	14	14	mA max	
T_{min} to T_{max}	18	18	20	20	mA max	

SINGLE SUPPLY[7] (V_{DD} = +15V ±10%, V_{SS} = GND = 0V; V_{REF} = +10V; R_L = 2kΩ, C_L = 100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
REFERENCE INPUT						
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
DIGITAL INPUTS	As per Dual Supply Specifications					
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/μs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full-Scale Change	7	7	7	7	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. V_{REF} = +10V; $\overline{WR}$ = 0V.
POWER SUPPLIES						
V_{DD} Range	13.5/16.5	13.5/16.5	13.5/16.5	13.5/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	

NOTES
[1]V_{OUT} must be less than V_{DD} by 3.5V to ensure correct operation.
[2]Temperature ranges are as follows:
K, L Versions; 0 to +70°C
B, C Versions; −25°C to +85°C
T, U Versions; −55°C to +125°C
[3]Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
[4]Calculated after zero code error has been adjusted out.
[5]Sample tested at 25°C to ensure compliance.
[6]The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.
[7]Single +5V operation is also possible with degraded performance (see Figure 14).

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1,2] (See Figures 1, 2; V_{DD} = +10.8V to +16.5V; V_{SS} = 0V or −5V ±10%)

Parameters	Limit at 25°C All Grades	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_3	70	90	100	ns min	Data Valid to $\overline{WR}$ Setup Time
t_4	10	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_5	95	120	150	ns min	Write Pulse Width

NOTES
[1]Sample tested at 25°C to ensure compliance. All input rise and fall times measured from 10% to 90% of +5V, $t_R = t_F = 5$ns.
[2]Timing measurement reference level is $\frac{V_{INH} + V_{INL}}{2}$

INTERFACE LOGIC INFORMATION

Address lines A0, A1 and A2 select which DAC accepts data from the input port. Table I shows the selection table for the eight DACs with Figure 1 showing the input control logic. When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent, and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

AD7228 Control Inputs				AD7228
$\overline{WR}$	A2	A1	A0	Operation
H	X	X	X	No Operation Device Not Selected
L	L	L	L	DAC 1 Transparent
↑	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

H = High State L = Low State X = Don't Care

Table I. AD7228 Truth Table

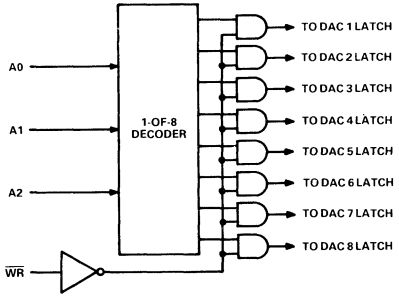
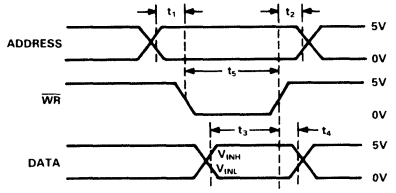


Figure 1. Input Control Logic



NOTE:
THE SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW. THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS

Figure 2. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND	−0.3V, +17V
V_{DD} to V_{SS}	−0.3V, +24V
Digital Input Voltage to GND	−0.3V, V_{DD} +0.3V
V_{REF} to GND	−0.3V, V_{DD} +0.3V
V_{OUT} to GND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	1000mW
Derates above 75°C by	2.0mW/C
Operating Temperature	
Commercial	0 to +70°C
Industrial	−25°C to +85°C
Extended	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTE
[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to GND or V_{SS} is 50mA.

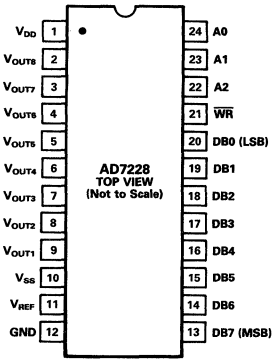
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

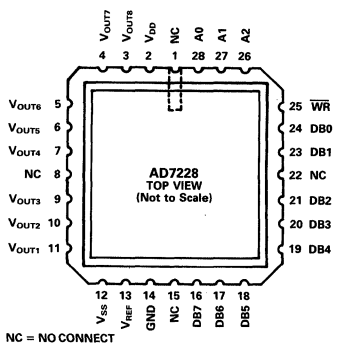
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

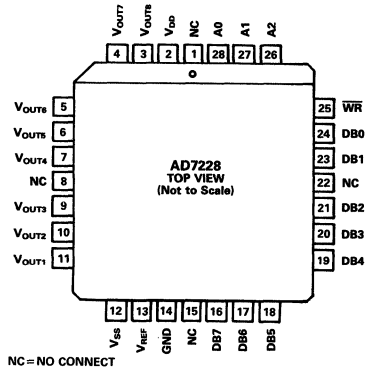
DIP



LCCC



PLCC



ORDERING INFORMATION[1]

Total Unadjusted Error (LSB)	Temperature Range and Package Options[2]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-24)	**Hermetic (Q-24)**	**Hermetic (Q-24)**
±2	AD7228KN	AD7228BQ	AD7228TQ
±1	AD7228LN	AD7228CQ	AD7228UQ
	PLCC[3] (P-28A)		**LCCC[4] (E-28A)**
±2	AD7228KP		AD7228TE
±1	AD7228LP		AD7228UE

NOTE
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-88663.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

CIRCUIT INFORMATION

D/A SECTION

The AD7228 contains eight identical, 8-bit, voltage-mode digital-to-analog converters. The output voltages from the converters have the same polarity as the reference voltage, allowing single supply operation. A novel DAC switch pair arrangement on the AD7228 allows a reference voltage range from +2V to +10V. Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high-speed NMOS switches. The simplified circuit diagram for one channel is shown in Figure 3. Note that V_{REF} (Pin 11) and GND (Pin 12) are common to all eight DACs.

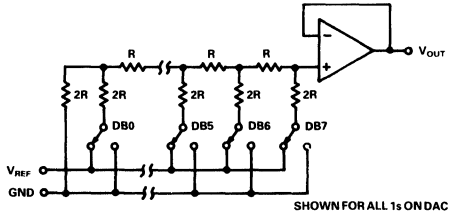


Figure 3. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin of the AD7228 is the parallel combination of the eight individual DAC reference input impedances. It is code dependent and can vary from 2kΩ to infinity. The lowest input impedance occurs when all eight DACs are loaded with digital code 01010101. Therefore, it is important that the external reference source presents a low output impedance to the V_{REF} terminal of the AD7228 under changing load conditions. Due to transient currents at the reference input during digital code changes a 0.1μF (or greater) decoupling capacitor is recommended on the V_{REF} input for dc applications. The nodal capacitance at the reference terminal is also code dependent and typically varies from 120pF to 350pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage:

$$V_{OUTN} = D_N \cdot V_{REF}$$

where D_N is a fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier as described in the following section.

OP AMP SECTION

Each voltage-mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is tested with a 2kΩ and 100pF load but will typically drive a 2kΩ and 500pF load.

The AD7228 can be operated single or dual supply. Operating the part from single or dual supplies has no effect on the positive-going settling time. However, the negative-going settling time to voltages near 0V in single supply will be slightly longer than the settling time for dual supply operation. Additionally, to ensure that the output voltage can go to 0V in single supply, a transistor on the output acts as a passive pull-down as the output voltage nears 0V. As a result, the sink capability of the amplifier is reduced as the output voltage nears 0V in single supply. In dual supply operation, the full sink capability of 400μA at 25°C is maintained over the entire output voltage range. The single supply output sink capability is shown in Figure 4. The negative V_{SS} also gives improved output amplifier performance allowing an extended input reference voltage range and giving improved slew rate at the output.

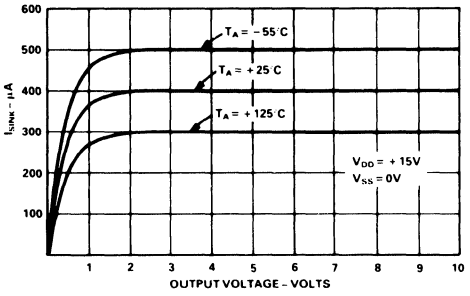


Figure 4. Single Supply Sink Current

The output broadband noise from the amplifier is 300μV peak-to-peak. Figure 5 shows a plot of noise spectral density versus frequency.

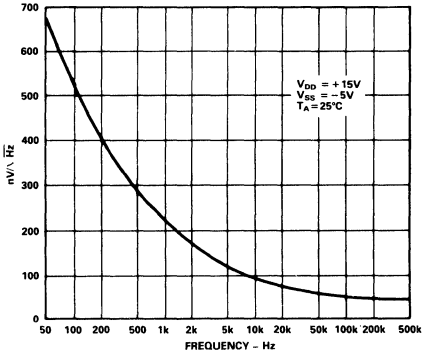


Figure 5. Noise Spectral Density vs. Frequency

DIGITAL INPUTS

The AD7228 digital inputs are compatible with either TTL or 5V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by on-chip distributed diodes.

SUPPLY CURRENT

The AD7228 has a maximum I_{DD} specification of 22mA and a maximum I_{SS} of 20mA over the −55°C to +125°C temperature range. This maximum current specification is actually determined by the current at −55°C. Figure 6 shows a typical plot of power supply current versus temperature.

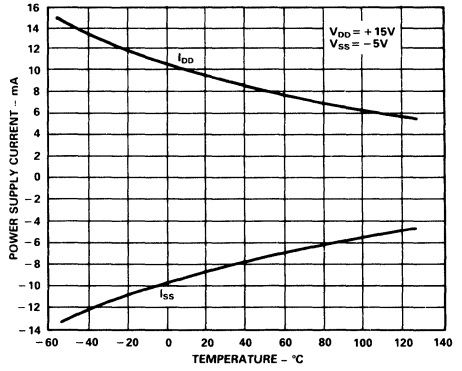


Figure 6. Power Supply Current vs. Temperature

APPLYING THE AD7228

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for each channel of the AD7228, with the output voltage having the same positive polarity as V_{REF}. Connections for unipolar output operation are shown in Figure 7. The AD7228 can be operated from single or dual supplies as outlined earlier. The voltage at the reference input must never be negative with respect to GND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table II.

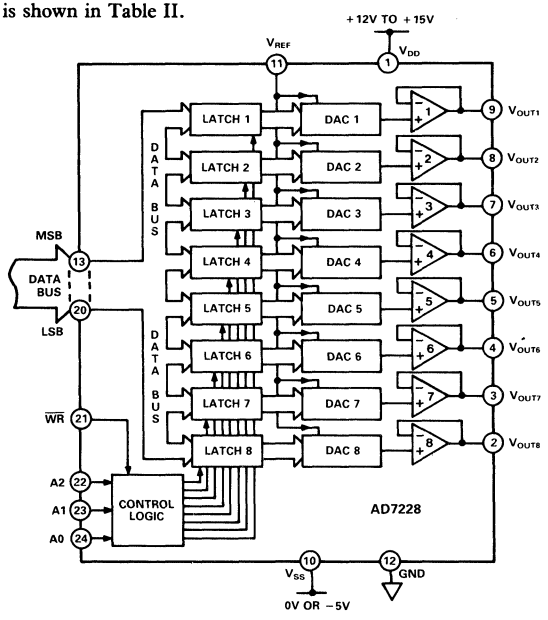


Figure 7. Unipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table II. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

Each of the DACs on the AD7228 can be individually configured for bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 8 shows a circuit used to implement offset binary coding (bipolar operation) with DAC 1 of the AD7228. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_1 \cdot V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_1 - 1) \cdot (V_{REF})$$

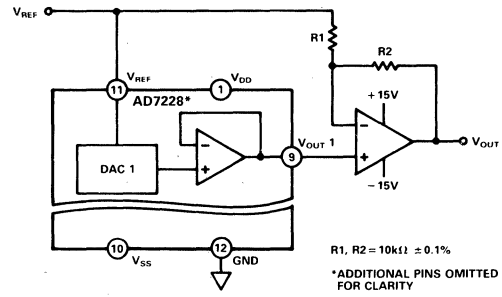


Figure 8. Bipolar Output Circuit

where D_1 is a fractional representation of the digital word in latch 1 of the AD7228. ($0 \leq D_1 \leq 255/256$)

Mismatch between R1 and R2 causes gain and offset errors, and therefore, these resistors must match and track over temperature. Once again, the AD7228 can be operated from single supply or from dual supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 8 with R1 = R2.

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table III. Bipolar Code Table

AC REFERENCE SIGNAL

In some applications it may be desirable to have an ac signal applied as the reference input to the AD7228. The AD7228 has multiplying capability within the upper (+10V) and lower (+2V) limits of reference voltage when operated with dual supplies. Therefore, ac signals need to be ac coupled and biased up before being applied to the reference input. Figure 9 shows a sine-wave signal applied to the reference input of the AD7228. For input frequencies up to 50kHz, the output distortion typically remains less than 0.1%. The typical 3dB bandwidth for small signal inputs is 800kHz.

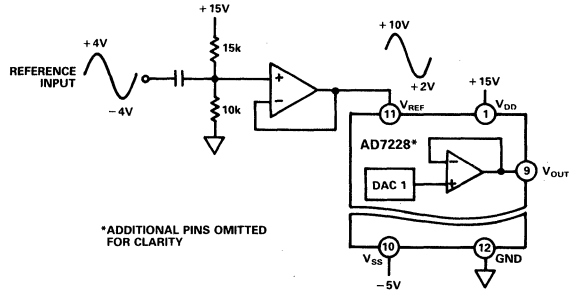


Figure 9. Applying an ac Signal to the AD7228

TIMING DESKEW

A common problem in ATE applications is the slowing or "rounding-off" of signal edges by the time they reach the pin-driver circuitry. This problem can easily be overcome by "squaring-up" the edge at the pin-driver. However, since each edge will not have been "rounded-off" by the same extent, this "squaring-up" could lead to incorrect timing relationship between signals. This effect is shown in Figure 10a.

The circuit of Figure 10b shows how two DACs of the AD7228 can help in overcoming this problem. The same two signals are applied to this circuit as were applied in Figure 10b. The output of each DAC is applied to one input of a high-speed comparator, and the signals are applied to the other inputs. Varying the output voltage of the DAC effectively varies the trigger point at which the comparator flips. Thus the timing relationship between the two signals can be programmably corrected (or deskewed) by varying the code to the DAC of the AD7228. In a typical application, the code is loaded to the DACs for correct timing relationships during the calibration cycle of the instrument.

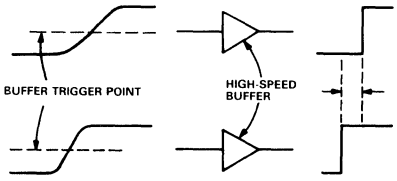


Figure 10a. Time Skewing Due to Slowing of Edges

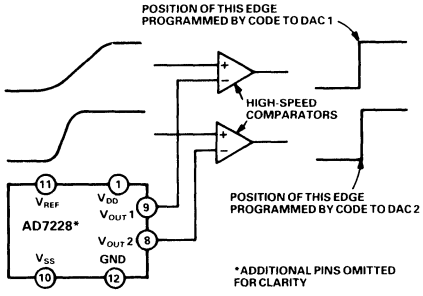


Figure 10b. AD7228 Timing Deskew Circuit

COARSE/FINE ADJUST

The DACs on the AD7228 can be paired together to form a coarse/fine adjust function as indicated in Figure 11. The function is achieved using one external op amp and a few resistors per pair of DACs.

DAC1 is the most significant or coarse DAC. Data is first loaded to this DAC to coarsely set the output voltage. DAC2 is then used to fine tune this output voltage. Varying the ratio of R1 to R2 varies the relative effect of the coarse and fine DACs on the output voltage. For the resistor values shown, DAC2 has a resolution of 150μV in a 10V output range. Since each DAC on the AD7228 is guaranteed monotonic, the coarse adjustment and fine adjustment are each monotonic. One application for this is as a set-point controller (see "Circuit Applications of the AD7226 Quad CMOS DAC" available from Analog Devices, Publication Number E873-15-11/84).

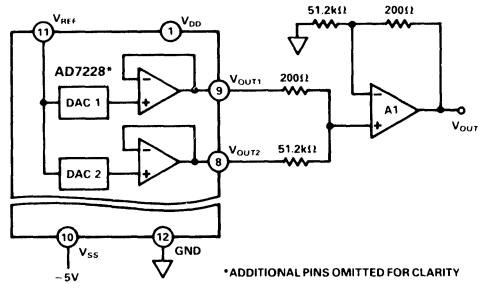


Figure 11. Coarse/Fine Adjust Circuit

SELF-PROGRAMMABLE REFERENCE

The circuit of Figure 12 shows how one DAC of the AD7228, in this case DAC1, may be used in a feedback configuration to provide a programmable reference for itself and the other seven converters. The relationship of V_{REF} to V_{IN} is expressed by

$$V_{REF} = \frac{(1+G)}{(1+G \cdot D_1)} \cdot V_{IN} \quad \text{where } G = R2/R1$$

Figure 13 shows typical plots of V_{REF} versus digital code, D_1, for three different values of G. With $V_{IN} = 2.5V$ and $G = 3$ the voltage at the output varies between 2.5V and 10V giving an effective 10-bit dynamic range to the other seven converters. For correct operation of the circuit, V_{SS} should be $-5V$ and R1 greater than 6.8kΩ.

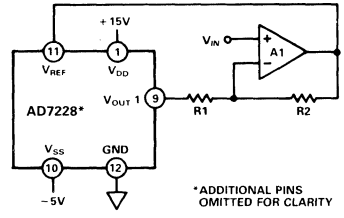


Figure 12. Self-Programmable Reference

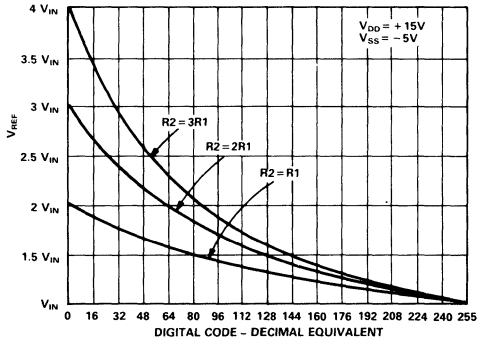


Figure 13. Variation of V_{REF} with Feedback Configuration

5V SINGLE SUPPLY OPERATION

The AD7228 can be operated from a single +5V power supply resulting in only slightly degraded accuracy performance from the part. Figure 14 shows a typical plot of relative accuracy for the part with 5V V_{DD} and a reference voltage of +1.23V. One important parameter which retains its specified performance is differential nonlinearity which remains within ±1LSB ensuring that the DACs on the AD7228 remain monotonic over the output voltage range.

The output transfer function sits on top of the amplifier offset voltage. Since the reference voltage is reduced, the offset voltage amounts to a few LSBs. For parts with a true negative offset (when V_{SS} = −5V), the transfer function does not move off the bottom rail for the first few LSBs of code. After this the transfer function will continue as normal. The relative accuracy plot of Figure 14 is for a part with a true positive offset.

The required overhead voltage of 3.5V must be maintained between V_{DD} and the reference voltage which limits the reference voltage range. However, operating the part from a single +5V supply gives a considerable reduction in power dissipation (to typically 50mW). The digital input threshold levels and digital input currents are not affected by operating the part from the single +5V supply.

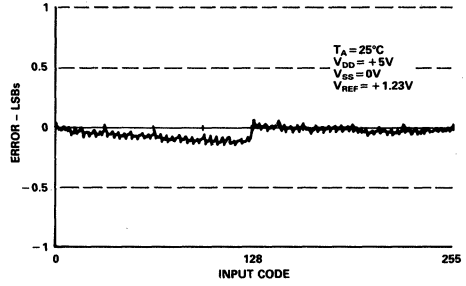


Figure 14. Relative Accuracy at +5V V_{DD}

MICROPROCESSOR INTERFACING

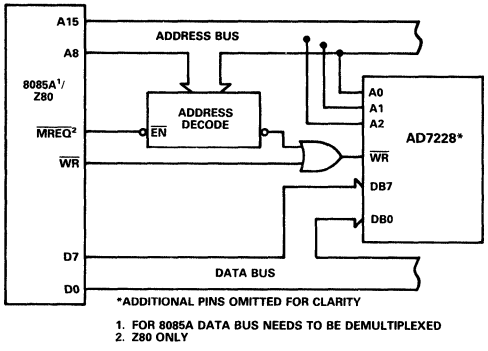


Figure 15. AD7228 to 8085A/Z80 Interface

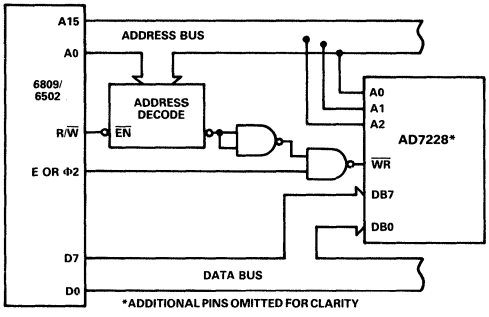


Figure 16. AD7228 to 6809/6502 Interface

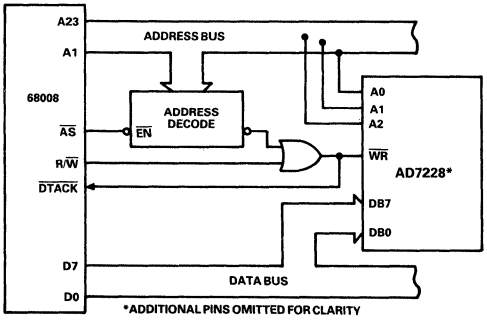


Figure 17. AD7228 to 68008 Interface

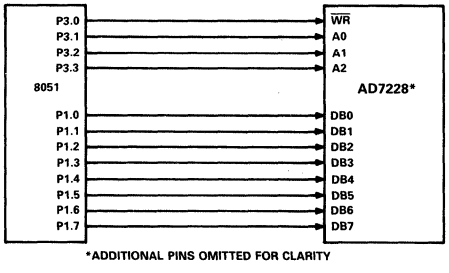


Figure 18. AD7228 to MCS-51 Interface

LC²MOS Dual 12-Bit DACPORT

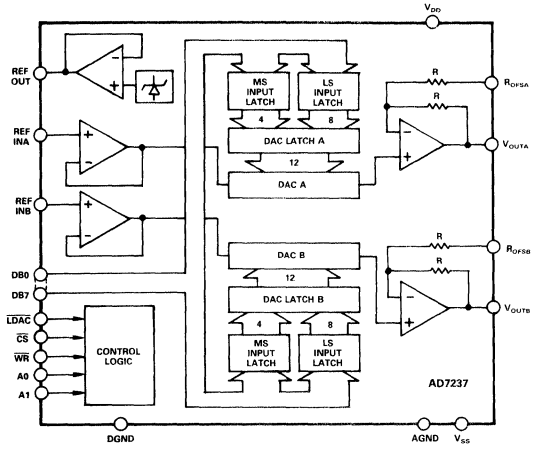
AD7237/AD7247

FEATURES

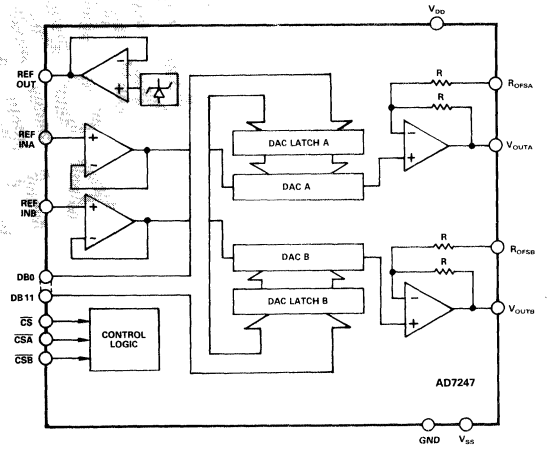
Complete Dual 12-Bit DAC Comprising
- **Two 12-Bit CMOS DACs**
- **On-Chip Voltage Reference**
- **Output Amplifiers**
- **Reference Buffer Amplifiers**

Parallel Loading Structure: AD7247
(8+4) Loading Structure: AD7237
Single or Dual Supply Operation
Low Power – 150 mW typ in Single Supply

AD7237 FUNCTIONAL BLOCK DIAGRAM



AD7247 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7237/AD7247 is a complete, dual, 12-bit, voltage output digital-to-analog converter with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7247 accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7237 has a double buffered interface structure and an 8-bit wide data bus with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7237 updates the DAC latches and analog outputs.

A REF OUT/REF IN function is provided which means that the on-chip 5 V reference or an external reference can be used to supply the reference voltage for the part. For single supply operation, two output ranges of 0 to +5 V and 0 to +10 V are available, while an additional ±5 V range is available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7237/AD7247 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin plastic and hermetic dual-in-line package (DIP) and are also packaged in a 28-terminal plastic leaded chip carrier (PLCC).

DACPORT is a trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. The AD7237/AD7247 is a dual 12-bit DACPORT™ on a single chip. This single chip design offers considerable space saving and increased reliability over multichip designs.
2. Between them the AD7237 and AD7247 offer a versatile interface arrangement to either 8-bit or 16-bit data bus structures.

SPECIFICATIONS (V_{DD} = +15 V, ±5%, V_{SS} = 0 V or −15 V ±5%, AGND = DGND (GND) = 0 V, REF IN = +5 V, R_L = 2 kΩ, C_L = 100 pF. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A[1]	K, B	S	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[2]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[2]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[2]	±3	±3	±5	LSB max	V_{SS} = 0 V. DAC Latch Contents All 0s
Bipolar Zero Error[2]	±4	±4	±6	LSB max	V_{SS} = −15 V. DAC Latch Contents 1000 0000 0000
Full Scale Error[2,3]	±5	±5	±8	LSB max	
REFERENCE OUTPUT					
REF OUT	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	
Reference Temperature Coefficient	±25	±25	±30	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0–100 μA)
REFERENCE INPUT					
Reference Input Range	4.75/5.25	4.75/5.25	4.75/5.25	V min/V max	5 V ± 5%
Input Current	50	50	50	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current					
I_{IN} (Data Inputs)	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
I_{INH} (Control Inputs)[4]	±10	±10	±10	μA max	V_{IN} = V_{DD}
I_{INL} (Control Inputs)[4]	±150	±150	±200	μA max	V_{IN} = 0 V
Input Capacitance[5] (AD7247)	8	8	8	pF max	
Input Capacitance[5] (AD7237)	16	16	16	pF max	
ANALOG OUTPUTS					
Output Range Resistors	15/30	15/30	15/30	kΩ min/ kΩ max	
Output Voltage Ranges	+5, +10	+5, +10	+5, +10	V	V_{SS} = 0 V. Pin Strappable
Output Voltage Ranges	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	V_{SS} = −15 V. Pin Strappable
DC Output Impedance	0.5	0.5	0.5	Ω typ	
Short Circuit Current	40	40	40	mA typ	
AC CHARACTERISTICS[5]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full Scale Change	5	5	5	μs max	Typically 3 μs. DAC Latch All 0s to all 1s
Negative Full Scale Change	10	10	10	μs max	Typically 5 μs. DAC Latch All 1s to All 0s V_{SS} = −15 V
Negative Full Scale Change	10	10	10	μs typ	DAC Latch All 1s to All 0s. V_{SS} = 0V
Digital-to-Analog Glitch Impulse[2]	30	30	30	nV secs typ	
Digital Feedthrough[2]	10	10	10	nV secs typ	
Digital Crosstalk[2]	30	30	30	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+15	+15	+15	V nom	±5% for Specified Performance Unless Otherwise Stated
V_{SS} (Dual Supplies)	−15	−15	−15	V nom	±5% for Specified Performance Unless Otherwise Stated
I_{DD}	18	18	18	mA max	Output Unloaded. Typically 10 mA
I_{SS} (Dual Supplies)	8	8	8	mA max	Output Unloaded. Typically 5 mA

NOTES
[1]Temperature ranges are as follows: J, K Versions, −40°C to +85°C; A, B Versions, −40°C to +85°C; S Version, −55°C to +125°C.
[2]See Terminology.
[3]Measured with respect to REF IN and includes unipolar/bipolar offset error.
[4]Control inputs are A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$ for the AD7237 and $\overline{CSA}$, $\overline{CSB}$ and $\overline{WR}$ for the AD7247.
[5]Sample tested @+25°C to ensure compliance.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +15 V, ±5%; V_{SS} = 0 V or −15 V, ±5%)

Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	100	110	ns min	$\overline{WR}$ Pulse Width
t_4	130	150	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	10	15	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6[3]	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_7[3]	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_8[3]	100	100	ns min	$\overline{LDAC}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figures 3 and 5.
[3]AD7237 Only.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to GND (AD7247) . . . . . −0.3 V to +17 V
V_{DD} to AGND, DGND (AD7237) . . . . . −0.3 V to +17 V
V_{DD} to V_{SS} . . . . . −0.3 V to +34 V
AGND to DGND (AD7237) . . . . . −0.3 V , V_{DD} +0.3 V
V_{OUTA}, V_{OUTB} to AGND (GND). . V_{SS} −0.3 V to V_{DD} +0.3 V
REF OUT[1] to AGND (GND) . . . . . 0 V to V_{DD}
REF IN to AGND (GND). . . . . −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND (GND) . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K Versions). . . . . −40°C to +85°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C. . . . . 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

NOTE
[1]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD7237 ORDERING INFORMATION[1]

Relative Accuracy (LSB)	Temperature Range and Package Options[2]		
	−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
	Plastic DIP (N-24)	Hermetic DIP (Q-24)	Hermetic DIP (Q-24)
±1 max	AD7237JN	AD7237AQ	AD7237SQ[3]
±1/2 max	AD7237KN	AD7237BQ	
	PLCC (P-28A)[4]		
±1 max	AD7237JP		
±1/2 max	AD7247KP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Available to /883 processing only.
[4]PLCC: Plastic Leaded Chip Carrier.

AD7247 ORDERING INFORMATION[1]

Relative Accuracy (LSB)	Temperature Range and Package Options[2]		
	−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
	Plastic DIP (N-24)	Hermetic DIP (Q-24)	Hermetic DIP (Q-24)
±1 max	AD7247JN	AD7247AQ	AD7247SQ[3]
±1/2 max	AD7247KN	AD7247BQ	
	PLCC (P-28A)[4]		
±1 max	AD7247JP		
±1/2 max	AD7247KP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Available to /883 processing only.
[4]PLCC: Plastic Leaded Chip Carrier.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY (LINEARITY)

Relative Accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full scale errors and is expressed in LSBs or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±0.9 LSB max over the operating temperature range ensures monotonicity.

SINGLE SUPPLY LINEARITY AND GAIN ERROR

The output amplifiers of the AD7237/AD7247 can have true negative offsets even when the part is operated from a single +15 V supply. However, because the negative supply rail (V_{SS}) is 0 V, the output cannot actually go negative. Instead, when the output voltage is less than the (negative) offset voltage, the output voltage sits at 0 V, resulting in the transfer function shown in Figure 1. This "knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

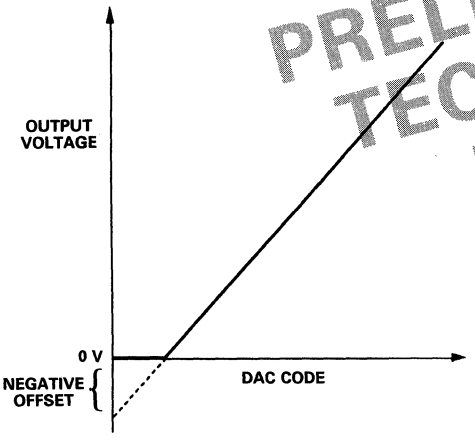


Figure 1. Effect of Negative Offset (Single Supply)

Normally, linearity is measured between zero (all 0s input code) and full scale (all 1s input code) after offset and full scale have been adjusted out or allowed for, but this is not possible in single supply operation if the offset is negative, due to the knee in the transfer function. Instead, linearity of the AD7237/AD7247 in the unipolar mode is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset. For the J, A, K, B versions, the linearity is measured between Codes 3 and 4095. For the S grade, linearity is measured between Code 5 and Code 4095.

UNIPOLAR OFFSET ERROR

Unipolar Offset Error is the measured output voltage from V_{OUTA} or V_{OUTB} with all zeros loaded into the DAC latches when the DACs are configured for unipolar output. It is a combination of the offset errors of the DAC and output amplifier.

BIPOLAR ZERO ERROR

Bipolar Zero Error is the voltage measured at V_{OUTA} or V_{OUTB} when the DAC is connected in the bipolar mode and loaded with code 2048. It is due to a combination of offset errors in the DAC, amplifier offset and mismatch in the application resistors around the amplifier.

FULL SCALE ERROR

Full Scale Error is a measure of the output error when the amplifier output is at full scale (for the bipolar output range full scale is either positive or negative full scale). It is measured with respect to the reference input voltage and includes the offset errors.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse injected for the digital inputs to the analog output when the data inputs change state, but the data in the DAC latches is not changed.

For the AD7237 it is measured with $\overline{LDAC}$ held high. For the AD7247 it is measured with $\overline{CSA}$ and $\overline{CSB}$ held high.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in digital code to the DAC latch of the other converter. It is specified in nV secs.

DIGITAL-TO-ANALOG GLITCH IMPULSE

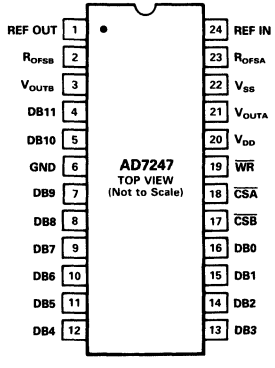
This is the voltage spike that appears at the output of the DAC when the digital code changes before the output settles to its final value. The energy in the glitch is specified in nV secs and is measured for a 1 LSB change around the major carry transition (0111 1111 1111 to 1000 0000 0000).

AD7247 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

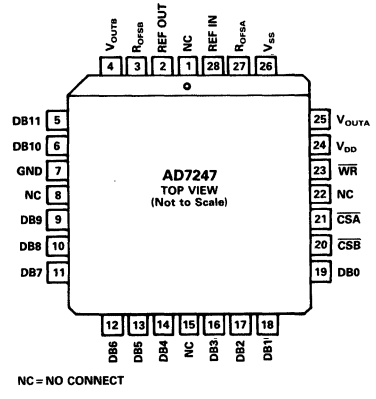
Pin	Mnemonic	Description
1	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference, REF OUT should be connected to REF IN.
2	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
3	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to + 10 V and ± 5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
4	DB11	Data Bit 11 (MSB).
5	DB10	Data Bit 10.
6	GND	Ground. Ground reference for all on-chip circuitry.
7–15	DB9–DB1	Data Bit 9 to Data Bit 1.
16	DB0	Data Bit 0 (LSB).
17	$\overline{CSB}$	Chip Select Input for DAC B. Active low logic input. DAC B is selected when this input is active.
18	$\overline{CSA}$	Chip Select Input for DAC A. Active low logic input. DAC A is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CSA}$ and $\overline{CSB}$ to write data to the DAC latches.
20	V_{DD}	Positive Supply, +15 V.
21	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
22	V_{SS}	Negative Supply, −15 V.
23	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to GND for the +10 V range and to REF IN for the ±5 V range.
24	REF IN	Voltage Reference Input. The common reference voltage for both DACs is applied to this pin. It is internally buffered before being applied to both DACs. The nominal reference voltage for correct operation of the AD7247 is 5 V.

AD7247 PIN CONFIGURATIONS

DIP



PLCC



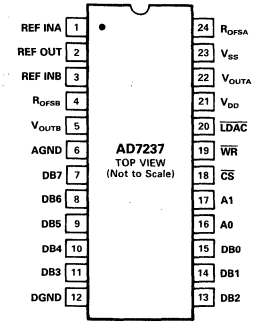
NC = NO CONNECT

AD7237 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

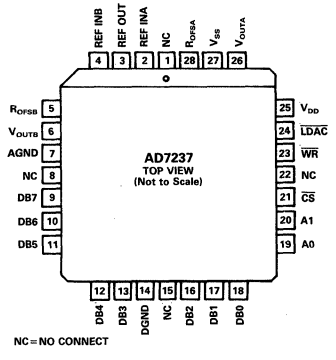
Pin	Mnemonic	Description
1	REF INA	Voltage Reference Input for DAC A. The reference voltage for DAC A is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237 is 5 V.
2	REF OUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part with internal reference REF OUT should be connected to REF INA, REF INB.
3	REF INB	Voltage Reference Input for DAC B. The reference voltage for DAC B is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7237 is 5 V.
4	R_{OFSB}	Output Offset Resistor for DAC B. This input configures the output ranges for DAC B. It is connected to V_{OUTB} for the +5 V range, to AGND for the +10 V range and to REF INB for the ±5 V range.
5	V_{OUTB}	Analog Output Voltage from DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
6	AGND	Analog Ground. Ground reference for DACs, reference and output buffer amplifiers.
7	DB7	Data Bit 7.
8–10	DB6–DB4	Data Bit 6 to Data Bit 4.
11	DB3	Data Bit 3/Data Bit 11 (MSB).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13	DB2	Data Bit 2/Data Bit 10.
14	DB1	Data Bit 1/Data Bit 9.
15	DB0	Data Bit 0 (LSB)/Data Bit 8.
16	A0	Address Input. Least significant address input for input latches. A0 and A1 select which of the four input latches data is written to (see Table II).
17	A1	Address Input. Most significant address input for input latches.
18	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
19	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input which is used in conjunction with $\overline{CS}$, A0 and A1 to write data to the input latches.
20	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latches from the respective input latches on the falling edge of this signal.
21	V_{DD}	Positive Supply, +15 V.
22	V_{OUTA}	Analog Output Voltage from DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 to +5 V, 0 to +10 V and ±5 V. The amplifier is capable of developing +10 V across a 2 kΩ resistor to GND.
23	V_{SS}	Negative Supply, −15 V.
24	R_{OFSA}	Output Offset Resistor for DAC A. This input configures the output ranges for DAC A. It is connected to V_{OUTA} for the +5 V range, to AGND for the +10 V range and to REF INA for the ±5 V range.

AD7237 PIN CONFIGURATIONS

DIP



PLCC



INTERFACE LOGIC INFORMATION – AD7247

Table I shows the truth table for AD7247 operation. The part contains a single, parallel 12-bit latch for each DAC. It can be treated as two independent DACs, each with its own $\overline{CS}$ input and a common $\overline{WR}$ input. $\overline{CSA}$ and $\overline{WR}$ control the loading of data to the DAC A latch while $\overline{CSB}$ and $\overline{WR}$ control the loading of the DAC B latch. If $\overline{CSA}$ and $\overline{CSB}$ are both low, with $\overline{WR}$ low, the same data will be written to both DAC latches. All control signals are level triggered and therefore either or both latches can be made transparent. Input data is latched to the respective latch on the rising edge of $\overline{WR}$. Figure 2 shows the input control logic for the AD7247, while the write cycle timing diagram for the part is shown in Figure 3.

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No Data Transfer
1	1	X	No Data Transfer
0	1	0	DACA Latch Transparent
1	0	0	DACB Latch Transparent
0	0	0	Both DAC Latches Transparent

X = Don't Care.

Table I. AD7247 Truth Table

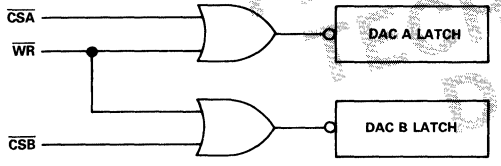


Figure 2. AD7247 Input Control Logic

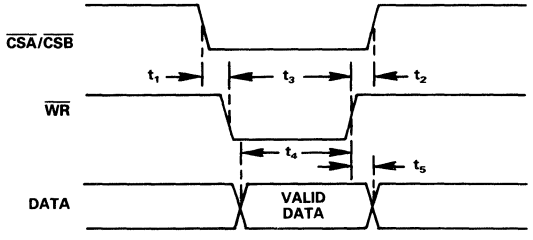


Figure 3. AD7247 Write Cycle Timing Diagram

INTERFACE LOGIC INFORMATION – AD7237

The input loading structure on the AD7237 is configured for interfacing to microprocessors with an 8-bit-wide data bus. The part contains two 12-bit latches per DAC – an input latch and a DAC latch. Each input latch is further subdivided into a least significant 8-bit latch and a most significant 4-bit latch. Only the data held in the DAC latches determines the outputs from the part. The input control logic for the AD7237 is shown in Figure 4, while the write cycle timing diagram is shown in Figure 5.

$\overline{CS}$, $\overline{WR}$, A0 and A1 control the loading of data to the input latches. The eight data inputs accept right-justified data. Data can be loaded to the input latches in any sequence. Provided that $\overline{LDAC}$ is held high, there is no analog output change as a result of loading data to the input latches. Address lines A0 and A1 determine which latch data is loaded to when $\overline{CS}$ and $\overline{WR}$ are low. The selection of the input latches is shown in the truth table for AD7237 operation in Table II.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latches to the DAC latches. Both DAC latches, and hence both analog outputs, are updated at the same time. The $\overline{LDAC}$ signal is level triggered and data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in the simultaneous updating of multiple AD7237s. However, care must be taken while exercising $\overline{LDAC}$ during a write cycle. If an $\overline{LDAC}$ operation overlaps a $\overline{CS}$ and $\overline{WR}$ operation, there is a possibility of invalid data being latched to the output. To avoid this, $\overline{LDAC}$ must remain low after $\overline{CS}$ or $\overline{WR}$ return high for a period equal to or greater than t_8, the minimum $\overline{LDAC}$ pulse width.

$\overline{CS}$	$\overline{WR}$	A1	A0	$\overline{LDAC}$	Function
1	X	X	X	1	No Data Transfer
X	1	X	X	1	No Data Transfer
0	0	0	0	1	DAC A LS Input Latch Transparent
0	0	0	1	1	DAC A MS Input Latch Transparent
0	0	1	0	1	DAC B LS Input Latch Transparent
0	0	1	1	1	DAC B MS Input Latch Transparent
1	1	X	X	0	DACA and DACB DAC Latches Updated Simultaneously from the Respective Input Latches

X = Don't Care.

Table II. AD7237 Truth Table

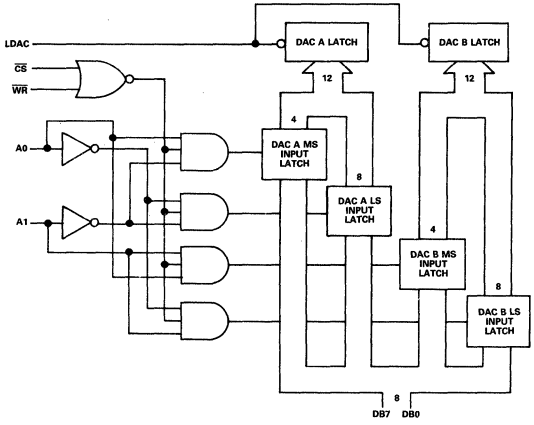


Figure 4. AD7237 Input Control Logic

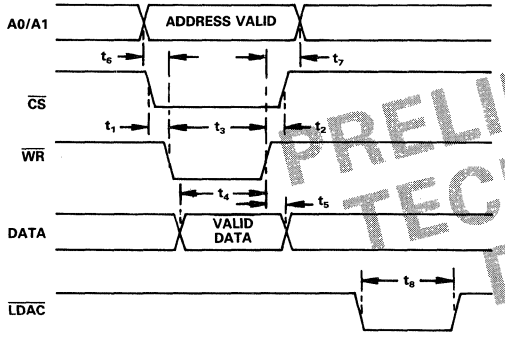


Figure 5. AD7237 Write Cycle Timing Diagram

APPLYING THE AD7237/AD7247

The internal scaling resistors provided on the AD7237/AD7247 allow several output voltage ranges. The part can produce unipolar output ranges of 0 to +5 V or 0 to +10 V and a bipolar output range of ±5 V. Connections for the various ranges are outlined below. Since each DAC has its own R_{OFS} input, the two DACs on each part can be set up for different output ranges.

Unipolar (0 to +10 V) Configuration

The first of the configurations provides an output voltage range of 0 V to +10 V. This is achieved by connecting the output offset resistor, R_{OFSA}, or R_{OFSB}, to GND (AGND for AD7237). In this configuration, the AD7237/AD7247 can be operated from single or dual supplies. Figure 6 shows the connection diagram for unipolar operation for DAC A of the AD7237, while the table for output voltage versus digital code in the DAC latch is shown in Table III. Similar connections apply to the AD7247.

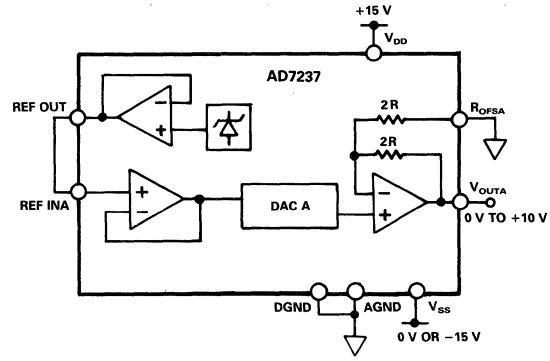


Figure 6. Unipolar (0 to +10 V) Configuration

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	+2 · REF IN · (4095/4096)
1000 0000 0001	+2 · REF IN · (2049/4096)
1000 0000 0000	+2 · REF IN · (2048/4096) = +REF IN
0111 1111 1111	+2 · REF IN · (2047/4096)
0000 0000 0001	+2 · REF IN · (1/4096)
0000 0000 0000	0 V

Note: 1 LSB = REF IN/2048.

Table III. Unipolar Code Table (0 to+10 V Range)

Unipolar (0 to +5 V) Configuration

The 0 to +5 V output voltage range is achieved by tying R_{OFSA} or R_{OFSB} to V_{OUTA} or V_{OUTB}. Once again, the AD7237/AD7247 can be operated single supply or from dual supplies. The table for output voltage versus digital code is as in Table III, with 2 · REF IN replaced by REF IN. Note, for this range, 1LSB = REF IN · (2^{-12}) = (REF IN/4096).

Bipolar Configuration

The bipolar configuration for the AD7237/AD7247, which gives an output range of −5 V to +5 V, is achieved by connecting R_{OFSA}, or R_{OFSB}, to REF IN. The AD7237/AD7247 must be operated from dual supplies to achieve this output voltage range. The code table for bipolar operation is shown in Table IV.

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	+REF IN · (2047/2048)
1000 0000 0001	+REF IN · (1/2048)
1000 0000 0000	0V
0111 1111 1111	−REF IN · (1/2048)
0000 0000 0001	−REF IN · (2047/2048)
0000 0000 0000	−REF IN · (2048/2048) = −REF IN

Note: 1 LSB = REF IN/2048.

Table IV. Bipolar Code Table

ANALOG DEVICES

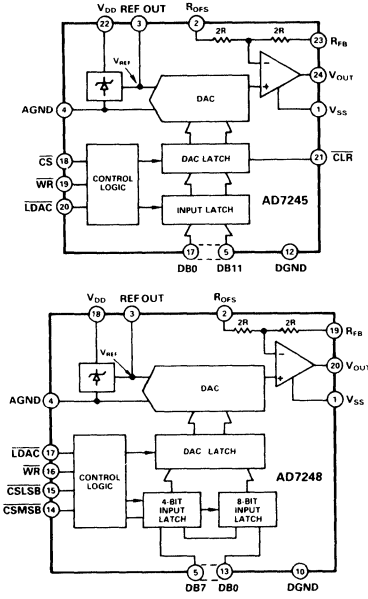
LC²MOS 12-Bit DACPORTS

AD7245/AD7248

FEATURES

12-Bit CMOS DAC with Output Amplifier and Reference
Parallel Loading Structure: AD7245
(8+4) Loading Structure: AD7248
Single or Dual Supply Operation
Fast Digital Interface (80ns $\overline{WR}$ Pulse)
Low Power (65mW typ)
0.3", Skinny, 20- and 24-Pin DIP
20- and 28-Terminal Surface Mount Packages

AD7245/AD7248 FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD7245/AD7248 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The part features double-buffered interface logic with a 12-bit input latch and 12-bit DAC latch. The data held in the DAC latch determines the analog output of the converter. The AD7245 accepts 12-bit parallel data which is latched into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$. The AD7248 has an 8-bit-wide data bus, and data is loaded to the input latch in two write operations, an 8-bit LSB load and a 4-bit MSB load. The input data must be right justified. For both parts, an asynchronous $\overline{LDAC}$ signal transfers data from the input latch to the DAC latch. The AD7245 also has a $\overline{CLR}$ signal on the DAC latch which allows features such as power-on reset to be implemented. All logic inputs are level triggered and are TTL and CMOS (5V) level compatible, while the control logic is speed compatible with most microprocessors.

The on-chip 5V buried Zener diode provides a low-noise, temperature compensated reference for the DAC. The gain setting resistors allow a number of ranges at the output: 0 to +5V, 0 to +10V when using single supply and 0 to +5V, −5V to +5V when operated in dual supplies. The output amplifier is capable of developing +10V across a 2kΩ load to GND.

The AD7245/AD7248 is fabricated in an all ion-implanted, high-speed linear, compatible CMOS (LC²MOS) process. The AD7245 is packaged in a small, 0.3"-wide, 24-pin DIP and 28-terminal surface mount packages. The AD7248 is available in a 0.3"-wide, 20-pin DIP and 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT™
   The AD7245/AD7248 is a complete, voltage output, 12-bit DAC on one chip. This single-chip design of the DAC reference and output amplifier is inherently more reliable than multichip designs.
2. Microprocessor Compatibility
   The parallel loading structure of the AD7245 allows connection to microprocessors with a 16-bit-wide data bus. The AD7248 is aimed at microprocessors which have an 8-bit-wide data bus structure. The high-speed logic of both parts allows direct interfacing to most modern microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7245/AD7248 in multiple DAC systems.

DACPORT is a trademark of Analog Devices, Inc.

SPECIFICATIONS

SINGLE SUPPLY (V_{DD} = +15V ±5%[1]. V_{SS} = AGND = DGND = 0V; R_L = 2kΩ to GND; C_L = 100pF to GND; REF OUT unloaded unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Version[2]	S Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy	±1		LSB max	
		±1	LSB max	V_{DD} = +11.4V to +14.25V
		±1.5	LSB max	V_{DD} = +14.25V to +15.75V
Differential Nonlinearity[3]	±1	±1	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]				
at +25°C	±3	±3	LSB max	
T_{min} to T_{max}	±5	±5	LSB max	Typical Tempco is ±3ppm of FSR[4]/°C
DAC Gain Error[3,5]	±2	±2	LSB max	
Full-Scale Output Voltage Error[6]				
T_A = +25°C	±0.2	±0.2	% of FSR max	V_{DD} = +15V for J, A Grades; V_{DD} = +12V & +15V for S Grade
T_{min} to T_{max}		±0.6	% of FSR max	V_{DD} = +12V & +15V
ΔFull Scale/ΔV_{DD}				
T_A = +25°C	±0.12	±0.12	% of FSR/V max	ΔV_{DD} = +5%
Full-Scale Temperature Coefficient[7]	±30		ppm of FSR/°C max	
ΔOffset/ΔV_{DD}	±1	±2	mV max	ΔV_{DD} = ±5%
REFERENCE				
Reference Output @ +25°C	4.99/5.01	4.99/5.01	V min to V max	V_{DD} = +15V for J, A Grades; V_{DD} ± +12V & +15V for S Grade
ΔReference/ΔV_{DD}				
T_A = +25°C	6	6	mV/V max	ΔV_{DD} = ±5%
Reference Temperature Coefficient	±30	±40	ppm of FSR/°C typ	FSR = 5V
Reference Load Sensitivity (ΔReference/ΔI)	±1	±1.5	mV max	Reference Load Current Change (0-100μA)
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN} (Data Inputs)				V_{IN} = 0V or V_{DD}
at +25°C	±1	±1	μA max	
T_{min} to T_{max}	±10	±10	μA max	
I_{INH} (Control Inputs)[8]				V_{IN} = V_{DD}
at +25°C	±1	±1	μA max	
T_{min} to T_{max}	±10	±10	μA max	
I_{INL} (Control Inputs)[8]				V_{IN} = 0V
at +25°C	150	150	μA max	
T_{min} to T_{max}	200	200	μA max	
Input Capacitance[9] (AD7245)	8	8	pF max	
Input Capacitance[9] (AD7248)	16	16	pF max	
ANALOG OUTPUT				
Output Range Resistors	15/30	15/30	kΩ min/kΩ max	
Ranges	+5, +10	+5, +10	V	Pin Strappable. Min Load Resistance is 2kΩ to GND
dc Output Impedance	0.5	0.5	Ω typ	
Short-Circuit Current	40	40	mA typ	
DYNAMIC PERFORMANCE[9]				
Output Voltage Settling Time				Settling Time to ±1LSB. R_L = 5kΩ, C_L = 100pF
Positive Full-Scale Change	5	8	μs max	DAC Register all 0s to all 1s
Negative Full-Scale Change	10	10	μs typ	DAC Register all 1s to all 0s
Output Voltage Slew Rate	2	1.5	V/μs min	
Digital Feedthrough[3,10]	10	10	nV secs typ	
Digital-to-Analog Glitch Impulse	30	30	nV secs typ	Major Carry Transition
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	11.4/15.75	V min/V max	For Specified Performance
I_{DD}				Output Unloaded
at +25°C	9	9	mA max	Typically 4.5mA
T_{min} to T_{max}	12	12	mA max	

NOTES

[1]For the S Version only: V_{DD} = +12V ±5% to +15V ±5%

[2]Temperature ranges are as follows:
J Version, 0 to +70°C
A Version, −25°C to +85°C
S Version, −55°C to +125°C.

[3]See Terminology.

[4]FSR means Full-Scale Range and is 5V with R_{OFS} connected to R_{FB}, V_{OUT} and 10V with R_{OFS} connected to GND and R_{FB} connected to V_{OUT}.

[5]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

[6]This error is calculated w.r.t. an ideal 4.9988V (on the 5V range) or 9.9976V (on the 10V range).
It includes the effects of internal voltage reference, gain and offset errors.

[7]Full-scale T.C. = ΔFS/ΔT, where ΔFS is the full-scale change from T_A = +25°C to T_{min} or T_{max}.

[8]Control inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$ and $\overline{CLR}$ for AD7245 and $\overline{CSMSB}$, $\overline{CSLSB}$, $\overline{WR}$ and $\overline{LDAC}$ for AD7248.

[9]Sample tested at +25°C to ensure compliance.

[10]The metal lid on the AD7245 (only) ceramic (D-24A) package is connected to Pin 12 (DGND).

Specifications subject to change without notice.

SPECIFICATIONS

DUAL SUPPLY (V_{DD} = +15V ±5%[1], V_{SS} = −15V ±5%[1], AGND = DGND = 0V; R_L = 2kΩ to GND; C_L = 100pF to GND; REF OUT unloaded unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Version[2]	S Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1		LSB max	
		±1	LSB max	V_{DD}/V_{SS} = ±11.4V to ±14.25V
		±1.5	LSB max	V_{DD}/V_{SS} = ±14.25V to ±15.75V
Differential Nonlinearity[3]	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Offset Error[3]				R_{OFS} Connected to REF OUT
at +25°C	±3	±3	LSB max	
T_{min} to T_{max}	±5	±5	LSB max	Typical Tempco is ±3ppm of FSR[4]/°C
DAC Gain Error[3,5]	±2	±2	LSB max	
Full-Scale Output Voltage Error[6]				
T_A = +25°C	±0.2	±0.2	% of FSR max	V_{DD}/V_{SS} = ±15V for J, A Grades; V_{DD}/V_{SS} = ±12V & ±15V for S Grade
T_{min} to T_{max}		±0.6	% of FSR max	V_{DD}/V_{SS} = ±12V & ±15V
ΔFull Scale/ΔV_{DD}				
T_A = +25°C	±0.12	±0.12	% of FSR/V max	ΔV_{DD} = ±5%
ΔFull Scale/ΔV_{SS}				
T_A = +25°C	±0.01	±0.01	% of FSR/V max	ΔV_{SS} = ±5%
Full-Scale Temperature Coefficient[7]	±30		ppm of FSR/°C max	
ΔOffset/ΔV_{DD}	±1	±2	mV max	ΔV_{DD} = ±5%
ΔOffset/ΔV_{SS}	±1	±1	mV max	ΔV_{SS} = ±5%
REFERENCE				
Reference Output @ +25°C	4.99/5.01	4.99/5.01	V min to V max	V_{DD}/V_{SS} = ±15V for J, A Grades; V_{DD}/V_{SS} = ±12V & ±15V for S Grade
ΔReference/ΔV_{DD}				
T_A = +25°C	6	6	mV/V max	ΔV_{DD} = ±5%
Reference Temperature Coefficient	±30	±40	ppm of FSR/°C typ	FSR = 5V
Reference Load Sensitivity (ΔReference/ΔI)	±1	±1.5	mV max	Reference Load Current Change (0-100μA) (Not Including R_{OFS} Current)
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN} (Data Inputs)				V_{IN} = 0V or V_{DD}
at +25°C	±1	±1	μA max	
T_{min} to T_{max}	±10	±10	μA max	
I_{INH} (Control Inputs)[8]				V_{IN} = V_{DD}
at +25°C	±1	±1	μA max	
T_{min} to T_{max}	±10	±10	μA max	
I_{INL} (Control Inputs)[8]				V_{IN} = 0V
at +25°C	150	150	μA max	
T_{min} to T_{max}	200	200	μA max	
Input Capacitance[9] (AD7245)	8	8	pF max	
Input Capacitance[9] (AD7248)	16	16	pF max	
ANALOG OUTPUT				
Output Range Resistors	15/30	15/30	kΩ min/kΩ max	
Ranges	±5, +5	±5, +5	V	Pin Strappable. Min Load Resistance is 2kΩ to GND
dc Output Impedance	0.5	0.5	Ω typ	
Short-Circuit Current	40	40	mA typ	
DYNAMIC PERFORMANCE[9]				
Output Voltage Settling Time				Settling Time to ±1LSB. R_L = 5kΩ, C_L = 100pF
Positive Full-Scale Change	5	10	μs max	DAC Register all 0s to all 1s
Negative Full-Scale Change	10	10	μs max	DAC Register all 1s to all 0s
Output Voltage Slew Rate	2	1.5	V/μs min	
Digital Feedthrough[3,10]	10	10	nV secs typ	
Digital-to-Analog Glitch Impulse	30	30	nV secs typ	Major Carry Transition
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	11.4/15.75	V min/V max	For Specified Performance
V_{SS} Range	−14.25/−15.75	−11.4/−15.75	V min/V max	For Specified Performance
I_{DD}				Output Unloaded
at +25°C	9	9	mA max	Typically 5mA
T_{min} to T_{max}	12	12	mA max	
I_{SS}				Output Unloaded
at +25°C	3	3	mA max	Typically 2mA
T_{min} to T_{max}	5	5	mA max	

NOTES

[1]For the S Version only: V_{DD} = +12V ±5% to +15V ±5%; V_{SS} = −12V ±5% to −15V ±5%.

[2]Temperature ranges are as follows:
J Version, 0 to +70°C
A Version, −25°C to +85°C
S Version, −55°C to +125°C.

[3]See Terminology.

[4]FSR means Full-Scale Range and is 5V with R_{OFS} connected to R_{FB}, V_{OUT} and 10V with R_{OFS} connected to GND and R_{FB} connected to V_{OUT}.

[5]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

[6]This error is calculated w.r.t. an ideal 4.9988V (on the 5V range) or 9.9976V (on the 10V range).
It includes the effects of internal voltage reference, gain and offset errors.

[7]Full-scale T.C. = ΔFS/ΔT, where ΔFS is the full-scale change from T_A = +25°C to T_{min} or T_{max}.

[8]Control inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$ and $\overline{CLR}$ for AD7245 and $\overline{CSMSB}$, $\overline{CSLSB}$, $\overline{WR}$ and $\overline{LDAC}$ for AD7248.

[9]Sample tested at +25°C to ensure compliance.

[10]The metal lid on the AD7245 (only) ceramic (D-24A) package is connected to Pin 12 (DGND).

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1] (V_{DD} = +15V ±5%[2]; V_{SS} = 0V or −15V ±5%[2]; See Figures 5 and 7)

Parameter	J Grade	A Grade	S Grade	Units	Conditions
t_1					
@ +25°C	80	80	105	ns min	Chip Select Pulse Width
T_{min} to T_{max}	100	100	135	ns min	
t_2					
@ +25°C	80	80	105	ns min	Write Pulse Width
T_{min} to T_{max}	100	100	135	ns min	
t_3					
@ +25°C	0	0	0	ns min	Chip Select to Write Setup Time
T_{min} to T_{max}	0	0	0	ns min	
t_4					
@ +25°C	0	0	0	ns min	Chip Select to Write Hold Time
T_{min} to T_{max}	0	0	0	ns min	
t_5 (AD7245 Only)					
@ +25°C	100	100	155	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	110	130	250	ns min	
t_5 (AD7248 Only)					
@ +25°C	110	110	180	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	130	130	270	ns min	
t_6					
@ +25°C	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	ns min	
t_7					
@ +25°C	80	80	90	ns min	Load DAC Pulse Width
T_{min} to T_{max}	100	100	120	ns min	
t_8 (AD7245 Only)					
@ +25°C	80	80	140	ns min	Clear Pulse Width
T_{min} to T_{max}	100	100	200	ns min	

NOTE
[1]Sample tested at +25°C to ensure compliance.
[2]For the S Version only: V_{DD} = +12V ±5% to +15V ±5%; V_{SS} = 0V or −12V ±5% to −15V ±5%. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V, +17V
V_{DD} to DGND . . . . . −0.3V, +17V
V_{DD} to V_{SS} . . . . . −0.3V, +34V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
V_{OUT} to V_{SS}[1] . . . . . 0V, +24V
V_{OUT} to V_{DD}[1] . . . . . −32V, 0V
REF OUT[1] to AGND . . . . . 0V, V_{DD}
Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature
Commercial . . . . . 0 to +70°C
Industrial . . . . . −25°C to +85°C
Extended . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTE
[1]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

AD7245 ORDERING INFORMATION

Relative Accuracy (LSB)	Temperature Range and Package Options[1] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-24)	Hermetic DIP[2] (Q-24)	Hermetic DIP[2,3] (Q-24)
±1	AD7245JN	AD7245AQ	AD7245SQ
	PLCC[4] (P-28A)		LCCC[5] (E-28A)
±1	AD7245JP		AD7245SE

NOTES
[1]See Section 14 for package outline information.
[2]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.
[3]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

AD7248 ORDERING INFORMATION

Relative Accuracy (LSB)	Temperature Range and Package Options[1] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-20)	Hermetic DIP[2] (Q-20)	Hermetic DIP[2,3] (Q-20)
±1	AD7248JN	AD7248AQ	AD7248SQ
	PLCC[4] (P-20A)		LCCC[5] (E-20A)
±1	AD7248JP		AD7248SE

NOTES
[1]See Section 14 for package outline information.
[2]Analog Devices reserves the right to ship either ceramic (D-20) or cerdip (Q-20) hermetic packages.
[3]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

TERMINOLOGY

RELATIVE ACCURACY
Relative Accuracy, or end-point nonlinearity, is a measure of the actual deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY
Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH
Digital Feedthrough is the glitch impulse injected from the digital inputs to the analog output when the inputs change state. It is measured with $\overline{LDAC}$ high and is specified in nV secs.

DAC GAIN ERROR
DAC Gain Error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been allowed for. It is therefore defined as:

Measured Value – Offset – Ideal Value

where the ideal value is calculated relative to the actual reference value.

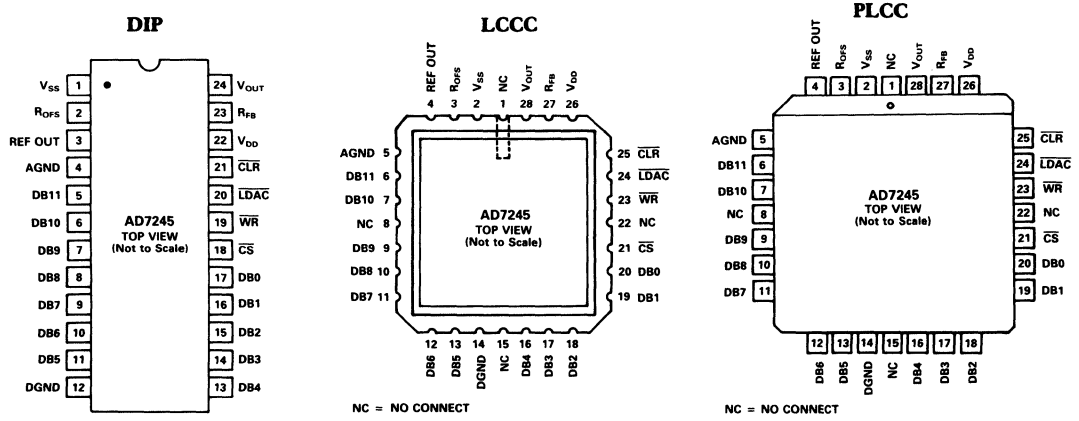
UNIPOLAR OFFSET ERROR
Unipolar Offset Error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured when the part is configured for unipolar outputs. It is present for all codes and is measured with all 0s in the DAC register.

BIPOLAR ZERO OFFSET ERROR
Bipolar Zero Offset Error is measured when the part is configured for bipolar output and is a combination of errors from the DAC and output amplifier. It is present for all codes and is measured with a code of 2048 (decimal) in the DAC register.

AD7245 PIN FUNCTION DESCRIPTION (DIP PIN NUMBERS)

Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB11	Data Bit 11. Most Significant Bit (MSB).
6–11	DB10–DB5	Data Bit 10 to Data Bit 5.
12	DGND	Digital Ground.
13–16	DB4–DB1	Data Bit 4 to Data Bit 1.
17	DB0	Data Bit 0. Least Significant Bit (LSB).
18	$\overline{CS}$	Chip Select Input (Active LOW). The device is selected when this input is active.
19	$\overline{WR}$	Write Input (Active LOW). This is used in conjunction with $\overline{CS}$ to write data into the input latch of the AD7245.
20	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
21	$\overline{CLR}$	Clear Input (Active LOW). When this input is active the contents of the DAC latch are reset to all 0s.
22	V_{DD}	Positive Supply Voltage.
23	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
24	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 to +5V, 0 to +10V or −5V to +5V.

AD7245 PIN CONFIGURATIONS

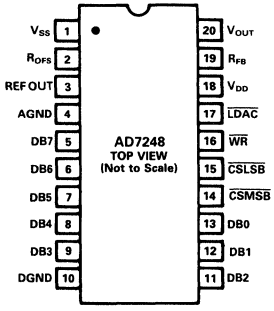


AD7248 PIN FUNCTION DESCRIPTION
(ANY PACKAGE)

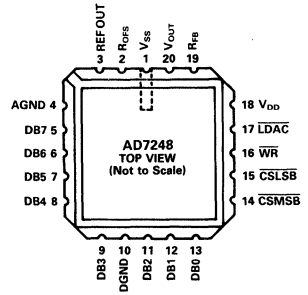
Pin	Mnemonic	Description
1	V_{SS}	Negative Supply Voltage (0V for single supply operation).
2	R_{OFS}	Bipolar Offset Resistor. This provides access to the on-chip application resistors and allows different output voltage ranges.
3	REF OUT	Reference Output. The on-chip reference is provided at this pin and is used when configuring the part for bipolar outputs.
4	AGND	Analog Ground.
5	DB7	Data Bit 7.
6	DB6	Data Bit 6.
7	DB5	Data Bit 5.
8	DB4	Data Bit 4.
9	DB3	Data Bit 3/Data Bit 11 (MSB).
10	DGND	Digital Ground.
11	DB2	Data Bit 2/Data Bit 10.
12	DB1	Data Bit 1/Data Bit 9.
13	DB0	Data Bit 0 (LSB)/Data Bit 8.
14	$\overline{CSMSB}$	Chip Select Input for MS Nibble. (Active LOW). This selects the upper 4 bits of the input latch. Input data is right-justified.
15	$\overline{CSLSB}$	Chip Select Input for LS byte. (Active LOW). This selects the lower 8 bits of the input latch.
16	$\overline{WR}$	Write Input. This is used in conjunction with $\overline{CSMSB}$ and $\overline{CSLSB}$ to load data into the input latch of the AD7248.
17	$\overline{LDAC}$	Load DAC Input (Active LOW). This is an asynchronous input which when active transfers data from the input latch to the DAC latch.
18	V_{DD}	Positive Supply Voltage.
19	R_{FB}	Feedback Resistor. This allows access to the amplifier's feedback loop.
20	V_{OUT}	Output Voltage. Three different output voltage ranges can be chosen: 0 to +5V, 0 to +10V or −5V to +5V.

AD7248 PIN CONFIGURATIONS

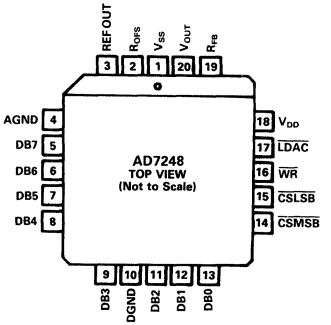
DIP



LCCC

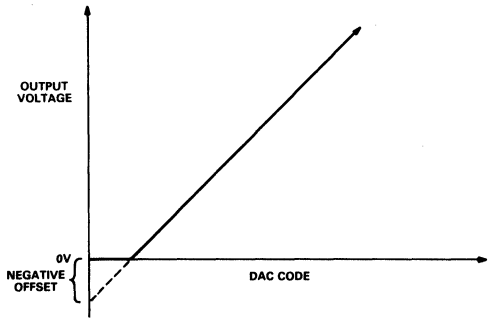


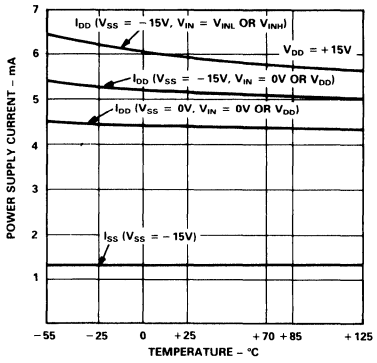
PLCC



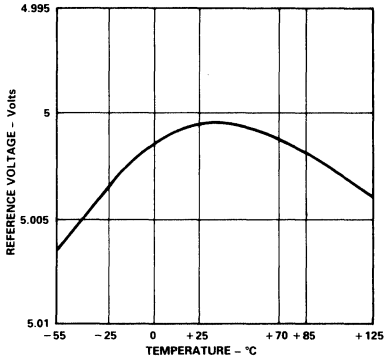
SINGLE SUPPLY LINEARITY AND GAIN ERROR

The output amplifier of the AD7245/AD7248 can have a true negative offset even when the part is operated from a single positive power supply. However, because the lower supply rail to the part is 0V, the output voltage cannot actually go negative. Instead the output voltage sits on the lower rail and this results in the transfer function shown across. This is an offset effect and the transfer function would have followed the dotted line if the output voltage could have gone negative. Normally, linearity is measured after offset and full scale have been adjusted or allowed for. On the AD7245/AD7248 the negative offset is allowed for by calculating the linearity from the code which the amplifier comes off the lower rail. This code is given by the negative offset specification. For example, the single supply linearity specification applies between Code 3 and Code 4095 for the 25°C specification and between Code 5 and Code 4095 over the T_{min} to T_{max} temperature range. Since gain error is also measured after offset has been allowed for, it is calculated between the same codes as the linearity error. Bipolar linearity and gain error are measured between Code 0 and Code 4095.

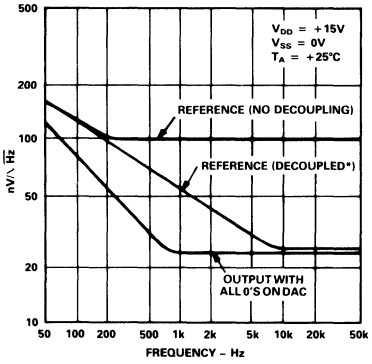




Power Supply Current vs. Temperature

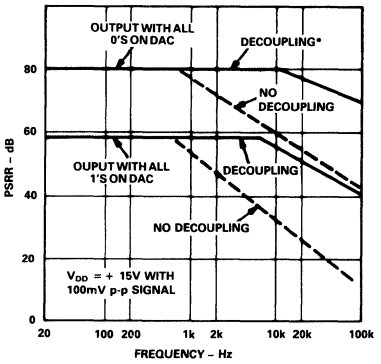


Reference Voltage vs. Temperature



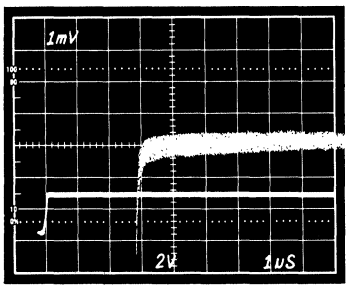
*REFERENCE DECOUPLING COMPONENTS AS PER FIGURE 8

Noise Spectral Density vs. Frequency

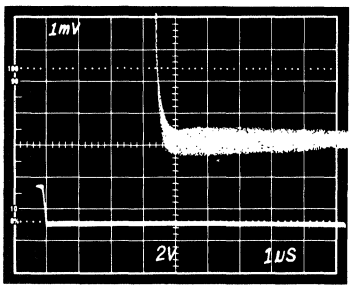


*POWER SUPPLY DECOUPLING CAPACITORS ARE 10μF and 0.1μF

Power Supply Rejection Ratio vs. Frequency



Positive-Going Settling Time (V_{DD} = +15V, V_{SS} = −15V)



Negative-Going Settling Time (V_{DD} = +15V, V_{SS} = −15V)

CIRCUIT INFORMATION

D/A SECTION

The AD7245/AD7248 contains a 12-bit voltage-mode digital-to-analog converter. The output voltage from the converter has the same positive polarity as the reference voltage allowing single supply operation. The reference voltage for the DAC is provided by an on-chip buried-Zener diode.

The DAC consists of a highly stable, thin-film, R-2R ladder and twelve high-speed NMOS single-pole, double-throw switches. The simplified circuit diagram for this DAC is shown in Figure 1.

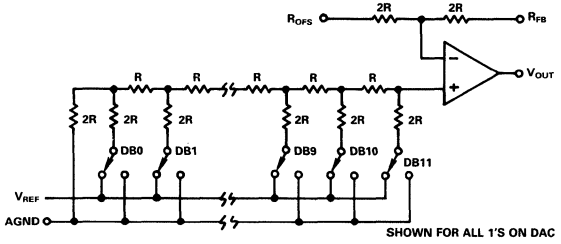


Figure 1. D/A Simplified Circuit Diagram

The input impedance of the DAC is code dependent and can vary from 8kΩ to infinity. The input capacitance also varies with code, typically from 50pF to 200pF.

OP AMP SECTION

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The user has access to two gain setting resistors which can be connected to allow different output voltage ranges (discussed later). The buffer amplifier is capable of developing up to 10V across a 2kΩ load to GND.

The output amplifier can be operated from a single positive power supply by tying V_{SS} = AGND = 0V. The amplifier can also be operated from dual supplies to allow a bipolar output range of −5V to +5V. *The amplifier should not be configured for the 0 to +10V output range when V_{SS} is more negative than −5V.* For dual supply operation on this range a V_{SS} of −5V should be applied to the part. The advantage of having dual supplies for the unipolar output ranges are faster settling time to voltages near 0V, full-sink capability of 2.5mA maintained over the entire output range and elimination of the effects of negative offset on the transfer characteristic (outlined previously). Figure 2 shows the sink capability of the amplifier for single supply operation.

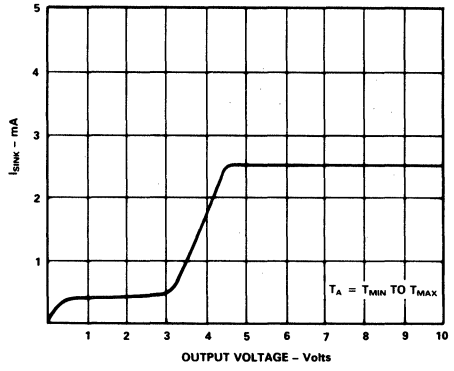


Figure 2. Typical Single Supply Sink Current vs. Output Voltage

The small-signal (200mV p-p) bandwidth of the output buffer amplifier is typically 1MHz. The output noise from the amplifier is low with a figure of 25nV/$\sqrt{Hz}$ at a frequency of 1kHz. The broadband noise from the amplifier has a typical peak-to-peak figure of 150μV for a 1MHz output bandwidth. There is no significant difference in the output noise between single and dual supply operation.

VOLTAGE REFERENCE

The AD7245/AD7248 contains an internal low-noise buried-Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. The reference is internally connected to the DAC. Since the DAC has a variable input impedance at its reference input the Zener diode reference is buffered. This buffered reference is available to the user to drive the circuitry required for bipolar output ranges. It can be used as a reference for other parts in the system provided it is externally buffered. The reference will give long-term stability comparable with the best discrete Zener reference diodes. The performance of the AD7245/AD7248 is specified with internal reference, and all the testing and trimming is done with this reference. The reference should be decoupled at the REF OUT pin and recommended decoupling components are 10μF and 0.1μF capacitors in series with a 10Ω resistor. A simplified schematic of the reference circuitry is shown in Figure 3.

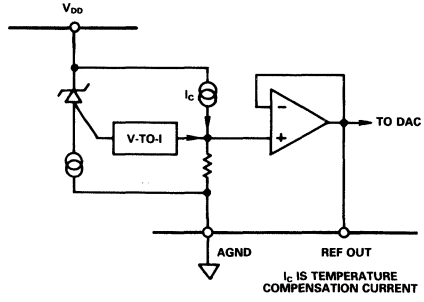


Figure 3. Internal Reference

DIGITAL SECTION

The AD7245/AD7248 digital inputs are compatible with either TTL or 5V CMOS levels. All data inputs are static-protected MOS gates with typical input currents of less than 1nA. The control inputs sink higher currents (150μA max) as a result of the fast digital interfacing. Internal input protection of all logic inputs is achieved by on-chip distributed diodes.

The AD7245/AD7248 features a very low digital feedthrough figure of 10nV secs in a 5V output range. This is due to the voltage-mode configuration of the DAC. Most of the impulse is actually as a result of feedthrough across the package. Normally, ceramic packages show more feedthrough than the other packages because of the metal lid. However, on the AD7245, the lid of the ceramic package is connected to DGND (Pin 12), and this reduces the feedthrough. The AD7248 metal lid is not connected to DGND on the package, but this can be done externally to reduce the feedthrough.

INTERFACE LOGIC INFORMATION – AD7245

Table I shows the truth table for AD7245 operation. The part contains two 12-bit latches, an input latch and a DAC latch. $\overline{CS}$ and $\overline{WR}$ control the loading of the input latch while $\overline{LDAC}$ controls the transfer of information from the input latch to the DAC latch. All control signals are level-triggered; and therefore either or both latches may be made transparent, the input latch by keeping $\overline{CS}$ and $\overline{WR}$ "LOW", the DAC latch by keeping $\overline{LDAC}$ "LOW". Input data is latched on the rising edge of $\overline{WR}$.

The data held in the DAC latch determines the analog output of the converter. Data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. This $\overline{LDAC}$ signal is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. For example, if $\overline{LDAC}$ goes LOW while $\overline{WR}$ is "LOW", then the $\overline{LDAC}$ signal must stay LOW for t_7 or longer after $\overline{WR}$ goes high to ensure correct data is latched through to the output.

$\overline{CLR}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Latches are Transparent
H	H	H	X	Both Latches are Latched
H	H	X	H	Both Latches are Latched
H	H	L	L	Input Latches Transparent
H	H	↓	L	Input Latches Latched
H	L	H	H	DAC Latches Transparent
H	↓	H	H	DAC Latches Latched
L	X	X	X	DAC Latches Loaded with all 0s
↓	H	H	H	DAC Latches Latched with All 0s and Output Remains at 0V or −5V
↓	L	L	L	Both Latches are Transparent and Output Follows Input Data

H = High State L = Low State X = Don't Care

Table I. AD7245 Truth Table

The contents of the DAC latch are reset to all 0s by a low level on the $\overline{CLR}$ line. With both latches transparent, the $\overline{CLR}$ line functions like a zero override with the output brought to 0V in the unipolar mode and −5V in the bipolar mode for the duration of the $\overline{CLR}$ pulse. If both latches are latched, a "LOW" pulse on the $\overline{CLR}$ input latches all 0s into the DAC latch and the output remains at 0V (or −5V) after the $\overline{CLR}$ line has returned "HIGH". The $\overline{CLR}$ line can be used to ensure powerup to 0V on the AD7245 output in unipolar operation and is also useful, when used as a zero override, in system calibration cycles.

Figure 4 shows the input control logic for the AD7245 and the write cycle timing for the part is shown in Figure 5.

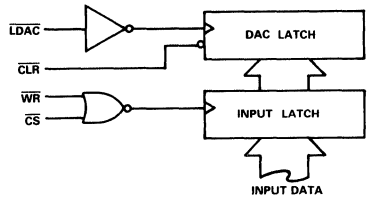


Figure 4. AD7245 Input Control Logic

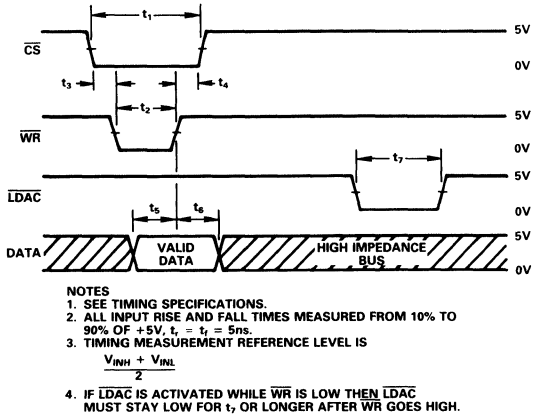


Figure 5. AD7245 Write-Cycle Timing Diagram

INTERFACE LOGIC INFORMATION – AD7248

The input loading structure on the AD7248 is configured for interfacing to microprocessors with an 8-bit-wide data bus. The part contains two 12-bit latches – an input latch and a DAC latch. Only the data held in the DAC latch determines the analog output from the converter. The truth table for AD7248 operation is shown in Table II, while the input control logic diagram is shown in Figure 6.

$\overline{CSMSB}$, $\overline{CSLSB}$ and $\overline{WR}$ control the loading of data from the external data bus to the input latch. The eight data inputs on the AD7248 accept right-justified data. This data is loaded to the input latch in two separate write operations. $\overline{CSLSB}$ and $\overline{WR}$ control the loading of the lower 8-bits into the 12-bit-wide latch. The loading of the upper 4-bit nibble is controlled by $\overline{CSMSB}$ and $\overline{WR}$. All control inputs are level triggered, and input data for either the lower byte or upper 4-bit nibble is latched into the input latches on the rising edge of $\overline{WR}$ (or either $\overline{CSMSB}$ or $\overline{CSLSB}$). The order in which the data is loaded to the input latch (i.e., lower byte or upper 4-bit nibble first) is not important.

The $\overline{LDAC}$ input controls the transfer of 12-bit data from the input latch to the DAC latch. This $\overline{LDAC}$ signal is also level triggered, and data is latched into the DAC latch on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ input is asynchronous and independent of $\overline{WR}$. This is useful in many applications especially in the simultaneous updating of multiple AD7248 outputs. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that

incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ goes low while $\overline{WR}$ and either $\overline{CS}$ input are low (or $\overline{WR}$ and either $\overline{CS}$ go low while $\overline{LDAC}$ is low), then the $\overline{LDAC}$ signal must stay low for t_7 or longer after $\overline{WR}$ returns high to ensure correct data is latched through to the output. The write cycle timing diagram for the AD7248 is shown in Figure 7.

An alternate scheme for writing data to the AD7248 is to tie the $\overline{CSMSB}$ and $\overline{LDAC}$ inputs together. In this case exercising $\overline{CSLSB}$ and $\overline{WR}$ latches the lower 8 bits into the input latch. The second write, which exercises $\overline{CSMSB}$, $\overline{WR}$ and $\overline{LDAC}$ loads the upper 4-bit nibble to the input latch and at the same time transfers the 12-bit data to the DAC latch. This automatic transfer mode updates the output of the AD7248 in two write operations. This scheme works equally well for $\overline{CSLSB}$ and $\overline{LDAC}$ tied together provided the upper 4-bit nibble is loaded to the input latch followed by a write to the lower 8 bits of the input latch.

$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	Function
L	H	L	H	Loads LS Byte into Input Latch
L	H	↓	H	Latches LS Byte into Input Latch
↓	H	L	H	Latches LS Byte into Input Latch
H	L	L	H	Loads MS Nibble into Input Latch
H	L	↓	H	Latches MS Nibble into Input Latch
H	↓	L	H	Latches MS Nibble into Input Latch
H	H	H	L	Loads Input Latch into DAC Latch
H	H	H	↓	Latches Input Latch into DAC Latch
H	L	L	L	Loads MS Nibble into Input Latch and Loads Input Latch into DAC Latch
H	H	H	H	No Data Transfer Operation

H = High State L = Low State

Table II. AD7248 Truth Table

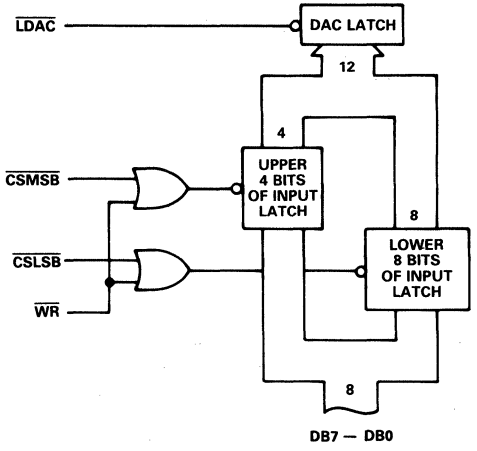


Figure 6. AD7248 Input Control Logic

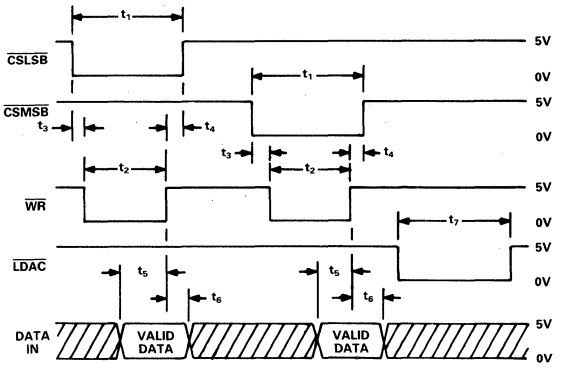


Figure 7. AD7248 Write Cycle Timing Diagram

APPLYING THE AD7245/AD7248

The internal scaling resistors provided on the AD7245/AD7248 allow several output voltage ranges. The part can produce unipolar output ranges of 0V to +5V or 0V to +10V and a bipolar output range of −5V to +5V. Connections for the various ranges are outlined below.

UNIPOLAR (0V to +10V) CONFIGURATION

The first of the configurations provides an output voltage range of 0V to +10V. This is achieved by connecting the bipolar offset resistor, R_{OFS}, to AGND and connecting R_{FB} to V_{OUT}. In this configuration the AD7245/AD7248 can be operated single supply (V_{SS} = 0V = AGND). If dual supply performance is required, a V_{SS} of −5V should be applied. Note that a V_{SS} supply more negative than −5V should not be applied to the AD7245/AD7248 when it is configured for a 0 to +10V output range. Figure 8 shows the connection diagram for unipolar operation while the table for output voltage versus the digital code in the DAC latch is shown in Table III.

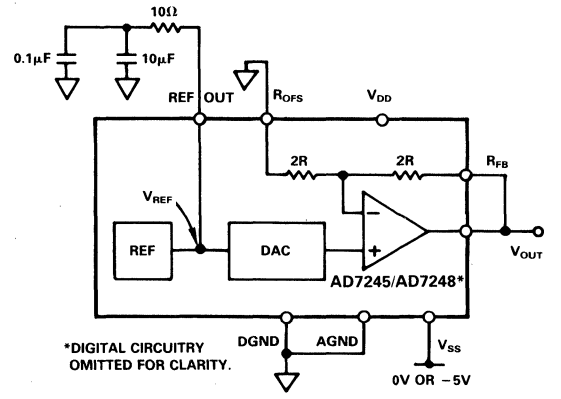


Figure 8. Unipolar (0 to +10V) Configuration

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+2 \cdot V_{REF} \cdot \left(\frac{4095}{4096}\right)$
1000 0000 0001	$+2 \cdot V_{REF} \cdot \left(\frac{2049}{4096}\right)$
1000 0000 0000	$+2 \cdot V_{REF} \cdot \left(\frac{2048}{4096}\right) = +V_{REF}$
0111 1111 1111	$+2 \cdot V_{REF} \cdot \left(\frac{2047}{4096}\right)$
0000 0000 0001	$+2 \cdot V_{REF} \cdot \left(\frac{1}{4096}\right)$
0000 0000 0000	0V

NOTE: $1LSB = 2 \cdot V_{REF}(2^{-12}) = V_{REF}\left(\frac{1}{2048}\right)$

Table III. Unipolar Code Table (0V to +10V Range)

UNIPOLAR (0V to +5V) CONFIGURATION

The 0V to +5V output voltage range is achieved by tying R_{OFS}, R_{FB} and V_{OUT} together. For this output range the AD7245/AD7248 can be operated single supply (V_{SS} = 0V) or dual supply. The table for output voltage versus digital code is as in Table III, with $2 \cdot V_{REF}$ replaced by V_{REF}. Note that for this range

$$1LSB = V_{REF}(2^{-12}) = V_{REF} \cdot \frac{1}{4096}.$$

BIPOLAR CONFIGURATION

The bipolar configuration for the AD7245/AD7248, which gives an output voltage range from −5V to +5V, is achieved by connecting the R_{OFS} input to REF OUT and connecting R_{FB} and V_{OUT}. The AD7245/AD7248 must be operated from dual supplies to achieve this output voltage range. The code table for bipolar operation is shown in Table IV.

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{REF} \cdot \left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF} \cdot \left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF} \cdot \left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF} \cdot \left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF} \cdot \left(\frac{2048}{2048}\right) = -V_{REF}$

NOTE: $1LSB = 2 \cdot V_{REF}(2^{-11}) = V_{REF}\left(\frac{1}{2048}\right)$

Table IV. Bipolar Code Table

AGND BIAS

The AD7245/AD7248 AGND pin can be biased above system GND (AD7245/AD7248 DGND) to provide an offset "zero" analog output voltage level. With unity gain on the amplifier ($R_{OFS} = V_{OUT} = R_{FB}$) the output voltage, V_{OUT} is expressed as:

$$V_{OUT} = V_{BIAS} + D \cdot V_{REF}$$

where D is a fractional representation of the digital word in the DAC latch and V_{BIAS} is the voltage applied to the AD7245/AD7248 AGND pin.

Because the current flowing out of the AGND pin varies with digital code, the AGND pin should be driven from a low impedance source. A circuit configuration is outlined for AGND bias in Figure 9 using the AD589, a +1.23V bandgap reference.

If a gain of 2 is used on the buffer amplifier the output voltage, V_{OUT} is expressed as

$$V_{OUT} = 2(V_{BIAS} + D \cdot V_{REF})$$

In this case care must be taken to ensure that the maximum output voltage is not greater than V_{DD} −3V. The $V_{DD} - V_{OUT}$ overhead must be greater than 3V to ensure correct operation of the part. Note that V_{DD} and V_{SS} for the AD7245/AD7248 must be referenced to DGND (system GND). The entire circuit can be operated in single supply with the V_{SS} pin of the AD7245/AD7248 connected to system GND.

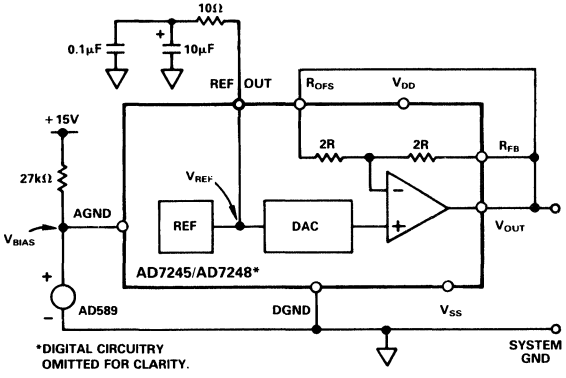


Figure 9. AGND Bias Current

PROGRAMMABLE CURRENT SINK

Figure 10 shows how the AD7245/AD7248 can be configured with a power MOSFET transistor, the VN0300M, to provide a

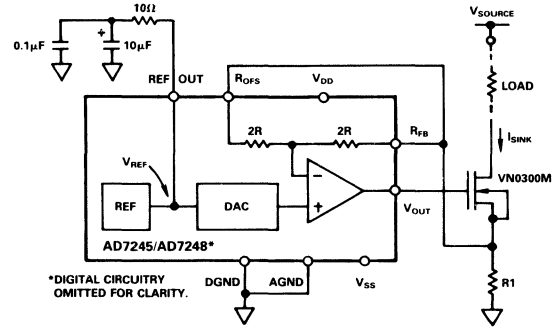


Figure 10. Programmable Current Sink

programmable current sink from V_{DD} or V_{SOURCE}. The VN0300M is placed in the feedback of the AD7245/AD7248 amplifier. The entire circuit can be operated in single supply by tying the V_{SS} of the AD7245/AD7248 to AGND. The sink current, I_{SINK}, can be expressed as:

$$I_{SINK} = \frac{D \cdot V_{REF}}{R1}$$

Using the VN0300M, the voltage drop across the load can typically be as large as (V_{SOURCE} −6V) with V_{OUT} of the DAC at +5V. Therefore, for a current of 50mA flowing in the R1 (with all 1s in the DAC register) the maximum load is 200Ω with V_{SOURCE} = +15V. The VN0300M can actually handle currents up to 500mA and still function correctly in the circuit, but in practice the circuit must be used with larger values of V_{SOURCE} otherwise it requires a very small load.

Since the tolerance value on the reference voltage of the AD7245/AD7248 is ±0.2%, then the absolute value of I_{SINK} can vary by ±0.2% from device to device for a fixed value of R1.

Because the input bias current of the AD7245/AD7248's op amp is only of the order of pA's, its effect on the sink current is negligible. Tying the R_{OFS} input to the R_{FB} input reduces this effect even further and prevents noise pickup which could occur if the R_{OFS} pin was left unconnected.

The circuit of Figure 10 can be modified to provide a programmable current source to AGND or $-V_{SINK}$ (for $-V_{SINK}$, dual supplies are required on the AD7245/AD7248). The AD7245/AD7248 is configured as before. The current through R1 is mirrored with a current mirror circuit to provide the programmable source current (see CMOS DAC Application Guide, Publication No. G872-30-10/84, for suitable current mirror circuit). As before the absolute value of the source current will be affected by the ±0.2% tolerance on V_{REF}. In this case the performance of the current mirror will also affect the value of the source current.

FUNCTION GENERATOR WITH PROGRAMMABLE FREQUENCY

Figure 11 shows how the AD7245/AD7248 can be configured with the AD537, voltage-to-frequency converter and the AD639, trigonometric function generator to provide a complete function generator with programmable frequency. The circuit provides square-wave, triwave and sinewave outputs, each output of ±10V amplitude.

The AD7245/AD7248 provides a programmable voltage to the AD537 input. Since both the AD7245/AD7248 and AD537 are guaranteed monotonic, the output frequency will always increase with increasing digital code. The AD537 provides a square-wave output which is conditioned for ±10V by amplifier A1. The AD537 also provides a differential triwave output. This is conditioned by amplifiers A2 and A3 to provide the ±1.8V triwave required at the input of the AD639. The triwave is further scaled by amplifier A4 to provide a ±10V output.

Adjusting the triwave applied to the AD639 adjusts the distortion performance of the sine wave output, (+10V in configuration shown). Amplitude, offset and symmetry of the triwave can affect the distortion. By adjusting these, via VR1 and VR2, an output sine wave with harmonic distortion of better than −50dB can be achieved at low and intermediate frequencies.

Using the capacitor value shown in Figure 11 for C_F (i.e. 680pF) the output frequency range is 0 to 100kHz over the digital input code range. The step size for frequency increments is 25Hz. The accuracy of the output frequency is limited to 8 or 9 bits by the AD537, but it is guaranteed monotonic to 12 bits.

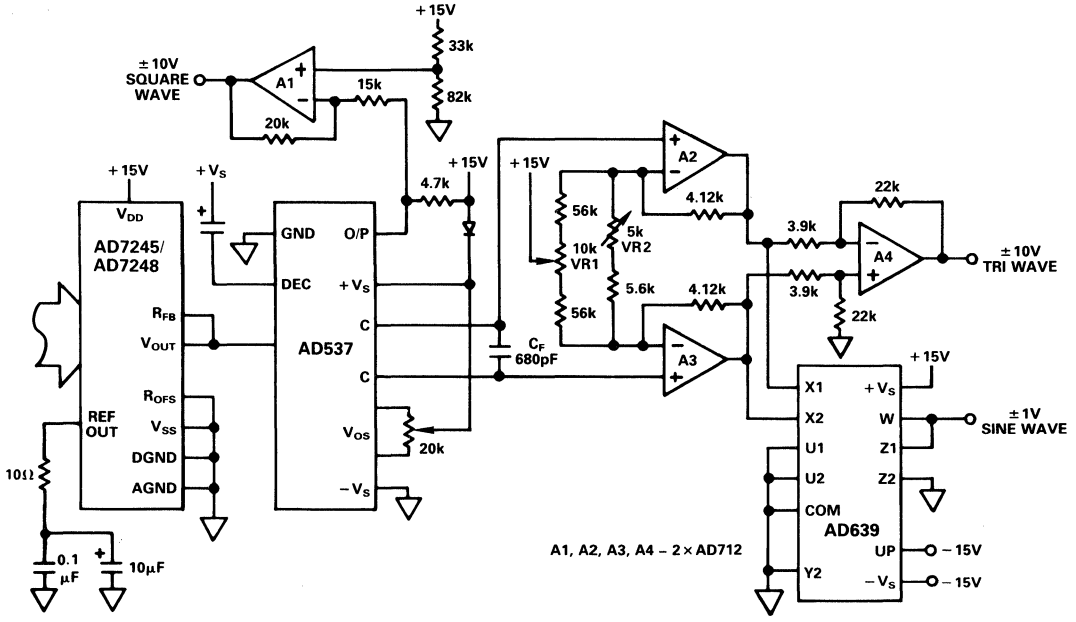


Figure 11. Programmable Function Generator

MICROPROCESSOR INTERFACING – AD7245

AD7245 – 8086A INTERFACE

Figure 12 shows the 8086 16-bit processor interfacing to the AD7245. In the setup shown the double-buffering feature of the DAC is not used and the $\overline{LDAC}$ input is tied LOW. AD0-AD11 of the 16-bit data bus are connected to the AD7245 data bus (DB0-DB11). The 12-bit word is written to the AD7245 in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 12 is given in Table V.

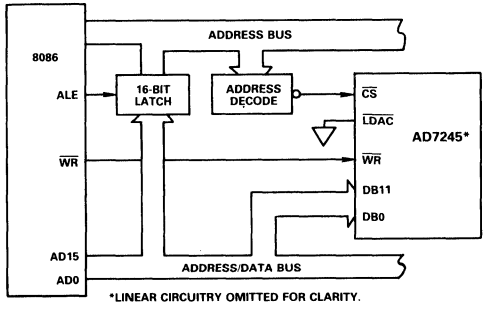


Figure 12. AD7245 to 8086 Interface

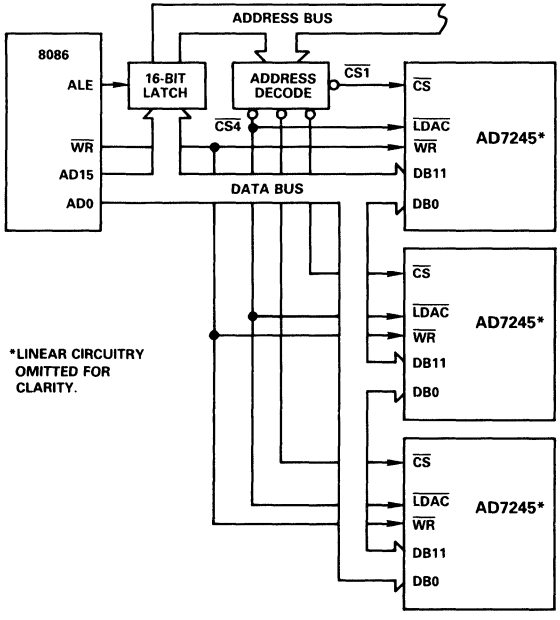


Figure 13. AD7245 to 8086 Multiple DAC Interface

```
                ASSUME DS : DACLOAD, CS : DACLOAD
                DACLOAD SEGMENT AT 000

00  8CC9        MOV CX,     : DEFINE DATA SEGMENT
                CS            REGISTER
02  8ED9        MOV DS,     : EQUAL TO CODE
                CX            SEGMENT REGISTER
04  BF00D0      MOV DI,     : LOAD DI WITH D000
                #D000
07  C705        MOV MEM,    : DAC LOADED WITH WXYZ
    "YZWX"      #YZWX
0B  EA00 00                 : CONTROL IS RETURNED TO
0E  00 FF                     THE MONITOR PROGRAM
```

Table V. Sample Program for Loading AD7245 from 8086

In a multiple DAC system the double-buffering of the AD7245 allows the user to simultaneously update all DACs. In Figure 13, a 12-bit word is loaded to the input latches of each of the DACs in sequence. Then, with one instruction to the appropriate address, $\overline{CS4}$ (i.e., $\overline{LDAC}$) is brought LOW, updating all the DACs simultaneously.

AD7245 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7245 is accomplished using the circuit of Figure 14. Once again the AD7245 is used in the single-buffered mode. A software routine for loading data to the AD7245 is given in Table VI. In this example the AD7245 is located at address E000, and the 12-bit word is written to the DAC in one MOVE instruction.

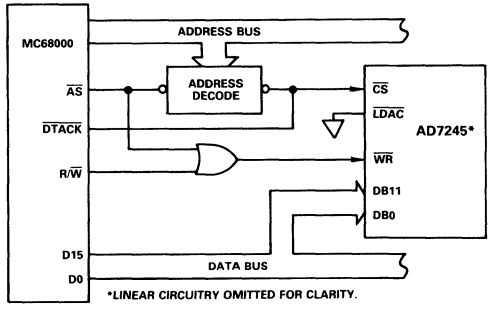


Figure 14. AD7245 to 68000 Interface

01000	MOVE.W	#X,D0	The desired DAC data, X, is loaded into Data Register 0. X may be any value between 0 and 4095 (decimal) or 0 and OFFF (hexadecimal).
	MOVE.W	D0,$E000	The Data X is transferred between D0 and the DAC Latch.
	MOVE.B	#228,D7	Control is returned to the System Monitor Program using these two instructions.
	TRAP	#14	

Table VI. Sample Routine for Loading AD7245 from 68000

MICROPROCESSOR INTERFACING – AD7248

Figure 15 shows the connection diagram for interfacing the AD7248 to both the 8085A and 8088 microprocessors. This scheme is also suited to the Z80 microprocessor, but the Z80 address/data bus does not have to be demutiplexed. Data to be loaded to the AD7248 is right-justified. The AD7248 is memory mapped with a separate memory address for the input latch high byte, the input latch low byte and the DAC latch. Data is first written to the AD7248 input latch in two write operations. Either the high byte or the low byte data can be written first to the AD7248 input latch. A write to the AD7248 DAC latch address transfers the input latch data to the DAC latch and updates the output voltage. Alternatively, the $\overline{LDAC}$ input can be asynchronous or can be common to a number of AD7248s for simultaneous updating of a number of voltage channels.

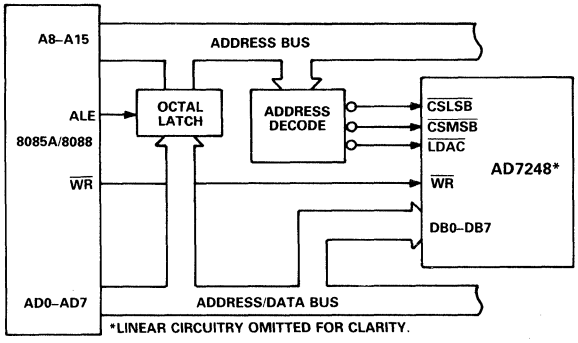


Figure 15. AD7248 to 8085A/8088 Interface

A connection diagram for the interface between the AD7248 and 68008 microprocessor is shown in Figure 16. Once again, the AD7248 acts as a memory mapped device and data is right-justified. In this case the AD7248 is configured in the automatic transfer mode which means that the high byte of the input latch has the same address as the DAC latch. Data is written to the AD7248 by first writing data to the AD7248 low byte. Writing data to the high byte of the input latch also transfers the input latch contents to the DAC latch and updates the output.

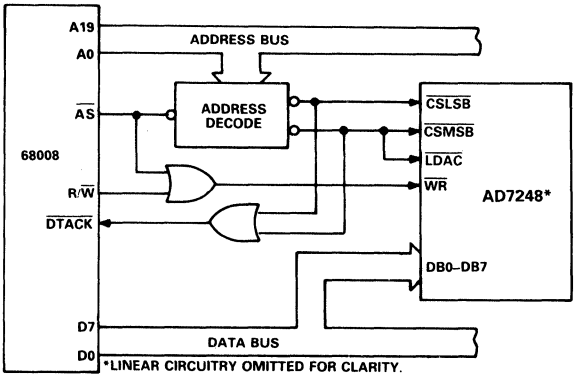


Figure 16. AD7248 to 68008 Interface

An interface circuit for connections to the 6502 or 6809 microprocessors is shown in Figure 17. Once again, the AD7248 is memory mapped and data is right-justified. The procedure for writing data to the AD7248 is as outlined for the 8085A/8088. For the 6502 microprocessor the $\phi 2$ clock is used to generate the $\overline{WR}$, while for the 6809 the E signal is used.

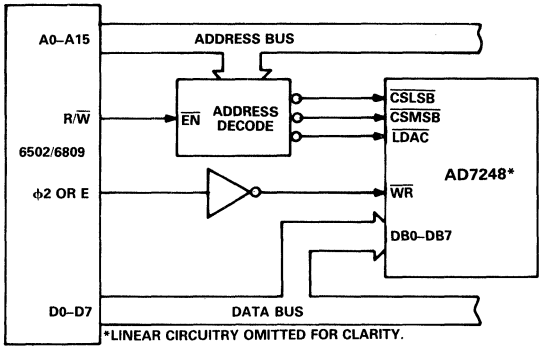


Figure 17. AD7248 to 6502/6809 Interface

Figure 18 shows a connection diagram between the AD7248 and the 8051 microprocessor. The AD7248 is port mapped in this interface and is configured in the automatic transfer mode. Data to be loaded to the input latch low byte is output to Port 1. Output Line P3.0, which is connected to $\overline{CSLSB}$ of the AD7248, is pulsed to load data into the low byte of the input latch. Pulsing the P3.1 line, after the high byte data has been set up on Port 1, updates the output of the AD7248. The $\overline{WR}$ input of the AD7248 can be hardwired low in this application because spurious address strobes on $\overline{CSLSB}$ and $\overline{CSMSB}$ do not occur.

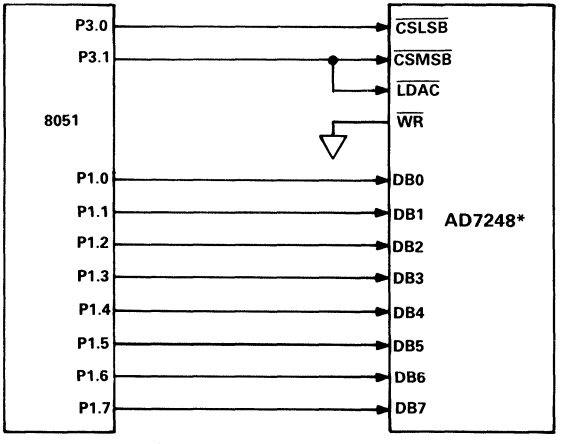


Figure 18. AD7248 to MCS-51 Interface

ANALOG DEVICES

CMOS 8-Bit Buffered Multiplying DAC

AD7524

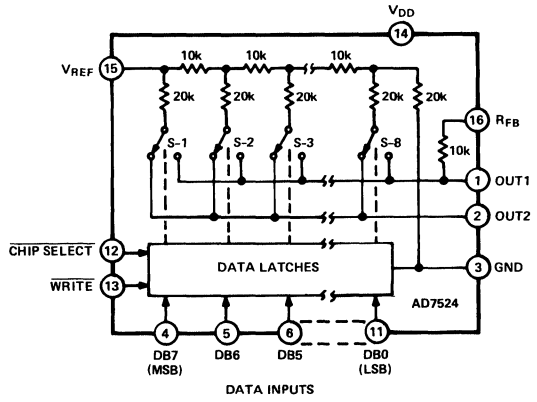
FEATURES

- Microprocessor Compatible (6800, 8085, Z80, Etc.)
- TTL/CMOS Compatible Inputs
- On-Chip Data Latches
- End Point Linearity
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Latch Free (No Protection Schottky Required)

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits
- Bus Structured Instruments

AD7524 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5V to +15V, the AD7524 interfaces directly to most microprocessor buses or output ports.

Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

ORDERING INFORMATION[1]

Nonlinearity (V_{DD} = +15V)	Temperature Range and Package Options[2,3] −40°C to +85°C	−40°C to +85°C	−55°C to +125°C
	Plastic DIP (N-16)	**Hermetic (Q-16)**	**Hermetic (Q-16)**
±1/2LSB	AD7524JN	AD7524AQ	AD7524SQ
±1/4LSB	AD7524KN	AD7524BQ	AD7524TQ
±1/8LSB	AD7524LN	AD7524CQ	AD7524UQ
	PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
±1/2LSB	AD7524JP		AD7524SE
±1/4LSB	AD7524KP		AD7524TE
±1/8LSB	AD7524LP		AD7524UE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC drawing #5962-87700.
[2]See Section 14 for package outline information.
[3]Also available in SOIC package (AD7524JR).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

PARAMETER	LIMIT, T_A = +25°C V_{DD} = +5V	LIMIT, T_A = +25°C V_{DD} = +15V	LIMIT, T_{MIN}, T_{MAX}[1] V_{DD} = 5V	LIMIT, T_{MIN}, T_{MAX}[1] V_{DD} = +15V	UNITS	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE						
Resolution		8	8	8	Bits	
Relative Accuracy						
J, A, S Versions	±1/2	±1/2	±1/2	±1/2	LSB max	
K, B, T Versions	±1/2	±1/4	±1/2	±1/4	LSB max	
L, C, U Versions	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	guaranteed	guaranteed	guaranteed	guaranteed		
Gain Error[2]	±2 1/2	±1 1/4	±3 1/2	±1 1/2	LSB max	
Average Gain TC[3]	±40	±10	±40	±10	ppm/°C	Gain TC measured from +25°C to T_{min} or from +25°C to T_{max}
dc Supply Rejection,[3] $\Delta Gain/\Delta V_{DD}$	0.08 0.002	0.02 0.001	0.16 0.01	0.04 0.005	% FSR/% max % FSR/% typ	ΔV_{DD} = ±10%
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
DYNAMIC PERFORMANCE						
Output Current Settling Time[3] (to 1/2 LSB)	400	250	500	350	ns max	OUT1 Load = 100Ω, C_{EXT} = 13pF; $\overline{WR}$, $\overline{CS}$ = 0V; DB0–DB7 = 0V to V_{DD} to 0V.
ac Feedthrough[3]						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10V, 100kHz sine wave; DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
at OUT2	0.25	0.25	0.5	0.5	% FSR max	
REFERENCE INPUT						
R_{IN} (pin 15 to GND)[4]	5 20	5 20	5 20	5 20	kΩ min kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (pin 1)	120	120	120	120	pF max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	30	30	30	30	pF max	
C_{OUT1} (pin 1)	30	30	30	30	pF max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement V_{IH}	+2.4	+13.5	+2.4	+13.5	V min	
Input LOW Voltage Requirement V_{IL}	+0.8	+1.5	+0.8	+1.5	V max	
Input Current I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]						
DB0–DB7	5	5	5	5	pF max	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	20	20	20	20	pF max	V_{IN} = 0V
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time[5] t_{CS}						See timing diagram $t_{WR} = t_{CS}$
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Chip Select to Write Hold Time t_{CH}						
All Grades	0	0	0	0	ns min	
Write Pulse Width t_{WR}						$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Data Setup Time t_{DS}						
AD7524J, K, L, A, B, C	135	60	170	80	ns min	
AD7524S, T, U	135	60	170	100	ns min	
Data Hold Time t_{DH}						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1 100	2 100	2 500	2 500	mA max μA max	All Digital Inputs V_{IL} or V_{IH} All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature ranges as follows: J, K, L versions: -40°C to +85°C
A, B, C versions: -40°C to +85°C
S, T, U versions: -55°C to +125°C

[2] Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.

[3] Guaranteed, not tested.

[4] DAC thin-film resistor temperature coefficient is approximately -300ppm/°C.

[5] AC parameter, sample tested @ 25°C to ensure conformance to specifications.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
V_{RFB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage to GND	−0.3V to V_{DD} +0.3V
OUT1, OUT2 to GND	−0.3V to V_{DD} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Power Dissipation (Any Package)	
To +75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commerical (J, K, L)	−40°C to +85°C
Industrial (A, B, C)	−40°C to +85°C
Extended (S, T, U)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: A measure of the deviation from a straight line through the end points of the DAC transfer function. Normally expressed as a percentage of full scale range. For the AD7524 DAC, this holds true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

GAIN ERROR: Gain Error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in LSBs. Gain Error is adjustable to zero with an external potentiometer.

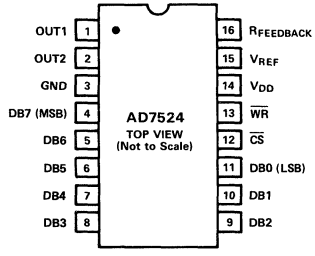
FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT1 and OUT2 terminals to ground.

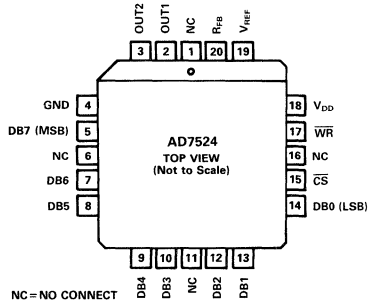
OUTPUT LEAKAGE CURRENT: Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage at the amplifier output.

PIN CONFIGURATIONS

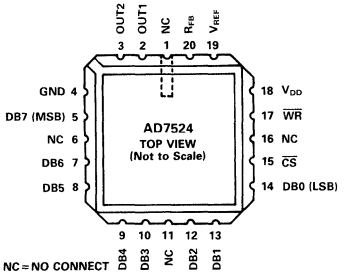
DIP



PLCC



LCCC



CIRCUIT DESCRIPTION

CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

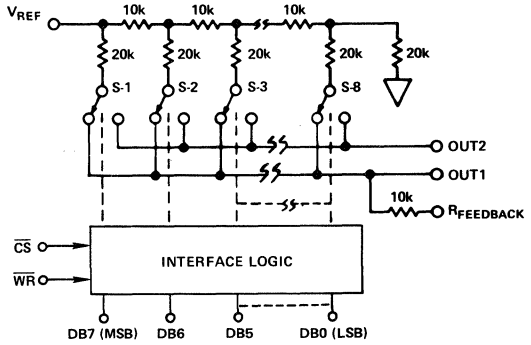


Figure 1. AD7524 Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit for all digital inputs LOW is shown in Figures 2. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{1}{256}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switches is 120pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 30pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high is similar to Figure 2 however, the "ON" switches are now on terminal OUT1, hence the 120pF appears at that terminal.

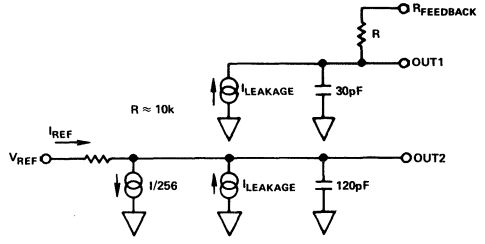


Figure 2. AD7524 DAC Equivalent Circuit – All Digital Inputs Low

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB0–DB7 data bus inputs. In this mode, the AD7524 acts like a nonlatched input D/A converter.

HOLD MODE

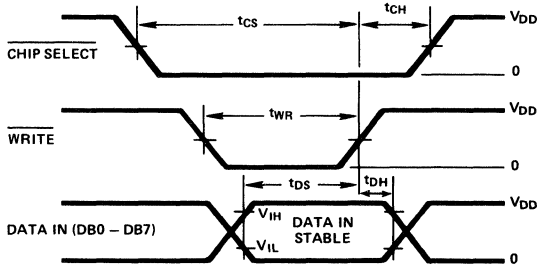
When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB0–DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the HIGH state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$
3. $t_{DS} + t_{DH}$ is approximately constant at 145ns min at +25°C, V_{DD} = +5V and t_{WR} = 170ns min. The AD7524 is specified for a minimum t_{DH} of 10ns, however, in applications where $t_{DH} > 10$ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65ns, t_{DH} = 80ns.

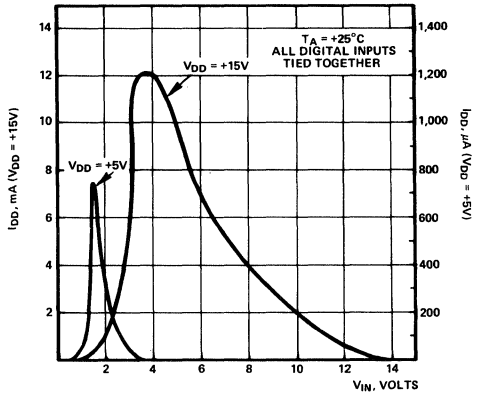


Figure 3. Supply Current vs. Logic Level

Typical plots of supply current, I_{DD}, versus logic input voltage, V_{IN}, for V_{DD} = +5V and V_{DD} = +15V are shown above.

ANALOG CIRCUIT CONNECTIONS

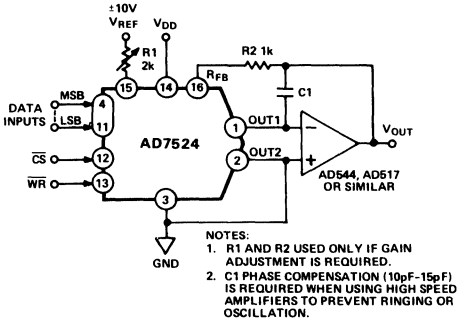


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

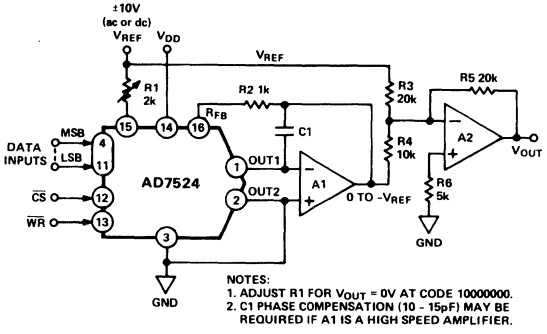


Figure 5. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$-V_{REF}\left(\frac{255}{256}\right)$
10000001		$-V_{REF}\left(\frac{129}{256}\right)$
10000000		$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111		$-V_{REF}\left(\frac{127}{256}\right)$
00000001		$-V_{REF}\left(\frac{1}{256}\right)$
00000000		$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

Table I. Unipolar Binary Code Table

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$+V_{REF}\left(\frac{127}{128}\right)$
10000001		$+V_{REF}\left(\frac{1}{128}\right)$
10000000		0
01111111		$-V_{REF}\left(\frac{1}{128}\right)$
00000001		$-V_{REF}\left(\frac{127}{128}\right)$
00000000		$-V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

Table II. Bipolar (Offset Binary) Code Table

MICROPROCESSOR INTERFACE

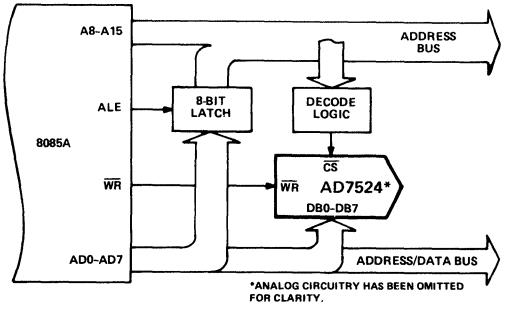


Figure 6. AD7524/8085A Interface

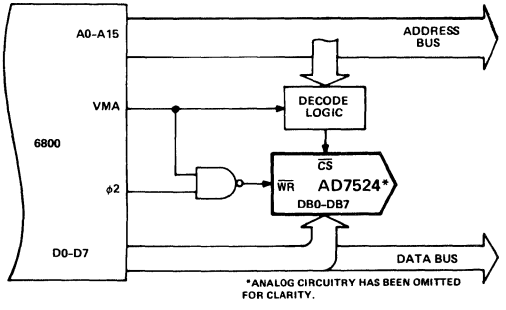
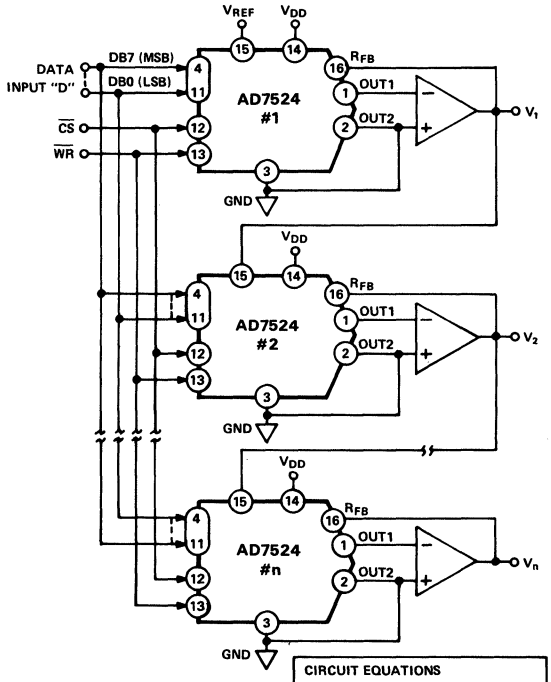


Figure 7. AD7524/MC6800 Interface

POWER GENERATION



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$

$V_2 = +(V_{REF})(D^2)$

$V_n = -(V_{REF})(D^n)$, n an odd integer

$V_n = +(V_{REF})(D^n)$, n an even integer

WHERE:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$$

and

$DB_n = 1$ or 0

CMOS Dual 8-Bit Buffered Multiplying DAC

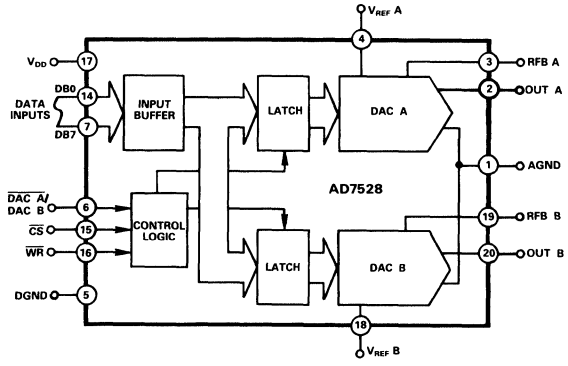
AD7528

FEATURES
- On-Chip Latches for Both DACs
- +5V to +15V Operation
- DACs Matched to 1%
- Four Quadrant Multiplication
- TTL/CMOS Compatible
- Latch Free (Protection Schottkys not Required)

APPLICATIONS

Digital Control of:
- Gain/Attenuation
- Filter Parameters
- Stereo Audio Circuits
- X–Y Graphics

AD7528 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3″ wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20mW of power.

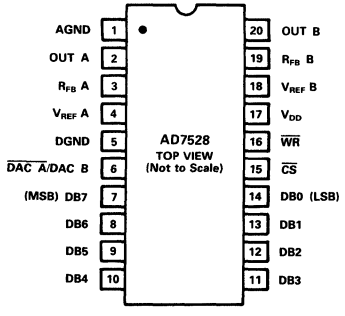
Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

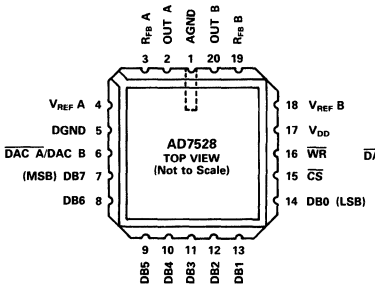
1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in either a small 20-pin 0.3″ wide DIP or in 20-terminal surface mount packages.

PIN CONFIGURATIONS

DIP



LCCC



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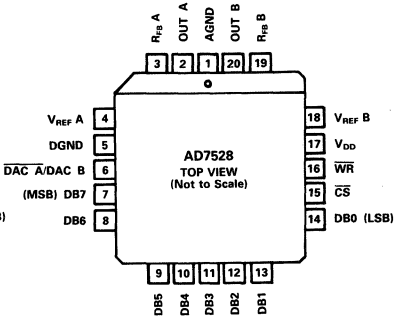


SPECIFICATIONS (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±1/2	±1/2	±1/2	±1/2	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111.
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 1 and 2.
Gain Temperature Coefficient[4]							
ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	All	8	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage							
V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage							
V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current							
I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	10	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, DAC A/DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time							
t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time							
t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time							
t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time							
t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time							
t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time							
t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended P.C. Board Layout and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME[2]	All	350	400	180	200	ns max	To 1/2LSB. Out A/Out B load = 100Ω. $\overline{WR}$ = $\overline{CS}$ = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10V OUT A, OUT B Load = 100Ω C_{EXT} = 13pF $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL TO ANALOG GLITCH IMPULSE	All	160	–	440	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT} A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT} B		50	50	50	50	pF max	
C_{OUT} A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT} B		120	120	120	120	pF max	
AC FEEDTHROUGH							
V_{REF} A to OUT A	All	−70	−65	−70	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave @ 100kHz
V_{REF} B to OUT B		−70	−65	−70	−65	dB max	
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	All	−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} B = 0V.
V_{REF} B to OUT A		−77	–	−77	–	dB typ	V_{REF} B = 20V p-p Sine Wave @ 100kHz V_{REF} A = 0V.
DIGITAL CROSSTALK	All	30	–	60	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	−85	–	−85	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES

[1]Temperature Ranges are J, K, L Versions; −40°C to +85°C
A, B, C Versions; −40°C to +85°C
S, T, U Versions; −55°C to +125°C

[2]Specification applies to both DACs in AD7528.

[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.

[4]Guaranteed by design but not production tested.

[5]These characteristics are for design guidance only and are not subject to test.

Specifications subject to change without notice.

INTERFACE LOGIC INFORMATION

DAC Selection:
Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:
Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:
When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{\text{DAC A}}$/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

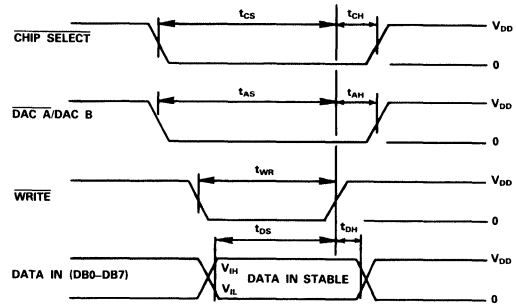
L = Low State H = High State X = Don't Care

Mode Selection Table

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}.
   V_{DD} = +5V, t_r = t_f = 20ns;
   V_{DD} = +15V, t_r = t_f = 40ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH}+V_{IL}}{2}$

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

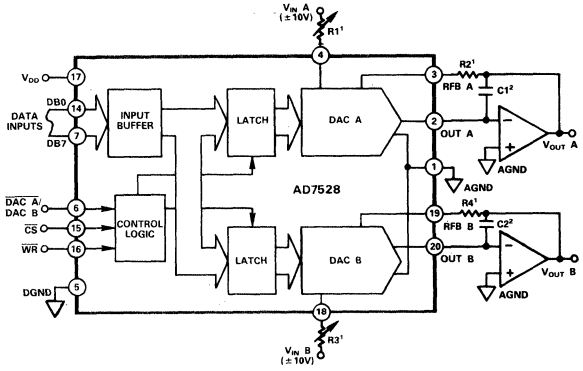
V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, L) Grades	−40°C to +85°C
Industrial (A, B, C) Grades	−40°C to +85°C
Extended (S, T, U) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

ORDERING INFORMATION[1]

Relative Accuracy	Gain Error T_A = +25°C	Temperature Range and Package Options[2,3] −40°C to +85°C	−40°C to +85°C	−55°C to +125°C
		Plastic DIP (N-20)	**Hermetic (Q-20)**	**Hermetic (Q-20)**
±1LSB	±4LSB	AD7528JN	AD7528AQ	AD7528SQ
±1/2LSB	±2LSB	AD7528KN	AD7528BQ	AD7528TQ
±1/2LSB	±1LSB	AD7528LN	AD7528CQ	AD7528UQ
		PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
±1LSB	±4LSB	AD7528JP		AD7528SE
±1/2LSB	±2LSB	AD7528KP		AD7528TE
±1/2LSB	±1LSB	AD7528LP		AD7528UE

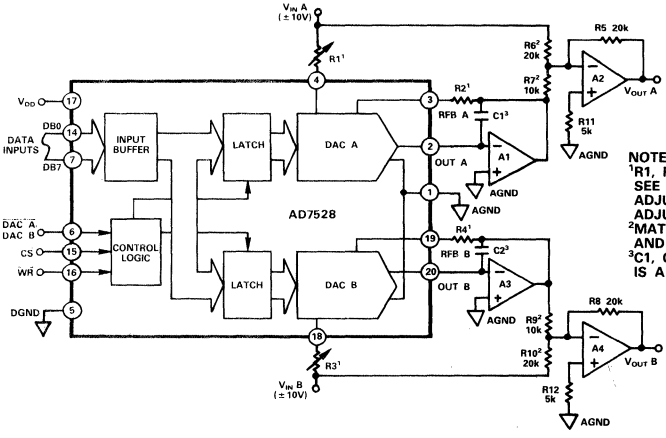
NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-87701.
[2]See Section 14 for package outline information.
[3]Also available in SOIC package (AD7528KR, AD7528LR).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

Applying the AD7528



NOTES:
¹R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
²C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 1. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table I.



NOTES:
¹R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH.
ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.
²MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
³C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BY REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER.

Figure 2. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table II.

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

Table I. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

Table II. Bipolar (Offset Binary) Code Table

Trim Resistor	J/A/S	K/B/T	L/C/U
R1;R3	1k	500	200
R2;R4	330	150	82

Table III. Recommended Trim Resistor Values vs. Grade

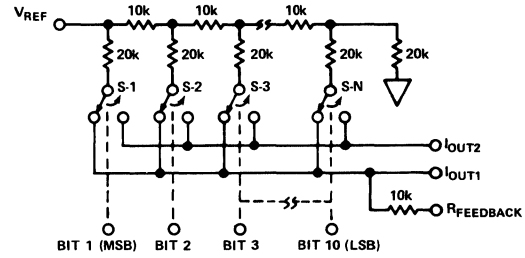
CMOS Low Cost 10-Bit Multiplying DAC

AD7533

FEATURES
- Lowest Cost 10-Bit DAC
- Low Cost AD7520 Replacement
- Linearity: 1/2, 1 or 2LSB
- Low Power Dissipation
- Full Four-Quadrant Multiplying DAC
- CMOS/TTL Direct Interface
- Latch Free (Protection Schottky not Required)
- End-Point Linearity

APPLICATIONS
- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control

AD7533 FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

ORDERING INFORMATION[1,2]

	Temperature Range and Package Options[3]		
Nonlinearity	−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
	Plastic DIP (N-16)	Hermetic (Q-16)	Hermetic (Q-16)
±0.2%	AD7533JN	AD7533AQ	AD7533SQ
±0.1%	AD7533KN	AD7533BQ	AD7533TQ
±0.05%	AD7533LN	AD7533CQ	AD7533UQ
	PLCC[4] (P-20A)		LCCC[5] (E-20A)
±0.2%	AD7533JP		AD7533SE
±0.1%	AD7533KP		AD7533TE
±0.05%	AD7533LP		AD7533UE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]Analog Devices reserves the right to ship ceramic (package outline D-16) packages in lieu of cerdip (package outline Q-16) packages.
[3]See Section 14 for package outline information.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS (V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy[1]			
AD7533JN, AD, SD, AQ, SQ	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD, BQ, TQ	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD, CQ, UQ	±0.05% FSR max	±0.05% FSR max	
Gain Error[2,3]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[4]			
$\Delta Gain/\Delta V_{DD}$	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1}	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2}	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[4]	800ns[5]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[5]	±0.1% FSR max[5]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sine wave.
REFERENCE INPUT			
Input Resistance (Pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[6]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1}	100pF max[5]	100pF max[5]	Digital Inputs = V_{INH}
C_{OUT2}	35pF max[5]	35pF max[5]	
C_{OUT1}	35pF max[5]	35pF max[5]	Digital Inputs = V_{INL}
C_{OUT2}	100pF max[5]	100pF max[5]	
DIGITAL INPUTS			
Input High Voltage			
V_{INH}	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	8pF max[5]	8pF max[5]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[5]	+5V to +16V	+5V to +16V	Functionality with Degraded Performance
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}

NOTES
[1]"FSR" is Full-Scale Range.
[2]Full Scale (FS) = (V_{REF})
[3]Max gain change from T_A = +25°C to T_{min} or T_{max} is ±0.1% FSR.
[4]AC parameter, sample tested to ensure specification compliance.
[5]Guaranteed, not tested.
[6]Absolute temperature coefficient is approximately −300ppm/°C.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
R_{FB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage Range	−0.3V to V_{DD} +0.3V
OUT 1, OUT 2 to GND	−0.3V to V_{DD} +0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, L Versions)	−40°C to +85°C
Industrial (A, B, C Versions	−40°C to +85°C
Extended (S, T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % of full-scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution fo $[2^{-(n-1)}]$ (V_{REF}). Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustble to zero with an external potentiometer.

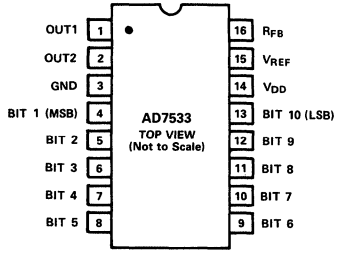
FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

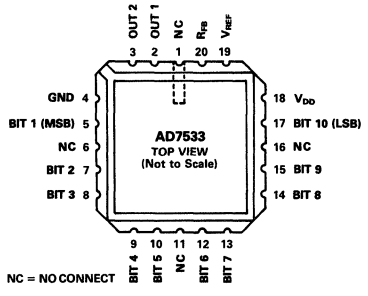
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

PIN CONFIGURATIONS

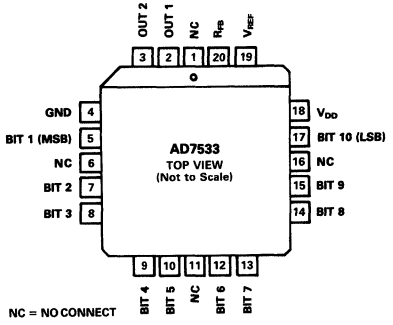
DIP



LCCC



PLCC



CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

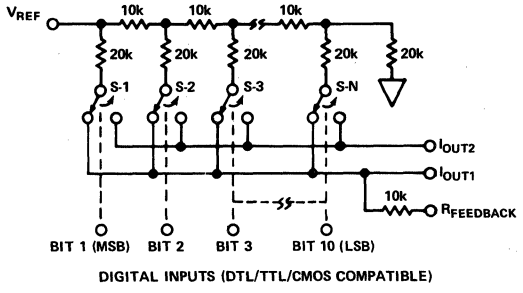


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20Ω, switch 2 for 40Ω, and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

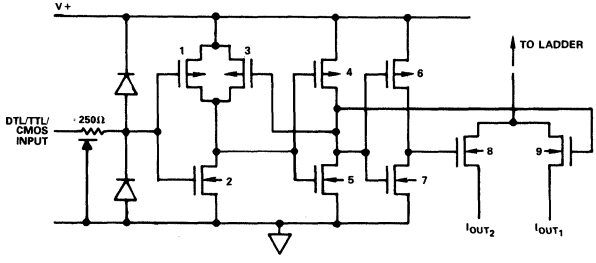


Figure 2. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 100pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 35pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

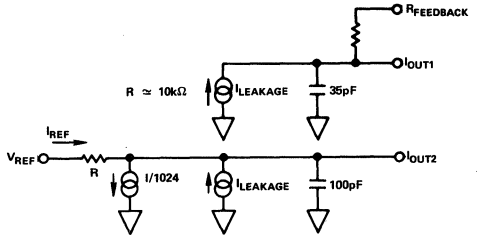


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

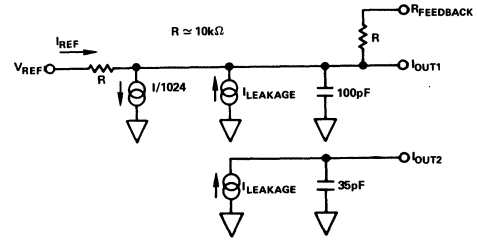


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right)=\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right)=0$

NOTE:
1. Nominal LSB magnitude for the circuit of Figure 5 is given by $LSB = V_{REF}\left(\frac{1}{1024}\right)$

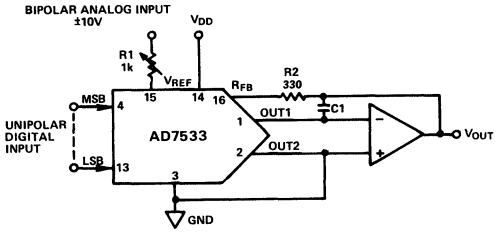
Table I. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{511}{512}\right)$
1 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{512}\right)$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{512}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{511}{512}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{512}\right)$

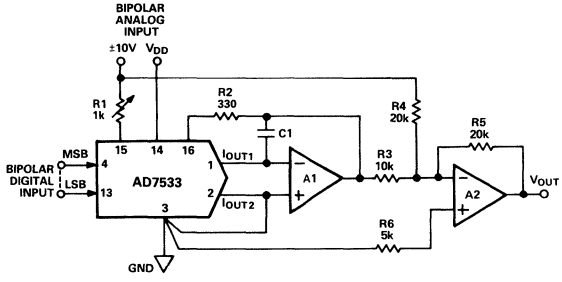
NOTE
1. Nominal LSB magnitude for the circuit of Figure 6 is given by $LSB = V_{REF}\left(\frac{1}{512}\right)$

Table II. Bipolar (Offset Binary) Code Table



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

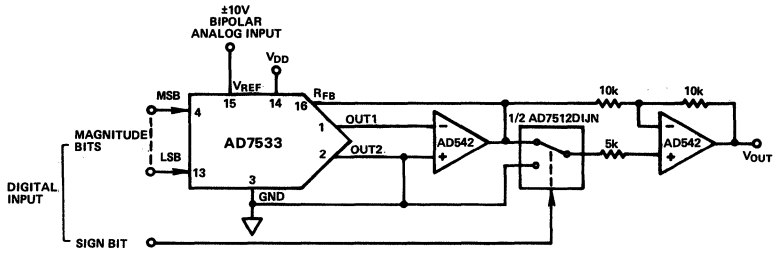


NOTES
1. R3, R4 AND R5 SELECTED FOR MATCHING AND TRACKING.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. C1 PHASE COMPENSATION (5-15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.

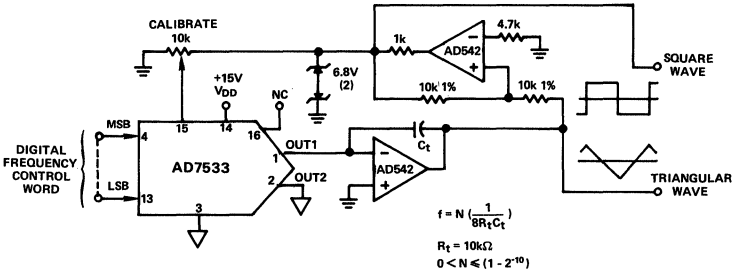
Figure 6. Bipolar Operation (4-Quadrant Multiplication)

APPLICATIONS

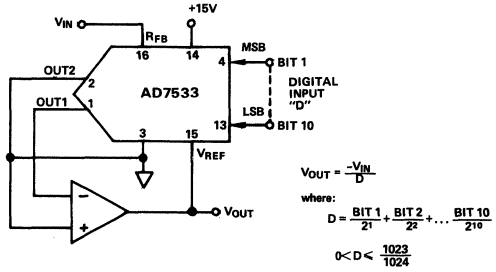
10-BIT AND SIGN MULTIPLYING DAC



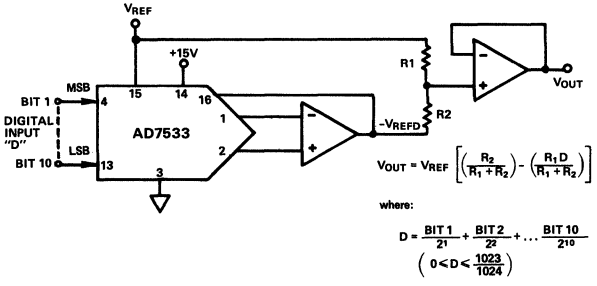
PROGRAMMABLE FUNCTION GENERATOR



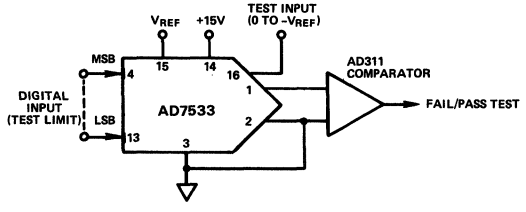
DIVIDER (DIGITALLY CONTROLLED GAIN)



MODIFIED SCALE FACTOR AND OFFSET



DIGITALLY PROGRAMMABLE LIMIT DETECTOR



LC²MOS µP-Compatible 14-Bit DAC

AD7534

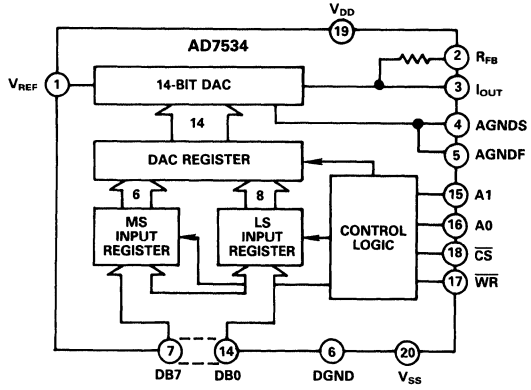
FEATURES

- All Grades 14-Bit Monotonic Over the Full Temperature Range
- Full 4-Quadrant Multiplication
- Microprocessor Compatible with Double Buffered Inputs
- Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
- Small 20-Pin DIP and Surface Mount Package
- Low Output Leakage (<20nA) Over the Full Temperature Range

APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio Reconstruction
- High Precision Servo Control
- Control and Measurement in High Temperature Environments

AD7534 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7534 is a 14-bit monolithic CMOS D/A converter which uses thin-film resistors and laser trimming to achieve excellent linearity.

The device is configured to accept right-justified data in two bytes from an 8-bit data bus. Standard Chip Select and Memory Write logic is used to access the DAC. Address lines A0 and A1 control internal register loading and transfer.

A novel low leakage configuration (patent pending) enables the AD7534 to exhibit excellent output leakage current characteristics over the specified temperature range.

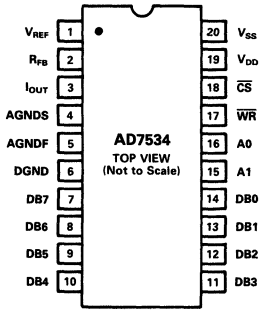
The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op amp. The AD7534 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

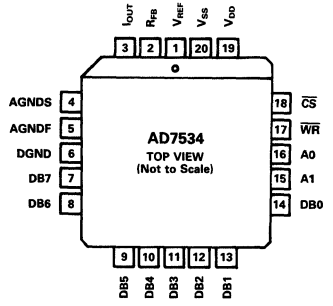
1. Guaranteed Montonicity
   The AD7534 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (Pin 20) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3" 20-pin DIP and 20-terminal surface mount package.

PIN CONFIGURATIONS

DIP



PLCC



SPECIFICATIONS[1]

(V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV. All specifications T_{min} to T_{max} unless otherwise stated)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3]						
ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specifications guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range.
I_{DD}	3	3	3	3	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.
(V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV, Output Amplifier is AD544 except where stated).

Parameter	V_{DD} = +11.4V to +15.75V T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	100	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection				
ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Guaranteed by Product Assurance testing.

[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	140	160	180	ns min	Data Setup Time
t_4	20	20	30	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select to Write Setup Time
t_6	0	0	0	ns min	Chip Select to Write Hold Time
t_7	170	200	240	ns min	Write Pulse Width

NOTES
[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} (Pin 19) to DGND . . . . . −0.3V, +17V
V_{SS} (Pin 20) to AGND . . . . . −15V, +0.3V
V_{REF} (Pin 1) to AGND . . . . . ±25V
V_{RFB} (Pin 2) to AGND . . . . . ±25V
Digital Input Voltage (Pins 7–18) to DGND
. . . . . −0.3V, V_{DD} +0.3V
V_{PIN3} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C

Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

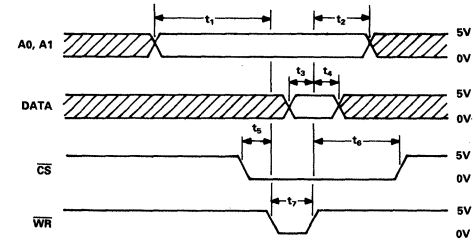
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION[1]

Relative Accuracy T_{min} to T_{max}	Full-Scale Error T_{min} to T_{max}	Temperature Range and Package Options[2] Plastic DIP (N-20) 0 to +70°C	Hermetic DIP (D-20) −25°C to +85°C	Hermetic DIP (D-20) −55°C to +125°C	PLCC[3] (P-20A) 0 to +70°C
±2LSB	±8LSB	AD7534JN	AD7534AD	AD7534SD	AD7534JP
±1LSB	±4LSB	AD7534KN	AD7534BD	AD7534TD	AD7534KP

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. AD7534 Timing Diagram

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high speed op-amps are used.

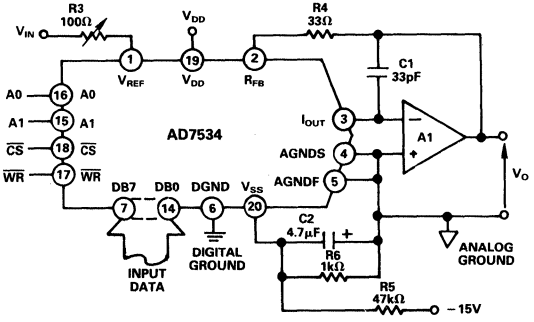


Figure 2. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB	
11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7534

WR	CS	A1	A0	Function
X[1]	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus[2]
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers.

NOTES
1. X = Don't Care
2. When $A_1 = 0$, $A_0 = 0$ all DAC registers are transparent, so by placing all 0s or all 1s on the data inputs the user can load the DAC to zero or full-scale output in one write operation. This facility simplifies system calibration.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the DAC loaded to 10 0000 0000 0000, adjust R3 for V_O = 0V. Alternatively, one can omit R3 and R4 and adjust the ratio of R7 and R8 for V_O = 0V. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R9.

Resistors R7, R8 and R9 should be matched to 0.003%. Mismatch of R7 and R8 causes both offset and full scale error. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficient match.

The code table for Figure 3 is given in Table II.

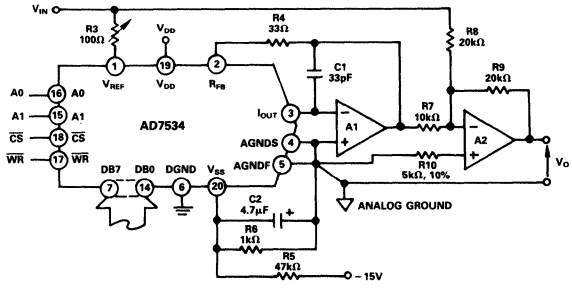


Figure 3. Bipolar Operation

Binary Number in DAC Register MSB LSB	Analog Output
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

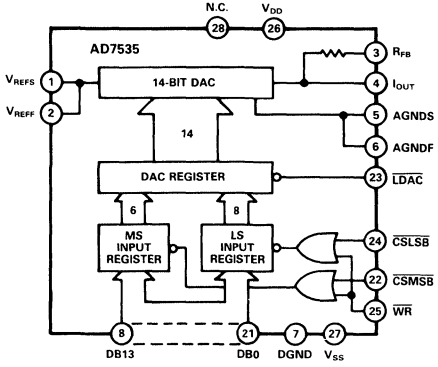
Table II. Bipolar Code Table for Offset Binary Circuit of Figure 3.

LC²MOS
µP-Compatible 14-Bit DAC
AD7535

FEATURES
- All Grades 14-Bit Monotonic over the Full Temperature Range
- Full 4 Quadrant Multiplication
- Microprocessor Compatible with Double Buffered Inputs
- Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
- Low Output Leakage (<20nA) over the Full Temperature Range

APPLICATIONS
- Microprocessor Based Control Systems
- Digital Audio
- Precision Servo Control
- Control and Measurement in High Temperature Environments

AD7535 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7535 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

Standard Chip Select and Memory Write logic is used to access the DAC.

A novel low leakage configuration (patent pending) enables the AD7535 to exhibit excellent output leakage current characteristics over the specified temperature range.

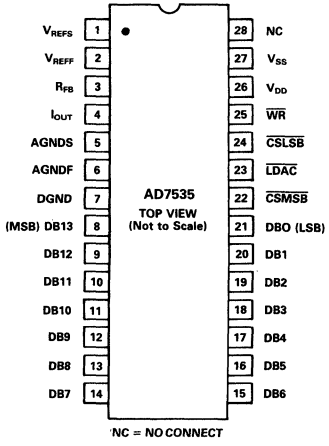
The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp. The AD7535 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

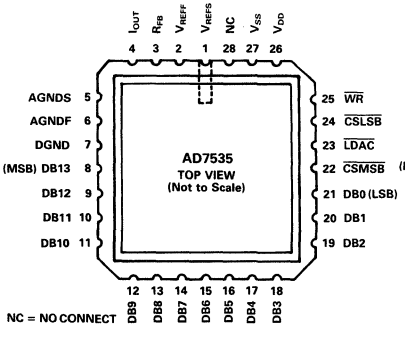
1. Guaranteed Monotonicity
   The AD7535 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (Pin 27) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors. When interfacing to 8-bit processors $\overline{CSMSB}$ and $\overline{CSLSB}$ are separate and the 8-bit data bus is connected to both the MS Input Register and the LS Input Register. For straight 14-bit parallel loading $\overline{CSMSB}$ and $\overline{CSLSB}$ are tied together giving one chip select to load the 14-bit word.

PIN CONFIGURATIONS

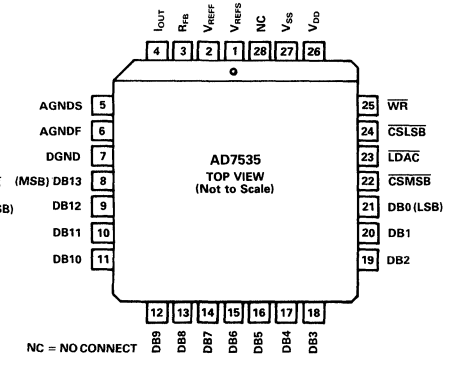
DIP



LCCC



PLCC



SPECIFICATIONS[1]

(V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN4} = V_{PIN5} = 0V, V_{SS} = −300mV
All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3];						
ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 4)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input resistance, pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.
(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V OR −300mV,
Output Amplifier is AD544 except where stated.)

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	50	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 4)	260	260	pF max	DAC register loaded with all 1s
C_{OUT} (Pin 4)	130	130	pF max	DAC register loaded with all 0s
Output Noise Voltage Density				
(10Hz – 100kHz)	15	–	$nV\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Guaranteed by Product Assurance testing.

[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	LDAC Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

NOTES
[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)
V_{DD} (Pin 26) to DGND . . . . . −0.3V, +17V
V_{SS} (Pin 27) to AGND . . . . . −15V, +0.3V
V_{REFS} (Pin 1) to AGND . . . . . ±25V
V_{REFF} (Pin 2) to AGND . . . . . ±25V
V_{RFB} (Pin 3) to AGND . . . . . ±25V
Digital Input Voltage (Pins 8–25) to DGND
. . . . . −0.3V, V_{DD} +0.3V
V_{PIN4} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C

Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

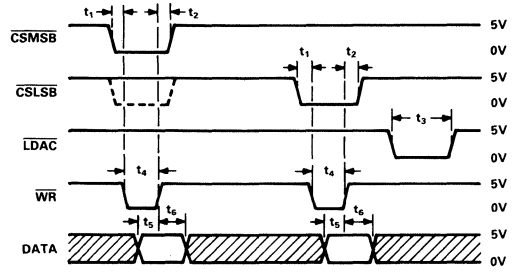
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION[1]

Relative Accuracy T_{min} to T_{max}	Full-Scale Error T_{min} to T_{max}	Temperature Range and Package Options[2] Plastic DIP (N-28) 0 to +70°C	Hermetic DIP (D-28) −25°C to +85°C	Hermetic DIP (D-28) −55°C to +125°C	PLCC[3] (P-28A) 0 to +70°C	LCCC[4] (E-28A) −55°C to +125°C
±2LSB	±8LSB	AD7535JN	AD7535AD	AD7535SD	AD7535JP	AD7535SE
±1LSB	±4LSB	AD7535KN	AD7535BD	AD7535TD	AD7535KP	AD7535TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7535 Timing Diagram

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2 quadrant multiplication. The code table for Figure 2 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high-speed op amps are used.

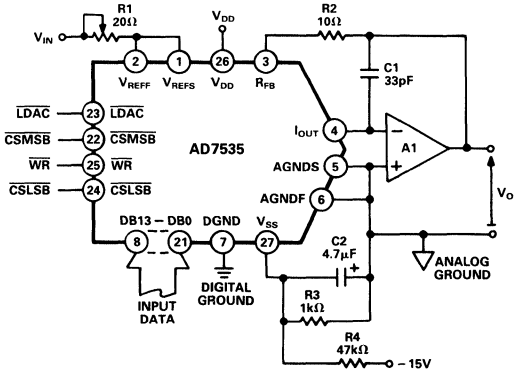


Figure 2. Unipolar Bipolar Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB	
11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7535

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	Operation
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load MS and LS Input Registers
1	1	0	X	Load DAC Register from Input Registers
0	0	0	0	All Registers are transparent
1	1	1	X	No operation
X	X	1	1	No operation

NOTE X = Don't Care

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the DAC loaded to 10 0000 0000 0000, adjust R1 for $V_O = 0$V. Alternatively, one can omit R1 and R2 and adjust the ratio of R5 and R6 for $V_O = 0$V. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R7.

Resistors R5, R6 and R7 should be ratio matched to 0.006%. Mismatch of R5 and R6 causes both offset and full-scale error. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

A range of precision voltage dividers, manufactured by Vishay, offers a suitable solution to implementing the bipolar circuit described above. The resistor networks are TCR and Ratio Matched, giving excellent performance over temperature.

The code table for Figure 3 is given in Table II.

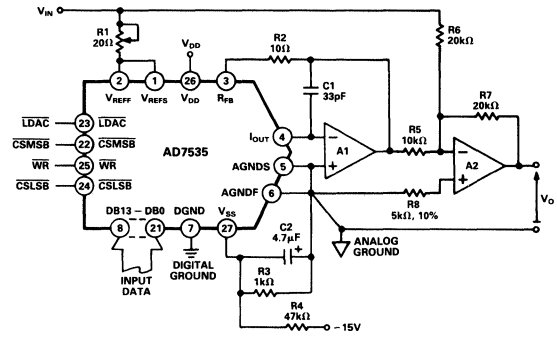


Figure 3. Bipolar Operation

Binary Number in DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 3.

ANALOG DEVICES

LC²MOS 14-Bit µP-Compatible DAC

AD7536

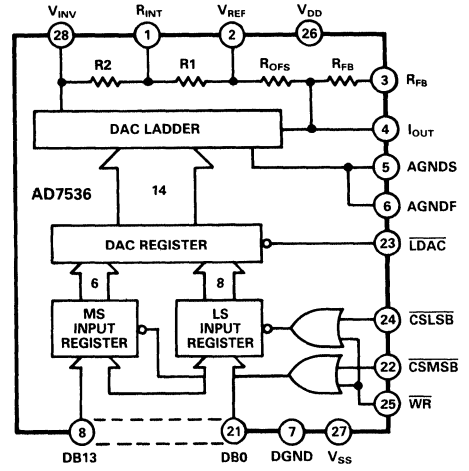
FEATURES

- Full 4-Quadrant Multiplication without External Resistors
- All Grades 14-Bit Monotonic over the Full Temperature Range
- Low Output Leakage (<20nA) over the Full Temperature Range
- Low Gain Temperature Coefficient, 2ppm/°C

APPLICATIONS

- Control and Measurement in High Temperature Environments
- Digital Audio
- Precision Servo Control
- All Microprocessor Based Control Systems

AD7536 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7536 is a 14-bit monolithic CMOS D/A converter. The part is laser trimmed and specified as a dedicated bipolar DAC. The resistors needed for 4-quadrant multiplication are contained on the chip. Thus, the user requires only the AD7536, a voltage reference and two op-amps for bipolar operation. The AD7536 has the same low leakage configuration (patent pending) as the other members of the 14-bit CMOS DAC family. The excellent output leakage current characteristics also ensure exceptional stability of linearity and gain error over the full temperature range.

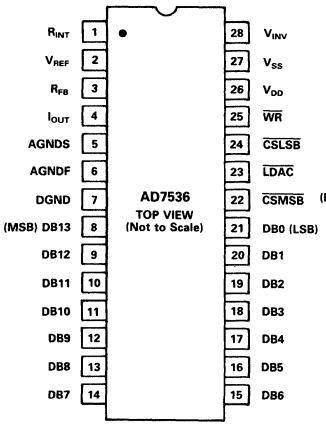
The device is speed compatible with most microprocessors and accepts TTL or 5V CMOS logic level inputs. There is standard Chip Select and Memory Write logic for easy interfacing. The AD7536 has full protection against CMOS "latch-up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp.

PRODUCT HIGHLIGHTS

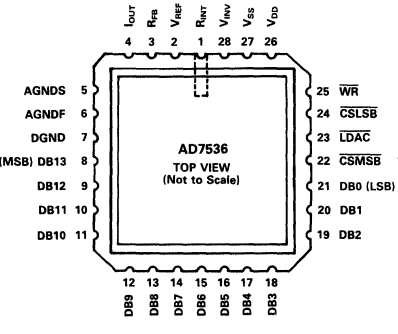
1. Bipolar Operation
   The AD7536 gives the user 4-Quadrant Multiplication without any external resistors.
2. Guaranteed Monotonicity
   14-bit monotonicity is guaranteed over the full temperature range for all grades.
3. Low Output Leakage
   The device has excellent output leakage current characteristics at all temperatures.

PIN CONFIGURATIONS

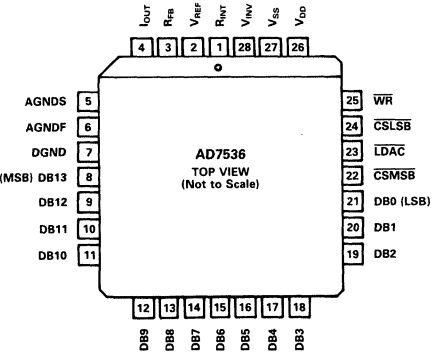
DIP



LCCC



PLCC



SPECIFICATIONS[1] (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN4} = V_{PIN5} = 0V, V_{SS} = −300mV. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	1LSB = $2V_{REF}/2^{14}$
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Gain Error	±16	±8	±16	±8	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Offset Error	±4	±4	±4	±4	LSB max	Error due to mismatch between R_{FB} and offset resistor. It also includes leakage current to I_{OUT} and is measured when DAC is loaded with all 0's.
Gain Temperature Coefficient[3], ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical Value is 2ppm/°C
Offset Temperature Coefficient[3] ΔOffset/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical Value is 1ppm/°C
INPUT RESISTANCES						
V_{REF} Input Resistance, Pin 2	3	3	3	3	kΩ min	Typical Input Resistance = 6kΩ
	13	13	13	13	kΩ max	
V_{INV} Input Resistance, Pin 28	2	2	2	2	kΩ min	Typical Input Resistance = 4kΩ
	8	8	8	8	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range.
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}
Power Supply Rejection ΔGain/ΔV_{DD}	±0.02	±0.02	±0.02	±0.02	% per % max	$\Delta V_{DD} = V_{DD}$ max − V_{DD} min

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V OR −300mV.)

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	50	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	4	–	mV p-p typ	V_{REF} = ±10V, 1kHz sine wave DAC register loaded with 10 0000 0000 0000
Output Capacitance				
C_{OUT} (Pin 4)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 4)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	50	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Guaranteed by Product Assurance testing.

[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	LDAC Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise stated)

V_{DD} (pin 26) to DGND . . . . . −0.3V, +17V
V_{SS} (pin 27) to AGND . . . . . −15V, +0.3V
V_{REF} (pin 2) to AGND . . . . . ±25V
V_{INV} (pin 28) to AGND . . . . . ±25V
R_{INT} (pin 1) to AGND . . . . . ±25V
R_{FB} (pin 3) to AGND . . . . . ±25V
Digital Input Voltage (pins 8–25) to DGND
. . . . . −0.3V, V_{DD} +0.3V
V_{PIN4} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C
Operating Temperature Range
Commercial Plastic (J, K versions) . . . . . 0 to +70°C
Industrial Ceramic (A, B versions) . . . . −25°C to +85°C
Extended Ceramic (S, T versions) . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

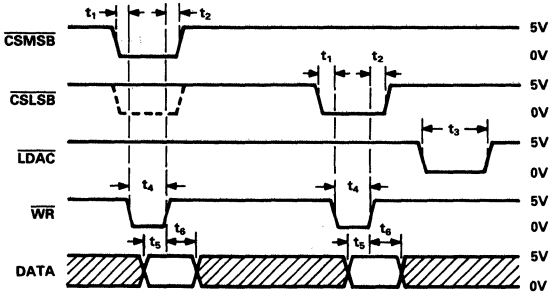
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION[1]

Relative Accuracy T_{min} to T_{max}	Gain Error T_{min} to T_{max}	Temperature Range and Package Options[2] Plastic DIP (N-28) 0 to +70°C	Hermetic DIP (D-28) −25°C to +85°C	Hermetic DIP (D-28) −55°C to +125°C	PLCC[3] (P-28A) 0 to +70°C	LCCC[4] (E-28A) −55°C to +125°C
±2LSB	±16LSB	AD7536JN	AD7536AD	AD7536SD	AD7536JP	AD7536SE
±1LSB	±8LSB	AD7536KN	AD7536BD	AD7536TD	AD7536KP	AD7536TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7536 Timing Diagram

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	Operation
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load MS and LS Input Registers
1	1	0	X	Load DAC Register from Input Registers
0	0	0	0	All Registers are transparent
1	1	1	X	No operation
X	X	1	1	No operation

NOTE X = Don't Care

BIPOLAR OPERATION
(4-Quadrant Multiplication)

Figure 2 shows the AD7536 connected for bipolar operation. Specified accuracy is attained without the need for expensive closely matched external resistors. R1 and R2 provide an optional gain adjustment and capacitor C1 helps prevent overshoot and ringing when high-speed op-amps are used. The −300mV bias voltage for V_{SS} is derived from R3, R4 and C2.

Table I shows the Offset Binary Code Table obtained with the circuit of Figure 2. It should be noted that the user can get a 2's Complement transfer function by inverting the MSB of the DAC word.

Binary Number in DAC Register (MSB LSB)	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
00 0000 0000 0001	$-V_{IN}\left(\frac{8191}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right) = -V_{IN}$

Table I. Offset Binary Code Table for AD7536

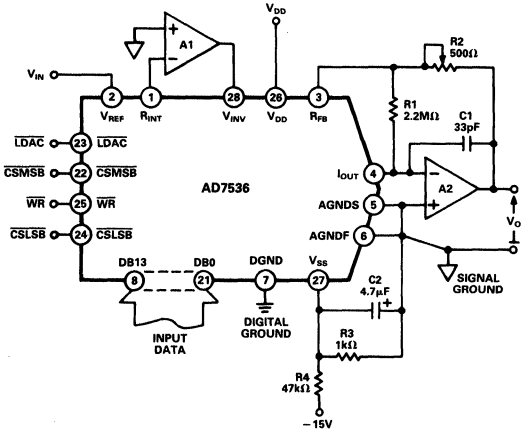


Figure 2. AD7536 Operation

OFFSET AND GAIN ADJUSTMENT FOR FIGURE 2.

Offset Adjustment

1. Adjust offset of amplifier A1 so that potential at R_{INT} is <10μV with respect to Signal Ground.
2. Load DAC register with 10 0000 0000 0000.
3. Adjust offset of amplifier A2 until V_O = 0V (<10μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R2 so that $V_O = +V_{IN}\frac{(8191)}{(8192)}$

For high-temperature applications, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Offset Error, Full Scale Error and Gain T.C. specifications of the AD7536, trimming of the Offset and Gain is not necessary.

ANALOG DEVICES

LC²MOS (8 + 4) Loading Dual 12-Bit DAC

AD7537

FEATURES
- Two 12-Bit DACs in One Package
- DAC Ladder Resistance Matching: 0.5%
- Space Saving Skinny DIP and Surface Mount Packages
- 4-Quadrant Multiplication
- Low Gain Error (1LSB max Over Temperature)
- Byte Loading Structure
- Fast Interface Timing

APPLICATIONS
- Automatic Test Equipment
- Programmable Filters
- Audio Applications
- Synchro Applications
- Process Control

GENERAL DESCRIPTION

The AD7537 contains two 12-bit current output DACs on one monolithic chip. A separate reference input is provided for each DAC. The dual DAC saves valuable board space, and the monolithic construction ensures excellent thermal tracking. Both DACs are guaranteed 12-bit monotonic over the full temperature range.

The AD7537 has a 2-byte (8LSBs, 4MSBs) loading structure. It is designed for right-justified data format. The control signals for register loading are A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{UPD}$. Data is loaded to the input registers when $\overline{CS}$ and $\overline{WR}$ are low. To transfer this data to the DAC registers, $\overline{UPD}$ must be taken low with $\overline{WR}$.

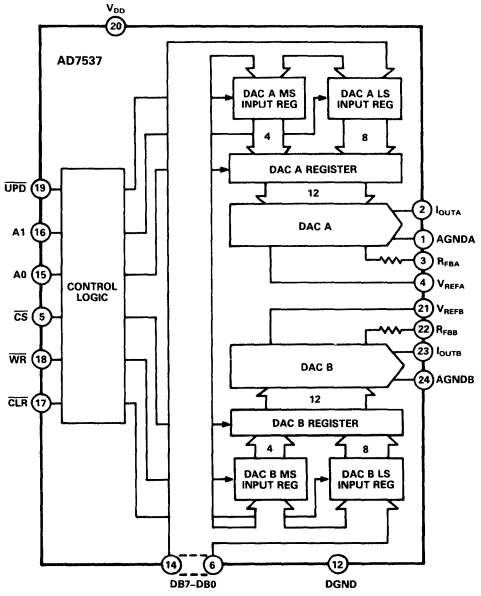
Added features on the AD7537 include an asynchronous $\overline{CLR}$ line which is very useful in calibration routines. When this is taken low, all registers are cleared. The double buffering of the data inputs allows simultaneous update of both DACs. Also, each DAC has a separate AGND line. This increases the device versatility; for instance one DAC may be operated with AGND biased while the other is connected in the standard configuration.

The AD7537 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC and 5V CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching:
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Small Package Size:
   The AD7537 is available in both 0.3" wide 24-pin DIPs and in 28-terminal surface mount packages.
3. Wide Power Supply Tolerance:
   The device operates on a +12V to +15V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

AD7537 FUNCTIONAL BLOCK DIAGRAM



$\overline{CLR}$	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A1	A0	FUNCTION
1	1	1	X	X	X	No Data Transfer
1	1	X	1	X	X	No Data Transfer
0	X	X	X	X	X	All Registers Cleared
1	1	0	0	0	0	DAC A LS Input Register Loaded with DB7-DB0 (LSB)
1	1	0	0	0	1	DAC A MS Input Register Loaded with DB3 (MSB)-DB0
1	1	0	0	1	0	DAC B LS Input Register Loaded with DB7-DB0 (LSB)
1	1	0	0	1	1	DAC B MS Input Register Loaded with DB3 (MSB)-DB0
1	0	1	0	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
1	0	0	0	X	X	DAC A, DAC B Registers are Transparent

NOTE: X = Don't care

Table I. AD7537 Truth Table

SPECIFICATIONS[1] (V_{DD} = +12V to +15V, ±10%, V_{REFA} = V_{REFB} = 10V; I_{OUTA} = AGNDA = 0V, I_{OUTB} = AGNDB = 0V. All specifications T_{min} to T_{max} unless otherwise specified.)

Parameter	J/A Versions	K/B Versions	L/C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1's.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current								
I_{OUTA} (Pin 2)								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0s
I_{OUTB} (Pin 23)								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0s
REFERENCE INPUT								
Input Resistance (Pin 4, Pin 21)	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14kΩ
	20	20	20	20	20	20	kΩ max	
V_{REFA}, V_{REFB}								
Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12V to +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = AGNDA = 0V, I_{OUTB} = AGNDB = 0V. Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. Typical Value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	7	–	nV-s typ	Measured with V_{REFA} = V_{REFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0s and all 1s.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20Vp-p 10kHz sine wave.
V_{REFB} to I_{OUTB}	−70	−65	dB max	DAC registers loaded with all 0s.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max − V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0s
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1s
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−84	–	dB typ	V_{REFA} = 20V p-p 10kHz sine wave, V_{REFB} = 0V. Both DACs loaded with all 1s.
V_{REFB} to I_{OUTA}	−84	–	dB typ	V_{REFB} = 20V p-p 10kHz sine wave, V_{REFA} = 0V. Both DACs loaded with all 1s.
Digital Crosstalk	7	–	nV-s typ	Measured for a Code Transition of all 0s to all 1s. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF.
Output Noise Voltage Density (10Hz-100kHz)	25	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10Hz–100kHz.
Total Harmonic Distortion	−82	–	dB typ	V_{IN} = 6V rms, 1kHz. Both DACs loaded with all 1s.

NOTES

[1]Temperature range as follows: J, K, L Versions: −40°C to +85°C.
A, B, C Versions: −40°C to +85°C.
S, T, U Versions: −55°C to +125°C.

[2]Sample tested at 25°C to ensure compliance.

[3]Functional at V_{DD} = 5V with degraded specifications.

[4]Pin 12 (DGND) on ceramic packages is connected to lid.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 10.8V to 16.5V, V_{REFA} = V_{REFB} = +10V, I_{OUTA} = AGNDA = 0V, I_{OUTB} = AGNDB = 0V).

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = +55°C to +125°C	Units	Test Conditions/Comments
t_1	15	15	30	ns min	Address Valid to Write Setup Time
t_2	15	15	25	ns min	Address Valid to Write Hold Time
t_3	60	80	80	ns min	Data Setup Time
t_4	25	25	25	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	80	80	100	ns min	Write Pulse Width
t_8	80	80	100	ns min	Clear Pulse Width

NOTE
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} to AGNDA, AGNDB . . . . . ±25V
V_{RFBA}, V_{RFBB} to AGNDA, AGNDB . . . . . ±25V
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
I_{OUTA}, I_{OUTB} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGNDA, AGNDB to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C
Operating Temperature Range
Commercial (J, K, L Versions) . . . . . −40°C to +85°C
Industrial (A, B, C Versions) . . . . . −40°C to +85°C
Extended (S, T, U Versions) . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

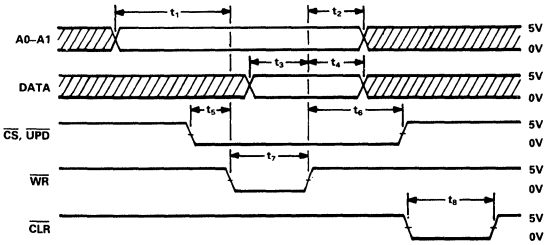


Figure 1. Timing Diagram for AD7537

ORDERING INFORMATION[1,2]

Relative Accuracy T_{min}–T_{max}	Gain Error T_{min}–T_{max}	Temperature Range and Package Options[3] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-24)	Hermetic (Q-24)	Hermetic (Q-24)
±1LSB	±6LSB	AD7537JN	AD7537AQ	AD7537SQ
±1/2LSB	±3LSB	AD7537KN	AD7537BQ	AD7537TQ
±1/2LSB	±1LSB	AD7537LN	AD7537CQ	
±1/2LSB	±2LSB			AD7537UQ
		PLCC[4] (P-28A)		LCCC[5] (E-28A)
±1LSB	±6LSB	AD7537JP		AD7537SE
±1/2LSB	±3LSB	AD7537KP		AD7537TE
±1/2LSB	±1LSB	AD7537LP		
±1/2LSB	±2LSB			AD7537UQ

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing, see DESC drawing #5962-87763.
[2]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.
[3]See Section 14 for package outline information.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

CIRCUIT INFORMATION – D/A SECTION

The AD7537 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 2 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGNDA. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op amp to convert the current flowing in I_{OUTA} to a voltage output.

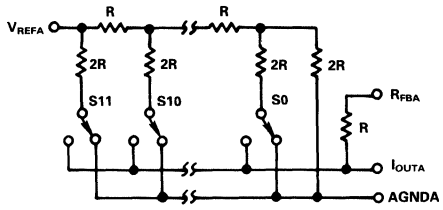


Figure 2. Simplified Circuit Diagram for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7537. A similar equivalent circuit can be drawn for DAC B.

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50pF to 150pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_0 is the equivalent output resistance of the device which varies with input code.

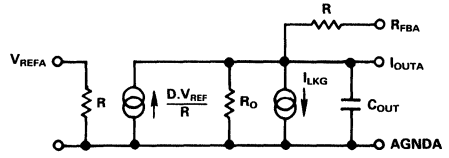


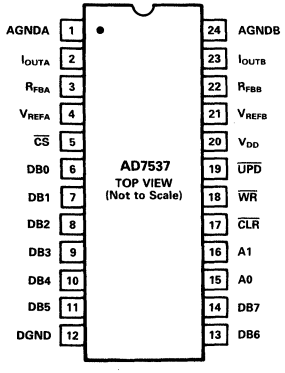
Figure 3. Equivalent Analog Circuit for DAC A

DIGITAL CIRCUIT INFORMATION

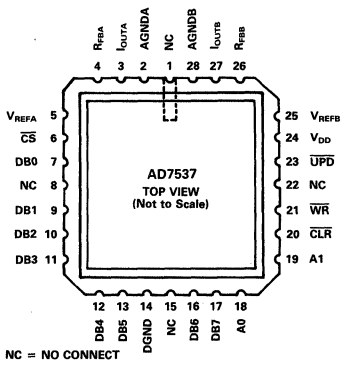
The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA.

PIN CONFIGURATIONS

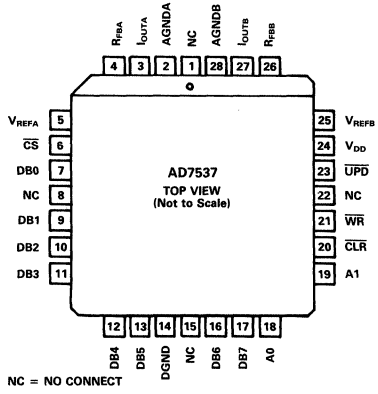
DIP



LCCC



PLCC



PIN FUNCTION DESCRIPTION (DIP)

PIN	MNEMONIC	DESCRIPTION
1	AGNDA	Analog Ground for DAC A.
2	I_{OUTA}	Current output terminal of DAC A.
3	R_{FBA}	Feedback resistor for DAC A.
4	V_{REFA}	Reference input to DAC A.
5	$\overline{CS}$	Chip Select Input. Active low.
6-14	DB0-DB7	Eight data inputs, DB0-DB7.
12	DGND	Digital Ground.
15	A0	Address Line 0.
16	A1	Address Line 1.
17	$\overline{CLR}$	Clear Input. Active low. Clears all registers.
18	$\overline{WR}$	Write Input. Active low.
19	$\overline{UPD}$	Updates DAC Registers from inputs registers.
20	V_{DD}	Power supply input. Nominally + 12V to + 15V, with ± 10% tolerance.
21	V_{REFB}	Reference input to DAC B.
22	R_{FBB}	Feedback resistor for DAC B.
23	I_{OUTB}	Current output terminal of DAC B.
24	AGNDB	Analog Ground for DAC B.

ANALOG DEVICES

LC²MOS µP-Compatible 14-Bit DAC

AD7538

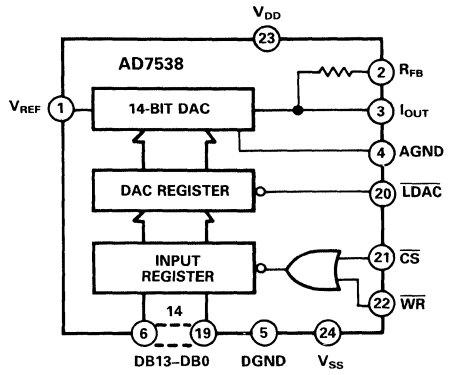
FEATURES

- All Grades 14-Bit Monotonic over the Full Temperature Range
- Low Cost 14-Bit Upgrade for 12-Bit Systems
- 14-Bit Parallel Load with Double Buffered Inputs
- Small 24-Pin, 0.3" DIP
- Low Output Leakage (<20nA) over the Full Temperature Range

APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio
- Precision Servo Control
- Control and Measurement in High Temperature Environments

AD7538 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7538 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

The DAC is loaded by a single 14-bit wide word using standard Chip Select and Memory Write Logic. Double buffering, which is optional using $\overline{\text{LDAC}}$, allows simultaneous update in a system containing multiple AD7538s.

A novel low leakage configuration (U.S. Patent No. 4,590,456) enables the AD7538 to exhibit excellent output leakage current characteristics over the specified temperature range.

The AD7538 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Monotonicity
   The AD7538 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Cost
   The AD7538, with its 14-bit dynamic range, affords a low cost solution for 12-bit system upgrades.
3. Small Package Size
   The AD7538 is packaged in a small 24-pin, 0.3" DIP.
4. Low Output Leakage
   By tying V_{SS} (Pin 24) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
5. Wide Power Supply Tolerance
   The device operates on a +12 to +15V V_{DD}, with a ±5% tolerance on this nominal figure. All specifications are guaranteed over this range.

SPECIFICATIONS[1] (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, K Versions	A, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full-Scale Error						Measured using internal R_{FB}
+25°C	±4	±4	±4	±4	LSB max	DAC registers loaded with
T_{min}–T_{max}	±8	±5	±10	±6	LSB max	all 1s.
Gain Temperature Coefficient[3];						
ΔGain/ΔTemperature	±2	±2	±2	±2	ppm/°C typ	
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = 0V OR −300mV, Output Amplifier is AD711 except where stated.)

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	20	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s.
Multiplying Feedthrough Error	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0s.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1s
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0s
Output Noise Voltage Density				
(10Hz–100kHz)	15	–	$nV\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows:

J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Sample tested to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	$\overline{LDAC}$ Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

NOTES
[1]Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

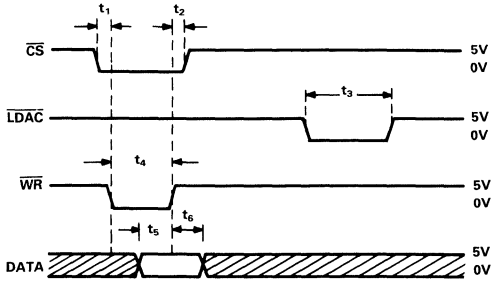
V_{DD} (Pin 23) to DGND . . . . . −0.3V, +17V
V_{SS} (Pin 24) to AGND . . . . . −15V, +0.3V
V_{REF} (Pin 1) to AGND . . . . . ±25V
V_{RFB} (Pin 2) to AGND . . . . . ±25V
Digital Input Voltage (Pins 6–22)
to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{PIN3} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C

Operating Temperature Range
Commercial (J, K versions) . . . . . 0 to +70°C
Industrial (A, B versions) . . . . . −25°C to +85°C
Extended (S, T versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

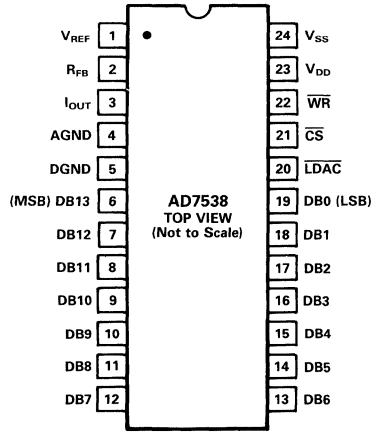
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURES FROM 10% TO 90% OF +5V. $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. If $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 or LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7538 Timing Diagram

PIN CONFIGURATION



TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustable to zero with an external potentiometer.

DIGITAL-TO-ANALOG GLITCH IMPULSE
The amount of charge injected from the digital inputs to the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

OUTPUT CAPACITANCE
This is the capacitance from I_{OUT} to AGND.

OUTPUT LEAKAGE CURRENT
Output Leakage Current is current which appears at I_{OUT} with the DAC register loaded to all 0s.

MULTIPLYING FEEDTHROUGH ERROR
This is the ac error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

ORDERING INFORMATION

		Temperature Range and Package Options*		
Relative Accuracy T_{min} to T_{max}	Full Scale Error T_{min} to T_{max}	Plastic (N-24) 0 to +70°C	Hermetic (Q-24) −25°C to +85°C	Hermetic (Q-24) −55°C to +125°C
±2LSB	±8LSB	AD7538JN	AD7538AQ	AD7538SQ
±1LSB	±4LSB	AD7538KN	AD7538BQ	AD7538TQ

*See Section 14 for package outline information.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{REF}	Voltage Reference.
2	R_{FB}	Feedback resistor. Used to close the loop around an external op amp.
3	I_{OUT}	Current Output Terminal.
4	AGND	Analog Ground
5	DGND	Digital Ground
6–19	DB13–DB0	Data Inputs. Bit 13 (MSB) to Bit 0 (LSB).
20	$\overline{LDAC}$	Chip Select input. Active LOW.
21	$\overline{CS}$	Asynchronous Load DAC input. Active LOW.
22	$\overline{WR}$	Write input. Active LOW.

$\overline{CS}$	$\overline{LDAC}$	$\overline{WR}$	OPERATION
0	1	0	Load Input Register.
1	0	X	Load DAC Register from Input Register.
0	0	0	Input and DAC Registers are transparent
1	1	X	No operation.
X	1	1	No operation.

NOTE: X = Don't Care.

23	V_{DD}	+12V to +15V supply input.
24	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figures 4 and 5 for recommended circuitry.

CIRCUIT INFORMATION

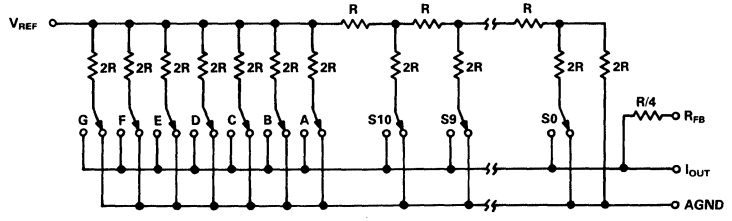


Figure 2. Simplified Circuit Diagram for the AD7538 D/A Section

D/A SECTION

Figure 2 shows a simplified circuit diagram for the AD7538 D/A section. The three MSBs of the 14-bit Data Word are decoded to drive the seven switches A-G. The 11 LSBs of the Data Word consist of an R-2R ladder operated in a current steering configuration.

The R-2R ladder current is 1/8 of the total reference input current. 7/8 I flows in the parallel ladder structure. Switches A-G steer equally weighted currents between I_{OUT} and AGND.

Since the input resistance at V_{REF} is constant, it may be driven by a voltage source or a current source of positive or negative polarity.

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7538 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O denotes the equivalent output resistance of the DAC which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of the DAC ladder, N.

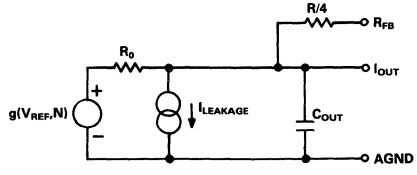


Figure 3. AD7538 Equivalent Analog Output Circuit

DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2 quadrant multiplication. The code table for Figure 4 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high-speed op amps are used.

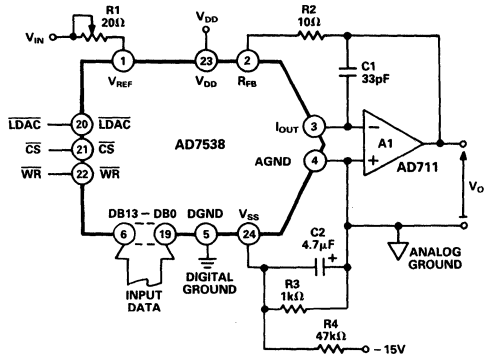


Figure 4. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB	
11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7538

For zero offset adjustment, the DAC register is loaded with all 0s and amplifier offset (V_{OS}) adjusted so that V_{OUT} is 0V. Adjusting V_{OUT} to 0V is not necessary in many applications, but it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) to maintain specified DAC accuracy (see Applications Hints).

Full-scale trimming is accomplished by loading the DAC register with all 1s and adjusting R1 so that $V_{OUTA} = -V_{IN}(16383/16384)$. For high temperature operation, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7538, Gain Error trimming is not necessary. In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used. The code table for Figure 5 is given in Table II.

With the DAC loaded to 10 0000 0000 0000, adjust R1 for $V_O = 0V$. Alternatively, one can omit R1 and R2 and adjust the ratio of R5 and R6 for $V_O = 0V$. Full-scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R7.

The values given for R1, R2 are the minimum necessary to calibrate the system for resistors, R5, R6, R7 ratio matched to 0.1%. System linearity error is independent of resistor ratio matching and is affected by DAC linearity error only.

When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

For further information see "CMOS DAC Application Guide", 3rd Edition, Publication Number G872b–8–1/89 available from Analog Devices.

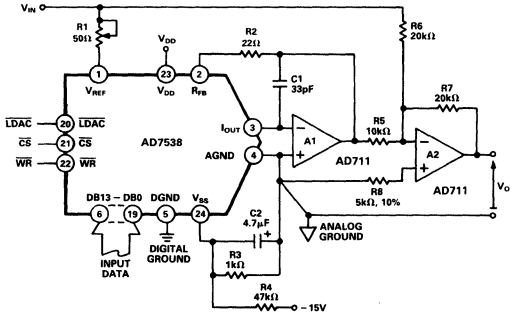


Figure 5. Bipolar Operation

Binary Number in DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 5.

LOW LEAKAGE CONFIGURATION

For CMOS Multiplying D/A converters, as the device is operated at higher temperatures, the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7538 features a leakage reduction configuration (U.S. Patent No. 4,590,456) to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (Pin 24) is tied to AGND then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to a voltage of approximately $-0.3V$ as in Figures 4 and 5. A simple resistor divider (R3, R4) produces approximately $-300mV$ from $-15V$. The capacitor C2 in parallel with R3 is an integral part of the low leakage configuration and must be $4.7\mu F$ or greater. Figure 6 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

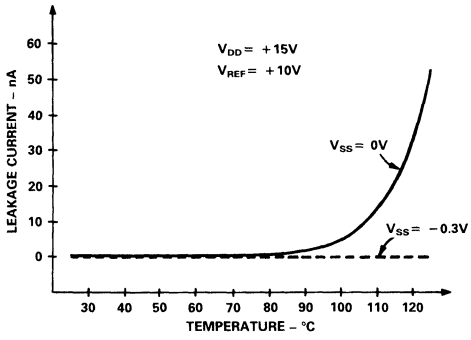


Figure 6. Graph of Typical Leakage Current vs. Temperature for AD7538

PROGRAMMABLE GAIN AMPLIFIER

The circuit shown in Figure 7 provides a programmable gain amplifier (PGA). In it the DAC behaves as a programmable resistance and thus allows the circuit gain to be digitally controlled.

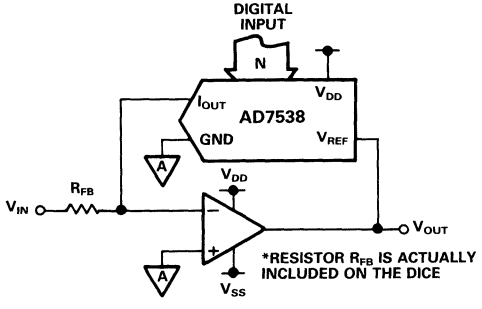


Figure 7. Programmable Gain Amplifier (PGA)

The transfer function of Figure 7 is:

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = -\frac{R_{EQ}}{R_{FB}} \quad (1)$$

R_{EQ} is the equivalent transfer impedance of the DAC from the V_{REF} pin to the I_{OUT} pin and can be expressed as

$$R_{EQ} = \frac{2^n R_{IN}}{N} \quad (2)$$

Where: n is the resolution of the DAC

N is the DAC input code in decimal

R_{IN} is the constant input impedance of the DAC ($R_{IN} = R_{LAD}$)

Substituting this expression into Equation 1 and assuming zero gain error for the DAC ($R_{IN} = R_{FB}$) the transfer function simplifies to

$$\frac{V_{OUT}}{V_{IN}} = -\frac{2^n}{N} \quad (3)$$

The ratio $N/2^n$ is commonly represented by the term D and, as such, is the fractional representation of the digital input word.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{2^n}{N} = \frac{-1}{D} \quad (4)$$

Equation 4 indicates that the gain of the circuit can be varied from 16,384 down to unity (actually 16,384/16,383) in 16,383 steps. The all 0s code is never applied. This avoids an open-loop condition thereby saturating the amplifier. With the all 0s code excluded there remains $2^n - 1$ possible input codes allowing a choice of $2^n - 1$ output levels. In dB terms the dynamic range is

$$20 \log_{10} \frac{V_{OUT}}{V_{IN}} = 20 \log_{10} (2^n - 1) = 84dB.$$

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 4 and 5 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified accuracy with V_{REF} at 10V, it is recommended that V_{OS} be no greater than 0.25mV, or (25×10^{-6}) (V_{REF}), over the temperature range of operation. The AD711 is a suitable op amp. The op amp has a wide bandwidth and high slew rate and is recommended for ac and other applications requiring fast settling.

General Ground Management: Since the AD7538 is specified for high accuracy, it is important to use a proper grounding technique. AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7538. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7538 AGND and DGND pins (1N914 or equivalent).

MICROPROCESSOR INTERFACING

The AD7538 is designed for easy interfacing to 16-bit microprocessors and can be treated as a memory mapped peripheral. This reduces the amount of external logic needed for interfacing to a minimal.

AD7538-8086 INTERFACE

Figure 8 shows the 8086 processor interface to a single device. In this setup the double buffering feature (using $\overline{\text{LDAC}}$) of the DAC is not used. The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately.

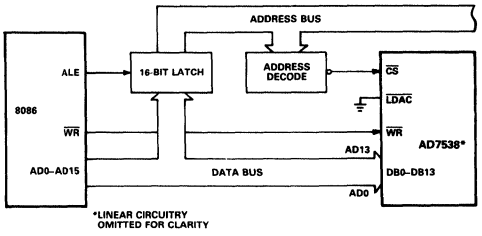


Figure 8. AD7538 – 8086 Interface Circuit

In a multiple DAC system the double buffering of the AD7538 allows the user to simulatenously update all DACs. In Figure 9, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., LDAC) is brought low, updating all the DACs simultaneoulsy.

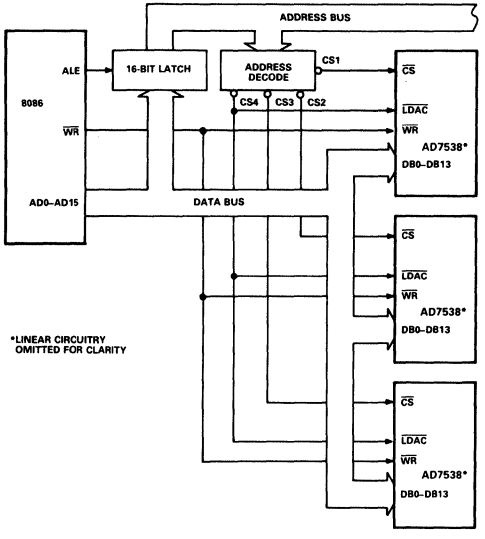


Figure 9. AD7538 – 8086 Interface: Multiple DAC System

AD7538-MC68000 INTERFACE

Figure 10 shows the MC68000 processor interface to a single device. In this setup the double buffering feature of the DAC is not used and the appropriate data is written into the DAC in one MOVE instruction.

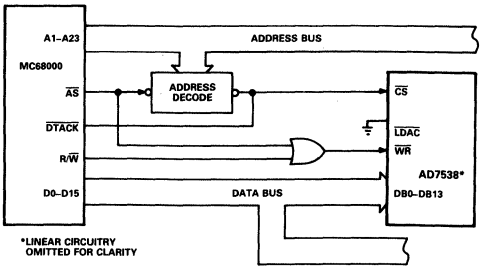


Figure 10. AD7538 – MC68000 Interface

DIGITAL FEEDTHROUGH

The digital inputs to the AD7538 are directly connected to the microprocessor bus in the preceding interface configurations. These inputs will be constantly changing even when the device is not selected. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 11 shows an interface circuit which uses this technique. All data inputs are latched from the bus by the $\overline{\text{CS}}$ signal. One may also use other means, such as peripheral interface devices, to reduce the Digital Feedthrough.

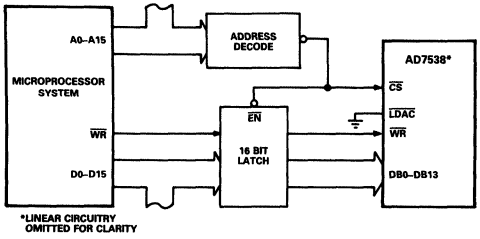


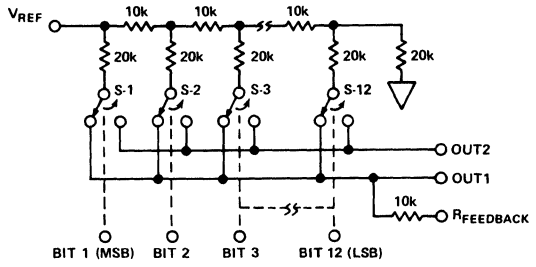
Figure 11. AD7538 Interface Circuit Using Latches to Minimize Digital Feedthrough

CMOS 12-Bit Monolithic Multiplying DAC

AD7541A

FEATURES
- Improved Version of AD7541
- Full Four Quadrant Multiplication
- 12-Bit Linearity (End-Point)
- All Parts Guaranteed Monotonic
- TTL/CMOS Compatible
- Low Cost
- Protection Schottky Not Required
- Low Logic Input Leakage

AD7541A FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

GENERAL DESCRIPTION

The Analog Devices' AD7541A is a low cost, high performance 12-bit monolithic multiplying digital to analog converter. It is fabricated using advanced, low noise, thin film on CMOS technology and is available in a standard 18-pin DIP and in 20-terminal surface mount packages.

The AD7541A is functionally and pin compatible with the industry standard AD7541 device and offers improved specifications and performance. The improved design ensures that the device is latch-up free so no output Schottky protection diodes are required.

This new device uses laser wafer trimming to provide full 12-bit end-point linearity with several new high performance grades.

PRODUCT HIGHLIGHTS

Compatability: The AD7541A can be used as a direct replacement for any AD7541–type device. As with the Analog Devices AD7541, the digital inputs are TTL/CMOS compatible and have been designed to have a $\pm 1\mu A$ maximum input current requirement so as not to load the driving circuitry.

Improvements: The AD7541A offers the following improved specifications over the AD7541:

1. Gain Error for all grades has been reduced with premium grade versions having a maximum gain error of ±3LSB.
2. Gain Error temperature coefficient has been reduced to 2ppm/°C typical and 5ppm/°C maximum.
3. Digital to analog charge injection energy for this new device is typically 20% less than the standard AD7541 part.
4. Latch-up proof.
5. Improvements in laser wafer trimming provides 1/2LSB max differential nonlinearity for top grade devices over the operating temperature range (vs. 1LSB on older 7541 types).
6. All grades are guaranteed monotonic to 12 bits over the operating temperature range.

ORDERING INFORMATION[1,2]

Relative Accuracy, LSB T_{min} to T_{max}	Gain Error, LSB $T_A = +25°C$	Temperature Range and Package Options[3] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-18)	**Hermetic (Q-18)**	**Hermetic (Q-18)**
±1	±6	AD7541AJN	AD7541AAQ	AD7541ASQ
±1/2	±1	AD7541AKN	AD7541ABQ	AD7541ATQ
		PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
±1	±6	AD7541AJP		AD7541ASE
±1/2	±1	AD7541AKP		AD7541ATE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]Analog Devices reserves to right to ship ceramic packages (package outline D-18) in lieu of cerdip packages (package outline Q-18).
[3]See Section 14 for package outline information.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +10V; OUT 1 = OUT 2 = GND = 0V unless otherwise specified)

Parameter	Version	T_A = +25°C	T_A = T_{min}, T_{max}[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J, A, S	±1	±1	LSB max	±1LSB = ±0.024% of Full Scale
	K, B, T	±1/2	±1/2	LSB max	±1/2LSB = ±0.012% of Full Scale
Differential Nonlinearity	J, A, S	±1	±1	LSB max	All grades guaranteed monotonic
	K, B, T	±1/2	±1/2	LSB max	to 12 bits, T_{min} to T_{max}
Gain Error	J, A, S	±6	±8	LSB max	Measured using internal R_{FB} and includes
	K, B, T	±3	±5	LSB max	effect of leakage current and gain T.C.
					Gain error can be trimmed to zero.
Gain Temperature Coefficient[2]					
ΔGain/ΔTemperature	All	5	5	ppm/°C max	Typical value is 2ppm/°C.
Output Leakage Current					
OUT1 (Pin 1)	J, K	±5	±10	nA max	All digital inputs = 0V.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
OUT 2 (Pin 2)	J, K	±5	±10	nA max	All digital inputs = V_{DD}.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
REFERENCE INPUT					
Input Resistance (Pin 17 to GND)	All	7–18	7–18	kΩ min/max	Typical input resistance = 11kΩ.
					Typical input resistance temperature coefficient = −300ppm/°C.
DIGITAL INPUTS					
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	V min	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	μA max	Logic inputs are MOS gates. I_{IN} typ (25°C) = 1nA.
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY REJECTION					
ΔGain/ΔV_{DD}	All	±0.01	±0.02	%per% max	ΔV_{DD} = ±5%
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min/V max	Accuracy is not guaranteed over this range.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IH}.
		100	500	μA max	All digital inputs 0V or V_{DD}.

AC PERFORMANCE CHARACTERISTICS

These Characteristics are Included for Design Guidance Only and are not Subject to Test.
V_{DD} = +15V, V_{IN} = +10V except where stated, OUT 1 = OUT 2 = GND = 0V, Output Amp is AD544 except where stated.

Parameter	Version[1]	T_A = +25°C	T_A = T_{min}, T_{max}[1]	Units	Test Conditions/Comments
PROPAGATION DELAY (From Digital Input					OUT 1 Load = 100Ω C_{EXT} = 13pF
Change to 90% of Final Analog Output)	All	100	–	ns typ	Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
DIGITAL TO ANALOG GLITCH					V_{REF} = 0V. All digital inputs 0V to V_{DD} or V_{DD}
IMPULSE					to 0V.
	All	1000	–	nV-sec typ	Measured using Model 50K as output amplifier.
MULTIPLYING FEEDTHROUGH ERROR[3]					
(V_{REF} to OUT1)	All	1.0	–	mV p-p typ	V_{REF} = ± 10V, 10kHz sine wave.
OUTPUT CURRENT SETTLING TIME	All	0.6	–	μs typ	To 0.01% of full scale range.
					OUT1 load = 100Ω, C_{EXT} = 13pF.
					Digital inputs = 0V to V_{DD} or V_{DD} to 0V
OUTPUT CAPACITANCE					
C_{OUT1} (Pin 1)	All	200	200	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	70	70	pF max	$= V_{IH}$
C_{OUT1} (Pin 1)	All	70	70	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	200	200	pF max	$= V_{IL}$

NOTES
[1]Temperature range as follows: J, K versions: 0 to +70°C
A, B versions: −25°C to +85°C
S, T versions: −55°C to +125°C.
[2]Guaranteed by design but not production tested.
[3]To minimize feedthrough in the ceramic package (Suffix D) the user must ground the metal lid.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	+17V
V_{REF} to GND	±25V
V_{RFB} to GND	±25V
Digital Input Voltage to GND	−0.3V, V_{DD} +0.3V
OUT 1, OUT 2 to GND	−0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	
Commercial (J, K versions)	0 to +70°C
Industrial (A, B versions)	−25°C to +85°C
Extended (S, T versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output. For the AD7541A, ideal maximum output is $-\left(\frac{4095}{4096}\right)(V_{REF})$. Gain error is adjustable to zero using external trims as shown in Figures 4, 5 and 6.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

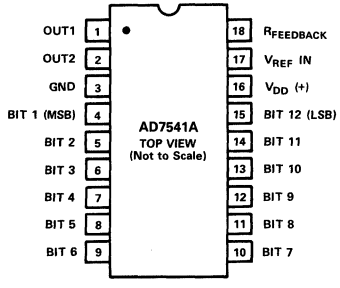
This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL-TO-ANALOG CHARGE INJECTION (QDA)

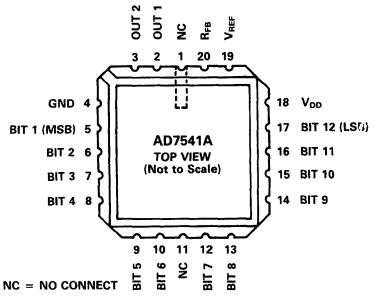
This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV secs and is measured with V_{REF} = GND and a Model 50K as the output op amp, C1 (phase compensation) = 0pF.

PIN CONFIGURATIONS

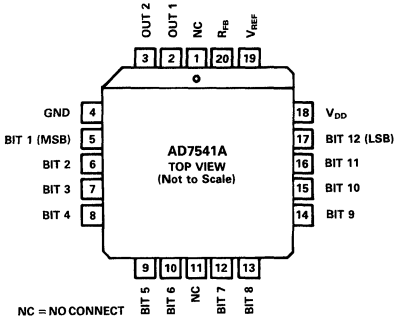
DIP



LCCC



PLCC



GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used–that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

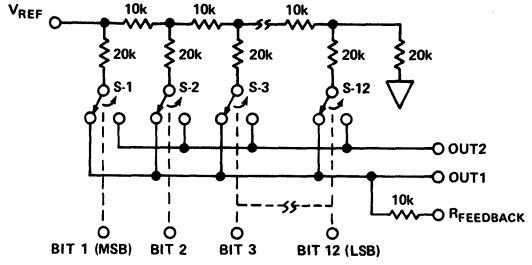


Figure 1. AD7541A Functional Diagram (Inputs "High")

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 2 and 3. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 70pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 3 is similar to Figure 2; however, the "ON" switches are now on terminal OUT1, hence the 200pF at that terminal.

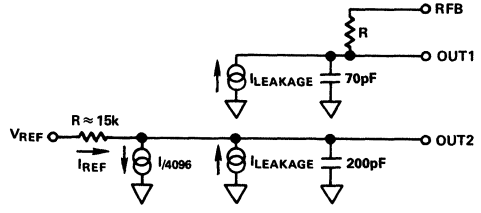


Figure 2. AD7541A DAC Equivalent Circuit All Digital Inputs LOW

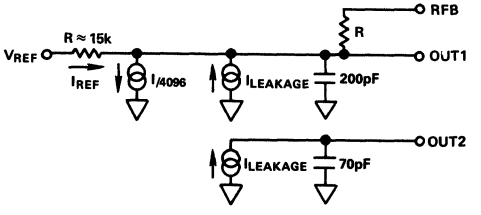


Figure 3. AD7541A DAC Equivalent Circuit All Digital Inputs HIGH

Applications

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at pin 17, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full scale trim capability [i.e.–load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq$ 10% of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 11kΩ). The AD544L is a high-speed implanted FET-input op amp with low factory-trimmed V_{OS}.

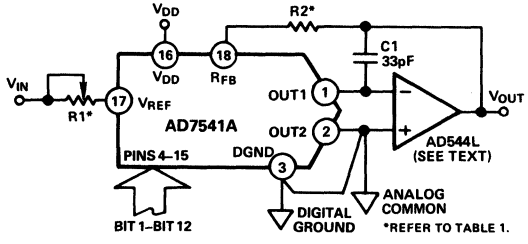


Figure 4. Unipolar Binary Operation

Trim Resistor	JN/AQ/SD	KN/BQ/TD
R1	100Ω	100Ω
R2	47Ω	33Ω

Table I. Recommended Trim Resistor Values vs. Grades

Binary Number in DAC MSB	LSB	Analog Output, V_{OUT}
1111 1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\,V_{IN}$
0000 0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000	0000	0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 4

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference the circuit provides full 4-quadrant multiplication.

With the DAC loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10pF to 50pF) may be required for stability, depending on amplifier used.

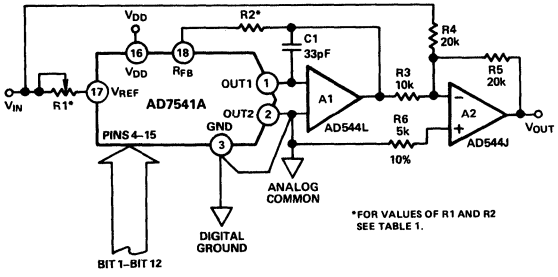


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Binary Number in DAC MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.

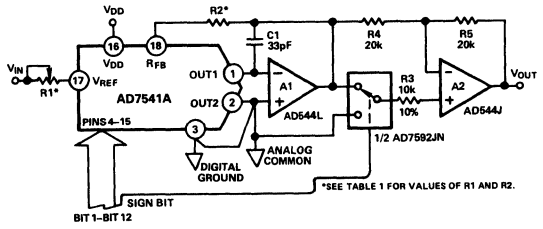


Figure 6. 12-Bit Plus Sign Magnitude Operation

Sign Bit	Binary Number in DAC MSB LSB	Analog Output, V_{OUT}
0	1111 1111 1111	$+V_{IN} \cdot \left(\frac{4095}{4096}\right)$
0	0000 0000 0000	0 Volts
1	0000 0000 0000	0 Volts
1	1111 1111 1111	$-V_{IN} \cdot \left(\frac{4095}{4096}\right)$

Note: Sign bit of "0" connects R3 to GND.

Table IV. 12-Plus Sign Magnitude Code Table for Circuit of Figure 6

APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

Digital Glitches: One cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and OUT2 terminals. This should be minimized by screening the analog pins of the AD7541A (pins 1, 2, 17, 18) from the digital pins by a ground track run between pins 2 and 3 and between pins 16 and 17 of the AD7541A. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and GND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7541A, particularly in circuits with high currents and fast rise and fall times.

Temperature Coefficients: The gain temperature coefficient of the AD7541A has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630c–5–3/86.

SINGLE SUPPLY OPERATION

Figure 7 shows the AD7541A connected in a voltage switching mode. OUT1 is connected to the reference voltage and OUT2 is connected to GND. The D/A converter output voltage is available at the V_{REF} pin (pin 17) and has a constant output impedance equal to R_{LDR}. The feedback resistor R_{FB} is not used in this circuit.

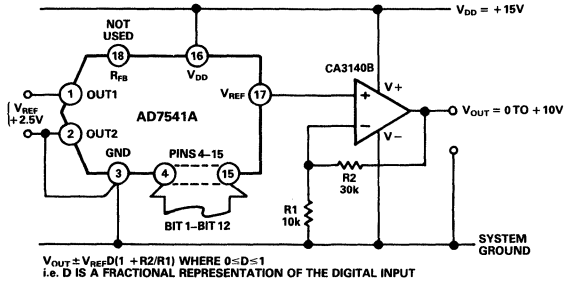


Figure 7. Single Supply Operation Using Voltage Switching Mode

The reference voltage must always be positive. If OUT1 goes more than 0.3V less than GND an internal diode will be turned on and a heavy current may flow causing device damage (the AD7541A is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices). Suitable references include the AD580 and AD584.

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltage at OUT1 should remain within 2.5V of GND, for a V_{DD} of 15V. If V_{DD} is reduced from 15V or the reference voltage at OUT1 increased to more than 2.5V the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded.

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

CMOS DAC Application Guide, Publication Number G872b–8–1/89 available from Analog Devices.

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs Application Note, Publication Number E630c–5–3/86 available from Analog Devices.

Analog-Digital Conversion Handbook – available from Analog Devices, price $32.95.

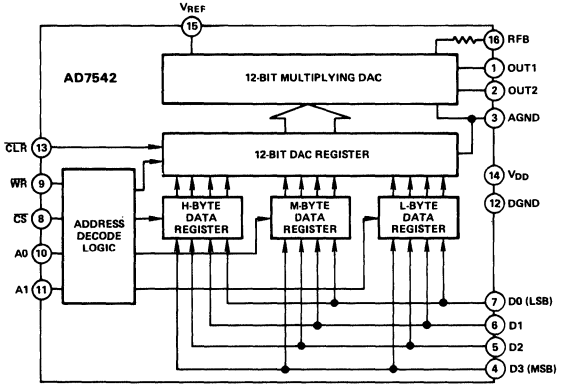
ANALOG DEVICES

CMOS µP-Compatible 12-Bit DAC

AD7542

FEATURES
- **Resolution: 12 Bits**
- **Nonlinearity: ±1/2LSB T_{min} to T_{max}**
- **Low Gain Drift: 2ppm/°C typ, 5ppm/°C max**
- **Microprocessor Compatible**
- **Full 4-Quadrant Multiplication**
- **Fast Interface Timing**
- **Low Power Dissipation: 40mW max**
- **Low Cost**
- **Small Size: 16-Pin DIP and 20 Terminal Surface Mount Packages**
- **Latch Free (Protection Schottky Not Required)**

AD7542 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

The functional diagram shows the AD7542 to consist of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A clear input allows the DAC register to be easily reset to all zeros when powering up the device.

The AD7542 is manufactured using an advanced thin-film on monolithic CMOS fabrication process. Multiplying capability, low power dissipation, +5V operation, small size (16-pin DIP and 20 terminal surface mount packages) and easy µP interface make the AD7542 ideal for many instrumentation, industrial control and avionics applications.

ORDERING INFORMATION[1]

Relative Accuracy (T_{min} to T_{max})	Gain Error +25°C	Temperature Range and Package Options[2,3] Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Extended (Ceramic) -55°C to +125°C
±1LSB	±3LSB	AD7542JN	AD7542AD	AD7542SD
±1LSB	±3LSB	AD7542JP	AD7542AE	AD7542SE
±1/2LSB	±3LSB	AD7542KN	AD7542BD	AD7542TD
±1/2LSB	±3LSB	AD7542KP	AD7542BE	AD7542TE
±1/2LSB	±1LSB	AD7542GKN	AD7542GBD	AD7542GTD
±1/2LSB	±1LSB	AD7542GKP	AD7542GBE	AD7542GTE

NOTES
[1]To order MIL-STD-883 Class B processed parts, add/883B to part number.
[2]Package Designation: Plastic DIP (N-16); Plastic Leaded Chip Carrier (PLCC) (P-20A); Ceramic DIP (D-16); Leadless Ceramic Chip Carrier (LCCC) (E-20A).
[3]See Section 14 for package outline information.

SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = 0, +70°C, -25°C & +85°C	Limit At[1] T_A = -55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
J, A, S Versions	±1	±1	±1	LSB max	
K, B, T Versions	±1/2	±1/2	±1/2	LSB max	
GK, GB, GT Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
J, A, S Versions	±1	±1	±1	LSB max	All grades are guaranteed monotonic
K, B, T Versions	±1	±1	±1	LSB max	T_{min} to T_{max}
GK, GB, GT Versions	±1	±1	±1	LSB max	
Gain Error[2]					
J, K, A, B, S, T	±3	±4	±4	LSB max	Using internal R_{FB} only (gain error can be
GK, GB, GT	±1	±1	±2	LSB max	trimmed to zero using circuits of Figure 4 & 5)
Gain Temperature Coefficient ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1}	10	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2}	10	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	μs max	To 1/2LSB, OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	DAC register loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	DAC register loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+2.4	+2.4	+2.4	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (See Figures 4 and 5). Data is Loaded into Data Registers in 4-Bit Bytes.				
SWITCHING CHARACTERISTICS[5]	(See Figure 1)				
t_{WR}	80	120	160	ns min	t_{WR}: WRITE pulse width
t_{AWH}	0	10	10	ns min	t_{AWH}: Address-to-WRITE hold time
t_{CWH}	0	10	10	ns min	t_{CWH}: Chip select-to-WRITE hold time
t_{CLR}	200	200	250	ns min	t_{CLR}: Minimum CLEAR pulse width
t_{CWS}	10	20	20	ns min	t_{CWS}: Chip select-to-WRITE setup time
t_{AWS}	40	40	40	ns min	t_{AWS}: Address valid-to-WRITE setup time
t_{DS}	60	100	100	ns min	t_{DS}: Data setup time
t_{DH}	10	10	10	ns min	t_{DH}: Data hold time
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	±5% for specified performance
I_{DD} (Supply Current)	2.5	2.5	2.5	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES
[1] Temperature Ranges as follows: J, K, GK versions; 0 to +70°C
A, B, GB versions; -25°C to +85°C
S, T, GT versions; -55°C to +125°C

[2] See definitions on next page.
[3] Guaranteed but not tested.
[4] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
[5] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

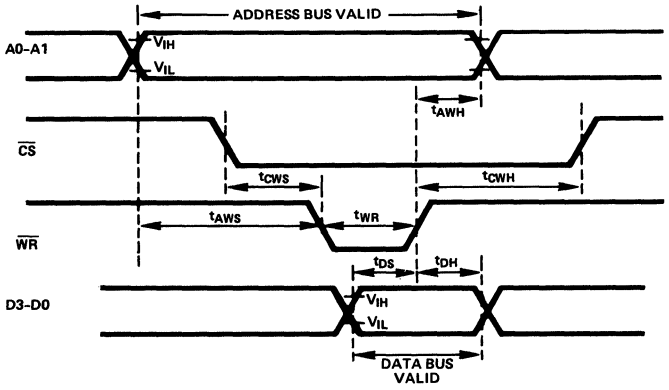
(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to GND	−0.3V, V_{DD} +0.3V
V_{OUT1}, V_{OUT2} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	±25V
V_{RFB} to AGND	±25V
Power Dissipation (Package)	
Plastic	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, GK Versions)	0 to +70°C
Industrial (A, B, GB Versions)	−25°C to +85°C
Extended (S, T, GT Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*COMMENTS: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

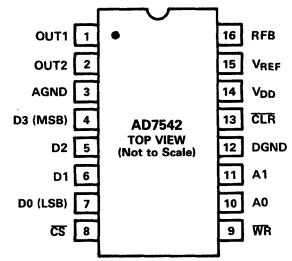


NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

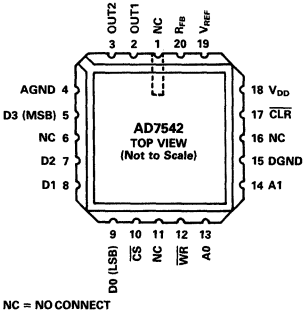
Figure 1. AD7542 Timing Diagram

PIN CONFIGURATIONS

DIP

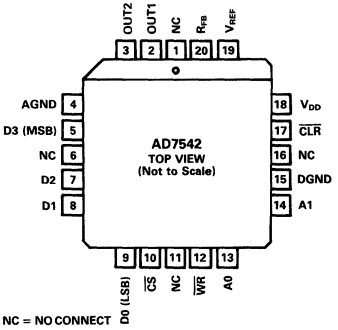


LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR

Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7542 would exhibit a gain of –4095/4096. Gain error is adjustable using external trims as shown in Figures 4 and 5.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC register loaded to all 0s or at OUT2 with the DAC register loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at ground
3	AGND	Analog Ground
4	D3	Data Input (MSB)
5	D2	Data Input
6	D1	Data Input
7	D0	Data Input (LSB)
8	$\overline{CS}$	Chip Select Input
9	$\overline{WR}$	WRITE Input
10	A0	Address Bus Input
11	A1	Address Bus Input
12	DGND	Digital Ground
13	$\overline{CLR}$	Clear Input
14	V_{DD}	+5V Supply Input
15	V_{REF}	Reference Input
16	R_{FB}	DAC Feedback Resistor

Table I. Pin Function Description (DIP Pin Numbers)

Analog Circuit Description

GENERAL CIRCUIT INFORMATION

The AD7542, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 2. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

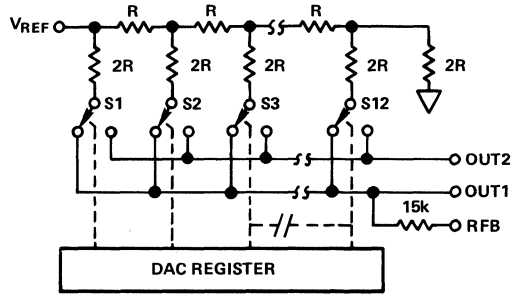


Figure 2. D/A Simplified Circuit Diagram

One of the current switches is shown in Figure 3. The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient R_{FB} is recommended to define scale factor.)

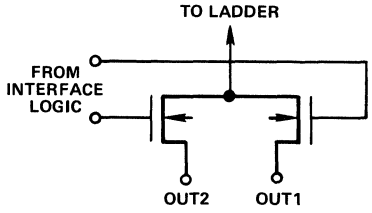


Figure 3. N-Channel Current Steering Switch

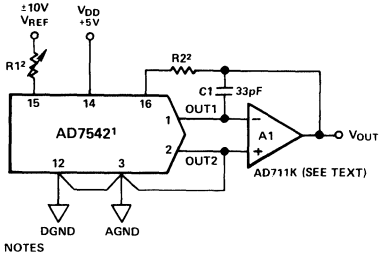
UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at V_{REF}, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 33pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD711K is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.



NOTES
1. LOGIC INPUTS OMITTED FOR CLARITY, DIP PIN NUMBERS SHOWN.
2. SEE APPLICATION HINT NO. 4.

Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

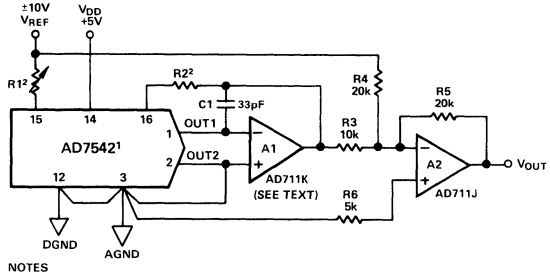
Table II. Unipolar Binary Code Table for Circuit of Figure 4

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the circuit provides full 4-quadrant multiplication.

With the DAC register loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.



NOTES
1. LOGIC INPUTS OMITTED FOR CLARITY, DIP PIN NUMBERS SHOWN.
2. SEE APPLICATION HINT NO. 4.

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

INTERFACE LOGIC

INTERFACE LOGIC INFORMATION

The AD7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown in Figure 6. $\overline{CS}$ is the decoded *device* address, and is derived by decoding the three higher order address bits. A0 and A1 is the AD7542 *operation* address, and is decoded internally in the AD7542 to point to the desired loading operation (i.e., load high byte, middle byte, low byte or DAC register). Table IV shows the AD7542 truth table.

All data loading operations are identical to the write cycle of a RAM as shown in Figure 1.

Additionally, the $\overline{CLR}$ input allows the AD7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the AD7542 in a unipolar mode (Figure 4), a CLEAR causes the DAC output to assume 0V. In the bipolar mode (Figure 5), a CLEAR causes the DAC output to go to $-V_{REF}$.

In summary:

1. The AD7542 DAC register can be asynchronously cleared with the $\overline{CLR}$ input.
2. Each AD7542 requires 4 locations in memory.
3. Performing any of the four basic loading operations (i.e. load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) is accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

AD7542 Control Inputs					AD7542 Operation	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	X	1	No Operation Device Not Selected	
0	0	0	↓	1	Load LOW Byte[5] Data Register On Edge As Shown	Load Applicable Data Register With Data At $D_0 - D_3$
0	1	0	↓	1	Load MIDDLE Byte[5] Data Register On Edge As Shown	
1	0	0	↓	1	Load HIGH Byte[5] Data Register On Edge As Shown	
1	1	0	⊓	1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers[6]	

NOTES:
[1] 1 indicates logic HIGH
[2] 0 indicates logic LOW
[3] X indicates don't care
[4] ↓ indicates LOW to HIGH transition
[5] MSB → XXXX (high byte) XXXX (middle byte) XXXX (low byte) ← LSB
[6] These control signals are level triggered.

Table IV. AD7542 Truth Table

AD7542 INTERFACE TO MC6800

A typical 6800 system configuration is shown in Figure 6. Since the AD7542 contains four registers each AD7542 is assigned four locations in memory. A0 and A1 provides the operational addresses and are decoded internally to point to the desired register. Register loading is accomplished by executing a memory WRITE instruction to one of the four addresses. Table V gives a sample loading subroutine written in re-entrant form.

Choosing an arbitrary start address of PPQQ, locations PPQQ, PPQQ+1 and PPQQ+2 select the low, middle and high byte registers respectively while address PPQQ+3 selects the 12-bit DAC register. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1.

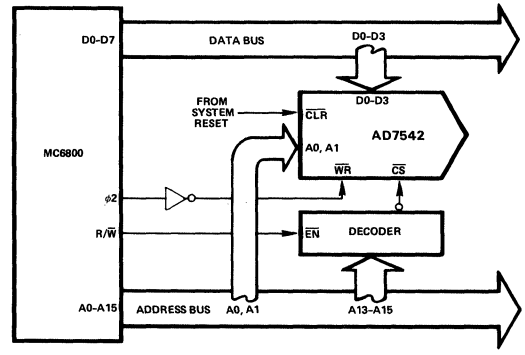


Figure 6. Interfacing the AD7542 to an MC6800 Microprocessor

```
                JSR     WWZZ
WWZZ    PSH A                   PUSH ACC. A ONTO STACK
        TPA
        PSH A                   PUSH CCR ONTO STACK
        LDA A   XXYY
        STA A   PPQQ            LOAD LOW BYTE
        ROR A
        ROR A
        ROR A
        ROR A
        STA A   PPQQ+1          LOAD MIDDLE BYTE
        LDA A   XXYY+1
        STA A   PPQQ+2          LOAD HIGH BYTE
        STA A   PPQQ+3          LOAD DAC REGISTER
        PUL A
        TAP                     POP CCR FROM STACK
        PUL A                   POP ACC. A FROM STACK
        RTS                     RETURN TO MAIN PROGRAM
```

Table V. Sample Routine for AD7542–6800 Interface

AD7542 INTERFACE TO 8085

A typical 8085 system configuration is shown in Figure 7. The AD7542 $\overline{CS}$ input is decoded from the three high order address lines A13–A15. The 8085 $\overline{WR}$ output is directly connected to the $\overline{WR}$ input of the AD7542. Table VI gives a sample loading subroutine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1. As before, arbitrary addresses PPQQ to PPQQ+3 select the low byte, middle byte, high byte and DAC registers respectively.

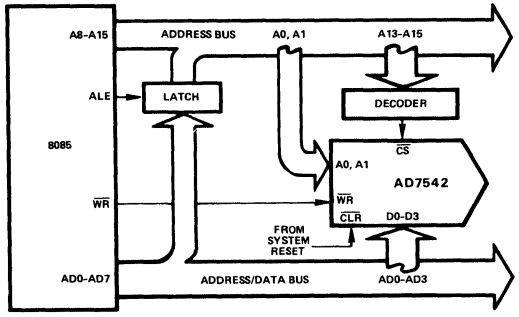


Figure 7. Interfacing the AD7542 to an 8085 Microprocessor

```
        CALL    7542
7542    PUSH    PSW         PUSH REGISTER CONTENTS
        PUSH    B           ONTO STACK
        PUSH    H
        LXI     H, XXYY
        MOV     A, M
        STA     PPQQ        LOAD LOW BYTE
        MVI     B, 04
LOOP    RAR
        DCR     B
        JNZ     LOOP
        STA     PPQQ+1      LOAD MIDDLE BYTE
        INX     H
        MOV     A, M
        STA     PPQQ+2      LOAD HIGH BYTE
        STA     PPQQ+3      LOAD DAC REGISTER
        POP     H           POP REGISTER CONTENTS
        POP     B           FROM STACK
        POP     PSW
        RET                 RETURN TO MAIN PROGRAM
```

Table VI. Sample Routine for AD7542–8085 Interface

APPLICATION HINTS

The AD7542 is a precision 12-bit multiplying DAC designed for system interface. To ensure system performance consistent with AD7542 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7542 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7542. In more complex systems where the AGND-DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7542 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This nonlinearity term adds to the R/2R nonlinearity. To maintain specified operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = V_{REF} (2^{-n}) where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7542 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7542 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 4 and 5 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows: –

$$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wirewound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7542 gain error specification of ±3LSBs it is recommended that R1 = 50Ω and R2 = 25Ω. With γ = 50 these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.025}{8}(50 + 300) = 6\text{ppm/°C}$$

However, if the AD7542GTD is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630–10–6/81 available from Analog Devices.

5. For additional information on multiplying DACs refer to "CMOS DAC Application Guide," Publication Number G872a–15–4/86, available from Analog Devices.

ANALOG DEVICES

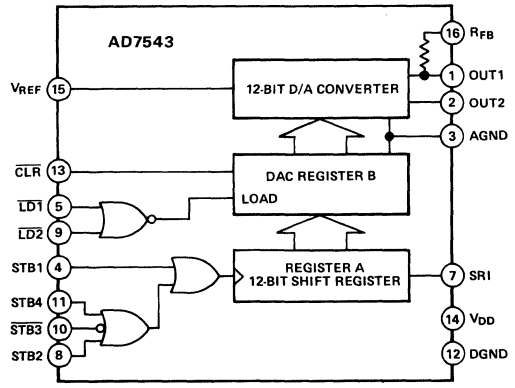
CMOS Serial Input 12-Bit DAC

AD7543

FEATURES

- Resolution: 12 Bits
- Nonlinearity: ±1/2LSB T_{min} to T_{max}
- Low Gain T.C.: 2ppm/°C typ, 5ppm/°C max
- Serial Load on Positive or Negative Strobe
- Asynchronous CLEAR Input for Initialization
- Full 4-Quadrant Multiplication
- Low Multiplying Feedthrough: 1LSB max @ 10kHz
- Requires no Schottky Diode Output Protection
- Low Power Dissipation: 40mW max
- +5V Supply
- Small Size: 16-Pin DIP or 20-Terminal Surface Mount Package
- Low Cost

AD7543 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7543 is a precision 12-bit monolithic CMOS multiplying DAC designed for serial interface applications.

The DAC's logic circuitry consists of a 12-bit serial-in parallel-out shift register (Register A) and a 12-bit DAC input register (Register B). Serial data at the AD7543 SRI pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input. Once Register A is full its contents are loaded into Register B under control of the LOAD inputs.

Initialization is simplified by the use of the CLR input which provides an asynchronous reset of Register B.

Packaged in 16-pin DIP and 20-pin LCCC and PLCC, the AD7543 features excellent gain T.C. (2ppm/°C typ; 5ppm/°C max), +5V operation and latch-free operation. (No protection Schottky Diodes required.)

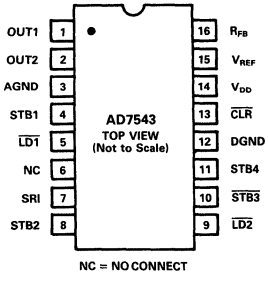
ORDERING INFORMATION[1]

Relative Accuracy T_{min}–T_{max}	Gain Error T_{min}–T_{max}	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-16)	Hermetic DIP (D-16)	Hermetic DIP (D-16)
±1LSB	±12.3LSB	AD7543JN	AD7543AD	AD7543SD
±1/2LSB	±12.3LSB	AD7543KN	AD753BD	AD7543TD
±1/2LSB	±1LSB	AD7543GKN	AD7543GBD	AD7543GTD
		PLCC (P-20A)		LCCC (E-20A)
±1LSB	±12.3LSB	AD7543JP		AD7543SE
±1/2LSB	±12.3LSB	AD7543KP		AD7543TE
±1/2LSB	±1LSB	AD7543GKP		AD7543GTE

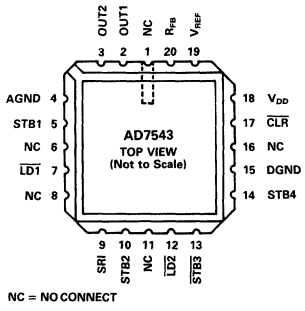
NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.

PIN CONFIGURATIONS

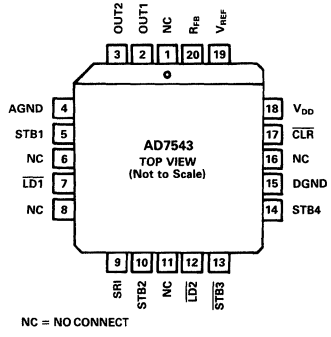
DIP



LCCC



PLCC



SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = 0, +70°C, -25°C & +85°C	Limit At[1] T_A = -55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
J, A, S Versions	±1	±1	±1	LSB max	
K, B, T Versions	±1/2	±1/2	±1/2	LSB max	
GK, GB, GT Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
J, A, S Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T_{min} to T_{max}
K, B, T Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
GK, GB, GT Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
Gain Error[2]					
J, K, A, B, S, T	±12.3	±13.5	±14.5	LSB max	Using internal RFB only
GK, GB, GT	±1	±1	±2	LSB max	
Gain Temperature Coefficient ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	µs max	To 1/2LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{LD1}$ and $\overline{LD2}$, see Figure 1.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance (pin 15)	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	Typical temperature coefficient is -300ppm/°C
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	Register B loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	Register B loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	Register B loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	Register B loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+3.0	+3.0	+3.0	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	µA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary, serial load (MSB First)				
SWITCHING CHARACTERISTICS[5]					
t_{DS1}	50	100	100	ns min	(Serial Input to Strobe Setup Time) STB1 used as a strobe
t_{DS4}	0	0	0	ns min	STB4 used as a strobe
t_{DS3}	0	0	0	ns min	$\overline{STB3}$ used as a strobe
t_{DS2}	20	40	40	ns min	STB2 used as a strobe
t_{DH1}	30	60	60	ns min	(Serial Input to Strobe Hold Time) STB1 used as a strobe
t_{DH4}	80	160	160	ns min	STB4 used as a strobe
t_{DH3}	80	160	160	ns min	$\overline{STB3}$ used as a strobe
t_{DH2}	60	120	120	ns min	STB2 used as a strobe
t_{SRI}	80	160	160	ns min	SRI data pulse width
t_{STB1}	80	160	160	ns min	STB1 pulse width
t_{STB4}	100	200	200	ns min	STB4 pulse width
t_{STB3}	100	200	200	ns min	$\overline{STB3}$ pulse width
t_{STB2}	80	160	160	ns min	STB2 pulse width
t_{LD1}, t_{LD2}	150	300	300	ns min	Load pulse width
t_{ASB}	0	0	0	ns min	Min time between strobing LSB into Register A and loading Register B
t_{CLR}	200	400	400	ns min	CLR pulse width
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	
I_{DD} (Supply Current)	2.5	2.5	2.5	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES

[1] Temperature ranges as follows: J, K, GK versions; 0 to +70°C
A, B, GB versions; -25°C to +85°C
S, T, GT versions; -55°C to +125°C

[2] See Terminology on following page.

[3] Guaranteed but not tested.

[4] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[5] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND	0V, +7V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{OUT1}, V_{OUT2} to AGND	−0.3V, V_{DD} to +0.3V
V_{REF} to AGND	±25V
V_{RFB} to AGND	±25V
Power Dissipation (Package)	
Plastic	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (J, K, GK Versions)	0 to +70°C
Industrial (A, B, GB Versions)	−25°C to +85°C
Extended (S, T, GT Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7543 would exhibit a gain of −4095/4096. Gain error is adjustable using external trims.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with Register B loaded to all 0's or at OUT 2 with Register B loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0's.

PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at AGND
3	AGND	Analog Ground
4	STB1	Register A Strobe 1 input, see Table II
5	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
6	N/C	No Connection
7	SRI	Serial Data Input to Register A
8	STB2	Register A Strobe 2 input, see Table II
9	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
10	$\overline{STB3}$	Register A Strobe 3 input, see Table II
11	STB4	Register A Strobe 4 input, see Table II
12	DGND	Digital Ground
13	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000
14	V_{DD}	+5V Supply Input
15	V_{REF}	Reference input. Can be positive or negative dc voltage or ac signal
16	R_{FB}	DAC Feedback Resistor

Table I. Pin Function Description, DIP Configuration

INTERFACE LOGIC INFORMATION

Shown in the AD7543 Functional Diagram Register A is a 12-bit shift register. Serial data appearing at pin SRI is clocked into the shift register on the leading (rising) edge of STB1, STB2 or STB4 or on the leading (falling) edge of STB3. Table II defines the various logic states required on the Register A control inputs, while Figure 1 illustrates the Register A loading sequence.

Once Register A is full, the data is transferred to Register B by bringing $\overline{LD1}$ and $\overline{LD2}$ momentarily LOW.

Register B can be asynchronously reset to 0000 0000 0000 by bringing $\overline{CLR}$ momentarily LOW. This allows the DAC output voltage to be set to a known condition, thus simplifying system initialization procedure. When operating the AD7543 in the unipolar circuit, a CLEAR causes the DAC output voltage to equal 0V. When using the bipolar circuit, a CLEAR causes the DAC output to equal $-V_{REF}$.

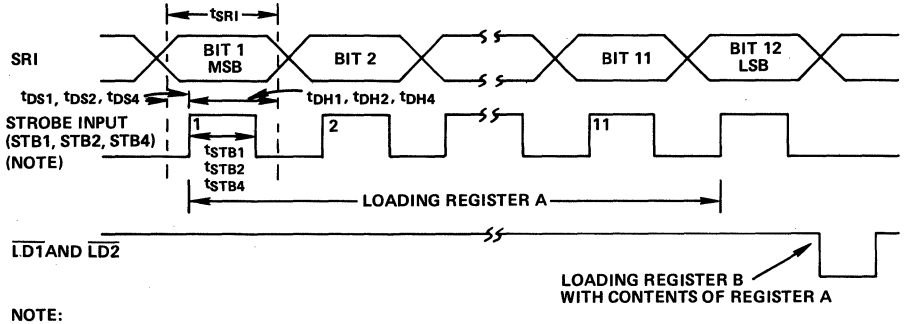


Figure 1. Timing Diagram

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↑	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1	↑	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	↓	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
↑	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↑ is positive edge ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table II. AD7543 Truth Table

ANALOG DEVICES

CMOS 12-Bit Buffered Multiplying DAC

AD7545

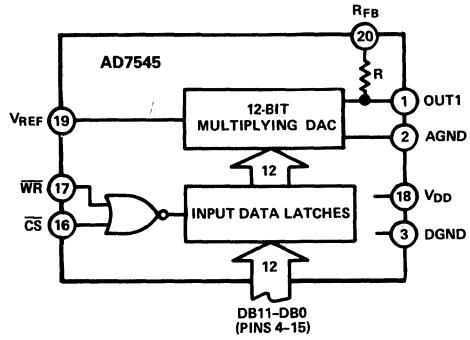
FEATURES
- 12-Bit Resolution
- Low Gain T.C.: 2ppm/°C typ
- Fast TTL Compatible Data Latches
- Single +5V to +15V Supply
- Small 20-Pin 0.3" DIP and 20-Terminal Surface Mount Packages
- Latch Free (Schottky Protection Diode Not Required)
- Low Cost
- Ideal for Battery Operated Equipment

GENERAL DESCRIPTION

The AD7545 is a monolithic 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The AD7545 is particularly suitable for single supply operation and applications with wide temperature variations.

AD7545 FUNCTIONAL BLOCK DIAGRAM



The AD7545 can be used with any supply voltage from +5V to +15V. With CMOS logic levels at the inputs the device dissipates less than 0.5mW for V_{DD} = +5V.

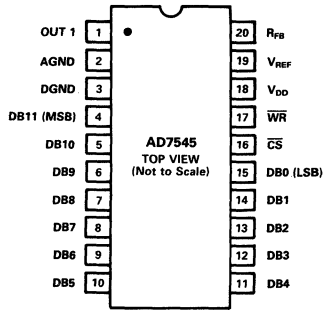
ORDERING INFORMATION[1,2]

Relative Accuracy, LSB	Maximum Gain Error, LSB T_A = +25@C V_{DD} = +5V	Temperature Range and Package Options[3] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-20)	Hermetic (Q-20)	Hermetic (Q-20)
±2	±20	AD7545JN	AD7545AQ	AD7545SQ
±1	±10	AD7545KN	AD7545BQ	AD7545TQ
±1/2	±5	AD7545LN	AD7545CQ	AD7545UQ
±1/2	±1	AD7545GLN	AD7545GCQ	AD7545GUQ
		PLCC[4] (P-20A)		LCCC[5] (E-20A)
±2	±20	AD7545JP		AD7545SE
±1	±10	AD7545KP		AD7545TE
±1/2	±5	AD7545LP		AD7545UE
±1/2	±1	AD7545GLP		AD7545GUE

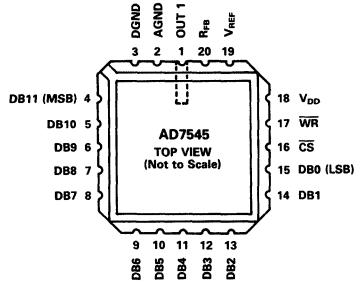
NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC drawing 5962-87702.
[2]Analog Devices reserves to right to ship ceramic packages (D-20) in lieu of cerdip packages (Q-20).
[3]See Section 14 for package outline information.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

PIN CONFIGURATIONS

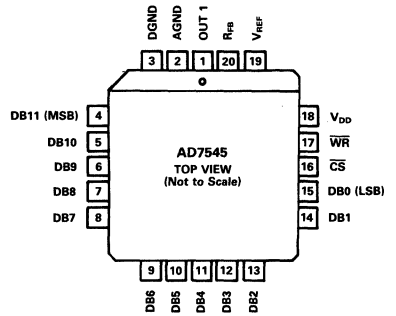
DIP



LCCC



PLCC



SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified)

Parameter	Version	V_{DD} = +5V Limits T_A = +25°C	T_{min}, T_{max} [1]	V_{DD} = +15V Limits T_A = +25°C	T_{min}, T_{max} [1]	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	J, A, S	±2	±2	±2	±2	LSB max	
	K, B, T	±1	±1	±1	±1	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB max	10-Bit Monotonic T_{min} to T_{max}
	K, B, T	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	L, C, U	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	GL, GC, GU	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
Gain Error (Using Internal RFB)[2]	J, A, S	±20	±20	±25	±25	LSB max	DAC Register Loaded with
	K, B, T	±10	±10	±15	±15	LSB max	1111 1111 1111
	L, C, U	±5	±6	±10	±10	LSB max	Gain Error is Adjustable Using
	GL, GC, GU	±1	±2	±6	±7	LSB max	the Circuits of Figures 4, 5 and 6
Gain Temperature Coefficient[3] ΔGain/ΔTemperature	All	±5	±5	±10	±10	ppm/°C max	Typical Value is 2ppm/°C for V_{DD} = +5V
DC Supply Rejection[3] ΔGain/ΔV_{DD}	All	0.015	0.03	0.01	0.02	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	J, K, L, GL	10	50	10	50	nA max	DB0-DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
	A, B, C, GC	10	50	10	50	nA max	
	S, T, U, GU	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	μs max	To 1/2LSB. OUT 1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.
Propagation Delay[3] (from Digital Input Change to 90% of final Analog Output)	All	300	–	250	–	ns max	OUT1 LOAD = 100Ω C_{EXT} = 13pF[4]
Digital to Analog Glitch Impulse	All	400	–	250	–	nV sec typ	V_{REF} = AGND
AC Feedthrough[5] At V_{OUT1}	All	5	5	5	5	mV p-p typ	V_{REF} = ±10V, 10kHz Sinewave
REFERENCE INPUT							
Input Resistance	All	7	7	7	7	kΩ min	Input Resistance TC = -300ppm/°C typ
(Pin 19 to GND)		25	25	25	25	kΩ max	Typical Input Resistance = 11kΩ
ANALOG OUTPUTS							
Output Capacitance[3]							
C_{OUT1}	All	70	70	70	70	pF max	DB0-DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT1}	All	200	200	200	200	pF max	DB0-DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[6] I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[3]							
DB0-DB11	All	5	5	5	5	pF max	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF max	V_{IN} = 0
SWITCHING CHARACTERISTICS[7]							
Chip Select to Write Setup Time	All	280	380	180	200	ns min	See Timing Diagram on next page
t_{CS}		200	270	120	150	ns typ	
Chip Select to Write Hold Time t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	250	400	160	240	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns typ	
Data Setup Time	All	140	210	90	120	ns min	
t_{DS}		100	150	60	80	ns typ	
Data Hold Time t_{DH}	All	10	10	10	10	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}
		10	10	10	10	μA typ	All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature Ranges as follows: J, K, L, GL versions; 0 to +70°C
A, B, C, GC versions; -25°C to +85°C
S, T, U, GU versions; -55°C to +125°C

[2] This includes the effect of 5ppm max gain TC.

[3] Guaranteed but not tested.

[4] DB0-DB11 = 0V to V_{DD} or V_{DD} to 0V.

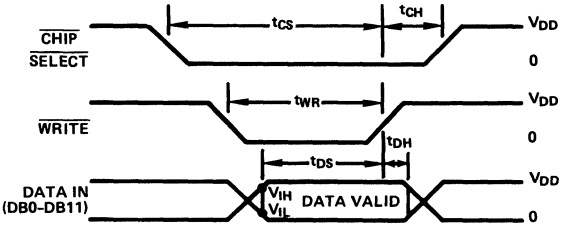
[5] Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

[6] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[7] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0–DB11) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0–DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $V_{IH} + V_{IL}/2$.

2

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V, +17V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND	±25V
V_{PIN1} to DGND	−0.3V, V_{DD} +0.3V
AGND to DGND	−0.3V, V_{DD} +0.3V
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commercial (J, K, L, GL) Grades	0 to +70°C
Industrial (A, B, C, GC) Grades	−25°C to +85°C
Extended (S, T, U, GU) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

APPLICATION HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5 volts. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

BASIC APPLICATIONS

Figures 1 and 2 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. The "G" versions (AD7545GLN, AD7545GCQ, AD7545GUD) have a guaranteed maximum gain error of ±1LSB at +25°C (V_{DD} = +5V) and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that all the circuits of Figures 1 and 2 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 1 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leqslant V_{IN} \leqslant +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table II shows the code relationship for the circuit of Figure 1.

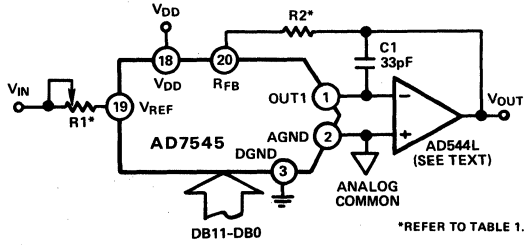


Figure 1. Unipolar Binary Operation

TRIM RESISTOR	J/A/S	K/B/T	L/C/U	GL/GC/GU
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades for V_{DD} = +5V

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 1

Figure 2 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive –OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wirewound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

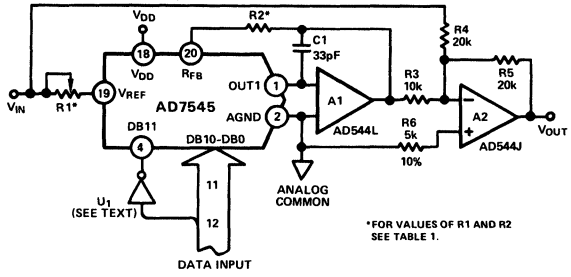


Figure 2. Bipolar Operation (2's Complement Code)

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

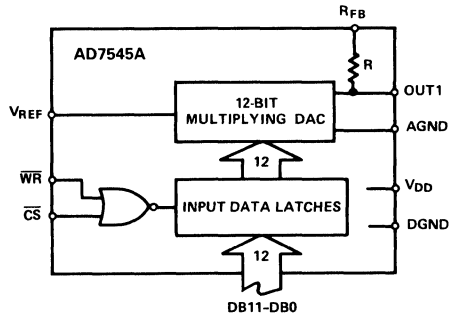
Table III. 2's Complement Code Table for Circuit of Figure 2

CMOS 12-Bit Buffered Multiplying DAC

AD7545A

FEATURES
Improved Version of AD7545
Fast Interface Timing
All Grades 12-Bit Accurate
Small 20-Pin 0.3" DIP and
20-Terminal Surface Mount Package
Low Cost

AD7545A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7545A, a 12-bit CMOS multiplying DAC with internal data latches, is an improved version of the industry standard AD7545. This new design features a $\overline{WR}$ pulse width of 100ns which allows interfacing to a much wider range of fast 8-bit and 16-bit microprocessors. It is loaded by a single 12-bit wide word under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing unbuffered operation of the DAC.

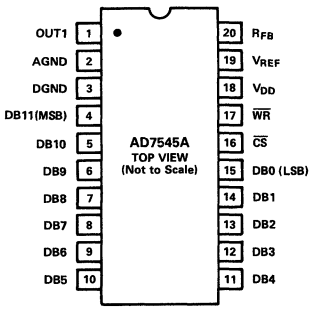
ORDERING INFORMATION[1,2]

Relative Accuracy, LSB	Gain Error, LSB	Temperature Range and Package Options[3]		
T_{min}-T_{max}	T_{min}-T_{max}	0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-20)	**Hermetic (Q-20)**	**Hermetic (Q-20)**
±1/2	±4	AD7545AKN	AD7545ABQ	AD7545ATQ
±1/2	±2	AD7545ALN	AD7545ACQ	AD7545AUQ
		PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
±1/2	±4	AD7545AKP		AD7545ATE
±1/2	±2	AD7545ALP		AD7545AUE

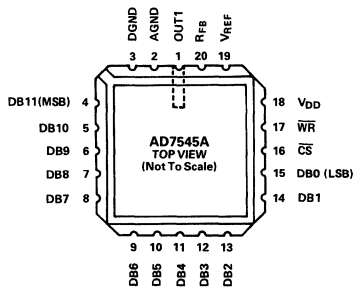
NOTES
[1]To order MIL-STD-883C, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]Analog Devices reserves the right to ship ceramic packages (D-20) in lieu of cerdip packages (Q-20).
[3]See Section 14 for package outline information.
[4]PLCC: Plastic Leaded Chip Carier.
[5]LCCC: Leadless Ceramic Chip Carrier.

PIN CONFIGURATIONS

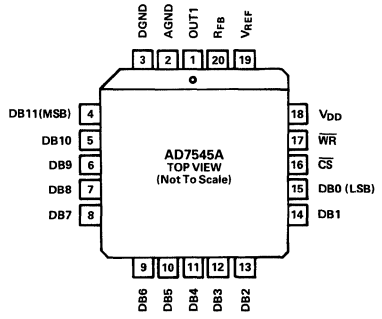
DIP



LCCC



PLCC



SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified)

Parameter	Version	V_{DD} = +5V Limits T_A = +25°C	T_{min}-T_{max}[1]	V_{DD} = +15V Limits T_A = +25°C	T_{min}-T_{max}[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	K, B, T	±1/2	±1/2	±1/2	±1/2	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	Endpoint Measurement
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed 12-Bit Monotonic Over Temperature
Gain Error	K, B, T	±3	±4	±3	±4	LSB max	Measured Using Internal R_{FB}.
	L, C, U	±1	±2	±1	±2	LSB max	DAC Register Loaded with All 1s.
Gain Temperature Coefficient[2]	All	±5	±5	±5	±5	ppm/°C max	
ΔGain/ΔTemperature	All	±2	±2	±2	±2	ppm/°C typ	
DC Supply Rejection [2]							
ΔGain/ΔV_{DD}	All	0.002	0.004	0.002	0.004	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	K, L	10	50	10	50	nA max	DB0-DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
	B, C	10	50	10	50	nA max	
	T, U	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Current Settling Time[2]	All	1	1	1	1	μs max	To 1/2LSB. OUT 1 load = 100Ω, C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.
Propagation Delay[2] (from Digital Input Change to 90% of Final Analog Output)	All	200	–	150	–	ns max	OUT1 LOAD = 100Ω, C_{EXT} = 13pF[3]
Digital-to-Analog Glitch Inpulse[2]	All	5	–	5	–	nV sec typ	V_{REF} = AGND. OUT1 Load = 100Ω, C_{EXT} = 13pF. DAC Register Alternately Loaded with All 0s and All 1s.
AC Feedthrough [2,4]							
At OUT1	All	5	5	5	5	mV p-p typ	V_{REF} = ±10V, 10kHz Sinewave
REFERENCE INPUT							
InputResistance	All	10	10	10	10	kΩ min	Input Resistance TC = −300ppm/°C typ
(Pin 19 to GND)		20	20	20	20	kΩ max	Typical Input Resistance = 15kΩ
ANALOG OUTPUTS							
Output Capacitance[2]							
C_{OUT1}	All	70	70	70	70	pF max	DB0-DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT1}	All	150	150	150	150	pF max	DB0-DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[5] I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[2]							
DB0-DB11, $\overline{WR}$, $\overline{CS}$	All	8	8	8	8	pF max	
SWITCHING CHARACTERISTICS[2]							
Chip Select to Write Setup Time	K, B, L, C	100	130	75	85	ns min	See Timing Diagram
t_{CS}	T, U	100	170	75	95	ns min	
Chip Select to Write Hold Time t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width	K, B, L, C	100	130	75	85	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
t_{WR}	T, U	100	170	75	95	ns min	
Data Setup Time t_{DS}	All	100	150	60	80	ns min	
Data Hold Time t_{DH}	All	5	5	5	5	ns min	
POWER SUPPLY							
V_{DD}	All	5	5	15	15	V	±5% for Specified Performance
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	100	100	100	μA max	All Digital Inputs 0V or V_{DD}
		10	10	10	10	μA typ	All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature Ranges as follows:

K, L versions; 0 to +70°C
B, C versions; −25°C to +85°C
T, U versions; −55°C to +125°C

[2] Sample tested to ensure compliance.

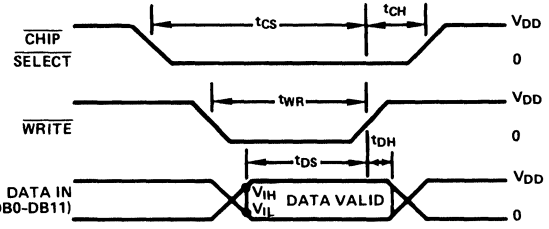
[3] DB0-DB11 = 0V to V_{DD} or V_{DD} to 0V.

[4] Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

[5] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

2

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V, +17V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND	±25V
V_{PIN1} to DGND	−0.3V, V_{DD} +0.3V
AGND to DGND	−0.3V, V_{DD} +0.3V
Power Dissipation (Any Package) to 75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commercial (K, L) Grades	0 to +70°C
Industrial (B, C) Grades	−25°C to +85°C
Extended (T, U) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 1 and 2 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this error, which adds to the D/A converter nonlinearity, depends on V_{OS}, where V_{OS} is the amplifier input offset voltage. To maintain specified accuracy with V_{REF} at 10V, it is recommended that V_{OS} be no greater than 0.25mV, or (25×10^{-6}) (V_{REF}), over the temperature range of operation. Suitable op amps are AD517 and AD711. The AD517 is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (150µV max for lowest grade) and in most applications will not require an offset trim. The AD711 has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD711 may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545A. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545A AGND and DGND pins (1N914 or equivalent).

Invalid Data: When $\overline{WR}$ and $\overline{CS}$ are both low, the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low, and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted signals or glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Digital Glitches: Digital glitches result due to capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545A (Pins 1, 2, 19, 20) from the digital pins by a ground track run between Pins 2 and 3 and between Pins 18 and 19 of the AD7545A. Note how the analog pins are at one end (DIP) or side (LCC and PLCC) of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the ditigal-to-analog sections of the AD7545A, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5 volts. However, great care should be taken to ensure that the +5V used to power the AD7545A is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545A has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 (such as in Figure 4) are used to adjust full-scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient to CMOS Multiplying DACs", Publication Number E630c–5–3/86.

BASIC APPLICATIONS

Figures 1 and 2 show simple unipolar and bipolar circuits using the AD7545A. Resistor R1 is used to trim for full scale. The L, C, U grades have a guaranteed maximum gain error of ±1LSB at +25°C, and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high-speed op amps. Note that all the circuits of Figures 1 and 2 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 1 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table II shows the code relationship for the circuit of Figure 1.

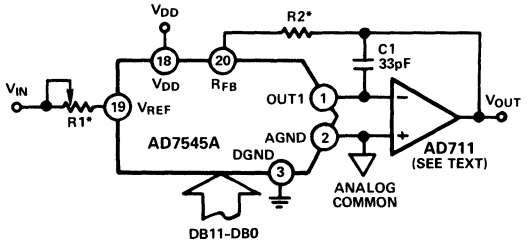


Figure 1. Unipolar Binary Operation

TRIM RESISTOR	K, B, T	L, C, U
R1	50Ω	20Ω
R2	27Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 1.

Figure 2 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code, and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive – OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01%, and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full-scale error. Mismatch of R5 to R4 causes full-scale error.

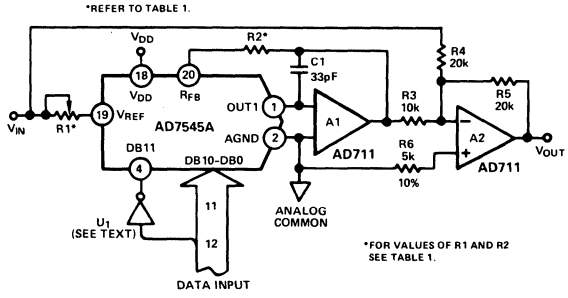


Figure 2. Bipolar Operation (2's Complement Code)

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Table III. 2's Complement Code Table for Circuit of Figure 2.

ANALOG DEVICES

LC²MOS Parallel Loading Dual 12-Bit DAC

AD7547

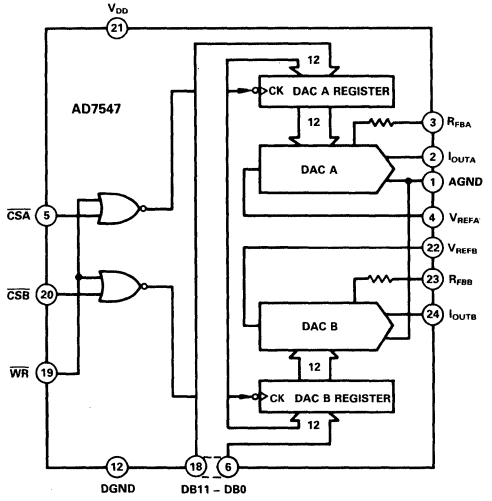
FEATURES

Two 12-Bit DACs in One Package
DAC Ladder Resistance Matching: 0.5%
Space Saving Skinny DIP and Surface Mount Packages
4-Quadrant Multiplication
Low Gain Error (1LSB max Over Temperature)
Fast Interface Timing

APPLICATIONS

Automatic Test Equipment
Programmable Filters
Audio Applications
Synchro Applications
Process Control

AD7547 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7547 contains two 12-bit current output DACs on one monolithic chip. Also on-chip are the level shifters, data registers and control logic for easy microprocessor interfacing. There are 12 data inputs. $\overline{CSA}$, $\overline{CSB}$, $\overline{WR}$ control DAC selection and loading. Data is latched into the DAC registers on the rising edge of $\overline{WR}$. The device is speed compatible with most microprocessors and accepts TTL, 74HC and 5V CMOS logic level inputs.

The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Monolithic construction ensures that thermal and gain error tracking is excellent. 12-bit monotonicity is guaranteed for both DACs over the full temperature range.

The AD7547 is manufactured using the Linear Compatible CMOS (LC²MOS) process. This allows fast digital logic and precision linear circuitry to be fabricated on the same die.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching:
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Small Package Size:
   The AD7547 is available in both 0.3" wide, 24-pin DIPs and in 28-terminal surface mount packages.
3. Wide Power Supply Tolerance:
   The device operates on a +12V to +15V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC from the Data Bus
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

NOTES
1. X = Don't care
2. ↓ means rising edge triggered

Table I. AD7547 Truth Table

SPECIFICATIONS[1] (V_{DD} = +12V to +15V, ±10%, V_{REFA} = V_{REFB} = 10V; I_{OUTA} = I_{OUTB} = AGND = 0V. All specifications T_{min} to T_{max} unless otherwise specified.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1's.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current I_{OUTA} (Pin 2)								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0's.
I_{OUTB} (Pin 24)								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{min} to T_{max}	150	150	150	250	250	250	nA max	with all 0's.
REFERENCE INPUT								
Input Resistance (Pin 4, Pin 22)	9 20	9 20	9 20	9 20	9 20	9 20	kΩ min kΩ max	Typical Input Resistance = 14kΩ
V_{REFA}, V_{REFB} Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12V to +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V. Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full-scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from rising edge of $\overline{WR}$. Typical Value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	7	–	nV-s typ	Measured with V_{REFA} = V_{REFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20Vp-p 10kHz sinewave. DAC
V_{REFB} to I_{OUTB}	−70	−65	dB max	registers loaded with all 0's.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max − V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−84	–	dB typ	V_{REFA} = 20V p-p 10kHz sinewave, V_{REFB} = 0V. Both DACs loaded with all 1's.
V_{REFB} to I_{OUTA}	−84	–	dB typ	V_{REFB} = 20V p-p 10kHz sinewave, V_{REFA} = 0V. Both DACs loaded with all 1's.
Digital Crosstalk	7	–	nV-s typ	Measured for a Code Transition of all 0's to all 1's. I_{OUTA}, I_{OUTB} Load = 100Ω, C_{EXT} = 13pF
Output Noise Voltage Density (10Hz-100kHz)	25	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10Hz–100kHz.
Total Harmonic Distortion	−82	–	dB typ	V_{IN} = 6V rms, 1kHz. Both DACs loaded with all 1's.

NOTES

[1]Temperature range as follows: J, K, L Versions: −40°C to +85°C.
A, B, C Versions: −40°C to +85°C.
S, T, U Versions: −55°C to +125°C.

[2]Sample tested at 25°C to ensure compliance.

[3]Functional at V_{DD} = 5V with degraded specifications.

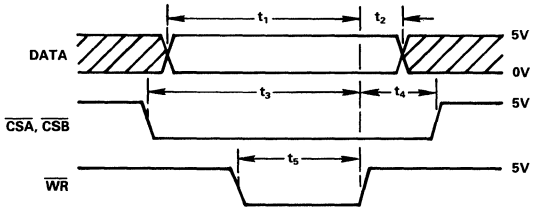
[4]Pin 12 (DGND) on ceramic DIP packages is connected to lid.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = 10.8V to 16.5V, V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V).

Parameter	Limit at T_A = +25°C	Limit at T_A = −40°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	60	80	80	ns min	Data Setup Time
t_2	25	25	25	ns min	Data Hold Time
t_3	80	80	100	ns min	Chip Select to Write Setup Time
t_4	0	0	0	ns min	Chip Select to Write Hold Time
t_5	80	80	100	ns min	Write Pulse Width

NOTE
Specifications subject to change without notice.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. t_r = t_f = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH}+V_{IL}}{2}$

Figure 1. Timing Diagram for AD7547

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} to AGND, ... ±25V
V_{RFBA}, V_{RFBB} to AGND, ... ±25V
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
I_{OUTA}, I_{OUTB} to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C
Operating Temperature Range
Commercial (J, K, L Versions) . . . . . −40°C to +85°C
Industrial (A, B, C Versions) . . . . . −40°C to +85°C
Extended (S, T, U Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION[1,2]

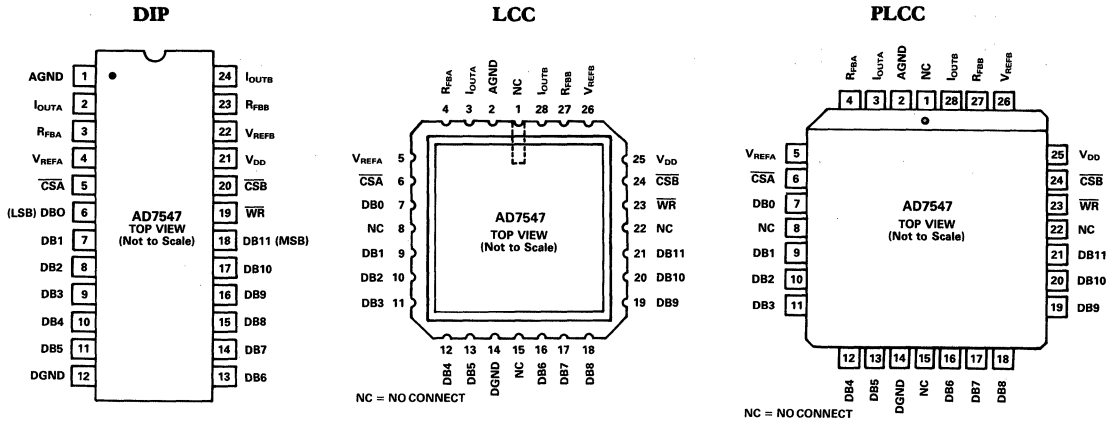
Relative Accuracy T_{min} to T_{max}	Gain Error T_{min} to T_{max}	Temperature Range and Package Options[3]		
		−40°C to +85°C Plastic DIP (N-24)	−40°C to +85°C Hermetic (Q-24)	−55°C to +125°C Hermetic (Q-24)
±1LSB	±6LSB	AD7547JN	AD7547AQ	AD7547SQ
±1/2LSB	±3LSB	AD7547KN	AD7547BQ	AD7547TQ
±1/2LSB	±1LSB	AD7547LN	AD7547CQ	
±1/2LSB	±2LSB			AD7547UQ
		PLCC[4] (P-28A)		LCCC[5] (E-28A)
±1LSB	±6LSB	AD7547JP		AD7547SE
±1/2LSB	±3LSB	AD7547KP		AD7547TE
±1/2LSB	±1LSB	AD7547LP		
±1/2LSB	±2LSB			AD7547UQ

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheets.
[2]Analog Devices reserves the right to ship ceramic packages (D-24A)in lieu of cerdip packages (Q-24).
[3]See Section 14 for package outline information.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	AGND	Analog Ground.
2	I_{OUTA}	Current output terminal of DACA.
3	R_{FBA}	Feedback resistor for DACA.
4	V_{REFA}	Reference input to DACA.
5	$\overline{CSA}$	Chip Select Input for DAC A. Active low.
6-18	DB0-DB11	12 data inputs, DB0 (LSB) – DB11 (MSB).
12	DGND	Digital Ground.
19	$\overline{WR}$	Write Input. Data transfer occurs on rising edge of $\overline{WR}$. See Table I.
20	$\overline{CSB}$	Chip Select Input for DACB. Active low.
21	V_{DD}	Power supply input. Nominally + 12V to + 15V with ± 10% tolerance.
22	V_{REFB}	Reference input to DACB.
23	R_{FBB}	Feedback resistor of DACB.
24	I_{OUTB}	Current output terminal of DACB.

CIRCUIT INFORMATION

D/A SECTION

The AD7547 contains two identical 12-bit multiplying D/A converters. Each DAC consists of a highly stable R-2R ladder and 12 N-channel current steering switches. Figure 2 shows a simplified D/A circuit for DAC A. In the R-2R ladder, binary weighted currents are steered between I_{OUTA} and AGND. The current flowing in each ladder leg is constant, irrespective of switch state. The feedback resistor R_{FBA} is used with an op-amp to convert the current flowing in I_{OUTA} to a voltage output.

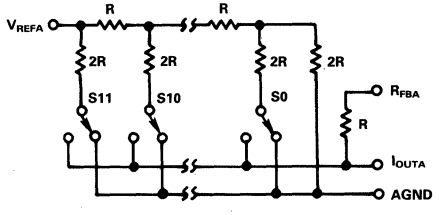


Figure 2. Simplified Circuit Diagram for DACA

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for one of the D/A converters (DAC A) in the AD7547. A similar equivalent circuit can be drawn for DACB. Note that AGND is common to both DAC A and DAC B.

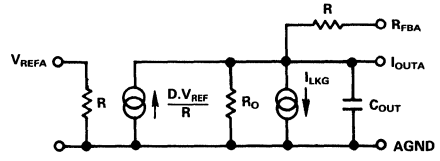


Figure 3. Equivalent Analog Circuit for DACA

C_{OUT} is the output capacitance due to the N-channel switches and varies from about 50pF to 150pF with digital input code. The current source I_{LKG} is composed of surface and junction leakages and approximately doubles every 10°C. R_0 is the equivalent output resistance of the device which varies with input code.

DIGITAL CIRCUIT INFORMATION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA.

ANALOG DEVICES

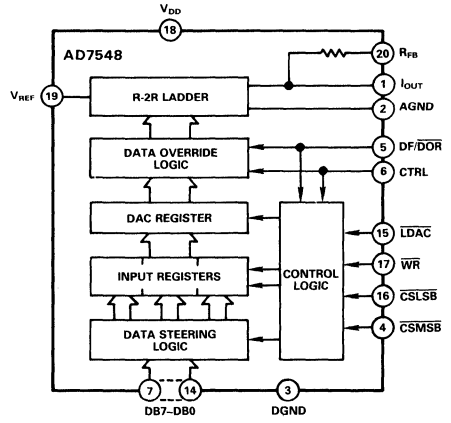
LC²MOS 8-Bit µP-Compatible 12-Bit DAC

AD7548

FEATURES
- 8-Bit Bus Compatible 12-Bit DAC
- All Grades 12-Bit Monotonic Over Full Temperature Ranges
- Operation Specified at +5V, +12V or +15V Power Supply
- Low Gain Drift of 5ppm/°C Maximum
- Full 4 Quadrant Multiplication
- Skinny DIP and Surface Mount Packages

APPLICATIONS
- 8-Bit Microprocessor Based Control Systems
- Programmable Amplifiers
- Function Generation
- Servo Control

AD7548 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7548 is a 12-bit monolithic CMOS D/A converter for use with 8-bit bus microprocessors. Data is loaded in two bytes to input holding registers as shown in the block diagram opposite. The AD7548 can be configured to accept either left- or right-justified data, least significant byte or most significant byte first, using standard TTL compatible control inputs.

A separate load DAC control input allows the user the choice of updating the analog output coincident with loading new data to the DAC input register or at any time after the data loading event. This feature is especially important in multi-DAC systems where simultaneous update of all DACs is required.

The new Linear Compatible CMOS (LC²MOS) process used in the manufacture of the AD7548 allows precision thin-film linear circuitry and high-speed low-power CMOS logic to be integrated on the same small chip. The high-speed logic allows direct interfacing to most of the popular 8-bit microprocessors.

PRODUCT HIGHLIGHTS

1. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allow direct interfacing to most of the popular 8-bit microprocessors.
2. Guaranteed Monotonicity
   The AD7548 is guaranteed monotonic to 12-bits over the full temperature range for all grades and at all specified supply voltages.
3. Selectable Data Input Format
   Left- or right-justified data, least significant or most significant byte first. This allows the AD7548 to be interfaced with microprocessors using either Motorola or Intel-type data formatting.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3″ 20-pin DIP and 20-terminal surface mount packages.
5. Single Supply Operation – See Figure 8.
6. Low Gain Error and Gain Error T.C.

SPECIFICATIONS[1] (V_{DD} = +5V, V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V. All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1/2	±1	±1/2	LSB max	All grades guaranteed monotonic to 12-bits over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC. Full Scale Error can be trimmed to zero.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 2ppm/°C
Output Leakage Current I_{OUT} (Pin 1)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs = 0V
T_{min} to T_{max}	±25	±25	±150	±150	nA max	
REFERENCE INPUT						
Input Resistance, Pin 19	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	20	20	20	20	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/V max	Specifications guaranteed over this range
I_{DD}	2	2	2	2	mA max	All digital inputs V_{IL} or V_{IH}
	300	300	300	300	μA max	All digital inputs 0V or V_{DD}

SPECIFICATIONS[1] (V_{DD} = +12V to +15V, V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V. All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1/2	±1	±1/2	LSB max	All grades guaranteed monotonic to 12-bits over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC. Full Scale Error can be trimmed to zero.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 2ppm/°C
Output Leakage Current I_{OUT} (Pin 1)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs = 0V
T_{min} to T_{max}	±25	±25	±150	±150	nA max	
REFERENCE INPUT						
Input Resistance, Pin 19	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	20	20	20	20	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specifications guaranteed over this range
I_{DD}	3	3	3	3	mA max	All digital inputs V_{IL} or V_{IH}
	1	1	1	1	mA max	All digital inputs 0V or V_{DD}

NOTES

[1]Temperature range as follows: J, K versions: 0 to +70°C
A, B versions: −40°C to +85°C
S, T versions: −55°C to +125°C

[2]Guaranteed by design but not production tested.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V, V_{REF} = +10V, V_{PIN1} = V_{PIN2} = 0V unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit[2] at T_A = 0 to +70°C −40°C to +85°C	Limit[2] at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{DS}	240	240	290	ns min	Data Valid Setup Time
t_{DH}	50	50	70	ns min	Data Valid Hold Time
t_{CWS}	30	40	50	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_{CWH}	15	20	25	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_{LWS}	30	40	50	ns min	$\overline{LDAC}$ to $\overline{WR}$ Setup Time
t_{LWH}	15	20	25	ns min	$\overline{LDAC}$ to $\overline{WR}$ Hold Time
t_{WR}	250	280	320	ns min	Write Pulse Width

TIMING CHARACTERISTICS[1] (V_{DD} = +12V to +15V, V_{REF} = +10V, V_{PIN1} = V_{PIN2} = 0V unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit[2] at T_A = 0 to +70°C −40°C to +85°C	Limit[2] at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{DS}	160	190	230	ns min	Data Valid Setup Time
t_{DH}	30	30	50	ns min	Data Valid Hold Time
t_{CWS}	30	40	50	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_{CWH}	15	20	25	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_{LWS}	30	40	50	ns min	$\overline{LDAC}$ to $\overline{WR}$ Setup Time
t_{LWH}	15	20	25	ns min	$\overline{LDAC}$ to $\overline{WR}$ Hold Time
t_{WR}	170	200	240	ns min	Write Pulse Width

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V, Output Amplifier is AD544 except where stated)

Parameter	Version	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_A = T_{MIN}, T_{MAX}	V_{DD} = +12V to +15V T_A = +25°C	V_{DD} = +12V to +15V T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time		1.5	–	1	–	µs typ	To 0.01% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s
Digital to Analog Glitch Impulse		400	–	330	–	nV-sec typ	Measured with V_{REF} = 0V, I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s
Multiplying Feedthrough Error[3]		3	5	3	5	mV p-p typ	V_{REF} = ±5V, 10kHz sine wave DAC register loaded with all 0s.
Total Harmonic Distortion		−85	–	−85	–	dB typ	V_{REF} = 6V rms @ 1kHz. DAC register loaded with all 1s.
Power Supply Rejection $\Delta GAIN/\Delta V_{DD}$		±0.015	±0.03	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance I_{OUT} (Pin 1)		200 100	200 100	200 100	200 100	pF max pF max	DAC register loaded with all 1s. DAC register loaded with all 0s.
Output Noise Voltage Density (10Hz–100kHz)		15	–	15	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES
[1]Guaranteed by design but not production tested.
[2]Temperature range as follows: J, K versions: 0 to +70°C
A, B versions: −40°C to +85°C
S, T versions: −55°C to +125°C
[3]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (D-20) to DGND.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (pin 18) to DGND	+17V
V_{REF} (pin 19) to AGND	±25V
V_{RFB} (pin 20) to AGND	±25V
Digital Input Voltage (pins 4–17) to DGND	−0.3V, V_{DD}+0.3V
$V_{PIN\ 1}$ to DGND	−0.3V, V_{DD}+0.3V
AGND to DGND	−0.3V, V_{DD}+0.3V
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	
Commercial (J, K versions)	0 to +70°C
Industrial (A, B versions)	−40°C to +85°C
Extended (S, T versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

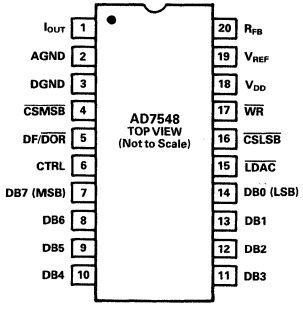
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

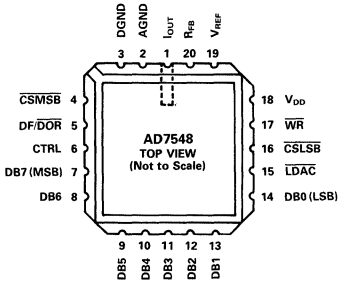
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

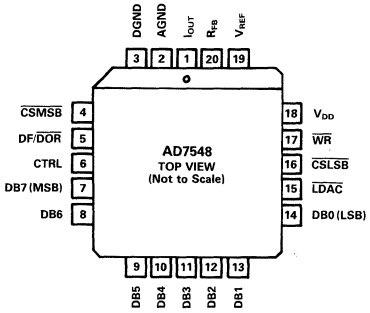
DIP



LCCC



PLCC



ORDERING INFORMATION[1,2]

Relative Accuracy T_{min}–T_{max}	Full-Scale Error T_{min}–T_{max}	Temperature Range and Package Options[3] 0 to +70°C	−40°C to +85°C	−55°C to +125°C
		Plastic DIP (N-20)	**Hermetic (Q-20)**	**Hermetic (Q-20)**
±1LSB	±6LSB	AD7548JN	AD7548AQ	AD7548SQ
±1/2LSB	±3LSB	AD7548KN	AD7548BQ	AD7548TQ
		PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
±1LSB	±6LSB	AD7548JP		AD7548SE
±1/2LSB	±3LSB	AD7548KP		AD7548TE

NOTES

[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.

[2]Analog Devices reserves the right to ship ceramic (package outline D-20) packages in lieu of cerdip (package outline Q-20) packages.

[3]See Section 14 for package outline information.

[4]PLCC: Plastic Leaded Chip Carrier.

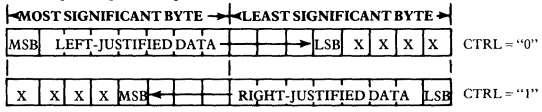
[5]LCCC: Leadless Ceramic Chip Carrier.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	I_{OUT}	DAC current OUT bus. Normally terminated at virtual ground of output amplifier.
2	AGND	Analog Ground.
3	DGND	Digital Ground.
4	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active Low Input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
5	DF/$\overline{DOR}$	Data Format/Data Override. When this input is LOW, data in the DAC register is forced to one of two override codes selected by CTRL. When the override signal is removed, the DAC output returns to reflect the value in the DAC register. With DF/$\overline{DOR}$ HIGH, CTRL selects either a left or right justified input data format. For normal operation, DF/$\overline{DOR}$ is held HIGH.

DF/$\overline{DOR}$	CTRL	FUNCTION
0	0	DAC register contents overridden by all 0's
0	1	DAC register contents overriden by all 1's
1	0	Left-justified input data selected
1	1	Right-justified input data selected

6	CTRL	Control Input. See pin 5 description.



X = Don't care states.

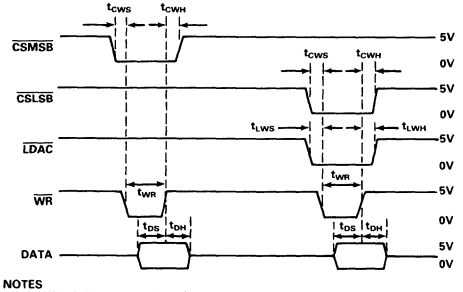
7	DB7	Data Bit 7. Most Significant Bit (MSB).
8	DB6	Data Bit 6.
9	DB5	Data Bit 5.
10	DB4	Data Bit 4.
11	DB3	Data Bit 3.
12	DB2	Data Bit 2.
13	DB1	Data Bit 1.
14	DB0	Data Bit 0. Least Significant Bit (LSB).
15	$\overline{LDAC}$	Load DAC Input, active LOW. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus.
16	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
17	$\overline{WR}$	WRITE Input. This active low signal, in combination with others is used in loading external data into the AD7548 input register and in transferring data from the input register to the DAC register.

$\overline{WR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	FUNCTION
0	1	0	1	Load LS Byte to Input Register.
0	1	0	0	Load LS Byte to Input Register and DAC Register.
0	0	1	1	Load MS Byte to Input Register.
0	0	1	0	Load MS Byte to Input Register and DAC Register.
0	1	1	0	Load Input Register to DAC Register.
1	X	X	X	No Data Transfer

18	V_{DD}	+5V to +15V Supply Input.
19	V_{REF}	Reference Voltage Input.
20	R_{FB}	Feedback Resistor. Used for normal D/A conversion.

CONTROL INPUT INFORMATION

Figure 1a shows the data load timing diagram for the AD7548. Figure 1b shows the simplified input control structure of the AD7548.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. $\overline{CSMSB}$ (PIN 4) AND $\overline{CSLSB}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/$\overline{DOR}$ = +5V. FOR RIGHT-JUSTIFIED DATA CTRL = +5V WITH DF/$\overline{DOR}$ = +5V.

Figure 1a. AD7548 Timing Diagram

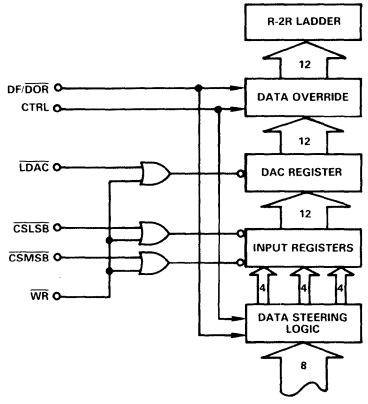


Figure 1b. Simplified AD7548 Input Control Structure

GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 2. An inverted R-2R ladder structure is used, which steers binarily weighted currents between I_{OUT} and AGND, thus maintaining a constant current in each ladder leg independent of the switch state.

The input resistance at V_{REF} is constant and equal to the value "R" in Figure 2. Since the input resistance is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor).

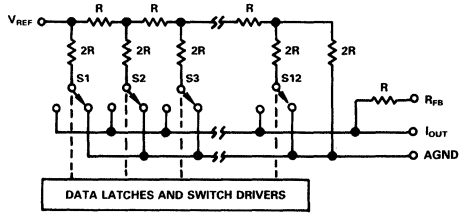


Figure 2. AD7548 Simplified Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7548 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O, denotes the equivalent output resistance of the DAC which varies with input code (excluding all 0's code) from 0.8R to 2R, where R is typically 11kΩ. C_{OUT} is the capacitance due to the current steering switches and varies from about 50pF to 120pF (typical values) depending upon the digital input. g(V_{REF}, N) is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of R-2R ladder, N.

For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

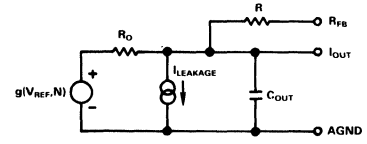


Figure 3. AD7548 Equivalent Analog Output Circuit

DATA LOADING

The AD7548 accepts incoming data in either left-justified format or right-justified format depending on the control inputs DF/$\overline{DOR}$ and CTRL.

(See pin description of DF/$\overline{DOR}$ and CTRL on preceding page).

Two operating modes are possible for controlling the transfer of data from the input register to the DAC register, the automatic transfer mode and the strobed transfer mode.

AUTOMATIC TRANSFER MODE

This is the simplest and fastest method of transferring data to the DAC register. It is facilitated by connecting $\overline{LDAC}$ to either $\overline{CSMSB}$, as shown in Figure 10, or $\overline{CSLSB}$.

Figure 4 shows the timing diagram for automatic transfer of 8 +4-bit data to the DAC register. The first write cycle loads the first byte of data to the input register. The second write cycle loads the second byte of data to the input register and automatically transfers both bytes to the DAC register.

Updating a single byte (High or Low) in the DAC register can be achieved in one write cycle using the automatic transfer mode.

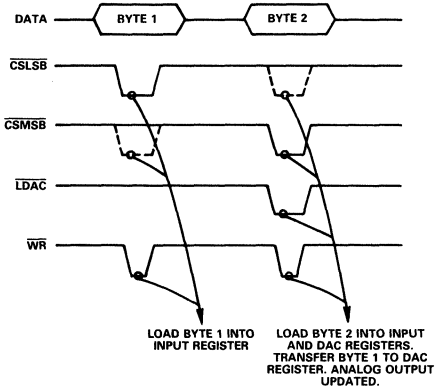


Figure 4. Automatic Transfer Mode

STROBED TRANSFER MODE

Figure 5 shows the timing diagram for the strobed transfer of 8 +4-bit data to the DAC register. Three write cycles are required for this transfer mode. The first two write cycles sequentially load bytes 1 and 2 into the input register. The third write cycle transfers data from the input register to the DAC register.

The strobed transfer mode allows the DAC registers of several AD7548's to be updated simultaneously, as shown in Figure 13, by means of a master strobe signal connected to the $\overline{LDAC}$ of each device.

A single byte of data (High or Low) can be transferred to the DAC register in two write cycles using the strobed transfer mode.

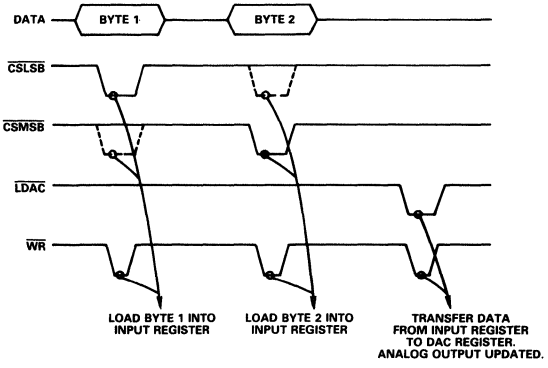


Figure 5. Strobed Transfer Mode

DATA OVERRIDE

The contents of the DAC register can be overridden by pulling DF/$\overline{DOR}$ (pin 5) LOW. The CTRL (pin 6) input then determines whether the DAC register data is overidden by all 0s (CTRL LOW) or all 1s (CTRL HIGH). This feature allows the user to calibrate the AD7548 in circuits such as Figure 6 without calling on the microprocessor to load calibration data.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary operation. With a dc input voltage or current (positive or negative polarity) applied at pin 19, the circuit is a unipolar D/A converter. With an ac input voltage the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

Table I shows the code relationship for the circuit of Figure 6.

For full scale trimming the DAC register is loaded with 1111 1111 1111. This is most easily accomplished by using the data override function. R1 is then adjusted for $V_{OUT} = -V_{IN}$ (4095/4096). Alternatively full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps.

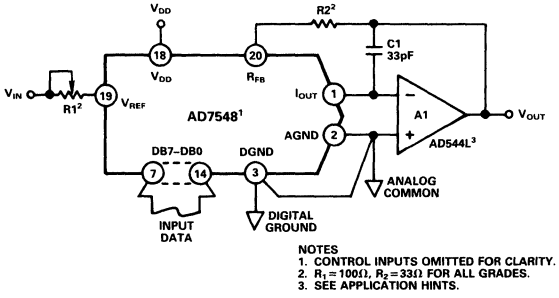


Figure 6. Unipolar Binary Operation

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table I. Unipolar Binary Code Table for Circuit of Figure 6

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The circuit uses offset binary input coding. However, 2's complement coding can be accommodated if the MSB is inverted (done in software) before data is loaded into the DAC.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively one can omit R1 and R2 and adjust the ratio of R3 and R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5.

R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably metal film) so that their temperature coefficients match. Mismatch of R3 to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

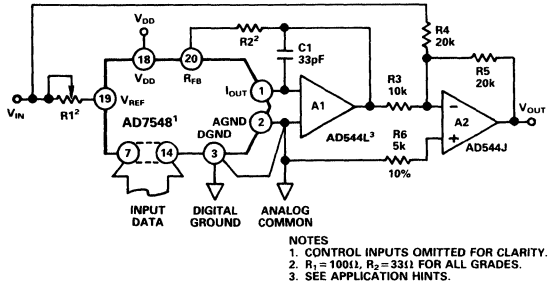


Figure 7. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 7

SINGLE SUPPLY OPERATION

Figure 8 shows the AD7548 connected in a voltage switching mode. The input voltage is connected to I_{OUT}. The D/A converter output voltage is taken from the V_{REF} pin and has a constant impedance equal to R. R_{FB} is not used in this circuit. The input voltage V_{IN} must always be positive with respect to AGND in order to prevent an internal diode from turning on. To maintain linearity the input voltage should remain within 2.5V of AGND with V_{DD} from +12V to +15V.

The output voltage V_{OUT} of Figure 8 is expressed as

$$V_{OUT} = (V_{IN})\,(D)\left(\frac{R_1 + R_2}{R_1}\right)$$

Where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

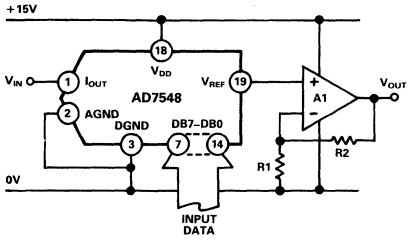


Figure 8. Single Supply Operation Using Voltage Switching Mode

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 6 and 7 exhibit a code dependent output resistance which in turn cause a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which, depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7548. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7548 AGND and DGND pins (1N914 or equivalent).

Temperature Coefficients: The gain temperature coefficient of the AD7548 has a maximum value of 5ppm/°C and typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

High Frequency Considerations: AD7548 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

Feedthrough: The dynamic performance of the AD7548 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 6 is shown in Figure 9 which minimizes feedthrough from V_{REF} to the output in multiplying applications.

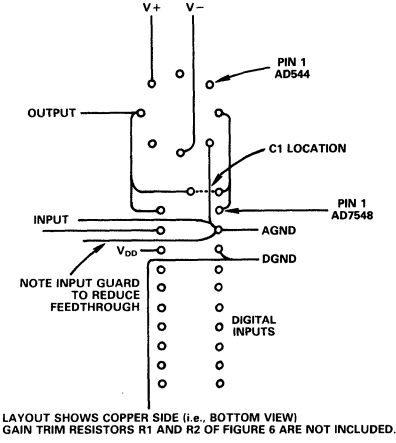


Figure 9. Suggested Layout for AD7548 and Op Amp

For additional information on multiplying DACs refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.

MICROPROCESSOR INTERFACING

AD7548 – MC6800 INTERFACE

A typical 6800 configuration using the automatic transfer mode of the AD7548 is shown in Figure 10. Table III gives a sample loading routine written in re-entrant form. Data load and store instructions use extended addressing. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY + 1. The data is considered right-justified with the four most significant bits occupying the lower half of XXYY + 1. The AD7548 is assigned a base address of PPQQ. This address selects the low byte register of the AD7548. Address PPQQ + 1 selects both the high byte register and the $\overline{\text{LDAC}}$ control input.

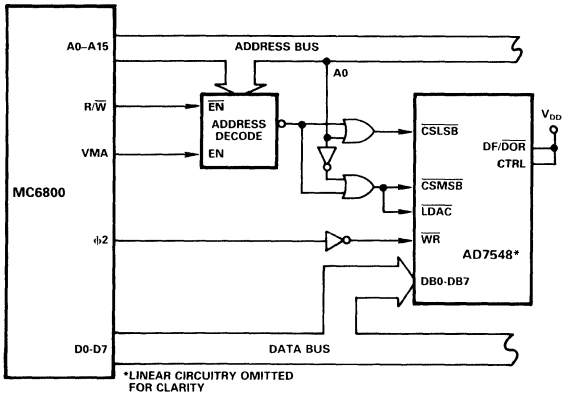


Figure 10. AD7548 – MC6800 Interface (Automatic Transfer Mode)

	JSR	WWZZ	Jump to AD7548 subroutine
WWZZ	PSH A		Push A onto stack
	TPA		
	PSH A		Push CCR onto stack
	LDA A	$XXYY	
	STA A	$PPQQ	Load low byte to AD7548
	LDA A	$XXYY + 1	
	STA A'	$PPQQ + 1	Load high byte to AD7548 and update analog output
	PUL A		
	TAP		Pull CCR from stack
	PUL A		Pull A from stack
	RTS		Return to main program

Table III. Sample Routine for AD7548 – MC6800 Interface

AD7548 – 8085A INTERFACE

Figure 11 shows a typical AD7548 to 8085A microprocessor interface configured for automatic transfer of 8 + 4-bit right-justified data. Table IV gives a sample loading routine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY + 1. The four most significant data bits occupy the lower half of XXYY + 1. As before, addresses PPQQ and PPQQ + 1 select the $\overline{\text{CSLSB}}$ and $\overline{\text{CSMSB}}/\overline{\text{LDAC}}$ control inputs respectively. Since only two instructions (LHLD, SHLD) are required to both fetch and load the 12-bit data word to the AD7548, it may be more efficient to insert these instructions as required in the main program rather than use a subroutine such as illustrated here.

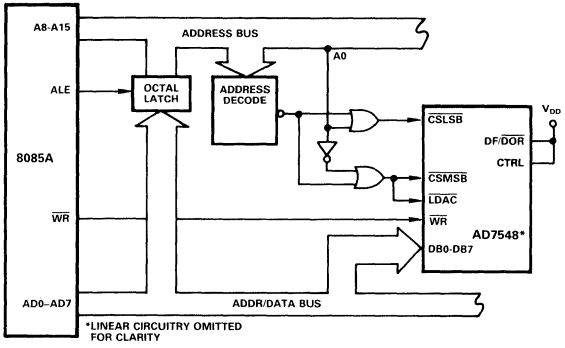


Figure 11. AD7548 – 8085A Interface (Automatic Transfer Mode)

	CALL	7548	
7548	PUSH	PSW	Push register contents onto stack
	PUSH	H	
	LHLD	XXYY	Fetch 12-bit data
	SHLD	PPQQ	Load 12-bit data
	POP	H	Pop register contents from stack
	POP	PSW	
	RET		Return to main program

Table IV. Sample Routine for AD7548–8085A Interface

AD7548 – MC6809 INTERFACE

The AD7548 can be interfaced to the MC6809 microprocessor as shown in Figure 12 for automatic transfer of 8 +4-bit data. Similar to the 8085A instructions LHLD and SHLD, the 6809 has two instructions to fetch and store 12-bit (16-bit) data to the AD7548, LDD and STD. However, in the 6809, the high byte of data is moved first, then the low byte (this is the opposite of the 8085A). This means that if the 12-bit data is assumed to reside at addresses XXYY and XXYY+1 then XXYY must contain the high byte. It also means that the address decoding logic of Figure 11 must be slightly changed so that the even-order AD7548 address, PPQQ from before, selects the $\overline{CSMSB}$ input to load the high byte first. In this automatic transfer configuration $\overline{LDAC}$ is tied to the $\overline{CSLSB}$ input. The AD7548 analog output can thus be updated using only two instructions as follows:

```
LDD     $XXYY
STD     $PPQQ
```

The strobed transfer configuration is shown in Figure 13 with a dedicated decoder output assigned to each chip select input. The common $\overline{LDAC}$ signal allows simultaneous update of both AD7548 DAC registers.

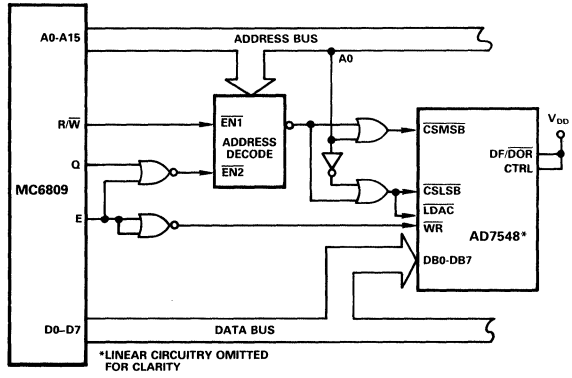


Figure 12. AD7548 – MC6809 Interface (Automatic Transfer Mode)

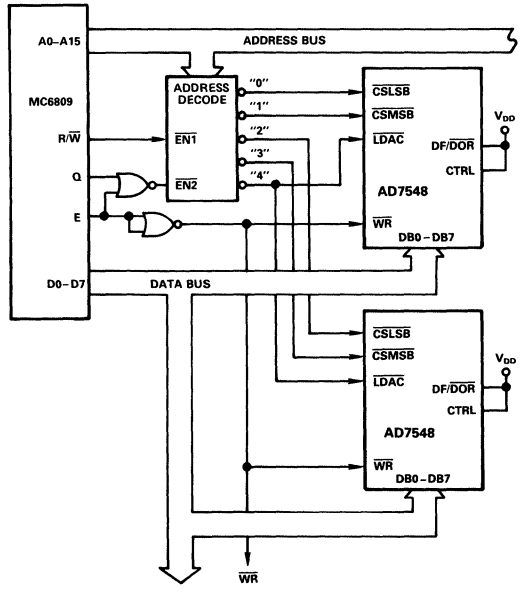


Figure 13. AD7548 – MC6809 Interface (Strobed Transfer Mode)

AD7548 – 6502 INTERFACE

Figure 14 shows a typical AD7548 to 6502 microprocessor interface configured for automatic transfer of right-justified data. As a programming example, Figure 15 shows a flow chart for producing a 12-bit (4095-step-max) voltage ramp under 6502 control. Index registers X and Y of the 6502 form a 12-bit counter with the X-register holding the low byte of data and the Y-register the high byte. Table V shows the program listing. The X-register is compared with FF_H and the Y-register with 10_H to determine when the ramp voltage has reached its maximum value (FFF_H). By changing the comparison data in the program the maximum ramp output voltage can be varied from levels corresponding to FFF_H down to 000_H. In the program listing of Table V the AD7548 has been assigned contiguous addresses 0400 (low byte) and 0401 (high byte and DAC register).

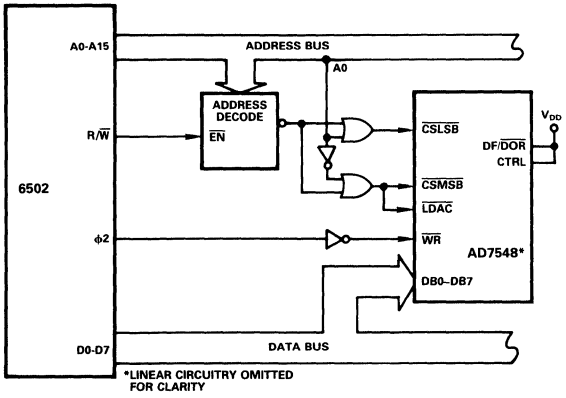


Figure 14. AD7548 – 6502 Interface (Automatic Transfer Mode)

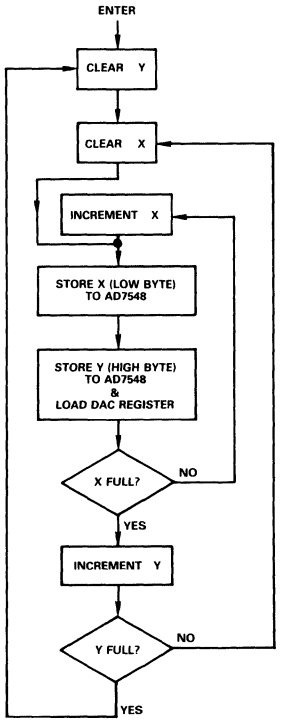


Figure 15. Flow Chart for Voltage Ramp Generation

ADDRESS	OP-CODE	MNEMONIC	OPERAND
0000	A0	LDY	# 00
01	00		
02	A2	LDX	# 00
03	00		
04	4C	JMP	0008
05	08		
06	00		
07	E8	INX	
08	8E	STX	0400
09	00		
0A	04		
0B	8C	STY	0401
0C	01		
0D	04		
0E	E0	CPX	# FF
0F	FF		
10	D0	BNE	0007
11	F5		
12	C8	INY	
13	C0	CPY	# 10
14	10		
15	D0	BNE	0002
16	EB		
17	FO	BEQ	0000
0018	E7		

Table V. Program Listing for Figure 15

AD7548 – Z80 INTERFACE

Figure 16 shows a typical AD7548 to Z80 microprocessor interface configured for automatic transfer of right-justified data. Similar to the 8085A and 6809 cases, 16-bit load instructions are available in the Z80 which can fetch and load 12-bit data to the AD7548. Since the low byte of data is moved first and assuming the 12-bit data resides at addresses XXYY and XXYY + 1, address XXYY must contain the low byte. As before, addresses PPQQ and PPQQ + 1 select the AD7548 $\overline{\text{CSLSB}}$ and $\overline{\text{CSMSB}}$/$\overline{\text{LDAC}}$ control inputs respectively. Choosing the Z80 register pair BC to hold the 12-bit data, the two instructions required to update the AD7548 analog output are as follows:

```
LD BC, (XXYY)
LD (PPQQ), BC
```

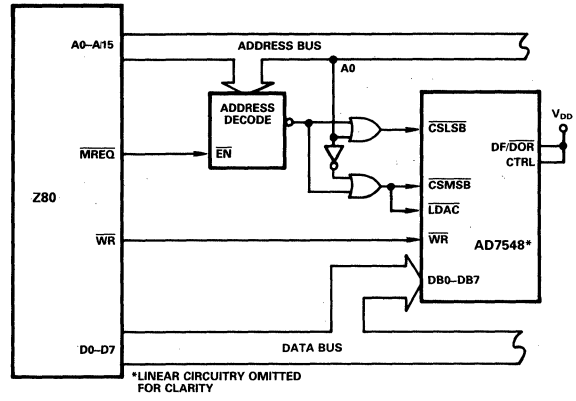


Figure 16. AD7548 – Z80 Interface (Automatic Transfer Mode)

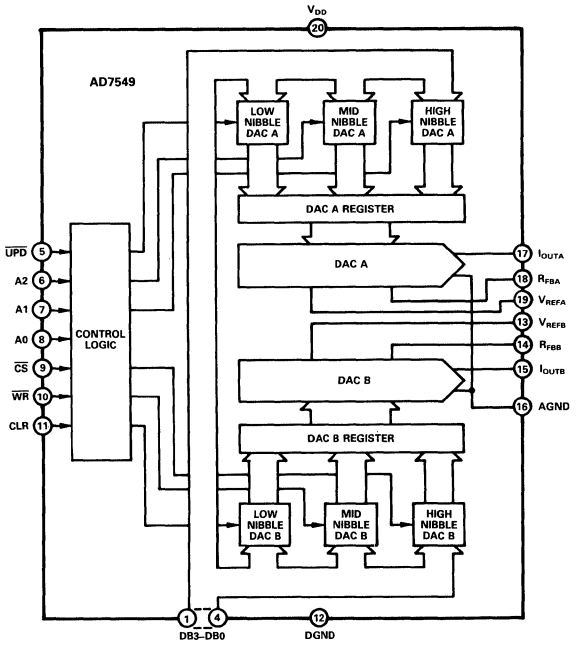
LC²MOS
Dual 12-Bit µP-Compatible DAC

AD7549

FEATURES
- Two Doubled Buffered 12-Bit DACs
- 4-Quadrant Multiplication
- Low Gain Error (3LSBs max)
- DAC Ladder Resistance Matching: 1%
- Space Saving Skinny DIP and Surface Mount Packages
- Latch-Up Proof

APPLICATIONS
- Programmable Filters
- Automatic Test Equipment
- Microcomputer Based Process Control
- Audio Systems
- Programmable Power Supplies
- Synchro Applications

AD7549 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7549 is a monolithic dual, 12-bit, current output D/A converter. It is packaged in both 0.3″ wide 20-pin DIPs and in 20-terminal surface mount packages. Both DACs provide four quadrant multiplication capabilities with a separate reference input and feedback resistor for each DAC. The monolithic construction ensures excellent thermal tracking and gain error tracking between the two DACs.

The DACs in the AD7549 are each loaded in three 4-bit nibbles. The control logic is designed for easy processor interfacing. Input and DAC register loading is accomplished using address lines A0, A1, A2 and $\overline{CS}$, $\overline{WR}$ lines. A logic high level on the CLR input clears all registers. Both DACs may be simultaneously updated using the $\overline{UPD}$ input.

The AD7549 is manufactured using the Linear Compatible CMOS(LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC or 5V CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Small package size: the loading structure adopted for the AD7549 enables two 12-Bit DACs to be packaged in either a small 20-pin 0.3″ DIP or in 20-terminal surface mount packages.
2. DAC to DAC matching: since both DACs are fabricated on the same chip, precise matching and tracking is inherent. This opens up applications which otherwise would not be considered, i.e., Programmable Filters, Audio Systems, etc.

ORDERING INFORMATION[1]

Relative Accuracy T_{min} to T_{max}	Full-Scale Error T_{min} to T_{max}	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-20)	**Hermetic (D-20)**	**Hermetic (D-20)**
±1LSB	±6LSB	AD7549JN	AD7549AD	AD7549SD
±1/2LSB	±3LSB	AD7549KN	AD7549BD	AD7549TD
		PLCC[3] (P-20A)		**LCCC[4] (E-20A)**
±1LSB	±6LSB	AD7549JP		AD7549SE
±1/2LSB	±3LSB	AD7549KP		AD7549TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS[1] (V_{DD} = +15V ±5%[2], V_{REFA} = V_{REFB} = 10V; I_{OUTA} = I_{OUTB} = AGND = 0V. All specifications T_{min} to T_{max} unless otherwise specified.)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC.
Gain Temperature Coefficient[3]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current I_{OUTA} (Pin 17)						
+25°C	20	20	20	20	nA max	DAC A Register loaded with all 0's
T_{min} to T_{max}	150	150	250	250	nA max	
I_{OUTB} (Pin 15)						
+25°C	20	20	20	20	nA max	DAC B Register loaded with all 0's
T_{min} to T_{max}	150	150	250	250	nA max	
REFERENCE INPUT						
Input Resistance (Pin 19, Pin 13)	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	18	18	18	18	kΩ max	
V_{REFA}/V_{REFB} Input Resistance Match	±3	±2	±3	±2	% max	Typically ±1%
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
I_{DD}	5	5	5	5	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +15V; V_{REFA} = V_{REFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V, Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. Typical value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	10	–	nV-sec typ	Measured with V_{REFA} = V_{RFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20V p-p 10kHz sine wave.
V_{REFB} to I_{OUTB}	−70	−65	dB max	DAC registers loaded with all 0s.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUTA}	80	80	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	80	80	pF max	
C_{OUTA}	160	160	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	160	160	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−62	–	dB typ	V_{REFA} = 20V p-p 100kHz sine wave, V_{REFB} = 0V
V_{REFB} to I_{OUTA}	−62	–	dB typ	V_{REFB} = 20V p-p 100kHz sine wave, V_{REFA} = 0V
Digital Crosstalk	10	–	nV-sec typ	Measured for a Code Transition of all 0's to all 1's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}
Harmonic Distortion	−90	–	dB typ	V_{IN} = 6V rms 1kHz

NOTES

[1]Temperature range as follows: J, K Versions; 0 to +70°C
A, B Versions; −25°C to +85°C
S, T Versions; −55°C to +125°C

[2]At V_{DD} = 5V, the device is fully functional with degraded performance.

[3]Guaranteed by Product Assurance testing.

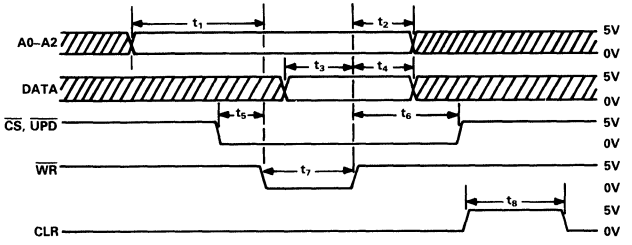
[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +15V, V_{REFA} = V_{RFB} = +10V, I_{OUTA} = I_{OUTB} = AGND = 0V unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	50	80	110	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	150	190	240	ns min	Data Setup Time
t_4	0	0	0	ns min	Data Hold Time
t_5	20	20	20	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	170	200	250	ns min	Write Pulse Width
t_8	170	200	250	ns min	Clear Pulse Width

Specifications subject to change without notice.



NOTES
1. All input signal rise and fall times measured from 10% to 90% of +5V. $t_r = t_f = 20ns$.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. Timing Diagram for AD7549

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (Pin 20) to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} (Pins 19, 13) to AGND . . . . . ±25V
V_{RFBA}, V_{RFBB} (Pins 18, 14) to AGND . . . . . ±25V
Digital Input Voltage (Pins 1–11)
to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{PIN15}, V_{PIN17}, to DGND . . . . . −0.3V, V_{DD} +0.3V
AGND to DGND . . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C

Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of 1LSB max over the operating temperature range ensures montonicity.

FULL-SCALE ERROR
Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero.

OUTPUT CAPACITANCE
This is the capacitance from I_{OUTA} or I_{OUTB} to AGND.

DIGITAL-TO-ANALOG GLITCH IMPULSE
The amount of charge injected into the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{REFA} and V_{REFB} equal to AGND.

OUTPUT LEAKAGE CURRENT
Output Leakage Current is current which appears at I_{OUTA} or I_{OUTB} with the DAC registers loaded to all zeros.

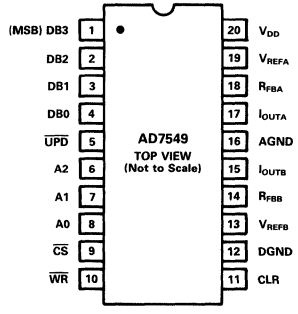
MULTIPLYING FEEDTHROUGH ERROR
This is the error due to capacitive feedthrough from V_{REFA} to I_{OUTA} or V_{REFB} to I_{OUTB} with the DAC registers loaded to all zeros.

CHANNEL-TO-CHANNEL ISOLATION
Channel-to-Channel Isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

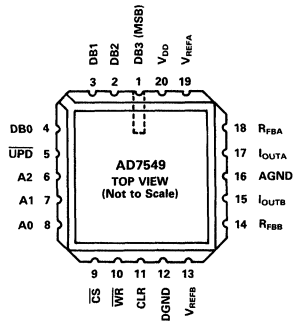
DIGITAL CROSSTALK
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as Digital Crosstalk and is specified in nV-secs.

PIN CONFIGURATIONS

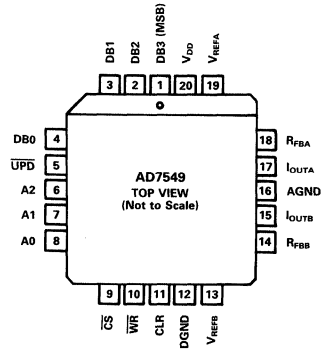
DIP



LCCC



PLCC



PIN	FUNCTION	DESCRIPTION
1	DB3	Data Bit 3, Data Bit 7 or Data Bit 11 (MSB)
2	DB2	Data Bit 2, Data Bit 6 or Data Bit 10.
3	DB1	Data Bit 1, Data Bit 5 or Data Bit 9.
4	DB0	Data Bit 0, Data Bit 4 or Data Bit 8.
5	$\overline{UPD}$	Updates DAC Registers from 4-bit input registers. DAC A and DAC B both updated simultaneously.
6	A2	Address line 2.
7	A1	Address line 1.
8	A0	Address line 0.
9	$\overline{CS}$	Chip Select Input. Active low.
10	$\overline{WR}$	Write Input. Active low.
11	CLR	Clear Input. Active High. Clears all registers.
12	DGND	Digital Ground.
13	V_{REFB}	Voltage reference input to DAC B.
14	R_{FBB}	Feedback resistor of DAC B.
15	I_{OUTB}	Current output terminal of DAC B.
16	AGND	Analog ground.
17	I_{OUTA}	Current output terminal of DAC A.
18	R_{FBA}	Feedback resistor of DAC A.
19	V_{REFA}	Voltage reference input to DAC A.
20	V_{DD}	+15V supply input.

CLR	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A2	A1	A0	FUNCTION
0	X	X	1	X	X	X	No data transfer.
0	1	1	X	X	X	X	No data transfer.
1	X	X	X	X	X	X	All registers cleared.
0	1	0	⊓	0	0	0	DAC A LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	0	1	DAC A MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	1	0	DAC A HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	1	1	DAC A Register loaded from Input Registers.
0	1	0	⊓	1	0	0	DAC B LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	0	1	DAC B MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	1	0	DAC B HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	1	1	DAC B Register loaded from Input Registers.
0	0	1	⊓	X	X	X	DAC A, DAC B Registers updated simultaneously from Input Registers.

NOTE: X = Don't Care

Table I. AD7549 Truth Table

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (i.e. AD644) or separate packages (AD544). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high speed op-amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all O's and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is at a minimum (i.e. $\leq 120\mu V$). Full scale trimming is accomplished by loading the DAC register with all 1's and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, 10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

Resistors R5, R6, R7 (R8, R9, R10) must be ratio matched to 0.01%. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 3 is given in Table III.

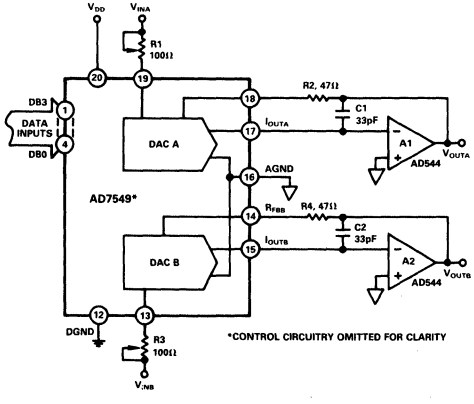


Figure 2. AD7549 Unipolar Binary Operation

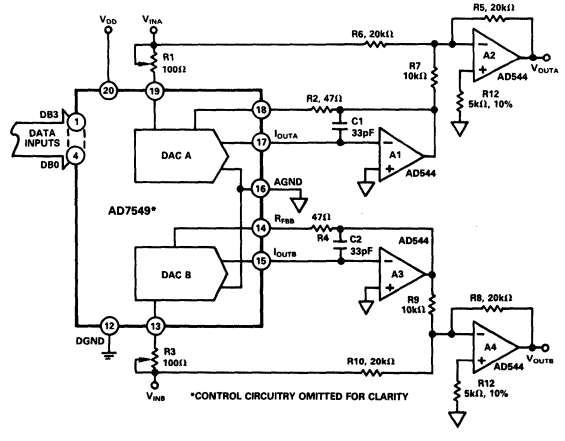


Figure 3. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 2

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 3

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 2 and 3 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD644L, AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

Temperature Coefficients: The gain temperature coefficient of the AD7549 has a maximum value of 5ppm/°C and typical value of 1ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.4LSBs respectively over a 100°C temperature range. When trim resistors R1(R3) and R2(R4) are used to adjust full scale range, the temperature coefficient of R1(R3) and R2(R4) should also be taken into account.

High Frequency Considerations: AD7549 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

Feedthrough: The dynamic performance of the AD7549 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 2 is shown in Figure 4 which minimizes feedthrough from V_{REFA}, V_{REFB} to the output in multiplying applications.

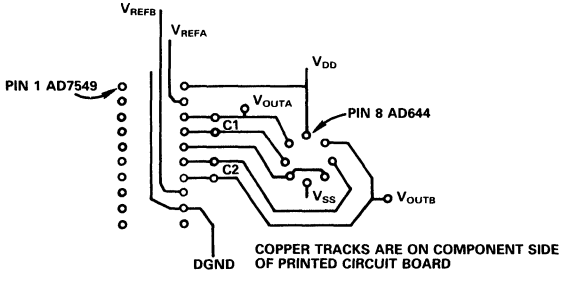


Figure 4. Suggested Layout for AD7549 with AD644 (Dual Op Amp)

AD7549 – 8085A INTERFACE

A typical interface circuit for the AD7549 and the 8085A microprocessor is given in Figure 5. Only the bottom 4 bits of the microprocessor data bus are used. The address decoder provides both the $\overline{CS}$ and $\overline{UPD}$ signals for the DAC. Address lines A0, A1, A2 select one of six DAC Input Registers for accepting data. In applications where simultaneous loading of the DACs is required then the $\overline{UPD}$ pin must be used to strobe both DAC registers. Otherwise, $\overline{UPD}$ may be tied high and address lines A0-A2, in conjunction with $\overline{CS}$ and $\overline{WR}$ signals, will select each DAC register separately (see Pin Function Description).

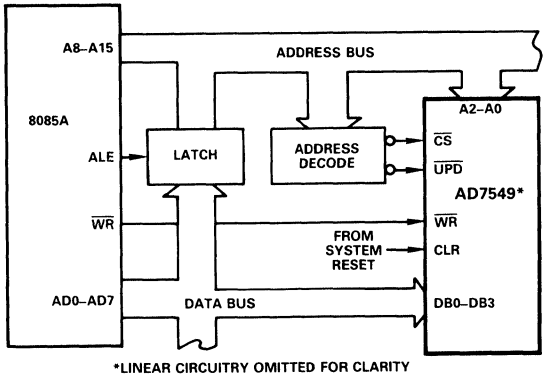


Figure 5. AD7549–8085A Interface

AD7549 – Z80 INTERFACE

Figure 6 shows the AD7549 connected to the Z80 microprocessor. The interface structure is similar to that for the 8085A.

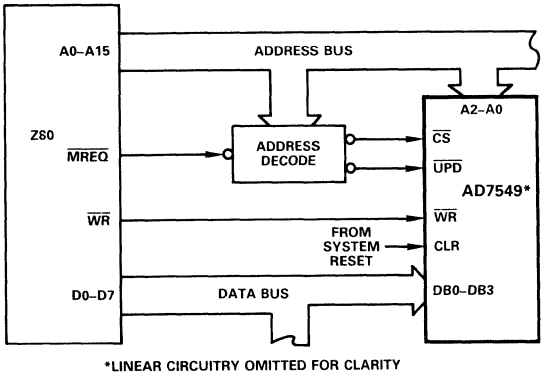
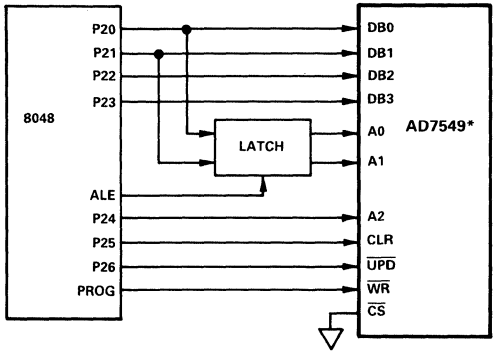


Figure 6. AD7549–Z80 Interface

AD7549 – 8048 INTERFACE

The AD7549 can be interfaced to the 8048 single component microcomputer using the circuit of Figure 7. A minimum number of I/O lines are needed. The system is easily expanded by using extra port lines to provide Chip Selects for more AD7549's. The advantage of this interface lies in its simplicity. In either single or multiple DAC applications both the software and chip select decoding are simplified over what would be required if the devices were memory mapped in a conventional manner.



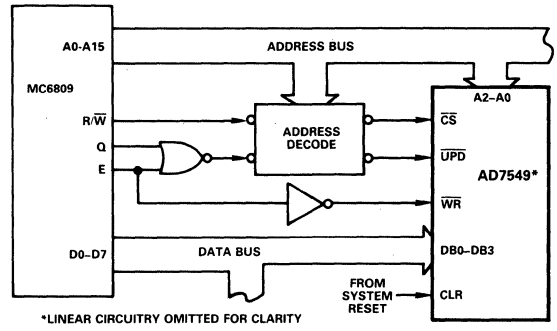
*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 7. AD7549–8048 Interface

The combination of 8048 system and AD7549 is particularly suitable for dedicated control applications. By adding reference and output circuitry a complete control system can be configured with a minimum number of components.

AD7549 – MC6809 INTERFACE

Figure 8 is the interface circuit for the popular MC6809 8-bit microprocessor. $\overline{CS}$ and $\overline{UPD}$ signals are decoded from the address for the simultaneous update facility while the $\overline{WR}$ pulse is provided by inverting the microprocessor clock, E.



*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 8. AD7549–MC6809 Interface

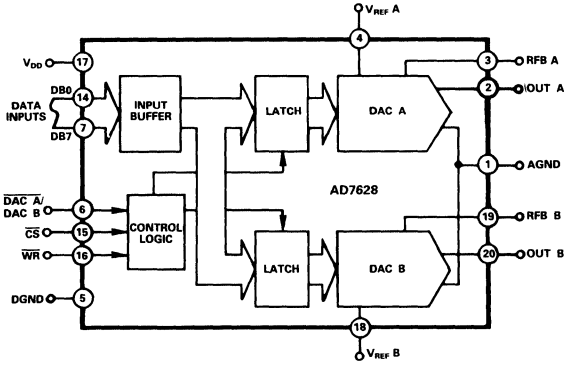
CMOS Dual 8-Bit Buffered Multiplying DAC

AD7628

FEATURES
- On-Chip Latches for Both DACs
- +12V to +15V Operation
- DACs Matched to 1%
- Four Quadrant Multiplication
- TTL/CMOS Compatible from +12V to +15V
- Latch Free (Protection Schottkys not Required)

APPLICATIONS
- Disk Drives
- Programmable Filters
- X-Y Graphics
- Gain/Attenuation

AD7628 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7628 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7628's load cycle is similar to the write cycle of a random access memory, and the device is bus compatible with most 8-bit microprocessors, including 6502, 6809, 8085, Z80.

The device operates from a +12V to +15V power supply and is TTL-compatible over this range. Power dissipation is a low 20mW.

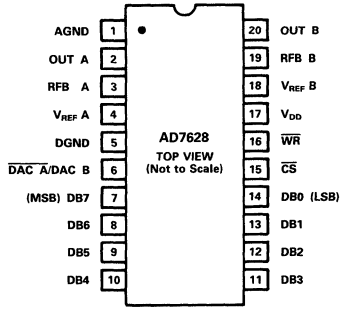
Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

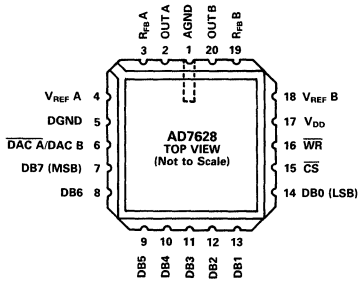
1. DAC to DAC matching: since both of the AD7628 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7628's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7628 to be packaged in either a small 20-pin 0.3" wide DIP or in 20-terminal surface mount packages.
3. TTL-Compatibility: All digital inputs are TTL-compatible over a +12V to +15V power supply range.

PIN CONFIGURATIONS

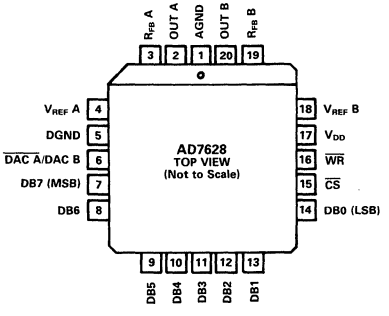
DIP



LCCC



PLCC



SPECIFICATIONS (V_{DD} = +10.8V to +15.75V, (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	T_A = +25°C[1]	T_A = 0 to +70°C −25°C to +85°C[1]	T_A = −55°C to +125°C[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]					
Resolution	8	8	8	Bits	
Relative Accuracy	±1/2	±1/2	±1/2	LSB max	This is an Endpoint Linearity Specification
Differential Nonlinearity	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	±2	±3	±3	LSB max	Measured Using Internal RFB A and RFB B. Both DAC Latches Loaded with 11111111. Gain Error is Adjustable Using Circuits of Figures 1 and 2.
Gain Temperature Coefficient[3]					
ΔGain/ΔTemperature	–	±0.0035	±0.0035	%/°C max	
Output Leakage Current					
OUT A (Pin 2)	±50	±200	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	±50	±200	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	±1	±1	±1	% max	
DIGITAL INPUTS[4]					
Input High Voltage					
V_{IH}	2.4	2.4	2.4	V min	
Input Low Voltage					
V_{IL}	0.8	0.8	0.8	V max	
Input Current					
I_{IN}	±1	±10	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance					
DB0–DB7	10	10	10	pF max	
WR, CS, DAC A/DAC B	15	15	15	pF max	
SWITCHING CHARACTERISTICS[3] See Timing Diagram					
Chip Select to Write Set Up Time					
t_{CS}	160	160	210	ns min	
Chip Select to Write Hold Time					
t_{CH}	10	10	10	ns min	
DAC Select to Write Set Up Time					
t_{AS}	160	160	210	ns min	
DAC Select to Write Hold Time					
t_{AH}	10	10	10	ns min	
Data Valid to Write Set Up Time					
t_{DS}	160	160	210	ns min	
Data Valid to Write Hold Time					
t_{DH}	10	10	10	ns min	
Write Pulse Width					
t_{WR}	150	170	210	ns min	
POWER SUPPLY					
I_{DD}, K Grade	2	2	–	mA	All Digital Inputs V_{IL} or V_{IH}
B, T Grades	2	2.5	2.5	mA	All Digital Inputs V_{IL} or V_{IH}
All Grades	100	500	500	μA	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

V_{DD} = +10.8V to +15.75V. (Measured Using Recommended P.C. Board Layout and AD644 as Output Amplifiers)

Parameter	T_A = +25°C[1]	T_A = 0 to +70°C −25°C to +85°C[1]	T_A = −55°C to +125°C[1]	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	0.01	0.02	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME	350	400	400	ns max	To 1/2LSB. Out A/Out B load = 100Ω. WR = CS = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL-TO-ANALOG GLITCH IMPULSE	330	–	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE					
C_{OUT} A	25	25	25	pF max	DAC Latches Loaded with 00000000
C_{OUT} B	25	25	25	pF max	
C_{OUT} A	60	60	60	pF max	DAC Latches Loaded with 11111111
C_{OUT} B	60	60	60	pF max	
AC FEEDTHROUGH					
V_{REF} A to OUT A	−70	−65	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave @ 10kHz
V_{REF} B to OUT B	−70	−65	−65	dB max	
CHANNEL-TO-CHANNEL ISOLATION					Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	−80	–	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 10kHz, V_{REF} B = 0V
V_{REF} B to OUT A	−80	–	–	dB typ	V_{REF} B = 20V p-p Sine Wave @ 10kHz, V_{REF} A = 0V
DIGITAL CROSSTALK	60	–	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	−85	–	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES

[1]Temperature Ranges are K Version: 0 to +70°C
B Version: −25°C to +85°C
T Version: −55°C to +125°C

[2]Specification applies to both DACs in AD7628.

[3]Guaranteed by design but not production tested.

[4]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.

Specifications subject to change without notice.

INTERFACE LOGIC INFORMATION

DAC Selection:
Both DAC latches share a common 8-bit input port. The control input $\overline{DAC\ A}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:
Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:
When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

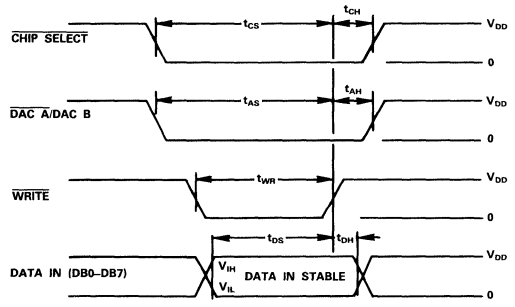
Hold Mode:
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{DAC\ A}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. V_{DD} = +10.8V TO +15.75V, $t_R = t_F$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD} +0.3V
DGND to AGND	V_{DD} +0.3V
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, V_{DD} +0.3V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (K) Grades	0 to +70°C
Industrial (B) Grades	−25°C to +85°C
Extended (T) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

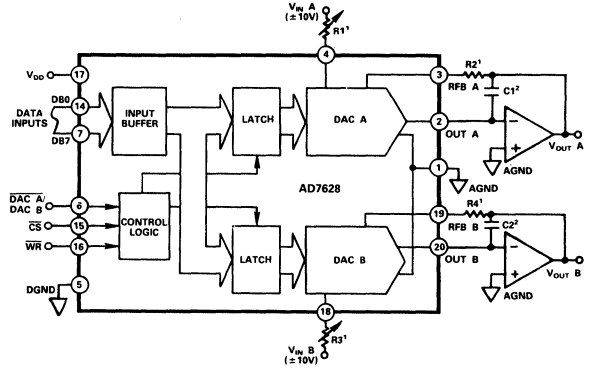
CAUTION:
1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

ORDERING INFORMATION[1]

Relative Accuracy	Gain Error T_A = +25°C	Temperature Range and Package Options[2,3] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-20)	Hermetic (Q-20)	Hermetic (Q-20)
±1/2LSB	±2LSB	AD7628KN	AD7628BQ	AD7628TQ
		PLCC[4] (P-20A)		LCCC[5] (E-20A)
±1/2LSB	±2LSB	AD7628KP		AD7628TE

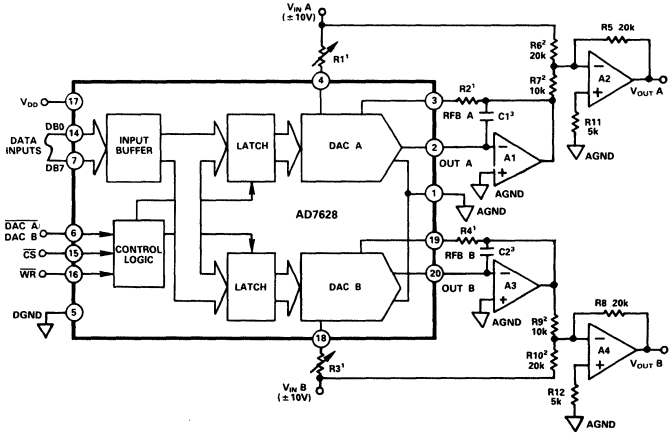
NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Also available in SOIC package (AD7628KR).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

Applying The AD7628



NOTES:
¹R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
²C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 1. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table I.



NOTES:
¹R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES. ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH. ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.
²MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
³C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BY REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER.

Figure 2. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table II.

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$-V_{IN}\left(\frac{255}{256}\right)$
10000001	$-V_{IN}\left(\frac{129}{256}\right)$
10000000	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
01111111	$-V_{IN}\left(\frac{127}{256}\right)$
00000001	$-V_{IN}\left(\frac{1}{256}\right)$
00000000	$-V_{IN}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

Table I. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$+V_{IN}\left(\frac{127}{128}\right)$
10000001	$+V_{IN}\left(\frac{1}{128}\right)$
10000000	0
01111111	$-V_{IN}\left(\frac{1}{128}\right)$
00000001	$-V_{IN}\left(\frac{127}{128}\right)$
00000000	$-V_{IN}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

Table II. Bipolar (Offset Binary) Code Table

Trim Resistor	K/B/T
R1;R3	500
R2;R4	150

Table III. Recommended Trim Resistor Values

ANALOG DEVICES

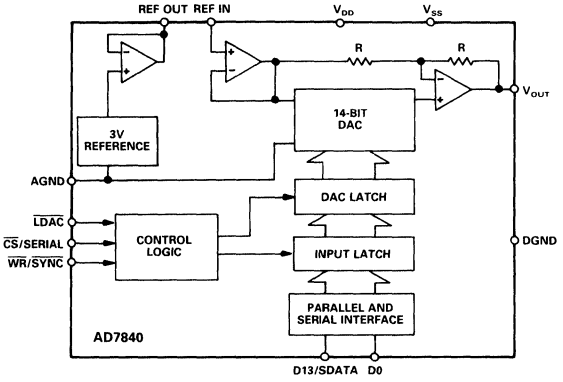
LC²MOS Complete 14-Bit DAC

AD7840

FEATURES

Complete 14-Bit Voltage Output DAC
Parallel and Serial Interface Capability
80dB Signal-to-Noise Ratio
Interfaces to High Speed DSP Processors
e.g., ADSP-2100, TMS32010, TMS32020
45ns min $\overline{WR}$ Pulse Width
Low Power – 70mW typ.
Operates from ±5V Supplies

AD7840 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7840 is a fast, complete 14-bit voltage output D/A converter. It consists of a 14-bit DAC, 3V buried Zener reference, DAC output amplifier and high speed control logic.

The part features double-buffered interface logic with a 14-bit input latch and 14-bit DAC latch. Data is loaded to the input latch in either of two modes, parallel or serial. This data is then transferred to the DAC latch under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 21ns allows direct parallel interfacing to digital signal processors and high speed 16-bit microprocessors. In the serial mode, the maximum serial data clock rate can be as high as 6MHz.

The analog output from the AD7840 provides a bipolar output range of ±3V. The AD7840 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion as well as for traditional dc specifications. Full power output signals up to 20kHz can be created.

The AD7840 is fabricated in linear compatible CMOS (LC^2MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin plastic and hermetic dual-in-line package (DIP) and is also packaged in a 28-terminal plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete 14-Bit D/A Function
   The AD7840 provides the complete function for creating ac signals and dc voltages to 14-bit accuracy. The part features an on-chip reference, an output buffer amplifier and 14-bit D/A converter.
2. Dynamic Specifications for DSP Users
   In addition to traditional dc specifications, the AD7840 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Fast, Versatile Microprocessor Interface
   The AD7840 is capable of 14-bit parallel and serial interfacing. In the parallel mode, data setup times of 21ns and write pulse widths of 45ns make the AD7840 compatible with modern 16-bit microprocessors and digital signal processors. In the serial mode, the part features a high data transfer rate of 6MHz.

SPECIFICATIONS (V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V, REF IN = +3V, R_L = 2kΩ, C_L = 100pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A[1]	K, B[1]	L, C[1]	S[1]	T[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]							
Signal to Noise Ratio[3] (SNR)	76	78	80	76	78	dB min	V_{OUT} = 1kHz Sine Wave, f_{SAMPLE} = 100kHz Typically 82dB at +25°C for 0 < V_{OUT} < 20kHz[4]
Total Harmonic Distortion (THD)	−78	−80	−84	−78	−80	dB max	V_{OUT} = 1kHz Sine Wave, f_{SAMPLE} = 100kHz Typically −84dB at +25°C for 0 < V_{OUT} < 20kHz[4]
Peak Harmonic or Spurious Noise	−78	−80	−84	−78	−80	dB max	V_{OUT} = 1kHz Sine Wave, f_{SAMPLE} = 100kHz Typically −84dB at +25°C for 0 < V_{OUT} < 20kHz[4]
DC ACCURACY							
Resolution	14	14	14	14	14	Bits	
Integral Nonlinearity	±2	±1	±1/2	±2	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	±5	±10	±10	LSB max	
Positive Full Scale Error[5]	±10	±10	±10	±10	±10	LSB max	
Negative Full Scale Error[5]	±10	±10	±10	±10	±10	LSB max	
REFERENCE OUTPUT[6]							
REF OUT @ +25°C	2.99	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	3.01	V max	
REF OUT TC	±60	±60	±35	±60	±35	ppm/°C max	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	−1	−1	−1	mV max	Reference Load Current Change (0-500μA)
REFERENCE INPUT							
Reference Input Range	2.85	2.85	2.85	2.85	2.85	V min	3V ±5%
	3.15	3.15	3.15	3.15	3.15	V max	
Input Current	50	50	50	50	50	μA max	
LOGIC INPUTS							
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	2.4	V min	V_{DD} = 5V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	0.8	V max	V_{DD} = 5V ±5%
Input Current, I_{IN}	±10	±10	±10	±10	±10	μA max	V_{IN} = 0V to V_{DD}
Input Current ($\overline{CS}$ Input Only)	±10	±10	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	10	10	pF max	
ANALOG OUTPUT							
Output Voltage Range	±3	±3	±3	±3	±3	V Nom	
dc Output Impedance	0.1	0.1	0.1	0.1	0.1	Ω typ	
Short-Circuit Current	20	20	20	20	20	mA typ	
AC CHARACTERISTICS[7]							
Voltage Output Settling Time							Settling Time to within ±1/2LSB of Final Value
Positive Full-Scale Change	4	4	4	4	4	μs max	Typically 2μs
Negative Full-Scale Change	4	4	4	4	4	μs max	Typically 2.5μs
Digital-to-Analog Glitch Impulse	10	10	10	10	10	nV secs typ	
Digital Feedthrough	2	2	2	2	2	nV secs typ	
POWER REQUIREMENTS							
V_{DD}	+5	+5	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	14	14	14	15	15	mA max	Output Unloaded, SCLK = +5V. Typically 10mA
I_{SS}	6	6	6	7	7	mA max	Output Unloaded, SCLK = +5V. Typically 4mA
Power Dissipation	100	100	100	110	110	mW max	Typically 70mW

NOTES

[1]Temperature Ranges are as follows: J, K, L Versions, 0 to +70°C; A, B, C Versions, −25°C to +85°C; S, T Versions, −55°C to +125°C.

[2]V_{OUT} (pk-pk) = ±3V.

[3]SNR calculation includes distortion and noise components.

[4]Using external sample-and-hold (see Testing the AD7840).

[5]Measured with respect to REF IN and includes bipolar offset error.

[6]For capacitive loads greater than 50pF, a series resistor is required (see Internal Reference section).

[7]Sample tested @25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1,2] (V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V.)

Parameter	Limit at T_{min}, T_{max} (J, K, L, A, B, C Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	**45**	**50**	ns min	$\overline{WR}$ Pulse Width
t_4	**21**	**28**	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	**10**	**15**	ns min	Data Valid to $\overline{WR}$ Hold Time
t_6	40	40	ns min	$\overline{LDAC}$ Pulse Width
t_7	50	50	ns min	$\overline{SYNC}$ to SCLK Falling Edge
t_8[3]	150	200	ns min	SCLK Cycle Time
t_9	30	40	ns min	Data Valid to SCLK Setup Time
t_{10}	75	100	ns min	Data Valid to SCLK Hold Time
t_{11}	75	100	ns min	$\overline{SYNC}$ to SCLK Hold Time

NOTE
[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
[2]See Figures 6 and 8.
[3]SCLK mark/space ratio is 40/60 to 60/40.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V to +7V
V_{SS} to AGND . . . . . +0.3V to −7V
AGND to DGND . . . . . −0.3V to V_{DD} +0.3V
V_{OUT} to AGND . . . . . V_{SS} to V_{DD}
REF OUT to AGND . . . . . 0V to V_{DD}
REF IN to AGND . . . . . −0.3V to V_{DD} +0.3V
Digital Inputs to DGND . . . . . −0.3V to V_{DD} +0.3V
Operating Temperature Range
Commercial (J, K, L Versions) . . . . . 0 to +70°C
Industrial (A, B, C Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION[1]

SNR (dBs)	Relative Accuracy (LSB)	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-24)	**Hermetic DIP[3] (Q-24)**	**Hermetic DIP[3] (Q-24)**
78 min	±2 max	AD7840JN	AD7840AQ	AD7840SQ[4]
80 min	±1 max	AD7840KN	AD7840BQ	AD7840TQ[4]
82 min	±1/2 max	AD7840LN	AD7840CQ	
		PLCC[5, 6] (P-28A)		
78 min	±2 max	AD7840JP		
80 min	±1 max	AD7840KP		
82 min	±1/2 max	AD7840LP		

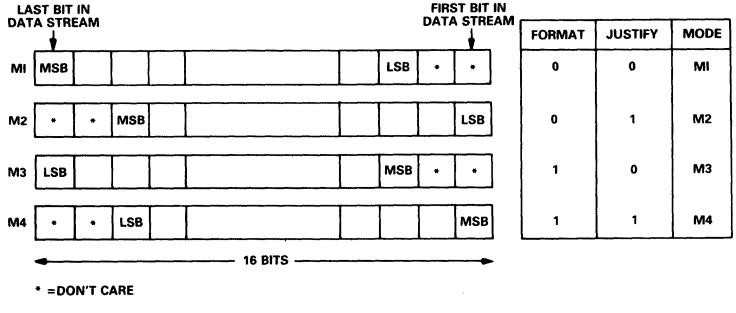
NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Analog Devices reserves the right to ship ceramic (D-24A) in lieu of cerdip (Q-24) packages.
[4]Available to /883B processing only.
[5]PLCC: Plastic Leaded Chip Carrier.
[6]Contact your local sales office for LCCC availability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

DIP Pin No.	Pin Mnemonic	Function
1	$\overline{CS}$/SERIAL	Chip Select/Serial Input. When driven with normal logic levels, it is an active low logic input which is used in conjunction with $\overline{WR}$ to load parallel data to the input latch. For applications where $\overline{CS}$ is permanently low, an R, C is required for correct power-up (see $\overline{LDAC}$ input). If this input is tied to V_{SS}, it defines the AD7840 for serial mode operation.
2	$\overline{WR}/\overline{SYNC}$	Write/Frame Synchronization Input. In the parallel data mode, it is used in conjunction with $\overline{CS}$ to load parallel data. In the serial mode of operation, this pin functions as a Frame Synchronization pulse with serial data expected after the falling edge of this signal.
3	D13/SDATA	Data Bit 13(MSB)/Serial Data. When parallel data is selected, this pin is the D13 input. In serial mode, SDATA is the serial data input which is used in conjunction with $\overline{SYNC}$ and SCLK to transfer serial data to the AD7840 input latch.
4	D12/SCLK	Data Bit 12/Serial Clock. When parallel data is selected, this pin is the D12 input. In the serial mode, it is the serial clock input. Serial data bits are latched on the falling edge of SCLK when $\overline{SYNC}$ is low.
5	D11/FORMAT	Data Bit 11/Data Format. When parallel data is selected, this pin is the D11 input. In serial mode, a logic 1 on this input indicates that the MSB is the first valid bit in the serial data stream. A logic 0 indicates that the LSB is the first valid bit (see Table I).
6	D10/JUSTIFY	Data Bit 10/Data Justification. When parallel data is selected, this pin is the D10 input. In serial mode, this input controls the serial data justification (see Table I).
7–11	D9—D5	Data Bit 9 to Data Bit 5. Parallel data inputs.
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	D4—D1	Data Bit 4 to Data Bit 1. Parallel data inputs.
17	D0	Data Bit 0 (LSB). Parallel data input.
18	V_{DD}	Positive Supply, +5V± 5%.
19	AGND	Analog Ground. Ground reference for DAC, reference and output buffer amplifier.
20	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Bipolar output range (±3V with REF IN = +3V).
21	V_{SS}	Negative Supply Voltage, −5V ±5%.
22	REF OUT	Voltage Reference Output. The internal 3V analog reference is provided at this pin. To operate the AD7840 with internal reference, REF OUT should be connected to REF IN. The external load capability of the reference is 500μA.
23	REF IN	Voltage Reference Input. The reference voltage for the DAC is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7840 is 3V.
24	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latch from the input latch on the falling edge of this signal (see Interface Logic Information section). The AD7840 should be powered-up with $\overline{LDAC}$ high. For applications where $\overline{LDAC}$ is permanently low, an R, C is required for correct power-up (see Figure 19).

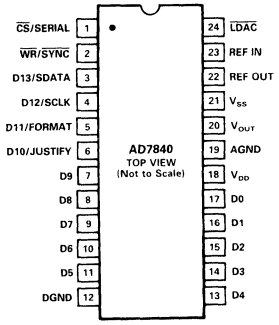


FORMAT	JUSTIFY	MODE
0	0	MI
0	1	M2
1	0	M3
1	1	M4

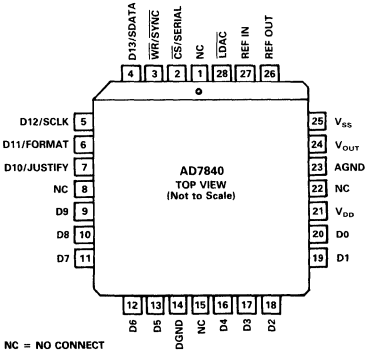
Table I. Serial Data Modes

PIN CONFIGURATIONS

DIP



PLCC



NC = NO CONNECT

D/A SECTION

The AD7840 contains a 14-bit voltage mode D/A converter consisting of highly stable thin film resistors and high speed NMOS single-pole, double-throw switches. The simplified circuit diagram for the DAC section is shown in Figure 1. The three MSBs of the data word are decoded to drive the seven switches A—G. The 11LSBs switch an 11-bit R-2R ladder structure. The output voltage from this converter has the same polarity as the reference voltage, REF IN.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter and the bipolar bias circuitry. The D/A converter is configured and scaled for a 3V reference and the device is tested with 3V applied to REF IN. Operating the AD7840 at reference voltages outside the ± 5% tolerance range may result in degraded performance from the part.

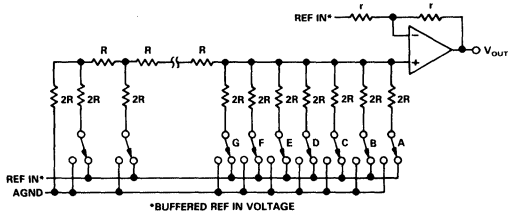


Figure 1. DAC Ladder Structure

INTERNAL REFERENCE

The AD7840 has an on-chip temperature compensated buried Zener reference (see Figure 2) which is factory trimmed to 3V ±10mV. The reference voltage is provided at the REF OUT pin. This reference can be used to provide both the reference voltage for the D/A converter and the bipolar bias circuitry. This is achieved by connecting the REF OUT pin to the REF IN pin of the device.

The reference voltage can also be used as a reference for other components and is capable of providing up to 500μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50pF. If the reference is required for external use, it should be decoupled to AGND with a 200Ω resistor in series with a parallel combination of a 10μF tantalum capacitor and a 0.1μF ceramic capacitor.

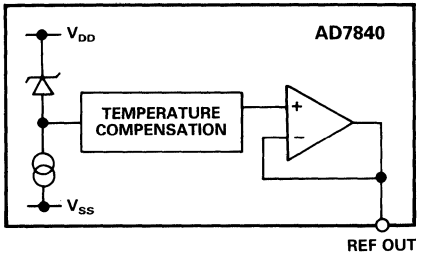


Figure 2. Internal Reference

EXTERNAL REFERENCE

In some applications, the user may require a system reference or some other external reference to drive the AD7840 reference input. Figure 3 shows how the AD586 5V reference can be conditioned to provide the 3V reference required by the AD7840 REF IN. An alternate source of reference voltage for the AD7840 in systems which use both a DAC and an ADC is to use the REF OUT voltage of ADCs such as the AD7870 and AD7871. A circuit showing this arrangement is shown in Figure 20.

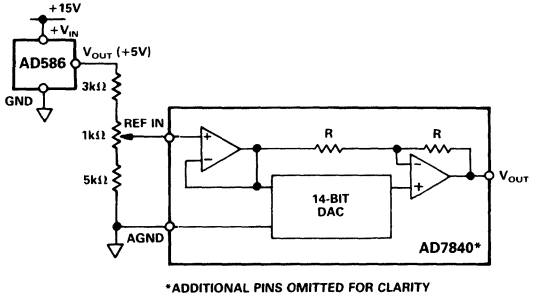


Figure 3. AD586 Driving AD7840 REF IN

OP AMP SECTION

The output from the voltage mode DAC is buffered by a non-inverting amplifier. Internal scaling resistors on the AD7840 configure an output voltage range of ±3V for an input reference voltage of +3V. The arrangement of these resistors around the output op amp is as shown in Figure 1. The buffer amplifier is capable of developing ±3V across a 2kΩ and 100pF load to ground and can produce 6V peak-to-peak sine wave signals to a frequency of 20kHz. The output is updated on the falling edge of the $\overline{\text{LDAC}}$ input. The amplifier settles to within 1/2LSB of its final value in typically less than 2.5μs.

The small signal (200mV p-p) bandwidth of the output buffer amplifier is typically 1MHz. The output noise from the amplifier is low with a figure of 30nV/$\sqrt{\text{Hz}}$ at a frequency of 1kHz. The broadband noise from the amplifier exhibits a typical peak-to-peak figure of 150μV for a 1MHz output bandwidth. Figure 4 shows a typical plot of noise spectral density versus frequency for the output buffer amplifier and for the on-chip reference.

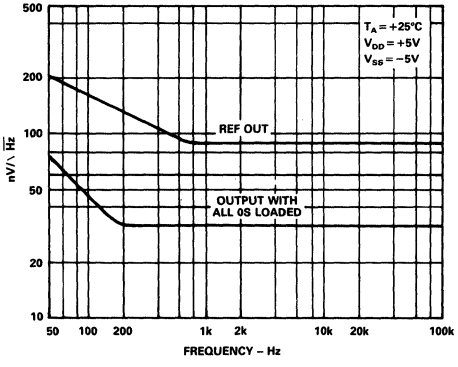


Figure 4. Noise Spectral Density vs. Frequency

TRANSFER FUNCTION

The basic circuit configuration for the AD7840 is shown in Figure 5. Table II shows the ideal input code to output voltage relationship for this configuration. Input coding to the DAC is 2s complement with 1LSB = FS/16,384 = 6V/16,384 = 366μV.

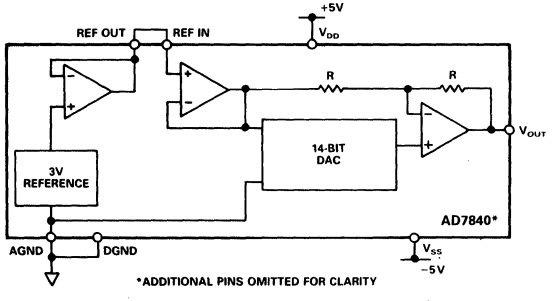


Figure 5. AD7840 Basic Connection Diagram

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	+2.999634V
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	+2.999268V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	+0.000366V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0V
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	−0.000366V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	−2.999634V
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	−3V

*Assuming REF IN = +3V.

Table II. Ideal Input/Output Code Table

The output voltage can be expressed in terms of the input code, N, using the following expression:

$$V_{OUT} = \frac{2 \times N \times REFIN}{16384} \quad -8192 \leq N \leq +8191$$

INTERFACE LOGIC INFORMATION

The AD7840 contains two 14-bit latches, an input latch and a DAC latch. Data can be loaded to the input latch in one of two basic interface formats. The first is a parallel 14-bit wide data word; the second is a serial interface where 16 bits of data are serially clocked into the input latch. In the parallel mode, $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the loading of data. When the serial data format is selected, data is loaded using the SCLK, $\overline{\text{SYNC}}$ and SDATA serial inputs. Data is transferred from the input latch to the DAC latch under control of the $\overline{\text{LDAC}}$ signal. Only the data in the DAC latch determines the analog output of the AD7840.

Parallel Data Format

Table III shows the truth table for AD7840 parallel mode operation. The AD7840 normally operates with a parallel input data format. In this case, all 14 bits of data (appearing on data inputs D13 (MSB) through D0 (LSB)) are loaded to the AD7840 input latch at the same time. $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the loading of this data. These control signals are level-triggered; therefore, the input latch can be made transparent by holding both signals at a logic low level. Input data is latched into the input latch on the rising edge of $\overline{\text{CS}}$ or $\overline{\text{WR}}$.

The DAC latch is also level triggered. The DAC output is normally updated on the falling edge of the $\overline{\text{LDAC}}$ signal. However, both latches cannot become transparent at the same time. Therefore, if $\overline{\text{LDAC}}$ is hardwired low, the part operates as follows; with $\overline{\text{LDAC}}$ low and $\overline{\text{CS}}$ and $\overline{\text{WR}}$ high, the DAC latch is transparent. When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ go low (with $\overline{\text{LDAC}}$ still low), the input latch becomes transparent but the DAC latch is disabled. When $\overline{\text{CS}}$ or $\overline{\text{WR}}$ return high, the input latch is locked out and the DAC latch becomes transparent again and the DAC output is updated. The write cycle timing diagram for parallel data is shown in Figure 6. Figure 7 shows the simplified parallel input control logic for the AD7840.

$\overline{CS}$	$\overline{WR}$	$\overline{LDAC}$	Function
H	X	H	Both Latches Latched
X	H	H	
L	L	H	Input Latch Transparent
H	H	L	Input Latch Latched
H	X	L	DAC Latch Transparent
X	H	L	Analog Output Updated
↓	↓	L	Input Latch Transparent DAC Latch Data Transfer Inhibited
L	↑	L	Input Latch Is Latched
↑	L	L	DAC Latch Data Transfer Occurs

X = Don't Care

Table III. Parallel Mode Truth Table

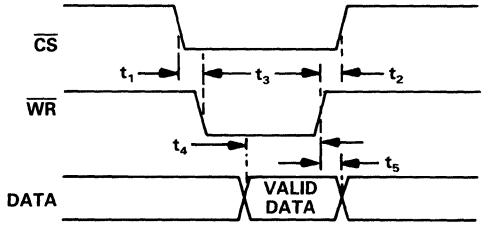


Figure 6. Parallel Mode Timing Diagram

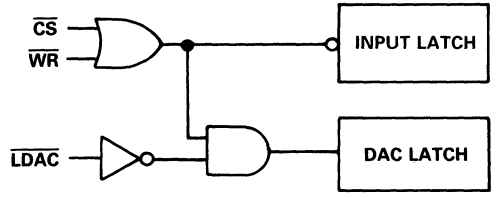


Figure 7. AD7840 Simplified Parallel Input Control Logic

Serial Data Format

The serial data format is selected for the AD7840 by connecting the $\overline{CS}$/SERIAL line to −5V. In this case, the $\overline{WR}$/$\overline{SYNC}$, D13/SDATA, D12/SCLK, D11/FORMAT and D10/JUSTIFY pins all assume their serial functions. The unused parallel inputs should not be left unconnected to avoid noise pickup. Serial data is loaded to the input latch under control of SCLK, $\overline{SYNC}$ and SDATA. The AD7840 expects a 16-bit stream of serial data on its SDATA input. Serial data must be valid on the falling edge of SCLK. The $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7840 that valid serial data will be available for the next 16 falling edges of SCLK. Figure 8 shows the timing diagram for serial data format.

Although 16 bits of data are clocked into the AD7840, only 14 bits go into the input latch. Therefore, two bits in the stream are don't cares since their value does not affect the input latch data. The order and position in which the AD7840 accepts the 14 bits of input data depends upon the FORMAT and JUSTIFY inputs. There are four different input data modes which can be chosen (see Table I in the Pin Function Description section).

The first mode (M1) assumes that the first two bits of the input data stream are don't cares, the third bit is the LSB and the last (or 16th bit) is the MSB. This mode is chosen by tying both the FORMAT and JUSTIFY pins to a logic 0. The second mode (M2; FORMAT = 0, JUSTIFY = 1) assumes that the first bit in the data stream is the LSB, the fourteenth bit is the MSB and the last two bits are don't cares. The third mode (M3; FORMAT = 1, JUSTIFY = 0) assumes that the first two bits in the stream are again don't cares, the third bit is now the MSB and the sixteenth bit is the LSB. The final mode (M4; FORMAT = 1, JUSTIFY = 1) assumes that the first bit is the MSB, the fourteenth bit is the LSB and the last two bits of the stream are don't cares.

As in the parallel mode, the $\overline{LDAC}$ signal controls the loading of data to the DAC latch. Normally, data is loaded to the DAC latch on the falling edge of $\overline{LDAC}$. However, if $\overline{LDAC}$ is held low, then serial data is loaded to the DAC latch on the sixteenth falling edge of SCLK. If $\overline{LDAC}$ goes low during the transfer of serial data to the input latch, no DAC latch update takes place on the falling edge of $\overline{LDAC}$. If $\overline{LDAC}$ stays low until the serial transfer is completed, then the update takes place on the sixteenth falling edge of SCLK. If $\overline{LDAC}$ returns high before the serial data transfer is completed, no DAC latch update takes place. Figure 9 shows the simplified serial input control logic for the AD7840.

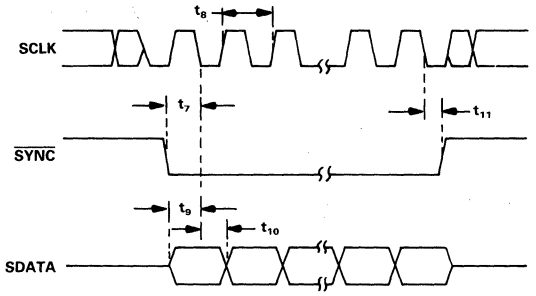


Figure 8. Serial Mode Timing Diagram

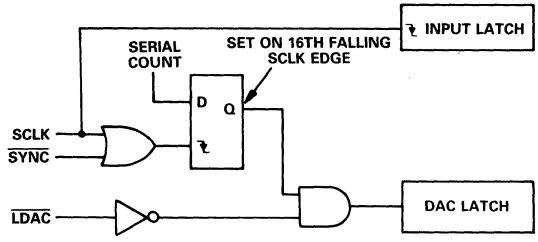


Figure 9. AD7840 Simplified Serial Input Control Logic

AD7840 DYNAMIC SPECIFICATIONS

The AD7840 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for the signal processing applications such as speech synthesis, servo control and high speed modems. These applications require information on the DAC's effect on the spectral content of the signal it is creating. Hence, the parameters for which the AD7840 is specified include signal-to-noise ratio, harmonic distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the DAC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (fs/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave output is given by

$$SNR = (6.02N + 1.76)dB \quad (1)$$

where N is the number of bits. Thus for an ideal 14-bit converter, SNR = 86dB.

Figure 10 shows a typical 2048 point Fast Fourier Transform (FFT) plot of the AD7840KN with an output frequency of 1kHz and an update rate of 100kHz. The SNR obtained from this graph is 81.8dB. It should be noted that the harmonics are taken into account when calculating the SNR.

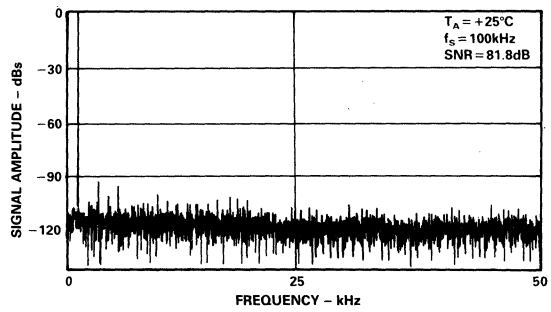


Figure 10. AD7840 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7840, total harmonic distortion (THD) is defined as

$$THD = 20 \log \frac{\sqrt{V_2^2+V_3^2+V_4^2+V_5^2+V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the 2048-point FFT plot.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the DAC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

Testing the AD7840

A simplified diagram of the method used to test the dynamic performance specifications is outlined in Figure 11. Data is loaded to the AD7840 under control of the microcontroller and associated logic at a 100kHz update rate. The output of the AD7840 is applied to a ninth order, 50kHz, low-pass filter. The output of the filter is in turn applied to a 16-bit accurate digitizer. This digitizes the signal and the microcontroller generates an FFT plot from which the dynamic performance of the AD7840 can be evaluated.

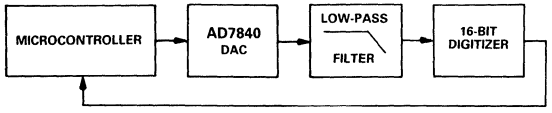


Figure 11. AD7840 Dynamic Performance Test Circuit

The digitizer sampling is synchronized with the AD7840 update rate to ease FFT calculations. The digitizer samples the AD7840 after the output has settled to its new value. Therefore, if the digitizer was to sample the output directly it would effectively be sampling a dc value each time. As a result, the dynamic performance of the AD7840 would not be measured correctly. Using the digitizer directly on the AD7840 output would give better results than the actual performance of the AD7840. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7840 is measured.

Some applications will require improved performance versus frequency from the AD7840. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 12 will extend the very good performance of the AD7840 to 20kHz.

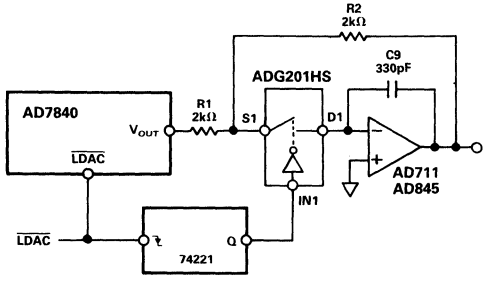


Figure 12. Sample-and-Hold Circuit

Other applications will already have an inherent sample-and-hold function following the AD7840. An example of this type of application is driving a switched-capacitor filter where the updating of the DAC is synchronized with the switched-capacitor filter. This inherent sample-and-hold function also extends the frequency range performance of the AD7840.

Performance versus Frequency

The typical performance plots of Figures 13 and 14 show the AD7840's performance over a wide range of input frequencies at an update rate of 100kHz. The plot of Figure 13 is without a sample-and-hold on the AD7840 output while the plot of Figure 14 is generated with the sample-and-hold circuit of Figure 12 on the output.

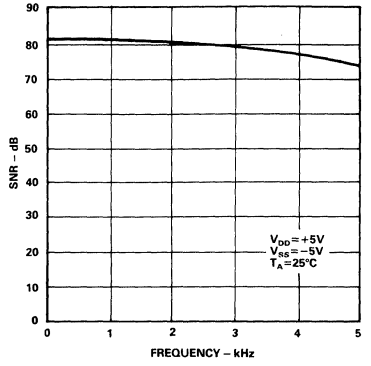


Figure 13. Performance vs. Frequency (No Sample-and-Hold)

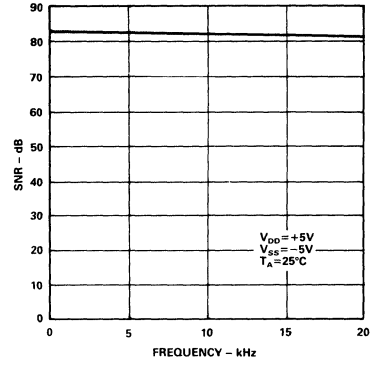


Figure 14. Performance vs. Frequency (with Sample-and-Hold)

MICROPROCESSOR INTERFACING

The AD7840 logic architecture allows two interfacing options for interfacing the part to microprocessor systems. It offers a 14-bit wide parallel format and a serial format. Fast pulse widths and data setup times allow the AD7840 to interface directly to most microprocessors including the DSP processors. Suitable interfaces to various microprocessors are shown in Figures 15 to 23.

Parallel Interfacing

Figures 15 to 17 show interfaces to the DSP processors, the ADSP-2100, the TMS32010 and TMS32020. An external timer controls the updating of the AD7840. Data is loaded to the AD7840 input latch using the following instructions:

ADSP-2100 : DM(DAC) = MR0
TMS32010 : OUT DAC,D
TMS32020 : OUT DAC,D
MR0 = ADSP-2100 MR0 Register
D = Data Memory Address
DAC = AD7840 Address

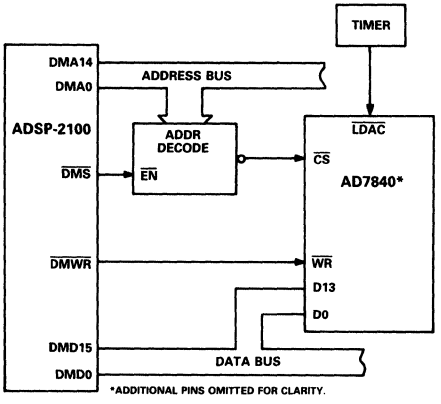


Figure 15 AD7840 – ADSP-2100 Parallel Interface

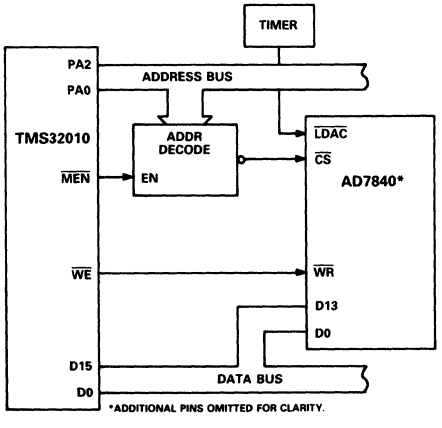


Figure 16. AD7840 – TM32010 Parallel Interface

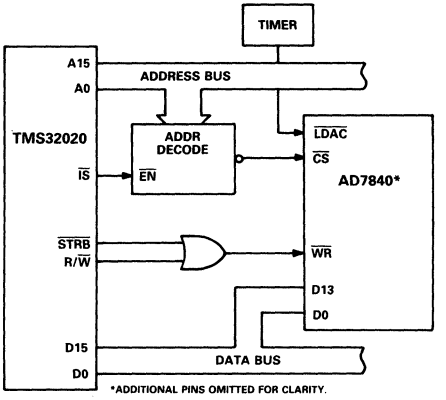


Figure 17. AD7840 – TMS32020 Parallel Interface

Some applications may require that the updating of the AD7840 DAC latch be controlled by the microprocessor rather than the external timer. One option (for double-buffered interfacing) is to decode the AD7840 $\overline{LDAC}$ from the address bus so that a write operation to the DAC latch (at a separate address than the input latch) updates the output. An example of this is shown in the 8086 interface of Figure 18. Note that connecting the $\overline{LDAC}$ input to the $\overline{CS}$ input will not load the DAC latch correctly since both latches cannot be transparent at the same time.

AD7840 – 8086 Interface

Figure 18 shows an interface between the AD7840 and the 8086 microprocessor. For this interface, the $\overline{LDAC}$ input is derived from a decoded address. If the least significant address line, A0, is decoded then the input latch and the DAC latch can reside at consecutive addresses. A move instruction loads the input latch while a second move instruction updates the DAC latch and the AD7840 output. The move instruction to load a data word WXYZ to the input latch is as follows:

MOV DAC,#YZWX
DAC = AD7840 Address

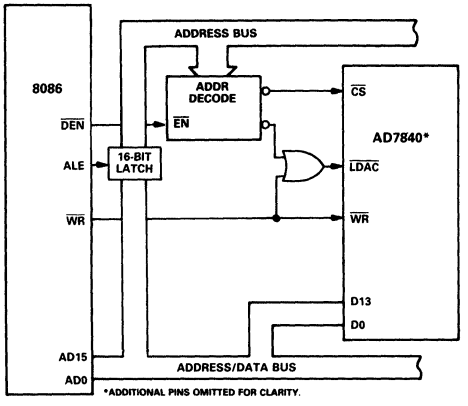


Figure 18. AD7840 – 8086 Parallel Interface

AD7840 – 68000 Interface
An interface between the AD7840 and the 68000 microprocessor is shown in Figure 19. In this interface example, the $\overline{LDAC}$ input is hardwired low. As a result the DAC latch and analog output are updated on the rising edge of $\overline{WR}$. A single move instruction, therefore, loads the input latch and updates the output.

MOVE.W D0,$DAC
D0 = 68000 D0 Register
DAC = AD7840 Address

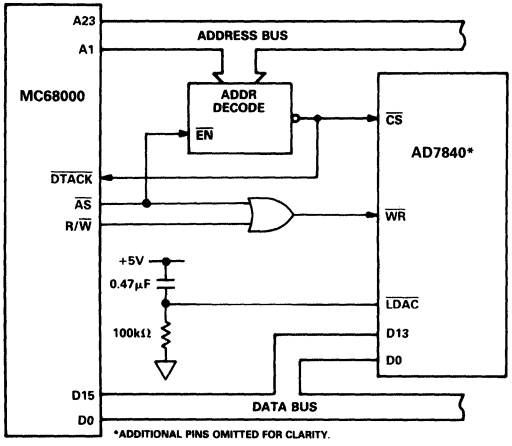


Figure 19. AD7840 – MC68000 Parallel Interface

Serial Interfacing
Figures 20 to 23 show the AD7840 configured for serial interfacing with the $\overline{CS}$ input hardwired to −5V. The parallel bus is not activated during serial communication with the AD7840.

AD7840 – ADSP-2101/ADSP-2102 Serial Interface
Figure 20 shows a serial interface between the AD7840 and the ADSP-2101/ADSP-2102 DSP processor. Also included in the interface is the AD7870, a 12-bit A/D converter. An interface such as this is suitable for modem and other applications which have a DAC and an ADC in serial communication with a microprocessor.

The interface uses just one of the two serial ports of the ADSP-2101/ADSP-2102. Conversion is initiated on the AD7870 at a fixed sample rate (e.g., 9.6kHz) which is provided by a timer or clock recovery circuitry. While communication takes place between the ADC and the ADSP-2101/ADSP-2102, the AD7870 $\overline{SSTRB}$ line is low. This $\overline{SSTRB}$ line is used to provide a frame synchronization pulse for the AD7840 $\overline{SYNC}$ and ADSP-2101/ADSP-2102 TFS lines. This means that communication between the processor and the AD7840 can only take place while the AD7870 is communicating with the processor. This arrangement is desirable in systems such as modems where the DAC and ADC communication should be synchronous.

The use of the AD7870 SCLK for the AD7840 SCLK and ADSP-2101/ADSP-2102 SCLK means that only one serial serial port of the processor is used. The serial clock for the AD7870 must be set for continuous clock for correct operation of this interface.

Data from the ADSP-2101/ADSP-2102 is valid on the falling edge of SCLK. The $\overline{LDAC}$ input of the AD7840 is permanently low so the update of the DAC latch and analog output takes place on the sixteenth falling edge of SCLK (with $\overline{SYNC}$ low). The FORMAT pin of the AD7840 must be tied to +5V and the JUSTIFY pin tied to DGND for this interface to operate correctly.

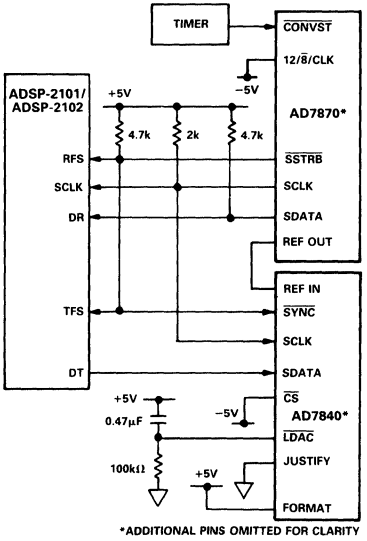


Figure 20. Complete DAC/ADC Serial Interface

AD7840 – DSP56000 Serial Interface
A serial interface between the AD7840 and the DSP56000 is shown in Figure 21. The DSP56000 is configured for normal mode synchronous operation with gated clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a 0. SCK is internally generated on the DSP56000 and applied to the AD7840 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{SYNC}$ input of the AD7840.

The $\overline{LDAC}$ input of the AD7840 is connected to DGND so the update of the DAC latch takes place on the sixteenth falling edge of SCLK. As with the previous interface, the FORMAT pin of the AD7840 must be tied to +5V and the JUSTIFY pin tied to DGND.

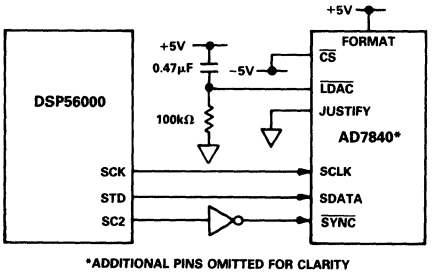


Figure 21. AD7840 – DSP56000 Serial Interface

AD7840 – TMS32020 Serial Interface

Figure 22 shows a serial interface between the AD7840 and the TMS32020 DSP processor. In this interface, the CLKX and FSX pin of the TMS32020 are generated from the clock/timer circuitry. The same clock/timer circuitry generates the $\overline{\text{LDAC}}$ signal of the AD7840 to synchronize the update of the output with the serial transmission. The FSX pin of the TMS32020 must be configured as an input.

Data from the TMS32020 is valid on the falling edge of CLKX. Once again, the FORMAT pin of the AD7840 must be tied to +5V while the JUSTIFY pin must be tied to DGND.

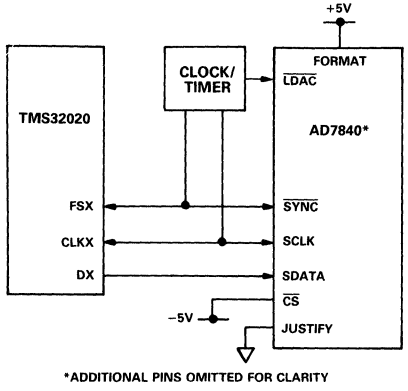


Figure 22. AD7840 – TMS32020 Serial Interface

AD7840 – NEC7720 Serial Interface

A serial interface between the AD7840 and the NEC7720 is shown in Figure 23. This clock must be inverted before being applied to the AD7840 SCLK input because data from the processor is valid on the rising edge of SCK.

The NEC7720 is programmed for the LSB to be the first bit in the serial data stream. Therefore, the AD7840 is set up with the FORMAT pin tied to DGND and the JUSTIFY pin tied to +5V.

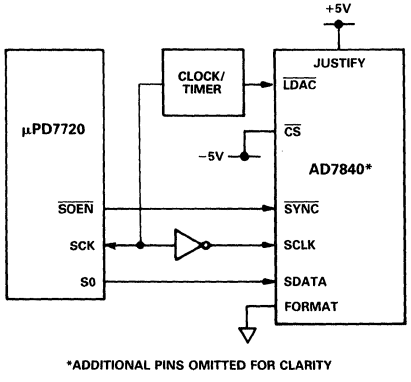


Figure 23. AD7840 – NEC7720 Serial Interface

APPLYING THE AD7840

Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7840 works on an LSB size of 366µV. Therefore, the designer must be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as the switching spikes can feed through to the on-chip amplifier. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any high performance converter, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground (star ground) separate from the logic system ground. Place this star ground as close as possible to the AD7840 as shown in Figure 24. Connect all analog grounds to this star ground and also connect the AD7840 DGND pin to this ground. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of high performance converters. Therefore, the foil width for these tracks should be kept as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 27 and 28 have both analog and digital ground planes which are kept separated and only joined at the star ground close to the AD7840.

NOISE

Keep the signal leads on the V_{OUT} signal and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible, use a shielded cable between the DAC output and its destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

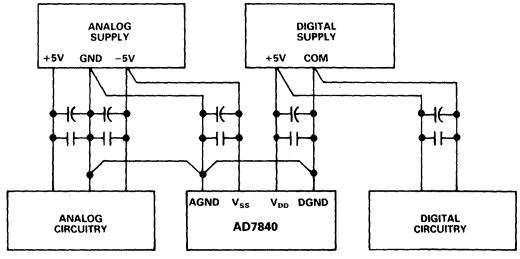


Figure 24. Power Supply Grounding Practice

DATA ACQUISITION BOARD

Figure 25 shows the AD7840 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 26 to 28. The board layout has three interface ports: one serial and two parallel. One of the parallel ports is directly compatible with the ADSP-2100 evaluation board expansion connector.

Some systems will require the addition of a re-construction filter on the output of the AD7840 to complete the data acquisition system. There is a component grid provided near the analog output on the PCB which may be used for such a filter or any other output conditioning circuitry. To facilitate this option, there is a shorting plug (labeled LK1 on the PCB) on the analog output track. If this shorting plug is used, the analog output connects to the output of the AD7840; otherwise this shorting plug can be omitted and a wire link used to connect the analog output to the PCB component grid.

The board also contains a simple sample-and-hold circuit which can be used on the output of the AD7840 to extend the very good performance of the AD7840 over a wider frequency range. A second wire link (labelled LK2 on the PCB) connects V_{OUT} (SKT1) to either the output of this sample-and-hold circuit or directly to the output of the AD7840.

INTERFACE CONNECTIONS

There are two parallel connectors, labeled SKT4 and SKT6, and one serial connector, labeled SKT5. A shorting plug option (LK8 in Figure 25) on the AD7840 $\overline{CS}$/SERIAL input configures the DAC for the appropriate interface (see Pin Function Description).

SKT6 is a 96-contact (3-row) Eurocard connector which is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded chip enable outputs labeled $\overline{ECE1}$ to $\overline{ECE8}$. $\overline{ECE6}$ is used to drive the AD7840 $\overline{CS}$ input on the data acquisition board. To avoid selecting on-board sockets at the same time, LK6 on the ADSP-2100 board must be removed. The AD7840 and ADSP-2100 data lines are aligned for left justified data transfer.

SKT4 is a 26-way (2-row) IDC connector. This connector contains the same signal contacts as SKT6 and in addition contains decoded R/$\overline{W}$ and $\overline{STRB}$ inputs which are necessary for TMS32020 interfacing. This decoded $\overline{WR}$ can be selected via LK4. The pinout for this connector is shown in Figure 29.

SKT5 is a nine-way D-type connector which is meant for serial interfacing only. The evaluation board has the facility to invert $\overline{SYNC}$ line via LK7. This is necessary for serial interfacing between the AD7840 and DSP processors such as the DSP56000 The SKT5 pinout is shown in Figure 30.

SKT1, SKT2 and SKT3 are three BNC connectors which provide connections for the analog output, the $\overline{LDAC}$ input and an external reference input. The use of an external reference is optional; the shorting plug (LK3) connects the REF IN pin to either this external reference or to the AD7840's own internal reference.

Wire links LK5 and LK6 connect the D11 and D10 inputs to the data lines for parallel operation. In the serial mode, these links allow the user to select the required format and justification for serial data (see Table I).

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5V digital supply. Connections to the analog supplies are made directly to the PCB as shown on the silkscreen in Figure 26. The connections are labelled V+ and V− and the range for both of these supplies is 12V to 15V. Connection to the 5V digital supply is made through any of the connectors (SKT4 to SKT6). The −5V analog supply required by the AD7840 is generated from a voltage regulator on the V− power supply input (IC5 in Figure 25).

SHORTING PLUG OPTIONS

There are eight shorting plug options which must be set before using the board. These are outlined below:

LK1	Connects the analog output to SKT1. The analog output may also be connected to a component grid for signal conditioning.
LK2	Selects either the AD7840 V_{OUT} or the sample-and-hold output.
LK3	Selects either the internal or external reference.
LK4	Selects the decoded R/$\overline{W}$ and $\overline{STRB}$ inputs for TMS32020 interfacing.
LK5	Configures the D11/FORMAT input.
LK6	Configures the D10/JUSTIFY input.
LK7	Selects either the inverted or noninverted $\overline{SYNC}$.
LK8	Selects either parallel or serial interfacing.

COMPONENT LIST

IC1	AD7840 Digital-to-Analog Converter
IC2	AD711 Op Amp
IC3	ADG201HS High Speed Switch
IC4	74HC221 Monostable
IC5	79L05 Voltage Regulator
IC6	74HC02
C1, C3, C5, C7, C11, C13, C15, C17	10μF Capacitors
C2, C4, C6, C8, C12, C14, C16, C18	0.1μF Capacitors
C9	330pF Capacitor
C10	68pF Capacitor
R1, R2	2.2kΩ Resistors
R3	15kΩ Resistor
RP1, RP2	100kΩ Resistor Packs
LK1, LK2, LK3, LK4, LK5, LK6, LK7, LK8	Shorting Plugs
SKT1, SKT2, SKT3	BNC Sockets
SKT4	26-Contact (2-Row) IDC Connector
SKT5	9-Contact D-Type Connector
SKT6	96-Contact (3-Row) Eurocard Connector

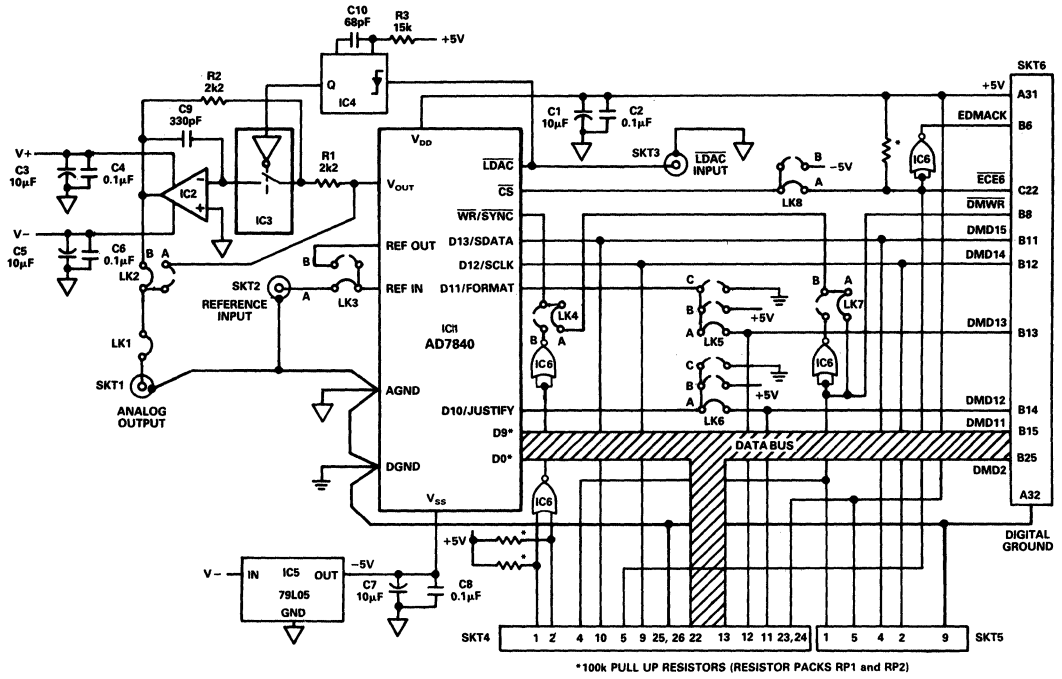


Figure 25. Data Acquisition Circuit Using the AD7840

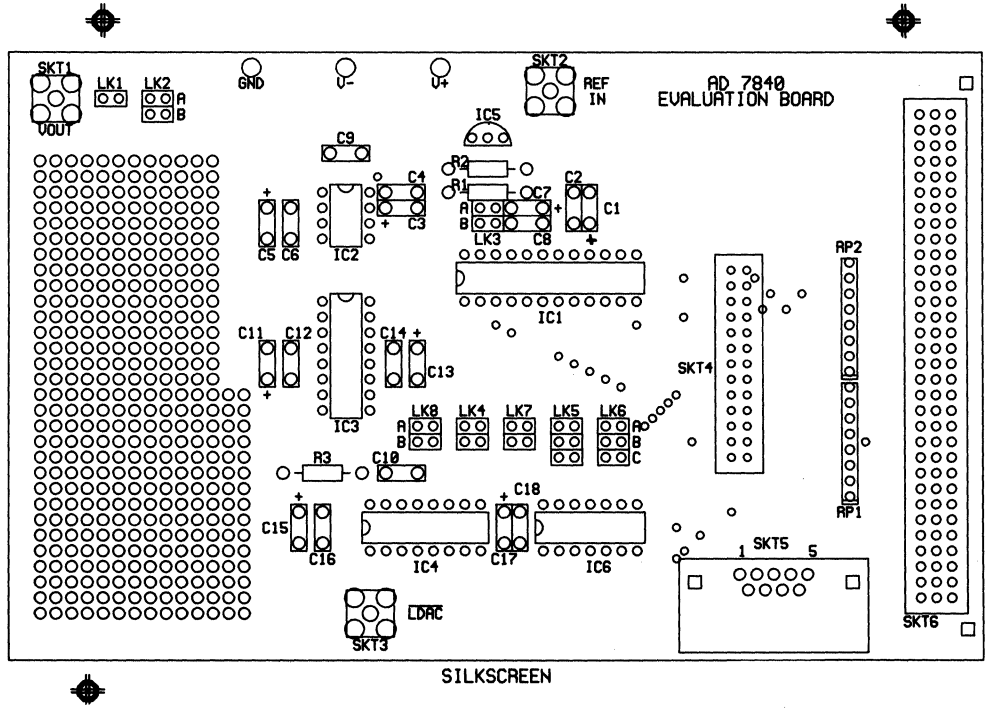


Figure 26. PCB Silkscreen for Figure 25

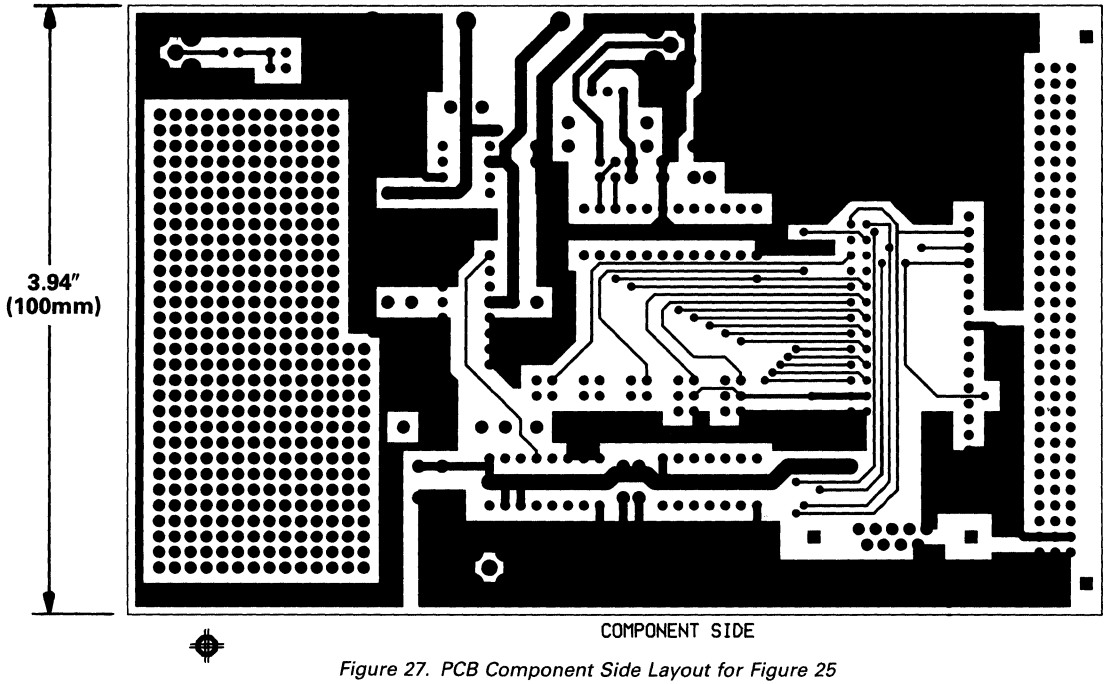


Figure 27. PCB Component Side Layout for Figure 25

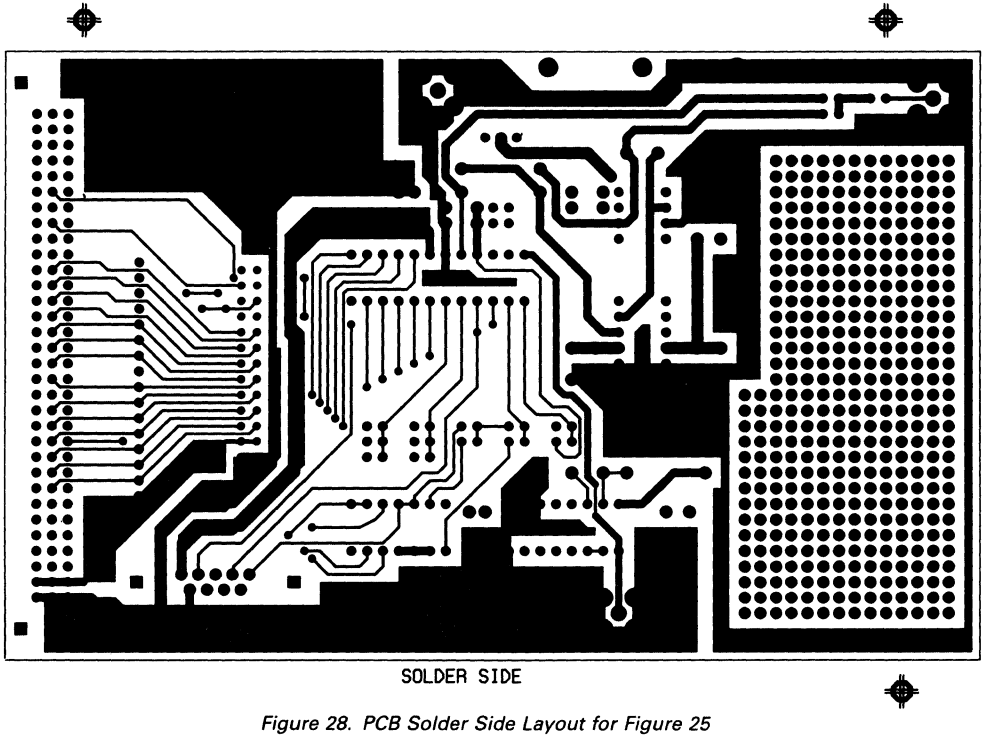


Figure 28. PCB Solder Side Layout for Figure 25

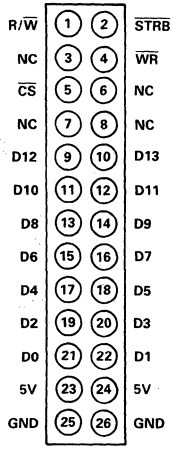


Figure 29. SKT4, IDC Connector Pinout

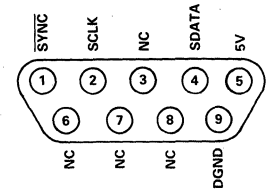


Figure 30. SKT5, D-Type Connector Pinout

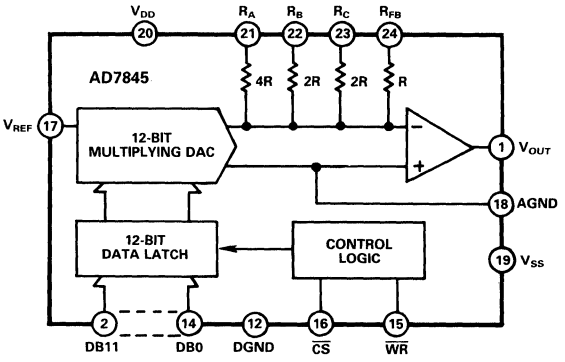
ANALOG DEVICES

LC²MOS
Complete 12-Bit Multiplying DAC
AD7845

FEATURES
- 12-Bit CMOS MDAC with Output Amplifier
- 4-Quadrant Multiplication
- Guaranteed Monotonic (T_{min} to T_{max})
- Space-Saving 0.3", 24-Pin DIPs and 28-Terminal Surface Mount Packages
- Application Resistors On Chip for Gain Ranging, etc.
- Low Power LC²MOS

APPLICATIONS
- Automatic Test Equipment
- Digital Attenuators
- Programmable Power Supplies
- Programmable Gain Amplifiers
- Digital-to-4-20mA Converters

AD7845 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7845 is the industry's first 4-quadrant multiplying D/A converter with an on-chip amplifier. It is fabricated on the LC²MOS process, which allows precision linear components and digital circuitry to be implemented on the same chip.

The 12 data inputs drive latches which are controlled by standard $\overline{CS}$ and $\overline{WR}$ signals, making microprocessor interfacing simple. For stand-alone operation, the $\overline{CS}$ and $\overline{WR}$ inputs can be tied to ground, making all latches transparent. All digital inputs are TTL and 5V CMOS compatible.

The output amplifier can supply ± 10V into a 2kΩ load. It is internally compensated, and its input offset voltage is low due to laser trimming at wafer level. For normal operation, R_{FB} is tied to V_{OUT}, but the user may alternatively choose R_A, R_B or R_C to scale the output voltage range.

PRODUCT HIGHLIGHTS

1. Voltage Output Multiplying DAC
   The AD7845 is the first DAC which has a full 4-quadrant multiplying capability and an output amplifier on-chip. All specifications include amplifier performance.
2. Matched Application Resistors
   Three application resistors provide an easy facility for gain ranging, voltage offsetting, etc.
3. Space Saving
   The AD7845 saves space in two ways. The integration of the output amplifier on-chip means that chip count is reduced. The part is housed in a skinny 24-pin, 0.3" DIP and 28-terminal surface mount package.

SPECIFICATIONS[1] (V_{DD} = +15V, ±5%, V_{SS} = −15V, ±5%, V_{REF} = +10V, AGND = DGND = 0V, V_{OUT} connected to R_{FB}. V_{OUT} load = 2kΩ, 100pF. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J Version	K Version	A Version	B Version	S Version	T Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	$1LSB = \frac{V_{REF}}{2^{12}} = 2.4mV$
Relative Accuracy								
at +25°C	±1	±1/2	±1	±1/2	±1	±1/2	LSB max	All grades are guaranteed
T_{min} to T_{max}	±1	±3/4	±3/2	±1	±2	±1	LSB max	monotonic over temperature
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	DAC register loaded with
Zero Code Offset Error								all 0s.
at +25°C	±2	±1	±2	±1	±2	±1	mV max	
T_{min} to T_{max}	±4	±3	±4	±3	±5	±4	mV max	
Offset Temperature Coefficient; (ΔOffset/ΔTemperature)[2]	±5	±5	±5	±5	±5	±5	µV/°C typ	
Gain Error	±6	±3	±6	±3	±6	±3	LSB max	R_{FB}, V_{OUT} connected.
	±9	±6	±9	±6	±9	±6	LSB max	R_C, V_{OUT} connected, V_{REF} = +5V
	±9	±6	±9	±6	±9	±6	LSB max	R_B, V_{OUT} connected, V_{REF} = +5V
	±10	±8	±10	±8	±10	±8	LSB max	R_A, V_{OUT} connected, V_{REF} = 2.5V
Gain Temperature Coefficient; (ΔGain/ΔTemperature)[2]	±2	±2	±2	±2	±2	±2	ppm of FSR/°C typ	R_{FB}, V_{OUT} connected.
REFERENCE INPUT								
Input Resistance, Pin 17	8	8	8	8	8	8	kΩ min	Typical input resistance = 12kΩ
	16	16	16	16	16	16	kΩ max	
APPLICATION RESISTOR RATIO MATCHING	0.5	0.5	0.5	0.5	0.5	0.5	% max	Matching between R_A, R_B, R_C
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±1	±1	±1	±1	±1	±1	µA max	Digital Inputs at 0V and V_{DD}
C_{IN} (Input Capacitance)[2]	7	7	7	7	7	7	pF max	
POWER SUPPLY[4]								
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V min/V max	
V_{SS} Range	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	−14.25/−15.75	V min/V max	
Power Supply Rejection								
ΔGain/ΔV_{DD}	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	V_{DD} = 15V ± 5%, V_{REF} = −10V
ΔGain/ΔV_{SS}	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	V_{SS} = −15V ± 5%.
I_{DD}	10	10	10	10	10	10	mA max	V_{OUT} unloaded.
I_{SS}	4	4	4	4	4	4	mA max	V_{OUT} unloaded.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance and are not subject to test.

DYNAMIC PERFORMANCE								
Output Voltage Settling Time	5	5	5	5	5	5	µs max	To 0.01% of full-scale range. V_{OUT} load = 2kΩ, 100pF. DAC register alternately loaded with all 0s and all 1s. Typically 2.5µs at 25°C.
Slew Rate	7	7	7	7	7	7	V/µs typ	V_{OUT} load = 2kΩ, 100pF.
Digital-to-Analog Glitch Impulse	450	450	450	450	450	450	nV-s typ	Measured with V_{REF} = 0V. DAC register alternately loaded with all 0s and all 1s.
Multiplying Feedthrough Error[3]	5	5	5	5	5	5	mVp-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0s.
Unity Gain Small Signal Bandwidth	600	600	600	600	600	600	kHz typ	V_{OUT}, R_{FB} connected. DAC loaded with all 1s. V_{REF} = 100mV p-p sine wave.
Full Power Bandwidth	250	250	250	250	250	250	kHz typ	V_{OUT}, R_{FB} connected. DAC loaded with all 1s. V_{REF} = 20V p-p sine wave. R_L = 2kΩ.
Total Harmonic Distortion	−90	−90	−90	−90	−90	−90	dB typ	V_{REF} = 6V rms, 1kHz sine wave.
OUTPUT CHARACTERISTICS[5]								
Open Loop Gain	85	85	85	85	85	85	dB min	V_{OUT}, R_{FB} not connected
Output Voltage Swing	±10	±10	±10	±10	±10	±10	V min	V_{OUT} = ±10V, R_L = 2kΩ R_L = 2kΩ, C_L = 100pF
Output Resistance	0.2	0.2	0.2	0.2	0.2	0.2	Ω typ	R_{FB}, V_{OUT} connected,
Short Circuit Current (@ +25°C	15	15	15	15	15	15	mA typ	V_{OUT} shorted to AGND
Output Noise Voltage (0.1Hz to 10Hz) (@ +25°C	2	2	2	2	2	2	µV rms typ	Includes noise due to output amplifier and Johnson Noise of R_{FB}
f = 10Hz	250	250	250	250	250	250	nV/√Hz typ	
f = 100Hz	100	100	100	100	100	100	nV/√Hz typ	
f = 1kHz	50	50	50	50	50	50	nV/√Hz typ	
f = 10kHz	50	50	50	50	50	50	nV/√Hz typ	
f = 100kHz	50	50	50	50	50	50	nV/√Hz typ	

NOTES

[1]Temperature Ranges are as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2]Sample tested to ensure compliance.

[3]The metal lid on the ceramic D-24A package is connected to Pin 12 (DGND).

[4]The device is functional with a power supply of ±12V. See Figure 6.

[5]Minimum specified load resistance is 2kΩ.

Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{DD} = +15V, ±5%. V_{SS} = −15V, ±5%. V_{REF} = +10V. AGND = DGND = 0V.)

Parameter	Limit at T_A = +25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{CS}	100	135	140	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	100	135	140	ns min	Write Pulse Width
t_{DS}	100	100	120	ns min	Data Setup Time
t_{DH}	20	20	20	ns min	Data Hold Time

Specifications subject to change without notice

2

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3V, +17V
V_{SS} to DGND . . . . . +0.3V, −17V
V_{REF} to AGND . . . . . ±25V
V_{RFB} to AGND . . . . . ±25V
V_{RA} to AGND . . . . . ±25V
V_{RB} to AGND . . . . . ±25V
V_{RC} to AGND . . . . . ±25V
V_{OUT} to AGND[1] . . . . . V_{DD} +0.3V, V_{SS} −0.3V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package)
To +75°C 650mW
Derates above +75°C . . . . . 10mW/°C

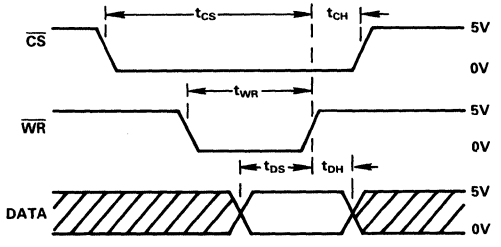
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

NOTE
[1]V_{OUT} may be shorted to AGND provided that the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



NOTES
1. All INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% to 90% of +5V. $t_R = t_F = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. AD7845 Timing Diagram

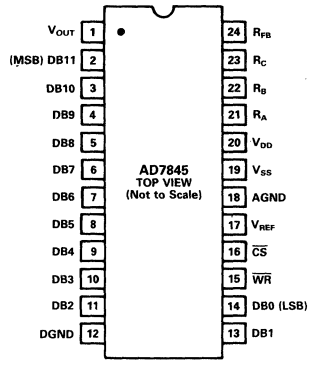
ORDERING INFORMATION[1]

Relative Accuracy +25°C	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C[3]
	Plastic DIP (N-24)	Hermetic DIP (Q-24)	Hermetic DIP (Q-24)
±1LSB	AD7845JN	AD7845AQ	AD7845SQ/883B
±1/2LSB	AD7845KN	AD7845BQ	AD7845TQ/883B
	PLCC[4] (P-28A)		LCCC[5] (E-28A)
±1LSB	AD7845JP		AD7845SE /883B
±1/2LSB	AD7845KP		

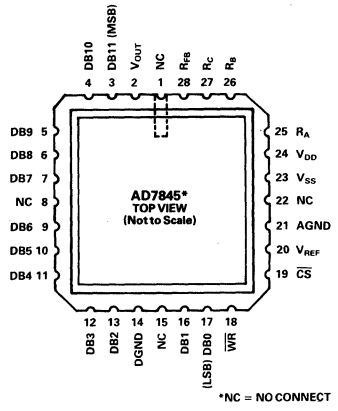
NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24A) hermetic packages.
[2]See Section 14 for package outline information.
[3]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier. Available to 883B processing only.

PIN CONFIGURATIONS

DIP

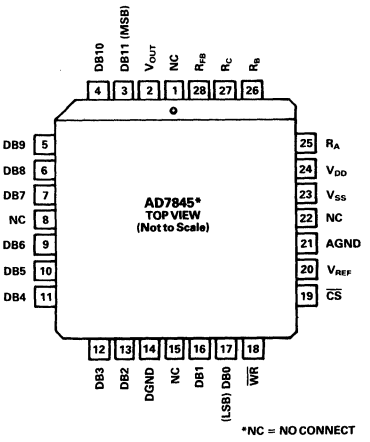


LCCC



*NC = NO CONNECT

PLCC



*NC = NO CONNECT

TERMINOLOGY

LEAST SIGNIFICANT BIT
This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7845, 1LSB = $\frac{V_{REF}}{2^{12}}$

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., offset and gain error are adjusted out) and is normally expressed in least significant bits or as a percentage of full-scale range.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of +1LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer. See Figure 13.

ZERO CODE OFFSET ERROR
This is the error present at the device output with all 0s loaded in the DAC. It is due to the op amp input offset voltage and bias current and the DAC leakage current.

TOTAL HARMONIC DISTORTION
This is the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental, expressed in dBs.

OUTPUT NOISE
This is the noise due to the white noise of the DAC and the input noise of the amplifier.

DIGITAL-TO-ANALOG GLITCH IMPULSE
This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. The measurement takes place with V_{REF} = AGND.

DIGITAL FEEDTHROUGH
When the DAC is not selected (i.e., $\overline{CS}$ is high) high frequency logic activity on the device digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

MULTIPLYING FEEDTHROUGH ERROR
This is ac error due to capacitive feedthrough from the V_{REF} terminal to V_{OUT} when the DAC is loaded with all 0s.

OPEN LOOP GAIN
Open loop gain is defined as the ratio of a change of output voltage to the voltage applied at the V_{REF} pin with all 1s loaded in the DAC. It is specified at dc.

UNITY GAIN SMALL SIGNAL BANDWIDTH
This is the frequency at which the magnitude of the small signal voltage gain of the output amplifier is 3dB below unity. The device is operated as a closed loop unity gain inverter (i.e., DAC is loaded with all 1s).

OUTPUT RESISTANCE
This is the effective output source resistance.

FULL POWER BANDWIDTH
Full power bandwidth is specified as the maximum frequency, at unity closed loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a distortion level of 3%.

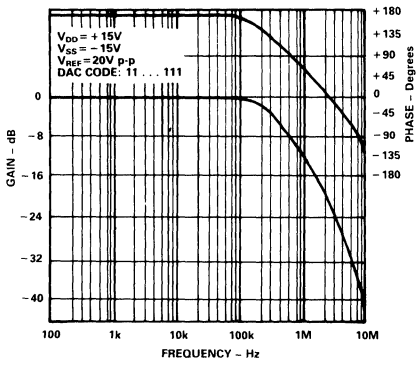


Figure 2. Frequency Response, G = −1

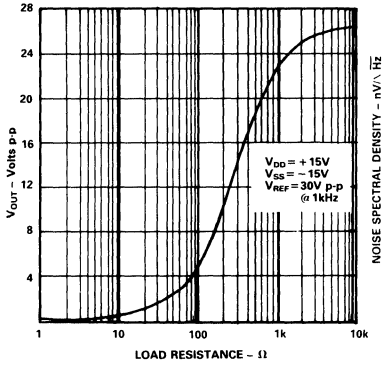


Figure 3. Output Voltage Swing vs. Resistive Load

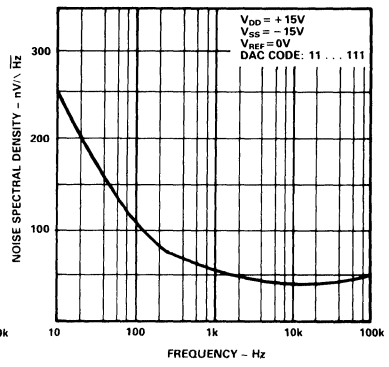


Figure 4. Noise Spectral Density

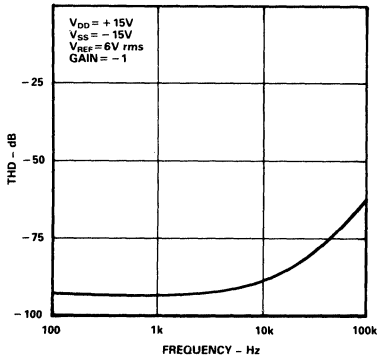


Figure 5. THD vs. Frequency

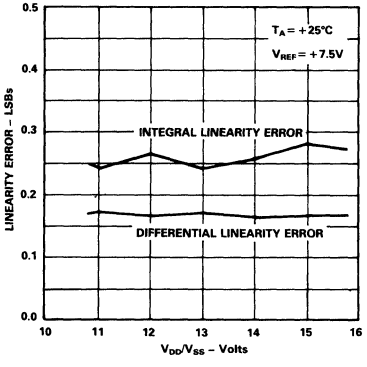


Figure 6.Typical AD7845 Linearity vs. Power Supply

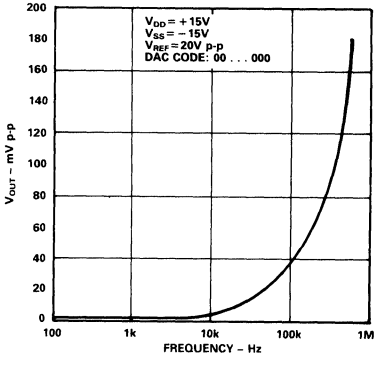


Figure 7. Multiplying Feedthrough Error vs. Frequency

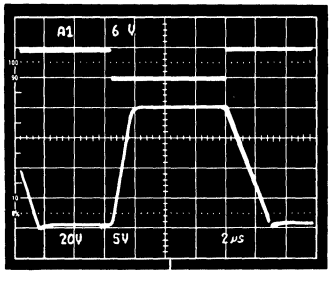


Figure 8. Unity Gain Inverter Pulse Response (Large Signal)

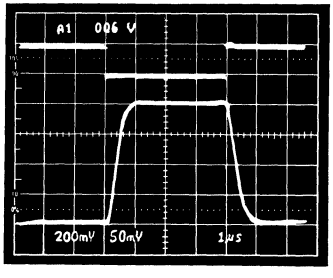


Figure 9. Unity Gain Inverter Pulse Response (Small Signal)

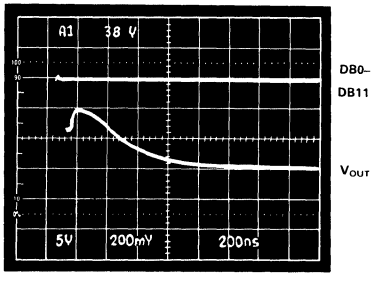


Figure 10. Digital-to-Analog Glitch Impulse (All 1s to All 0s Transition)

PIN FUNCTION DESCRIPTION (DIP)

Pin	Mnemonic	Description
1	V_{OUT}	Voltage Output Terminal
2-11	DB11-DB2	Data Bit 11 (MSB) to Data Bit 2
12	DGND	Digital Ground. The metal lid on the ceramic package is connected to this pin
13-14	DB1-DB0	Data Bit 1 to Data Bit 0 (LSB)
15	$\overline{WR}$	Write Input. Active low
16	$\overline{CS}$	Chip Select Input. Active low
17	V_{REF}	Reference Input Voltage which can be an ac or dc signal
18	AGND	Analog Ground. This is the reference point for external analog circuitry
19	V_{SS}	Negative power supply for the output amplifier (nominal −12V to −15V)
20	V_{DD}	Positive power supply (nominal +12V to +15V)
21	R_A	Application resistor. $R_A = 4R_{FB}$
22	R_B	Application resistor. $R_B = 2R_{FB}$
23	R_C	Application resistor. $R_C = 2R_{FB}$
24	R_{FB}	Feedback resistor in the DAC. For normal operation this is connected to V_{OUT}

CIRCUIT INFORMATION

Digital Section

Figure 11 is a simplified circuit diagram of the AD7845 input control logic. When $\overline{CS}$ and $\overline{WR}$ are both low, the DAC latch is loaded with the data on the data inputs. All the digital inputs are TTL, HCMOS and +5V CMOS compatible, facilitating easy microprocessor interfacing. All digital inputs incorporate standard protection circuitry.

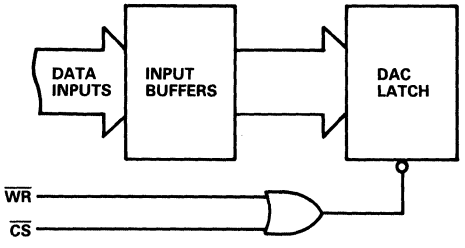


Figure 11. AD7845 Input Control Logic

D/A Section

Figure 12 shows a simplified circuit diagram for the AD7845 D/A section and output amplifier. The D/A converter is a standard R-2R ladder. Binarily weighted currents are switched between AGND and the inverting terminal of the on-chip output amplifier. The output amplifier and feedback resistor R_{FB} perform the current-to-voltage conversion. When connected in the standard configuration (i.e., R_{FB} connected to V_{OUT}),

$$V_{OUT} = -D \cdot V_{REF},$$

where D is the fractional representation of the digital input code. D can vary from 0 to 4095/4096.

The amplifier can maintain ±10V across a 2kΩ load. It is internally compensated and settles to 0.01% FSR (1/2LSB) in less than 5μs. The input offset voltage is laser trimmed at wafer level. The amplifier slew rate is typically 7V/μs, and the unity gain small signal bandwidth is 600kHz. There are three extra on-chip resistors (R_A, R_B, R_C) connected to the amplifier inverting terminal. These are useful in a number of applications including offset adjustment and gain ranging.

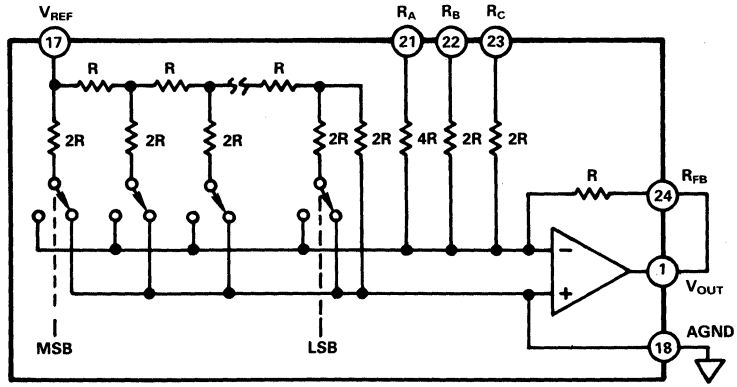


Figure 12. Simplified Circuit Diagram for the AD7845 D/A Section and Output Amplifier

UNIPOLAR BINARY OPERATION

Figure 13 shows the AD7845 connected for unipolar binary operation. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. The code table for Figure 13 is given in Table I.

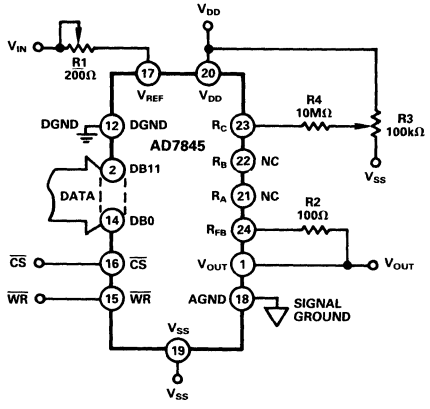


Figure 13. Unipolar Binary Operation

Binary Number In DAC Register			Analog Output, V_{OUT}
MSB		LSB	
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\,V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0V

Table I. Unipolar Binary Code Table for AD7845

OFFSET AND GAIN ADJUSTMENT FOR FIGURE 13

Zero Offset Adjustment

1. Load DAC with all 0s.
2. Trim R3 until V_{OUT} = 0V.

Gain Adjustment

1. Load DAC with all 1s.
2. Trim R1 so that $V_{OUT} = -V_{IN}\frac{4095}{4096}$

In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude. For high temperature applications, resistors and potentiometers should have a low temperature coefficient.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit for bipolar operation is shown in Figure 14. Offset binary coding is used.

The offset specification of this circuit is determined by the matching of internal resistors R_B and R_C and by the zero code offset error of the device. Gain error may be adjusted by varying the ratio of R1 and R2.

To use this circuit without trimming and keep within the gain error specifications, resistors R1 and R2 should be ratio matched to 0.01%.

The code table for Figure 14 is given in Table II.

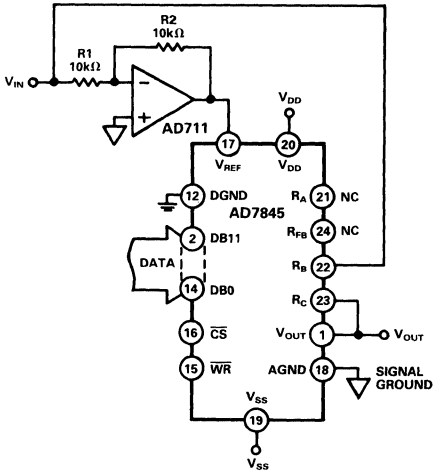


Figure 14. Bipolar Offset Binary Operation

Binary Number In DAC Register			Analog Output, V_{OUT}
MSB		LSB	
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right) = -V_{IN}$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 14

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The AD7845 performs a PGA function when connected as in Figure 15. In this configuration, the R-2R ladder is connected in the amplifier feedback loop. R_{FB} is the amplifier input resistor. As the code decreases, the R-2R ladder resistance increases and so the gain increases.

$$V_{OUT} = -V_{IN} \cdot \frac{R_{DAC}}{D} \cdot \frac{1}{R_{FB}}, \quad \left(D = 0 \text{ to } \frac{4095}{4096}\right)$$

$$= -V_{IN} \cdot \frac{R_{DAC}}{D} \cdot \frac{1}{R_{DAC}} = \frac{-V_{IN}}{D}, \text{ since } R_{FB} = R_{DAC}$$

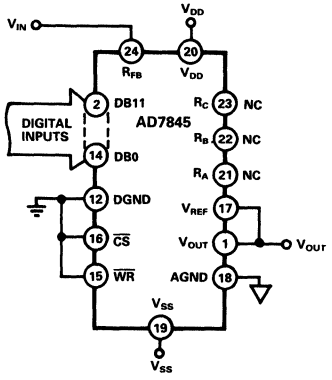


Figure 15. AD7845 Connected as PGA

As the programmed gain increases, the error and noise also increase. For this reason, the maximum gain should be limited to 256. Table III shows gain versus code.

Digital Inputs			Gain	Error (%)
1111	1111	1111	4096/4095 ≈1	0.04
1000	0000	0000	2	0.07
0100	0000	0000	4	0.13
0010	0000	0000	8	0.26
0001	0000	0000	16	0.51
0000	1000	0000	32	1.02
0000	0100	0000	64	2.0
0000	0010	0000	128	4.0
0000	0001	0000	256	8.0

Table III. Gain and Error vs. Input Code for Figure 15

Note that instead of using R_{FB} as the input resistor, it is also possible to use combinations of the other application resistors, R_A, R_B and R_C. For instance, if R_B is used instead of R_{FB}, the gain range for the same codes of Table II now goes from 1/2 to 128.

PROGRAMMABLE CURRENT SOURCES

The AD7845 is ideal for designing programmable current sources using a minimum of external components. Figures 16 and 17 are examples. The circuit of Figure 16 drives a programmable current I_L into a load referenced to a negative supply. Figure 17 shows the circuit for sinking a programmable current, I_L. The same set of circuit equations apply for both diagrams.

$$I_L = I_3 = I_2 + I_1$$

$$I_1 = \frac{D \cdot |V_{IN}|}{R_{DAC}}, \left(D = 0 \text{ to } \frac{4095}{4096}\right)$$

$$I_2 = \frac{1}{R1}\left(\frac{D \cdot |V_{IN}|}{R_{DAC}}\right) R_{FB} = \frac{D \cdot |V_{IN}|}{R1}, \text{ since } R_{FB} = R_{DAC}$$

$$I_L = \frac{D \cdot |V_{IN}|}{R1} + \frac{D \cdot |V_{IN}|}{R_{DAC}}$$

$$= \frac{D \cdot |V_{IN}|}{R1} \cdot \left(1 + \frac{R1}{R_{DAC}}\right)$$

Note that by making R1 much smaller than R_{DAC}, the circuit becomes insensitive to both the absolute value of R_{DAC} and its temperature variations. Now, the only resistor determining load current I_L is the sense resistor R1.

If $R_1 = 100\Omega$, then the programming range is 0 to 100mA, and the resolution is 0.024mA.

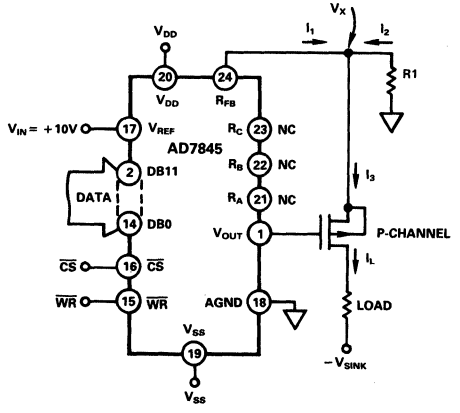


Figure 16. Programmable Current Source

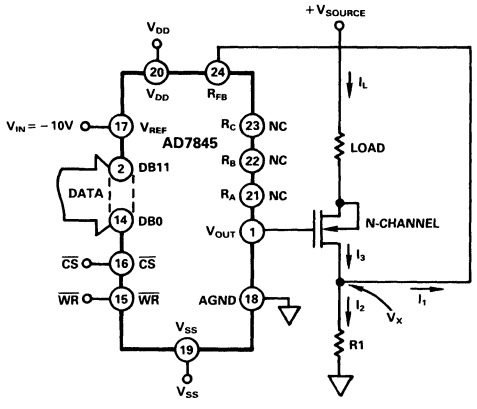


Figure 17. Programmable Current Sink

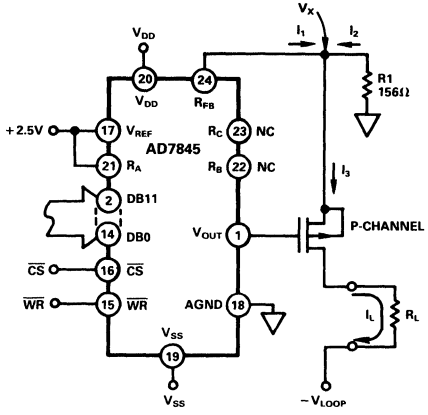


Figure 18. 4-20mA Current Loop

4-20mA CURRENT LOOP

The AD7845 provides an excellent way of making a 4-20mA current loop circuit. This is basically a variation of the circuits in Figures 16 and 17 and is shown in Figure 18. The application resistor R_A (Value 4R) produces the effective 4mA offset.

$$I_L = I_3 = I_2 + I_1$$

Since $I_2 >> I_1$,

$$I_L = -\frac{V_X}{156} = \left(\frac{2.5}{4R} \times R_{FB} + \frac{2.5}{R_{DAC}} \times D \times R_{FB}\right) \times \frac{1}{156}$$

and since $R_{DAC} = R_{FB} = R$

$$I_L = \left(\frac{2.5}{4} + D \times 2.5\right) \times \frac{1000}{156} \text{ mA}$$

$= [4 + (16 \times D)]$mA, where D goes from 0 to 1 with Digital Code

When D = 0 (Code of all 0s):
$I_L = 4$mA

When D = 1 (Code of all 1s):
$I_L = 20$mA

The above circuit succeeds in significantly reducing the circuit component count. Both the on-chip output amplifier and the application resistor R_A contribute to this.

APPLICATION HINTS

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7845. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7845 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When a new digital word is written into the DAC, it results in a change of voltage applied to some of the DAC switch gates. This voltage change is coupled across the switch stray capacitance and appears as an impulse on the current output bus of the DAC. In the AD7845, impulses on this bus are converted to a voltage by R_{FB} and the output amplifier. The output voltage glitch energy is specified as the area of the resulting spike in nV-seconds. It is measured with V_{REF} connected to analog ground and for a zero to full scale input code transition. Since microprocessor based systems generally have noisy grounds which couple into the power supplies, the AD7845 V_{DD} and V_{SS} terminals should be decoupled to signal ground.

Temperature Coefficients: The gain temperature coefficient of the AD7845 has a maximum value of 5ppm/°C. This corresponds to worst case gain shift of 2LSBs over a 100°C temperature range. When trim resistors R1 and R2 in Figure 13 are used to adjust full scale range, the temperature coefficient of R1 and R2 must also be taken into account. The offset temperature coefficient is 5ppm of FSR/°C maximum. This corresponds to a worst case offset shift of 2 LSBs over a 100°C temperature range.

The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs," Publication Number E630C-5-3/86.

MICROPROCESSOR INTERFACING

16-BIT MICROPROCESSOR SYSTEMS

Figures 19, 20 and 21 show how the AD7845 interfaces to three popular 16-bit microprocessor systems. These are the MC68000, 8086 and the TMS32010. The AD7845 is treated as a memory-mapped peripheral to the processors. In each case, a write instruction loads the AD7845 with the appropriate data. The particular instructions used are as follows:

MC68000: MOVE
8086: MOV
TMS32010: OUT

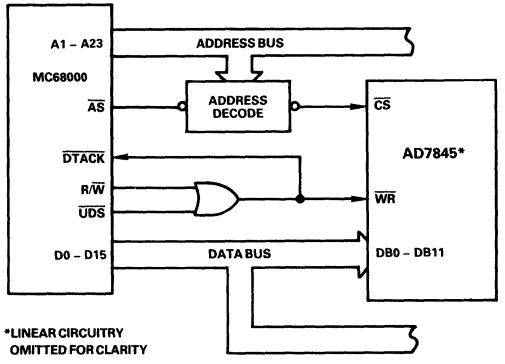


Figure 19. AD7845 to MC68000 Interface

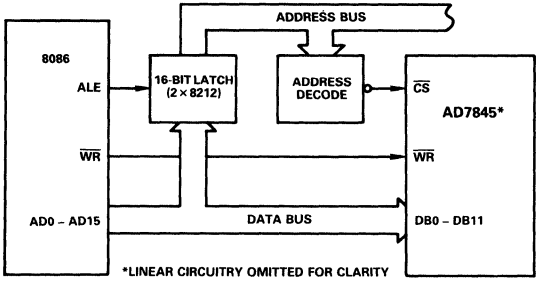


Figure 20. AD7845 to 8086 Interface

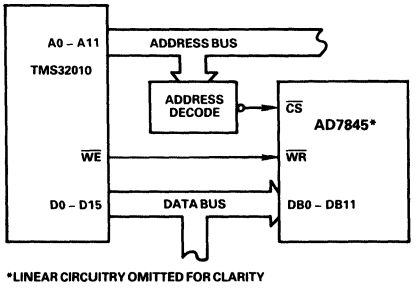


Figure 21. TMS32010 Interface

8-BIT MICROPROCESSOR SYSTEMS

Figure 22 shows an interface circuit for the AD7845 to the 8085A 8-bit microprocessor. The software routine to load data to the device is given in Table IV. Note that the transfer of the 12-bits of data requires two write operations. The first of these loads the 4 MSBs into the 7475 latch. The second write operation loads the 8 LSBs plus the 4 MSBs (which are held by the latch) into the DAC.

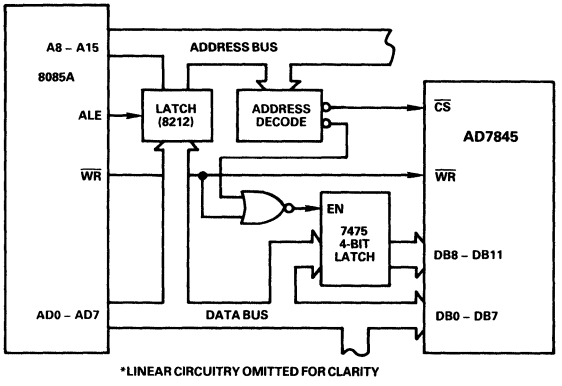
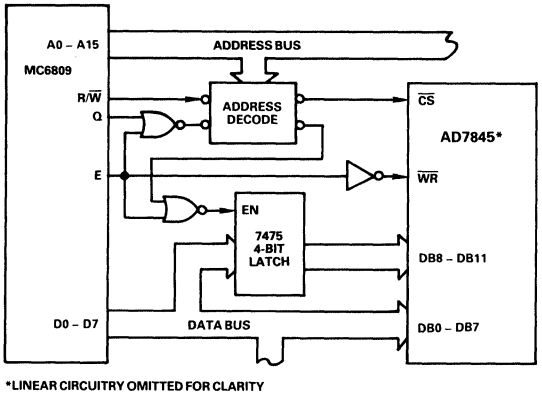


Figure 22. 8085A Interface

2000	LOAD DAC : LXI	H,#3000	The H,L register pair are loaded with latch address 3000.
	MVI	A,#"MS"	Load the 4 MSBs of data into accumulator.
	MOV	M,A	Transfer data from accumulator to latch.
	INR	L	Increment H,L pair to AD7845 address.
	MVI	A,#"LS"	Load the 8 LSBs of data into accumulator.
	MOV	M,A	Transfer data from accumulator to DAC.
	RET		End of routine.

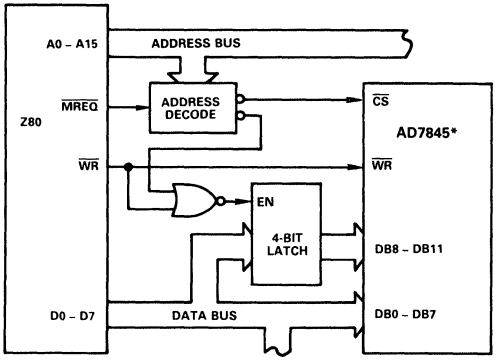
Table IV. Subroutine Listing for Figure 22

Figures 23 and 24 are the interface circuits for the Z80 and MC6809 microprocessors. Again, these use the same basic format as the 8085A interface.



*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 23. AD7845 to Z80 Interface

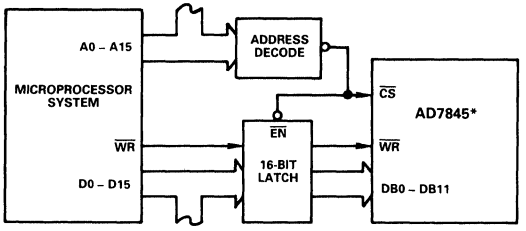


*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 24. MC6809 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7845 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this digital feedthrough isolate the DAC from the noise source. Figure 25 shows an interface circuit which uses this technique. All data inputs are latched from the busy by the $\overline{CS}$ signal. One may also use other means, such as peripheral interface devices, to reduce the digital feedthrough.



*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 25. AD7845 Interface Circuit Using Latches to Minimize Digital Feedthrough

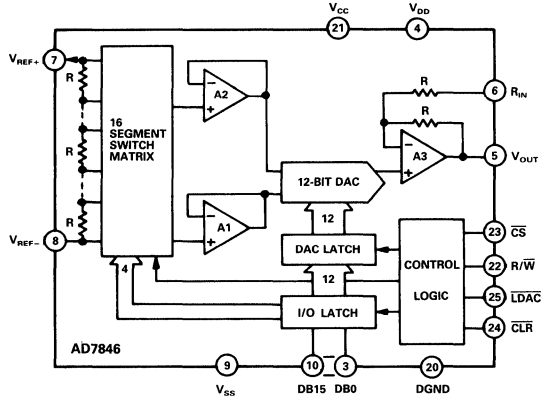
LC²MOS 16-Bit Voltage Output DAC

AD7846

FEATURES

16-Bit Monotonicity over Temperature
±2LSBs Integral Linearity Error
Microprocessor Compatible with Readback Capability
Unipolar or Bipolar Output
Multiplying Capability
Low Power (100mW typical)

AD7846 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7846 is a 16-bit DAC constructed with Analog Devices' LC²MOS process. It has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier. These can be configured to give a unipolar output range (0 to +5V, 0 to +10V) or bipolar output ranges (±5V, ±10V).

The DAC uses a segmented architecture. The 4MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers.

In addition to the excellent accuracy specifications, the AD7846 also offers a comprehensive microprocessor interface. There are 16 data I/O pins, plus control lines ($\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$). R/$\overline{W}$ and $\overline{CS}$ allow writing to and reading from the I/O latch. This is the readback function which is useful in ATE applications. $\overline{LDAC}$ allows simultaneous updating of DACs in a multi-DAC system and the $\overline{CLR}$ line will reset the contents the DAC latch to 00 . . . 000 or 10 . . . 000 depending on the state of R/$\overline{W}$. This means that the DAC output can be reset to 0V in both the unipolar and bipolar configurations.

The AD7846 is available in 28-pin plastic, ceramic and LCCC packages.

PRODUCT HIGHLIGHTS

1. 16-Bit Monotonicity
   The guaranteed 16-bit monotonicity over temperature makes the AD7846 ideal for closed-loop applications.
2. Readback
   The ability to read back the DAC register contents minimizes software routines when the AD7846 is used in ATE systems.
3. Power Dissipation
   Power dissipation of 100mW makes the AD7846 the lowest power, high accuracy DAC on the market.

SPECIFICATIONS[1]

(V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V. V_{OUT} loaded with 2kΩ, 1000pF to 0V. V_{REF+} = +5V, R_{IN} connected to 0V. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	J, A Versions	K, B Versions	S Version[2]	Units	Test Conditions/Comments
RESOLUTION	16	16	16	Bits	
UNIPOLAR OUTPUT					V_{REF-} = 0V, V_{OUT} = 0V to +10V
Relative Accuracy @ 25°C	±16	±4	±16	LSB max	1LSB = 153μV
T_{min} to T_{max}	±16	±8	±16	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ 25°C	±16	±8	±16	LSB max	V_{OUT} Load = 10MΩ
T_{min} to T_{max}	±16	±16	±24	LSB max	
Offset Error @ 25°C	±16	±8	±16	LSB max	
T_{min} to T_{max}	±16	±16	±24	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
BIPOLAR OUTPUT					V_{REF-} = −5V, V_{OUT} = −10V to +10V
Relative Accuracy @ 25°C	±8	±2	±8	LSB max	1LSB = 305μV
T_{min} to T_{max}	±8	±4	±8	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ 25°C	±8	±4	±8	LSB max	V_{OUT} Load = 10MΩ
T_{min} to T_{max}	±12	±8	±16	LSB max	
Offset Error @ 25°C	±8	±4	±8	LSB max	V_{OUT} Load = 10MΩ
T_{min} to T_{max}	±12	±8	±16	LSB max	
Bipolar Zero Error @ 25°C	±8	±4	±8	LSB max	
T_{min} to T_{max}	±12	±8	±16	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero TC[3]	±2	±2	±2	ppm FSR/°C typ	
REFERENCE INPUT					
Input Resistance	20	20	20	kΩ min	Resistance from V_{REF-} to V_{REF+}
	40	40	40	kΩ max	Typically 30kΩ
V_{REF+} Range	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	Volts	
V_{REF-} Range	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	Volts	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS}+4 to V_{DD}−3	V_{SS}+4 to V_{DD}−3	V_{SS}+4 to V_{DD}−3	V max	
Resistive Load	2	2	3	kΩ min	To 0V
Capacitive Load	1000	1000	1000	pF max	To 0V
Output Resistance	0.3	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	±25	mA typ	To 0V or Any Power Supply
DIGITAL INPUTS					
V_{IH} (Input High Voltage)	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	10	10	10	pF max	
DIGITAL OUTPUTS					
V_{OL} (Output Low Voltage)	0.4	0.4	0.4	Volts max	I_{SINK} = 1.6mA
V_{OH} (Output High Voltage)	4.0	4.0	4.0	Volts min	I_{SOURCE} = 400μA
Floating State Leakage Current	±10	±10	±10	μA max	DB0-DB15 = 0 to V_{CC}
Floating State Output Capacitance[3]	10	10	10	pF max	
POWER REQUIREMENTS[4]					
V_{DD}	+11.4/+15.75	+11.4/+15.75	+11.4/+15.75	Vmin/Vmax	
V_{SS}	−11.4/−15.75	−11.4/−15.75	−11.4/−15.75	Vmin/Vmax	
V_{CC}	+4.75/+5.25	+4.75/+5.25	+4.75/+5.25	Vmin/Vmax	
I_{DD}	5	5	5	mA max	V_{OUT} Unloaded
I_{SS}	5	5	5	mA max	V_{OUT} Unloaded
I_{CC}	1	1	1	mA max	
Power Supply Sensitivity[5]	1.5	1.5	2	LSB/V max	
Power Dissipation	100	100	100	mW typ	V_{OUT} Unloaded

NOTES

[1]Temperature Ranges as follows: J, K versions; 0 to +70°C
A, B versions; −25°C to +85°C
S version; −55°C to +125°C

[2]Minimum load for S version is 3kΩ.

[3]Sample tested to ensure compliance.

[4]AD7846 is functional with power supplies of ±12V. See Typical Performance Curves.

[5]Sensitivity of Gain Error, Offset Error and Bipolar Zero Error to V_{DD}, V_{SS} variations.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

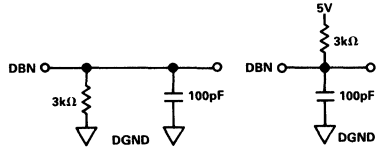
These characteristics are included for design guidance only and are not subject to test. (V_{REF+} = +5V, V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V, R_{IN} connected to 0V.)

Parameter	T_A = 25°C	T_A = T_{min} to T_{max}	Units	Test Conditions/Comments
Output Settling Time	7	7	μs max	To 0.006% FSR. V_{OUT} loaded. V_{REF-} = 0V.
	9	9	μs max	To 0.003% FSR. V_{OUT} loaded. V_{REF-} = −5V.
Digital-to-Analog Glitch Impulse	400	400	nV-secs typ	DAC alternately loaded with 10 . . . 0000 and 01 . . . 1111. V_{OUT} unloaded.
AC Feedthrough	0.5	0.5	mV pk-pk typ	V_{REF-} = 0V, V_{REF+} = 1V rms, 10kHz sine wave. DAC loaded with all 0s.
Digital Feedthrough	10	10	nV-secs typ	DAC alternately loaded with all 1s and all 0s. $\overline{CS}$ High.
Output Noise Voltage Density (1kHz–100kHz)	50	50	nV/$\sqrt{Hz}$ typ	Measured at V_{OUT}. DAC loaded with 0111011 . . . 11. V_{REF+} = V_{REF-} = 0V.

TIMING CHARACTERISTICS (V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V.)

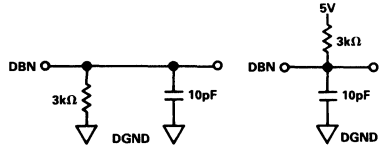
Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C, T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	40	40	50	ns min	R/$\overline{W}$ to $\overline{CS}$ Setup Time
t_2	150	160	190	ns min	$\overline{CS}$ Pulse Width (Write Cycle)
t_3	40	40	50	ns min	R/$\overline{W}$ to $\overline{CS}$ Hold Time
t_4	110	110	120	ns min	Data Setup Time
t_5	0	0	0	ns min	Data Hold Time
t_6	230	270	320	ns max	Data Access Time
t_7	10	10	10	ns min	Bus Relinquish Time
	80	90	90	ns max	
t_8	20	20	20	ns min	$\overline{CLR}$ Setup Time
t_9	150	150	150	ns min	$\overline{CLR}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{CLR}$ Hold Time
t_{11}	80	100	100	ns min	$\overline{LDAC}$ Pulse Width
t_{12}	240	280	330	ns min	$\overline{CS}$ Pulse Width (Read Cycle)

NOTES
[1]Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_R = t_F = 5 ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for an output to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High Z to V_{OH} *b. High Z to V_{OL}*

Figure 1. Load Circuits for Access Time (t_6)



a. V_{OH} to High Z *b. V_{OL} to High Z*

Figure 2. Load Circuits for Bus Relinquish Time (t_7)

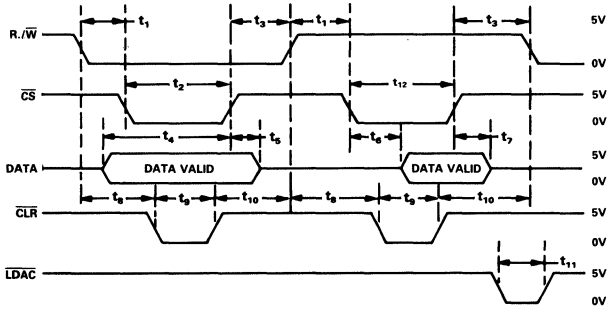


Figure 3. AD7846 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND . . . . . −0.3V to +17V
V_{CC} to DGND . . . . . −0.3V to +7V
V_{SS} to DGND . . . . . +0.3V to −17V
V_{REF+} to DGND . . . . . ±25V
V_{REF-} to DGND . . . . . ±25V
V_{OUT} to DGND[2] . . . . . ±25V
R_{IN} to DGND . . . . . ±25V
Digital Input Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Digital Output Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C
Operating Temperature Range
J, K Versions . . . . . 0 to +70°C
A, B Versions . . . . . −25°C to +85°C
S Version . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.
[2]V_{OUT} may be shorted to DGND, V_{DD}, V_{SS}, V_{CC} provided that the power dissipation of the package is not exceeded.

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however. permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

Least Significant Bit
This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7846, 1LSB = $(V_{REF+} - V_{REF-})/2^{16}$.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., offset and gain errors are adjusted out) and is normally expressed in least significant bits or as a percentage of full scale range.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error
Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer.

Offset Error
This is the error present at the device output with all 0s loaded in the DAC. It is due to op amp input offset voltage and bias current and the DAC leakage current.

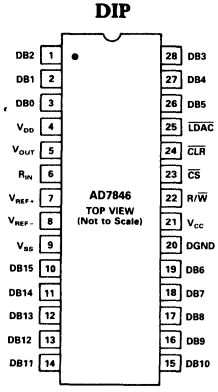
Bipolar Zero Error
When the AD7846 is connected for bipolar output and 10 . . . 000 is loaded to the DAC, the deviation of the analog output from the ideal midscale of 0V is called the bipolar zero error.

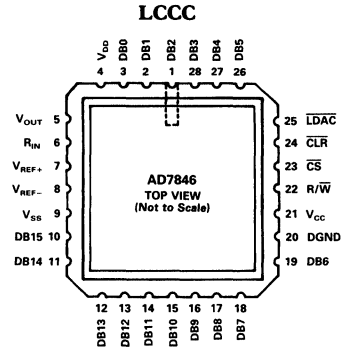
Digital-to-Analog Glitch Impulse
This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or a voltage.

Multiplying Feedthrough Error
This is an ac error due to capacitive feedthrough from either of the V_{REF} terminals to V_{OUT} when the DAC is loaded with all 0s.

Digital Feedthrough
When the DAC is not selected (i.e., $\overline{CS}$ is held high), high frequency logic activity on the digital inputs in capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

PIN CONFIGURATIONS





PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1–3	DB2–DB0	Data I/O pins. DB0 is LSB.
4	V_{DD}	Positive supply for analog circuitry. This is +15V nominal.
5	V_{OUT}	DAC output voltage pin.
6	R_{IN}	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges. See Table I.
7	V_{REF+}	V_{REF+} input. The DAC is specified for V_{REF+} = +5V.
8	V_{REF-}	V_{REF-} input. For unipolar operation connect V_{REF-} to 0V and for bipolar operation connect it to −5V. The device is specified for both conditions.
9	V_{SS}	Negative supply for analog circuitry. This is −15V nominal.
10–19	DB15–DB6	Data I/O pins. DB15 is MSB.
20	DGND	Ground pin for digital circuitry.
21	V_{CC}	Positive supply for digital circuitry. This is +5V nominal.
22	R/$\overline{W}$	R/$\overline{W}$ input. This can be used to load data to the DAC or to read back the DAC latch contents.
23	$\overline{CS}$	Chip select input. This selects the device.
24	$\overline{CLR}$	Clear input. The DAC can be cleared to 000 . . . 000 or 100 . . . 000. See Table II.
25	$\overline{LDAC}$	Asynchronous load input to DAC.
26–28	DB5–DB3	Data I/O pins.

Output Range	V_{REF+}	V_{REF-}	R_{IN}
0V to +5V	+5V	0V	V_{OUT}
0V to +10V	+5V	0V	0V
+5V to −5V	+5V	−5V	V_{OUT}
+5V to −5V	+5V	0V	+5V
+10V to −10V	+5V	−5V	0V

Table I. AD7846 Output Voltage Ranges

ORDERING INFORMATION

Relative Accuracy @ +25°C	Temperature Range and Package Options[1]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-28)	**Ceramic DIP (D-28)**	**Ceramic DIP (D-28)**
±16LSB	AD7846JN	AD7846AD	AD7846SD/883B
±4LSB	AD7846KN	AD7846BD	
			LCCC[2] (E-28A)
±16LSB			AD7846SE/883B

NOTES
[1]See Section 14 for package outline information.
[2]Leadless ceramic chip carrier.

Typical Performance Curves

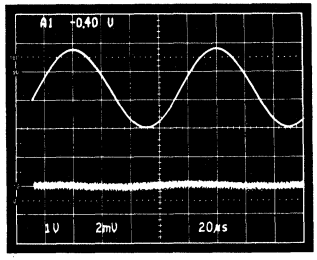


Figure 4. AC Feedthrough. $V_{REF+} = 1V$ rms, 10kHz Sine Wave.

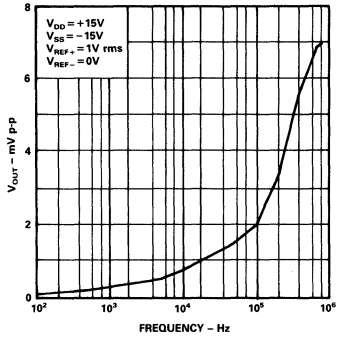


Figure 5. AC Feedthrough vs. Frequency

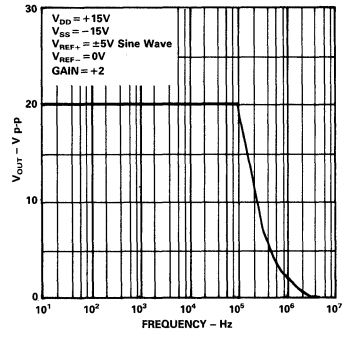


Figure 6. Large Signal Frequency Response

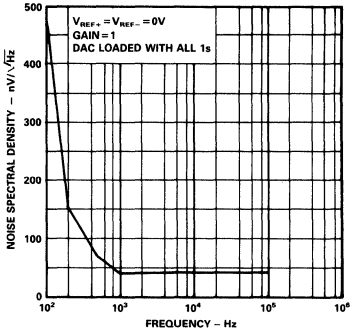


Figure 7. Noise Spectral Density

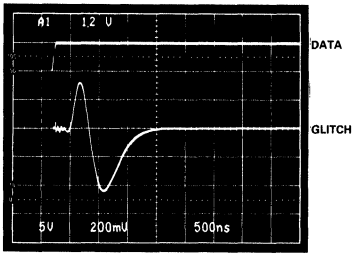


Figure 8. Digital-to-Analog Glitch Impulse without Internal Deglitcher (10 . . . 000 to 011 . . . 111 Transition)

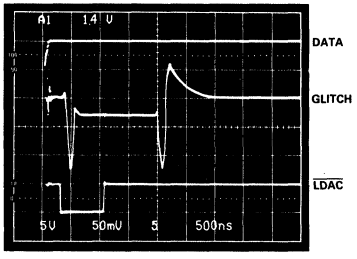


Figure 9. Digital-to-Analog Glitch Impulse with Internal Deglitcher (10 . . . 000 to 011 . . . 111 Transition)

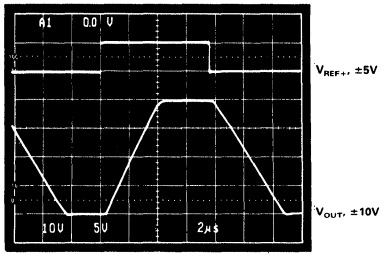


Figure 10. Pulse Response (Large Signal)

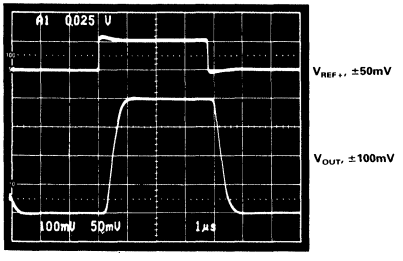


Figure 11. Pulse Response (Small Signal)

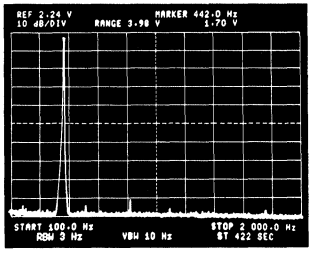


Figure 12. Spectral Response of Digitally Constructed Sine Wave

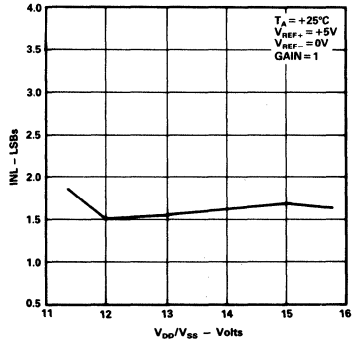


Figure 13. Typical Linearity vs. V_{DD}/V_{SS}

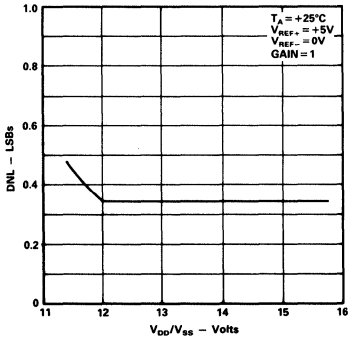


Figure 14. Typical Monotonicity vs. V_{DD}/V_{SS}

CIRCUIT DESCRIPTION

Digital Section

Figure 15 shows the digital control logic and on-chip data latches in the AD7846. Table II is the associated truth table. The D/A converter had two latches which are controlled by four signals: $\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$. The input latch is connected to the data bus (DB15–DB0). A word is written to the input latch by bringing $\overline{CS}$ low and R/$\overline{W}$ low. The contents of the input latch may be read back by bringing $\overline{CS}$ low and R/$\overline{W}$ high. This feature is called "readback" and is used in system diagnostic and calibration routines.

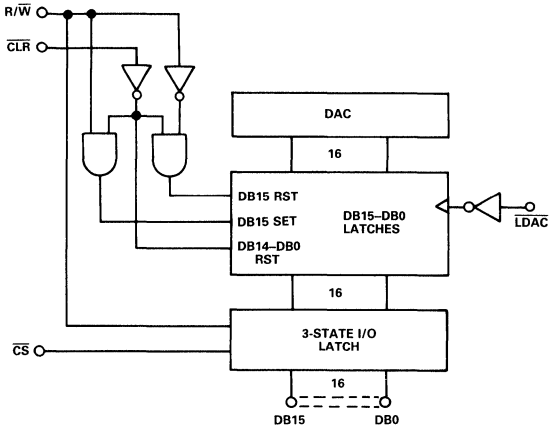


Figure 15. AD7846 Input Control Logic

$\overline{CS}$	R/$\overline{W}$	$\overline{LDAC}$	$\overline{CLR}$	Function
1	X	X	X	3-State DAC I/O Latch in High Z State
0	0	X	X	DAC I/O Latch Loaded with DB15–DB0
0	1	X	X	Contents of DAC I/O Latch Available on DB15–DB0
X	X	0	1	Contents of DAC I/O Latch Transferred to DAC Latch
X	0	X	0	DAC Latch Loaded with 000 . . . 000
X	1	X	0	DAC Latch Loaded with 100 . . . 000

Table II. AD7846 Control Logic Truth Table

Data is transferred from the input latch to the DAC latch with the $\overline{LDAC}$ strobe. The equivalent analog value of the DAC latch contents appears at the DAC output. The $\overline{CLR}$ pin resets the DAC latch contents to 000 . . . 000 or 100 . . . 000, depending on the state of R/$\overline{W}$. Writing a $\overline{CLR}$ loads 000 . . . 000 and reading a $\overline{CLR}$ loads 100 . . . 000. To reset a DAC to 0V in a unipolar system the user should exercise $\overline{CLR}$ while R/$\overline{W}$ is low; to reset to 0V in a bipolar system exercise the $\overline{CLR}$ while R/$\overline{W}$ is high.

D/A Conversion

Figure 16 shows the D/A section of the AD7846. There are three DACs, each of which have their own buffer amplifiers. DAC1 and DAC2 are 4-bit DACs. They share a 16-resistor string but have their own analog multiplexers. The voltage reference is applied to the resistor string. DAC3 is a 12-bit voltage mode DAC with its own output stage.

The 4MSBs of the 16-bit digital code drive DAC1 and DAC2 while the 12LSBs control DAC3. Using DAC1 and DAC2, the MSBs select a pair of adjacent nodes on the resistor string and present that voltage to the positive and negative inputs of DAC3. This DAC interpolates between these two voltages to produce the analog output voltage.

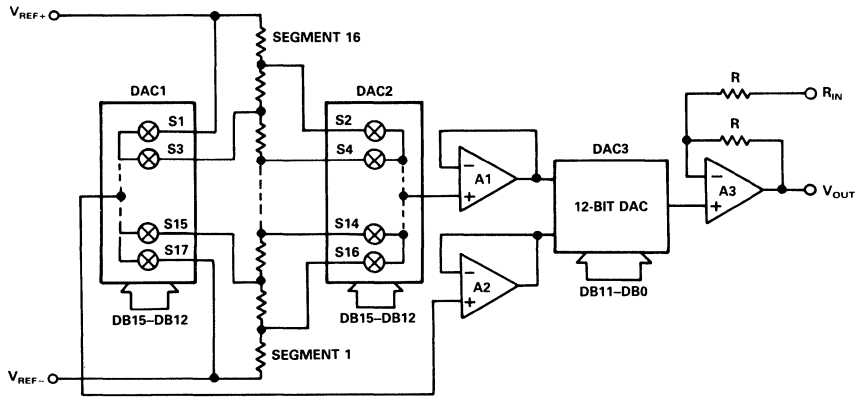


Figure 16. AD7846 D/A Conversion

To prevent non-monotonicity in the DAC due to amplifier offset voltages, DAC1 and DAC2 "leap-frog" along the resistor string. For example, when switching from Segment 1 to Segment 2, DAC1 switches from the bottom of Segment 1 to the top of Segment 2 while DAC2 stays connected to the top of Segment 1. The code driving DAC3 is automatically complemented to compensate for the inversion of its inputs. This means that any linearity effects due to amplifier offset voltages remain unchanged when switching from one segment to the next and 16-bit monotonicity is ensured if DAC3 is monotonic. So, 12-bit resistor matching in DAC3 guarantees overall 16-bit monotonicity. This is much more acheivable than the 16-bit matching which a conventional R-2R structure would have needed.

Output Stage

The output stage of the AD7846 is shown in Figure 17. It is capable of driving a 2kΩ/1000pF load. It also has a resistor feedback network which allows the user to configure it for gains of one or two. Table I shows the different output ranges that are possible.

An additional feature is that the output buffer is configured as a track-and-hold amplifier. Although normally tracking its input, this amplifier is placed in a hold mode for approximately 1μs after the leading edge of $\overline{\text{LDAC}}$. This short state keeps the DAC output at its previous voltage while the AD7846 is internally changing to its new value. So, any glitches that occur in the transition are not seen at the output. In systems where the $\overline{\text{LDAC}}$ is tied permanently low, the deglitching will not be in operation. Figures 8 and 9 show the outputs of the AD7846 with and without the deglitcher.

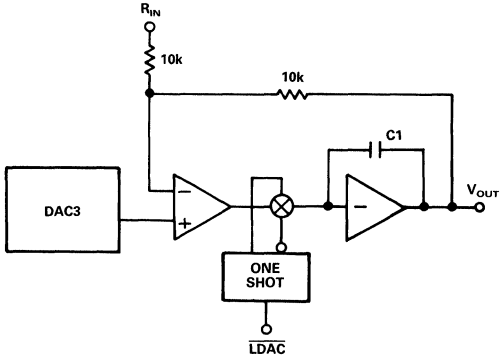


Figure 17. AD7846 Output Stage

UNIPOLAR BINARY OPERATION

Figure 18 shows the AD7846 in the unipolar binary circuit configuration. The DAC is driven by the AD586, +5V reference. Since R_{IN} is tied to 0V, the output amplifier has a gain of 2 and the output range is 0 to +10V. If a 0 to +5V range is required, R_{IN} should be tied to V_{OUT}, configuring the output stage for a gain of 1. Table III gives the code table for the circuit of Figure 18.

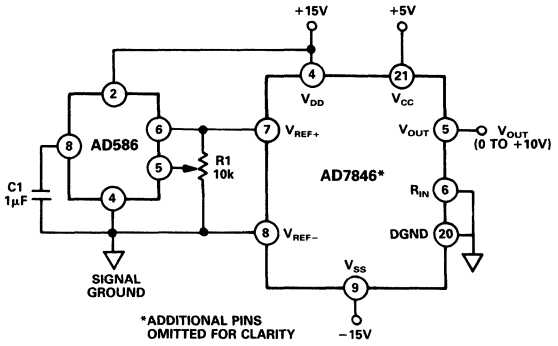


Figure 18. Unipolar Binary Operation

Binary Number in DAC Latch	Analog Output (V_{OUT})
MSB LSB	
1111 1111 1111 1111	+10 (65535/65536) V
1000 0000 0000 0000	+10 (32768/65536) V
0000 0000 0000 0001	+10 (1/65536) V
0000 0000 0000 0000	0V

NOTE
1LSB = $10V/2^{16}$ = 10V/65536 = 152μV.

Table III. Code Table for Figure 18

Offset and gain may be adjusted in Figure 18 as follows : To adjust offset, disconnect the V_{REF-} input from 0V, load the DAC with all 0s and adjust the V_{REF-} voltage until V_{OUT} = 0V. For gain adjustment, the AD7846 should be loaded with all 1s and R1 adjusted until V_{OUT} = 10(65535)/(65536) = 9.999847V. If a simple resistor divider is used to vary the V_{REF-} voltage, it is important that the temperature coefficients of these resistors match that of the DAC input resistance (−300ppm/°C). Otherwise, extra offset errors will be introduced over temperature. Many circuits will not require these offset and gain adjustments. In these circuits, R1, can be omitted. Pin 5 of the AD586 may be left open circuit and Pin 8 (V_{REF-}) of the AD7846 tied to 0V.

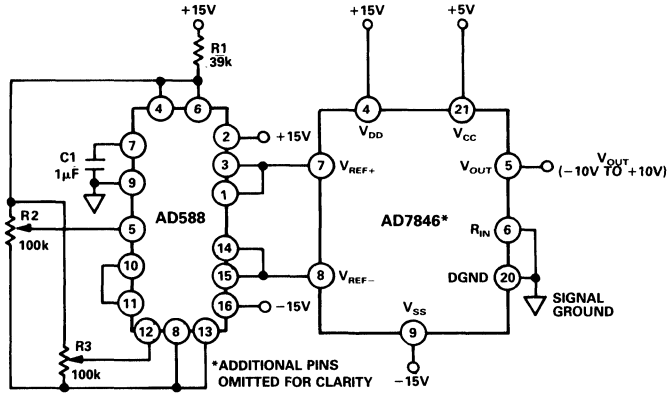


Figure 19. Bipolar ±10V Operation

BIPOLAR OPERATION

Figure 19 shows the AD7846 set up for ±10V bipolar operation. The AD588 provides precision ±5V tracking outputs which are fed to the V_{REF+} and V_{REF-} inputs of the AD7846. The code table for Figure 19 is shown in Table IV.

Binary Number in DAC Latch	Analog Output (V_{OUT})
MSB LSB	
1111 1111 1111 1111	+10 (32767/32768) V
1000 0000 0000 0001	+10 (1/32768) V
1000 0000 0000 0000	0V
0111 1111 1111 1111	−10 (1/32768) V
0000 0000 0000 0000	−10 (32768/32768) V

NOTE
1LSB = $10V/2^{15}$ = 10V/32768 = 305μV.

Table IV. Offset Binary Code Table for Figure 19

Full scale and bipolar zero adjustment are provided by varying the gain and balance on the AD588. R2 varies the gain on the AD588 while R3 adjusts the +5V and −5V outputs together with respect to ground.

For bipolar zero adjustment on the AD7846, load the DAC with 100 . . . 000 and adjust R3 until V_{OUT} = 0V. Full scale is adjusted by loading the DAC with all 1s and adjusting R2 until V_{OUT} = 9.999694V.

When bipolar zero and full scale adjustment are not needed, R2 and R3 can be omitted, Pin 12 on the AD588 should be connected to Pin 11 and Pin 5 should be left floating. If a user wants a ±5V output range, there are two choices. By tying Pin 6 (R_{IN}) of the AD7846 to V_{OUT} (Pin 5), the output stage gain is reduced to unity and the output range is ±5V. If only a positive +5V reference is available, bipolar ±5V operation is still possible. Tie V_{REF-} to 0V and connect R_{IN} to V_{REF+}. This will also give a ±5V output range. However, the linearity, gain, and offset error specifications will be the same as the unipolar 0 to +5V range.

Other Output Voltage Ranges

In some cases, users may require output voltage ranges other than those already mentioned. One example is systems which need the output voltage to be a whole number of millivolts (i.e. 1mV, 2mV, etc.). If the AD689 (8.192V reference) is used with the AD7846 as in Figure 20, then the LSB size is 125μV. This makes it possible to program whole millivolt values at the output. Table V shows the code table for Figure 20.

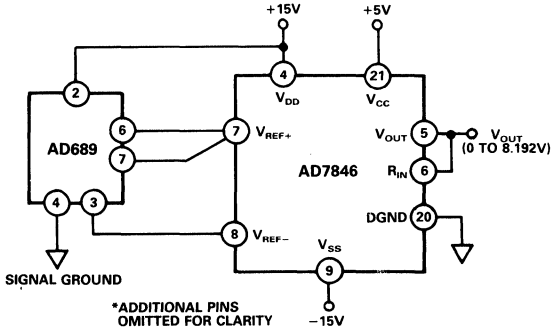


Figure 20. Unipolar Output with AD689

Binary Number in DAC Latch	Analog Output (V_{OUT})
MSB LSB	
1111 1111 1111 1111	8.192V (65535/65536) = 8.1919V
1000 0000 0000 0000	8.192V (32768/65536) = 4.096V
0000 0000 0000 1000	8.192V (8/65536) = 0.001V
0000 0000 0000 0100	8.192V (4/65536) = 0.0005V
0000 0000 0000 0010	8.192V (2/65536) = 0.00025V
0000 0000 0000 0001	8.192V (1/65536) = 0.000125V

NOTE
1LSB = 8.192V/2^{16} = 125μV.

Table V. Code Table for Figure 20

Multiplying Operation

The AD7846 is a full multiplying DAC. To get four-quadrant multiplication, tie V_{REF-} to 0V, apply the ac input to V_{REF+} and tie R_{IN} to V_{REF+}. Figure 6 shows the Large Signal Frequency Response when the DAC is used in this fashion.

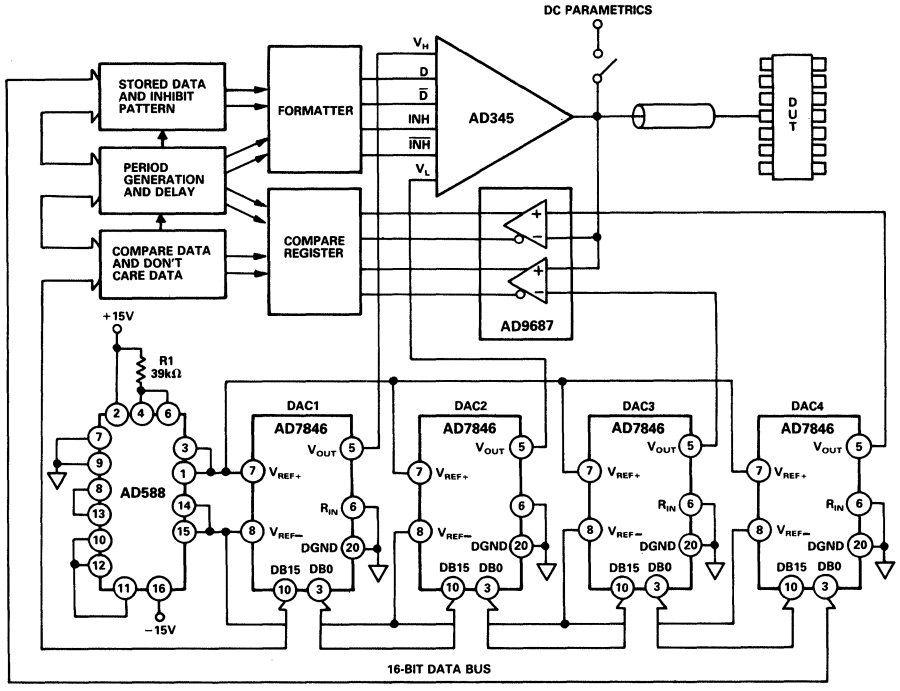


Figure 21. Digital Test System with 16-Bit Performance

TEST APPLICATION

Figure 21 shows the AD7846 in an Automatic Test Equipment application. The readback feature of the AD7846 is very useful in these systems. It allows the designer to eliminate phantom memory used for storing DAC contents and increases system reliability since the phantom memory is now effectively on chip with the DAC. The readback feature is used in the following manner to control a data transfer. First, write the desired 16-bit word to the DAC input latch using the $\overline{CS}$ and R/$\overline{W}$ inputs. Verify that correct data has been received by reading back the latch contents. Now, the data transfer can be completed by bringing the asynchronous $\overline{LDAC}$ control line low. The analog equivalent of the digital word now appears at the DAC output.

In Figure 21, each pin on the Device Under Test can be an input or output. The AD345 is the pin driver for the digital inputs, and the AD9687 is the receiver for the digital outputs. The digital control circuitry determines the signal timing and format.

DACs 1 and 2 set the pin driver voltage levels (V_H and V_L), and DACs 3 and 4 set the receiver voltage levels. The pin drivers used in ATE systems normally have a nonlinearity between input and output. The 16-bit resolution of the AD7846 allows compensation for these input/output nonlinearities. The dc parametrics shown in Figure 21 measure the voltage at the device pin and feed this back to the system processor. The pin voltage can thus be fine-tuned by incrementing or decrementing DACs 1 and 2 under system processor control.

POSITION MEASUREMENT APPLICATION

Figure 22 shows the AD7846 in a position measurement application using an LVDT (Linear Variable Displacement Transducer), an AD630 synchronous demodulator and a comparator to make a 16-bit LVDT-to-Digital Convertor. The LVDT is excited with a fixed frequency and fixed amplitude sine wave (usually 2.5kHz, 2V pk-pk). The outputs of the secondary coil are in anti-phase and their relative amplitudes depend on the position of the core in the LVDT. The AD7846 output interpolates between these two inputs in response to the DAC input code. The AD630 is set up so that it rectifies the DAC output signal. Thus, if the output of the DAC is in phase with the V_{REF+} input, the inverting input to the comparator will be positive, and if it is in phase with V_{REF-}, the output will be negative. By turning on each bit of the DAC in succession starting with the MSB, and deciding to leave it on or turn it off based on the comparator output, a 16-bit measurement of the core position is obtained.

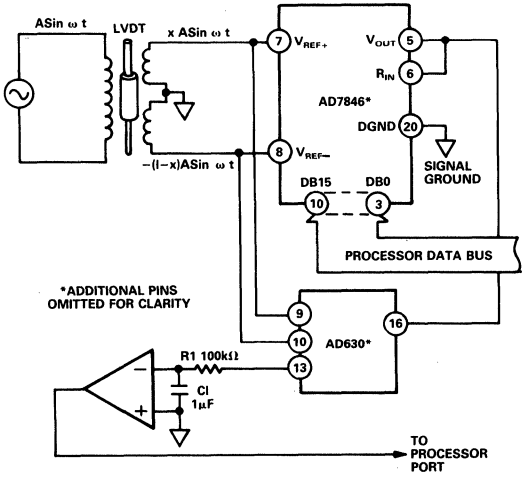


Figure 22. AD7846 in Position Measurement Application

MICROPROCESSOR INTERFACING

AD7846–8086 Interface

Figure 23 shows the 8086 16-bit processor interfacing to the AD7846. The double buffering feature of the DAC is not used in this circuit since $\overline{LDAC}$ is permanently tied to 0V. AD0–AD15 (the 16-bit data bus) are connected to the DAC data bus (DB0–DB15). The 16-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example, the DAC address is D000H.

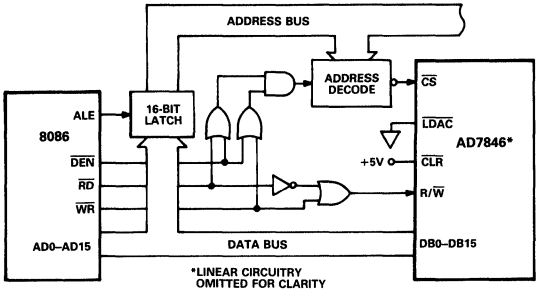


Figure 23. AD7846 to 8086 Interface Circuit

In a multiple DAC system, the double buffering of the AD7846 allows the user to simultaneously update all DACs. In Figure 24, a 16-bit word is loaded to the input latches of each of the DACs in sequence. Then, with one instruction to the appropriate address, $\overline{CS4}$ (i.e., $\overline{LDAC}$) is brought low, updating all the DACs simultaneously.

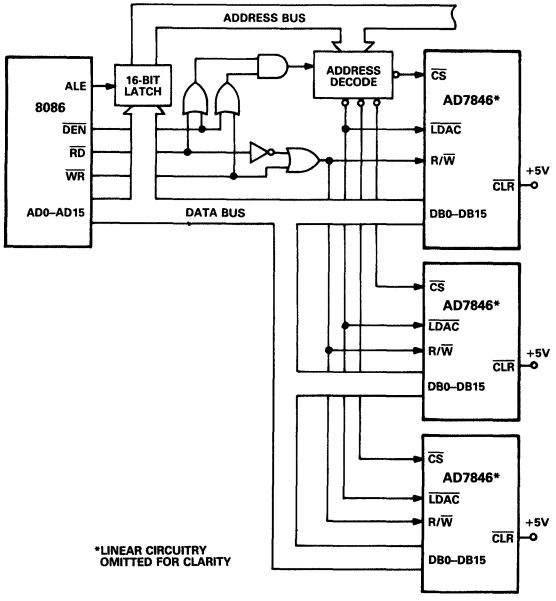


Figure 24. AD7846 to 8086 Interface: Multiple DAC System

AD7846 to MC68000 Interface

Interfacing between the AD7846 and MC68000 is accomplished using the circuit of Figure 25. The following routine writes data to the DAC latches and then outputs the data via the DAC latch.

1000	MOVE.W	#W, D0	The desired DAC data, W, is loaded into Data Register 0. W may be any value between 0 and 65535 (decimal) or 0 and FFFF (hexadecimal).
	MOVE.W	D0, $E000	The data, W, is transferred between D0 and the DAC register.
	MOVE.W	#228, D7	Control is returned to the System Monitor using these two instructions.
	TRAP	#14	

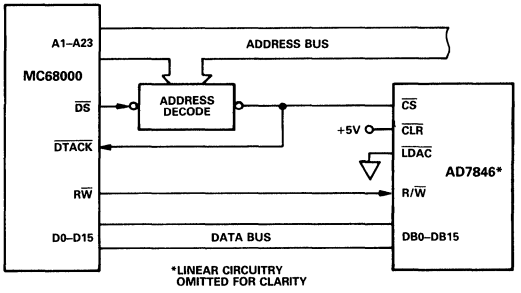


Figure 25. AD7846 to MC68000 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7846 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus

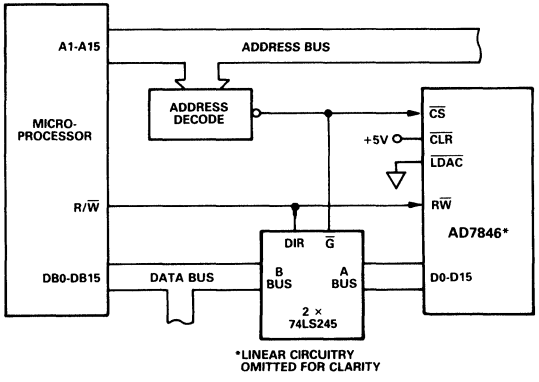


Figure 26. AD7846 Interface Circuit Using Latches to Minimize Digital Feedthrough

noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 26 shows an interface circuit which isolates the DAC from the bus. Note that to make use of the AD7846 readback feature using the isolation technique of Figure 26, the latch needs to be bidirectional.

APPLICATION HINTS

Noise

In high resolution systems, noise is often the limiting factor. With a 10 volt span, a 16-bit LSB is 152μV (−96dB). Thus, the noise floor must stay below −96dB in the frequency range of interest. Figure 7 shows the noise spectral density for the AD7846.

Grounding

As well as noise, the other prime consideration in high resolution DAC systems is grounding. With an LSB size of 152μV and a load current of 5mA, 1LSB of error can be introduced by series resistance of only 0.03Ω.

Figure 27 below shows recommended grounding for the AD7846 in a typical application.

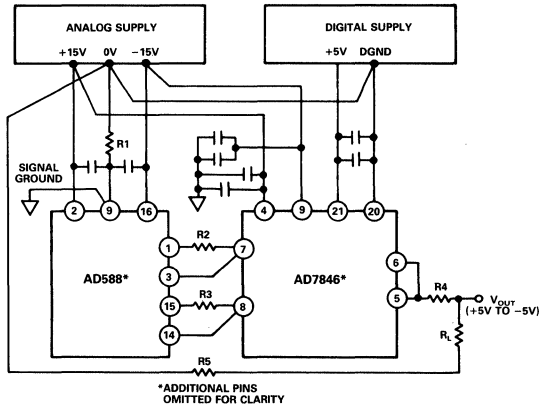


Figure 27. AD7846 Grounding

R1 to R5 represent lead and track resistances on the printed circuit board. R1 is the resistance between the Analog Power Supply ground and the Signal Ground. Since current flowing in R1 is very low (bias current of AD588 sense amplifier), the effect of R1 is negligible. R2 and R3 represent track resistance between the AD588 outputs and the AD7846 reference inputs. Because of the Force and Sense outputs on the AD588, these resistances will also have a negligible effect on accuracy.

R4 is the resistance between the DAC output and the load. If R_L is constant, then R4 will introduce a gain error only which can be trimmed out in the calibration cycle. R5 is the resistance between the load and the analog common. If the output voltage is sensed across the load, R5 will introduce a further gain error which can be trimmed out. If, on the other hand, the output voltage is sensed at the analog supply common, R5 appears as part of the load and therefore introduces no errors.

Printed Circuit Board Layout

Figure 28 shows the AD7846 in a typical application with the AD588 reference, producing an output analog voltage in the ±10 volts range. Full scale and bipolar zero adjustment are provided by potentiometers R2 and R3. Latches (2×74LS245) isolate the DAC digital inputs from the active microprocessor bus and minimize digital feedthrough.

The printed circuit board layout for Figure 28 is shown in Figures 29 and 30. Figure 29 is the component side layout while Figure 30 is the solder side layout. The component overlay is shown in Figure 31.

In the layout, the general grounding guidelines given in Figure 27 are followed. The AD588 and AD7846 are as close as possible, and the decoupling capacitors for these are also kept as close to the device pins as possible.

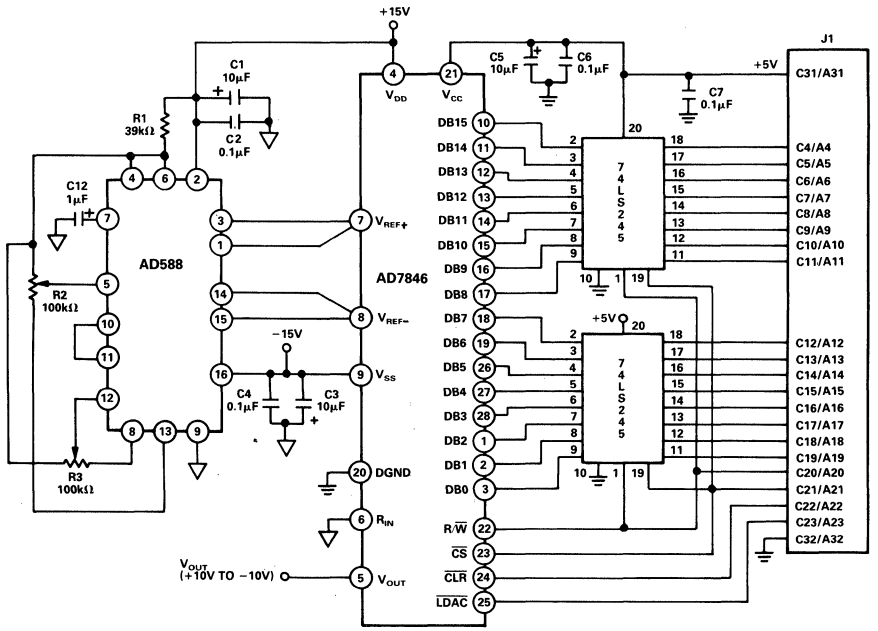


Figure 28. Schematic for AD7846 Board

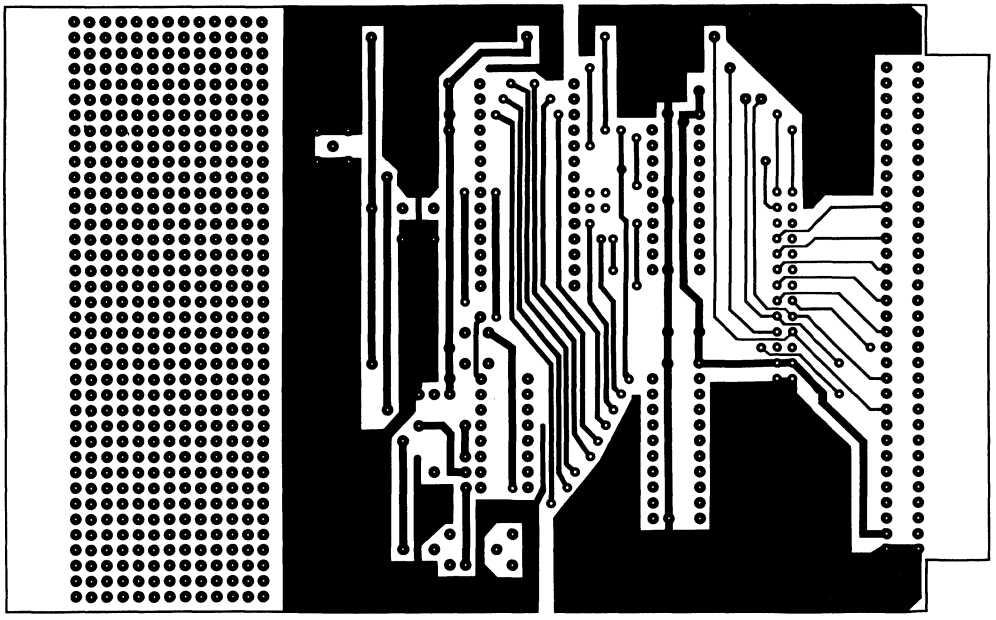


Figure 29. PCB Component Side Layout for Figure 28

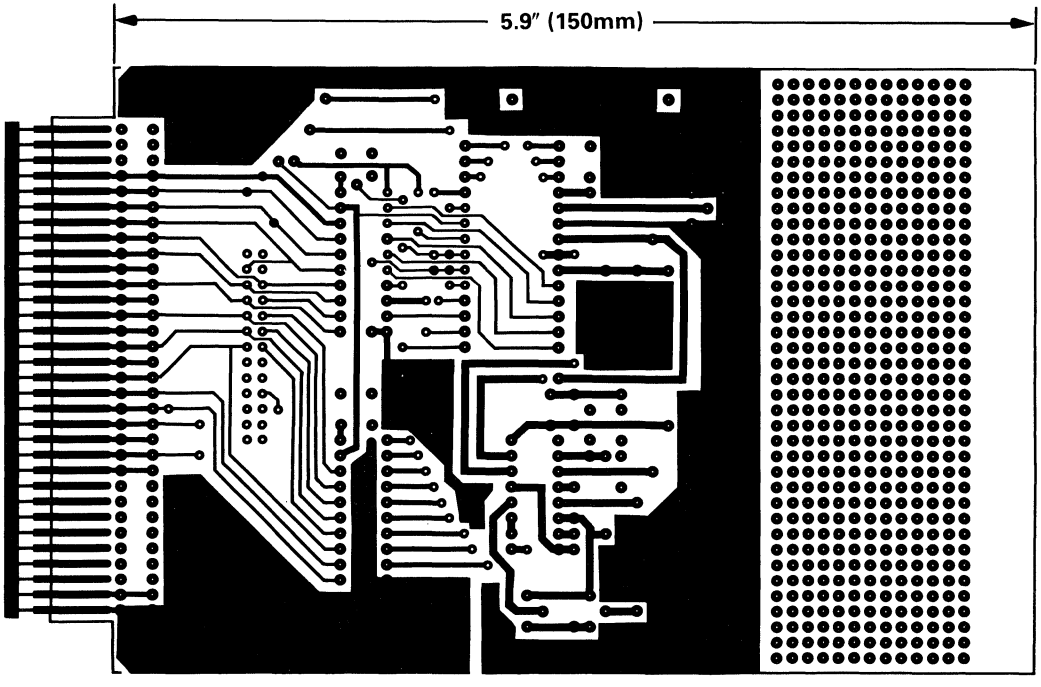


Figure 30. PCB Solder Side Layout for Figure 28

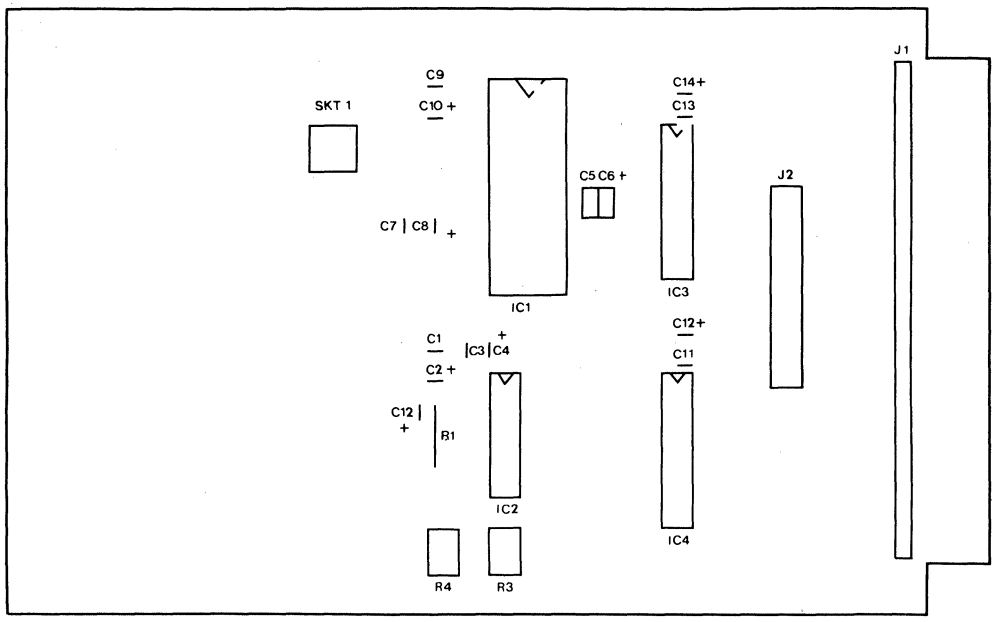


Figure 31. Component Overlay for Circuit of Figure 28

ANALOG DEVICES

LC²MOS Complete 12-BIT DAC with DSP Interface

AD7848

FEATURES

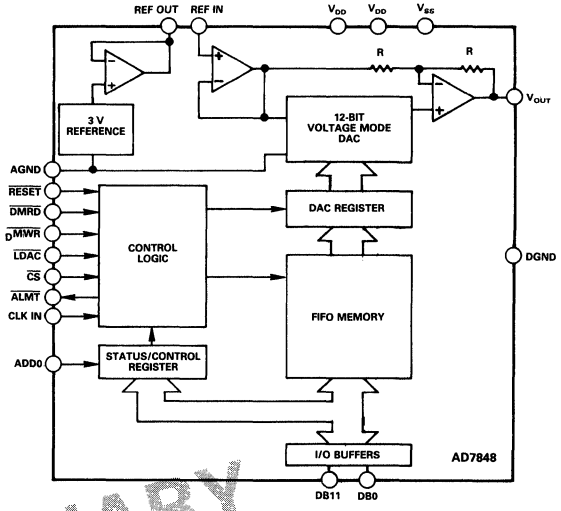
Complete DAC with DSP Interface, Comprising:
- **12-Bit Voltage Mode DAC**
- **3 V Zener Reference**
- **Output Buffer Amplifier with 4 μs Settling Time**
- **8-Word FIFO and Interface Logic**

72 dB Signal-to-Noise Ratio
Interfaces to High Speed DSP Processors, e.g., ADSP-2100, TMS32010, TMS32020
42 ns min $\overline{WR}$ Pulse Width
Low Power – 95 mW max

APPLICATIONS

Digital Signal Processing
Speech Synthesis
High Speed Modems
DSP Servo Control When Used with AD7878

AD7848 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7848 is a fast, complete, 12-bit, voltage output D/A converter with a versatile DSP interface consisting of an 8-word, first-in, first-out (FIFO) memory and associated control logic.

The FIFO memory allows up to eight samples to be loaded to the AD7848 at full microprocessor speed. The samples are then loaded to the DAC register under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 21 ns allows direct interfacing to DSP processors and high speed 16-bit microprocessors.

An on-chip status/control register allows the user to program the effective length of the FIFO and contains FIFO empty, FIFO full and FIFO word count information.

The analog output from the AD7848 provides a bipolar output range of ±3 V. Full power output signals up to 20 kHz can be created, and the AD7848 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion.

The AD7848 is fabricated in Linear Compatible CMOS (LC^2MOS), an advanced, mixed technology, process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-pin plastic and hermetic dual-in-line package (DIP) and in a 28-terminal plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete D/A Function with DSP Interface
   The AD7848 provides the complete function for creating ac signals to 12-bit accuracy. The part features an on-chip reference, an output buffer amplifier and 12-bit D/A converter. The additional feature of an 8-word FIFO reduces the high software overheads associated with servicing peripherals in DSP processors.
2. Dynamic Specifications for DSP Users
   The AD7848 is fully specified and tested for ac parameters, including signal-to-noise ratio and harmonic distortion. Key digital timing parameters are also tested and specified over the full operating temperature range.
3. Fast Microprocessor Interface
   Data setup times of 21 ns and write pulse widths of 42 ns make the AD7848 compatible with all modern 16-bit microprocessors and digital signal processors.

SPECIFICATIONS (V_{DD} = 5 V± 5%, V_{SS} = −5 V ±5%, AGND = DGND = 0V, REF IN = +3 V, R_L = 2 kΩ, C_L = 100 pF, f_{CLK} = 8 MHz. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A Versions[1]	K, L, B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR) @ +25°C	70	72	70	dB min	V_{OUT} =1 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	71	70	dB min	Typically 71.5 dB at +25°C for 0 <V_{OUT}< 20 kHz[4]
Total Harmonic Distortion (THD)	−80	−80	−80	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz
					Typically −84 dB at +25°C for 0 <V_{OUT}<20 kHz[4]
Peak Harmonic or Spurious Noise	−81	−81	−81	dB max	V_{OUT} = 1 kHz, f_{SAMPLE} = 100 kHz
					Typically −84 dB at +25°C for 0 <V_{OUT}<20 kHz[4]
DC ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB typ	
Differential Nonlinearity	±1/2	±1/2	±1/2	LSB typ	Guaranteed Monotonic
Bipolar Zero Error	±5	±5	±5	LSB max	
Positive Full Scale Error[5]	±5	±5	±5	LSB max	
Negative Full Scale Error[5]	±5	±5	±5	LSB max	
REFERENCE OUTPUT[6]					
REF OUT	3	3	3	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
T_{min} to T_{max}	±15	±15	±15	mV max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT					
Input Voltage	2.85	2.85	2.85	V min	
	3.15	3.15	3.15	V max	
Input Current	50	50	50	μA max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V±5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	2.7	2.7	2.7	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating State Leakage Current	10	10	10	μA max	
Floating State Output Capacitance[7]	15	15	15	pF max	
ANALOG OUTPUT					
Output Voltage Range	±3	±3	±3	V nom	
DC Output Impedance	0.1	0.1	0.1	Ω typ	
Short Circuit Current	20	20	20	mA typ	
AC CHARACTERISTICS[7]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	4	μs max	
Negative Full-Scale Change	4	4	4	μs max	
Digital to Analog Glitch Impulse	10	10	10	nV secs typ	
Digital Feedthrough	2	2	2	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
I_{SS}	6	6	6	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5 V
Power Dissipation	95	95	95	mW max	Typically 60 mW

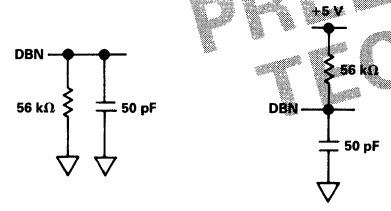
NOTES
[1]Temperature Ranges are as follows: J, K, L Versions, 0 to +70°C; A, B Versions, −25°C to +85°C; S Version; −55°C to +125°C.
[2]V_{OUT} (pk-pk) = ±3 V.
[3]SNR includes distortion and noise components.
[4]Using external sample-and-hold (see Testing the AD7848).
[5]Measured with respect to REF IN and includes bipolar offset error.
[6]For Capacitive Loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).
[7]Sample Tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5 V±5%, V_{SS} = −5 V±5%, AGND=DGND=0 V)

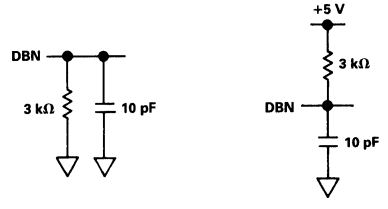
Parameter	Limit at T_{min}, T_{max} (L Version)	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (S Version)	Units	Conditions/Comments
t_1	**42**	**42**	**55**	**ns min**	INTERNAL WRITE Pulse Width
t_2	5	5	5	ns min	ADD0 to INTERNAL WRITE Setup Time
t_3	0	0	0	ns min	ADD0 to INTERNAL WRITE Hold Time
t_4	**21**	**21**	**30**	ns min	Data Valid to INTERNAL WRITE Setup Time
t_5	10	10	10	ns min	Data Valid to INTERNAL WRITE Hold Time
t_6	1.5 CLK IN Cycles	1.5 CLK IN Cycles	1.5 CLK IN Cycles	min	$\overline{LDAC}$ Pulse Width
t_7	0	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$ Setup Time
t_8	0	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$ Hold Time
t_9	**45**	**60**	**60**	ns min	$\overline{DMRD}$ Pulse Width
t_{10}[2]	**41**	**57**	**57**	ns max	Data Access Time after $\overline{DMRD}$
t_{11}[3]	5	5	5	ns min	Bus Relinquish Time
	45	**45**	**45**	ns max	

NOTES
[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr= tf= 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]t_{10} is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[3]t_{11} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise stated)

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{OUT} to AGND . . . . . V_{SS} −0.3 V to V_{DD} +0.3 V
REF IN to AGND . . . . . −0.3 V to V_{DD}+0.3V
REF OUT to AGND . . . . . −0.3 V to V_{DD}+0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_{DD}+0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD}+0.3 V
Operating Temperature Range
Commercial (J, K, L Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 1000 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

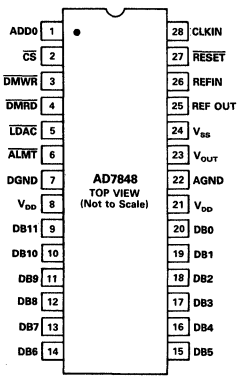
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

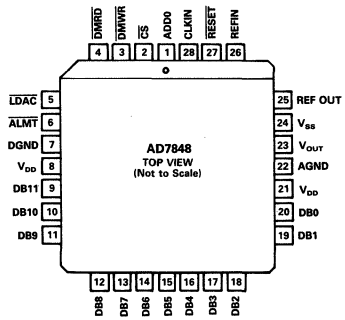
Pin No.	Pin Mnemonic	Function
1	ADD0	Address Input. This input determines whether the word on the data bus during a write operation is loaded to the FIFO RAM or to the status/control register. A logic low selects the FIFO memory, while a logic high selects the status/control register (see Status/Control Register section).
2	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
3	$\overline{DMWR}$	Data Memory Write. Active low logic input. $\overline{DMWR}$ is used in conjunction with $\overline{CS}$ to write data to either the FIFO memory or the status/control register. Corresponds directly to $\overline{DMWR}$ (ADSP-2100), R/$\overline{W}$ (MC68000, TMS32020), $\overline{WE}$ (TMS32010).
4	$\overline{DMRD}$	Data Memory Read. Active low logic input. $\overline{DMRD}$ is used in conjunction with $\overline{CS}$ low to access data from the status/control register. Corresponds directly to $\overline{DMRD}$ (ADSP-2100), $\overline{DEN}$ (TMS32010).
5	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded to the DAC register from FIFO memory Location 0 on the falling edge of this signal. The $\overline{LDAC}$ input is asynchronous to CLK IN and is independent of $\overline{CS}$, $\overline{DMWR}$ and $\overline{DMRD}$.
6	$\overline{ALMT}$	FIFO Almost Empty. A logic low indicates that the word count (i.e., number of data words in the FIFO) has reached the programmed almost empty word count in the status/control register. $\overline{ALMT}$ is updated after every $\overline{LDAC}$ operation. The $\overline{ALMT}$ output can be disabled (i.e., set to a logic high) by writing a logic 1 to DB7 ($\overline{ENAL}$) of the status/control register.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	V_{DD}	Positive Supply Voltage, +5 V ± 5%.
9–20	DB11–DB0	Data Bit 11 (MSB) to DB0 (LSB). Three-state TTL input/outputs. Coding for data words is assumed to be 2s complement.
21	V_{DD}	Positive Supply Voltage, +5 V ±5%. Same as Pin 8.
22	AGND	Analog Ground. Ground reference for DAC, reference and output buffer amplifier.
23	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Bipolar output range (±3 V with REF IN = +3 V).
24	V_{SS}	Negative Supply Voltage, −5 V± 5%.
25	REF OUT	Voltage Reference Output. The internal 3 V analog reference is provided at this pin. To operate the AD7848 with internal reference, REF OUT should be connected to REF IN. The external load capability of the reference is 500 μA.
26	REF IN	Voltage Reference Input. The reference voltage for the DAC is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7848 is 3 V.
27	RESET	Reset. Active low logic input. A logic low clears the words in the FIFO memory and the contents of the DAC register to 1000 0000 0000 and resets the status/control register and control logic.
28	CLK IN	Clock Input. TTL-compatible logic input. Used as the clock source for all internal dynamic logic and provides synchronization during bus transactions. The mark/space ratio of this clock can vary from 35/65 to 65/35.

PIN CONFIGURATIONS

DIP



PLCC



STATUS/CONTROL REGISTER

The status/control register serves the dual function of providing control and monitoring the status of the FIFO memory. This register is directly accessible through the data bus (DB11–DB0) with a read or a write operation when ADD0 is high. A write operation to the status/control register provides control for the $\overline{ALMT}$ output, DAC register updates and FIFO word count reset. This is normally done on power-up initialization. The FIFO memory address pointer is decremented after every DAC register update and this pointer is compared with a preprogrammed count in the status/control register. When this preprogrammed count is reached, the $\overline{ALMT}$ output is asserted if the $\overline{ENAL}$ control bit is set to zero. This $\overline{ALMT}$ can be used to interrupt the microprocessor after any predetermined number of DAC register updates (between 1 and 8). The status of the address pointer, along with FIFO underflow, FIFO empty and $\overline{ALMT}$ status can be accessed at any time by reading the status/control register. Note, reading from the status/control register does not cause any internal movement in the FIFO memory.

STATUS/CONTROL REGISTER FUNCTION DESCRIPTION

DB11 ($\overline{ALMT}$)
Almost Empty Flag. Read only. This is the same as the Pin 6 ($\overline{ALMT}$ output) status. A logic low indicates that the word count in the FIFO memory has reached the preprogrammed word count in bit locations DB10–DB8. $\overline{ALMT}$ is updated at the end of an $\overline{LDAC}$ operation. $\overline{ALMT}$ is active following a device reset because both the FIFO word count and the almost empty word count are 000.

DB10–DB8 (AEC2–AEC0)
Almost Empty Word Count. Read/Write. The count value determines the number of words in the FIFO memory which will cause $\overline{ALMT}$ to be set. When the FIFO word count equals the programmed count in these three bits then both the $\overline{ALMT}$ output and DB11 of the status/control register are set to a logic low. For example, when a code of 011 is written to these bits, $\overline{ALMT}$ is set when Location 0 through Location 3 of the FIFO memory contain valid data. AEC2 is the most significant bit of the word count. The count value can be read back if required.

DB7 ($\overline{ENAL}$)
Enable Almost Empty. Read/Write. Writing a 1 to this bit disables the $\overline{ALMT}$ output and status/control register bit DB11.

DB6 ($\overline{FFUL}$/RESET)
FIFO Full/Reset. Read/Write. Reading a 0 from this bit indicates that there are 8 words in the FIFO memory (i.e., the FIFO is full). Writing a 1 to this bit location will cause a system reset as per the $\overline{RESET}$ input (Pin 27).

DB5 ($\overline{LDAC}$)
Load DAC. Write only. Writing a 0 to this location causes the sample in Location 0 of the FIFO to be loaded into the DAC register. The function of this bit is the same as the $\overline{LDAC}$ input (Pin 5).

DB4 (FEMP)
FIFO Empty. Read only. Reading a 1 indicates that there are no words in FIFO memory. When the FIFO is empty, any further $\overline{LDAC}$ operations will continue to update the DAC register with the contents of Location 0 of the FIFO.

DB3 (FUND)
FIFO Underflow. Read only. If the FIFO memory is empty and further DAC register updates occur, then this bit is set to a 1. It will remain set until an $\overline{LDAC}$ operation occurs with valid data in FIFO Location 0.

DB2–DB0 (FCN2–FCN0)
FIFO Word Count. Read only. The value read from these bits indicates the number of words in FIFO memory. For example, reading 011 from these bits indicates that Location 0 through Location 3 contain valid data. Note, reading all 0s indicates that there is either one word or no word in the FIFO memory; in this case, the FIFO Empty bit determines if there is no word in memory. FCN2 is the most significant bit of the word count.

BIT LOCATION	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
STATUS INFORMATION (READ)	$\overline{ALMT}$	AEC2	AEC1	AEC0	$\overline{ENAL}$	$\overline{FFUL}$	–	FEMP	FUND	FCN2	FCN1	FCN0
CONTROL FUNCTION (WRITE)	X	AEC2	AEC1	AEC0	$\overline{ENAL}$	RESET	$\overline{LDAC}$	X	X	X	X	X
RESET STATUS	0	0	0	0	0	1	–	0	0	0	0	0

X =DON'T CARE

Table I. Status/Control Bit Function Description

ORDERING INFORMATION[1]

Signal-to-Noise Ratio	Data Access Time	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-28)	**Hermetic DIP (Q-28)[3]**	**Hermetic DIP (Q-28)[3]**
70 dB	57 ns	AD7848JN	AD7848AQ	AD7848SQ[4]
72 dB	57 ns	AD7848KN	AD7848BQ	
72 dB	41 ns	AD7848LN		
		PLCC[5]		
70 dB	57 ns	AD7848JP		
72 dB	57 ns	AD7848KP		
72 dB	41 ns	AD7848LP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact our local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Analog Devices reserves the right to ship either ceramic (D-28) packages or cerdip (Q-28) hermetic packages.
[4]Available to /883B processing only.
[5]PLCC: Plastic Leaded Chip Carrier.

INTERNAL FIFO MEMORY

The internal FIFO memory of the AD7848 consists of eight memory locations, each memory location 12 bits wide. A block diagram of the AD7848 FIFO architecture is shown in Figure 3.

Data is loaded to the FIFO under control of $\overline{CS}$ and $\overline{DMWR}$. The FIFO Address Pointer always points to the top of memory, i.e., the uppermost location which contains valid data. This pointer is incremented when a new word is loaded to the FIFO from the data bus. Data is loaded from the FIFO to the DAC register under control of an asynchronous $\overline{LDAC}$ signal. When $\overline{LDAC}$ is asserted, the data contained in the bottom location of the FIFO (Location 0) is transferred to the DAC register. On completion of this transfer operation, each word in the FIFO moves down one location and the Address Pointer is decremented by one. Therefore, each data word enters at the top of memory, propagates down with successive $\overline{LDAC}$ operations until it reaches Location 0 from where it can be transferred to the DAC register.

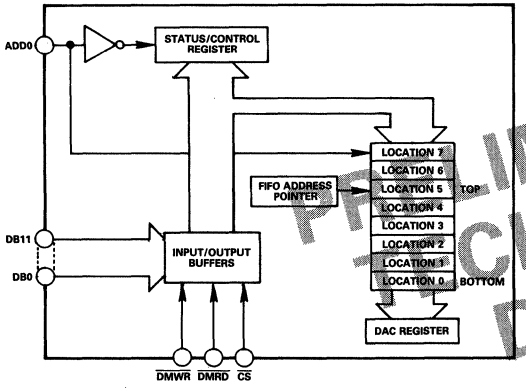


Figure 3. Internal FIFO Architecuture

The propagation of data words down the FIFO occurs in synchronization with the AD7848 input clock (CLK IN). As a result, a write operation to the FIFO memory must also be synchronous with CLK IN to avoid input/output conflicts in the FIFO (i.e., writing to the FIFO while the FIFO data words are rippling down after a DAC register update). This requires that the microprocessor clock and the AD7848 CLK IN are derived from the same source.

D/A SECTION

The AD7848 contains a 12-bit, voltage output D/A converter consisting of highly stable thin film resistors and high speed NMOS single pole, double throw switches. The simplified circuit diagram for the DAC section is shown in Figure 4. The three MSBs of the data word are decoded to drive the seven switches A–G. The 9 LSBs switch a 9-bit R-2R ladder structure. The output voltage from this converter has the same polarity as the reference voltage, REF IN.

The REF IN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter and the bipolar bias circuitry. The D/A converter is configured and scaled for a 3 V reference and the device is tested with 3 V applied to REF IN. Operating the AD7848 at reference voltages outside the ±5% tolerance range may result in degraded performance from the part.

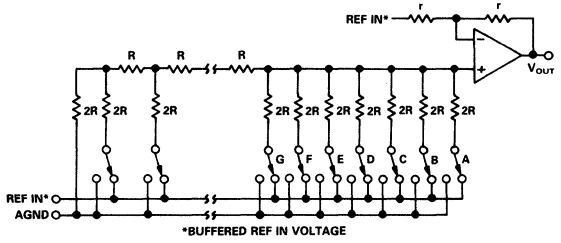


Figure 4. DAC Ladder Structure

INTERNAL REFERENCE

The AD7848 has an on-chip temperature compensated buried Zener reference (see Figure 5) which is factory trimmed to 3 V ± 10 mV. The reference voltage is provided at the REF OUT pin. This reference can be used to provide both the reference voltage for the D/A converter and the bipolar bias circuitry. This is achieved by connecting the REF OUT pin to the REF IN pin of the device.

The reference voltage can also be used as a reference for other components in the system and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for external use, it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor.

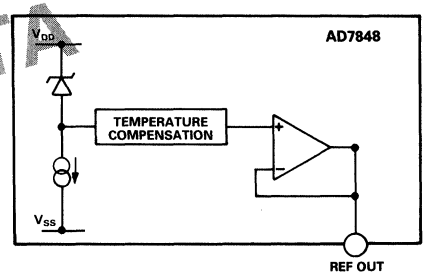


Figure 5. Internal Reference

EXTERNAL REFERENCE

In some applications, the user may require a system reference or some other external reference to drive the AD7848 reference input. Figure 6 shows how the AD586 5 V reference can be conditioned to provide the 3 V reference required by the AD7848 REF IN. An alternate source of reference voltage for the AD7848 in systems which use both a DAC and an ADC is to use the REF OUT voltage of an ADC such as the AD7878 or AD7870.

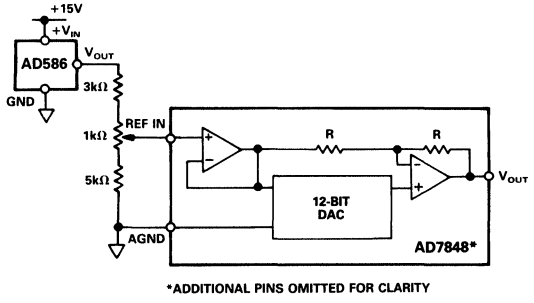


Figure 6. AD586 Driving AD7848 REF IN

OP AMP SECTION

The output from the converter is buffered by a noninverting amplifier. Internal scaling resistors on the AD7848 configure the output voltage for ±3 V from an input reference voltage of +3 V. Figure 4 shows the arrangement of these resistors around the output op amp. The buffer amplifier is capable of developing ± 3 V across a 2 kΩ and 100 pF load to ground and can produce 6 V peak-to-peak sine wave signals up to a frequency of 20 kHz.

The output is updated on the falling edge of the $\overline{LDAC}$ input. For a software DAC update, the output is updated on the next rising clock edge after receiving a software $\overline{LDAC}$. The amplifier settles to within 1/2 LSB of its final value in typically less than 2 μs.

TRANSFER FUNCTION

The basic circuit configuration for the AD7848 is shown in Figure 7. Table II shows the ideal input code to output voltage relationship for this configuration. Input coding to the DAC is 2s complement with 1 LSB=FS/4096=6 V/4096= 1.465 mV. The output voltage, V_{OUT}, can be expressed in terms of the input code, N, using the following relationship:

$$V_{OUT} = \frac{2 \cdot N \cdot REFIN}{4096} \quad -2048 \leq N \leq +2047$$

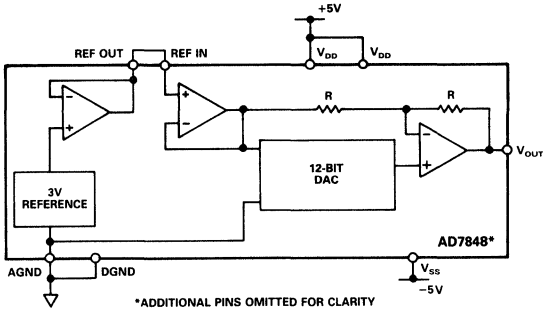


Figure 7. Basic Connection Diagram

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}*
0111 1111 1111	+2.998535 V
0111 1111 1110	+2.99707 V
0000 0000 0001	+0.001465 V
0000 0000 0000	0 V
1111 1111 1111	−0.001465 V
1000 0000 0001	−2.998535 V
1000 0000 0000	−3 V

*Assuming REF IN = +3 V.

Table II. Ideal Input/Output Code Table

READ/WRITE OPERATIONS

The AD7848 read/write operations consist of writing to the FIFO memory and status/control register and reading from the status/control register. These operations are controlled by the $\overline{CS}$, $\overline{DMWR}$, $\overline{DMRD}$ and ADD0 logic inputs.

Write Operation

A write operation to the AD7848 FIFO memory consists of bringing $\overline{CS}$ and $\overline{DMWR}$ low with ADD0 low. Internally, these signals are gated with CLK IN to provide an INTERNAL WRITE signal (see Figure 8). The pulse width of this INTERNAL WRITE signal is effectively the overlap between the CLK IN low time and the $\overline{CS}$ and $\overline{DMWR}$ pulses. This may result in shorter write pulse widths, setup times and data hold times than those given by a microprocessor. The timing on the AD7848 timing diagram of Figure 9 is therefore given with respect to the INTERNAL WRITE signal rather than the $\overline{DMWR}$ signal. A similar situation exists for writing information to the AD7848 status/control register. A write operation to the status/control register consists of bringing $\overline{CS}$ and $\overline{DMWR}$ low with ADD0 high.

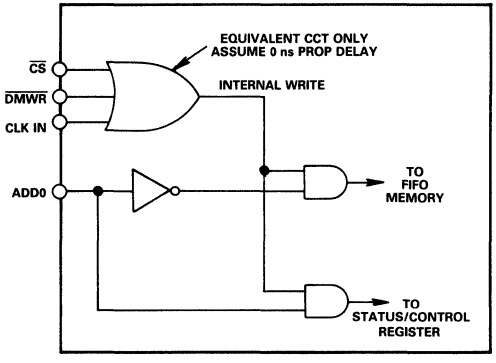


Figure 8. $\overline{DMWR}$ Internal Logic

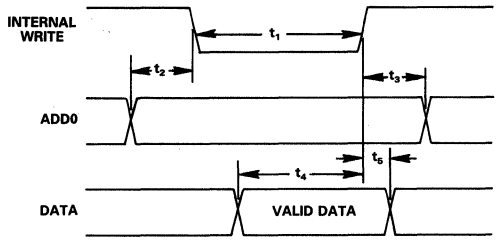


Figure 9. AD7848 Write Operation

Read Operation

Figure 10 shows the timing diagram for a read operation from the status/control register of the AD7848. $\overline{CS}$ and $\overline{DMRD}$ going low accesses data from the status/control register. Status information for a particular word should be read before the word is transferred to the DAC register.

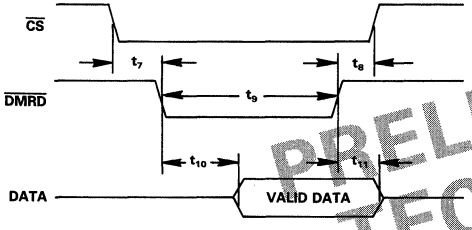


Figure 10. AD7848 Read Operation

UPDATING THE DAC OUTPUT

The DAC output on the AD7848 can be updated under software or hardware control. For hardware control, the output is updated by asserting the $\overline{LDAC}$ input; for software control, writing a 0 to DB5 of the status/control register updates the output.

The $\overline{LDAC}$ input is an asynchronous input which is independent of either the DAC or DSP clocks. This is essential for applications where precise sampling in time is important. In these applications, the signal update must occur at exactly equal intervals to minimize errors due to updating uncertainty or jitter. In these cases, the $\overline{LDAC}$ input is driven from a timer or some precise clock source.

In applications where precise sampling is not critical, the $\overline{LDAC}$ pulse can be generated from a microprocessor $\overline{WR}$ line gated with a decoded address (different to the AD7848 $\overline{CS}$ address). Note, the $\overline{LDAC}$ input must stay low for at least 1.5 CLK IN cycles.

The alternative method for updating the DAC output is a software update which is achieved by writing a 0 to DB5 of the status/control register. In this case, the DAC register is updated on the next rising clock edge of CLK IN. Continuous DAC register updates do not take place when there is a 0 in DB5. The update only occurs on the next falling CLK IN edge after the 0 is written to DB5. The $\overline{LDAC}$ input (Pin 5) should be tied high for software control of the DAC update.

Testing the AD7848

The method used to test the dynamic performance specifications is outlined in Figure 11. Data is loaded to the AD7848 under control of the microcontroller and associated logic. The output of the AD7848 is applied to a 9th order low pass filter. The output of the filter is in turn applied to a 14-bit accurate digitizer. This samples the signal and the microcontroller generates an FFT plot from which the dynamic performance of the AD7848 can be evaluated.

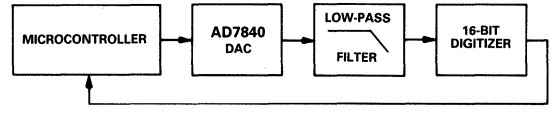


Figure 11. AD7848 Dynamic Performance Test Circuit

The digitizer's sampling is synchronized with the AD7848 update rate to ease FFT calculations. The digitizer samples the AD7848 after the output has settled to its new value. Therefore, if the digitizer was to sample the output directly, it would effectively be sampling a dc value each time. As a result, the dynamic performance of the AD7848 would not be measured correctly. Using the digitizer directly on the AD7848 output would give better results than the actual performance of the AD7848. Using a filter between the DAC and the digitizer means that the digitizer samples a continuously moving signal and the true dynamic performance of the AD7848 is measured.

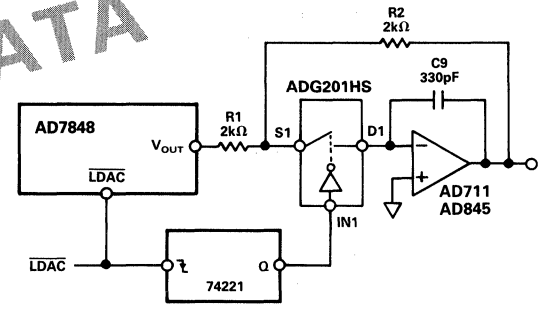


Figure 12. Sample-and-Hold Circuit

Some applications will require improved performance versus frequency from the AD7848. In these applications, a simple sample-and-hold circuit such as that outlined in Figure 12 will extend the very good performance of the AD7848 to 20 kHz. Other applications will already have an inherent sample-and-hold function following the AD7848. An example of this type of application is driving a switched-capacitor filter where the updating of the DAC is synchronized with the switched-capacitor filter. This inherent sample-and-hold function also extends the frequency range performancce of the AD7848.

ANALOG DEVICES

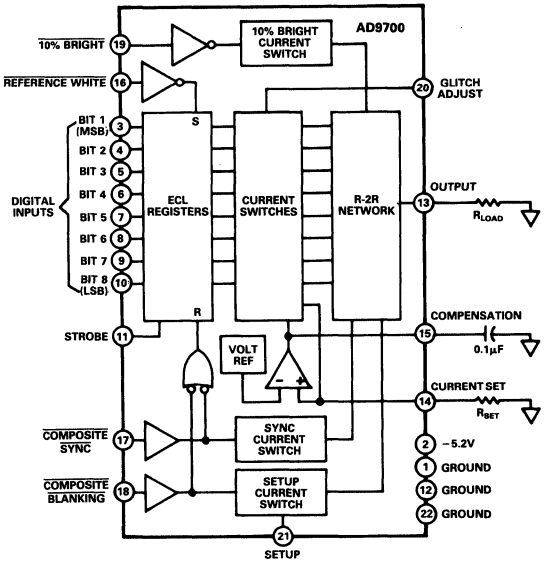
Monolithic Video D/A Converter

AD9700

FEATURES
Update Rates to 125MHz
Low Glitch Energy
Complete Composite Inputs
On-Chip Reference Voltage
Single −5.2V Power Supply

APPLICATIONS
Raster Scan Displays
Color Graphics
Automated Test Equipment
TV Video Reconstruction

AD9700 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9700 digital-to-analog converter is a monolithic device capable of accepting eight bits of digital data at update rates as high as 125MHz. On-chip registers on the data lines help minimize "glitches" in the output signal.

Incorporating the AD9700 into system designs is eased by its blanking, sync, 10% brightness, and reference white control signals. An on-board reference eliminates the need for external circuits, making it considerably easier to design the AD9700 into high-speed applications than it is for converters which do not have this feature.

The unit is housed in a 22-pin package; operates from a single −5.2V power supply; and dissipates only 650mW, making this the smallest, lowest power D/A converter available to design engineers who need true "graphics ready" converters for raster scan, color graphics, and other high-speed systems.

This device is a natural extension of the Analog Devices advanced technology that produced the first hybrid converters which included composite capabilities. Like the earlier HDG-Series D/A converters, the AD9700 is designed to have general output compatibility with EIA Standards RS-170 and RS-343.

Five versions of the AD9700 are available. The AD9700BW (non-hermetic) and AD9700BD (hermetic) are DIP units operating over a temperature range of −25°C to +85°C; the hermetic DIP AD9700SD is for use over a temperature range of −55°C to +125°C. The AD9700BE and AD9700SE are leadless chip carrier (LCC) devices for temperature ranges of −25°C to +85°C and −55°C to +125°C, respectively.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	AD9700BD/BW[1]	AD9700SD[2]
RESOLUTION	Bits	8	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Voltage (adjustable)	mV	2.5	*
Current (adjustable)	μA	67	*
ACCURACY (GS = Gray Scale; FS = Full Scale)			
Linearity	±%GS	0.2	*
Differential Linearity	±%GS, max	0.2	*
Integral Linearity	±%GS, max	0.2	*
Zero Offset (Initial) Voltage	mV (max)	0.3 (0.9)	*
Monotonicity		Guaranteed	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C (max)	15	*(30)
Gain	ppm/°C (max)	50	*(125)
Zero Offset	ppm/°C (max)	10	*(15)
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[3]			
Settling Time to 0.4% GS; 0V to 637.5mV GS change			
Voltage	ns (max)	10 (12)	*
Update Rate[4]	MHz (min)	125 (100)	*
Slew Rate	V/μs	300	*
Rise Time	ns	2	*
Glitch Impulse[5]	pV-s	80	*
DIGITAL DATA INPUTS			
Logic Compatibility		ECL[6]	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1./−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading (each bit)		5pF and 50kΩ to −5.2V	*
STROBE INPUT			
Logic Compatibility		ECL[6]	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		5pF and 50kΩ to −5.2V	*
Setup Time (Data)	ns, min	2.5	*
Hold Time (Data)	ns, min	1.5	*
Propagation Delay	ns (max)	4 (5)	*
$\overline{10\% \text{ BRIGHT}}$, $\overline{\text{REFERENCE WHITE}}$, $\overline{\text{COMPOSITE SYNC}}$, AND $\overline{\text{COMPOSITE BLANKING}}$ INPUTS			
Logic Compatibility		ECL[6]	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		5pF and 50kΩ to −5.2V	*
SPEED PERFORMANCE – CONTROL INPUTS			
Settling Time to 10% of Final Value for:			
$\overline{10\% \text{ Bright}}$	ns, max	10	*
$\overline{\text{Reference White}}$	ns, max	10	*
$\overline{\text{Composite Sync}}$	ns, max	10	*
$\overline{\text{Composite Blanking}}$	ns, max	10	*
SETUP CONTROL			
Ground	mV (IRE Units)	0 (0)	*
Open	mV (IRE Units)	53.25 (7.5)	*
1k to −5.2V	mV (IRE Units)	71 (10)	*
−5.2V	mV (IRE Units)	142 (20)	*
ANALOG OUTPUT			
GS Current[7]	mA	0 to −17	*
GS Voltage[8]	mV (±1%)	0 to −637.5	*
Compliance	V	−1.2 to +0.1	*
Internal Impedance	Ω (min/max)	800 (680/920)	*
$\overline{\text{REFERENCE WHITE}}$[9]			
Current			
Logic "1"	mA (±5%)	Normal Operation	*
Logic "0"	mA (±3%)	0 or −1.9	*
Voltage			
Logic "1"	mV (±3%)	Normal Operation	*
Logic "0"	mV (±3%)	0 or −71	*
$\overline{10\% \text{ BRIGHT}}$[10]			
Current			
Logic "1"	mA (±5%)	−1.9	*
Logic "0"	mA (±5%)	0	*
Voltage			
Logic "1"	mV (±5%)	−71	*
Logic "0"	mV (±5%)	0	*

Parameter	Units	AD9700BD/BW[1]	AD9700SD[2]
COMPOSITE SYNC[10,11]			
Current			
Logic "1"	mA (±5%)	0	*
Logic "0"	mA (±5%)	−7.6	*
Voltage			
Logic "1"	mV (±5%)	0	*
Logic "0"	mV (±5%)	−285	*
COMPOSITE BLANKING[10,11]			
(Assumes Setup is Open, Which is Equivalent to 7.5 IRE Units)			
Current			
Logic "1"	mA (±5%)	0	*
Logic "0"	mA (±5%)	−1.4	*
Voltage			
Logic "1"	mV (±5%)	0	*
Logic "0"	mV (±5%)	−53.25	*
VOLTAGE REFERENCE TOLERANCE			
(Deviation from Nominal −1.26V)	mV (max)	±20 (±60)	*
POWER REQUIREMENTS			
−5.2V ±0.25V	mA (max)	125 (155)[12]	125 (155)[12]
Power Supply Rejection Ratio	%/V	0.025/0.25	*
Power Dissipation	mW (max)	650 (728)	*
TEMPERATURE RANGE			
Operating (Case)	°C	−25 to +85	−55 to +125
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[13]			
Junction to Air, θja (Free Air)	°C/W, max	55	*
Junction to Case, θjc	°C/W, max	15	*
MTBF[14]			
Mean Time Between Failures	Hours	1.95×10^5	*
PACKAGE OPTIONS[15]			
Ceramic (D-22)		AD9700BD AD9700BW	AD9700SD
Cerdip (Q-22)		AD9700BD	AD9700SD
LCC (E-28A)		AD9700BE	AD9700SE

For applications assistance, phone (919) 668-9511.

NOTES
[1]Electrical specifications for AD9700BE same as AD9700BD/BW.
[2]Electrical specifications for AD9700SE same as AD9700SD.
[3]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50% points) is not included.
[4]Minimum update rate limited by full-scale settling time for eight bits. Unit can be updated to 125MHz.
[5]Glitch can be reduced with glitch adjustment.
[6]See Figure 2 for operation with TTL logic.
[7]FS current = GS current + video functions = 30mA.
[8]LSB value of 2.5mV used for calibration. This causes Gray Scale output to to be 637.5mV rather than 643mV shown in idealized composite waveform elsewhere in this data sheet; both values are well within the output and EIA Standard RS-170 tolerances. $I_{OUT} = (1.26/R_{SET}) \times 4$ when $R_{SET} = 300\Omega$.
[9]Effect on analog output of logic "0" at Reference White input depends on signal at 10% Bright input (see Table I).
[10]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray Scale analog output at Pin 13.
[11]Composite Sync or Composite Blanking control signals reset input registers. Composite Sync or Composite Blanking should not be operated simultaneously with Reference White.
[12]Maximums shown are at temperature extremes.
[13]Maximum junction temperature = +150°C.
[14]Calculated using MIL HNBK-217; Ground Fixed; +25°C Ambient.
[15]See Section 14 for package outline information.
*Specifications same as AD9700BD/BW.
Specifications subject to change without notice.

PIN CONFIGURATIONS

MODELS AD9700BD, AD9700BW, and AD9700SD

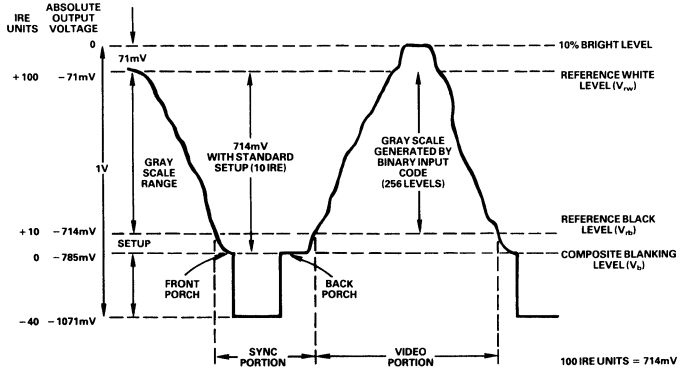
PIN	FUNCTION	PIN	FUNCTION
1	GROUND	12	GROUND
2	−5.2V	13	OUTPUT
3	BIT 1 (MSB)	14	CURRENT SET
4	BIT 2	15	COMPENSATION
5	BIT 3	16	REFERENCE WHITE
6	BIT 4	17	COMPOSITE SYNC
7	BIT 5	18	COMPOSITE BLANKING
8	BIT 6	19	10% BRIGHT
9	BIT 7	20	GLITCH ADJUST
10	BIT 8 (LSB)	21	SETUP
11	STROBE	22	GROUND

NOTE: CONNECT PINS 1, 12, AND 22 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.

MODELS AD9700BE, AD9700SE

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	15	GROUND
2	GROUND	16	OUTPUT
3	GROUND	17	−5.2V
4	−5.2V	18	CURRENT SET
5	BIT 1 (MSB)	19	COMPENSATION
6	BIT 2	20	REFERENCE WHITE
7	BIT 3	21	COMPOSITE SYNC
8	BIT 4	22	NO CONNECTION
9	BIT 5	23	COMPOSITE BLANKING
10	BIT 6	24	10% BRIGHT
11	BIT 7	25	GLITCH ADJUST
12	BIT 8	26	SETUP
13	STROBE	27	−5.2V
14	NC	28	V_{BB}

NOTE: CONNECT PINS 1, 2, 3, AND 15 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.



Idealized Composite Output Waveform

DIGITAL INPUTS VS. ANALOG OUTPUT

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	10% Bright	Ref. White	Comp. Blanking	Comp. Sync	Analog Output (mV)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.50[1]
X	X	X	X	X	X	X	X	0	1	0	1	−690.75[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.50[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.50[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.50[1]
X	X	X	X	X	X	X	X	0	1	0	0	−975.75[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.50[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.50[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.50[1]
X	X	X	X	X	X	X	X	1	1	0	0	−1046.75[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.50[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.50[4]

NOTES
[1]Setup (Pin 21) grounded (0 IRE units).
[2]Setup (Pin 21) open (7.5 IRE units).
[3]Setup (Pin 21) to −5.2V through 1k (10 IRE units).
[4]Setup (Pin 21) to −5.2V (20 IRE units).

Analog output values shown are based on LSB value of 2.5mV used for ease of calibration; this causes Gray Scale output to be 637.5mV rather than 643mV shown elsewhere in this data sheet in sketch of idealized composite output. Both values are well within the output and EIA Standard RS-170 tolerances.

Table I.

USING AD9700 AS RASTER SCAN D/A

Refer to the block diagram of the AD9700 D/A converter.

The digital input bits represent the Gray Scale value of the 256 (2^8) discrete levels between Reference Black and Reference White in a composite video signal, and are applied to Pins 3 through 10.

The output analog signal (at Pin 13) will be a function of these digital inputs. The output will also be affected by the ECL levels at the control inputs of 10% Bright, Reference White, Composite Sync, and Composite Blanking; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs and various combinations of control inputs are selected.

Refer to Table I.

As the footnote to this figure points out, the full-scale (−637.5mV) output of the AD9700 is different from the −643mV output of the idealized composite waveform shown elsewhere in this data sheet. The reason for this discrepancy is Analog Devices' use of 2.5mV for the value of the LSB; that choice of LSB weighting eases calibration of the converter. The disparity does not cause any problems in using the device, since both values are well within the tolerances of the output and the RS-170 standard.

Referring again to the block diagram, the Strobe input applied to the AD9700 clocks the input registers when the strobe signal makes the transition from a logic "0" to a logic "1". The purpose of the registers is to remove time skew from the digital input bits and minimize pertubations or "glitches" in the analog output signal.

The signal applied to the Reference White input sets the input registers, thereby overriding the video input word. When this occurs, the analog output of the AD9700 goes to 0V or to −71mV, depending upon whether or not the 10% Bright signal is also operated.

A logic "0" applied to either the Composite Sync or Composite Blanking input will reset the input registers to 00000000. The analog output at Pin 13 will be −922.5mV (−637.5mV plus −285mV) if the Composite Sync input is operated; this is not affected by the value of IRE units at the setup input.

When Composite Blanking is operated, the analog output will go to its full-scale value of −637.5mV plus some additional amount, as determined by the voltage at setup. The −53.25mV example used in the specifications section of the data sheet is based on the setup input floating, which is equivalent to 7.5 IRE units. (For this example, the analog output would be 690.75mV.)

The internal voltage reference shown in the block diagram is a bandgap type. Including this reference within the converter eliminates the need for external circuits, making it markedly easier to design the AD9700 into various applications. The internal precision reference also provides superior power supply rejection and gain tempco.

Details on the connections for using the AD9700 in composite video applications are shown in Figure 1.

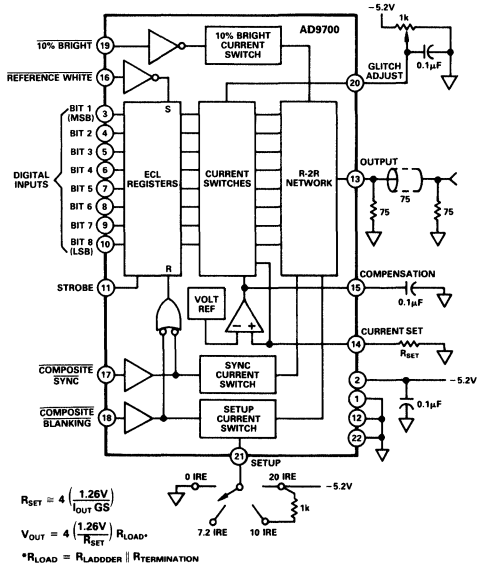


Figure 1. AD9700 D/A Connections

The value of R_{SET} can be established by using the first of the two equations which are part of the connection illustration; in the formula, the 1.26 volts is the reference voltage. When that voltage is divided by the desired Gray Scale current, the value which results is approximately one-fourth the resistance of R_{SET}.

The resistance of R_{SET}, in turn, can be used in the calculation of analog output voltage when the AD9700 is operating as a raster scan D/A converter. The full-scale current of the device is the Gray Scale current plus the video functions, and is specified at 30mA total. The user needs to keep that number in mind to assure that the AD9700 is utilized correctly in circuit designs.

In some instances, the user may be driving a lighter load than the coaxial cable shown in Figure 1 and prefers to operate with lower power dissipation than that in high speed raster scan use. For these situations, the value of R_{SET} can be doubled, which halves the output current while still maintaining a useable current drive from the converter. Power dissipation would be reduced approximately 75mW; the trade-off to obtain this is a decrease in the speed of the AD9700 and a lengthening of setting time.

Ground pins 1, 12, and 22 are shown connected together and to ground near the unit; this is the recommended procedure for obtaining optimum performance, especially in high-speed applications. Inside the AD9700, Pin 1 is register ground; Pin 12 is analog ground; and Pin 22 is digital ground.

For some applications, in addition to by-passing the $-5.2V$ supply with $0.01\mu F$ as shown, it may be desirable to by-pass it also with a tantalum capacitor of $3.3 - 10\mu F$. Although this is not generally necessary, it may enhance the converter's performance in some designs.

The circuit connected to Pin 21 setup is used for illustrative purposes to demonstrate the relationships of various IRE units; it is not intended to imply this is the preferred way to obtain these values. At Pin 20, the circuit used for adjusting the glitch can reduce the amount of glitch from its typical 50pV-s to a lesser value for those applications which require it.

USING AD9700 IN TTL MODE

Most applications using the AD9700 for composite video reconstruction will be in ECL systems, but there may be instances where its high-performance characteristics need to be applied in TTL designs.

A method of accomplishing this is illustrated in Figure 2.

Except as shown, all input pull-up resistors which are used are the same value: $2k\Omega$. If some of the input bit connections are not used because of operating with fewer than eight bits of resolution, the unused input pins should be resistively connected to $+5V$ to prevent undesirable side effects in the performance of the converter.

This same technique of resistively connecting unused inputs to $+5V$ also applies for the Reference White, Composite Sync, and Composite Blanking inputs. If 10% Bright is not used, Pin 19 should be either grounded or left open; no pull-up resistor should be used.

The table which is part of Figure 2 shows the required connections to Pin 21 for the various blanking levels when operating in the TTL mode.

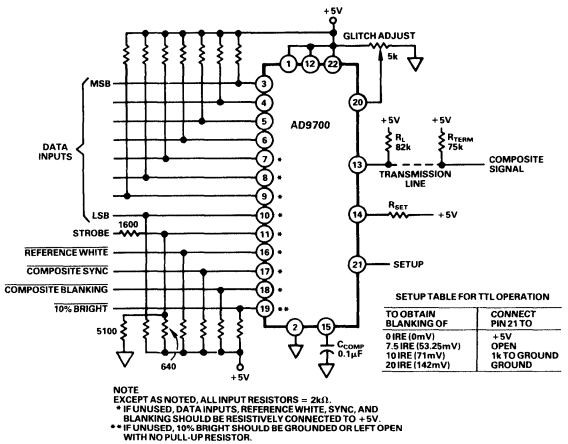


Figure 2. Using AD9700 in TTL Mode

USING AD9700 AS STANDARD D/A

Although designed for use in composite video applications, the AD9700 can also be utilized as a standard D/A converter with remarkable performance. The extremely low glitch energy of the unit makes it especially attractive, because video reconstruction can be accomplished with exceptional spectral purity.

Refer to Figure 3.

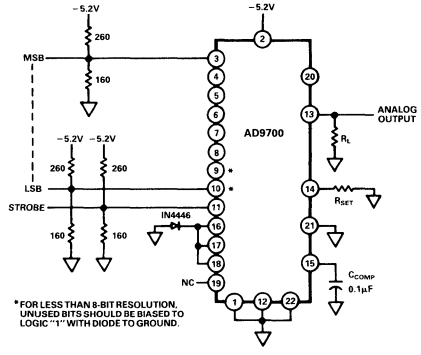


Figure 3. AD9700 as Standard D/A

When used as a standard D/A, the unused control inputs required for video applications are connected to ground; in most cases, this connection is made through a diode. Examples of that are shown on Pins 16, 17, and 18, the inputs for Reference White, Composite Sync, and Composite Blanking, respectively. The 10% Bright input (Pin 19) is left open, and setup (Pin 21) is tied directly to ground.

If fewer than eight bits of digital input will be applied, the unused input pins should be connected to ground via a diode with the same technique used at Pins 16, 17, and 18. If they are tied directly to ground, converter performance may be affected adversely.

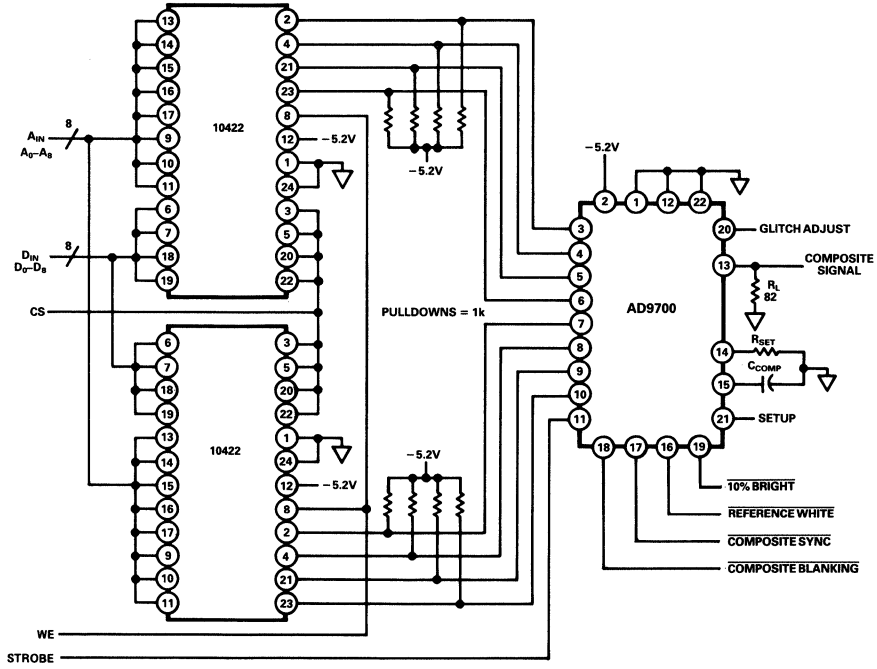


Figure 4. Using the AD9700 with Look-Up Table

USING AD9700 WITH RANDOM ACCESS MEMORY

In many applications, it may be necessary to operate the AD9700 D/A converter with look-up tables (LUT's) for raster scan display applications. One possible way to operate with fast random access memory (RAM) is shown in Figure 4.

If the user is interested in obtaining an RGB video subsystem, the circuit which is shown would be repeated three times. The Address Bus (A_{IN}), Data Bus (D_{IN}), Write enable (WE), and Strobe lines for the three would be connected in parallel. During write operations, the appropriate Chip Select (CS) line would be operated to control which RAM will receive data on the Data Bus.

Data are written into the RAM during an inactive portion of the scan cycle. The full tables can be written during the vertical retrace time; or small blocks of data can be written during the horizontal retrace. Write cycle timing requirements for the 10422 RAM which is illustrated are shown in Figure 5.

The major advantage of the configuration recommended here is realized during the read mode of the RGB system. In the method illustrated in Figure 4, all three D/A converter outputs are updated simply by changing the 8-bit address. Refer to Figure 6.

This illustrates the timing relationships and the intervals for the various operations which occur during the read cycle of the LUT.

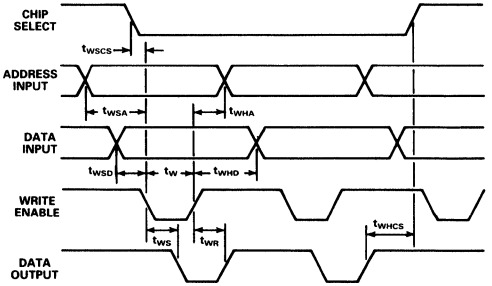


Figure 5. LUT Write Cycle Timing Diagram

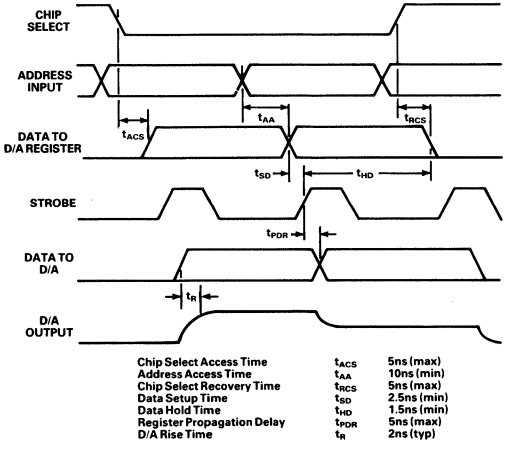


Figure 6. LUT Read Cycle Timing Diagram

ANALOG DEVICES

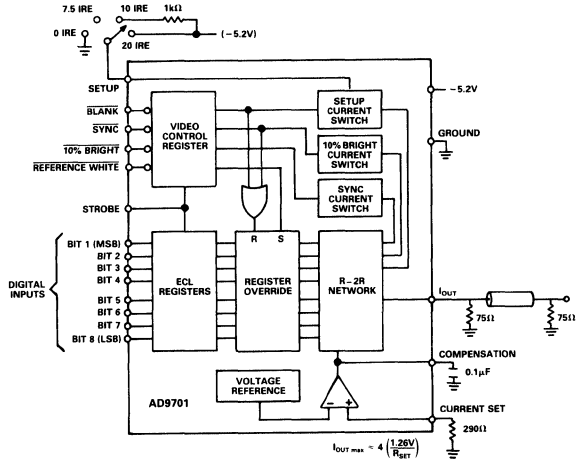
250MHz Video Digital-to-Analog Converter

AD9701

FEATURES
250MHz Update Rate
Low Glitch Impulse
Complete Composite Functions
Internal Voltage Reference
Single −5.2V Supply

APPLICATIONS
Raster Scan Displays
Color Graphics
Automated Test Equipment
TV Video Reconstruction

AD9701 FUNCTIONAL BLOCK DIAGRAM



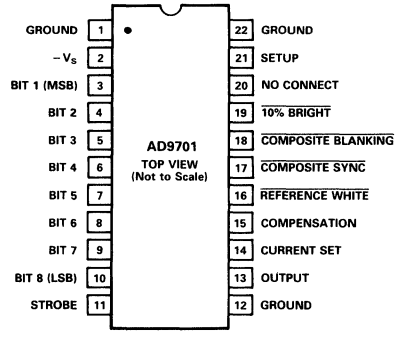
GENERAL DESCRIPTION

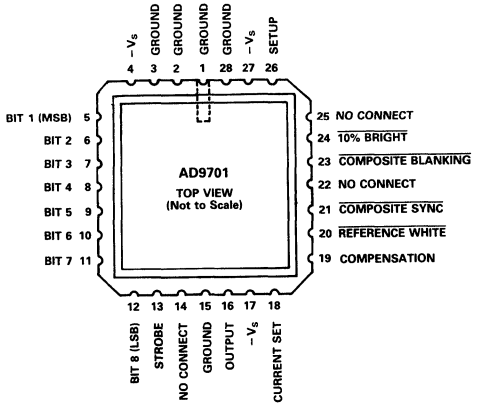
The AD9701 is a high-speed, 8-bit digital-to-analog converter with fully integrated composite video functions. High-speed ECL input registers provide synchronous operation of data and control functions up to 250MHz.

The AD9701 incorporates on-board control functions including horizontal sync, blanking, reference white level, and a 10% bright signal for highlighting. The setup level is also adjustable from 0 IRE units to 20 IRE units, through the control pin. An internal voltage reference allows the AD9701 to operate as a stand-alone video reconstruction DAC.

The AD9701 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades of the AD9701 are packaged in a 22-pin ceramic DIP, with the extended temperature device also available in a 28-pin LCC package.

PIN CONFIGURATIONS





ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9701BQ	−25°C to +85°C	22-Pin DIP, Industrial Temperature	D-22
AD9701SE	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9701SQ	−55°C to +125°C	22-Pin DIP, Extended Temperature	D-22

*See Section 14 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($-V_S$) . . . . . −7V
Digital Input Voltages (including STROBE, SYNC, BLANKING, 10% BRIGHT, and REFERENCE WHITE) . . . . . 0V to $-V_S$
Analog Output Current 37mA
Power Dissipation (+25°C Free Air)[2] 780mW
Operating Temperature Range
AD9701BQ . . . . . −25°C to +85°C
AD9701SQ/SE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2V; R_L = 37.5Ω; Setup = 0V, unless otherwise stated)

Parameter	Temp	AD9701BQ Min	AD9701BQ Typ	AD9701BQ Max	AD9701SQ/SE Min	AD9701SQ/SE Typ	AD9701SQ/SE Max	Units
RESOLUTION		8			8			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Integral Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Monotonicity	Full	GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR[3]								
Zero-Scale Offset Error[4]	+25°C		0.05	0.9		0.05	0.9	mV
	Full			0.9			0.9	mV
Zero-Scale Offset Drift Coefficient	Full		2			2		µV/°C
Full-Scale Drift Coefficient	Full		50			50		µV/°C
ANALOG OUTPUT								
Voltage Output[5]								
10% Bright[6]	Full	−0.9	0		−0.9	0		mV
Reference White	Full	−67.45	−71	−74.55	−67.45	−71	−74.55	mV
Blanking (Setup = 0 IRE)[7]	Full	−698.55	−708.5	−718.45	−698.55	−708.5	−718.45	mV
Sync (Setup = 0 IRE)[8]	Full	−979.25	−993.5	−1007.75	−979.25	−993.5	−1007.75	mV
Current Output[5]								
10% Bright[6]	Full	−0.024	0		−0.024	0		mA
Reference White	Full	−1.805	−1.9	−1.996	−1.805	−1.9	−1.995	mA
Blanking (Setup = 0 IRE)[7]	Full	−18.63	−18.9	−19.16	−18.63	−18.9	−19.16	mA
Sync (Setup = 0 IRE)[8]	Full	−26.11	−26.5	−26.87	−26.11	−26.5	−26.87	mA
Output Compliance Range	Full		−1.6; +0.1			−1.6; +0.1		V
Output Resistance	+25°C	640	800		640	800		Ω
DYNAMIC PERFORMANCE								
Update Rate	+25°C	225	250		225	250		MHz
Output Propagation Delay[9]	+25°C		5	6		5	6	ns
Output Settling Time[10]								
Current	+25°C		8			8		ns
Voltage	+25°C		12			12		ns
Output Slew Rate[11]	+25°C	255	300		255	300		V/µs
Output Rise Time[11]	+25°C		1.7	2.0		1.7	2.0	ns
Output Fall Time[11]	+25°C		1.7	2.0		1.7	2.0	ns
Glitch Impulse	+25°C		60	70		60	70	pV-s
SETUP CONTROL[12]								
Setup Level (Grounded)	Full		0			0		IRE
Setup Level (Open)	Full		7.5			7.5		IRE
Setup Level (Tied to −5.2V with 1kΩ)	Full		10			10		IRE
Setup Level (−5.2V)	Full		20			20		IRE
DIGITAL INPUTS								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
Logic "1" Current	Full			100			100	µA
Logic "0" Current	Full			15			15	µA
Input Capacitance	+25°C		4	5.5		4	5.5	pF
Data Setup Time	+25°C	0.1			0.1			ns
Data Hold Time	+25°C	1.4			1.4			ns

Parameter	Temp	AD9701BQ Min	AD9701BQ Typ	AD9701BQ Max	AD9701SQ/SE Min	AD9701SQ/SE Typ	AD9701SQ/SE Max	Units
POWER SUPPLY [13]								
Supply Current (−5.2V)	+25°C		140	160		140	160	mA
	Full			160			160	mA
Nominal Power Dissipation	+25°C		728			728		mW
Power Supply Rejection Ratio[14]	Full		3	6		3	6	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance . . .
22-Pin Ceramic $\theta_{ja} = 64°C/W$; $\theta_{jc} = 16°C/W$
28-Pin Ceramic LCC $\theta_{ja} = 70°C/W$; $\theta_{jc} = 21°C/W$

[3]SYNC, BLANKING, and REFERENCE WHITE are inactive (Logic "1"). $I_{SET} \approx 1.26V/R_{SET}$.

[4]All bits at logic HIGH.

[5]All values are relative to full-scale output, after being normalized to nominal value. Typical variation in full-scale output from device to device can reach ± 10%, for a fixed R_{SET} resistor.

[6]The effect of 10% BRIGHT algebraically adds to the output waveform.

[7]The output level with BLANKING active (Logic "0"), is determined by the setup control level.

[8]In normal operation, the BLANKING input is activated (Logic "0") prior to or in conjunction with the SYNC input. The effect of the SYNC utput is relative to the setup level.

[9]Measured from edge of STROBE to 50% transition point of the output signal.

[10]Measured with full-scale change in output level, from the 10% transition level to within ± 0.2% of the final output value.

[11]Measured from 10% to 90% transition point for full-scale step output.

[12]An IRE unit is 1% of the Grey Scale (GS range) with a 0 IRE setup level.

[13]Supply Voltage should remain stable within ± 5% for normal operation.

[14]Measured at ± 5% of $-V_S$.

Specifications subject to change without notice.

DIGITAL INPUTS VS. ANALOG OUTPUT

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	10% Bright	Ref. White	Blanking	Comp. Sync	Analog Output (mV)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.50[1]
X	X	X	X	X	X	X	X	0	1	0	1	−690.75[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.50[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.50[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.50[1]
X	X	X	X	X	X	X	X	0	1	0	0	−975.75[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.50[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.50[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.50[1]
X	X	X	X	X	X	X	X	1	1	0	0	−1046.75[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.50[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.50[4]

NOTES
1. Setup (Pin 21) grounded (0 IRE units).
2. Setup (Pin 21) open (7.5 IRE units).
3. Setup (Pin 21) to −5.2V through 1k (0 IRE units).
4. Setup (Pin 21) to −5.2V (20 IRE units).

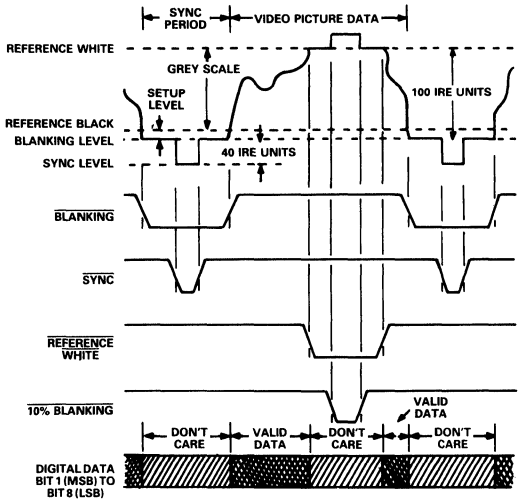
FUNCTIONAL DESCRIPTION

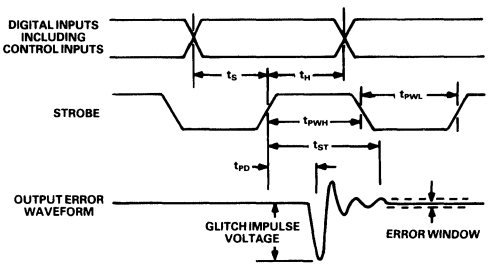
PIN NAME	DESCRIPTION
GROUND	– One of three ground returns. All grounds should be connected together near the AD9701.
$-V_S$	– Negative supply pin, nominally $-5.2V$.
BIT 1 (MSB)	– One of eight digital input bits. BIT 1 (MSB) is the most-significant-bit of the digital input word.
BIT 2 – BIT 7	– One of eight digital input bits.
BIT 8 (LSB)	– One of eight digital input bits. BIT 8 (LSB) is the least-significant-bit of the digital input word.
STROBE	– Data and control register strobe input. STROBE is leading edge triggered.
GROUND	– One of three ground returns. All grounds should be connected together near the AD9701.
SETUP	– The SETUP input determines the position of the blanking level relative to the "reference black" level (all data bits at logic "0"). The setup level is adjustable from 0 IRE units to 20 IRE units below the reference black level (an IRE unit is 1% of the "grey scale" range).

SETUP LEVEL	CONFIGURATION (PIN 21)
0 IRE Units	Ground
7.5 IRE Units	Open
10 IRE Units	Connection to $-5.2V$ through $1k\Omega$
20 IRE Units	Connection to $-5.2V$

$\overline{\text{10\% BRIGHT}}$	– $\overline{\text{10\% BRIGHT}}$ adds an additional current to the output level, equal to roughly 10% of the "grey scale" range. The $\overline{\text{10\% BRIGHT}}$ is active logic LOW, and operates independently of all other inputs.
$\overline{\text{COMPOSITE BLANKING}}$	– The $\overline{\text{COMPOSITE BLANKING}}$ input, active logic LOW, forces output to the blanking level set with the SETUP input.
$\overline{\text{COMPOSITE SYNC}}$	– The $\overline{\text{COMPOSITE SYNC}}$ input, active LOW, creates a negative going horizontal synchronization pulse relative to the blanking level. Under normal operating conditions the $\overline{\text{COMPOSITE BLANKING}}$ signal should precede and extend past the $\overline{\text{COMPOSITE SYNC}}$ signal. See SETUP for additional information.
$\overline{\text{REFERENCE WHITE}}$	– The $\overline{\text{REFERENCE WHITE}}$ input, active LOW, overrides the data inputs, and forces the output to the maximum "grey scale" level.
COMPENSATION	– The COMPENSATION input insures adequate gain stability for the internal reference amplifier. Under normal operating conditions, the COMPENSATION input is decoupled to ground through a $0.1\mu F$ capacitor.
CURRENT SET	– The CURRENT SET input determines the full-scale or "grey scale" range. The effects of the video control functions are in addition to the "grey scale" range. ($168\Omega \leq R_{SET} \leq 600\Omega$). $I_{OUTmax} \approx 4I_{SET} = 4(1.26V/R_{SET})$
OUTPUT	– Analog output.
GROUND	– One of three ground returns. All grounds should be connected together near the AD9701.

SYSTEM TIMING DIAGRAMS

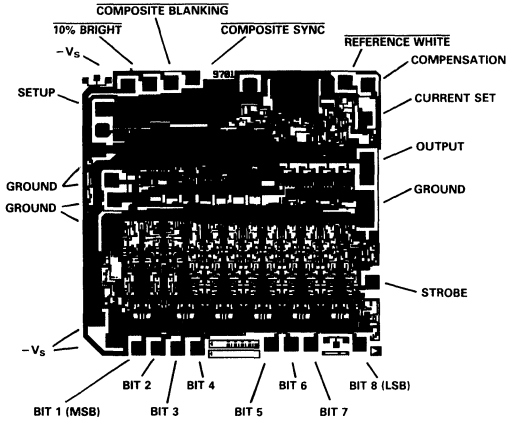




t_S	DIGITAL DATA SETUP TIME
t_H	DIGITAL DATA HOLD TIME
t_{PWH}	STROBE PULSE WIDTH HIGH
t_{PWL}	STROBE PULSE WIDTH LOW
t_{ST}	SETTLING TIME
t_{PD}	MINIMUM PROPAGATION DELAY

NOTES
1. ALL INPUTS, INCLUDING THE VIDEO CONTROL FUNCTIONS, ARE SYNCHRONIZED TO THE STROBE INPUT.
2. THE 10% BRIGHT CONTROL WILL INCREASE THE OUTPUT LEVEL BY APPROXIMATELY 10 IRE UNITS OVER THE PRESENT OUTPUT LEVEL.
3. AN IRE UNIT IS IDEALLY 7.14mV.

DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	107 × 104 × 15 (± 2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding or 1mil Gold; Gold Ball Bonding

APPLICATIONS INFORMATION

Raster scan video displays image data on a line by line basis, with timing and control signals inserted between the lines. The control signals include the horizontal synchronization pulses which are used to align the display circuitry at the beginning of each line. After the complete video image is displayed on the monitor, the process begins again with the next image. The vertical reset pulse(s) that initiate this timing sequence are located between each video image.

The image data is distinguished from the timing information by its location relative to the blanking level. The blanking reference level is at the blackest extreme of the image data, and all timing signals are designed to fall below the blanking level so as not to be seen on the monitor. The actual image data is located above the blanking level, and it may be further separated from the timing signal by the setup level. The setup level is simply a buffer zone between the timing and image data.

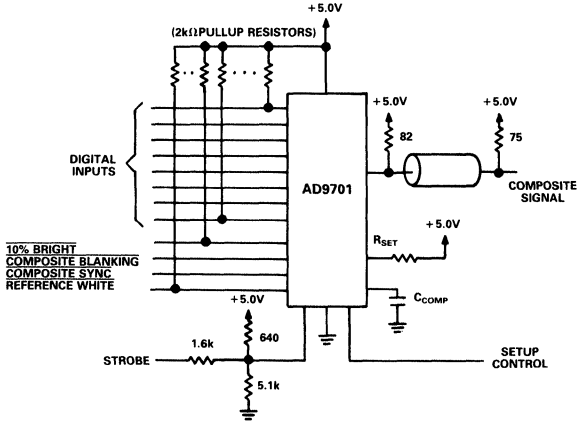
Generation of the timing signals for the AD9701 is controlled by the $\overline{\text{COMPOSITE BLANKING}}$ and the $\overline{\text{COMPOSITE SYNC}}$ inputs. In normal operation the output level of the AD9701 is forced to the blanking level (black) with the $\overline{\text{COMPOSITE BLANKING}}$ control so that when the synchronization occurs, it will not interfere (be seen) with the monitor image. The $\overline{\text{COMPOSITE SYNC}}$ control forces the output level below the blanking level, generating the synchronization pulse.

The "grey scale" is the image intensity range, located above the blanking level by the amount of the setup level. The setup level is "reference black," the darkest displayable picture intensity. The top of the "grey scale" is "reference white," or the brightest picture intensity. As an 8-bit device, the AD9701 divides the "grey scale" into 256 individual levels.

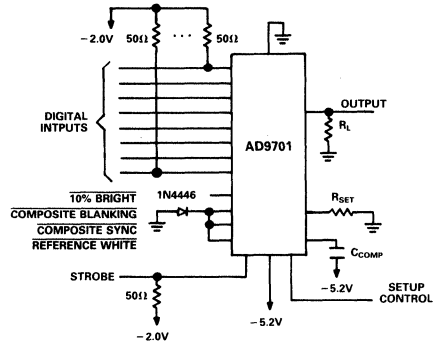
Normal raster scan waveforms divide the region between the blanking level and reference white into 100 IRE units (International Radio Engineers). The setup level can range from 0 to 20 IRE units, but typically is around 10 IRE units, and the synchronization pulse level typically falls 40 IRE units below the blanking level. For the AD9701, the reference white level is 10 IRE units below the full-scale output range ($0mA_{OUT}$).

In terms of priority, the $\overline{\text{REFERENCE WHITE}}$ control overrides the data inputs, but both $\overline{\text{COMPOSITE SYNC}}$ and $\overline{\text{COMPOSITE BLANKING}}$ override the data inputs and the $\overline{\text{REFERENCE WHITE}}$ control. A fourth control is active at all times, $\overline{\text{10\% BRIGHT}}$, which adds approximately 10 IRE units to the output level no matter what the input state of the AD9701. The $\overline{\text{10\% BRIGHT}}$ control is primarily used to highlight areas of the video image.

As with any high-speed device, the AD9701 requires a substantial low impedance ground plane and high quality ground connections to achieve the best performance. Performance can also be improved with adequate power supply decoupling near the supply pins of the AD9701. In ECL mode, the output of the AD9701 is designed to drive 75Ω cable directly, with 75Ω terminations to ground at both ends of the cable. For TTL configurations the output should be terminated to +5.0V through an 82Ω resistor (see circuit below).



Raster Graphics Configuration for TTL Systems



Standard Reconstruction Configuration

ANALOG DEVICES

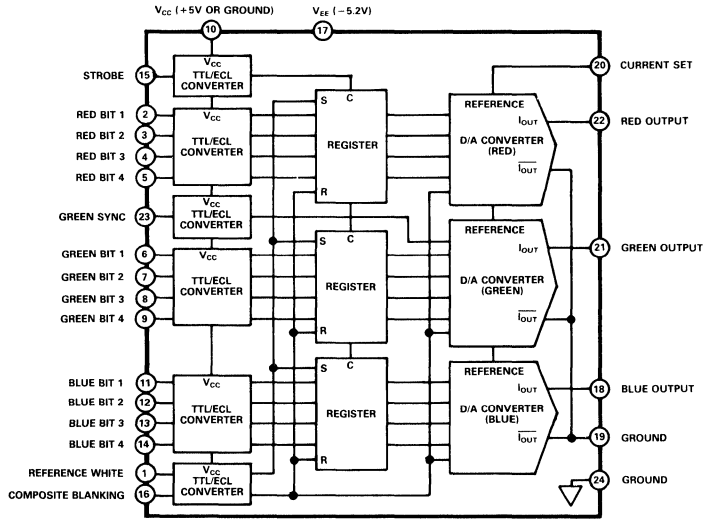
Triple 4-Bit D/A Converter

AD9702

FEATURES
ECL or TTL Compatible
Composite Inputs
125MHz Update Rates Minimum

APPLICATIONS
Raster Scan Displays
Color Graphics Systems
General Video Reconstruction

AD9702 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9702 D/A Converter is a single monolithic IC containing three separate 4-bit digital-to-analog (D/A) converters for red, green, blue (RGB) graphics display applications; 4,096 colors are available to the user. Composite blanking, green sync, and reference white digital control inputs are also included. On-chip data registers and a capability for varying output drive make this a *total* functional solution for graphics displays.

A unique TTL/ECL interface allows the designer a choice of logic compatibility for all inputs; this can be accomplished by applying either +5V or ground to the V_{CC} pin. Internally, the registers and control switching signals operate at ECL logic levels to help assure low glitch impulse at the DAC outputs.

The unit is housed in a 24-pin ceramic package and operates with −5.2V applied for the ECL mode; and −5.2V and +5V for TTL mode. Power dissipation is 1.3 watts for ECL operation and 1.5 watts for TTL.

Monolithic devices are inherently less expensive and more reliable than hybrids. When combined with its small size and outstanding electrical characteristics, these attributes make the AD9702 D/A Converter the first choice for designers of next-generation, medium-resolution displays.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	AD9702BD/BW
RESOLUTION	Bits	4
LEAST SIGNIFICANT BIT (LSB) WEIGHT		
Voltage (Adjustable)	mV	40
Current (Adjustable)	mA	1
ACCURACY (GS = Gray Scale; FS = Full Scale)		
Linearity	±% GS	0.8
Differential Linearity	±% GS, max	0.8
Zero Offset (Initial)	mV, max	0.5
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C (max)	20 (30)
Zero Offset	ppm/°C (max)	10 (15)
Gain	ppm/°C (max)	200 (400)
Gain Tracking	ppm/°C	100
DYNAMIC CHARACTERISTICS		
Settling Time – Voltage[1]		
ECL Mode (to ±3.2% GS)	ns, max	5
TTL Mode (to ±3.2% GS)	ns, max	6
Update Rate		
ECL Mode	MHz, min	125
TTL Mode	MHz, min	75
Rise Time	ns	3
Glitch Impulse	pV-s	80
DIGITAL INPUTS		
Logic Compatibility		ECL/TTL
Coding		Binary (BIN)
ECL Logic Levels		
"1"	V (min/max)	−0.9 (−1.1/−0.6)
"0"	V (min/max)	−1.7 (−2.0/−1.5)
TTL Logic Levels		
"1"	V (min/max)	+3.5 (+2.0/+5.0)
"0"	V (min/max)	+0.2 (+0.0/+0.8)
Loading (Each Bit; with Typical Input Logic Levels)		
ECL "1"	µA/pF	50/5
ECL "0"	µA/pF	−100/5
TTL "1"	µA/pF	10/5
TTL "0"	mA/pF	1.5/5
Setup Time (Data)		
ECL	ns, max	2.5
TTL	ns, max	3.5
Hold Time (Data)		
ECL	ns, max	2
TTL	ns, max	3
Propagation Delay		
ECL	ns (max)	4 (5)
TTL	ns (max)	5 (6)
SPEED PERFORMANCE – CONTROL INPUTS		
ECL and TTL Settling Time to 10% of GS for:		
$\overline{\text{Reference White}}$	ns, max	10
$\overline{\text{Composite Blanking}}$	ns, max	10
$\overline{\text{Green Sync}}$	ns, max	10
10% Bright	ns	10
RED, GREEN, AND BLUE ANALOG OUTPUTS		
Gray Scale Current	mA	0 to −16
$\overline{\text{Ref White}}$[2] = "0"	mA	0
$\overline{\text{Ref White}}$ = "1"	mA	Normal Operation[3]
$\overline{\text{Composite Blanking}}$[4] = "0"	mA	−1.4
$\overline{\text{Composite Blanking}}$ = "1"	mA	Normal Operation
$\overline{\text{Green Sync}}$[5] = "0"	mA	−7.6
$\overline{\text{Green Sync}}$ = "1"	mA	Normal Operation
Gray Scale Voltage	mV	0 to −600 (±1%)
$\overline{\text{Ref White}}$[2] = "0"	mV	0
$\overline{\text{Ref White}}$ = "1"	mV	Normal Operation[3]
$\overline{\text{Composite Blanking}}$[4] = "0"	mV	−53
$\overline{\text{Composite Blanking}}$ = "1"	mV	Normal Operation
$\overline{\text{Green Sync}}$[5] = "0"	mV	−285
$\overline{\text{Green Sync}}$ = "1"	mV	Normal Operation

ABSOLUTE MAXIMUM RATINGS

	ECL Lower	ECL Upper	TTL Lower	TTL Upper
Supply Voltages				
V_{CC} (Pin 10)	−0.1V	+1.0V	0.0V	+6.0V
V_{EE} (Pin 17)	−6.0V	+0.3	−6.0V	+0.3V
Power Dissipation (Nominal Voltages)	1.5W		1.8W	
D/A Output Current	30mA		30mA	
Temperature				
Operating (Case)	−55°C to +125°C		−55°C to +125°C	
Storage	−55°C to +150°C		−55°C to +150°C	

PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
24	GROUND	1	$\overline{\text{REFERENCE WHITE}}$
23	$\overline{\text{GREEN SYNC}}$	2	RED BIT 1 (MSB)
22	RED OUTPUT	3	RED BIT 2
21	GREEN OUTPUT	4	RED BIT 3
20	CURRENT SET	5	RED BIT 4 (LSB)
19	GROUND	6	GREEN BIT 1 (MSB)
18	BLUE OUTPUT	7	GREEN BIT 2
17	V_{EE} (−5.2V)	8	GREEN BIT 3
16	$\overline{\text{COMPOSITE BLANKING}}$	9	GREEN BIT 4 (LSB)
15	STROBE	10	V_{CC} (+5V OR GROUND)
14	BLUE BIT 4 (LSB)	11	BLUE BIT 1 (MSB)
13	BLUE BIT 3	12	BLUE BIT 2

NOTE: FOR NORMAL OPERATION, CONNECT PINS 19 AND 24 TOGETHER AND TO LOW-IMPEDANCE GROUND PLANE AS CLOSE TO CASE AS POSSIBLE.

Parameter	Units	AD9702BD/BW
RED, GREEN, AND BLUE ANALOG OUTPUTS (Cont.)		
Output Impedance	Ω (min/max)	10k (5k/15k)
Compliance	V	+3.0 to −1.2
Matching (Between any Two Gray Scale Outputs)	±% GS	1.0
RGB Outputs Time Skew	ns, max	2
RGB Outputs Crosstalk[6] (100MHz Bandwidth)	mV	20
Clock Noise on Outputs (100MHz Bandwidth)	mV	5
POWER REQUIREMENTS		
−5.2V ±0.25V[7]	mA (max)	250 (288)
+5V ±0.25V (TTL Only)	mA (max)	50 (60)
Power Supply Rejection Ratio	mV/mV	0.115
ECL Power Dissipation	W (max)	1.3 (1.5)
TTL Power Dissipation	W (max)	1.55 (1.8)
TEMPERATURE RANGE		
Operating (Case)	°C	−25 to +85
Storage	°C	−55 to +150
THERMAL RESISTANCE[8]		
Junction to Air, θ_{JA} (Free Air)	°C/W, max	40
Junction to Case, θ_{JC}	°C/W, max	12
PACKAGE OPTION[9]		
D-24A		AD9702BD
		AD9702BW

NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50% points) is not included.
[2]Digital "0" at Reference White control input (Pin 1) sets registers; red, green, and blue outputs go to zero.
[3]In "normal operation," GS current or GS voltage outputs for red, green, and/or blue are established by RGB digital inputs.
[4]Digital "0" at Composite Blanking control input (Pin 16) resets registers; value shown is added to full-scale outputs at red, green, and blue outputs. Reference White and Composite Blanking should not be operated simultaneously.
[5]Green Sync control signal (@ Pin 23) affects only Green Output (@ Pin 21); value shown is added to Green Output established by Green digital inputs (and by Composite Blanking if digital "0" is simultaneously applied to Pin 16).
[6]Logic "0" digital inputs applied to D/A under test; full scale step function "toggling" applied to active D/A.
[7]Power supplies should have less than 10mV p-p ripple.
[8]Maximum junction temperature = 150°C.
[9]See Section 14 for package outline information.
Specifications subject to change without notice.

2

THEORY OF OPERATION

Refer to the Block Diagram of the AD9702 D/A Converter.

The digital inputs are applied through TTL/ECL converters to registers within the AD9702; the purpose of the registers is to eliminate time skew from the inputs and help reduce glitch impulse in the output signals. The switching of the inputs through the registers to the three internal D/A converters is controlled by the Strobe, Green Sync, Reference White, and Composite Blanking signals.

When operating with ECL-compatible logic, V_{EE} (−5.2V) is applied to Pin 17 and Pin 10 is connected to ground. Under these conditions, the TTL/ECL converters at the input are transparent to incoming signals and the signals are applied directly to the registers. Regardless of the logic levels of the digital inputs, the registers and control logic internal to the AD9702 are operated at ECL levels to help assure maximum switching speed and minimum glitch on the analog outputs.

For TTL logic, V_{CC} (+5V) is applied to Pin 10 and −5.2V is applied to Pin 17. The positive voltage is used only on the TTL/ECL converters, and adds to the flexibility of the AD9702 by allowing it to be compatible with both forms of logic generally encountered in graphics displays.

There is an alternate method of operating with TTL logic without a need for −5.2V supplies. In this arrangement, Pins 10, 19, and 24 are connected to +5V; and Pin 17 is grounded. In addition, digital inputs (RGB Bits 1 – 4) are connected to +5V through 2k resistors on each input line.

The disadvantage of this technique is that the output is referenced to the +5V supply instead of ground. When this happens, the dc component of the output may exceed the general requirements of RS-170 and RS-343. In addition, any noise which is on the power supply can be coupled directly onto the video signal.

One method of overcoming these potential problems is illustrated in Figure 1, Using AD9702 in TTL Mode.

In this arrangement, the strobe signal is attenuated and shifted positively by a resistor network to minimize feedthrough of the clock signal. The digital input signals do not require the same kind of attenuation because their larger TTL swings do not present any problems.

The pull-up resistors which are used on the inputs help assure proper digital "1" logic levels regardless of which TTL logic family is used.

The PNP level shifter shown at the analog output in Figure 1 eliminates the possible problems of TTL operation cited above. Most of the noise which might be present on the +5V supply is cancelled by common mode rejection in this circuit; and level shifting helps insure the dc component of the output meets video standards.

Minor linearity degradation and temperature drift which might be introduced by the level shifter are not discernible on most video displays. The level shifter circuit is repeated three times for the Red, Green, and Blue analog outputs of the AD9702.

As shown in the block diagram and discussed in the Specifications section, a digital "0" level of the Reference White signal (at Pin 1) is used to set the registers within the converter. This action causes the three (RGB) analog outputs to go to zero output.

The Composite Blanking signal is applied to Pin 16; when a digital "0" level is used, it resets the registers and causes the three analog outputs to be −17.4mA or −653mV because of the amount added to the normal full-scale outputs.

The Green Sync signal at Pin 23 has an effect only on the Green Output of the AD9702 (at Pin 21). When this control and Composite Blanking are at a digital "0" level, the value of the Green analog output will be −25mA or −938mV.

When control inputs Reference White, Composite Blanking, and Green Sync are at digital "1" levels, the RGB analog outputs at Pins 22, 21, and 18 will be a function of their corresponding

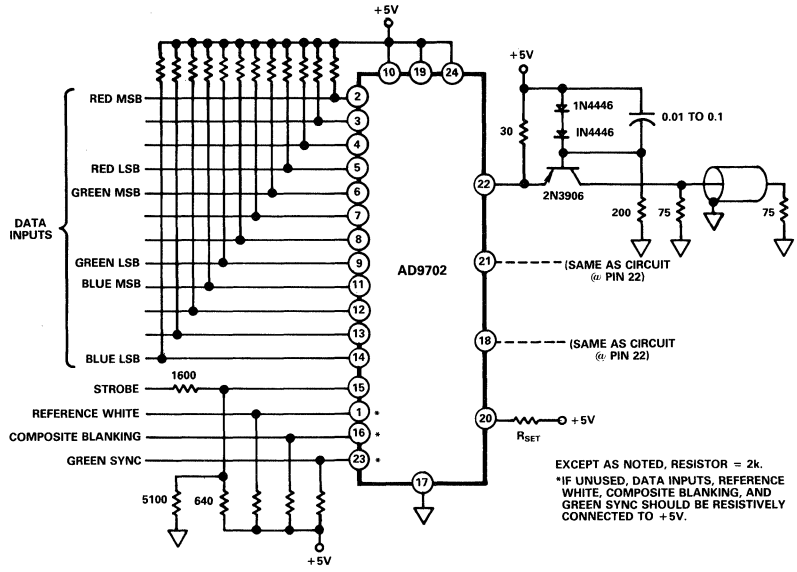


Figure 1. Using AD9702 in TTL Mode (Single Supply)

digital inputs. This is the "normal operation" referred to in the Specifications Table.

Resistor R_{SET} is connected between Pin 20, Current Set, and ground to establish the Gray Scale (GS) value of the RGB outputs. The value to be used is based on the desired full-scale GS output and the following equations:

$$I_{GS} = 5 \times I_{SET}$$

$$R_{SET} = \frac{4.4}{I_{SET}}$$

$$V_{OUT} = \frac{22 \times R_{LOAD}}{R_{SET}}$$

When using these equations, typical values of I_{SET} and V_{OUT} (Gray Scale output) will be within ±5%.

The idealized green analog output is illustrated in Figure 1.

The red and blue analog outputs are similar to the waveform shown in Figure 1, with the exception no sync portion is present on the Red and Blue outputs.

Sync control inputs are not required for Red and Blue outputs because of the RGB signals being synchronized within the AD9702. The majority of applications for the AD9702 in graphics displays use the green sync as the synchronizing signal for the monitor.

ORDERING INFORMATION

The standard AD9702 triple four-bit D/A converter is supplied in hermetic and non-hermetic units. Both versions operate over a case temperature range of −25°C to +85°C. The hermetically-sealed ceramic DIP configuration is model number AD9702BD; the non-hermetic unit is AD9702BW. For special applications or units for military applications, contact the factory for details.

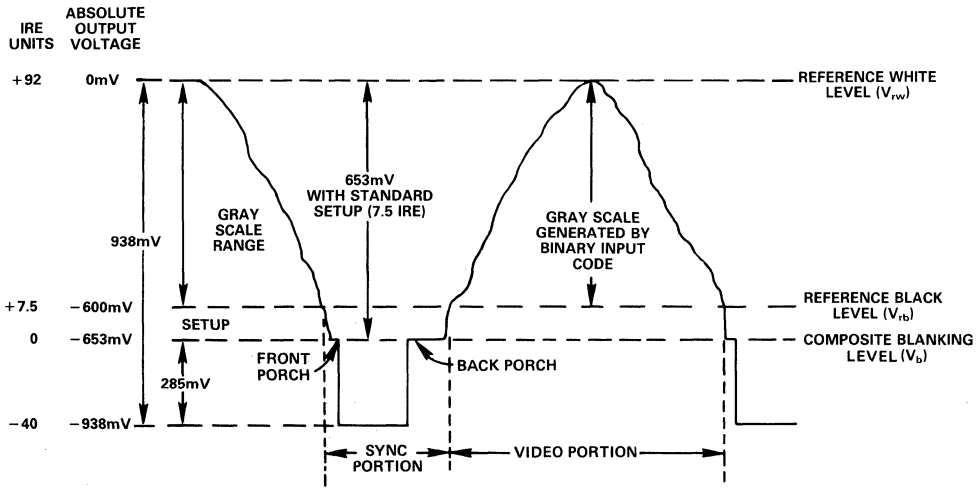


Figure 2. Idealized Green Output Waveform

ANALOG DEVICES

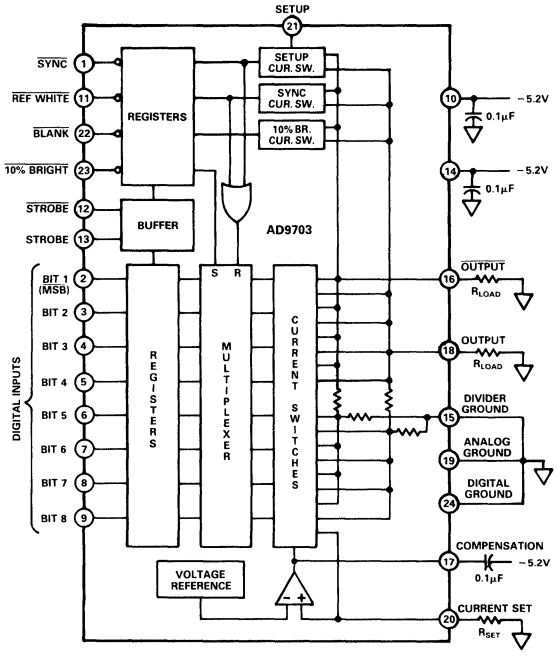
Monolithic Video D/A Converter

AD9703

FEATURES
Update Rates of 300MHz+
Ultra-Low Glitch Impulse
Synchronous Composite Functions
Raster Graphics Complete
Mil Spec Versions Available

APPLICATIONS
Radar/Raster Scan Displays
Color Graphics
Automated Test Equipment
2D/3D Workstations
FLIR/Heads-Up Displays
Medical Imaging

AD9703 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9703 D/A Converter is a state-of-the-art monolithic digital-to-analog converter capable of accepting 8 bits of digital data at update rates of 300MHz. It is designed specifically for ultra-high-performance, high-resolution raster graphics systems but can also be used for other applications which require low glitch, such as waveform generation.

It comes complete with synchronized composite functions including sync, blank, reference white, and 10% bright. The reference white input forces the analog output to the reference white level regardless of the data inputs. The 10% bright input can be used to generate a white cursor on a white background.

Synchronization of the inputs prevents short or missing pixels. Multiplexing video functions from synchronized inputs eliminates recovery times and the need to reset registers. This unique feature is different from most data input register designs and materially enhances the performance of the AD9703.

An on-board reference eases design effort by eliminating the need for external circuits. Input registers and a differential clock input minimize glitch impulse and clock feedthrough. The unit is housed in a 24-pin DIP and will operate in both 10KH and 100K ECL systems. The AD9703 dissipates 1.1 watts and is truly a "graphics ready" device.

Analog Devices' advanced technology produced the first hybrid converters which included composite capabilities; the AD9703 is one of a series of monolithic graphics DACs made by the company. (The AD9701 is an 8-bit 250MHz device; the AD9702 is a triple 4-bit 125MHz converter.)

SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

Model	AD9703BD/BW		AD9703TD/TDB
ABSOLUTE MAXIMUM RATINGS	Lower	Upper	
Supply Voltages			
Pins 10 and 14 (V_S)	−6V	0V	*
Power Dissipation (Continuous)	1.75W		*
Logic Inputs	$-V_S$	Ground	*
Current Set	1mA	4.5mA	*
Output Current	30mA		*
Setup	$-V_S$	Ground	*
Temperature			
Operating (Case)	−25°C to +85°C		−55°C to +125°C
Storage	−65°C to +150°C		*
Junction Temperature	+175°C		*
Lead (Soldering, 10sec)	+300°C		*

Parameter	Units	AD9703BD/BW	AD9703TD/TDB
RESOLUTION	Bits	8	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Voltage (Adjustable)	mV	2.5	*
Currrent (Adjustable)	µA	67	*
ACCURACY (GS = Gray Scale; FS = Full Scale)			
Differential Linearity	±% GS, max	0.2	*
Integral Linearity	±% GS, max	0.2	*
Zero Offset Voltage (Initial)	±mV, max	2	*
Monotonicity		Guaranteed	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C	7	*
Gain	ppm/°C	170	*
Zero Offset	µV/°C	5	*
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT			
Full-Scale Settling to 0.4% GS[1]	ns	6	*
Update Rate[2]	MHz (Guaranteed)	300 (250)	*
Rise Time (10%–90% GS)	ns (max)	1.2 (1.75)	*
Fall Time (10%–90% GS)	ns (max)	1.1 (1.75)	*
Glitch Impulse	pV-s (max)	45 (55)	*
Clock Feedthrough	mV	<10	*
DIGITAL DATA INPUTS			
Logic Compatability		100K and 10KH ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V	−0.9	*
"0"	V	−1.7	*
Loading (Each Bit)		5pF and 50kΩ to −5.2V	*
STROBE INPUT(S)			
Logic Compatibility		100K and 10KH ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V	−0.9	*
"0"	V	−1.7	*
Loading		5pF and 50kΩ to −5.2V	*
Setup Time (Data)	ns	0	*
Hold Time (Data)	ns, min	1	*
Propagation Delay (Strobe Input to Analog Output)	ns	1.2	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS			
Logic Compatibility		100K and 10KH ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V	−0.9	*
"0"	V	−1.7	*
Loading		5pF and 50kΩ to −5.2V	*
SPEED PERFORMANCE – CONTROL INPUTS[1]			
Settling Time to 10% of Final Value for:			
10% Bright	ns	6	*
Reference White	ns	6	*
Composite Sync	ns	6	*
Composite Blanking	ns	6	*
SETUP CONTROL			
Ground	mV (IRE Units)	0 (0)	*
Open	mV (IRE Units)	53.25 (7.5)	*
1k to −5.2V	mV (IRE Units)	71 (10)	*
−5.2V	mV (IRE Units)	142 (20)	*

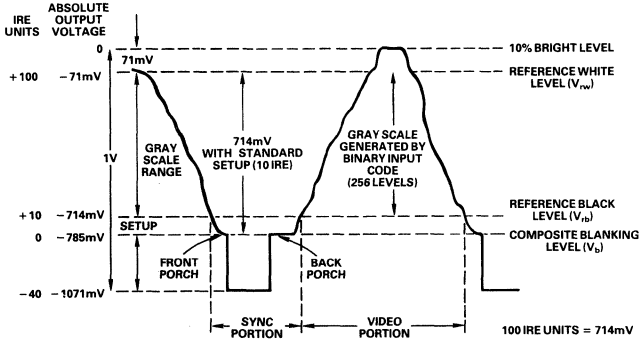
Parameter	Units	AD9703BD/BW	AD9703TD/TDB
ANALOG OUTPUT			
GS Current[3]	mA	0 to −17	*
GS Voltage[4,5]	mV	0 to −637.5	*
Compliance[6]	V	−1.2 to +3	*
Internal Impedance	Ω	800	*
REFERENCE WHITE[7]			
Current			
Logic "1"	mA	Normal Operation	*
Logic "0"	mA	0 or −1.9	*
Voltage			
Logic "1"	mV	Normal Operation	*
Logic "0"	mV	0 or −71.25	*
10% BRIGHT[8]			
Current			
Logic "1"	mA	−1.9	*
Logic "0"	mA	0	*
Voltage			
Logic "1"	mV	−71	*
Logic "0"	mV	0	*
COMPOSITE SYNC[8,9]			
Current			
Logic "1"	mA	0	*
Logic "0"	mA	−7.6	*
Voltage			
Logic "1"	mV	0	*
Logic "0"	mV	−285	*
COMPOSITE BLANKING[8,9]			
(Assumes Setup is Open, Which is Equivalent to 7.5 IRE Units)			
Current			
Logic "1"	mA	0	*
Logic "0"	mA	−1.42	*
Voltage			
Logic "1"	mV	0	*
Logic "0"	mV	−53.25	*
VOLTAGE REFERENCE TOLERANCE			
(Deviation from Nominal −1.26V)	mV (max)	±20 (±60)	*
POWER REQUIREMENTS			
−5.2V (Min/Max = −4.5V/−5.45V)	mA (max)	210 (275)	*
Power Supply Rejection Ratio	mV/V	1	*
Power Dissipation	W (max)	1.1 (1.43)	*
TEMPERATURE RANGE	°C	−25 to +85	−55 to +125
THERMAL RESISTANCE[10]			
Junction to Air, θ_{JA} (Free Air)	°C/W	29	*
Junction to Case, θ_{JC}	°C/W	12	*
MTBF[11]			
Mean Time Between Failures	Hours	3.04×10^5	*
PACKAGE OPTIONS[12]			
D-24		AD9703BD AD9703BW	AD9703TD AD9703TDB

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{COMPOSITE SYNC}}$	24	DIGITAL GROUND
2	BIT 1	23	$\overline{\text{10\% BRIGHT}}$
3	BIT 2	22	$\overline{\text{COMPOSITE BLANK}}$
4	BIT 3	21	SETUP
5	BIT 4	20	CURRENT SET
6	BIT 5	19	ANALOG GROUND
7	BIT 6	18	I_{OUT}
8	BIT 7	17	COMPENSATION
9	BIT 8	16	$\overline{I_{OUT}}$
10	−5.2V	15	DIVIDER GROUND
11	$\overline{\text{REFERENCE WHITE}}$	14	−5.2V
12	$\overline{\text{STROBE}}$	13	STROBE

NOTE: CONNECT PINS 15, 19, AND 24 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.

NOTES
[1]Inherent register delay (50% points) is not included.
[2]Maximum update rate limited by input registers.
[3]FS Current = GS Current + Video Functions = 30mA maximum.
[4]LSB value of 2.5mV used for calibration. This causes Gray Scale output to be 637.5mV, rather than 643mV of idealized composite waveform shown elsewhere. $I_{OUT} = 4(1.26/R_{SET})$ when $R_{SET} = 300\Omega$.
[5]Output voltages based on $R_{LOAD} = 75\Omega \| R_{TERMINATION} = 75\Omega$.
[6]Divider Ground (Pin 15) must be at +3V for +3V compliance. (See text.)
[7]The effect on the analog output of logic "0" at Reference White input (Pin 11) depends on signal at 10% Bright input (Pin 23).
[8]10% Bright, Composite Sync, and Composite Blanking outputs add to analog output.
[9]Composite Sync and/or Composite Blanking signals override input registers. Neither of these signals should be operated simultaneously with Reference White.
[10]Maximum junction temperature is +175°C.
[11]Calculated using MIL HNBK-217; Ground; Fixed; +25°C Ambient.
[12]See Section 14 for package outline information.
Specifications subject to change without notice.



Idealized Composite Output Waveform

USING AD9703 AS RASTER SCAN D/A

Refer to the block diagram of the AD9703. The digital input bits applied to Pins 2 through 9 represent the Gray Scale value of the 256 (2^8) discrete levels between Reference Black and Reference White in a composite video signal.

The (true and complementary) analog outputs are also affected by the 100K or 10KH ECL levels at the control inputs, and the level (in IRE units) of the control signal at SETUP, Pin 21.

STROBE and $\overline{\text{STROBE}}$ signal pulses clock the input registers to remove time skew from the digital input bits and minimize discontinuities or "glitches" in the analog output.

In the idealized waveform, the full-scale output is −643mV. Normal fullscale output of the AD9703, however, is −637.5mV because of using 2.5mV for the weight of the LSB during calibration of the unit. Both values are well within the tolerances of the output and the RS-170 standard.

The internal voltage reference shown in the block diagram is a bandgap type and eliminates the need for external circuits. Other benefits of the internal precision reference include superior power supply rejection and gain tempco.

The value of the internal reference is 1.26 volts (±20mV; ±60mV max), and that knowledge can be combined with information on Gray Scale output current to determine the value of the R_{SET} resistor. R_{SET} is approximately four times the value of the number which results when the reference voltage is divided by the Gray Scale current. Expressed mathematically:

$$R_{SET} \approx 4\left(\frac{1.26V}{I_{OUT}GS}\right)$$

Assume the user's desired Gray Scale voltage is 637.5mV; and the external load is 37.5 ohms. Dividing 637.5mV by 37.5 ohms sets Gray Scale current at 17mA. The reference voltage of 1.26 volts divided by 17mA, and multiplied by four, determines a (rounded) R_{SET} value of 296 ohms.

Full-scale current is Gray Scale current **plus** the video functions and is specified for a **total** of 30mA.

Using the value of R_{SET}, the user can calculate Gray Scale output voltage within 15% with the equation:

$$V_{OUT} = 4\left(\frac{1.26V}{R_{SET}}\right)\left(R_{LOAD} \parallel R_{INTERNAL}\right)$$

The resistance of the internal ladder is 800 ohms in parallel with the load resistor and is included in the above example.

APPLICATION HINTS

In the Specifications, data on $\overline{\text{COMPOSITE BLANKING}}$ assume the SETUP connection is open, equivalent to 7.5 IRE Units. Pin 20 connected to ground is equivalent to 0 IRE Units. Connecting to −5.2V through a 1kΩ resistor is 10 units; connecting to −5.2V directly is 20 units.

For some applications, additional by-pass capacitors for the −5.2V supply lines may be desirable. In addition to the ceramic 0.1μF capacitors shown on the block diagram, tantalum capacitors of 3.3 − 10μF may enhance the converter's performance in some designs. All by-pass capacitors should be connected as closely as possible to the supply pins of the converter.

If the user is driving a lighter load than a coaxial cable and needs lower power dissipation, doubling the value of R_{SET} halves the output current but still maintains useable drive.

Ground pins 15, 19, and 24 are normally connected together and to ground; these connections should also be made close to the unit. Divider Ground must be referenced to +3V to obtain +3V compliance. Figure 1 shows a method of doing this.

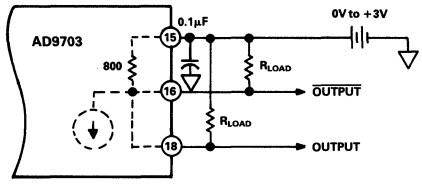


Figure 1. Connection for Positive Voltage Compliance

Values of up to +3V might be applied. Assume R_{LOAD} is 75 ohms. With +1V applied, the output would be ±1V; at +3V, the output would be +1V to +3V.

USING AD9703 AS STANDARD D/A

The AD9703 can also be used as a standard D/A converter capable of remarkable performance; it is attractive for that application because of the low value of glitch impulse.

Refer to Figure 2.

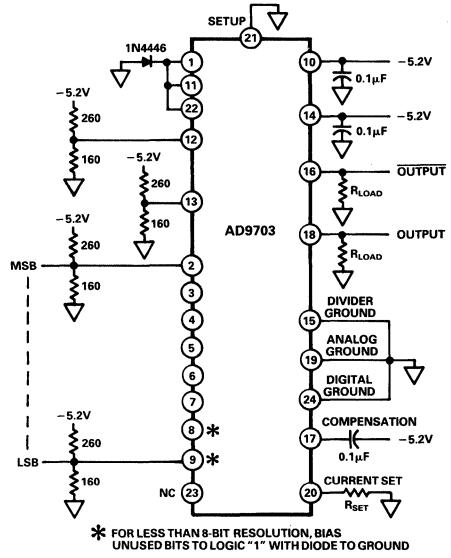


Figure 2. AD9703 as Standard D/A

As a standard D/A, unused control inputs are tied to ground via a diode as shown on Pins 1, 11, and 22. The $\overline{\text{10\% Bright}}$ input (Pin 23) is left open; and Setup (Pin 21) is tied directly to ground. For less than eight bits of data, unused input pins are also grounded via diodes.

ORDERING INFORMATION

Three versions of the AD9703 are available, all in ceramic DIP packages. The non-hermetic AD9703BW and hermetic AD9703BD operate over a temperature range of −25°C to +85°C. The hermetic AD9703TD and mil-processed AD9703TDB are for −55°C to +125°C.

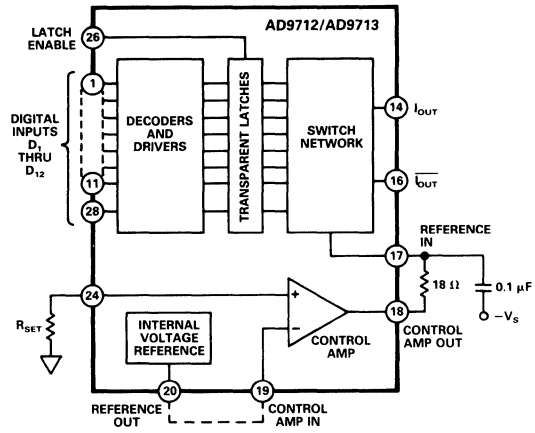
12-Bit, 100 MSPS D/A Converters

AD9712/AD9713

FEATURES
100 MSPS Update Rate
ECL/TTL Compatibility
Low Glitch Impulse: 100 pV–s
Fast Settling: 30 ns to ±1 LSB
Low Power: 700 mW

APPLICATIONS
ATE
Signal Reconstruction
Arbitrary Waveform Generators
Digital Synthesizers
Signal Generators

AD9712/AD9713 FUNCTIONAL BLOCK DIAGRAM

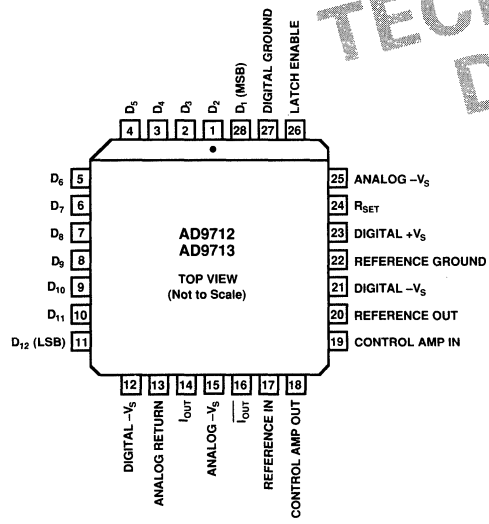


GENERAL DESCRIPTION

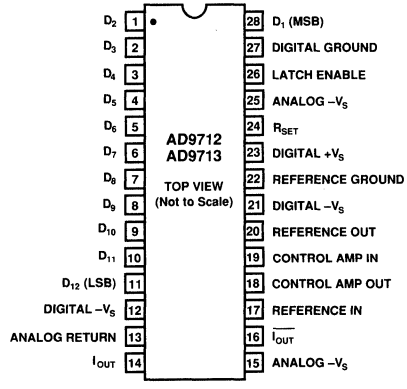
The AD9712 and AD9713 are 12-bit, high speed digital-to-analog converters constructed in an advanced oxide isolated bipolar process. The AD9712 is an ECL-compatible device featuring update rates of 100 MSPS minimum; the TTL-compatible AD9713 will update at 80 MSPS minimum.

Designed for direct digital synthesis, waveform reconstruction, and high resolution imaging applications, both devices feature low glitch impulse of 100 pV-s; and fast settling times of 30 ns to ±1 LSB. Both units are characterized for dynamic performance, and have excellent harmonic suppression.

The AD9712 and AD9713 are available in 28-pin plastic DIPs and PLCCs, with an operating temperature range of 0 to +70°C. Contact the factory for availability of military-grade devices.



PLCC Pinout Designations



Plastic DIP Pinout Designations (Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) (AD9713 Only) . . . . . +6 V
Negative Supply Voltage ($-V_S$)
(AD9712 and AD9713) . . . . . −7 V
DAC Outputs to ANALOG RETURN . . . . . +0.5 V to −2 V
Digital Input Voltages (D_1–D_{12}, LATCH ENABLE)
AD9712 . . . . . 0 V to $-V_S$
AD9713 . . . . . 0 V to $+V_S$
Internal Reference Output Current . . . . . 500 μA
Control Amplifier Input Voltage Range . . . . . 0 V to −4 V
Control Amplifier Output Current . . . . . ±2.5 mA
REFERENCE IN Voltage Range . . . . . −3.7 V to $-V_S$
Analog Output Current (I_{OUT} or $\overline{I_{OUT}}$) . . . . . 30 mA
Operating Temperature Range
AD9712JN/JP/KN/KP. . . . . 0 to +70°C
AD9713JN/JP/KN/KP. . . . . 0 to +70°C
Maximum Junction Temperature[2] . . . . . +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($-V_S$ = −5.2 V; $+V_S$ = +5 V (AD9713 Only); CONTROL AMP IN = −1.2 V (external); R_{SET} = 7.5 kΩ, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9712JN/JP/KN/KP Min	Typ	Max	AD9713/JN/JP/KN/KP Min	Typ	Max	Units
RESOLUTION			12			12			Bits
DC ACCURACY									
Differential Nonlinearity (J)	+25°C	I		0.75	1.0		0.75	1.0	LSB
	Full	VI			2.0			2.0	LSB
Differential Nonlinearity (K)	+25°C	I		0.6	0.75		0.6	0.75	LSB
	Full	VI			1.0			1.0	LSB
Integral Nonlinearity (J)	+25°C	I		1.5	2.0		1.5	2.0	LSB
("Best Fit" Straight Line)	Full	VI			3.0			3.0	LSB
Integral Nonlinearity (K)	+25°C	I		1.0	1.5		1.0	1.5	LSB
("Best Fit" Straight Line)	Full	VI			2.5			2.5	LSB
Monotonicity	Full	IV		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR									
Zero-Scale Offset Error	+25°C	I		0.5	1.5		0.5	1.5	μA
	Full	VI			5.0			5.0	μA
Full-Scale Gain Error[3]	+25°C	I		4.0	8.5		4.0	8.5	%
	Full	VI			11.0			11.0	%
Offset Drift Coefficient	+25°C	V		0.03			0.03		μA/°C
REFERENCE/CONTROL AMP									
Internal Reference Voltage	+25°C	I	−1.13	−1.26	−1.39	−1.13	−1.26	−1.39	V
	Full	I	−1.11		−1.41	−1.11		−1.41	V
Internal Reference Voltage Drift	Full	V		440			440		μV/°C
Amplifier Input Impedance	+25°C	V		50			50		kΩ
Amplifier Bandwidth	+25°C	V		300			300		kHz
REFERENCE INPUT[4]									
Reference Input Impedance	+25°C	V		3			3		kΩ
Reference Multiplying Bandwidth[5]	+25°C	V		40			40		MHz
OUTPUT PERFORMANCE									
Full-Scale Output Current[6]	+25°C	V		20.48			20.48		mA
Output Compliance Range	+25°C	IV	−1.2		+3	−1.2		+3	V
Output Resistance	+25°C	IV	2.0	2.5	3.0	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C	V		30			30		pF
Output Update Rate[7]	+25°C	IV	100	110		80	90		MSPS
Output Settling Time (t_{ST})[8]									
Current Settling	+25°C	V		30			30		ns
Voltage Settling (R_L = 50 Ω)	+25°C	V		30			30		ns
Output Propagation Delay (t_{PD})[9]	+25°C	V		8			11		ns
Glitch Impulse[10]	+25°C	V		100			100		pV-s
Output Slew Rate[11]	+25°C	V		400			400		V/μs
Output Rise Time[11]	+25°C	V		3			3		ns
Output Fall Time[11]	+25°C	V		2			2		ns

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter (Conditions)	Temp	Test Level	AD9712JN/JP/KN/KP Min	Typ	Max	AD9713JN/JP/KN/KP Min	Typ	Max	Units
DIGITAL INPUTS									
Logic "1" Voltage	Full	VI	−1.0	−0.8		2.0			V
Logic "0" Voltage	Full	VI		−1.7	−1.5			0.8	V
Logic "1" Current	Full	VI			20			20	μA
Logic "0" Current	Full	VI			10			600	μA
Input Capacitance	+25°C	V		3			3		pF
Input Setup Time (t_S)[12]	+25°C	V		3			3		ns
Input Hold Time (t_H)[13]	+25°C	V		3			3		ns
Latch Pulse Width (t_{LPW}) (Transparent)	+25°C	V		2.5			4		ns
AC LINEARITY[14]									
Spurious-Free Dynamic Range	+25°C	V		−60			−55		dBc
POWER SUPPLY[15]									
Positive Supply Current (+5.0 V)	+25°C	I					10	20	mA
	Full	VI						23	mA
Negative Supply Current (−5.2 V)	+25°C	I		130	160		135	165	mA
	Full	VI			170			175	mA
Nominal Power Dissipation	+25°C	V		676			726		mW
Power Supply Rejection Ratio (PSRR)[16]	+25°C	I		50	110		50	110	μA/V

For applications assistance, phone Computer Labs Division at (919) 668-9511

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances: 28-pin plastic DIP θ_{JA} = 42°C/W; θ_{JC} = 7°C/W; 28-pin PLCC θ_{JA} = 48°C/W; θ_{JC} = 10°C/W.

[3]Measured as error of the ratio of full-scale current to current through R_{SET} (160 μA nominal); ratio is nominally 128.

[4]Full-scale variations among devices are more severe when driving REFERENCE IN directly.

[5]Frequency at which a 3 dB reduction in output of DAC is observed; R_L = 50 Ω; 50% modulation at midscale.

[6]Based on $I_{FS} = 128 (V_{REF}/R_{SET})$ when using internal amplifier.

[7]Output settling to 0.1%.

[8]Measured at midscale transition, to ±0.024%.

[9]Measured from falling edge of LATCH ENABLE signal to 50% point of full-scale transition.

[10]Glitch impulse combines the absolute value of positive and negative transitions operating in latched mode.

[11]Measured with R_L = 50 Ω and DAC operating in latched mode.

[12]Data must remain stable prior to falling edge of LATCH ENABLE signal for specified time.

[13]Data must remain stable after rising edge of LATCH ENABLE signal for specified time.

[14]Update rate ≤50 MSPS; output frequency = 5 MHz.

[15]Supply voltages should remain stable within ±5% for normal operation.

[16]Measured at ±5% of $+V_S$ (AD9713 only) and $-V_S$ (AD9712 or AD9713) using external reference.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

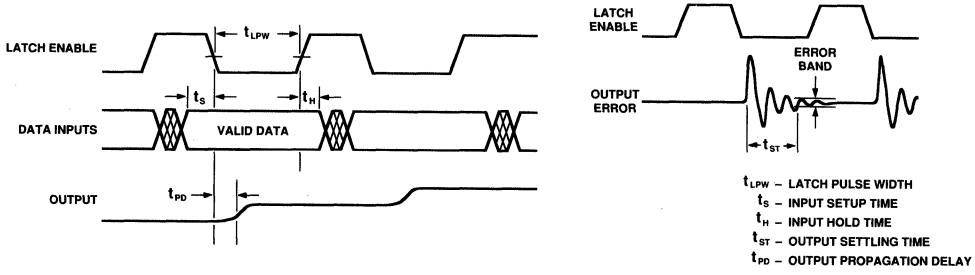
ORDERING INFORMATION

Part. No.	Description	Package Options*
AD9712JN	ECL-Compatible Plastic DIP	N-28
AD9712JP	ECL-Compatible PLCC	P-28A
AD9712KN	ECL-Compatible Plastic DIP	N-28
AD9712KP	ECL-Compatible PLCC	P-28A
AD9713JN	TTL-Compatible Plastic DIP	N-28
AD9713JP	TTL-Compatible PLCC	P-28A
AD9713KN	TTL-Compatible Plastic DIP	N-28
AD9713KP	TTL-Compatible PLCC	P-28A

*See Section 14 for package outline information.

AD9712/AD9713 PIN DESCRIPTIONS

Pin No.	Name	Function
1–10	D_2–D_{11}	Ten of twelve digital input bits.
11	D_{12} (LSB)	Least Significant Bit (LSB) of digital input word.
12	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
13	ANALOG RETURN	Analog ground return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
14	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1."
15	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
16	$\overline{I_{OUT}}$	Complementary analog current output; zero scale output occurs with digital inputs at all "1."
17	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 18). Direct line to DAC current switch network. Voltage changes at this point have a direct effect on the full-scale output. Full-scale current output = 128 (Reference voltage/R_{SET}) when using internal amplifier.
18	CONTROL AMP OUT	Normally connected to REFERENCE IN (Pin 17). Output of internal control amplifier, which provides a temperature compensated drive level to the current switch network.
19	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 20) if not connected to external reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier.
20	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 19). Internal voltage reference, nominally −1.26 V.
21	DIGITAL $-V_S$	One of two negative digital supply pins; nominally −5.2 V.
22	REFERENCE GROUND	Ground return for the internal voltage reference and amplifier.
23	DIGITAL $+V_S$	Positive digital supply pin; used only on the AD9713; nominally +5 V.
24	R_{SET}	Connection for external resistance reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier.
25	ANALOG $-V_S$	One of two negative analog supply pins; nominally −5.2 V.
26	LATCH ENABLE	Transparent latch control line.
27	DIGITAL GROUND	Digital ground return.
28	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.



AD9712/AD9713 Timing Diagram

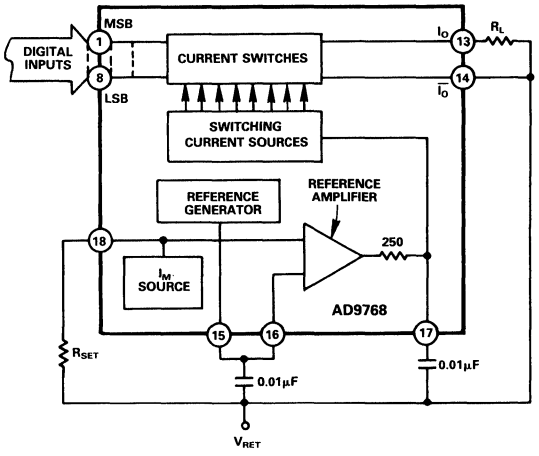
Ultrahigh Speed IC D/A Converter

AD9768

FEATURES
5ns Settling Time
100MHz Update Rate
20mA Output Current
ECL-Compatible
40MHz Multiplying Mode

APPLICATIONS
Raster Scan & Vector Graphic Displays
High Speed Waveform Generation
Digital VCOs
Ultra-Fast Digital Attenuators

AD9768 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept 8 bits of ECL-level digital input voltages and convert them into analog signals at update rates as high as 100MHz. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at multiplying bandwidths as high as 40MHz.

An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20mA, which corresponds to a 1-volt drop across a 50Ω load, or ±1 volt across 100Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage ($V_{REF} \approx -1.26V$) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} with digital "1" at all inputs is calculated with the equation:

$$I_{OUT} = 4 \times \frac{V_{RET} - V_{REF}}{R_{SET}}$$

The setting resistor R_{SET} and the output load resistor should both have low temperature coefficients. A complementary $\overline{I_{OUT}}$ is also provided.

The reference voltage source is a modified bandgap type and is nominally −1.26 volts. This reference supply requires no external regulation. To reduce the possibility of noise generation and/or instability, pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900pF, although a 0.01μF ceramic chip capacitor is recommended.

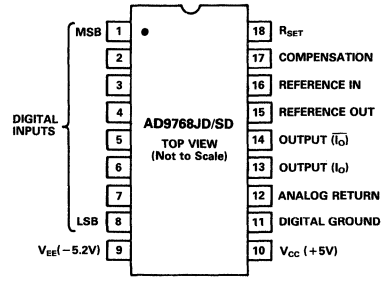
The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.

SPECIFICATIONS (typical @ +25°C under following conditions unless otherwise noted; nominal digital input levels; nominal power supplies; $R_L = 50\Omega$; $R_{SET} = 220\Omega$; $V_{RET} = 0V$)

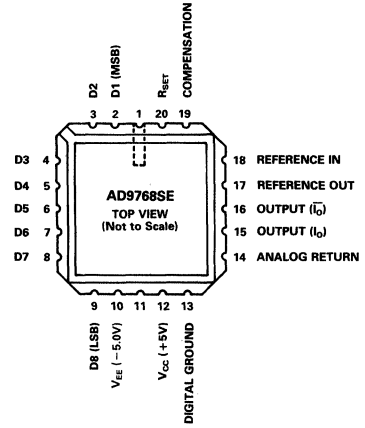
Parameter	Units	AD9768SJD/SD/SE
RESOLUTION (FS = FULL SCALE)	Bits	8
LSB WEIGHT (CURRENT)	μA	78
ACCURACY[1]		
Differential Nonlinearity	±% FS	0.2
Integral Nonlinearity	±% FS	0.2
Monotonicity		Guaranteed
Zero Offset (Initial)	μA	60
TEMPERATURE COEFFICIENTS		
Zero Offset	ppm/°C	1.5
Reference Voltage (−1.26V)	ppm/°C	70
DIGITAL DATA INPUTS		
Logic Compatibility		ECL
Logic Voltage Levels "1" =	V	−0.9
"0" =	V	−1.7
Coding	Binary (BIN) = Unipolar Out Offset Binary (OBN) = Bipolar Out	
OUTPUT		
Current (Unipolar) FS	mA (max)	2 to 20 (30)
I_{OUT} (@ Pin 13)		
All Digital "1" Input	mA	20
All Digital "0" Input	mA	0
$\overline{I_{OUT}}$ (@ Pin 14)		
All Digital "1" Input	mA	0
All Digital "0" Input	mA	20
Compliance	V (Pin 13)	−0.7 to +3.0
	V (Pin 14)	−1.1 to +3.0
Impedance	Ω (±15%)	750
SPEED PERFORMANCE		
Settling Time (to 0.2% FS)[2]	ns	5
Slew Rate	V/μs	400
Update Rate	MHz	100
Rise Time	ns	1.8
Glitch Energy	pV-sec	200
REFERENCE		
Internal, Monolithic[3]	V	−1.26
External, Variable[4]		
Voltage-Multiplying Mode	V (max)	0 to −1.1 (−2)
Current-Multiplying Mode	mA (max)	0 to −5 (−7.5)
VOLTAGE-MULTIPLYING MODE[4] (See Figure 2)		
V_M Range (at Pin 16)	V	±0.5
V_M Center	V	−0.6
Resistance (at Pin 16)	kΩ	800
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8: −0.1 V_M Input = 0mA I_{OUT} −1.1 V_M Input = 0mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: −0.1 V_M Input = 1mA I_{OUT} −1.1 V_M Input = 20mA I_{OUT}	
Large Signal Bandwidth (−3dB Point)	kHz	250
CURRENT-MULTIPLYING MODE (See Figure 4)		
I_M Range (at Pins 17 & 18)	mA	0 to 5
Resistance (at Pin 18)	Ω	160
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8: 1mA I_M Input = 0mA I_{OUT} 5mA I_M Input = 0mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: 1mA I_M Input = 4mA I_{OUT} 5mA I_M Input = 20mA I_{OUT}	
Large Signal Bandwidth (−3dB Point)	MHz	40
POWER REQUIREMENTS		
−5.2V ±0.25	mA (max)	66 (70)
+5.0V ±0.25	mA (max)	14 (15)
Power Dissipation	mW (max)	410 (430)
Power Supply Sensitivity[5]	%/%	0.07
TEMPERATURE RANGES[6]		
Operating	°C	−30 to +115
Storage	°C	−55 to +150
THERMAL RESISTANCE[7]		
Junction to Air, θ_{JA} (Free Air)	°C/W	90
Junction to Case, θ_{JA}	°C/W	20
PACKAGE OPTIONS[8]		
Ceramic (D-18)		AD9768JD AD9768SD
LCC (E-20A)		AD9768SE

For applications assistance, phone Computer Labs Division at (919) 668-9511

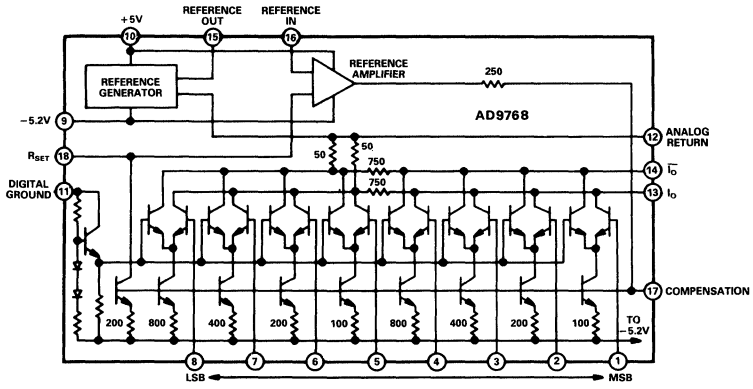
AD9768JD/SD PIN CONNECTIONS



AD9768SE PIN CONNECTIONS



NOTES
[1]Relative to FS, including linearity (within voltage compliance limits).
[2]Worst case settling time; includes FS and Most Significant Bit (MSB) transitions.
[3]Applies when operating AD9768 as standard D/A.
[4]Based on R_L = 50 ohms; R_{SET} = 220 ohms; V_{RET} = 0V.
[5]1% change in either power supply voltage causes 0.07% change in analog output.
[6]Case temperature.
[7]Maximum junction temperature 125°C.
[8]See Section 14 for package outline information.
Specifications subject to change without notice.



AD9768SD D/A Schematic

THEORY OF OPERATION

Refer to the AD9768SD schematic.

The transistors pictured on the bottom of the diagram, connected to paired transistors in the middle of the schematic, are current sources which are always "on". The paired transistors are differential current switches, designed to steer current from the current sources to either pin 13 (I_O) or pin 14 ($\overline{I_O}$).

Digital inputs applied to pins 1-8 determine which transistors will be operating in each pair and establish what current will flow at pins 13 and 14.

The transistor on the extreme left of the schematic is a base reference for the paired current switches and is used to assure the switches will be centered around an ECL voltage swing. The diodes connected to the base of this transistor are temperature compensation devices for the base reference circuit.

There are three different current sources in the AD9768 D/A. The eight transistors shown on the bottom of the schematic are structured as two identical groups of four current sources, each of which is binarily weighted. The MSB group, comprised of the four on the right, is connected to the LSB group through a 15:1 current divider made up of two 50Ω and two 750Ω resistor networks. The geometry of the AD9768 guarantees the binary weighing ratios among the 100, 200, 400 and 800 resistors in each emitter circuit are correct.

The resistor values which are shown indicate the ratios among the resistors, and not their nominal values.

The third current source is a single transistor, pictured in the lower left portion of the schematic with its collector connected to pin 18 R_{SET}. Its function is to help establish the base voltage on the eight current sources; it works in conjunction with the external R_{SET} resistor selected by the user of the AD9768, and the reference amplifier. Current flowing through this transistor is referred to as I_M in the figures and test.

When the AD9768 is operating as a conventional current-output D/A converter, I_M develops a voltage across R_{SET} which is one of the inputs to the on-board reference amplifier shown in the schematic. The other input to this amplifier is the on-chip reference voltage of −1.26 volts.

The output of the reference amplifier adjusts the current-source base reference voltage at pin 17; this, in turn, adjusts the value of I_M in the single-transistor current source and causes it to develop a voltage across R_{SET} which maintains pin 18 at the −1.26 volts of the on-chip reference supply.

To maintain good stability in the internal loop reference amplifier, a ceramic chip capacitor with a nominal value of 0.01μF should be connected to pin 17 COMPENSATION; minimum recommended value for this capacitor is 3900pF.

The temperature coefficient of the load resistor (R_L) can affect the performance of the AD9768 D/A converter, as it can with any current-output converter. The design and use of the AD9768 and its dependence on an external R_{SET} resistor, however, make it sensitive also to the tempco of R_{SET}. The user is cautioned to select R_L and R_{SET} resistors which have low temperature coefficients.

DIGITAL GROUND (pin 11) and ANALOG RETURN (pin 12) are normally connected together; this connection should be made as close as possible to the device case to minimize possible noise problems. The AD9768 D/A is similar to any other high-speed, high performance device: optimum use requires careful attention to all design details, including the layout of the circuit in which the converter is used.

CONVENTIONAL AD9768

Refer to Figure 1, Conventional AD9768SD.

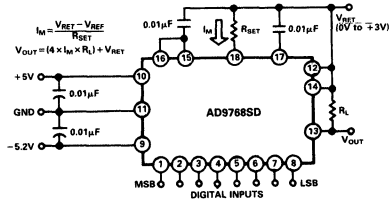


Figure 1. Conventional AD9768SD

The output current of the AD9768 appears at pin 13 (I_O) and develops a voltage across the load resistor R_L which is based on:

A. I_M (the current flowing through the single-transistor source discussed above)
B. Value of R_L

I_M is a function of the return voltage (V_{RET}), the reference voltage (V_{REF}), and the value of R_{SET}; all of these are selected by the user for his application. The necessary equations for calculating precise values for each are part of Figure 1. As indicated,

the voltage drop across R_L is added to the return voltage; the resulting voltage is the total V_{OUT} of the converter.

VOLTAGE MULTIPLYING MODE

In addition to its use as an ultra-high speed current output D/A converter, the AD9768 can also be used as a two-quadrant multiplying D/A in either a voltage mode or a current mode.

Refer to Figure 2, Multiplying AD9768 (Voltage Mode).

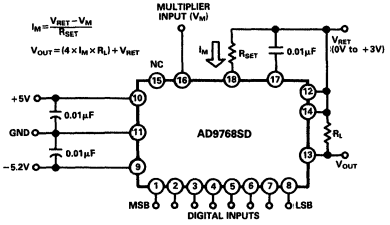


Figure 2. Multiplying AD9768 (Voltage Mode)

When operating in this mode, the analog output of the AD9768 is influenced by the digital inputs and an external multiplying voltage (V_M) applied to pin 16 REFERENCE IN, which takes the place of the internal reference used when the D/A is operating in a conventional manner.

The value of I_M flowing through R_{SET} is set by the voltage of V_{RET} minus the multiplying voltage (V_M), divided by R_{SET}; the amount of this current is part of the equation which establishes the analog output (V_{OUT}) of the AD9768 and is chosen by the user for his application. As it is when operating the D/A in a conventional fashion, V_{RET} can be any value between 0 volts and +3 volts. V_M (for purposes of discussion here) is some negative voltage and can be varied over a range which is approximately 1 volt peak-to-peak.

If the load resistor (R_L) has a value of 50 ohms, if R_{SET} has a value of 220 ohms, and if V_{RET} is 0V, the center of the V_M voltage will be −0.6V; and it can vary from −0.1V to −1.1V. Typically, the frequency of these variations has an upper limit of 250kHz when operating in the voltage multiplying mode; that frequency is the 3dB point of the bandwidth of the internal reference amplifier.

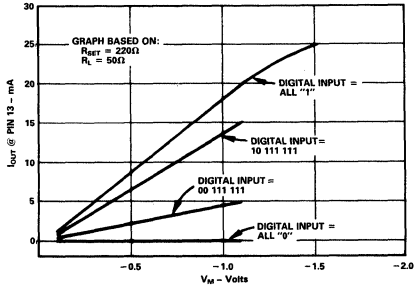


Figure 3. I_{OUT} vs. Multiplying Voltage

The combined effects of variations in V_M and changes in digital input values are shown in Figure 3, I_{OUT} vs. Multiplying Voltage. In this illustration, the ordinate of the graph is expressed in terms of milliamps of I_{OUT} current at pin 13. V_{OUT}, of course, will be a function of the value of R_L chosen by the user.

The negative value of V_M on the horizontal axis is shown starting at approximately −0.1V, rather than 0V, because the AD9768 must have some small value of voltage applied to perform a multiplying function. For the conditions shown in the figure, output current starts to become nonlinear at approximately 20mA because of the maximum 30mA output drive capabilities of the device. Different values for R_{SET} and R_L would alter the point where limiting first appears.

CURRENT MULTIPLYING MODE

The AD9768 D/A converter can be operated at markedly higher multiplying rates when operated in a current-multiplying mode, as contrasted with the voltage-multiplying mode. Refer to Figure 4, Multiplying AD9768SD (Current Mode).

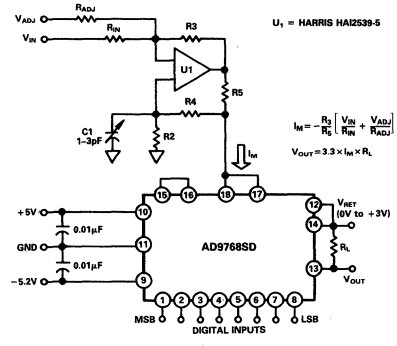


Figure 4. Multiplying AD9768SD (Current Mode)

In this mode, the internal reference amplifier and its inherent frequency limitations are replaced by a current source comprised of U1 and associated circuits. These circuits supply a unipolar current I_M which is one-fourth the full-scale output current (with digital "1" applied to all inputs) and set current flow through the load resistor.

V_{IN} is some voltage chosen by the user for his particular application; the value of this voltage is based in part on the size of the load resistor and the 0mA to 5mA range of I_M. V_{IN} can have frequency components as high as 40MHz. V_{ADJ} and R_{ADJ} provide an offset adjustment to compensate for the dc component of V_{IN} to assure I_M is always a unipolar current between 0mA and 5mA. The values of the required voltages and resistors can be calculated using the equations which are part of Figure 4.

Refer to Figure 5, I_{OUT} vs. Multiplying Current.

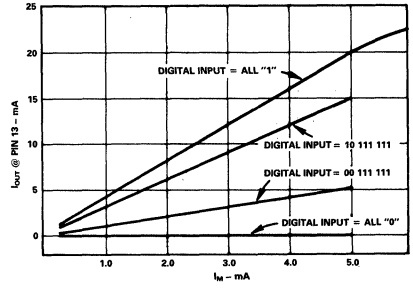


Figure 5. I_{OUT} vs. Multiplying Current

As shown, I_M can vary over the range of 0mA to 5mA; a value of approximately 0.3mA may be the practical lower limit because of nonlinearities at extremely small current levels. These changes in I_M are combined with variations in digital inputs, producing complex changes in the output current (at pin 13) and in V_{OUT}. The "rounding" of the current curve in the graph is the result of I_{OUT} approaching the 30mA maximum drive capabilities of the AD9768 and needs to be taken into account to assure optimum performance in the selected application.

ANALOG DEVICES

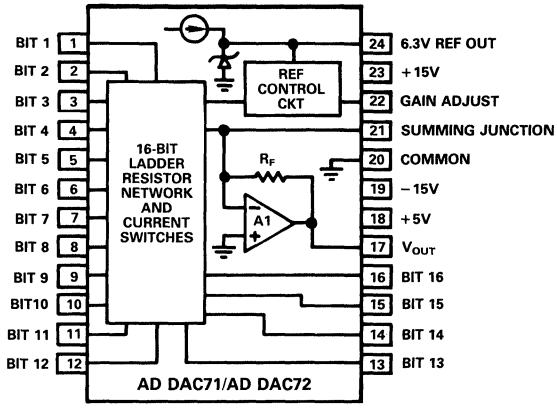
High Resolution 16-Bit D/A Converters

AD DAC71/AD DAC72*

FEATURES

16-Bit Resolution
±0.003% Maximum Nonlinearity
Low Gain Drift ±7ppm/°C
0 to +70°C Operation (AD DAC71, AD DAC71H, AD DAC72C)
−25°C to +85°C Operation (AD DAC72)
Current and Voltage Models Available
Improved Second-Source
Low Cost

AD DAC71/AD DAC72 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD DAC71 and AD DAC72 are high resolution 16-bit hybrid IC digital-to-analog converters including reference, scaling resistors and output amplifier (V models).

The devices offer outstanding accuracy, including maximum linearity error of 0.003% at room temperature and maximum gain drifts of 15ppm/°C (AD DAC71, AD DAC71H, AD DAC72C) and 7ppm/°C (AD DAC72). This performance is possible due to the innovative design, using proprietary monolithic D/A converter chips. Laser-trimmed thin film resistors provide the linearity and wide temperature range for guaranteed monotonicity.

The AD DAC71 and AD DAC72 digital inputs are TTL-compatible. Coding is complementary straight binary (CSB) for unipolar output versions and complementary offset binary (COB) for bipolar output versions.

All versions are packaged in a 24-pin metal DIP. The AD DAC71, AD DAC71H and AD DAC72C are specified for operation from 0 to +70°C, and the AD DAC72 is specified from −25°C to +85°C. The AD DAC71H, AD DAC72 and AD DAC72C are supplied in hermetically-sealed packages.

The AD DAC71 and AD DAC72 are intended to serve as improved second sources to DAC71 and DAC72 devices from other manufacturers.

PRODUCT HIGHLIGHTS

1. The AD DAC71 and AD DAC72 provide 16-bit resolution with 0.003% linearity error.
2. The proprietary chips used in the hybrid design provide excellent stability over temperature and improved reliability.
3. Unipolar and bipolar current and voltage output versions are available to fill a wide range of system requirements.
4. The AD DAC71 and AD DAC72 are improved second source replacements for DAC71 and DAC72 devices from other manufacturers.

***Covered by Patent Numbers: 3,978,473; RE28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326; 4,213,806; 4,136,349.**

SPECIFICATIONS (@ T_A = +25°C, rated power supplies unless otherwise noted)

MODEL	AD DAC71/AD DAC71H MIN	TYP	MAX	AD DAC72C MIN	TYP	MAX	AD DAC72 MIN	TYP	MAX	UNITS
DIGITAL INPUTS										
Resolution		16			16			16		Bits
Logic Levels (TTL-Compatible)[1]										
Logical "1"	+2.4		+5.5	+2.4		+5.5	+2.4		+5.5	V dc
Logical "0"	+0		+0.4	+0		+0.4	+0		+0.4	V dc
ACCURACY[2]										
Linearity Error at 25°C			±0.003			±0.003			±0.003	% of FSR[3]
Gain Error[4], Voltage		±0.01	±0.1		±0.05	±0.15		±0.05	±0.15	%
Current		±0.05	±0.25		±0.05	±0.25		±0.05	±0.25	%
Offset Error[4], Voltage, Unipolar		±0.1	±2.0		±0.1	±2.0		±0.1	±2.0	mV
Voltage, Bipolar			±5.0			±10.0			±10.0	mV
Current, Unipolar			±1.0			±1.0			±1.0	μA
Current, Bipolar			±5.0			±5.0			±5.0	μA
Monotonicity Temp. Range (14-Bits)	0		+50	0		+50	0		+70	°C
DRIFT (Over Specified Temp. Range)										
Total Bipolar Drift (includes gain, offset, and linearity drift)										
Voltage										
T_{min} to 25°C		±7	±15		±7	±15		±5	±19	ppm of FSR/°C
25°C to T_{max}		±7	±15		±7	±15		±5	±11	ppm of FSR/°C
Current										
T_{min} to T_{max}		±15			±15			±10		ppm of FSR/°C
TOTAL ERROR OVER TEMP. RANGE[5]										
Voltage, Unipolar										
T_{min} to +25°C			±0.083			±0.083			±0.100	% of FSR
+25°C to T_{max}			±0.083			±0.083			±0.072	% of FSR
Voltage, Bipolar										
T_{min} to +25°C			±0.071			±0.071			±0.100	% of FSR
+25°C to T_{max}			±0.071			±0.071			±0.072	% of FSR
Current, Unipolar (T_{min} to T_{max})			±0.23			±0.23			±0.24	% of FSR
Bipolar (T_{min} to T_{max})			±0.23			±0.23			±0.24	% of FSR
TEMPERATURE COEFFICIENTS										
Gain										
Voltage										
T_{min} to +25°C			±15			±15			±15	ppm of FSR/°C
+25°C to T_{max}			±15			±15			±7	ppm of FSR/°C
Current		±15			±15			±10		ppm of FSR/°C
Offset										
Voltage, Unipolar		±1	±2		±1	±2		±1	±2	ppm of FSR/°C
Bipolar			±10			±10			±8	ppm of FSR/°C
Current, Unipolar			±1			±1			±1	ppm of FSR/°C
Bipolar		±15			±15			±10		ppm of FSR/°C
Differential Linearity over Temperature			±2			±2			±1	ppm of FSR/°C
Linearity Error over Temperature			±2			±2			±1	ppm of FSR/°C
SETTLING TIME										
Voltage Models (to ±0.003% of FSR)										
Output: 20V Step		5	10		5	10		5	10	μs
1LSB Step[6]		3	5		3	5		3	5	μs
Slew Rate		20			20			20		V/μs
Current Models (to ±0.003% of FSR)[7]										
Output: 2mA step 10Ω to 100Ω Load			1			1			1	μs
1kΩ Load			3			3			3	μs
Switching Transient		500			500			500		mV
ANALOG OUTPUT										
Voltage Models										
Ranges–CSB		0 to +10			0 to +10			0 to +10		V
COB		±10			±10			±10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges–CSB		0 to −2			0 to −2			0 to −2		mA
COB		±1			±1			±1		mA
Output Impedance–Unipolar		6.0			6.0			6.0		kΩ
Bipolar		3.0			3.0			3.0		kΩ
Compliance	−1.5		+10	−1.5		+10	−1.5		+10	V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	6.0	6.3	6.6	V
Maximum External Current[8]			±3			±3			±3	mA
Temp. Coeff. of Drift			±10			±10			±5	ppm/°C
POWER SUPPLY SENSITIVITY										
Unipolar Offset										
±15V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S
+5V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S
Bipolar Offset										
±15V dc		±0.0004			±0.0004			±0.0004		% of FSR/% V_S
+5V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S

MODEL	AD DAC71/AD DAC71H MIN	TYP	MAX	AD DAC72C MIN	TYP	MAX	AD DAC72 MIN	TYP	MAX	UNITS
POWER SUPPLY SENSITIVITY (Continued)										
Gain										
±15V dc		±0.001			±0.001			±0.001		% of FSR/% V_S
+5V dc		±0.0005			±0.0005			±0.0005		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS										
DAC71/72	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	V dc
Supply Drain, +15V dc (no load)		10	20		10	20		10	20	mA
−15V dc (no load)		30	55		30	55		30	55	mA
+5V dc (logic supply)		10	20		10	20		10	20	mA
TEMPERATURE RANGE										
Specification	0		+70	0		+70	−25		+85	°C
Operating (double above Drift Specs)	−25		+85	−25		+85	−55		+100	°C
Storage	−55		+100	−55		+100	−55		+110	°C

NOTES
[1]Adding external CMOS hex buffers CD4009A will provide 15V dc CMOS input compatibility.
[2]Accuracy is specified when using internal feedback resistors. Current output specifications are guaranteed at the voltage output of an external op amp using the internal feedback resistor.
[3]FSR means Full Scale Range and is 20V for ±10V range.
[4]Adjustable to zero with external trim potentiometer.
[5]With gain and offset errors adjusted to zero at 25°C.
[6]LSB is for 14-bit resolution.
[7]Parameter guaranteed, not tested.
[8]Maximum with no degradation of specification.

Specifications subject to change without notice.

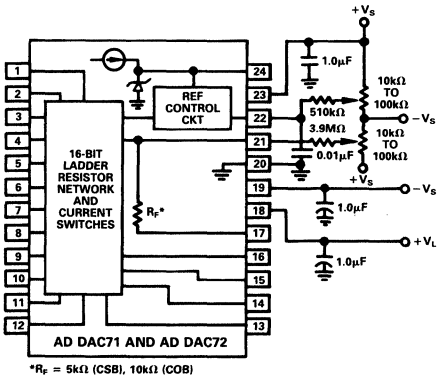


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

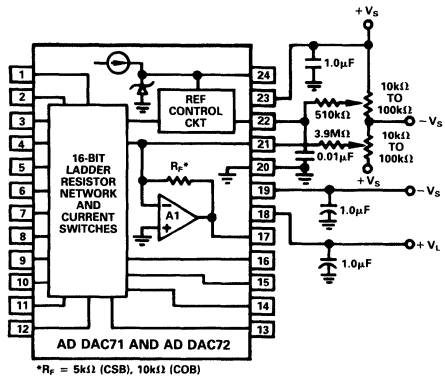


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

ORDERING GUIDE

Model	Output	Input Code	Temperature Range	Seal	Package Option*
AD DAC71–COB–I	Current	Comp. Offset Binary	0 to +70°C	Polymer	DH-24D
AD DAC71–CSB–I	Current	Comp. Straight Binary	0 to +70°C	Polymer	DH-24D
AD DAC71H–COB–I	Current	Comp. Offset Binary	0 to +70°C	Hermetic	DH-24D
AD DAC71H–CSB–I	Current	Comp. Straight Binary	0 to +70°C	Hermetic	DH-24D
AD DAC72C–COB–I	Current	Comp. Offset Binary	0 to +70°C	Hermetic	DH-24D
AD DAC72C–CSB–I	Current	Comp. Straight Binary	0 to +70°C	Hermetic	DH-24D
AD DAC72–COB–I	Current	Comp. Offset Binary	−25°C to +85°C	Hermetic	DH-24D
AD DAC72–CSB–I	Current	Comp. Straight Binary	−25°C to +85°C	Hermetic	DH-24D
AD DAC71–COB–V	Voltage	Comp. Offset Binary	0 to +70°C	Polymer	DH-24D
AD DAC71–CSB–V	Voltage	Comp. Straight Binary	0 to +70°C	Polymer	DH-24D
AD DAC71H–COB–V	Voltage	Comp. Offset Binary	0 to +70°C	Hermetic	DH-24D
AD DAC71H–CSB–V	Voltage	Comp. Straight Binary	0 to +70°C	Hermetic	DH-24D
AD DAC72C–COB–V	Voltage	Comp. Offset Binary	0 to +70°C	Hermetic	DH-24D
AD DAC72C–CSB–V	Voltage	Comp. Straight Binary	0 to +70°C	Hermetic	DH-24D
AD DAC72–COB–V	Voltage	Comp. Offset Binary	−25°C to +85°C	Hermetic	DH-24D
AD DAC72–CSB–V	Voltage	Comp. Straight Binary	−25°C to +85°C	Hermetic	DH-24D

*See Section 14 for package outline information.

PRESERVING THE ACCURACY OF THE AD DAC71 AND AD DAC72

A great deal of care must be exercised when using high resolution converters such as the AD DAC71 and AD DAC72. Since one least significant bit of a 16-bit converter (LSB) represents an analog voltage of only 153 microvolts out of a 10V scale, normally negligible error sources become significant. Series resistances of connectors and wiring can be major contributors, as can thermocouple effects. Figure 3 illustrates the connections for voltage output versions of the AD DAC71 and AD DAC72.

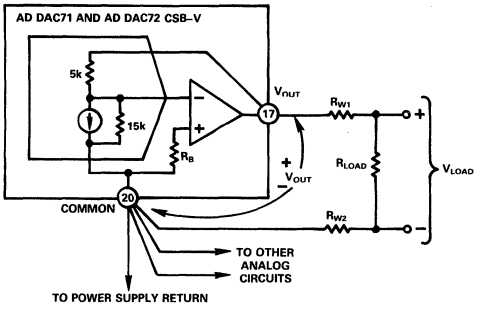


Figure 3. AD DAC71 and AD DAC72 Connection Diagram (Voltage Models)

In this circuit, the analog output voltage is accurately developed between pin 17 and pin 20 of the DAC. The voltage measured at the load will be inaccurate if there is significant resistance in the wiring (and any connectors) between the DAC and the load. If the load resistance is constant, the effects of R_{W1} and R_{W2} can be treated as a simple gain error, and can be trimmed out. However, if R_L is variable, then R_{W1} and R_{W2} should be reduced to a value less than $\frac{R_{L\ MIN}}{2^{16}}$. This will reduce the effect of the wiring resistances to a gain error of less than 1LSB. The AD DAC71 and AD DAC72 are rated at an output current of 5mA which translates to a minimum load resistance of 2kΩ. Thus wiring resistances should be held to a maximum of 30 milliohms. This corresponds to approximately six inches of #28 wire or a six inch long printed circuit track 0.050 inches wide.

The current output versions of the AD DAC71 and AD DAC72 use an external operational amplifier to convert the output current to an output voltage. The recommended configuration is shown in Figure 4. Notice that this configuration permits the voltage at the load to the sensed remotely. The resistance (R_{W1}) of the lead connecting the load to the internal feedback resistor introduces a gain error equal to $\frac{R_{W1}}{R_{LOAD}}$, independent of R_{LOAD} and R_{W2}. The error contributed by R_{W3} depends upon where the output is measured. If the output is measured between the top of R_{LOAD} and pin 20 of the DAC, no error results since R_{W3} effectively becomes part of the load resistance.

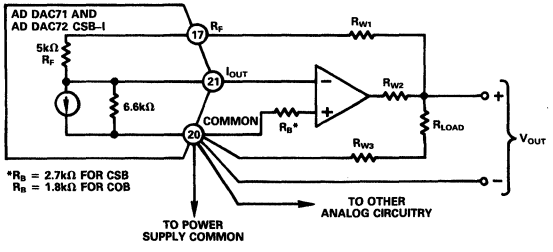


Figure 4. Connections for AD DAC71 and AD DAC72 Current Output Versions

In applications where R_{W3} is large or large currents flow in R_{W3}, it is necessary to use remote sensing as shown in Figure 5.

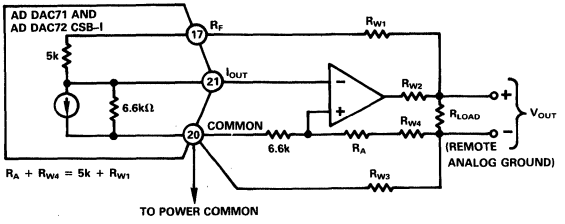


Figure 5. Use of Output Amplifier as Subtractor for Remote Ground Sensing

This circuit uses the output amplifier as a subtractor stage. Any spurious voltage developed across R_{W3} becomes a common mode voltage and its error contribution is reduced by the common mode rejection of the op amp.

In the circuits of both Figure 4 and Figure 5, R_{W2}'s effect is negligible since it is inside the loop of the amplifier. If current boosting is required in order to drive heavy loads, a suitable booster stage can be inserted between the amplifier's output and the load. Since the loop is closed from the load end, offsets and other errors induced by the booster are eliminated.

It is also important to minimize thermocouple effects in circuitry using the AD DAC71 and AD DAC72. Recalling that 1LSB of a 16 bit, 10 volt scale converter is only 153 microvolts, a stray uncompensated thermocouple can introduce several LSBs of offset in response to minor changes in ambient temperature. Any part of a circuit which includes a junction between two dissimilar metals forms a thermocouple. Such junctions include connectors, sockets, and any soldered connections. The solution to thermocouple errors is to insure that every junction is cancelled by an identical, but opposite, junction at the same temperature. While this is often automatically accomplished (for example, in a connector carrying both signal and return leads), careful attention should be given to the physical layout of circuits using the AD DAC71 and AD DAC72.

Another source of signal degradation in high-resolution converter circuits is magnetically-coupled interference from stray fields. Signal and return leads should be arranged in a way which minimizes both length and the total cross-section area of the loop. Of course, high resolution circuits should be located as far as possible from any sources of electromagnetic interference, including power transformers, digital logic and electromechanical devices.

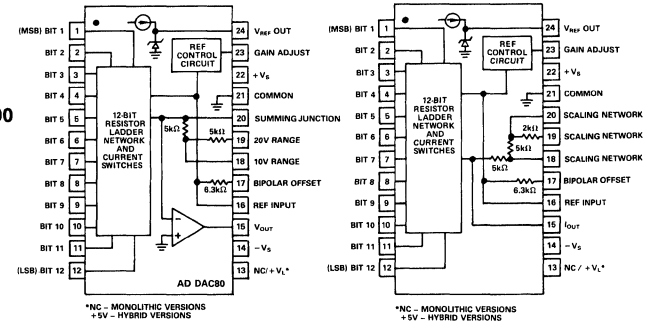
Complete Low Cost 12-Bit D/A Converters

AD DAC80/AD DAC85/AD DAC87

FEATURES

- Single Chip Construction
- On-Board Output Amplifier
- Low Power Dissipation: 300mW
- Monotonicity Guaranteed over Temperature
- Guaranteed for Operation with ±12V Supplies
- Improved Replacement for Standard DAC80, DAC800 HI-5680
- High Stability, High Current Output Buried Zener Reference
- Laser Trimmed to High Accuracy: ±1/2LSB max Nonlinearity
- Low Cost Plastic Packaging

AD DAC80 SERIES FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD DAC80 Series is a family of low cost 12-bit digital-to-analog converters with both a high stability voltage reference and output amplifier combined on a single monolithic chip. The AD DAC80 Series is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional DAC80 devices. Innovative circuit design reduces the total power consumption to 300mW which not only improves reliability but also improves long term stability.

The AD DAC80 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface Zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete Zener references.

The AD DAC80 Series is available in three performance grades and two package types. The AD DAC80 is specified for use over the 0 to +70°C temperature range and is available in both plastic and ceramic DIP packages. The AD DAC85 and AD DAC87 are available in hermetically sealed ceramic packages and are specified for the −25°C to +85°C and −55°C to +125°C temperature ranges.

PRODUCT HIGHLIGHTS

1. The AD DAC80 series of D/A converters directly replaces all other devices of this type with significant increases in performance.
2. Single chip construction and low power consumption provides the optimum choice for applications where low cost and high reliability are major considerations.
3. The high speed output amplifier has been designed to settle within 1/2LSB for a 10V full scale transition in 2.0μs, when properly compensated.
4. The precision buried Zener reference can supply up to 2.5mA for use elsewhere in the application.
5. The low TC binary ladder guarantees that all units are monotonic over the specified temperature range.
6. System performance upgrading is possible without redesign.

PRODUCT OFFERING

Analog Devices has developed a number of technologies to support products within the data acquisition market. In serving the market new products are implemented with the technology best suited to the application. The DAC80 series of products was first implemented in hybrid form and now it is available in a single monolithic chip. We will provide both the hybrid and monolithic versions of the family so that in existing designs changes to documentation or product qualification will not have to be done. Specifications and ordering information for both versions are delineated in this data sheet.

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC80 Min	AD DAC80 Typ	AD DAC80 Max	AD DAC85 Min	AD DAC85 Typ	AD DAC85 Max	AD DAC87 Min	AD DAC87 Typ	AD DAC87 Max	Units
TECHNOLOGY		Monolithic			Monolithic			Monolithic		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD		–			–			–		Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)			250			250			250	µA
I_{IL} (V_{IL} = 0.8V)			100			100			100	µA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI			±1/2			±1/2			±1/2	LSB[1]
CCD										LSB
T_A @ T_{min} to T_{max}		±1/4	±1/2		±1/4	±1/2		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C										
CBI			±3/4			±3/4			±3/4	LSB
CCD										LSB
T_A @ T_{min} to T_{max}			±3/4			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1	±0.2		±0.1	±0.2	%FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05	±0.1		±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	−25		+85	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20			±20			±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15		±0.12	±0.2		±0.18	±0.3	% of FSR
Bipolar		±0.06	±0.10		±0.08	±0.12		±0.14	±0.24	% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±4	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	µs
with 5kΩ Feedback		2	3		2	3		2	3	µs
For LSB Change		1			1			1		µs
Slew Rate	10			10			10			V/µs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		µs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
Current Models										
Ranges – Unipolar	−1.96	−2.0	−2.04	−1.96	−2.0	−2.04	−1.96	−2.0	−2.04	mA
– Bipolar	±0.96	±1.0	±1.04	±0.96	±1.0	±1.04	±0.96	±1.0	±1.04	mA
Output Impedance – Bipolar	2.5	3.2	4.1	2.5	3.2	4.1	2.5	3.2	4.1	kΩ
– Unipolar	5.0	6.6	8.2	5.0	6.6	8.2	5.0	6.6	8.2	kΩ
Compliance	−2.5		+10	−2.5		+10	−2.5		+10	V
Internal Reference Voltage (V_R)	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	±20		±10	±20			±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable			±0.002			±0.002			±0.002	% of FSR/%V_S
±12V ±5%			±0.002			±0.002			±0.002	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15			±15			±15		V
Range										
Analog Supplies	±11.4[7]		±16.5	±11.4[7]		±16.5	±11.4[7]		±16.5	V
Logic Supplies									V	
Supply Drain										
+12, +15V		5	10		5	10		5	10	mA
−12, −15V		14	20		14	20		14	20	mA
+5V										mA
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating	−25		+85	−55		+125	−55		+125	°C
Storage	−25		+125	−65		+150	−65		+150	°C

NOTES

[1]Least Significant Bit.

[2]Adjustable to zero with external trim potentiometer.

[3] FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.

[4]Gain and offset errors adjusted to zero at +25°C.

[5]C_F = 0, see Figure 1a.

[6]Maximum with no degradation of specification, must be a constant load.

[7]A minimum of ±12.3V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC80 Min	AD DAC80 Typ	AD DAC80 Max	AD DAC85C Min	AD DAC85C Typ	AD DAC85C Max	AD DAC85 Min	AD DAC85 Typ	AD DAC85 Max	Units
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD			3			3			3	Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		+250			+250			+250		μA
I_{IL} (V_{IL} = 0.8V)		−100			−100			−100		μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI		±1/4	±1/2			±1/2			±1/2	LSB[1]
CCD		±1/8	±1/4			±1/4			±1/4	LSB
T_A @ T_{min} to T_{max}		±1/4	±1/2		±1/4	±1/2		±1/2	±1/2	LSB
Differential Linearity Error @ +25°C										
CBI		±1/2	±3/4		±1/2			±1/2		LSB
CCD		±1/4	±1/2		±1/2			±1/2		LSB
T_A @ T_{min} to T_{max}			±1			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1			±0.1		%FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05			±0.05		%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	0		+70	−25		+85	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20							ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15							% of FSR
Bipolar		±0.06	±0.10							% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±5	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3		±1			±1		ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩFeedback		5			5			5		μs
with 5kΩFeedback		3			3			3		μs
For LSB Change		1.5			1.5			1.5		μs
Slew Rate	10	15			20			20		V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR										
for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD		±10			+10			+10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges – Unipolar		−2.0			−2.0			−2.0		mA
– Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance – Bipolar		3.2			3.2			3.2		kΩ
– Unipolar		6.6			6.6			6.6		kΩ
Compliance		−1.5, +10			−2.5, +10			−2.5, +10		V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	±20		±10	±20		±10	±20	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable		±0.002			±0.002			±0.002		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14		±16	±14.5		±15.5	±14.5		±15.5	V
Logic Supplies	+4.5		+16	+4.5		+15.5	+4.5		+15.5	V
Supply Drain[7]										
+15V		10	20		15	20		15	20	mA
−15V		20	35		25	30		25	30	mA
+5V		8	20		15	20		15	20	mA
TEMPERATURE RANGE										
Specification	0		+70	0		+70	−25		+85	°C
Operating	−25		+85	−25		+85	−55		+125	°C
Storage	−55		+130	−65		+150	−65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3] FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_F = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5mA load.
Specifications subject to change without notice.

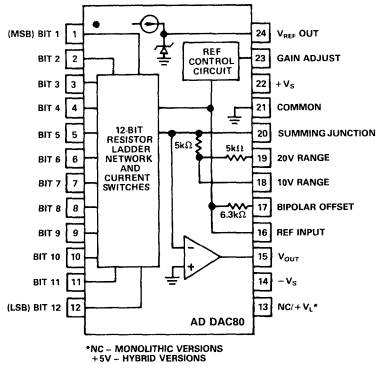
SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC85LD			AD DAC85MIL			AD DAC87			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD		–			–			–		Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		+250			+250			+250		μA
I_{IL} (V_{IL} = 0.8V)		−100			−100			−100		μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI			±1/2			±1/2		±1/4	±1/2	LSB[1]
CCD		–			–			–		LSB
T_A @ T_{min} to T_{max}			±1/2			±3/4			±3/4	LSB
Differential Linearity Error @ +25°C										
CBI		±1/2			±1/2			±1/2		LSB
CCD										LSB
T_A @ T_{min} to T_{max}			±1			±1			±1	LSB
Gain Error[2]		±0.1			±0.1			±0.1	±0.2	%FSR[3]
Offset Error[2]		±0.05			±0.05			±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	−25		+85	−55		+125	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)		–			–			±15	±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		–			–			±0.13	±0.30	% of FSR
Bipolar		–			–			±0.12	±0.24	% of FSR
Gain										
Including Internal Reference			±10			±20		±10	±25	ppm of FSR/°C
Excluding Internal Reference								±5	±10	ppm of FSR/°C
Unipolar Offset		±1			±2			±1	±3	ppm of FSR/°C
Bipolar Offset			±5			±10		±5	±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩFeedback		5			5			5		μs
with 5kΩFeedback		3			3			3		μs
For LSB Change		1.5			1.5			1.5		μs
Slew Rate		20			20			20		V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges – Unipolar		−2.0			−2.0			−2.0		mA
– Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance – Bipolar		3.2			3.2		2.5	3.2	4.1	kΩ
– Unipolar		6.6			6.6		5.0	6.6	8.2	kΩ
Compliance		−2.5, +10			−2.5, +10			−1.5, +10		V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	20		10	20		±5	10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable		±0.002			±0.002			±0.002	±0.003	%FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14.5		±15.5	±14.5		±15.5	±13.5		±16.5	V
Logic Supplies	+4.5		+15.5	+4.5		+15.5	+4.5		+16.5	V
Supply Drain[7]										
+15V		15	20		15	20		10	20	mA
−15V		25	30		25	30		20	30	mA
+5V		15	20		15	20		10	20	mA
TEMPERATURE RANGE										
Specification	−25		+85	−55		+125	−55		+125	°C
Operating	−55		+125	−55		+125	−55		+125	°C
Storage	−55		+125	−55		+120	−65		+150	°C

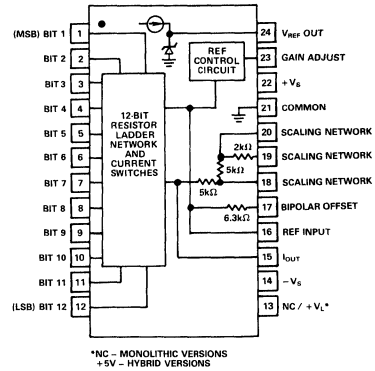
NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3] FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_F = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5mA load.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to Power Ground . . . . . 0V to +18V
$-V_S$ to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 1 to 12) to Power Ground . . . −1.0V to +7V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out . . . . . Indefinite short to power ground or $+V_S$



Voltage Model Functional Diagram and Pin Configuration



Current Model Functional Diagram and Pin Configuration

ORDERING GUIDE

Model	Input Code	Output Mode	Technology	Temperature Range	Linearity Error	Package Options*
AD DAC80N-CBI-V	Binary	Voltage	Monolithic	0 to +70°C	±1/2LSB	N-24
AD DAC80D-CBI-V	Binary	Voltage	Monolithic	0 to +70°C	±1/2LSB	D-24
AD DAC80D-CBI-I	Binary	Current	Monolithic	0 to +70°C	±1/2LSB	D-24
AD DAC85D-CBI-V	Binary	Voltage	Monolithic	−25°C to +85°C	±1/2LSB	D-24
AD DAC87D-CBI-V	Binary	Voltage	Monolithic	−55°C to +125°C	±1/2LSB	D-24
AD DAC80-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80Z-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80Z-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC80Z-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC80Z-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85C-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC85C-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	DH-24A
AD DAC85-CBI-V	Binary	Voltage	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85-CBI-I	Binary	Current	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85LD-CBI-V	Binary	Voltage	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85LD-CBI-I	Binary	Current	Hybrid	−25°C to +85°C	±1/2LSB	DH-24A
AD DAC85MIL-CBI-V	Binary	Voltage	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC85MIL-CBI-I	Binary	Current	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC85C-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85C-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	DH-24A
AD DAC85-CCD-V	Binary Coded Decimal	Voltage	Hybrid	−25°C to +85°C	±1/4LSB	DH-24A
AD DAC85-CCD-I	Binary Coded Decimal	Current	Hybrid	−25°C to +85°C	±1/4LSB	DH-24A
AD DAC87-CBI-V	Binary	Voltage	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A
AD DAC87-CBI-I	Binary	Current	Hybrid	−55°C to +125°C	±1/2LSB	DH-24A

*See Section 14 for package outline information.

DIGITAL INPUT CODES

The AD DAC80 Series accepts complementary digital input code in binary (CBI) format. The CBI model may be connected by the user for anyone of three complementary codes: CSB, COB or CTC.

Digital Input		Analog Output		
MSB	LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
0 0 0 0 0 0 0 0 0 0 0 0		+ Full Scale	+ Full Scale	− 1LSB
0 1 1 1 1 1 1 1 1 1 1 1		+ 1/2 Full Scale	Zero	− Full Scale
1 0 0 0 0 0 0 0 0 0 0 0		Mid-Scale	− 1LSB	+ Full Scale
1 1 1 1 1 1 1 1 1 1 1 1		Zero	− Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table I. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected. Linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than its maximum specification, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ± 1/2LSB means that the output voltage step sizes can range from 1/2LSB to 1 1/2LSB when the input changes from one adjacent input state to the next.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC80 model at the lowest operating temperature, + 25°C and the highest operating temperature; 2) calculating the gain error with respect to the + 25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The maximum change in offset is referenced to the offset at + 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output Models. Three settling times are specified to ± 0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 . . . 1 1 to 1 0 0 0 . . . 0 0), the point at which the worst case settling time occurs. The settling time characteristic depends on the compensation capacitor selected, the optimum value is 25pF as shown in Figure 1a.

Current Output Models. Two settling times are specified to ± 0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage ranges of ± 1V and 0 to − 2V.

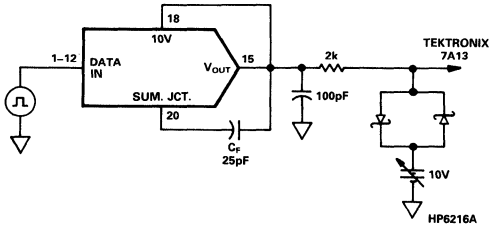


Figure 1a. Voltage Model Settling Time Circuit

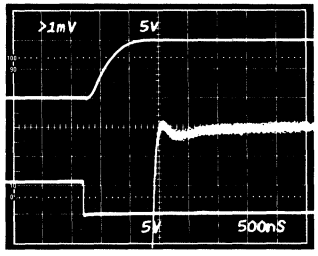


Figure 1b. Voltage Model Settling Time C_F = 25pF

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive or negative supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ± 1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations. All gain adjustments should be made under constant load conditions.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 2. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input codes, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried zener diode reference element results in superior wide temperature range performance. The gain setting resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

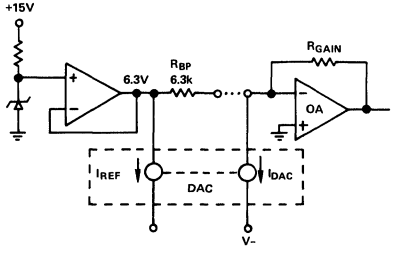


Figure 2. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ± 1/2LSB max and the differential linearity error of ± 3/4LSB max guarantee monotonic performance over the specified range. It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 3. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see Figure 2) to generate a current which, exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 3. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD DAC80 this error is held to 10ppm/°C max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full scale drift, but again is held to 10ppm/°C max.

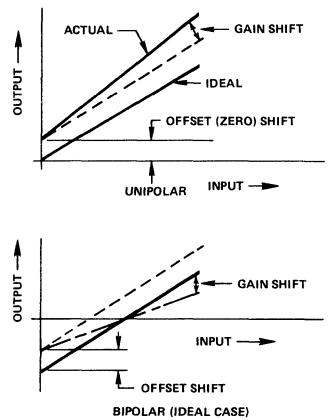


Figure 3. Unipolar and Bipolar Drifts

Using the AD DAC80 Series

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams. These capacitors (1μF electrolytic recommended) should be located close to the AD DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the AD DAC80 to prevent noise pickup. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 6 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01μF ceramic capacitor should be connected from this pin to common to prevent noise pickup.

Offset Adjustment. For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is −10V. See Table II for corresponding codes.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

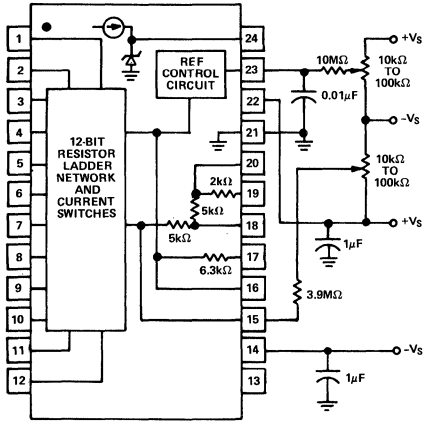


Figure 4. External Adjustment and Voltage Supply Connection Diagram, Current Model

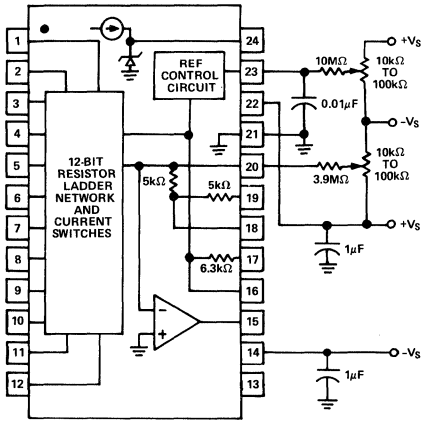


Figure 5. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

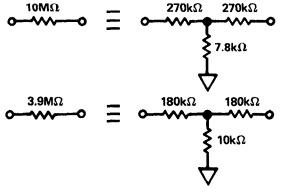


Figure 6. Equivalent Resistances

Digital Input		Analog Output			
12 Bit Resolution		Voltage*		Current	
MSB	LSB	0 to +10V	±10V	0 to −2mA	±1mA
0 0 0 0 0 0 0 0 0 0 0 0		+9.9976V	+9.9951V	−1.9995mA	−0.9995mA
0 1 1 1 1 1 1 1 1 1 1 1		+5.0000V	0.0000V	−1.0000mA	0.0000mA
1 0 0 0 0 0 0 0 0 0 0 0		+4.9976V	4.88mV	−0.9995mA	+0.0005mA
1 1 1 1 1 1 1 1 1 1 1 1		0.0000V	−10.0000V	0.0000mA	−1.00mA
1LSB		2.44mV	−0.0049V	0.488μA	0.488μA

*To obtain values for other binary ranges 0 to +5V range: divide 0 to +10 values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

Table II. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC80 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 7).

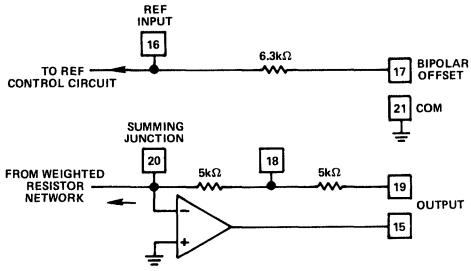


Figure 7. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 4 microseconds for a 10kΩ feedback resistor; 3 microseconds for a 5kΩ feedback resistor when using the compensation capacitor shown in Figure 1.

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 8 and 9. External R_{LS} resistors are required to produce exactly 0 to −2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the AD DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

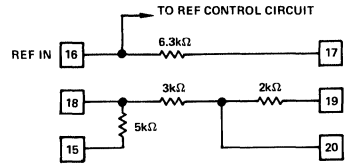


Figure 8. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to −2V. These resistors (R_{LI}: TCR = 20ppm/°C) are an integral part of the AD DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C + the TCR of R_L (or R_F) to the total drift.

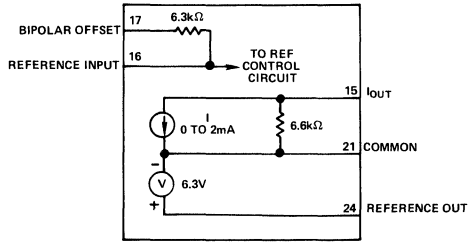


Figure 9. AD DAC80 Current Model Equivalent Output Circuit

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections-Voltage Model AD DAC80

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	R_{LI} Connections			Reference	Bipolar Offset	
				Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R_{LS}
CSB	0 to −2V	0.968kΩ	210Ω	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)
COB or CTC	±1V	1.2kΩ	249Ω	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)
CCD	0 to ±2V	3kΩ	N/A	N.C.	21	N.C.	24	N.C.	N/A

Table IV. Current Model/Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 10 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{6.6k \times R_L}{6.6k + R_L}\right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = −2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to −2V. With $R_{LS} = 0$, $V_{OUT} = -1.69V$.

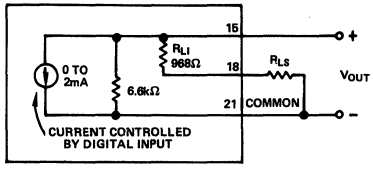


Figure 10. Equivalent Circuit AD DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 3.22k}{R_L + 3.22k}\right)$$

Where R_L max = 11.18kΩ

and V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

DRIVING AN EXTERNAL OP AMP

The current model AD DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 12,

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the AD DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model AD DAC80 provides output voltage ranges the

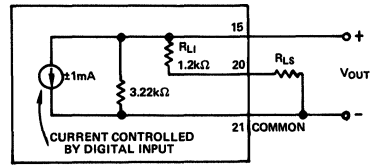


Figure 11. AD DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

same as the voltage model AD DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 12.

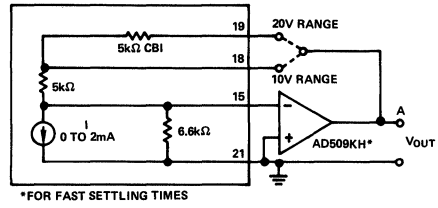


Figure 12. External Op Amp–Using Internal Feedback Resistors

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 13). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

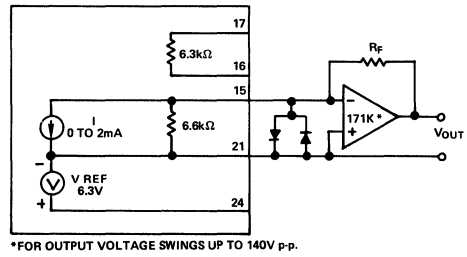


Figure 13. External Op Amp–Using External Feedback Resistors

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	A	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24

Table V. External Op Amp Voltage Mode Connections

CMOS 66MHz Monolithic 256×24 Color Palette RAM-DAC

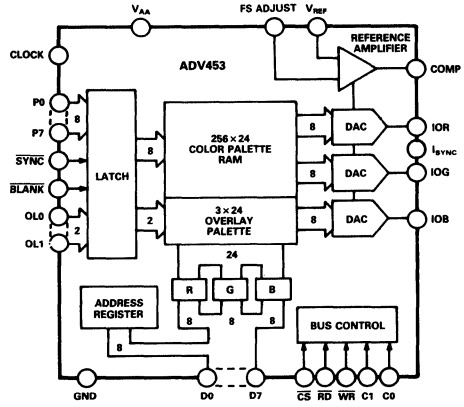
ADV453

FEATURES
66MHz Pipelined Operation
Triple 8-Bit D/A Converters
256×24 Color Palette RAM
3×24 Overlay Registers
RS-343A/RS-170 Compatible Outputs
+5V CMOS Monolithic Construction
40-Pin DIP or Small 44-Pin PLCC Package
Power Dissipation: 1000mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
66MHz
40MHz

ADV453 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV453 is a complete analog video output RAM-DAC on a single monolithic chip. It is specifically designed for high resolution color graphics systems. The part contains a 256×24 color lookup table, a 3×24 overlay palette as well as triple 8-bit video D/A converters. The ADV453 is capable of simultaneously displaying up to 259 colors, 256 from the lookup table and three from the overlay registers, out of a total color palette of 16.8 million addressable colors.

The three overlay registers allow for the implementation of overlaying cursors, pull down menus and grids. There is an independent, asynchronous MPU bus which allows access to the color lookup table without affecting the input of video data via the pixel port. The ADV453 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV453 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6", 40-pin DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 66MHz.
2. Compatible with a wide variety of high resolution color graphics systems including VGA* and Macintosh II**.
3. Three overlay registers allow for implementation of overlaying cursors, pull down menus and grids.
4. Guaranteed monotonic. Integral and differential nonlinearities guaranteed to be a maximum of ±1LSB.
5. Low glitch energy, 50pV secs.

*VGA is a trademark of International Business Machines Corp.
**Macintosh II is a registered trademark of Apple Computer Inc.

SPECIFICATIONS (V_{AA} = +5V ±5%, V_{REF} = +1.235V, R_{SET} = 280Ω. I_{SYNC} connected to IOG. All specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5%	Gray Scale max	
Coding		Binary	
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	± 1	µA max	V_{IN} = 0.4V or 2.4V
Input Capacitance, C_{IN}	10	pF typ	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2mA
Floating State Leakage Current	20	µA max	
Floating State Output Capacitance	20	pF typ	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44mA
	1.90	mA max	
Blank Level on IOR, IOB	0	µA min	Typically 5µA
	50	µA max	
Blank Level on IOG	6.29	mA min	Typically 7.62mA
	8.96	mA max	
Sync Level on IOG	0	µA min	Typically 5µA
	50	µA max	
LSB Size	69.1	µA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF typ	I_{OUT} = 0mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	
Input Current, I_{VREF}	−5	mA typ	
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	
Supply Current, I_{AA}	275	mA max	Typically 220mA, 66MHz Parts
	250	mA max	Typically 190mA, 40MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%, f = 1kHz, COMP = 0.1µF
Power Dissipation	1375	mW max	Typically 1000mW, 66MHz Parts
	1250	mW max	Typically 900mW, 40MHz Parts
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[2,3]	−30	dB typ	
Glitch Impulse[2,3]	50	pV secs typ	
DAC to DAC Crosstalk	−23	dB typ	

NOTES

[1]Temperature Range (T_{min} to T_{max}); 0 to +70°C

[2]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.

[3]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2 × clock rate.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA} = +5V ±5%, V_{REF} = +1.235V, R_{SET} = 280Ω. I_{SYNC} connected to IOG. All Specifications T_{min} to T_{max}[2]).

Parameter	66MHz Version	40MHz Version	Units	Conditions/Comments
f_{max}	66	40	MHz max	Clock Rate
t_1	35	35	ns min	$\overline{CS}$, C0, C1 Setup Time
t_2	35	35	ns min	$\overline{CS}$, C0, C1 Hold Time
t_3	25	25	ns min	$\overline{RD}$, $\overline{WR}$ High Time
t_4	10	10	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_5	100	100	ns max	$\overline{RD}$ Asserted to Data Valid
t_6	15	15	ns max	$\overline{RD}$ Negated to Data Bus Three Stated
t_7	50	50	ns min	$\overline{WR}$ Low Time
t_8	35	35	ns min	Write Data Setup Time
t_9	0	0	ns min	Write Data Hold Time
t_{10}	5	7	ns min	Pixel & Control Setup Time
t_{11}	2	3	ns min	Pixel & Control Hold Time
t_{12}	15	25	ns min	Clock Cycle Time
t_{13}	5	7	ns min	Clock Pulse Width High Time
t_{14}	5	7	ns min	Clock Pulse Width Low Time
t_{15}	20	20	ns typ	Analog Output Delay
	30	30	ns max	
t_{16}	3	3	ns typ	Analog Output Rise/Fall Time
t_{17}[3]	25	25	ns typ	Analog Output Settling Time
t_{PD}	$2\times t_{12}$	$2\times t_{12}$	ns max	Pipeline Delay
t_{SK}	1	1	ns typ	Analog Output Skew
	2	2	ns max	

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.
[2]Temperature Range (T_{min} to T_{max}); 0 to +70°C.
[3]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by HC logic.
Specifications subject to change without notice.

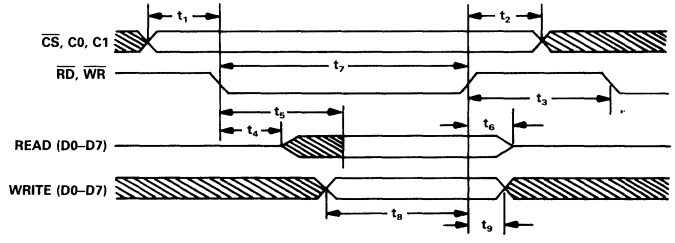
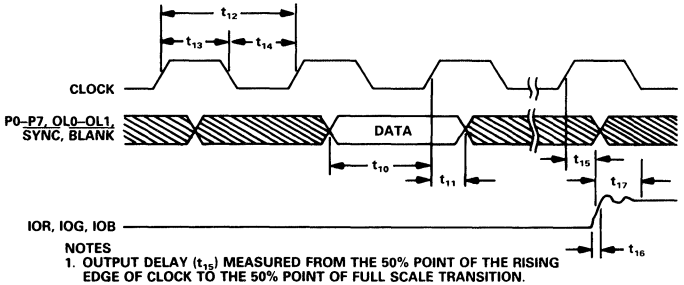


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME(t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1LSB.
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 2. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

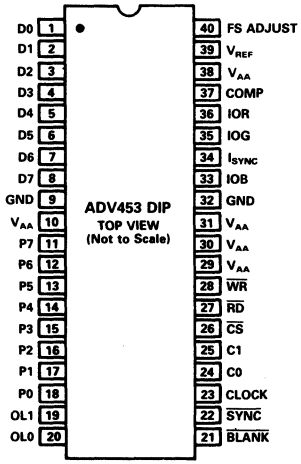
ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7V
Voltage on Any Digital Pin . . . . . .GND–0.5V to V_{AA} +0.5V
Ambient Operating Temperature (T_A) . . . . . .0 to +70°C
Storage Temperature (T_S) . . . . . .–65°C to +150°C
Junction Temperature (T_J) . . . . . .+175°C
Soldering Temperature (5secs) . . . . . .260°C
IOR, IOB, IOG to GND[1] . . . . . .0V to V_{AA}

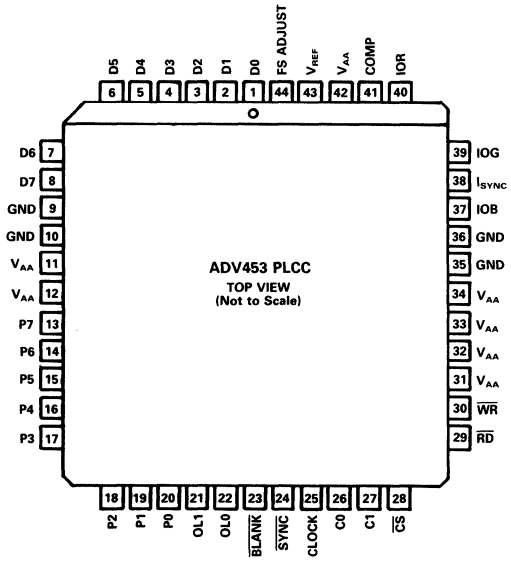
NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PIN CONFIGURATIONS

DIP



PLCC



ORDERING INFORMATION[1]

Package Options[2]	Speed	
	66MHz	40MHz
Plastic DIP (N-40A)	ADV453KN66	ADV453KN40
PLCC[3] (P-44A)	ADV453KP66	ADV453KP40

NOTES
[1]All devices are specified for 0 to +70°C operation.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier (J-lead).

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is at logical zero, the pixel and overlay inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source on the I_{SYNC} output (see Figure 5). $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Table V; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7 and OL0–OL1 data inputs as well as the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of CLOCK. P0 is the LSB. Unused pixel select inputs should be connected to GND.
OL0–OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information (see Table IV), i.e., the 256×24 color palette or the 3×24 overlay palette. When accessing the overlay palette, the P0–P7 inputs are ignored. OL0–OL1 are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output (see Figure 3). This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{\text{SYNC}}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{\text{SYNC}}$ is at logical one is given by: I_{SYNC} (mA) = 1,728 * V_{REF}(V)/ R_{SET} (Ω). If sync information is not required on the green channel, I_{SYNC} should be connected to GND.
FS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and GND (see Figure 6) controls the magnitude of the full scale video signal. Note that the IRE relationships in Figure 5 are maintained, regardless of the full scale output current. The relationship between R_{SET} and the full scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: IOG (mA) = (K + 326 + 1,728) * V_{REF}(V)/R_{SET} (Ω) The relationship between R_{SET} and the full scale output current on IOR and IOB is given by: IOR, IOB (mA) = (K + 326)* V_{REF}(V)/R_{SET}(Ω) where K = 3,993
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1μF ceramic capacitor must be connected between COMP and V_{AA} (Figure 6).
V_{REF}	Voltage reference input. An external 1.235V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA} (Figure 6.)
V_{AA}	Analog power supply (5V±5%). All V_{AA} pins on the ADV453 must be connected.
GND	Analog ground. All GND pins must be connected.
$\overline{\text{CS}}$	Chip select control input (TTL compatible). $\overline{\text{CS}}$ must be at logical zero to enable the reading and writing of data to and from the device. The IOR, IOG and IOB outputs are forced to the black level while $\overline{\text{CS}}$ is at logical zero. Note that the ADV453 will not operate properly if $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are simultaneously at logical zero.
$\overline{\text{WR}}$	Write control input (TTL compatible). $\overline{\text{CS}}$ and $\overline{\text{WR}}$ must both be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$ or $\overline{\text{CS}}$. See Figure 1.
$\overline{\text{RD}}$	Read control input (TTL compatible). $\overline{\text{CS}}$ and $\overline{\text{RD}}$ must both be at logical zero when reading data from the device. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being carried out, i.e., address register, color palette RAM or overlay registers read or write operations. See Tables I, II, III.
D0–D7	Data bus (TTL compatible). Data is transferred to and from the address register, the color palette RAM and the overlay registers over this 8-bit bidirectional data bus. D0 is the least significant bit.

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal (SYNC)
The position of the composite video signal which synchronizes the scanning process.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

ADV453 CIRCUIT DESCRIPTION

MPU Interface
As illustrated in the functional block diagram, the ADV453 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers. The color palette RAM and overlay color registers can be accessed only when $\overline{CS}$ is low. The Pixel and Overlay Select inputs are disabled while $\overline{CS}$ is low.

The C0 and C1 control inputs specify whether the MPU is accessing the address register, color palette RAM or the overlay registers, as shown in Table I. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

$\overline{CS}$	C1	C0	Addressed by MPU
0	X	0	Address Register
0	0	1	Color Palette RAM
0	1	1	Overlay Register

Table I. Control Input Truth Table

To write color data, the MPU writes to the address register with either the address of the color palette RAM location or the address of the overlay register which is to be modified. The MPU performs three successive write cycles (8 bits of red data, 8 bits of green data and 8 bits of blue data). This color data is diverted to either the color palette RAM or the overlay registers, as determined by C0 and C1. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then automatically increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

To read back color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 bits each of red, green and blue data), using C0 and C1 to select either the color palette RAM or the overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

When $\overline{CS}$ is low, i.e., during MPU read/write cycles, the video outputs are forced to the black level. During color palette RAM access, the address register resets to 00H following a blue read or write operation to RAM location FFH.

The three overlay registers can be accessed in the same way as the color palette RAM. The overlays are selected using C0 and C1 according to Table I. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the six most significant bits of the address register (ADDR2–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G and B in the block diagram) are synchronized by internal logic and occur in the period between MPU accesses. Color (RGB) data is normally loaded to the color palette RAM/overlay registers during video screen retrace, i.e. during the video waveform blanking period (see Figure 5).

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as shown in Table III. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing and Table III shows the associated functional instructions.

	Value	C1	C0	Addressed by MPU
ADDRa,b (Counts Modulo 3)	00	X	1	Red Value
	01	X	1	Green Value
	10	X	1	Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	1	Color Palette RAM
	XXXX XX00	1	1	Reserved
	XXXX XX01	1	1	Overlay Color 1
	XXXX XX10	1	1	Overlay Color 2
	XXXX XX11	1	1	Overlay Color 3

Note: Control input C1 determines whether a read/write operation is performed on the color palette RAM or the overlay registers.

Table II. Address Register (ADDR) Operation

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	C0	C1	ADDRb	ADDRa	Operation Performed	
0	1	0	0	X	X	X	Write Address Register;	D0–D7→ADDR0–7 0→ADDRa,b
0	1	0	1	X	0	0	Write Red Value;	Increment ADDRa-b
0	1	0	1	X	0	1	Write Green Value;	Increment ADDRa-b
0	1	0	1	X	1	0	Write Blue Value;	Modify RAM/Overlay Location Increment ADDR0–7 Increment ADDRa-b
0	0	1	0	X	X	X	Read Address Register;	ADDR0–7→D0–D7
0	0	1	1	X	0	0	Read Red Value;	Increment ADDRa-b
0	0	1	1	X	0	1	Read Green Value;	Increment ADDRa-b
0	0	1	1	X	1	0	Read Blue Value; Increment ADDRa-b	Increment ADDR0–7
0	0	0	X	X	X	X	Invalid Operation	

Note: Control input C1 determines whether a read/write operation is performed on the color palette RAM or the overlay registers.

Table III. Truth Table for Read/Write Operations

Frame Buffer Interface

The P0–P7, OL0 and OL1 inputs are used to address the color palette RAM and overlay registers, as shown in Table IV. These inputs are latched on the rising edge of CLOCK and address any of the 256 locations in the color palette RAM or the three overlay registers. The addressed location contains 24 bits of color (8 bits of red, 8 bits of green and 8 bits of blue) information.This data is transferred to the three DACs and is then converted to an analog output (IOR, IOG and IOB), these outputs then control the red green and blue electron guns in the monitor.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs are also latched on the rising edge of CLOCK. This is to maintain synchronization with the color data.

OL1	OL0	P0–P7	Addressed by Frame Buffer
0	0	00H	Color Palette RAM Location 00H
0	0	01H	Color Palette RAM Location 01H
.	.	.	.
.	.	.	.
0	0	FFH	Color Palette RAM Location FFH
0	1	XXH	Overlay Color 1
1	0	XXH	Overlay Color 2
1	1	XXH	Overlay Color 3

Table IV. Pixel and Overlay Control Truth Table

Analog Interface

The ADV453 has three analog outputs, corresponding to the red, green and blue video signals. A fourth analog output (I_{SYNC}) can be used if it is required to encode video synchronization information onto the green signal. In this case, I_{SYNC} is connected to IOG as shown in Figure 3. If it is not required to encode sync information onto the green signal (as would be the case if a separate synchronization circuit was used), I_{SYNC} should be connected to GND and the digital $\overline{\text{SYNC}}$ input pin should be tied low.

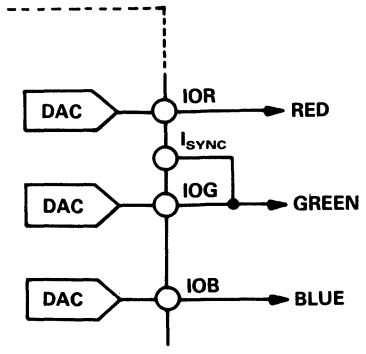


Figure 3. Encoding SYNC onto Green Signal

The red, green and blue analog outputs of the ADV453 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω coaxial cable. Figure 4a shows the required configuration for each of the three RGB outputs connected into a doubly terminated 75Ω load. This arrangement will develop RS-343A video output voltage levels across a 75Ω monitor. A simple method of driving RS-170 video levels into a 75Ω monitor is shown in Figure 4b. The output current levels of the DACs remain unchanged, but the source termination resistance, Z_S, on each of the three DACs is increased from 75Ω to 150Ω.

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an application note entitled "Video Formats & Required Load Terminations" available from Analog Devices.

Figure 5 shows the video waveforms associated with the three RGB outputs driving the doubly terminated 75Ω load of Figure 4a. As well as the grey scale levels, Black Level to White Level, the diagram also shows the contributions of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$. These control inputs add appropriately weighted currents to the analog outputs producing the specific output level requirements for video applications. Table V details how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

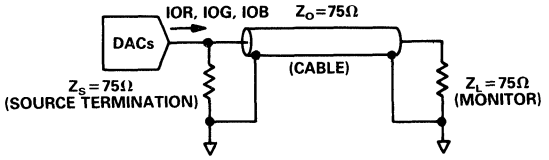


Figure 4a. Recommended Analog OutputTermination for RS-343A

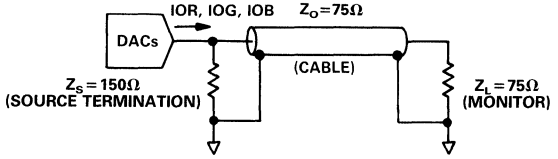
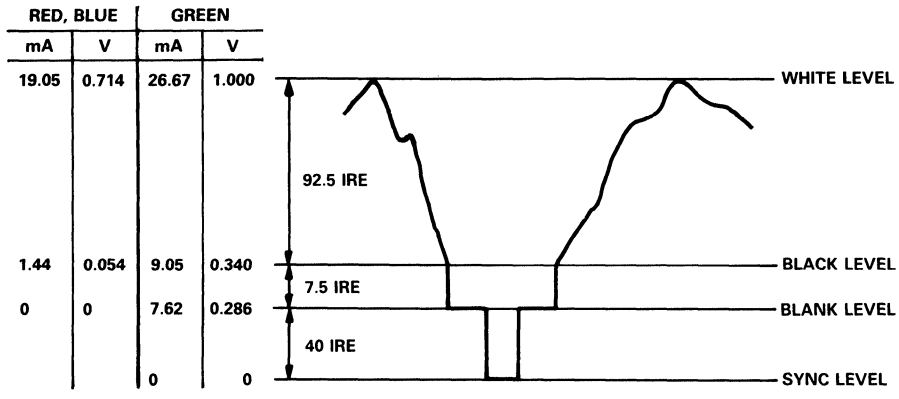


Figure 4b. Recommended Analog Output Termination for RS-170



NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. V_{REF} = 1.235V, R_{SET} = 280Ω, I_{SYNC} CONNECTED TO IOG.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 5. RGB Video Output Waveform

Description	IOG mA[1]	IOR, IOB mA	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
White Level	26.67	19.05	1	1	FFH
Video	Video + 9.05	Video + 1.44	1	1	Data
Video to Blank	Video + 1.44	Video + 1.44	0	1	Data
Black Level	9.05	1.44	1	1	00H
Black to Blank	1.44	1.44	0	1	00H
Blank Level	7.62	0	1	0	XXH
SYNC Level	0	0	0	0	XXH

NOTES
[1]Typical with full scale IOG = 26.67mA.
V_{REF} = 1.235V, R_{SET} = 280Ω, I_{SYNC} connected to IOG.

Table V. Video Output Truth Table

PC BOARD LAYOUT CONSIDERATIONS

The ADV453 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV453, it is imperative that great care be given to the PC board layout. The layout should be optimized for lowest noise on the ADV453 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

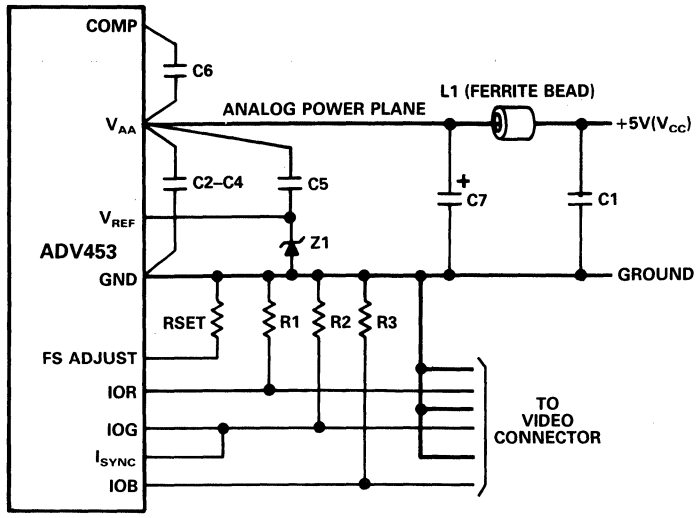
The ground plane should encompass all ADV453 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and all the digital signal traces leading up to the ADV453.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV453 (V_{AA}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 6. This bead should be located within three inches of the ADV453.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV453 power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C6	0.1μF CERAMIC CAPACITOR	
C7	10μF TANTALUM CAPACITOR	
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	280Ω 1% METAL FILM RESISTOR	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589KH

Figure 6. ADV453 Typical Connection Diagram and Component List

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors (see Figure 6).

Optimum performance is achieved by the use of 0.1μF ceramic capacitors. Each of the three groups of V_{AA} should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV453 contains circuitry to reject power supply noise; this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI supression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three-terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV453 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV453 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV453 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75Ω. This termination resistance should be as close as possible to the ADV453 to minimize reflections.

Monolithic 256×18 CMOS Color Palette RAM-DAC

ADV476

FEATURES
Personal System/2* and VGA* Compatible
Plug-in Replacement for INMOS 171/176
66MHz Pipelined Operation
Three 6-Bit D/A Converters
256×18 Color Palette RAM
RS-343A/RS-170 Compatible Outputs
Blank on All Three Channels
Standard MPU Interface
Asynchronous Access to All Internal Registers
+5V CMOS Monolithic Construction
Low Power Dissipation
Standard 28-Pin, 0.6" DIP

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
66MHz
50MHz
35MHz

GENERAL DESCRIPTION

The ADV476 is a pin compatible and software compatible RAM-DAC designed specifically for VGA and Personal System/2 color graphics.

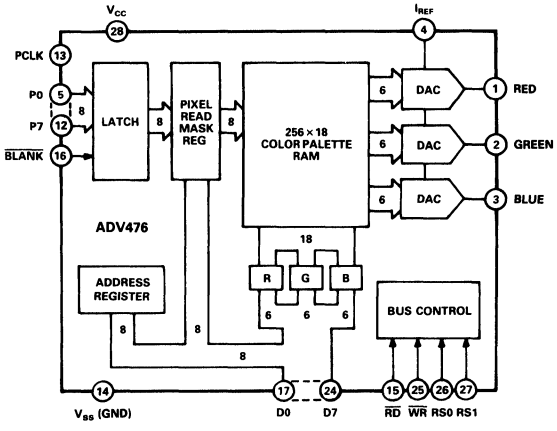
The ADV476 is a complete analog output RAM-DAC on a single monolithic chip. The part contains a 256×18 color lookup table, a pixel mask register as well as a triple 6-bit video D/A converter. The ADV476 is capable of simultaneously displaying up to 256 colors, from a total color palette of 262,144 addressable colors.

The on-chip asynchronous MPU bus allows access to the color lookup table without affecting the input video data via the pixel port. The pixel read mask register provides a convenient way of altering the displayed colors without updating the color lookup table. The ADV476 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV476 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation and small board area. The part is packaged in a 0.6", 28-pin DIP.

***Personal System/2 and VGA are trademarks of International Business Machines Corp.**

ADV476 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Standard video refresh rates, 35MHz, 50MHz and 66MHz.
2. Fully compatible with VGA and Personal System/2 color graphics.
3. Guaranteed monotonic. Integral and differential linearity guaranteed to be a maximum of ±1LSB.
4. Low glitch energy, 75pV secs.

SPECIFICATIONS

(V_{CC} = +5V ±10%, I_{REF} = 8.88mA. All Specifications T_{min} to T_{max}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	6	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±0.5	LSB max	Guaranteed Monotonic
Full Scale Error	±5	% max	Full Scale = $2.15 \times I_{REF} \times R_L$, I_{REF} = 8.39mA
Blank Level	±0.5	LSB max	$\overline{BLANK}$ = Logic Low
Offset Error	±0.5	LSB max	$\overline{BLANK}$ = Logic High
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±10	µA max	V_{CC} = 5.5V, V_{IN} = 0.4V to V_{CC}
Input Current ($\overline{RD}$ Input Only)	±100	µA max	V_{CC} = 5.5V, V_{IN} = 0.4V to V_{CC}
Input Capacitance, C_{IN}	7	pF typ	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 500µA, V_{CC} = 4.5V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 5.0mA, V_{CC} = 4.5V
Floating-State Leakage Current	±50	µA max	V_{CC} = 5.5V, 0.4V < V_{IN} < V_{CC}
Floating-State Output Capacitance	7	pF typ	
ANALOG OUTPUTS			
Max Output Voltage	1.5	V min	IO ≤ 10mA, IO = $2.15 \times I_{REF}$
Max Output Current	21	mA min	VO ≤ 1V
DAC to DAC Matching[2]	±2.5	% max	
Analog Output Capacitance	10	pF typ	$\overline{BLANK}$ = Logic Low
CURRENT REFERENCE			
Input Current (I_{REF}) Range	−3/−10	mA min/mA max	
Voltage at I_{REF}	V_{CC} −3/V_{CC}	V min/V max	I_{REF} = 8.88mA
POWER SUPPLY			
Supply Voltage, V_{CC}	4.5/5.5	V min/V max	
Supply Current, I_{CC}	220	mA max	f_{MAX} = 66MHz, IO = $2.15 \times I_{REF}$, D0 to D7 Unloaded
Power Supply Rejection Ratio	6	%/V	4.5 < V_{CC} < 5.5V, IO = $2.15 \times I_{REF}$, R_L = 37.5Ω, C_L = 30pF, I_{REF} = 8.88mA
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[3,4]	−35	dB typ	
Glitch Impulse[3,4]	75	pV secs typ	

NOTES

[1]Temperature range (T_{min} to T_{max}); 0 to +70°C.

[2]Relative to the midpoint of the distribution of the three DACs measured at full scale.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0–D7 output load ≤50pF. See timing notes in Figure 2.

[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2×clock rate.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{CC} = +5V±10%. All Specifications T_{min} to T_{max}[2])

Parameter	66MHz Version	50MHz Version	35MHz Version	Units	Conditions/Comments
f_{max}	66	50	35	MHz	Clock Rate
t_1	10	10	15	ns min	RS0, RS1 Setup Time
t_2	10	10	15	ns min	RS0, RS1 Hold Time
t_3	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6	10	10	15	ns min	Write Data Setup Time
t_7	10	10	15	ns min	Write Data Hold Time
t_8	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_9	$4\times t_{12}$	$4\times t_{12}$	$4\times t_{12}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{10}	3	3	4	ns min	Pixel & Control Setup Time
t_{11}	3	3	4	ns min	Pixel & Control Hold Time
t_{12}	15.3	20	28	ns min	Clock Cycle Time
t_{13}	5	6	7	ns min	Clock Pulse Width High Time
t_{14}	5	6	9	ns min	Clock Pulse Width Low Time
t_{15}	30	30	30	ns max	Analog Output Delay
	5	5	5	ns min	
t_{16}	6	8	8	ns max	Analog Output Rise/Fall Time
t_{17}[3]	15.3	20	25	ns typ	Analog Output Settling Time
t_{18}	2	2	2	ns min	Analog Output Skew
t_{PD}	4	4	4	clocks	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load≤10 pF, 37.5Ω. D0–D7 output load≤50 pF. See timing notes in Figure 2.
[2]Temperature Range (T_{min} to T_{max}); 0 to +70°C
[3]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic.
Specifications subject to change without notice.

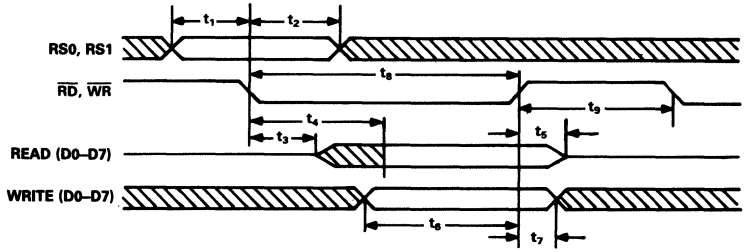
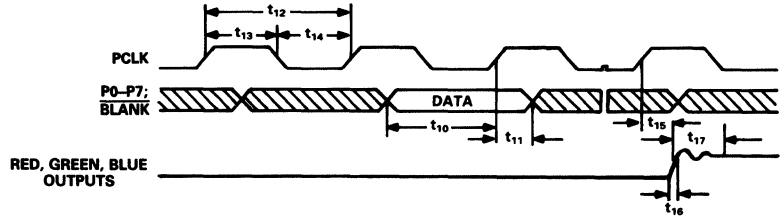


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF THE PCLK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME (t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1/4 LSB.
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

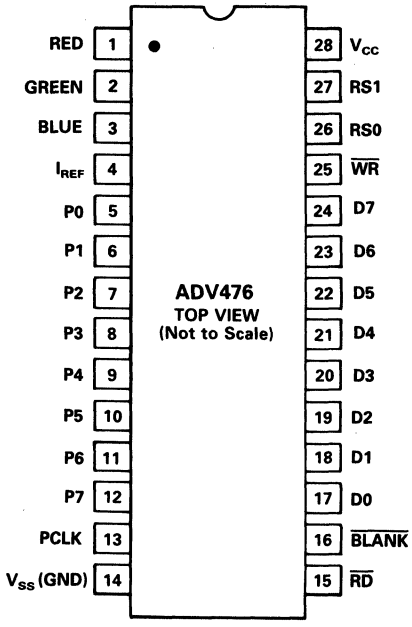
Figure 2. Video Input/Output Timing

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to GND . . . . . +7V
Voltage on any Digital Pin. . . . . .GND−0.5V to V_{CC}+0.5V
Ambient Operating Temperature (T_A). . . . . .−55°C to +125°C
Storage Temperature (T_S). . . . . .−65°C to +150°C
Junction Temperature (T_J). . . . . .+175°C
Soldering Temperature (5secs) . . . . . .+260°C
Red, Green, Blue to GND[1]. . . . . .0V to V_{CC}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

DIP PIN CONFIGURATIONS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{CC}	4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Current	I_{REF}	−3		−10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION[1]

Model	Speed	Package Options[2, 3]
ADV476KN35	35MHz	N-28
ADV476KN50	50MHz	N-28
ADV476KN66	66MHz	N-28

NOTES
[1]All devices are specified for 0 to +70°C operation.
[2]All devices are packaged in 0.6" 28-pin plastic DIPs (N-28).
[3]See Section 14 for package outline information.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs to the blanking level, as shown in Table V. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of PCLK. While $\overline{\text{BLANK}}$ is a logical zero, the pixel inputs are ignored.
PCLK	Clock input (TTL compatible). The rising edge of PCLK latches the P0–P7 data inputs and the $\overline{\text{BLANK}}$ control input. It is typically the pixel clock rate of the video system. PCLK should be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. P0–P7 pixel select inputs are latched on the rising edge of PCLK. P0 is the LSB. Unused pixel select inputs should be connected to GND.
RED, GREEN, BLUE	Red, green and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable, as shown in Figure 4a. All three current outputs should have similar output loads whether or not they are all being used.
V_{CC}	Analog power supply (5V ±10%).
GND	Analog ground.
I_{REF}	Current reference input. The relationship between the current input and the full scale output voltage of the DACs is given by the following expression: I_{REF} = VO (Full Scale)/2.15 × R_L R_L = Load Resistance
$\overline{\text{WR}}$	Write control input (TTL compatible). $\overline{\text{WR}}$ must be at logical zero when writing data to the device. D0–D7 data is latched on the rising edge of $\overline{\text{WR}}$. See Figure 1.
$\overline{\text{RD}}$	Read control input (TTL compatible). $\overline{\text{RD}}$ must both be at logical zero when reading data from the device. See Figure 1.
RS0, RS1	Command control inputs (TTL compatible). RS0 and RS1 specify the type of read or write operation being carried out, i.e., address register or color palette RAM read or write operations. See Tables I, II, III.
D0–D7	Data bus (TTL compatible). Data is transferred to and from the address register and the color palette RAM over this 8-bit bidirectional data bus. D0 is the least significant bit.

TERMINOLOGY

Blanking Level
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch or Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of Red, Green and Blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Gray Scale
The discrete levels of video signal between Reference Black and Reference White levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

MPU Interface

As illustrated in the functional block diagram, the ADV476 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM .

The RS0 and RS1 control inputs specify whether the MPU is accessing the address register or the color palette RAM, as shown in Table I. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers.

RS1	RS0	Addressed by MPU
0	0	Pixel Address Register (RAM Write Mode)
1	1	Pixel Address Register (RAM Read Mode)
0	1	Color Palette RAM
1	0	Pixel Read Mask Register

Table I. Control Input Truth Table

To write color data, the MPU writes to the address register with the 8-bit address of the color palette RAM location which is to be modified. The MPU performs three successive write cycles (six bits of red data, six bits of green data and six bits of blue data). During the blue write cycle, the three bytes of color information are concatenated into an 18-bit word and written to the location specified by the address register. The address register then automatically increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

To read back color data, the MPU loads the address register with the address of the color palette RAM location to be read. The MPU performs three successive read cycles (6 bits each of red, green and blue data). Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

This 6-bit color data is right justified, i.e., the lower six bits of the data bus with D0 being the LSB and D5 the MSB. D6 and D7 are ignored during a color write cycle and are set to zero during a color read cycle.

During color palette RAM access, the address register resets to 00H following a blue read or write operation to RAM location FFH.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Color (RGB) data is normally loaded to the color palette RAM during video screen retrace, i.e., during the video waveform blanking period, see Figure 5.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations, as shown in Table III. ADDR0 is the LSB when the MPU is accessing the RAM. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing and Table III shows the associated functional instructions.

	Value	RS1	RS0	Addressed by MPU
ADDRa,b (Counts Modulo 3)	00			Red Value
	01			Green Value
	10			Blue Value
ADDR0–7 (Counts Binary)	00H–FFH	0	1	Color Palette RAM

Table II. Address Register (ADDR) Operation

$\overline{RD}$	$\overline{WR}$	RS0	RS1	ADDRa	ADDRb	Operation Performed	
1	0	0	0	X	X	Write Address Register;	D0–D7 → ADDR0–7 0 → ADDRa,b
1	0	1	0	0	0	Write Red Value;	Increment ADDRa–b
1	0	1	0	0	1	Write Green Value;	Increment ADDRa–b
1	0	1	0	1	0	Write Blue Value;	Modify RAM Location Increment ADDR0–7 Increment ADDRa–b
0	1	1	1	X	X	Read Address Register;	ADDR0–7 → D0–D7
0	1	1	0	0	0	Read Red Value;	Increment ADDRa–b
0	1	1	0	0	1	Read Green Value;	Increment ADDRa–b
0	1	1	0	1	0	Read Blue Value;	Increment ADDR0–7 Increment ADDRa–b
0	0	X	X	X	X	Invalid Operation	

Table III. Truth Table for Read/Write Operations

Frame Buffer Interface

The P0–P7 inputs are used to address the color palette RAM, as shown in Table IV. These inputs are latched on the rising edge of PCLK and address any of the 256 locations in the color palette RAM. The addressed location contains 18 bits of color (6 bits of red, 6 bits of green and 6 bits of blue) information. This data is transferred to the three DACs and is then converted to an analog output (RED, GREEN, BLUE), these outputs then control the red, green and blue electron guns in the monitor.

The $\overline{\text{BLANK}}$ input is also latched on the rising edge of PCLK. This is to maintain synchronization with the color data.

P0–P7	Addressed by Frame Buffer
00H	Color Palette RAM Location 00H
01H	Color Palette RAM Location 01H
•	• •
•	• •
FFH	Color Palette RAM Location FFH

Table IV. Pixel Select/Color Palette Control Truth Table

Pixel Read Mask Register

The Pixel Read Mask Register in the ADV476 can be used to implement register level pixel processing, thereby cutting down on software overhead. This is achieved by gating the input pixel stream (P0–P7) with the contents of the pixel read mask register. The operation is a bitwise logical ANDing of the pixel data. The contents of this register can be accessed and altered at any time by the MPU (D0–D7). Table I shows the relevant control signals.

This pixel masking operation can be used to alter the displayed colors without changing the contents of either the video frame buffer or the color palette RAM. The effect of this operation is to partition the color palette into a user determined number of color planes. This process can be used for special effects including animation, overlays and flashing objects.

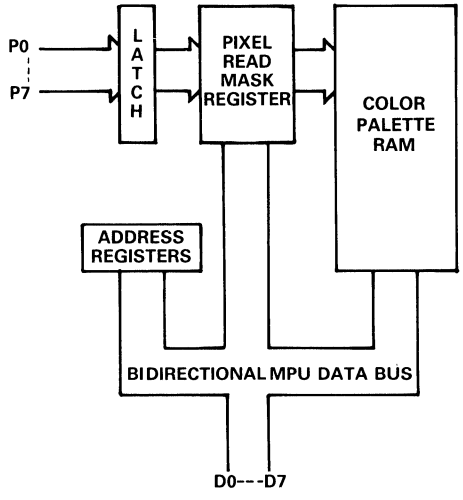


Figure 3. Block Diagram Showing Pixel Read Mask Register

Analog Interface

The ADV476 has three analog outputs, corresponding to the Red, Green and Blue video signals.

The Red, Green and Blue analog outputs of the ADV476 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5Ω load, such as a doubly-terminated 75Ω coaxial cable. Figure 4a shows the required configuration for each of the three RGB outputs connected into a doubly-terminated 75Ω load. This arrangement will develop RS-343A video output voltage levels across a 75Ω monitor. A simple method of driving RS-170 video levels into a 75Ω monitor is shown in Figure 4b. The output current levels of the DACs remain unchanged but the source termination resistance, Z_S, on each of the three DACs is increased from 75Ω to 150Ω.

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an application note entitled "Video Formats & Required Load Terminations" available from Analog Devices.

Figure 5 shows the video waveforms associated with the three RGB outputs, driving the doubly terminated 75Ω load of Figure 4a. The $\overline{\text{BLANK}}$ control input drives the analog outputs to the Black Level. $\overline{\text{BLANK}}$ is asserted prior to horizontal and vertical screen retrace. Table V details how the $\overline{\text{BLANK}}$ input modifies the output levels.

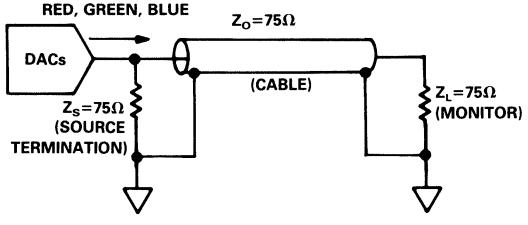


Figure 4a. Recommended Analog Output Termination for RS-343A

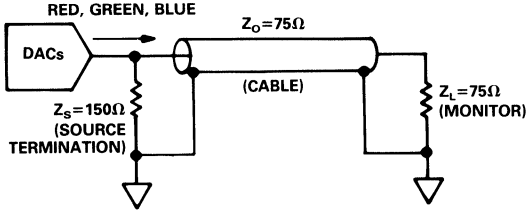
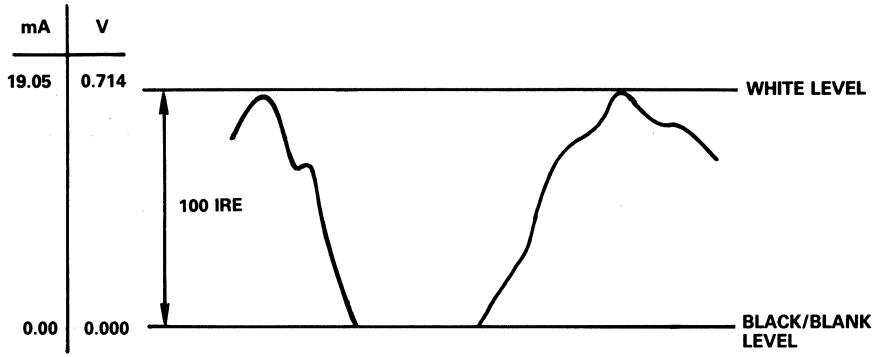


Figure 4b. Recommended Analog Output Termination for RS-170



NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. I_{REF}=8.88mA.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 5. RGB Video Output Waveform

Description	RED, GREEN, BLUE, (mA)[1]	$\overline{\text{BLANK}}$	DAC Input Data
WHITE LEVEL	19.05	1	FFH
VIDEO	Video	1	DATA
BLACK LEVEL	0	1	00H
BLANK LEVEL	0	0	xxH

NOTE
[1]Typical with full scale RED, GREEN, BLUE = 19.05mA. I_{REF} = 8.88mA.

Table V. Video Output Truth Table

Reference Input
The ADV476 requires an active current reference to enable the DACs provide stable and accurate video output levels. The relationship between the output voltage and the required input reference current is given by:

$$I_{REF}=\frac{VO\ (FULL\ SCALE)}{2.15\times R_L}$$

where R_L = 37.5Ω (for doubly terminated 75Ω load)
= 75Ω (for singly terminated 75Ω load)

and VO = 0.714V (RS-343A video levels)
= 1.0V (RS-170 video levels).

In a standard application which requires RS-343A video levels to be driven into a doubly terminated 75Ω load (R_L = 37.5Ω), the necessary reference input current is:

I_{REF} = 8.88mA.

To drive the same levels into a singly terminated 75Ω load (R_L = 75Ω), the reference current is:

I_{REF} = 4.44mA.

A suggested current reference design for the doubly terminated case, with RS-343A video levels and based on the LM334, a three-terminal adjustable current source, is shown in Figure 6.

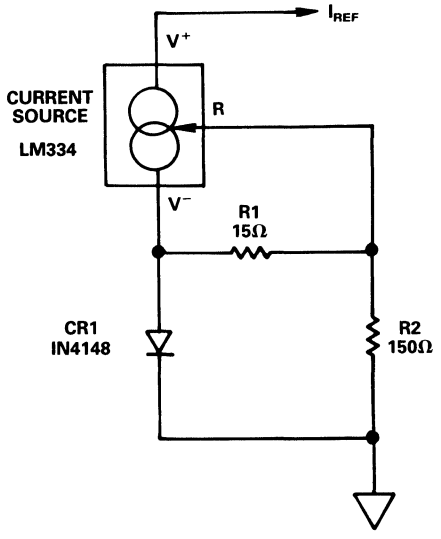


Figure 6. Current Reference Design Using an LM334 Current Source

PC BOARD LAYOUT CONSIDERATIONS

The ADV476 is optimally designed for lowest noise performance, both radiated and conducted noise. For optimum system noise performance, it is imperative that great care be given to the PC board layout. The layout should be optimized for lowest noise on the ADV476 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{CC} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV476 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and all the digital signal traces leading up to the ADV476.

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane (V_{CC}) should encompass the ADV476 and all associated analog circuitry. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 7. This bead should be located within three inches of the ADV476.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV476 power pins, current reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors, see Figure 7.

Optimum performance is achieved by the use of 0.1μF ceramic capacitors. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV476 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV476 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV476 should be avoided so as to minimize noise pickup.

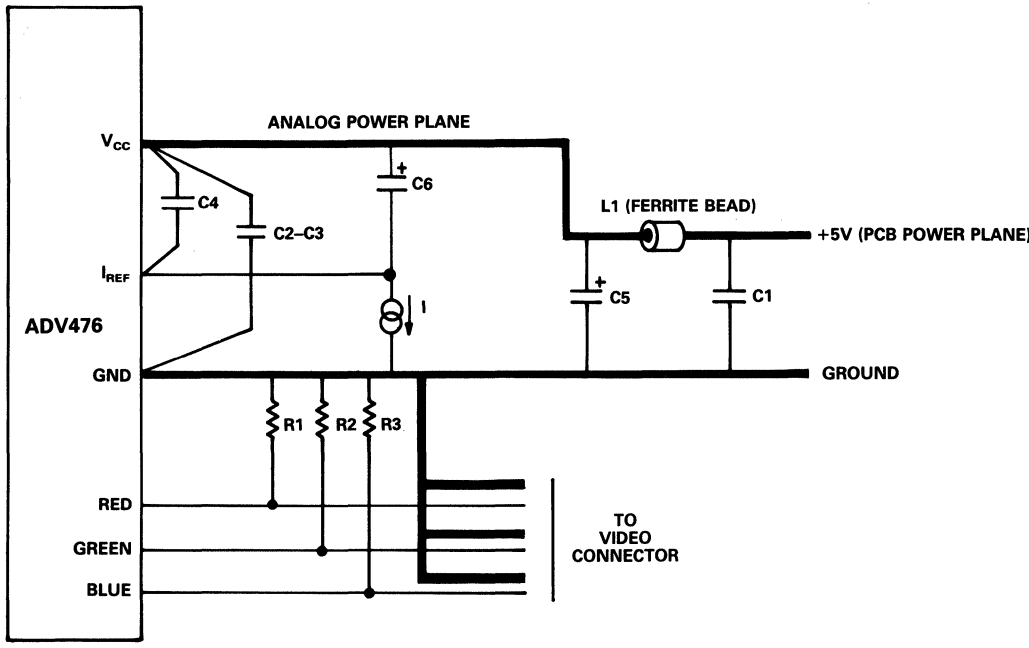
Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane and not the analog power plane.

Analog Signal Interconnect

The ADV476 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75Ω. This termination resistance should be as close as possible to the ADV476 to minimize reflections.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1–C4	0.1μF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C5	10μF TANTALUM CAPACITOR	MALLORY CSR13G106KM
C6	47μF TANTALUM CAPACITOR	MALLORY CSR13F476KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C

Figure 7. ADV476 Typical Connection Diagram and Component List

CMOS 80MHz Monolithic 256 × 24(18) Color Palette RAM-DAC

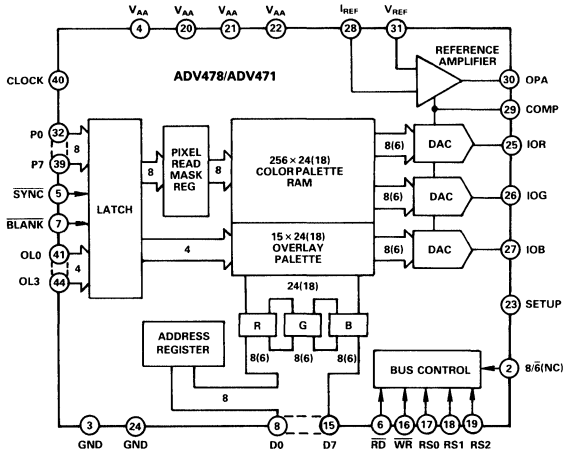
ADV478/ADV471

FEATURES
Personal System/2* Compatible
80MHz Pipelined Operation
Triple 8-Bit (6-Bit) D/A Converters
256 × 24(18) Color Palette RAM
15 × 24(18) Overlay Registers
RS-343A/RS-170 Compatible Outputs
Sync on All Three Channels
Programmable Pedestal (0 or 7.5 IRE)
External Voltage or Current Reference
Standard MPU Interface
+5V CMOS Monolithic Construction
44-Pin PLCC Package
Power Dissipation: 800mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
80MHz
66MHz
50MHz
35MHz

ADV478/ADV471 FUNCTIONAL BLOCK DIAGRAM



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

GENERAL DESCRIPTION

The ADV478 and ADV471 are pin compatible and software compatible RAM-DACs designed specifically for Personal System/2 compatible color graphics.

The ADV478 has a 256 × 24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6 bits or 8 bits per color operation. The ADV471 has a 256 × 18 color lookup table with triple 6-bit video D/A converters.

Options on both parts include a programmable pedestal (0 or 7.5 IRE) and use of an external voltage or current reference. Fifteen overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is a pixel read mask register and sync generation on all three channels.

The ADV478 and ADV471 generate RS-343A compatible video signals into a doubly terminated 75Ω load, and RS-170 compatible video signals into a singly terminated 75Ω load, without requiring external buffering. Differential and integral linearity errors are guaranteed to be a maximum of ±1LSB for the ADV478 and ±1/4LSB for the ADV471 over the full temperature range.

*Personal System/2 is a trademark of International Business Machines Corp.

SPECIFICATIONS (V_{AA}[1] = +5V, SETUP = 8/$\overline{6}$ = V_{AA}, V_{REF} = +1.235V. R_{SET} = 147Ω. All Specifications T_{min} to T_{max}[2] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)[3]	8 (6)	Bits	
Accuracy (Each DAC)[3]			
Integral Nonlinearity	±1 (1/4)	LSB max	
Differential Nonlinearity	±1 (1/4)	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4V or 2.4V
Input Capacitance, C_{IN}	7	pF max	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 400μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 3.2mA
Floating-State Leakage Current	50	μA max	
Floating-State Output Capacitance	7	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	20	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44mA
(SETUP = V_{AA})	1.90	mA max	
Black Level Relative to Blank	0	μA min	Typically 5μA
(SETUP = GND)	50	μA max	
Blank Level	6.29	mA min	Typically 7.62mA
	8.96	mA max	
Sync Level	0	μA min	Typically 5μA
	50	μA max	
LSB Size[3]	69.1 (279.68)	μA typ	8/$\overline{6}$ = Logical 1 for ADV478
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−1	V min	
	+1.5	V max	
Output Impedance, R_{OUT}	10	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	I_{OUT} = 0mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	
Input Current, I_{VREF}	10	μA typ	Tested in Voltage Reference Configuration with V_{REF} = 1.235V
POWER SUPPLY			
Supply Voltage, V_{AA}	4.75/5.25	V min/V max	80MHz Parts
	4.50/5.50	V min/V max	50MHz and 35MHz Parts
Supply Current, I_{AA}	220	mA max	Typically 180mA
Power Supply Rejection Ratio	0.5	%/% max	f = 1kHz, COMP = 0.1μF
Power Dissipation	1100	mW max	Typically 900mW, V_{AA} = 5V
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[4,5]	−30	dB typ	
Glitch Impulse[4,5]	75	pV secs typ	
DAC to DAC Crosstalk[6]	−23	dB typ	

NOTES

[1] ±5% for 80MHz parts; ±10% for 66MHz, 50MHz and 35MHz parts.

[2] Temperature Range (T_{min} to T_{max}); 0 to +70°C.

[3] Numbers in parentheses indicate ADV471 parameter value.

[4] Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic. Glitch impulse includes clock and data feedthrough, −3dB test bandwidth = 2 × clock rate.

[5] TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, D0 – D7 output load ≤50pF. See timing notes in Figure 2.

[6] DAC to DAC crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = +5V, SETUP = 8/$\overline{6}$ = V_{AA}, V_{REF} = 1.235V. R_{SET} = 147Ω. All Specifications T_{min} to T_{max}[3].)

Parameter	KP80 Version	KP66 Version	KP50 Version	KP35 Version	Units	Conditions/Comments
f_{max}	80	66	50	35	MHz	Clock Rate
t_1	10	10	10	15	ns min	RS0 – RS2 Setup Time
t_2	10	10	10	15	ns min	RS0 – RS2 Hold Time
t_3	5	5	5	5	ns min	$\overline{RD}$ Asserted to Data Bus Driven
t_4	40	40	40	40	ns max	$\overline{RD}$ Asserted to Data Valid
t_5	20	20	20	20	ns max	$\overline{RD}$ Negated to Data Bus 3-Stated
t_6	10	10	10	15	ns min	Write Data Setup Time
t_7	10	10	10	15	ns min	Write Data Hold Time
t_8	50	50	50	50	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width Low
t_9	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	ns min	$\overline{RD}$, $\overline{WR}$ Pulse Width High
t_{10}	3	3	3	4	ns min	Pixel and Control Setup Time
t_{11}	3	3	3	4	ns min	Pixel and Control Hold Time
t_{12}	12.5	15.3	20	28	ns min	Clock Cycle Time
t_{13}	4	5	6	7	ns min	Clock Pulse Width High Time
t_{14}	4	5	6	9	ns min	Clock Pulse Width Low Time
t_{15}	30	30	30	30	ns max	Analog Output Delay
t_{16}	3	3	3	3	ns typ	Analog Output Rise/Fall Time
t_{17}[4]	13	15.3	20	28	ns typ	Analog Output Settling Time
t_{18}	2	2	2	2	ns max	Analog Output Skew
t_{PD}	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	$4 \times t_{12}$	ns min	Pipeline Delay

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10pF, 37.5Ω. D0 – D7 output load ≤50pF. See timing notes in Figure 2.
[2]±5% for 80MHz parts; ±10% for 66MHz, 50MHz and 35MHz parts.
[3]Temperature Range (T_{min} to T_{max}); 0 to +70°C.
[4]Settling time does not include clock and data feedthrough. For this test, the digital inputs have a 1kΩ resistor to ground and are driven by 74HC logic.
Specifications subject to change without notice

TIMING DIAGRAMS

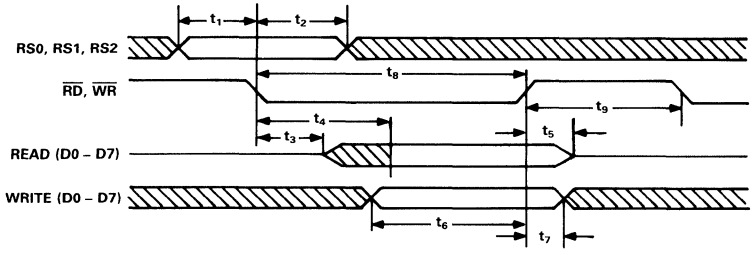
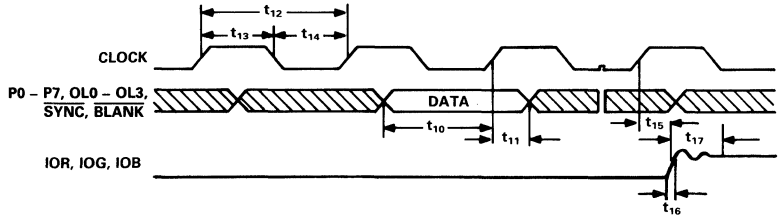


Figure 1. MPU Read/Write Timing



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSISTION.
2. SETTLING TIME (t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1LSB (ADV478) OR ±1/4LSB (ADV471).
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 2. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}				
80MHz Parts		4.75	5.00	5.25	Volts
50, 35MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts
Current Reference Configuration					
Reference Current	I_{REF}	−3		−10	mA

CAUTION

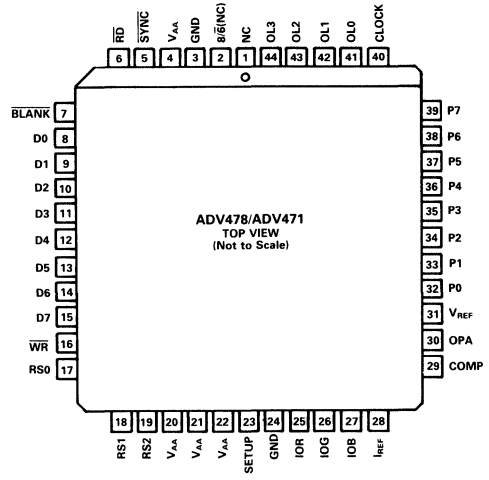
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND . . . . . +7V
Voltage on Any Digital Pin . . . GND −0.5V to V_{AA} +0.5V
Ambient Operating Temperature (T_A) . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +175°C
Vapor Phase Soldering (2 minutes) . . . . . TBD
IOR, IOB, IOG to GND[1] . . . . . 0V to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog output short circuit to any power supply or common can be of an indefinite duration.

PLCC PIN CONFIGURATION



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

ORDERING INFORMATION[1, 2]

Color Palette RAM	Speed				Package Options[3]
	80MHz	66MHz	50MHz	35MHz	
256 × 18	ADV471KP80	ADV471KP66	ADV471KP50	ADV471KP35	P-44A
256 × 24	ADV478KP80	ADV478KP66	ADV478KP50	ADV478KP35	P-44A

NOTES
[1]All devices are packaged in a 44-pin plastic leaded (J-lead) chip carrier, PLCC.
[2]All devices are specified for 0 to +70°C operation.
[3]See Section 14 for package outline information.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level as illustrated in Tables IV and V. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel and overlay inputs are ignored
SETUP	Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Tables IV and V; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0 – P7, OL0 – OL3, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0 – P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0 – OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table III. When accessing the overlay palette, the P0 – P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable (Figures 5 and 6).
I_{REF}	Full-scale adjust control. Note that the IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current. When using an external voltage reference (Figure 5), a resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between R_{SET} and the full-scale output current on each output is: $R_{SET}\ (\Omega) = K * 1{,}000 * V_{REF}\ (V)/I_{OUT}\ (mA)$ K is defined in the table below, along with corresponding R_{SET} values for doubly terminated 75Ω loads. When using an external current reference (Figure 6), the relationship between I_{REF} and the full-scale output current on each output is: $I_{REF}\ (mA) = I_{OUT}\ (mA)/K$

Mode	Pedestal	K	R_{SET} (Ω)
6-Bit	7.5 IRE	3.170	147
8-Bit	7.5 IRE	3.195	147
6-Bit	0 IRE	3.000	147
8-Bit	0 IRE	3.025	147

COMP	Compensation pin. If an external voltage reference is used (Figure 5), this pin should be connected to OPA. If an external current reference is used, this pin should be connected to I_{REF}. A 0.1μF ceramic capacitor must always be used to bypass this pin to V_{AA}.
V_{REF}	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2V (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating, except for the bypass capacitor. A 0.1μF ceramic capacitor must always be used to decouple this input to V_{AA} as shown in Figures 5 and 6.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 5), this pin must be connected to COMP. When using an external current reference (Figure 6), this pin should be left floating.
V_{AA}	Analog power. All V_{AA} pins must be connected to the Analog Power Plane.
GND	Analog ground. All GND pins must be connected to the Ground Plane.
$\overline{\text{WR}}$	Write control input (TTL compatible). D0 – D7 data is latched on the rising edge of $\overline{\text{WR}}$, and RS0 – RS2 are latched on the falling edge of $\overline{\text{WR}}$ during MPU write operations. See Figure 1.

Pin Mnemonic	Function
$\overline{RD}$	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS0 – RS2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0 – RS2 specify the type of read or write operation being performed as illustrated in Tables I and II.
D0 – D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
8/$\overline{6}$	8-bit/6-bit select input (TTL compatible). This control input specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and are logical zero during color read cycles). This control input is implemented only on the ADV478.

TERMINOLOGY

Blanking Level
The level seperating the SYNC portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs would be required, one for each color.

Composite SYNC Signal (SYNC)
The position of the composite video signal which synchronizes the scanning process.

Composite Video Signal
The video signal with or without setup, plus the composite SYNC signal.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Setup
The difference between the reference black level and the blanking level.

SYNC Level
The peak level of the composite SYNC signal.

Video Signal
That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the ADV478 and ADV471 support a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0 – RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers or read mask register, as shown in Table I. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers.

To write color data, the MPU writes to the address register (selecting RAM or overlay write mode) with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 or 6 bits each of red, green and blue), using RS0 – RS2 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the ADV471) and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green and blue data.

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Registers
1	1	0	Reserved

Table I. Control Input Truth Table

To read color data, the MPU loads the address register (selecting RAM or overlay read mode) with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 or 6 bits each of red, green and blue), using RS0 – RS2 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green and blue data.

When accessing the color palette RAM, the address register resets to 00H following a blue read or write cycle to RAM location FFH. When accessing the overlay color registers, the address register increments following a blue read or write cycle. However, while accessing the overlay color registers, the four most significant bits of the address register (ADDR4 – 7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G and B in the block diagram) are synchronized by internal logic and occur in the period between MPU accesses. As only one pixel clock cycle is required to complete the transfer, the color palette RAM and overlay registers may be accessed at any time with no noticeable disturbance on the display screen.

To keep track of the red, green and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table II. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle (ADDR0 – 7), are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as shown in Table II. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Figure 1 illustrates the MPU read/write timing.

	Value	RS2	RS1	RS0	Addressed By MPU
ADDRa,b (Counts Modulo 3)	00				Red Value
	01				Green Value
	10				Blue Value
ADDR0 – 7 (Counts Binary)	00H – FFH	0	0	1	Color Palette RAM
	XXXX 0000	1	0	1	Reserved
	XXXX 0001	1	0	1	Overlay Color 1
	XXXX 0010	1	0	1	Overlay Color 2
	•	•	•	•	•
	•	•	•	•	•
	XXXX 1111	1	0	1	Overlay Color 15

Table II. Address Register (ADDR) Operation

ADV478 Data Bus Interface

On the ADV478, the 8/$\overline{6}$ control input is used to specify whether the MPU is reading and writing 8 bits (8/$\overline{6}$ = logical one) or 6 bits (8/$\overline{6}$ = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and also when using the ADV471), color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

ADV471 Data Bus Interface

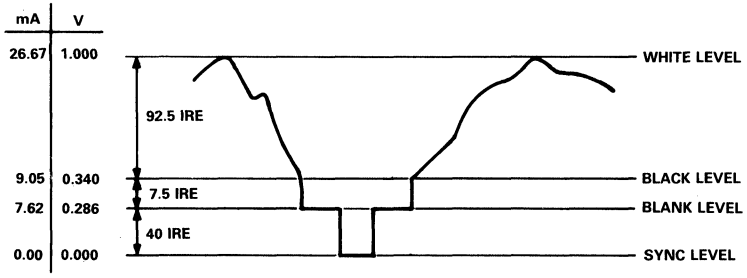
Color data is contained on the lower six bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Frame Buffer Interface

The P0 – P7 and OL0 – OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table III.

OL0 – OL3	P0 – P7	Addressed by Frame Buffer
0H	00H	Color Palette RAM Location 00H
0H	01H	Color Palette RAM Location 01H
•	•	•
•	•	•
0H	FFH	Color Palette RAM Location FFH
1H	XXH	Overlay Color 1
2H	XXH	Overlay Color 2
•	•	•
•	•	•
FH	XXH	Overlay Color 15

Table III. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = FFH)



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = V_{AA}.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 3. Composite Video Output Waveform (SETUP = V_{AA})

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	1	1	FFH
DATA	data + 9.05	1	1	data
DATA-SYNC	data + 1.44	0	1	data
BLACK LEVEL	9.05	1	1	00H
BLACK-SYNC	1.44	0	1	00H
BLANK LEVEL	7.62	1	0	xxH
SYNC LEVEL	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67mA, SETUP = V_{AA}.
External voltage or current reference adjusted for 26.67mA full-scale output.

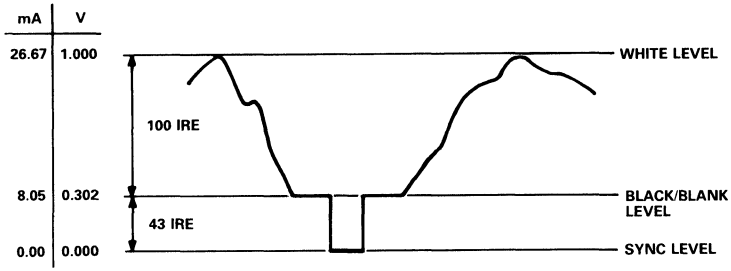
Table IV. Video Output Truth Table (SETUP = V_{AA})

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0 – P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the ADV471) of color information to the three D/A converters.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables IV and V detail how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used.

The analog outputs of the ADV478 and ADV471 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω coaxial cable.



NOTES
1. CONNECTED WITH A 75Ω DOUBLY TERMINATED LOAD, SETUP = GND.
2. EXTERNAL VOLTAGE OR CURRENT REFERENCE ADJUSTED FOR 26.67mA FULL-SCALE OUTPUT.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 4. Composite Video Output Waveform (SETUP = GND)

Description	I_{OUT} (mA)[1]	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	1	1	FFH
DATA	data + 8.05	1	1	data
DATA-SYNC	data	0	1	data
BLACK LEVEL	8.05	1	1	00H
BLACK-SYNC	0	0	1	00H
BLANK LEVEL	8.05	1	0	xxH
SYNC LEVEL	0	0	0	xxH

NOTES
[1]Typical with full-scale IOG = 26.67mA, SETUP = GND
External voltage or current reference adjusted for 26.67mA full-scale output.

Table V. Video Output Truth Table (SETUP = GND)

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the ADV478/ADV471 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV478/ADV471 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the ADV478/ADV471, the analog output traces and all the digital signal traces leading up to the ADV478/ADV471.

Power Planes

The ADV478/ADV471 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figures 5 and 6. This bead should be located within three inches of the ADV478/ADV471.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV478/ADV471 power pins and current/voltage reference circuitry.

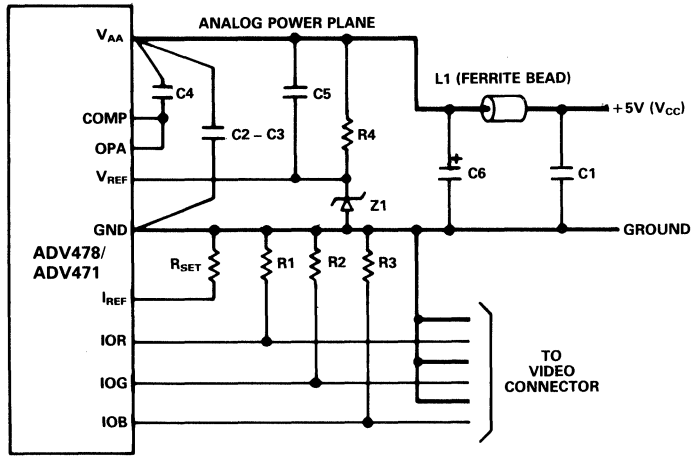
Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1μF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV478 and ADV471 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1μF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10μF Tantalum Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75Ω 1% Metal Film Resistor	Dale CMF-55C
R4	1kΩ 5% Resistor	
R_{SET}	1% Metal Film Resistor	Dale CMF-55C
Z1	1.2V Voltage Reference	Analog Devices AD589KH

Figure 5. Typical Connection Diagram and Component List (External Voltage Reference)

Digital Signal Interconnect

The digital inputs to the ADV478/ADV471 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV478/ADV471 should be avoided to reduce noise pickup.

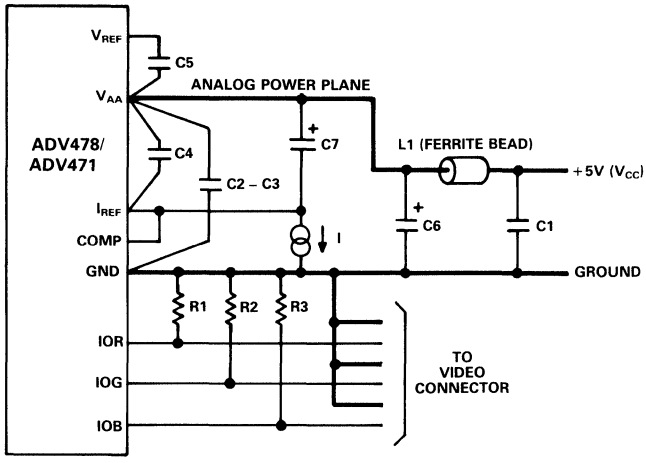
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV478/ADV471 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the ADV478/ADV471 to minimize reflections.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1μF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10μF Tantalum Capacitor	Mallory CSR13G106KM
C7	47μF Tantalum Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead	Fair-Rite 2743001111
R1, R2, R3	75Ω 1% Metal Film Resistor	Dale CMF-55C

Figure 6. Typical Connection Diagram and Component List (External Current Reference)

APPLICATION INFORMATION

External Voltage vs. Current Reference

The ADV478/ADV471 is designed to have excellent performance using either an external voltage or current reference. The voltage reference design (Figure 5) has the advantages of temperature compensation, simplicity, lower cost and provides excellent power supply rejection. The current reference design (Figure 6) requires more components to provide adequate power supply rejection and temperature compensation (two transistors, three resistors and additional capacitors).

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that the DAC outputs be connected to a singly terminated 75Ωload. If the ADV478/ADV471 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads.

If driving a large capacitive load (load RC> $1/(2\pi f_C)$), it is recommended that an output buffer (such as a MC1378 with an unloaded gain>2) be used to drive a doubly terminated 75Ω load.

ANALOG DEVICES

High Resolution 16- and 18-Bit Digital-to-Analog Converters

DAC1136/DAC1138

FEATURES

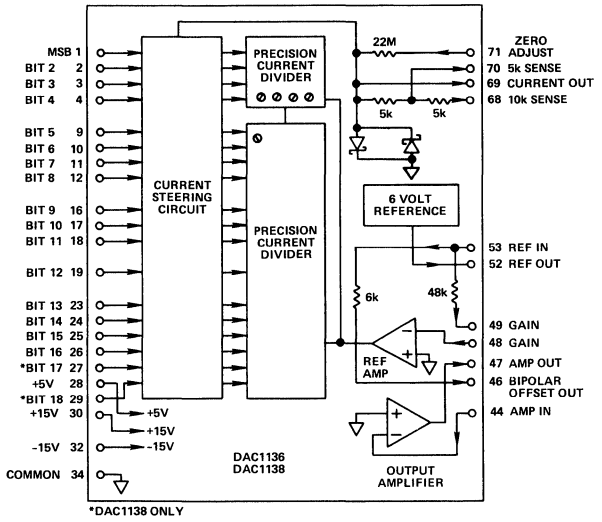
DAC1138

18-Bit Resolution and Accuracy (38μV, 1 Part in 262,144)
Nonlinearity 1/2LSB max (DAC1138K)
Excellent Stability
Settling to 1/2LSB (0.0002%) in 10μs
Hermetically-Sealed Semiconductors

DAC1136

16-Bit Resolution and Accuracy (152μV, 1 Part in 65,536)
Low Cost
Nonlinearity 1/2LSB max (DAC1136K, L)
Settling to 1/2LSB max (0.0008%) in 6μs

DAC1136/DAC1138 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC1136/1138 are complete self-contained current or voltage output modular digital-to-analog converters with resolutions and accuracies of 16 and 18 bits.

The DAC1136/1138 combine precision current sources with state-of-the-art steering switches to produce a very linear output. Inputs to these converters are compatible with TTL levels. The converters have a current output of -2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V, ±5V, or ±10V.

WHERE TO USE HIGH RESOLUTION DACS

The DAC1136/1138 deliver exceptional accuracy for a broad range of display, test and instrumentation applications. The DAC1136, with a resolution of 16 bits or 1 part in 65,536, and the DAC1138 with a resolution of 18 bits or 1 part in 262,144 are ideally suited for applications requiring wide dynamic range measurement and control. Applications include data acquisition systems, high resolution CRT displays, automatic semiconductor testing, photo-typesetting, frequency synthesis and nuclear reactor control.

CERTIFICATE OF CALIBRATION

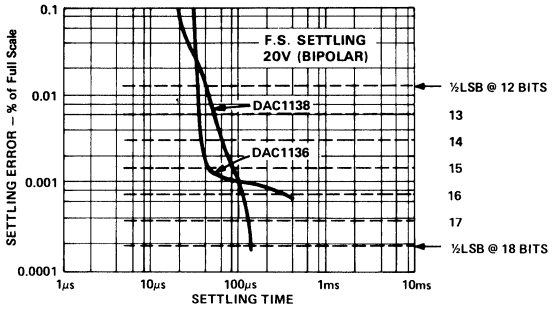
Each DAC1138 has been calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A Certificate of Performance is sent with each unit, which includes linearity test data.

SPECIFICATIONS (typical @ +25°C, rated power supplies unless otherwise noted)

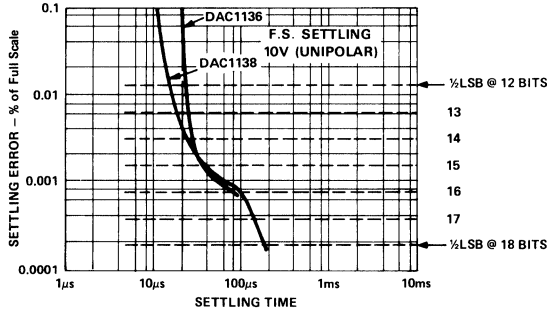
	DAC1136		DAC1138	
	J	K	J	K
RESOLUTION, BITS	16		18	
ACCURACY				
Integral Nonlinearity	±1LSB max	±1/2LSB max	±1LSB max	±1/2LSB max
Differential Nonlinearity	±1LSB max	±1/2LSB max	±1LSB max	±1/2LSB max
Gain and Offset Error (Externally Adjustable)				
ANALOG OUTPUT				
Unipolar Mode	−2mA to 0mA		−2mA to 0mA	
Bipolar Mode	−1mA to +1mA		−1mA to +1mA	
Voltage Output Range (Pin Selectable)	0 to +5V, 0 to +10V, ±5V, ±10V		0 to +5V, 0 to +10V, ±5V, ±10V	
DIGITAL INPUTS	TTL/CMOS; See Figure 2		TTL/CMOS; See Figure 2	
INPUT CODES				
Unipolar Mode	Complementary Binary (COMP BIN)		Complementary Binary (COMP BIN)	
Bipolar Mode	Complementary Offset Binary (COMP OBIN)		Complementary Offset Binary (COMP OBIN)	
DYNAMIC CHARACTERISTICS				
Settling Time to 1/2LSB				
Current				
Full Scale Step	8µs		10µs	
LSB Step	6µs		8µs	
Voltage				
Unipolar (10V Step)	90µs		175µs	
Bipolar (20V Step)	250µs		140µs	
LSB Step	8µs		18µs	
Slew Rate	1V/µs		2V/µs	
TEMPERATURE COEFFICIENTS (ppm of FSR/°C)				
Integral Nonlinearity	±1	±1	±0.3	
Differential Nonlinearity	±1	±1	±0.4	
Gain (Excluding V_{REF})	±5	±5	±0.8	
Offset				
Unipolar Mode	±0.5		±0.5	
Bipolar Mode	±5		±1	
STABILITY, LONG TERM (ppm of FSR/1,000 hrs.)[1]				
Gain (Excluding V_{REF})	±5		±2	
Offset	±6		±2	
NOISE (Include V_{REF}; Double for Bipolar Mode)				
Output Current (BW = 100kHz)	0.5nA rms		0.5nA rms	
Output Voltage (BW = 0.1–10Hz)				
@ 0V (All 1's Code; "ZERO")	4µV pk-pk		4µV pk-pk	
@ 5V (MSB = 0 Code; "Half Scale")	6µV pk-pk		6µV pk-pk	
@10V (A11 0's Code; "Full Scale")	9µV pk-pk		9µV pk-pk	
Output Voltage (BW = 100kHz)	30µV rms		30µV rms	
VOLTAGE COMPLIANCE (Amplifier Offset, E_{OS})				
Max E_{OS} Allowed for Rated Accuracy	±2mV max		±200µV max	
Initial E_{OS} (Factory Adj.)	±100µV		±100µV	
E_{OS} Drift	±10µV/°C		±10µV/°C	
Current Output (pin 69)				
Voltage Protection	via Internal Schottky Diodes		via Internal Schottky Diodes	
Source Resistance				
Unipolar Mode	>33kΩ		>33kΩ	
Bipolar Mode	>5kΩ		>5kΩ	
Source Capacitance	150pF		150pF	
REFERENCE VOLTAGE (V_{REF})				
Voltage ($Z_{OUT} \approx 200\Omega$)	+6.000V (Maximum Error, ±0.024V)		+6.000V (Maximum Error, ±0.024V)	
Noise (BW = 0.1–10Hz)	3µV pk-pk		3µV pk-pk	
Tempco	5ppm/°C		5ppm/°C	
POWER SUPPLY REQUIREMENTS[2]				
+5V dc, ±5%	9mA		9mA	
±15V dc, ±5%	±30mA		±30mA	
POWER SUPPLY REJECTION (±15V dc)				
Gain or Offset vs. FSR	80dB		80dB	
Differential Nonlinearity	±1/4LSB per Volt ΔV_S		±1/4LSB per Volt ΔV_S	
ENVIRONMENTAL				
Operating Temperature	0 to +70°C		0 to +70°C	
Storage Temperature	−55°C to +85°C		−55°C to +85°C	
Humidity	5% to 95%, Noncondensing		5% to 95%, Noncondensing	

NOTES:
[1]Recommended DNL calibration check: 6 months.
[2]Recommended Power Supply: Analog Devices Model 923.
Specifications subject to change without notice.

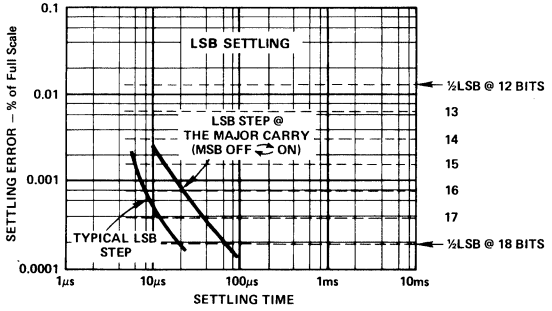
Characteristic Curves*



Settling Time (Voltage Output) vs. % of Full Scale Error for 20V Output Step (+10V⇄-10V)



Settling Time (Voltage Output) vs. % of Full Scale Error for 10V Output Step (0V⇄+10V)

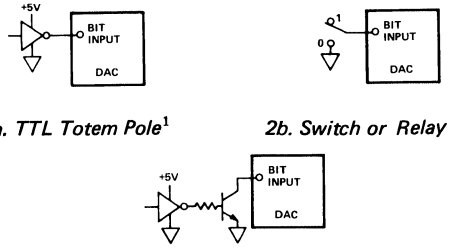


Settling Time (Voltage Output vs. % of Full Scale Error for LSB Steps

*NOTE: All curves typical at rated supply voltage.
F.S. = Full Scale

INPUT CONSIDERATIONS

The DAC1136/1138 may be driven by TTL or CMOS as shown in Figure 2. Note that the TTL input is shown with inputs for both a direct "totem pole" TTL gate and open collector (or "pull-up") configurations.



2a. TTL Totem Pole[1] *2b. Switch or Relay Input[2]*

2c. CMOS Input

1. FOR TTL WITH OPEN COLLECTOR, DO NOT USE EXTERNAL PULL-UP. CONVERTERS HAVE INTERNAL 10kΩ PULL-UP ON EACH INPUT TO 3.8V.
2. USE SPST SWITCH OR RELAY TO GROUND. WHEN SWITCH IS OPEN, THE INTERNAL 10kΩ WILL PULL INPUT UP TO 3.8V.

Figure 2. Input Connections

OUTPUT CONNECTIONS AND GUARDING

The DAC1136/1138 output connections for various voltage ranges are shown in Figure 3.

Since an LSB is only 38µV (at 10 volts full scale for the DAC1138), care must be exercised to properly guard the current output of the converter from leakage current. Any connection made to the DAC's current output (pin 69) should be guarded. Suggested printed circuit board guarding is shown in Figure 3

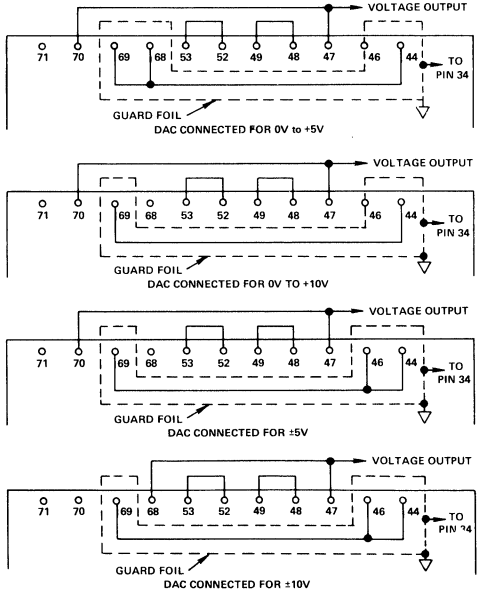
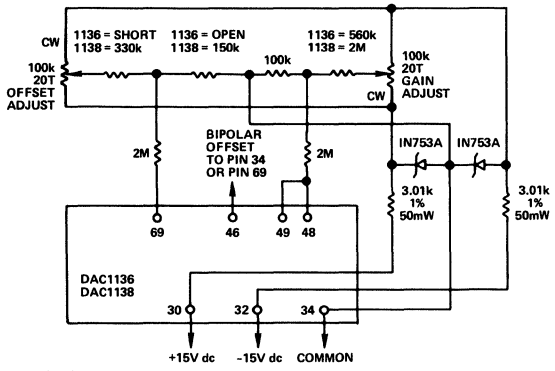


Figure 3. Output Voltage Connections and Suggested PCB Guarding (Unipolar and Bipolar)

GAIN AND OFFSET ADJUSTMENTS

The gain and offset adjustments are made with external potentiometers which the user supplies. With the appropriate digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The proper connections for offset and gain are shown in Figure 4. The voltmeter used to measure the output should be capable of stable resolution of 1/4LSB in the region of zero and full scale. Because of the interaction between offset and gain adjustments, the adjustment procedure described below should be carefully followed. Offset adjustment affects gain, but gain adjustment does not affect offset.



NOTES:
1. ALL FIXED RESISTORS ARE 5% CARBON COMP, UNLESS OTHERWISE NOTED.
2. ALL POTENTIOMETERS ARE 20-TURN INFINITE RESOLUTION TYPE.

Figure 4. Gain and Offset Adjustments

For unipolar mode, apply a digital input of all "1's" (complementary binary code for zero output) and adjust the offset potentiometer until a 0.00000V output is obtained (see Table I). Once the appropriate offset adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output is obtained (see Table I).

For bipolar mode, apply a digital input of all "1's" (complementary offset binary code for minus full scale) and adjust the offset potentiometer for the proper minus full scale output voltage (see Table I). Once the appropriate minus full scale adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output shown below is obtained.

RANGE	IDEAL OUTPUT		
		DAC1138	DAC1136
Unipolar:	All 11...1	All 00...0	
0V→+10V	0.00000V	+9.999962V	+9.999848V
0V→+5V	0.00000V	+4.999981V	+4.999924V
Bipolar:			
-10V→+10V	-10.00000V	+9.999934V	+9.999695V
-5V → +5V	-5.00000V	+4.999962V	+4.999848V
To adjust:	Adjust ZERO pot	Adjust GAIN pot	

Table I. Full Scale Output

DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1136/1138 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Before attempting recalibration, it is imperative that the circuit be checked to confirm that all previously described precautions have been taken to insure proper application at the 16- or 18-bit level. Basically, the DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusting, if necessary, for a one LSB positive difference. The top 4 major carries, i.e., MSB minus the sum of bits 2-through-the-LSB, down through bit 4 minus the sum of bits 5-through-the-LSB, can be trimmed using the procedure outlined below. A differential voltmeter capable of 100μV Full Scale should be connected to V_{OUT} of the DAC. This will resolve an LSB which at 18 bits is 38μV (10V range). A Fluke 895A or equivalent is recommended.

1. Bit 4 Trim
   a. Set bit inputs to 11110 . . . . 0.
   b. Read the output voltage by nulling the voltmeter.
   c. Set bit inputs to 11101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 1b plus 1LSB. Adjust bit 4 if required (see B4, Figure 6).

2. Bit 3 Trim
   a. Set bit inputs to 1110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set inputs to 1101 . . . . 1.
   d. Read voltage by nulling the voltmeter. This reading should be equal to that of step 2b plus 1LSB. Adjust bit 3 if required (see B3, Figure 6).

3. Bit 2 Trim
   a. Set bit inputs to 110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit inputs to 101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 3b plus 1LSB. Adjust bit 2 if required (see B2, Figure 6),

4. Bit 1 (MSB) Trim
   a. Set bit switches to 100 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit switches to 011 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 4b plus 1LSB. Adjust bit 1 (MSB) if required (see MSB, Figure 6).

If insufficient range exists on any adjustment, then a separate adjustment for the weight of bits 5-through-the-LSB (see Sum B5 → LSB, Figure 6) should be performed. This condition will probably not occur on bit 2, 3 and 4 but might occur on the MSB. If adjustment of the sum of bits 5-through-the-LSB is made, the trim procedure for all bits should be repeated. Obviously, since the procedure affects the weight of individual bits, it affects the overall gain of the DAC. The final step should be adjustment of gain (user supplied adjustment external to module).

USING AN EXTERNAL 6V REFERENCE

The DAC1136/1138 can be operated with an external reference connected to pin 53 of the module. The current drain on the external reference will be 1.125mA in bipolar mode or 0.125mA in unipolar mode (pin 46 should be left open and not grounded when using an external reference in the unipolar mode). When an external reference is used, pin 52, (the output of the internal reference) is left open.

Codi Semiconductor manufactures a reference module called Certavolt[1] with a 10 volt output accurate to 0.001%. This output is temperature compensated to within 1ppm/°C from +15°C to +55°C. The Certavolt requires a power supply of +28V dc @ 20mA. To convert the +10 volt output of the Certavolt to the +6 volt reguired by the DAC, the circuit shown in Figure 5 is recommended.

[1] Certavolt is a registered trade name by Codi Semiconductor.

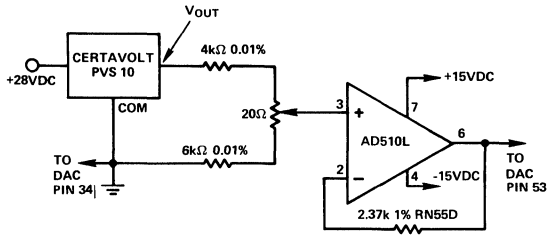
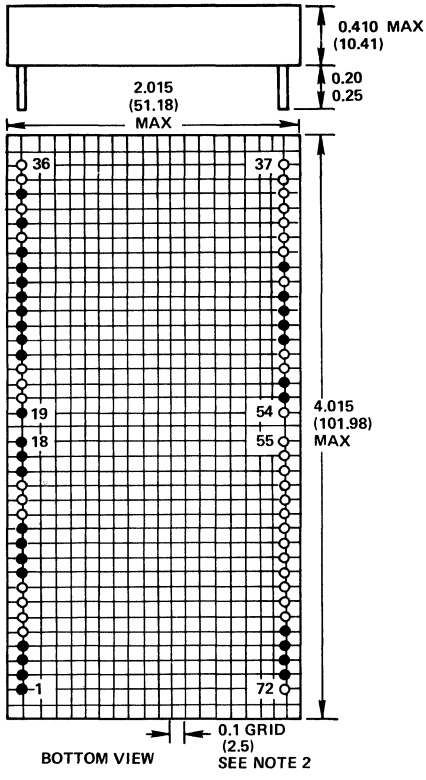
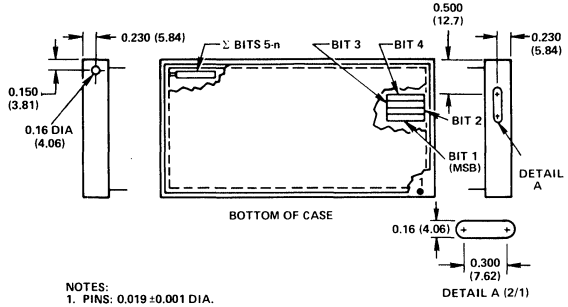


Figure 5. DAC1136/1138 with External Precision Reference

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).





NOTES:
1. PINS: 0.019 ±0.001 DIA.
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
3. PINS 27 AND 29 ARE NOT PRESENT ON DAC1136.

ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

ANALOG DEVICES

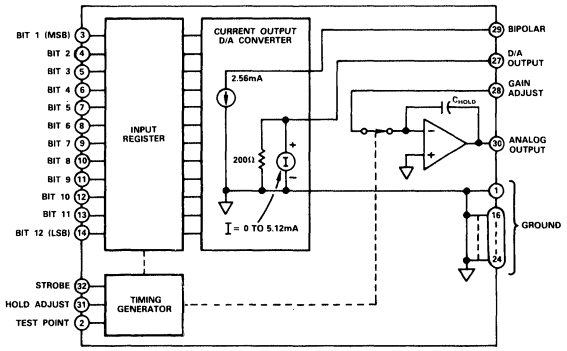
12-Bit Deglitched Voltage Out D/A Converter

HDD-1206

FEATURES
Registers, D/A, Amplifier in Single Hybrid
Deglitched Voltage Output
6MHz Update Rate

APPLICATIONS
Vector Scan Displays
Analytical Instrumentation
Digital VCOs
Military Systems

HDD-1206 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices HDD-1206 D/A converter combines innovative design techniques with remarkable hybrid construction to achieve deglitched voltage outputs at digital update rates as high as 6MHz.

Despite its small size and low power, the HDD-1206 provides the user with a complete solution to demanding applications which require the conversion of high-speed digital inputs into deglitched analog output voltages.

The unit is housed in an industry standard 32-pin hybrid and contains all the necessary circuit components to provide analog outputs at high update rates without the need for designing external circuits. Input registers, current-output D/A, deglitching circuits, and an output amplifier are all included inside the HDD-1206.

With the deglitching problem solved in a single package, the user of the HDD-1206 is able to incorporate the solution into his system with a minimum of design effort. User involvement is limited to the simple task of establishing the "hold" time for an optimum value by selecting the correct resistor value.

After that step is accomplished, the addition of a low-pass filter at the output of the D/A assures a "clean" voltage representation of the 12 bits of digital information applied to the inputs at video update rates.

The HDD-1206 is available in 32-pin dual in-line ceramic packages.

PIN DESIGNATIONS
HDD-1206

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	17	GROUND
2	TEST POINT	18	GROUND
3	BIT 1 (MSB)	19	GROUND
4	BIT 2	20	GROUND
5	BIT 3	21	GROUND
6	BIT 4	22	GROUND
7	BIT 5	23	GROUND
8	BIT 6	24	GROUND
9	BIT 7	25	+15V
10	BIT 8	26	−15V
11	BIT 9	27	D/A OUTPUT
12	BIT 10	28	GAIN ADJUST
13	BIT 11	29	BIPOLAR
14	BIT 12 (LSB)	30	OUTPUT
15	+5V	31	HOLD ADJUST
16	GROUND	32	STROBE

SPECIFICATIONS (typical @ +25°C with nominal power supplies and 1kΩ output load unless otherwise noted)

Model	HDD-1206JW			HDD-1206SM			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION		12			*		Bits
LSB WEIGHT (FS = 10.24V)		2.5			*		mV
ACCURACY (Linearity)			±0.0125			*	% FS
Differential Nonlinearity		±1/2			*		LSB
Zero Offset[1] (Initial)		±35	±50		*	*	mV
Monotonicity		Guaranteed			*		
TEMPERATURE COEFFICIENTS							
Linearity		5			*		ppm/°C
Gain		60			*		ppm/°C
Offset		100			*		ppm/°C
DYNAMIC CHARACTERISTICS[2]							
Settling Time to ½LSB							
±5.12V FS Change		2			*		µs
1LSB Change		60			*		ns
Internal Current D/A		50			*		ns
Slew Rate		25			*		V/µs
Gain		Adjustable			*		V/V
DIGITAL DATA INPUTS							
Logic Compatibility		TTL(S)			*		
Logic Levels							
"1"	+2.4		+5	*		*	V
"0"	0		+0.4	*		*	V
Load (each bit)		One Standard			*		TTL(S) Load
Coding (see Table on last page)		Complementary Binary (CBN);			*		
		Complementary Offset Binary (COB)			*		
STROBE INPUT							
Logic Compatiblity		TTL			*		
Logic Levels							
"1"	+2.4		+5	*		*	V
"0"	0		+0.4	*		*	V
Load		One Standard			*		TTL Load
Risetime/Falltime (10%–90%)			15			*	ns
Width	50		.65/word rate	*		*	ns
Frequency (see chart below)			6			*	MHz
OUTPUT (see Coding Table)							
R_{FB} = 1,000Ω							
Bipolar Voltage[3]		±2.56			*		V
Unipolar Voltage		0 to −5.12			*		V
Current	8			*			mA
R_{FB} = 2,000Ω							
Bipolar Voltage		±5.12			*		V
Current	8			*		*	mA
Residual Glitch		50	100		*	*	mV
Output Impedance		0.1	1		*	*	Ω
Capacitive Loading		1,000			*		pF
POWER REQUIREMENTS							
+15V ± 3% Current		55	60		*	*	mA
−15V ± 3% Current		30	35		*	*	mA
+5V ± 5% Current		95	130		*	*	mA
Power Supply Rejection Ratio	−2		+2		*		mV/V
Power Dissipation		1.95	2.25		*	*	W
TEMPERATURE RANGE							
Operating[4]	0		+70	−55		+125	°C
Storage	−55		+125	*		*	°C
THERMAL RESISTANCE[5]							
Junction to Air, θja (free air)		32			*		°C/W
Junction to Case, θjc		13			*		°C/W
MTBF[6]							
Mean Time Between Failures					3.015×10^5		Hours
PACKAGE OPTIONS[7]							
Ceramic (DH-32A)		HDD-1206JW					
Metal (DH-32C)					HDD-1206SM		

NOTES
[1]Adjustable to zero.
[2]All dynamic characteristics are based on FS = ±5.12V; R_{FB} = 2,000Ω.
[3]With R_{FB} = 1k, analog output voltages are half those shown in Table on last page.
[4]Case Temperature.
[5]Maximum junction temperature is 150°C.
[6]Calculated per MIL-HDBK 217, Ground; Fixed; Case Temperature = 60°C.
[7]See Section 14 for package outline information.
*Specifications same as HDD-1206JW.
Specifications subject to change without notice.

THEORY OF OPERATION

The equivalent circuit for the for the HDD-1206 D/A converter is shown in functional block diagram.

The unit consists of input registers, fast-settling current output D/A, output amplifier, timing generator, and associated circuits.

The purpose of the input register circuits is to de-skew the input bits and assure their simultaneous arrival at the input of the current D/A. This is critical because time skew on the input data bits is a major contributor to discontinuities, or "glitches," in the analog output of a D/A.

The Timing Generator includes a Track & Hold circuit and generates the required internal pulses for operation whenever it receives a Strobe input pulse. See Figure 1, the HDD-1206 timing diagram.

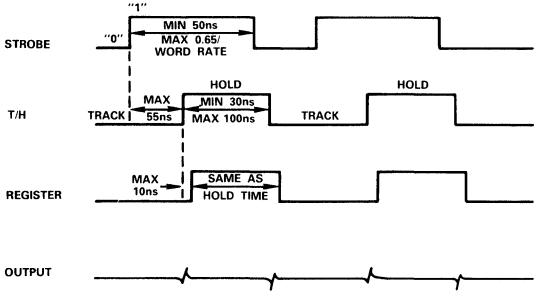


Figure 1. HDD-1206 Timing Diagram (Digital Inputs not Changing)

As shown, the Strobe pulse is a positive-going TTL pulse supplied by the user of the HDD-1206. Internal timing circuits establish the maximum 55ns delay from the leading edge of the Strobe pulse to the leading edge of the T/H (Track/Hold) pulse; and the maximum 10ns delay from the leading edge of the T/H pulse to the leading edge of the Register pulse. The data from the input registers are strobed into the current D/A at the end of this 65ns interval, so they must be valid by that time.

The user determines the width of the T/H pulse (and the Register pulse) by selecting the value of the R_{HOLD} resistor. See Figures 1 and 2. As shown, the width of the Hold pulse can vary from approximately 30ns to approximately 100ns by using resistor values from 1k to 5k, respectively.

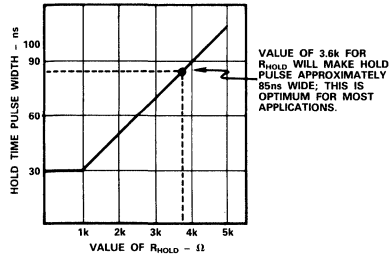


Figure 2. Hold Time vs. R_{HOLD}

For most applications, a value of 3.6kΩ and a pulse width of approximately 85ns is the optimum choice. This pulse width will "hold" the analog output of the HDD-1206 D/A until the "glitch" resulting from the most recent update has passed, without infringing on the word rate capabilities of the HDD-1206.

CURRENT-OUTPUT D/A CONVERTERS

A brief review of the salient characteristics of current D/A converters may be a useful approach to understanding the operation of the HDD-1206 unit.

Current-switching D/A converters are inherently faster than voltage-output types because of the absence of an output amplifier. This means current-switching converters have no slew rate limitation which can slow settling; nor are they subject to the overshoot and ringing problems often associated with feedback amplifiers.

Both current-switching and voltage-output converters display a discontinuity, or "glitch," in their analog outputs because of the basic characteristic of saturated logic (TTL is an example) which causes the propagation delay to be less for negative-going inputs than it is for positive-going inputs.

This difference in propagation delay manifests itself as a "worst case glitch" at the major carry point, or mid-scale, of the output range of the current converter. This is the point at which nearly equal and opposite currents are being switched within the converter.

The "glitch" at mid-scale, the switching point of the Most Significant Bit (MSB), will be halved at the ¼ and ¾ points; halved again at the ⅛ and ⅞ points, etc. The amplitude of the "glitch," therefore, is a function of signal dynamics and cannot be eliminated with filtering.

The variations in glitch amplitude caused by signal dynamics create a multitude of intermodulation (IM) products, some of which fall into the video pass-band as spurious signals, and increased noise level. These IM products are also relatively immune to elimination by filtering.

The amplitude of the glitch can be reduced by de-skewing the input bits; but no amount of de-skewing or filtering can negate the physics of saturated logic which cause the glitch to be generated initially.

The best solution, then, is to cause the glitch to remain a constant across the entire output range of the converter. The efficiencies of the circuit will be enhanced if the solution can also permit using the full drive capabilities of the current-output D/A in either unipolar or bipolar modes of operation.

The design approach used in the Analog Devices HDD-1206 D/A converter accomplishes these desired goals and provides voltage outputs at high update rates.

NOTES ON DEGLITCHING

Refer again to the equivalent circuit for the HDD-1206. The data bits are applied through the input register to the current-output D/A converter, which is capable of supplying up to 5.12mA of output current.

The output of the current D/A, in turn, is applied to the input of the output amplifier via strapping external to the HDD-1206. The Timing Generator supplies the necessary pulses and timing to apply signals to the current D/A and output amplifier after the initial glitch caused by the digital inputs has subsided.

The digital "1" (Hold) level of the T/H pulse causes the switch at the input of the amplifier to open, holding the last value of the current D/A converter. During this hold interval, the switching transients caused by updating digital inputs are masked from the amplifier, thereby avoiding HDD-1206 output discontinuities whose amplitude would be a function of signal dynamics.

Ten nanoseconds after the T/H pulse goes to the digital "1" level, the register pulse also changes state from "0" to "1".

This transition moves the output of the current D/A to the new value established by the most recent digital inputs applied to the HDD-1206.

Any change in the current D/A output has stablized by the time the T/H pulse returns to the digital "0" (Track) level. Re-establishing the track mode closes the switch at the input of the amplifier and the output of the HDD-1206 moves to the new analog value dictated by the digital input word.

As shown in Figure 1, the output of the HDD-1206 will contain switching transients associated with the T/H pulse. But these "glitches" will be constant in amplitude and duration and will occur at the update rate, since they are a function of the strobe pulse applied by the user.

These switching transients will settle out in approximately 500ns, and will have uniform amplitude over the complete analog output range of the D/A. For strobe rates of 2MHz and above, the settling interval switching from "hold" to "track", and vice versa, will produce a constant dc offset on the output. The HDD-1206 is not intended to get rid of all glitches per se; it is designed to provide a constant-amplitude glitch.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line, i.e., a single-line spectrum at the sample rate frequencies, and harmonics of the sample frequency.

The HDD–1206 effectively eliminates the IM products discussed above. When it does, the signal-to-noise (S/N) ratio approaches that of an ideally-quantized signal, where the rms noise is $q/\sqrt{12}$, when frequencies above Nyquist are filtered out.

GLITCH VS. PEDESTAL

In addition to the "glitch" which is a characteristic of current D/As, the track & hold used in the HDD-1206 also contributes an anomaly to the output signal.

Refer to Figure 3. This diagram compares the "glitch" created by the HDD-1206 to the pedestal created by the internal T/H circuits.

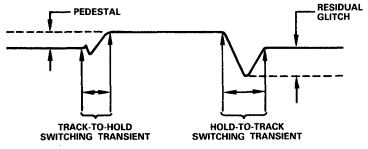


Figure 3. Pedestal/Glitch Relationship

As shown, the "glitch" is a transient signal which remains constant in width and amplitude over the entire output range, at all update rates. The pedestal, on the other hand, is an offset signal whose amplitude can vary (because of switching transient settling) as a function of hold time and word rate.

This pedestal is caused by charge transfer associated with the hold capacitor; the transfer occurs when the HDD-1206 circuits are switched from a "track" to "hold" condition. The pedestal is basically an offset error in the HDD-1206 output and can be compensated with the Offset Adjust when the unit is installed in the user's system.

Figure 3 is not drawn to scale; there is no attempt to imply the identified elements have precisely that relationship to one another. They are exaggerated for illustrative purposes.

Applications

Bipolar connections for the HDD-1206 D/A converter are shown in Figure 4. As indicated, a unipolar negative output is accomplished by connecting Bipolar Pin 29 to ground, instead of to Pins 27 and 28.

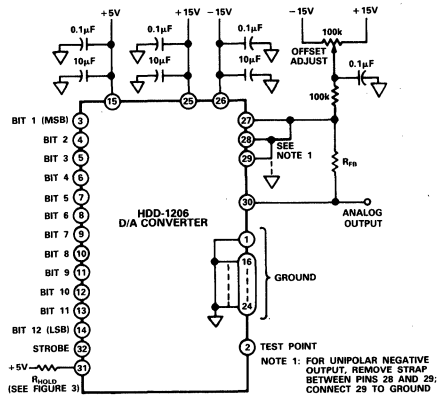


Figure 4. HDD-1206 Bipolar Connections

The output voltage swing is established by the value of feedback resistor R_{FB}. The table below indicates output levels for both unipolar and bipolar operation, with feedback resistors of either 1,000Ω or 2,000Ω.

Hold resistor R_{HOLD} connected between the +5V supply and Pin 31 sets the width of the Hold mode of the T/H pulse. Test Point Pin 2 is used for observing the pulse.

The Offset Adjust potentiometer is used to set the desired analog output of the HDD-1206 and can be used to help assure correct voltages are present when the D/A is installed in the system.

When operated in a unipolar mode with digital "0" applied to all inputs but no continuous strobe pulses applied, the Offset Adjust is set for an analog output of −5.12V or less 1LSB, with 1k for the value of R_{FB}. (NOTE: At least one strobe pulse needs to be applied to latch the input data into the registers.)

If the HDD-1206 is installed in a system and the strobe pulse is applied continuously, the Offset Adjust is calibrated for the desired output value with a digital "0" applied to all input pins.

HDD-1206 ANALOG OUTPUT WITH 1kΩ LOAD

Digital Inputs	Complementary Offset Binary (COB) Bipolar Output R_{FB} = 2k	Complementary Binary (CBN) Unipolar Negative Output R_{FB} = 1k
111...111	+5.12 (+FS)	0.0000 (0)
111...110	+5.1175	− 0.00125 (+1LSB)
110...000	+2.5625 (+1/2FS)	− 1.27875
101...111	+2.56	− 1.28 (1/4)
100...000	+0.0025 (+1LSB)	− 2.55875
011...111	0.0000	− 2.56 (1/2)
010...000	−2.5575 (−1/2FS)	− 3.83875
001...111	−2.56	− 3.84 (3/4)
000...001	−5.1150	−5.1175
000...000	−5.1175 (−FS − 1LSB)	−5.11875 (FS − 1LSB)

ORDERING INFORMATION

Model HDD-1206JW D/A converter is housed in a ceramic package, the model HDD-1206SM is a hermetically sealed version; outline dimensions are shown elsewhere.

Mating individual pin sockets are available from AMP. Part number 6-330808-0 are knockout end type; 6-330808-3 are open end type.

ANALOG DEVICES

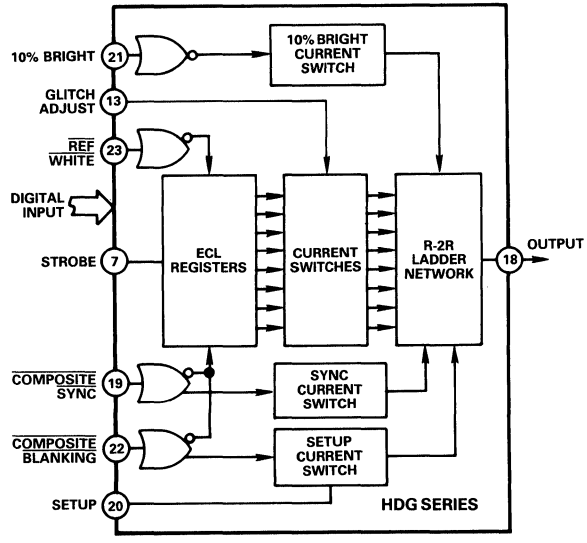
Hybrid Video Digital-to-Analog Converters

HDG Series

FEATURES
- **Update Rates to 150MHz**
- **Low Glitch Energy**
- **Complete Composite Inputs**
- **Single −5.2V Power Supply**
- **Military Temperature Range Available**

APPLICATIONS
- **Raster Scan Displays**
- **Color Graphics**
- **Analytical Instrumentation**
- **TV Video Reconstruction**

HDG SERIES FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

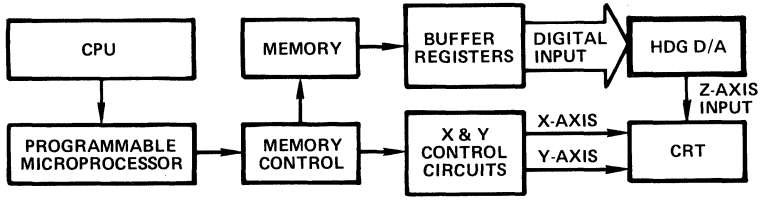
The HDG-Series D/A Converters have become the standard of comparison for fast-settling D/As with complete composite inputs. The HDG-0805 is an eight-bit (256 Gray levels) device.

All versions have complete composite controls, including self-contained, digitally-controlled sync and blanking; and a reference white control input to help assure compatibility with EIA Standards RS-170, RS-330, and RS-343-A. Their performance is enhanced even more with a 10% bright input capability.

Output inpedance is 75 ohms and their full-scale output current is capable of developing standard video levels across video loads. In addition to all of these characteristics which make them easy to incorporate into circuits, the need for a single −5.2V power supply also adds to their attractiveness.

The model number without a suffix designates the "original" HDG Series D/A Converter and is housed in 24-pin metal packages. The model numbers with suffixes make use internally of the Analog Devices Model AD9700 to obtain better performance; these devices are housed in ceramic DIP packages.

The "BD" and "BW" versions in the newer (suffixed) units are close equivalents to the original design, but a number of advantages accrue by using the newer units. Note particularly the parameters for linearity tempco; strobe input loading; Composite Sync and Composite Blanking outputs; Power Supply Rejection Ratio (PSRR); supply current; and power dissipation. Conversely, the original design is slightly better in terms of voltage settling time, glitch energy, and output compliance.



Typical Raster Scan Display System

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDG-0805	HDG-0805BD/ BW/SD
RESOLUTION	Bits	8	8
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Voltage (adjustable)	mV	2.5	*
Current (adjustable)	μA	67	*
ACCURACY			
(GS = Gray Scale; FS = Full-Scale)			
Linearity	± % GS	0.2	*
Differential Linearity	± % GS, max	0.2	*
Zero Offset (Initial)			
Voltage	mV, max	0.9	*
Monotonicity		Guaranteed	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C (max)	20 (35)	15 (30)
Gain	ppm/°C (max)	50 (125)	*
Zero Offset	ppm/°C (max)	10 (15)	*
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[1]			
Settling Time (0V to FS GS change)	% GS;	0.4	*
Voltage	ns (max)	8 (10)	9 (11)
Update Rate[2]	MHz (min)	150 (125)	*
Slew Rate	V/μs	200	*
Rise Time	ns	2	*
Glitch Energy[3]	pV-s	50	80
DIGITAL DATA INPUTS			
Logic Compatibility		ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading (each bit)		5pF and 50kΩ to −5.2V	*
STROBE INPUT			
Logic Compatibility		ECL	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		50pF and 5kΩ to −5.2V	5pF and 50kΩ to −5.2V
Setup Time (Data)	ns, min	2.5	*
Hold Time (Data)	ns, min	1.5	*
Propagation Delay	ns (max)	3 (4)	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS			
Logic Compatibility		ECL	*
Logic Levels			
"1"	V (min/max),	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		5pF and 50kΩ to −5.2V	*
SPEED PERFORMANCE – CONTROL INPUTS			
Settling Time to 10% of Final Value for:			
10% Bright	ns (max)	8 (10)	*
Reference White	ns (max)	8 (10)	*
Composite Sync	ns (max)	8 (10)	*
Composite Blanking	ns (max)	8 (10)	*
SETUP CONTROL			
Ground	mV (IRE Units)	0 (0)	*
Open	mV (IRE Units)	71 (10)	*
−5.2V	mV (IRE Units)	142 (20)	*
ANALOG OUTPUT			
GS Current	mA (± 1%)	0 to −17	*
GS Voltage[4]	mV	0 to −637.5	*
Compliance	V	−1.1 to +1.1	−1.2 to +0.1
Internal Impedance	Ω (min/max)	75 (71/79)	*

Parameter	Units	HDG-0805	HDG-0805BD/ BW/SD
OUTPUT – $\overline{\text{REFERENCE WHITE}}$[5]			
Current			
Logic "1"	mA (±4%)	Normal Operation	*
Logic "0"	mA (±4%)	0 or −1.9	*
Voltage			
Logic "1"	mV (±4%)	Normal Operation	*
Logic "0"	mV (±4%)	0 or −71	
OUTPUT – 10% BRIGHT[6]			
Current			
Logic "1"	mA (±5%)	−1.9	*
Logic "0"	mA (±5%)	0	*
Voltage			
Logic "1"	mV (±5%)	−71	*
Logic "0"	mV (±5%)	0	*
OUTPUT – $\overline{\text{COMPOSITE SYNC}}$[6,7]			
Current			
Logic "1"	mA (±4%)	0	*
Logic "0"	mA (±4%)	−7.6	*
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	−285	*
OUTPUT – $\overline{\text{COMPOSITE BLANKING}}$[6,7]			
(Assumes Setup is Open, Which is Equivalent to 10 IRE Units)			
Current			
Logic "1"	mA (±4%)	0	*
Logic "0"	mA (±4%)	−1.9	*
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	−71	*
POWER REQUIREMENTS			
−5.2V ±0.25V[8]	mA (max)	320 (360)	125 (140)
Power Supply Rejection Ratio	%/%	1/1	0.005/1
Power Dissipation	mW (max)	1665 (1875)	650 (730)
TEMPERATURE RANGE			
Operating (Case)[9]	°C	−25 to +85	* (BD and BW)
Operating ("SD" Case)	°C		−55 to +125
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[10]			
Junction to Air, θ_{JA} (free air)	°C/W, max	45	*
Junction to Case, θ_{JA}	°C/W, max	12	*
MTBF[11]			
Mean Time Between Failures	Hours		3.23×10^5
PACKAGE OPTIONS[12]			
M-24A		HDG-0805	
DH-24B			HDG-0805BD HDG-0805BW HDG-0805SD

For applications assistance, phone Computer Labs Division at (919) 668-9511

NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50%) points) is not included.
[2]Minimum update rates limited by full-scale settling time for useable number of bits.
Units can be updated to 150MHz with settling degradation.
[3]Glitch can be reduced with glitch adjustment.
[4]LSB value used for calibration causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform; both values are well within the output and EIA Standard RS-170 tolerances.
[5]Effect on analog output of logic "0" at $\overline{\text{Reference White}}$ input depends on 10% Bright signal input (See Table I).
[6]10% Bright, $\overline{\text{Composite Sync}}$, and $\overline{\text{Composite Blanking}}$ outputs shown add to Gray scale analog output at Pin 18 (See Table I).
[7]$\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ control signals reset input registers. $\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ should not be operated simultaneously with $\overline{\text{Reference White}}$.
[8]Power supply must have less than 5mV p-p ripple.
[9]Operating temperature −55°C to +125°C on "SD" units.
[10]Maximum junction temperature = 150°C.
[11]Calculated for HDG-0805SDB using MIL HNBK-217; Ground Fixed; +25°C Ambient.
[12]See Section 14 for package outline information.

* Specification same as HDG-0405.
**Specifications same as HDG-0405BD/BW/SD.

Specifications subject to change without notice.

PIN DESIGNATIONS

Pin	Function	Pin	Function
12	GROUND	13	GLITCH ADJUST
11	BIT 8 (LSB)	14	GROUND
10	BIT 7	15	GROUND
9	BIT 6	16	GROUND
8	BIT 5	17	GROUND
7	STROBE	18	ANALOG OUTPUT
6	BIT 4	19	COMPOSITE SYNC
5	BIT 3	20	SETUP
4	BIT 2	21	10% BRIGHT
3	BIT 1 (MSB)	22	COMPOSITE BLANKING
2	−5.2V	23	REFERENCE WHITE
1	GROUND	24	−5.2V

NOTE: Connect Pins 1, 12, and 14–17 together and to low-impedance ground plane as close to case as possible.

USING HDG-SERIES UNIT FOR RASTER SCAN

Refer to the block diagram of the HDG-Series D/A Converter and the idealized composite output waveform.

The digital input bits represent the Gray Scale values (the discrete levels between Reference Black and Reference White) in a composite video signal. There are 256 (2^8) of these levels.

The input bits are applied to Pins 3–6 or Pins 8–11 of the HDG-0805.

The output analog signal (at Pin 18) will be a function of these digital inputs. The output will also be affected by the ECL levels at the control inputs of 10% Bright, Reference White, Composite Sync, and Composite Blanking; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs, and various combinations of control inputs are selected.

Refer to Table I.

DIGITAL INPUTS VS. ANALOG OUTPUT

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	10% BRIGHT	REF. WHITE	BLANKING	COMP. SYNC	ANALOG OUTPUT IN mV[1] (HDG-0805BD/BW/SD)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.5[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.5mV[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.5mV[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.5mV[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.5mV[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.5mV[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.5mV[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.5mV[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.5mV[4]

NOTES

[1]Values are for Gray Scale output of 8-bit D/A's.

[2]Setup (Pin 20) grounded. (0 IRE units)

[3]Setup (Pin 20) open. (10 IRE units)

[4]Setup (Pin 20) to −5.2V (20 IRE units)

Actual analog output value of −637.5mV is different from ideal value of −643mV because of LSB value used in calibration.

Table I. Digital Inputs vs. Analog Output

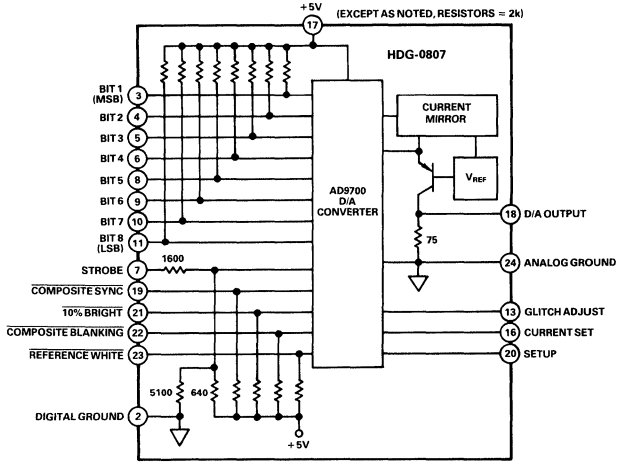
Hybrid Video Digital-to-Analog Converter

HDG-0807

FEATURES
- Update Rates to 50MHz
- Low Glitch
- Complete Composite Inputs
- Single +5V Power Supply
- TTL-Compatible Inputs
- Directly Drives 75Ω to Ground

APPLICATIONS
- Raster Scan Displays
- Color Graphics
- Analytical Instrumentation
- TV Video Reconstruction

HDG-0807 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

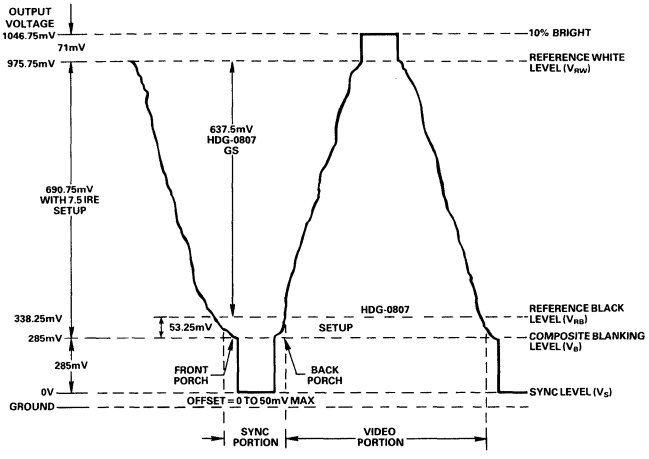
The HDG-0807 D/A Converters are extensions of the technology and capabilities of the HDG-Series high-speed raster scan D/A converters. They offer the user increased flexibility because of their ability to operate on a single +5V power supply, and their compatibility with TTL signals.

The HDG-0807 is an eight-bit (256 levels) device.

Both versions have complete composite controls, including self-contained, digitally-controlled sync and blanking; and a reference white control input to help assure compatibility with EIA Standards RS-170, RS-330, and RS-343-A. Performance is enhanced even more with a 10% bright input capability.

Output impedance is 75Ω and the full-scale output current is capable of developing standard video levels across video loads. An output current mirror shifts the output to ground reference while attenuating power supply noise by means of common-mode rejection.

Model numbers with "BW" suffixes are housed in 24-pin non-hermetic ceramic dual-in-line packages. Versions with "BD" suffixes are housed in hermetically-sealed ceramic DIP packages.



HDG-0807 Composite Waveform

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDG-0807BD/BW
RESOLUTION	Bits	8
LEAST SIGNIFICANT BIT (LSB) WEIGHT		
Voltage (adjustable)	mV	2.5
Current (adjustable)	μA	67
ACCURACY		
(GS = Gray Scale; FS = Full-Scale)		
Linearity	±% GS	0.2
Differential Linearity	±% GS, max	0.2
Zero Offset (Initial)		
Voltage	mV, max	50
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C (max)	15 (30)
Gain	ppm/°C (max)	350 (1,000)
Zero Offset	mV/°C (max)	1.0 (2.0)
DYNAMIC CHARACTERISTICS – GS OUTPUT[1]		
Settling Time	% GS;	0.4
1LSB Midscale Voltage Change	ns (max)	14 (16)
0V to FS GS Voltage Change	ns (max)	15 (18)
Slew Rate	V/μs	250
Rise Time	ns	2.2
Glitch Impulse[2]	pV-s	50
DIGITAL DATA INPUTS		
Logic Compatibility		TTL
Coding		Binary (BIN)
Logic Levels[3]		
"1"	V (min/max)	(+3.8/+5.0)
"0"	V (min/max)	(0/+3.0)
Loading (each bit)		5pF and 2kΩ to +5V
Data Update Rate	MHz (Guaranteed)	50 (45)
STROBE INPUT		
Logic Compatibility		TTL
Logic Levels		
"1"	V (min/max)	(+2.5/+5.0)
"0"	V (min/max)	(0/+1.5)
Loading		1pF and 2.2kΩ to +4.4V
Setup Time (Data)	ns, min	3
Hold Time (Data)	ns, min	3
Propagation Delay	ns (max)	8
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS		
Logic Compatibility		TTL
Logic Levels		
"1"	V (min/max)	(+3.8/+5)
"0"	V (min/max)	(0/+3.5)
Loading		5pF and 2kΩ to +5V
SPEED PERFORMANCE – CONTROL INPUTS		
Settling Time to 10% of Final Value for:		
10% Bright	ns (max)	15
Reference White	ns (max)	15
Composite Sync	ns (max)	15
Composite Blanking	ns (max)	15
SETUP CONTROL		
+5V	mV (IRE Units)	0 (0)
Open	mV (IRE Units)	53.25 (7.5)
ANALOG OUTPUT		
GS Voltage p-p[4]	mV (±4%)	637.5
Compliance	V	−3 to +3
Internal Impedance	Ω (min/max)	75 (71/79)

Parameter	Units	HDG-0807BD/BW
OUTPUT – $\overline{\text{REFERENCE WHITE}}$[5]		
(Assumes Setup is Open, Which is Equivalent to 7.5 IRE Units)		
Voltage		
Logic "1"	mV (±4%)	Normal Operation
Logic "0"		
$\overline{\text{10% Bright}}$ @ "0"	mV	1046.75
$\overline{\text{10% Bright}}$ @ "1"	mV	975.75
OUTPUT – $\overline{\text{10% BRIGHT}}$[6]		
Voltage		
Logic "1"	mV (±4%)	0
Logic "0"	mV (±4%)	71
OUTPUT – $\overline{\text{COMPOSITE SYNC}}$[6,7]		
Voltage		
Logic "1"	mV (±4%)	0
Logic "0"	mV (±4%)	285
OUTPUT – $\overline{\text{COMPOSITE BLANKING}}$[6,7]		
(Assumes Setup is Open)		
Voltage		
Logic "1"	mV (±4%)	0
Logic "0"	mV (±4%)	53.25
POWER REQUIREMENTS		
+5V to ±0.25V	mA (max)	185 (225)
Power Supply Rejection Ratio	%/V	0.025/0.25
Power Dissipation	mW (max)	925 (1125)
TEMPERATURE RANGE		
Operating (Case)	°C	−25 to +85
Storage	°C	−55 to +150
THERMAL RESISTANCE[8]		
Junction to Air, θ_{JA} (Free Air)	°C/W, max	45
Junction to Case, θ_{JC}	°C/W, max	12
PACKAGE OPTION[9]		
DH-24B		HDG-0807BD HDG-0807BW

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NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50%) points) is not included.
[2]Glitch can be reduced with glitch adjustment.
[3]Internal 2k pull-up resistors help assure compatibility with logic levels of multiple TTL families.
[4]LSB value used for calibration causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform; both values are well within the output and EIA Standard RS-170 tolerances.
[5]Effect on analog output of logic "0" at Reference White input depends on 10% Bright signal input.
[6]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray scale analog output at Pin 18 and are measured with respect to sync level (V_S) shown in waveform.
[7]Composite Sync or Composite Blanking control signals reset input registers. Composite Sync or Composite Blanking should not be operated simultaneously with Reference White, which sets input registers.
[8]Maximum junction temperature = 150°C.
[9]See Section 14 for package outline information.

Specifications subject to change without notice.

PIN DESIGNATIONS
(As Viewed from Bottom)

Pin	Function	Pin	Function
24	ANALOG GROUND	1	+5V
23	$\overline{\text{REFERENCE WHITE}}$	2	DIGITAL GROUND
22	$\overline{\text{COMPOSITE BLANKING}}$	3	BIT 1 (MSB)
21	$\overline{\text{10% BRIGHT}}$	4	BIT 2
20	SETUP	5	BIT 3
19	$\overline{\text{COMPOSITE SYNC}}$	6	BIT 4
18	ANALOG OUTPUT	7	STROBE
17	+5V	8	BIT 5
16	+5V	9	BIT 6
15	+5V	10	BIT 7
14	+5V	11	BIT 8 (LSB)
13	GLITCH ADJUST	12	+5V

NOTES: Connect Pins 2 and 24 together and to low-impedance ground plane as close to case as possible.
+5V must be applied to all designated pins.

THEORY OF OPERATION

Refer to the block diagram of the HDG-0807 D/A Converter and the HDG-0807 composite output waveform.

The digital input bits represent the Gray Scale values (the discrete levels between Reference Black and Reference White) in a composite video signal. For HDG-0807 units, there are 256 (2^8) levels.

Input bits are applied to Pins 3-6 and Pins 8-11 for the HDG-0807.

The output analog signal (at Pin 18) will be a function of these digital inputs. The output will also be affected by the TTL levels at the control inputs of $\overline{\text{10\% Bright}}$, $\overline{\text{Reference White}}$, $\overline{\text{Composite Sync}}$, and $\overline{\text{Composite Blanking}}$; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs, and various combinations of control inputs are selected.

Refer to Table I.

Analog Devices uses 2.5mV for weighting the LSB during calibration of the converter, which causes the full-scale 637.5mV output of the HDG-0807 to be different from the ideal 643mV output shown in the composite waveform in the RS-170 standard.

This disparity does not cause any problems in using the device, since both the ideal value and the actual value are well within the tolerances of the output and the RS-170 standard.

Referring again to the block diagram, the Strobe input applied to the HDG D/A clocks the input registers when the strobe signal makes the transition from a logic "0" to a logic "1". The purpose of the registers is to remove time skew from the digital input bits and minimize perturbations or "glitches" in the analog output signal.

A logic "0" applied to either the $\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ input resets the input registers to 00 000 000. A logic "0" signal applied to the $\overline{\text{Reference White}}$ input sets the input registers, thereby overriding the video input word. When this occurs, the analog output of the converter goes to 1046.75mV or to 975.75mV, depending upon whether or not the $\overline{\text{10\% Bright}}$ signal is also operated.

When $\overline{\text{Composite Blanking}}$ is operated, the analog output will go to a Reference Black value of 338.25mV less some amount, as determined by the voltage at Setup. The 53.25mV example used in the Specifications section of the data sheet is based on the Setup input floating, which is equivalent to 7.5 IRE units. (For this example, the analog output would be 285mV.)

APPLICATIONS

The HDG-0807 is specifically designed for operation in raster scan graphics applications, in which digital input data are being changed at a relatively high rate.

The D/A output is generally ac-coupled to the monitor, which eliminates the changing dc offset associated with the thermal drift of the level shift circuits. This offset drift, which is a function of output level, is held to a maximum of 50mV and will not affect dynamic video levels.

For optimum performance, ground pins 2 and 24 should be connected together and to a large ground plane near the unit. As indicated in the footnotes on the pin designations table, +5V must be applied to all pins which are called out to receive it.

The performance of the HDG devices can be enhanced with external bypass capacitors which will supplement the internal components. Low-frequency bypassing should be provided with 1μF (or larger) tantalum capacitors between the +5V supply pins and ground. High-frequency bypassing can be provided with ceramic capacitors of 0.1μF or larger. All bypass capacitors should be tied as closely as possible to the hybrid power supply pins.

A 200Ω potentiometer between +5V and ground with the center arm connected to Pin 13 changes the threshold of the internal current switches; this can reduce the amount of glitch from the typical 50pV-s to a lesser value when required.

For best performance, standard 24-pin hybrid sockets should be avoided. Individual pin sockets are preferable for evaluating devices and are available from Analog Devices; in final designs, the D/A should be soldered directly into the printed circuit board without sockets.

If it is necessary to route digital signals and/or strobe signals for distances greater than one inch (2.54cm), microstrip techniques should be used. Otherwise, the performance of the D/A converter may be affected adversely.

ORDERING INFORMATION

There are two versions of the 8-bit converter; both units operate over a temperature range of −25°C to +85°C. The model numbers are HDG-0807BD or HDG-0807BW. In these model numbers, the "D" in the suffix indicates a ceramic, hermetically-sealed DIP; and the "W" indicates a non-hermetic ceramic DIP.

Versions are available screened to military requirements; contact the factory for details. It is also possible to order units with synchronous functions on a "special order" basis; detailed information is available from the factory.

DIGITAL INPUTS VS. ANALOG OUTPUT

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	10% BRIGHT	REF. WHITE	BLANK-ING	COMP. SYNC	ANALOG OUTPUT IN mV[1] (HDG-0807)
1	1	1	1	1	1	1	1	0	1	1	1	1046.75
1	1	1	1	1	1	1	1	1	1	1	1	975.75
1	0	0	0	0	0	0	0	0	1	1	1	729.25
0	0	0	0	0	0	0	0	0	1	1	1	409.25
0	0	0	0	0	0	0	0	1	1	1	1	338.25
X	X	X	X	X	X	X	X	0	0	1	1	1046.75
X	X	X	X	X	X	X	X	1	0	1	1	975.75
X	X	X	X	X	X	X	X	0	1	0	1	338.25[2]
X	X	X	X	X	X	X	X	0	1	0	1	285[3]
X	X	X	X	X	X	X	X	0	1	0	0	124.25[2]
X	X	X	X	X	X	X	X	0	1	0	0	71[3]
X	X	X	X	X	X	X	X	1	1	0	0	53.25[2]
X	X	X	X	X	X	X	X	1	1	0	0	0[3]

NOTES
[1]Values are for Gray Scale output of HDG-0807 measured with respect to Sync level.
[2]Setup (Pin 20) to +5V. (0 IRE units)
[3]Setup (Pin 20) open. (7.5 IRE units)

Table I. Digital Inputs vs. Analog Output

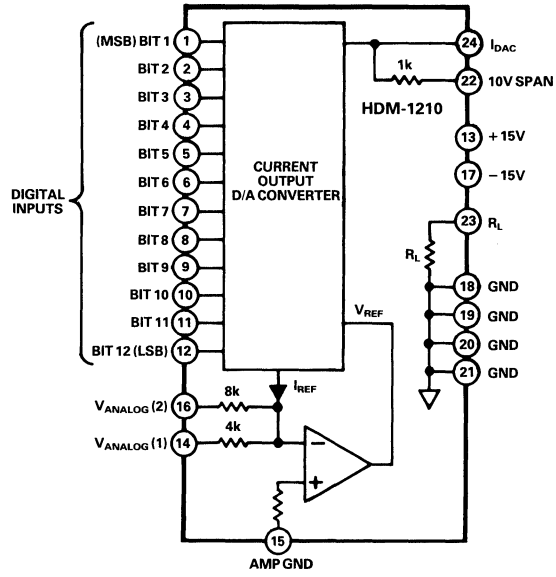
Ultrahigh-Speed Multiplying D/A Converter

HDM-1210

FEATURES
12-Bit Multiplying Accuracy
Highest Speed Available
Good Drive: 10.24mA
Small Size: 24-Pin DIP

APPLICATIONS
CRT Displays
Waveform Generation
Vector Generation
MHz-Rate Digital or Analog Attenuators

HDM-1210 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HDM-1210 D/A converter is an ultrahigh-speed current output multiplying converter which offers circuit designers a chance to obtain high speed, good drive, and flexible design parameters in a DIP package. Its output is the product of 12 bits of digital input data and the analog input(s), providing flexibility for a wide variety of applications.

Typical analog settling time to 1% is only 85ns; and 3dB analog bandwidth is 10MHz. Digital settling time to 0.1% accuracy at the major carry transition is an incredible 80ns, making the HDM-1210 D/A extremely attractive for a range of high-speed multiplying functions.

In one mode of operation, its output current is precisely proportional to the analog input signal, multiplied by the digital input code. The analog signal being multiplied can be a sine wave, triangle wave, sawtooth, or any one of a variety of complex waveforms. The output is an accurate scaled version of the input, with the digital input used as the scale factor.

In another mode of operation, the analog input voltage can be used as the scale factor for the digital input code. In addition to this kind of flexibility, the HDM-1210 also has various offsetting capabilities which allow the analog input, digital input, analog output, and/or an external amplifier to be combined. With these features, the HDM-1210 can be used to accommodate unipolar or bipolar operation; and provide either one-quadrant or two-quadrant multiplication.

SPECIFICATIONS (typical @ +25°C with nominal power supplies; V_{ANALOG} (1) = −5V; and V_{ANALOG} (2) = 0V unless otherwise noted)

Parameter	HDM-1210BD	HDM-1210SD/SDB	Units
RESOLUTION	12	*	Bits
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Current	2.5	*	μA
Voltage[1]	250	*	μV
ACCURACY (FS = Full Scale)[2]			
Differential Linearity	±1/2 (1)	*	LSB (max)
Integral Linearity	±1/2 (1)	*	LSB (max)
Gain	±0.2 (±0.5)	*	% FS (max)
Monotonicity	Guaranteed	*	
TEMPERATURE COEFFICIENTS			
Differential Linearity	±3 (±6)	*	ppm/°C (max)
Integral Linearity	±3 (±6)	*	ppm/°C (max)
Gain	±20 (±50)	*	ppm/°C (max)
Digital Offset[2,3]	±2 (±5)	*	ppm/°C (max)
Analog Offset[2,4]	±3.5 (±8)	*	ppm/°C (max)
DYNAMIC CHARACTERISTICS			
Voltage Settling Time[5]			
Digital (Major Carry Transition)			
To ±1%	35	*	ns
To ±0.1%	80 (110)	*	ns (max)
To ±0.025%	120 (170)	*	ns (max)
Analog Settling to ±1% FS			
(V_{ANALOG} (1) = 0V to −5V Step;			
All Digital Inputs (@ "1")	85 (120)	*	ns (max)
Overvoltage Recovery Time[6]	200	*	ns
Glitch Impulse	700	*	pV-s
DIGITAL DATA INPUTS			
Logic Compatability	TTL	*	
Logic Levels			
"1"	+3.5 (+2.4/+5.0)	*	V (min/max)
"0"	+0.2 (0.0/+0.6)	*	V (min/max)
Loading[7] (Each Bit; with Typical Input Logic Levels)			
TTL "1"	40/4.8	*	nA/pF
TTL "0"	1.25/4.8	*	mA/pF
Coding			
Unipolar	Binary (BIN)	*	
All "1s" Input	Max Positive Output	*	
All "0s" Input	Max Negative Output	*	
OUTPUT[8] (FS = Full Scale)			
Current Range (±1% Accurate @ FS)	0 to +10.24 FS	*	mA
Voltage Range (±1% Accurate @ FS)	0 to +1.024 FS	*	V
Digital Zero Offset[2,3]	0.5 (2.5)	*	μA (max)
Analog Zero Offset[2,4]	2.5 (10)	*	μA (max)
Voltage Noise, rms (0.1Hz to 10MHz)	15	*	μV
Compliance	+1.5; −2	*	V
Impedance[1,9]	100 (2)	*	Ω (±)
MULTIPLYING CHARACTERISTICS[10]			
V_{ANALOG} (1) Input Impedance	4 (±5.0%)	*	kΩ (max)
V_{ANALOG} (2) Input Impedance	8 (±5.0%)	*	kΩ (max)
V_{ANALOG} (1) Input Range (Pin 14):			
V_{ANALOG} (2) = 0V	0 to −5 VS	*	V
to	to		
V_{ANALOG} (2) = −5V	+2.5 to −2.5 FS	*	V
to	to		
V_{ANALOG} (2) = −10V	+5 to 0 FS	*	V
V_{ANALOG} (2) Input Range (Pin 16):			
V_{ANALOG} (1) = 0V	0 to −10 VS	*	V
to	to		
V_{ANALOG} (1) = −2.5V	+5 to −5 FS	*	V
to	to		
V_{ANALOG} (1) = −5V	+10 to 0 FS	*	V
Analog Feedthrough at I_{DAC} (Output)			
(V_{ANALOG} (1) = 5V p-p;			
All Digital Inputs @ "0")			
At 1.4MHz Input Frequency	0.024	*	% FS
At 10MHz Input Frequency	0.1	*	% FS
FS Analog Bandwidth (3dB)	10	*	MHz
POWER REQUIREMENTS			
+15V ±3%	60 (72)	*	mA (max)
−15V ±3%	25 (35)	*	mA (max)
Power Dissipation	1.3 (1.6)	*	W (max)
Power Supply Rejection Ratio	0.01 (0.05)	*	%/V (max)
TEMPERATURE RANGE			
Operating (Case)	−25 to +85	−55 to +100	°C
Storage	−55 to +150	*	°C
PACKAGE OPTION[11]			
DH-24B	HDM-1210-BD	HDM-1210SD HDM-1210SDB	

NOTES
[1] R_L (Pin 23) connected to I_{DAC} (Pin 24).
[2] Current output into short circuit.
[3] Bit inputs at "0" and V_{ANALOG} (1) @ −5V.
[4] Bit inputs at "1" and V_{ANALOG} (1) @ 0V.
[5] Settling times shown are slightly longer at low levels of analog input.
[6] Recovery time shown is for 0.5V analog overdrive at V_{ANALOG} (1) with V_{ANALOG} (2) grounded (see text).
[7] Value which is shown for digital "0" for Bits 3-12. Bit 1 = 5.0mA; Bit 2 = 2.5mA.
[8] FS accuracies are ±1% when using V_{ANALOG} (2) input.
[9] Trimmed to value.
[10] Two-quadrant and four-quadrant multiplying requires external op amp operating in bipolar mode.
[11] See Section 14 for package outline information.

*Specifications same as HDM-1210BD.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages . . . . . ±18V
Logic Inputs
Digital "1" . . . . . +7V
Digital "0" . . . . . −0.5V
Analog Inputs
V_{ANALOG} (1) . . . . . −6V
V_{ANALOG} (2) . . . . . −12V
Junction Temperature . . . . . +165°C

PIN DESIGNATIONS

(As Viewed from Bottom)

PIN	FUNCTION	PIN	FUNCTION
24	I_{DAC} (OUTPUT)	1	BIT 1 (MSB)
23	R_L	2	BIT 2
22	10V SPAN	3	BIT 3
21	GROUND	4	BIT 4
20	GROUND	5	BIT 5
19	GROUND	6	BIT 6
18	GROUND	7	BIT 7
17	−15V	8	BIT 8
16	V_{ANALOG} (2)	9	BIT 9
15	AMPLIFIER GROUND	10	BIT 10
14	V_{ANALOG} (1)	11	BIT 11
13	+15V	12	BIT 12 (LSB)

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THEORY OF OPERATION

Refer to the block diagram of the HDM-1210 D/A Converter.

The HDM-1210 uses the analog input voltages to set the reference current, designated as I_{REF} in the block diagram. Since this reference current is limited to 1.25mA, maximum inputs applied to V_{ANALOG} (1) (Pin 14) and V_{ANALOG} (2) (Pin 16) are also limited. When V_{ANALOG} (2) is open or grounded, the maximum input at V_{ANALOG} (1) is −5V; when V_{ANALOG} (1) is open or grounded, maximum input at V_{ANALOG} (2) is −10V.

If some combination of voltages in excess of those cited above is applied to the analog inputs, the analog output becomes limited to zero and remains at that value until the excessive analog input(s) is removed.

The output of the unit will not be limited if:

$$-1.25\text{mA} \leq \frac{V_{ANALOG\ (1)}}{4k} + \frac{V_{ANALOG\ (2)}}{8k} \leq 0\text{mA}$$

Permanent damage to the HDM-1210 may take place if the input at V_{ANALOG} (1) exceeds +1V with V_{ANALOG} (2) open or grounded; with V_{ANALOG} (1) open or grounded, voltage at V_{ANALOG} (2) should not exceed +2V.

The amount of overvoltage (up to the levels which may cause damage) will have an effect on the interval required for the converter to recover; the larger the overvoltage, the longer the interval. As shown in the SPECIFICATIONS section, a voltage of +0.5V overdrive is applied to V_{ANALOG} (1) when specifying recovery time.

Maximum output at I_{DAC} (Pin 24) is a function of the reference current established by the inputs; with all digital inputs at logic "1", the output current is based on the equation:

$$I_{OUT}\ (\text{max}) = I_{REF}\ (8.192)$$

where

$$I_{REF} = \frac{-V_{ANALOG\ (1)}}{4k\Omega} + \frac{-V_{ANALOG\ (2)}}{8k\Omega}$$

I_{REF} (max) is 1.25mA; therefore, maximum output current is 10.24mA.

This characteristic of the HDM-1210 means output current can be digitally adjusted, just as it is in a conventional D/A which has a variable maximum output current.

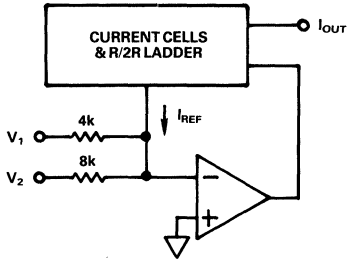


Figure 1. HDM-1210 Functional Block Diagram

There are 4,096 digital steps from zero to full-scale output for the HDM-1210, calculated with the equation:

$$I_{OUT} = (D)\ (8.192)\ (I_{REF})$$

where

D = 0 to 1 digital word in 4,096 steps (0.024%/step)

The two analog inputs at Pins 14 and 16 provide various offsetting capabilities which allow the HDM-1210 to accommodate either unipolar or bipolar input operation. When one of these inputs is properly offset to a negative voltage, the other input can be used for both negative and positive inputs. I_{REF} is still limited to 1.25mA, which limits the total output to the range from 0 to 10.24mA. Examples of outputs versus various inputs are shown in Table I.

Voltage @ V_{ANALOG} (1) (Pin 14)	Voltage @ V_{ANALOG} (2) (Pin 16)	D/A Output @ Pin 24	
		All "1" Digital Input	All "0" Digital Input
0V	Ground	0mA	0mA
−5V		+10.24mA	0mA
+2.5V	−5V	0mA	0mA
−2.5V		+1.024mA	0mA
+5V	−10V	0mA	0mA
0V		+10.24mA	0mA
Ground	0V	0mA	0mA
	−10V	+10.24mA	0mA
−2.5V	+5V	0mA	0mA
	−5V	+10.24mA	0mA
−5V	+10V	0mA	0mA
	0V	+10.24mA	0mA

Table I. Output vs. Inputs

There are two methods of obtaining a voltage output from the current output HDM-1210. The first method simply requires connecting a load resistor from Pin 24 to ground, as shown in Figure 2.

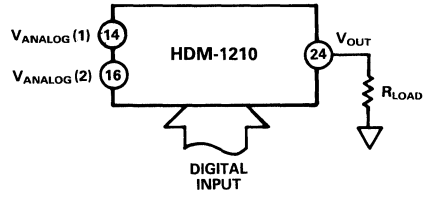


Figure 2. Passive I-to-V Converter (External Load)

The output voltage for this circuit is established by the equation $V_{OUT} = (R_{LOAD} \| R_{LADDER})\ (I_{OUT})$. R_{LADDER} is approximately 200Ω. The user must exercise care to avoid exceeding the compliance of the HDM-1210.

Alternatively, the output of the HDM-1210 can be connected to an internal load, as shown in Figure 3. This connection provides output resistance of 100Ω (±2%) and an output voltage swing of 0V to 1.024V.

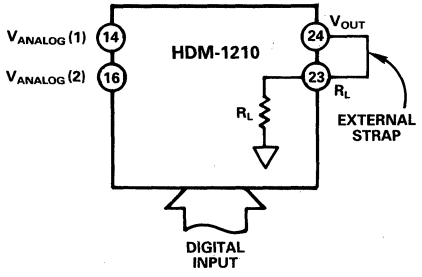


Figure 3. Passive I-to-V Converter (Internal Load)

The second method of obtaining a voltage output from the HDM-1210 D/A converter requires an external operational amplifier and a feedback resistor, as shown in Figure 4.

When the correct op amp is chosen, the output voltage from the combination shown in Figure 4 can be considerably greater than the output of an HDM-1210 operating as a passive I-to-V converter.

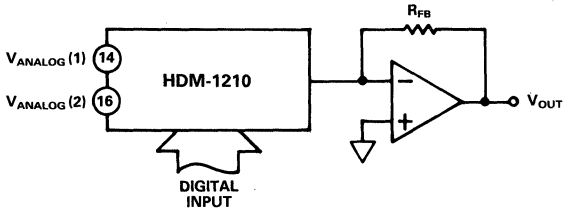


Figure 4. Active I-to-V Converter

If the Analog Devices' HOS-050A or HOS-060 operational amplifier is selected, the user will have wide output range, good drive, and easy compensation.

An internal feedback resistor of 1,000Ω in the HDM-1210 makes the circuit shown in Figure 4 capable of providing an output voltage of 0V to −10.24V.

TWO-QUADRANT ANALOG MULTIPLYING

Two HDM-1210 D/A converters can be used in combination with op amps to provide two-quadrant analog multiplying, as illustrated in Figure 5. The circuit uses standard binary coding; it will accept a bipolar input and provide a bipolar output.

The offset at the V_{ANALOG} (1) input (Pin 14) of each D/A converter allows maximum analog speed over the entire analog input range. The signal is inverted after the D/A in the lower channel, so effects of any offset are cancelled at the output of the circuit. The overall analog output range can be adjusted by changing the value of feedback resistor R_{FB} in the output driver circuit changing the value of this resistor will not affect the linearity of the circuit.

Any gain errors which may exist between the HDM-1210 D/As can be compensated by adjusting the values of R_A and R_B to match the gain of the lower channel to the gain of the upper channel.

The output voltage of the two-quadrant multiplier is calculated with the equation:

$$V_{OUT} = (D)\,(16.384)\left(\frac{V_{IN}}{8k}\right)(R_{FB})$$

where D is a digital word which varies from 0 to 1.

FOUR-QUADRANT ANALOG MULTIPLYING

Adding a feed-forward resistor, as shown in Figure 6, expands the circuit in Figure 5 to a four-quadrant multiplier whose output voltage is based on the equation:

$$V_{OUT} = \left(-\frac{R_{FB}}{R_{FF}}\right)V_{IN} + (D)\,(16.384)\left(\frac{V_{IN}}{8k}\right)(R_{FB})$$

where D is a digital word which varies from 0 to 1.

Overall, the circuit in Figure 6 uses offset binary coding; individually, the HDM-1210 D/A converters continues to use standard binary coding.

Gain error between the two channels can be adjusted by varing the values of R_A and R_B, as explained earlier. After their gains have been matched, the feed-forward resistor R_{FF} must be adjusted to match the gain of the two converters. To accomplish this, set the digital input code to 1000 000 000 000 and vary the value of R_{FF} to obtain an analog output V_{OUT} of zero volts.

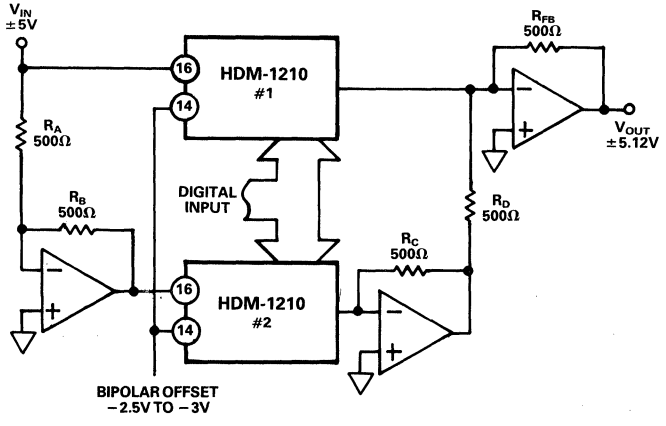


Figure 5. Two-Quadrant Analog Multiplier

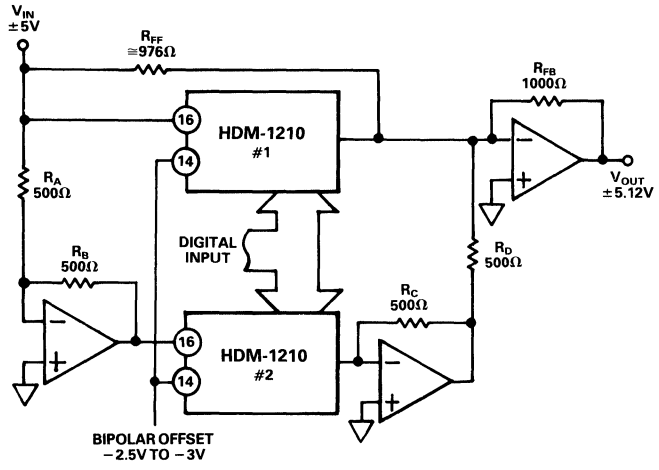


Figure 6. Four-Quadrant Analog Multiplier

The overall offset of the input signal should be fixed at zero in the four-quadrant multiplier because it cannot be cancelled out as it is in the two-quadrant version. The value of R_{FF} will be approximately 976Ω, as shown in Figure 6. The value is based on the equation:

$$R_{FF} = \frac{V\ max}{I\ max/2}$$

where V max = maximum input voltage (5V)

I max = maximum HDM-1210 output (10.24mA)

In the circuits shown in Figures 5 and 6, the recommended op amp is the Analog Devices' HOD-050A or HOS-060 operational amplifier, just as it is in Figure 4.

OUTPUT VERSUS INPUTS

Table I above lists various output currents versus several combinations of input voltages a V_{ANALOG} (1) and V_{ANALOG} (2). Additional information regarding outputs with various inputs is shown in Figure 7 through Figure 11.

In Figures 8, 10, and 11, varying outputs which are the result of changes in digital inputs are designated as follows:

Digital Input Code	BIN	OBN	Output
111 111 111 111	Full Scale	Max Positive	A
110 000 000 000	3/4 Scale	1/2 Scale Positive	B
100 000 000 000	Half Scale	Zero	C
010 000 000 000	1/4 Scale	1/2 Scale Negative	D
000 000 000 000	Zero	Max Negative	E

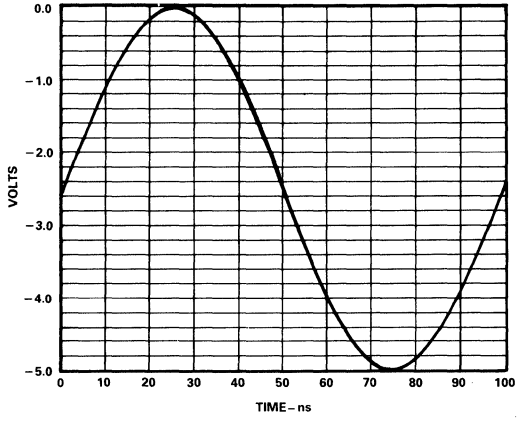


Figure 7. Input for Circuit in Figure 3

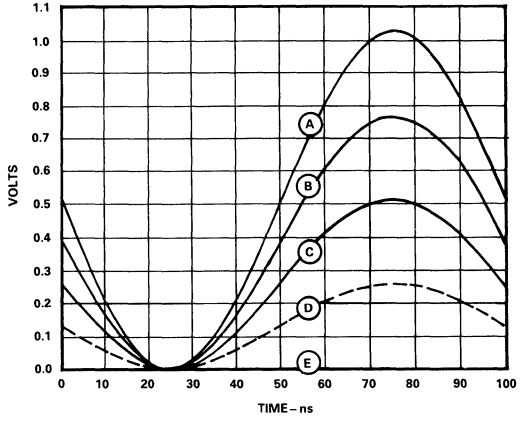


Figure 8. Outputs of Circuit in Figure 3

The input signal at V_{IN} in Figures 5 and 6 is shown in Figure 9.

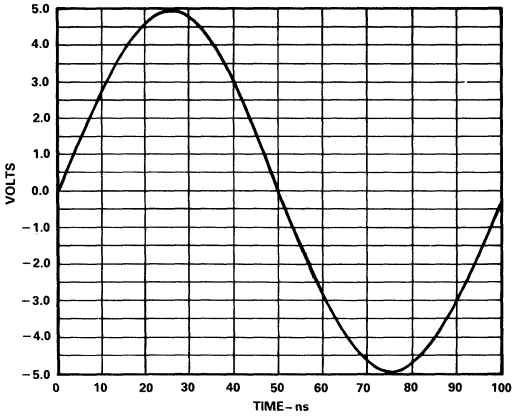


Figure 9. Inputs for Circuits In Figures 5 and 6

The outputs of the two-quadrant multiplying circuits of Figure 5 are shown in Figure 10, with the outputs labeled for various digital multiplying inputs.

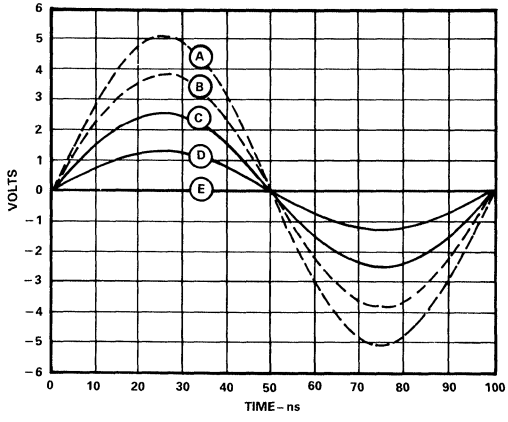


Figure 10. Outputs of Circuit in Figure 5

Refer to Figure 11.

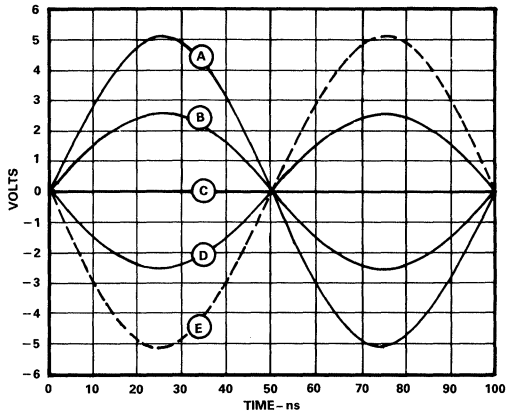


Figure 11. Outputs of Circuit in Figure 6

Four-quadrant multiplying of an analog input is shown in this illustration. The changes in output which result from variations in the digital inputs are labeled as described earlier.

SETTLING VERSUS INPUT

The SPECIFICATIONS table and footnote 5 point out digital settling time is affected by the level of the analog input signal. This characteristic of the HDM-1210 is shown in Figure 12.

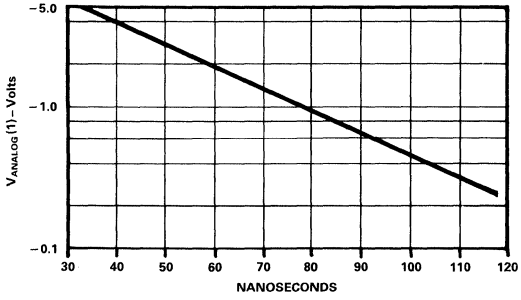


Figure 12. Digital Settling Time to ± 1%

Settling is fastest with high levels of analog input; settling time increases as levels decrease, but there is no direct ratio between the two variables.

ORDERING INFORMATION

There are three versions of the HDM-1210 D/A converter, all in hermetic ceramic DIP housings; with the exception of temperature ranges, all models meet the same electrical specifications.

The HDM-1210BD operates over a temperature range of −25°C to +85°C; the HDM-1210SD operates over a range of −55°C to +100°C. For this latter temperature range and military screening of components, order part number HDM-1210SDB; contact the factory for details.

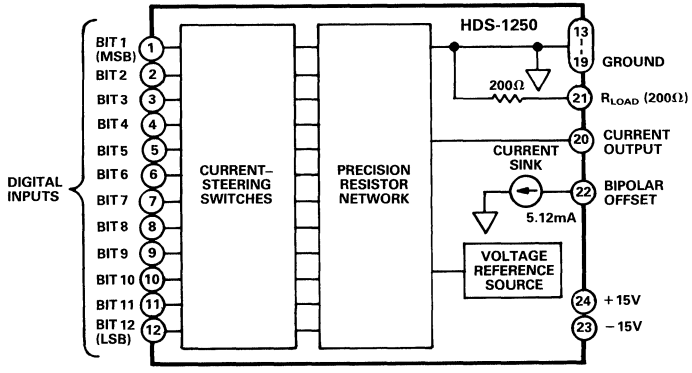
Ultrahigh-Speed 12-Bit D/A Converter

HDS-1250

FEATURES
35ns Settling Time
10mA Output Current
Monotonic Over Temperature
Available to MIL-STD-883

APPLICATIONS
Waveform Generation
Analytical and Medical Instrumentation
Military Equipment
Display Systems

HDS-1250 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HDS-1250 D/A Converter is an ultrahigh-speed current output digital-to-analog converter using reliable thin film construction in a 24-pin hermetically sealed hybrid package.

Active laser trimming assures precise 12-bit operation over a wide temperature range, and the device is guaranteed to be monotonic over its entire operating range. These characteristics and the assembly and testing in a MIL-STD-1772-certified facility make the HDS-1250 attractive for a variety of military and high-reliability applications.

Full-scale output is 10.24mA, making the converter useful for directly driving capacitive loads and transmission lines. An internal precision reference eliminates the need for external circuits for most applications.

SPECIFICATIONS (with nominal supplies, unless otherwise noted)

Parameter[1,2] (Conditions)	Sub-Group	Temp	HDS-1250KD[1] Min	Typ	Max	HDS-1250TM & TM/883B[2] Min	Typ	Max	Units
RESOLUTION (FS = Full Scale)			12			12			Bits
LSB WEIGHT				2.5			2.5		μA
ACCURACY									
√ Integral Linearity	4	+25°C		±0.25	±0.5		±0.25	±0.5	LSB
(I_{OUT}; Best Fit Line)	5,6	Full		±1.0	±1.5		±1.0	±1.5	LSB
√ Differential Linearity	4	+25°C		±0.25	±0.5		±0.25	±0.5	LSB
(I_{OUT}; All Major Carries)	5,6	Full	−1.0	±0.5	+2.0	−1.0	±0.5	+2.0	LSB
Unipolar FS									
√ Offset (Bits 1 – 12 Off)	1,2,3	Full		+0.5	+1.5		+0.5	+1.5	μA
√ Gain (Bits 1 – 12 On; I_{OUT} or V_{OUT} with Internal Load)	4	+25°C		±0.1	±0.25		±0.1	±0.25	% FS
√ Gain vs. Temperature (Bits 1 – 12 On; I_{OUT})	5,6	Full		±30	±60		±30	±60	ppm/°C
Bipolar FS									
√ Offset (Bits 1 – 12 Off; Pins 20 and 22 Connected)	4	+25°C		±0.25	±0.5		±0.25	±0.5	% FS
√ Offset vs. Temperature (Bits 1 – 12 Off; Pins 20 and 22 Connected)	5,6	Full		±15	±30		±15	±30	ppm/°C
√ Gain (Bits 1 – 12 On; Pins 20 and 22 Connected)	4	+25°C		±0.1	±0.25		±0.1	±0.25	% FS
√ Zero (Bit 1 On; Bits 2 – 12 Off; Pins 20 and 22 Connected)	4	+25°C		±0.1	±0.2		±0.1	±0.2	% FS
√ Zero vs. Temperature (Bit 1 On; Bits 2 – 12 Off; Pins 20 and 22 Connected)	5,6	Full			±75			±75	ppm/°C
DATA INPUTS									
Coding				BIN/OBN			BIN/OBN		
Logic Compatibility				TTL and 5V CMOS			TTL and 5V CMOS		
Logic Levels									
"1"		Full	+2.5			+2.5			V
"0"		Full			+0.8			+0.8	V
Logic Loading									
√ Bits 1 – 12 "1"	1	+25°C			40			40	μA
	2	+125°C			100			100	μA
	3	−55°C			40			40	μA
√ Bit 1 "0"	1	+25°C			7.0			7.0	mA
(Bits 1 – 12 @ 0.0V)	2,3	Full			7.0			7.0	mA
√ Bits 2 – 12 "0"	1	+25°C			3.5			3.5	mA
(Bits 1 – 12 @ 0.0V)	2,3	Full			3.5			3.5	mA
OUTPUT									
Current FS									
Unipolar		+25°C		10.24			10.24		mA
Bipolar		+25°C		±5.12			±5.12		mA
Voltage FS[3]									
Unipolar		+25°C		+1.024			+1.024		V
Bipolar		+25°C		±0.512			±0.512		V
Compliance		+25°C	−2.0		+1.5	−2.0		+1.5	V
Impedance		+25°C		200			200		Ω
SETTLING TIME									
Current (To ±0.025% FS)		+25°C		35			35		ns
√ Voltage (To ±0.1% FS; 1LSB step at midscale; Internal R_{LOAD})	9	+25°C			35			35	ns
POWER REQUIREMENTS									
√ +V_{SUPPLY} (Bits 1 – 12 Off; +15V)	1	+25°C			54			54	mA
	2,3	Full			54			54	mA
√ −V_{SUPPLY} (Bits 1 – 12 Off; −15V)	1	+25°C			19			19	mA
	2,3	Full			19			19	mA

(Continued on next page)

Parameter[1,2] (Conditions)	Sub-Group	Temp	HDS-1250KD[1] Min	Typ	Max	HDS-1250TM & TM/883B[2] Min	Typ	Max	Units
√Power Supply Rejection Ratio (PSRR) (Bits 1 – 12 On;	1	+25°C			0.06			0.06	%/%
± V_S = ± 14.5, ± 15.5V)	2, 3	Full			0.08			0.08	%/%
THERMAL RESISTANCE									
Junction to Case (θ_{jc})					12			12	°C/W
Case to Air (θ_{ca})[4]					34			34	°C/W
MEAN TIME BETWEEN FAILURES (MTBF)[5]						2.7×10^6			Hours
PACKAGE OPTIONS[6]									
DH-24B			HDS-1250KD			HDS-1250TM			
M-24A						HDS-1250TM/883B			

NOTES
[1]HDS-1250KD specifications preceded by a check (√) are tested at +25°C ambient temperature; performance is guaranteed over case temperature range of 0 to 70°C.
[2]HDS-1250TM and HDS-1250TM/883B specifications preceded by a check (√) are tested at −55°C case, +25°C ambient, and +125°C case temperatures unless otherwise indicated (See Subgroups).
[3]With internal 200Ω load resistor. Other voltages within the compliance range may be obtained with an external load resistor using following:

$$V_{OUT} = I_{OUT} \times R_{EQUIVALENT}$$

Where: $R_{EQUIVALENT}$ = 200Ω internal impedance in parallel with external load resistance.
[4]The relationship between the device package and outside environment (θ_{ca}) varies with the application. Value shown is based on measuring case temperature with supply voltages applied to a device in a ZIF socket mounted on a standard "EJ" burn-in board.
[5]MTBF calculated for HDS-1250TM/883B using MIL-HNBK 217D; Ground Fixed; Temperature (ambient) = 25°C.
[6]See Section 14 for package outline information.
Specifications subject to change without notice.

EXPLANATION OF SUBGROUPS

Subgroup 1 – Static tests at +25°C.
(10% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 – Static tests at maximum rated temperature.
Subgroup 3 – Static tests at minimum rated temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated temperature.
Subgroup 6 – Dynamic tests at minimum rated temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated temperature.
Subgroup 11 – Switching tests at minimum rated temperature.
Subgroup 12 – Periodically sample tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V_S) . . . . . +17V
Supply Voltage (−V_S) . . . . . −17V
Digital Inputs . . . . . 0 to +8V
Storage Temperature . . . . . −55°C to +125°C
Lead Soldering (10sec) . . . . . +300°C
Junction Temperature . . . . . +165°C

PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
24	+15V	1	BIT 1 (MSB)
23	−15V	2	BIT 2
22	BIPOLAR OFFSET	3	BIT 3
21	R_{LOAD} (200Ω)	4	BIT 4
20	OUTPUT	5	BIT 5
19	GROUND	6	BIT 6
18	GROUND	7	BIT 7
17	GROUND	8	BIT 8
16	GROUND	9	BIT 9
15	GROUND	10	BIT 10
14	GROUND	11	BIT 11
13	GROUND	12	BIT 12 (LSB)

THEORY OF OPERATION

Refer to the HDS-1250 Block Diagram.

The HDS-1250 consists of an array of high-speed, current-steering switches and a precision R2R resistor network. An internal voltage reference provides current which is switched between the digital input and the resistor network, depending on digital input level. Full-scale output current is 10.24mA, scaled by the binary digital input word.

The parallel combination of the R2R network and the internal load resistor (R_L) causes the HDS-1250 D/A Converter to have a unipolar output voltage of +1.024V. A 5.12mA current sink contained within the device provides a bipolar function (Pin 22) when it is connected to the output pin.

ANALOG OUTPUT CIRCUITS

The HDS-1250 is primarily a current-output DAC which can be operated in either a unipolar or bipolar mode. The connections for unipolar operation are shown in Figure 1.

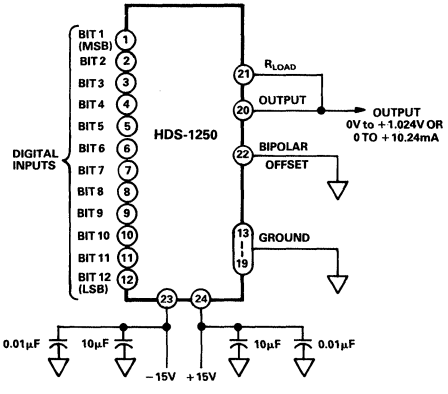


Figure 1.

When a load resistor is connected between the output (Pin 20) and ground, the HDS-1250 can also function as a voltage DAC. Its output voltage must remain within a certain tolerance or the linearity of the device will be affected adversely. This "compliance" voltage range for the HDS-1250 is −2.0V to +1.5V. The voltage output of 0V to +1.024V provided by the internal 200Ω load is well within the compliance range of the device.

Bipolar use of the HDS-1250 is illustrated in Figure 2.

An alternate way of achieving a voltage output with the HDS-1250 is to use an operational amplifier as a current-to-voltage converter on the output as shown in Figure 3.

The DAC output is connected directly to the summing node of the amplifier; the output impedance of the R2R network serves as the Thevenin equivalent feed forward resistance in the circuit.

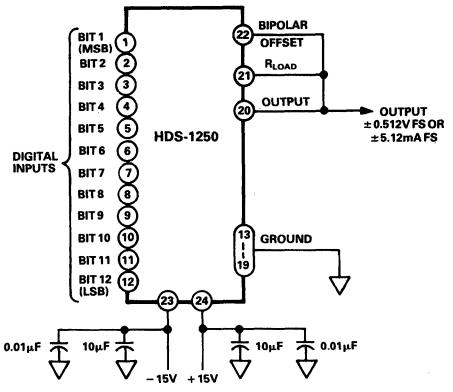


Figure 2.

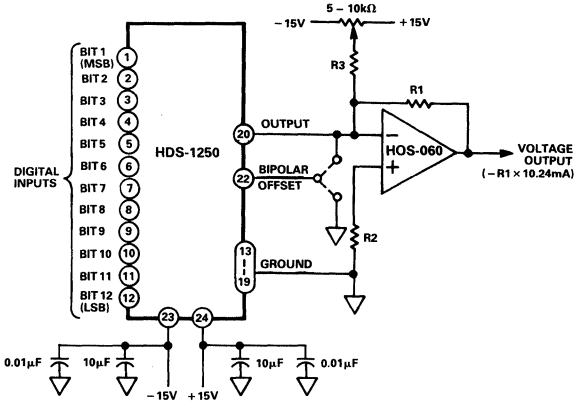


Figure 3.

This technique allows the fastest possible settling of the combination, which is approximated by:

$$T_S = \sqrt{(T_D)^2 + (T_A)^2}$$

Where: T_S = Total settling time
T_D = DAC settling time
T_A = Op Amp settling time

The gain of the amplifier can be controlled most accurately by varying the ratio between current flow through the feedback resistor (R1) and the 10.24mA current output of the DAC. The amplifier's output offset can be adjusted by sinking current from or sourcing current to the summing node through a potentiometer connected to the positive and negative supply voltages. The value of R3 in Figure 2 will be based on the desired range of adjustment.

DESIGN RULES

There are certain circuit layout rules that must be observed to obtain successful high-speed data conversion. Heavy ground currents and fast switching speeds can combine to present a formidable challenge to noise-free performance unless precautions are taken.

The foundation for a good high-speed design lies in the ground plane. The HDS-1250 should be mounted on a PC board that has one side (or layer) dedicated as a large, low-impedance ground plane. This helps ensure that ground loops and differences in ground potential do not develop in the vicinity of the DAC and erode its effective linearity.

To avoid loss of resolution due to noise, it is imperative to decouple the power supply pins of the HDS-1250 directly to the ground plane as physically close to the package as possible. Minimum decoupling should consist of a 10μF tantalum capacitor and a 0.01μF ceramic capacitor in parallel at each supply voltage pin. This will help suppress both high- and low-frequency noise components in the supply voltage.

If a voltage output op amp is used, locate it as close as practical to the DAC output to minimize the length of the summing node circuit trace. At high switching speeds, parasitic capacitance and inductance become critical factors in determining settling characteristics, and precautions must be observed to limit their effects. Any offset control functions connected to the summing node must also be as short as possible to minimize output ringing.

When selecting resistors to use as the output load or as feedback for the op amp, the designer should bear in mind that the temperature coefficient of these resistors will materially affect the overall temperature stability of the data conversion design. Resistor grades should be selected to support the allotted error budget of the system.

Output "glitches" are another anomaly that plague the success of high-speed DAC designs. These aberrations in the output are generally caused by skewing in the transition points of the parallel bit inputs. Small differences in the start of switching among the input bits cause the DAC output to try to respond with each change.

The glitches appear in the output as small triangular waveforms at the bit transitions, and are measured in terms of area as a function of voltage and time. Bit-weighting causes glitch impulse to be most significant at the Bit 1 transition, and it diminishes by half at each successive bit. This causes the amplitudes of the glitches to be code-dependent, making it virtually impossible to eliminate them with a filter.

Glitches of 100-500 pico-volt seconds are common for high-speed TTL DACs and can have an undesirable effect on the reconstructed signal purity in some applications.

There are two methods for minimizing glitch impulse in applications using the HDS-1250. In one, a set of high-speed registers in front of the bit inputs will reduce the amount of skew in the input data. These registers should be mounted physically close to the HDS-1250 package, and Bits 1-4 should be located in a single quad package.

The second method is to utilize a deglitching amplifier on the output of the DAC. See Figure 4.

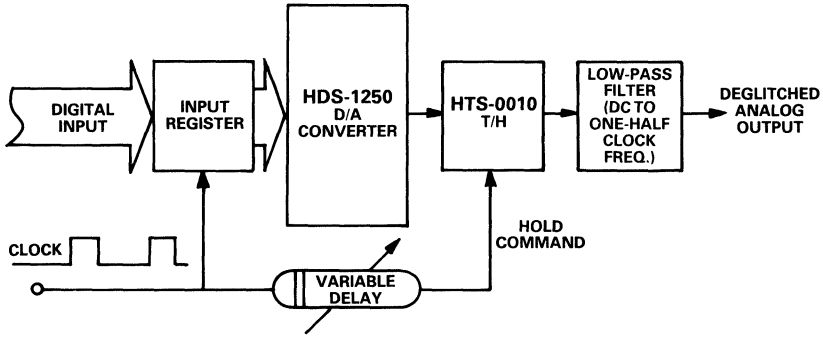


Figure 4.

This deglitching circuit includes the input registers mentioned above and a high-speed track-and-hold (T/H) amplifier. The HTS-0010 shown is timed to "hold" a constant output during the time of the glitch activity; and update the output after DAC settling has occurred.

The deglitching amplifier introduces its own switching anomalies, but they occur at the update rate of the input data and are beyond the reconstructed bandwidth of interest.

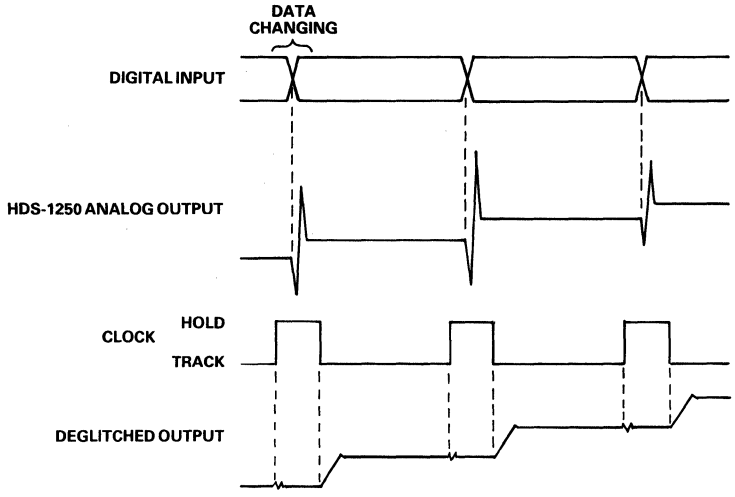


Figure 5.

These aberrations can be filtered with a bandpass filter at the output of the (T/H) deglitching amplifier. The filter should be selected to pass a frequency range from dc to one-half the DAC's update rate.

For a better insight into the timing involved, refer to Figure 5.

As shown, the analog output of the HDS-1250 will attempt to follow the switching of the digital inputs as they change; if time skew exists among the input bits, the glitches which result will be pronounced. The clock signal shown in Figure 5 serves as a strobe for the input register and also causes the T/H to switch from a "track" to "hold" mode of operation. After the glitch on the output of the HDS-1250 has subsided, the T/H will return to the track condition and slew to the new value established by the most recent digital input changes.

Minor switching transients introduced by the action of the T/H occur at the input data rates and are outside the passband of interest. Their effects can be eliminated with a bandpass filter at the output of the HTS-0010.

ORDERING INFORMATION

Three models of the HDS-1250 D/A Converter are available; all are manufactured in a MIL-STD-1772-certified facility.

Model HDS-1250KD operates over a case temperature range of 0 to +70°C; the KD suffix indicates a 24-pin hermetic ceramic DIP package.

For operating case temperatures of −55°C to +125°C, order either the HDS-1250TM or the HDS-1250TM/883B; both units are housed in hermetic 24-pin metal packages. The 883B designation indicates units which are intended for military or other high-reliability applications; these devices are manufactured and screened per the requirements of MIL-STD-883.

A/D Converters
Contents

Selection Guide
Analog-to-Digital Converters

GENERAL PURPOSE ADCs

Model	Res Bits	Conv Time µs	Int SHA BW kHz[1]	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
AD7821	**8**	**0.66**	**100**	**0–5 V, Ext**	**8, µP**	**N, P, Q**	**C, I**	**3–367**	**CMOS, Bipolar or Unipolar Operation**
AD7569	**8**	**2**	**200**	**Int**	**8, µP**	**E, N, P, Q**	**C, I, M**	**3–233**	**CMOS, Complete I/O Port with DAC, ADC, SHA, Amps and Reference**
***AD7669**	**8**	**2**	**200**	**Int**	**8, µP**	**N, P**	**C, I, M**	**3–233**	**CMOS, Complete I/O Port with 2 DACS, ADC, SHA, Amps and Reference**
AD7820	**8**	**2**	**7**	**0–5 V, Ext**	**8, µP**	**E, N, P, Q, R**	**C, I, M**	**3–357**	**CMOS, 8-Bit Sampling ADC**
***AD7769**	**8**	**2.5**	**200**	**Ext**	**8, µP**	**N, P**	**C, I**	**3–325**	**CMOS, Two-Channel ADC/DAC with Output Amplifiers**
AD7824	**8**	**2.5**	**10**	**0–5 V, Ext**	**8, µP**	**N, Q**	**C, I, M**	**3–379**	**CMOS, 4 Channel, 8-Bit Sampling ADC**
AD7828	**8**	**2.5**	**10**	**0–5 V, Ext**	**8, µP**	**E, N, P, Q**	**C, I, M**	**3–379**	**CMOS, 8 Channel, 8-Bit Sampling ADC**
AD7575	8	5	50	1.23 V, Ext	8, µP	E, N, P, Q	C, I, M	3–265	CMOS, Low Cost
AD670	**8**	**10**		**Int**	**8, µP**	**D, E, N, P**	**C, I, M**	**3–69**	**Single Supply, Including In-Amp and Reference**
AD7576	8	10		1.23 V, Ext	8, µP	E, N, P, Q	C, I, M	3–269	CMOS, Low Cost
AD570	8	25		Int	8	D	C, M	3–15	
AD673	8	30		Int	8, µP	D, N, P	C, M	3–81	
AD7581	8	66.7		−5 V—(−15 V), Ext	8, µP	D, N	C, I	3–295	CMOS 8-Bit ADC
AD579	**10**	**1.8**		**10 V, Int**	**10/Serial**	**D, N**	**C, I**	**3–63**	
AD7579	**10**	**18.5**	**25**	**2.5 V, Ext**	**8, µP**	**E, N, P, Q**	**C, I, M**	**3–279**	**CMOS, Low Cost 10-Bit Sampling ADC**
AD7580	**10**	**18.5**	**25**	**2.5 V, Ext**	**10, µP**	**E, N, P, Q**	**C, I, M**	**3–279**	**CMOS, Low Cost 10-Bit Sampling ADC**
AD571	**10**	**25**		**Int**	**10**	**D**	**C, M**	**3–15**	
AD573	**10**	**30**		**Int**	**8/10, µP**	**D, N, P**	**C, M**	**3–29**	
AD575	**10**	**30**		**Int**	**Serial**	**D, N**	**C, M**	**3–49**	
***AD9005**	**12**	**0.1**	**38000**	**Int**	**12**	**M**	**C, M**	**3–459**	**Complete 12-Bit ADC with T/H, Reference and Timing Circuitry**
CAV-1205	**12**	**0.2**	**15000**	**Int**	**12**	**Card**	**C**	**3–567**	**12-Bit, 5MSPS Eurocard**
MOD-1205	**12**	**0.5**	**15000**	**Int**	**12**	**Card**	**C**	**3–593**	**12-Bit, 5MSPS Video ADC**
AD9003	**12**	**1**	**10000**	**Int**	**12**	**M**	**C**	**3–451**	**12-Bit, 1MSPS ADC. Single 40-Pin DIP**
HAS-1201	**12**	**1**	**2000**	**Int**	**12**	**M**	**C, M**	**3–573**	**12-Bit, 1MSPS ADC**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
[5]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

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GENERAL PURPOSE ADCs

Model	Res Bits	Conv Time µs	Int SHA BW kHz[1]	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
HAS-1202A	**12**	**1.6**		**Int**	**12**	**D**	**C, I, M**	**3-579**	**12-Bit, 641kHz ADC**
HAS-1204	**12**	**2**	**7000**	**Int**	**12**	**M**	**C, M**	**3-583**	**12-Bit, 500kHz ADC. Single 40-Pin DIP**
HAS-1202	**12**	**2.9**		**Int**	**12**	**D**	**C, I, M**	**3-579**	**12-Bit, 349kHz ADC**
AD578	**12**	**3**		**10 V, Int**	**12**	**D, N**	**C, M**	**3-57**	**Complete, 3µs, 12-Bit ADC**
AD7672	**12**	**3**		**−5 V, Ext**	**12, µP**	**E, N, P, Q**	**C, I, M**	**3-309**	**CMOS, Unipolar or Bipolar, −12 V, +5 V Supply**
AD678	**12**	**4**	**X**	**5 V, Int**	**12, µP**	**D, N, P**	**C**	**3-99**	**BiMOS, High-Impedance, High-Bandwidth Sampling Input, 10 V Range**
***AD1678**	**12**	**4**	**500**	**Int**	**8/12, µP**	**D, N, P**	**C**	**3-191**	**BiMOS, 12-Bit Sampling ADC, ac Characterized**
AD5240	12	5		6.3 V, Int	12	D	C, I	3-547	Industry Standard
AD7572	**12**	**5**		**−5.25 V, Int**	**12, µP**	**E, N, P, Q**	**C, I, M**	**3-253**	**CMOS 12-Bit ADC**
AD1332	**12**	**8**	**125**	**−5 V, Int**	**12, µP**	**D**	**I**	**9-31**	**Complete 12-Bit 125kHz Sampling ADC for Digital Signal Processing**
AD7870	**12**	**10**	**X**	**3 V, Int**	**8/12/Serial, µP**	**E, N, P, Q**	**C, I, M**	**3-391**	**CMOS, 100kHz Throughput—**
AD7878	**12**	**10**	**X**	**3 V, Int**	**12, µP**	**E, N, P, Q**	**C, I, M**	**3-419**	**CMOS, 100kHz Throughput, On-Chip FIFO. Serial, Parallel or Byte Output**
***AD7772**	**12**	**10**	**X**	**5.25, Int**	**Serial, µP**	**E, N, P, Q**	**C, I, M**	**3-341**	**CMOS, Serial Output 12-Bit ADC**
***AD1334**	**12**	**15**	**235**	**−5 V, Int**	**12, µP**	**D**	**I**	**9-49**	**Four Channel 65kHz 12-Bit Sampling ADC for Digital Signal Processing**
AD ADC84	12	10		6.3 V, Int	12	D	C	3-547	Industry Standard
AD ADC85	12	10		6.3 V, Int	12	D	C, I	3-547	Industry Standard
AD5210	12	13		−10 V, Int/Ext	12	D	I, M	3-227	Industry Standard
AD674A	**12**	**15**		**10 V, Int**	**12, µP**	**D**	**C, M**	**3-89**	**Complete 12-Bit ADC**
AD368	**12**	**15**	**40–1000**	**6.3 V, Int**	**12**	**D**	**I, M**	**9-19**	**Complete 12-Bit ADC with Programmable Gains of 1, 8, 64, 512**
AD369	**12**	**15**	**40–1000**	**6.3 V, Int**	**12**	**M**	**I**	**9-19**	**Complete 12-Bit ADC with Programmable Gains of 1, 10, 100, 500**
AD572	12	25		10 V, Int	12	D, M	I, M	3-21	12-Bit Successive Approximation ADC
AD ADC80	12	30		6.3 V, Int	12	D	I	3-539	Industry Standard
AD574A	**12**	**35**		**10 V, Int**	**8/12, µP**	**D, E, N, P**	**C, M**	**3-37**	**Complete ADC with Reference and Clock**
AD363	**12**	**40**	**X**	**10 V, Int**	**12, µP**	**D**	**C, M**	**9-5**	**High Speed 16-Channel, 12-Bit DAS**
AD364	**12**	**50**	**X**	**10 V, Int**	**12, µP**	**D**	**C, M**	**9-5**	**16-Channel, 12-Bit DAS with Three-State Buffered Output**
AD5200	12	50		−10 V, Int/Ext	12	D	I, M	3-227	Industry Standard
AD7578	**12**	**100**		**5 V, Ext**	**12, µP**	**D, N**	**C, I, M**	**3-273**	**CMOS, 1LSB Total Unadjusted Error**

GENERAL PURPOSE ADCs

Model	Res Bits	Conv Time µs	Int SHA BW kHz[1]	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
AD7582	**12**	**100**		**5 V, Ext**	**12, µP**	**D, E, N, P**	**C, I, M**	**3–303**	**CMOS, 1LSB Total Unadjusted Error**
HAS-1409	**14**	**9**	**200–800**	**Int**	**14**	**M**	**C**	**3–587**	**14-Bit, 125kHz ADC. Single 40-Pin DIP**
AD679	**14**	**10**	**X**	**5 V, Int**	**14, µP**	**D, N, P**	**C**	**3–111**	**BiMOS, High Impedance, High Bandwidth Sampling Input, 10 V Input Range**
***AD1679**	**14**	**10**	**500**	**5 V, Int**	**8/14, µP**	**D, N, P**	**C**	**3–203**	**14-Bit BiMOS Sampling ADC, ac Characterized**
***AD7871**	**14**	**10**	**X**	**3 V, Int**	**8/14/Serial, µP**	**E, N, P, Q**	**C, I, M**	**3–407**	**CMOS, 14-Bit, 100kHz Sampling ADC**
ADC1131	**14**	**12**		**Int**	**14**	**Module**	**C**	**3–555**	**14-Bit, High Speed ADC**
ADC1130	**14**	**25**		**Int**	**14**	**Module**	**C**	**3–555**	**14-Bit, High Speed ADC**
DAS1152	**14**	**40**	**X**	**10 V, Int**	**16**	**Module**	**I**	**9–73**	**14-Bit High Accuracy Sampling ADC**
DAS1157	**14**	**55**	**X**	**10 V, Int**	**16**	**Module**	**I**	**9–77**	**Low Power, 14-Bit Sampling ADC**
DAS1153	**15**	**50**	**X**	**10 V, Int**	**16**	**Module**	**I**	**9–73**	**15-Bit High Accuracy Sampling ADC**
DAS1158	**15**	**55**	**X**	**10 V, Int**	**16**	**Module**	**I**	**9–77**	**Low Power, 15-Bit Sampling ADC**
***AD1377**	**16**	**10**	**X**	**Int**	**16, Serial**	**D**	**C**	**3–175**	**Complete 16-Bit Converter. Industry Standard Pin Out**
AD1376	**16**	**15**		**Int**	**16, Serial**	**V**	**C**	**3–167**	**Complete, High Speed 16-Bit ADC Operation over −25°C to +85°C**
AD1380	**16**	**20**	**900**	**Int**	**16, Serial**	**D**	**C**	**3–183**	**Low Cost, 16-Bit Sampling ADC Operation over −55°C to +85°C Temperature Range**
ADC1140	**16**	**35**		**10 V, Int**	**16**	**Module**	**C**	**3–559**	**16-Bit ADC, Operates over −25°C to +85°C Temperature Range**
AD ADC71	16	50		6.3 V, Int	16	D, M	C	3–531	Industry Standard
AD ADC72	16	50		6.3 V, Int	16	D, M	C, I	3–531	Industry Standard
DAS1159	**16**	**55**	**X**	**10 V, Int**	**16**	**D**	**I**	**9–77**	**Low Power, 16-Bit Sampling ADC**
AD1170	**18**	**1000**		**5 V, Int**	**24**	**D**	**C**	**3–147**	**7 to 22-Bit Programmable Integrating ADC**
AD1175K	**22**	**50ms**		**6.95 V, Int/Ext**	**24**	**Module**	**C**	**3–159**	**High Accuracy, 22-Bit Integrating ADC**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
[5]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

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SAMPLING ADCs

Model	Res Bits	Conv Time µs max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
AD7821	8	0.66	100	0–5 V, Ext	8, µP	N, P, Q	C, I	3–367	CMOS, Bipolar or Unipolar Operation
AD7569	8	2	200	Int	8, µP	E, N, P, Q	C, I, M	3–233	CMOS, Complete I/O Port with DAC, ADC, SHA, AMPs, & Reference
***AD7669**	8	2	200	Int	8, µP	N, P	C, I, M	3–233	CMOS, Complete I/O Port with 2 DACs, ADC, SHA, AMPs, & Reference
AD7820	8	2	7	0–5 V, Ext	8, µP	E, N, P, Q, R	C, I, M	3–357	CMOS, 8-Bit Sampling ADC
AD7824	8	2.5	10	0–5 V, Ext	8, µP	N, Q	C, I, M	3–379	CMOS, 4 Channel, 8-Bit Sampling ADC
AD7828	8	2.5	10	0–5 V, Ext	8, µP	E, N, P, Q	C, I, M	3–379	CMOS, 8 Channel, 8-Bit Sampling ADC
AD7575	8	5	50	1.23 V, Ext	8, µP	E, N, P, Q	C, I, M	3–265	CMOS, Low Cost
AD7579	10	18.5	25	2.5 V, Ext	8, µP	E, N, P, Q	C, I, M	3–279	CMOS, Low Cost 10-Bit Sampling ADC
AD7580	10	18.5	25	2.5 V, Ext	10, µP	E, N, P, Q	C, I, M	3–279	CMOS, Low Cost 10-Bit Sampling ADC
***AD9005**	12	0.1	38000	Int	12	M	C, M	3–459	Complete 12-Bit ADC with T/H, Reference and Timing Circuitry
CAV-1205	12	0.2	15000	Int	12	Card	C	3–567	12-Bit, 5MSPS Eurocard
MOD-1205	12	0.5	15000	Int	12	Card	C	3–593	12-Bit, 5MSPS Video ADC
AD9003	12	1	10000	Int	12	M	C	3–451	12-Bit, 1MSPS ADC, Single 40-Pin DIP
HAS-1201	12	1	2000	Int	12	M	C, M	3–573	12-Bit, 1MSPS ADC
HAS-1204	12	2	7000	Int	12	M	C, M	3–583	12-Bit 500kHz. ADC Single 40-Pin DIP
AD678	12	4	500	5 V, Int	8/12, µP	D, N, P	C, M	3–99	BiMOS, High Impedance High Bandwidth Sampling Input, 10 V Range
***AD1678**	12	4	500	Int	8/12, µP	D, N, P	C	3–195	BiMOS, 12-Bit Sampling ADC, ac Characterized
AD1332	12	8	125	−5 V, Int	12, µP	D	I	9–31	Complete 12-Bit 125kHz Sampling ADC for Digital Signal Processing
AD7870	12	8	500	3 V, Int	8/12/Serial, µP	N, P, Q	C, I, M	3–391	CMOS, 100kHz Throughput Rate
AD7878	12	8	500	3 V, Int	12, µP	E, N, P, Q	C, I, M	3–419	CMOS, 100kHz Throughput, On-Chip FIFO
***AD1334**	12	15	235	−5 V, Int	12, µP	D	I	9–49	Four Channel 65kHz 12-Bit Sampling ADC for Digital Signal Processing
AD368	12	15	40–1000	6.3 V, Int	12	D	I, M	9–19	Complete 12-Bit ADC with Programmable Gains of 1, 8, 64, 512
AD369	12	15	40–1000	6.3 V, Int	12	M	I	9–19	Complete 12-Bit ADC with Programmable Gains of 1, 10, 100, 500
AD363	12	40	X	10 V, Int	12, µP	D	C, M	9–5	16-Channel, 12-Bit DAS
AD364	12	50	X	10 V, Int	12, µP	D	C, M	9–5	High Speed, 16-Channel, 12-Bit DAS with Three-State Buffered Output

SAMPLING ADCs

Model	Res Bits	Conv Time µs max	SHA BW kHz typ[1]	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
HAS-1409	**14**	**9**	**200–800**	**Int**	**14**	**M**	**C**	**3–587**	**125kHz Word Rates; Includes T/H**
AD679	**14**	**10**	**500**	**5 V, Int**	**8, µP**	**D, N, P**	**C, M**	**3–111**	**BiMOS, High-Impedance High-Bandwidth Sampling Input, 10 V Input Range**
***AD1679**	**14**	**10**	**500**	**5 V, Int**	**8, µP**	**D, N, P**	**C**	**3–203**	**14-Bit BiMOS Sampling ADC, ac Characterized**
***AD779**	**14**	**10**	**500**	**5 V, Int**	**14, µP**	**D, N**	**C, M**	**3–135**	**BiMOS, High-Impedance High-Bandwidth Sampling Input, 10 V Input Range**
***AD1779**	**14**	**10**	**500**	**5 V, Int**	**14, µP**	**D, N**	**C, M**	**3–215**	**14-Bit BiMOS Sampling ADC, ac Characterized**
***AD7871**	**14**	**10**	**X**	**3 V, Int**	**8/14/Serial, µP**	**N, P, Q**	**C, I, M**	**3–407**	**CMOS, 14-Bit, 100kHz Sampling ADC**
***AD7872**	**14**	**12**	**X**	**3 V, Int**	**Serial, µP**	**N, Q**	**C, I, M**	**3–407**	**CMOS, 14-Bit, Sampling ADC with Serial Output**
DAS1152	**14**	**40**	**X**	**10 V, Int**	**14**	**D**	**I**	**9–73**	**14-Bit High Accuracy Sampling ADC**
DAS1157	**14**	**55**	**X**	**10 V, Int**	**14**	**D**	**I**	**9–77**	**Low Power, 14-Bit Sampling ADC**
DAS1153	**15**	**50**	**X**	**10 V, Int**	**15**	**D**	**I**	**9–73**	**15-Bit High Accuracy Sampling ADC**
DAS1158	**15**	**55**	**X**	**10 V, Int**	**15**	**D**	**I**	**9–77**	**Low Power, 15-Bit Sampling ADC**
AD1380	**16**	**20**	**900**	**Int**	**16/Serial**	**D**	**C**	**3–183**	**Low Cost, 16-Bit Sampling ADC. Operation Over −55°C to +85°C Temperature Range**
DAS1159	**16**	**55**	**X**	**10 V, Int**	**16**	**D**	**I**	**9–77**	**Low Power, 16-Bit Sampling ADC**

MULTIPLEXED ADCs

Model	Res Bits	# Chan	Conv Time µs	SHA BW kHz	Reference Volt Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
AD7824	**8**	**4**	**2.5**	**10**	**0–5 V, Ext**	**8, µP**	**N, Q**	**C, I, M**	**3–379**	**CMOS, On-Chip Track-Hold**
AD7828	**8**	**8**	**2.5**	**10**	**0–5 V, Ext**	**8, µP**	**E, N, P, Q**	**C, I, M**	**3–379**	**CMOS, On-Chip Track-Hold**
AD7581	8	8	66.7		−5 V−(−15 V), Ext	8, µP	D, N	C, I	3–295	CMOS
AD363	**12**	**16**	**40**		**10 V, Int**	**12, µP**	**D**	**C, M**	**9–5**	**High Speed, 16-Channel, 12-Bit DAS**
AD364	**12**	**16**	**50**		**10 V, Int**	**12, µP**	**D**	**C, M**	**9–5**	**16-Channel, 12-Bit DAS with Three-State Buffers**
AD7582	**12**	**4**	**100**		**4 V–6 V, Ext**	**12, µP**	**D, E, N, P**	**C, I, M**	**3–303**	**CMOS, 1LSB Total Unadjusted Error**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
[5]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

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VIDEO ADCs

Model	Res Bits	Throughput Rate MSPS min	Full Power BW MHz typ	Reference Voltage Int/Ext[2]	Bus Interface Bits[3]	Package Options[4]	Temp Range[5]	Page	Comments
AD9688	**4**	**175**	**100**	**0.16–6 V, Ext**	**4**	**E, Q**	**I, M**	**3–525**	**Second Source to AM688, Overrange Bits, Stackable to 8 Bits**
***AD9006**	**6**	**470**	**250 (min)**	**±1 V, Ext**	**6, µP**	**E, Z**	**C, M**	**3–467**	**470MSPS, 6-Bit ADC. 8.5pF Input Capacitance**
***AD9016**	**6**	**470**	**250 (min)**	**±1 V, Ext**	**6, µP**	**E, Z**	**C, M**	**3–467**	**470MSPS, 6-Bit ADC with On-Board Demultiplexing Circuitry**
AD9000	**6**	**50**	**20**	**0.5–2 V, Ext**	**6**	**D, E**	**C, M**	**3–435**	**MIL-STD-883, Rev. C, Devices Available. Low Error Rate**
***AD9028**	**8**	**300**	**250**	**–2 V, Ext**	**8**	**E**	**C, M**	**3–497**	**300 MSPS, 8-Bit ADC, Guaranteed Dynamic Performance**
***AD9038**	**8**	**300**	**250**	**–2 V, Ext**	**Dual 8**	**E**	**C, M**	**3–497**	**300 MSPS, 5-Bit ADC with On-Board 1:2 Demultiplexed Data Outputs**
AD770	**8**	**200**	**250**	**±2 V, Ext**	**8**	**D**	**C, M**	**3–123**	**High Bandwidth, Error Correction**
AD9002	**8**	**125**	**115 (Sm. Sig.)**	**0.1—(−2.1) Ext**	**8**	**D, E**	**I, M**	**3–443**	**Single Supply, Low Power, Low Input Capacitance, MIL-STD-883, Rev. C Device Available**
***AD9011**	**8**	**100**	**80**	**Int**	**8**	**M**	**C, M**	**3–483**	**8-Bit, 100MSPS ADC with On-Board Amp and Reference, Multiple Gain Selection**
AD9012	**8**	**75**	**180**	**−2 V, Ext**	**8**	**Q, E**	**I, M**	**3–489**	**TTL Compatible Outputs**
***AD9048**	**8**	**35**	**15**	**−2 V, Ext**	**8, µP**	**N, P, Q, Z**	**C, M**	**3–509**	**35MSPS, 8-Bit Video ADC, 16pF Input Capacitance**
AD9502	**8**	**13**	**7.5**	**Int**	**8**	**M**	**I**	**3–517**	**RS-170 Video Frame Grabber. Digitizes RS-170, NTSC, PAL Signals**
CAV-1040	10	40	20	Int	10	Card	C	3–563	Excellent Dynamic Performance over Frequency
CAV-1040A	**10**	**40**	**40**	**Int**	**10**	**Card**	**C**	**3–563**	**Higher Input Bandwidth Version of CAV-1040**
CAV-1220	**12**	**20**	**35**	**Int**	**12**	**Card**	**C**	**3–569**	**Fastest 12-Bit A/D Converter Available**

[1]X indicates that the internal SHA bandwidth is not specified in kHz.
[2]Ext indicates external reference with the range of voltages listed where applicable. Ext (M) indicates external reference with multiplying capability. Int indicates reference is internal. A voltage value is given if the reference is pinned out.
[3]This column lists the data format for the bus with "µP" indicating microprocessor capability—i.e., for a 12-bit converter 8/12, µP indicates that the data can be formatted for an 8-bit bus or can be in parallel (12 bits) and is microprocessor compatible.
[4]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; V–Pin-Stake; Z–Ceramic Leaded Chip Carrier.
[5]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

FACTORS IN CHOOSING AN A/D CONVERTER

In this catalog, there are listed approximately 50 different families of analog-to-digital converters (ADCs). If one were to consider all the variations, there would be considerably more than 100 different types to choose among. The reason for so many different types is the number of degrees of freedom in selection-technological, functional, performance and package. Complete information on converters may be found in the 700-page book, *Analog-Digital Conversion Handbook*, published by Prentice-Hall, Inc.

FUNCTIONAL CHARACTERISTICS

Block diagrams illustrating the various conversion techniques appear on individual data sheets.

The moderate-speed converters described in this catalog (<1MHz) employ two fundamental techniques – *successive approximations* for moderate-to-high resolution at moderate-to-high speed, and *integration* for high resolution at modest speeds. The AD574A and ADC1130/1131 are examples of the former, the AD1175 the latter.

Like a chemist's balance with binary weights (1/2, 1/4, 1/8, etc.), the *successive approximation* converter compares the unknown input with sums of accurately-known binary fractions of full scale starting with the largest (2^{-1}) and rejecting any that change the comparator's state ("tip the scale"). At the end of conversion (EOC), the output of the converter is a digital word representing the ratio of the input to full scale by a fractional-binary code.

Integrating types count pulses for a period proportional to the input. The charge balancing integrating converter (essentially a voltage-to-frequency converter) measures the input signal by balancing a proportional current against a train of precisely controlled reference pulses using an integrator (AD1170). During the integration phase, the input signal is measured; during the computation phase, the data from the first phase is processed and calibration factors applied. This type of converter can provide very high resolution and accuracy.

The video converters described here (AD9002, CAV-1205, etc.) employ two basic encoding techniques: simultaneous, or *flash* conversion, and serial-Gray-Code conversion. High resolution and high speed are obtained by *subranging* i.e., by performing an n-bit conversion in two steps; Analog Devices has perfected a form of subranging known as DCS – *digitally corrected subranging* – which permits accurate resolutions of 12 bits and more.*

In *flash* conversion, the analog signal is compared against $2^n - 1$ graded voltage levels using as many comparators, and the comparator output logic levels are processed by a priority encoder which converts the "thermometer" output to a binary (or Gray) code. Since the whole conversion occurs essentially simultaneously, it is the fastest means of conversion, but it requires many accurate comparators and large numbers of gates.

In *serial* analog-parallel-digital conversion, there are a number of cascaded stages, each having a gain of +2 for signals less than one-half the reference, and a gain of −2 for signals between one-half the reference and full scale. At each stage, a decision is made as to whether the signal is larger (1) or smaller (0) than one-half the reference; the stage's analog output becomes the input to the next stage. The complete time for one conversion is determined by the propagation delay of the analog signal through all stages; however, since the decision of each stage can be latched as soon as the stage has settled (and a new conversion can, in principle, be started as soon as the first bit has been latched), the rate at which conversions come out of the pipeline is considerably faster than the time for one sample to go through the conversion process. Though fast, this process is difficult to implement accurately for more than a few bits because of the compounding of gain (hence errors).

A *subranging* converter digitizes to a group of more-significant bits and stores them in a latch. A fast, very high-accuracy D/A converter converts them to an analog signal which is then subtracted from the input. The difference, or residue, is amplified and digitized, and (in DCS) the result is combined digitally in such a way as to correct for midscale conversion errors.

Whatever the technique, these A/D converters comprise several essential functions: an analog section, a digital data-generating section, data outputs and digital controls.

Analog Section

This section requires a reference, one or more high-gain comparators, and either a D/A converter (successive approximations) or a controllable integrator. The reference may be internal or external, fixed or variable, and of a specified polarity/sense in relation to the analog input. In ratiometric conversion, the reference is usually external and variable.

In successive approximation converters, the comparator is generally used in the *current-summing* mode; that is, the current output of the DAC is summed with the current developed in the DAC's "feedback resistor" by the input voltage (of opposite polarity), and the balancing action of the converter tends to bring the summing junction towards a voltage null (much like that of an op amp) at the end of conversion. The typical DAC feedback options, when applied in an ADC, provide input-scaling choices. When the bipolar-offset connection is jumpered to the summing point, input signals of both polarities can be handled. The current-switching action of the DAC, at the typically fast clock rates used in successive approximation converters, can disturb the output of the analog signal source, especially if it is a slow high-precision op amp. In such cases, buffering may be necessary.

Sample and Hold

When an ADC without a sample and hold is used, the analog input must not change by more than 1/2 LSB during the conversion. For some applications this constraint is not a concern, but it limits the bandwidth of the signal that can be applied to the converter. A sample-and-hold circuit must be used in front of the ADC if increased bandwidth is required. This sample and hold can be external, or an integral part of the converter (e.g., AD7579/AD7580).

***A considerable amount of useful information about the differences between video conversion and moderate-speed conversion can be found in the article "Very High Speed Data Acquisition," by Ed Graves in *Analog Dialogue* 13–2, available upon request.**

Digital Data-Generating Section
In successive-approximation types, this section consists of a discrete or integrated successive-approximations register (SAR), its controls and inputs from the comparator and clock (which is on-board, but in many cases permits external clock pulses, frequency adjustment and/or control). In integrating types, this section consists of the clock-pulse generator, the counter(s), the input from the comparator and the associated controls. Often, provisions are made for the pulse train to be jumpered to the counter externally so that the pulse train can be operated on externally, or can transmit its train of pulses to a remote counter. In a few types there are no on-board counters or registers; the pulse train, magnitude, overrange and control terminals are intended to communicate with external counters and registers.

Data Outputs
Factors to consider here include coding, resolution, overrange information, levels, format, validity and timing. *Coding* is usually binary including jumper-connected offset-binary and/or twos complement for bipolar input signals. For some types, BCD is available with sign-magnitude for bipolar inputs. Output coding specs should always be checked for digital polarity (positive- or negative-true) of both magnitude and sign information. The *resolution* (number of output bits) must be sufficient for the application; in addition, the specifications must be checked to ascertain that not only will all 2^n (binary) output codes be present (no missing codes), but they must all be present at any temperature in the operating range and related to the input with sufficient accuracy. Integrating types generally have no problems with missing codes (except sometimes at zero, with sign-magnitude coding); nevertheless, nonlinear integration can cause the conversion relationship to become nonlinear. Successive-approximation types have no way of determining *overrange*; they simply fill up. However, counter types roll over and put out a carry flag to signal overrange. Analog Devices offers ADCs, with 4- through 22-bit resolution, with a span of conversion times from milliseconds to nanoseconds.

The *data levels* available at the converter output must be checked (TTL, low-voltage CMOS, high-voltage CMOS, ECL), as must the load-driving capability and fanout, and the supply conditions under which appropriate output levels will be furnished. The available choice of output *formats* must also be as desired – parallel, serial, byte-serial, and/or pulse-train. If the converter is intended to communicate directly with an 8-bit data bus, the output should have three-state capability, and parallel outputs must be enabled in bytes of eight or fewer lines (AD573, AD574A). If the output is serial, it is usually NRZ (non-return-to-zero) and should be accompanied by a set of synchronized clock-pulses.

A *status* (or *busy* or EOC) output changes state to indicate when the data becomes *valid*. The exact nature of this transition should be specified – polarity, timing, levels, etc. For serial data, the exact relationship between the data and the synchronizing clock should be specified to indicate when each bit becomes valid, and for how long. In general, the *timing* of the whole conversion process must be clearly understood, especially if high speeds are necessary, either for conversion or for communication with a processor (or both). The timing diagrams on specification sheets are usually accompanied by adequate descriptions of the conversion process and specifications of the critical interface parameters.

Controls
The functions, action (levels or edges), polarity and timing of all control inputs and outputs should be clearly understood, as well as their loading characteristics and dependence on the supply. In addition to the essential *start-conversion-command* input and a *status* output, various control commands may be available, such as *clock inhibit, high- (low-) byte enable, status enable* and – for speeding up conversion at the cost of resolution in successive-approximation converters – *short-cycle*.

Many ADCs are designed to interface directly to the bus of a computer or microprocessor. These ADCs provide the necessary control and handshake lines, as well as data bit registers, to minimize and often eliminate the required interface circuitry. The bus timing should be studied with respect to the timing provided by the ADC interface, especially as the processor executes a data read cycle to the ADC to retrieve the conversion results. Systems with higher speed clocks require either shorter minimum write pulse widths (such as 50ns for the AD7579/AD7580) or the use of processor-wait states when the ADC is addressed.

STATIC AND DYNAMIC PERFORMANCE SPECIFICATIONS

All ADCs are specified using terms such as accuracy, linearity, offset, defined and explained below. These static, or "dc," parameters are necessary and sufficient for many applications; they may not be sufficient for others, such as those in digital signal processing, adaptive filtering or waveform generation. Dynamic ac specifications define how the ADC performs using parameters such as signal-to-noise ratio (SNR), intermodulation distortion (IMD) and total harmonic distortion (THD). These specifications characterize the performance of the ADC output in applications where the envelope of output changes and output timing errors are critical.

POWER SUPPLIES

Appropriate power supplies should be made available considering the logic levels and analog input signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specifications should be provided. Any recommended external protection circuitry should be planned for. In many cases, separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals while ensuring that a connection between grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

APPLICATION CHECKLIST

The designer will generally require specific information in the following categories before proceeding to the selection process:

- Accurate description of input and output
  1. Analog signal range and source or load impedance
  2. Digital code needed – binary, offset binary, twos complement, BCD, etc.
  3. Logic level system, i.e., TTL/DTL compatible

- What is the needed data throughput rate?
- What are the control interface details?
- What does the system error budget allow for the converter?
- What are environmental conditions – temperature range, time, supply voltage – over which the converter should operate to the desired accuracy?

For A/D converters, the following considerations are typical.

- What is the analog input voltage range, and to what resolution must the signal be measured?
- What is the requirement for linearity error (or relative accuracy error)?
- To what extent must the various sources of error be minimized as environmental temperature changes?
- How much time can be allowed in the system for each complete conversion? What aperture uncertainty and acquisition time are needed for the sample-hold?
- How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
- Can the system tolerate missed codes under any conditions?
- What is the character of the input signal? Is it noisy, sampled, filtered, rapidly varying, slowly varying? What kind of pre processing is to be (or can be) done that will affect the choice (and cost) of the converter? Is aliasing a potential problem?

SPECIFICATIONS AND TERMS

Definitions of performance specifications and related information are to be found on the following pages in alphabetical order.*

Accuracy, Absolute

The error of an A/D converter at a given output code is the difference between the theoretical and the actual analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see Quantizing Uncertainty), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code. For example, if 5 volts ($\pm$ 1.2mV) will theoretically produce a 12-bit half-scale code of 100000000000, then a converter for which any voltage from 4.997V to 4.999V will produce that code will have absolute error of 1/2 (4.997 + 4.999) $-$5 volts = $-$2mV.

Absolute error comprises gain error, zero error and nonlinearity, together with noise. Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

***For video converters, there are a number of additional application-oriented specifications pertaining to the device's use in a system (e.g., *noise power ratio, differential phase, differential gain, signal-to-noise ratio*). Some useful references for understanding such specifications can be found in the following publications available from Analog Devices, Computer Labs Division, 7910 Triad Center Drive, Greensboro, NC 27409.**

Kester, W.A., "PCM Signal Codecs for Video Applications," *SMPTE Journal*, Volume 88, November 1979, pp 770-778.

Pratt, W.J., "Test A/D Converters Digitally," *Electronic Design*, December 6, 1975.

Smith, B.F. and Pratt, W.J., "Understanding High-Speed A/D Converter Specifications," Computer Labs, 1974.

Accuracy, Relative

Relative accuracy error, expressed in %, ppm or fractions of an LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range) after the full-scale range (FSR) has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

The "discrete points" of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see Accuracy, Absolute).

Aperture Time

This is the interval between the application of the *hold* command to a sample/track-hold and the actual opening of the switch. The aperture time consists of a delay (which depends on the logic and the switching device – 5ns for HTS-0025) and an uncertainty (due to jitter – 20ps max rms for HTS-0025). When a sample-hold is used in an application where timing is critical, the timing of the hold command can be advanced to compensate for the known component of aperture delay. The jitter, however, imposes the ultimate limitation on timing accuracy. When a sample-hold is used with an ADC, the timing uncertainty of the conversion process is reduced by the ratio of aperture jitter to the conversion time, i.e., the maximum frequency which can be handled with less than 1LSB error due to timing is $2^{-n}/(\pi\ \tau_{au})$ instead of $2^{-n}/(\pi\ \tau_c)$, where τ_{au} is the aperture uncertainty and τ_c is the conversion time.

Common-Mode Rejection (CMR)

The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 1,000,000 to 1 means that a 1V common-mode voltage passes through the amplifier as though it were a differential signal of one microvolt at the input.

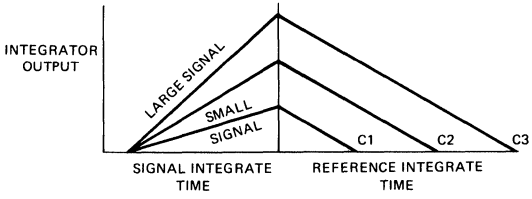
Conformance, Straight-Line

This indicates how closely the ADC transfer characteristic conforms to a reference straight line. This straight-line conformance is critical in DSP applications where deviations from a straight line are seen as distortion, while gain and offset errors are not as serious. The straight-line conformance error is measured from the center of each code to the best-fit straight line.

Conversion Time and Conversion Rate

The time required for a complete measurement by an ADC is called *conversion time*. For most converters (assuming no significant additional systemic delays), this is identical to the inverse of *conversion rate*. However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined; thus, for example, the CAV-1250 can provide 12-bit output data at a 3.85MHz word rate (260ns/conversion), even though the time for any one conversion, from start to finish, is two 280ns encode periods plus 195ns, or 755ns at 3.85MHz.

Dual-Slope Converter
An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator and integrates "down" from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time-interval meter (i.e., counter) is generally used as the output indicator.



Feedthrough
Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplexer. It is variously specified in %, ppm, fractions of 1LSB, or fractions of 1 volt, with a given set of inputs at a specified frequency.

"Flash" Converter
A converter in which all the bit choices are made at the same time. It requires $2^n - 1$ voltage-divider taps and comparators, and a comparable amount of priority encoding logic. An extremely fast scheme, it requires large numbers of precision components. Flash converters are often used for partial conversions in *subranging converters*.

Full-Scale Error
The ideal difference between the first transition voltage and last transition voltage for an ADC is (F.S. -2LSB). Full-Scale Error is defined as the deviation between this ideal difference and the measured difference.

Gain Adjustment
The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g., 10V full scale in a fixed-reference converter, or 100% of full scale in a ratiometric converter. Gain- and zero-adjustment principles are discussed under *zero*.

Harmonic Distortion (and Total Harmonic Distortion)
The ADC is driven by a spectrally pure, analog sine wave from a signal generator. The ADC outputs are analyzed via FFT and the ratio of the rms sum of the harmonics of the ADC output to the fundamental value is the THD. Usually, only the lower order harmonics are included, such as second through fifth:

$$\text{THD} = 20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4 and V_5 are the rms amplitudes of the individual harmonics.

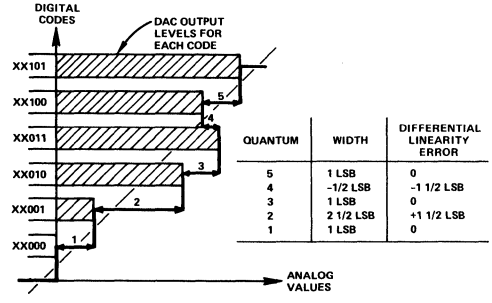
Intermodulation Distortion
The ADC is driven by an analog signal source producing two combined sine waves of frequencies f_a and f_b. As with any imperfectly linear device, distortion products (of order $m+n$) are produced at sum and difference frequencies of $mf_a \pm nf_b$ where m, n = 0, 1, 2, 3 . . . by the ADC. Intermodulation terms are those for which m or n is not equal to zero. The second order terms include $(f_a + f_b)$, and $f_a - f_b)$, and the third order terms are $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$. The ADC outputs are analyzed by FFT. IMD is defined as:

$$\text{IMD} = 20 \log \frac{\text{(rms sum of the sum and difference distortion products)}}{\text{rms amplitude of the fundamental}}$$

Least Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost "1" is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest change that can be resolved by an n-bit converter.

Linearity Error
Linearity error of a converter, expressed in percent or parts-per-million of full-scale range, or fractions of a least-significant bit, is the deviation of the analog values from a straight line, in a plot of the measured conversion relationship. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated. Sometimes referred to as "end-point" nonlinearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Accuracy, Relative). Linearity has two components – *differential* and *integral* nonlinearity.

Linearity, Differential and Integral
A digital output code should correspond to a quantum of analog input values exactly 1LSB in width (2^{-n} of full scale, for an n-bit converter). Any deviation of the measured "step" from the ideal width is called Differential Nonlinearity. It is an important specification, because a differential nonlinearity error greater than 1LSB can lead to nonmonotonic behavior of a D/A converter and missed codes in an A/D converter employing such a DAC. A flagrant example of differential nonlinearity is shown here.



QUANTUM	WIDTH	DIFFERENTIAL LINEARITY ERROR
5	1 LSB	0
4	-1/2 LSB	-1 1/2 LSB
3	1 LSB	0
2	2 1/2 LSB	+1 1/2 LSB
1	1 LSB	0

In the illustration, the horizontal bars represent the measured DAC output values corresponding to six adjacent digital codes. The DAC is nonlinear in that the next least-significant bit (XX010) is 1 1/2LSB too large. Thus, instead of the five quanta, or steps, being all equal (=1LSB), quantum 2 is 2 1/2LSB and quantum 4 is −1/2LSB. The differential linearity error, the difference between the actual quantum width and the ideal 1LSB, is 1 1/2LSB for quantum 2 and −1 1/2LSB for quantum 4.

When this DAC is used in successive-approximations conversion, it will lead to a missed code. Analog inputs slightly larger than the value of XX100 will be converted to XX100, and analog inputs slightly less than the value of XX100 will be converted to XX010. The code XX011 will not exist; it will be a *missed code.*

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of "no missed codes" which implies a differential nonlinearity less than 1LSB.

While differential nonlinearity deals with errors in step size, *integral nonlinearity* has to do with deviations of the overall shape of the conversion response. Even converters that are not subject to differential linearity errors (e.g., integrating types) have integral linearity (sometimes just "linearity") errors.

Power-Supply Sensitivity
The sensitivity of a converter to dc changes in power-supply voltages is normally expressed in terms of percentage change in analog input value (or fractions of the analog equivalent of 1LSB), corresponding to a given code for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$. Power-supply sensitivity may also be expressed in relation to a specified dc shift of the supply voltage. High-accuracy ADCs intended for battery operation require excellent rejection of large supply variations.

Quad-Slope Converter
This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ± 1/2LSB, in addition to the actual conversion errors. In integrating converters, this "error" is often expressed as "± 1 count."

Ratiometric Converter
The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage (e.g., the voltage applied to a bridge), it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation. Ratiometric conversion can also serve as a substitute for analog signal division (where the denominator changes but little during the conversion).

Signal-to-Noise Ratio
Signal-to-Noise Ratio (SNR) is measured signal to noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine-wave input is given by:

$$SNR = (6.02N + 1.76)\ dB,$$

where N is the number of bits in the ADC. Thus for an ideal 10-bit ADC, SNR = 62dB.

Slew Rate
Slew rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error.

Stability
Stability of a converter usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see "Temperature Coefficients").

Subranging Converters
In this type of converter, an extremely fast conversion produces the most significant portion of the output word. This portion is converted back to analog with a fast high-accuracy D/A converter and subtracted from the input. The resulting residue is converted to digital at high speed and combined with the results of the earlier conversion to form the output word. In *digitally corrected subranging* (DCS), the two bytes are combined in a manner that corrects for the error of the LSB of the most significant byte. For example, using 8-bit and 5-bit conversion, and this proprietary technique, a full-accuracy high-speed 12-bit converter can be built.

Successive Approximations
Successive approximations is a high-speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, 1/16 gram, etc. The weights are tried in order, starting with the largest. Any weight that tips the scale is removed. At the end of the process, the sum of the weights remaining on the scale will be within 1LSB of the actual weight (± 1/2LSB, if the scale is properly biased – see *zero*).

Temperature Coefficients
In general, temperature instabilities are expressed in %/°C, ppm/°C, as fractions of 1LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter divided by the corresponding temperature change. Parameters of interest include, *gain, linearity, offset* (bipolar) and *zero*. The last three are expressed in % or ppm of full-scale range per Celsius degree.

Gain Tempco: Two factors principally affect converter gain instability with temperature:

1. In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of an AD581L is typically 5ppm/°C.
2. The ratiometric circuitry has a sensitivity to temperature.

Linearity Tempco: Sensitivity of linearity to temperature over the specified range. To avoid missed codes, it is sufficient that the differential nonlinearity error be less than 1LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a specified temperature range, and/or implied by a statement that there are no missed codes when operating within a specified temperature range.

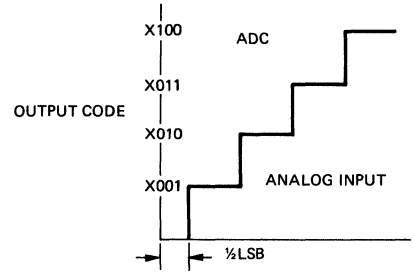
Offset Tempco: The temperature coefficient of the all-DAC-switches-off (minus full-scale) point, of a bipolar successive-approximations converter, is dependent on three variables:

1. The tempco of the reference source
2. The voltage stability of the input buffer and the comparator
3. The tracking capability of the bipolar-offset resistors and the gain resistors.

Unipolar Zero: The zero tempco of an ADC is dependent only on the zero stability of the integrator and/or the input buffer and the comparator. It may be expressed in μV/°C, or in percent or ppm of full-scale per degree C.

Zero- and Gain-Adjustment Principles

The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at $1/2 \times 2^{-n}$ of nominal full scale. The gain is set for the final transition to all-bits-on to occur at F.S. $(1 - 3/2 \times 2^{-n})$. The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at $-$F.S. $(1-2^{-n})$ and the last transition at $+$F.S. $(1-3\times2^{-n})$. The data sheet instructions should be followed.



Zero Code Error

This is a measure of the difference between the ideal (0.5LSB) and the actual differential analog input level required to produce the first positive LSB code to transition (00 . . . 00 to 00 . . . 01).

ANALOG DEVICES

8- and 10-Bit Analog-to-Digital Converters

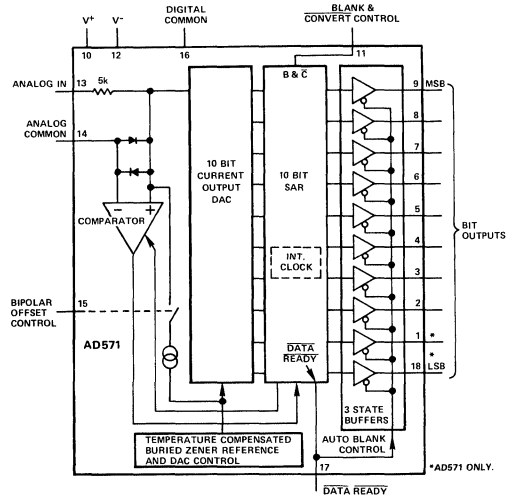
AD570/AD571*

FEATURES

Complete A/D Converters with Reference and Clock
- **AD570: 8 Bit**
- **AD571: 10 Bit**

Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
Digital Multiplexing – 3 State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction

AD570/AD571 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTIONS

The AD570/AD571 are successive approximation A/D converters consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform full accuracy conversions in 25μs.

The AD570/AD571 incorporate advanced integrated circuit design and processing technologies. They employ I^2L (integrated logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin-film resistor ladder network insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and −15V, the AD570/AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three-state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ high blanks the outputs and readies the device for the next conversion.

The devices are available in two versions: the "J" and "K" specified for the 0 to +70°C temperature range. The "S" guarantees the specified accuracy and no missing codes from −55°C to +125°C.

*Covered by Patent Nos. 3,940,760; 4,213,806; 4,136,349.

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. The AD570 is an 8-bit version which employs the same architecture. No external components are required to perform a conversion.
2. The AD570/AD571 are single chip devices employing advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The converters accept either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
4. Each device offers the specified accuracy with no missing codes over its entire operating temperature range.
5. Operation is guaranteed with −15V and +5V to +15V supplies. The devices will also operate with a −12V supply.

SPECIFICATIONS ($T_A = +25°C$, $V+ = +5V$, $V- = -12V$ or $-15V$, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD570J Min	AD570J Typ	AD570J Max	AD570S Min	AD570S Typ	AD570S Max	Units
RESOLUTION[1]			8			8	Bits
RELATIVE ACCURACY							
T_{min} to T_{max}			±1/2			±1/2	LSB
FULL-SCALE CALIBRATION		±2			±2		LSB
UNIPOLAR OFFSET			±1/2			±1/2	LSB
BIPOLAR ZERO			±1/2			±1/2	LSB
DIFFERENTIAL NONLINEARITY							
T_{min} to T_{max}	**8**			**8**			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			±1			±1	LSB
Bipolar Offset			±1			±1	LSB
Full-Scale Calibration			±2			±2	LSB
POWER SUPPLY REJECTION							
CMOS Positive Supply							
$+13.5V \le V+ \le +16.5V$	–	–	–	–	–	–	LSB
TTL Positive Supply							
$+4.5V \le V+ \le +5.5V$			±2			±2	LSB
Negative Supply							
$-16.0V \le V- \le -13.5V$			±2			±2	LSB
ANALOG INPUT IMPEDANCE	**3.0**	5.0	**7.0**	**3.0**	5.0	**7.0**	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
($V_{OUT} = 0.4V$ max, T_{min} to T_{max})	**3.2**			**3.2**			mA
Output Source Current							
($V_{OUT} = 2.4V$ max, T_{min} to T_{max})	**0.5**			**0.5**			mA
Output Leakage			±40			±40	μA
LOGIC INPUTS							
Input Current			±100			±100	μA
Logic "1"	**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**	V
CONVERSION TIME							
T_{min} to T_{max}	**15**	25	**40**	**15**	25	**40**	μs
POWER SUPPLY							
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V−	**−12.0**	−15	**−16.5**	**−12.0**	−15	**−16.5**	V
OPERATING CURRENT							
V+		7	**10**		7	**10**	mA
V−		9	**15**		9	**15**	mA
PACKAGE OPTION[2]							
Ceramic (D-18)		AD570JD			AD579SD		

NOTES

[1]The AD570 is a selected version of the AD571 10-bit A-to-D converter. Only TTL logic inputs should be connected to Pins 1 and 18 (or no connection made) or damage may result.

[2]See Section 13 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

SPECIFICATIONS (T_A = +25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

AD570/AD571

Model	AD571J Min	AD571J Typ	AD571J Max	AD571K Min	AD571K Typ	AD571K Max	AD571S Min	AD571S Typ	AD571S Max	Units
RESOLUTION			10			10			10	Bits
RELATIVE ACCURACY, T_A			±1			±1/2			±1	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
FULL-SCALE CALIBRATION		±2			±2			±2		LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR ZERO			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY, T_A	**10**			**10**			**10**			Bits
T_{min} to T_{max}	**9**			**10**			**10**			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full-Scale Calibration			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
CMOS Positive Supply										
+13.5V≤V+≤+16.5V	–	–	–			±1	–	–	–	LSB
TTL Positive Supply										
+4.5V≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−16.0V≤V−≤−13.5V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	**3.0**	5.0	**7.0**	**3.0**	5.0	**7.0**	**3.0**	5.0	**7.0**	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	**3.2**			**3.2**			**3.2**			mA
Output Source Current[1]										
(V_{OUT} = 2.4V max, T_{min} to T_{max})	**0.5**			**0.5**			**0.5**			mA
Output Leakage			±40			±40			±40	μA
LOGIC INPUTS										
Input Current			±100			±100			±100	μA
Logic "1"	**2.0**			**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**			**0.8**	V
CONVERSION TIME										
T_{min} to T_{max}	**15**	25	**40**	**15**	25	**40**	**15**	25	**40**	μs
POWER SUPPLY										
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+16.5**	**+4.5**	+5.0	**+7.0**	V
V−	**−12.0**	−15	**−16.5**	**−12.0**	−15	**−16.5**	**−12.0**	−15	**−16.5**	V
OPERATING CURRENT										
V+		7	**10**		7	**10**		7	**10**	mA
V−		9	**15**		9	**15**		9	**15**	mA
PACKAGE OPTION[2]										
Ceramic (D-18)		AD571JD			AD571KD			AD571SD		

NOTES

[1]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[2]See Section 14 for package outline information.

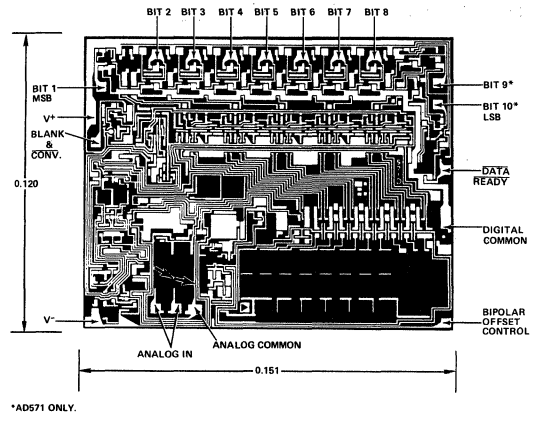
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common AD570J, S/AD571J, S	0 to +7V
AD571K	0 to +16.5V
V− to Digital Common	0 to −16.0V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (Blank Mode)	0 to V+
Power Dissipation	800mW

CHIP BONDING DIAGRAM



CIRCUIT DESCRIPTION

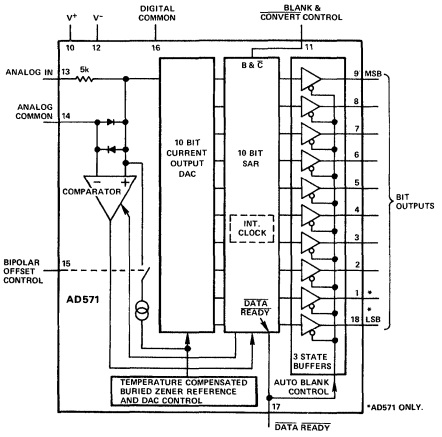
The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive approximation analog-to-digital conversion function. The AD570 is an 8-bit version. A functional block diagram of the AD570/AD571 is shown below. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 10-bit (AD571) current output DAC is sequenced by the I^2L successive approximation register (SAR) from its most-significant bit (MSB) to least-significiant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±1/2LSB (0.05%).

Upon completion of the sequences, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further on.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows a positive bipolar offset current to be injected into the summing (+) node of the comparator to offset the DAC output. The nominal 0 to +10V unipolar input range now becomes a −5V to +5V range. The 5kΩ thin-film input resistor is trimmed so that with a full-scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

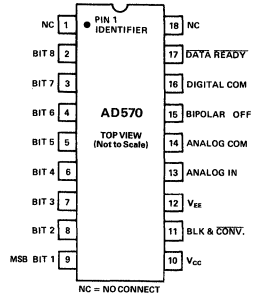
The AD570/AD571 are designed for optimum performance using a +5V and −15V supply, for which the J and S grades are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic.



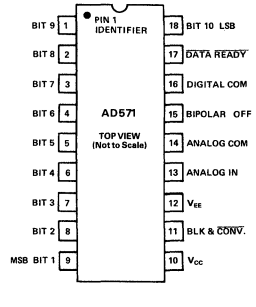
AD570/AD571 Functional Block Diagram

CONNECTING THE AD570/AD571 FOR STANDARD OPERATION

The AD570/AD571 contain all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and −15), the analog input, and the conversion start pulse. The functional pin outs are shown below.



AD570 Pin Connections



AD571 Pin Connections

FULL-SCALE CALIBRATION

The 5kΩ thin-film input resistor is laser trimmed to produce a current which matches the full-scale current of the internal DAC when a full-scale analog input voltage of 10 volts – 1LSB is applied at the input. The input resistor is trimmed in this way so that if a fine-trimming potentiometer is inserted in series with the input signal, the input current at the full-scale input voltage can be trimmed down to match the DAC full-scale current as precisely as desired. However, for many applications the nominal 9.990 (9.961 for the AD570) volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to Pin 13. Typical full-scale calibration error will then be about ±2LSB. If the more precise calibration is desired, a trimmer should be used instead. A 50Ω potentiometer should be used with the AD571 and a 200Ω with the AD570. Set the analog input at full scale and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of $10V/2^N$ (where N = number of bits).

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a −5V to +5V range with an offset binary code. The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 1.

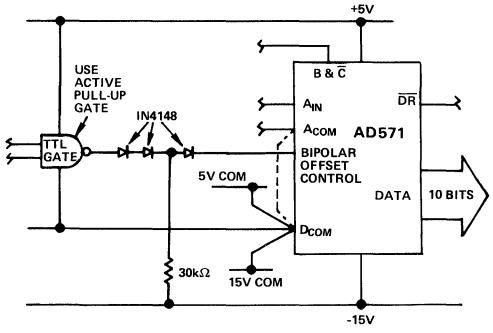


Figure 1. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0 – 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

COMMON-MODE RANGE

The AD570/AD571 provide separate analog and digital common connections. The circuit will operate properly with as much as ±200mV of common-mode range between the two commons. This permits more flexible control of system common bussing and digital and analog return.

In normal operation the analog common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into analog common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The analog common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

ZERO OFFSET

The apparent zero point of the AD570/AD571 can be adjusted by inserting an offset voltage between the analog common of the device and the actual signal return or signal common. Figure 2 illustrates two methods of providing this offset for the AD571. Figure 2a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

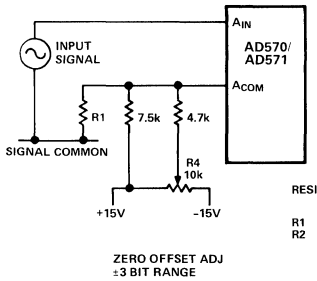


Figure 2a.

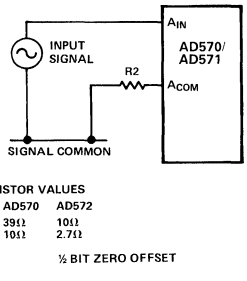


Figure 2b.

Figure 3 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 2b. At balance (after a conversion) approximately 2mA flows into the analog common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired 1/2 bit offset of the transfer characteristics. The nominal 2mA analog common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full-scale transition point will also move. Thus, if an offset of 1/2LSB is introduced, full-scale trimming as previously described should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the analog common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

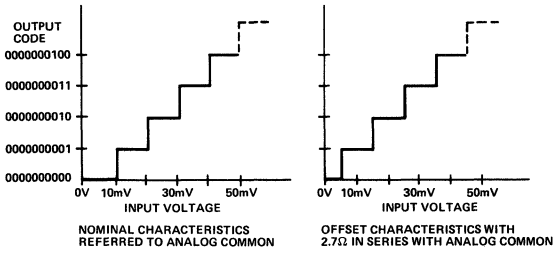


Figure 3. AD571 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights~9.755mV)

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code the bipolar offset control pin is left open.

A −5.0 volt signal will give a 10-bit code of 00000000 00; an input of 0.00 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve for the AD571 is shown in Figure 4. The MSB transition for both the AD570 and the AD571 occurs at a −4.88mV input.

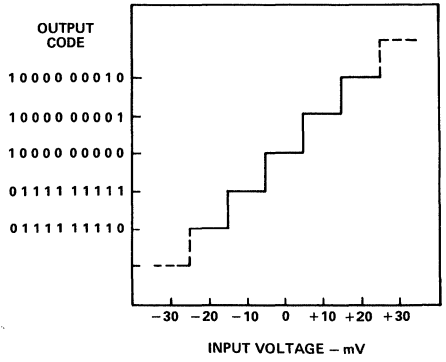


Figure 4. AD571 Transfer Curve – Bipolar Operation

CONTROL AND TIMING OF THE AD570/AD571

There are several important timing and control features on the AD570/AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 5.

The normal standby situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ will go high and the data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and data lines will not change. If a 2μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

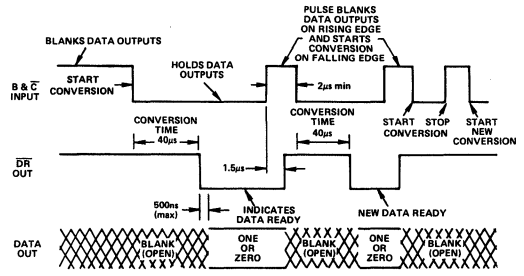


Figure 5. AD570/AD571 Timing and Control Sequences

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD570/AD571 discussed above allows the devices to be easily operated in a variety of systems with differing control modes. The two most common control modes, the convert pulse mode and the multiplex mode, are illustrated here.

Convert Pulse Mode – In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 6 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse.

Multiplex Mode – In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 7.

This operating mode allows multiple converters to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several converters are multiplexed in sequence, a new conversion may be started in one AD570/AD571 while data is being read from another. As long as the data is read and the first AD570/AD571 is cleared within 15μs after the start of conversion of the second AD570/AD571, no data overlap will occur.

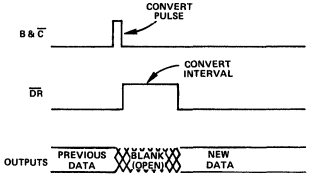


Figure 6. Convert Pulse Mode

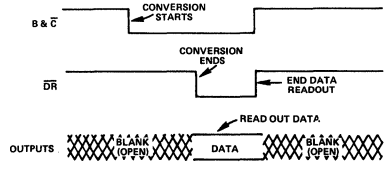


Figure 7. Multiplex Mode

ANALOG DEVICES

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD572

FEATURES

Performance

- True 12-Bit Operation: Max Nonlinearity < ±0.012%
- Low Gain T.C.: < ±15ppm/°C (AD572B)
- Low Power: 900mW
- Fast Conversion Time: < 25μs
- Monotonic Feedback DAC Guarantees No Missing Codes
- MIL-STD-883B Processing Available

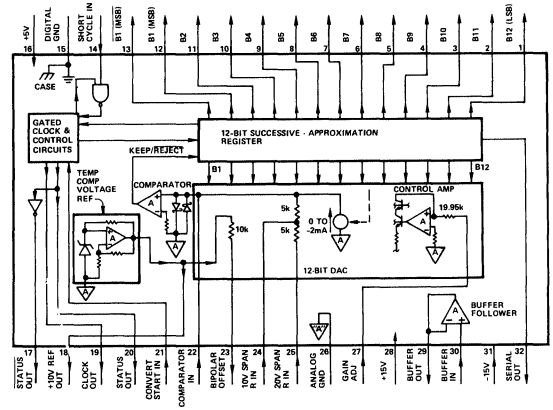
Versatility

- Aerospace Temperature Range: -55°C to +125°C (AD572S)
- Positive-True Serial or Parallel Logic Outputs
- Short-Cycle Capability

Value

- Precision +10V Reference for External Application
- Internal Buffer Amplifier
- High Reliability Package

AD572 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

GENERAL DESCRIPTION

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide superior performance, flexibility and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 900mW, and conversion time of less than 25μs. Of considerable significance in aerospace applications is the guaranteed performance from -55°C to +125°C of the AD572S. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5.0, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +10V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is positive-true and available in either serial or parallel form.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from -25°C to +85°C, and the "S" from -55°C to +125°C.

PRODUCT DESCRIPTION

The AD572 functional diagram and pin-out are shown in Figure 1. The device consists of the following monolithic bipolar circuit elements:

1. 12-bit successive-approximation register
2. 12-bit DAC
3. low-drift comparator
4. temperature-compensated precision +10V reference
5. high-impedance buffer follower
6. gated clock and digital control circuits

AD572 ORDERING GUIDE

Model	Specification Temp Range	Max Gain T.C.	Max Reference T.C.	Guaranteed Temp Range No Missing Codes	Package Option*
AD572AD	-25°C to +85°C	±30ppm/°C	±20ppm/°C	0 to +70°C	DH-32C
AD572BD	-25°C to +85°C	±15ppm/°C	±10ppm/°C	-25°C to +85°C	DH-32C
AD572SD	-55°C to +125°C	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)	±20ppm/°C	-55°C to +125°C	DH-32C
AD572SD/883B	Meets all specifications after processing to the requirements of MIL-STD-883, Method 5008, Class B.				

NOTES: D suffix = Ceramic DIP package designator.
(Analog Devices reserves the right to substitute metal packages in lieu of the standard ceramic package on commercial grades.)

*See Section 14 for package outline information.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0V	*	*
Unipolar	0 to +5, 0 to +10V	*	*
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5kΩ	*	*
0 to +10V, ±5V	5.0kΩ	*	*
±10V	10kΩ	*	*
Buffer Amplifier			
Impedance (min)	100MΩ	*	*
Bias Current	50nA	*	*
Settling Time			
to 0.01% of FSR for 20V step	2μs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	0.012% FSR	*	*
Inherent Quantization Error	±½ LSB	*	*
Differential Linearity Error	±½ LSB	*	*
No Missing Codes	Guaranteed: 0 to +70°C	Guaranteed: -25°C to +85°C	Guaranteed: -55°C to +125°C
Power Supply Sensitivity			
±15V	±0.002% FSR/%ΔV_S	*	*
±5V	±0.001% FSR/%ΔV_S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)
Unipolar Offset	±3ppm FSR/°C	±5ppm FSR/°C (max)	**
Bipolar Offset (max)	±15ppm FSR/°C	±7ppm FSR/°C	**
Linearity	±3ppm FSR/°C	±2ppm FSR/°C	**
CONVERSION TIME (max)	25μs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
$\overline{\text{Status}}$	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500kHz	*	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV typ	*	*
Max External Current	±1mA	*	*
Voltage Temperature Coefficient (max)	±20ppm/°C	±10ppm/°C	*
POWER REQUIREMENTS			
Supply Voltages/Currents	+15V, ±5% @ +25mA (40 max)	*	*
	-15V, ±5% @ -20mA (35 max)	*	*
	+5V, ±5% @ +80mA (150 max)	*	*
Total Power Dissipation	925mW	*	*
TEMPERATURE RANGE			
Specification	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-55°C to +150°C	*	*

NOTES
*Same specification as AD572AD.
**Same specification as AD572BD.

Specifications subject to change without notice.

Note 1 Positive pulse 200ns wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.

Note 2 With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 4 and 5.

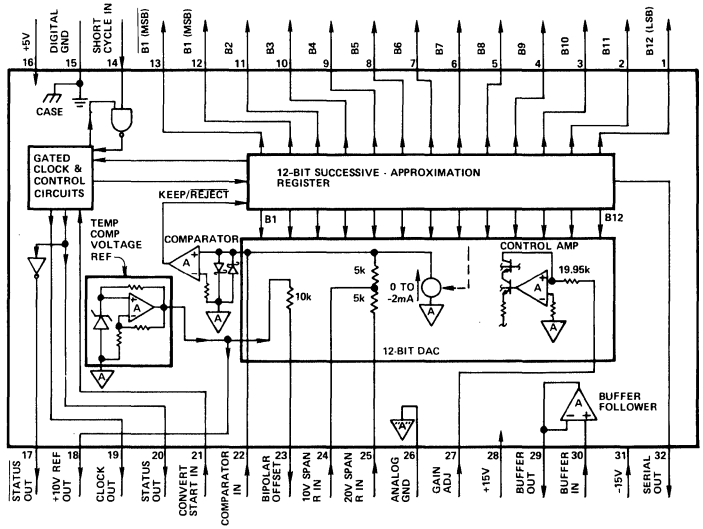


Figure 1. AD572 Functional Diagram & Pinout

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, ±10mV by active laser trimming of the thin-film resistors which determine the closed-loop gain of this op amp.

The DAC chip uses 12 precision, high speed bipolar current steering switches, a control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current. The DAC is laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.0005% of FSR (full-scale range) to guarantee no missing codes over the appropriate temperature ranges specified for the AD572A, AD572B, and AD572S versions.

Different unipolar and bipolar analog input ranges can be selected by changing connections at the device terminal pins. The analog voltage input can be applied to either of the span (direct input) resistors. Alternatively, the unity buffer follower can be connected between the analog signal and either direct input terminal when a high impedance input is required.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD572 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through

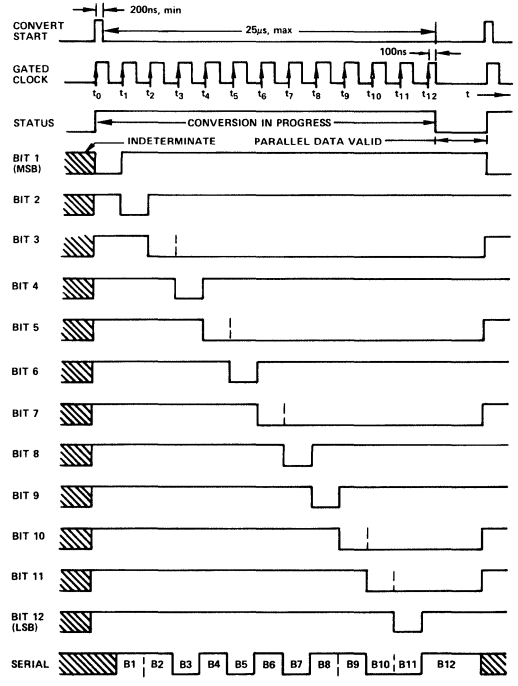


Figure 2. Timing Diagram (Binary Code 110101011001)

13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 100ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 8).

Incorporation of this 100ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

BINARY CODING

The AD572 binary output number $N_o = B_1\ B_2\ B_3 \ldots B_{12}$ is related to the analog input voltage E_{in} for all unipolar ranges by the expression:

$$\frac{B_1\ 2^{11} + B_2\ 2^{10} + B_3\ 2^9 + \ldots + B_{12}\ 2^0}{2^{12}} = \frac{E_{in}}{FSR} \qquad (1)$$

. . .where B_1 = MSB, B_{12} = LSB, and FSR = full-scale range. For all bipolar ranges a fixed bipolar offset equal to $\frac{+FSR}{2}$ is internally summed with E_{in} so that the sum of E_{in} plus this offset will be positive over the rated operating range. For bipolar ranges, expression (1) becomes:

$$\frac{B_1\ 2^{11} + B_2\ 2^{10} + B_3 2^9 + \ldots + B_{12}\ 2^0}{2^{12}} = \frac{E_{in} + \frac{FSR}{2}}{FSR} \qquad (2)$$

Expressions (1) and (2) can be put in an alternate form:

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR = E_{in} \qquad (3)$$

Unipolar (Binary Coding)

...and...

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR - \frac{FSR}{2} = E_{in} \qquad (4)$$

Bipolar (Offset Binary Coding)

Several examples will illustrate how this binary coding works.

0 TO +10V INPUT RANGE

Assume FSR = 10V and $B_1\ B_2\ B_3\ .\ .B_{12}$ = 110001000001, then from (3), E_{in} = +5V +2.5V +0.1563V + 0.0024V = +7.6587V.

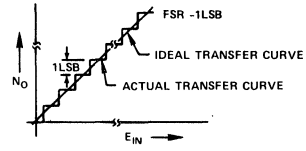
-5V TO +5V INPUT RANGE

Assume FSR = 10V as above, but that the bipolar offset is connected and $B_1\ B_2\ B_3\ .\ .B_{12}$ = 0110000000001. Then from (4), E_{in} = (+2.5V + 1.25V + 0.0024V) - 5V = -1.2476V.

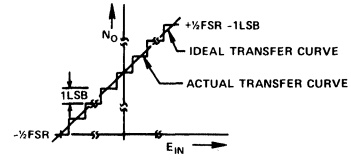
-10V TO +10V INPUT RANGE

Assume the bipolar offset is connected as above, but that the input span is now 20V. Assuming the same digital output code as in the -5V to +5V input range example, from (4), E_{in} = (+5V +2.5V +0.0049V) -10V = -2.4951V, or twice the value of the previous example (neglecting round-off errors).

The encoding process defined by the previous relations (1) and (2) or (3) and (4) determines that the analog input lies within one of the 2^{12} = 4096 quantization levels between 0 and FSR (or -FSR/2 and +FSR/2). Figures 3 (A) and 3 (B) show the actual device transfer curves for unipolar and bipolar ranges (offset binary coding). They also show the ideal straight-line transfer curves which pass through the center of each quantization level. As can be seen from these figures, the actual and ideal transfer curves differ by exactly ±½LSB at the end of each quantization interval, giving rise to the fundamental ±½LSB quantization error inherent in the digitizing process.



(A) Unipolar Range (Binary Coding)



(B) Bipolar Range (Offset Binary Coding)

Figure 3. Unipolar and Bipolar Range Transfer Curves

ANALOG INPUT AND POWER CONNECTIONS

Offset Adjust: Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 4 and 5, respectively. The Bipolar Offset pin 23 is open-circuited for all unipolar input ranges, and connected to Comparator Input pin 22 for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9MΩ resistor to Comparator Input pin 22 for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of 8 x 244 x 10^{-6} x 1200ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

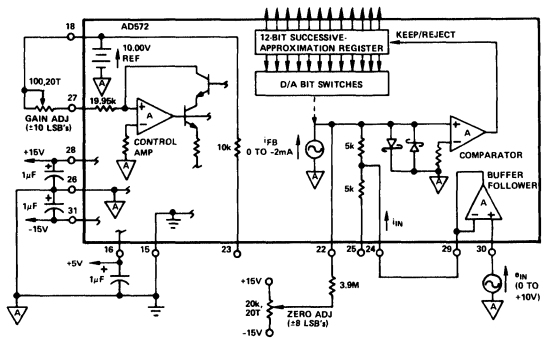


Figure 4. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

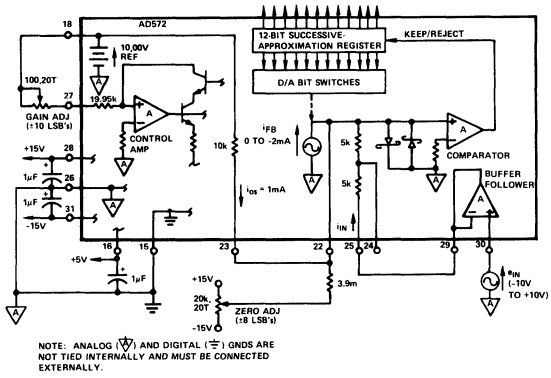


Figure 5. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 6.

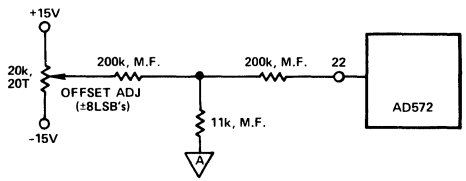


Figure 6. Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin 22 connection runs short, since the Comparator Input pin 22 is quite sensitive to external noise pick-up.

Gain Adjust: The gain adjust circuit consists of a 100Ω potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input pin 27 for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types; 20T cermet (tempco = 100ppm/°C max) types are recommended. If the 100Ω GAIN ADJ potentiometer is replaced by a fixed 50Ω resistor, absolute gain calibration to ±0.1% of FSR is guaranteed.

Grounding: Analog and digital power supply grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground pin 26 and Digital Ground pin 15 are not connected internally; these two pins must be connected externally for the device to operate properly. Preferably, this connection is made at only one point, and as close to the device as possible.

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the device. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling (as is required with some competitive products), since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 3 and 4, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -½FSR for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table I. Coding relationships and calibration points for 0 to +5V and -2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -5V to +5V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB)	B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1	
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0	
:	:	:	:	:	:	
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1	
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0	
:	:	:	:	:	:	
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1	
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0	

Table I. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

RANGE AND BUFFER FOLLOWER PIN CONNECTIONS

Analog pin connections for each of the ranges, with and without the buffer follower being used, are shown in Table II.

Range	Buffer Follower	Connect Analog Input To Pin:	Connect Span Pin:	Connect Bipolar Pin 23 To:
0 to +5V	Used	30, and 29 to 24	25 to 22	—
	Not Used	24		
0 to +10V	Used	30, and 29 to 24	—	
	Not Used	24		
-2.5 to +2.5V	Used	30, and 29 to 24	25 to 22	22
	Not Used	24		
-5 to +5V	Used	30, and 29 to 24	—	
	Not Used	24		
-10 to +10V	Used	30, and 29 to 25	—	
	Not Used	25		

Table II. Range and Buffer Follower Pin Connections

When the analog signal source has a low impedance (as would be the case if it were the output of the sample-hold amplifier of Figure 9), it can be connected to either of the direct input pins 24 or 25. The buffer follower is used in the application as shown in Figure 6, in which the analog input to the converter comes directly from the output of a FET analog multiplexer. The selected channel has a typical r_{on} = 200Ω which has a 3000ppm/°C tempco. If the multiplexer output were connected to the 0 to +10V direct input pin 24 (5kΩ input impedance, nominal), this r_{on} would introduce a 4% gain scale-factor loading error, which is well beyond the normal ±0.25% FSR external gain adjustment range, and a tempco of approximately 3000ppm/°C x 4% = 120ppm/°C. By connecting the buffer between the multiplexer output and direct input, these errors are eliminated. The buffer amplifier input bias current (50nA typical) must flow through the analog signal source, however. This limits the upper practical source impedance to several kilohms so that the offset voltage I_{BIAS} R_{SOURCE} can be kept negligible, even though the buffer amplifier dynamic input impedance ⩾ 100MΩ. The buffer amplifier has a 2μs settling time to 0.01% FSR for a 20V input step. This must be added to the conversion time when the input voltage can change significantly between successive conversions (as could be the case in the circuit of Figure 7).

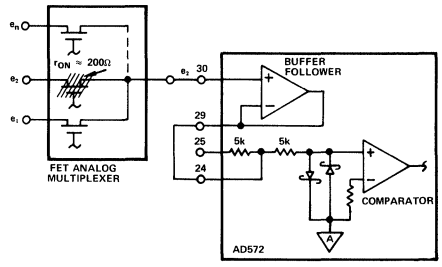


Figure 7. Using Buffer Follower With Multiplexed Analog Input

Short Cycle Input: A Short Cycle Input pin 14 permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +100ns in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table III.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset at: (Figure 2)
16	12	0.024	25	t_{12} + 100ns
2	10	0.10	21	t_{10} + 100ns
4	8	0.39	17	t_8 + 100ns

Table III. Short Cycle Connections

(One should note that the calibration voltages listed in Table I are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolutions.)

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary

or two's complement binary, depending on whether Bit 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 8. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 2. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

APPLICATIONS

Sample-Hold Amplifier: A sample-hold amplifier (SHA) is normally connected between the analog signal source and AD572 analog input when the analog signal can change by more than ½LSB during conversion. Typical SHA-AD572 interconnections are shown in Figure 9. The $\overline{\text{STATUS}}$ output drives the SHA SAMPLE/HOLD input directly. On receipt of a CONVERT START pulse, the $\overline{\text{STATUS}}$ flag changes from "1" to "0" causing SHA mode to change from SAMPLE to HOLD. The SHA output voltage $e_{o\ S\text{-}H}$ is then held constant at the value existing just prior to application of the HOLD command for the complete conversion period. At the end of conversion, the $\overline{\text{STATUS}}$ flag returns to "1", restoring the SHA mode to SAMPLE, and $e_{o\ S\text{-}H}$ again tracks the analog signal voltage $e_{in\ S\text{-}H}$ (after the signal acquisition transient has subsided).

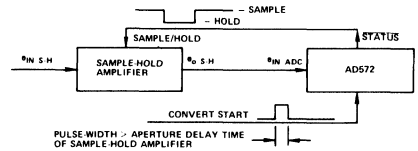


Figure 9. Sample-Hold Amplifier – AD572 Interconnections

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 9, for example, the CONVERT START signal pulse-width can be extended beyond the aperture delay time of the SHA to assure that $e_{o\ S\text{-}H}$ is in steady-state before conversion is initiated. This assures accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse-width on the conversion timing cycle is shown in Figure 10.

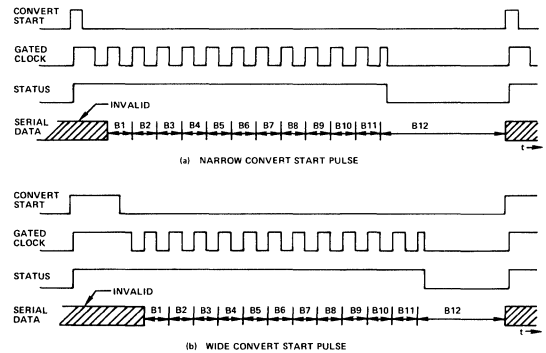


Figure 10. Effect of Convert Start Pulse-Width on Timing

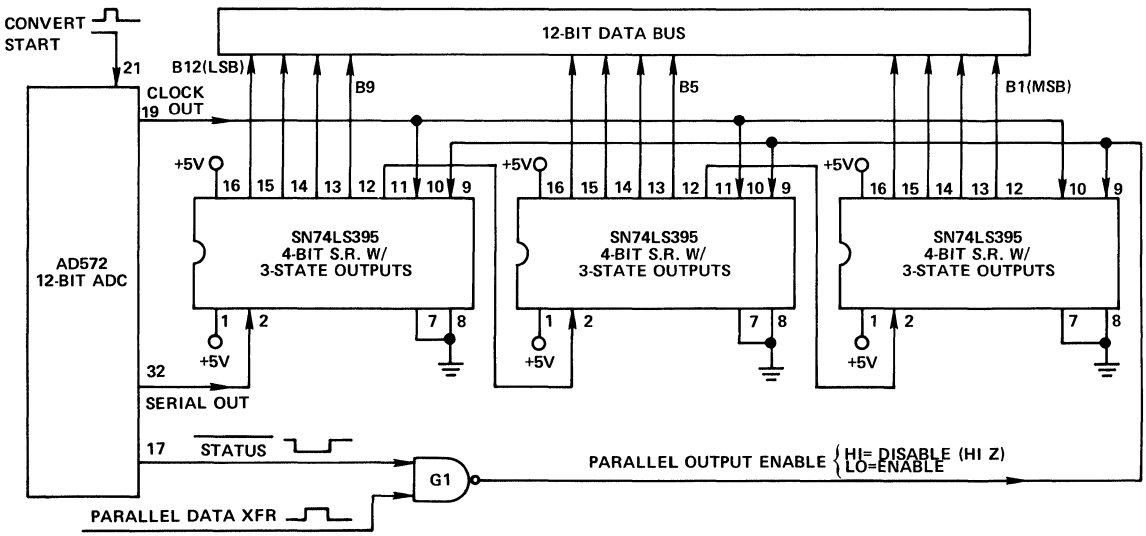


Figure 8. Serial Data Transfer Into Shift Register With Parallel Output to Data Bus

Digital Gain Control: Figure 11 shows a method of varying the AD572 gain digitally, using an 8-bit DAC. The 100Ω GAIN ADJ potentiometer is replaced by a 15Ω fixed resistor. This biases full-scale high by approximately 35Ω/20,000Ω = +0.18% of FSR. The AD559 has a large positive compliance voltage which permits its Current Output pin 4 to be connected directly to the AD572 Reference Input pin 27. The AD559 2.5mA output current is established by the AD580 +2.5V voltage reference connected through a 1kΩ resistor to Reference Current Input pin 14. The 2.5mA DAC full-scale output current removed from the AD572 pin 27 node changes the pin 27 input current -2.5mA x 15Ω/20kΩ = -1.88μA, or -1.88μA/500μA = -0.38% of FSR; this permits a digital gain adjustment range of approximately ±0.2% FSR from nominal.

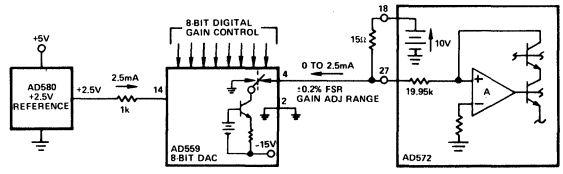


Figure 11. Digital Gain Control Using 8-Bit DAC

ANALOG DEVICES

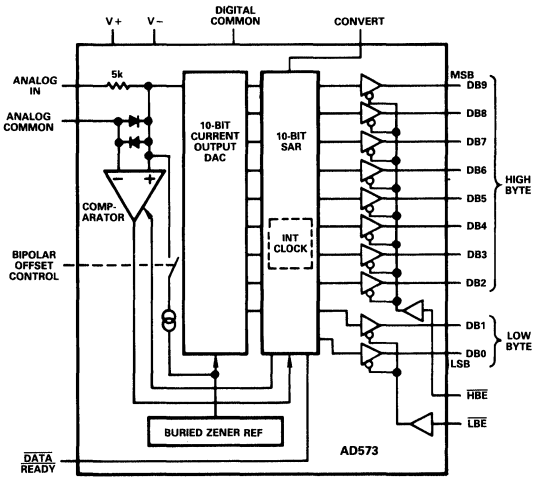
10-Bit A/D Converter

AD573*

FEATURES

Complete 10-Bit A/D Converter with Reference, Clock and Comparator
Full 8- or 16-Bit Microprocessor Bus Interface
Fast Successive Approximation Conversion – 20μs typ
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Low Cost Monolithic Construction

AD573 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD573 is a complete 10-bit successive approximation analog to digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 20μs.

The AD573 incorporates advanced integrated circuit design and processing technologies. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD573 will accept analog inputs of 0 to +10V or −5V to +5V. The trailing edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion. $\overline{\text{HIGH BYTE ENABLE}}$ ($\overline{\text{HBE}}$) and $\overline{\text{LOW BYTE ENABLE}}$ ($\overline{\text{LBE}}$) control the 8-bit and 2-bit three state output buffers.

The AD573 is available in two versions for the 0 to +70°C temperature range, the AD573J and AD573K. The AD573S guarantees ±1LSB relative accuracy and no missing codes from −55°C to +125°C.

Two package configurations are offered. All versions are also offered in a 20-pin hermetically sealed ceramic DIP. The AD573J and AD573K are also available in a 20-pin plastic DIP.

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690**

PRODUCT HIGHLIGHTS

1. The AD573 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The AD573 interfaces to many popular microprocessors without external buffers or peripheral interface adapters. The 10 bits of output data can be read as a 10-bit word or as 8- and 2-bit words.
3. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD573 adapts to either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.

SPECIFICATIONS (T_A=25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD573J Min	AD573J Typ	AD573J Max	AD573K Min	AD573K Typ	AD573K Max	AD573S Min	AD573S Typ	AD573S Max	Units
RESOLUTION		10			10			10		Bits
RELATIVE ACCURACY[1]			±1			±1/2			±1	LSB
$T_A = T_{min}$ to T_{max}			±1			±1/2			±1	LSB
FULL SCALE CALIBRATION[2]		±2			±2				±2	LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR OFFSET			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY[3]	**10**			**10**			**10**			Bits
$T_A = T_{min}$ to T_{max}	**9**			**10**			**10**			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS[4]										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full Scale Calibration[2]			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
Positive Supply										
$+4.5 \le V+ \le +5.5V$			±2			±1			±2	LSB
Negative Supply										
$-15.75V \le V- \le -14.25V$			±2			±1			±2	LSB
$-12.6V \le V- \le -11.4V$			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	**3.2**			**3.2**			**3.2**			mA
Output Source Current[5]										
(V_{OUT} = 2.4V min, T_{min} to T_{max})	**0.5**			**0.5**			**0.5**			mA
Output Leakage			±40			±40			±40	μA
LOGIC INPUTS										
Input Current			±100			±100			±100	μA
Logic "1"	**2.0**			**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**			**0.8**	V
CONVERSION TIME										
$T_A = T_{min}$ to T_{max}	**10**	20	**30**	**10**	20	**30**	**10**	20	**30**	μs
POWER SUPPLY										
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V−	**−11.4**	−15	**−16.5**	**+11.4**	−15	**−16.5**	**−11.4**	−15	**−16.5**	V
OPERATING CURRENT										
V+		15	**20**		15	**20**		15	**20**	mA
V−		9	**15**		9	**15**		9	**15**	mA

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full-scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]Change from +25°C value from +25°C to T_{min} or T_{max}.

[5]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

AD573 ORDERING GUIDE

Model	Package Options*	Temperature Range	Relative Accuracy
AD573JN	20-Pin Plastic DIP (N-20)	0 to +70°C	±1LSB max
AD573KN	20-Pin Plastic DIP (N-20)	0 to +70°C	± 1/2LSB max
AD573JP	20-Pin Leaded Chip Carrier (P-20A)	0 to +70°C	±1LSB max
AD573KP	20-Pin Leaded Chip Carrier (P-20A)	0 to +70°C	±1/2LSB max
AD573JD	20-Pin Ceramic DIP (D-20)	0 to +70°C	±1LSB max
AD573KD	20-Pin Ceramic DIP (D-20)	0 to +70°C	± 1/2LSB max
AD573SD	20-Pin Ceramic DIP (D-20)	−55°C to +125°C	±1LSB max

*See Section 14 for package outline information.

FUNCTIONAL DESCRIPTION

A block diagram of the AD573 is shown in Figure 1. The positive CONVERT pulse must be at least 500ns wide. $\overline{DR}$ goes high within 1.5μs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 10-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is more, the bit is turned off. After testing all bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ½LSB (0.05% of full scale).

The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{HBE}$ and $\overline{LBE}$ can then be activated to enable the upper 8-bit and lower 2-bit buffers as desired. $\overline{HBE}$ and $\overline{LBE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state.

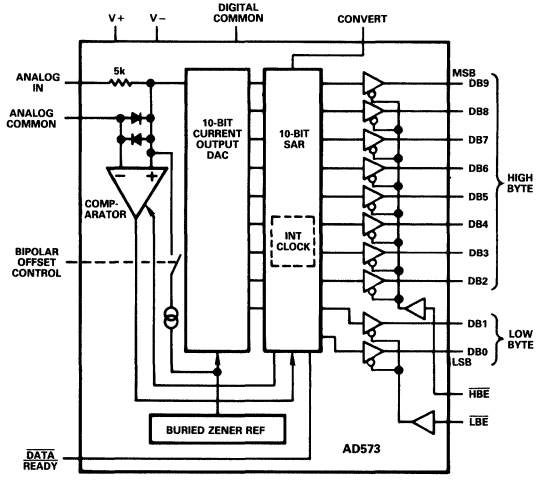


Figure 1. AD573 Functional Block Diagram

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

UNIPOLAR CONNECTION

The AD573 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −12V to −15V), the analog input and the convert pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 2.

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 16) to digital common (pin 17).

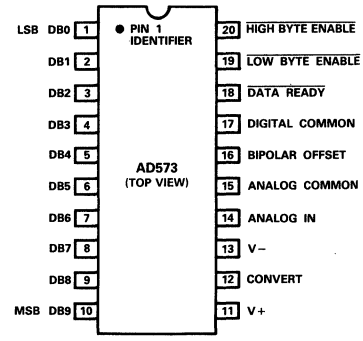


Figure 2. AD573 Pin Connections

Full Scale Calibration

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when an analog input voltage of 9.990 volts (10 volts – 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be within ±2LSB or ±0.2%. If more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 11111111 10 and 11111111 11. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a weight of exactly 10.00mV), a 100Ω resistor and a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ. Figure 3 illustrates the connections required for full scale calibration.

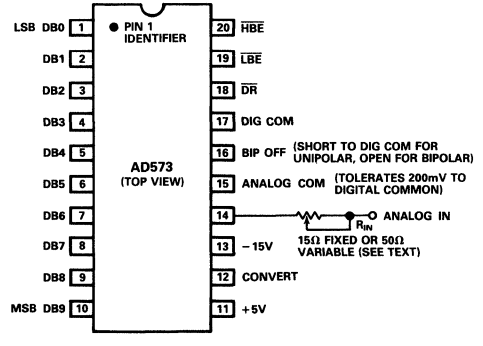


Figure 3. Standard AD573 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ±1LSB for all versions of the AD573, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

Figure 4a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

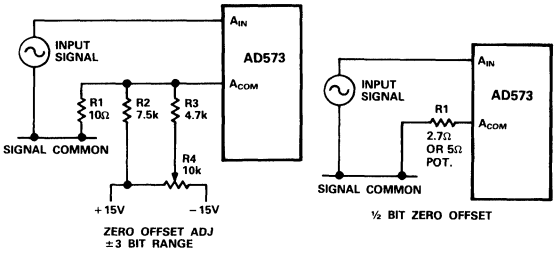


Figure 4a. *Figure 4b.*

Figure 4. Offset Trims

Figure 5 shows the nominal transfer curve near zero for an AD573 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

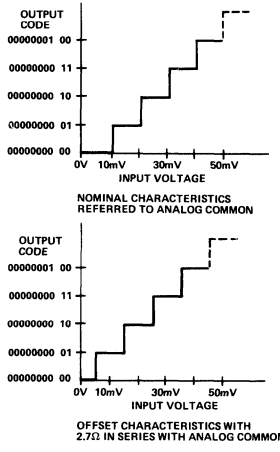


Figure 5. AD573 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766mV)

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on the previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle appropriately during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code, the bipolar offset control pin is left open.

A −5.000 volt signal will give a 10-bit code of 00000000 00; an input of 0.000 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve is shown in Figure 6.

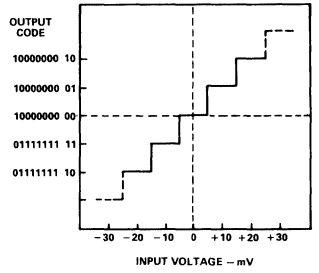


Figure 6. AD573 Transfer Curve – Bipolar Operation

Note that in the bipolar mode, the code transitions are offset ½LSB such that an input voltage of 0 volts ±5mV yields the code representing zero (10000000 00). Each output code is then *centered* on its nominal input voltage.

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is +4.985 volts.

Negative Full Scale Calibration

The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally −5V) which results in the 00000000 00 code. R2 should be omitted to obtain a symmetrical range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 7.

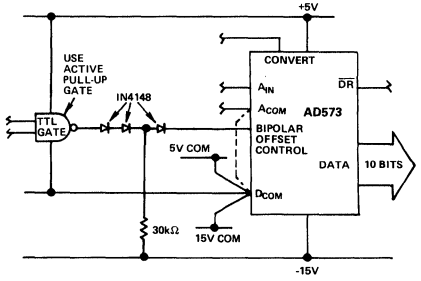


Figure 7. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0 – 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD573

Many situations in high-speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a

signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD573, a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD573 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms.

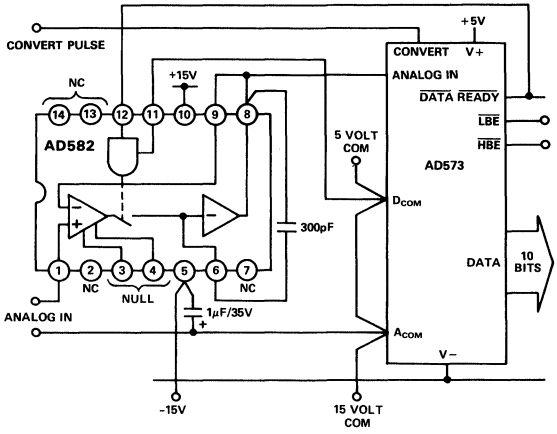


Figure 8. Sample-Hold Interface to the AD573

$\overline{DR}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD573 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD573).

$\overline{DR}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

GROUNDING CONSIDERATIONS

The AD573 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD573

The operation of the AD573 is controlled by three inputs: CONVERT, $\overline{HBE}$ and $\overline{LBE}$.

Starting a Conversion

The conversion cycle is initiated by a positive-going CONVERT pulse at least 500ns wide. The rising edge of this pulse resets the internal logic, clears the result of the previous conversion, and sets $\overline{DR}$ high. The falling edge of CONVERT begins the conversion cycle. When conversion is completed $\overline{DR}$ returns low. During the conversion cycle, $\overline{HBE}$ and $\overline{LBE}$ should be held high. If $\overline{HBE}$ or $\overline{LBE}$ goes low during a conversion, the data output buffers will be enabled and intermediate conversion results will be present on the data output pins. This may cause bus conflicts if other devices in a system are trying to use the bus.

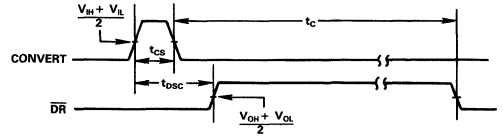


Figure 9. Convert Timing

Reading the Data

The three-state data output buffers are enabled by $\overline{HBE}$ and $\overline{LBE}$. Access time of these buffers is typically 150ns (250 maximum). The Data outputs remain valid until 50ns after the enable signal returns high, and are completely into the high-impedance state 100ns later.

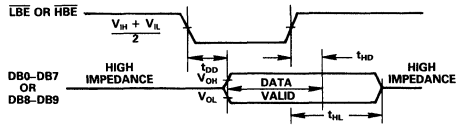


Figure 10. Read Timing

TIMING SPECIFICATIONS (All grades, $T_A = T_{min} - T_{max}$)

Parameter	Symbol	Min	Typ	Max	Units
CONVERT Pulse Width	t_{CS}	500	–	–	ns
$\overline{DR}$ Delay from CONVERT	t_{DSC}	–	1	1.5	μs
Conversion Time	t_C	10	20	30	μs
Data Access Time	t_{DD}	0	150	250	ns
Data Valid after $\overline{HBE}$/$\overline{LBE}$ High	t_{HD}	50	–	–	ns
Output Float Delay	t_{HL}	–	100	200	ns

MICROPROCESSOR INTERFACE CONSIDERATIONS – GENERAL

When an analog-to-digital converter like the AD573 is interfaced to a microprocessor, several details of the interface must be considered. First, a signal to start the converter must be generated; then an appropriate delay period must be allowed to pass before valid conversion data may be read. In most applications, the AD573 can interface to a microprocessor system with little or no external logic.

The most popular control signal configuration consists of decoding the address assigned to the AD573, then gating this signal with the system's WR signal to generate the CONVERT pulse, and gating it with RD to enable the output buffers. The use of a memory address and memory WR and RD signals denotes "memory-mapped" I/O interfacing, while the use of a separate I/O address space denotes "isolated I/O" interfacing. In 8-bit bus systems, the 10-bit AD573 will occupy two locations when data is to be read; therefore, two (usually consecutive) addresses must be decoded. One of the addresses can also be used as the address which produces the CONVERT signal during WR operations.

Figure 11 shows a generalized diagram of the control logic for

an AD573 interfaced to an 8-bit data bus, where two addresses (ADC ADDR and ADC ADDR + 1) have been decoded. ADC ADDR starts the converter when written to (the actual data being written to the converter does not matter) and contains the high byte data during read operations. ADC ADDR + 1 performs no function during write operations, but contains the low byte data during read operations.

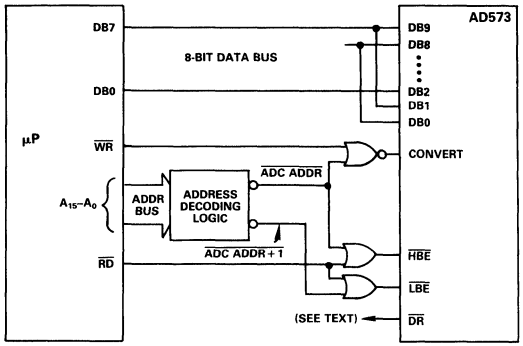


Figure 11. General AD573 Interface to 8-Bit Microprocessor

In systems where this read-write interface is used, at least 30 microseconds (the maximum conversion time) must be allowed to pass between starting a conversion and reading the results. This delay or "timeout" period can be implemented in a short software routine such as a countdown loop, enough dummy instructions to consume 30 microseconds, or enough actual useful instructions to consume the required time. In tightly-timed systems, the $\overline{DR}$ line may be read through an external three-state buffer to determine precisely when a conversion is complete. Higher-speed systems may choose to use $\overline{DR}$ to signal an interrupt to the processor at the end of a conversion.

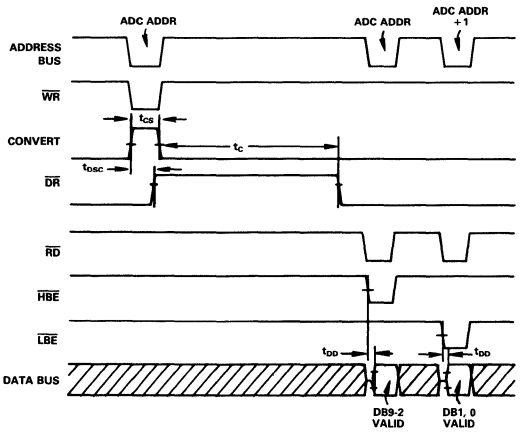


Figure 12. Typical AD573 Interface Timing Diagram

CONVERT Pulse Generation

The AD573 is tested with a CONVERT pulse width of 500ns and will typically operate with a pulse as short as 300ns. However, some microprocessors produce active WR pulses which are shorter than this. Either of the circuits shown in Figure 13 can be used to generate an adequate CONVERT pulse for the AD573.

In both circuits, the short low-going WR pulse sets the CONVERT line high through a flip-flop. The rising edge of $\overline{DR}$ (which signifies that the internal logic has been reset) resets the flip-flop and brings CONVERT low, which starts the conversion.

Note that t_{DSC} is slightly longer when the result of the previous conversion contains a logic 1 on the LSB. This means that the actual CONVERT pulse generated by the circuits in Figure 13 will vary slightly in width.

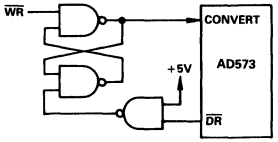


Figure 13a. Using 74LS00

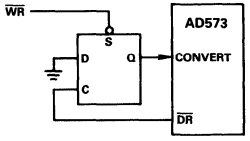


Figure 13b. Using 1/2 74LS74

Output Data Format

The AD573 output data is presented in a left-justified format. The 8 MSBs (DB9–DB2, pins 10 through 3) are enabled by $\overline{HBE}$ (pin 20) and the 2 LSBs (DB1, DB0 – pins 2 and 1) are enabled by $\overline{LBE}$ (pin 19). This allows simple interface to 8-bit system buses by overlapping the 2 MSBs and the 2 LSBs. The organization of the data is shown in Figure 14.

When the least significant bits are read ($\overline{LBE}$ brought low), the six remaining bits of the byte will contain meaningless data. These unwanted bits can be masked by logically ANDing the byte with 11000000 (C0 hex), which forces the 6 lower bits to logic 0 while preserving the two most significant bits of the byte.

Note that it is not possible to reconfigure the AD573 for right justified data.

$\overline{HBE}$	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
$\overline{LBE}$	DB1	DB0	X	X	X	X	X	X

Figure 14. AD573 Output Data Format

In systems where all 10 bits are desired at the same time, $\overline{HBE}$ and $\overline{LBE}$ may be tied together. This is useful in interfacing to 16-bit bus systems. The resulting 10-bit word can then be placed at the high end of the 16-bit bus for left justification or at the low end for right justification.

It is also possible to use the AD573 in a "stand-alone" mode, where the output data buffers are automatically enabled at the end of a conversion cycle. In this mode, the $\overline{DR}$ output is wired to the $\overline{HBE}$ and $\overline{LBE}$ inputs. The outputs thus are forced into the high-impedance state during the conversion period, and valid data becomes available approximately 500ns after the $\overline{DR}$ signal goes low at the end of the conversion. The 500ns delay allows propagation of the least significant bit through the internal logic.

This mode is particularly useful for bench-testing of the AD573, and in applications where dedicated I/O ports of peripheral interface adapter chips are available.

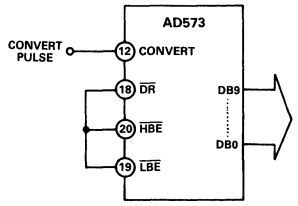


Figure 15. AD573 in "Stand-Alone" Mode (Output Data Valid 500ns After DR Goes Low)

Apple II Microcomputer Interface

The AD573 can provide a flexible, low-cost analog interface for the popular Apple II microcomputer. The Apple II, based on a 1MHz 6502 microprocessor, meets all timing requirements for the AD573. Only a few TTL gates are required to decode the signals available on the Apple II's peripheral connector. The recommended connections are shown in Figure 16.

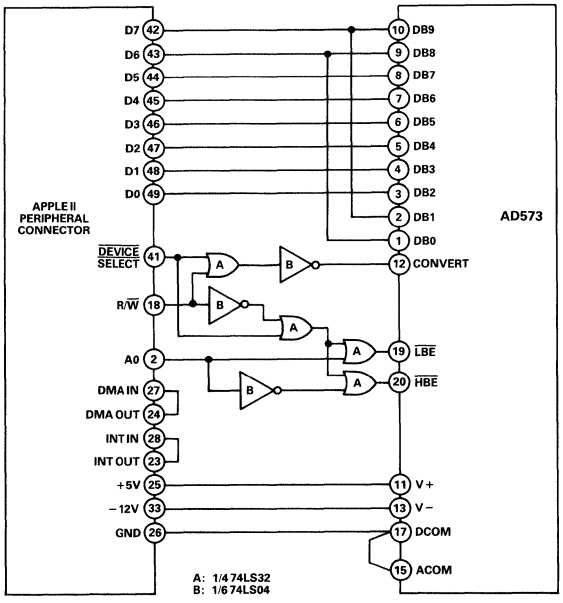


Figure 16. AD573 Interface to Apple II

The BASIC routine listed here will operate the AD573 circuit shown in Figure 16. The conversion is started by POKEing to the location which contains the AD573. The relatively slow execution speed of BASIC eliminates the need for a delay routine between starting and reading the converter. This routine assumes that the AD573 is connected for a ±5 volt input range. Variable I represents the integer value (from 0 to 1023) read from the AD573. Variable V represents the actual value of the input signal (in volts).

```
100 PRINT "WHICH SLOT IS THE A/D IN";:INPUT S
110 A= 49280+16*S
120 POKE A,0
130 L=PEEK(A) :H=PEEK(A+1)
140 I=(4*H)+INT(L/64)
150 V=(I/1024)*10-5
160 PRINT "THE INPUT SIGNAL IS ";V;"VOLTS."
```

It is also possible to write a faster-executing assembly-language routine to control the AD573. Such a routine will require a delay between starting and reading the converter. This can be easily implemented by calling the Apple's WAIT subroutine (which resides at location $FCA8) after loading the accumulator with a number greater than or equal to two.

8085-Series Microprocessor Interface

The AD573 can also be used with 8085-series microprocessors. These processors use separate control signals for RD and WR, as opposed to the single R/$\overline{W}$ control signal used in the 6800/6500 series processors.

There are two constraints related to operation of the AD573 with 8085-series processors. The first problem is the width of the CONVERT pulse. The circuit shown in Figure 17 (essentially the same as that shown in Figure 13) will produce a wide enough CONVERT pulse when the 8085 is running at 5MHz. For 8085 systems running at slower clock rates (3MHz), the flip-flop-based circuit can be eliminated since the $\overline{WR}$ pulse will be approximately 500ns wide.

The other consideration is the access time of the AD573's three-state output data buffers, which is 250ns maximum. It may be necessary to insert wait states during RD operations from the AD573. This will not be a problem in systems using memories with comparable access times, since wait states will have already been provided in the basic system design.

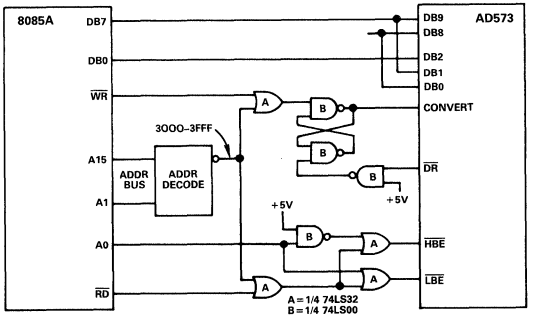


Figure 17. AD573–8085A Interface Connections

The following assembly-language subroutine can be used to control an AD573 residing at memory locations 3000_H and 3001_H. The 10 bits of data are returned (left-justified) in the DE register pair.

```
ADC:  LXI  H,3000  ;LOAD HL WITH AD573 ADDRESS
      MOV  M,A     ;START CONVERSION
      MVI  B,06    ;LOAD DELAY PERIOD
LOOP: DCR  B       ;DELAY LOOP
      JNZ  LOOP    ;
      MOV  A,M     ;READ LOW BYTE
      ANI  C0      ;MASK LOWER 6 BITS
      MOV  E,A     ;STORE CLEAN LOW BYTE IN E
      INR  L       ;LOAD HIGH BYTE ADDRESS
      MOV  D,M     ;MOVE HIGH BYTE TO D
      RET          ;EXIT
```

ANALOG DEVICES

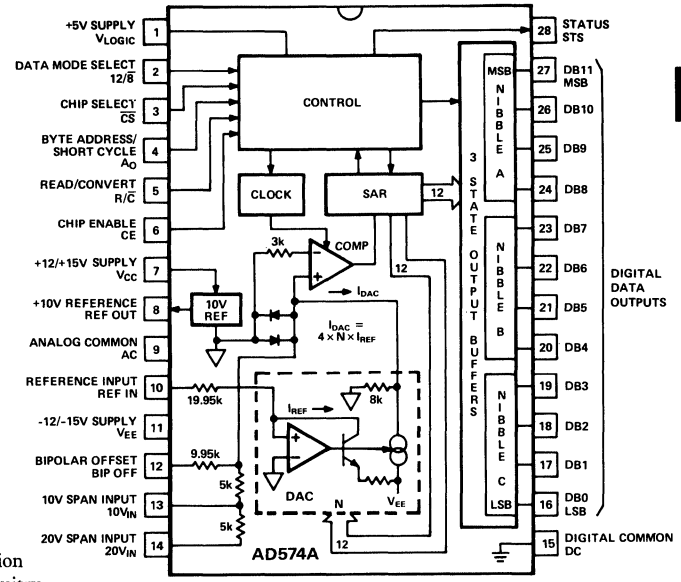
Complete 12-Bit A/D Converter

AD574A*

FEATURES

Complete 12-Bit A/D Converter with Reference and Clock
8- and 16-Bit Microprocessor Bus Interface
Guaranteed Linearity Over Temperature
0 to +70°C – AD574AJ, K, L
−55°C to +125°C – AD574AS, T, U
No Missing Codes Over Temperature
35μs Maximum Conversion Time
Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL
12.5ppm/°C max AD574AU
Ceramic DIP, Plastic DIP or PLCC Package

AD574A BLOCK DIAGRAM AND PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8- or 16-bit microprocessor bus. A high-precision voltage reference and clock are included on-chip, and the circuit guarantees full-rated performance without external circuitry or clock signals.

The AD574A design is implemented using Analog Devices' Bipolar/I^2L process, and integrates all analog and digital functions on one chip. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors at the wafer stage. The voltage reference uses an implanted buried Zener for low noise and low drift. On the digital side, I^2L logic is used for the successive-approximation register, control circuitry and 3-state output buffers.

The AD574A is available in six different grades. The AD574AJ, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, T, and U are specified for the −55°C to +125°C range. All grades are available in a 28-pin hermetically-sealed ceramic DIP. The J, K, and L grades are also available in a 28-pin plastic DIP and PLCC.

The S, T, and U grades are available with optional processing to MIL-STD-883C Class B. The Analog Devices' Military Products Databook should be consulted for details on /883B testing of the AD574A.

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 and 0 to +20 volts unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried Zener reference is trimmed to 10.00 volts with 0.2% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond the requirements of the reference and bipolar offset resistors.

SPECIFICATIONS (@ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise indicated)

Model	AD574AJ Min	AD574AJ Typ	AD574AJ Max	AD574AK Min	AD574AK Typ	AD574AK Max	AD574AL Min	AD574AL Typ	AD574AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			0.25			0.25			0.125	% of F.S.
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2(10)			±1(5)			±1(5)	LSB (ppm/°C)
Bipolar Offset			±2(10)			±1(5)			±1(5)	LSB (ppm/°C)
Full-Scale Calibration			±9(50)			±5(27)			±2(10)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min}–T_{max})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE}≤500μA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK}≤1.6mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output current (available for external loads)[3] (External load should not change during conversion)			1.5			1.5			1.5	mA
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574AKD			AD574ALD		
Plastic (N-28)		AD574AJN			AD574AKN			AD574ALN		
PLCC (P-28A)		AD574AJP			AD574AKP					

NOTES
[1]Detailed Timing Specifications appear in the Timing Section.
[2]12/8 Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.
[3]The reference should be buffered for operation on ±12V supplies.
[4]See Section 14 for package outline information.

Specifications subject to change without notice.

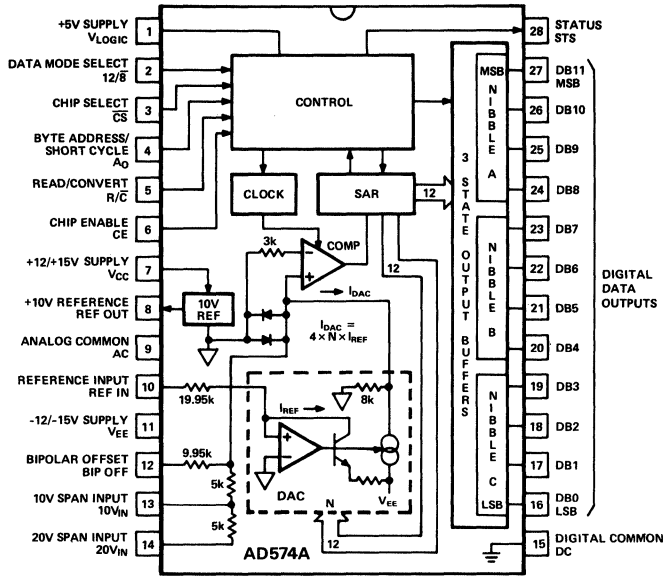
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD574AS Min	AD574AS Typ	AD574AS Max	AD574AT Min	AD574AT Typ	AD574AT Max	AD574AU Min	AD574AU Typ	AD574AU Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)			0.25			0.25			0.125	% of F.S.
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2(5)			±1(2.5)			±1(2.5)	LSB (ppm/°C)
Bipolar Offset			±4(10)			±2(5)			±1(2.5)	LSB (ppm/°C)
Full-Scale Calibration			±20(50)			±10(25)			±5(12.5)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min}–T_{max})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage ($I_{SOURCE} \leq 500\mu A$)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage ($I_{SINK} \leq 1.6mA$)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output current (available for external loads)[3] (External load should not change during conversion)			1.5			1.5			1.5	mA
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574ATD			AD574AUD		

NOTES
[1]Detailed Timing Specifications appear in the Timing Section.
[2]12/$\overline{8}$ Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.
[3]The reference should be buffered for operation on ±12V supplies.
[4]See Section 14 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



AD574A Block Diagram and Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{EE} to Digital Common . . . . . 0 to −16.5V
V_{LOGIC} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common . . −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common . . . . . V_{EE} to V_{CC}
$20V_{IN}$ to Analog Common . . . . . ±24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}

Chip Temperature . . . . . 175°C
Power Dissipation 825mW
Lead Temperature, Soldering . . . . . +300°C, 10 sec.
Storage Temperature (Ceramic) . . . . . −65°C to +150°C
(Plastic) . . . . . −25°C to +100°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD574A ORDERING GUIDE

Model*	Temp. Range	Linearity Error Max (T_{min} to T_{max})	Resolution No Missing Codes (T_{min} to T_{max})	Max Full Scale T.C. (ppm/°C)
AD574AJ(X)	0 to +70°C	±1LSB	11 Bits	50.0
AD574AK(X)	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574AL(X)	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574AS(X)	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574AT(X)	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574AU(X)	−55°C to +125°C	±1LSB	12 Bits	12.5

NOTES
*X = Package designator. Available packages are:
D (D-28) for all grades.
E (E-28) for J, K, S, T, U grades.
N (N-28) for J, K, and L grades.
P for PLCC in J, K grades.
Example: AD574AKN is K grade in plastic DIP.

THE AD574A OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING TEMPERATURE RANGE

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR
Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574AK, L, T, and U grades are guaranteed for maximum nonlinearity of ± 1/2LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574AJ and S grades are guaranteed to ± 1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)
A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD574AK, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574AJ and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET
The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET
In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

QUANTIZATION UNCERTAINTY
Analog-to-digital converters exhibit an inherent quantization uncertainty of ± 1/2LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA
The data format used in the AD574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

FULL-SCALE CALIBRATION ERROR
The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full-scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 3 and 4.

TEMPERATURE COEFFICIENTS
The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION
The standard specifications for the AD574A assume use of +5.00 and ± 15.00 or ± 12.00V supplies. The only effect of power supply error on the performance of the device will be a small change in the full-scale calibration. This will result in a linear change in all lower-order codes. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

CODE WIDTH
A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full-scale range or 2.44mV out of 10 volts for a 12-bit ADC.

CIRCUIT OPERATION

The AD574A is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574A is shown in Figure 1.

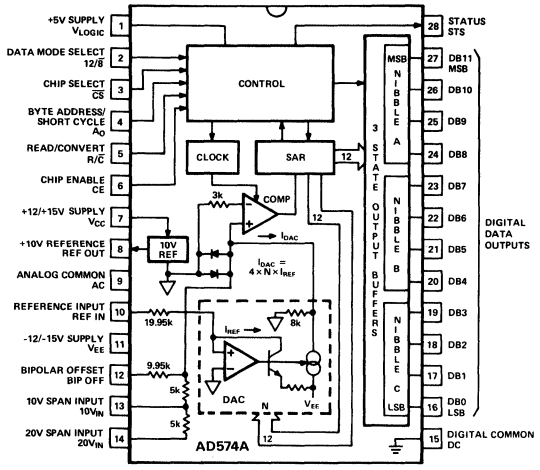


Figure 1. Block Diagram of AD574A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most significant bit (MSB) to least significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2LSB.

The temperature-compensated buried zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±0.2%; it can supply up to 1.5mA to an external load in addition to the requirements of the reference input resistor (0.5mA) and bipolar offset resistor (1mA) when the AD574A is powered from ±15V supplies. If the AD574A is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD574A reference must remain constant during conversion. The thin-film application resistors are trimmed to match the full-scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation and connected to the 10 volt reference for bipolar operation.

DRIVING THE AD574 ANALOG INPUT

The internal circuitry of the AD574 dictates that its analog input be driven by a low source impedance. Voltage changes at the current summing node of the internal comparator result in abrupt modulations of the current at the analog input. For accurate 12-bit conversions the driving source must be capable of holding a constant output voltage under these dynamically changing load conditions.

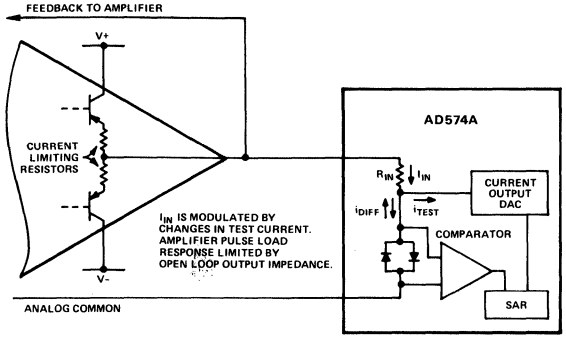


Figure 2. Op Amp – AD574A Interface

The output impedance of an op amp has an open-loop value which, in a closed loop, is divided by the loop gain available at the frequency of interest. The amplifier should have acceptable loop gain at 500kHz for use with the AD574A. To check whether the output properties of a signal source are suitable, monitor the AD574's input with an oscilloscope while a conversion is in progress. Each of the 12 disturbances should subside in 1μs or less.

For applications involving the use of a sample-and-hold amplifier, the AD585 is recommended. The AD711 or AD544 op amps are recommended for dc applications.

SAMPLE-AND-HOLD AMPLIFIERS

Although the conversion time of the AD574A is a maximum of 35μs, to achieve accurate 12-bit conversions of frequencies greater than a few Hz requires the use of a sample-and-hold amplifier (SHA). If the voltage of the analog input signal driving the AD574A changes by more than 1/2LSB over the time interval needed to make a conversion, then the input requires a SHA.

The AD585 is a high-linearity SHA capable of directly driving the analog input of the AD574A. The AD585's fast acquisition time, low aperture and low aperture jitter are ideally suited for high-speed data acquisition systems. Consider the AD574A converter with a 35μs conversion time and an input signal of 10V p-p: the maximum frequency which may be applied to achieve rated accuracy is 1.5Hz. However, with the addition of an AD585, as shown in Figure 3, the maximum frequency increases to 26kHz.

The AD585's low output impedance, fast-loop response, and low droop maintain 12-bits of accuracy under the changing load conditions that occur during a conversion, making it suitable for use in high-accuracy conversion systems. Many other SHAs cannot achieve 12-bits of accuracy and can thus compromise a system. The AD585 is recommended for AD574A applications requiring a sample and hold.

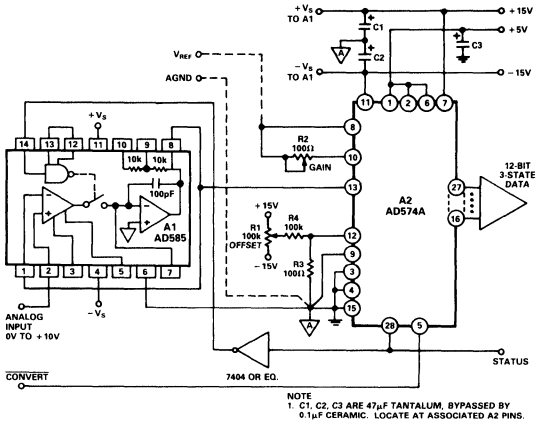


Figure 3. AD574A with AD585 Sample and Hold

SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

It is critically important that the AD574A power supplies be filtered, well regulated, and free from high-frequency noise. Use of noisy supplies will cause unstable output codes. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Remember that a few millivolts of noise represents several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitor should be connected directly from pin 1 to pin 15 (digital common) and the $+V_{CC}$ and $-V_{EE}$ pins should be decoupled directly to analog common (pin 9). A suitable decoupling capacitor is a 4.7μF tantalum type in parallel with a 0.1μF disc ceramic type.

Circuit layout should attempt to locate the AD574A, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred.

GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574A; it should be connected directly to the analog reference point of the system. In order to achieve all of the high-accuracy performance available from the AD574A in an environment of high digital noise content, the analog and digital commons should be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD574A

The AD574A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +12/+15 and −12/−15 volts), the analog input, and the conversion initiation command, as discussed on the next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

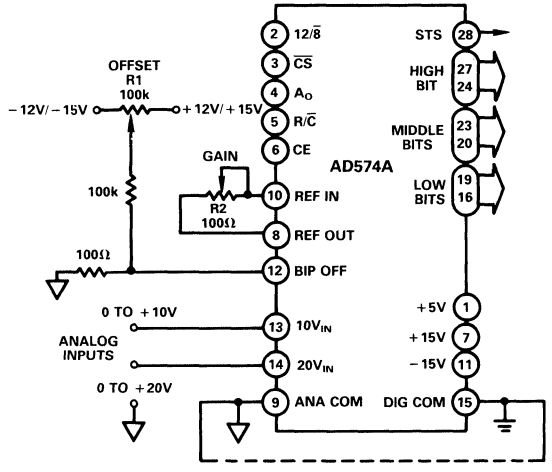


Figure 4. Unipolar Input Connections

All of the thin-film application resistors of the AD574A are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574AK guarantees ±1LSB max zero offset error and ±0.25% (10LSB) max full-scale error. (Typical full-scale error is ±2LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full-scale trim is not needed, a 50Ω ±1% metal film resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574A easily accommodates an input signal beyond the supplies. For the 10 volt span input, the LSB has a nominal value of 2.44mV; for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13 for a full-scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14. The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is 5kΩ, and 10kΩ into pin 14.

UNIPOLAR CALIBRATION

The AD574A is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of + 1/2LSB (1.22mV for 10V range).

If pin 12 is connected to pin 9, the unit will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ± 15mV of offset trim range.

The full-scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 5. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ± 1% fixed resistor. Bipolar calibration is similar to unipolar calibration. First, a signal ½LSB above negative full scale (−4.9988V for the ±5V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1½LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

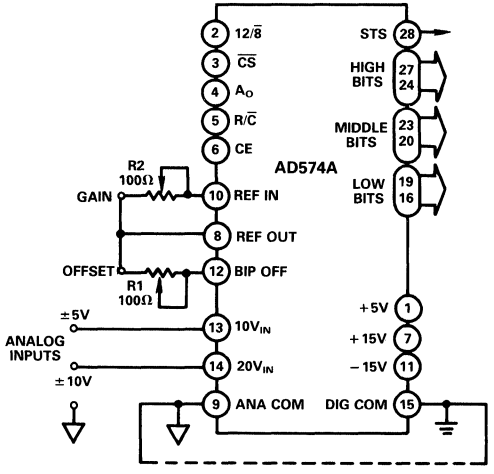
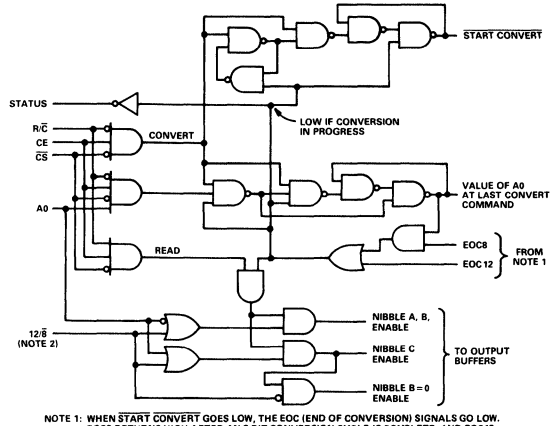


Figure 5. Bipolar Input Connections

CONTROL LOGIC

The AD574A contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 6 shows the internal logic circuitry of the AD574A.

The control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data read (R/$\overline{C}$ = 1) or a convert (R/$\overline{C}$ = 0) is in progress. The register control inputs A_0 and 12/$\overline{8}$ control conversion length and data format. The A_0 line is usually tied to the least significant bit of the address bus. If a conversion is started with A_0 low, a full 12-bit conversion cycle is initiated. If



NOTE 1: WHEN $\overline{START\ CONVERT}$ GOES LOW, THE EOC (END OF CONVERSION) SIGNALS GO LOW. EOC8 RETURNS HIGH AFTER AN 8-BIT CONVERSION CYCLE IS COMPLETE, AND EOC12 RETURNS HIGH WHEN ALL 12 BITS HAVE BEEN CONVERTED. THE EOC SIGNALS PREVENT DATA FROM BEING READ DURING CONVERSIONS.

NOTE 2: 12/$\overline{8}$ IS NOT A TTL-COMPATIBLE INPUT AND SHOULD ALWAYS BE WIRED DIRECTLY TO V_{LOGIC} OR DIGITAL COMMON.

Figure 6. AD574A Control Logic

A_0 is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word (12/$\overline{8}$ tied to V_{LOGIC}). The 12/$\overline{8}$ pin is not TTL-compatible and must be hard-wired to either V_{LOGIC} or DIGITAL COMMON. In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

It is not recommended that A_0 change state during a data read operation. Asymmetrical enable and disable times of the three-state buffers could cause internal bus contention resulting in potential damage to the AD574A.

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	Pin 1	X	Enable 12-Bit Parallel Output
1	0	1	Pin 15	0	Enable 8 Most Significant Bits
1	0	1	Pin 15	1	Enable 4LSBs + 4 Trailing Zeroes

Table I. AD574A Truth Table

TIMING

The AD574A is easily interfaced to a wide variety of microprocessors and other digital systems. The following discussion of the timing requirements of the AD574A control signals should provide the system designer with useful insight into the operation of the device.

CONVERT START TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE			400	ns
t_{HEC}	CE Pulse Width	300			ns
t_{SSC}	$\overline{CS}$ to CE Setup	300			ns
t_{HSC}	$\overline{CS}$ Low During CE High	200			ns
t_{SRC}	R/$\overline{C}$ to CE Setup	250			ns
t_{HRC}	R/$\overline{C}$ Low During CE High	200			ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	300			ns
t_C	Conversion Time				
	8-Bit Cycle	10		24	µs
	12-Bit Cycle	15		35	µs

Figure 7 shows a complete timing diagram for the AD574A convert start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention. Either CE or $\overline{CS}$ may be used to initiate a conversion; however, use of CE is recommended since it includes one less propagation delay than $\overline{CS}$ and is the faster input. In Figure 7, CE is used to initiate the conversion.

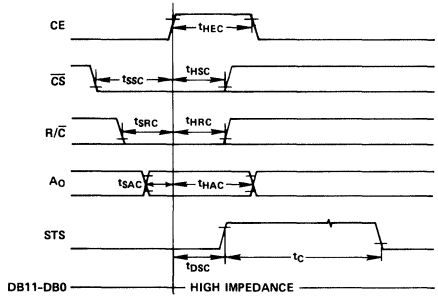


Figure 7. Convert Start Timing

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffers cannot be enabled during conversion.

Figure 8 shows the timing for data read operations. During data read operations, access time is measured from the point where CE and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low). If $\overline{CS}$ is used to enable the device, access time is extended by 100ns.

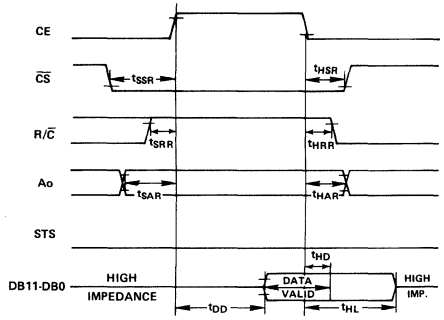


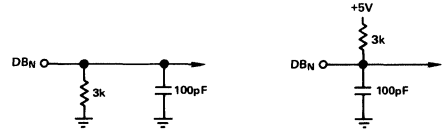
Figure 8. Read Cycle Timing

In the 8-bit bus interface mode (12/$\overline{8}$ input wired to DIGITAL COMMON), the address bit, A_0, must be stable at least 150ns prior to $\overline{CE}$ going high and must remain stable during the entire read cycle. If A_0 is allowed to change, damage to the AD574A output buffers may result.

READ TIMING – FULL CONTROL MODE

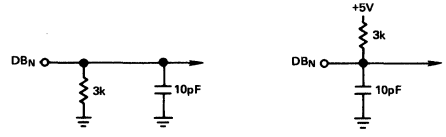
Symbol	Parameter	Min	Typ	Max	Units
t_{DD}[1]	Access Time (from CE)			200	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}[2]	Output Float Delay			100	ns
t_{SSR}	$\overline{CS}$ to CE Setup	150			ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	150			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE low	50			ns

[1] t_{DD} is measured with the load circuit of Figure 9 and defined as the time required for an output to cross 0.4V or 2.4V.
[2] t_{HL} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 10.



a. High-Z to Logic 1 *b. High-Z to Logic 0*

Figure 9. Load Circuit for Access Time Test



a. Logic 1 to High-Z *b. Logic 0 to High-Z*

Figure 10. Load Circuit for Output Float Delay Test

"STAND-ALONE" OPERATION

The AD574A can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This allows two possible control signals – a high pulse or a low pulse. Operation with a low pulse is shown in Figure 11. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return

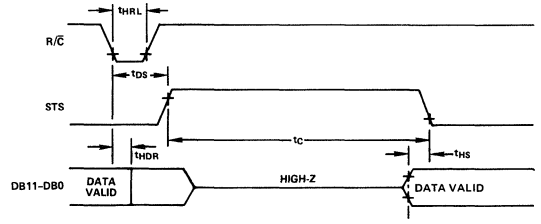


Figure 11. Low Pulse for R/$\overline{C}$ – Outputs Enabled After Conversion

to valid logic levels after the conversion cycle is completed. The STS line goes high 600ns after R/$\overline{C}$ goes low and returns low 300ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 12, the data lines are enabled during the time when R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion, and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

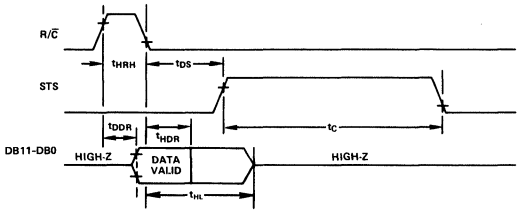


Figure 12. High Pulse for R/$\overline{C}$ – Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	250			ns
t_{DS}	STS Delay from R/$\overline{C}$			600	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HL}	Output Float Delay			150	ns
t_{HS}	STS Delay After Data Valid	300		1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	300			ns
t_{DDR}	Data Access Time			250	ns

Usually the low pulse for R/$\overline{C}$ stand-alone mode will be used. Figure 13 illustrates a typical stand-alone confirguration for 8086 type processors. The addition of the 74F/S374 latches improves bus access/release times and helps minimize digital feedthrough to the analog portion of the converter.

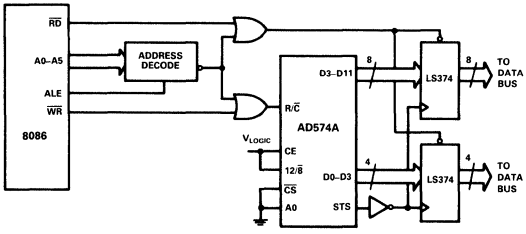


Figure 13. 8086 Stand-Alone Configuration

INTERFACING THE AD574A TO MICROPROCESSORS

The control logic of the AD574A makes direct connection to most microprocessor system buses possible. While it is impossible to describe the details of the interface connections for every microprocessor type, several representative examples will be described here.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD574A provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD574A is only 35 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 35 microseconds to convert, and insert a sufficient number of "do-nothing" instructions to ensure that 35 microseconds of processor time is consumed.

Once it is established that the conversion is finished, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD574A includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by connection of the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A0 low) contains the 8MSBs (DB11 through DB4). The odd address (A0 high) contains the 4LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

It is not possible to rearrange the AD574A data lines for right-justified 8-bit bus interface.

	D7							D0
XXX0 (EVEN ADDR):	DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4
XXX1 (ODD ADDR):	DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

Figure 14. AD574A Data Format for 8-Bit Bus

SPECIFIC PROCESSOR INTERFACE EXAMPLES

Z-80 System Interface

The AD574A may be interfaced to the Z-80 processor in an I/O or memory mapped configuration. Figure 15 illustrates an I/O mapped configuration. The Z-80 uses address lines A0-A7 to decode the I/O port address.

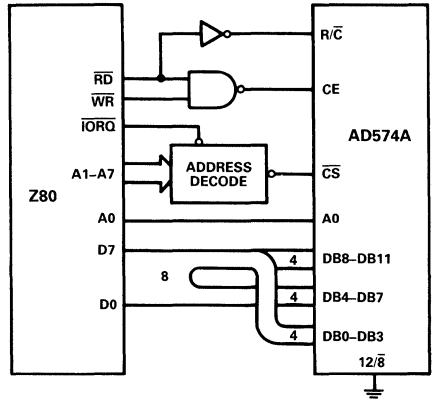


Figure 15. Z80–AD574A Interface

An interesting feature of the Z-80 is that during I/O operations a single wait state is automatically inserted, allowing the AD574A to be used with Z-80 processors having clock speeds up to 4MHz. For applications faster than 4MHz use the wait state generator in Figure 16. In a memory mapped configuration the AD574A may be interfaced to Z-80 processors with clock speeds of up to 2.5MHz.

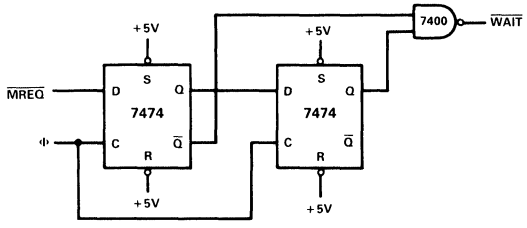


Figure 16. Wait State Generator

IBM PC Interface

The AD574A appears in Figure 17 interfaced to the 4MHz 8088 processor of an IBM PC. Since the device resides in I/O space, its address is decoded from only the lower ten address lines and must be gated with AEN (active low) to mask out internal DMA cycles which use the same I/O address space. This active low signal is applied to $\overline{CS}$. $\overline{IOR}$ and $\overline{IOW}$ are used to initiate the conversion and read, and are gated together to drive the chip enable, CE. Because the data bus width is limited to 8 bits, the AD574A data resides in two adjacent addresses selected by A0.

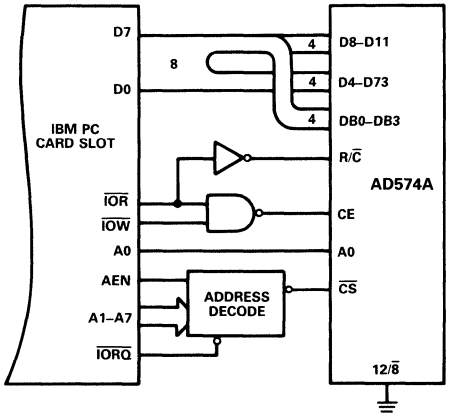


Figure 17. IBM PC – AD574A Interface

Note: Due to the large number of of options that may be installed in the PC, the I/O bus loading should be limited to one Schottky TTL load. Therefore, a buffer/driver should be used when interfacing more than two AD574As to the I/O bus.

8086 Interface

The data mode select pin (12/$\overline{8}$) of the AD574A should be connected to V_{LOGIC} to provide a 12-bit data output. To prevent possible bus contention, a demultiplexed and buffered address/data bus is recommended. In the cases where the 8-bit short conversion cycle is not used, A0 should be tied to digital common. Figure 18 shows a typical 8086 configuration.

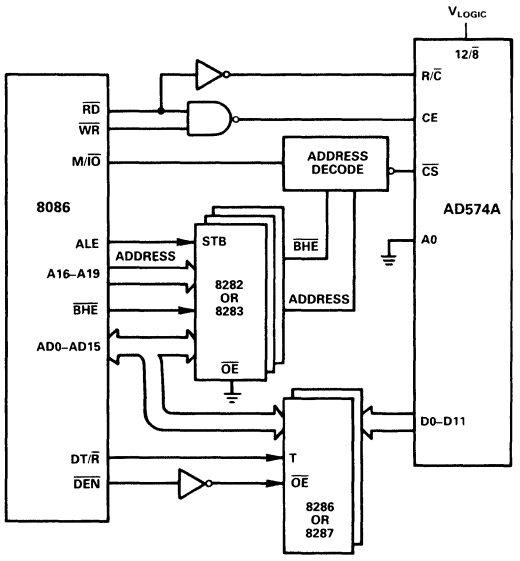


Figure 18. 8086 – AD574A with Buffered Bus Interface

For clock speeds greater than 4MHz wait state insertion similar to Figure 16 is recommended to ensure sufficient CE and R/$\overline{C}$ pulse duration.

The AD574A can also be interfaced in a stand-alone mode (see Figure 13). A low-going pulse derived from the 8086's $\overline{WR}$ signal logically ORed with a low address decode starts the conversion. At the end of the conversion, STS clocks the data into the three-state latches.

68000 Interface

The AD574, when configured in the stand-alone mode, will easily interface to the 4MHz version of the 68000 microprocessor. The 68000 R/$\overline{W}$ signal combined with a low address decode initiates conversion. The $\overline{UDS}$ or $\overline{LDS}$ signal, with the decoded address, generates the $\overline{DTACK}$ input to the processor, latching in the AD574A's data. Figure 19 illustrates this configuration.

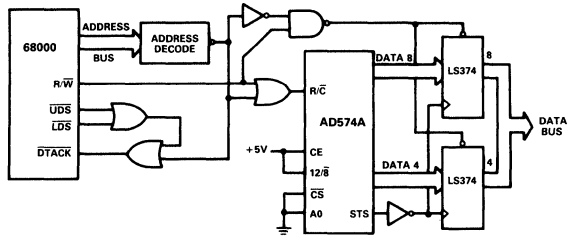


Figure 19. 68000 – AD574A Interface

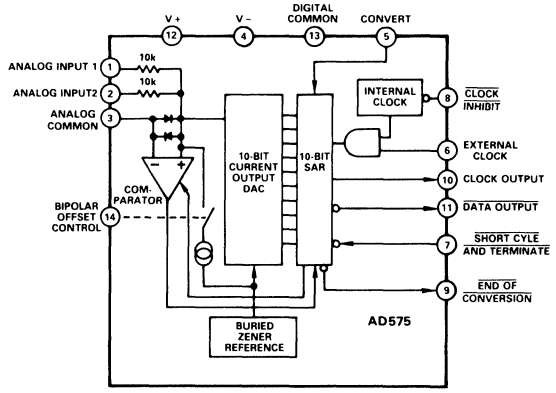
Complete 10-Bit A/D Converter with Serial Output

AD575*

FEATURES

Complete Serial Output 10-Bit A/D Converter with Reference, Clock and Comparator
30μs Conversion
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Low Cost Monolithic Construction
Internal or External Clock
Triggered or Continuous Conversions
Short Cycle Capability

AD575 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD575 is a complete 10-bit successive-approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and serial interface on a single chip. No additional components are required to perform a full-accuracy 10-bit conversion in 30μs.

The AD575 incorporates the most advanced integrated circuit design and processing technology available. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the SiCr thin-film resistor ladder network at the wafer stage insures high accuracy, which is maintained with a temperature-compensated sub-surface zener reference.

Operating on supplies of +5V and −12V to −15V, the AD575 will accept full scale analog inputs of 0V to +10V, 0V to +20V, −5V to +5V or −10V to +10V. The rising edge of a positive pulse on the CONVERT line initiates the conversion cycle. Eleven pulses will appear at the CLOCK OUTPUT pin with data valid on the falling edges of the clock waveform. The data is presented serially beginning with the MSB which is valid on the falling edge of the second clock pulse. The part may be programmed to perform 8-bit conversions or short cycled to 2-, 4-, 6- or 8-bit word lengths. $\overline{EOC}$ indicates that conversion is complete. The AD575 may be synchronized to an external clock if desired.

The AD575 is available in two versions for the 0 to +70°C temperature range, the AD575J and AD575K. The AD575S guarantees ±1LSB relative accuracy and no missing codes from −55°C to +125°C.

***Protected by U.S. Patent Nos. 3,940,760; 4,400,689; and 4,400,690.**

Two package types are available. All versions are offered in a 14-pin hermetically-sealed ceramic DIP. The AD575J and AD575K are also available in a 14-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD575 is a complete 10-bit A/D converter. No external active components or control signals are required to perform a conversion.
2. The serial output of the AD575 allows a wide range of microprocessor interfacing and data transmission possibilities.
3. The device offers true 10-bit relative accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD575 adapts to unipolar or bipolar analog inputs by grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.
6. The AD575 can be synchronized to an external clock.
7. Conversions can be initiated externally or internally.
8. The AD575 can be short-cycled to 8 bits by pin programming.
9. The Short Cycle and Terminate feature allows the user to program conversions of 2, 4, 6 or 8 bits.

SPECIFICATIONS (@ 25°C, V+ = +5V, V− = −12V or −15V, unless otherwise noted)

	AD575J			AD575K			AD575S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION										
For Which No Missing Codes is Guaranteed	10			10			10			Bits
T_{min} to T_{max}	9			10			10			Bits
UNIPOLAR OFFSET			±2			±1			±2	LSB
T_{min} to T_{max}			±2			±1			±2	LSB
BIPOLAR ZERO			±2			±1			±2	LSB
T_{min} to T_{max}			±2			±1			±2	LSB
GAIN ERROR[1]		±2				±2			±2	LSB
GAIN DRIFT[2]										
T_{min} to +25°C			±2			±1			±5	LSB
+25°C to T_{max}			±4			±2			±5	LSB
RELATIVE ACCURACY[3]			±1			±1/2			±1	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
POWER SUPPLY REJECTION[4]										
Positive Supply:										
+4.5V≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply:										
−15.75V≤V−≤−14.25V			±2			±1			±2	LSB
−12.6V≤V−≤−11.4V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE										
Pin 1, Pin 2	6	10	14	6	10	14	6	10	14	kΩ
ANALOG INPUT RANGES										
Unipolar		0 to 10			0 to 10			0 to 10		V
		0 to 20			0 to 20			0 to 20		V
Bipolar		−5 to +5			−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10			−10 to +10		V
OUTPUT CODING										
Unipolar	NEGATIVE TRUE BINARY			NEGATIVE TRUE BINARY			NEGATIVE TRUE BINARY			
Bipolar	NEGATIVE TRUE OFFSET BINARY			NEGATIVE TRUE OFFSET BINARY			NEGATIVE TRUE OFFSET BINARY			
LOGIC OUTPUTS (T_{min} to T_{max})										
V_{OL} @ I_{SINK} = 3.2mA	0		0.4	0		0.4	0		0.4	V
V_{OH} @ I_{SOURCE} = 0.5mA	2.4		5.0	2.4		5.0	2.4		5.0	V
LOGIC INPUTS (T_{min} to T_{max})										
I_{INH} @ V_{IN} = 5V[5]			+50			+50			+50	μA
I_{INL} @ V_{IN} = 0V[5]	−800			−800			−800			μA
V_{INH}	2.0		5.5	2.0		5.5	2.0		5.5	V
V_{INL}	0		0.8	0		0.8	0		0.8	V
CONVERSION TIME (T_{min} to T_{max})										
Internal Clock	10	20	30	10	20	30	10	20	30	μs
External Clock	25			25			25			μs
POWER SUPPLY										
V+	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	V
V−	−11.4		−15.75	−11.4		−15.75	−11.4		−15.75	V
OPERATING CURRENT										
V+		15	25		15	25		15	25	mA
V−		9	15		9	15		9	15	mA

NOTES

[1]Gain Error is specified with a 15Ω resistor in series with the 10V input (Pins 1 and 2 tied together) or a 30Ω resistor in series with the 20V input (Pin 1 with Pin 2 tied to analog common). Gain Error is guaranteed trimmable to zero (see text).

[2]The gain drift is calculated from gain measurements at the extremes of the temperature range under consideration.

[3]Relative Accuracy, also referred to as Integral Linearity, is defined as the deviation of the code transition points from the ideal transfer points on a straight line from zero to full-scale. It is also a measure of the error which remains when offset and full scale errors are trimmed to zero in an application.

[4]Measured at full scale.

[5]These specifications apply to the CONV, XCL, and $\overline{SCAT}$ inputs. $\overline{CLI}$ is hardwired to DGND or $+V_S$ in most applications. Typically I_{INH} = +350μA and I_{INL} = 120μA for the $\overline{CLI}$ input.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . 0 to +7V
V− to Digital Common . . . . . 0 to −16.5V
Analog Common to Digital Common . . . . . ±1V
Analog Inputs . . . . . (V−) −0.3V to +22V
Control Inputs . . . . . 0 to V+
Power Dissipation 800mW

NOTE
All pins must be kept more positive than (V−) −0.3V.

AD575 ORDERING GUIDE

Model	Package Options*	Temperature Range −°C	Relative Accuracy
AD575JN	N-14	0 to +70	±1LSB max
AD575KN	N-14	0 to +70	±1/2LSB max
AD575JD	D-14	0 to +70	±1LSB max
AD575KD	D-14	0 to +70	±1/2LSB max
AD575SD	D-14	−55 to +125	±1LSB max

*See Section 14 for package outline information.

FUNCTIONAL DESCRIPTION

A block diagram of the AD575 is shown in Figure 1. A conversion is initiated by a positive pulse on the CONVERT line. $\overline{EOC}$ goes high within 150ns indicating that a conversion has started. The internal 10-bit current-output DAC is sequenced by the successive approximation register (SAR) from most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 10kΩ input resistor(s). The comparator determines whether the addition of each successively-weighted bit current causes the DAC current to be higher or lower than the input current. If the sum is less the bit is left on ($\overline{DO}$ set low). If the sum is more, the bit is turned off ($\overline{DO}$ set high). The result of each bit decision is passed to $\overline{DO}$ on the rising edge of CO.

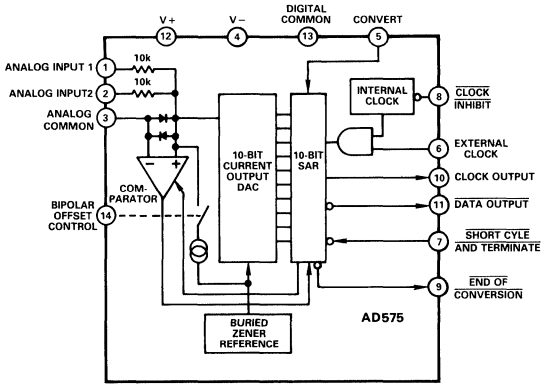


Figure 1. AD575 Functional Block Diagram

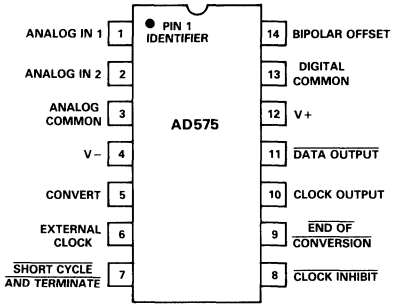


Figure 2. AD575 Pin Connections

After all bits have been tested, the DAC output current will match the input signal current to within 0.05% (1/2LSB). $\overline{EOC}$ returns low after the final bit decision to indicate that the AD575 has been reset and is ready to perform a new conversion. The output data stream can be synchronized to an external clock using the XCL input and short cycled to any desired word length using the $\overline{SCAT}$ line.

The AD575 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is to connect the power supplies (+5V and −12V or −15V), and the analog input. The pinout is shown in Figure 2.

ANALOG INPUT CONNECTIONS

The AD575 can be configured for unipolar or bipolar operation on 10V span or 20V span input signals. The appropriate input range is selected by connecting pins 2 and 14 according to the table of Figure 3.

The AD575's low offset and gain errors (shown in the Specifications) are adequate for most applications. For these cases, a fixed gain resistor (R2 in Figure 3) is the only external component, in addition to any power supply decoupling that may be required. Pins 3 and 13 should be connected directly together.

Figure 3 shows a trimming circuit that can be used to adjust the offset to zero, using the appropriate value of the R1 potentiometer as shown in the table. If gain trim is required, R2 should also be replaced by the appropriate potentiometer as shown in the table.

ANALOG INPUT RANGE	CONNECTIONS PIN 2	PIN 14	COMPONENTS R1 (OFFSET)	R2 (GAIN)
0V TO +10V	PIN 1	PIN 13	10Ω	15Ω FIXED OR 50Ω POT
0V TO +20V	PIN 3	PIN 13	20Ω	30Ω FIXED OR 100Ω POT
−5V TO +5V	PIN 1	OPEN	10Ω	15Ω FIXED OR 50Ω POT
−10V TO +10V	PIN 3	OPEN	20Ω	30Ω FIXED OR 100Ω POT

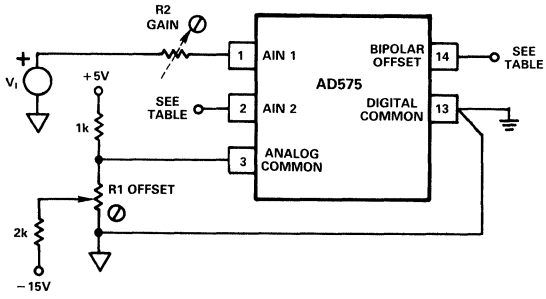


Figure 3. AD575 Input Circuit Showing Offset and Gain Adjustment

UNIPOLAR MODE OPERATION

In unipolar mode, the nominal location of the low side transition of the first code (1111111110) occurs at an input voltage of +1LSB (10mV for the 10V span, 20mV for the 20V span). The offset error of the AD575 can be trimmed out, if required, by applying an input voltage of +1LSB to the analog input and adjusting R1 until the low side transition of the first code occurs.

If the Gain Error needs to be trimmed, the gain resistor should be replaced with a potentiometer according to Figure 3. The nominal location of the low side transition of the full scale code (0000000000) in unipolar mode is full scale minus 1LSB (9.99V for 10V span, 19.98V for 20V span). Once the offset has been adjusted, the full scale range can be set by adjusting the gain potentiometer.

BIPOLAR CONNECTION

If the bipolar offset control (pin 14) is left open, the AD575 will accept bipolar input voltages with 0V as the nominal bipolar zero point. The input voltage corresponding to the low side transition of the mid-scale code (0111111111) is −1/2LSB (−5mV for 10V spans and −10mV for 20V spans). The nominal location of the code transitions are therefore offset by 1/2LSB as shown in Figure 4. This offset may be adjusted using the trim scheme shown in Figure 3 with a 1.2kΩ resistor in place of the 1kΩ resistor shown.

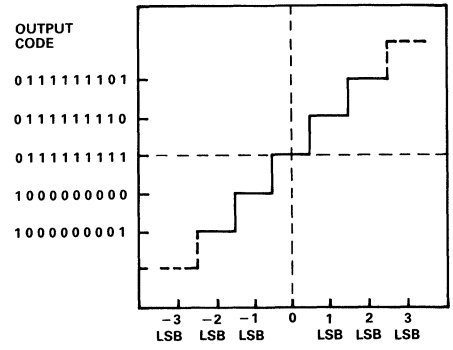


Figure 4. AD575 Transfer Characteristic (Bipolar Operation)

The gain error should be adjusted after any offset adjustment. An input voltage of full scale minus 1 1/2LSBs is applied (4.985V for −5V to +5V range, 9.971V for −10V to +10V range) and R2 is adjusted until the low-side transition of the full scale code (0000000000) occurs.

The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 5.

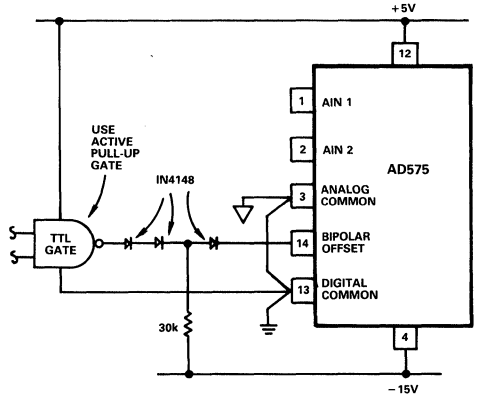


Figure 5. Bipolar Offset Controlled by Logic Gate

CONTROL AND TIMING OF THE AD575

The AD575 has a flexible control architecture which supports several operating modes. It can provide its own clock or it can be synchronized to an external clock. Conversions can be initiated externally, or the part can perform continuous conversions yielding a stream of output data. In addition, the AD575 can be short-cycled to any of several convenient data word lengths to tailor the output to the specific input requirements of the system. Figure 6 shows the control logic diagram of the AD575. The four inputs which control the operation of the AD575 are CONV (convert), $\overline{CLI}$ (clock inhibit), XCL (external clock), and $\overline{SCAT}$ (short cycle and terminate). Three outputs are provided: $\overline{DO}$ (Data Out), CO (Clock Out), and $\overline{EOC}$ (End of Conversion).

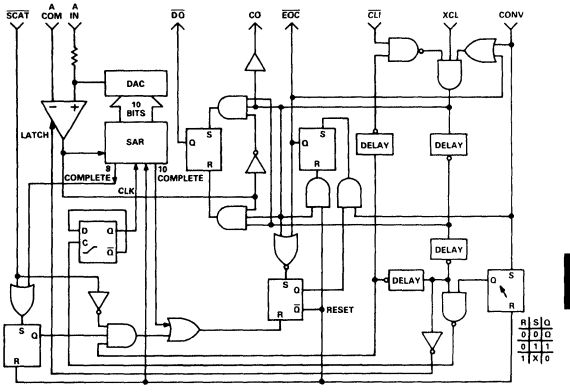


Figure 6. AD575 Control Logic Diagram

EXTERNALLY INITIATED CONVERSIONS

Figure 7 is the timing diagram which illustrates the operation of the AD575 with an externally applied convert signal. Conversions are initiated by a positive-going pulse applied to the CONV (convert) input. This pulse should be at least 250ns wide and should return low before $\overline{EOC}$ returns low to prevent the initiation of a second conversion. If the internal clock is used, the clock will start on the rising edge of the convert start pulse. If an external clock is used, the falling edge of the clock must occur no earlier than 900ns following the rising edge of the convert command.

INTERNAL CLOCK MODE

The AD575 can be configured for internal clock operation by tying $\overline{CLI}$ and XCL to +5V. CO (clock output) provides the necessary synchronizing information in this mode. Data is transferred to $\overline{DO}$ on the rising clock edge and is stable on the falling edge. The duty cycle of the CO waveform in this mode will be in the range of 30% to 70%.

EXTERNAL CLOCK MODE

When $\overline{CLI}$ is connected to digital common, an external clock can be applied to XCL. The external clock should have a maximum frequency of 450kHz with a minimum of 900ns in the high or low phase. Arbitrarily slow clocks may be used as long as these minimum high and low periods are observed. Conversion time will increase as clock frequency decreases. Each data bit will be stable within 150ns of the rising edge of the associated external clock pulse and will remain stable until the rising edge of the subsequent clock pulse. Data is guaranteed to be stable on the falling edge of the clock pulse.

The state of the $\overline{DO}$ output during the first clock period is undefined but it is stable until the rising edge of the second clock period. The MSB appears at $\overline{DO}$ during the second clock period. The subsequent data bits are then clocked out until the N^{th} bit or LSB is clocked out on the $(N+1)^{th}$ clock pulse. $\overline{EOC}$ returns low within 150ns of the rising edge of this final clock pulse. In internal clock mode, the output clock pulse associated with the LSB is shorter than the others but the LSB is guaranteed to be stable on the falling edge of this pulse. The LSB will remain stable until a new conversion is initiated. The value of N will be 10 unless the conversion has been short cycled (see "short cycle and terminate" text).

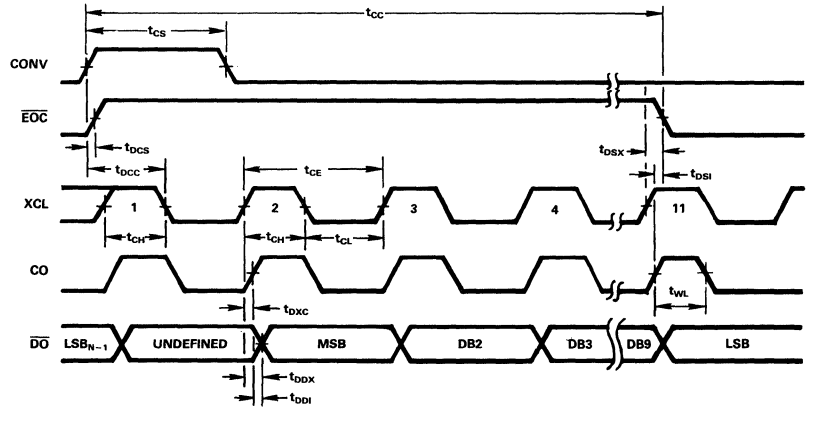


Figure 7. Externally Initiated Conversions

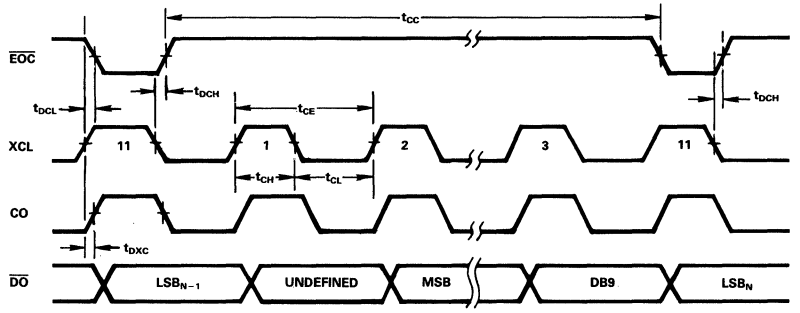


Figure 8. Continuous Conversion Mode (CONV. Held High)

CONTINUOUS CONVERSIONS

Figure 8 is the timing diagram associated with the continuous conversion mode of operation. If CONV is high when $\overline{EOC}$ goes low, another conversion will begin immediately. $\overline{EOC}$ will be set (high) following the falling edge of the $(N+1)^{st}$ CO pulse and conversion commences with the rising edge of the next CO pulse. The $(N+1)^{st}$ CO pulse is not shortened in this mode. If CONVERT is held high the AD575 will put out a continuous stream of conversions, punctuated by $\overline{EOC}$ which will mark the last clock pulse of a conversion. $\overline{EOC}$ will remain low until the falling edge of CO, the output clock, in this mode. Therefore, the rising edge of $\overline{EOC}$ may be used to signal that conversion is complete and that data is transferred. This sequence is useful for initiating parallel dumps from a serially loaded shift register.

SHORT CYCLE AND TERMINATE

For normal 10-bit operation, the Short Cycle and Terminate ($\overline{SCAT}$) line should be tied high. If 8-bit conversions are required, $\overline{SCAT}$ should be tied low. In this mode, $\overline{EOC}$ will go low after the rising edge of the ninth clock pulse to indicate that the eighth and final data bit is valid. This mode is useful when parallel loads to 8-bit data buses are desired since it avoids the complication of suppressing the 9th and 10th data bits.

Conversions of 2, 4, 6 or 8 bits can be performed by pulling $\overline{SCAT}$ low during the negative clock phase prior to the positive clock associated with the desired LSB. Figure 9 illustrates the timing associated with this mode of operation. For example, to terminate the conversion after six data bits, $\overline{SCAT}$ should be driven low during the negative clock phase following the sixth clock pulse. $\overline{EOC}$ will then go low following the rising edge of the seventh clock pulse to indicate that the sixth and final data bit is valid.

This terminate feature can also be used to program conversions of 1, 3, 5, 7 or 9 bits. However, the conversion immediately following a conversion of an odd number of data bits will be spurious. All subsequent conversions will be normal until the conversion following another odd data word length conversion.

The negative edge of the $\overline{SCAT}$ signal should always occur during the negative phase of a clock cycle and it should be held low for a minimum of 900ns. $\overline{SCAT}$ may be held low into the next conversion but it must be restored high at least one clock cycle prior to being used to terminate a conversion. If $\overline{SCAT}$ is not restored high prior to the eighth clock pulse, $\overline{EOC}$ will go low and an 8-bit short cycle will occur. Care should be taken not to pulse $\overline{SCAT}$ from high to low between conversions (when $\overline{EOC}$ is low). This would initiate a terminate sequence which will execute on the rising edge of the first clock pulse following the next Convert command.

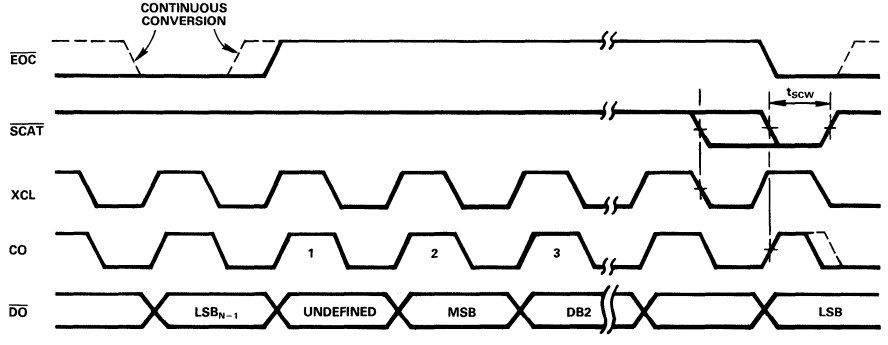


Figure 9. Short Cycle and Terminate Operation

Parameter	Symbol	Min	Typ	Max	Units
EXTERNALLY-INITIATED CONVERSIONS					
Convert Pulse Width	t_{CS}	300			ns
Convert to $\overline{EOC}$ Delay	t_{DCS}			150	ns
CO LSB Clock Pulse Width	t_{WL}	400			ns
XCL to $\overline{EOC}$ Reset	t_{DSX}	50		150	ns
↑ CO to ↓ $\overline{EOC}$ Reset Delay	t_{DSI}	20		150	ns
CONTINUOUS CONVERSIONS					
↑ XCL to ↓ $\overline{EOC}$ Reset Delay	t_{DCL}	50		150	ns
↓ XCL to ↑ $\overline{EOC}$ Delay	t_{DCH}	50		1000	ns
INTERNAL CLOCK TIMING					
Conversion Time	t_{CC}	10	20	30	μs
CO to $\overline{DO}$ Output Delay	t_{DDI}	−100		+100	ns
EXTERNAL CLOCK TIMING					
Conversion Time	t_{CC}	25			μs
↑ XCL to $\overline{DO}$ Output	t_{DDX}	30		150	ns
XCL to CO Output	t_{DXC}	30		160	ns
↑ Convert to ↓ XCL Set-Up Time	t_{DCC}	900			ns
XCL Period	t_{CE}	2.2			μs
XCL High	t_{CH}	900			ns
XCL Low	t_{CL}	900			ns
SHORT CYCLE TIMING					
$\overline{SCAT}$ Pulse Width	t_{SCW}	900			ns

Table I. AD575 Timing Specifications

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD575

Many data acquisition systems for digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A/D converter. A SHA can be used to accurately define the exact point in time at which the signal is sampled. A SHA can also serve as a high input-impedance buffer for the AD575.

Figure 10 shows the AD575 connected to the AD585 monolithic SHA. In this configuration, the AD585 will acquire a 10V signal in less than 2μs and droop less than 1mV/ms using the on-chip hold capacitor.

$\overline{EOC}$ goes high after the conversion is initiated to indicate that a conversion is underway. In Figure 10 it is also used to put the AD585 into the hold mode while the AD575 begins its conversion cycle. (The AD585 output settles to final value well in advance of the first comparator decision within the AD575.) $\overline{EOC}$ goes low when the conversion is complete placing the AD585 back in the sample mode.

Configured as shown in Figure 10, the next conversion can be initiated after a 2μs delay to allow for signal acquisition by the AD585.

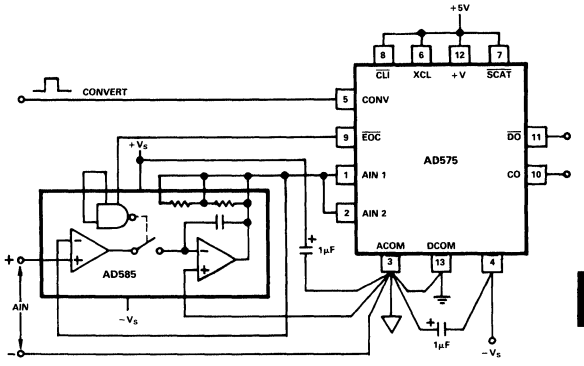


Figure 10. AD575 to AD585 Sample and Hold Interface

SUPPLY DECOUPLING AND LAYOUT

For proper operation, the AD575's power supplies should be free from high-frequency noise. The stability of the transfer function is especially sensitive to noise on the V− supply. Noise on the V+ supply can also propagate to the digital outputs.

If decoupling is required, tantalum capacitors are suggested. Best results will be obtained if the capacitors are connected directly to the appropriate pins of the AD575. Decoupling capacitors for V− should be connected between pin 4 and Analog Common (pin 3). Decoupling capacitors for V+ should be connected between pin 12 and Digital Common (pin 13).

Good circuit layout practice suggests that the AD575 and its associated analog input circuitry be kept separate from system logic circuitry to avoid unwanted interactions.

GROUNDING CONSIDERATIONS

The AD575 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common-mode voltage between the two commons. The absolute maximum voltage rating between the two commons is ±1V. A parallel pair of back-to-back protection diodes should be connected between the commons if they are not connected locally.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

AD575 TO 8085 INTERFACE

The 8085 has both serial output (SOD) and serial input (SID) capability. A simple 3 hardware line interface can be constructed between the AD575 and 8085. These leads can be opto-coupled in order to establish galvanic isolation between the two devices as shown in Figure 11.

The software routine in Table II will read a complete 10-bit data word from the AD575 in 180μs (3MHz 8085). The software generates the clock for the AD575 in order to synchronize the data output with the 8085 serial read operation.

The DATA procedure loads appropriate constants into the 8085 registers and initiates the conversion. The CONV procedure assumes that the AD575 clock was in the high state when the CONVERT pulse was generated (upon completion, this sample routine leaves the SOD line in the appropriate state to insure this). A low clock pulse is generated, and the data bit is read into the MSB of the accumulator. The data bit is then shifted into the LSB of the temporary register (L), the clock is set high, and the procedure is repeated.

After the loop has executed three times, a logical AND is performed to set the first bit (the undefined bit) to zero, and the result is placed into the high byte (H) register. The loop counter is then reset, and the CONV procedure is executed 8 more times. Upon completion of the sample routine, 10 bits of right-justified data will reside in the HL register pair.

Note that the opto-isolators invert the clock and data lines. If these are not used (no inversion present), the constants in the D and E registers should be swapped, a CMA instruction should be inserted after the RIM instruction, and an inverter should be connected between the address decoder and the CONVERT pin. Also, the results of the first pass through the routine should be ignored following power up and reset cycles to insure that the AD575 has been reset.

LABEL	MNEMONIC	OPERAND	COMMENT
DATA	MVI	B,03	Set inner loop counter to 3
	MVI	C,02	Set outer loop counter to 2
	MVI	D,CO	Setup register D for clock low
	MVI	E,40	Setup register E for clock high
	MVI	H,10	AD575 address location
	MVI	L,00	Clear temp register
	MOV	M,B	Generate CONVERT pulse
CONV	MOV	A,D	Setup ACC for clock low
	SIM		Output clock low
	RIM		Read AD575 data bit into ACC
	RAL		Shift data bit into Carry
	MOV	A,L	Move temp to ACC
	RAL		Shift data bit from Carry to ACC
	MOV	L,A	Replace temp
	MOV	A,E	Setup ACC for clock high
	SIM		Output clock high
	DCR	B	Decrement inner loop counter
	JNZ	CONV	Repeat CONV until done
	DCR	C	Decrement outer loop counter
	JZ	DONE	Skip to DONE on 2nd pass
	MOV	A,L	Move temp to ACC
	ANI	03	Mask undefined bit
	MOV	H,A	Store temp in H register
	MVI	B,OB	Set inner loop counter to 8
	JMP	CONV	Repeat CONV for 8 LSBs
DONE	RET		10 bits of right-justified data now reside in HL; return

Table II. Sample Assembly Code for AD575 to 8085 Isolated Interface

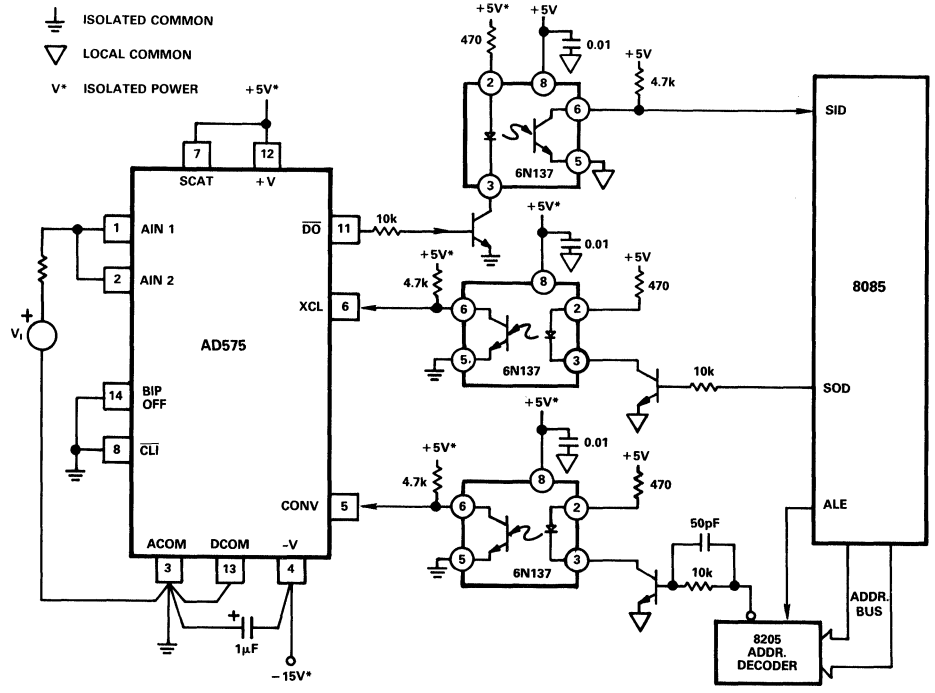


Figure 11. AD575 to 8085 Isolated Interface

ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD578

FEATURES

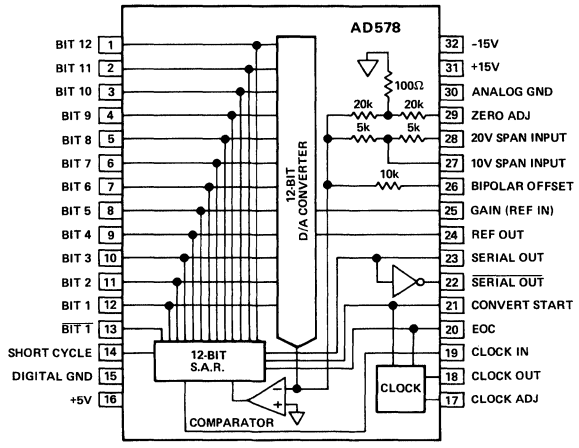
Performance

- **Complete 12-Bit A/D Converter with Reference and Clock**
- **Fast Conversion: 3μs (max)**
- **Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max**
- **Max Nonlinearity: <±0.012%**
- **No Missing Codes Over Temperature**
- **Low Power: 875mW**
- **Hermetic Package Available**
- **Available to MIL-STD-883**

Versatility

- **Positive-True Parallel or Serial Logic Outputs**
- **Short Cycle Capability**
- **Precision +10V Reference for External Applications**
- **Adjustable Internal Clock**
- **"Z" Models for ±12V Supplies**

AD578 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD578 is a high speed 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide superior performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD578 include a maximum linearity error at +25°C of ±0.012%, maximum gain temperature coefficient of ±30ppm/°C, typical power dissipation of 875mW and maximum conversion time of 3μs.

The fast conversion speeds of 3μs (L grade) 4.5μs (K, T grades) and 6μs (J, S grades) make the AD578 an excellent choice in a variety of applications where system throughput rates from 166kHz to 333kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD578 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD578 is available with either the polymer seal (N) for use in benign environmental applications or hermetic solder-seal (D) for more harsh or rigorous surroundings. Both are contained in a 32-pin side-brazed, ceramic DIP.

The AD578S, T are available processed to MIL-STD-883 Level B, Method 5008.

PRODUCT HIGHLIGHTS

1. The AD578 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD578 makes it an excellent choice for high speed data acquisition and digital signal processing applications.
3. The internal buried zener reference is laser trimmed to 10.00V ±1.0% and ±15ppm/°C typical T.C. The reference is available for external use and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The component count is minimized, resulting in low bond wire and chip count and high MTBF.
6. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
7. The integrated package construction provides high quality and reliability with small size and weight.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

Model	AD578J	AD578K	AD578L	AD578SD[1]	AD578TD[1]
RESOLUTION	12 Bits	*	*	*	*
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±5.0V, ±10V	*	*	*	*
Unipolar	0 to +10V, 0 to +20V	*	*	*	*
Input Impedance					
0 to +10V, ±5V	5kΩ	*	*	*	*
±10V, 0 to +20V	10kΩ	*	*	*	*
DIGITAL INPUTS					
Convert Command[2]	1LSTTL Load	*	*	*	*
Clock Input	1LSTTL Load	*	*	*	*
TRANSFER CHARACTERISTICS					
Gain Error[3,4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Unipolar Offset[4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Bipolar Error[4,5]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Linearity Error, 25°C	±1/2LSB max	*	*	*	*
T_{min} to T_{max}	±3/4LSB	*	*	±3/4LSB max	±3/4LSB max
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)					
+25°C	12 Bits	*	*	*	*
T_{min} to T_{max}	12 Bits	*	*	*	*
POWER SUPPLY SENSITIVITY					
+15V ±10%	0.005%/%ΔV_S max	*	*	*	*
−15V ±10%	0.005%/%ΔV_S max	*	*	*	*
+5V ±10%	0.005%/%ΔV_S max	*	*	*	*
TEMPERATURE COEFFICIENTS					
Gain	±15ppm/°C typ	*	*	*	*
	±30ppm/°C max	*	*	±50ppm/°C max	±30ppm/°C max
Unipolar Offset	±3ppm/°C typ	*	*	*	*
	±10ppm/°C max	*	*	±15ppm/°C max	±10ppm/°C max
Bipolar Offset	±8ppm/°C typ	*	*	*	*
	±20ppm/°C max	*	*	±25ppm/°C max	±20ppm/°C max
Differential Linearity	±2ppm/°C typ	*	*	*	*
CONVERSION TIME[6,7,8](max)	6.0μs	4.5μs	3μs	6.0μs	4.5μs
PARALLEL OUTPUTS					
Unipolar Code	Binary	*	*	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*	*	*
Output Drive	2LSTTL Loads	*	*	*	*
SERIAL OUTPUTS (NRZ FORMAT)					
Unipolar Code	Binary/Complementary Binary	*	*	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*	*	*
Output Drive	2LSTTL Loads	*	*	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*	*	*
Output Drive	8LSTTL Loads	*	*	*	*
INTERNAL CLOCK[8]					
Output Drive	2LSTTL Loads	*	*	*	*
INTERNAL REFERENCE					
Voltage	10.000 ±100mV	*	*	*	*
Drift	±12ppm/°C, ±20ppm/°C max	*	*	*	*
External Current	±1mA max	*	*	*	*
POWER SUPPLY REQUIREMENTS[9]					
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	*
Supply Current +15V	3mA typ, 8mA max	*	*	*	*
−15V	22mA typ, 35mA max	*	*	*	*
+5V	100mA typ, 140mA max	*	*	*	*
Power Dissipation	875mW typ	*	*	*	*
TEMPERATURE RANGE					
Operating	0 to +70°C	*	*	−55°C to +125°C	−55°C to +125°C
Storage	−55°C to +150°C	*	*	−65°C to +150°C	−65°C to +150°C

NOTES
[1]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.
[2]Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.
[3]With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.
[4]Adjustable to zero.
[5]With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).
[6]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.
[7]Each grade is specified at the conversion speed shown.
[8]Externally adjustable by a resistor or capacitor (see Figure 7).
[9]For "Z" models order AD578ZJ, ZK, ZL (±11.6V to ±16.5V).
*Specifications same as AD578J.
Specifications subject to change without notice.

THEORY OF OPERATION

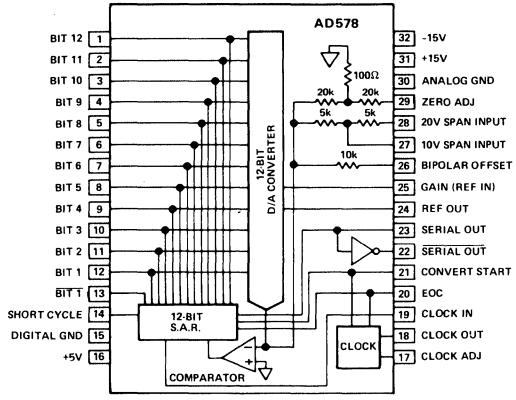


Figure 1. AD578 Functional Diagram and Pinout

The AD578 is a complete pretrimmed 12-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD578 is shown in Figure 1.

When the control section is commanded to initiate a conversion it enables the clock and resets the successive-approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The parallel data bits become valid on the rising edge of the clock pulse starting with t_1 and ending with t_{12} (Figure 2), and accurately represent the input signal to within ±1/2LSB.

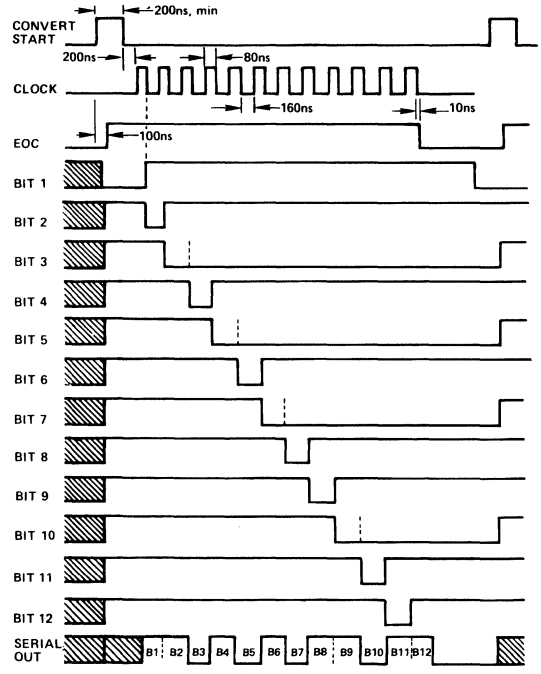
The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1.0%, it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin-film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table I and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±25mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963V for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
[1]THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 2. AD578 3µs Timing Diagram

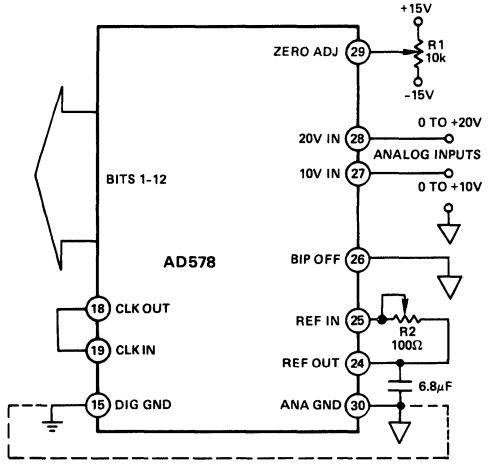


Figure 3. Unipolar Input Connections

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (−4.9988V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

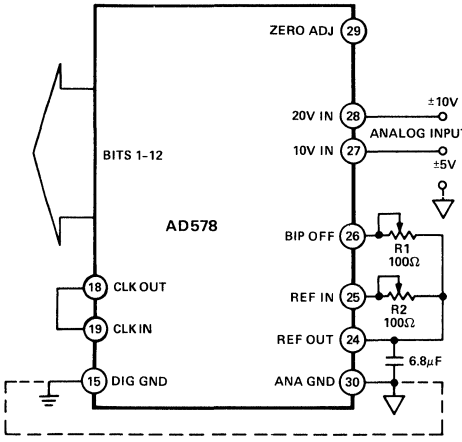


Figure 4. Bipolar Input Connections

LAYOUT CONSIDERATION

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD578's supply terminals should be capacitively decoupled as close to the AD578 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

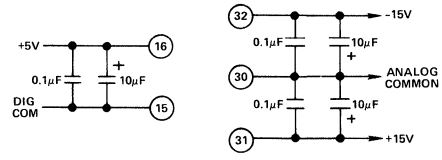


Figure 5. Basic Grounding Practice

To minimize noise the reference output (pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 5.6μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

For slower conversions connect a capacitor between pin 15 and pin 17.

The curves in Figure 6 characterize the conversion time for a given resistor or capacitor connection.

Note: 12-bit operation with no missing codes is not guaranteed when operating in this mode if a particular grade's conversion speed specification has been exceeded.

Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 12-bit resolution. Short cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table II.

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	−5V to +5V Range	−10V to +10V Range	B1 (MSB) B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0024	+0.0051	−4.9976	−9.9951	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0

Table I. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

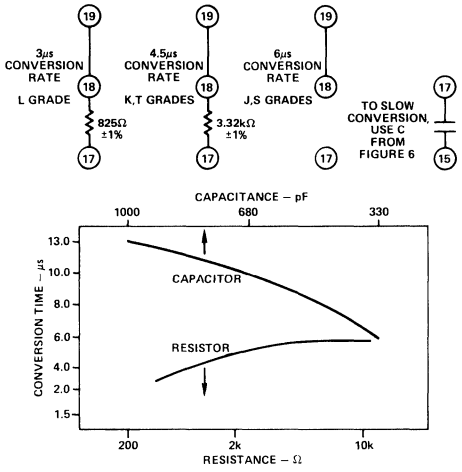


Figure 6. Conversion Times vs. R or C Values

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	3	2.5	2

Table II. Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier – In applications where the AD578 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD711 should be used.

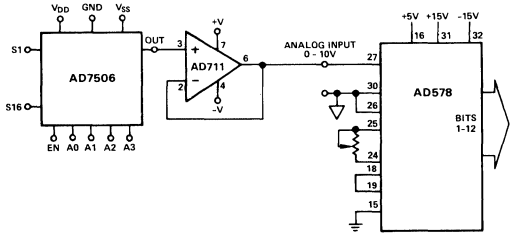


Figure 7. Input Buffer

MICROPROCESSOR INTERFACING

The 3μs conversion times of the AD578 suggests several different methods of interface to microprocessors. In systems where the AD578 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

In many multichannel data acquisition systems, the processor spends a good deal of time waiting for the ADC to complete its cycle. Converters with total conversion times of 25μs to 100μs are not slow enough to justify use of interrupts, nor fast enough to finish converting during one instruction and are usually timed out with loops, or continuously polled for status. The AD578 allows the microprocessor to time out the converter with just a few dummy instructions. For example, an 8085 system running at a 5MHz clock rate will time out an AD578 by pushing a register pair onto the stack and popping the same pair back off the stack. Such a time-out routine only occupies two bytes of program memory but requires 22 clock cyles (4.4μs). The time saved by not having to wait for the converter allows the processor to run much more efficiently particularly in multichannel systems.

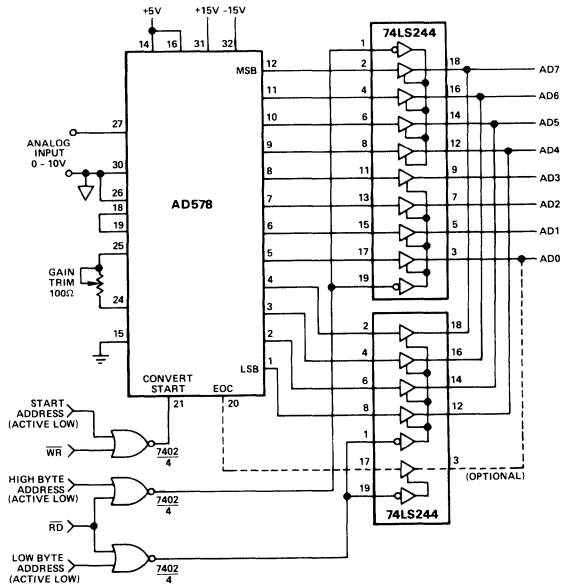


Figure 8. AD578–8085A Interface Connections

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSBs reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSBs in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 8 shows a typical connection to an 8085-type bus, using left-justified data format for unipolar inputs. Status polling is

optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD578 should be reversed, as well as the connections to the data bus and high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields an offset binary-coded output. If two's complement coding is desired, it can be produced by substituting $\overline{MSB}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

SAMPLED DATA SYSTEMS

The conversion speed of the AD578 allows accurate digitization of high frequency signals and high throughput rates in multi-channel data acquisition systems. The AD578LD, for example, is capable of a full accuracy conversion in 3μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 4μs. This means a sample rate of 250kHz can be realized, allowing a signal with no frequency components above 125kHz to be sampled with no loss of information. Note that the EOC signal from the AD578 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.

AD578 ORDERING GUIDE*

	Conversion Speed	Temperature Range	Package Option[1]
AD578JN(JD)	6.0μs	0 to +70°C	Solder Seal (DH-32B)
AD578KN(KD)	4.5μs	0 to +70°C	Solder Seal (DH-32B)
AD578LN(LD)	3.0μs	0 to +70°C	Solder Seal (DH-32B)
AD578SD	6.0μs	−55°C to +125°C	Solder Seal (DH-32B)
AD578SD/883B	6.0μs	−55°C to +125°C	Solder Seal (DH-32B)
AD578TD/883B	4.5μs	−55°C to +125°C	Solder Seal (DH-32B)

*For ±12V operation "Z" version order: AD578ZJN, . . .

[1] See Section 14 for package outline information.

ANALOG DEVICES

Very Fast, Complete 10-Bit A/D Converter

AD579

FEATURES

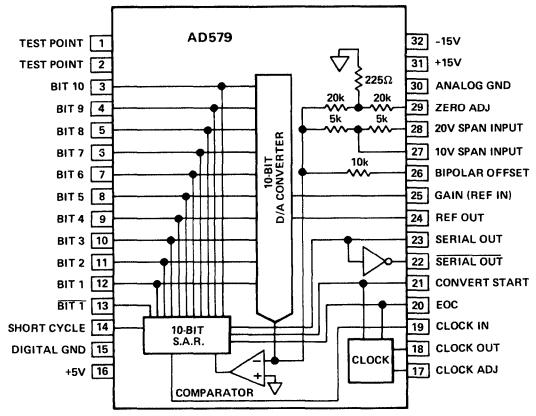
Performance

- Complete 10-Bit A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion: 1.8μs
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±40ppm/°C max
- Max Nonlinearity: <±0.048%
- Low Power: 775mW
- MIL-STD-883B Processing Available

Versatility

- Positive-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +10V Reference for External Applications
- Adjustable Internal Clock
- "Z" Models for ±12V Supplies

AD579 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT DESCRIPTION

The AD579 is a high speed low cost 10-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 10-bit monolithic DAC to provide superior performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD579 include a maximum linearity error at +25°C of ±0.048%, maximum gain temperature coefficient of ±40ppm/°C, typical power dissipation of 775mW and maximum conversion time of 1.8μs.

The fast conversion speeds of 1.8μs (K and T grades) and 2.2μs (J grade) make the AD579 an excellent choice in a variety of applications where system throughput rates from 454kHz to 555kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD579 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD579 is available with solder-seal (D) for harsh or rigorous surroundings and is contained in a 32-pin side-brazed, ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD579 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD579 makes it an excellent choice for high speed data acquisition on systems requiring high throughput rate.
3. The internal buried Zener reference is laser trimmed to 10.00V ±0.1% and ±15ppm/°C typ T.C. The reference is available externally and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
6. The integrated package construction provides high quality and reliability with small size and weight.

AD579 ORDERING GUIDE

Model	Conversion Speed	Package	Temperature Range	Power Supply Range	Package Outline*
AD579JN	2.2μs	Hermetic-Seal	0 to +70°C	±15V ±10%	DH-32B
AD579KN	1.8μs	Hermetic-Seal	0 to +70°C	±15V ±10%	DH-32B
AD579TD	1.8μs	Hermetic-Seal	-55°C to +125°C	±15V ±10%	DH-32B
AD579ZJN	2.2μs	Hermetic-Seal	0 to +70°C	±12V ±5%	DH-32B
AD579ZKN	1.8μs	Hermetic-Seal	0 to +70°C	±12V ±5%	DH-32B
AD579ZTD	1.8μs	Hermetic-Seal	-55°C to +125°C	±12V ±5%	DH-32B
AD579TD/883B	1.8μs	Hermetic-Seal	-55°C to +125°C	±15V ±10%	DH-32B
AD579ZTD/883B	1.8μs	Hermetic-Seal	-55°C to +125°C	±12V ±5%	DH-32B

*See Section 14 for package outline information.

SPECIFICATIONS (typical @ +25°C; ±15V and +5V power supplies unless otherwise noted)

Model	AD579JN	AD579KN	AD579TD
RESOLUTION	10 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0V, ±10V	*	*
Unipolar	0 to +10V, 0 to +20V	*	*
Input Impedance			
0 to +10V, ±5V	5kΩ (±20%)	*	*
±10V, 0 to +20V	10kΩ (±20%)	*	*
DIGITAL INPUTS			
Convert Command[1]	1LS TTL Load	*	*
Clock Input	1LS TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error[2,3]	±0.1% FSR (±0.25% FSR max)	*	*
Unipolar Offset[3]	±0.1% FSR (±0.25% FSR max)	*	*
Bipolar Offset[3,4]	±0.1% FSR (±0.25% FSR max)	*	*
Linearity Error			
+25°C	±1/2LSB max	*	*
T_{min} to T_{max}	±3/4LSB max	*	*
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	10 Bits	*	*
POWER SUPPLY SENSITIVITY			
+15V ±10%	0.005%/%ΔV_S max	*	*
-15V ±10%	0.005%/%ΔV_S max	*	*
+5V ±10%	0.001%/%ΔV_S max	*	*
"Z" Versions			
+12V ±5%	0.007%/%ΔV_S max	*	*
-12V ±5%	0.007%/%ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	±25ppm/°C typ	*	*
	±40ppm/°C max	*	*
Unipolar Offset	±5ppm/°C typ	*	*
	±15ppm/°C max	*	*
Bipolar Offset	±8ppm/°C typ	*	*
	±20ppm/°C max	*	*
Differential Linearity	±2ppm/°C typ	*	*
CONVERSION TIME[5,6] (max)	2.2μs	1.8μs	**
Conversion Time T_{min} to T_{max}	2.4μs	2.0μs	**
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2LSTTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive	2LSTTL Loads	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*
Output Drive	8LSTTL Loads	*	*
INTERNAL CLOCK[7]			
Output Drive	2LSTTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 ±10mV typ	*	*
Temperature Coefficient	15ppm/°C	*	*
External Current	±1mA max	*	*
POWER SUPPLY REQUIREMENTS			
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*
Supply Current +15V	3mA typ, 8mA max	*	*
-15V	22mA typ, 35mA max	*	*
+5V	100mA typ, 150mA max	*	*
Power Dissipation	775mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	-55°C to +125°C
Storage	-55°C to +150°C	*	*

NOTES

[1] Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

[2] With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.

[3] Adjustable to zero.

[4] With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).

[5] Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.

[6] Each grade is specified at the conversion speed shown. See Figure 7 for appropriate connections.

[7] Externally adjustable by a resistor or capacitor.

[8] For "Z" models order AD579ZJN, AD579ZKN or AD579ZTD.

*Specifications same as AD579JN.

**Specifications same as AD579KN.

Specifications subject to change without notice.

THEORY OF OPERATION

The AD579 is a complete 10-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD579 is shown in Figure 1.

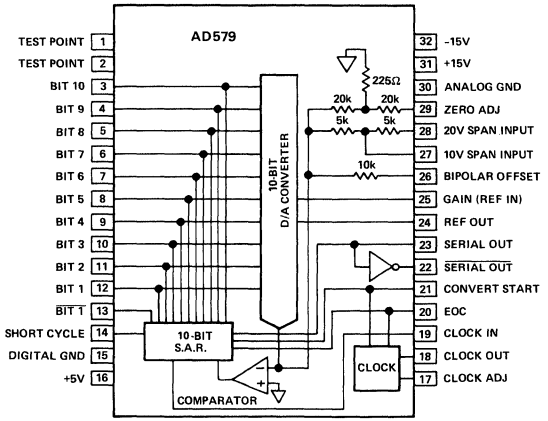


Figure 1. AD579 Functional Diagram and Pinout

On receipt of a CONVERT START command, the AD579 converts the voltage at its analog input into an equivalent bit binary number. This conversion is accomplished as follows: the 10-bit successive-approximation register (SAR) has its 10-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±0.1%; it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 10 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{10} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until Bit 10 (LSB) decision (keep) is made at t_{10}. After a 15ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to Logic "0" state.

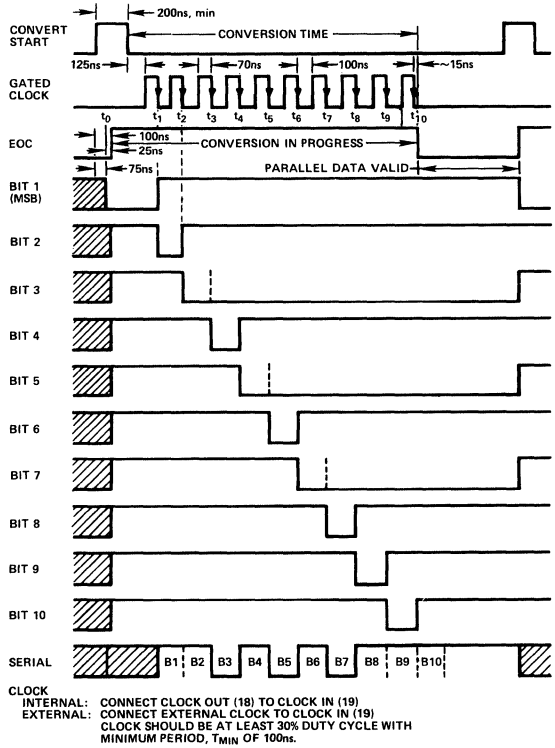


Figure 2. AD579 Timing Diagram

Serial data does not change and is guaranteed valid on negative-going clock edges, therefore; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 2).

Incorporation of this 15ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

UNIPOLAR CALIBRATION

The AD579 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 00 to 0000 0000 01) will occur for an input level of +1/2LSB (4.88mV for 10V range).

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table I and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±50mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.985V for a 10V range). Trim R2 to give the last transition (1111 1111 10 to 1111 1111 11).

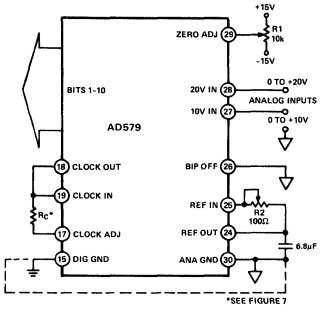


Figure 3. Unipolar Input Connections

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (-4.9957V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 00 to 0000 0000 01). Then, a signel 1 1/2LSB below positive full scale (+4.9853V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 10 to 1111 1111 11).

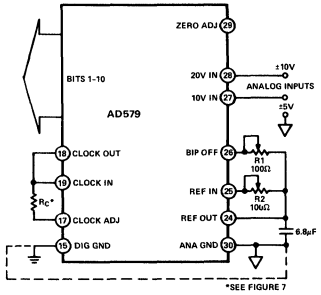


Figure 4. Bipolar Input Connections

ERROR SOURCES

The analog continuum is partitioned into 2^{10} discrete ranges for 10-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection.

The matching and tracking errors in the AD579 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR typical. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 3 and 4. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 5).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can having missing codes; the AD579TD is specified as having no missing codes from -55°C to +125°C and thus is monotonic.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	-5V to +5V Range	-10V to +10V Range	B1 (MSB) B10 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1 1 1 1 1 1 1 1 1 1
+9.9804	+19.9609	+4.9804	+9.9609	1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0097	+10.0195	+0.0097	+0.0195	1 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0097	+0.0195	-4.9902	-9.9804	0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	-5.0000	-10.0000	0 0 0 0 0 0 0 0 0 0

Table I. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

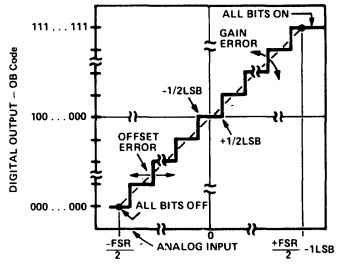


Figure 5. Transfer Characteristic for an Ideal Bipolar A/D

LAYOUT CONSIDERATIONS

Many data acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD579. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD579's supply terminals should be capacitively decoupled as close to the AD579 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

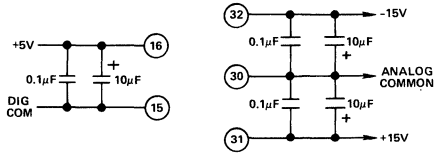


Figure 6. Basic Grounding Practice

To minimize noise the reference output (Pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 4.8μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

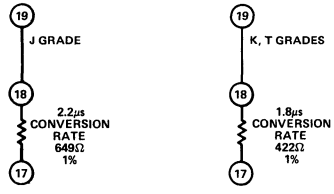


Figure 7. Clock Rate Control Connection

Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 10-bit resolution. Short cycle pin connections and associated maximum 10- and 8-bit conversion times are summarized in Table II.

Resolution (Bits)	10	8
Connect Pin 14 to Pin	2	4
Conversion Speed (μs)	1.8	1.5

Table II. Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle.

External Buffer Amplifier – In applications where the AD579 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD841 should be used.

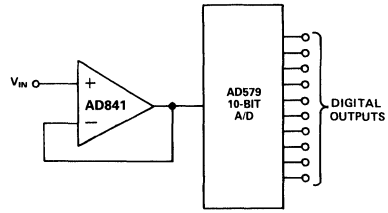


Figure 8. Input Buffer

SAMPLED DATA SYSTEMS

The conversion speed of the AD579 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD579TD, for example, is capable of a full accuracy conversion in 1.8μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 2.5μs. This means a sample rate of 400kHz can be realized, allowing a signal with no frequency components above 200kHz to be sampled with no loss of information. Note that the EOC signal from the AD579 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.

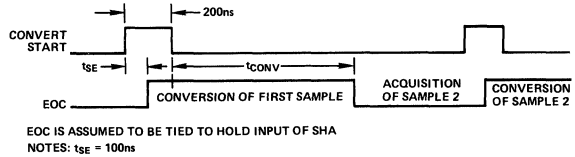


Figure 9. Start/EOC Timing for Sampled Data System

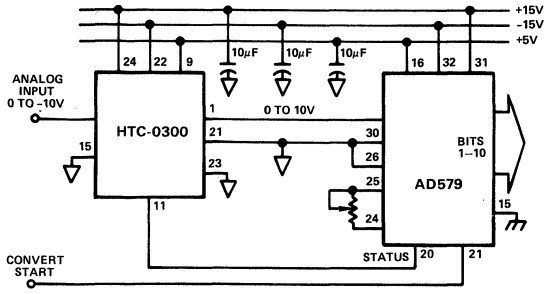


Figure 10. 400kHz – 10-Bit, A/D Conversion System

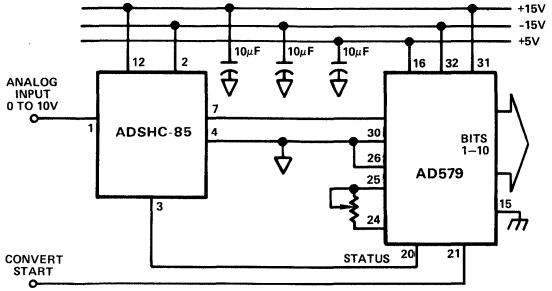


Figure 11. 154kHz – 10-Bit, A/D Conversion System

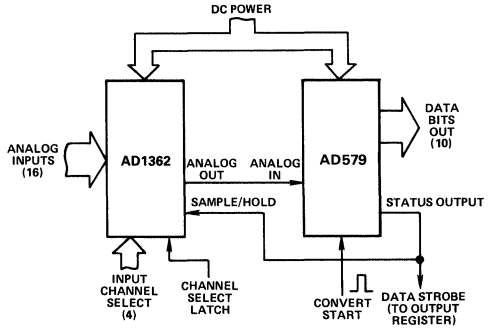


Figure 12. High Speed 10-Bit DAS

A fast (85kHz) 10-bit DAS can be configured using the AD1362 and the AD579. The AD1362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD1362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

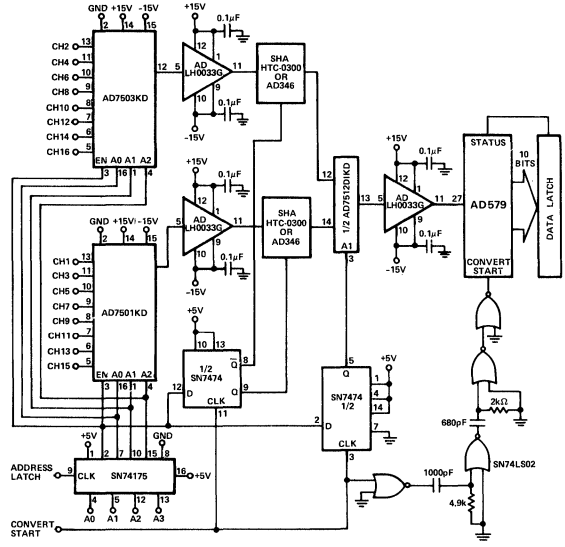


Figure 13. High Speed–165kHz–10-Bit DAS

A high speed 10-bit DAS with a throughput rate of 165kHz can be built around an AD579. The DAS of Figure 13 "Ping Pongs" two sample and hold amplifiers to eliminate the effects of the acquisition time of the sample and hold amplifiers. By applying sequential channel address the A0 of the address enables one of the two multiplexers. The incorporation of the flip-flops on the SHA mode controls and the switch address allows a new channel address to be latched in while a conversion is in progress.

ANALOG DEVICES

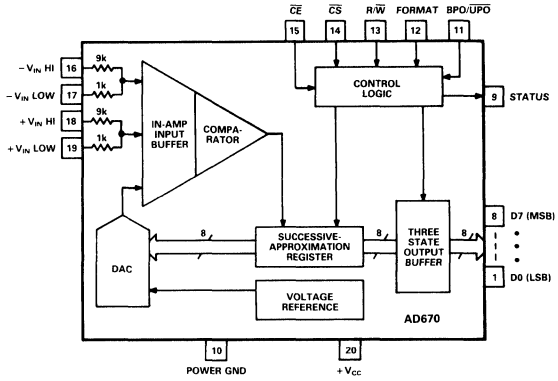
Low Cost Signal Conditioning 8-Bit ADC

AD670

FEATURES

Complete 8-Bit Signal Conditioning A/D Converter Including Instrumentation Amp and Reference
Microprocessor Bus Interface
10μs Conversion Speed
Flexible Input Stage: Instrumentation Amp Front End Provides Differential Inputs and High Common-Mode Rejection
No User Trims Required
No Missing Codes Over Temperature
Single +5V Supply Operation
Convenient Input Ranges
20-Pin DIP or Surface-Mount Package
Low Cost Monolithic Construction

AD670 BLOCK DIAGRAM AND TERMINAL CONFIGURATION (ALL PACKAGES)



GENERAL DESCRIPTION

The AD670 is a complete 8-bit signal conditioning analog-to-digital converter. It consists of an instrumentation amplifier front end along with a DAC, comparator, successive approximation register (SAR), precision voltage reference, and a three-state output buffer on a single monolithic chip. No external components or user trims are required to interface, with full accuracy, an analog system to an 8-bit data bus. The AD670 will operate on the +5V system supply. The input stage provides differential inputs with excellent common-mode rejection and allows direct interface to a variety of transducers.

The device is configured with input scaling resistors to permit two input ranges: 0 to 255mV (1mV/LSB) and 0 to 2.55V (10mV/LSB). The AD670 can be configured for both unipolar and bipolar inputs over these ranges. The differential inputs and common-mode rejection of this front end are useful in applications such as conversion of transducer signals superimposed on common-mode voltages.

The AD670 incorporates advanced circuit design and proven processing technology. The successive approximation function is implemented with I^2L (integrated injection logic). Thin-film SiCr resistors provide the stability required to prevent missing codes over the entire operating temperature range while laser wafer trimming of the resistor ladder permits calibration of the device to within ±1LSB. Thus, no user trims for gain or offset are required. Conversion time of the device is 10μs.

The AD670 is available in four package types and five grades. The J and K grades are specified over 0 to +70°C and come in 20-pin plastic DIP packages or 20-terminal PLCC packages. The A and B grades (−40°C to +85°C) and the S grade (−55°C to +125°C) come in 20-pin ceramic DIP packages.

The S grade is also available with optional processing to MIL-STD-883 in 20-pin ceramic DIP or 20-terminal LCC packages. The Analog Devices Military Products Databook should be consulted for details on these configurations.

PRODUCT HIGHLIGHTS

1. The AD670 is a complete 8-bit A/D including three-state outputs and microprocessor control for direct connection to 8-bit data buses. No external components are required to perform a conversion.
2. The flexible input stage features a differential instrumentation amp input with excellent common-mode rejection. This allows direct interface to a variety of transducers without preamplification.
3. No user trims are required for 8-bit accurate performance.
4. Operation from a single +5V supply allows the AD670 to run off of the microprocessor's supply.
5. Four convenient input ranges (two unipolar and two bipolar) are available through internal scaling resistors: 0 to 255mV (1mV/LSB) and 0 to 2.55V (10mV/LSB).
6. Software control of the output mode is provided. The user can easily select unipolar or bipolar inputs and binary or 2's complement output codes.

SPECIFICATIONS (@ V_{CC} = +5V and +25°C unless otherwise noted)

Model	AD670J			AD670K			Units
	Min	Typ	Max	Min	Typ	Max	
OPERATING TEMPERATURE RANGE	0		+70	0		+70	°C
RESOLUTION	8			8			Bit
CONVERSION TIME			10			10	μs
RELATIVE ACCURACY			±1/2			±1/4	LSB
T_{min} to T_{max}			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR							
T_{min} to T_{max}			GUARANTEED NO MISSING CODES ALL GRADES				
GAIN ACCURACY							
@ +25°C			±1.5			±0.75	LSB
T_{min} to T_{max}			±2.0			±1.0	LSB
UNIPOLAR ZERO ERROR							
@ +25°C			±1.5			±0.75	LSB
T_{min} to T_{max}			±2.0			±1.0	LSB
BIPOLAR ZERO ERROR							
@ +25°C			±1.5			±0.75	LSB
T_{min} to T_{max}			±2.0			±1.0	LSB
ANALOG INPUT RANGES							
DIFFERENTIAL ($-V_{IN}$ to $+V_{IN}$)							
Low Range		0 to +255			0 to +255		mV
		−128 to +127			−128 to +127		mV
High Range		0 to +2.55			0 to +2.55		V
		−1.28 to +1.27			−1.28 to +1.27		V
ABSOLUTE (Inputs to Power Gnd)							
Low Range T_{min} to T_{max}	−0.150		V_{CC} −3.4	−0.150		V_{CC} −3.4	V
High Range T_{min} to T_{max}	−1.50		V_{CC}	−1.50		V_{CC}	V
BIAS CURRENT (255mV RANGE)							
T_{min} to T_{max}		200	500		200	500	nA
OFFSET CURRENT (255mV RANGE)							
T_{min} to T_{max}		40	200		40	200	nA
2.55V RANGE INPUT RESISTANCE	8.0		12.0	8.0		12.0	kΩ
2.55V RANGE FULL SCALE MATCH							
+ AND − INPUT		±1/2			±1/2		LSB
COMMON-MODE REJECTION							
RATIO (255mV RANGE)			1			1	LSB
COMMON-MODE REJECTION							
RATIO (2.55V RANGE)			1			1	LSB
POWER SUPPLY							
Operating Range	4.5		5.5	4.5		5.5	V
Current I_{CC}		30	45		30	45	mA
Rejection Ratio T_{min} to T_{max}			0.015			0.015	% of FS/%
DIGITAL OUTPUTS							
SINK CURRENT (V_{OUT} = 0.4V)							
T_{min} to T_{max}	1.6			1.6			mA
SOURCE CURRENT (V_{OUT} = 2.4V)							
T_{min} to T_{max}	0.5			0.5			mA
THREE-STATE LEAKAGE CURRENT			±40			±40	μA
OUTPUT CAPACITANCE		5			5		pF
DIGITAL INPUT VOLTAGE							
V_{INL}			0.8			0.8	V
V_{INH}	2.0			2.0			V
DIGITAL INPUT CURRENT							
($0 \le V_{IN} \le +5V$)							
I_{INL}	−100			−100			μA
I_{INH}			+100			+100	μA
INPUT CAPACITANCE		10			10		pF

NOTES

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

Model	AD670A			AD670B			AD670S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPERATING TEMPERATURE RANGE	−40		+85	−40		+85	−55		+125	°C
RESOLUTION	8			8			8			Bit
CONVERSION TIME			10			10			10	μs
RELATIVE ACCURACY			±1/2			±1/4			±1/2	LSB
T_{min} to T_{max}			±1/2			±1/2			±1	LSB
DIFFERENTIAL LINEARITY ERROR										
T_{min} to T_{max}	GUARANTEED NO MISSING CODES ALL GRADES									
GAIN ACCURACY										
@ +25°C			±1.5			±0.75			±1.5	LSB
T_{min} to T_{max}			±2.5			±1.5			±2.5	LSB
UNIPOLAR ZERO ERROR										
@ +25°C			±1.0			±0.5			±1.0	LSB
T_{min} to T_{max}			±2.0			±1.0			±2.0	LSB
BIPOLAR ZERO ERROR										
@ +25°C			±1.0			±0.5			±1.0	LSB
T_{min} to T_{max}			±2.0			±1.0			±2.0	LSB
ANALOG INPUT RANGES										
DIFFERENTIAL ($-V_{IN}$ to $+V_{IN}$)										
Low Range		0 to +255			0 to +255			0 to +255		mV
		−128 to +127			−128 to +127			−128 to +127		mV
High Range		0 to +2.55			0 to +2.55			0 to +2.55		V
		−1.28 to +1.27			−1.28 to +1.27			−1.28 to +1.27		V
ABSOLUTE (Inputs to Power Gnd)										
Low Range T_{min} to T_{max}	−0.150		V_{CC} −3.5	−0.150		V_{CC} −3.5	−0.150		V_{CC} −3.5	V
High Range T_{min} to T_{max}	−1.50		V_{CC}	−1.50		V_{CC}	−1.50		V_{CC}	V
BIAS CURRENT (255mV RANGE)										
T_{min} to T_{max}		200	500		200	500		200	750	nA
OFFSET CURRENT (255mV RANGE)										
T_{min} to T_{max}		40	200		40	200		40	200	nA
2.55V RANGE INPUT RESISTANCE	8.0		12.0	8.0		12.0	8.0		12.0	kΩ
2.55V RANGE FULL SCALE MATCH										
+ AND − INPUT		±1/2			±1/2			±1/2		LSB
COMMON-MODE REJECTION										
RATIO (255mV RANGE)			1			1			1	LSB
COMMON-MODE REJECTION										
RATIO (2.55V RANGE)			1			1			1	LSB
POWER SUPPLY										
Operating Range	4.5		5.5	4.5		5.5	4.75		5.5	V
Current I_{CC}		30	45		30	45		30	45	mA
Rejection Ratio T_{min} to T_{max}			0.015			0.015			0.015	% of FS/
DIGITAL OUTPUTS										
SINK CURRENT (V_{OUT} = 0.4V)										
T_{min} to T_{max}	1.6			1.6			1.6			mA
SOURCE CURRENT (V_{OUT} = 2.4V)										
T_{min} to T_{max}	0.5			0.5			0.5			mA
THREE-STATE LEAKAGE CURRENT			±40			±40			±40	μA
OUTPUT CAPACITANCE		5			5			5		pF
DIGITAL INPUT VOLTAGE										
V_{INL}			0.8			0.8			0.7	V
V_{INH}	2.0			2.0			2.0			V
DIGITAL INPUT CURRENT										
($0 \le V_{IN} \le +5V$)										
I_{INL}	−100			−100			−100			μA
I_{INH}			+100			+100			+100	μA
INPUT CAPACITANCE		10			10			10		pF

NOTES

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

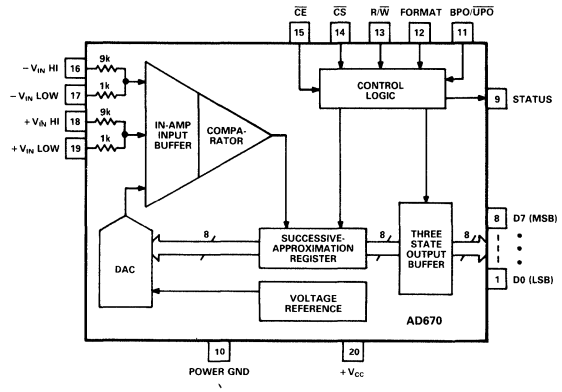


Figure 1. AD670 Block Diagram and Terminal Configuration (All Packages)

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground	0V to +7.5V
Digital Inputs (Pins 11-15)	−0.5V to V_{CC} +0.5V
Digital Outputs (Pins 1-9)	Momentary Short to V_{CC} or Ground
Analog Inputs (Pins 16-19)	−30V to +30V
Power Dissipation	450mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD670 ORDERING GUIDE

Model	Temperature Range	Relative Accuracy @ 25°C	Gain Accuracy @ 25°C	Package Options*
AD670JN	0 to +70°C	±1/2LSB	±1.5LSB	Plastic DIP (N-20)
AD670JP	0 to +70°C	±1/2LSB	±1.5LSB	PLCC (P-20A)
AD670KN	0 to +70°C	±1/4LSB	±0.75LSB	Plastic DIP (N-20)
AD670KP	0 to +70°C	±1/4LSB	±0.75LSB	PLCC (P-20A)
AD670AD	−40°C to +85°C	±1/2LSB	±1.5LSB	Ceramic DIP (D-20)
AD670BD	−40°C to +85°C	±1/4LSB	±0.75LSB	Ceramic DIP (D-20)
AD670SD	−55°C to +125°C	±1/2LSB	±1.5LSB	Ceramic DIP (D-20)

*Section 13 for package outline information.

CIRCUIT OPERATION/FUNCTIONAL DESCRIPTION

The AD670 is a functionally complete 8-bit signal conditioning A/D converter with microprocessor compatibility. The input section uses an instrumentation amplifier to accomplish the voltage to current conversion. This front end provides a high impedance, low bias current differential amplifier. The common-mode range allows the user to directly interface the device to a variety of transducers.

The A/D conversions are controlled by R/$\overline{W}$, $\overline{CS}$, and $\overline{CE}$. The R/$\overline{W}$ line directs the converter to read or start a conversion. A minimum write/start pulse of 300ns is required on either $\overline{CE}$ or $\overline{CS}$. The STATUS line goes high, indicating that a conversion is in process. The conversion thus begun, the internal 8-bit DAC is sequenced from MSB to LSB using a novel successive approximation technique. In conventional designs, the DAC is stepped through the bits by a clock. This can be thought of as a static design since the speed at which the DAC is sequenced is determined solely by the clock. No clock is used in the AD670. Instead, a "dynamic SAR" is created consisting of a string of inverters with taps along the delay line. Sections of the delay line between taps act as one shots. The pulses are used to set and reset the DAC's bits and strobe the comparator. When strobed, the comparator then determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is turned off. After all bits are tested, the SAR holds an 8-bit code representing the input signal to within 1/2LSB accuracy. Ease of implementation and reduced dependence on process related variables make this an attractive approach to a successive approximation design.

The SAR provides an end-of-conversion signal to the control logic which then brings the STATUS line low. Data outputs remain in a high impedance state until R/$\overline{W}$ is brought high with $\overline{CE}$ and $\overline{CS}$ low and allows the converter to be read. Bringing $\overline{CE}$ or $\overline{CS}$ high during the valid data period ends the read cycle. The output buffers cannot be enabled during a conversion. Any convert start commands will be ignored until the conversion cycle is completed; once a conversion cycle has been started it cannot be stopped or restarted.

The AD670 provides the user with a great deal of flexibility by offering two input spans and formats and a choice of output codes. Input format and input range can each be selected. The BPO/$\overline{UPO}$ pin controls a switch which injects a bipolar offset current of a value equal to the MSB less 1/2LSB into the summing node of the comparator to offset the DAC output. Two precision 10 to 1 attenuators are included on board to provide input range selection of 0 to 2.55V or 0 to 255mV. Additional ranges of

– 1.28 to 1.27V and – 128 to 127mV are possible if the BPO/$\overline{\text{UPO}}$ switch is high when the conversion is started. Finally, output coding can be chosen using the FORMAT pin when the conversion is started. In the bipolar mode and with a logic 1 on FORMAT, the output is in two's complement; with a logic 0, the output is offset binary.

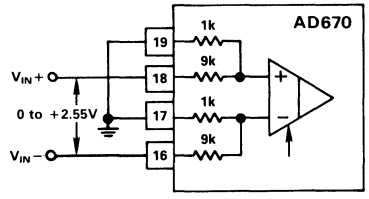
CONNECTING THE AD670

The AD670 has been designed for ease of use. All active components required to perform a complete A/D conversion are on board and are connected internally. In addition, all calibration trims are performed at the factory, assuring specified accuracy without user trims. There are, however, a number of options and connections that should be considered to obtain maximum flexibility from the part.

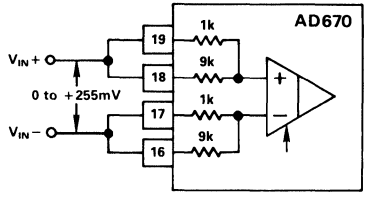
INPUT CONNECTIONS

Standard connections are shown in the figures that follow. An input range of 0 to 2.55V may be configured as shown in Figure 2a. This will provide a one LSB change for each 10mV of input change. The input range of 0 to 255mV is configured as shown in Figure 2b. In this case, each LSB represents 1mV of input change. When unipolar input signals are used, Pin 11, BPO/$\overline{\text{UPO}}$, should be grounded. Pin 11 selects the input format for either unipolar or bipolar signals. Figures 3a and 3b show the input connections for bipolar signals. Pin 11 should be tied to $+V_{CC}$ for bipolar inputs.

Although the instrumentation amplifier has a differential input, there must be a return path to ground for the bias currents. If it is not provided, these currents will charge stray capacitances and cause internal circuit nodes to drift uncontrollably causing the digital output to change. Such a return path is provided in Figures 2a and 3a (larger input ranges) since the 1k resistor leg



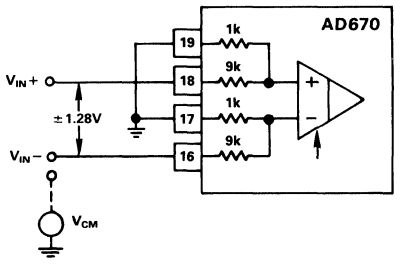
2a. 0 to 2.55V (10mV/LSB)



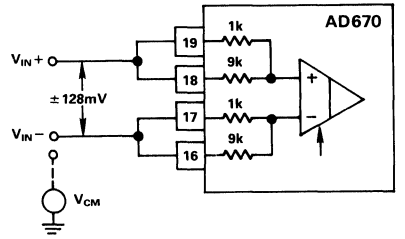
2b. 0 to 255mV (1mV/LSB)

NOTE: PIN 11, BPO/$\overline{\text{UPO}}$ SHOULD BE LOW WHEN CONVERSION IS STARTED.

Figure 2. Unipolar Input Connections



3a. ± 1.28V Range



3b. ± 128mV Range

NOTE: PIN 11, BPO/$\overline{\text{UPO}}$ SHOULD BE HIGH WHEN CONVERSION IS STARTED.

Figure 3. Bipolar Input Connections

is tied to ground. This is not the case for Figures 2b and 3b (the lower input ranges). When connecting the AD670 inputs to floating sources, such as transformers and ac-coupled sources, there must still be a dc path from each input to common. This can be accomplished by connecting a 10kΩ resistor from each input to ground.

Bipolar Operation

Through special design of the instrumentation amplifier, the AD670 accommodates input signal excursions below ground, even though it operates from a single 5V supply. To the user, this means that true bipolar input signals can be used without the need for any additional external components. Bipolar signals can be applied differentially across both inputs, or one of the inputs can be grounded and a bipolar signal applied to the other.

Common-Mode Performance

The AD670 is designed to reject dc and ac common-mode voltages. In some applications it is useful to apply a differential input signal V_{IN} in the presence of a dc common-mode voltage V_{CM}. The user must observe the absolute input signal limits listed in the specifications, which represent the maximum voltage V_{IN} + V_{CM} that can be applied to either input without affecting proper operation. Exceeding these limits (within the range of absolute maximum ratings), however, will not cause permanent damage.

The excellent common-mode rejection of the AD670 is due to the instrumentation amplifier front end, which maintains the differential signal until it reaches the output of the comparator. In contrast to a standard operational amplifier, the instrumentation amplifier front end provides significantly improved CMRR over a wide frequency range (Figure 4a).

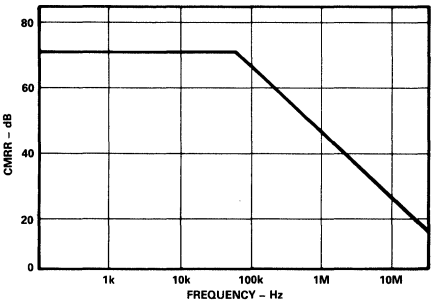


Figure 4a. CMRR over Frequency

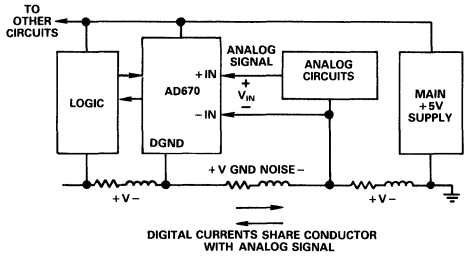


Figure 4b. AD670 Input Rejects Common-Mode Ground Noise

Good common-mode performance is useful in a number of situations. In bridge-type transducer applications, such performance facilitates the recovery of differential analog signals in the presence of a dc common-mode or a noisy electrical environment. High-frequency CMRR also becomes important when the analog signal is referred to a noisy, remote digital ground. In each case, the CMRR specification of the AD670 allows the integrity of the input signal to be preserved.

The AD670's common-mode voltage tolerance allows great flexibility in circuit layout. Most other A/D converters require the establishment of one point as the analog reference point. This is necessary in order to minimize the effects of parasitic voltages. The AD670, however, eliminates the need to make the analog ground reference point and A/D analog ground one and the same. Instead, a system such as that shown in Figure 4b is possible as a result of the AD670's common-mode performance. The resistors and inductors in the ground return represent unavoidable system parasitic impedances.

Input/Output Options

Data output coding (2's complement vs. straight binary) is selected using Pin 12, the FORMAT pin. The selection of input format (bipolar vs. unipolar) is controlled using Pin 11, BPO/$\overline{\text{UPO}}$. Prior to a write/convert, the state of FORMAT and BPO/$\overline{\text{UPO}}$ should be available to the converter. These lines may be tied to the data bus and may be changed with each conversion if desired. The configurations are shown in Table I. Output coding for representative signals in each of these configurations is shown in Figure 5.

An output signal, STATUS, indicates the status of the conversion. STATUS goes high at the beginning of the conversion and returns low when the conversion cycle has been completed.

BPO/$\overline{\text{UPO}}$	FORMAT	INPUT RANGE/OUTPUT FORMAT
0	0	Unipolar/Straight Binary
1	0	Bipolar/Offset Binary
0	1	Unipolar/2's Complement
1	1	Bipolar/2's Complement

Table I. AD670 Input Selection/Output Format Truth Table

$+V_{IN}$	$-V_{IN}$	DIFF V_{IN}	STRAIGHT BINARY (FORMAT = 0, BPO/$\overline{\text{UPO}}$ = 0)
0	0	0	0000 0000
128mV	0	128mV	1000 0000
255mV	0	255mV	1111 1111
255mV	255mV	0	0000 0000
128mV	127mV	1mV	0000 0001
128mV	–127mV	255mV	1111 1111

Figure 5a. Unipolar Output Codes (Low Range)

$+V_{IN}$	$-V_{IN}$	DIFF V_{IN}	OFFSET BINARY (FORMAT = 0, BPO/$\overline{\text{UPO}}$ = 1)	2's COMPLEMENT (FORMAT = 1, BPO/$\overline{\text{UPO}}$ = 1)
0	0	0	1000 0000	0000 0000
127mV	0	127mV	1111 1111	0111 1111
1.127V	1.000V	127mV	1111 1111	0111 1111
255mV	255mV	0	1000 0000	0000 0000
128mV	127mV	1mV	1000 0001	0000 0001
127mV	128mV	–1mV	0111 1111	1111 1111
127mV	255mV	–128mV	0000 0000	1000 0000
–128mV	0	–128mV	0000 0000	1000 0000

Figure 5b. Bipolar Output Codes (Low Range)

Calibration

Because of its precise factory calibration, the AD670 is intended to be operated without user trims for gain and offset; therefore, no provisions have been made for such user trims. Figures 6a, 6b, and 6c show the transfer curves at zero and full scale for the unipolar and bipolar modes. The code transitions are positioned so that the desired value is centered at that code. The first LSB transition for the unipolar mode occurs for an input of +1/2LSB (5mV or 0.5mV). Similarly, the MSB transition for the bipolar mode is set at –1/2LSB (–5mV or –0.5mV). The full scale transition is located at the full scale value –1 1/2LSB. These values are 2.545V and 254.5mV.

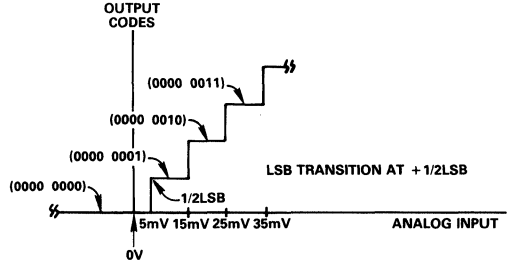


Figure 6a. Unipolar Transfer Curve

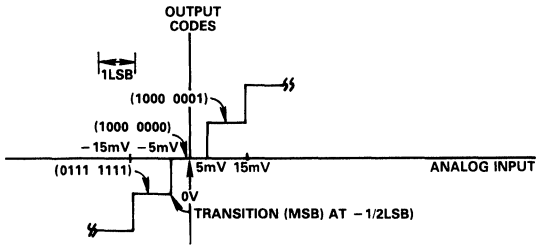


Figure 6b. Bipolar

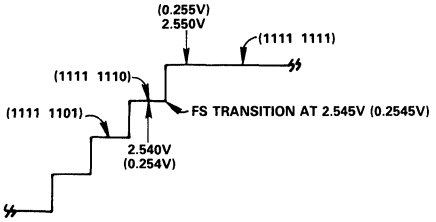


Figure 6c. Full Scale (Unipolar)

Figure 6. Transfer Curves

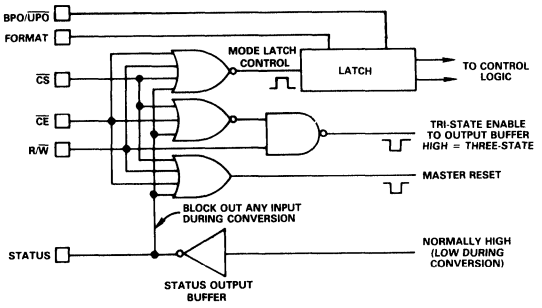


Figure 7. Control Logic Block Diagram

R/$\overline{W}$	$\overline{CS}$	$\overline{CE}$	OPERATION
0	0	0	WRITE/CONVERT
1	0	0	READ
X	X	1	NONE
X	1	X	NONE

Table II. AD670 Control Signal Truth Table

CONTROL AND TIMING OF THE AD670

Control Logic

The AD670 contains on-chip logic to provide conversion and data read operations from signals commonly available in microprocessor systems. Figure 7 shows the internal logic circuitry of the AD670. The control signals, $\overline{CE}$, $\overline{CS}$, and R/$\overline{W}$ control the operation of the converter. The read or write function is determined by R/$\overline{W}$ when both $\overline{CS}$ and $\overline{CE}$ are low as shown in Table II. If all three control inputs are held low longer than the conversion time, the device will continuously convert until one input, $\overline{CE}$, $\overline{CS}$, or R/$\overline{W}$ is brought high. The relative timing of these signals is discussed later in this section.

Timing

The AD670 is easily interfaced to a variety of microprocessors and other digital systems. The following discussion of the timing requirements of the AD670 control signals will provide the designer with useful insight into the operation of the device.

Write/Convert Start Cycle

Figure 8 shows a complete timing diagram for the write/convert start cycle. $\overline{CS}$ (chip select) and $\overline{CE}$ (chip enable) are active low and are interchangeable signals. Both $\overline{CS}$ and $\overline{CE}$ must be low for the converter to read or start a conversion. The minimum pulse width, t_W, on either $\overline{CS}$ or $\overline{CE}$ is 300ns to start a conversion.

Table III. AD670 TIMING SPECIFICATIONS

Boldface indicates parameters tested 100% unless otherwise noted. See Specifications page for explanation.

		@ +25°C			
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**
WRITE/CONVERT START MODE					
t_W	Write/Start Pulse Width	300			ns
t_{DS}	Input Data Setup Time	200			ns
t_{DH}	Input Data Hold	10			ns
t_{RWC}	Read/Write Setup Before Control	0			ns
t_{DC}	Delay to Convert Start			700	ns
t_C	**Conversion Time**			**10**	µs
READ MODE					
t_R	Read Time	250			ns
t_{SD}	Delay from Status Low to Data Read			250	ns
t_{TD}	**Bus Access Time**		200	**250**	ns
t_{DH}	Data Hold Time	25			ns
t_{DT}	**Output Float Delay**			**150**	ns
t_{RT}	R/$\overline{W}$ before $\overline{CE}$ or $\overline{CS}$ low	0			ns

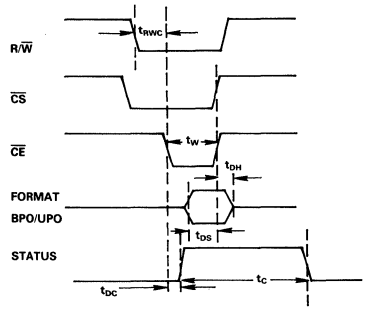


Figure 8. Write/Convert Start Timing

The R/$\overline{W}$ line is used to direct the converter to start a conversion (R/$\overline{W}$ low) or read data (R/$\overline{W}$ high). The relative sequencing of the three control signals (R/$\overline{W}$, $\overline{CE}$, $\overline{CS}$) is unimportant. However, when all three signals remain low for at least 300ns (t_W), STATUS will go high to signal that a conversion is taking place.

Once a conversion is started and the STATUS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffer cannot be enabled during a conversion.

Read Cycle

Figure 9 shows the timing for the data read operation. The data outputs are in a high impedance state until a read cycle is initiated. To begin the read cycle, R/$\overline{W}$ is brought high. During a read cycle, the minimum pulse length for $\overline{CE}$ and $\overline{CS}$ is a function of the length of time required for the output data to be valid. The data becomes valid and is available to the data bus in a maximum of 250ns. This delay between the high impedance state and valid data is the maximum bus access time or t_{TD}. Bringing $\overline{CE}$ or $\overline{CS}$ high during valid data ends the read cycle. The outputs remain valid for a minimum of 25ns (t_{DH}) and return to the high impedance state after a delay, t_{DT}, of 150ns maximum.

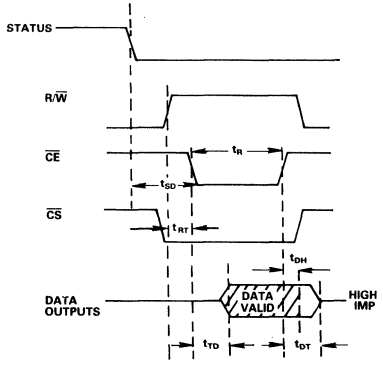


Figure 9. Read Cycle Timing

STAND-ALONE OPERATION

The AD670 can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available. Two typical conditions are described and illustrated by the timing diagrams which follow.

Single Conversion, Single Read

When the AD670 is used in a stand-alone mode, $\overline{CS}$ and $\overline{CE}$ should be tied together. Conversion will be initiated by bringing R/$\overline{W}$ low. Within 700ns, a conversion will begin. The R/$\overline{W}$ pulse should be brought high again once the conversion has started so that the data will be valid upon completion of the conversion. Data will remain valid until $\overline{CE}$ and $\overline{CS}$ are brought high to indicate the end of the read cycle or R/$\overline{W}$goes low. The timing diagram is shown in Figure 10.

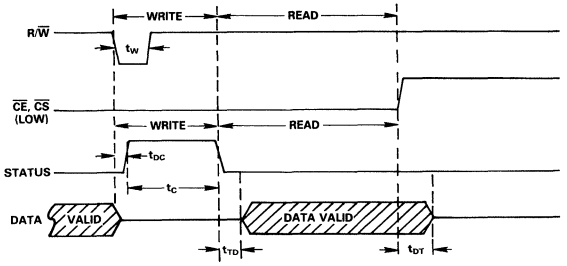


Figure 10. Stand-Alone Mode Single Conversion/ Single Read

Continuous Conversion, Single Read

A variety of applications may call for the A/D to be read after several conversions. In process control systems, this is often the case since a reading from a sensor may only need to be updated every few conversions. Figure 11 shows the timing relationships.

Once again, $\overline{CE}$ and $\overline{CS}$ should be tied together. Conversion will begin when the R/$\overline{W}$ signal is brought low. The device will convert repeatedly as indicated by the status line. A final conversion will take place once the R/$\overline{W}$ line has been brought high. The rising edge of R/$\overline{W}$ must occur while STATUS is high. R/$\overline{W}$ should not return high while STATUS is low since the circuit is in a reset state prior to the next conversion. Since the rising edge of R/$\overline{W}$ must occur while STATUS is high, R/$\overline{W}$'s length must be a minimum of 10.25μs (t_C + t_{TD}). Data becomes valid upon completion of the conversion and will remain so until the $\overline{CE}$ and $\overline{CS}$ lines are brought high indicating the end of the read cycle or R/$\overline{W}$ goes low initiating a new series of conversions.

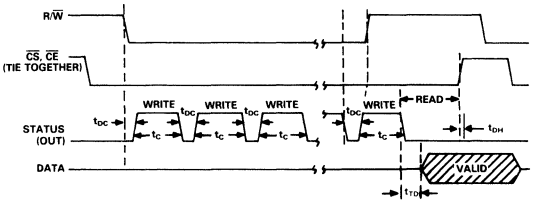


Figure 11. Stand-Alone Mode Continuous Conversion/ Single Read

APPLYING THE AD670

The AD670 has been designed for ease of use, system compatibility, and minimization of external components. Transducer interfaces generally require signal conditioning and preamplification before the signal can be converted. The AD670 will reduce and even eliminate this excess circuitry in many cases. To illustrate the flexibility and superior solution that the AD670 can bring to a transducer interface problem, the following discussions are offered.

Temperature Measurements

Temperature transducers are one of the most common sources of analog signals in data acquisition systems. These sensors require circuitry for excitation and preamplification/buffering. The instrumentation amplifier input of the AD670 eliminates the need for this signal conditioning. The output signals from temperature transducers are generally sufficiently slow that a sample/hold amplifier is not required. Figure 12 shows the AD590 IC temperature transducer interfaced to the AD670. The AD580 voltage reference is used to offset the input for 0°C calibration. The current output of the AD590 is converted into a voltage by R1. The high impedance unbuffered voltage is applied directly to the AD670 configured in the −128mV to 127mV bipolar range. The digital output will have a resolution of 1°C.

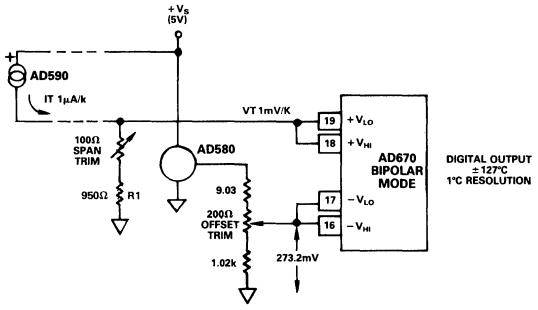


Figure 12. AD670 Temperature Transducer Interface

Platinum RTDs are also a popular, temperature transducer. Typical RTDs have a resistance of 100Ω at 0°C and change resistance 0.4Ω per °C. If a constant excitation current is caused to flow in the RTD, the change in voltage drop will be a measure of the change in temperature. Figure 13 shows such a method and the required connections to the AD670. The AD580 2.5V reference provides the accurate voltage for the excitation current and range offsetting for the RTD. The op-amp is configured to force a constant 2.5mA current through the RTD. The differential inputs of the AD670 measure the difference between a fixed offset voltage and the temperature dependent output of the op-amp which varies with the resistance of the RTD. The RTD change of approximately 0.4Ω/°C results in a 1mV/°C voltage change. With the AD670 in the 1mV/LSB range, temperatures from 0 to 255°C can be measured.

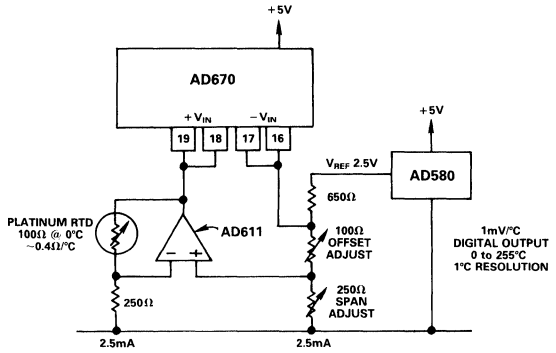


Figure 13. Low Cost RTD Interface

Differential temperature measurements can be made using an AD590 connected to each of the inputs as shown in Figure 14. This configuration will allow the user to measure the relative temperature difference between two points with a 1°C resolution. Although the internal 1k and 9k resistors on the inputs have ±20% tolerance, trimming the AD590 is unnecessary as most differential temperature applications are concerned with the relative differences between the two. However, the user may see up to a 20% scale factor error in the differential temperature to digital output transfer curve.

This scale factor error can be eliminated through a software correction. Offset corrections can be made by adjusting for any difference that results when both sensors are held at the same temperature. A span adjustment can then be made by immersing one AD590 in an ice bath and one in boiling water and eliminating any deviation from 100°C. For a low cost version of this setup, the plastic AD592 can be substituted for the AD590.

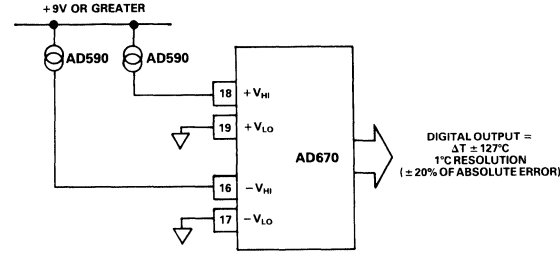


Figure 14. Differential Temperature Measurement Using the AD590

STRAIN GAUGE MEASUREMENTS

Many semiconductor-type strain gauges, pressure transducers, and load cells may also be connected directly to the AD670. These types of transducers typically produce 30 millivolts full-scale per volt of excitation. In the circuit shown in Figure 15, the AD670 is connected directly to a Data Instruments model JP-20 load cell. The AD584 programmable voltage reference is used along with an AD741 op-amp to provide the ±2.5V excitation for the load cell. The output of the transducer will be ±150mV for a force of ±20 pounds. The AD670 is configured for the ±128 millivolt range. The resolution is then approximately 2.1 ounces per LSB over a range of ±17 pounds. Scaling to exactly 2 ounces per LSB can be accomplished by trimming the reference voltage which excites the load cell.

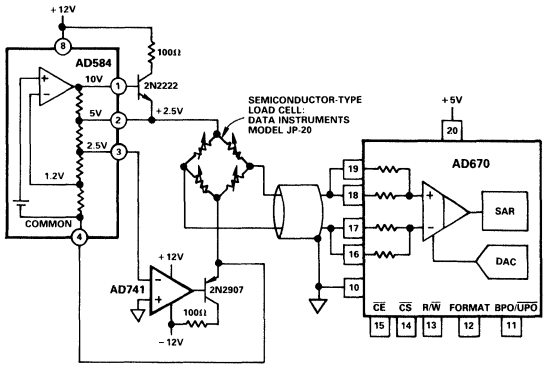


Figure 15. AD670 Load Cell Interface

MULTIPLEXED INPUTS

Most data acquisition systems require the measurement of several analog signals. Multiple A/D converters are often used to digitize these inputs, requiring additional preamplification and buffer stages per channel. Since these signals vary slowly, a differential MUX can multiplex inputs from several transducers into a single AD670. And since the AD670's signal-conditioning capability is preserved, the cost of several ADCs, differential amplifiers, and other support components can be reduced to that of a single AD670, a MUX, and a few digital logic gates.

An AD7502 dual 4-channel MUX appears in Figure 16 multiplexing four differential signals to the AD670. The AD7502's decoded address is gated with the microprocessor's write signal to provice a latching strobe at the flip-flops. A write cycle to the AD7502's address then latches the two LSBs of the data word thereby selecting the input channel for subsequent conversions.

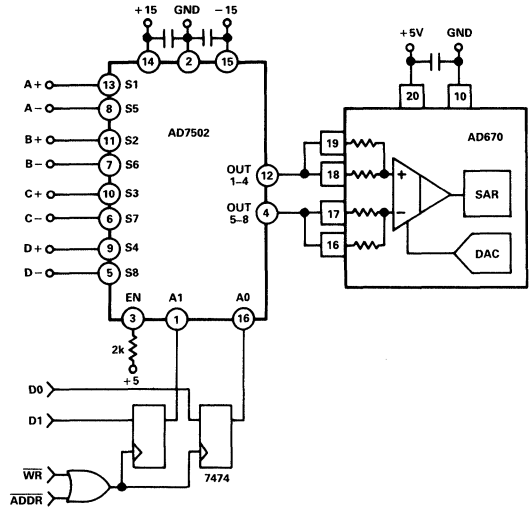


Figure 16. Multiplexed Analog Inputs to AD670

SAMPLED INPUTS

For those applications where the input signal is capable of slewing more than 1/2LSB during the AD670's 10μs conversion cycle, the input should be held constant for the cycle's duration. The circuit shown in Figure 17 uses a CMOS switch and two capacitors to sample/hold the input. The AD670's STATUS output, once inverted, supplies the sample/hold ($S/\overline{H}$) signal.

A convert command applied on the $\overline{CE}$, $\overline{CS}$ OR $R/\overline{W}$ lines will initiate the conversion. The AD670's STATUS output, once inverted, supplies the sample/hold signal to the CD4066. The CD4066 CMOS switch shown in Figure 17 was chosen for its fast transition times, low on-resistance and low cost. The control input's propagation delay for switch-closed to switch-open should remain less than 150ns to ensure that the sample-to-hold transition occurs before the first bit decision in the AD670.

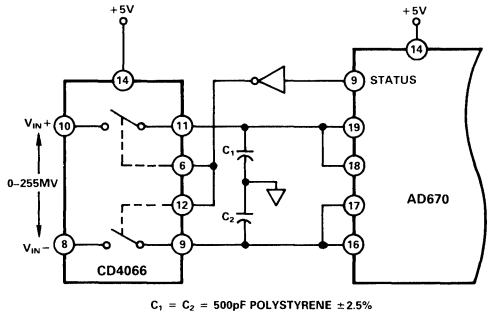


Figure 17. Low Cost Sample-and-Hold Circuit for AD670

Since settling to 1/2LSB at 8-bits of resolution requires 6.2 RC time constants, the 500pF hold capacitors and CD4066's 300Ω on-resistance yield an acquisition time of under 1μs, assuming a low impedance source.

This sample/hold approach makes use of the differential capabilities of the AD670. Because 500pF hold capacitors are used on both $V_{IN}+$ and $V_{IN}-$ inputs, the droop rate depends only on the offset current of the AD670, typically 20nA. With the matched 500pF capacitors, the droop rate is 40μV/μs. The input will then droop only 0.4mV (0.4LSB) during the AD670's 10μs conversion time. The differential approach also minimizes pedestal error since only the difference in charge injection between the two switches results in errors at the A/D.

The fast conversion time and differential and common-mode capabilities of the AD670 permit this simple sample-hold design to perform well with low sample-to-hold offset, droop rate of about 40μV/μs and acquisition time under 1μs. The effective aperture time of the AD670 is reduced by about 2 orders of magnitude with this circuit, allowing frequencies to be converted up to several kilohertz.

While no input anti-aliasing filter is shown, filtering will be necessary to prevent output errors if higher frequencies are present in the input signal. Many practical variations are possible with this circuit, including input MUX control, for digitizing a number of AC channels.

IBM PC INTERFACE

The AD670 appears in Figure 18 interfaced to the IBM PC. Since the device resides in I/O space, its address is decoded from only the lower ten address lines and must be gated with AEN (active low) to mask out internal (DMA) cycles which use the same I/O address space. This active low signal is applied to $\overline{CS}$. AO, meanwhile, is reserved for the R/$\overline{W}$ input. This places

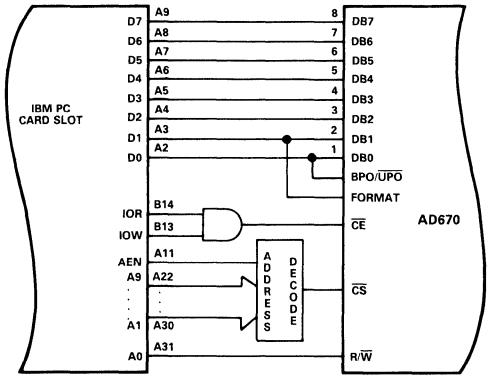


Figure 18. IBM PC Interface to AD670

the AD670 in two adjacent addresses; one for starting the conversion and the other for reading the result. The $\overline{IOR}$ and $\overline{IOW}$ signals are then gated and applied to $\overline{CE}$, while the lower two data lines are applied to FORMAT and BPO/$\overline{UPO}$ inputs to provide software programmable input formats and output coding.

In BASIC, a simple OUT ADDR, WORD command initiates a conversion. While the upper six bits of the data WORD are meaningless, the lower two bits define the analog input format and digital output coding according to Table IV. The data is available ten microseconds later (which is negligible in BASIC) and can be read using INP (ADDR + 1). The 3-line subroutine in Figure 19, used in conjunction with the interface of Figure 18, converts an analog input within a bipolar range to an offset binary coded digital word.

NOTE: Due to the large number of options that may be installed in the PC, the I/O bus loading should be limited to one Schottky TTL load. Therefore, a buffer/driver should be used when interfacing more than two AD670's to the I/O bus.

DATA	INPUT FORMAT	OUTPUT CODING
0	Unipolar	Straight Binary
1	Bipolar	Offset Binary
2	Unipolar	2's Complement
3	Bipolar	2's Complement

Table IV.

```
10 OUT &H310,1                  'INITIATE CONVERSION
20 ANALOGIN=INP (&H311)         'READ ANALOG INPUT
30 RETURN
```

Figure 19. Conversion Subroutine

ANALOG DEVICES

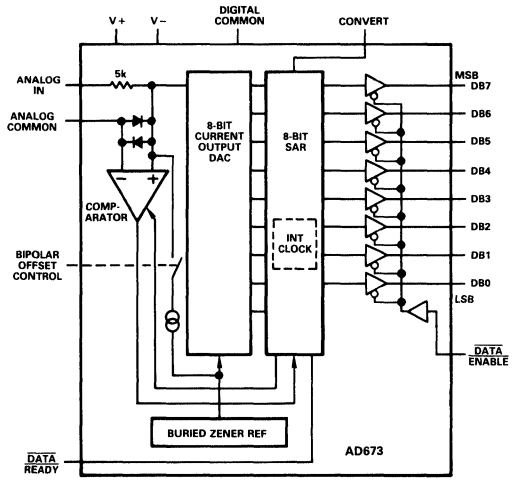
8-Bit A/D Converter

AD673*

FEATURES

Complete 8-Bit A/D Converter with Reference, Clock and Comparator
30μs Maximum Conversion Time
Full 8- or 16-Bit Microprocessor Bus Interface
Unipolar and Bipolar Inputs
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies

AD673 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD673 is a complete 8-bit successive approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 20μs.

The AD673 incorporates advanced integrated circuit design and processing technologies. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD673 will accept analog inputs of 0 to +10V or −5V to +5V. The trailing edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion.

The AD673 is available in two versions. The AD673J as specified over the 0 to +70°C temperature range and the AD673S guarantees ±½LSB relative accuracy and no missing codes from −55°C to +125°C.

Two package configurations are offered. All versions are also offered in a 20-pin hermetically sealed ceramic DIP. The AD673J is also available in a 20-pin plastic DIP.

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690**

PRODUCT HIGHLIGHTS

1. The AD673 is a complete 8-bit A/D converter. No external components are required to perform a conversion.
2. The AD673 interfaces to many popular microprocessors without external buffers or peripheral interface adapters.
3. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD673 adapts to either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.

SPECIFICATIONS (T_A=25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD673J Min	AD673J Typ	AD673J Max	AD673S Min	AD673S Typ	AD673S Max	Units
RESOLUTION		8			8		Bits
RELATIVE ACCURACY,[1]			±1/2			±1/2	LSB
$T_A = T_{min}$ to T_{max}			±1/2			±1/2	LSB
FULL SCALE CALIBRATION[2]		±2			±2		LSB
UNIPOLAR OFFSET			±1/2			±1/2	LSB
BIPOLAR OFFSET			±1/2			±1/2	LSB
DIFFERENTIAL NONLINEARITY,[3]	8			8			Bits
$T_A = T_{min}$ to T_{max}	8			8			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			±1			±1	LSB
Bipolar Offset			±1			±1	LSB
Full Scale Calibration[2]			±2			±2	LSB
POWER SUPPLY REJECTION							
Positive Supply							
+4.5≤V+≤+5.5V			±2			±2	LSB
Negative Supply							
−15.75V≤V−≤−14.25V			±2			±2	LSB
−12.6V≤V−≤−11.4V			±2			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			mA
Output Source Current[4]							
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5			0.5			mA
Output Leakage			±40			±40	µA
LOGIC INPUTS							
Input Current			±100			±100	µA
Logic "1"	2.0			2.0			V
Logic "0"			0.8			0.8	V
CONVERSION TIME, T_A and T_{min} to T_{max}	10	20	30	10	20	30	µs
POWER SUPPLY							
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	V
V−	−11.4	−15	−16.5	−11.4	−15	−16.5	V
OPERATING CURRENT							
V+		15	20		15	20	mA
V−		9	15		9	15	mA

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full scale calibration is guaranteed trimmable to zero with an external 200Ω potentiometer in place of the 15Ω fixed resistor.

Full scale is defined as 10 volts minus 1LSB, or 9.961 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]The data output lines have active pull-ups to source 0.5mA. The DATA READY line is open collector with a nominal 6kΩ internal pull-up resistor.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

AD673 ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Options*
AD673JN	0 to +70°C	±1/2LSB max	Plastic DIP (N-20)
AD673JD	0 to +70°C	±1/2LSB max	Ceramic DIP (D-20)
AD673SD	−55°C to +125°C	±1/2LSB max	Ceramic DIP (D-20)
AD673JP	0 to +70°C	±1/2LSB max	PLCC (P-20A)

*See Section 14 for package outline information.

FUNCTIONAL DESCRIPTION

A block diagram of the AD673 is shown in Figure 1. The positive CONVERT pulse must be at least 500ns wide. $\overline{DR}$ goes high within 1.5μs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 8-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is more, the bit is turned off. After testing all bits, the SAR contains a 8-bit binary code which accurately represents the input signal to within (0.05% of full scale).

The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{DATA\ ENABLE}$ can then be activated to enable the 8-bits of data desired. $\overline{DATA\ ENABLE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state.

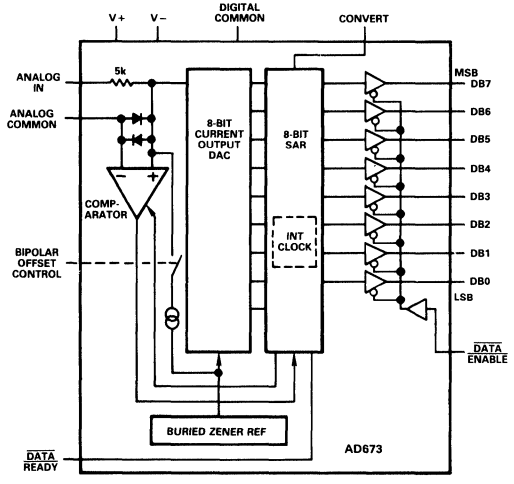


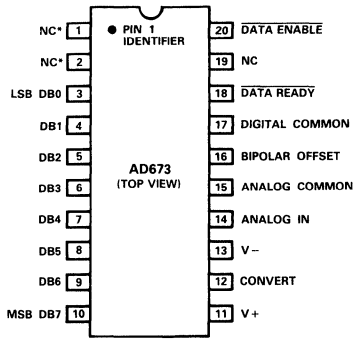
Figure 1. AD673 Functional Block Diagram

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

UNIPOLAR CONNECTION

The AD673 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −12V to −15V), the analog input and the convert pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 2.

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 16) to digital common (pin 17).



*PINS 1 & 2 ARE INTERNALLY CONNECTED TO TEST POINTS AND SHOULD BE LEFT FLOATING

Figure 2. AD673 Pin Connections

Full Scale Calibration

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when an analog input voltage of 9.961 volts (10 volts – 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be within ±2LSB or ±0.8%. If more precise calibration is desired, a 200Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 111111 10 and 11111111. Each LSB will then have a weight of 39.06mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a weight of exactly 40.0mV), a 100Ω resistor and a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ. Figure 3 illustrates the connections required for full scale calibration.

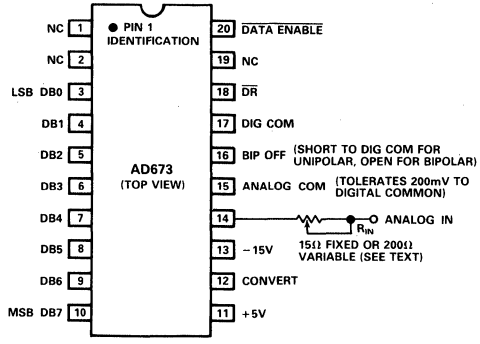


Figure 3. Standard AD673 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ±½LSB for all versions of the AD673, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

Figure 4a shows how the converter zero may be offset to correct for initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

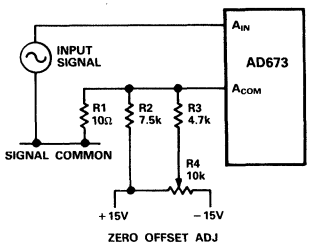


Figure 4a.

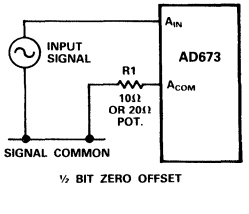


Figure 4b.

Figure 4. Unipolar Offset Trimming

Figure 5 shows the nominal transfer curve near zero for an AD673 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

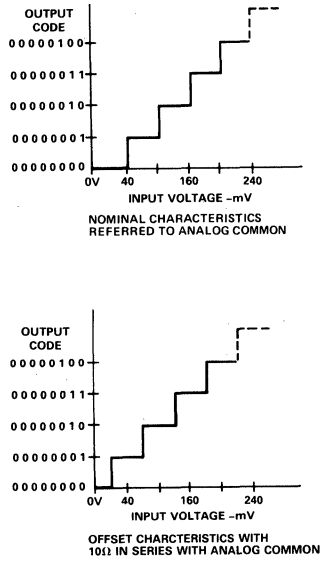


Figure 5. AD673 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights % 39.06mV)

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 10Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 20Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on the previous page should be done with an analog input of 9.941 volts.

NOTE: During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle appropriately during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code, the bipolar offset control pin is left open.

A −5.00 volt signal will give a 8-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and +4.961 volts at the input yields the 11111111 code. The nominal transfer curve is shown in Figure 6.

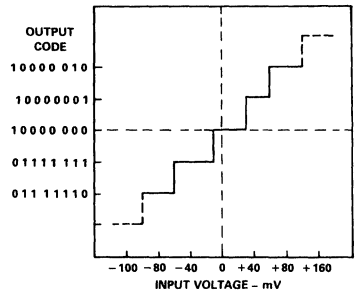


Figure 6. AD673 Transfer Curve–Bipolar Operation

Note that in the bipolar mode, the code transitions are offset ¼LSB such that an input voltage of 0 volts −5mV to +35mV yields the code representing zero (10000000). Each output code is then *centered* on its nominal input voltage.

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is +4.61 volts.

Negative Full Scale Calibration

The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally −5V) which results in the 000000 00 code. R2 should be omitted to obtain a symmetrical range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 7.

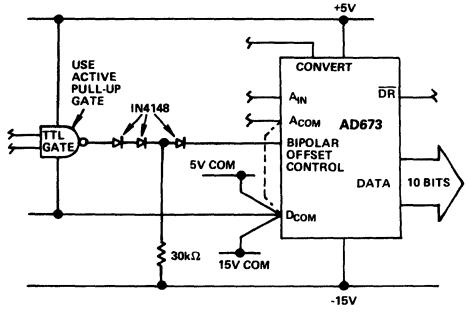


Figure 7. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0–10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD673

Many situations in high-speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD673, a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD673 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms.

$\overline{DR}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD673 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD673).

$\overline{DR}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

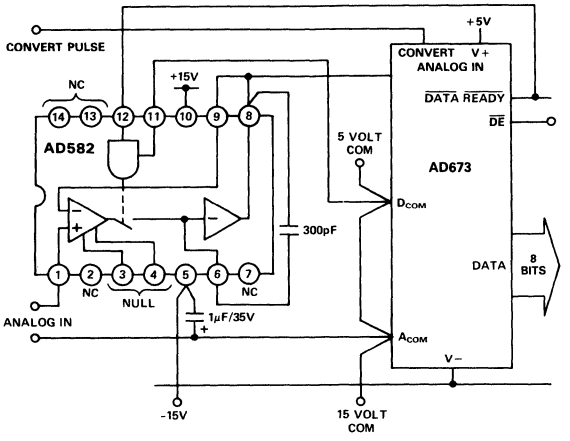


Figure 8. Sample-Hold Interface to the AD673

GROUNDING CONSIDERATIONS

The AD673 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD673

The operation of the AD673 is controlled by two inputs: CONVERT and $\overline{\text{DATA ENABLE}}$.

Starting a Conversion

The conversion cycle is initiated by a positive-going CONVERT pulse at least 500ns wide. The rising edge of this pulse resets the internal logic, clears the result of the previous conversion, and sets $\overline{\text{DR}}$ high. The falling edge of CONVERT begins the conversion cycle. When conversion is completed $\overline{\text{DR}}$ returns low. During the conversion cycle, $\overline{\text{DE}}$ should be held high. If $\overline{\text{DE}}$ goes low during a conversion, the data output buffers will be enabled and intermediate conversion results will be present on the data output pins. This may cause bus conflicts if other devices in a system are trying to use the bus.

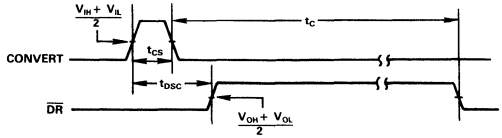


Figure 9. Convert Timing

Reading the Data

The three-state data output buffers is enabled by $\overline{\text{DE}}$. Access time of these buffers is typically 150ns (250 maximum). The Data outputs remain valid until 50ns after the enable signal returns high, and are completely into the high-impedance state 100ns later.

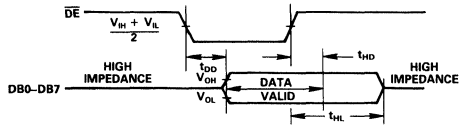


Figure 10. Read Timing

TIMING SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Units
CONVERT Pulse Width	t_{CS}	500	–	–	ns
$\overline{\text{DR}}$ Delay from CONVERT	t_{DSC}	–	1	1.5	µs
Conversion Time	t_C	10	20	30	µs
Data Access Time	t_{DD}	0	150	250	ns
Data Valid after $\overline{\text{DE}}$ High	t_{HD}	50	–	–	ns
Output Float Delay	t_{HL}	–	100	200	ns

MICROPROCESSOR INTERFACE CONSIDERATIONS – GENERAL

When an analog-to-digital converter like the AD673 is interfaced to a microprocessor, several details of the interface must be considered. First, a signal to start the converter must be generated; then an appropriate delay period must be allowed to pass before valid conversion data may be read. In most applications, the AD673 can interface to a microprocessor system with little or no external logic.

The most popular control signal configuration consists of decoding the address assigned to the AD673, then gating this signal with the system's WR signal to generate the CONVERT pulse, and gating it with RD to enable the output buffers. The use of a memory address and memory WR and RD signals denotes "memory-mapped" I/O interfacing, while the use of a separate I/O address space denotes "isolated I/O" interfacing.

Figure 11 shows a generalized diagram of the control logic for an AD673 interfaced to an 8-bit data bus, where an address ADC ADDR has been decoded. ADC ADDR starts the converter when written to (the actual data being written to the converter does not matter) and contains the high byte data during read operations.

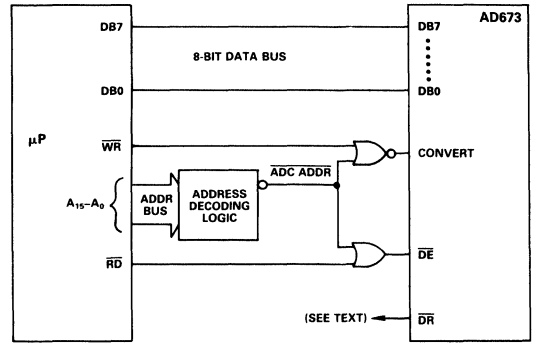


Figure 11. General AD673 Interface to 8-Bit Microprocessor

In systems where this read-write interface is used, at least 30 microseconds (the maximum conversion time) must be allowed to pass between starting a conversion and reading the results. This delay or "timeout" period can be implemented in a short software routine such as a countdown loop, enough dummy instructions to consume 30 microseconds, or enough actual useful instructions to consume the required time. In tightly-timed systems, the $\overline{DR}$ line may be read through an external three-state buffer to determine precisely when a conversion is complete. Higher-speed systems may choose to use $\overline{DR}$ to signal an interrupt to the processor at the end of a conversion.

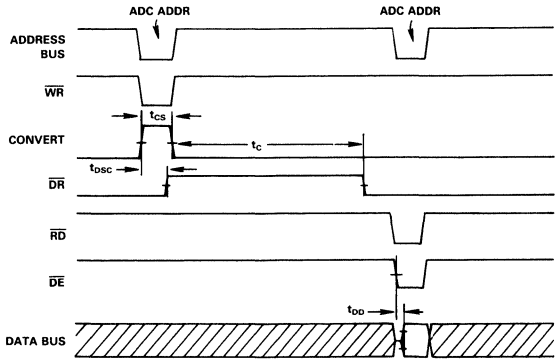


Figure 12. Typical AD673 Timing Diagram

CONVERT Pulse Generation

The AD673 is tested with a CONVERT pulse width of 500ns and will typically operate with a pulse as short as 300ns. However, some microprocessors produce active WR pulses which are shorter than this. Either of the circuits shown in Figure 13 can be used to generate an adequate CONVERT pulse for the AD673. In both circuits, the short low-going WR pulse sets the CONVERT line high through a flip-flop. The rising edge of $\overline{DR}$ (which signifies that the internal logic has been reset) resets the flip-flop and brings CONVERT low, which starts the conversion.

Note that t_{DSC} is slightly longer when the result of the previous conversion contains a logic 1 on the LSB. This means that the actual CONVERT pulse generated by the circuits in Figure 13 will vary slightly in width.

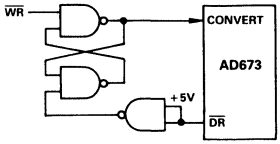


Figure 13a. Using 74LS00

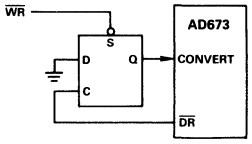


Figure 13b. Using 1/2 74LS74

ANALOG DEVICES

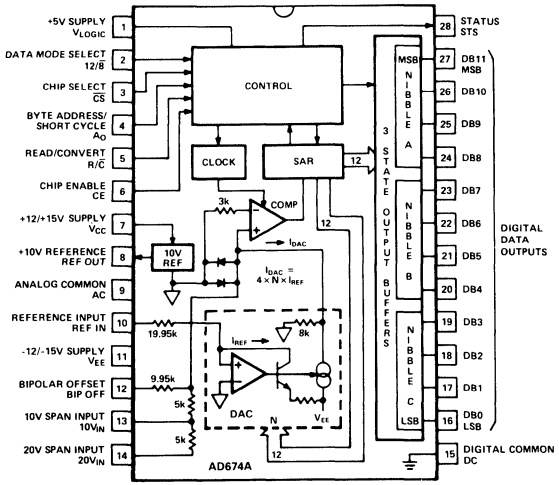
Complete 12-Bit A/D Converter

AD674A*

FEATURES

Complete 12-Bit A/D Converter with Reference and Clock
Faster Version of AD574A
8- and 16-Bit Bus Interface
No Missing Codes Over Temperature
15μs max Conversion Time
±12V and ±15V Operation
Unipolar and Bipolar Inputs
DIP Package

AD674A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD674A is a complete 12-bit successive-approximation analog-to-digital converter with three-state output buffer circuitry for direct interface to an 8- and 16-bit microprocessor bus. A high-precision voltage reference and clock are included on-chip, and the circuit requires only power supplies and control signals for operation.

The AD674A is pin compatible with the industry-standard AD574A but offers faster conversion time and bus-access speed.

The AD674A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost. The chips are laser trimmed at the wafer stage to obtain full rated performance without external trims.

The AD674A is available in six different grades. The AD674AJ, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD674AS, T, and U are specified for the −55°C to +125°C range. All grades are available in a 28-pin hermetically sealed ceramic DIP.

The S, T, and U grades are also available with optional processing to MIL-STD-883C Class B in 28-pin DIP. The Analog Devices Military Products Databook should be consulted for details on /883B testing of the AD674A.

***Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.**

PRODUCT HIGHLIGHTS

1. The AD674A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 to +10 and 0 to +20 volts unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried zener reference is trimmed to 10.00 volts with 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 2.0mA beyond the requirements of the reference and bipolar offset resistors.

SPECIFICATIONS (@ = 25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise indicated)

Model	AD674AJ Min	AD674AJ Typ	AD674AJ Max	AD674AK Min	AD674AK Typ	AD674AK Max	AD674AL Min	AD674AL Typ	AD674AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (Adjustable to zero)			±10			±4			±4	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)		0.1	0.25		0.1	0.25		0.1	0.25	% of F.S.
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Bipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Full-Scale Calibration			±9 (50)			±5 (27)			±2 (10)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min} to T_{max})										
Inputs										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−100		+100	−100		+100	−100		+100	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage ($I_{SOURCE} \leq 500\mu A$)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage ($I_{SINK} \leq 1.6mA$)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	29		18	29		18	29	mA
POWER DISSIPATION		390	720		390	720		390	720	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads)[2] (External load should not change during conversion)			2.0			2.0			2.0	mA

NOTES

[1] Detailed Timing Specifications appear in the Timing Section.

[2] The reference should be buffered for operation on ±12V supplies.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD674AS Min	AD674AS Typ	AD674AS Max	AD674AT Min	AD674AT Typ	AD674AT Max	AD674AU Min	AD674AU Typ	AD674AU Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (Adjustable to zero)			±10			±4			±4	LSB
FULL-SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT to REF IN) (Adjustable to zero)		0.1	0.25		0.1	0.25		0.1	0.25	% of F.S.
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2(5)			±1(2.5)			±1(2.5)	LSB (ppm/°C)
Bipolar Offset			±4(10)			±2(5)			±1(2.5)	LSB (ppm/°C)
Full-Scale Calibration			±20(50)			±10(25)			±5(12.5)	LSB (ppm/°C)
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
V_{CC} = 15V ±1.5V or 12V ±0.6V			±2			±1			±1	LSB
V_{LOGIC} = 5V ±0.5V			±1/2			±1/2			±1/2	LSB
V_{EE} = −15V ±1.5V or −12V ±0.6V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	−5		+5	−5		+5	−5		+5	Volts
	−10		+10	−10		+10	−10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{min} to T_{max})										
Inputs										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	Volts
Current	−100		+100	−100		+100	−100		+100	μA
Capacitance		5			5			5		pF
Outputs (DB11–DB0, STS)										
Logic "1" Voltage ($I_{SOURCE} \leq 500\mu A$)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage ($I_{SINK} \leq 1.6mA$)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	−20		+20	−20		+20	−20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	29		18	29		18	29	mA
POWER DISSIPATION		390	720		390	720		390	720	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads)[2] (External load should not change during conversion)			2.0			2.0			2.0	mA

NOTES

[1]Detailed Timing Specifications appear in the Timing Section.

[2]The reference should be buffered for operation on ±12V supplies.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{EE} to Digital Common . . . . . 0 to −16.5V
V_{LOGIC} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±1V
Digital Inputs to Digital Common . −0.5V to V_{LOGIC} +0.5V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
$20V_{IN}$ to Analog Common . . . . . ±24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}
Chip Temperature . . . . . 175°C
Power Dissipation 825mW
Lead Temperature, Soldering . . . . . 300°C, 10sec
Storage Temperature . . . . . −65°C to +150°C

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD674A ORDERING GUIDE

Model	Temperature Range	Linearity Error (T_{min} to T_{max})	No Missing Codes (T_{min} to T_{max})	Full Scale T.C. (ppm/°C)	Package Option*
AD674AJD	0 to +70°C	±1LSB	11 Bits	50.0	D-28
AD674AKD	0 to +70°C	±1/2LSB	12 Bits	27.0	D-28
AD674ALD	0 to +70°C	±1/2LSB	12 Bits	10.0	D-28
AD674ASD	−55°C to +125°C	±1LSB	11 Bits	50.0	D-28
AD674ATD	−55°C to +125°C	±1LSB	12 Bits	25.0	D-28
AD674AUD	−55°C to +125°C	±1LSB	12 Bits	12.5	D-28

*See Section 14 for package outline information.

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD674AK, L, T, and U grades are guaranteed for maximum nonlinearity of ±1/2LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD674AJ and S grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD674AK, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD674AJ and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed later. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the AD674A is left-justified. This means that the data represents the analog input as a fraction of full scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

FULL-SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full-scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 3 and 4. The full-scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full-scale gain from the initial value using the internal 10V reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the AD674A assume use of +5.00 and ±15.00 or ±12.00V supplies. The only effect of power supply error on the performance of the device will be a small change in the full-scale calibration. This will result in a linear change in all lower-order codes. The specifications show the maximum full-scale change from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full-scale range or 2.44mV out of 10 volts for a 12-bit ADC.

CIRCUIT OPERATION

The AD674A is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD674A is shown in Figure 1.

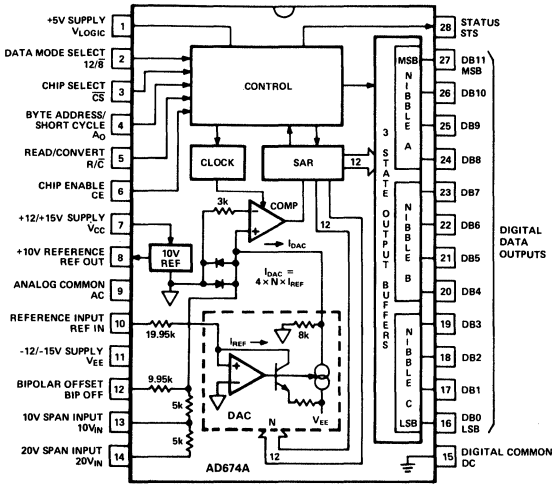


Figure 1. Block Diagram of AD674A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers. The SAR, timed by the clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2LSB.

The temperature-compensated buried zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1%; it can supply up to 1.5mA to an external load in addition to the requirements of the reference input resistor (0.5mA) and bipolar offset resistor (1mA) when the AD674A is powered from ±15V supplies. If the AD674A is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD674A reference must remain constant during conversion. The thin film application resistors are trimmed to match the full-scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation and connected to the 10 volt reference for bipolar operation.

DRIVING THE AD674A ANALOG INPUT

The AD674A is a successive-approximation analog-to-digital converter. During the conversion cycle, the ADC input current is modulated by the DAC test current at approximately a 1MHz rate. Thus it is important to recognize that the signal source driving the AD674A must be capable of holding a constant output voltage under dynamically-changing load conditions.

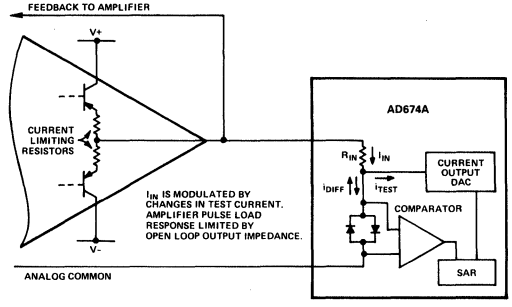


Figure 2. Op Amp – AD674A Interface

The closed-loop output impedance of an op amp is equal to the open-loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. It is often assumed that the loop gain of a follower-connected op amp is sufficiently high to reduce the closed-loop output impedance to a negligibly small value, particularly if the signal is low frequency. However, the amplifier driving an AD674A must either have sufficient loop gain at 1MHz to reduce the closed-loop output impedance to a low value or have low open-loop output impedance. This can be accomplished by using a wideband op amp, such as the AD711.

If a sample-hold amplifier is required, the monolithic AD585 is recommended. Its output buffer will drive the AD674A input directly.

SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

It is critically important that the AD674A power supplies be filtered, well regulated, and free from high frequency noise. Use of noisy supplies will cause unstable output codes. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Remember that a few millivolts of noise represents several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitor should be connected directly from Pin 1 to Pin 15 (digital common) and the $+V_{CC}$ and $-V_{EE}$ pins should be decoupled directly to analog common (Pin 9). A suitable decoupling capacitor is a 4.7μF tantalum type in parallel with a 0.1μF disc ceramic type.

Circuit layout should attempt to locate the AD674A, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD674A

The AD674A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +12/+15 and −12/−15 volts), the analog input, and the conversion initiation command, as discussed on the next page.

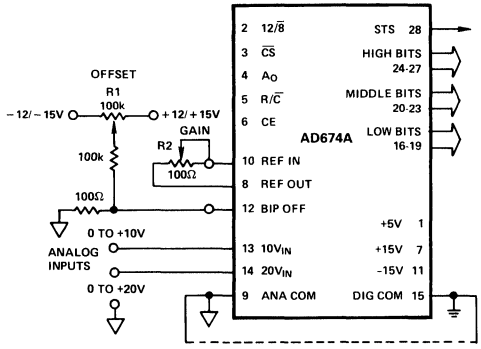


Figure 3. Unipolar Input Connections

All of the thin-film application resistors of the AD674A are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD674A guarantees ±2LSB max zero offset error and ±0.25% (10LSB) max full scale error. If the offset trim is not required, Pin 12 can be connected directly to Pin 9; the two resistors and trimmer for Pin 12 are then not needed. If the full-scale trim is not required, a 50Ω ±1% metal film resistor should be connected between Pin 8 and Pin 10.

The analog input is connected between Pins 13 and 9 for a 0 to +10V input range, between Pins 14 and 9 for a 0 to +20V input range. The AD674A easily accommodates input signals beyond the supplies. For the 10 volt span input, the LSB has a nominal value of 2.44mV; for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to Pin 13 (for a full-scale range of 20.48V (5mV/bit), use a 500Ω trimmer into Pin 14). The gain trim described below is now done with these trimmers. The nominal input impedance into Pin 13 is 5kΩ, and 10kΩ into Pin 14.

UNIPOLAR CALIBRATION

The connections for unipolar ranges are shown in Figure 3. The AD674A is trimmed to a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If Pin 12 is connected to Pin 9, the unit will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15mV of offset trim range.

The full-scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal ½LSB above negative full scale (−4.9988V for the ±5V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1½LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

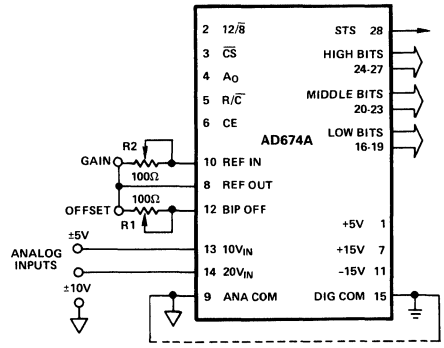


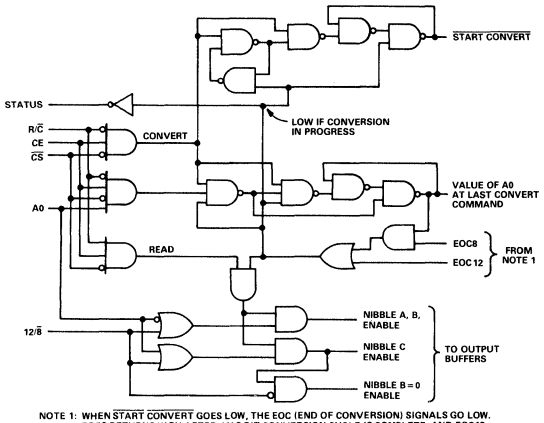
Figure 4. Bipolar Input Connections

GROUNDING CONSIDERATIONS

The analog common at Pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD674A; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD674A in an environment of high digital noise content, it is required that the analog and digital commons be connected together at the package. In some situations, the digital common at Pin 15 can be connected to the most convenient ground reference point; digital power return is preferred.

CONTROL LOGIC

The AD674A contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 5 shows the internal logic circuitry of the AD674A.



NOTE 1: WHEN START CONVERT GOES LOW, THE EOC (END OF CONVERSION) SIGNALS GO LOW. EOC8 RETURNS HIGH AFTER AN 8-BIT CONVERSION CYCLE IS COMPLETE, AND EOC12 RETURNS HIGH WHEN ALL 12 BITS HAVE BEEN CONVERTED. THE EOC SIGNALS PREVENT DATA FROM BEING READ DURING CONVERSIONS.

Figure 5. AD674A Control Logic

The control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data read (R/$\overline{C}$ = 1) or a convert (R/$\overline{C}$ = 0) is in progress. The register control inputs A_0 and 12/$\overline{8}$ control conversion length and data format. If a conversion is started with A_0 low, a full 12-bit conversion cycle is initiated. If A_0 is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word (12/$\overline{8}$ tied to V_{LOGIC}). In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	1	X	Enable 12-Bit Parallel Output
1	0	1	0	0	Enable 8 Most Significant Bits
1	0	1	0	1	Enable 4LSBs + 4 Trailing Zeroes

Table I. AD674A Truth Table

TIMING

The AD674A is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the AD674A control signals will provide the system designer with useful insight into the operation of the device.

Figure 6 shows a complete timing diagram for the AD674A convert start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention. Either CE or $\overline{CS}$ may be used to initiate a conversion. As shown in Figure 6, CE is used. Note that CE includes one less propagation delay than $\overline{CS}$ and is therefore the faster input.

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffers cannot be enabled during conversion.

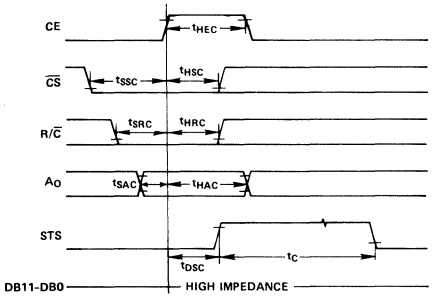


Figure 6. Convert Start Timing

CONVERT START TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE			200	ns
t_{HEC}	CE Pulse Width	50			ns
t_{SSC}	$\overline{CS}$ to CE Setup	50			ns
t_{HSC}	$\overline{CS}$ Low During CE High	50			ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50			ns
t_{HRC}	R/$\overline{C}$ Low During CE High	50			ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	50			ns
t_C	Conversion Time				
	8-Bit Cycle	6	8	10	µs
	12-Bit Cycle	9	12	15	µs

Figure 7 shows the timing for data read operations. During data read operations, access time is measured from the point where CE and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low).

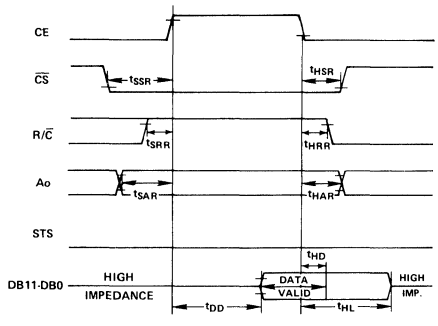
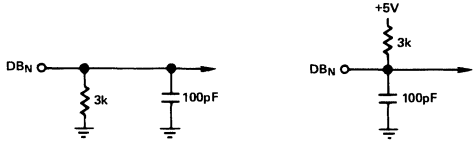


Figure 7. Read Cycle Timing

READ TIMING – FULL CONTROL MODE

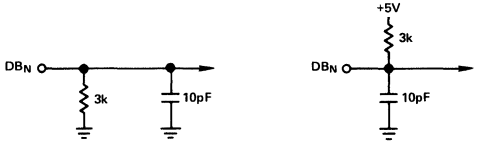
Symbol	Parameter	Min	Typ	Max	Units
t_{DD}[1]	Access Time (from CE)		75	150	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}[2]	Output Float Delay			150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50			ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	50			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE low	50			ns

[1] t_{DD} is measured with the load circuit of Figure 8 and defined as the time required for an output to cross 0.4V or 2.4V.
[2] t_{HL} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 9.



a. High-Z to Logic 1 *b. High-Z to Logic 0*

Figure 8. Load Circuit for Access Time Test



a. Logic 1 to High-Z *b. Logic 0 to High-Z*

Figure 9. Load Circuit for Output Float Delay Test

"STAND-ALONE" OPERATION

The AD674A can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This gives rise to two possible control signals–a high pulse or a low pulse. Operation with a low pulse is shown in Figure 10. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes high 200ns after R/$\overline{C}$ goes low and returns low 600ns after data is valid.

If conversion is initiated by a high pulse as shown in Figure 11, the data lines are enabled during the time when R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

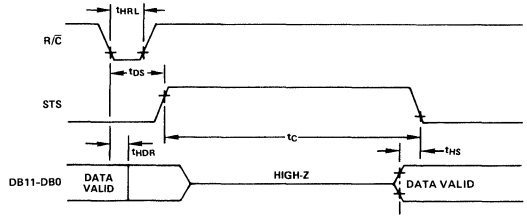


Figure 10. Low Pulse fo R/$\overline{C}$–Outputs Enabled After Conversion

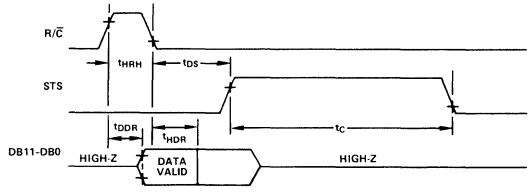


Figure 11. High Pulse for R/$\overline{C}$-Outputs Enable While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	30	55	600	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most integrated circuit ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD674A provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD674A is only 15 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 15 microseconds to convert, and insert a sufficient number of "no-op" instructions to ensure that 15 microseconds of processor time is consumed.

Once conversion is complete, the data can be read. For converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD674A includes internal logic to permit direct interface to 8-bit and 16-bit data buses, selected by the state of the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A0 low) contains the 8MSBs (DB11 through DB4). The odd address (A0 high) contains the 4LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

It is not possible to rearrange the AD674A data lines for right-justified 8-bit bus interface.

	D7							D0
XXX0 (EVEN ADDR):	DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4
XXX1 (ODD ADDR):	DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

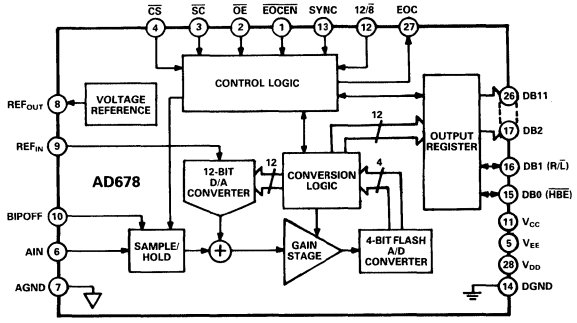
Figure 12. AD674A Data Format for 8-Bit Bus

12-Bit 200 KSPS Complete Sampling ADC

AD678

FEATURES
AC and DC Characterized and Specified
200k Conversions per Second
1 MHz Full Power Bandwidth
500 kHz Full Linear Bandwidth
72 dB S/N+D (K Grade)
Twos Complement Data Format (Bipolar Mode)
Straight Binary Data Format (Unipolar Mode)
10 MΩ Input Impedance
8-Bit or 16-Bit Bus Interface
On-Board Reference and Clock
10 V Unipolar or Bipolar Input Range

AD678 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD678 is a complete, multipurpose 12-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD678 is similar to the AD1678 in that it is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD678 is fully specified for dc parameters which are important in measurement applications.

The AD678 offers a choice of digital interface formats; the 12 data bits can be accessed by a 16-bit bus in a single read operation or by an 8-bit bus in two read operations (8+4), with right or left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD678 operates from +5 V and ±12 V supplies and dissipates 745 mW. A 28-pin plastic DIP and a 0.6″ wide ceramic DIP are available. Contact factory for surface-mount package options.

Screening to MIL-STD-883C Class B is also available.

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD678 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD678 is specified for both dc and ac parameters. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the choice of single or two read cycle output provides compatibility with 16- or 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD678 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

AD678 ORDERING GUIDE
Temperature Range and Package Options[1]

Plastic DIP (N-28A) 0 to +70°C	PLCC (P-28A) 0 to +70°C	Ceramic DIP (D-28A) 0 to +70°C	Ceramic DIP (D-28A) −55°C to +125°C	Integral Nonlinearity T_{min} to T_{max}	S/N&D[2]
AD678JN	AD678JP	AD678JD	AD678SD	±1 LSB	71
AD678KN	AD678KP	AD678KD	AD678TD	±1/2 LSB	73

NOTE
[1]See Section 14 for package outline information.
[2]Typical at 10 kHz, −0.5 dB input.

SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = + 5 V ±10%, f_{SAMPLE} = 200 KSPS, f_{IN} = 10.06 kHz unless otherwise noted)[1]

Parameter	AD678J/S Min	AD678J/S Typ	AD678J/S Max	AD678K/T Min	AD678K/T Typ	AD678K/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO							
@ +25°C	**70**	71		**72**	73		dB
T_{min} to T_{max}	**70**	71		**71**	73		dB
TOTAL HARMONIC DISTORTION (THD)							
@ +25°C		−88	**−80**		−88	**−80**	dB
		0.004	**0.010**		0.004	**0.010**	%
T_{min} to T_{max}		−85	**−78**		−85	**−78**	dB
		0.005	**0.012**		0.005	**0.012**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−87	**−80**		−87	**−80**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−85	**−80**		−85	**−80**	dB
3rd Order Products		−90	**−80**		−90	**−80**	dB

NOTE
[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal.
[2]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 200 KSPS. See Definition of Specifications section.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.4**		V
V_{IL}	Low Level Input Voltage			**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = 5 V		**10**	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V		**10**	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V		**10**	μA
C_{Oz}	High Z Output Capacitance			10	pF

NOTES
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

DC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10% unless otherwise indicated)

Parameter	AD678J Min	AD678J Typ	AD678J Max	AD678K Min	AD678K Typ	AD678K Max	Units
TEMPERATURE RANGE	0		+70	0		+70	°C
ACCURACY							
Resolution	12			12			Bits
Integral Linearity Error			±1			±1/2	LSB
Differential Linearity	11			12			Bits
Unipolar Zero Error (@ 25°C)[1]			±2			±2	LSB
Bipolar Zero Error (@ 25°C)[1]			±2			±2	LSB
Gain Error (@ 25°C)[1,2]			±8			±4	LSB
Temperature Drift (Coefficients)							
Unipolar Zero[3]			±2 (10)			± 1 (5)	LSB (ppm/°C)
Bipolar Zero[3]			±2 (10)			± 1 (5)	LSB (ppm/°C)
Gain[3]			±9 (50)			±5 (27)	LSB (ppm/°C)
Gain[4]			±2 (10)			±2 (10)	LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Range	0		+10	0		+10	V
Bipolar Range	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1		1		μs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	4.95		5.05	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ±5%[6]			±1			±1	LSB
V_{EE} = −12 V ±5%			±1			±1	LSB
V_{DD} = +5 V ±10%			±1			±1	LSB
Operating Current							
I_{CC}		18	20		18	20	mA
I_{EE}		25	34		25	34	mA
I_{DD}		8	12		8	12	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero. See Figures 6 and 7.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
[6]1.4 V of headroom is required between V_{CC} and AIN.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

SPECIFICATIONS

DC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10% unless otherwise indicated)

Parameter	AD678S Min	AD678S Typ	AD678S Max	AD678T Min	AD678T Typ	AD678T Max	Units
TEMPERATURE RANGE	−55		+125	−55		+125	°C
ACCURACY							
Resolution	12			12			Bits
Integral Linearity Error			±1			±1/2	LSB
Differential Linearity	11			12			Bits
Unipolar Zero Error (@ 25°C)[1]			±2			±2	LSB
Bipolar Zero Error (@ 25°C)[1]			±2			±2	LSB
Gain Error (@ 25°C)[1,2]			±8			±4	LSB
Temperature Drift (Coefficients)							
Unipolar Zero[3]			±4 (10)			± 4 (10)	LSB (ppm/°C)
Bipolar Zero[3]			±4 (10)			± 4 (10)	LSB (ppm/°C)
Gain[3]			±18 (44)			±18 (44)	LSB (ppm/°C)
Gain[4]			±4 (10)			±4 (10)	LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Range	0		+10	0		+10	V
Bipolar Range	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time		1			1		μs
Aperture Delay		10			10		ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	4.95		5.05	4.98		5.02	V
External Load							
Unipolar Mode			+1.5			+1.5	mA
Bipolar Mode			+0.5			+0.5	mA
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ±5%[6]			±1			±1	LSB
V_{EE} = −12 V ±5%			±1			±1	LSB
V_{DD} = +5 V ±10%			±1			±1	LSB
Operating Current							
I_{CC}		18	20		18	20	mA
I_{EE}		25	34		25	34	mA
I_{DD}		8	12		8	12	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero. See Figures 6 and 7.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
[6]1.4 V of headroom is required between V_{CC} and AIN.

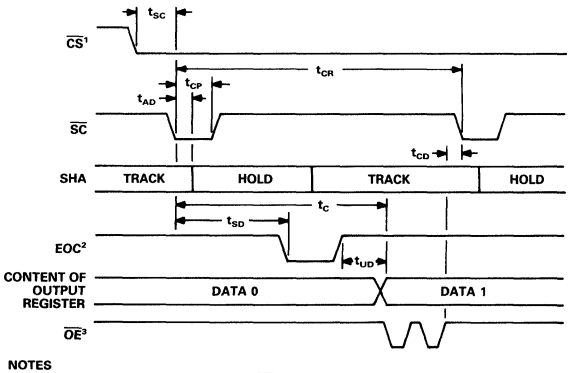
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

TIMING SPECIFICATIONS (All grades, T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10% unless otherwise noted)

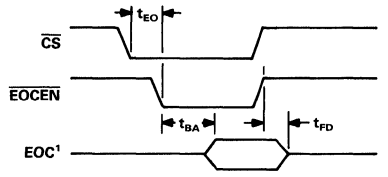
Parameter	Symbol	Min	Typ	Max	Units
$\overline{SC}$ Delay	t_{SC}	50			ns
Conversion Rate	t_{CR}			5	µs
				5.23	µs[1]
Convert Pulse Width	t_{CP}	150			ns
Aperture Delay	t_{AD}	5		20	ns
Conversion Time[2]	t_C		**3.9**	**4.47**	µs
	t_C		4.1	**4.70**	µs[3]
Status Delay	t_{SD}	0		**400**	ns
Access Time[4]	t_{BA}			**100**	ns
Float Delay[5]	t_{FD}	10		**80**	ns
Update Delay	t_{UD}			200	ns
Format Setup	t_{FS}	60			ns
$\overline{OE}$ Delay	t_{OE}	20			ns
Read Pulse Width	t_{RP}	100			ns[6]
		150			ns[7]
Conversion Delay	t_{CD}	150			ns
$\overline{EOCEN}$ Delay	t_{EO}	20			ns

NOTES
[1]S,T grades in 8-bit read mode (see Figure 4).
[2]Includes Acquisition Time.
[3]S, T grades.
[4]Measured from the falling edge of $\overline{OE}/\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 3; C_{OUT} = 100 pF.
[5]Measured from the rising edge of $\overline{OE}/\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 3; C_{OUT} = 10 pF.
[6]12-bit read mode.
[7]8-bit read mode.
Specifications subject to change without notice.



NOTES
[1]IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2]$\overline{EOCEN}$ = LOW; FIGURE 2. IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
[3]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing



NOTE
[1]SEE END-OF-CONVERT (EOC) PARAGRAPH FOR DETAILS.

Figure 2. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

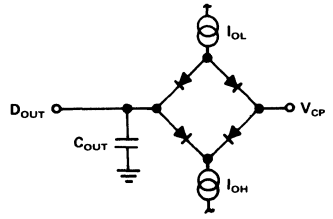


Figure 3. Load Circuit for Bus Timing Specifications

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both Chip Select ($\overline{CS}$) and Start Convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW t_{SC} before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ low, regardless of the state of $\overline{CS}$.

Before a conversion is started, End-of-Convert (EOC) is HIGH, and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample. EOC goes HIGH when the conversion is finished.

In track mode, the sample-hold will settle to ±0.01% (12 bits) in 1 μs maximum. The acquisition time does not affect the throughput rate as the AD678 goes back into track mode more than 1 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

END-OF-CONVERT

In asynchronous mode, End-of-Convert (EOC) is an open drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by End-of-Convert ENable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output which is enabled by $\overline{EOCEN}$ and $\overline{CS}$. See the Conversion Status Truth Table for details. Access (t_{BA}) and float (t_{FD}) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the 10 pF output capacitance and the pull-up resistor.

12-BIT MODE CODING FORMAT (1 LSB = 2.44 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}	Output Code	V_{IN}	Output Code
0	000 . . . 0	−5.000 V	100 . . . 0
5.000 V	100 . . . 0	−0.002 V	111 . . . 1
9.9964 V	111 . . . 1	0	000 . . . 0
		+2.500 V	010 . . . 0
		+4.9964 V	011 . . . 1

OUTPUT ENABLE TRUTH TABLES

12-BIT MODE (12/$\overline{8}$ = HIGH)

INPUTS	OUTPUT
($\overline{CS}$ U $\overline{OE}$)	DB11–DB0
1	High Z
↓	Enable 12-Bit Output

8-BIT MODE (12/$\overline{8}$ = LOW)

	INPUTS			OUTPUTS							
	R/$\overline{L}$	$\overline{HBE}$	($\overline{CS}$ U $\overline{OE}$)	DB11 . . . DB4							
	X	X	1	← High Z →							
	1	0	↓	0	0	0	0	a	b	c	d
Unipolar	1	1	↓	e	f	g	h	i	j	k	l
Mode	0	0	↓	a	b	c	d	e	f	g	h
	0	1	↓	i	j	k	l	0	0	0	0
	1	0	↓	a	a	a	a	a	b	c	d
Bipolar	1	1	↓	e	f	g	h	i	j	k	l
Mode	0	0	↓	a	b	c	d	e	f	g	h
	0	1	↓	i	j	k	l	0	0	0	0

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
U = Logical OR.
a = MSB.
l = LSB.
↓ = HIGH to LOW transition. Must stay low for t = t_{RP}.

START CONVERSION TRUTH TABLE

	INPUTS			
	SYNC	$\overline{CS}$	$\overline{SC}$	STATUS
Synchronous Mode	1	1	X	No Conversion
	1	0	↓	Start Conversion
	1	↓	0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion
Asynchronous Mode	0	X	1	No Conversion
	0	X	↓	Start Conversion
	0	X	0	Continuous Conversion

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay low for t = t_{CP}.

CONVERSION STATUS TRUTH TABLE

	INPUTS			OUTPUT	
	SYNC	$\overline{CS}$	$\overline{EOCEN}$	EOC	STATUS
Synchronous Mode	1	0	0	0	Converting
	1	0	0	1	Not Converting
	1	1	X	High Z	Either
	1	X	1	High Z	Either
Asynchronous Mode*	0	X	0	0	Converting
	0	X	0	High Z	Not Converting
	0	X	1	High Z	Either

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
*EOC requires a pull-up resistor in asynchronous mode.

OUTPUT ENABLE OPERATION

The data bits (DB11–DB0) are three-state outputs enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. Bits DB1 (R/$\overline{L}$) and DB0 ($\overline{HBE}$) are bidirectional. In 12-bit mode they are data output bits. In 8-bit mode they are inputs which define the format of the output register.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REF_{OUT}), output coding is twos complement binary.

When EOC goes HIGH, the output register contains the results of the previous conversion. A period of time t_{UD} is required for the present conversion results to be loaded into the output register. Bringing $\overline{OE}$ LOW t_{OE} after $\overline{CS}$ goes LOW makes the output register contents available on the data bits. A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued. This allows internal logic states to reset and guarantees minimum aperture jitter for the next conversion.

Output Enable ($\overline{OE}$) must be toggled to update the output register in both 8- and 12-bit read modes.

Figure 4 illustrates the 8-bit read mode (12/$\overline{8}$ = LOW), where only DB11–DB4 are used as output lines onto an 8-bit bus. The output is read in two steps, with the high byte read first, followed by the low byte. High Byte Enable ($\overline{HBE}$) controls the output sequence. The 12-bit result can be right or left justified depending on the state of R/$\overline{L}$. Note that for S and T grades, the 8-bit read mode results in a conversion rate of 5.23 µs.

In 12-bit read mode (12/$\overline{8}$ = HIGH), a single READ operation accesses all 12 output bits on DB11–DB0 for interface to a 16-bit bus. Figure 5 provides the output timing relationships. Note that t_{CR} must be ovserved, in that $\overline{SC}$ pulses should not be issued at intervals closer than 5 µs. If $\overline{SC}$ is asserted sooner than 5 µs, conversion accuracy may deteriorate. For this reason, $\overline{SC}$ should not be held LOW in an attempt to operate in a continuous convert mode.

POWER-UP

A conversion sequence, consisting of one $\overline{SC}$ instruction, is required after power-up to reset internal logic.

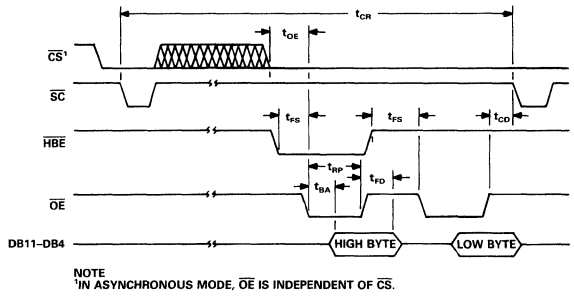


Figure 4. Output Timing, 8-Bit Read Mode

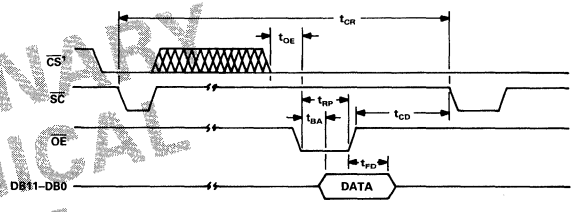


Figure 5. Output Timing, 12-Bit Read Mode

Definition of Specifications

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD678 has been designed to optimize input bandwidth, allowing the AD678 to undersample input signals with frequencies significantly above the converter's Nyquist frequency.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL LINEARITY (DNL)
In an ideal ADC, code transitions are 1LSB apart. Differential linearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

This specification is 12 bits from T_{min} to T_{max} for the AD678K and T grades, which guarantees that all 4096 codes are present over temperature. The AD678J and S grades specify 11 bits NMC T_{min} to T_{max}, which means that missing codes do not occur adjacent to each other.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (1111 1111 1111 to 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for a 0–10 V range, 4.9963 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

INTEGRAL LINEARITY ERROR (INL)
The ideal transfer function for a linear ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2LSB before the first code transition. "Full scale" is defined as a level 1 1/2LSB beyond the last code transition. Integral linearity error is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

The AD678K and T grades are guaranteed for maximum integral linearity error of ±1/2LSB T_{min} to T_{max}. For these grades, this means that an analog value which falls exactly in the center of a given code will result in the correct digital output code. Values nearer the upper or lower transition of the code may produce the next upper or lower digital output code. The AD678J and S grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user adjustable.

POWER SUPPLY REJECTION

Variations in power supply will affect the full-scale calibration. This will result in a linear change in all lower-order codes. The specifications show the maximum change in the full-scale transition point due to a change in power-supply voltage from the nominal value.

TEMPERATURE COEFFICIENT

This is the maximum change in the parameter from the initial value (@ 25°C) to the value at T_{min} or T_{max}.

AD678 PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground. This is the ground return for AIN only.
AIN	6	A1	Analog Signal Input.
BIPOFF	10	A1	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} through 50 Ω resistor for ±5 V input bipolar mode and twos complement binary output coding. See Figures 7 and 8.
$\overline{CS}$	4	D1	Chip Select. Active LOW.
DGND	14	P	Digital Ground
DB11–DB4	26–19	DO	Data Bits 11 through 4. In 12-bit format (see 12/$\overline{8}$ pin), these pins provide the upper 8 bits of data. In 8-bit format, these pins provide all 12 bits in two bytes (see R/$\overline{L}$ pin). Active HIGH.
DB3, DB2	18, 17	DO	Data Bits 3 and 2. In 12-bit format, these pins provide Data Bit 3 and Data Bit 2. Active HIGH. In 8-bit format they are undefined and should be tied to V_{DD}.
DB1 (R/$\overline{L}$)	16	DO	In 12-bit format, Data Bit 1. Active HIGH.
DB0($\overline{HBE}$)	15	DO	In 12-bit format, Data Bit 0. Active HIGH.
EOC	27	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. In asynchronous mode, EOC is an open drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	DI	End-Of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$ (DB0)	15	DI	In 8-bit format, High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte.
$\overline{OE}$	2	DI	Output Enable. The falling edge of $\overline{OE}$ enables DB11–DB0 in 12-bit format and DB11–DB4 in 8-bit format. Gated with $\overline{CS}$. Active LOW.
REF_{IN}	9	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	AO	+5 V Reference Output. Tied to REF_{IN} through 50 Ω resistor for normal operation.
R/$\overline{L}$ (DB1)	16	DI	In 8-bit format, Right/Left justified. Sets alignment of 12-bit result within 16-bit field. Tied to V_{DD} for right-justified output and tied to DGND for left-justified output.
$\overline{SC}$	3	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	DI	SYNC Control. If tied to V_{DD} (synchronous mode), $\overline{SC}$, EOC and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open drain output. EOC requires an external 3 kΩ pull-up resistor in asynchronous mode.
V_{CC}	11	P	+12 V Analog Power.
V_{EE}	5	P	−12 V Analog Power.
V_{DD}	28	P	+5 V Digital Power.
12/$\overline{8}$	12	DI	Twelve/eight bit format. If tied HIGH, sets output format to 12-bit parallel. If tied LOW, sets output format to 8-bit multiplexed.

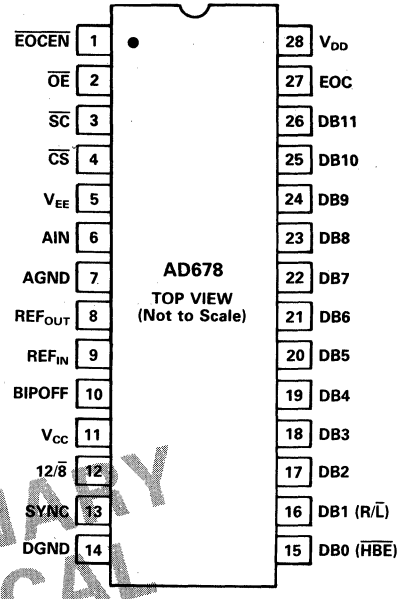
Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers.
P = Power.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	−12	+12	V
REF_{IN}	V_{EE}	0	V_{CC}	V
REF_{IN}	V_{CC}	V_{EE}	0	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature				
J and K Grades		0	+70	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ESD SENSITIVITY

The AD678 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD678 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

Application Information

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD678 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 1000 Ω. The 10 V p-p full-scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

The AD678 is factory trimmed to minimize linearity, offset and gain errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical (as in some ac applications), even these components can be eliminated.

In some applications, offset and gain errors need to be trimmed out completely. The following sections describe the correct procedure for these various situations.

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 6. This circuit allows approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim (±20 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code will be centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 0000 0000 0000 to 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (1.22 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 1.22 mV signal to AIN and adjust R1 until the first transition is located. range

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9963 V for a 10 V range) and adjust R2 until the last transition is located (1111 1111 1110 to 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 7. In this mode, data output coding will be in twos-complement binary. This circuit will allow approximately ±25 mV of offset trim range (±10 LSB) and ± 0.5% of gain trim range (20 LSB).

Either or both of the trim pots can be replaced with 50 Ω ± 1% fixed resistors if the AD678 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 1%.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−1.22 mV for a ±5 V range) and adjust R1 until the major carry transition is located (1111 1111 1111 to 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9963 V for a ±5 V range) and adjust R2 to give the last positive transition (0111 1111 1110 to 0111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single-pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9988 V for a ±5 V range) and adjust R1 until the minus full-scale transition is located (1000 0000 0000 to 1000 0000 001). Then perform the gain error trim as outlined above.

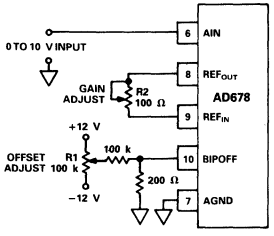


Figure 6. Unipolar Input Connections with Gain and Offset Trims

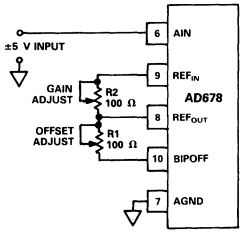


Figure 7. Bipolar Input Connections with Gain and Offset Trims

BOARD LAYOUT

Designing with high-resolution data converters requires careful attention to layout considerations. Trace impedance is the first issue. At the 12-bit level, a 5 mA current through a 0.5 Ω trace will develop a voltage drop of 2.5 mV, which is 1 LSB for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high-accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD678 incorporates several features to help the user's layout. First of all, analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit design. Current through AGND is 200 μA, with no code-dependent variation. The only current through DGND is the return current for DB11–DB0 and EOC.

SUPPLY DECOUPLING

The AD678 power supplies should be well filtered, well regulated, and free from high-frequency noise. Switching power supplies are not recommended. These supplies generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and analog ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic provides adequate decoupling. The power supply pins should be decoupled directly to DGND.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD678, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD678 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD678 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD678. If multiple AD678s are used or the AD678 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

INTERFACING THE AD678 TO MICROPROCESSORS

The I/O capabilities of the AD678 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD678 interface configurations.

AD678 TO TMS320C25

In Figure 8 the AD678 is mapped into the TMS320C25 I/O space. AD678 conversions are initiated by issuing an OUT instruction to Port 8. EOC status and the conversion result are read in with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 8 and $\overline{MSC}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD678 read instruction.

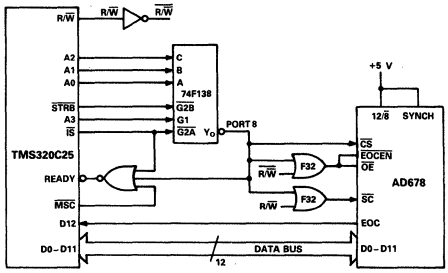


Figure 8. AD678 to TMS320C25 Interface

AD678 TO 80186

Figure 9 shows the AD678 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD678 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD678 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD678 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ operation resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6-MHz and 8-MHz 80186 processors.

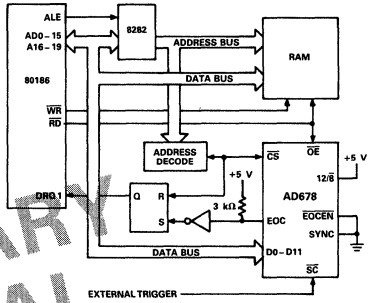


Figure 9. AD678 to 80186 DMA Interface

AD678 TO Z80

The AD678 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 10 illustrates an I/O configuration, where the AD678 occupies several port addresses to allow separate polling of the EOC status and reading of the data. The lower address bit, A0, is used to select the high and low order bytes of the result. The AD678 R/$\overline{L}$ line is tied HIGH, resulting in right justified output data.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD678 to be used with Z80 processors having clock speeds up to 8 MHz.

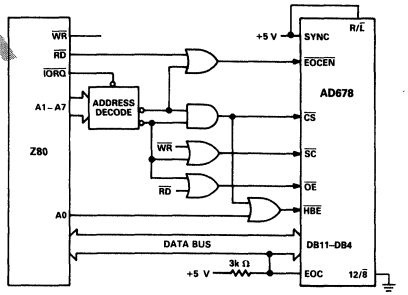


Figure 10. AD678 to Z80 Interface

AD678 TO ANALOG DEVICES ADSP-2100A

Figure 11 demonstrates the AD678 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD678 data memory interface with two hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD678 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts $\overline{HBE}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latches, is used to force the ADSP-2100A into a two cycle wait state by generating DMACK. The read operation is thus started and completed within 3 processor cycles (240 ns). $\overline{HBE}$ is released during "high byte read." This allows the processor to read the lower byte of data as soon as "high byte read" is complete. The low byte read operation executes in a similar manner to the first and is completed during the next 240 ns.

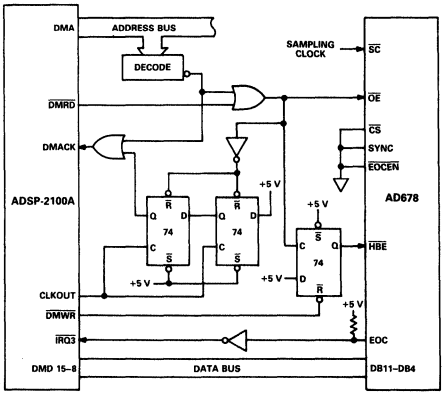


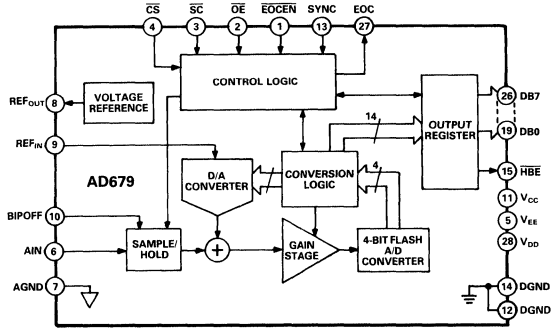
Figure 11. AD678 to ADSP-2100A Interface

14-Bit 100 KSPS Complete Sampling ADC

AD679

FEATURES
AC and DC Characterized and Specified
100k Conversions per Second
1 MHz Full Power Bandwidth
500 kHz Full Linear Bandwidth
80 dB S/N+D (K Grade)
Twos Complement Data Format (Bipolar Mode)
Straight Binary Data Format (Unipolar Mode)
10 MΩ Input Impedance
8 Bit Bus Interface (See AD779 for 16-Bit Interface)
On Board Reference and Clock
10 V Unipolar or Bipolar Input Range

AD679 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD679 is a complete, multipurpose 14-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD679 is similar to the AD1679 in that it is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD679 is fully specified for dc parameters which are important in measurement applications.

The 14 data bits are accessed in two read operations (8+6), with left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation. Conversions can be initiated either under microprocessor control or by an external clock asynchronous to the system clock.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD679 operates from +5 V and ±12 V supplies and dissipates 720 mW. A 28-pin plastic DIP and a 0.6″ wide ceramic DIP are available. Contact factory for surface-mount package options.

Screening to MIL-STD-883C Class B is available.

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD679 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD679 is specified for both dc and ac parameters. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the two read output provides compatibility with 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD679 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%, f_{SAMPLE} = 100 KSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD679J/S Min	AD679J/S Typ	AD679J/S Max	AD679K/T Min	AD679K/T Typ	AD679K/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO							
−0.5 dB Input (Referred to −0 dB Input)	**78**	79		**80**	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)							
@ +25°C		−90	**−84**		−90	**−84**	dB
		0.003	**0.006**		0.003	**0.006**	%
T_{min} to T_{max}		−88	**−82**		−88	**−82**	dB
		0.004	**0.008**		0.004	**0.008**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	**−84**		−90	**−84**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−90	−84		−90	−84	dB
3rd Order Products		−90	−84		−90	−84	dB

NOTES
[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB(9.997 V p-p) input signal unless otherwise noted.
[2]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 100 KSPS. See Definition of Specifications section.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.4**		V
V_{IL}	Low Level Input Voltage			**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = 5 V		**10**	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V		**10**	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V		**10**	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

DC SPECIFICATIONS

(T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10% unless otherwise indicated)

Parameter	AD679J Min	AD679J Typ	AD679J Max	AD679K Min	AD679K Typ	AD679K Max	Units
TEMPERATURE RANGE	0		+70	0		+70	°C
ACCURACY							
Resolution	**14**			**14**			Bits
Integral Linearity Error @ 25°C			±2			±1	LSB
T_{min} to T_{max}			±2			±2	LSB
Differential Linearity	**14**			**14**			Bits
Unipolar Zero Error[1] (@ 25°C)			±8			±4	LSB
Bipolar Zero Error[1] (@ 25°C)			±8			±4	LSB
Gain Error[1,2] (@ 25°C)			±16			±8	LSB
Temperature Drift (Coefficients)							
Unipolar Zero[3]			±8 (10)			±6 (8)	LSB (ppm/°C)
Bipolar Zero[3]			±8 (10)			±6 (8)	LSB (ppm/°C)
Gain[3]			±36 (50)			±24 (33)	LSB (ppm/°C)
Gain[4]			±8 (10)			±6 (8)	LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	μs
Aperture Delay			20			20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	**4.95**		**5.05**	**4.98**		**5.02**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
POWER SUPPLIES (T_{min} to T_{max})							
Power Supply Rejection							
V_{CC} = + 12 V ±5%[6]			±4			±4	LSB
V_{EE} = −12 V ±5%			±4			±4	LSB
V_{DD} = +5 V ±10%			±4			±4	LSB
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**32**		25	**32**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	720		560	720	mW

NOTES
[1]Adjustable to zero. See Figures 5 and 6.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
[6]1.4 V headroom is required between V_{CC} and AIN.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

SPECIFICATIONS

DC SPECIFICATIONS

(T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10% unless otherwise indicated)

Parameter	AD679S Min	AD679S Typ	AD679S Max	AD679T Min	AD679T Typ	AD679T Max	Units
TEMPERATURE RANGE	−55		+125	−55		+125	°C
ACCURACY							
Resolution	**14**			**14**			Bits
Integral Linearity Error (@ 25°C)			±2			±1	LSB
T_{min} to T_{max}			TBD			TBD	LSB
Differential Linearity (@ 25°C)	**14**			**14**			Bits
T_{min} to T_{max}	13			14			Bits
Unipolar Zero Error[1] (@ 25°C)			±8			±4	LSB
Bipolar Zero Error[1] (@ 25°C)			±8			±4	LSB
Gain Error[1,2] (@ 25°C)			±16			±8	LSB
Temperature Drift (Coefficients)							
Unipolar Zero[3]			±16 (10)			±16 (10)	LSB (ppm/°C)
Bipolar Zero[3]			±16 (10)			±16 (10)	LSB (ppm/°C)
Gain[3]			±82 (50)			±82 (50)	LSB (ppm/°C)
Gain[4]			±16 (10)			±16 (10)	LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	µs
Aperture Delay	5		20	5		20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	**4.95**		**5.05**	**4.98**		**5.02**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
POWER SUPPLIES (T_{min} to T_{max})							
Power Supply Rejection							
V_{CC} = +12 V ±5%[6]			±4			±4	LSB
V_{EE} = −12 V ±5%			±4			±4	LSB
V_{DD} = +5 V ±10%			±4			±4	LSB
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**32**		25	**32**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	720		560	720	mW

NOTES
[1]Adjustable to zero. See Figures 5 and 6.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
[6]1.4 V headroom is required between V_{CC} and AIN.

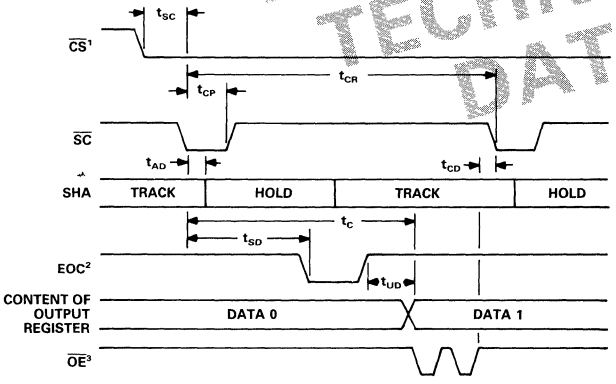
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at −55°C, +25°C, and +125°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter	Symbol	Min	Max	Units
$\overline{SC}$ Delay	t_{SC}	50		ns
Conversion Rate[1]	t_{CR}		10	µs
Convert Pulse Width	t_{CP}	150		ns
Aperture Delay	t_{AD}	5	20	ns
Conversion Time	t_C		**8.5**	µs
Status Delay	t_{SD}	0	400	ns
Access Time[2]	t_{BA}		**100**	ns
Float Delay[3]	t_{FD}	10	**80**	ns
Update Delay	t_{UD}		200	ns
Format Setup	t_{FS}	60		ns
$\overline{OE}$ Delay	t_{OE}	20		ns
Read Pulse Width	t_{RP}	150		ns
Conversion Delay	t_{CD}	400		ns
$\overline{EOCEN}$ Delay	t_{EO}	20		ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}$/EOCEN (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4; C_{OUT} = 100 pF.
[3]Measured from the rising edge of $\overline{OE}$/EOCEN (2.0 V) to the time at which the output voltage changes by 0.5 . See Figure 4; C_{OUT} = 10 pF.
Specifications subject to change without notice.



NOTES
[1]IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2]$\overline{EOCEN}$ = LOW. IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT. SEE CONVERSION TRUTH TABLE.
[3]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

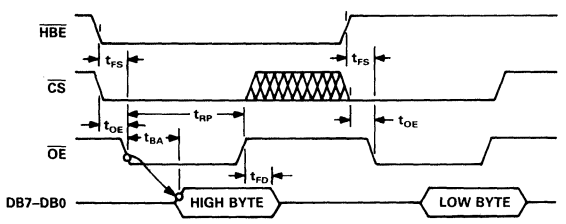
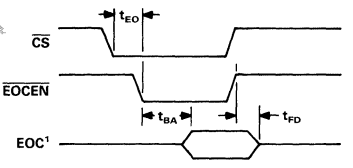


Figure 2. Output Timing



NOTE
[1]EOC IS A THREE-STATE OUTPUT IN SYNCHRONOUS MODE AND AN OPEN DRAIN OUTPUT IN ASYNCHRONOUS. ACCESS (t_{BA}) AND FLOAT (t_{FD}) TIMING SPECIFICATIONS DO NOT APPLY IN ASYNCHRONOUS MODE WHERE THEY ARE A FUNCTION THE TIME CONSTANT FORMED BY THE 10 pF OUTPUT CAPACITANCE AND THE PULL-UP RESISTOR.

Figure 3. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

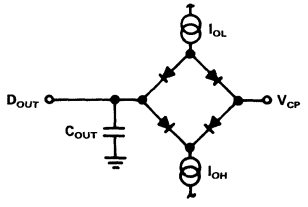


Figure 4. Load Circuit for Bus Timing Specifications

CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both Chip Select ($\overline{CS}$) and Start Convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW t_{SC} before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ low, regardless of the state of $\overline{CS}$.

Before a conversion is started, End Of Convert (EOC) is HIGH and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample.

In track mode, the sample-hold will settle to ±0.003% (14 bits) in 1.5 μs maximum. The acquisition time does not affect the throughput rate as the AD679 goes back into track mode more than 2 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW.

When the conversion is finished, EOC goes HIGH and the result is loaded into the output register after a period of time t_{UD}. Bringing $\overline{OE}$ LOW t_{OE} after $\overline{CS}$ goes LOW makes the output register contents available on the output data bits (DB7–DB0). A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued. This allows internal logic states to reset and guarantees minimum aperture jitter for the next conversion.

If $\overline{SC}$ is held LOW, conversions will occur continuously. EOC will go HIGH for approximately 1.5 μs between conversions.

START CONVERSION TRUTH TABLE

	INPUTS			
	SYNC	$\overline{CS}$	$\overline{SC}$	STATUS
Synchronous Mode	1	1	X	No Conversion
	1	0	↓	Start Conversion
	1	↓	0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion
Asynchronous Mode	0	X	1	No Conversion
	0	X	↓	Start Conversion
	0	X	0	Continuous Conversion

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay low for t = t_{CP}.

14-BIT MODE CODING FORMAT (1 LSB = 0.61 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}	Output Code	V_{IN}	Output Code
0	000 . . . 0	−5.00000 V	100 . . . 0
5.00000 V	100 . . . 0	−0.00061 V	111 . . . 1
9.99939 V	111 . . . 1	0	000 . . . 0
		+2.50000 V	010 . . . 0
		+4.99939 V	011 . . . 1

END OF CONVERT

In asynchronous mode, End of Convert (EOC) is an open drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by End of Convert ENable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output which is enabled by $\overline{EOCEN}$ and $\overline{CS}$. See Conversion Status Truth Table. Access (t_{BA}) and float (t_{FD}) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the external load capacitance and the pull-up resistor.

OUTPUT ENABLE OPERATION

The data bits (DB7–DB0) are three-state outputs that are enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. Output Enable ($\overline{OE}$) must be toggled to update the output register.

The output is read as a 16-bit word, with the high byte read first, followed by the low byte. High Byte Enable ($\overline{HBE}$) controls the output sequence. The 14-bit result is left justified within the 16-bit field.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REFOUT), output coding is twos-complement binary.

POWER-UP

A conversion sequence, consisting of one $\overline{SC}$ instruction, is required after power-up to reset internal logic.

CONVERSION STATUS TRUTH TABLE

	INPUTS			OUTPUT	
	SYNC	$\overline{CS}$	$\overline{EOCEN}$	EOC	STATUS
Synchronous Mode	1	0	0	0	Converting
	1	0	0	1	Not Converting
	1	1	X	High Z	Either
	1	X	1	High Z	Either
Asynchronous Mode*	0	X	0	0	Converting
	0	X	0	High Z	Not Converting
	0	X	1	High Z	Either

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.

*EOC requires a pull-up resistor in asynchronous mode.

OUTPUT ENABLE TRUTH TABLE

	INPUTS		OUTPUTS							
	$\overline{HBE}$	($\overline{CS}$ U $\overline{OE}$)	DB7 . . . DB0							
	X	1	← High Z →							
Unipolar or Bipolar	0	↓	a	b	c	d	e	f	g	h
	1	↓	i	j	k	l	m	n	0	0

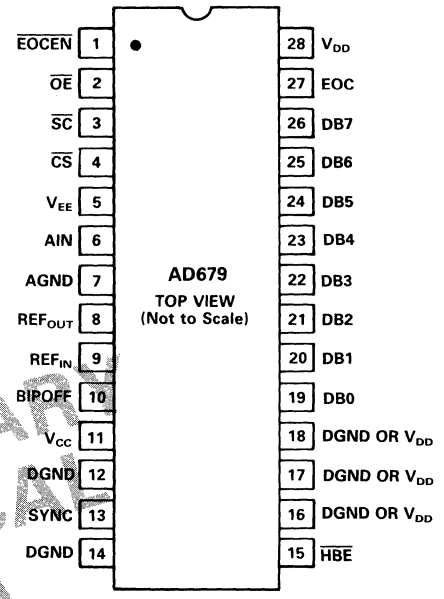
NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
U = Logical OR.
a = MSB.
n = LSB.
↓ = HIGH to LOW transition. Must stay low for t = t_{RP}.
Data coding is binary for Unipolar Mode and 2s complement binary for Bipolar Mode.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	−12	+12	V
REF_{IN}	V_{EE}	0	V_{CC}	V
REF_{IN}	V_{CC}	V_{EE}	0	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature				
J and K Grades		0	+70	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



AD679 ORDERING GUIDE[1]

Temperature Range and Package Options[2]

Plastic DIP (N-28A) 0 to +70°C	Ceramic DIP (D-28A) 0 to+70°C	Ceramic DIP (D-28A) −55°C to +125°C	Integral Nonlinearity	S/N+D[3]
AD679JN	AD679JD	AD679SD	±2 LSB	79 dB
AD679KN	AD679KD	AD679TD	±1 LSB	81 dB

NOTES
[1]For single cycle read (14 bits) interface to 16-bit buses, see AD779.
[2]See Section 14 for package outline information.
[3]Typical at 10kHz, −0.5dB input.

ESD SENSITIVITY

The AD679 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD679 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

AD679 PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground. This is the ground return for AIN only.
AIN	6	AI	Analog Signal Input.
BIPOFF	10	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} for ±5 V input bipolar mode and twos complement binary output coding.
$\overline{CS}$	4	DI	Chip Select. Active LOW.
DGND	12, 14	P	Digital Ground
DB7–DB0	26–19	DO	Data Bits. These pins provide all 14 bits in two bytes (8+6 bits). Active HIGH.
EOC	27	DO	End of Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. In asynchronous mode, EOC is an open drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	DI	End of Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$	15	DI	High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte (corresponding to the most recently read high byte).
$\overline{OE}$	2	DI	Output Enable. A down-going transition on $\overline{OE}$ enables DB7–DB0. Gated with $\overline{CS}$. Active LOW.
REF_{IN}	9	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	AO	+5 V Reference Output. Tied to REF_{IN} for normal operation.
$\overline{SC}$	3	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	DI	SYNC Control. If tied to V_{DD} (synchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open drain output. EOC requires an external 3 kΩ pull-up resistor in asynchronous mode.
V_{CC}	11	P	+12 V Analog Power.
V_{EE}	5	P	−12 V Analog Power.
V_{DD}	28	P	+5 V Digital Power.
—	16–18	U	These pins are unused and should be connected to DGND or V_{DD}.

Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers.
P = Power.
U = Unused.

Definition of Specifications

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a 0-dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD679 has been designed to optimize input bandwidth, allowing it to undersample input signals with frequencies significantly above the converter's Nyquist frequency. If the input signal is suitably band-limited, the spectral content of the input signal can be recovered.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL LINEARITY (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential linearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

This specification is 14 bits for the AD679J, K and T grades, which guarantees that all 16,384 codes are present. The AD679S grade specifies 13 bits NMC, which means that missing codes do not occur adjacent to each other.

INTEGRAL LINEARITY ERROR (INL)
The ideal transfer function for a linear ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral linearity error is the worst case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

Note that the linearity error is not user adjustable.

POWER SUPPLY REJECTION
Variations in power supply will affect the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in the full scale transition point due to a change in power supply voltage from the nominal value.

TEMPERATURE COEFFICIENT
This is the maximum change in the parameter from the initial value (@+25°C) to the value at T_{min} or T_{max}.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (11 1111 1111 1111 to 00 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9991 volts for a 0–10 V range, 4.9991 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

Application Information – AD679

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD679 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 300 Ω. The 10 V p-p full scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

The AD679 is factory trimmed to minimize offset, gain and linearity errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical, even these components can be eliminated.

In some applications, offset and gain errors need to be more precisely trimmed. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 5. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the AD679 accuracy limits are sufficient for application. If the pins are shorted together, the additional offset and gain errors will be approximately 80 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−0.305 mV for a ±5 V range) and adjust R1 until the major carry transition is located (11 1111 1111 1111 to 00 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9997 V for a ±5 V range) and adjust R2 to give the last positive transition (01 1111 1111 1110 to 01 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9997 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (10 0000 0000 0000 to 10 000 000 0001). Then perform the gain error trim as outlined above.

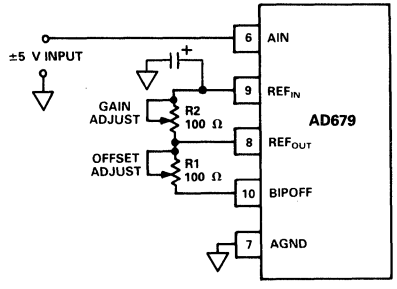


Figure 5. Bipolar Input Connections with Gain and Offset Trims

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 6. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code will be centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 00 0000 0000 0000 to 00 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (0.305 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 0.305 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9997 V for a 10 V range) and adjust R2 until the last transition is located (11 1111 1111 1110 to 11 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

REFERENCE DECOUPLING

It is recommended that a 10 μF tantalum capacitor be connected between REF_{IN} (Pin 9) and ground. This has the effect of improving the S/N+D ratio through filtering possible broad-band noise contributions from the voltage reference.

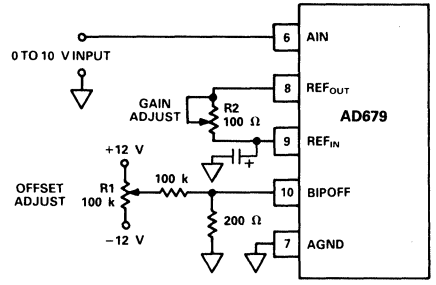


Figure 6. Unipolar Input Connections with Gain and Offset Trims

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 1 LSB at the 14 bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD679 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB7–DB0 and EOC.

SUPPLY DECOUPLING

The AD679 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and analog ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD679, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD679 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD679 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD679. If multiple AD679s are used or the AD679 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

INTERFACING THE AD679 TO MICROPROCESSORS

The I/O capabilities of the AD679 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD679 interface configurations.

AD679 TO TMS320C25

In Figure 7 the AD679 is mapped into the TMS320C25 I/O space. AD679 conversions are initiated by issuing an OUT instruction to Port 1. EOC status and the conversion result are read in with an IN instruction to Port 1. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 1 and $\overline{MSC}$. Address line A0 provides $\overline{HBE}$ decoding to select between the high and low bytes of data. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD679 read instruction.

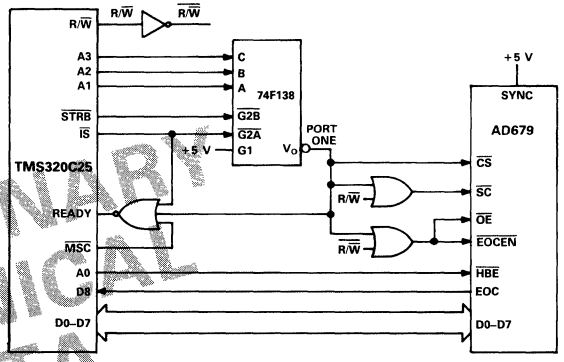


Figure 7. AD679 to TMS320C25 Interface

AD679 TO 80186

Figure 8 shows the AD679 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD679 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD679 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD679 EOC signal generates a DMA

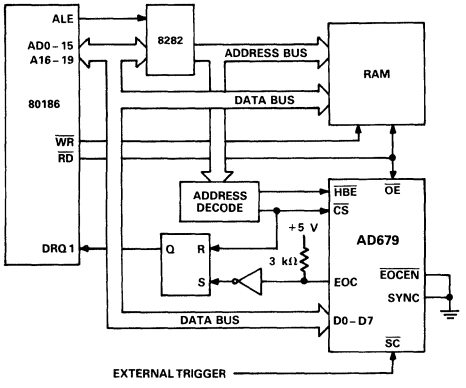


Figure 8. AD679 to 80186 DMA Interface

request to Channel 1 (DRQ1). The subsequent DMA READ sequences the high and low byte AD679 data and resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

AD679 TO Z80

The AD679 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 9 illustrates an I/O configuration, where the AD679 occupies several port addresses to allow separate polling of the EOC status and reading of the data. The lower address bit, A0, is used to select the high and low order bytes of the result.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD679 to be used with Z80 processors having clock speeds up to 8 MHz.

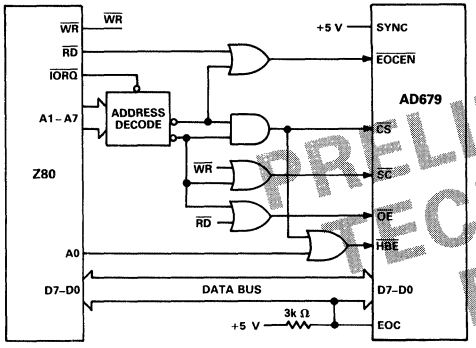


Figure 9. AD679 to Z80 Interface

AD679 TO ANALOG DEVICES' ADSP-2100A

Figure 10 demonstrates the AD679 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD679 data memory interface with a two hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD679 is asserted at the end of each conversion and creates a high priority interrupt to the processor through $\overline{IRQ3}$. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts $\overline{HBE}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latches, is used to force the ADSP-2100A into a two-cycle wait state by generating DMACK. The read operation is thus started and completed within three processor cycles (240 ns). $\overline{HBE}$ is released during "high byte read." This allows the processor to read the lower byte of data as soon as "high byte read" is complete. Low byte read is executed in a similar manner and is completed during the next 240 ns.,

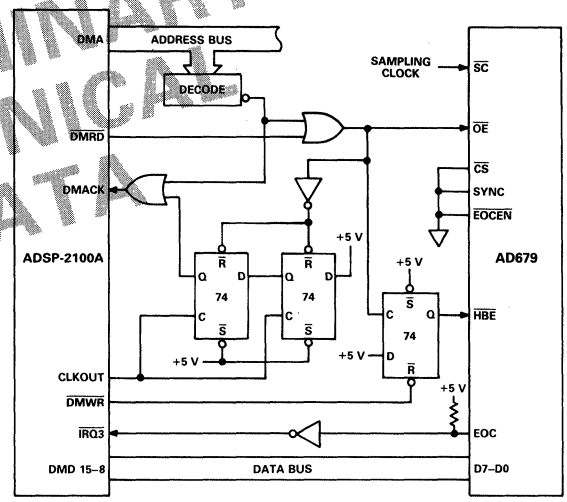


Figure 10. AD679 to ADSP-2100A Interface

ANALOG DEVICES

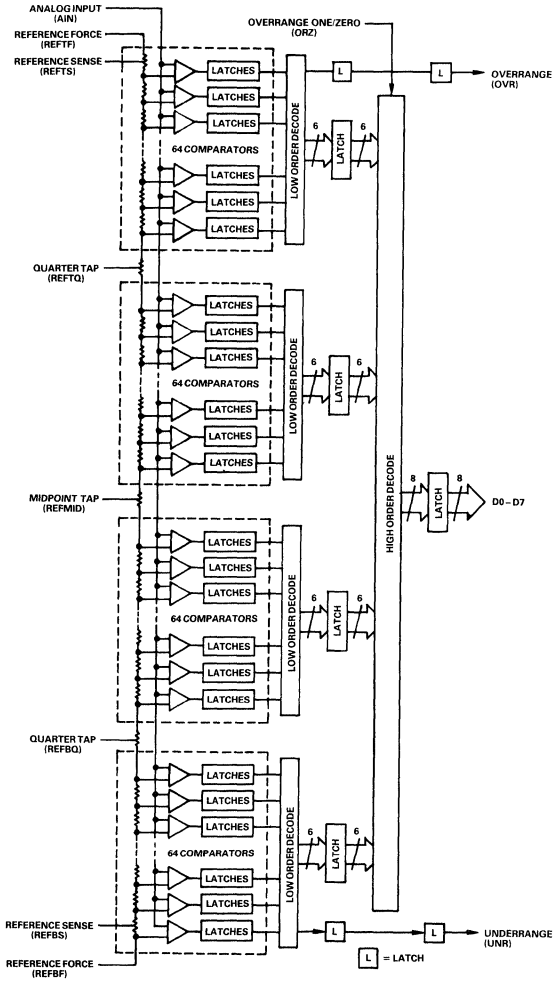
200 MSPS Wideband 8-Bit A/D Converter

AD770

FEATURES

250MHz Full Power Bandwidth
200 MSPS Guaranteed Conversion Rate
19pF typ Input Capacitance
Unipolar and Bipolar Input Range
+5V/−5.2V Power Supplies
Overflow and Underflow Signals

AD770 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD770 is an 8-bit analog-to-digital converter that is designed for high-speed digitization of wide-bandwidth signals. It uses an advanced VLSI bipolar process and a proprietary design to achieve a combination of sampling rate and signal bandwidth previously unavailable in flash ADCs.

The AD770 incorporates 257 high speed comparators that are optimized for low input capacitance and wide bandwidth, unaffected by temperature or signal amplitude. The multistage comparator design reduces the probability of errors due to metastable states or insufficient gain.

The decoding logic further reduces errors by using a two-stage error-correcting architecture to virtually eliminate "sparkle codes." Inputs and outputs are ECL compatible. Output format controls allow stacking of two devices for 9-bit resolution. Overflow and underflow output signals are provided.

The AD770 can operate with unipolar and bipolar signal ranges up to 4V p-p. End-point reference Force and Sense connections are provided to preserve high accuracy and minimize temperature drift. Midpoint and quarter-point reference taps are also provided to allow linearity or transfer function corrections.

The AD770 is available in three grades. The JD and KD grades are specified for operation over the 0 to +70°C temperature range, while the SD grade is specified for the −55°C to +125°C temperature range. All grades are packaged in a 40-pin ceramic DIP. Other package options are available on request; please contact the factory.

PRODUCT HIGHLIGHTS

1. **Performance:** The AD770 is specified for operation at 200 MSPS. Full power bandwidth is 250MHz; small signal bandwidth is 400MHz.
2. **Ease of Use:** The AD770 input has a typical capacitance of 19pF, simplifying input buffering requirements. Bipolar and unipolar input signals can be converted without offsetting. Differential or single-ended clock inputs can be accommodated by pin-strapping.
3. **Features:** Taps are provided at mid- and quarter-scale points of the reference ladder to permit linearity trimming or piecewise-linear transfer function modification. Overflow and underflow signals are also provided. These can be wire-or'd to provide an indication that the input signal has exceeded the range of the converter.

DC SPECIFICATIONS (typical at +25°C, V_{CC} = 5.0V, V_{EE} = −5.2V, V_{REFTS} = +1.0V, V_{REFBS} = −1.0V, unless otherwise specified)

Parameter	Conditions	AD770J/S Min	AD770J/S Typ	AD770J/S Max	AD770K Min	AD770K Typ	AD770K Max	Units
TEMPERATURE RANGE	AD770J, AD770K	0		+70	0		+70	°C
	AD770S	−55		+125				°C
RESOLUTION		8			8			Bits
DC ACCURACY								
Linearity Error	+25°C	−1		+1	−0.75		+0.75	LSB
	T_{min}–T_{max}	−1.25		+1.25	−1		+1	LSB
Differential Linearity	+25°C	−0.9		+0.9	−0.75		+0.75	LSB
	T_{min}–T_{max}	−1.25		+1.25	−0.9		+0.9	LSB
Absolute Accuracy	+25°C	−1.75		+1.75	−1		+1	LSB
	T_{min}–T_{max}	−2		+2	−1.25		+1.25	LSB
REFERENCE LADDER								
Ladder Resistance		160	200	260	160	200	260	Ω
Ladder TC			0.34			0.34		%/°C
Top Force-Sense Offset	T_{min}–T_{max}		3	5		3	5	LSB
Bottom Force-Sense Offset	T_{min}–T_{max}		3	5		3	5	LSB
ANALOG INPUT								
Input Current	V_{IN} = −1V to +1V			300			300	μA
	T_{min}–T_{max}			500			500	μA
Input Capacitance		17	19	22	17	19	22	pF
DIGITAL INPUTS	T_{min}–T_{max}							
Logic HIGH (V_{IH})		−1.0		−0.7	−1.0		−0.7	V
Logic LOW (V_{IL})		−1.9		−1.6	−1.9		−1.6	V
Logic HIGH Current (I_{IH})				200			200	μA
Logic LOW Current (I_{IL})				200			200	μA
Input Capacitance			3			3		pF
DIGITAL OUTPUTS								
Logic HIGH (V_{OH})	100Ω Load to −2V	−1.0		−0.7	−1.0		−0.7	V
Logic LOW (V_{OL})	100Ω Load to −2V	−1.9		−1.6	−1.9		−1.6	V
V_{BB}			−1.2			−1.2		V
POWER SUPPLIES								
V_{CC}		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{EE}		−5.46	−5.2	−4.9	−5.46	−5.2	−4.9	V
I_{CC} (Analog)			210	269		210	269	mA
I_{CC} (Digital)			62	78		62	78	mA
I_{EE} (Analog)			54	69		54	69	mA
I_{EE} (Digital)			69	88		69	88	mA
Power Consumption			2000	2550		2000	2550	mW

Specifications subject to change without notice.

AC SPECIFICATIONS (typical +25°C, V_{CC} = 5.0V, V_{EE} = −5.2V, unless otherwise noted)

Parameter	Conditions		AD770J/S Min	AD770J/S Typ	AD770J/S Max	AD770K Min	AD770K Typ	AD770K Max	Units
TIMING	T_{min}–T_{max}, 100Ω Load to −2V								
Max Conversion Rate			**200**			**200**			MSPS
Aperture Delay				340			340		ps
Aperture Jitter				3			3		ps rms
Pipeline Delay			1.5		1.5	1.5		1.5	Clock Cycles
Output Delay			**2**		**6**	**2**		**6**	ns
Output Rise				1			1		ns
Output Fall				1			1		ns
Output Skew				1.4	**2.35**		1.4	**2.35**	ns
DYNAMIC PERFORMANCE (@200 MSPS)	F_{IN} (MHz)	Full Scale A_{IN} (Volts)							
Full-Power Bandwidth		±1		250			250		MHz
Small-Signal Bandwidth		±1		400			400		MHz
Harmonic Distortion[1]	1	±1		50			53		dB
	10	±1		43.5			45.5		dB
	50	±1		35.5			36		dB
	100	±1		25.5			26		dB
	1	±0.5		49			52		dB
	10	±0.5		42			43.5		dB
	50	±0.5		38			39		dB
	100	±0.5		31.5			32		dB
Signal-to-Noise Ratio[1]	1	±1		44.0 (7.0)			44.5 (7.1)		dB (ENOB)
	10	±1		41.5 (6.6)			42.0 (6.7)		dB (ENOB)
	50	±1		34.0 (5.4)			34.5 (5.4)		dB (ENOB)
	100	±1		25.0 (3.9)			25.5 (3.9)		dB (ENOB)
	1	±0.5		40.5 (6.4)			41.0 (6.5)		dB (ENOB)
	10	±0.5		39.0 (6.2)			39.5 (6.3)		dB (ENOB)
	50	±0.5		35.5 (5.6)			35.5 (5.6)		dB (ENOB)
	100	±0.5		30.0 (4.7)			31.0 (4.9)		dB (ENOB)

NOTES
[1]Signal-to-Noise Ratio includes harmonics in the noise factor.
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

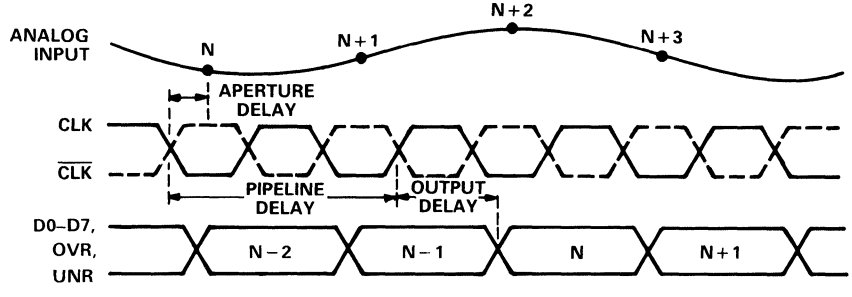
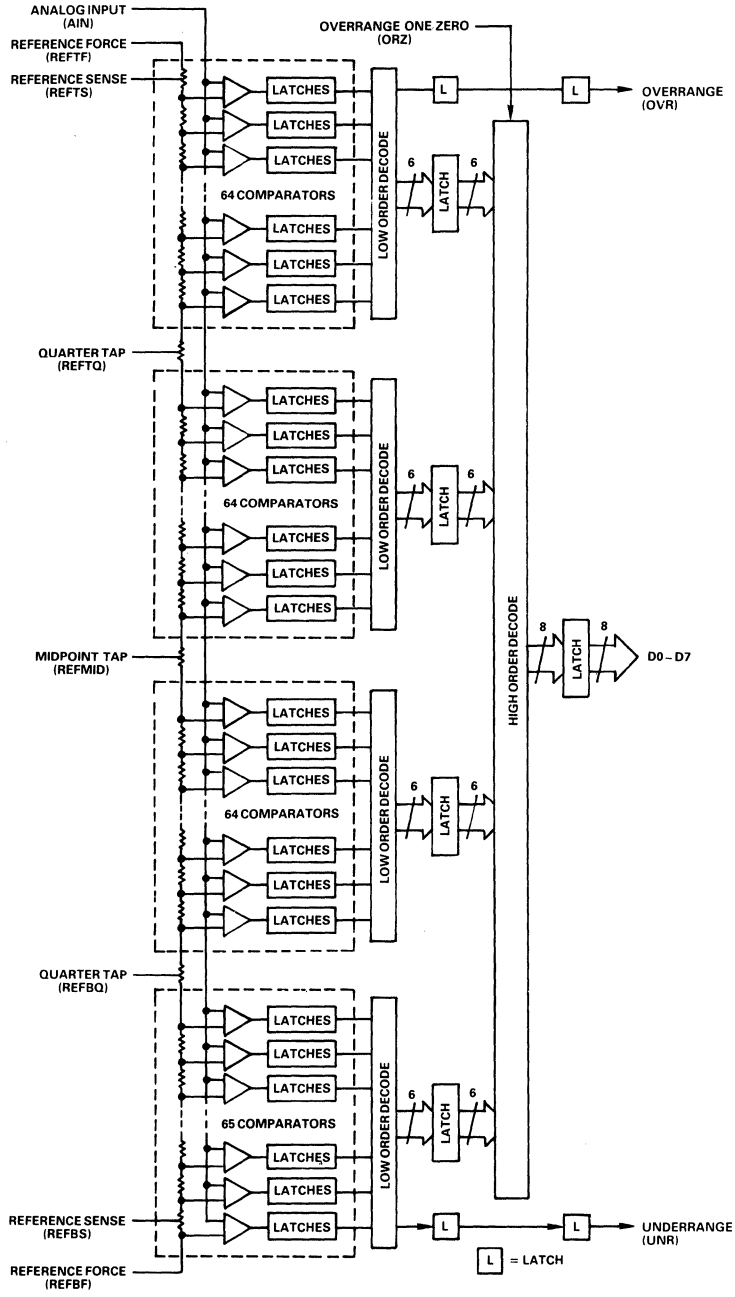
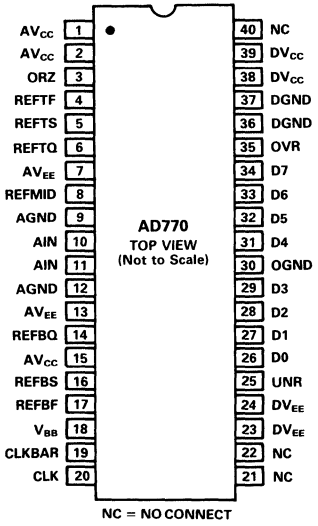


Figure 1. AD770 Timing Diagram



AD770 Block Diagram



AD770 Pinout (40-Pin DIP)

AD770 PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
AGND	9, 12	P	Analog Ground
AIN	10, 11	AI	Analog Input
AV_{CC}	1, 2, 15	P	+5V Analog Power
AV_{EE}	7, 13	P	−5.2V Analog Power
CLK	20	DI	Clock Input
CLKBAR	19	DI	Complementary Clock Input
DGND	36, 37	P	Digital Ground
DV_{CC}	38, 39	P	+5V Digital Power
DV_{EE}	23, 24	P	−5.2V Digital Power
D0	26	DO	Data Bit Output (LSB)
D1	27	DO	Data Bit Output
D2	28	DO	Data Bit Output
D3	29	DO	Data Bit Output
D4	31	DO	Data Bit Output
D5	32	DO	Data Bit Output
D6	33	DO	Data Bit Output
D7	34	DO	Data Bit Output (MSB)
OGND	30	P	Digital Output Ground (collectors of output transistors.)
ORZ	3	DI	Overrange Zero. Sets the Polarity of the Data Bits for Overrange Condition. If ORZ = HIGH, D0–D7 are LOW for Overrange Conditions.
OVR	35	DO	Overrange Output. Indicates that AIN> (REFTS − 0.5LSB).
REFBF	17	AI	Negative Reference Force
REFBQ	14	AI	Negative Reference Quarter Point
REFBS	16	AO	Negative Reference Sense
REFMID	8	AI	Reference Midpoint
REFTF	4	AI	Positive Reference Force
REFTQ	6	AI	Positive Reference Quarter Point
REFTS	5	AO	Positive Reference Sense
UNR	25	DO	Underrange Output. UNR = HIGH when AIN<(REFBS − 0.5LSB).
V_{BB}	18	DO	ECL Threshold Output for Clocks

TYPE: AI = Analog Input
AO = Analog Output
DI = Digital Input
DO = Digital Output
P = Power

EVALUATION BOARD

The ADEB770 Evaluation Board allows the designer to easily evaluate the performance of the AD770. The ADEB770 includes a pin-socketed AD770, an input signal buffer and an adjustable reference generator. The input buffer can be bypassed for maximum versatility.

On the output side, latched and buffered digital data is available at the output connector along with an output clock. Decimation hardware allows output data to be undersampled by factors of 16 through 2, allowing the user to interface the board to commonly available logic analyzers.

A reconstructed analog output is also provided by an on-board D/A converter.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect to	Min	Max	Units
AV_{CC}	AGND	−0.3	5.5	V
DV_{CC}	DGND	−0.3	5.5	V
AV_{EE}	AGND	−5.72	0.3	V
DV_{EE}	DGND	−5.72	0.3	V
AV_{CC}	DV_{CC}	−0.5	0.5	V
AV_{EE}	DV_{EE}	−0.5	0.5	V
AIN	AGND	−3	+2.25	V
AIN	REFTF, REFBF	−4.3	4.3	V
CLK, CLKBAR, ORZ	AGND	−4.0	0	V
REFTF, REFBF	AGND	−3	+2.25	V
AGND	DGND	−0.5	0.5	V
CLK	CLKBAR	−4.5	4.5	V
I_{AIN}			110	mA
I_{REFTF}, I_{REFBF}			30	mA
I_{REFTS}, I_{REFBS}			3	mA
I_{REFMID}, I_{REFTQ}, I_{REFBQ}			30	mA
I_{BB}			4	mA
I_{CLK}, $I_{CLK\,BAR}$, I_{ORZ} |			1	mA
$I_{D0\text{-}D7}$, I_{OVR}, I_{UNR}			40	mA
Junction Temperature			175	°C
Power Dissipation (+25°C)			3	W
Storage Temperature		−65	+150	°C
Thermal Resistance				
θ_{JA} (Still Air) (typ)			36	°C/W
θ_{JC} (typ)			10	°C/W

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Package	Temperature Range °C	Linearity Error Max @ +25°C	Package Options*
AD770JD	40-Pin Ceramic DIP	0 to +70	±1	D-40
AD770KD	40-Pin Ceramic DIP	0 to +70	±3/4	D-40
AD770SD	40-Pin Ceramic DIP	−55 to +125	±1	D-40
ADEB770-1	Evaluation Board for AD770		±1	–
ADEB770-2	Evaluation Board for AD770		±3/4	–

*See Section 14 for package outline information.

DEFINITION OF SPECIFICATIONS

Linearity Error
Linearity Error is the deviation of the transfer function from a reference line. For the AD770, the linearity error is measured from the center of each code to the best-fit straight line.

Differential Linearity
In an ideal ADC, the code transitions are exactly 1LSB apart. The Differential Linearity is the deviation of the transition spacing from the ideal value. A Differential Linearity spec of less than 1LSB signifies that there are no missing output codes over the entire input range.

Absolute Accuracy
The Absolute Accuracy is the deviation of the center-point of each code from a straight line drawn between the reference sense points (REFTS, REFBS).

Force-Sense Offset
The Force-Sense Offset is the difference between the force and sense pin voltages divided by the input range. This offset will cause a corresponding offset error if the full-scale range is defined w.r.t. the reference force lines rather than with respect to the reference sense lines.

Aperture Delay
The delay between the falling edge of CLK and the time at which AIN is sampled.

Aperture Jitter
The sample-to-sample variation in aperture delay.

Pipeline Delay
The delay from the falling edge of CLK that samples the input to the rising edge of CLK that outputs the corresponding digital code.

Output Delay
The delay between the rising edge of CLK and the time when the output bits reach the logic threshold value for bits D0 to D7 and OVR.

Output Skew
The bit-to-bit variation in output delay for bits D0 to D7 and OVR.

Full-Power Bandwidth
The input frequency at which the amplitude of the reconstructed output signal is reduced by 3dB for a full-scale input.

Total Harmonic Distortion (THD)
The rms sum of the first six harmonic components divided by the output signal amplitude. For frequencies above the Nyquist frequency, the aliased components are used.

Signal-to-Noise Ratio (SNR)
The ratio of the signal amplitude to the rms sum of all other spectral components, including harmonics but excluding dc. SNR is expressed in dB and in Effective Number Of Bits (ENOB). These two notations are related by the following formula for full-scale inputs:

$$ENOB = (SNR - 1.8)/6.02$$

(For REFTS = +1.000V, REFBS = −1.000V)

Input			Output		
$A_{IN}>$	$A_{IN}<$	ORZ	D7 . . . . . D0	UNR	OVR
0.996V		0	1 1 1 1 1 1 1 1	0	1
0.996V		1	0 0 0 0 0 0 0 0	0	1
0.988V	0.996V	X	1 1 1 1 1 1 1 1	0	0
0.980V	0.988V	X	1 1 1 1 1 1 1 0	0	0
0.973V	0.980V	X	1 1 1 1 1 1 0 1	0	0
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
−0.004V	0.004V	X	1 0 0 0 0 0 0 0	0	0
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
−0.998V	0.980V	X	0 0 0 0 0 0 1 0	0	0
−0.996V	0.998V	X	0 0 0 0 0 0 0 1	0	0
−1.004	−0.996V	X	0 0 0 0 0 0 0 0	0	0
	−1.004V	X	0 0 0 0 0 0 0 0	1	0

X = Don't care

Table I. AD770 Truth Table

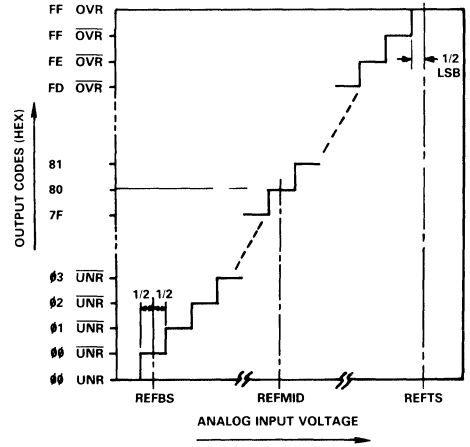


Figure 2. AD770 Transfer Function

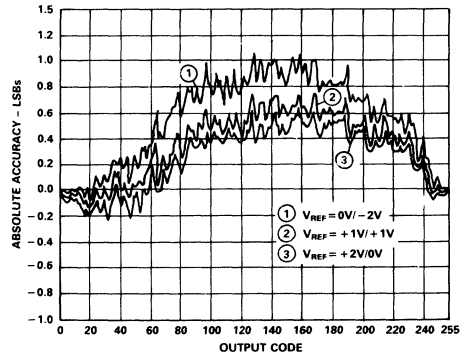


Figure 3. Typical Absolute Accuracy vs. Output Code for Various Range Offsets

Dynamic Performance

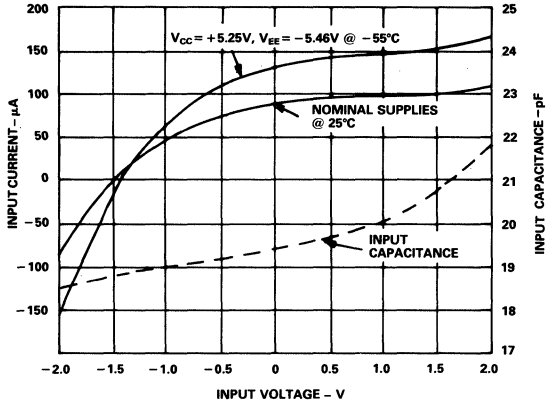


Figure 4. Input Current and Input Capacitance vs. Input Voltage

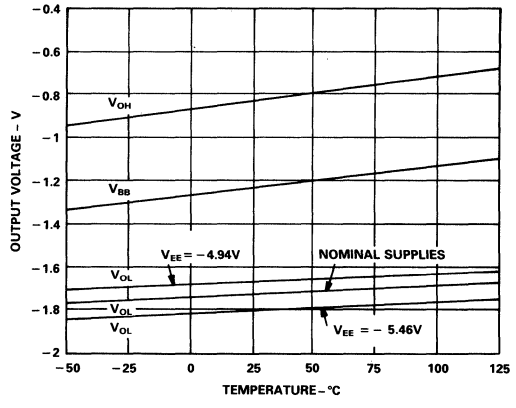


Figure 5. Logic Levels vs. Temperature

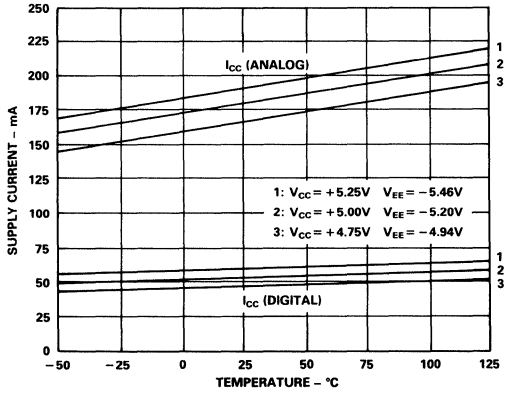


Figure 6. I_{CC} vs. Temperature

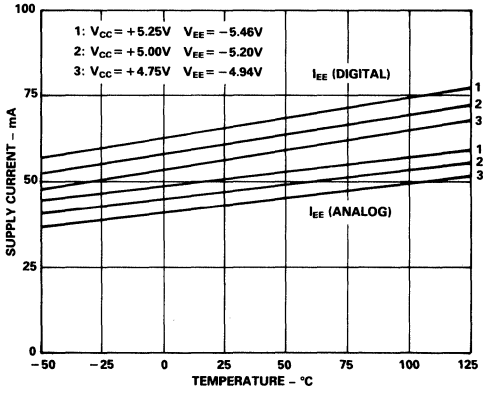


Figure 7. I_{EE} vs. Temperature

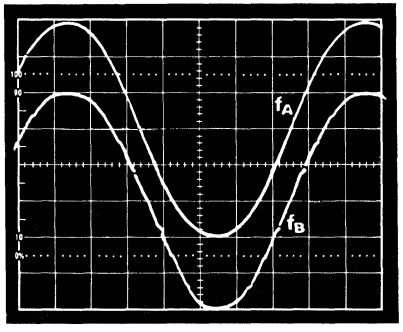


Figure 8. Reconstructed Output of AD770 Decimated by 1:32 @ 200MSPS

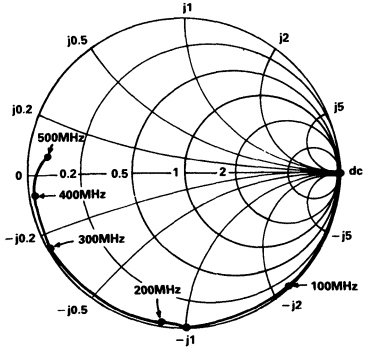


Figure 9. Smith Chart: Input Impedance Normalized to 50Ω vs. Input Frequency

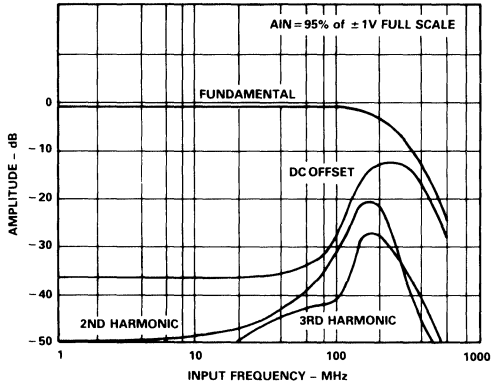


Figure 10. Harmonic Distortion vs. Input Frequency @ 200MSPS: Full Power

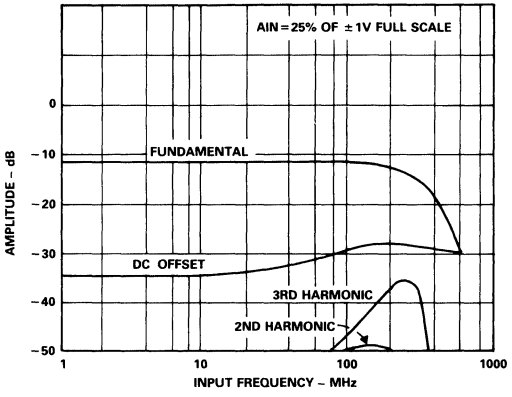


Figure 11. Harmonic Distortion vs. Input Frequency @ 200 MSPS: Small Signal

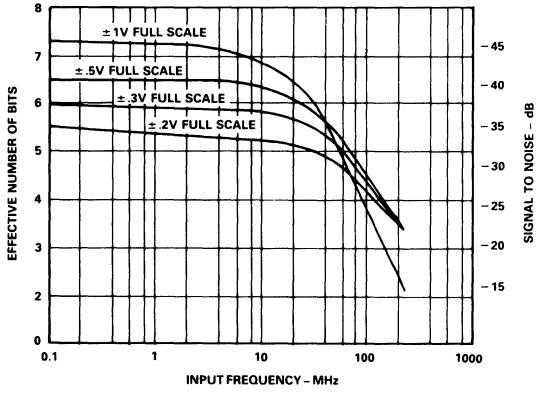


Figure 12. SNR vs. Input Frequency in ENOB and dB

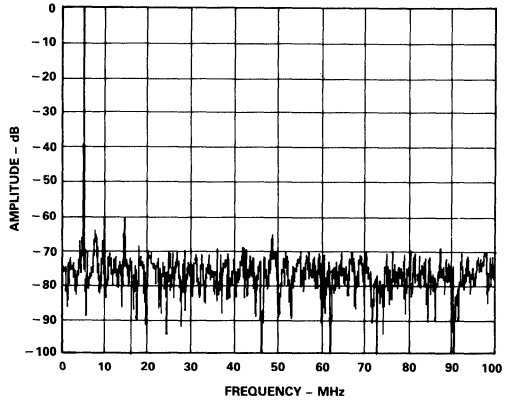


Figure 13. 1024pt FFT of AD770 Output @ 200 MSPS. F_{IN} = 5MHz at ±1V Full Scale

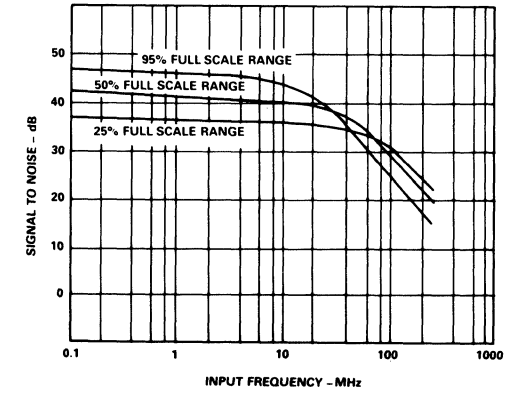


Figure 14. SNR vs. Input Frequency at ±1V F.S. Input

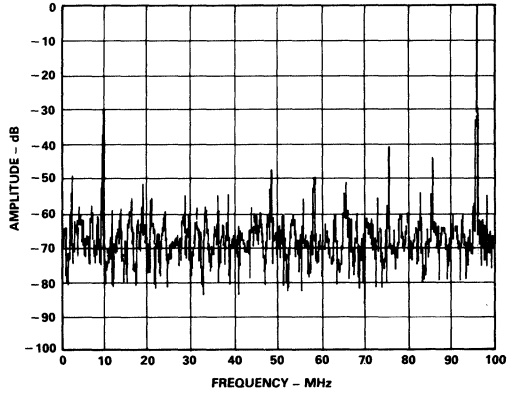


Figure 15. 1024pt FFT of AD770 Output @ 200 MSPS. F_{IN} = 95MHz at ±1V F.S.

GROUNDING AND DECOUPLING

The user is advised to provide separate, low impedance analog and digital ground planes and tie them together at one place on the board, preferably at, or as near to, the ADC as possible.

The dominant consideration in the selection of bypass capacitors for the AD770 is minimization of series resistance and inductance. Ceramic and film-type capacitors generally feature lower series inductance than tantalum or electrolytic types. The capacitors should be installed on the board with the shortest possible lead lengths. Chip capacitors are optimal in this respect. As shown in Figure 18, the analog ground plane provides bypassing for the analog power supplies (AV_{CC}, AV_{EE}) as well as for the reference top, bottom, mid and quarter voltages. The digital ground plane should be used to bypass the digital supplies (DV_{CC}, DV_{EE}).

To prevent output ringing, a ferrite bead in series with DGND Pins 36 and 37 is recommended. Output lines should be single fanout, properly terminated 100Ω striplines for best results.

DRIVING THE AD770

The AD770 can be driven directly from most signal sources. The termination of the signal source, however, will affect the input bandwidth. Two possibilities are shown in Figure 16.

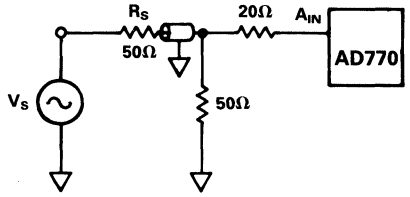


Figure 16a. 50Ω Shunt Termination

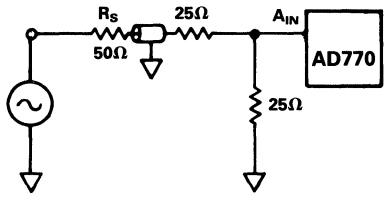
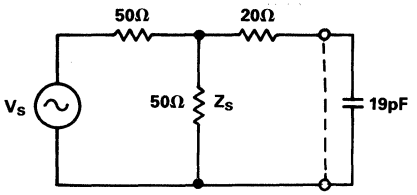


Figure 16b. 50Ω Termination (−6dB) Employing 25Ω Series and 25Ω Shunt Resistors

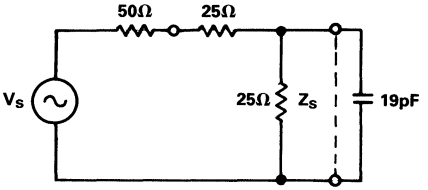
Both terminations result in 50Ω to ground; however the network of Figure 16b provides a lower impedance to the AD770 over frequency as well as a higher −3dB point at the device. The trade-off is that Figure 16b attenuates the signal source by a factor of two (−6dB). These effects may be illustrated by modeling the input to the AD770 as a 19pF capacitor and analyzing the two termination networks as shown in Figure 17.

The −6dB network requires an input signal with twice the amplitude of the simple 50Ω shunt termination, but the benefits can be easily justified. The termination impedance reaches a high frequency value of 25Ω, versus 14Ω for the standard termination network. Another advantage is that the half-power bandwidth is more than twice that of the standard 50Ω shunt network.



1. **IMPEDANCE SEEN BY AD770:**
   $Z_S = 20\Omega + (50 \| 50) = 45\Omega$
2. **−3dB POINT AT AD770:**
   $f_o = (2\pi 45\Omega \cdot 19pF)^{-1}$
   $f_o = 186MHz$

Figure 17a. Network for 50Ω Shunt Termination



1. **IMPEDANCE SEEN BY AD770:**
   $Z_S = 25\Omega \| 25\Omega + 50\Omega) = 19\Omega$
2. **−3dB POINT AT AD770:**
   $f_o = (2\pi 19\Omega \cdot 19pF)^{-1}$
   $f_o = 441MHz$

Figure 17b. Network for 25Ω Series and 25Ω Shunt Termination.

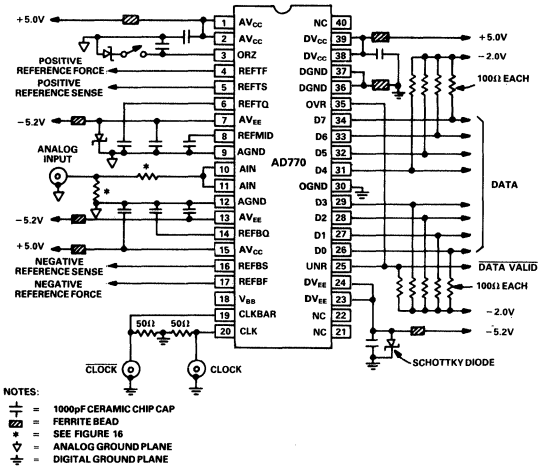


Figure 18. AD770 Application Example

LATCHING THE OUTPUT DATA

A simplified AD770 timing diagram is illustrated in Figure 19. The input signal is sampled on the falling edge of CLK. The output data for that sample is delayed by the Pipeline Delay plus the Output Delay. The Pipeline Delay is two CLK low periods and one CLK high period, and thus depends on the conversion rate and the clock duty cycle. Output Delay is measured from the second CLK rising edge after the falling edge which samples the analog input signal. Output Delay is not dependent on the conversion rate.

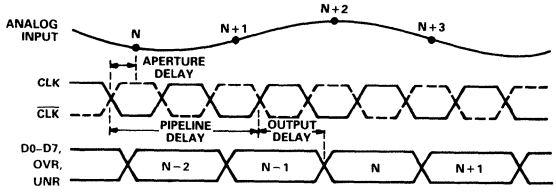


Figure 19. AD770 Timing Diagram

Output Delay varies from unit to unit due to manufacturing process variations. This factor, and the timing requirements of the external latch, must be considered when designing the output clock circuit.

Figure 20 shows a more detailed timing diagram that illustrates the effect of Output Delay variations and external latch timing requirements. Data bit transitions are shown for units at the extreme limits of Output Delay (T_D). For a unit with $T_D = T_{Dmin}$, the data bits will begin to slew after a delay of T_{Dmin}, and all bits will have settled after a further delay of T_{SK} (Output Skew). The data will then be stable until the next output data transition.

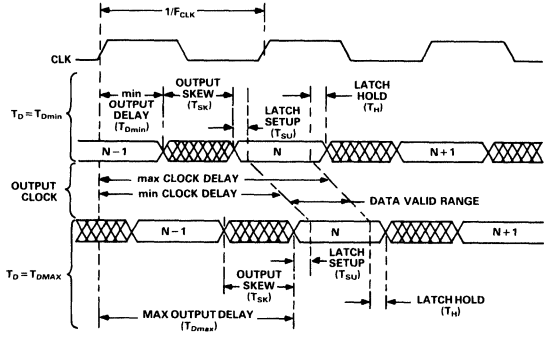


Figure 20. Detailed Timing Diagram Showing Output Delay Variation

However, the Setup and Hold times (T_{SU} and T_H) of the external latch must be subtracted to obtain the interval during which the external latch can be clocked (Data Valid Range). Thus:

$$\text{Data Valid Range} = 1/F_{CLK} - T_{SK} - T_{SU} - T_{TH}$$

The clock circuit will require a maximum delay that can also be easily derived:

$$\text{Max Clock Delay (for } T_D = T_{Dmin}) = 1/F_{CLK} + T_{Dmin} - T_H$$

For a unit with $T_D = T_{Dmax}$, the clock delay will be determined by the Maximum Output Delay (T_{Dmax}):

$$\text{Min Clock Delay (for } T_D = T_{Dmax}) = T_{Dmax} + T_{SU}$$

If the Maximum Clock Delay for $T_D = T_{Dmin}$ is greater than the Minimum Clock Delay for $T_D = T_{Dmax}$, a fixed clock delay set between these two values can be used to latch the output of the AD770.

$$T_{Dmax} + T_{SU} < \text{Fixed Clock Delay} < 1/F_{CLK} + T_{Dmin} - T_H$$

For example, a 120 MSPS system using 100K ECL logic would have the following conditions:

$T_{Dmax} = 6.0\text{ns}$
$T_{SU} = 0.7\text{ns}$
$F_{CLK} = 120\text{MHz}$
$T_{Dmin} = 2.0\text{ns}$
$T_H = 0.7\text{ns}$

$$\text{Max Clock Delay (for } T_D = T_{Dmin}) = 1/F_{CLK} + T_{Dmin} - T_H = 9.6\text{ns}$$

$$\text{Min Clock Delay (for } T_D = T_{Dmax}) = T_{Dmax} + T_{SU} = 6.7\text{ns}$$

A fixed clock delay could thus be used, with the following limits:

$$6.7\text{ns} < \text{Clock Delay} < 9.6\text{ns}$$

As the sample rate increases, the range of fixed clock delays becomes narrower. At 150 MSPS, using the same logic family, the range becomes:

$$6.7\text{ns} < \text{Clock Delay} < 8.0\text{ns}$$

At 200 MSPS, a fixed delay can no longer be used, since

Max Clock Delay (for $T_D = T_{Dmin}$) = 6.3ns
Min Clock Delay (for $T_D = T_{Dmax}$) = 6.7ns

The user should calculate whether a fixed delay can be used in the system. If a fixed delay cannot be used, a variable delay line is needed.

VARIABLE DELAY LINE

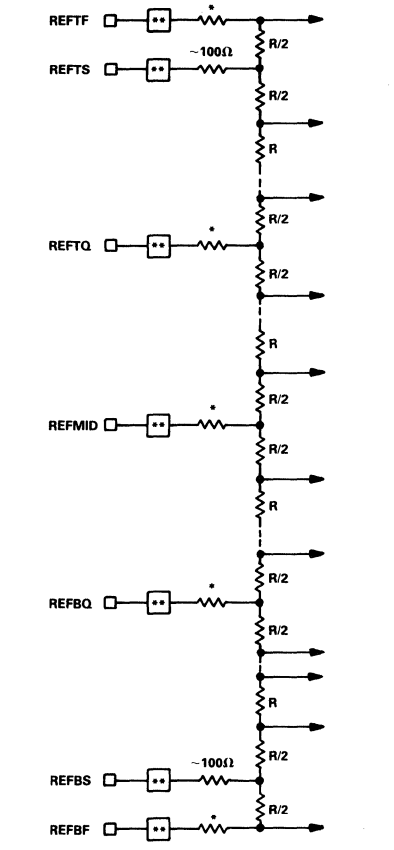
Continuing with the example above, we can determine the span of delays that is needed.

At 200 MSPS:

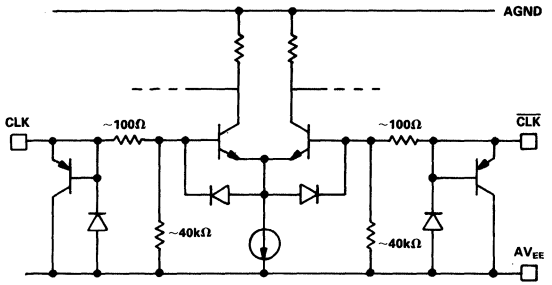
Max Clock Delay (for $T_D = T_{Dmin}$) = 6.3ns
Min Clock Delay (for $T_D = T_{Dmax}$) = 6.7ns
Data Valid Range (for each device) < 1.25ns.

The clock delay should have an adjustment range between (6.3 − 1.25/2) = 5.7ns and (6.7 + 1.25/2) = 7.3ns to center the clock edge in the middle of the Data Valid range for all devices.

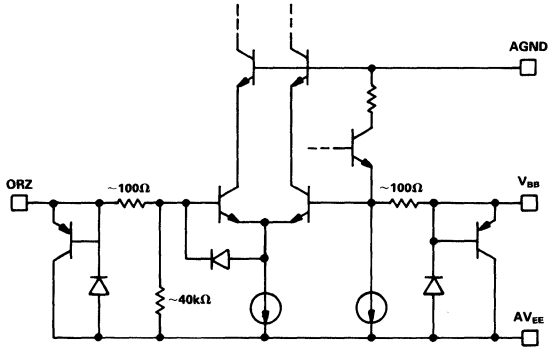
If a variable delay line is used, some means must be provided to verify that the delay is correctly set for each device. This can be done by providing a test signal synchronized to the system timing and adjusting the delay to the centerpoint of the range that gives a stable output.



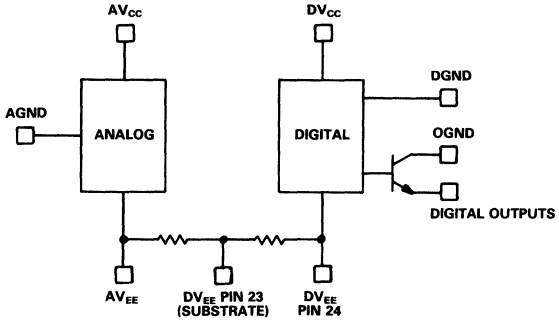
a. Reference Ladder



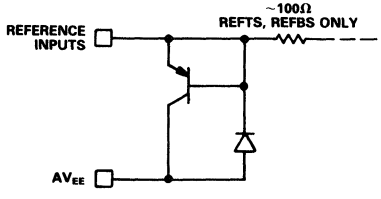
b. CLK, $\overline{CLK}$



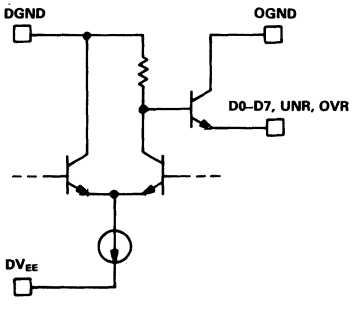
c. ORZ, V_{BB}



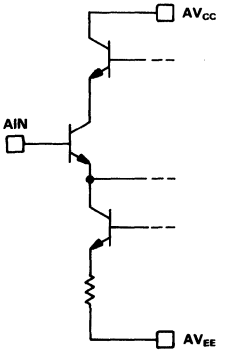
d. Internal Supply Connections



e. Reference Input Detail



f. Digital Outputs



g. Analog Input

Figure 21. Equivalent Circuits

ANALOG DEVICES

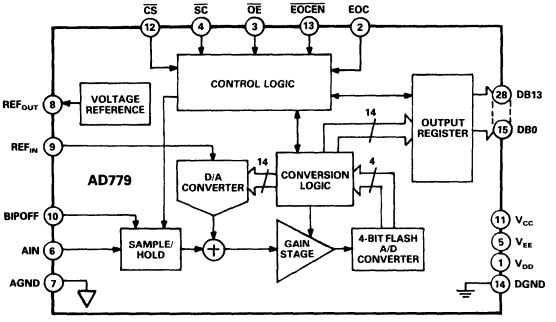
14-Bit 100 KSPS Complete Sampling ADC

AD779

FEATURES

AC and DC Characterized and Specified
100k Conversions per Second
1 MHz Full Power Bandwidth
500 kHz Full Linear Bandwidth
80 dB S/N+D (K Grade)
Twos Complement Data Format (Bipolar Mode)
Straight Binary Data Format (Unipolar Mode)
10 MΩ Input Impedance
16-Bit Bus Interface (See AD679 for 8-Bit Interface)
On-Board Reference and Clock
10 V Unipolar or Bipolar Input Range

AD779 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD779 is a complete, multipurpose 14-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD779 is similar to the AD1779 in that it is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD which are important in signal processing applications. In addition, the AD779 is fully specified for dc parameters which are important in measurement applications.

The 14 data bits are accessed by a 16-bit bus in a single read operation. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD779 operates from +5 V and ±12 V supplies and dissipates 720 mW. A 28-pin plastic DIP and a 0.6″ wide ceramic DIP are available. Contact factory for surface-mount package options.

Screening to MIL-STD-883C Class B is available.

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD779 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD779 is specified for both dc and ac parameters. DC specifications (such as INL, gain and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the single cycle read output provides compatibility with 16-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD779 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%, f_{SAMPLE} = 100 KSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD779J/S Min	AD779J/S Typ	AD779J/S Max	AD779K/T Min	AD779K/T Typ	AD779K/T Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO							
−0.5 dB Input (Referred to −0 dB Input)	**78**	79		**80**	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)							
@ +25°C		−90	**−84**		−90	**−84**	dB
		0.003	**0.006**		0.003	**0.006**	%
T_{min} to T_{max}		−88	**−82**		−88	**−82**	dB
		0.004	**0.008**		0.004	**0.008**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	**−84**		−90	**−84**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[2]							
2nd Order Products		−90	−84		−90	−84	dB
3rd Order Products		−90	−84		−90	−84	dB

NOTES
[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise noted.
[2]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 100 KSPS. See Definition of Specifications section.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.4**		V
V_{IL}	Low Level Input Voltage			**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = 5 V		**10**	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V		**10**	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V		**10**	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

DC SPECIFICATIONS

(T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10% unless otherwise indicated)

Parameter	AD779J Min	AD779J Typ	AD779J Max	AD779K Min	AD779K Typ	AD779K Max	Units
TEMPERATURE RANGE	0		+70	0		+70	°C
ACCURACY							
Resolution	**14**			**14**			Bits
Integral Linearity Error							
@ +25°C			±2			±1	LSB
T_{min} to T_{max}			±2			±2	LSB
Differential Linearity	**14**			**14**			Bits
Unipolar Zero Error[1] (@ +25°C)			±8			±4	LSB
Bipolar Zero Error[1] @ +25°C)			±8			±4	LSB
Gain Error[1,2] (@ +25°C)			±16			±8	LSB
Temperature Drift (Coefficients)							
Unipolar Zero[3]			±8 (10)			±6 (8)	LSB (ppm/°C)
Bipolar Zero[3]			±8 (10)			±6 (8)	LSB (ppm/°C)
Gain[3]			±36 (50)			±24 (33)	LSB (ppm/°C)
Gain[4]			±8 (10)			±6 (8)	LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	µs
Aperture Delay	5		20	5		20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	**4.95**		**5.05**	**4.98**		**5.02**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
POWER SUPPLIES (T_{min} to T_{max})							
Power Supply Rejection							
V_{CC} = +12 V ±5%[6]			±4			±4	LSB
V_{EE} = −12 V ±5%			±4			±4	LSB
V_{DD} = +5 V ±10%			±4			±4	LSB
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**32**		25	**32**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	720		560	720	mW

NOTE
[1]Adjustable to zero. See Figures 5 and 6.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
[6]1.4 V headroom is required between V_{CC} and AIN.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10% unless otherwise indicated)

Parameter	AD779S Min	AD779S Typ	AD779S Max	AD779T Min	AD779T Typ	AD779T Max	Units
TEMPERATURE RANGE	−55		+125	−55		+125	°C
ACCURACY							
Resolution	**14**			**14**			Bits
Integral Linearity Error @ +25°C			±2			±1	LSB
T_{min} to T_{max}			TBD			TBD	LSB
Differential Linearity							
(@ +25°C)	**14**			**14**			Bits
T_{min} to T_{max}	13			14			Bits
Unipolar Zero Error[1] (@ +25°C)			±8			±4	LSB
Bipolar Zero Error[1] (@ +25°C)			±8			±4	LSB
Gain Error[1, 2] (@ +25°C)			±16			±8	LSB
Temperature Drift (Coefficients)							
Unipolar Zero[3]			±16 (10)			±16 (10)	LSB (ppm/°C)
Bipolar Zero[3]			±16 (10)			±16 (10)	LSB (ppm/°C)
Gain[3]			±82 (50)			±82 (50)	LSB (ppm/°C)
Gain[4]			±16 (10)			±16 (10)	LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	μs
Aperture Delay	5		20	5		20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[5]	**4.95**		**5.05**	**4.98**		**5.02**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
POWER SUPPLIES (T_{min} to T_{max})							
Power Supply Rejection							
V_{CC} = +12 V ±5%[6]			±4			±4	LSB
V_{EE} = −12 V ±5%			±4			±4	LSB
V_{DD} = +5 V ±10%			±4			±4	LSB
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**32**		25	**32**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	720		560	720	mW

NOTE
[1]Adjustable to zero. See Figures 5 and 6.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]Excludes internal voltage reference drift.
[5]With maximum external load applied.
[6]1.4 V headroom is required between V_{CC} and AIN.

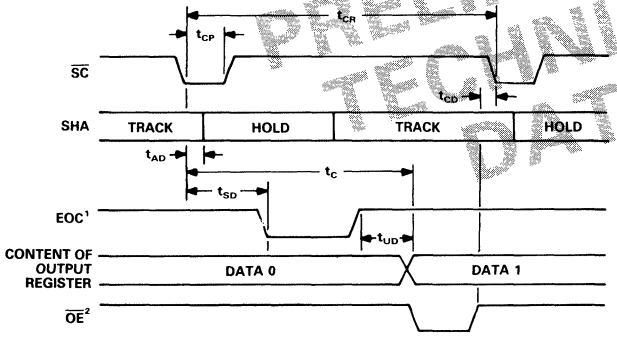
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at −55°C, +25°C and+125°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter	Symbol	Min	Max	Units
Conversion Rate[1]	t_{CR}		10	µs
Convert Pulse Width	t_{CP}	150		ns
Aperture Delay	t_{AD}	5	20	ns
Conversion Time	t_C		**8.5**	µs
Status Delay	t_{SD}	0	400	ns
Access Time[2]	t_{BA}		**100**	ns
Float Delay[3]	t_{FD}	10	**80**	ns
Update Delay	t_{UD}		200	ns
$\overline{OE}$ Delay	t_{OE}	20		ns
Read Pulse Width	t_{RP}	150		ns
Conversion Delay	t_{CD}	400		ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}$/$\overline{EOCEN}$ (0.8 V) to the time at which the data lines/$\overline{EOC}$ cross 2.0 V or 0.8 V. See Figure 4; C_{OUT} = 100 pF.
[3]Measured from the rising edge of $\overline{OE}$/$\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 4; C_{OUT} = 10 pF.
Specifications subject to change without notice.



NOTES
[1]$\overline{EOCEN}$ = LOW.
[2]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

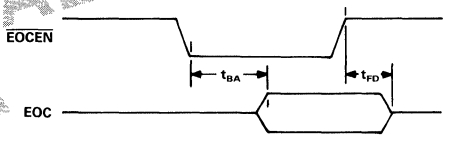


Figure 3. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

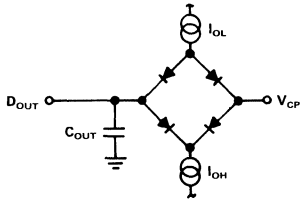


Figure 4. Load Circuit for Bus Timing Specifications

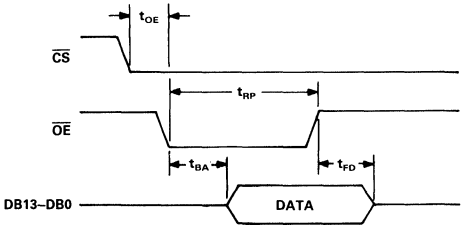


Figure 2. Output Timing

CONVERSION CONTROL

Before a conversion is started, End-of-Convert (EOC) is HIGH and the sample-hold is in track mode. A conversion is started by bringing $\overline{SC}$ LOW, regardless of the state of $\overline{CS}$.

After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample.

In track mode, the sample-hold will settle to ±0.003% (14 bits) in 1.5 μs maximum. The acquisition time does not affect the throughput rate as the AD779 goes back into track mode more than 2 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

When the conversion is finished, EOC goes HIGH and the result is loaded into the output register after a period of time t_{UD}. Bringing $\overline{OE}$ LOW makes the output register contents available on the output data bits (DB13–DB0). A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued. This is to allow internal logic states to reset and to guarantee minimum aperture jitter for the next conversion.

If $\overline{SC}$ is held LOW, conversions will occur continuously. EOC will go HIGH for approximately 1.5 μs between conversions.

END-OF-CONVERT

End-of-Convert (EOC) is a three-state output which is enabled by End-of-Convert ENable $\overline{EOCEN}$.

OUTPUT ENABLE OPERATION

The data bits (DB13–DB0) are three-state outputs that are enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. $\overline{OE}$ must be toggled to update the output register. The output is read in a single cycle as a 14-bit word.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REFOUT), output coding is twos-complement binary.

POWER-UP

A conversion sequence, consisting of one $\overline{SC}$ instruction, is required after power-up to reset internal logic.

14-BIT MODE CODING FORMAT (1 LSB = 0.61 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}	Output Code	V_{IN}	Output Code
0	000 . . . 0	−5.00000 V	100 . . . 0
5.00000 V	100 . . . 0	−0.00061 V	111 . . . 1
9.99939 V	111 . . . 1	0	000 . . . 0
		+2.50000 V	010 . . . 0
		+4.99939 V	011 . . . 1

CONVERSION TRUTH TABLE

	INPUTS				OUTPUTS		
Mode	$\overline{SC}$	$\overline{EOCEN}$	$\overline{CS}$	$\overline{OE}$	EOC	DB13 . . . DB0	Status
Start Conversion	1	X	X	X			No Conversion
	↓	X	X	X			Start Conversion
	0	X	X	X			Continuous Conversion
Conversion Status	X	0	X	X	0		Converting
	X	0	X	X	1		Not Converting
	X	1	X	X	High Z		Either
Data Access	X	X	X	1		High Z	Three-State
	X	X	1	X		High Z	Three-State
	X	X	0	0		MSB . . . LSB	Data Out

NOTES
U = Logical OR.
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ HIGH to LOW transition. Must stay LOW for t = t_{CP}.

AD779 PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground. This is the ground return for AIN only.
AIN	6	AI	Analog Signal Input.
BIPOFF	10	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} for ±5 V input bipolar mode and twos-complement binary output coding.
$\overline{CS}$	12	DI	Chip Select. Active LOW.
DGND	14	P	Digital Ground
DB13–DB0	28–15	DO	Data Bits. These pins provide all 14 bits in one 14 bit parallel output. Active HIGH.
EOC	2	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. EOC is a three-state output. See $\overline{EOCEN}$ pin for information on EOC gating.
$\overline{EOCEN}$	13	DI	End-of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{OE}$	3	DI	Output Enable. A down-going transition on $\overline{OE}$ enables data bits. Active LOW.
REF_{IN}	9	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	AO	+5 V Reference Output. Tied to REF_{IN} for normal operation.
$\overline{SC}$	4	DI	Start Convert. Active LOW.
V_{CC}	11	P	+12 V Analog Power.
V_{EE}	5	P	−12 V Analog Power.
V_{DD}	1	P	+5 V Digital Power.

Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers.
P = Power.

AD779 ORDERING GUIDE[1]

Plastic DIP (N-28A)[2] 0 to +70°C	Ceramic DIP (D-28A)[2] 0 to+70°C	Ceramic DIP (D-28A)[2] −55°C to +125°C	Integral Nonlinearity	S/N+D[3]
AD779JN	AD779JD	AD779SD	±2 LSB	79 dB
AD779KN	AD779KD	AD779TD	±1 LSB	81 dB

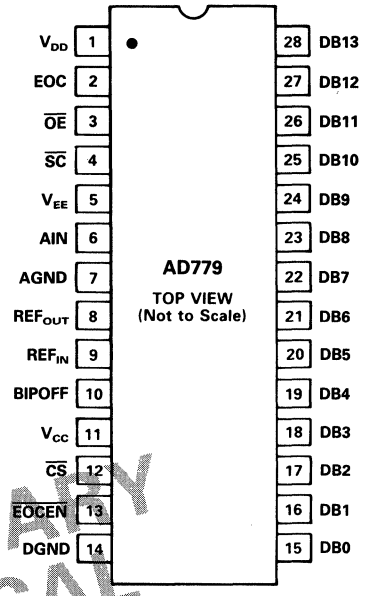
NOTES
[1]For two cycle read (8+6 bits) interface to 8-bit buses, see AD679.
[2]See Section 14 for package outline information.
[3]Typical at 10 kHz, −0.5 dB input.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	−12	+12	V
REF_{IN}	V_{EE}	0	V_{CC}	V
REF_{IN}	V_{CC}	V_{EE}	0	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature				
J and K Grades		0	+70	°C
S and T Grades		−55	+125	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ESD SENSITIVITY

The AD779 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD779 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

Definition of Specifications

NYQUIST FREQUENCY

An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT

The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD779 has been designed to optimize input bandwidth, allowing it to undersample input signals with frequencies significantly above the converter's Nyquist frequency. If the input signal is suitably band-limited, the spectral content of the input signal can be recovered.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL LINEARITY (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential linearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

This specification is 14 bits for the AD779J, K and T grades, which guarantees that all 16,384 codes are present. The AD779S grade specifies 13 bits NMC, which means that missing codes do not occur adjacent to each other.

INTEGRAL LINEARITY ERROR (INL)
The ideal transfer function for a linear ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral linearity error is the worst case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

Note that the linearity error is not user adjustable.

POWER SUPPLY REJECTION
Variations in power supply will affect the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in the full scale transition point due to a change in power supply voltage from the nominal value.

TEMPERATURE COEFFICIENT
This is the maximum change in the parameter from the initial value (@ +25°C) to the value at T_{min} or T_{max}.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (11 1111 1111 1111 to 00 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9991 volts for a 0–10 V range, 4.9991 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

Application Information

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD779 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 300 Ω. The 10 V p-p full scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

The AD779 is factory trimmed to minimize offset, gain and linearity errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical, even these components can be eliminated.

In some applications, offset and gain errors need to be more precisely trimmed. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 5. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the AD779 accuracy limits are sufficient for application. If the pins are shorted together, the additional offset and gain errors will be approximately 80 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−0.305 mV for a ±5 V range) and adjust R1 until the major carry transition is located (11 1111 1111 1111 to 00 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9997 V for a ±5 V range) and adjust R2 to give the last positive transition (01 1111 1111 1110 to 01 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9997 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (10 0000 0000 0000 to 10 000 000 0001). Then perform the gain error trim as outlined above.

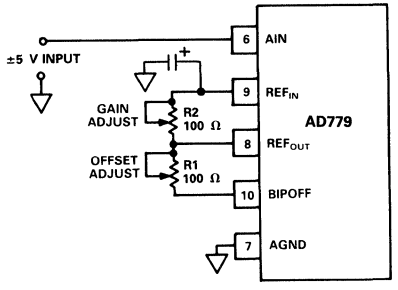


Figure 5. Bipolar Input Connections with Gain and Offset Trims

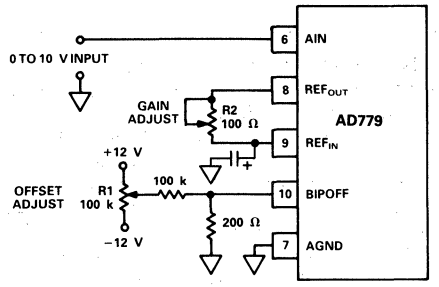


Figure 6. Unipolar Input Connections with Gain and Offset Trims

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 6. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code will be centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 00 0000 0000 0000 to 00 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (0.305 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 0.305 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9997 V for a 10 V range) and adjust R2 until the last transition is located (11 1111 1111 1110 to 11 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

REFERENCE DECOUPLING

It is recommended that a 10 μF tantalum capacitor be connected between REF_{IN} (Pin 9) and ground. This has the effect of improving the S/N+D ratio through filtering possible broad-band noise contributions from the voltage reference.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 1 LSB at the 14-bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD779 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB13–DB0 and EOC.

SUPPLY DECOUPLING

The AD779 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and analog ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD779, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD779 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD779 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD779. If multiple AD779s are used or the AD779 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

INTERFACING THE AD779 TO MICROPROCESSORS

The I/O capabilities of the AD779 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD779 interface configurations.

AD779 TO TMS320C25

In Figure 7 the AD779 is mapped into the TMS320C25 I/O space. AD779 conversions are initiated by issuing an OUT instruction to Port 1. EOC status and the conversion result are read in with an IN instruction to Port 1. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 1 and $\overline{MSC}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD779 read instruction.

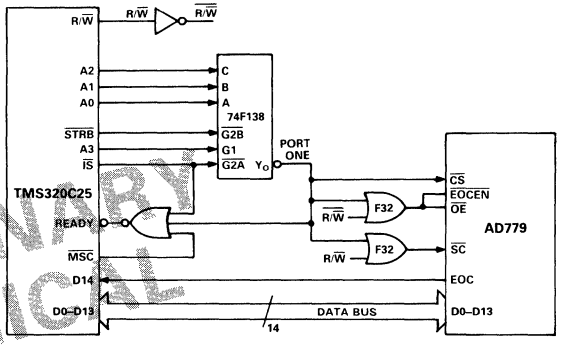


Figure 7. AD779 to TMS320C25 Interface

AD779 TO 80186

Figure 8 shows the AD779 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD779 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

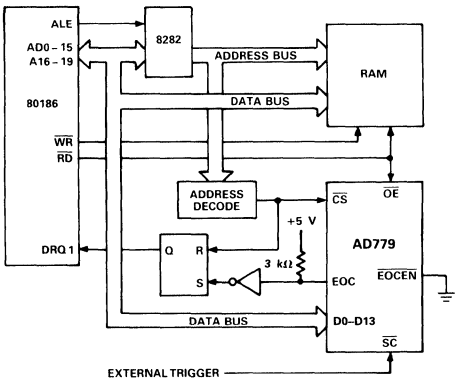


Figure 8. AD779 to 80186 DMA Interface

The AD779 is asynchronous which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD779 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

AD779 TO Z80

The AD779 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 9 illustrates an I/O configuration, where the AD779 occupies several port addresses to allow separate polling of the EOC status and reading of the data.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD779 to be used with Z80 processors having clock speeds up to 8 MHz.

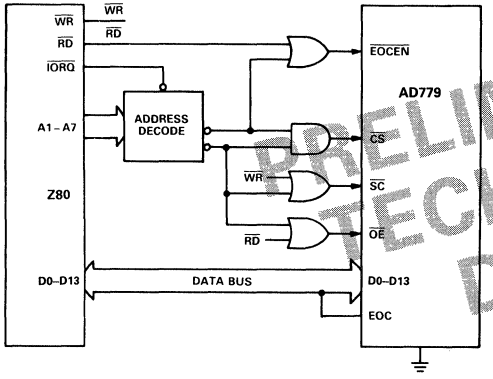


Figure 9. AD779 to Z80 Interface

AD779 TO ANALOG DEVICES ADSP-2100A

Figure 10 demonstrates the AD779 interfaced to an ADSP-2100A. With a clock frequency of 1.25 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD779 data memory interface with two wait states.

The converter runs asychronously using a sampling clock. The EOC output to the AD779 gets asserted at the end of each conversion and causes an interupt. Upon interrupt, the ADSP-2100A starts a data memory read by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latches, is used to force the ADSP-2100A into a two cycle wait state by generating DMACK. The read operation is thus started and completed within three processor cycles (240 ns).

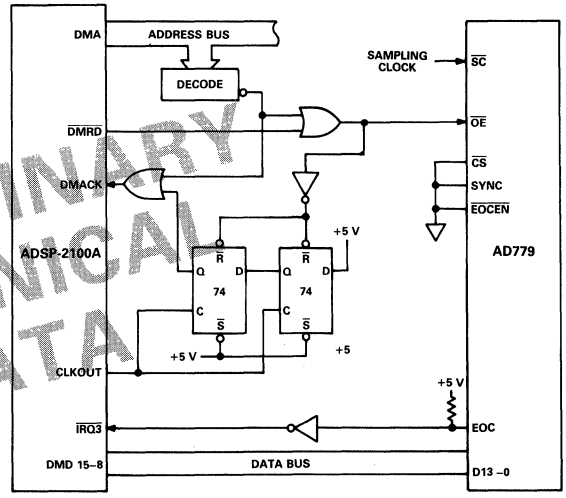


Figure 10. AD779 to ADSP-2100A Interface

High Resolution, Programmable Integrating A/D Converter

AD1170

FEATURES

Low Nonlinearity:
- **Integral: ±0.001%**
- **Differential: ±0.00035%**

Microcomputer-Based Design
- **Programmable Integration Time: 1 to 350ms with Resolution from 7 to 18 Bits**
- **Programmable Output Data Format**
- **Auto-Zeroed Operation and Electronic Calibration (No External Trim Potentiometers)**
- **Microprocessor Compatible Interface**

High Throughput: Over 50 Conversions/Second for Line Cycle Integration Period

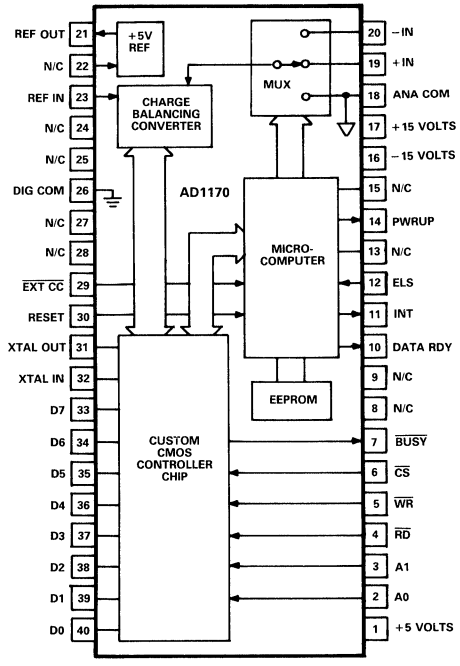
High Normal Mode Rejection: 54dB at 60Hz

Small Size: 1.24″ × 2.5″ × 0.55″ max

APPLICATIONS

Data Acquisition Systems
Scientific Instruments
Medical Instruments
Weighing Systems
Automatic Test Equipment

AD1170 FUNCTIONAL BLOCK DIAGRAM



LEAVE N/C PINS UNCONNECTED

GENERAL DESCRIPTION

The AD1170 is a high resolution integrating A/D converter intended for applications requiring high accuracy and high throughput at low cost. A novel conversion architecture provides the user with outstanding accuracy, stability and ease of use.

The AD1170 is a complete microcomputer-based measurement subsystem, composed of three major elements: a highly precise charge balancing converter, a single chip microcomputer, and a custom CMOS controller chip. The AD1170 offers independently programmable integration time (from one millisecond to 350 milliseconds) and data format (offset binary or two's complement, from 7 to 22 bits). The converter is fully auto-zeroed and exhibits a span drift of only 9ppm/°C, assuring stable, accurate readings.

The AD1170 may be interfaced to any microcomputer based system in a memory mapped or I/O mapped fashion via an 8-bit data bus. The AD1170's advanced features are controlled by simple commands sent to it via this bus.

The converter utilizes surface mount technology and is housed in a small 1.24″ × 2.5″ × 0.55″ package. It operates from ± 15V dc and +5V dc power.

PRODUCT HIGHLIGHTS

1. The AD1170, unlike dual slope converters, offers the user the capability of programming the integration time by selecting one of seven preset integration periods or by loading an arbitrary integration period over the interface bus.
2. The AD1170 architecture provides for user programmable data format independent of the integration time. All data is computed to 22-bit resolution and the user may specify any resolution from 7 to 22 bits. Usable resolution will typically be limited to 18-bits due to measurement and calibration noise error.
3. Electronic digital calibration eliminates the need for trim potentiometers. Calibration can be performed at any time by applying an external reference voltage to the input and invoking a calibration command. The calibration data is stored in an internal nonvolatile memory chip.
4. Internal calibration cycles may be programmed to occur whenever the converter is idle, assuring negligible offset drift and only 9ppm/°C span drift.
5. The conversion rate is greater than 50 conversions per second when programmed for 60Hz line cycle integration. The maximum conversion rate is greater than 250 conversions per second, using a one millisecond integration period.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, V_D = +5V unless otherwise specified)

Model	Min	Typ	Max	Units
RESOLUTION[1]	7		18	Bits
ACCURACY				
Integral Nonlinearity[2]		±0.001		% SPAN
THROUGHPUT RATE[3]				
Time (Integrate) = 1ms	250			conv/S
Time (Integrate) = 16.667ms	50			conv/S
Time (Integrate) = 100ms	9			conv/S
DIFFERENTIAL NONLINEARITY				
T(int) @ T(cal)				
1ms 10ms		±0.01		% SPAN
16.667ms 100ms		±0.0008		% SPAN
300ms 300ms		±0.00035		% SPAN
STABILITY				
Span		±9		ppm SPAN/°C
POWER SUPPLY REJECTION RATIO				
(Span Error vs. Analog Supply Voltage)		60		ppm of Reading/V
INPUT CHARACTERISTICS				
Analog Input Range				
dc	−5		+5	V
dc Plus Normal-Mode Voltage	−6		+6	V
Absolute Maximum (Without Damage)	−30		+30	V
Normal-Mode Rejection				
@60Hz		54		dB
@50Hz		60		dB
Input Bias Current		10		nA
Input Impedance		100		MΩ
REFERENCE				
Output Voltage		5		V dc
Output Current		2		mA
Input Range	4.5		5.5	V dc
DIGITAL LEVELS				
Inputs				
Low			0.8	V
High	2.0			V
Outputs				
Low (@4mA)			0.45	V
High (@100µA)	2.4			V
WARMUP TIME				
to 60ppm SPAN		5		min
to 20ppm SPAN		15		min
POWER REQUIREMENTS				
$+V_S$ and $-V_S$	9	15	18	V
$+V_D$	4.75	5	5.25	V
Supply Current Drain				
@ ±15V		12		mA
@ +5V		110		mA
TEMPERATURE RANGE				
Rated Performance	0		+70	°C
Storage	−25		+85	°C
SIZE	1.24" × 2.5" × 0.55" max (31.4 × 63.5 × 14.0) mm			

NOTES

[1]The usable resolution is limited by noise, which is largely determined by the integration period and calibration period. Consult the chart in Figure 4 for typical peak-to-peak noise versus integration and calibration period.

[2]The integral linearity is defined as the deviation from a straight line drawn between the endpoints of the converter. This specification is independent of gain and/or offset errors.

[3]Throughput Rate is calculated by the formula: $\frac{1000}{T(int) + 3 \text{ milliseconds}}$ = minimum conversions/second

Where T(int) is expressed in number of milliseconds.

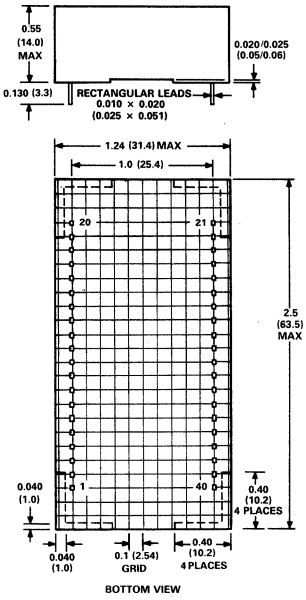
Specifications subject to change without notice.

IBM PC/XT/AT compatible evaluation board:* AC5004 (see last page of this data sheet for description).

*IBM PC/XT/AT is a trademark of International Business Machines Corp.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



CAUTION: OBSERVE PROPER PLUG-IN POLARITY TO PREVENT DAMAGE TO CONVERTER

PIN DESCRIPTIONS

PIN	SIGNAL	DESCRIPTION
1	+5V	Digital Power Supply
2,3	A0, A1	Address Control Lines
4	$\overline{RD}$	Read Data Strobe
5	$\overline{WR}$	Write Data Strobe
6	$\overline{CS}$	Chip Select
7	$\overline{BUSY}$	When Low, Indicates Device Busy When High, Indicates Device Ready for Command
10	DTA RDY	When High, Indicates That Data From Most Recent Conversion Command is Ready
11	INT	When High, Indicates Device is Currently Integrating Input Signal. Goes Low to Indicate Integration Complete
12	ELS	External Line Sample Input. Used with ELS Command to Sense an Externally Provided Sample of the Line Frequency
14	PWR UP	When High, Indicates Power Up Initialization in Progress
16	−15V	Negative Analog Power Supply
17	+15V	Positive Analog Power Supply
18	ANA COM	Analog Common: the Reference Point for Analog Power Supplies
19	+IN	Positive Signal Input
20	−IN	Negative Signal Input
21	REF OUT	Internal +5V Reference Output
23	REF IN	Reference Input; Normally Connected to Ref Out
26	DIG COM	Digital Common; the Reference Point for the Digital Power Supply
29	$E_{XT}\ \overline{CC}$	External Convert Command Input
30	RESET	Reset Input; Usually Connected to an RC Network for Automatic Reset Upon Power Up
31,32	XTAL OUT, XTAL IN	Connections for 12MHz Crystal (Series Resonant, 30Ω ESR). Alternatively, Xtal In May Be Driven From an External 12MHz Logic Signal
33-40	D7-D0	Bidirectional Data Bus
8, 9, 13, 15, 22, 24 25, 27 28		DO NOT CONNECT

FACTORY DEFAULT SETTINGS

The AD1170's internal nonvolatile memory stores various A/D parameters as programmed by the user (such as the integration period, output data format, calibration coefficient, etc.). The AD1170 is calibrated at the factory with the following default settings:

FORMAT: 16-bit, offset binary
DEFAULT T(int): 16.667 milliseconds (code 2)
DEFAULT T(cal): 100 milliseconds (code 4)

AD1170 ARCHITECTURAL OVERVIEW

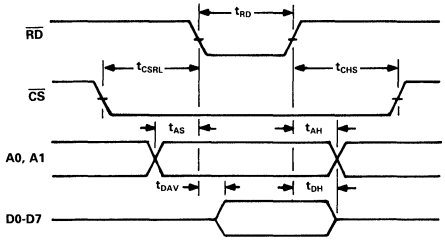
The AD1170 is a complete microcomputer-based measurement subsystem, containing three major elements: a highly precise charge balancing converter, a single chip microcomputer, and a custom CMOS controller chip.

The heart of the measurement technique is the charge balancing converter (essentially a voltage to frequency converter). This converter measures the input signal by balancing a proportional current against a train of precisely controlled reference current pulses using an integrator. The microprocessor, together with the counting and gating circuitry within the CMOS controller chip, measures the period of the reference current pulses by interpolating them using a 12MHz clock signal. The resulting data is converted to binary representation by the use of floating point firmware routines within the microprocessor.

When the AD1170 is triggered to perform a conversion, two separate phases are performed: first, an integration phase, where the input signal is actually measured, and then a computation phase, where the data from the integration phase is processed, along with both the volatile and nonvolatile calibration data, and formatted for output as the user desires.

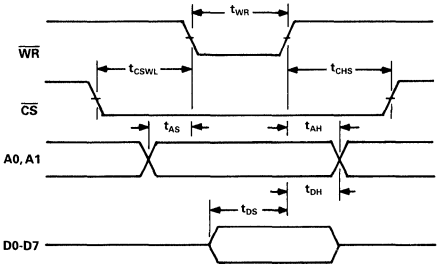
The duration of the integration phase can be programmed by the user, and may be as short as one millisecond, or as long as 350 milliseconds. The computation phase always lasts approximately three milliseconds and commences immediately after the integration phase is over. Therefore, the total conversion time will equal the user programmed integrate time plus a fixed 3 milliseconds. Status signals are provided to indicate when the data is ready and when the converter may be retriggered for the next conversion.

For maximum stability, the AD1170 periodically calibrates itself by performing measurements upon a zero input signal and a full-scale signal provided by the internal reference. This technique cancels any drift within the charge balancing converter itself, resulting in negligible offset drift, and gain stability equal to that of the reference. Calibration cycles may be programmed to take place whenever the AD1170 is idle, or they may be invoked under system control.



READ CYCLE TIMING REQUIREMENTS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RD}	RD Pulse Width	150			ns
t_{CSRL}	Chip Select to RD Low	0			ns
t_{CHS}	Chip Select Hold Time	0			ns
t_{AS}	Address Setup Time	10			ns
t_{AH}	Address Hold Time	0			ns
t_{DAV}	Data Valid Time			100	ns
t_{DH}	Data Hold Time			80	ns



WRITE CYCLE TIMING REQUIREMENTS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{WR}	$\overline{WR}$ Pulse Width	100			ns
t_{CSWL}	Chip Select to $\overline{WR}$ Low	0			ns
t_{CHS}	Chip Select Hold Time	0			ns
t_{AS}	Address Setup Time	10			ns
t_{AH}	Address Hold Time	0			ns
t_{DS}	Data Setup Time	80			ns
t_{DH}	Data Hold Time	20			ns

Figure 1. Timing Diagrams and Requirements

The AD1170 contains no internal trims; its span accuracy is factory calibrated by using the ECAL (Electronic CALibration) feature. This feature is a firmware routine which measures an externally applied reference voltage, compares it to the internal reference voltage, and computes a span correction factor which is stored in nonvolatile memory. The correction factor is then applied to all subsequent measurements, thereby compensating for the reference error. The ECAL function may be invoked by the user at any time, thereby replacing the usual trim potentiometer with a totally electronic calibration capability.

UNDERSTANDING THE AD1170 SPECIFICATIONS

The AD1170, because of its unique conversion technique, is specified quite differently from more conventional integrating converters. The following sections will help the user to understand where the sources of error are, and how to extract the best possible performance from the converter.

There are two primary sources of error in the AD1170: integral nonlinearity of the charge balancing converter, which influences all conversions equally, regardless of the integration period and calibration period; and the noise error of the measurement/calibration process, which is a function of the integration period and calibration period as selected by the user.

INTEGRAL NONLINEARITY

The integral nonlinearity of the charge balancing converter (CBC) is ±10ppm (±0.001%) of Span. This specification is an "endpoint" nonlinearity measurement; i.e., the typical deviation seen from a straight line drawn between the CBC output at −5 volts and its output at +5 volts. This specification excludes any gain or offset error.

If the converter was externally calibrated at its end points (−5 volts and +5 volts), then the integral nonlinearity would also be the relative accuracy of the converter. This is not the case in the AD1170, however, because calibration is performed internally at 0 and +5 volts, rather than −5 and +5 volts. This calibration technique, superimposed upon the integral nonlinearity of the CBC, results in the curve shown in Figure 2.

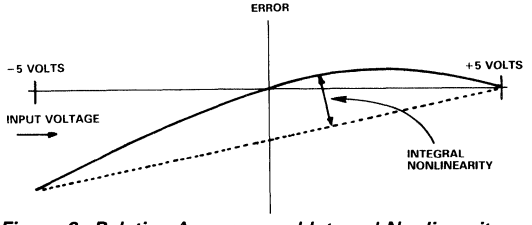


Figure 2. Relative Accuracy and Integral Nonlinearity when Calibrated

As shown in the diagram, the calibration technique tends to exaggerate the relative error at the negative end of the scale, and reduce the error between 0 and +5 volts. This characteristic happens to be most beneficial when using the AD1170 in systems where the input comes from a sensor whose signal is mostly positive, such as a thermocouple.

For systems where the user desires to minimize the relative error equally across the whole span of the converter, it is possible to intentionally introduce a span error during the ECAL procedure, as shown in Figure 3. This scheme sacrifices positive full-scale accuracy in order to minimize negative full scale error. The net result is a relative accuacy equal to the integral nonlinearity.

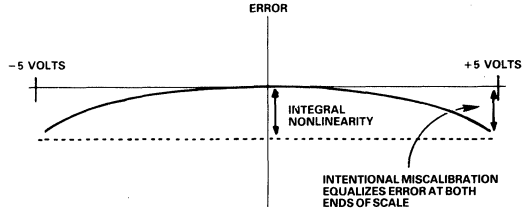


Figure 3. Relative Accuracy with Intentional Span Error at +F.S.

In both cases the accuracy of the input offset (which is servo controlled) is not compromised.

MEASUREMENT/CALIBRATION NOISE

Measurement noise refers to the conversion-to-conversion uncertainty caused either by mathematical truncation or device noise.

Calibration noise is actually the measurement noise resulting from the calibration process. The converter stabilizes itself by performing internal measurements of the reference, and of ground; these measurements have the same uncertainty due to noise as does the normal measurement process.

The measurement and calibration noise error of the AD1170 determines the differential linearity, or useable resolution, of the converter. This parameter determines the usable resolution because it defines what codes can be seen through the noise. The specified value is the amount of error, in either direction from the average reading, which will not be exceeded for 95% of all conversions. This parameter, as in all integrating converters, is a function of the integration time; long conversions result in very high resolution, while short conversions provide lower resolution. In the AD1170, all internal computations are always carried out to 22-bit resolution, but useable resolution is limited by the peak-to-peak noise, as determined by T(cal) and T(int).

The chart shown in Figure 4, illustrates the typical peak-to-peak noise (in ppm Span) versus T(int) and T(cal). These numbers can be used to indicate how much useable resolution can be

	T(cal) =	1ms	10ms	16.7ms	20ms	100ms	166.7ms	300ms	CAL DISABLED	UNITS
T(int) =	1ms	208	115	115	114	113	112	111	110	±ppm of SPAN
	10ms		24	18	16	13	13	13	12	
	16.7ms			14	13	8	8	8	8	
	20ms				12	7	7	7	7	
	100ms					4.0	4.0	3.5	3.5	
	166.7ms						4.0	3.5	3.5	
	300ms							3.5	3.5	

Figure 4. Typical Peak-to-Peak Noise (in ppm Span) Versus T(int) and T(cal)

expected under a given set of operating conditions. For example, a peak-to-peak noise of ±8ppm is approximately analogous to a flicker of ±0.5LSB at 16 bits of resolution. Under these conditions, a user could set the default format for the AD1170 to 16-bit resolution, and observe no more than ±1/2LSB of differential error. See Table I for conversion of typical peak-to-peak noise to Differential Nonlinearity and Useable Resolution.

The chart in Figure 4 may also be used to determine the minimum effective calibration time for a specified integration period; the noise contributions of both the measurement cycle and the calibration cycle combine as the "root sum square", and the combined effect tends to asymptotically approach a baseline value determined by the shorter of the two. For example, a T(cal) greater than 10 milliseconds does little or nothing to improve the noise performance for conversions using a T(int) of 1 millisecond.

NOISE (ppm Span)	RESOLUTION AT 1/2LSB DNL ERROR (NO. OF BITS)	RESOLUTION AT 1LSB DNL ERROR (NO. OF BITS)	DIFFERENTIAL NONLINEARITY (% Span)
244	11	12	0.024
122	12	13	0.012
61	13	14	0.006
31	14	15	0.003
15	15	16	0.0015
8	16	17	0.00076
4	17	18	0.00038
2	18	19	0.00019

Table I. Conversion of Noise Error to DNL and Usable Resolution

SIGNAL INPUT CONNECTIONS

The AD1170 has both a positive input pin (+IN) as well as a negative input pin (−IN), but the AD1170 input is not a true differential input. The negative input pin is an input used during calibration cycles to establish the zero reference. In applications with static ground offsets, the −IN pin may be used as a ground sense input, to sense a signal reference point which is offset from analog common by a small differential. Both the −IN and +IN signals must have a bias current path back to analog common. Figure 5 illustrates the proper use of the input signal connections.

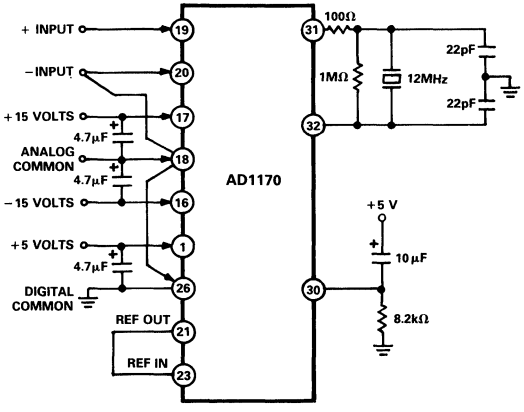


Figure 5. Input, Power, Reset, and Clock Connections

RESET

A reset sequence must be accomplished after power-up and before any access to the converter. The RESET line initializes the internal logic of the AD1170. This line may be driven from an external source, such as may exist in most computer based systems, or it may be connected to a simple RC circuit which will automatically invoke a reset sequence at power-up. Figure 5 illustrates the recommended circuit.

When driving the RESET line from an external source, the line must be held high for at least 2 microseconds after the oscillator is running and stable (typically 300 microseconds after power is applied) in order to assure a proper reset.

CLOCK

The AD1170 requires a 12MHz clock for operation. This clock may be supplied by connecting the XTAL OUT and XTAL IN pins to a 12MHz crystal, along with two resistors and two capacitors as shown in Figure 5.

The user may also supply a 12MHz logic signal from an external source, such as may be available in the user's system. In this case, the external clock should be applied to the XTAL IN pin, and the XTAL OUT pin should remain unconnected.

POWERING THE AD1170

For best performance, the user should pay careful attention to proper power supply bypassing, as well as grounding. Analog common and digital common are not connected internal to the module, but must be connected externally. Figure 5 illustrates the proper connection of power and ground to the AD1170[1].

REFERENCE CONNECTIONS

The internal +5 volt reference of the AD1170 is brought out to Pin 21 of the module; for normal operation, it should be connected to the reference input (Pin 23).

An external reference voltage of from 4.5 to 5.5 volts may be applied to the reference input (Pin 23), and the reference output may remain unconnected. The data will be ratiometric to that reference. The input impedance of the reference input is approximately 16K ohms. The reference input is not dynamic; any external reference voltage must be an essentially static DC signal.

INTERFACING TO THE AD1170

The AD1170 contains an eight-bit microprocessor compatible interface structure, including control lines. It can be interfaced to any microprocessor-based system in either a memory mapped or I/O mapped mode, and occupies four successive bytes of read/write address space, as shown in Figure 6.[1]

	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	FUNCTION
	H	X	X	X	X	Device Not Selected
WRITE	L	H	L	H	H	(Unused)
WRITE	L	H	L	H	L	Parameter 2 Write
WRITE	L	H	L	L	H	Parameter 1 Write
WRITE	L	H	L	L	L	Command Write
READ	L	L	H	H	H	High Data Read
READ	L	L	H	H	L	Mid Data Read
READ	L	L	H	L	H	Low Data Read
READ	L	L	H	L	L	Status Read

X = DON'T CARE

Figure 6. Control Functions

[1]Attempting to READ and WRITE at the same time ($\overline{RD}$ and $\overline{WR}$ set low) may alter the contents of the internal nonvolatile memory.

The AD1170 is controlled by writing a command into the lowest byte of the device image. Upon receipt of the command byte, the BUSY line is set low, indicating that command interpretation is in progress. The BUSY line returns high, following command interpretation and a command dependent execution time. This signals that the command execution has been completed, and another command may now be written. The logical inverse of the BUSY line is available in the STATUS byte for use in polling. See the section below about THE STATUS BYTE.

When the command requires one or two parameters, in addition to the command byte, they must be written into the second and third parameter bytes of the image *before* writing the command byte. This is because writing the command byte triggers the microprocessor to begin command interpretation.

Following the execution phase of any command, the CMD ERR bit in the STATUS byte will indicate acceptance or rejection of the command. When set, this bit indicates that there was a contextual or syntactic error in the command or parameters.

Conversions may be initiated either by bus command, or by a high to low transition of the EXT CC line[1]. Externally triggered conversions behave in the same way as bus triggered conversions, except that the BUSY line and the BUSY bit in the status word remain inactive; the end of execution of externally triggered conversions must be determined by examination of the DTA RDY line or the DTA RDY bit in the STATUS word.

THE STATUS BYTE

The lowest readable byte of the device image is the STATUS byte; it contains six bits of information about the current status of the AD1170. This byte may be examined by the host processor at any time. The individual bits in the status byte (see Figure 7) are assigned the following functions:

BIT0 The BUSY bit is an inverted version of the signal on Pin 7 of the module. When low, it indicates that the AD1170 is ready to receive a command. When high, it indicates that the AD1170 is busy executing the last command. Any commands loaded while the BUSY signal is high will be ignored.

BIT1 The DTA RDY bit (also available on Pin 10 of the module) goes high to indicate that the data from the most recent conversion is available in the LOW DATA, MID DATA, and HIGH DATA registers. This bit is cleared at the start of the next conversion. It may also be cleared by executing an EOI command.

BIT2 The DATA SAT bit is set by any conversion which is saturated, i.e., any conversion whose output data exceeds positive or negative full scale.

BIT3 The CMD ERR bit indicates that the most recently loaded command contained a contextual or syntactic error, or was not recognized. It is cleared when the next command is loaded.

BIT4 The INT bit (also available on Pin 11 of the module) goes high to indicate that the input signal is currently being integrated. It is used in multiplexed systems to determine when the input multiplexer may be switched.

BIT5 The PWRUP bit (also available on Pin 14 of the module) goes high when the module is powered up or when the RST command is executed. It remains high until device initialization is complete. This signal is used to indicate readiness of the converter after system initialization.

B7	B6	B5	B4	B3	B2	B1	B0
*	*	PWRUP	INT	CMD ERROR	DATA SAT	DATA RDY	BUSY

* UNUSED: CONTENTS INDETERMINATE

Figure 7. The Status Byte

OUTPUT DATA FORMAT

The AD1170 architecture allows a programmable data format independent of the integration time. The user may specify any resolution from 7 to 22 bits, and may specify either offset binary coding or two's complement coding. Programming the data format is accomplished via the use of the SDF command, using the format code described in the table in Figure 8 as the PARAMETER 1 value.

C_4	C_3	C_2	C_1	C_0	DATA FORMAT
H	X	X	X	X	Two's Complement
L	X	X	X	X	Offset Binary
X	H	H	H	H	22 Bits
X	H	H	H	L	21 Bits
X	H	H	L	H	20 Bits
X	H	H	L	L	19 Bits
X	H	L	H	H	18 Bits
X	H	L	H	L	17 Bits
X	H	L	L	H	16 Bits
X	H	L	L	L	15 Bits
X	L	H	H	H	14 Bits
X	L	H	H	L	13 Bits
X	L	H	L	H	12 Bits
X	L	H	L	L	11 Bits
X	L	L	H	H	10 Bits
X	L	L	H	L	9 Bits
X	L	L	L	H	8 Bits
X	L	L	L	L	7 Bits

X = DON'T CARE (C_7 C_6 C_5 = X FOR ALL DATA FORMATS)

Figure 8. Format Code

It should be noted that the AD1170 computes all data to 22 bit resolution. However, not all 22 bits are useable, since the differential performance is largely dependent upon factors such as integration period and calibration period. The SDF command simply serves to round off the result to the specified number of bits. The graph in Figure 4 can be used to estimate the amount of useable resolution achievable for a specified integration period and calibration period.

The output data is always right justified within the three output bytes (LOW DATA, MID DATA, and HIGH DATA). If two's complement format is selected, the MSB of the data is inverted and extended all the way to the top of the HIGH DATA byte. For example, if 16 bit two's complement format is selected, the data will appear in the LOW DATA and MID DATA bytes, and the MSB will be 0 for positive inputs.[2] The format is a nonvolatile parameter; whenever an SAVA command is executed, the current format will be saved to nonvolatile memory, and will become the default format upon powerup.

[1]The minimum duaration for $\overline{\text{EXT CC}}$ is one microsecond.

2Since the sign is extended all the way to the top of the uppermost byte, the HIGH DATA byte will be filled with the value of the MSB.

PROGRAMMING THE INTEGRATION PERIOD

The key parameter of any integrating A/D converter is the integration period. As shown in Figure 9, an integrating A/D converter provides maximum normal mode rejection at those frequencies which are integral multiples of 1/T(int), where T(int) is the integration period. The most common way to exploit this characteristic is to set the integration period equal to one period of the power line frequency so that ac hum will be rejected.

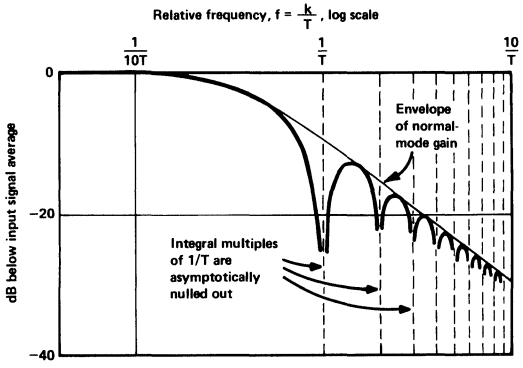


Figure 9. Normal Mode Rejection

The duration of the integration also affects the resulting resolution of the data; long integration times result in more usable resolution than do short integration periods.

The AD1170, unlike most dual slope converters, offers the user the capability of programming the integration time. This feature can be used to great advantage in systems design, since the integration time can be optimized for differing system conditions. For example, in systems whose inputs are severely polluted by 60Hz noise, the user may wish to program the AD1170 for a 100 millisecond integration time, which will result in excellent 60Hz normal mode rejection. In another application, a user may wish to scan a large number of channels rapidly, looking for gross input changes, then slow down in order to make a high resolution conversion before resuming rapid scanning.

The AD1170 offers the user a number of different ways to set the integration period. The simplest way is by using the SDI command to set the default integration period to one of seven preset periods (1ms, 10ms, 16.66ms, 20ms, 100ms, 166.66ms, 300ms). The first two preset periods offer fairly rapid scanning at reduced resolution; the other five represent American and European line voltage standards or multiples thereof. For single conversions without altering the default integration time, the CNVP command may be used, which also allows the selection of one of these seven preset periods. These preset periods and their corresponding codes are listed in the table of Figure 10.

Another way in which the integration period may be programmed is via the EIS command, which allows the user to load the externally definable period register with a binary value[1] proportional to the desired integration period. Using this technique, the user may specify any period from one millisecond to 350 milliseconds (with 200 microsecond accuracy). Access to this user definable period is via the SDI or CNVP commands; the last entry in Figure 10 is used to select the period defined by the EIS or ELS command.

C_2	C_1	C_0	INTEGRATION TIME	NOTES
L	L	L	1 Millisecond	
L	L	H	10 Milliseconds	
L	H	L	16.667 Milliseconds	1 cycle @ 60Hz
L	H	H	20 Milliseconds	1 cycle @ 50Hz
H	L	L	100 Milliseconds	50/60Hz
H	L	H	166.67 Milliseconds	10 cycles @ 60Hz
H	H	L	300 Milliseconds	50/60Hz
H	H	H	(See Note)	

NOTE
This code is used for externally loaded integration times (defined with the EIS Command) or externally measured times (from the ELS Command). The value can be anywhere from 1 Millisecond to 350 Milliseconds.

Figure 10. Preset Integration Periods

The third way to set the integration period is via the external line sampling feature, using the ELS command. This command samples the period of the logic signal presented to the ELS input pin (Pin 12), and sets the externally definable period register accordingly. This feature is most useful in environments with fluctuating line frequencies. By executing an occasional ELS command, the converter effectively "tracks" the line frequency. To use this feature, a clean, bounce free logic representation of the line frequency must be present at the ELS input during the execution of the ELS command. Once having performed the ELS command, the measured integration time may be selected using the SDI or CNVP commands along with the (HHH) code from the table in Figure 10[2].

It should be noted that the actual integration period used in the measurement process is accurate to about $\pm 200\mu s$, due to the limitations of the charge balancing converter. This is adequate, however, for greater than 50dB of normal mode rejection at 60Hz when using an integration period of 1/60 second. Even greater normal mode rejection may be obtained when the integration period is a multiple of the line frequency period.

CONTROLLING THE CALIBRATION CYCLES

The AD1170 achieves its excellent span and offset stability by calibrating itself against its internal reference voltages. The user can control the frequency of occurrence for calibration cycles and their duration.

The duration of the calibration cycle is an important parameter, because it affects the accuracy of the calibration cycle itself. Errors in the calibration cycle appear in the output data as instantaneous offset and span errors. If automatic "background" calibration is enabled, these errors effectively appear as noise. Just as in the case of input conversions, longer calibration times result in more accuracy and less noise.

Of course there may be system applications where there simply isn't sufficient time to perform a long calibration cycle. For this reason, the AD1170 offers the user the ability to specify the calibration period, using the SDC command.

[1]See the section titled "The AD1170 Command Set" for the formula used to compute the proper binary value.

[2]Caution is advised; if no signal is present at the ELS input when the ELS command is executed, or if the signal is not within acceptable frequency limits, the module may "hang" and require a hardware reset to continue operation.

The argument for the SDC command is the same three-bit code as is used for the SDI and CNVP commands. The reason for this is that each calibration cycle consists essentially of two ordinary conversion cycles, performed upon the internal zero and span references. For example, if an SDC command with an argument of 3 is executed, the default calibration time will then be approximately 49 milliseconds (two conversions of 20 milliseconds plus approximately 9 milliseconds for the internal mathematics).

The user may also disable or enable background calibration. In systems where the AD1170 may be periodically idle, i.e., not performing input conversions, background calibration is a good choice. This mode is enabled with the CALEN command and will cause the AD1170 to continually initiate an internal calibration cycle whenever the converter is otherwise unoccupied. Any conversion commands received during a cal cycle will cause that cal cycle to be aborted in favor of the input conversion, thereby giving the user priority over calibration. This mode of operation is automatic and transparent.

The CALDI instruction is used to disable background calibration. When this instruction is executed, the converter will be completely idle between convert commands, and calibration cycles will only occur when invoked by the SCAL command. This mode of operation is best when the user would like to perform input conversions at the maximum rate, and/or when the system affords a specific convenient time to perform calibration.

There are no hard and fast rules about the best way to apply all of this flexibility, but best performance will be obtained if the following points are observed:

- Consult the chart in Figure 4 to determine the minimum effective calibration period for use with a desired integration period.
- Don't use automatic background calibration unless your system will allow the converter enough uninterrupted time to perform at least one calibration cycle. For example, if you are using a calibration period code of 3, your system must periodically allow at least 49 milliseconds without a convert command or calibration will not occur.
- Remember that the purpose of the calibration cycle is to cancel the intrinsic drift of the charge balancing converter within the AD1170 itself. If the converter is in a stable environment, calibration may be done less frequently. The best possible performance will be achieved in stable ambient temperatures, where calibration is manually invoked by the system at relatively long intervals, using the longest allowable calibration time.
- Very short calibration times, although allowed by the AD1170 firmware, are not especially useful because they introduce more error than they compensate. The only useful purpose of very short calibration times is in systems which are operating in rapidly changing ambient temperatures, and then only for relatively low resolution conversions.

COMPENSATION OF EXTERNAL OFFSETS

An electronic "null" feature compensates for offset errors of signal conditioning stages preceding the AD1170.

The null feature comprises three commands: NULL measures the input signal (using the current integration time) and stores it in internal RAM; NULEN subtracts the measured value from all subsequent conversions; NULDI cancels the NULEN command's effect.

The sum of the offset value plus the full-scale input should be less than the ±6 volts linear input range of the AD1170. The offset value to be nulled should ideally be no more than a few hundred millivolts in amplitude.

The NULL command does not need to be executed every time the AD1170 is powered up. Since the value measured by the NULL command is saved and restored by the SAVA and RESA commands, the value of the null will be the one saved during the last SAVA command. Execute a NULL command only when a new null measurement is desired.

When NULEN is in effect, the length of each conversion will be extended by approximately 700 microseconds.

ELECTRONIC CALIBRATION

The AD1170 contains an Electronic CALibration capability, which, along with the internal nonvolatile memory chip, effectively eliminates the need for trim potentiometers of any kind. This capability, abbreviated as ECAL, should not be confused with the internal background calibration cycles. ECAL is a completely distinct function used to calibrate the AD1170 to an external reference standard.

The ECAL function measures the ratio of the internal reference voltage in the module with respect to an externally applied reference voltage. The resulting coefficient is applied to the math computations for all subsequent conversions, effectively compensating the module for absolute value errors in its own reference. The ratio is stored in random access memory until the user invokes a SAVA command, which will save this coefficient (along with the other nonvolatile parameters) in the nonvolatile memory chip. When the module is powered up, the previously saved coefficient is recalled from nonvolatile memory and stored in random access memory.

In order to use the ECAL command, the input to the AD1170 must first be presented with an external +5 volt reference standard such as is usually found in many calibration labs. The ECAL command may then be invoked; the external reference voltage must remain at the input until command execution is complete. If the calibration is to be made nonvolatile, a SAVA command must then be invoked.[1]

ECAL may also be used as a means of making limited ratiometric measurements. For example, in some applications, it may be useful to be able to measure the output of some transducer with respect to its excitation; if the excitation can be scaled to the range of 4.5 to 5.5 volts, then it can be used as an excitation for the ECAL process. Having digitized the excitation, all subsequent conversions will be ratioed to the ECAL value. For example, if an ECAL procedure is performed upon a 4.5 volt source, and the converter subsequently digitizes a 2.25 volt signal, the converter output will be half of full scale, or 11000... (assuming offset binary coding). The converter can be restored to absolute calibration by executing a RESA command, which will restore the last nonvolatile ECAL coefficient to random access memory.

The user is cautioned that the nonvolatile memory used in the AD1170 has a finite endurance of 1000 write cycles minimum. Assuming that the AD1170 is calibrated weekly, this implies a device life span of greater than 19 years. Less frequent calibrations mean a proportionately longer life span. This means ECAL may be performed any number of times, but the user should limit the number of SAVA commands in order to extend the life span of the nonvolatile memory.

[1]Since the SAVA command saves all nonvolatile parameters, the user should be sure that the other default parameters, such as integration time and data format, are set to their desired values before SAVA is invoked.

NONVOLATILE MEMORY

The internal nonvolatile memory in the AD1170 is used to store the various nonvolatile parameters associated with A/D operation (for example, the integration period, data format, ECAL coefficient, etc.).

In addition, eight 16-bit words of the nonvolatile memory are made available to the user for general purpose use. They may be accessed using the RDNV and WRNV commands. Because the nonvolatile memory is specified for a finite endurance of 1000 write cycles minimum, it is best used for data which does not regularly need to change, such as configuration information or system calibration parameters.

FACTORY DEFAULT SETTINGS

The AD1170 is calibrated at the factory; the factory default settings are:

Format: 16-bit, offset binary
Default T(int): 16.667 milliseconds (code 2)
Default T(cal): 100 milliseconds (code 4)

THE AD1170 COMMAND SET

The AD1170 command code set includes 20 different functions. Some of the commands require no parameters, while others require one or two parameters which must be loaded into the PARAMETER 1 and PARAMETER 2 registers prior to loading the command register. Some commands (for example, CNVP) have their option parameter embedded in the lowest three bits of the command itself.

The execution time for any command depends on the command. Figure 11 is a synopsis of the available commands, as well as estimates of their execution times.

Each of the commands described below is preceded by an opcode name, along with the digital code (in binary).

CALEN 10110000

CALEN (CALibration ENable) enables automatic background calibration cycling. In this mode, background calibration cycles are executed automatically whenever the AD1170 is not otherwise occupied. If a command is received during a calibration cycle, that cycle will be aborted and the command will be executed.

CALDI 10111000

CALDI (CALibration DIsable) disables automatic background calibration. After executing this command, the AD1170 will be completely idle between commands. While in this state, a single calibration cycle may be invoked with the SCAL command.

CNV 00001000

CNV (CoNVert) causes a single conversion to be performed, using the current default integration time and data format.

CNVP $00010C_2C_1C_0$

CNVP (CoNVert using specific Preset time) causes a single conversion to be performed, using one of the eight preset integration times as listed in Figure 10. The default integration time is not changed. The three bit code for the desired integration time is embedded in the lowest three bits of the command code.

ECAL 00011000

ECAL (Electronic CALibration) causes an electronic calibration cycle to be performed. An external +5 volt reference voltage must be presented to the input before this command is executed, and the input must remain stable until the end of command execution is signaled by the BUSY line or the BUSY bit in the status word. The calibration data computed by this command is applied to all subsequent conversions, but is not made nonvolatile until a SAVA command is performed.

MNEMONIC	FUNCTIONAL DESCRIPTION	EXECUTION TIME (APPROX)
CNV	Perform a Single Conversion Using the Default Integration Time	T(int) + 3ms
CNVP	Perform a Single Conversion Using the Specified Integration Time	T(int) + 3ms
ELS	Measure Period of Signal at the ELS Input	2 × T(int) + 20ms
ECAL	Perform Electronic CALibration Routine	1.5 seconds
SDI	Set Default Integration Time for Input Measurements	150µs
SDC	Set Default Calibration Period	160µs
SDF	Set Default Data Format	140µs
RESA	Restore All Nonvolatile Parameters from Memory	2.3ms
SAVA	Save All Nonvolatile Parameters to Memory	150ms
WRNV	Write a Word to the User EEPROM Area	22ms
RDNV	Read a Word from the User EEPROM Area	600µs
EOI	Clear the Data Ready Flag	260µs
SCAL	Perform a Single Cal Cycle	2 × T(cal) + 9ms
CALEN	Enable Background Calibration	300µs
CALDI	Disable Background Calibration	310µs
EIS	Set Integration Time to Arbitrary Value	130µs
RST	Reset AD1170 to Power Up Conditions	210ms
NULL	Measure the Offset Voltage Value at the AD1170 Input and Store	T(int) + 3ms
NULEN	Subtract NULL Measured Value from All Subsequent Conversions	250µs
NULDI	Cancel the Effect of the NULEN Command	250µs

Figure 11. Synopsis of Commands

EOI 10001000

EOI (End Of Interrupt) clears the DTA RDY bit in the status byte, as well as the DTA RDY line (Pin 10). It is provided as a means of clearing the interrupt source in systems which use an interrupt upon data ready.

ELS 00100000

ELS (External Line Sample) measures the period of the logic signal applied to the ELS input (Pin 12)[1]. This period is loaded into the register associated with the last entry of the table in Figure 10. Input conversions using this measurement as the integration period may be performed by invoking a CNVP command, or by setting the default integration period with the SDI command. This command is intended for use in environments with varying line power frequency; periodically invoking this command allows effective tracking for improved normal mode rejection.

EIS 00101000

EIS (External Integration Set) is used to establish an arbitrary integration period from 1 millisecond to 350 milliseconds. To use this command, first load the PARAMETER 1 and PARAMETER 2 registers with the 16-bit binary number N, which is calculated using the following expression:

$$N = 2^{16} - T(int)/21.333E\text{-}6$$

After the low and high bytes representing N are loaded into the PARAMETER 1 and PARAMETER 2 registers respectively, execute the EIS command. Once this command is executed, the externally loaded integration time can be used via the CNVP or SDI commands.

RESA 01101000

RESA (REStore All) restores all configuration parameters (default integration time, default calibration time, data format, EIS/ELS period, NULL value and electronic calibration data) from nonvolatile memory. After executing this function, all parameters will be restored to their last value as saved by the SAVA command.

SAVA 01001000

SAVA (SAVe All) saves all programmable attributes (default integration time, default calibration time, data format, EIS/ELS period, NULL value and electronic calibration data) into nonvolatile memory.

SDI $00111C_2C_1C_0$

SDI (Set Default Integration time) sets the default integration time to one of the eight preset times listed in Figure 10. The three-bit code for the desired integration time is embedded in the lowest three bits of the command code.

SDF 00110000

SDF (Set Default Format) sets the default data format according to the five bit code loaded into the PARAMETER 1 register prior to execution of this command. The table in Figure 8 illustrates the construction of the five bit code according to the desired data format and resolution.

SCAL 11000000

SCAL (Single CALibration) performs a single background calibration cycle. This command is intended for use when automatic background calibration has been disabled via the CALDI command.

SDC $01000C_2C_1C_0$

SDC (Set Default Calibration time) sets the default calibration time (Tcal) according to the three bit code embedded in the lowest three bits of the command. The calibration times are shown in Figure 10. Note that the actual duration of a calibration cycle is approximately $2 \times T(cal) + 9$ milliseconds.

WRNV $10011A_2A_1A_0$

WRNV (WRite NonVolatile) writes the user supplied data, in the PARAMETER 1 and PARAMETER 2 registers, into the user accessible area of the AD1170's nonvolatile memory. Eight words of this memory are available, and are addressed by the lowest three bits of the command.

RDNV $10100A_2A_1A_0$

RDNV (ReaD NonVolatile) reads one word from the user accessible portion of the nonvolatile memory within the AD1170, and places the data into the LOW DATA and MID DATA registers for retrieval by the user. The address of the desired word is embedded into the lowest three bits of the command.

RST 10010000

RST (ReSeT) is effectively equivalent to a hardware reset of the AD1170. After executing this command, all nonvolatile parameters (including the ECAL coefficient, the default integration and calibration periods, EIS/ELS period, NULL value and the default format) will be restored to their last saved values, automatic calibration will be enabled, and NULL will be disabled.

NULL 01110000

NULL measures the input signal (using the curent integration time value) and stores the measurement in internal RAM. It allows the user to establish the value of offset voltage at the input and subtract that offset from subsequent conversions through the execution of the NULEN command. The user must insure that the sum of the offset value plus the full scale input is less than the ± 6 volts linear input range of the AD1170. Ideally the offset value to be nulled should be no more than a few hundred millivolts in amplitude. The value measured by the NULL command is saved and restored by the SAVA and RESA commands – maintaining this value through subsequent powerups. The NULL command need only be invoked when a new null measurement is desired.

NULEN 01111000

NULEN (NULl ENable) subtracts the value, measured and stored by the last NULL command, from all subsequent conversions. When NULEN is in effect, each conversion's length will be extended by approximately 700 microseconds.

NULDI 10000000

NULDI (NULl DIsable) cancels the effect of the NULEN command.

[1]This logic signal should be a TTL or CMOS compatible continuous waveform. It need not be symmetrical, but the HIGH or LOW time should not be less than 25 microseconds.

IBM PC INTERFACE

Figure 12 is an example of an AD1170/IBM interface suitable for the IBM PC or XT personal computers. In this case, the AD1170 is interfaced in the I/O space; the DIP switch controls the specific location of the AD1170 within the available address space.

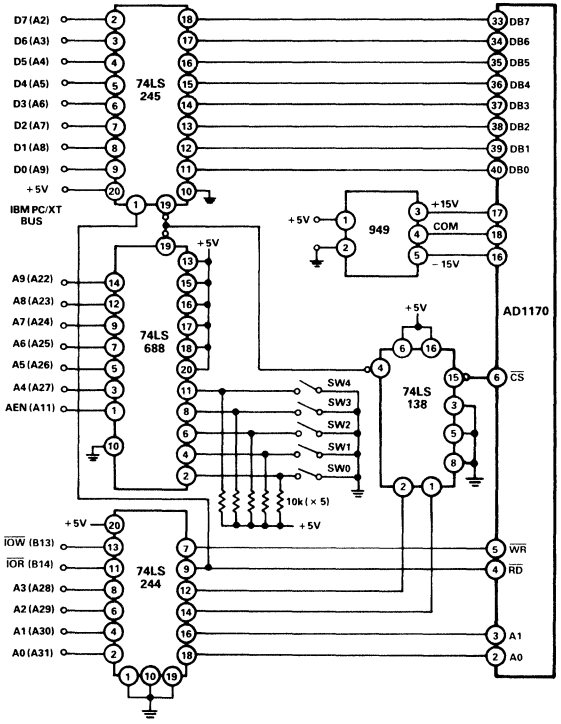


Figure 12. IBM PC/XT to AD1170 Interface

INTERFACING TO AN 8051 MICROCONTROLLER

Figure 13 shows how an AD1170 may be interfaced to an 8051 microcontroller using a technique commonly called "byte banging", where the control lines and data bus of a device are manipulated under firmware control. This "byte banging" technique can be adapted to most microprocessors and is useful in situations where a conventional bus structure is either nonexistent or unavailable for use.[1]

The AD1170's data bus is connected to the 8051 using I/O lines P2.0 through P2.7. The address lines A0 and A1 are connected to I/O lines P1.0 and P1.1 respectively. The RD/ and WR/ lines are connected to P1.2 and P1.3. The CS/ line of the AD1170 is grounded when it is the only device connected to the 8051, but multiple AD1170s could easily be connected in the same way if each CS/ line were separately controlled.

[1]Note that the 8051 microcontroller *does* contain a conventional bus structure; the "byte banging" interface shown here is presented as an example of an alternative technique.

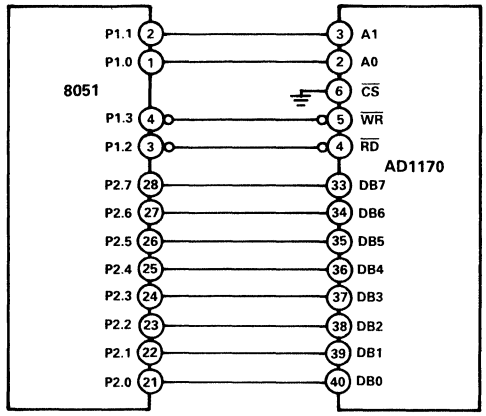


Figure 13. Simple 8051 to AD1170 Interface

To initialize the interface, first write "1"s to the port pins connected to the data bus and the RD/ and WR/ control lines. This puts the 8051 I/O lines into a lightly "pulled up" state, simulating a tri-stated condition on the bus to insure that neither RD/ or WR/ are selected:

```
INIT:   SETB  P1.2      ;DISABLE RD/
        SETB  P1.3      ;AND WR/
                        ;
        MOV   P2, #OFFH ;SET P2 TO ALL ONES
```

To write a command to the AD1170, first set the state of the P1.1 and P1.0 lines for the address corresponding to the byte to be written to. Set the P2 port to the command data, then strobe the WR/ line by first clearing the P1.3 line and then setting it:

```
WRCMD:  CLR   P1.0      ;FIRST CLEAR A0 AND A1
        CLR   P1.1      ;TO POINT TO CMD BYTE
                        ;
        MOV   P2, #CNV  ;CNV IS THE OPCODE FOR
                        ;A SINGLE CONVERSION
                        ;
        CLR   P1.3      ;STROBE THE WR/ LINE
        SETB  P1.3      ;ONE TIME
                        ;
        MOV   P2, #OFFH ;CLEAR DATA BUS TO
                        ;ALL ONES
```

To read a byte from the AD1170, first set the P1.0 and P1.1 lines to point to the address of the byte desired. Bring the RD/ line low, reading the contents of P2. Return the RD/ line high:

```
RDSTAT: CLR   P1.0      ;POINT TO STATUS BYTE
        CLR   P1.1      ;
                        ;
        CLR   P1.2      ;BRING RD/ LINE LOW
        MOV   A,P2      ;READ CONTENTS OF BUS
        SETB  P1.2      ;RESTORE RD/ LINE HIGH
```

PRESSURE TRANSDUCER DATA ACQUISITION

A two module solution for microcomputer based data acquisition uses a 1B31 hybrid signal conditioner and an AD1170 as shown in Figure 14. A 3 millivolt/volt pressure transducer (e.g., Dynisco's 800 series) is interfaced to a model 1B31 configured for a gain of 333.3, to provide a 0 to 5 volt output. The regulated excitation voltage is 5 volts, and is used as the reference input for the AD1170 to produce ratiometric operation. This configuration yields very high CMR enhanced by the 1B31 low pass filter and the integrating conversion scheme of the AD1170.

In addition, fixed offsets caused by bridge imbalance can be nulled out by the AD1170 with a power-up initialization command from the microcomputer (see COMPENSATION OF EXTERNAL OFFSETS section). The full-scale output of the 1B31 and Transducer can also be normalized to AD1170 full scale through the electronic calibration command ECAL. Both the offset and full-scale correction data can then be stored in nonvolatile memory to eliminate repeating this trim process after each power-up. The AD1170 eliminates a potentiometer or software overhead which might otherwise be needed for these functions.

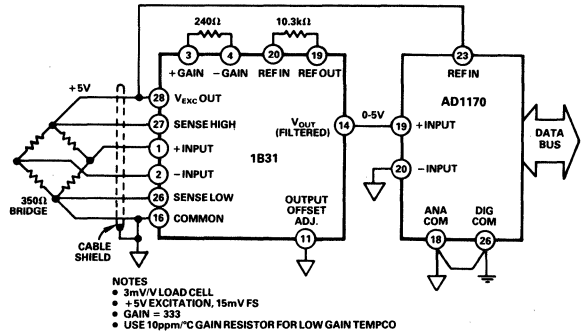


Figure 14. Pressure Transducer Data Acquisition Using 1B31 and AD1170

AC5004

. . . an IBM PC/XT/AT Compatible Evaluation Board for the AD1170

FEATURES

Compatible to the IBM PC/XT/AT or Equivalent
Menu-Driven Demonstration Software
Input Mating Connector
Full Documentation
  Example Listings of BASIC Programs
  Schematic
  Assembly Drawing
Complete Set of Tools to Evaluate an AD1170 A/D Converter

GENERAL DESCRIPTION

The AC5004 was designed as a support tool to enable the user to easily and quickly evaluate Analog Devices' AD1170 high-resolution programmable integrating A/D converter. The AD1170 is inserted directly into an AC5004 board which is designed to plug into the backplane of an IBM PC/XT/AT. Thus, armed with an IBM PC, an AD1170, and an AC5004 evaluation board, the user is fully prepared to examine the operation of the AD1170.

A User's Manual provides all the information required to put the AC5004/AD1170 evaluation process into operation. In the manual are full descriptions of the AC5004 memory address and power source selection jumpers as well as a schematic documenting the interface of the AD1170 to a computer bus.

The package also contains a comprehensive demonstration program written in BASIC that completely exercises all the functions of the AD1170. The AC5004 is an accessory that will make readily available to the user all the tools needed to comprehensively test the AD1170.

PRODUCT HIGHLIGHTS

1. AC5004 plugs directly into IBM PC/XT/AT or compatibles. Standard short slot card size (5 7/8″ × 5″ × 1″).
2. The AC5004 enables the user to evaluate the AD1170 high-resolution, programmable, integrating A/D converter without having to build a bread-board or prototype.
3. The evaluation boards come complete with software and programming examples designed to exercise all of the AD1170's functions.
4. AC5004 schematic and assembly drawings are provided to be used as examples of how to interface the AD1170 to a microprocessor bus.

Please note:
Order *AC5004* (does not include AD1170).

ANALOG DEVICES

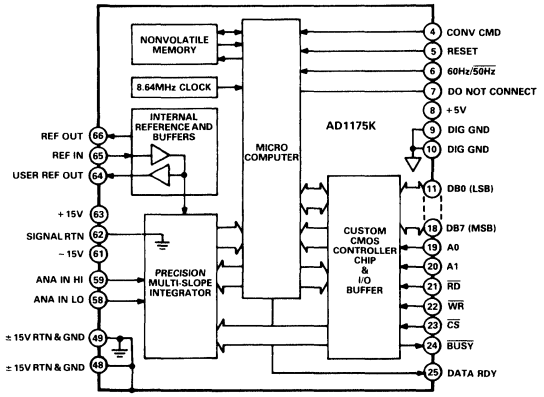
High Accuracy, 22-Bit Integrating A/D Converter

AD1175K

FEATURES
High Resolution: 22 Bits
Wide Dynamic Range: 133 dB
Low Nonlinearity:
Integral: ±0.5 ppm max
Differential: ±0.5 LSB max
High Stability:
Gain: ±1 ppm/°C max
Zero: ±0.5 mV/°C max
INL: ±0.01 ppm/°C
DNL: ±0.0025 ppm/°C
High Throughput Rate: 20 Conversions/Second
Microprocessor Compatible Interface
Compact Modular Package

APPLICATIONS
Data Acquisition Systems
Scientific Instruments
Medical Instruments
Weighing Systems
Automatic Test Equipment
Test and Measurement Equipment

AD1175K FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD1175 is a very high resolution integrating A/D converter intended for applications that require the highest possible accuracy without sacrificing conversion speed, board space or modest pricing. This converter provides the performance of large benchtop or rack mount instruments in a compact, modular package.

The AD1175 utilizes an auto-zeroed, multislope, integrating principle that features 22-bit resolution with extremely low nonlinearity (Integral: ±0.5 ppm max and Differential: ±0.5 LSB max). Temperature stability is specified at ±0.5 ppm/°C maximum for gain (exclusive of reference), ±0.5 μV/°C maximum for zero, ±0.01 ppm/°C for integral nonlinearity, and ±0.0025 ppm/°C for differential nonlinearity.

The integration time is user selectable for maximum, line frequency noise rejection at either 60 Hz or 50 Hz. The conversion rate is 20 or 16 per second respectively, which is many times faster than benchtop instruments of similar performance.

The nominal full-scale input range is ±5 V; however, rated accuracy is specified for inputs up to 10% over nominal, yielding a total dynamic range of greater than 4.6 million to 1. The analog input is a high impedance, high CMRR, true differential input pair. The input low operates within ±100 mV of analog ground and is used to sense signal low (at the source) to minimize ground loop problems.

The output of the AD1175 consists of four addressable 8-bit bytes (STATUS and 3 DATA) presented at an 8-bit tri-stated port with standard chip select.

Several modes of operation are available and allow writing to one of several addressable locations to program gain and offset, or to initiate a conversion.

The AD1175 requires no external components and operates from ±15 V dc and +5 V dc power. All digital inputs and outputs are LSTTL compatible. The 3.7″ × 5.2″ × 0.53″ metal case package provides excellent electrostatic and electromagnetic shielding.

PRODUCT HIGHLIGHTS

1. The unparalleled dynamic range, accuracy, linearity and stability of the AD1175 represent a breakthrough for an A/D converter offering small size and modest cost. Only large, expensive benchtop meters offer similar performance.
2. The AD1175 converts approximately ten times as fast as digital meters with like performance.
3. The microprocessor interface of the AD1175 provides for straightforward operation, but with the features required for optimum system performance. Simple commands control offset adjust, gain adjust, external offset null and initiate conversions. The output bytes indicate input polarity, off-scale condition and a variety of additional status information.
4. The AD1175 is a complete A/D converter including a precision internal reference, clock and integration capacitor. Offset and coarse gain adjust are bus controlled, while user accessible trim potentiometers allow fine gain adjust and ±full scale balance adjust.
5. Conversions may be made using either the offset and coarse gain settings stored in internal nonvolatile memory, or new settings made via the bus. The nonvolatile memory may be updated on command with the new settings.

SPECIFICATIONS (typical @ +25°C, V_S = ±15 V, V_D = +5 V unless otherwise specified)

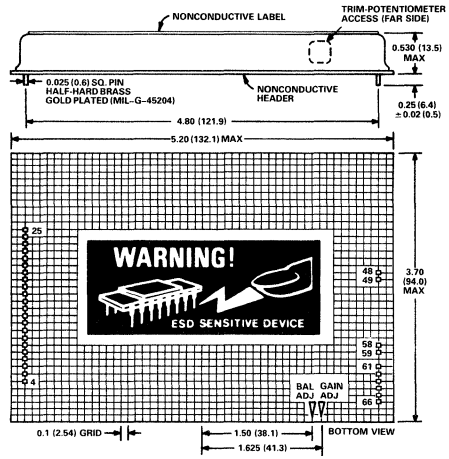
Model	AD1175K
RESOLUTION	22-Bits +10% Overrange (4,600,000 Counts) min
DYNAMIC RANGE	133 dB
ACCURACY	
Integral Nonlinearity[1]	±0.5 ppm FSR[2], max
Differential Nonlinearity (@ 22 Bits)	±0.5 LSB, max
Total Noise (Ref to Input, 95% Confidence)	5 μV p-p max
STABILITY	
Gain TC (Excluding Reference)	±1 ppm RDG/°C, max
Zero TC	±0.5 μV/°C, max
Integral Nonlinearity TC	±0.01 ppm FSR[2]/°C
Differential Nonlinearity TC	±0.0025 ppm FSR[2]/°C
POWER SUPPLY REJECTION RATIO (±15 V)	±5 ppm FSR[2]/V
WARMUP TIME	
Relative Accuracy (for Rated Performance)	15 Minutes
Full Rated Performance	45 Minutes
REFERENCE	
External Reference In	
For Rated Performance	+6.95 V ±2%[3]
Maximum Input (Operating Only)	+9.6 V
Reference Output	
Voltage	+6.95 ±2%
Output Resistance	250 Ω
Temperature Coefficient	±0.4 ppm/°C (±0.8 ppm/°C, max)
Drift with Time[4]	
1st 15 Days Operating	±1 ppm/Day
After 15 Days Operation	±25 ppm $\sqrt{1000}$ hrs., max
Noise, 0.01 Hz to 10 Hz (95% Confidence)	1 ppm p-p, max
User Reference Output	
Gain (Referred to Reference In)	1.000 to 1.012[5]
Current	±2 mA, max
Stability: Temperature Coefficient	±1 μV/°C, max
THROUGHPUT RATE[6]	
@ Integrate Time of 1/30 sec (60 Hz)	20 conversions/sec
@ Integrate Time of 1/25 sec (50 Hz)	16 conversions/sec
ANALOG INPUT CHARACTERISTICS	
Voltage Range[7,8]	±5 V Bipolar
Max $V_{IN}H$ (at Input Hi, Without Damage)	±12 V
Max $V_{IN}L$ (at Input Lo, Without Damage)	±3 V
Max $V_{IN}LR$ (Input Lo, for Rated Performance)	±100 mV
Input Resistance (Input Hi, or Input Lo)	1000 MΩ
Input Bias Current, Input Hi or Input Lo (+10°C to +50°C)	±10 nA, typ, ±40 nA max
Input Bandwidth[9]	
Small Signal	2.0 MHz
Large Signal	150 kHz
CMRR at dc to 60 Hz	80 dB, min
ADJUSTMENTS	
Offset (Programmable)	
Range	±75 mV
Resolution	1 LSB Steps
Gain-Coarse (Programmable)[8]	
Range	<4.7V to >5.6 V
Resolution	0.009% Steps
Gain-Fine Range[5,8]	±0.006% FS
Gain-Balance (±Full Scale) Range[5]	±0.005% FS
DIGITAL LEVELS	
Inputs	
Low	0.8 V max
High	2.0 V min
Outputs	
Low (@ 4 mA)	0.45 V max
High (@ 100 μA)	2.4 V min
POWER REQUIREMENTS	
Supply Voltages (for Rated Accuracy)	
$\pm V_S$	±15 V (±0.3 V each)
$+V_D$	+5 V (−0.2 V to +0.4 V)
Supply Current Drain	
@ ±15 V	
After Warm-Up	+55 mA, −70 mA
During Warm-Up	150 mA
@ +5 V	175 mA
ENVIRONMENTAL	
Rated Performance	10°C to +50°C, 70% RH
Operating	0 to +70°C
Storage	−25°C to +70°C
MECHANICAL	
Size	3.7" × 5.2" × 0.53" max
Shielding	Electrostatic, 6 Sides Electromagnetic, 5 Sides
Weight	170 grams

NOTES
[1]Integral Nonlinearity is specified over the entire input span (NOMINAL FULL-SCALE +10% Overrange). It is specified using the "End Point" definition, where the error is measured after removing the offset error and the gain errors at plus and minus full scale.
[2]FSR means Full Scale Range which = 10 volts.
[3]Single ended, ground referred.
[4]Average trend line.
[5]Adjustment is performed via user accessible 10-turn trim potentiometer.
[6]Integration Time is selectable to either 1/30 sec for 60 Hz rejection, or 1/25 sec for 50 Hz rejection.
[7]The Nominal Analog Input Voltage Range is ±5V, but the AD1175 may be calibrated for input voltages from ±4.7 V to ±5.6 V and maintain specified accuracy over the entire range, including a 10% on-scale overrange. Therefore, input voltages of up to ±6.16 V will be accurately converted when calibrated for ±5.6 V Nominal input.
[8]Converter section GAIN is digitally adjustable, via the data bus, in steps of 0.009% from <4.7 to >5.6V FS. A user accessible 10-turn trim potentiometer is also provided for fine GAIN adjust (±0.006% range). All units are factory calibrated for ±5 V Nominal Full Scale to within ±50 μV.
[9]Input Bandwidth specifications are for true integration without clipping.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE: SEE PAGE 3-161 FOR RECOMMENDED SOCKET.
SEE PAGE 3-166 FOR EVALUATION BOARD.

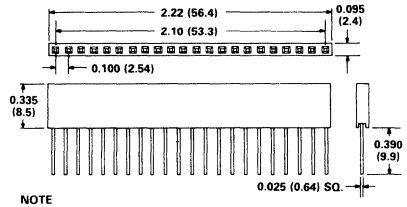
ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

PIN DESCRIPTIONS

PIN	SIGNAL	DESCRIPTION
4	CONV CMD	External Convert Command
5	RESET	Reset Internal Microcomputer Following Power-Up
6	60Hz/$\overline{50Hz}$	When Set Low, Integration Time is 1/25 sec When Set High, Integration Time is 1/30 sec
7	DO NOT CONNECT	Used Only for Factory Test
8	+5V	Digital Power Supply
9, 10	DIG GND	Digital Ground (Both Pins are Tied Together Internally)
11-18	DB0-DB7	Bidirectional Data Bus (LSB-MSB)
19	A0	Address, Bit Zero
20	A1	Address, Bit One
21	$\overline{RD}$	READ
22	$\overline{WR}$	WRITE
23	$\overline{CS}$	CHIP SELECT
24	$\overline{BUSY}$	BUSY, Responding to a Bus Command
25	DATA RDY	DATA READY
48, 49	±15V RTN & GND	Analog Power Ground and Case (Tied Together Internally)
58	ANA IN LO	Analog Input, Low
59	ANA IN HI	Analog Input, High
61	−15V	Negative Analog Power Supply
62	SIGNAL RTN	Signal Return (Non-Current Carrying Ground)
63	+15V	Positive Analog Power Supply
64	USER REF OUT	Buffered Output of Reference at REF IN
65	REF IN	Reference Input, Normally Connected to REF OUT
66	REF OUT	Internal +6.95V Reference Output, Unbuffered

SAMTEC Part Number SSQ-122-03-G-S (2 Each Required Per AD1175)
Available direct from the manufacturer or through distributors.



NOTE
0.025" (0.64) SQUARE SOCKET STRIP, 22-PIN POSITIONS GOLD PLATED CONTACTS AND PINS, BODY IS MOLDED DUPONT RYNITE PET POLYESTER.

ARCHITECTURAL OVERVIEW

The AD1175 is a complete, precision analog-to-digital converter. It consists of three major elements: a linearized, auto-zeroed integrator, a single-chip microcomputer, and a custom CMOS controller/bus interface chip. (See Figure 1 AD1175 Functional Block Diagram.)

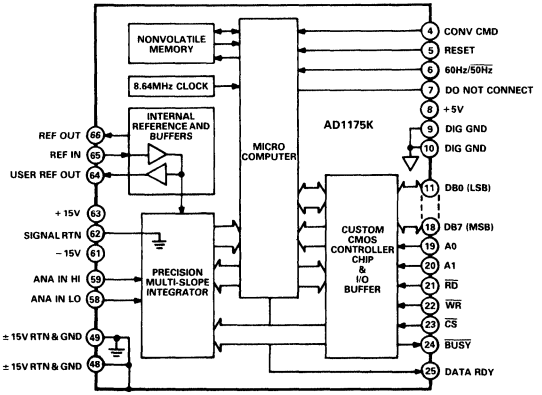


Figure 1. AD1175 Functional Block Diagram

The conversion process is similar to the classic dual-slope technique, where the input signal is integrated during a whole number of line cycles (for line noise rejection) and then a digital measurement is made of the time required for a known reference voltage to drive the integrator output back to zero (i.e., to zero charge). Since the process begins with zero charge in the integrator, and also ends there, we can express this function as follows:

$$\text{CHARGE IN} = \text{CHARGE OUT}$$

$$\text{WHERE CHARGE} = \int_0^t I\,dt = \frac{1}{R}\int_0^t V\,dt$$

$$\text{OR} \ldots \frac{1}{R_{INT}}\int_0^{T_{SIG}} V_{SIG}\,dt = \frac{1}{R_{INT}}\int_0^{T_{REF}} V_{REF}\,dt$$

$$\text{OR} \ldots \int_0^{T_{SIG}} V_{SIG}\,dt = V_{REF} \times T_{REF} \text{ (SINCE } V_{REF} = \text{CONSTANT)}$$

$$\text{OR} \ldots \frac{\int_0^{T_{SIG}} V_{SIG}\,dt}{T_{SIG}} = \text{AVG. } [V_{SIG}] = \frac{V_{REF} \times T_{REF}}{T_{SIG}}$$

$$\text{HENCE} \ldots \frac{\text{AVG. } [V_{SIG}]}{V_{REF}} = \frac{T_{REF}}{T_{SIG}} \begin{cases} \text{WHERE } T_{REF} \text{ IS MEASURED AND} \\ V_{REF} \text{ \& } T_{SIG} \text{ ARE CONSTANT} \end{cases}$$

Principle of Dual-Slope Conversion

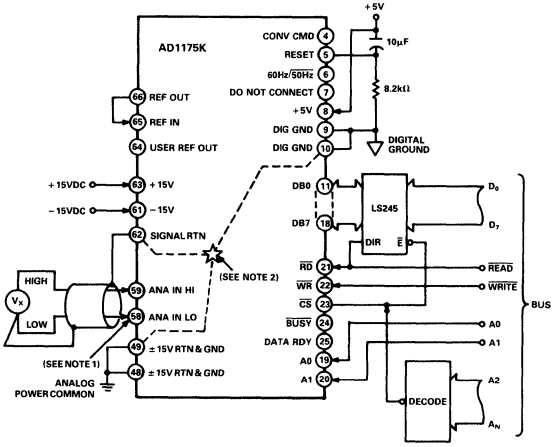
Therefore, the ratio of the signal measured (its average value) to the reference voltage, is equal to the ratio of the *measured time* (to force the integrator back to zero charge) to the signal integration time (which is held constant).

The AD1175 repeats the above sequence ten times during the first 33-1/3 milliseconds of each conversion for a 60 Hz integrate selection (40 milliseconds for a 50 Hz integrate selection). The 10 individual readings together with the result of a final, slow (about 6 ms) vernier reference integration are summed. The numeric result is then placed in the addressable output latches and DATA is indicated as AVAILABLE. During the next ten milliseconds, the integrator is reset and AUTO-ZERO nulls out offset errors in preparation for the next conversion.

The device status is indicated by the addressable STATUS byte (busy, converting, data available, etc.). DATA READY and $\overline{\text{BUSY}}$ are also indicated by logic levels at Pins 25 and 24, respectively.

SIGNAL INPUT CONNECTIONS

The ANA IN HI and ANA IN LO pins comprise a true, high-impedance, high CMRR, differential input pair. ANA IN LO must be within ±100 mV of SIGNAL RTN (Pin 62). The ANA IN LO pin is used to remote sense the source low (ground) to minimize system ground current related errors. Both *HI AND LO* SIGNALS MUST HAVE A BIAS CURRENT PATH BACK TO *SIGNAL RTN*. Figure 2 details the proper connections.



NOTES
1. BOTH HIGH AND LOW SIGNALS MUST HAVE A BIAS CURRENT PATH BACK TO GROUND AT THE AD1175. "ANA IN LO" SHOULD REFERENCE TO GROUND (SIGNAL RTN) AT THE SIGNAL SOURCE, VIA A MINIMUM OF RESISTANCE.
2. "DIG GND" AND "±15V RTN & GND" ARE STAR CONNECTED WITHIN THE CONVERTER, AND INTENDED TO BE SEPARATE OUTSIDE OF THE CONVERTER. HOWEVER, IF ±15V AND +5V POWER SHARE A SINGLE COMMON RETURN, THEN THAT COMMON MUST BE CONNECTED TO THE "±15V RTN & GND" PIN WHICH MUST BE CONNECTED VIA HEAVY COPPER TO THE "DIG GND" PIN. "SIGNAL RTN" (PIN 62) IS THE "NON-CURRENT CARRYING" GROUND, ONLY TO BE USED AS SHOWN AND AS GROUND REFERENCE FOR AN EXTERNALLY SUPPLIED REFERENCE SOURCE.

Figure 2. AD1175 Bus Driven Interface

Printed circuit board layout should insure that both analog inputs (Pins 58 and 59) are guarded by copper which is tied to SIGNAL RTN (Pin 62) on the front *and* back of the board.

Note that an offset error of up to one LSB per 120 Ω of source impedance can occur, due to input bias current, which may approach 20 nA at elevated temperatures.

REFERENCE CONNECTIONS

A very stable 6.95 V ±2% internal reference is filtered and brought out to REF OUT (Pin 66) of the converter. This output should be tied to REF IN (Pin 65) to accomplish the specifications for initial absolute accuracy. REF OUT is a high impedance output and should not be loaded in any way other than by REF IN (Pin 65). A buffered version of the reference applied to REF IN, and that which is used by the converter, is available at USER REF OUT (Pin 64).

When making ratiometric measurements, where the source excitation is derived from the converter reference, use the reference signal present at USER REF OUT (Pin 64). The load applied to Pin 64 should not exceed two milliamps. If an external reference source is to be used, it should be applied to REF IN (Pin 65).

POWER SUPPLIES AND GROUNDS

The power supply pins are all well bypassed internally to their respective common or ground pins. The converter is very tolerant of dc and low frequency noise (≤100 s of Hz) on any of the supplies, as evidenced in the power supply rejection specifications. High frequency noise (≥1 MHz) in excess of 10 mV on the ±15 V supplies could, however, degrade the converter's performance.

To avoid large, digital-rate, circulating ground currents, the system's analog supply common and that of the digital supply should be kept separate and then tied together at the converter by a heavy track (to supplement that which is internal to the converter) from ±15 V RTN & GND (Pins 48 and 49) to DIG GND (Pins 9 & 10).

If the logic supply and analog supply share a single common, then that common should be brought to ±15 V RTN & GND (Pins 48 and 49) and then from these pins a heavy track should be run to DIG GND (Pins 9 & 10).

RESET (Pin 5; Input)

After power-up and before access may be made to the converter, a reset of the internal microcomputer must be accomplished. The RESET (Pin 5) may be driven from an external source, such as may exist in most computer-based systems, or it may be connected to a simple RC circuit which will automatically generate a reset sequence upon power-up. See Figure 2 for the recommended circuit.

When driven from an external source, RESET must be held high for a minimum of 3 microseconds, but must not terminate before the +5 V logic supply and the ±15 V analog supply have been stable (>+4.7 V, and >±11 V) for 300 microseconds.

60 Hz/ $\overline{50\ Hz}$ (Pin 6; Input)

Pin 6 of the module selects either 33-1/3 milliseconds or 40 milliseconds for the signal integration time. This input is internally pulled up to 5 V via 10 kΩ and may be left open for 60 Hz normal mode rejection. The pin should be connected to Digital Ground for operation in a 50 Hz line frequency environment.

CONV CMD (Pin 4; Input)

A negative logic transition on this input causes a MODCON conversion to occur (see CALIBRATION section). A minimum hold time of 1.5 μs is required at both the High and the Low states, to operate properly. The $\overline{BUSY}$ output (Pin 24) will not respond, and BUSY (Bit 0) of the STATUS word will *not* be indicated, but all other bits of the STATUS word will be active. DATA RDY (Pin 25) will occur per Figure 8.

This input is provided to allow externally triggered conversions which will use the temporarily programmed gain and offset values (or the start-up defaults if no changes have been made).

DATA RDY (Pin 25; Output)

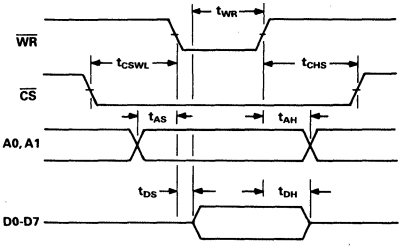
This signal will go to logic "1" when any conversion's new data has become stable in the output latches. It will remain high for the duration of the auto-zero phase (about 10 milliseconds) and go low at the end of that phase (at the end of BUSY).

$\overline{BUSY}$ (Pin 24; Output)

When a COMMAND byte is written to the microprocessor compatible port, this line is set low and remains low for the duration of the converter's response to that command. It is the opposite state of the BUSY bit within the STATUS byte.

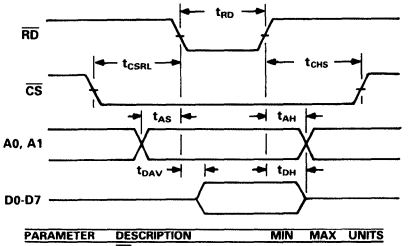
THE BUS INTERFACE

The AD1175's 8-bit microprocessor-compatible interface consists of an 8-bit, latched ,tri-stated, bidirectional port and its associated control lines: Chip Select ($\overline{CS}$), READ ($\overline{RD}$), WRITE ($\overline{WR}$) and two address bits (A1 and A0). Timing requirements for the bus interface are shown in Figure 3, and the operation of the interface is shown in Figure 4.



PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{WR}	$\overline{WR}$ Pulse Width	0.1	20	μs
t_{CSWL}	Chip Select to $\overline{WR}$ Low	0		ns
t_{CHS}	Chip Select Hold Time	0		ns
t_{AS}	Address Setup time	10		ns
t_{AH}	Address Hold Time	0		ns
t_{DS}	Data Setup Time	−∞	5	μs
t_{DH}	Data Hold Time	20		ns

Write Cycle Timing Requirements



PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{RD}	$\overline{RD}$ Pulse Width	150		ns
t_{CSRL}	Chip Select to $\overline{RD}$ Low	0		ns
t_{CHS}	Chip Select Hold Time	0		ns
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	0		ns
t_{DAV}	Data Valid Time		100	ns
t_{DH}	Data Hold Time		80	ns

Read Cycle Timing Requirements

Figure 3. Interface Timing Requirements

	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	FUNCTION
READ	L	L	H	H	H	High CONV Data Byte READ
	L	L	H	H	L	Mid CONV Data Byte READ
	L	L	H	L	H	Low CONV Data Byte READ
	L	L	H	L	L	STATUS READ
WRITE	L	H	L	H	H	Unused
	L	H	L	H	L	Unused
	L	H	L	L	H	PARAMETER WRITE
	L	H	L	L	L	COMMAND WRITE
	X	H	H	X	X	DEVICE NOT SELECTED
	H	X	X	X	X	

NOTE THAT X = DON'T CARE

Figure 4. Bus Control Functions

	BIT # MSB 23	22	21	20	19	18	17	16	15	14	13	//	5	4	3	2	1	LSB 0	HEX
POS. OVERLOAD	1	1	1	1	1	1	1	1	1	1	1	//	1	1	1	1	1	1	FF,FF,FF
+1.25 × FULL SCALE	0	1	1	0	1	0	0	0	0	0	0	//	0	0	0	0	0	0	68,00,00
+FULL SCALE	0	1	1	0	0	0	0	0	0	0	0	//	0	0	0	0	0	0	60,00,00
+1/2 SCALE	0	1	0	1	0	0	0	0	0	0	0	//	0	0	0	0	0	0	50,00,00
ZERO	0	1	0	0	0	0	0	0	0	0	0	//	0	0	0	0	0	0	40,00,00
−1/2 SCALE	0	0	1	1	0	0	0	0	0	0	0	//	0	0	0	0	0	0	30,00,00
−FULL SCALE	0	0	1	0	0	0	0	0	0	0	0	//	0	0	0	0	0	0	20,00,00
−1.25 × FULL SCALE	0	0	0	1	1	0	0	0	0	0	0	//	0	0	0	0	0	0	18,00,00
NEG. OVERLOAD	1	1	1	1	1	1	1	1	1	1	1	//	1	1	1	1	1	1	FF,FF,FF

Figure 5. Data Format

3

OUTPUT DATA FORMAT

The result of a conversion is made available in three 8-bit bytes (addressed as shown in Figure 4). The numeric result is presented as an offset binary number, where the offset value is equal to 2e22 (40,00,00 Hex), i.e., zero volts input yields this numerical output. Therefore, the nominal plus and minus full scale are 2e22 ±2e21, or 60,00,00 Hex and 20,00,00 Hex, respectively. For inputs greater than approximately 1.3× nominal full scale, the converter will indicate an overload error (Bit 5 of the STATUS byte) and will also flag the occurrence by forcing all "1s" in the conversion result, i.e., FF,FF,FF Hex. Bit 23 (MSB) cannot be a "1" for any legitimate conversion result, so that bit is used to flag an overload. The data format is depicted in Figure 5.

COMMAND BYTE

The COMMAND BYTE allows eight different instructions to be given. Five of these will require that a parameter be loaded into the PARAMETER* register prior to writing the command register. The commands are written at address 00 (ADDRESS lines A1 and A0, Pins 20 and 19, respectively) while a parameter is written to address 01. See Figure 4 for Bus Control Functions. Figure 8 details command timing requirements.

The commands are described below, preceded by an opcode name and the digital code (in hex). Figure 6 summarizes each command and its execution time.

DEFCON [00]

DEFault CONversion initiates a conversion, using the gain and offset values which are stored in the nonvolatile memory (power-up defaults).

MODCON [01]

MODified CONversion initiates a conversion using the gain and offset values which have been modified (since power-up) as in commands 02 through 07 below.

NEWOS [02]

NEW OffSet subtracts the result of the last conversion from all subsequent MODCON conversions, i.e., *acquire a new system offset*. The maximum range of this offset is 65,536 codes (= ±75 mV). Attempts to acquire an offset outside of this range will be ignored and BIT 5 and BIT 6 (Overload and command byte ERRor) will be set in the STATUS byte.

INCROS [03]

INCRease OffSet alters the offset (in LSBs) used by MODCON in the *positive* direction by a number between zero and 255 (decimal), which has already been written to PARAMETER*.

*The PARAMETER register retains the last word written to it. Any subsequent commands will repeatedly use that PARAMETER until it is updated.

This may be performed repeatedly until a maximum offset of +75 mV has been reached, as indicated by an Overload/BIT 5 response in the STATUS byte.

DECROS [04]

DECRease OffSet alters the offset (in LSBs) used by MODCON in the negative direction by a number between zero and 255 (decimal), which has already been written to PARAMETER*. This may be performed repeatedly until a maximum offset of −75 mV has been reached, as indicated by an Overload/BIT 5 response in the STATUS byte.

INCGAN [05]

INCrease GAiN by $N \times 0.01\%$, where N (a decimal number between 0 and 255) has already been written to PARAMETER*. This may be performed repeatedly until a maximum gain (<4.7 V full scale) has been reached, as indicated by an Overload/BIT 5 response in the STATUS byte. Further INCGAN commands will have no other effect.

DECGAN [06]

DECrease GAiN by $N \times 0.01$, where N (a decimal number between 0 and 255) has already been written to PARAMETER*. This may be performed repeatedly until a minimum gain (>5.6 V full scale) has been reached, as indicated by an Overload/BIT 5 response in the STATUS byte. Further DECGAN commands will have no other effect.

UPDATE [07]

Takes the current modified gain and offset values and writes them to nonvolatile memory as the new start-up defaults. To enable this function, decimal 165 (A5 in hex) must first be loaded into PARAMETER* – failure to do so will result in an ERRor (BIT 6) response in the STATUS byte.

Note: Codes other than 00 through 07 will do nothing, except cause an ERRor (BIT 6) response in the STATUS byte.

MNEMONIC	FUNCTIONAL DESCRIPTION	EXECUTION TIME (APPROXIMATE)
DEFCON	Initiate a Conversion Using the Power-Up Default Offset and Gain	50ms
MODCON	Initiate a Conversion Using the Modified Offset and Gain Values	50ms
NEWOS	Subtract System Offset (Last Conv. Result) from All MODCON Conversions	120µs
INCROS	Increase the Offset Used by MODCON Conversions	110µs
DECROS	Decrease the Offset Used by MODCON Conversions	110µs
INCGAN	Increase the Gain Used by MODCON Conversions	135µs
DECGAN	Decrease the Gain Used by MODCON Conversions	135µs
UPDATE	Write Most Recent Modified Offset & Gain Values to Nonvolatile Memory	48ms

Figure 6. Synopsis of Commands

THE STATUS BYTE

The STATUS byte contains eight bits of information about the current status of the AD1175. This byte may be examined by the host processor at any time. The individual bits in the status byte are assigned the following functions:

BIT 0 The BUSY bit is always set when the COMMAND BYTE is written, and cleared when the initiated routine has terminated. BUSY is also indicated at $\overline{\text{BUSY}}$ (Pin 24) of the module.

BIT 1 The CONVerting bit is set when the converter is in the active process of converting and computation. It is initiated by writing DEFCON or MODCON to the COMMAND-BYTE, or by a negative transition at CONV CMD (Pin 4).

BIT 2 The Data AVailable bit indicates that a new conversion is complete and the result is in the output latches. This bit sets to "1" at the conclusion of the converting process and remains "1" for the remainder of the minimum AUTO-ZERO time (about 10 milliseconds). It is reset to "0" at the end of BUSY.

BIT 3 The MODified bit, when set to "1," means that modified gain and offset values are being used for the current conversion; i.e., a conversion initiated by MODCON or an external signal at CONV CMD (Pin 4).

BIT 4 The VALue bit responds to COMMANDS 02 through 07 by setting to "1" at the end of BUSY, and remains until the next write to the COMMAND byte. This bit signals that a gain or offset value used by MODCON has been altered, or that the current MODCON gain and offset values have been loaded to nonvolatile memory as the new power-up defaults.

BIT 5 The Overload bit will be set following any conversion where the integrator has been exposed to an overload voltage. Following commands 03 through 06, it indicates that a parameter (gain or offset) has been incremented to its maximum or minimum possible value (note that further attempts to increment that parameter will not cause an overflow or underflow). Also, following NEWOS (02) command, this bit implies that an attempt was made, and ignored, to acquire an offset outside of the allowable range of ±75 mV.

BIT 6 The ERRor bit indicates one of the following: *1.* A COMMAND-BYTE was written which was not within the allowable range of 00 to 07. *2.* An update (07) command was attempted without the KEY number (165 decimal) having first been written to PARAMETER at ADDRESS 01. *3.* A NEWOS (02) command was attempted for a value outside the permissible range of ±32,768 codes (>75 mV) from zero.

BIT 7 The WaRMUP bit flags the three second time-out taken by the converter following RESET, to allow the reference and auto-zero circuits to settle. The converter will *not* convert during this time.

B7	B6	B5	B4	B3	B2	B1	B0
WRMUP	ERR	OL	VAL	MOD	DAV	CONV	BUSY

Figure 7. The Status Byte

CALIBRATION

The AD1175 is factory calibrated for plus and minus full scale (2e21) to be within ±50 μV of five volts, absolute. Since the converter will operate within specifications for inputs up to ten percent over nominal full scale, those inputs between ±5.5 V will be converted accurately. (See Figure 9 for typical linearity vs. input voltage.)

To correct for system offset voltage (particularly larger offset voltages – up to ±75 mV) the NEWOS (03) command subtracts the result of the last conversion from all subsequent MODCON conversions. If source noise is a concern when making the offset adjustment, follow a single NEWOS command with multiple MODCON conversions, average the results and adjust offset incrementally using the INCROS (03) or DECROS (04) commands.

The INCGAN 05 and DECGAN 06 commands are the *coarse gain* increment and decrement controls, respectively. The minimum gain attainable will require greater than 5.6 V to achieve a full-scale output. At maximum gain, less than 4.7 V will be required to yield a full-scale indication. The user accessible GAIN ADJ potentiometer is the vernier, or *fine gain* trim (10 turns, with a total adjustment range of about ±0.006 FS).

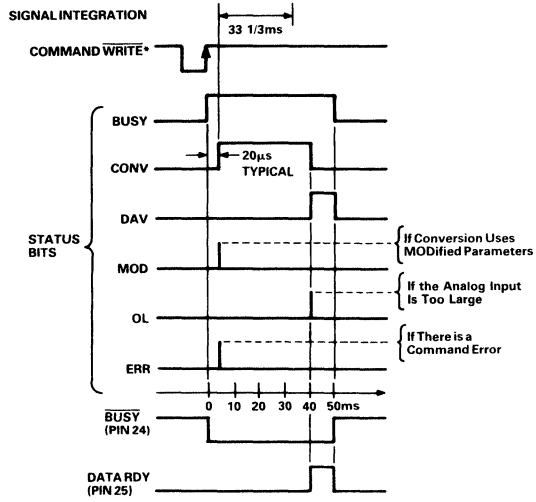
The modified offset and gain resulting from commands 02, 03, 04, 05 and 06 are used only when conversions are initiated by MODCON (command 01), or conversions triggered by a negative logic transition at the CONV CMD (Pin 4 of the converter). This pin requires a minimum hold time of 1.5 μs at both the High and the Low states in order to operate properly.

The GAIN ADJ potentiometer changes the overall gain for both positive and negative inputs. The BAL ADJ potentiometer changes the gain for positive inputs only and allows setting of plus and minus full-scale tracking to within ±1 ppm.

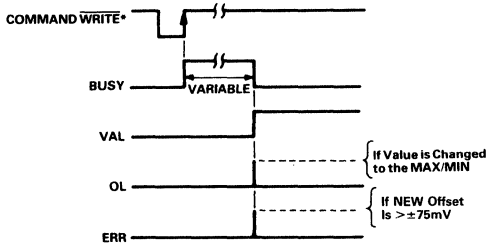
To Calibrate the AD1175:

1. Attach a calibration source and set its output to zero volts.
2. Perform MODCON conversions and null out any observed offset (via external computation, or by executing one or more of the AD1175's offset controlling commands: INCROS, DECROS and NEWOS).
3. Set the GAIN ADJ potentiometer fully clockwise (10 turns, i.e., maximum gain).
4. Apply a negative full-scale calibration voltage (−4.7 V to −5.6V).
5. Using the INCGAN or DECGAN command, coarse adjust the gain such that a subsequent MODCON conversion yields a result just larger than minus full scale. In other words, a subsequent DECGAN by 01 would just yield a result that is less than or equal to minus full scale.
6. Adjust the GAIN ADJ potentiometer to yield the precise value desired by turning counterclockwise and observing conversion results. When the correct gain is reached, rotate the potentiometer about 3 degrees in the opposite direction to remove the tension from its wiper.
7. Switch the polarity of the calibration source to positive.
8. Adjust the BAL ADJ potentiometer to yield the same gain as that achieved in Step 6 above.
9. Save the new offset value and coarse gain value, if you want them to become the power-up defaults, by performing UPDATE (Command 07).

Note: See the COMMAND BYTE section for details of command operation.

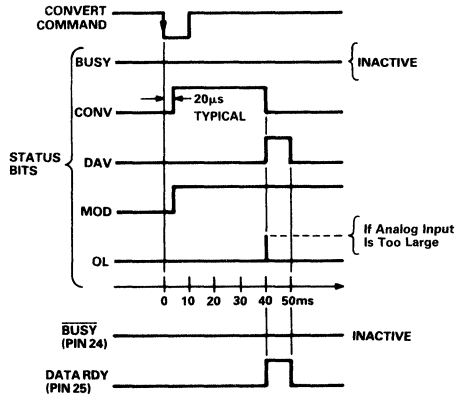


a. *COMMAND BYTE Initiated Conversion*



*NOTE: COMMAND WRITE Always Causes Rewrite of the Entire STATUS Byte. For Example: If the Overload Bit (OL) is Set as the Result of a Conversion, It Will Remain Set in the STATUS Byte Until the Next COMMAND WRITE.

b. *COMMAND BYTE Initiated Change to Gain and/or Offset*



c. *CONVERT COMMAND (Pin 4) Initiated Conversion*

Figure 8. Command Timing Requirements

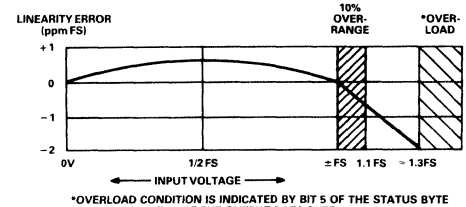


Figure 9. Typical Linearity Transfer Function

FACTORY TESTING

Each AD1175 converter is factory calibrated via test apparatus designed and constructed by Analog Devices. The heart of the test system is a digitally programmable voltage reference capable of sub-ppm accuracy and stability. Calibration of the test system is verified daily using the highest precision instruments commercially available, e.g., FLUKE* model 720A Kelvin Varley voltage divider (accurate to within ±0.1 ppm[1]) and model 732A dc secondary voltage standard (accurate to within ±1.5 ppm of the international volt[1]).

IBM PC INTERFACE

Figure 10 is an example of an AD1175/IBM interface suitable for the IBM PC, XT or AT** personal computers. In this case, the AD1175 is interfaced in the I/O space; a DIP switch controls the specific location of the AD1175 within the available address space.

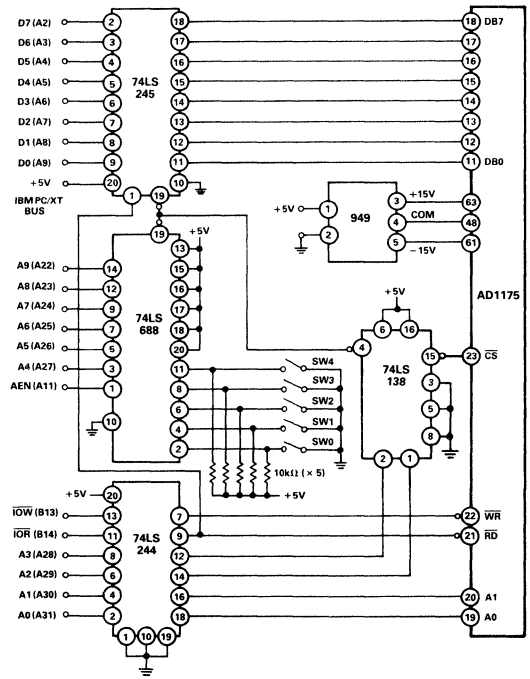


Figure 10. AD1175 to IBM PC/XT/AT Interface

*FLUKE is a registered trademark of John Fluke Manufacturing Company, Inc.

**IBM PC/XT/AT is a trademark of International Business Machines Corp.

[1]Traceable to the NATIONAL BUREAU OF STANDARDS.

INTERFACING TO AN 8051 MICROCONTROLLER

Figure 11 shows how the AD1175 may be interfaced to an 8051 microcontroller using a technique commonly called "byte banging," where the control lines and data bus of a device are manipulated under firmware control. This "byte banging" technique can be adapted to most microprocessors and is useful in situations where a conventional bus structure is either nonexistent or unavailable for use.[1]

The AD1175's data bus is connected to the 8051 using I/O lines P2.0 through P2.7. The address lines A0 and A1 are connected to I/O lines P1.0 and P1.1 respectively. The RD/ and WR/ lines are connected to P1.2 and P1.3. The CS/ line of the AD1175 is grounded when it is the only device connected to the 8051, but multiple AD1175s could easily be connected in the same way if each CS/ line were separately controlled.

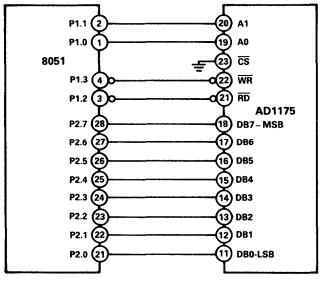


Figure 11. Simple AD1175 to 8051 Interface

To initialize the interface, first write "1"s to the port pins connected to the data bus and the RD/ and WR/ control lines. This puts the 8051 I/O lines into a lightly "pulled up" state, simulating a tri-stated condition on the bus to insure that neither RD/ nor WR/ are selected:

```
INIT:   SETB  P1.2        ;DISABLE RD/
        SETB  P1.3        ;AND WR/
                          ;
        MOV   P2, #OFFH   ;SET P2 TO ALL ONES
```

To write a command to the AD1175, first set the state of the P1.1 and P1:0 lines for the address corresponding to the byte to be written to (00=COMMAND BYTE, 01=PARAMETER). Set the P2 port to the command data, then strobe the WR/ line by first clearing the P1.3 line and then setting it:

```
WRCMD:  CLR   P1.0        ;FIRST CLEAR A0 AND A1
        CLR   P1.1        ;TO POINT TO CMD BYTE
                          ;
        MOV   P2, #00     ;00 IS THE OPCODE FOR
                          ;A DEFAULT MODE
                           CONVERSION
                          ;
        CLR   P1.3        ;STROBE THE WR/ LINE
        SETB  P1.3        ;ONE TIME
                          ;
        MOV   P2, #OFFH   ;SET DATA BUS TO
                          ;ALL ONES
```

To read a byte from the AD1175, first set the P1.0 and P1.1 lines to point to the address of the byte desired. Bring the RD/line low, reading the contents of P2. Return the RD/ line high:

```
RDSTAT: CLR   P1.0        ;POINT TO STATUS BYTE
        CLR   P1.1        ;
                          ;
        CLR   P1.2        ;BRING RD/ LINE LOW
        MOV   A,P2        ;READ CONTENTS OF BUS
        SETB  P1.2        ;RESTORE RD/ LINE HIGH
```

[1]Note that the 8051 microcontroller *does* contain a conventional bus structure; the "byte banging" interface shown here is presented as an example of an alternative technique.

AC5005

. . . an IBM PC/XT/AT Compatible Evaluation Board for the AD1175K

FEATURES

- **Compatible to IBM PC/XT/AT* or Equivalent**
- **Menu-Driven Demonstration Software**
- **Full Documentation**
  - **Example Listings of BASIC Programs**
  - **Schematic**
  - **Assembly Drawing**
- **Complete Set of Tools to Evaluate the AD1175K 22-Bit Resolution Integrating A/D Converter**

APPLICATIONS

- **Laboratory DVM**
- **Product Test and Measurement**
- **Analytical Instrumentation**
- **Material Analysis**
- **Seismic Analysis**

GENERAL DESCRIPTION

The AC5005 is an evaluation board for Analog Devices' AD1175K and is designed to plug directly into the backplane of an IBM PC/XT/AT and compatibles. The AC5005 is offered as a support tool to enable users to easily and quickly evaluate Analog Devices' AD1175K 22-bit multi-slope integrating A/D converter. The AC5005 comes with a demonstration program written in BASICA that completely exercises the functions of the AD1175K and emulates a 6 1/2 digit DVM. The onboard multiplexer allows selection via software from four differential analog input channels. A set of ten digital I/O lines are available to the user for control of lamps and actuators as well as to test switch positions. The AC5005 plugs directly into an IBM PC or compatible. Armed with an IBM PC and an AC5005 evaluation board, the user is ready to execute the demonstration program and evaluate the operation of the AD1175K.

A user's guide provides the user with all the information required to put the AC5005/AD1175K pair into operation. The schematic of the AC5005 is provided as an example of how to interface the AD1175K to a computer bus. The AC5005 is very easy to configure. It has one set of DIP switches to select the board's base address and one set of jumpers to select either 50 Hz or 60 Hz line cycle. All the tools needed to evaluate the AD1175K come with the AC5005. There is even a short example program listing written in BASIC to demonstrate the ease of programming the AD1175K.

PRODUCT HIGHLIGHTS

1. Plugs directly into IBM PC/XT/AT or compatibles.
2. Evaluates the AD1175K 22-bit multi-slope integrating A/D converter without having to build a breadboard or prototype.
3. Comes complete with software and programming examples to exercise all of the AD1175K's functions and emulate a 6 1/2 digit DVM.
4. AC5005 schematic and assembly drawing are provided to be used as examples of how to interface theAD1175K to a microprocessor bus.
5. Turnkey solution for laboratory measurement and analytical instrumentation.

***IBM PC/XT/AT is a trademark of International Business Machines Corp.**

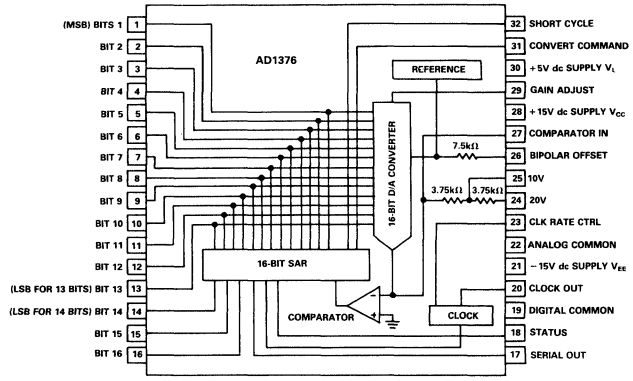
Complete, High Speed 16-Bit A/D Converter

AD1376

FEATURES

Complete 16-Bit Converter with Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits Over Temperature
Fast Conversion – 14μs (14 Bit)
Short Cycle Capability
Parallel and Serial Outputs
Low Power: 645mW Typical
Industry Standard Pin Out

AD1376 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1376 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock and laser-trimmed thin-film components. The package is a compact 32-pin, ceramic DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR, and maximum 14-bit conversion time of 15μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD1376 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD1376 is excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

PRODUCT HIGHLIGHTS

1. The AD1376 provides 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J grade) at 25°C.
2. Conversion time is 14μs typical to 14 bits with short cycle capability, and 16μs to 16 bits.
3. Two binary codes are available on the AD1376 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary twos complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.
5. The AD1376 includes an internal reference and clock, with external clock adjust pin, and a serial output.

SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 volts unless otherwise noted)

Model	AD1376JD	AD1376KD	Units
RESOLUTION	16 (max)	*	Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5, ±10	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	Volts
Impedance (Direct Input)			
0 to +5V, ±2.5V	1.88	*	kΩ
0 to +10V, ±5.0V	3.75	*	kΩ
0 to +20V, ±10V	7.50	*	kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion		
Logic Loading	1	*	LS TTL Load
TRANSFER CHARACTERISTICS[2]			
ACCURACY			
Gain Error	±0.05[3] (±0.2 max)	*	%
Offset Error			
Unipolar	±0.05[3] (±0.1 max)	*	% of FSR[4]
Bipolar	±0.05[3] (±0.2 max)	*	% of FSR
Linearity Error (max)	±0.006	±0.003	% of FSR
Inherent Quantization Error	±1/2	*	LSB
Differential Linearity Error	±0.003	*	% of FSR
POWER SUPPLY SENSITIVITY			
±15V dc (±0.75V)	0.0015	*	% of FSR/% ΔV_S
+5V dc (±0.25V)	0.001	*	% of FSR/% ΔV_S
CONVERSION TIME[6]			
12 Bits	11.5 (13 max)	*	µs
14 Bits	13.5 (15 max)	*	µs
16 Bits	15.5 (17 max)	*	µs
WARM-UP TIME	1 minute	*	Minutes
DRIFT[5]			
Gain	±15 (max)	±5 (±15 max)	ppm/°C
Offset			
Unipolar	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±3 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±0.3 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code			
Temperature Range	0 to 70 (13 Bits)	0 to 70 (14 Bits)	°C
DIGITAL OUTPUT[1]			
(All Codes Complementary)			
Parallel & Serial			
Output Codes[7]			
Unipolar	CSB	*	
Bipolar	COB, CTC[8]	*	
Output Drive	5	*	LSTTL Loads
Status		Logic "1" During Conversion	
Status Output Drive	5 (max)	*	LSTTL Loads
Internal Clock[9]			
Clock Output Drive	5 (max)	*	LSTTL Loads
Frequency	1040	*	kHz
POWER SUPPLY REQUIREMENTS			
Power Consumption	645 (850 max)	*	mW
Rated Voltage, Analog	±15 ±0.5 (max)	*	V dc
Rated Voltage, Digital	+5 ±0.25 (max)	*	V dc
Supply Drain +15V dc	+16	*	mA
Supply Drain −15V dc	−21	*	mA
Supply Drain +5V dc	+18	*	mA
TEMPERATURE RANGE			
Specification	0 to +70	*	°C
Operating	−25 to +85	*	°C
Storage	−55 to +125	*	°C

NOTES
[1]Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
[2]Tested on ±10V and 0 to +10V ranges.
[3]Adjustable to zero.
[4]Full Scale Range.
[5]Guaranteed but not 100% production tested.
[6]Conversion time may be shortened with "Short Cycle" set for lower resolution.
[7]CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Twos Complement.
[8]CTC coding obtained by inverting MSB (Pin 1).
[9]With Pin 23, clock rate controls tied to digital ground.
*Specifications same as AD1376JD.
Specifications subject to change without notice.

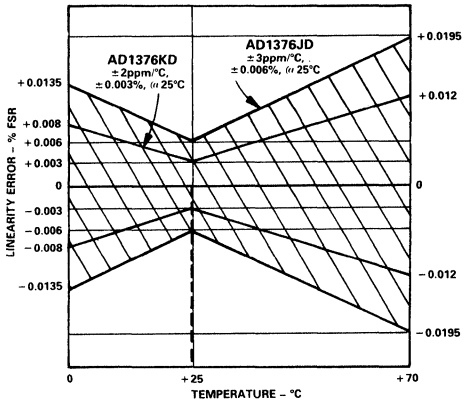


Figure 1. Linearity Error vs. Temperature

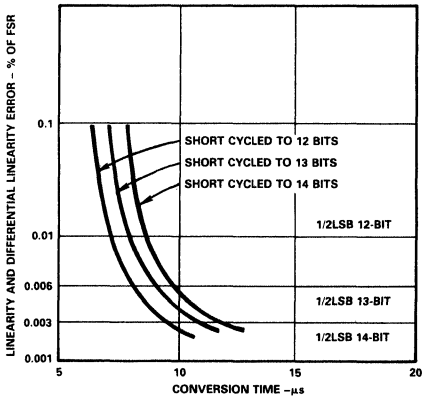


Figure 2. AD1376 Nonlinearity vs. Conversion Time

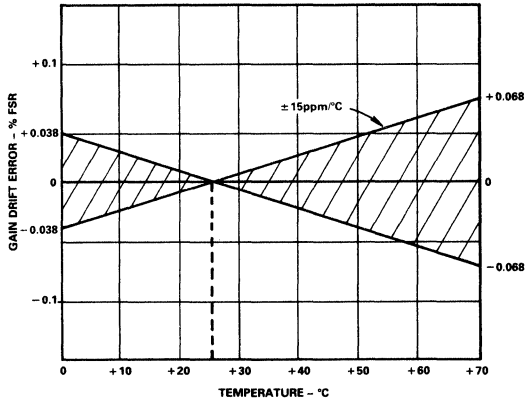


Figure 3. AD1376 Gain Drift Error vs. Temperature

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD1376JD	0.006% FSR	0 to +70°C	Ceramic (DH-32E)
AD1376KD	0.003% FSR	0 to +70°C	Ceramic (DH-32E)

*See Section 14 for package outline information.

THEORY OF OPERATION

The analog continuum is partitioned into 2^{16} discrete ranges for 16-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ± 1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.2% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 5 and 6. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD1376 is specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

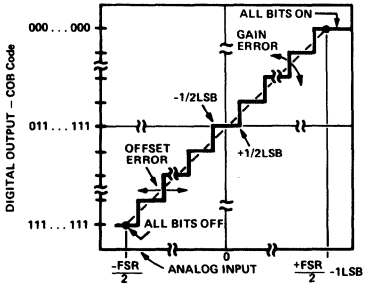


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD1376 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300kΩ resistor to the gain adjust Pin 29 as shown in Figure 5.

If no external trim adjustment is desired, Pin 27 (offset adj) and Pin 29 (gain adj) may be left open.

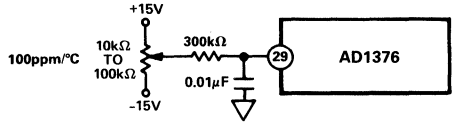


Figure 5. Gain Adjustment Circuit (±0.2% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input Pin 27 for all ranges. As shown in Figure 6, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $32LSB_{14} \times 61ppm/LSB_{14} \times 1200ppm/°C = 2.3ppm/°C$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than $\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

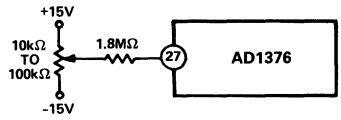


Figure 6. Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used, is shown in Figure 7.

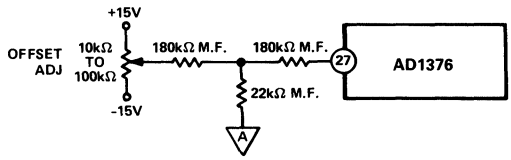


Figure 7. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to Pin 27 should be located close to this pin to keep the pin connection runs short. Comparator Input Pin 27 is quite sensitive to external noise pick-up and should be guarded by analog common.

TIMING

The timing diagram is shown in Figure 8. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

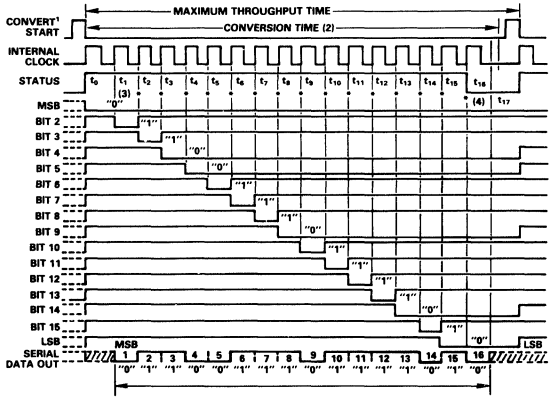


Figure 8. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20ns before the STATUS flag returns to Logic "0," permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 9).

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock

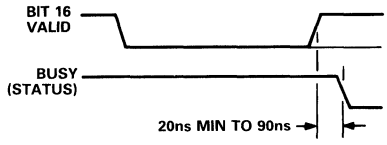


Figure 9. LSB Valid to Status Low

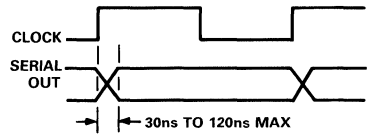


Figure 10. Clock High to Serial Out Valid

edges as shown in Figure 10. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, Pin 32, permits the timing cycle shown in Figure 8 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (timing diagram of Figure 8). Short cycle connections and associated 8-, 10-, 12-, 13-, 14- and 15-bit conversion times are summarized in Table I, for a 933kHz clock.

Resolution Bits	Resolution (%FSR)	Maximum Conversion Time (µs)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	17.1	t_{16}	N/C (Open)
15	0.003	16.1	t_{15}	16
14	0.006	15.0	t_{14}	15
13	0.012	13.9	t_{13}	14
12	0.024	12.9	t_{12}	13
10	0.100	10.7	t_{10}	11
8	0.390	8.6	t_8	9

Table I. Short Cycle Connections

INPUT SCALING

The AD1376 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 11 for circuit details.

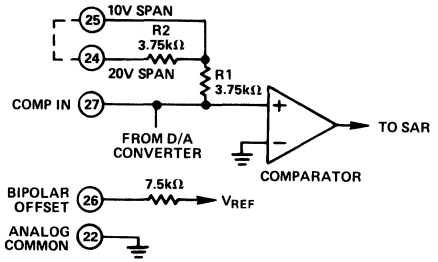


Figure 11. AD1376 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
±10V	COB	27	Input Signal	24
±5V	COB	27	Open	25
±2.5V	COB	27	Pin 27	25
0V to +5V	CSB	22	Pin 27	25
0V to +10V	CSB	22	Open	25
0V to +20V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should be guarded by analog common.

Table II. AD1376 Input Scaling Connections

Code Under Test			Low Side Transition Values			
MSB LSB	Range	±10V	±5V	±2.5V	0 to +10V	0 to +5V
000 . . . 000*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0-1/2LSB	0-1/2LSB	0-1/2LSB	+5V-1/2LSB	+2.5V-1/2LSB
111 . . . 110	− Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V +1/2LSB	0V +1/2LSB

*Voltages given are the nominal value for transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n=8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n=10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n=12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n=13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n=14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n=15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Twos Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

CALIBRATION (14-Bit Resolution Examples)

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 5 and 6, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to $+1LSB_{14}$ = 0.00061V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2LSB = +9.99878V. Adjust Gain for 00000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

−10V to +10V Range: Set analog input to −9.99878V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

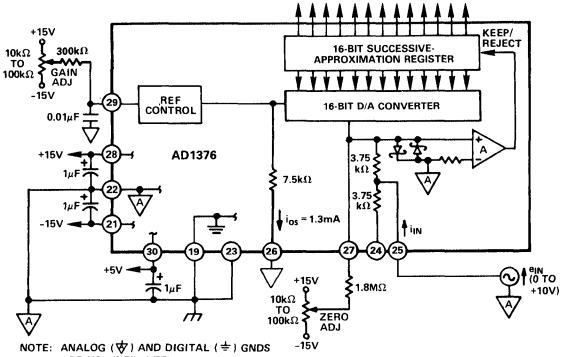


Figure 12. Analog and Power Connections for Unipolar 0 to +10V Input Range

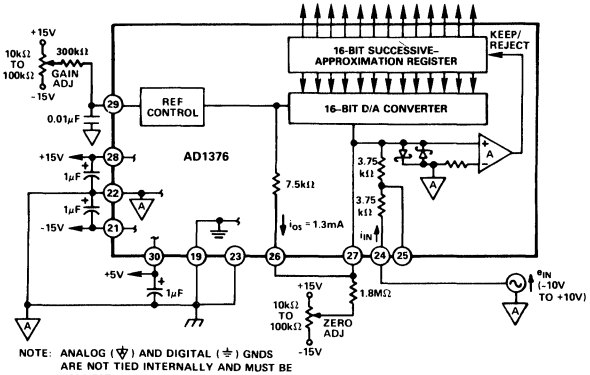


Figure 13. Analog and Power Connections for Bipolar +10V to +10V Input Range

Other Ranges: Representative digital coding for 0 to +10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

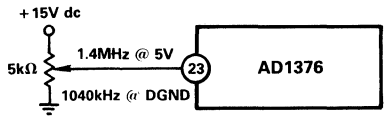


Figure 14. Clock Rate Control Circuit

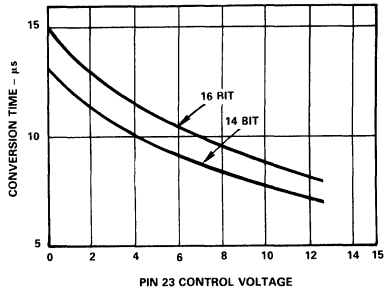


Figure 15. Conversion Time vs. Control Voltage

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (Pins 19 and 22) must be tied together at one point for the AD1376 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD1376. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD1376 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD1376 supply terminals should be capacitively decoupled as close to the AD1376 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

CLOCK RATE CONTROL

The AD1376 may be operated at faster conversion times by connecting the Clock Rate Control (Pin 23) to an external multiturn trim potentiometer (TCR <100ppm/°C) as shown in Figures 14 & 15. The integral linearity and differential linearity errors will vary with speed as shown in Figure 2.

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The AD389 is a companion T/H designed for use with the AD1376 family. The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients, and minimal droop rate.

The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1LSB. The amplitude of 1LSB of the companion A/D converter for a given input range will vary from 610μV for a 14-bit A/D using a 0 to 10V input range to 4.88mV for a 12-bit A/D using a ±10V input range. The hold mode droop rate should produce less than 1LSB of droop in the output during the conversion time of the A/D converter. For 610μV/LSB, as noted in the example above, for a 15μs 14-bit A/D converter, the maximum droop rate will be 610μV/15μs or 40.7μV/μs during the 15μs conversion period.

Minimal thermal tail effects are another requirement of high resolution applications. The self-heating errors induced by the changing current levels in the output stages of T/H amps may cause more than 1LSB of error due to thermal tail effects.

The linearity error should be less than 1LSB over the transfer function, as set by the resolution of the A/D converter. The T/H acquisition time, T/H settling time along, with the conversion time of the A/D converter determines the highest sampling rate. This in turn will determine the highest input signal frequency that can be sampled at twice a cycle.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, with an ideal brickwall low pass filter placed in the signal path prior to the AD389 and A/D converter to eliminate aliasing.

The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible as with the feedthrough spec. The temperature coefficients for drift should be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more above +70°C (+158°F). For commercial and industrial users, these shifts will only appear above the highest temperatures their equipment will ever expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment. Thus, the AD1376 used with a companion AD389 T/H offers high accuracy sampling in high precision applications.

Spec	14 Bit	AD389KD	Units
Aperture Jitter (max)	2.4	0.4	ns
Slew Rate (max w/20V pk-pk signal)	1.26	1.26	V/μs
Feedthrough (1LSB max)	−84.3	−86	dB
Droop Rate (1LSB max in 15μs)	40.7	0.1	μV/μs
Droop Rate (1LSB max in 50μs)	12.2	0.1	μV/μs
Acquisition Time (to ±1LSB max) for 20k Hz Signal w/15μs ADC	10	3-5	μs
Pedestal Shift (max) with Input Signal	−84.3	−86	dB
Gain Temperature Coefficient (max) for ±10°C Ambient Operation	6.1	2.0	ppm/°C
Thermal Tail (max) within 50μs after Hold	1.2	0.1	mV
Linearity Error (max) 1LSB	±0.0061	0.003	% FSR

Table V. T/H Amplifier Requirements vs. AD389 Specs

AD389 in Combination With an	Throughput Rate	Input Frequency Range	Acquisition Time & T/H Settling Time & A/D Conversion Time
AD1376JD (13 Bit)	48.8kHz	dc to 24.4kHz	20.5μs
AD1376KD (14 Bit)	52.6kHz	dc to 26.3kHz	23.0μs

Table VI. T/H & ADC Combinations and Maximum Throughput Rate

Using the AD1376 at Slower Conversion Times

The user may wish to run the AD1376 at slower conversion times in order to synchronize the A/D with an external clock. This is accomplished by running a slower clock than the internal clock into the START CONVERT input. This clock must consist of narrow negative-going clock pulses, as seen in Figure 16. The pulse must be a minimum of 100ns wide but not greater than 700ns. Having a raising edge immediately after a falling edge inhibits the internal clock pulse. This enables the AD1376 to function normally and complete a conversion after 16 clock pulses and serial out in 17 clock pulses. The STATUS command will function normally and switch high after the first clock pulse and will fall low after the 17th clock pulse. In this way an external clock can be used to control the AD1376 at slower conversion times.

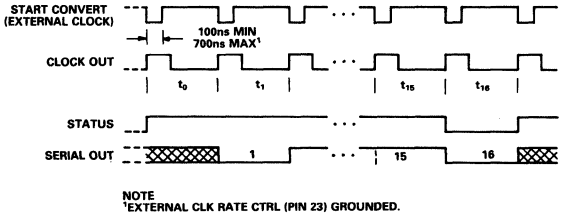


Figure 16. Timing Diagram for Use with an External Clock

ANALOG DEVICES

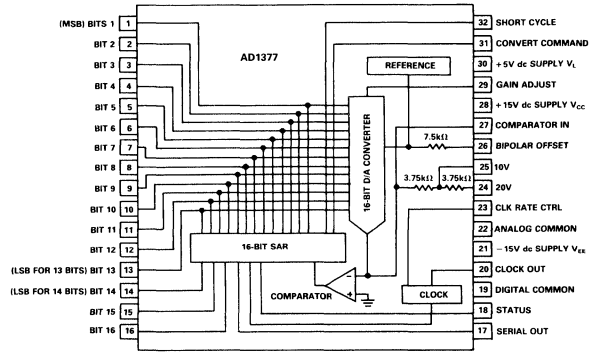
Complete, High Speed 16-Bit A/D Converter

AD1377

FEATURES

Complete 16-Bit Converter with Reference and Clock
±0.003% Maximum Nonlinearity
Fast Conversion – 10μs (16 Bit max)
Short Cycle Capability
Parallel and Serial Outputs
Low Power: 645mW Typical
Industry Standard Pinout

AD1377 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1377 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock and laser-trimmed thin-film components. It is packaged in a compact 32-pin, ceramic DIP. Thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

The AD1377 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD1377 is excellent for use in applications requiring high accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required. A proprietary monolithic D/A converter and laser-trimmed thin-film resistors guarantee a maximum nonlinearity of ±0.003% FSR. The device may be short-cycled to achieve 14-bit conversion in 8μs.

PRODUCT HIGHLIGHTS

1. The AD1377 provides 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J grade) at 25°C.
2. Conversion time is 8μs typical to 14 bits with short cycle capability, and 9μs to 16 bits.
3. Two binary codes are available on the AD1377 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary twos complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.
5. The AD1377 includes an internal reference and clock, with external clock adjust pin, and a serial output.

SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15V, +5V unless otherwise noted)

Model	AD1377JD	AD1377KD	Units
RESOLUTION	16 (max)	*	Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5, ±10	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	Volts
Impedance (Direct Input)			
0 to +5V, ±2.5V	1.88	*	kΩ
0 to +10V, ±5.0V	3.75	*	kΩ
±10V	7.50	*	kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion		
Logic Loading	1	*	LS TTL Load
TRANSFER CHARACTERISTICS[2]			
ACCURACY			
Gain Error	±0.05[3] (±0.1 max)	*	%
Offset Error			
Unipolar	±0.025[3] (±0.1 max)	*	% of FSR[4]
Bipolar	±0.025[3] (±0.1 max)	*	% of FSR
Linearity Error (max)	±0.006	±0.003	% of FSR
Inherent Quantization Error	±1/2	*	LSB
Differential Linearity Error	±0.003	*	% of FSR
POWER SUPPLY SENSITIVITY			
±15V dc (±0.75V)	0.0015	*	% of FSR/% ΔV_S
+5V dc (±0.25V)	0.001	*	% of FSR/% ΔV_S
CONVERSION TIME[5]			
14 Bits	8.75 max	*	μs
16 Bits	10 max	*	μs
WARM-UP TIME	1 minute	*	minutes
DRIFT[6]			
Gain	±15 (max)	±5 (±15 max)	ppm/°C
Offset			
Unipolar	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±3 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±0.3 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code			
Temperature Range	0 to 70 (13 Bits)	0 to 70 (14 Bits)	° C
DIGITAL OUTPUT[1]			
(All Codes Complementary)			
Parallel & Serial			
Output Codes[7]			
Unipolar	CSB	*	
Bipolar	COB, CTC[8]	*	
Output Drive	5	*	LSTTL Loads
Status		Logic "1" During Conversion	
Status Output Drive	5 (max)	*	LSTTL Loads
Internal Clock[9]			
Clock Output Drive	5 (max)	*	LSTTL Loads
Frequency	1750	*	kHz
POWER SUPPLY REQUIREMENTS			
Power Consumption	600 (800 max)	*	mW
Rated Voltage, Analog	±15 ±0.5 (max)	*	V dc
Rated Voltage, Digital	+5 ±0.25 (max)	*	V dc
Supply Drain +15V dc	+10	*	mA
Supply Drain −15V dc	−23	*	mA
Supply Drain +5V dc	+18	*	mA
TEMPERATURE RANGE			
Specification	0 to +70	*	°C
Operating	−25 to +85	*	°C
Storage	−55 to +125	*	°C

NOTES
[1]Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V max. Logic "1" = 2.4V min.
[2]Tested on ±10V and 0 to +10V ranges.
[3]Adjustable to zero.
[4]Full Scale Range.
[5]Conversion time may be shortened with "Short Cycle" set for lower resolution.
[6]Guaranteed but not 100% production tested.
[7]CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Twos Complement.
[8]CTC coding obtained by inverting MSB (Pin 1).
[9]With Pin 23, clock rate controls tied to digital ground.
*Specifications same as AD1377JD.
Specifications subject to change without notice.

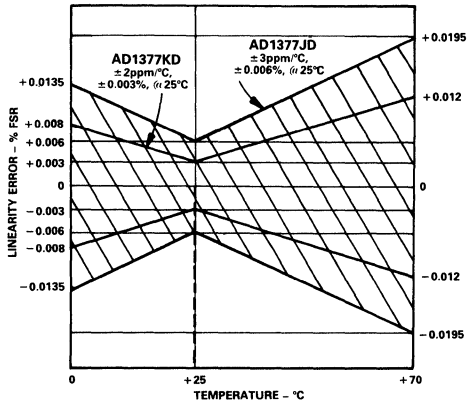


Figure 1. Linearity Error vs. Temperature

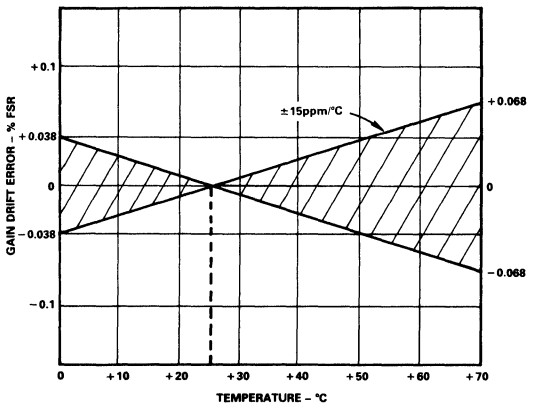


Figure 2 .AD1377 Gain Drift Error vs. Temperature

3

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD1377JD	0.006% FSR	0 to +70°C	Ceramic (DH-32E)
AD1377KD	0.003% FSR	0 to +70°C	Ceramic (DH-32E)

*See Section 14 for package outline information.

THEORY OF OPERATION

A 16-bit A/D converter partitions the range of analog inputs into 2^{16} discrete ranges or quanta. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 4 and 5. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 3).

Monotonic behavior requires that the differential linearity error be less than 1LSB; however, a monotonic converter can have missing codes. The AD1377 is specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

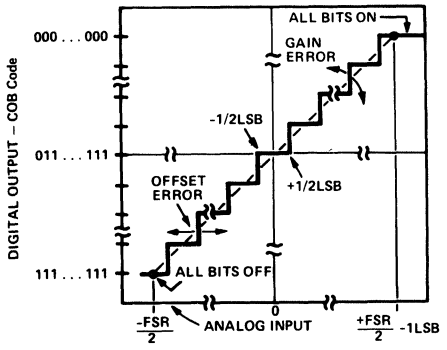


Figure 3. Transfer Characteristics for an Ideal Bipolar A/D

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD1377 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300kΩ resistor to the gain adjust Pin 29 as shown in Figure 4.

If no external trim adjustment is desired, Pin 27 (OFFSET ADJ) and Pin 29 (GAIN ADJ) may be left open.

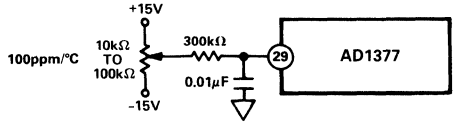


Figure 4. Gain Adjustment Circuit (±0.15% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input Pin 27 for all ranges. As shown in Figure 5, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst case offset tempco of $32LSB_{14}$ × $61ppm/LSB_{14}$ × 1200ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than $\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco ⟨100ppm/°C) are used, is shown in Figure 6.

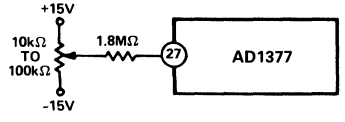


Figure 5. Offset Adjustment Circuit (±0.3% FSR)

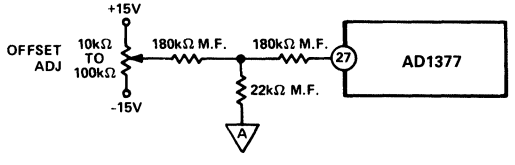


Figure 6. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to Pin 27 should be located close to this pin to keep the pin connection runs short. Comparator Input Pin 27 is quite sensitive to external noise pickup and should be guarded by analog common.

TIMING

The timing diagram is shown in Figure 7. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

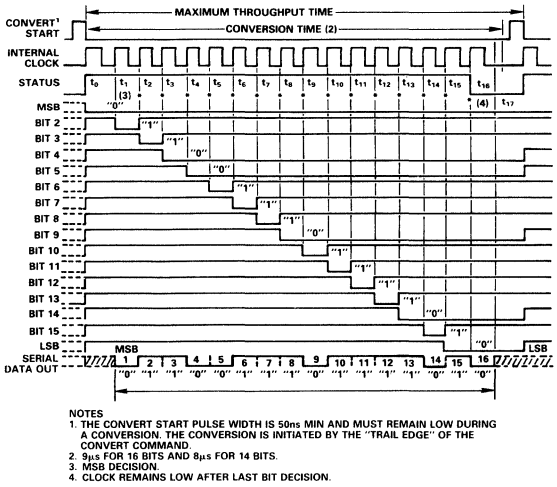


Figure 7. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 8).

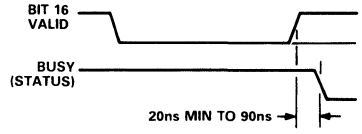


Figure 8. LSB Valid to Status Low

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 9. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

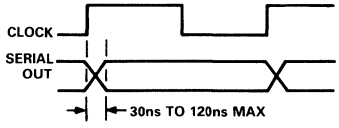


Figure 9. Clock High to Serial Out Valid

Short Cycle Input: A Short Cycle Input, Pin 32, permits the timing cycle shown in Figure 7 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (timing diagram of Figure 7). Short cycle connections and associated 8-, 10-, 12-, 13-, 14-, and 15-bit conversion times are summarized in Table I, for a 1.6MHz clock.

Resolution Bits	Resolution (% FSR)	Maximum Conversion Time (µs)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	10	t_{16}	N/C (Open)
15	0.003	9.4	t_{15}	16
14	0.006	8.7	t_{14}	15
13	0.012	8.1	t_{13}	14
12	0.024	7.5	t_{12}	13
10	0.100	6.3	t_{10}	11
8	0.390	5.0	t_8	9

Table I. Short Cycle Connections

INPUT SCALING

The AD1377 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit details.

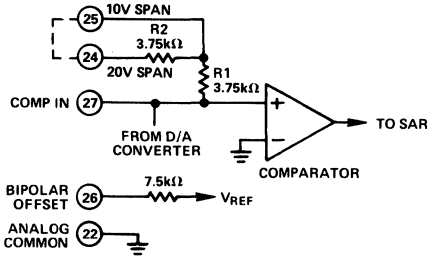


Figure 10. AD1377 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
±10V	COB	27	Input Signal	24
±5V	COB	27	Open	25
±2.5V	COB	27	Pin 27	25
0V to +5V	CSB	22	Pin 27	25
0V to +10V	CSB	22	Open	25
0V to +20V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should b e guarded by analog common.

Table II. AD1377 Input Scaling Connections

Code Under Test MSB LSB	Range	±10V	Low Side Transition Values ±5V	± 2.5V	0 to +10V	0 to +5V
000 . . . 000*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0–1/2LSB	0–1/2LSB	0–1/2LSB	+5V–1/2LSB	+2.5V–1/2LSB
111 . . . 110	− Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V + 1/2LSB	0V +1/2LSB

*Voltages given are the nominal value for transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range	±10V	±5V	±2.5V	0V to +10V	0V to +5V	
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n = 13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n = 14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n = 15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Twos Complement — achieved by using an inverter to complement the most significant bit to product ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

CALIBRATION

(14-Bit Resolution Examples)

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 4 and 5, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to + 10V Range: Set analog input to + $1LSB_{14}$ = 0.00061V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2LSB = + 9.99878V. Adjust Gain for 00000000000001 digital output code; full scale (Gain) is now calibrated. Half scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

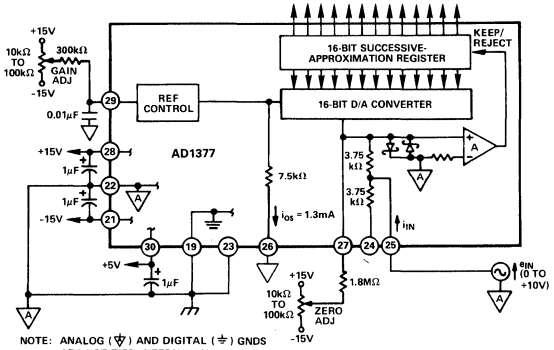


Figure 11. Analog and Power Connections for Unipolar 0 to +10V Input Range

−10V to + 10V Range: Set analog input to −9.99878V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

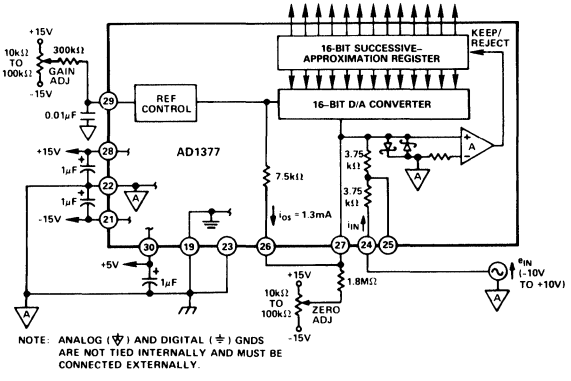


Figure 12. Analog and Power Connections for Bipolar +10V to +10V Input Range

Other Ranges: Representative digital coding for 0 to + 10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook* , edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (Pins 19 and 22) must be tied together at one point for the AD1377 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD1377. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD1377 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD1377 supply terminals should be capacitively decoupled as close to the AD1377 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

CLOCK RATE CONTROL

The AD1377 may be operated at faster conversion times by connecting the Clock Rate Control (Pin 23) to an external multiturn trim potentiometer (TCR <100ppm/°C) as shown in Figure 13.

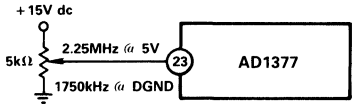


Figure 13. Clock Rate Control Circuit

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The AD389 is a companion T/H designed for use with the AD1377 family. The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients and minimal droop rate.

The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1LSB. The amplitude of 1LSB of the companion A/D converter for a given input range will vary from 610μV for a 14-bit A/D using a 0 to 10V input range to 4.88mV for a 12-bit A/D using a ±10V input range. The hold mode droop rate should produce less than 1LSB of droop in the output during the conversion time of the A/D converter. For 610μV/LSB, as noted in the example above, for an 8μs 14-bit A/D converter, the maximum droop rate will be 610μV/8μs or 76.3μV/μs during the 8μs conversion period.

The linearity error should be less than 1LSB over the transfer function, as set by the resolution of the A/D converter. The T/H acquisition time, T/H settling time along with the conversion time of the A/D converter, determines the highest sampling rate. This in turn will determine the highest input signal frequency that can be sampled at twice a cycle.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, with an ideal brickwall low pass filter placed in the signal path prior to the AD389 and A/D converter to eliminate aliasing.

The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible as with the feedthrough spec. The temperature coefficients for drift should be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more above +70°C (+158°F). For commercial and industrial users, these shifts will only appear above the highest temperatures their equipment will ever expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment. Thus, the AD1377 used with a companion AD389 T/H offers high accuracy sampling in high precision applications.

Spec	14 Bit	AD389KD	Units
Aperture Jitter (max)	2.4	0.4	ns
Slew Rate (max w/20V pk-pk signal)	1.26	1.26	V/μs
Feedthrough (1LSB max)	−84.3	−86	dB
Droop Rate (1LSB max in 8μs)	76.3	0.1	μV/μs
Acquisition Time for 20kHz Signal	8	3-5	μs
Pedestal Shift (max) with Input Signal	−84.3	−86	dB
Gain Temperature Coefficient (max) for ±10°C Ambient Operation	6.1	2.0	ppm/°C
Thermal Tail (max) within 50μs after Hold	1.2	0.1	mV
Linearity Error (max) 1LSB	±0.0061	0.003	% FSR

Table V. T/H Amplifier Requirements vs. AD389 Specs

AD389 in Combination With an	Throughput Rate	Input Freq. Range	Acq. Time & T/H Sett. Time & A/D Conv. Time
AD1377JD (13 Bit)	74.1kHz	dc to 37.1kHz	13.5μs
AD1377KD (14 Bit)	62.5kHz	dc to 31.3kHz	16.0μs

Table VI. T/H & ADC Combinations and Maximum Throughput Rate

Using the AD1377 at Slower Conversion Times

The user may wish to run the AD1377 at slower conversion times in order to synchronize the A/D with an external clock. This is accomplished by running a slower clock than the internal clock into the START CONVERT input. This clock must consist of narrow negative-going clock pulses, as seen in Figure 14. The pulse must be a minimum of 50ns wide but not greater than 400ns. Having a raising edge immediately after a falling edge inhibits the internal clock pulse. This enables the AD1377 to function normally and complete a conversion after 16 clock pulses and serial out in 17 clock pulses. The STATUS command will function normally and switch high after the first clock pulse and will fall low after the 17th clock pulse. In this way an external clock can be used to control the AD1377 at slower conversion times.

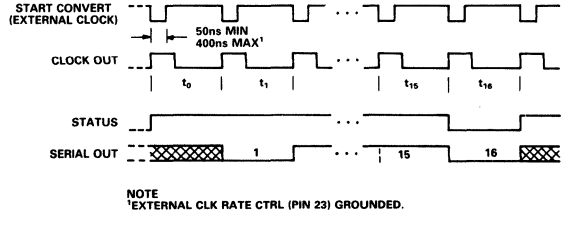


Figure 14. Timing Diagram for Use with an External Clock

ANALOG DEVICES

Low Cost 16-Bit Sampling ADC

AD1380

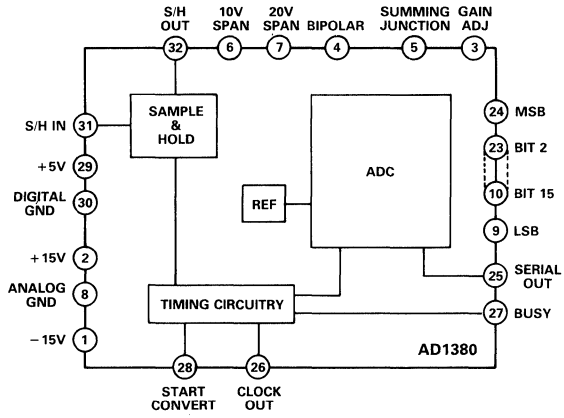
FEATURES

- Complete Sampling 16-Bit ADC With Reference and Clock
- 50kHz Throughput
- ±1/2LSB Nonlinearity
- Low Noise SHA: 300μV p-p
- 32-Pin Hermetic DIP
- Parallel and Serial Outputs
- Low Power: 900mW

APPLICATIONS

- Medical and Analytical Instrumentation
- Signal Processing
- Data Acquisition Systems
- Professional Audio
- Automatic Test Equipment (ATE)
- Telecommunications

AD1380 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1380 is a complete, low cost 16-bit analog-to-digital converter, including internal reference, clock and sample/hold amplifier. Internal thin-film-on-silicon scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V and 0 to +10V.

Important performance characteristics of the AD1380 include maximum linearity error of ±0.003% of FSR (AD1380KD) and maximum 16-bit conversion time of 14μs. Transfer characteristics of the AD1380 (gain, offset and linearity) are specified for the combined ADC/SHA, so total performance is guaranteed as a system. The AD1380 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL or 5V CMOS compatible.

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD1380JD	0.006% FSR	0 to +70°C	Ceramic (DH-32E)
AD1380KD	0.003% FSR	0 to +70°C	Ceramic (DH-32E)

*See Section 14 for package outline information.

SPECIFICATIONS (typical @ $T_A = +25°C$, $V_S = +15V$, $+5V$ combined sample and hold A/D converter unless otherwise noted)

Model	AD1380JD	AD1380KD	Units
RESOLUTION	16	*	Bits
ANALOG INPUTS			
Bipolar	±2.5, ±5, ±10	*	Volts
Unipolar	0 to +5, 0 to +10	*	Volts
DIGITAL INPUTS[1]			
Convert Command	TTL Compatible Trailing Edge of Positive 50ns (min) Pulse	*	
Logic Loading	1	*	LSTTL Load
TRANSFER CHARACTERISTICS[2] (COMBINED ADC/SHA)			
Gain Error	±0.1 max, ±0.05 typ[3]	*	% FSR[4]
Unipolar Offset Error	±0.05 max, ±0.02 typ[3]	*	% FSR
Bipolar Zero Error	±0.05 max, ±0.02 typ[3]	*	% FSR
Linearity Error	±0.006	±0.003	% FSR
Differential Linearity Error	±0.003	*	% FSR
Noise (10V Unipolar)	85	*	μV rms
(20V Bipolar)	115	*	μV rms
THROUGHPUT			
Conversion Time	14 max	*	μs
Acquisition Time (20V Step)	6 max	*	μs
SAMPLE & HOLD			
Small Signal Bandwidth	900	*	kHz
Aperture Time	50	*	ns
Aperture Jitter	100	*	ps rms
Droop Rate	50	*	μV/ms
T_{min} to T_{max}	1	*	mV/ms
Feedthrough	−80	*	dB
DRIFT (ADC & SHA)[5]			
Gain	±20 max	*	ppm/°C
Unipolar Offset	±5 max (±2 typ)	*	ppm/°C
Bipolar Zero	±5 max (±2 typ)	*	ppm/°C
No Missing Codes (Guaranteed)	0 to +70 (13 Bits)	0 to +70 (14 Bits)	°C
DIGITAL OUTPUTS	TTL Compatible	*	
All Codes Complementary	5	*	LSTTL Loads
Clock Frequency	1.1	*	MHz
POWER SUPPLY REQUIREMENTS			
Analog Supplies	±15 ±0.5	*	Volts
Digital Supply	+5 ±0.25	*	Volts
+15V Supply Current	25	*	mA
−15V Supply Current	30	*	mA
+5V Supply Current	15	*	mA
Power Dissipation	900	*	mW
TEMPERATURE RANGE			
Specified	0 to +70	*	°C
Operating	−25 to +85	*	°C

NOTES
[1]Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V max. Logic "1" = 2.4V min.
[2]Tested on ±10V and 0 to +10V ranges.
[3]Adjustable to zero.
[4]Full scale range.
[5]Guaranteed but not 100% production tested.
*Specifications same as AD1380JD.
Specifications subject to change without notice.

THEORY OF OPERATION

A 16-bit A/D converter partitions the range of analog inputs into 2^{16} discrete ranges or quanta. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 2 and 3. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 1).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD1380 is specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

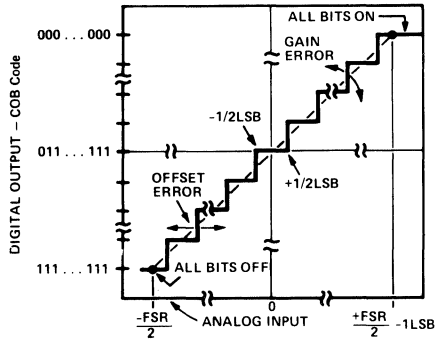


Figure 1. Transfer Characteristics for an Ideal Bipolar A/D

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD1380 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300kΩ resistor to the gain adjust Pin 3 as shown in Figure 2.

If no external trim adjustment is desired, Pin 5 (OFFSET ADJ) and Pin 3 (GAIN ADJ) may be left open.

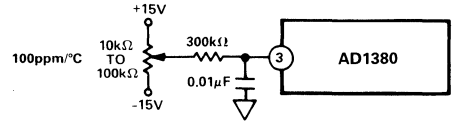


Figure 2. Gain Adjustment Circuit (±0.2% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input Pin 5 for all ranges. As shown in Figure 3, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $32LSB_{14} \times 61ppm/LSB_{14} \times 1200ppm/°C$ = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than $\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

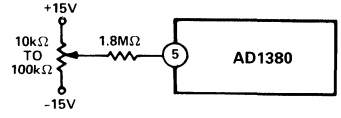


Figure 3. Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used, is shown in Figure 4.

In either adjust circuit, the fixed resistor connected to Pin 5 should be located close to this pin to keep the pin connection runs short. Comparator Input Pin 5 is quite sensitive to external noise pickup and should be guarded by analog common.

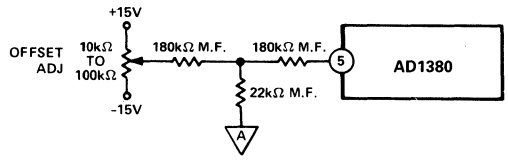


Figure 4. Low Tempco Zero Adjustment Circuit

TIMING

The timing diagram is shown in Figure 5. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

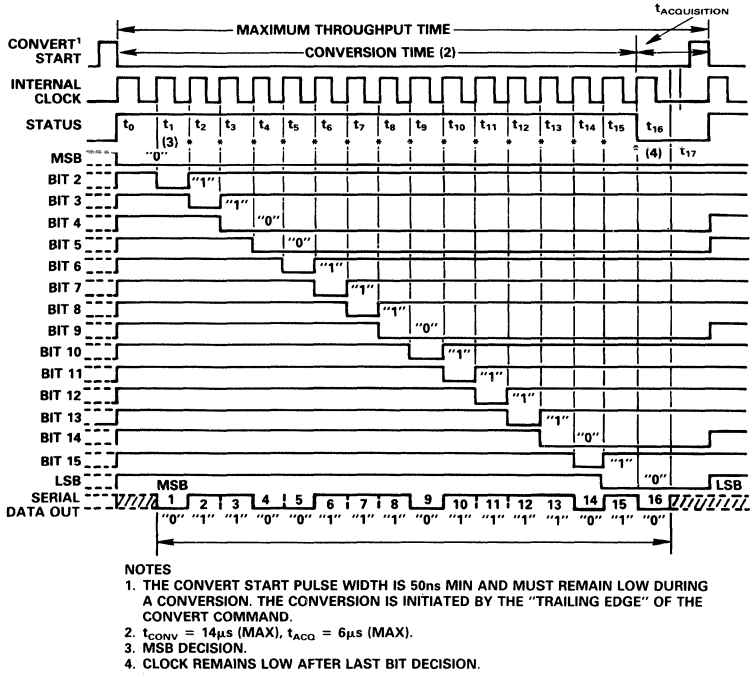


Figure 5. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 6).

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 7. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

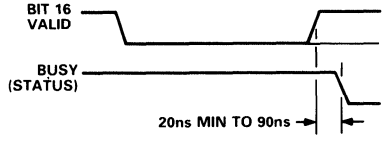


Figure 6. LSB Valid to Status Low

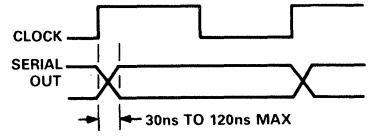


Figure 7. Clock High to Serial Out Valid

INPUT SCALING

The AD1380 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table I. See Figure 8 for circuit details.

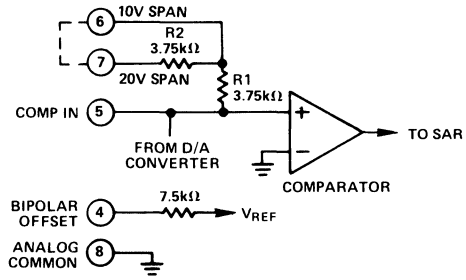


Figure 8. AD1380 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 4 to Pin	Connect Pin 7 to	Connect Input Signal to	Connect Pin 32 to
±10V	COB	5	32	31	7
±5V	COB	5	Open	31	6
±2.5V	COB	5	Pin 5	31	6
0V to +5V	CSB	NC	Pin 5	31	6
0V to +10V	CSB	NC	Open	31	6

NOTE
Pin 5 is extremely sensitive to noise and should be guarded by analog common.

Table I. AD1380 Input Scaling Connections

3

Code Under Test MSB LSB	Range	±10V	Low Side Transition Value ±5V	± 2.5V	0 to +10V	0 to +5V
000 . . . 000*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0–1/2LSB	0–1/2LSB	0–1/2LSB	+5V–1/2LSB	+2.5V–1/2LSB
111 . . . 110	−Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V +1/2LSB	0V +1/2LSB

NOTE
For LSB value for range and resolution used, see Table III.
*Voltages given are the nominal value for transition to the code specified.

Table II. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant (Bit LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n = 13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n = 14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n = 15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Twos Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

Table III. Input Voltage Range and LSB Values

CALIBRATION (14-Bit Resolution Examples)
External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 2 and 3, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to + 10V Range: Set analog input to + $1LSB_{14}$ = 0.00061V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2LSB = + 9.99878V. Adjust Gain for 00000000000001 digital output code; full scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

−10V to + 10V Range: Set analog input to −9.99878V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

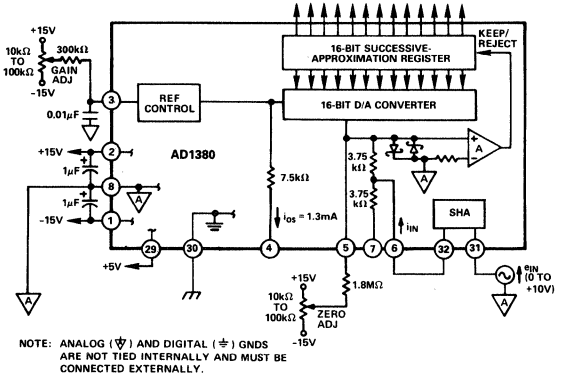


Figure 9. Analog and Power Connections for Unipolar 0 to +10V Input Range

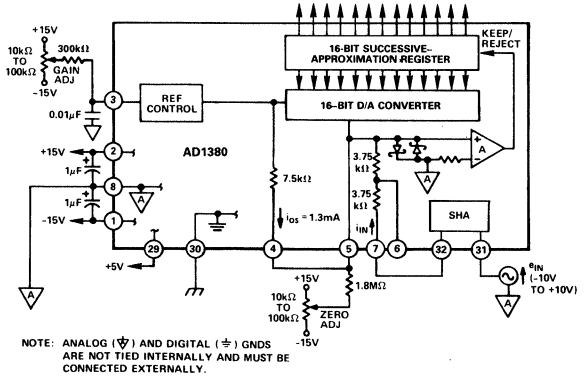


Figure 10. Analog and Power Connections for Bipolar −10V to +10V Input Range

Other Ranges: Representative digital coding for 0 to + 10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table II.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (Pins 8 and 30) must be tied together at one point for the AD1380 as close as possible to the converter. Ideally, a single, solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes on the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD1380. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD1380 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD1380 supply terminals should be capacitively decoupled as close to the AD1380 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

APPLICATION

AD1380 Dynamic Performance

High performance sampling analog-to-digital converters like the AD1380 require dynamic characterization to assure they meet or exceed their desired performance parameters for signal processing applications. Key dynamic parameters include signal-to-noise ratio (SNR) and total harmonic distortion (THD), which are characterized using Fast Fourier Transform (FFT) analysis techniques.

The results of that characterization are shown in Figure 11. In the test a 13.2kHz sine wave is applied as the analog input (f_O) at a level of 10dB below full scale; the AD1380 is operated at a word rate of 50kHz (its maximum sampling frequency).

The results of a 1024-point FFT demonstrate the exceptional performance of the converter, particularly in terms of low noise and harmonic distortion.

In Figure 11, the vertical scale is based on a full scale input referenced as 0dB. In this way, all (frequency) energy cells can be calculated with respect to full scale rms inputs.

The resulting signal-to-noise ratio is 83.2dB, which corresponds to a noise floor of −93.2dB.

Total harmonic distortion is calculated by adding the RMS energy of the first four harmonics and equals −97.5dB. Increasing the input signal amplitude to −0.4dB of full scale, causes THD to increase to −80.6dB as shown in Figure 12.

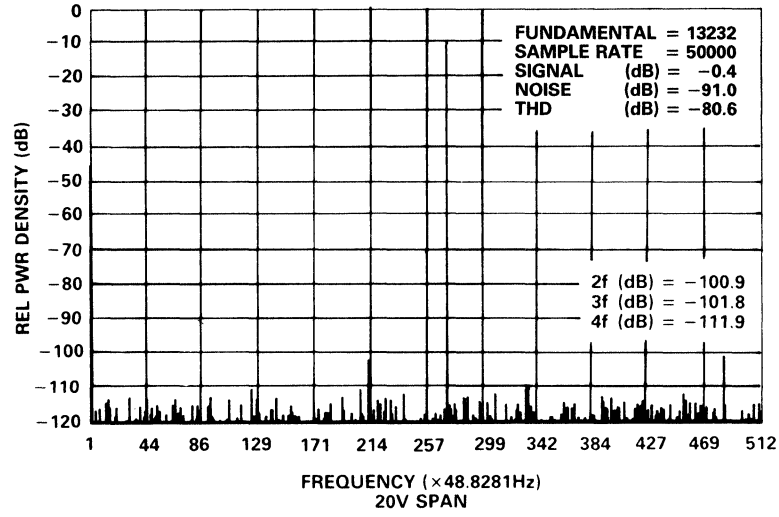


Figure 11.

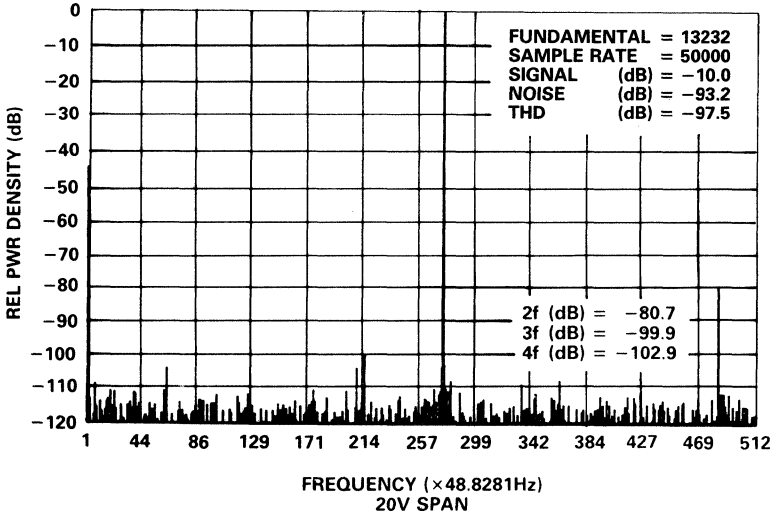


Figure 12.

At lower input frequencies, however, THD performance is improved. Figure 13 shows a full scale (−0.3dB) input signal at 1.41kHz. THD is now −96.0dB.

The ultimate noise floor can be seen with low level input signals of any frequency. In Figure 14 the noise floor is at −94dB, as demonstrated with an input signal of 24kHz at −39.8dB.

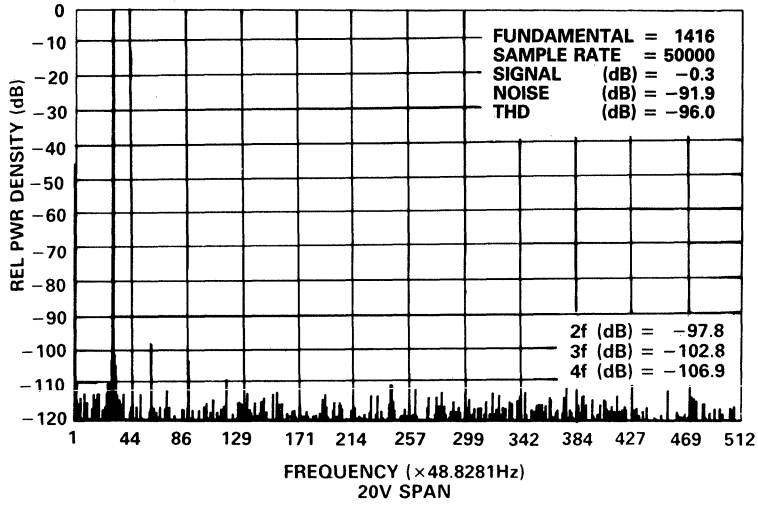


Figure 13.

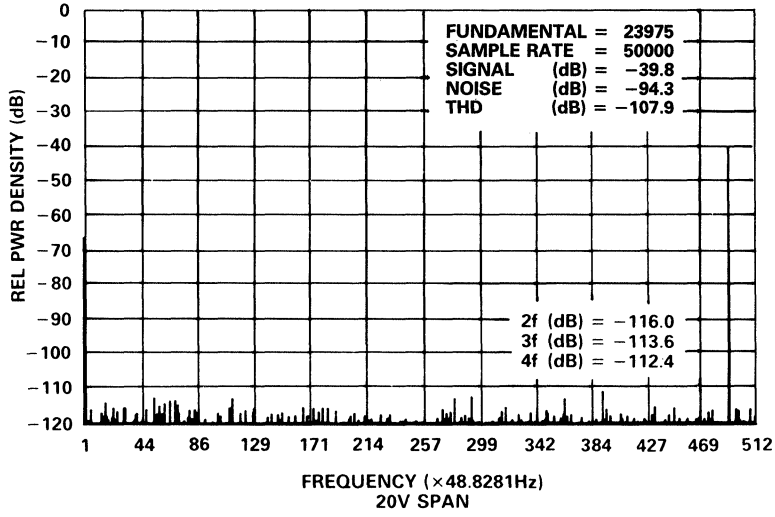


Figure 14.

ANALOG DEVICES

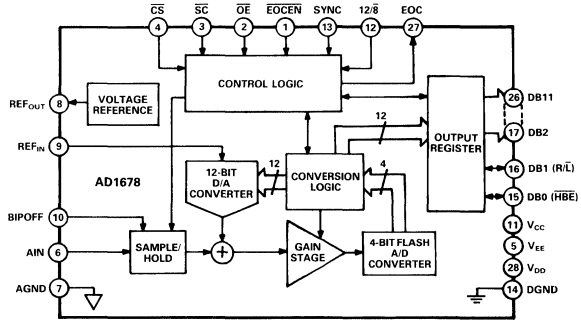
12-Bit 200 KSPS Complete Sampling ADC

AD1678

FEATURES

AC Characterized and Specified
200k Conversions per Second
1 MHz Full Power Bandwidth
500 kHz Full Linear Bandwidth
72 dB S/N+D (K Grade)
Twos Complement Data Format (Bipolar Mode)
Straight Binary Data Format (Unipolar Mode)
10 MΩ Input Impedance
8-Bit or 16-Bit Bus Interface
On-Board Reference and Clock
10 V Unipolar or Bipolar Input Range

AD1678 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1678 is a complete 12-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The AD1678 offers a choice of digital interface formats; the 12 data bits can be accessed by a 16-bit bus in a single read operation or by an 8-bit bus in two read operations (8+4), with right or left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD1678 operates from +5 V and ±12 V supplies and dissipates 745 mW. A 28-pin plastic DIP and a 0.6" wide ceramic DIP are available. Contact factory for surface-mount package options.

PRODUCT HIGHLIGHTS

1. INTEGRATION: The AD1678 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. PERFORMANCE: The AD1678 provides a throughput of 200k conversions per second. S/N+D is 72 dB (K grade) at 10 kHz and remains flat beyond the Nyquist frequency.
3. SPECIFICATIONS: The AD1678 is specified for ac (or "dynamic") specifications such as S/N+D ratio, THD and IMD. These parameters are important in signal processing applications as they represent the effect on the spectral content of the input signal.
4. EASE OF USE: The pinout is designed for easy board layout, and the choice of single or two read cycle output provides compatibility with 16- or 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
5. RELIABILITY: The AD1678 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V, V_{EE} = −12 V, V_{DD} = +5 V, f_{SAMPLE} = 200 KSPS, f_{IN} = 10.06 kHz[1], unless otherwise noted)

Parameter	AD1678J Min	AD1678J Typ	AD1678J Max	AD1678K Min	AD1678K Typ	AD1678K Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
@ +25°C	**70**	71		**72**	73		dB
T_{min} to T_{max}	**70**	71		**71**	73		dB
TOTAL HARMONIC DISTORTION (THD)[3]							
@ +25°C		−88	**−80**		−88	**−80**	dB
		0.004	**0.010**		0.004	**0.010**	%
T_{min} to T_{max}		−85	**−78**		−85	**−78**	dB
		0.005	**0.012**		0.005	**0.012**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−87	**−80**		−87	**−80**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		−85	**−80**		−85	**−80**	dB
3rd Order Products		−90	**−80**		−90	**−80**	dB

NOTE
[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a 0 dB (9.997 V p-p) input signal.
[2]See Figures 7 and 8 for higher frequencies and other input amplitudes.
[3]See Figure 6 for other conditions.
[4]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 200 KSPS. See Figure 10 and Definition of Specifications section.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V, V_{EE} = −12 V, V_{DD} = +5 V ±10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.4**		V
V_{IL}	Low Level Input Voltage			**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = 5 V		**10**	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V		**10**	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V		**10**	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES
Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

DC SPECIFICATIONS (@ +25°C, V_{CC} = +12 V, V_{EE} = −12 V, V_{DD} = +5 V unless otherwise indicated)

Parameter	AD1678J Min	AD1678J Typ	AD1678J Max	AD1678K Min	AD1678K Typ	AD1678K Max	Units
ACCURACY							
Resolution	**12**			**12**			Bits
Differential Linearity							
T_{min} to T_{max} (No Missing Codes)	**12**			**12**			Bits
Integral Linearity Error		±1			±1		LSB
Unipolar Zero Error[1]		±4			±4		LSB
Bipolar Zero Error[1]		±4			±4		LSB
Unipolar Gain Error[1,2]		±3			±3		LSB
Bipolar Gain Error[1,2]		±3			±3		LSB
Temperature Drift (Coefficients)[3]							
Unipolar Zero		±2 (10)			±2 (10)		LSB (ppm/°C)
Bipolar Zero		±2 (10)			±2 (10)		LSB (ppm/°C)
Unipolar Gain		±4 (20)			±4 (20)		LSB (ppm/°C)
Bipolar Gain		±4 (20)			±4 (20)		LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance (f_{IN} = 100 kHz)		10			10		pF
Input Settling Time			1			1	μs
Aperture Delay	5		20	5		20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[4]	**4.95**		**5.05**	**4.95**		**5.05**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
POWER SUPPLIES (T_{min} to T_{max})							
Operating Voltages							
V_{CC}	+11.4	+12	+12.6	+11.4	+12	+12.6	V
V_{EE}	−12.6	−12	−11.4	−12.6	−12	−11.4	V
V_{DD}	+4.5	+5	+5.5	+4.5	+5	+5.5	V
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**34**		25	**34**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	745		560	745	mW

NOTES
[1]Adjustable to zero; see Figures 12 and 13.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]With maximum external load applied.

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.

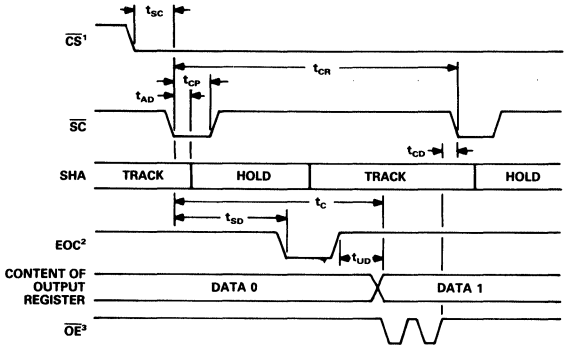
Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V, V_{EE} = −12 V, V_{DD} = +5 V)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{SC}$ Delay	t_{SC}	50			ns
Conversion Rate	t_{CR}			5	µs
Convert Pulse Width	t_{CP}	150			ns
Aperture Delay	t_{AD}	5		20	ns
Conversion Time[1]	t_C		3.9	**4.47**	µs
Status Delay	t_{SD}	0		400	ns
Access Time[2]	t_{BA}			**100**	ns
Float Delay[3]	t_{FD}	10		**80**	ns
Update Delay	t_{UD}			200	ns
Format Setup	t_{FS}	60			ns
$\overline{OE}$ Delay	t_{OE}	20			ns
Read Pulse Width	t_{RP}	100			ns[4]
		150			ns[5]
Conversion Delay	t_{CD}	150			ns
$\overline{EOCEN}$ Delay	t_{EO}	20			ns

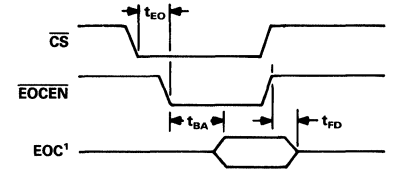
NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}$/$\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 3; C_{OUT} = 100 pF.
[3]Measured from the rising edge of $\overline{OE}$/$\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 3; C_{OUT} = 10 pF.
[4]12-bit read mode.
[5]8-bit read mode.

Specifications subject to change without notice.



NOTES
[1]IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2]$\overline{EOCEN}$ = LOW; SEE FIGURE 2. IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
[3]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing



NOTE
[1]SEE END-OF-CONVERT (EOC) PARAGRAPH FOR DETAILS.

Figure 2. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

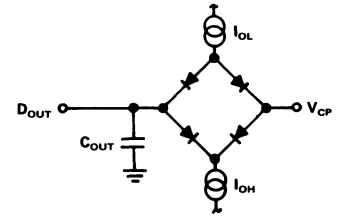


Figure 3. Load Circuit for Bus Timing Specifications

CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both Chip Select ($\overline{CS}$) and Start Convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW t_{SC} before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ low, regardless of the state of $\overline{CS}$.

Before a conversion is started, End-Of-Convert (EOC) is HIGH, and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample. EOC goes HIGH when the conversion is finished.

In track mode, the sample-hold will settle to ±0.01% (12 bits) in 1 μs maximum. The acquisition time does not affect the throughput rate as the AD1678 goes back into track mode more than 1 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

END-OF-CONVERT

In asynchronous mode, End-Of-Convert (EOC) is an open drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by End-Of-Convert ENable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output which is enabled by $\overline{EOCEN}$ and $\overline{CS}$. See the Conversion Status Truth Table for details. Access (t_{BA}) and float (t_{FD}) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the 10 pF output capacitance and the pull-up resistor.

3

12-BIT MODE CODING FORMAT (1 LSB = 2.44 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}	Output Code	V_{IN}	Output Code
0	000 . . . 0	−5.000 V	100 . . . 0
5.000 V	100 . . . 0	−0.002 V	111 . . . 1
9.9964 V	111 . . . 1	0	000 . . . 0
		+2.500 V	010 . . . 0
		+4.9964 V	011 . . . 1

OUTPUT ENABLE TRUTH TABLES

12-BIT MODE (12/$\overline{8}$ = HIGH)

INPUTS	OUTPUT
($\overline{CS}$ U $\overline{OE}$)	DB11–DB0
1	High Z
↓	Enable 12-Bit Output

8-BIT MODE (12/$\overline{8}$ = LOW)

	INPUTS			OUTPUTS							
	R/$\overline{L}$	$\overline{HBE}$	($\overline{CS}$ U $\overline{OE}$)	DB11 . . . DB4							
	X	X	1	← High Z →							
	1	0	↓	0	0	0	0	a	b	c	d
Unipolar	1	1	↓	e	f	g	h	i	j	k	l
Mode	0	0	↓	a	b	c	d	e	f	g	h
	0	1	↓	i	j	k	l	0	0	0	0
	1	0	↓	a	a	a	a	a	b	c	d
Bipolar	1	1	↓	e	f	g	h	i	j	k	l
Mode	0	0	↓	a	b	c	d	e	f	g	h
	0	1	↓	i	j	k	l	0	0	0	0

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
U = Logical OR.
a = MSB.
l = LSB.
↓ = HIGH to LOW transition. Must stay low for t = t_{RP}.

START CONVERSION TRUTH TABLE

	INPUTS			
	SYNC	$\overline{CS}$	$\overline{SC}$	STATUS
Synchronous Mode	1	1	X	No Conversion
	1	0	↓	Start Conversion
	1	↓	0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion
Asynchronous Mode	0	X	1	No Conversion
	0	X	↓	Start Conversion
	0	X	0	Continuous Conversion

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay low for t = t_{CP}.

CONVERSION STATUS TRUTH TABLE

	INPUTS			OUTPUT	
	SYNC	$\overline{CS}$	$\overline{EOCEN}$	EOC	STATUS
Synchronous Mode	1	0	0	0	Converting
	1	0	0	1	Not Converting
	1	1	X	High Z	Either
	1	X	1	High Z	Either
Asynchronous Mode*	0	X	0	0	Converting
	0	X	0	High Z	Not Converting
	0	X	1	High Z	Either

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
*EOC requires a pull-up resistor in asynchronous mode.

OUTPUT ENABLE OPERATION

The data bits (DB11–DB0) are three-state outputs enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. Bits DB1 (R/$\overline{L}$) and DB0 ($\overline{HBE}$) are bidirectional. In 12-bit mode they are data output bits. In 8-bit mode they are inputs which define the format of the output register.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REF_{OUT}), output coding is twos complement binary.

When EOC goes HIGH, the output register contains the results of the previous conversion. A period of time t_{UD} is required for the present conversion results to be loaded into the output register. Bringing $\overline{OE}$ LOW t_{OE} after $\overline{CS}$ goes LOW makes the output register contents available on the data bits. A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued. This allows internal logic states to reset and guarantees minimum aperture jitter for the next conversion.

Output Enable ($\overline{OE}$) must be toggled to update the output register in both 8- and 12-bit read modes.

Figure 4 illustrates the 8-bit read mode (12/$\overline{8}$ = LOW), where only DB11–DB4 are used as output lines onto an 8-bit bus. The output is read in two steps, with the high byte read first, followed by the low byte. High Byte Enable ($\overline{HBE}$) controls the output sequence. The 12-bit result can be right or left justified depending on the state of R/$\overline{L}$.

In 12-bit read mode (12/$\overline{8}$ = HIGH), a single READ operation accesses all 12 output bits on DB11–DB0 for interface to a 16-bit bus. Figure 5 provides the output timing relationships. Note that t_{CR} must be observed, in that $\overline{SC}$ pulses should not be issued at intervals closer than 5 μs. If $\overline{SC}$ is asserted sooner than 5 μs, conversion accuracy may deteriorate. For this reason $\overline{SC}$ should not be held LOW in an attempt to operate in a continuous convert mode.

POWER-UP

One conversion sequence, consisting of one $\overline{SC}$ instruction, is required after power-up to reset internal logic.

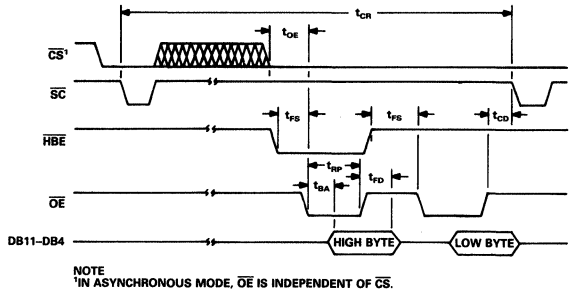


Figure 4. Output Timing, 8-Bit Read Mode

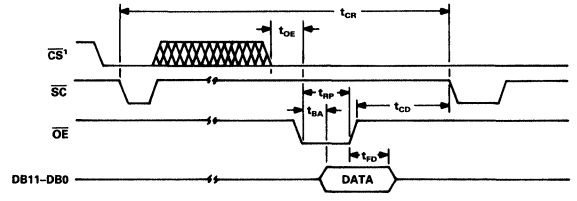


Figure 5. Output Timing, 12-Bit Read Mode

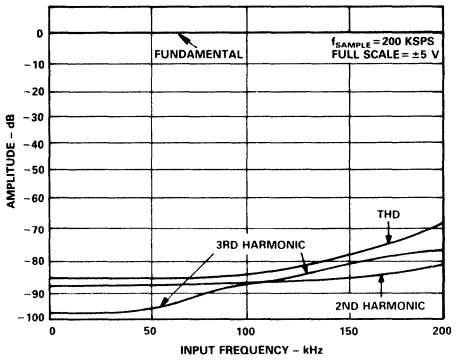


Figure 6. Harmonic Distortion vs. Input Frequency

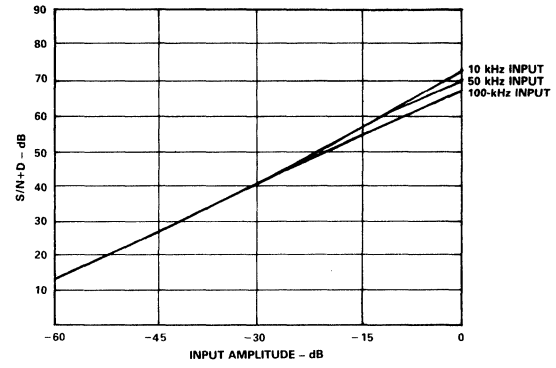


Figure 7. S/N+D vs. Input Amplitude (f_{SAMPLE} = 200 KSPS)

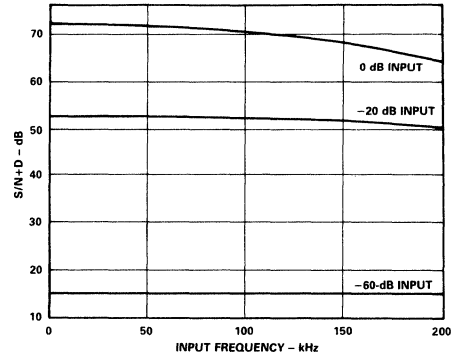


Figure 8. S/N+D vs. Input Frequency and Amplitude

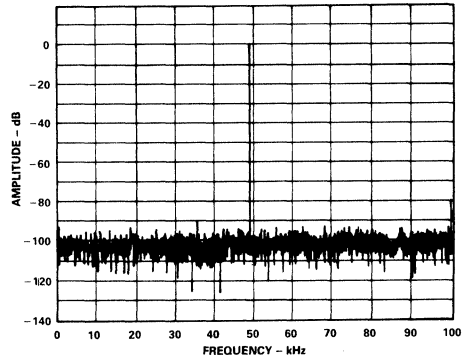


Figure 9. Nonaveraged 2048 Point FFT at 200 KSPS, F_{IN} = 49.902 kHz

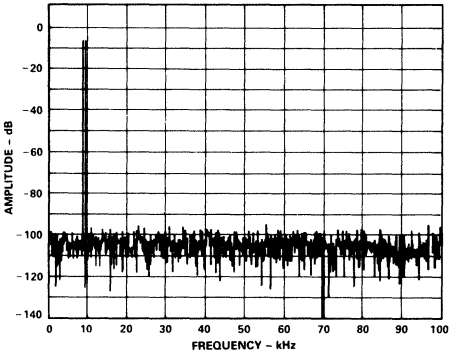


Figure 10. IMD Plot for F_{IN} = 9.08 kHz (fa), 9.58 kHz (fb)

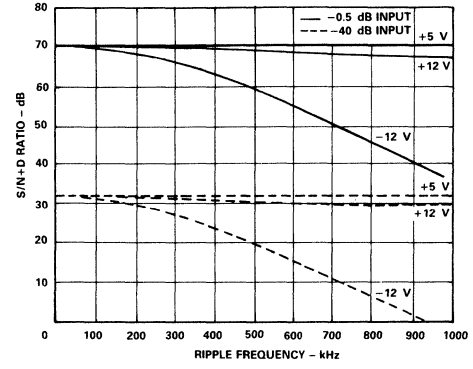


Figure 11. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 200 KSPS, V_{RIPPLE} = 0.1 V p-p)

Definition of Specifications

FREQUENCY DOMAIN TESTING
The AD1678 is tested dynamically using a sine wave input and a 2048 point Fast Fourier Transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral multiple of input cycles is captured, allowing direct FFT processing without windowing or digital filtering which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to be "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called Prime Coherent Sampling, is a highly accurate and repeatable measure of the actual frequency domain response of the converter.

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter, is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of the measured input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD1678 has been designed to optimize input bandwidth, allowing the AD1678 to undersample input signals with frequencies significantly above the converter's Nyquist frequency. If the input signal is suitably band-limited, the spectral content of the input signal can be recovered.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

For the AD1678, this specification is 12 bits from T_{min} to T_{max}, which guarantees that all 4096 codes are present over temperature.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (1111 1111 1111 to 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for a 0–10 V range, 4.9963 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

AD1678 PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground.
AIN	6	AI	Analog Signal Input.
BIPOFF	10	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} through 50 Ω resistor for ±5 V input bipolar mode and twos complement binary output coding. See Figures 12 and 13.
$\overline{CS}$	4	DI	Chip Select. Active LOW.
DGND	14	P	Digital Ground
DB11–DB4	26–19	DO	Data Bits 11 through 4. In 12-bit format (see 12/$\overline{8}$ pin), these pins provide the upper 8 bits of data. In 8-bit format, these pins provide all 12 bits in two bytes (see R/$\overline{L}$ pin). Active HIGH.
DB3, DB2	18, 17	DO	Data Bits 3 and 2. In 12-bit format, these pins provide Data Bit 3 and Data Bit 2. Active HIGH. In 8-bit format they are undefined and should be tied to V_{DD}.
DB1 (R/$\overline{L}$)	16	DO	In 12-bit format, Data Bit 1. Active HIGH.
DB0($\overline{HBE}$)	15	DO	In 12-bit format, Data Bit 0. Active HIGH.
EOC	27	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. In asynchronous mode, EOC is an open drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	DI	End-Of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$ (DB0)	15	DI	In 8-bit format, High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte.
$\overline{OE}$	2	DI	Output Enable. The falling edge of $\overline{OE}$ enables DB11–DB0 in 12-bit format and DB11–DB4 in 8-bit format. Gated with $\overline{CS}$. Active LOW.
REF_{IN}	9	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	AO	+5 V Reference Output. Tied to REF_{IN} through 50 Ω resistor for normal operation.
R/$\overline{L}$ (DB1)	16	DI	In 8-bit format, Right/Left justified. Sets alignment of 12-bit result within 16-bit field. Tied to V_{DD} for right-justified output and tied to DGND for left-justified output.
$\overline{SC}$	3	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	DI	SYNC Control. If tied to V_{DD} (synchronous mode), $\overline{SC}$, EOC and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open drain output. EOC requires an external 3k Ω pull-up resistor in asynchronous mode.
V_{CC}	11	P	+12 V Analog Power.
V_{EE}	5	P	−12 V Analog Power.
V_{DD}	28	P	+5 V Digital Power.
12/$\overline{8}$	12	DI	Twelve/eight bit format. If tied HIGH, sets output format to 12-bit parallel. If tied LOW, sets output format to 8-bit multiplexed.

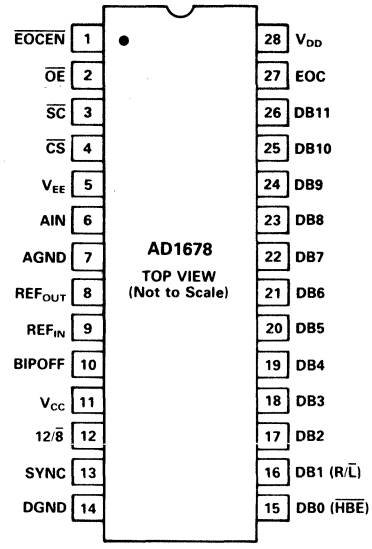
Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers.
P = Power.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	−12	+12	V
REF_{IN}	V_{EE}	0	V_{CC}	V
REF_{IN}	V_{CC}	V_{EE}	0	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature		0	+70	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Package	Mimimum S/N+D @ 10 kHz, −0.5 dB Input	Temperature Range	Package Options*
AD1678JN	28-Pin Plastic DIP	70 dB	0 to +70°C	N-28A
AD1678KN	28-Pin Plastic DIP	72 dB	0 to +70°C	N-28A
AD1678JD	28-Pin Ceramic DIP	70 dB	0 to +70°C	D-28A
AD1678KD	28-Pin Ceramic DIP	72 dB	0 to +70°C	D-28A

*See Section 14 for package outline information.

ESD SENSITIVITY

The AD1678 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD1678 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD1678 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 1000 Ω. The 10 V p-p full-scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC. The AD1678 is factory trimmed to minimize offset, gain and linearity errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical, even these components can be eliminated.

In some applications, offset and gain errors need to be more precisely trimmed. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 12. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim range (±20 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the AD1678 accuracy limits are sufficient for application. If the pins are shorted together, the additional offset and gain errors will be approximately 20 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−1.22 mV for a ±5 V range) and adjust R1 until the major carry transition is located (1111 1111 1111 to 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9963 V for a ±5 V range) and adjust R2 to give the last positive transition (0111 1111 1110 to 0111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9988 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (1000 0000 0000 to 1000 0000 0001). Then perform the gain error trim as outlined above.

UNIPOLAR RANGE INPUTS

The connections for the unipolar mode are shown in Figure 13. In this mode, data output coding will be straight binary. This circuit will allow approximately ±25 mV of offset trim range (±10 LSB) and ±0.5% of gain trim range (±20 LSB).

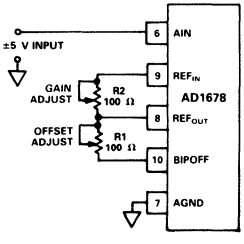


Figure 12. Bipolar Input Connections with Gain and Offset Trims

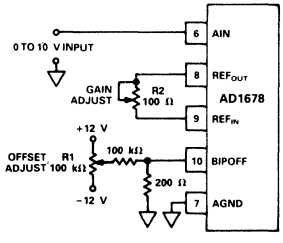


Figure 13. Unipolar Input Connections with Gain and Offset Trims

If the standard accuracy limits of the AD1678 are sufficient for the application, the gain adjust resistor (R2) can be replaced by a 50 Ω ±1% fixed resistor and BIPOFF can be connected to ground.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 5 mA current through a 0.5 Ω trace will develop a voltage drop of 2.5 mV, which is 1 LSB at the 12-bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD1678 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB11–DB0 and EOC.

SUPPLY DECOUPLING

The AD1678 power supplies should be well filtered, well regulated and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF disk ceramic capacitor provides adequate decoupling over a wide range of frequencies.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD1678, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD1678 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD1678 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD1678. If multiple AD1678s are used or the AD1678 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at

each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

INTERFACING THE AD1678 TO MICROPROCESSORS

The I/O capabilities of the AD1678 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD1678 interface configurations.

AD1678 TO TMS320C25

In Figure 14 the AD1678 is mapped into the TMS320C25 I/O space. AD1678 conversions are initiated by issuing an OUT instruction to Port 8. EOC status and the conversion result are read in with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 8 and $\overline{MSC}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD1678 read instruction.

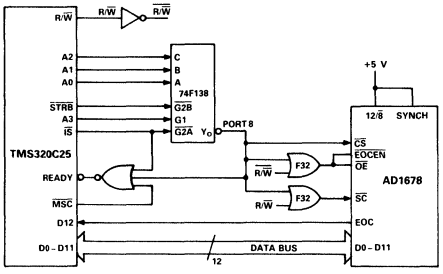


Figure 14. AD1678 to TMS320C25 Interface

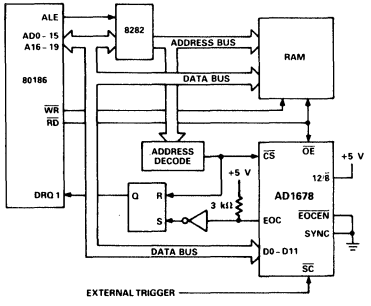


Figure 15. AD1678 to 80186 DMA Interface

AD1678 TO 80186

Figure 15 shows the AD1678 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD1678 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD1678 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD1678 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ operation resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

AD1678 TO Z80

The AD1678 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 16 illustrates an I/O configuration, where the AD1678 occupies several port addresses to allow separate polling of the EOC status and reading of the data. The lower address bit, A0, is used to select the high and low order bytes of the result. The AD1678 R/$\overline{L}$ line is tied HIGH, resulting in right justified output data.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD1678 to be used with Z80 processors having clock speeds up to 8 MHz.

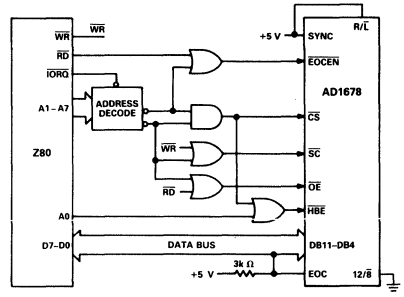


Figure 16. AD1678 to Z80 Interface

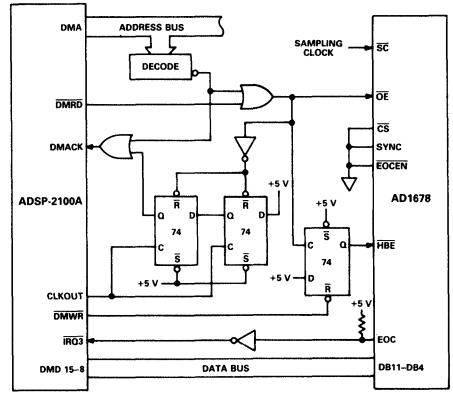


Figure 17. AD1678 to ADSP-2100A Interface

AD1678 TO ANALOG DEVICES' ADSP-2100A

Figure 17 demonstrates the AD1678 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD1678 data memory interface with two hardware wait states.

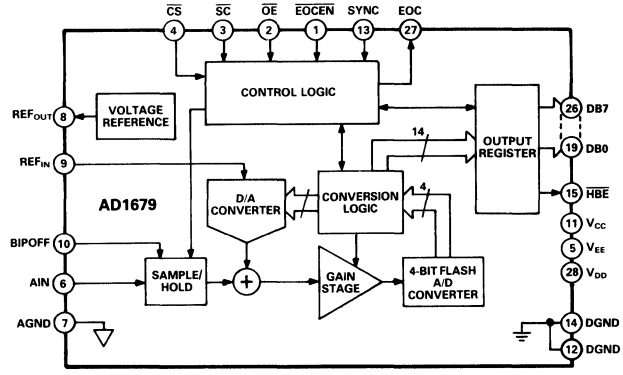
The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD1678 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts $\overline{HBE}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latches, is used to force the ADSP-2100A into a two cycle wait state by generating DMACK. The read operation is thus started and completed within three processor cycles (240 ns). HBE is released during "high byte read." This allows the processor to read the lower byte of data as soon as "high byte read" is complete. The low byte read operation executes in a similar manner to the first and is completed during the next 240 ns.

14-Bit 100 KSPS Complete Sampling ADC

AD1679

FEATURES
AC Characterized and Specified
100k Conversions per Second
1 MHz Full Power Bandwidth
500 kHz Full Linear Bandwidth
80 dB S/N+D (K Grade)
Twos Complement Data Format (Bipolar Mode)
Straight Binary Data Format (Unipolar Mode)
10 MΩ Input Impedance
8-Bit Bus Interface (See AD1779 for 16-Bit Interface)
On-Board Reference and Clock
10 V Unipolar or Bipolar Input Range

AD1679 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1679 is a complete, 14-bit monolithic analog-to-digital converter, consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The 14 data bits are accessed by an 8-bit bus in two read operations (8+6), with left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm, which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD1679 operates from +5 V and ±12 V supplies and dissipates 720 mW. A 28-pin plastic DIP and a 0.6″ wide ceramic DIP are available. Contact factory for surface-mount package options.

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD1679 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. PERFORMANCE: The AD1679 provides a throughput of 100k conversions per second. S/N+D is 80 dB (K grade) at 10 kHz and remains flat beyond the Nyquist frequency.
3. SPECIFICATIONS: The AD1679 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD. These parameters are important in signal processing applications as they indicate the AD1679's effect on the spectral content of the input signal.
4. EASE OF USE: The pinout is designed for easy board layout, and the two read output provides compatibility with 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
5. RELIABILITY: The AD1679 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = + 5 V ±10%, f_{SAMPLE} = 100 KSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD1679J Min	AD1679J Typ	AD1679J Max	AD1679K Min	AD1679K Typ	AD1679K Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
−0.5 dB Input (Referred to −0 dB Input)	**78**	79		**80**	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)[3]							
@ +25°C		−90	**−84**		−90	**−84**	dB
		0.003	**0.006**		0.003	**0.006**	%
T_{min} to T_{max}		−88	**−82**		−88	**−82**	dB
		0.004	**0.008**		0.004	**0.008**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	**−84**		−90	**−84**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		−90	−84		−90	−84	dB
3rd Order Products		−90	−84		−90	−84	dB

NOTES
[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise noted.
[2]See Figure 7 for higher frequencies and other input amplitudes.
[3]See Figures 5 and 6 for other conditions.
[4]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 100 KSPS. See Figure 9 and Definition of Specifications section.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD}= +5 V ±10%.)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.4**		V
V_{IL}	Low Level Input Voltage			**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = 5 V		**10**	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V		**10**	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5mA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V		**10**	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

DC SPECIFICATIONS (@ +25°C, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10% unless otherwise indicated)

Parameter	AD1679J Min	AD1679J Typ	AD1679J Max	AD1679K Min	AD1679K Typ	AD1679K Max	Units
ACCURACY							
Resolution	**14**			**14**			Bits
Integral Linearity Error		±1			±1		LSB
Differential Linearity							
T_{min} to T_{max} (No Missing Codes)	**14**			**14**			Bits
Unipolar Zero Error[1]		±10			±10		LSB
Bipolar Zero Error[1]		±10			±10		LSB
Unipolar Gain Error[1, 2]		±12			±12		LSB
Bipolar Gain Error[1, 2]		±12			±12		LSB
Temperature Drift (Coefficients)[3]							
Unipolar Zero		±8 (10)			±8 (10)		LSB (ppm/°C)
Bipolar Zero		±8 (10)			±8 (10)		LSB (ppm/°C)
Unipolar Gain		±16 (20)			±16 (20)		LSB (ppm/°C)
Bipolar Gain		±16 (20)			±16 (20)		LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	μs
Aperture Delay	5		20	5		20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[4]	**4.95**		**5.05**	**4.95**		**5.05**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
Power Supply Rejection		1			1		mV/V
POWER SUPPLIES (T_{min} to T_{max})							
Operating Voltages							
V_{CC}	+11.4	+12	+12.6	+11.4	+12	+12.6	V
V_{EE}	−12.6	−12	−11.4	−12.6	−12	−11.4	V
V_{DD}	+4.5	+5	+5.5	+4.5	+5	+5.5	V
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**32**		25	**32**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	**720**		560	**720**	mW

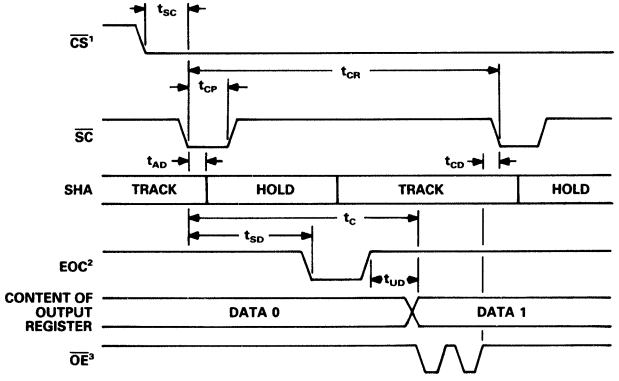
NOTES
[1]Adjustable to zero; see Figures 11 and 12.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]With maximum external load applied.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter	Symbol	Min	Max	Units
$\overline{SC}$ Delay	t_{SC}	50		ns
Conversion Rate[1]	t_{CR}		10	µs
Convert Pulse Width	t_{CP}	150		ns
Aperture Delay	t_{AD}	5	20	ns
Conversion Time	t_C		**8.5**	µs
Status Delay	t_{SD}	0	400	ns
Access Time[2]	t_{BA}		**100**	ns
Float Delay[3]	t_{FD}	10	**80**	ns
Update Delay	t_{UD}		200	ns
Format Setup	t_{FS}	60		ns
$\overline{OE}$ Delay	t_{OE}	20		ns
Read Pulse Width	t_{RP}	150		ns
Conversion Delay	t_{CD}	400		ns
$\overline{EOCEN}$ Delay	t_{EO}	20		ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}$/$\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4; C_{OUT}=100 pF.
[3]Measured from the rising edge of $\overline{OE}$/$\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 4; C_{OUT}=10 pF.
Specifications subject to change without notice.



NOTES
[1]IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2]$\overline{EOCEN}$ = LOW. IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT. SEE CONVERSION TRUTH TABLE.
[3]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

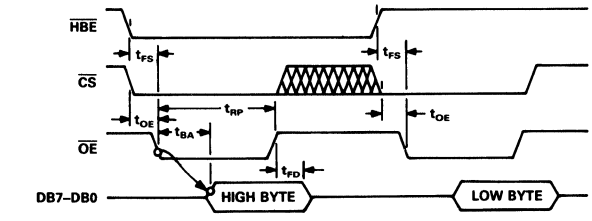
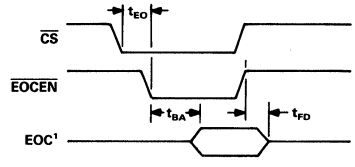


Figure 2. Output Timing



NOTE
[1]EOC IS A THREE-STATE OUTPUT IN SYNCHRONOUS MODE AND AN OPEN DRAIN OUTPUT IN ASYNCHRONOUS. ACCESS (t_{BA}) AND FLOAT (t_{FD}) TIMING SPECIFICATIONS DO NOT APPLY IN ASYNCHRONOUS MODE WHERE THEY ARE A FUNCTION THE TIME CONSTANT FORMED BY THE 10 pF PULL-UP CAPACITOR, OUTPUT CAPACITANCE AND THE PULL-UP RESISTOR.

Figure 3. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

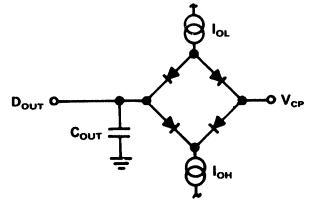


Figure 4. Load Circuit for Bus Timing Specifications

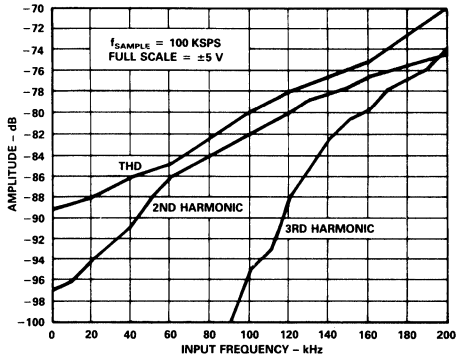


Figure 5. Harmonic Distortion vs. Input Frequency (−0.5 dB Input)

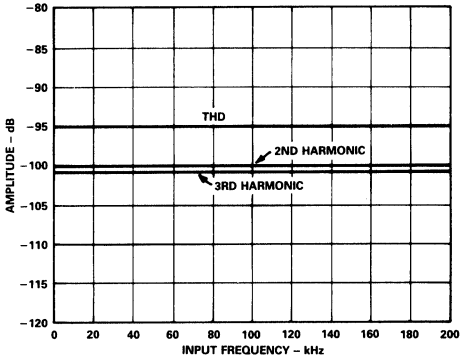


Figure 6. Harmonic Distortion vs. Input Frequency (−20 dB Input)

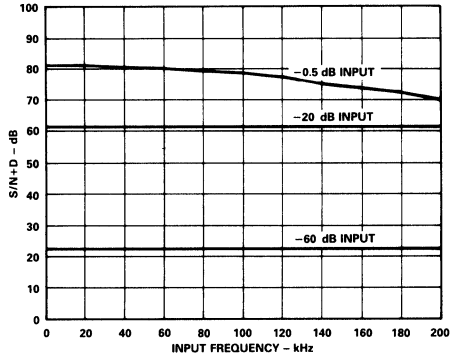


Figure 7. S/N+D vs. Input Frequency and Amplitude

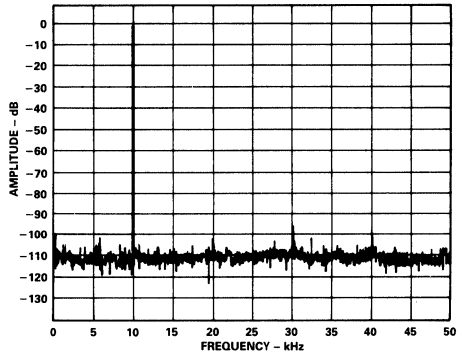


Figure 8. 5-Plot Averaged 2048 Point FFT at 100 KSPS, f_{IN} = 10.009 kHz

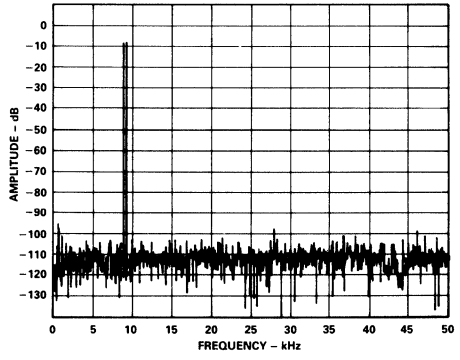


Figure 9. Nonaveraged IMD Plot for f_{IN} = 9.08 kHz (f_a), 9.58 kHz (f_b) at 100 KSPS

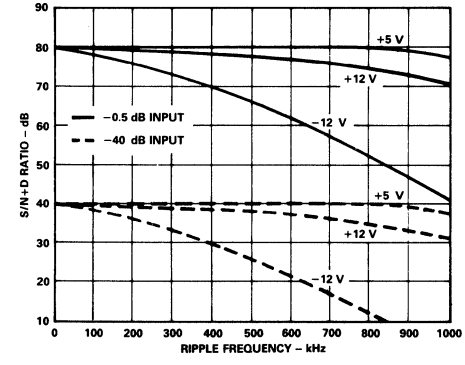


Figure 10. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 100 KSPS, V_{RIPPLE} = 0.1 V p-p)

CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both Chip Select ($\overline{CS}$) and Start Convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW t_{SC} before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ LOW, regardless of the state of $\overline{CS}$.

Before a conversion is started, End Of Convert (EOC) is HIGH and the sample-hold is in track mode. After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample.

In track mode, the sample-hold will settle to ±0.003% (14 bits) in 1.5 μs maximum. The acquisition time does not affect the throughput rate as the AD1679 goes back into track mode more than 2 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW.

When the conversion is finished, EOC goes HIGH and the result is loaded into the output register after a period of time t_{UD}. Bringing $\overline{OE}$ LOW t_{OE} after $\overline{CS}$ goes LOW makes the output register contents available on the output data bits (DB7–DB0). A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued. This allows internal logic states to reset and guarantees minimum aperture jitter for the next conversion.

If $\overline{SC}$ is held LOW, conversions will occur continuously. EOC will go HIGH for approximately 1.5 μs between conversions.

START CONVERSION TRUTH TABLE

	INPUTS			
	SYNC	$\overline{CS}$	$\overline{SC}$	STATUS
Synchronous Mode	1	1	X	No Conversion
	1	0	↓	Start Conversion
	1	↓	0	Start Conversion (Not Recommended)
	1	0	0	Continuous Conversion
Asynchronous Mode	0	X	1	No Conversion
	0	X	↓	Start Conversion
	0	X	0	Continuous Conversion

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay low for t = t_{CP}.

14-BIT MODE CODING FORMAT (1 LSB = 0.61 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}	Output Code	V_{IN}	Output Code
0	000 . . . 0	−5.00000 V	100 . . . 0
5.00000 V	100 . . . 0	−0.00061 V	111 . . . 1
9.99939 V	111 . . . 1	0	000 . . . 0
		+2.50000 V	010 . . . 0
		+4.99939 V	011 . . . 1

END OF CONVERT

In asynchronous mode, End Of Convert (EOC) is an open drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by End Of Convert ENable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output which is enabled by $\overline{EOCEN}$ and $\overline{CS}$. (See Conversion Status Truth Table.) Access (t_{BA}) and float (t_{FD}) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the external load capacitance and the pull-up resistor.

OUTPUT ENABLE OPERATION

The data bits (DB7–DB0) are three-state outputs that are enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. Output Enable ($\overline{OE}$) must be toggled to update the output register.

The output is read as a 16-bit word, with High-Byte Enable ($\overline{HBE}$) controlling the output sequence. The high byte should be read first, as doing so updates the value in the low byte register, which is read second. The 14-bit result is left-justified within the 16-bit field.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REFOUT), output coding is twos complement binary.

POWER-UP

A conversion sequence, consisting of one $\overline{SC}$ instruction, is required after power-up to reset internal logic.

CONVERSION STATUS TRUTH TABLE

	INPUTS			OUTPUT	
	SYNC	$\overline{CS}$	$\overline{EOCEN}$	EOC	STATUS
Synchronous Mode	1	0	0	0	Converting
	1	0	0	1	Not Converting
	1	1	X	High Z	Either
	1	X	1	High Z	Either
Asynchronous Mode*	0	X	0	0	Converting
	0	X	0	High Z	Not Converting
	0	X	1	High Z	Either

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
*EOC requires a pull-up resistor in asynchronous mode.

OUTPUT ENABLE TRUTH TABLE

	INPUTS		OUTPUTS							
	$\overline{HBE}$	($\overline{CS}$ U $\overline{OE}$)	DB7 . . . DB0							
	X	1	← High Z →							
Unipolar or Bipolar	0	0	a	b	c	d	e	f	g	h
	1	0	i	j	k	l	m	n	0	0

NOTES
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
U = Logical OR.
a = MSB.
n = LSB.

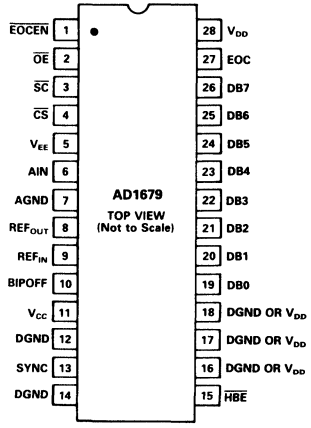
Data coding is straight binary for Unipolar Mode and 2s complement binary for Bipolar Mode.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	−12	+12	V
REF_{IN}	V_{EE}	0	V_{CC}	V
REF_{IN}	V_{CC}	V_{EE}	0	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature		0	+70	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



3

ESD SENSITIVITY

The AD1679 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD1679 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

ORDERING GUIDE

Model	Package	S/N+D[1]	Temperature Range	Digital Interface Format[2]	Package Options[3]
AD1679JN	28-Pin Plastic DIP	79 dB	0 to +70°C	2 Cycle Read (8+6 Bits)	N-28A
AD1679KN	28-Pin Plastic DIP	81 dB	0 to +70°C	2 Cycle Read (8+6 Bits)	N-28A
AD1679JD	28-Pin Ceramic DIP	79 dB	0 to +70°C	2 Cycle Read (8+6 Bits)	D-28A
AD1679KD	28-Pin Ceramic DIP	81 dB	0 to +70°C	2 Cycle Read (8+6 Bits)	D-28A

NOTES
[1]Typical @ 10 kHz, −0.5 dB input.
[2]For 14-bit parallel read interface to 16-bit buses, see AD1779.
[3]See Section 14 for package outline information.

AD1679 PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground. This is the ground return for AIN only.
AIN	6	A1	Analog Signal Input.
BIPOFF	10	A1	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} for ±5 V input bipolar mode and twos complement binary output coding.
$\overline{CS}$	4	D1	Chip Select. Active LOW.
DGND	12, 14	P	Digital Ground.
DB7–DB0	26–19	DO	Data Bits. These pins provide all 14 bits in two bytes (8+6 bits). Active HIGH.
EOC	27	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. In asynchronous mode, EOC is an open drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating.
$\overline{EOCEN}$	1	DI	End-Of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{HBE}$	15	DI	High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte (corresponding to the most recently read high byte).
$\overline{OE}$	2	DI	Output Enable. A down-going transition on $\overline{OE}$ enables data bits. Gated with $\overline{CS}$; Active LOW.
REF_{IN}	9	AI	Reference Input. +5 V input gives 10 V full-scale range.
REF_{OUT}	8	AO	+5 V Reference Output. Tied to REF_{IN} for normal operation.
$\overline{SC}$	3	DI	Start Convert. Active LOW. See SYNC pin for gating.
SYNC	13	DI	SYNC Control. If tied to V_{DD} (synchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open drain output. EOC requires an external 3k Ω pull-up resistor in asynchronous mode.
V_{CC}	11	P	+12 V Analog Power.
V_{EE}	5	P	−12 V Analog Power.
V_{DD}	28	P	+5 V Digital Power.
–	16–18	U	These pins are unused and should be connected to DGND or V_{DD}.

Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers.
P = Power.
U = Unused.

FREQUENCY DOMAIN TESTING
The AD1679 is tested dynamically using a sine wave input and a 2048 point Fast Fourier Transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral number of input cycles is captured, allowing direct FFT processing without windowing or digital filtering which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to be "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called Prime Coherent Sampling, is a highly accurate and repeatable measure of the actual frequency domain response of the converter.

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased components are used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD1679 has been designed to optimize input bandwidth, allowing it to undersample input signal frequencies significantly above the converter's Nyquist frequency. If the input signal is suitably band-limited, the spectral content of the input signal can be recovered.

APERTURE DELAY
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

For the AD1679, this specification is 14 bits from T_{min} to T_{max}, which guarantees that all 16,384 codes are present over temperature.

UNIPOLAR ZERO ERROR
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR
In the bipolar mode, the major carry transition (11 1111 1111 1111 to 00 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR
The full-scale transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9991 volts for a 0–10 V range, 4.9991 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

Application Information

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD1679 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 300 Ω. The 10 V p-p full scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

In some applications, offset and gain errors need to be more precisely trimmed. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 11. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the specified AD1679 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 80 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−0.305 mV for a ±5 V range) and adjust R1 until the major carry transition is located (11 1111 1111 1111 to 00 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9997 V for a ±5 V range) and adjust R2 to give the last positive transition (01 1111 1111 1110 to 01 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9997 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (10 0000 0000 0000 to 10 000 000 0001). Then perform the gain error trim as outlined above.

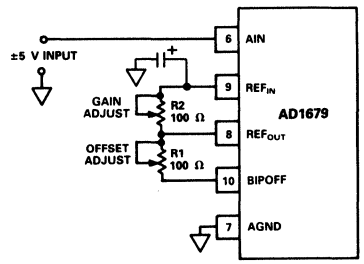


Figure 11. Bipolar Input Connections with Gain and Offset Trims

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 12. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code will be centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 00 0000 0000 0000 to 00 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (0.305 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 0.305 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9997 V for a 10 V range) and adjust R2 until the last transition is located (11 1111 1111 1110 to 11 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

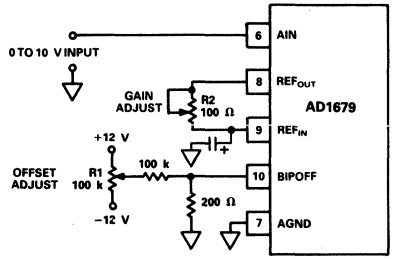


Figure 12. Unipolar Input Connections with Gain and Offset Trims

REFERENCE DECOUPLING

It is recommended that a 10 μF tantalum capacitor be connected between REF_{IN} (Pin 9) and ground. This has the effect of improving the S/N+D ratio through filtering possible broad-band noise contributions from the voltage reference.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 1 LSB at the 14-bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD1679 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB7–DB0 and EOC.

SUPPLY DECOUPLING

The AD1679 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling .

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD1679, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD1679 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD1679 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD1679. If multiple AD1679s are used or the AD1679 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This single interconnection of grounds prevents large ground loops and consequently prevents digital currents from flowing through the analog ground.

3

INTERFACING THE AD1679 TO MICROPROCESSORS

The I/O capabilities of the AD1679 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion option allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD1679 interface configurations.

AD1679 TO TMS320C25

In Figure 13 the AD1679 is mapped into the TMS320C25 I/O space. AD1679 conversions are initiated by issuing an OUT instruction to Port 1. EOC status and the conversion result are read in with an IN instruction to Port 1. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 1 and $\overline{MSC}$. Address line A0 provides HBE decoding to select between the high and low bytes of data. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD1679 read instruction.

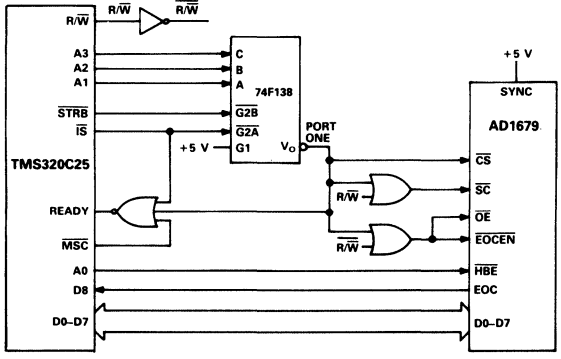


Figure 13. AD1679 to TMS320C25 Interface

AD1679 TO 80186

Figure 14 shows the AD1679 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD1679 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD1679 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD1679 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ sequences the high and low byte AD1679 data and resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

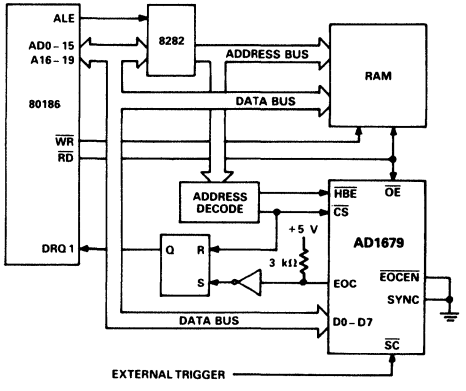


Figure 14. AD1679 to 80186 DMA Interface

AD1679 TO Z80

The AD1679 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 15 illustrates an I/O configuration, where the AD1679 occupies several port addresses to allow separate polling of the EOC status and reading of the data. The lower address bit, A0, is used to select the high and low order bytes of the result.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD1679 to be used with Z80 processors having clock speeds up to 8 MHz.

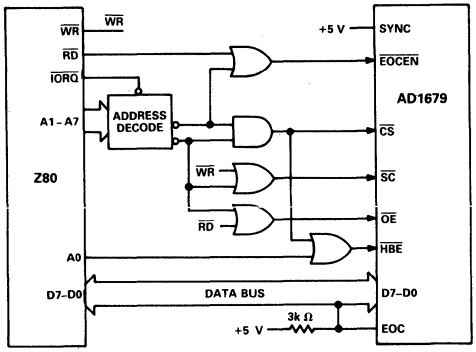


Figure 15. AD1679 to Z80 Interface

AD1679 TO ANALOG DEVICES ADSP-2100A

Figure 16 demonstrates the AD1679 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD1679 data memory interface with two hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD1679 is asserted at the end of each conversion and creates a high priority interrupt to the processor through $\overline{IRQ3}$. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction which asserts $\overline{HBE}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latches, is used to force the ADSP-2100A into a two-cycle wait state by generating DMACK. The read operation is thus started and completed within three processor cycles (240 ns). $\overline{HBE}$ is released during "high byte read." This allows the processor to read the lower byte of data as soon as "high byte read" is complete. Low byte read is executed in a similar manner and is completed during the next 240 ns.

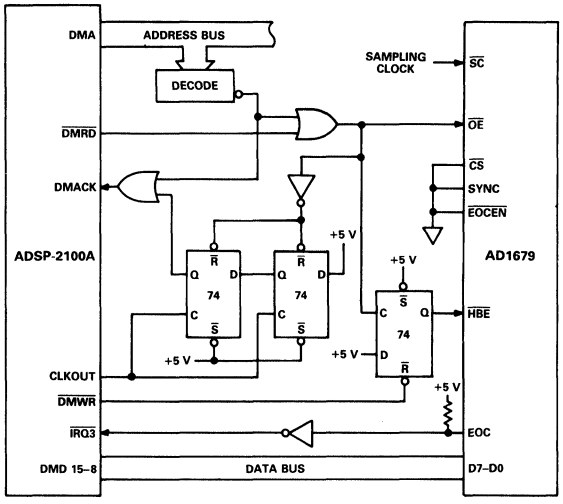


Figure 16. AD1679 to ADSP-2100A Interface

ANALOG DEVICES

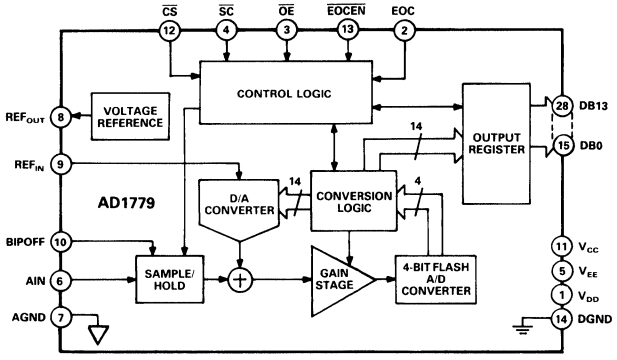
14-Bit 100 KSPS Complete Sampling ADC

AD1779

FEATURES

AC Characterized and Specified
100k Conversions per Second
1 MHz Full Power Bandwidth
500 kHz Full Linear Bandwidth
80 dB S/N+D (K Grade)
Twos Complement Data Format (Bipolar Mode)
Straight Binary Data Format (Unipolar Mode)
10 MΩ Input Impedance
16-Bit Bus Interface (See AD1679 for 8-Bit Interface)
On-Board Reference and Clock
10 V Unipolar or Bipolar Input Range

AD1779 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1779 is a complete, 14-bit monolithic analog-to-digital converter consisting of a sample-hold amplifier (SHA), a microprocessor compatible bus interface, a voltage reference and clock generation circuitry.

The 14 data bits are accessed by a 16-bit bus in a single read operation. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm, which includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD1779 operates from +5 V and ±12 V supplies and dissipates 720 mW. A 28-pin plastic DIP and a 0.6″ wide ceramic DIP are available. Contact factory for surface-mount package options.

PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD1779 minimizes external component requirements by combining a high speed sample-hold amplifier (SHA), ADC, 5 V reference, clock and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. PERFORMANCE: The AD1779 provides a throughput of 100k conversions per second. S/N+D is 80 dB (K grade) at 10 kHz and remains flat beyond the Nyquist frequency.
3. SPECIFICATIONS: The AD1779 is specified for ac (or "dynamic") parameters such as S/N+D ratio, THD and IMD. These parameters are important in signal processing applications as they indicate the AD1779's effect on the spectral content of the input signal.
4. EASE OF USE: The pinout is designed for easy board layout, and the single read output provides compatibility with 16-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
5. RELIABILITY: The AD1779 utilizes Analog Devices' monolithic BiMOS technology. This ensures long term reliability compared to multichip and hybrid designs.

SPECIFICATIONS

AC SPECIFICATIONS (T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = + 5 V ±10%, f_{SAMPLE} = 100 KSPS, f_{IN} = 10.009 kHz unless otherwise noted)[1]

Parameter	AD1779J Min	AD1779J Typ	AD1779J Max	AD1779K Min	AD1779K Typ	AD1779K Max	Units
SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2]							
−0.5 dB Input (Referred to −0 dB Input)	**78**	79		**80**	81		dB
−20 dB Input (Referred to −20 dB Input)	58	59		60	61		dB
−60 dB Input (Referred to −60 dB Input)	18	19		20	21		dB
TOTAL HARMONIC DISTORTION (THD)[3]							
@ +25°C		−90	**−84**		−90	**−84**	dB
		0.003	**0.006**		0.003	**0.006**	%
T_{min} to T_{max}		−88	**−82**		−88	**−82**	dB
		0.004	**0.008**		0.004	**0.008**	%
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		−90	**−84**		−90	**−84**	dB
FULL POWER BANDWIDTH		1			1		MHz
FULL LINEAR BANDWIDTH	500			500			kHz
INTERMODULATION DISTORTION (IMD)[4]							
2nd Order Products		−90	−84		−90	−84	dB
3rd Order Products		−90	−84		−90	−84	dB

NOTES
[1]f_{IN} amplitude = −0.5 dB (9.44 V p-p) bipolar mode full-scale unless otherwise indicated. All measurements referred to a −0 dB (9.997 V p-p) input signal unless otherwise noted.
[2]See Figure 7 for higher frequencies and other input amplitudes.
[3]See Figures 5 and 6 for other conditions.
[4]f_A = 9.08 kHz, f_B = 9.58 kHz, with f_{SAMPLE} = 100 KSPS. See Figure 9 and Definition of Specifications section.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		**2.4**		V
V_{IL}	Low Level Input Voltage			**0.8**	V
I_{IH}	High Level Input Current	V_{IN} = 5 V		**10**	μA
I_{IL}	Low Level Input Current	V_{IN} = 0 V		**10**	μA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	4.0		V
		I_{OH} = 0.5 mA	**2.4**		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		**0.4**	V
I_{OZ}	High Z Leakage Current	V_{IN} = 0 or 5 V		**10**	μA
C_{OZ}	High Z Output Capacitance			10	pF

NOTES
Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

DC SPECIFICATIONS (@ +25°C, V_{CC}=+12 V ±5%, V_{EE}=−12 V ±5%, V_{DD}=+5 V ±10% unless otherwise indicated)

Parameter	AD1779J Min	AD1779J Typ	AD1779J Max	AD1779K Min	AD1779K Typ	AD1779K Max	Units
ACCURACY							
Resolution	**14**			**14**			Bits
Integral Linearity Error		±1			±1		LSB
Differential Linearity							
T_{min} to T_{max} (No Missing Codes)	**14**			**14**			Bits
Unipolar Zero Error[1]		±10			±10		LSB
Bipolar Zero Error[1]		±10			±10		LSB
Unipolar Gain Error[1,2]		±12			±12		LSB
Bipolar Gain Error[1,2]		±12			±12		LSB
Temperature Drift (Coefficients)[3]							
Unipolar Zero		±8 (10)			±8 (10)		LSB (ppm/°C)
Bipolar Zero		±8 (10)			±8 (10)		LSB (ppm/°C)
Unipolar Gain		±16 (20)			±16 (20)		LSB (ppm/°C)
Bipolar Gain		±16 (20)			±16 (20)		LSB (ppm/°C)
ANALOG INPUT							
Input Ranges							
Unipolar Mode	0		+10	0		+10	V
Bipolar Mode	−5		+5	−5		+5	V
Input Resistance		10			10		MΩ
Input Capacitance		10			10		pF
Input Settling Time			1			1	μs
Aperture Delay	5		20	5		20	ns
Aperture Jitter		150			150		ps
INTERNAL VOLTAGE REFERENCE							
Output Voltage[4]	**4.95**		**5.05**	**4.95**		**5.05**	V
External Load							
Unipolar Mode			**+1.5**			**+1.5**	mA
Bipolar Mode			**+0.5**			**+0.5**	mA
Power Supply Rejection		1			1		mV/V
POWER SUPPLIES (T_{min} to T_{max})							
Operating Voltages							
V_{CC}	+11.4	+12	+12.6	+11.4	+12	+12.6	V
V_{EE}	−12.6	−12	−11.4	−12.6	−12	−11.4	V
V_{DD}	+4.5	+5	+5.5	+4.5	+5	+5.5	V
Operating Current							
I_{CC}		18	**20**		18	**20**	mA
I_{EE}		25	**32**		25	**32**	mA
I_{DD}		8	**12**		8	**12**	mA
Power Consumption		560	720		560	720	mW

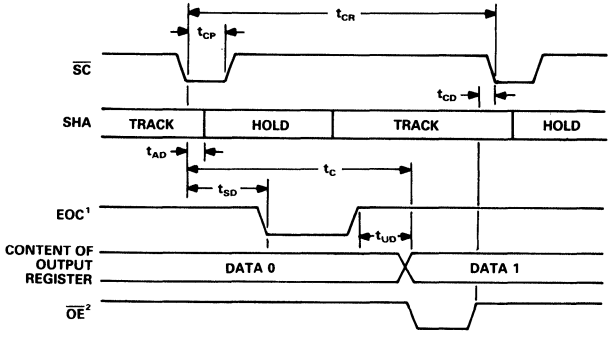
NOTES
[1]Adjustable to zero; see Figures 11 and 12.
[2]Includes internal voltage reference error.
[3]Includes internal voltage reference drift.
[4]With maximum external load applied.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at 0°C, +25°C and +70°C. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (All device types T_{min} to T_{max}, V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5%, V_{DD} = +5 V ±10%)

Parameter	Symbol	Min	Max	Units
Conversion Rate[1]	t_{CR}		10	µs
Convert Pulse Width	t_{CP}	150		ns
Aperture Delay	t_{AD}	5	20	ns
Conversion Time	t_C		**8.5**	µs
Status Delay	t_{SD}	0	400	ns
Access Time[2]	t_{BA}		**100**	ns
Float Delay[3]	t_{FD}	10	**80**	ns
Update Delay	t_{UD}		200	ns
$\overline{OE}$ Delay	t_{OE}	20		ns
Read Pulse Width	t_{RP}	150		ns
Conversion Delay	t_{CD}	400		ns

NOTES
[1]Includes Acquisition Time.
[2]Measured from the falling edge of $\overline{OE}$/$\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4; C_{OUT} = 100 pF.
[3]Measured from the rising edge of $\overline{OE}$/$\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5 V. See Figure 4; C_{OUT} = 10 pF.
Specifications subject to change without notice.



NOTES
[1]$\overline{EOCEN}$ = LOW.
[2]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

Figure 1. Conversion Timing

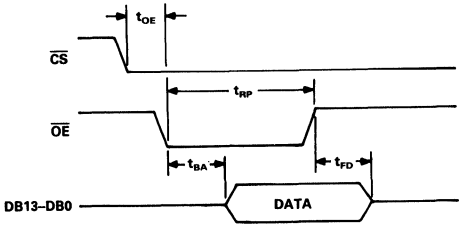


Figure 2. Output Timing

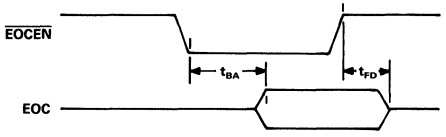


Figure 3. EOC Timing

TEST	V_{CP}	C_{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5 V	100 pF
FLOAT TIME LOGIC HIGH TO HIGH Z	5 V	10 pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0 V	100 pF
FLOAT TIME LOGIC LOW TO HIGH Z	0 V	10 pF

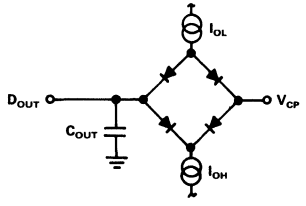


Figure 4. Load Circuit for Bus Timing Specifications

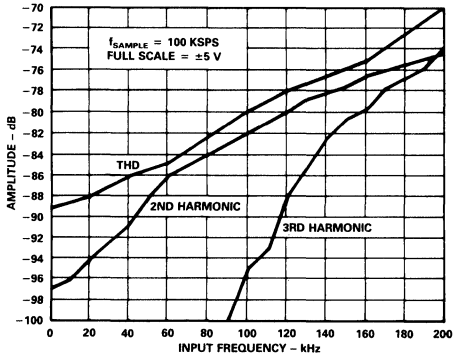


Figure 5. Harmonic Distortion vs. Input Frequency (−0.5 dB Input)

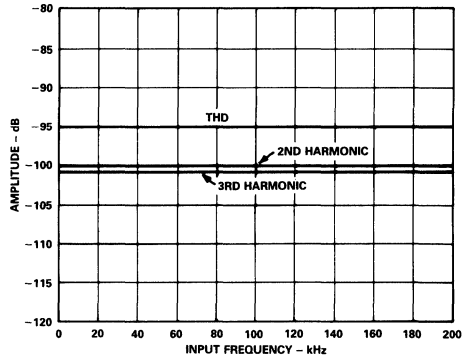


Figure 6. Harmonic Distortion vs. Input Frequency (−20 dB Input)

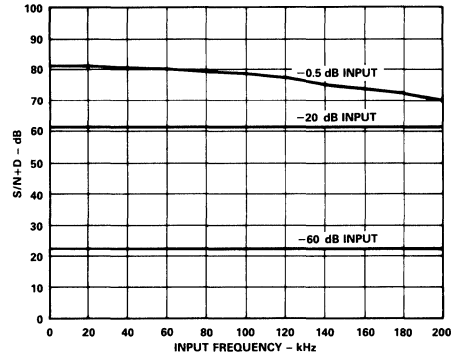


Figure 7. S/N+D vs. Input Frequency and Amplitude

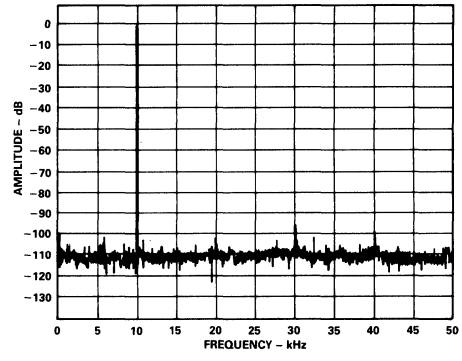


Figure 8. 5-Plot Averaged 2048 Point FFT at 100 KSPS, f_{IN} = 10.009 kHz

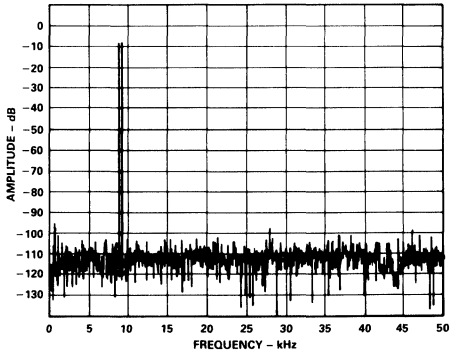


Figure 9. Nonaveraged IMD Plot for f_{IN} = 9.08 kHz (f_a), 9.58 kHz (f_b) at 100 KSPS

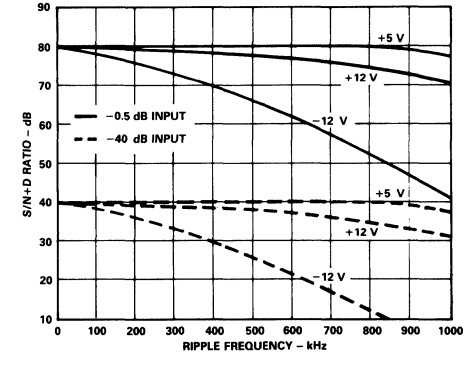


Figure 10. Power Supply Rejection (f_{IN} = 10 kHz, f_{SAMPLE} = 100 KSPS, V_{RIPPLE} = 0.1 V p-p)

CONVERSION CONTROL

Before a conversion is started, End Of Convert (EOC) is HIGH and the sample-hold is in track mode. A conversion is started by bringing $\overline{SC}$ LOW, regardless of the state of $\overline{CS}$.

After a conversion is started, the sample-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-hold will go back into track mode and start acquiring the next sample.

In track mode, the sample-hold will settle to ±0.003% (14 bits) in 1.5 μs maximum. The acquisition time does not affect the throughput rate as the AD1779 goes back into track mode more than 2 μs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW if the maximum throughput rate is needed.

When the conversion is finished, EOC goes HIGH and the result is loaded into the output register after a period of time t_{UD}. Bringing $\overline{OE}$ LOW makes the output register contents available on the output data bits (DB13–DB0). A period of time t_{CD} is required after $\overline{OE}$ is brought HIGH before the next $\overline{SC}$ instruction is issued. This is to allow internal logic states to reset and guarantees minimum aperture jitter for the next conversion.

If $\overline{SC}$ is held LOW, conversions will occur continuously. EOC will go HIGH for approximately 1.5 μs between conversions.

END-OF-CONVERT

End-of-Convert (EOC) is a three-state output which is enabled by End-of-Convert ENable $\overline{EOCEN}$.

OUTPUT ENABLE OPERATION

The data bits (DB13–DB0) are three-state outputs that are enabled by Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). $\overline{CS}$ should be LOW t_{OE} before $\overline{OE}$ is brought LOW. $\overline{OE}$ must be toggled to update the output register. The output is read in a single cycle as a 14-bit word.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to REFOUT), output coding is twos complement binary.

POWER-UP

A conversion sequence, consisting of one $\overline{SC}$ instruction, is required after power-up to reset internal logic.

14-BIT MODE CODING FORMAT (1 LSB =0.61 mV)

Unipolar Coding (Straight Binary)		Bipolar Coding (Twos Complement)	
V_{IN}	Output Code	V_{IN}	Output Code
0	000 . . . 0	−5.00000 V	100 . . . 0
5.00000 V	100 . . . 0	−0.00061 V	111 . . . 1
9.99939 V	111 . . . 1	0	000 . . . 0
		+2.50000 V	010 . . . 0
		+4.99939 V	011 . . . 1

CONVERSION TRUTH TABLE

	INPUTS				OUTPUTS		
Mode	$\overline{SC}$	$\overline{EOCEN}$	$\overline{CS}$	$\overline{OE}$	EOC	DB13 . . . DB0	Status
Start Conversion	1	X	X	X			No Conversion
	↓	X	X	X			Start Conversion
	0	X	X	X			Continuous Conversion
Conversion Status	X	0	X	X	0		Converting
	X	0	X	X	1		Not Converting
	X	1	X	X	High Z		Either
Data Access	X	X	X	1		High Z	Three-State
	X	X	1	X		High Z	Three-State
	X	X	0	0		MSB . . . LSB	Data Out

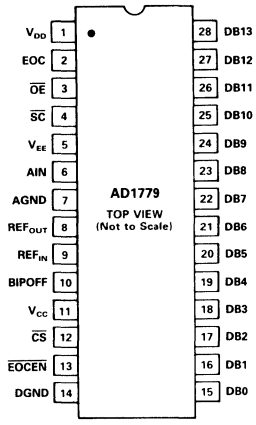
NOTES
U = Logical OR.
1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay LOW for t = t_{CP}.

ABSOLUTE MAXIMUM RATINGS*

Specification	With Respect To	Min	Max	Units
V_{CC}	AGND	−0.3	+18	V
V_{EE}	AGND	−18	+0.3	V
V_{CC}	V_{EE}	−0.3	+26.4	V
V_{DD}	DGND	0	+7	V
AGND	DGND	−1	+1	V
AIN, REF_{IN}	AGND	−12	+12	V
REF_{IN}	V_{EE}	0	V_{CC}	V
REF_{IN}	V_{CC}	V_{EE}	0	V
Digital Inputs	DGND	−0.5	+7	V
Digital Outputs	DGND	−0.5	V_{DD} +0.3	V
Max Junction Temperature			175	°C
Operating Temperature		0	+70	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



3

ESD SENSITIVITY

The AD1779 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD1779 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

ORDERING GUIDE

Model	Package	S/N+D[1]	Temperature Range	Digital Interface Format[2]	Package Options[3]
AD1779JN	28-Pin Plastic DIP	79 dB	0 to +70°C	1 Cycle Read (14 Bits)	N-28A
AD1779KN	28-Pin Plastic DIP	81 dB	0 to +70°C	1 Cycle Read (14 Bits)	N-28A
AD1779JD	28-Pin Ceramic DIP	79 dB	0 to +70°C	1 Cycle Read (14 Bits)	D-28A
AD1779KD	28-Pin Ceramic DIP	81 dB	0 to +70°C	1 Cycle Read (14 Bits)	D-28A

NOTES
[1]Typical @ 10 kHz, −0.5 dB input.
[2]For 2 cycle read (8+6 bits) interface to 8-bit buses, see AD1679.
[3]See Section 14 for package outline information.

AD1779 PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	7	P	Analog Ground. This is the ground return for AIN only.
AIN	6	AI	Analog Signal Input.
BIPOFF	10	AI	Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to REF_{OUT} for ±5 V input bipolar mode and twos complement binary output coding.
$\overline{CS}$	12	DI	Chip Select. Active LOW.
DGND	14	P	Digital Ground.
DB13–DB0	28–15	DO	Data Bits. These pins provide all 14 bits in one 14 bit parallel output. Active HIGH.
EOC	2	DO	End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion is finished. EOC is a three-state output. See $\overline{EOCEN}$ pin for information on EOC gating.
$\overline{EOCEN}$	13	DI	End-of-Convert Enable. Enables EOC pin. Active LOW.
$\overline{OE}$	3	DI	Output Enable. A down-going transition on $\overline{OE}$ enables data bits. Active LOW.
REF_{IN}	9	AI	Reference Input. +5 V input gives 10 V full scale range.
REF_{OUT}	8	AO	+5 V Reference Output. Tied to REF_{IN} for normal operation.
$\overline{SC}$	4	DI	Start Convert. Active LOW.
V_{CC}	11	P	+12 V Analog Power.
V_{EE}	5	P	−12 V Analog Power.
V_{DD}	1	P	+5 V Digital Power.

Type: AI = Analog Input.
AO = Analog Output.
DI = Digital Input (TTL and 5 V CMOS compatible).
DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are tri-state drivers.
P = Power.

FREQUENCY DOMAIN TESTING

The AD1779 is tested dynamically using a sine wave input and a 2048 point Fast Fourier Transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral number of input cycles is captured, allowing direct FFT processing without windowing or digital filtering which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to be "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called Prime Coherent Sampling, is a highly accurate and repeatable measure of the actual frequency domain response of the converter.

NYQUIST FREQUENCY

An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of a full-scale input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased components are used.

PEAK SPURIOUS OR PEAK HARMONIC COMPONENT

The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb) and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (fa − 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude and the peak value of their sum is −0.5 dB from full scale (9.44 V p-p). The IMD products are normalized to a −0 dB input signal.

BANDWIDTH

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than −0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD1779 has been designed to optimize input bandwidth, allowing it to undersample input signal frequencies significantly above the converter's Nyquist frequency. If the input signal is suitably band-limited, the spectral content of the input signal can be recovered.

APERTURE DELAY

Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Start Convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, Chip Select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

INPUT SETTLING TIME

Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

DIFFERENTIAL NONLINEARITY (DNL)

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

For the AD1779, this specification is 14 bits from T_{min} to T_{max}, which guarantees that all 16,384 codes are present over temperature.

UNIPOLAR ZERO ERROR

In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

BIPOLAR ZERO ERROR

In the bipolar mode, the major carry transition (11 1111 1111 1111 to 00 0000 0000 0000) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

GAIN ERROR

The full-scale transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9991 volts for a 0–10 V range, 4.9991 volts for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

Application Information

INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD1779 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 300 Ω. The 10 V p-p full scale input range accepts the majority of signal voltages without the need for voltage divider networks which could deteriorate the accuracy of the ADC.

In some applications, offset and gain errors need to be more precisely trimmed. The following sections describe the correct procedure for these various situations.

BIPOLAR RANGE INPUTS

The connections for the bipolar mode are shown in Figure 11. In this mode, data output coding will be twos complement binary. This circuit will allow approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the specified AD1779 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 80 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (−0.305 mV for a ±5 V range) and adjust R1 until the major carry transition is located (11 1111 1111 1111 to 00 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9997 V for a ±5 V range) and adjust R2 to give the last positive transition (01 1111 1111 1110 to 01 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (−4.9997 V for a ±5 V range) and adjust R1 until the minus full scale transition is located (10 0000 0000 0000 to 10 0000 0000 0001). Then perform the gain error trim as outlined above.

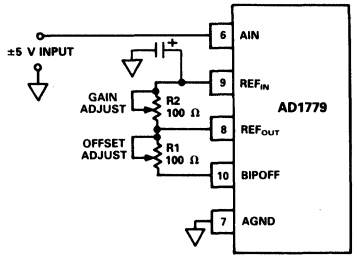


Figure 11. Bipolar Input Connections with Gain and Offset Trims

UNIPOLAR RANGE INPUTS

Offset and gain errors can be trimmed out by using the configuration shown in Figure 12. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code will be centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 00 0000 0000 0000 to 00 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (0.305 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 0.305 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9997 V for a 10 V range) and adjust R2 until the last transition is located (11 1111 1111 1110 to 11 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF_{OUT} is connected directly to REF_{IN}, the additional gain error will be approximately 1%.

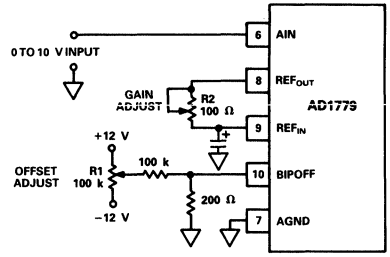


Figure 12. Unipolar Input Connections with Gain and Offset Trims

REFERENCE DECOUPLING

It is recommended that a 10 μF tantalum capacitor be connected between REF_{IN} (Pin 9) and ground. This has the effect of improving the S/N+D ratio through filtering possible broad-band noise contributions from the voltage reference.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 1 LSB at the 14-bit level for a 10 V full scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD1779 incorporates several features to help the user's layout. Analog pins (V_{EE}, AIN, AGND, REF_{OUT}, REF_{IN}, BIPOFF, V_{CC}) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB13–DB0 and EOC.

SUPPLY DECOUPLING

The AD1779 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling .

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD1779, associated analog input circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD1779 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

If a single AD1779 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD1779. If multiple AD1779s are used or the AD1779 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This single interconnection of grounds prevents large ground loops and consequently prevents digital currents from flowing through the analog ground.

3

INTERFACING THE AD1779 TO MICROPROCESSORS

The I/O capabilities of the AD1779 allow direct interfacing to general purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD1779 interface configurations.

AD1779 TO TMS320C25

In Figure 13 the AD1779 is mapped into the TMS320C25 I/O space. AD1779 conversions are initiated by issuing an OUT instruction to Port 8. EOC status and the conversion result are read in with an IN instruction to Port 8. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 8 and $\overline{MSC}$. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD1779 read instruction.

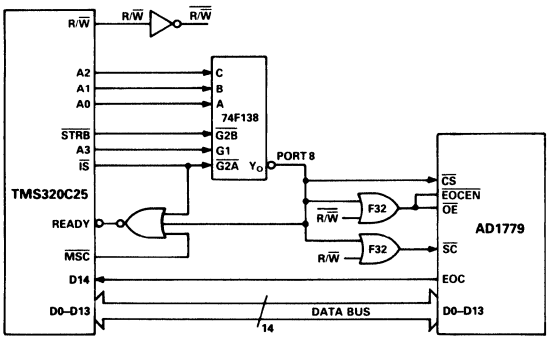


Figure 13. AD1779 to TMS320C25 Interface

AD1779 TO 80186

Figure 14 shows the AD1779 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD1779 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

The AD1779 is asynchronous which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD1779 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ sequences the high and low byte AD1779 data and resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

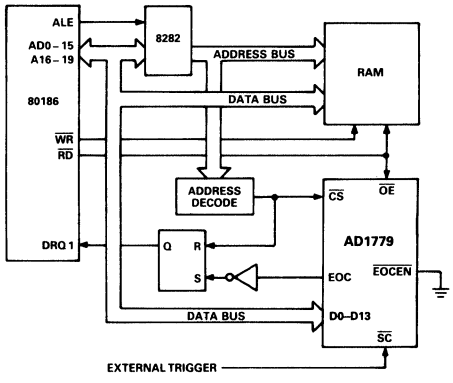


Figure 14. AD1779 to 80186 DMA Interface

AD1779 TO Z80

The AD1779 can be interfaced to the Z80 processor in an I/O or memory mapped configuration. Figure 15 illustrates an I/O configuration, where the AD1779 occupies several port addresses to allow separate polling of the EOC status and reading of the data.

A useful feature of the Z80 is that a single wait state is automatically inserted during I/O operations, allowing the AD1779 to be used with Z80 processors having clock speeds up to 8 MHz.

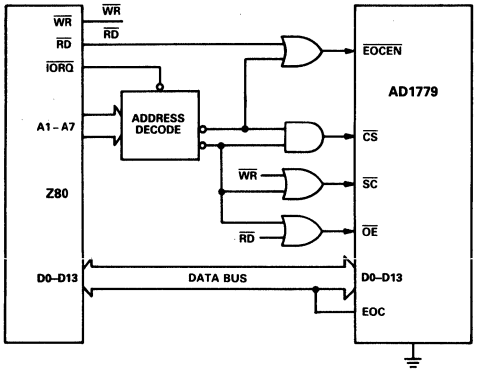


Figure 15. AD1779 to Z80 Interface

AD1779 TO ANALOG DEVICES ADSP-2100A

Figure 16 demonstrates the AD1779 interfaced to an ADSP-2100A. With a clock frequency of 1.25 MHz, and instruction execution in one 80 ns cycle, the digital signal processor will support the AD1779 data memory interface with two wait states.

The converter runs asychronously using a sampling clock. The EOC output of the AD1779 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A starts a data memory read by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latches, is used to force the ADSP-2100A into a two cycle wait state by generating DMACK. The read operation is thus started and completed within three processor cycles (240 ns).

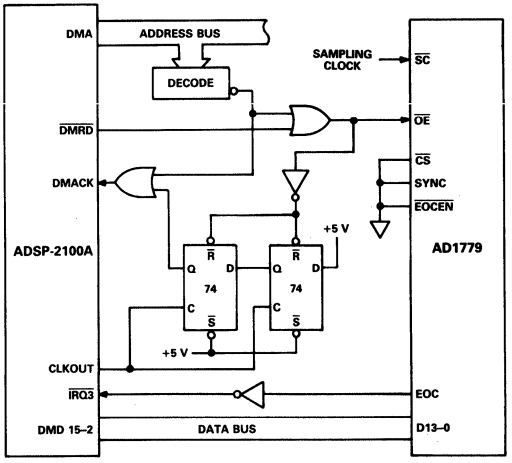


Figure 16. AD1779 to ADSP-2100A Interface

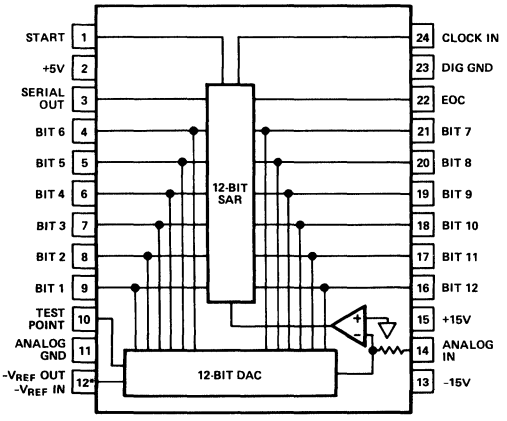
12-Bit Successive Approximation High Accuracy A/D Converters

AD5200/AD5210 Series

FEATURES

- True 12-Bit Operation: ±1/2LSB max Nonlinearity
- Totally Adjustment-Free
- Guaranteed No Missing Codes Over the Specified Temperature Range
- Hermetically-Sealed Package
- Standard Temperature Range: -25°C to +85°C
- Extended Temperature Range: -55°C to +125°C
- Serial and Parallel Outputs
- Monolithic DAC with Scaling Resistors for Stability
- Low Chip Count for High Reliability
- Industry Standard Pin Out
- Small 24-Pin DIP
- MIL-STD-883B Processing Available

AD5200/AD5210 FUNCTIONAL BLOCK DIAGRAM



*PIN 12 FUNCTION: $-V_{REF}$ OUT – AD52X1, AD52X2
$-V_{REF}$ IN – AD52X4, AD52X5

GENERAL DESCRIPTION

The AD52XX series devices are 12-bit successive approximation analog-to-digital converters. The hybrid design utilizes MSI digital, linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide a totally adjustment free converter—no potentiometers are required for calibration.

The innovative design of the AD52XX series devices incorporates a monolithic 12-bit feedback DAC for reduced chip count and higher reliability. The exceptional temperature coefficients of the monolithic DAC guarantees ±1/2LSB linearity over the entire operating temperature range of -25°C to +85°C for the BD grade and -55°C to +125°C for the TD grade.

The AD52XX series converters are available in 2 input voltage ranges: ±5V (AD52X1/AD52X4) and ±10V (AD52X2/AD52X5). The converters are available either complete with an internal buried zener reference or with the option of an external reference for improved absolute accuracy.

The AD52XX series converters are available in two performance grades; the "B" is specified from -25°C to +85°C and the "T" is specified from -55°C to +125°C. All units are available in a 24-pin hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD52XX series devices are laser trimmed at the factory to provide a totally adjustment free converter—no potentiometers are required for 12-bit performance.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The AD52XX series directly replaces other devices of this type with significant increases in performance.
4. The devices offer true 12-bit accuracy and exhibits no missing codes over the entire operating temperature range.
5. The fast conversion rate of the AD5210 series makes it an excellent choice for applications requiring high system throughput rates.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

INPUT RANGE[1]	INPUT IMPEDANCE				
-5V to +5V	5.0kΩ	AD52X1B	AD52X1T	AD52X4B	AD52X4T
-10V to +10V	10.0kΩ	AD52X2B	AD52X2T	AD52X5B	AD52X5T
REFERENCE		Internal	*	External -10.000V	***
RESOLUTION		12 Bits	*	*	*
LINEARITY ERROR, MAX		±1/2LSB	*	*	*
No Missing Codes T_{min} to T_{max}		Guaranteed	*	*	*
ZERO ERROR, MAX		±1LSB	*	*	*
ZERO ERROR, MAX T_{min} to T_{max}		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX T_{min} to T_{max}		±0.4% of FSR[2]	*	±0.1% of FSR[2]	***
CONVERSION TIME, MAX					
Clock = 1MHz (5210 Series)		13μs	*	*	*
Clock = 260kHz (5200 Series)		50μs	*	*	*
LOGIC RATINGS					
Input Logic Commands					
Logic "0"		0.8V max	*	*	*
Logic "1"		+2.0V min	*	*	*
Loading		0.5TTL Load	*	*	*
CLOCK INPUT PULSE WIDTH		100ns min	*	*	*
OUTPUT LOGIC					
Logic "0"		0.4V max	*	*	*
Logic "1"		3.6V (2.4 min)	*	*	*
FANOUT - HIGH		8TTL Loads	*	*	*
FANOUT - LOW		2TTL Loads	*	*	*
POWER SUPPLY REQUIREMENTS					
V_{LOGIC}		+5V ±10%	*	*	*
V_{CC}		+15V ±10%	*	*	*
V_{DD}		-15V ±10%	*	*	*
OPERATING CURRENT					
V_{LOGIC}		25mA (42mA max)	*	*	*
V_{CC}		10mA (16mA max)	*	*	*
V_{DD}		20mA (28mA max)	*	*	*
V_{REF}				0.5mA	***
POWER SUPPLY REJECTION					
V_{CC}		±0.005%/% (±0.02%/% max)	*	*	*
V_{DD}		±0.005%/% (±0.02%/% max)	*	*	*
POWER CONSUMPTION		575mW (870mW max)	*	575mW (875mW max)	***
OPERATING TEMPERATURE RANGE		-25°C to +85°C	-55°C to +125°C	*	**

NOTES
*Same specifications as AD52X1/X2B.
**Same specifications as AD52X1/X2T.
***Same specifications as AD52X4/X5B.
[1] Other input ranges are available, consult factory.
[2] FSR is Full Scale Range and is equal to the peak to peak input signal.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Positive Supply	+18V
Negative Supply	-18V
Logic Supply	-0.5V to +7V
Analog Input	±25V
Digital Outputs	Logic Supply
Digital Inputs	+5.5V
Reference Supply	-15V

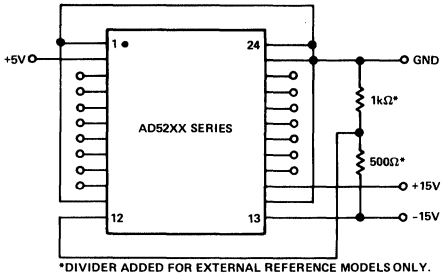


Figure 1. Burn In Circuit

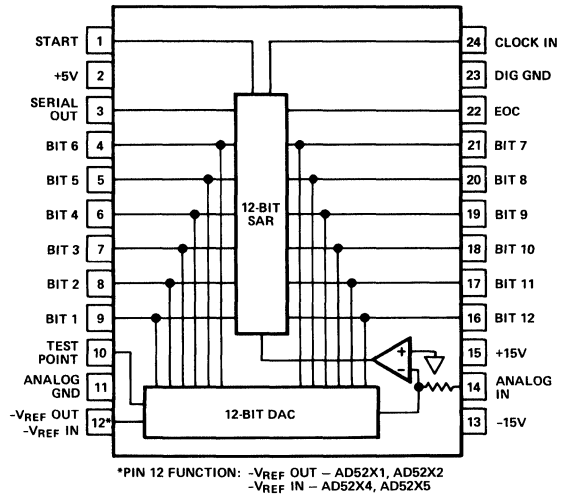


Figure 2. Pin Designations

AD52XX SERIES ORDERING GUIDE

Model	Linearity	Absolute Accuracy	Temperature Range	Conversion Time	Package Option*
AD521**BD	1/2LSB	2LSB	-25°C to +85°C	13μs	DH-24C
AD521**TD	1/2LSB	2LSB	-55°C to +125°C	13μs	DH-24C
AD520**BD	1/2LSB	2LSB	-25°C to +85°C	50μs	DH-24C
AD520**TD	1/2LSB	2LSB	-55°C to +125°C	50μs	DH-24C

NOTES:
TD grades are available with MIL-STD-883, Method 5008, Class B processing.
*See Section 14 for package outline information.
**Insert number according to desired input voltage range as shown in Table II.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD52XX converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12 outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 3. A conversion is initiated by holding the start convert low during a rising edge of the clock. The start convert transition must occur at a minimum of 25ns prior to the clock transition. The end of conversion (E.O.C.) signal will be set simultaneously with the initiation of conversion. The actual conversion will not start until the first rising edge of the clock after the start convert is again set high. At time t_0, B_1 is reset and B_2–B_{12} are set unconditionally. At t_1 the Bit 1 decision is made and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. The STATUS flag is reset at time t_{12} indicating that the conversion is complete and that the parallel output data is valid.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 3). An external clock of 1MHz (AD5210) will yield 13μs conversion time. An external clock of 260kHz (AD5200) will yield 50μs conversion time.

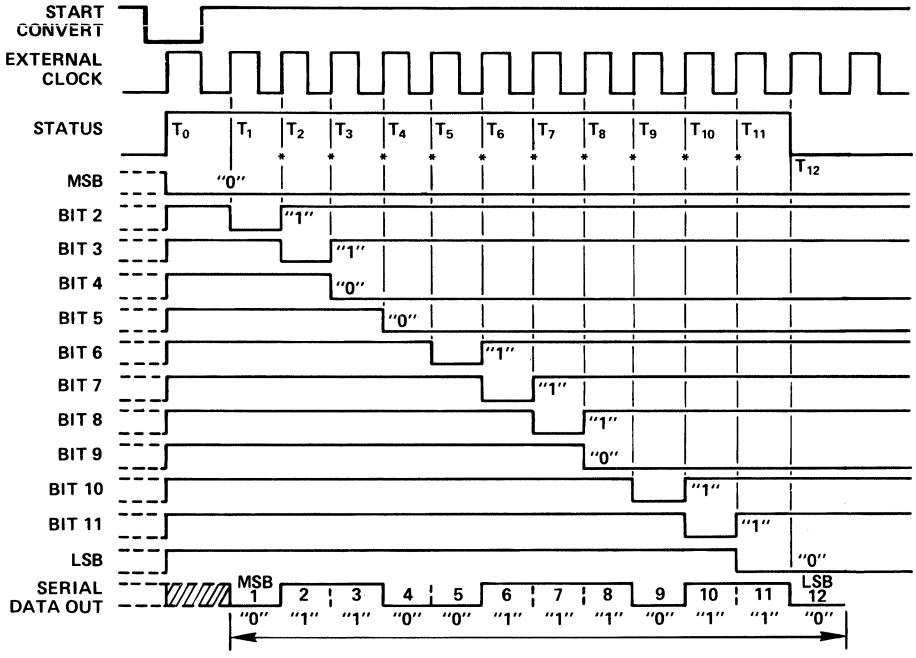


Figure 3. Timing Diagram

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors have been internally trimmed to provide an absolute accuracy of ±0.05%. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD52XX is specified as having no missing codes over the entire temperature range as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

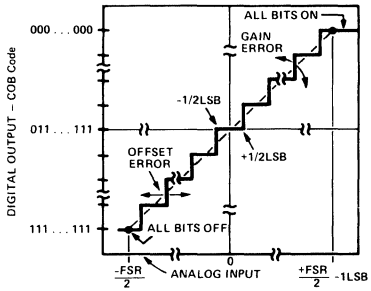


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Digital Ground and Analog Ground (Analog Power Return). These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD52XX. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

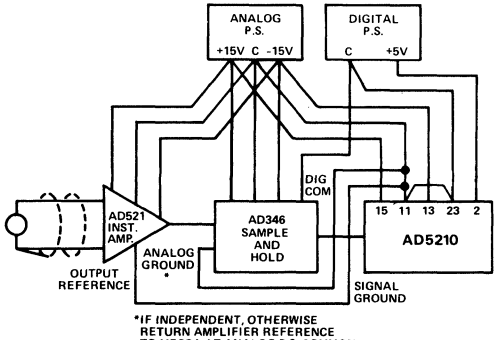


Figure 5. Basic Grounding Practice

Each of the AD52XX's supply terminals should be capacitively decoupled as close to the AD52XX as possible. A large value capacitor such as 1μF in parallel with 0.01μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Ground pin and the logic supply is bypassed to the Digital Ground pin.

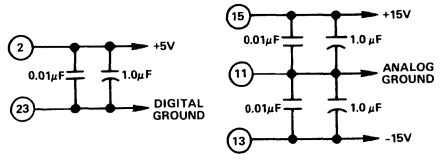


Figure 6. Power Supply Decoupling

SAMPLED DATA SYSTEMS

The conversion speed of the AD52XX allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. To make the AD52XX capable of full benefit from this high speed, a fast sample-hold amplifier such as the AD346 or ADSHC-85 is required. Figures 7 and 8 show the use of an AD346 and ADSHC-85 as sample and holds in combination with the AD52XX.

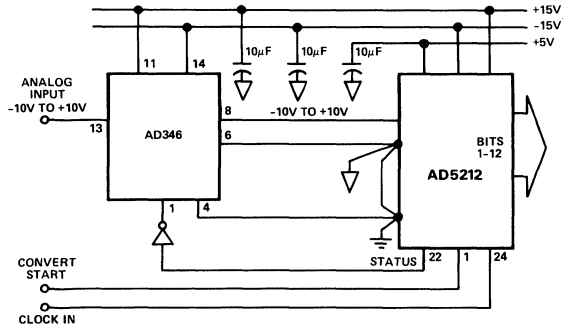


Figure 7. 66.6kHz–12 Bit, A/D Conversion System

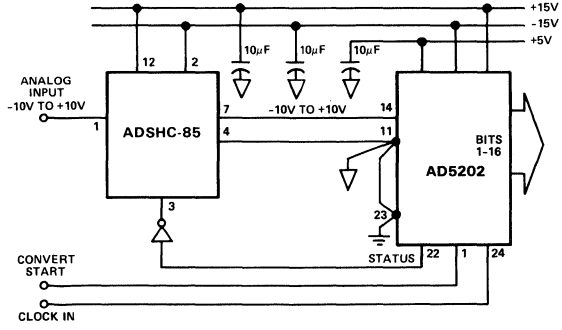


Figure 8. 18.3kHz–12-Bit, A/D Conversion System

In sampled data systems there are two limiting factors in digitizing high frequency signals. The maximum value of input signal frequency that can be acquired and digitized using a sample and hold amplifier and A/D converter combination is influenced by the bandwidth of the SHA, but it is also dictated by:

A. The aperture uncertainty (jitter) of the sample and hold amplifier.

B. The desired accuracy and corresponding resolution of the converter.

The resolution of an AD5210 is 1 part in 4096 to a tolerance of 0.012% of the full scale range, the maximum value of input signal frequency which can be digitized is determined by:

$$F_{MAX}/ = \frac{2^{-N}}{(2\pi)(\text{Aperture Uncertainty})}$$

$$F_{MAX}/AD346 = \frac{1}{(2\pi)\ (4096)\ (4 \times 10^{-10})} = 97.1\text{kHz}$$

$$F_{MAX}/ADSHC\text{-}85 = \frac{1}{(2\pi)\ (4096)\ (5 \times 10^{-10})} = 77.7\text{kHz}$$

The maximum throughput rate for each of these combinations is again different. The maximum throughput rate is the sum of the sample and hold acquisition time and A/D conversion time as shown in Figure 9.

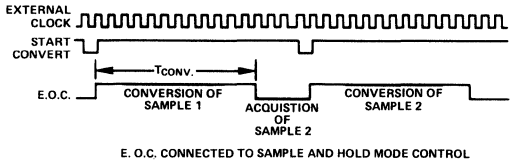


Figure 9. START/E.O.C. Timing for Sampled Data System

When using an AD346 with an AD5212 the throughput rate is, 2.0μs acquisition time plus 13μs conversion time, 66.6kHz. The ADSHC-85 used in combination with an AD5202 is, 4.5μs acquisition time plus 50μs conversion time, 18.3kHz. To meet the requirements of the Nyquist sampling criteria, the AD346 and AD5210 combination can be used for input frequencies from dc through 33.3kHz; the ADSHC-85 and AD5210 combination for inputs from dc through 9.2kHz. Input frequencies higher than these (up to the maximum frequency) would result in "under-sampling" of the input signal. Signals up to the maximum frequency could be processed if their bandwidth is less than one-half the sample frequency.

A fast (32kHz) 12-bit DAS can be configured using the AD1362 and the AD521X. The AD1362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD1362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

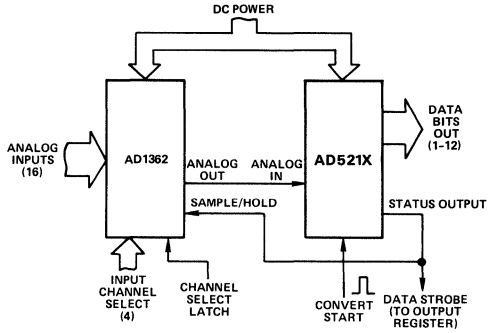


Figure 10. High Speed 12-Bit DAS

CONVERT START USING A POSITIVE EDGE

In some systems it may be inconvenient to generate a negative going start convert pulse of the proper width. The circuit of Figure 11 can be used to start a conversion on the AD521X series of A/Ds with a positive going edge. To perform a conversion both the convert start signal and the E.O.C. must be low. The output of the inverter and nand gate will then be in the high state. The converter will reset on the next rising clock edge. Resetting brings the E.O.C. to a high state; the inverter goes low; the convert start is still high so the output of the nand gate goes high allowing the conversion to continue immediately. The convert start line has only to be brought back down before the conversion is complete.

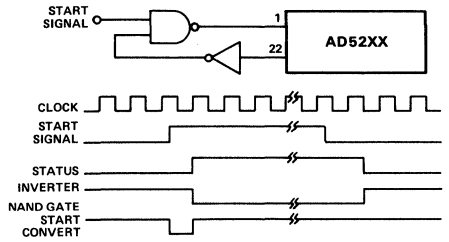


Figure 11. Convert Start Using a Positive Edge

Input Range	Speed	Internal Reference	External Reference
-5V to +5V	50μs	AD5201	AD5204
	13μs	AD5211	AD5214
-10V to +10V	50μs	AD5202	AD5205
	13μs	AD5212	AD5215

i.e., – the 13μs conversion time, ±10V input, external reference, extended temperature unit is the AD5215TD.

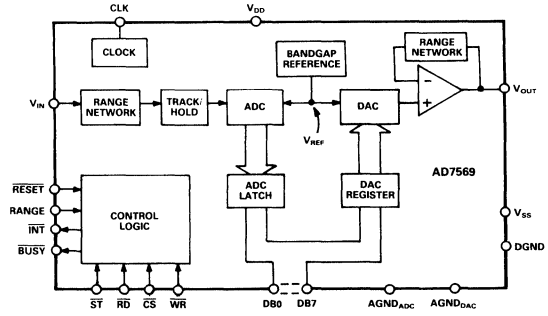
Table II.

LC²MOS
Complete, 8-Bit Analog I/O System

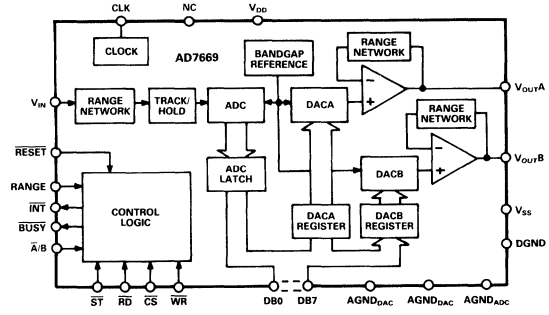
AD7569/AD7669

FEATURES
2μs ADC with Track/Hold
1μs DAC with Output Amplifier
AD7569, Single DAC Output
AD7669, Dual DAC Output
On-Chip Bandgap Reference
Fast Bus Interface
Single or Dual 5V Supplies

AD7569 FUNCTIONAL BLOCK DIAGRAM



AD7669 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7569/AD7669 is a complete, 8-bit, analog I/O system on a single monolithic chip. The AD7569 contains a high speed successive approximation ADC with 2μs conversion time, a track/hold with 200kHz bandwidth, a DAC and output buffer amplifier with 1μs settling time. A temperature-compensated 1.25V bandgap reference provides a precision reference voltage for the ADC and the DAC. The AD7669 is similar but contains two DACs with output buffer amplifiers.

A choice of analog input/output ranges is available. Using a supply voltage of +5V, input and output ranges of zero to 1.25V and zero to 2.5 volts may be programmed using the RANGE input pin. Using a ±5V supply, bipolar ranges of ±1.25V or ±2.5V may be programmed.

Digital interfacing is via an 8-bit I/O port and standard microprocessor control lines. Bus interface timing is extremely fast, allowing easy connection to all popular 8-bit microprocessors. A separate start convert line controls the track/hold and ADC to give precise control of the sampling period.

The AD7569/AD7669 is fabricated in Linear-Compatible CMOS (LC^2MOS), an advanced, mixed technology process combining precision bipolar circuits with low power CMOS logic. The AD7569 is packaged in a 24-pin, 0.3" wide "skinny" DIP and in 28-terminal PLCC and LCCC packages. The AD7669 is available in a 28-pin, 0.6" plastic DIP and 28-terminal PLCC package.

PRODUCT HIGHLIGHTS

1. Complete Analog I/O on a Single Chip.
   The AD7569/AD7669 provides everything necessary to interface a microprocessor to the analog world. No external components or user trims are required, and the overall accuracy of the system is tightly specified, eliminating the need to calculate error budgets from individual component specifications.
2. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications the AD7569/AD7669 is specified for AC parameters, including signal-to-noise ratio, distortion and input bandwidth.
3. Fast Microprocessor Interface.
   The AD7569/AD7669 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 75ns and Write pulse width less than 80ns.

DAC SPECIFICATIONS[1]

(V_{DD} = +5V ±5%; V_{SS}[2] = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0V; R_L = 2kΩ, C_L = 100pF to $AGND_{DAC}$ unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	AD7569 J, A Versions[3] AD7669 J Version	AD7569 K, B Versions	AD7569 S Version	AD7569 T Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution[4]	8	8	8	8	Bits	
Total Unadjusted Error[5]	±2	±2	±3	±3	LSB typ	
Relative Accuracy[5]	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity[5]	±1	±3/4	±1	±3/4	LSB max	Guaranteed Monotonic
Unipolar Offset Error						DAC data is all 0s; V_{SS} = 0V
@ 25°C	±2	±1.5	±2	±1.5	LSB max	Typical tempco is 10μV/°C for +1.25V range
T_{min} to T_{max}	±2.5	±2	±2.5	±2	LSB max	
Bipolar Zero Offset Error						DAC data is all 0s; V_{SS} = −5V
@ 25°C	±2	±1.5	±2	±1.5	LSB max	Typical tempco is 20μV/°C for ±1.25V range
T_{min} to T_{max}	±2.5	±2	±2.5	±2	LSB max	
Full-Scale Error[6] (AD7569 Only)						V_{DD} = 5V
@ 25°C	±2	±1	±2	±1	LSB max	
T_{min} to T_{max}	±3	±2	±4	±3	LSB max	
Full-Scale Error[6] (AD7669 Only)						V_{DD} = 5V
@ 25°C	±3				LSB max	
T_{min} to T_{max}	±4.5				LSB max	
DACA/DACB Full Scale Error Match[6] (AD7669 Only)	±2.5				LSB max	V_{DD} = 5V
ΔFull Scale/ΔV_{DD}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{OUT} = 2.5V; ΔV_{DD} = ±5%
ΔFull Scale/ΔV_{SS}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{OUT} = −2.5V; ΔV_{SS} = ±5%
Load Regulation at Full Scale	0.2	0.2	0.2	0.2	LSB max	R_L = 2kΩ to 0/C
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio[5] (SNR)	44	46	44	46	dB min	V_{OUT} = 20kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz
Total Harmonic Distortion[5] (THD)	48	48	48	48	dB max	V_{OUT} = 20kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz
Intermodulation Distortion[5] (IMD)	55	55	55	55	dB typ	fa = 18.4kHz, fb = 14.5kHz with $f_{SAMPLING}$ = 400kHz
ANALOG OUTPUT						
Output Voltage Ranges						
Unipolar	0 to +1.25/2.5				Volts	V_{DD} = +5V, V_{SS} = 0V
Bipolar	±1.25/±2.5				Volts	V_{DD} = +5V, V_{SS} = −5V
LOGIC INPUTS						
$\overline{CS}$, A/B, $\overline{WR}$, RANGE, $\overline{RESET}$, DB0 – DB7						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Leakage Current	10	10	10	10	μA max	V_{IN} = 0 to V_{DD}
Input Capacitance[7]	10	10	10	10	pF max	
DB0 – DB7						
Input Coding (Single Supply)			Binary			
Input Coding (Dual Supply)			2s Complement			
AC CHARACTERISTICS[7]						
Voltage Output Settling Time						Settling time to within ±1/2LSB of final value
Positive Full-Scale Change	2	2	2	2	μs max	Typically 1μs
Negative Full-Scale Change (Single Supply)	4	4	4	4	μs max	Typically 2μs
Negative Full-Scale Change (Dual Supply)	2	2	2	2	μs max	Typically 1μs
Digital-to-Analog Glitch Impulse[5]	15	15	15	15	nV secs typ	
Digital Feedthrough[5]	1	1	1	1	nV secs typ	
V_{IN} to V_{OUT} Isolation	60	60	60	60	dB typ	V_{IN} = ±2.5V, 50kHz Sine Wave
DAC to DAC Crosstalk[5] (AD7669 Only)	1				nV secs typ	
DACA to DACB Isolation[5] (AD7669 Only)	−70				dB max	
POWER REQUIREMENTS						
V_{DD} Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	Vmin/Vmax	For Specified Performance
V_{SS} Range (Dual Supplies)	−4.75/−5.25	−4.75/−5.25	−4.75/−5.25	−4.75/−5.25	Vmin/Vmax	Specified Performance also applies to V_{SS} = 0V for unipolar ranges.
I_{DD}						V_{OUT} = V_{IN} = 2.5V; Logic Inputs = 2.4V; CLK = 0.8V
(AD7569)	13	13	13	13	mA max	Output unloaded
(AD7669)	18				mA max	Outputs unloaded
I_{SS} (Dual Supplies)						V_{OUT} = V_{IN} = −2.5V; Logic Inputs = 2.4V; CLK = 0.8V
(AD7569)	4	4	4	4	mA max	Output unloaded
(AD7669)	6				mA max	Outputs unloaded
DAC/ADC MATCHING						
Gain Matching[6]						V_{IN} to V_{OUT} match with V_{IN} = ±2.5V,
@25°C	1	1	1	1	% typ	20kHz sine wave
T_{min} to T_{max}	1	1	1	1	% typ	

NOTES

[1]Specifications apply to both DACs in the AD7669. V_{OUT} applies to both $V_{OUT}A$ and $V_{OUT}B$ of the AD7669.

[2]Except where noted, specifications apply for all output ranges including bipolar ranges with dual supply operation.

[3]Temperature ranges are as follows: J, K versions; 0 to +70°C
A, B versions; −25°C to +85°C
S, T versions; −55°C to +125°C

[4]1LSB = 4.88mV for 0 to +1.25V output range, 9.76mV for 0 to +2.5V and ±1.25V ranges and 19.5mV for ±2.5V range.

[5]See Terminology.

[6]Includes internal voltage reference error and is calculated after offset error has been adjusted out. Ideal unipolar full-scale voltage is (FS – 1LSB); ideal bipolar positive full-scale voltage is (FS/2 – 1LSB) and ideal bipolar negative full-scale voltage is −FS/2.

[7]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

ADC SPECIFICATIONS

(V_{DD} = +5V ±5%; V_{SS}[1] = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0V; f_{CLK} = 5MHz external unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated.)

Specifications apply to Mode 1 interface.

Parameter	AD7569 J, A Versions[2] AD7669 J Version	AD7569 K, B Versions	AD7569 S Version	AD7569 T Version	Units	Conditions/Comments
DC ACCURACY						
Resolution[3]	8	8	8	8	Bits	
Total Unadjusted Error[4]	±3	±3	±4	±4	LSB typ	
Relative Accuracy[4]	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity[4]	±1	±3/4	±1	±3/4	LSB max	No Missing Codes
Unipolar Offset Error						Typical tempco is 10μV/°C for +1.25V range; V_{SS} = 0V
@25°C	±2	±1.5	±2	±1.5	LSB max	
T_{min} to T_{max}	±3	±2.5	±3	±2.5	LSB max	
Bipolar Zero Offset Error						Typical tempco is 20μV/°C for ±1.25V range; V_{SS} = −5V
@25°C	±3	±2.5	±3	±2.5	LSB max	
T_{min} to T_{max}	±3.5	±3	±4	±3.5	LSB max	
Full-Scale Error[5]						V_{DD} = 5V
@25°C	−4, +0	−4, +0	−4, +0	−4, +0	LSB max	
T_{min} to T_{max}	−5.5, +1.5	−5.5, +1.5	−7.5, +2	−7.5, +2	LSB max	
ΔFull Scale/ΔV_{DD}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{IN} = +2.5V; ΔV_{DD} = ±5%
ΔFull Scale/ΔV_{SS}, T_A = 25°C	0.5	0.5	0.5	0.5	LSB max	V_{IN} = −2.5V; ΔV_{SS} = ±5%
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio[4] (SNR)	44	46	44	45	dB min	V_{IN} = 100kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz[6]
Total Harmonic Distortion[4] (THD)	48	48	48	48	dB max	V_{IN} = 100kHz full-scale sine wave with $f_{SAMPLING}$ = 400kHz[6]
Intermodulation Distortion[4] (IMD)	60	60	60	60	dB typ	fa = 99kHz, fb = 96.7kHz with $f_{SAMPLING}$ = 400kHz
Frequency Response	0.1	0.1	0.1	0.1	dB typ	V_{IN} = ±2.5V, dc to 200kHz sine wave
Track/Hold Acquisition Time[7]	200	200	300	300	ns typ	
ANALOG INPUT						
Input Voltage Ranges						
Unipolar	0 to +1.25/+2.5				Volts	V_{DD} = +5V; V_{SS} = 0V
Bipolar	±1.25/±2.5				Volts	V_{DD} = +5V; V_{SS} = −5V
Input Current	±300	±300	±300	±300	μA max	See equivalent circuit Fig. 5
Input Capacitance	10	10	10	10	pF typ	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, $\overline{ST}$, CLK, $\overline{RESET}$, RANGE						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Capacitance[8]	10	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$, $\overline{ST}$, RANGE, $\overline{RESET}$						
Input Leakage Current	10	10	10	10	μA max	V_{IN} = 0 to V_{DD}
CLK						
Input Current						
I_{INL}	−1.6	−1.6	−1.6	−1.6	mA max	V_{IN} = 0V
I_{INH}	40	40	40	40	μA max	V_{IN} = V_{DD}
LOGIC OUTPUTS						
DB0 – DB7, $\overline{INT}$, $\overline{BUSY}$						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 200μA
DB0 – DB7						
Floating State Leakage Current	10	10	10	10	μA max	
Floating State Output Capacitance[8]	10	10	10	10	pF max	
Output Coding (Single Supply)		Binary				
Output Coding (Dual Supply)		2s Complement				
CONVERSION TIME						
With External Clock	2	2	2	2	μs max	f_{CLK} = 5MHz
With Internal Clock, T_A = 25°C	1.6	1.6	1.6	1.6	μs min	Using recommended clock components shown in Figure 21. Clock frequency can be adjusted by varying R_{CLK}.
	2.6	2.6	2.6	2.6	μs max	
POWER REQUIREMENTS	As per DAC Specifications					

NOTES

[1]Except where noted, specifications apply for all ranges including bipolar ranges with dual supply operation.

[2]Temperature ranges are as follows: J, K versions; 0 to +70°C
A, B versions; −25°C to +85°C
S, T versions; −55°C to +125°C

[3]1LSB = 4.88mV for 0 to +1.25V range, 9.76mV for 0 to +2.5V and ±1.25V ranges and 19.5mV for ±2.5V range.

[4]See Terminology.

[5]Includes internal voltage reference error and is calculated after offset error has been adjusted out. Ideal unipolar last code transition occurs at (FS – 3/2LSB); Ideal bipolar last code transition occurs at (FS/2 – 3/2LSB).

[6]Exact frequencies are 101kHz and 384kHz to avoid harmonics coinciding with sampling frequency.

[7]Rising edge of $\overline{BUSY}$ to falling edge of $\overline{ST}$. The time given refers to the acquisition time which gives a 3dB degradation in SNR from the tested figure.

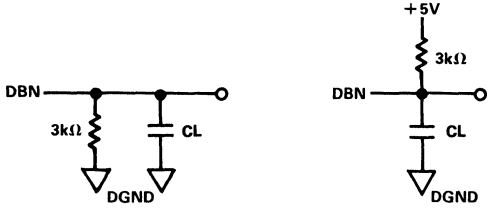
[8]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (See Figures 8, 10, 12; V_{DD} = 5V ±5%; V_{SS} = 0V or −5V ±5%)

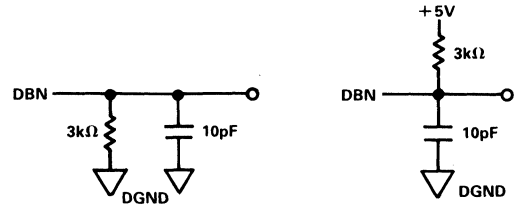
Parameter	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S, T Grades)	Units	Test Conditions/Comments
DAC Timing					
t_1	80	80	90	ns min	$\overline{WR}$ Pulse Width
t_2	0	0	0	ns min	$\overline{CS}$, A/B to $\overline{WR}$ Setup Time
t_3	0	0	0	ns min	$\overline{CS}$, A/B to $\overline{WR}$ Hold Time
t_4	60	70	80	ns min	Data Valid to $\overline{WR}$ Setup Time
t_5	10	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
ADC Timing					
t_6	50	50	50	ns min	$\overline{ST}$ Pulse Width
t_7	110	130	150	ns max	$\overline{ST}$ to $\overline{BUSY}$ Delay
t_8	20	30	30	ns max	$\overline{BUSY}$ to $\overline{INT}$ Delay
t_9	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{11}	60	75	90	ns min	$\overline{RD}$ Pulse Width. Determined by t_{13}.
t_{12}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{13}[2]	60	75	90	ns max	Data Access Time after $\overline{RD}$; C_L = 20pF
	95	120	135	ns max	Data Access Time after $\overline{RD}$; C_L = 100pF
t_{14}[3]	10	10	10	ns min	Bus Relinquish Time after $\overline{RD}$
	60	75	85	ns max	
t_{15}	65	75	85	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{16}	120	140	160	ns max	$\overline{RD}$ to $\overline{BUSY}$ Delay
t_{17}[2]	60	75	90	ns max	Data Valid Time after $\overline{BUSY}$; C_L = 20pF
	90	115	135	ns max	Data Valid Time after $\overline{BUSY}$; C_L = 100pF

NOTES
[1]Sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_{13} and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross either 0.8V or 2.4V.
[3]t_{14} is defined as the time required for the data line to change 0.5V when loaded with the circuit of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Bus Relinquish Time Test

ABSOLUTE MAXIMUM RATINGS

V_{DD} to $AGND_{DAC}$ or $AGND_{ADC}$ . . . . . −0.3V, +7V
V_{DD} to DGND . . . . . −0.3V, +7V
V_{DD} to V_{SS} . . . . . −0.3V, +14V
$AGND_{DAC}$ or $AGND_{ADC}$ to DGND . . −0.3V, V_{DD} +0.3V
$AGND_{DAC}$ to $AGND_{ADC}$ . . . . . ±5V
Logic Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{OUT} (V_{OUT}A, V_{OUT}B) to
$AGND^1_{DAC}$ . . . . . V_{SS} −0.3V, V_{DD}+0.3V
V_{IN} to $AGND_{ADC}$ . . . . . V_{SS} −0.3V, V_{DD} +0.3V

NOTE
[1]Output may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to AGND or V_{SS} is 50mA.

Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial (J, K) . . . . . 0 to +70°C
Industrial (A, B) . . . . . −25°C to +85°C
Extended (S, T) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 Secs) . . . . . +300°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

NOTE:
The term DAC (Digital-to-Analog Converter) throughout the data sheet applies equally to the dual DACs in the AD7669 as well as to the single DAC of the AD7569 unless otherwise stated. It follows that the term V_{OUT} applies to both $V_{OUT}A$ and $V_{OUT}B$ of the AD7669 also.

TERMINOLOGY

Total Unadjusted Error
Total unadjusted error is a comprehensive specification which includes internal voltage reference error, relative accuracy, gain and offset errors.

Relative Accuracy (DAC)
Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after allowing for offset and gain errors. For the bipolar output ranges the endpoints of the DAC transfer function are defined as those voltages which correspond to negative full-scale and positive full-scale codes. For the unipolar output ranges the endpoints are code 1 and code 255. Code 1 is chosen because the amplifier is now working in single supply and in cases where the true offset of the amplifier is negative it cannot be seen at code 0. If the relative accuracy was calculated between code 0 and code 255 the "negative offset" would appear as a linearity error. If the offset is negative and less than 1LSB, it will appear at code 1, and hence the true linearity of the converter is seen between code 1 and code 255.

Relative Accuracy (ADC)
Relative Accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function. For the bipolar input ranges these points are the measured negative full-scale transition point and the measured positive full-scale transition point. For the unipolar ranges the straight line is drawn between the measured first LSB transition point and the measured full-scale transition point.

Differential Nonlinearity
Differential Nonlinearity is the difference between the measured change and an ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1LSB max ensures monotonicity (DAC) or no missed codes (ADC). A differential nonlinearity of ± 3/4LSB max ensures that the minimum step size (DAC) or code width (ADC) is 1/4LSB and the maximum step size or code width is 3/4LSB.

Digital-to-Analog Glitch Impluse
Digital-to-Analog Glitch Impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected. It is normally specified as the area of the glitch in nVsecs and is measured when the digital input code is changed by 1LSB at the major carry transition.

Digital Feedthrough
Digital Feedthrough is also a measure of the impulse injected to the analog output from the digital inputs but is measured when the DAC is not selected. It is essentially feedthrough across the die and package. It is also a measure of the glitch impulse transferred to the analog output when data is read from the internal ADC. It is specified in nVsecs and is measured with $\overline{WR}$ high and a digital code change from all 0s to all 1s.

DAC-to-DAC Crosstalk (AD7669 Only)
The glitch energy transferred to the output of one DAC due to an update at the output of the second DAC. The figure given is the worst case and is expressed in nV secs. It is measured with an update voltage of full scale.

DAC-to-DAC Isolation (AD7669 Only)
DAC-to-DAC Isolation is the proportion of a digitized sine wave from the output of one DAC which appears at the output of the second DAC (loaded with all 1s). The figure given is the worst case for the second DAC output and is expressed as a ratio in dBs. It is measured with a digitized sine wave ($f_{SAMPLING}$ = 100kHz) of 20kHz at 2.5V pk-pk.

Signal-to-Noise Ratio
Signal-to-Noise Ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals (excluding dc) up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for an ideal 8-bit converter, SNR = 50dB.

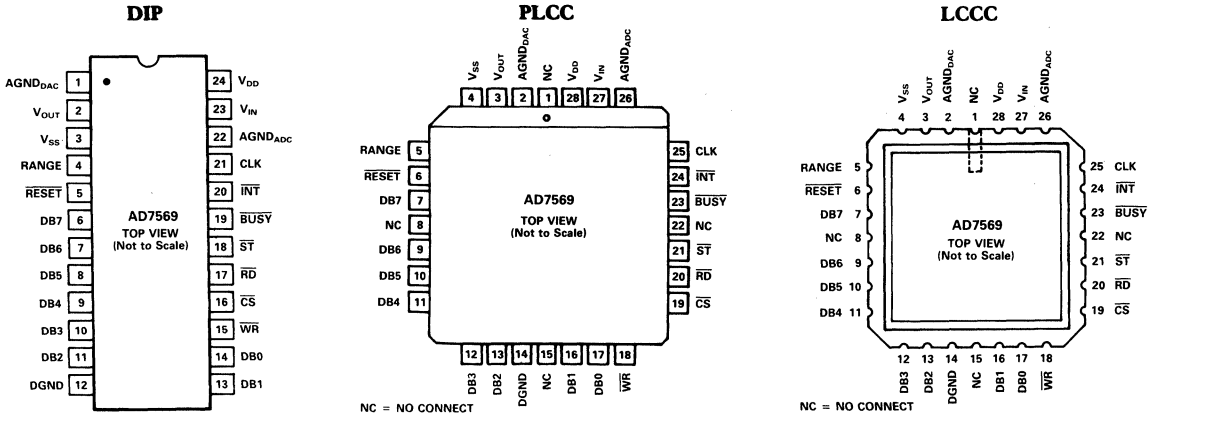
Harmonic Distortion
Harmonic Distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7569/AD7669, Total Harmonic Distortion (THD) is defined as

$$20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

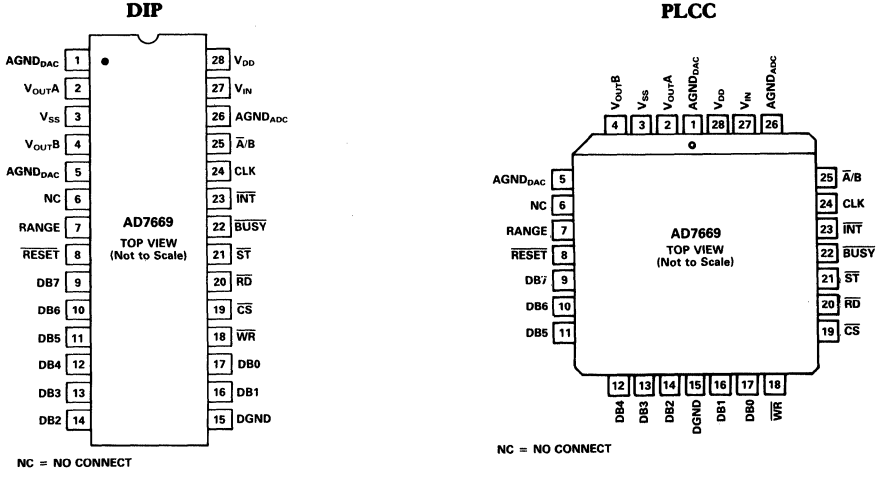
where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m,n = 0, 1, 2, 3,.... . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (fa + fb) and (fa − fb) and the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

AD7569 PIN CONFIGURATIONS



AD7669 PIN CONFIGURATIONS



AD7569 ORDERING INFORMATION[1]

Relative Accuracy (LSB) T_{min}–T_{max}	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-24)	**Hermetic DIP (Q-24)**	**Hermetic DIP (Q-24)**
±1	AD7569JN	AD7569AQ	AD7569SQ
±1/2	AD7569KN	AD7569BQ	AD7569TQ
	PLCC (P-28A)[3]		**LCCC (E-28A)[4]**
±1	AD7569JP		AD7569SE
±1/2	AD7569KP		AD7569TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to S or T grade part number.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

AD7669 ORDERING INFORMATION[1]

Relative Accuracy (LSB) T_{min}–T_{max}	Temperature Range and Package Options[2] 0 to +70°C
	Plastic DIP (N-28)
±1	AD7669JN
	PLCC (P-28A)[2]
±1	AD7669JP

NOTE
[1]PLCC: Plastic Leaded Chip Carrier.
[2]See Section 14 for package outline information.

PIN FUNCTION DESCRIPTION

(Applies to the AD7569 and AD7669 unless otherwise stated.)

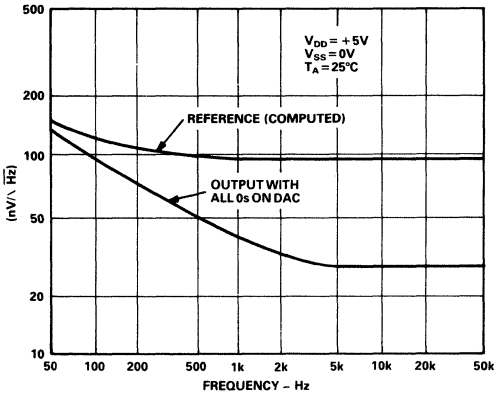
Pin Mnemonic	Description
$AGND_{DAC}$	Analog Ground for the DAC(s). Separate ground return paths are provided for the DAC(s) and ADC to minimize crosstalk.
V_{OUT} ($V_{OUT}A$, $V_{OUT}B$)	Output Voltage. V_{OUT} is the buffered output voltage from the AD7569 DAC. $V_{OUT}A$ and $V_{OUT}B$ are the buffered DAC output voltages from the AD7669. Four different output voltage ranges can be achieved (see Table I).
V_{SS}	Negative Supply Voltage ($-5V$ for dual supply or 0V for single supply). This pin is also used with the RANGE pin to select the different input/output ranges and changes the data format from binary ($V_{SS}=0V$) to 2s complement ($V_{SS}=-5V$) (see Table I).
RANGE	Range Selection Input. This is used with the V_{SS} input to select the different ranges as per Table I. The range selected applies to both the analog input voltage of the ADC and the output voltage from the DAC(s).
$\overline{RESET}$	Reset Input (Active Low). This is an asynchronous system reset which clears the DAC register(s) to all 0s and clears the $\overline{INT}$ line of the ADC (i.e., makes the ADC ready for new conversion). In unipolar operation this input sets the output voltage to 0V; in bipolar operation it sets the output to negative full scale.
DB7	Data Bit 7. Most Significant Bit (MSB).
DB6–DB2	Data Bit 6 to Data Bit 2.
DGND	Digital Ground.
DB1	Data Bit 1.
DB0	Data Bit 0. Least Significant Bit (LSB).
$\overline{WR}$	Write Input (Edge triggered). This is used in conjunction with $\overline{CS}$ to write data into the AD7569 DAC register. It is used in conjunction with $\overline{CS}$ and $\overline{A}$/B to write data into the selected DAC register of the AD7669. Data is transferred on the rising edge of $\overline{WR}$.

Pin Mnemonic	Description
$\overline{CS}$	Chip Select Input (Active Low). The device is selected when this input is active.
$\overline{RD}$	READ Input (Active Low). This input must be active to access data from the part. In the Mode 2 interface, $\overline{RD}$ going low starts conversion. It is used in conjunction with the $\overline{CS}$ input (see Digital Interface Section).
$\overline{ST}$	Start Conversion (Edge triggered). This is used when precise sampling is required. The falling edge of $\overline{ST}$ starts conversion and drives $\overline{BUSY}$ low. The $\overline{ST}$ signal is not gated with $\overline{CS}$.
$\overline{BUSY}$	BUSY Status Output (Active Low). When this pin is active the ADC is performing a conversion. The input signal is held prior to the falling edge of $\overline{BUSY}$ (see Digital Interface Section).
$\overline{INT}$	INTERRUPT Output (Active Low). $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ goes high on the rising edge of $\overline{CS}$ or $\overline{RD}$ and is also set high by a low pulse on $\overline{RESET}$ (see Digital Interface Section).
$\overline{A}$/B (AD7669 Only)	DAC Select Input. This input selects which DAC register data is written to under control of $\overline{CS}$ and $\overline{WR}$. With this input low data is written to the DACA register; with this input high data is written to the DACB register.
CLK	A TTL compatible clock signal may be used to determine the ADC conversion time. Internal clock operation is achieved by connecting a resistor and capacitor to ground.
$AGND_{ADC}$	Analog Ground for the ADC.
V_{IN}	Analog Input. Various input ranges can be selected (see Table I).
V_{DD}	Positive Supply Voltage ($+5V$).

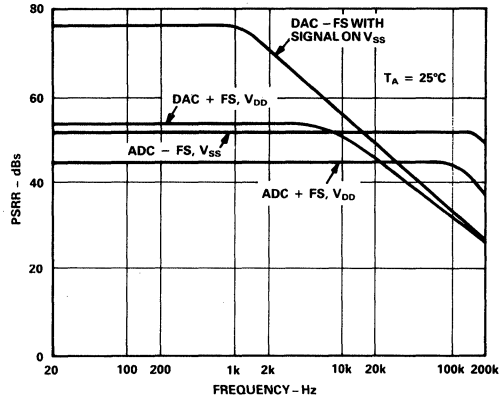
Range	V_{SS}	Input/Output Voltage Range	DB0–DB7 Data Format
0	0V	0 to +1.25V	Binary
1	0V	0 to +2.5V	Binary
0	−5V	±1.25V	2s Complement
1	−5V	±2.5V	2s Complement

Table I. Input/Output Ranges

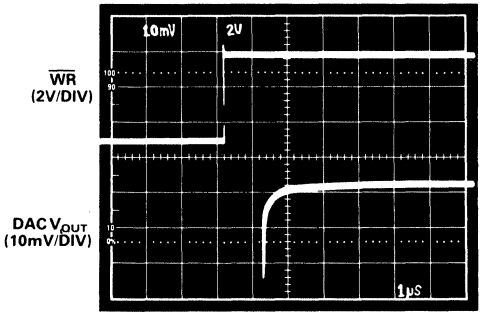
Typical Performance Graphs



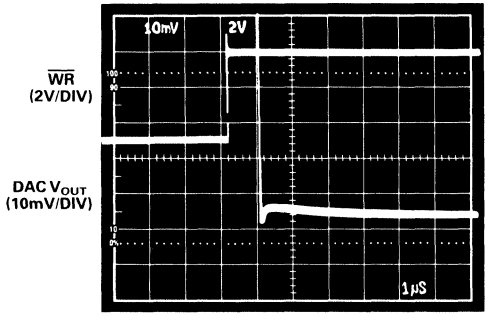
Noise Spectral Density vs. Frequency



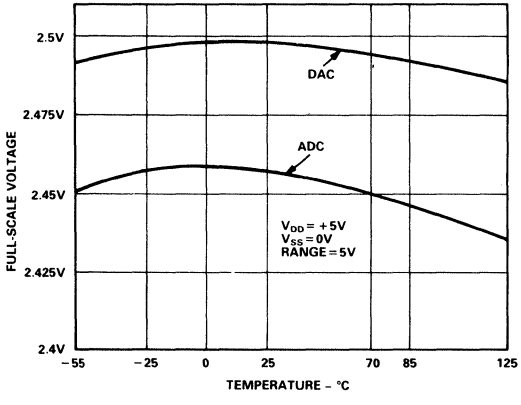
Power Supply Rejection Ratio vs. Frequency



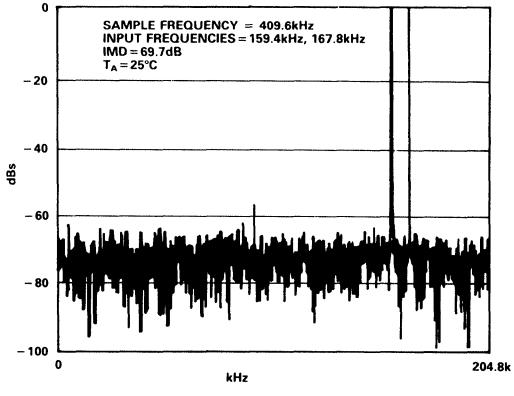
Positive-Going Settling Time (±2.5V Range)



Negative-Going Settling Time (±2.5V Range)



DAC/ADC Full-Scale Temperature Coefficient



IMD Plot for ADC

CIRCUIT DESCRIPTION

D/A SECTION

The AD7569 contains an 8-bit, voltage-mode, D/A converter which uses eight equally weighted current sources switched into an R-2R ladder network to give a direct but unbuffered 0 to +1.25V output range. The AD7669 is similar but contains two D/A converters. The current sources are fabricated using PNP transistors. These transistors allow current sources which are driven from positive voltage logic and give a zero-based output range. The output voltage from the voltage switching R-2R ladder network has the same positive polarity as the reference and therefore the D/A converter can be operated from a single power supply rail.

The PNP current sources are generated using the on-chip bandgap reference and a control amplifier. The current sources are switched to either the ladder or $AGND_{DAC}$ by high speed p-channel switches. These high-speed switches ensure a fast settling time for the output voltage of the DAC. The R-2R ladder network of the DAC consists of highly stable, thin-film resistors. A simplified circuit diagram for the D/A converter section is shown in Figure 3. An identical D/A converter is used as part of the A/D converter which is discussed later.

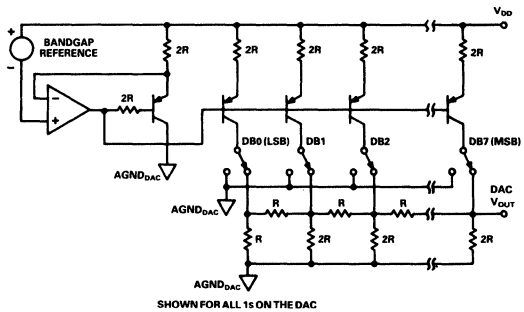


Figure 3. DAC Simplified Circuit Diagram

OP AMP SECTION

The output from the D/A converter is buffered by a high speed, noninverting op amp. This op amp is capable of developing ±2.5V across a 2kΩ and 100pF load to $AGND_{DAC}$. The amplifier can be operated from a single +5V supply to give two unipolar output ranges or from dual supplies (±5V) to allow two bipolar output ranges.

The feedback path of the amplifier contains a gain/offset network which provides four voltage ranges at the output of the op amp. The output voltage range is determined by the RANGE and V_{SS} inputs. (See Table I in the Pin Function Description section.) The four output ranges possible are: 0 to +1.25V, 0 to +2.5V, ±1.25V and ±2.5V. It should be noted that whatever range is selected for the output amplifier also applies to the input voltage range of the A/D converter.

The output amplifier settles to within 1/2LSB of its final value in typically less than 500ns. Operating the part from single or dual supplies has no effect on the positive-going settling time. However, the negative-going output settling time to voltages near 0V in single supply will be slightly longer than the settling time to negative full scale for dual supply operation. Additionally, to ensure that the output voltage can go to 0V in single supply, a transistor on the output acts as a passive pull-down with output voltages near 0V with V_{SS} = 0V. This means that the sink capability of the amplifier is reduced as the output voltage nears 0V in single supply. In dual supply operation the full sink capability of 1.25mA is maintained over the entire output voltage range.

For all other parameters the single and dual supply performances of the amplifier are essentially identical. The output noise from the amplifier with full scale on the DAC is 200μV peak-to-peak. The spot noise at 1kHz is $35nV/\sqrt{Hz}$ with all 0s on the DAC. A noise spectral density versus frequency plot for the amplifier is shown in the typical performance graphs.

VOLTAGE REFERENCE

The AD7569/AD7669 contains an on-chip bandgap reference which provides a low noise, temperature compensated reference voltage for both the DAC and the ADC. The reference is trimmed for both absolute accuracy and temperature coefficient. The bandgap reference is generated with respect to V_{DD}. It is buffered by a separate control amplifier for both the DAC and the ADC reference. This can be seen in the DAC ladder network configuration in Figure 3.

DIGITAL SECTION

The data pins on the AD7569/AD7669 provide a connection between the external bus and both the DAC data inputs and ADC data outputs. The threshold levels of all digital inputs and outputs are compatible with either TTL or 5V CMOS levels. Internal input protection of all digital pins is achieved by on-chip distributed diodes.

The data format is straight binary when the part is used in single supply (V_{SS} = 0V). However, when a V_{SS} of −5V is applied, the data format becomes 2s complement. This data format applies to the digital inputs of the DAC and the digital outputs of the ADC.

ADC SECTION

The analog-to-digital converter on the AD7569/AD7669 uses the successive approximation technique to achieve a fast conversion time of 2μs and provide an 8-bit parallel digital output. The reference for the ADC is provided by the on-chip bandgap reference.

Conversion start is controlled by $\overline{ST}$ or by $\overline{CS}$ and $\overline{RD}$. Once a conversion has been started another conversion start should not be attempted until the conversion in progress is completed. Exercising the $\overline{RESET}$ input does not affect conversion; the $\overline{RESET}$ input resets the $\overline{INT}$ line high which is useful in interrupt-driven systems where a READ has not been performed at the end of the previous conversion. The $\overline{INT}$ line does not have to be cleared at the end of conversion. The ADC will continue to convert correctly but the function of the $\overline{INT}$ line will be affected.

Figure 4 shows the operating waveforms for a conversion cycle. The analog input voltage, V_{IN}, is held 50ns typical after the falling edge of $\overline{ST}$ or ($\overline{CS}$ & $\overline{RD}$). The MSB decision is made approximately 50ns after the second falling edge of the input CLK following a conversion start. If t_1 in Figure 4 is greater than 50ns, then the falling edge of the input CLK will be seen as the first falling clock edge. If t_1 is less than 50ns, the first falling clock edge of the conversion will not occur until one clock cycle later. The succeeding bit decisions are made approximately 50ns after a CLK edge until conversion is complete. At

the end of conversion, the SAR contents are transferred to the output latch and the SAR is reset in readiness for a new conversion. A single conversion lasts for 8 input clock cycles.

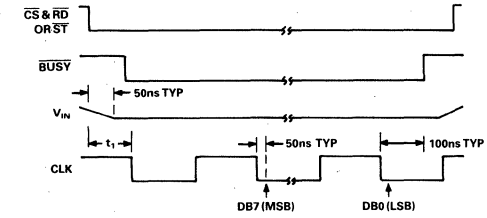
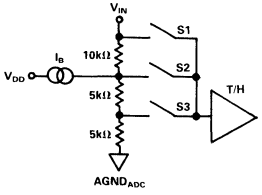


Figure 4. Operating Waveforms Using External Clock

ANALOG INPUT

The analog input of the AD7569/AD7669 feeds into an on-chip track-and-hold amplifier. To accommodate different full-scale ranges, the analog input signal is conditioned by a gain/offset network which conditions all input ranges so that the internal ADC always works with a 0 to +1.25V signal. As a result, the input current on the V_{IN} input varies with the input range selected as shown in Figure 5.



VOLTAGE RANGE	ON SWITCH	I_B
0 TO +1.25V	S1	20μA
0 TO +2.5V	S2	20μA
−1.25V TO +1.25V	S2	140μA
−2.5V TO +2.5V	S3	280μA

Figure 5. Equivalent V_{IN} Circuit

TRACK-AND-HOLD

The track-and-hold (T/H) amplifier on the analog input of the AD7569/AD7669 allows the ADC to accurately convert an input sine wave of 2.5V peak-to-peak amplitude up to a frequency of 200kHz, the Nyquist frequency of the ADC when operated at its maximum throughput rate of 400kHz. This maximum rate of conversion includes conversion time and time between conversions. Because the input bandwidth of the T/H amplifier is much larger than 200kHz, the input signal should be band-limited to avoid converting high-frequency noise components.

The operation of this T/H amplifier is essentially transparent to the user. The T/H amplifier goes from its tracking mode to its hold mode at the start of conversion. This occurs when the ADC receives a conversion start command from either $\overline{ST}$ or $\overline{CS}$ & $\overline{RD}$. At the end of conversion ($\overline{BUSY}$ going high) the T/H reverts back to tracking the input signal.

EXTERNAL CLOCK

The AD7569/AD7669 ADC can be used with its on-chip clock or with an externally applied clock. When using an external clock, the CLK input of the AD7569/AD7669 may be driven directly from 74HC, 4000B series buffers (such as 4049) or from TTL buffers. When conversion is complete, the internal clock is disabled. The external clock can continue to run between conversions without being disabled. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

INTERNAL CLOCK

Clock pulses are generated by the action of an internal current source charging the external capacitor (C_{CLK}) and this external capacitor discharging through the external resistor (R_{CLK}). When a conversion is complete, this internal clock stops operating and the CLK pin goes to the DGND potential. Connections for R_{CLK} and C_{CLK} are shown in the operating diagram of Figure 21. The nominal conversion time versus temperature for the recommended R_{CLK} and C_{CLK} combination is shown in Figure 6. The internal clock provides a convenient clock source for the AD7569/AD7669. Due to process variations, the actual operating frequency for this R_{CLK}/C_{CLK} combination can vary from device to device by up to ±25%.

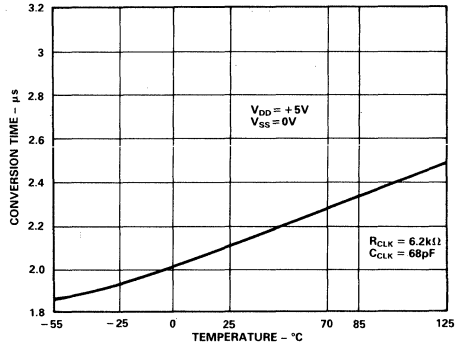


Figure 6. Conversion Time vs. Temperature for Internal Clock Operation

DIGITAL INTERFACE

DAC Timing and Control – AD7569

Table II shows the truth table for DAC operation for the AD7569. The part contains an 8-bit DAC register which is loaded from the data bus under control of $\overline{CS}$ and $\overline{WR}$. The data contained in the DAC register determines the analog output from the DAC. The $\overline{WR}$ input is an edge-triggered input and data is transferred into the DAC register on the rising edge of $\overline{WR}$. Holding $\overline{CS}$ and $\overline{WR}$ low does not make the DAC register transparent.

$\overline{CS}$	$\overline{WR}$	$\overline{RESET}$	DAC Function
H	H	H	DAC Register Unaffected
L	L	H	DAC Register Unaffected
L	↑	H	DAC Register Updated
↑	L	H	DAC Register Updated
X	X	L	DAC Register Loaded with All Zeros

L = Low State H = High State X = Don't Care

Table II. AD7569 DAC Truth Table

The contents of the DAC register are reset to all 0s by an active low pulse on the $\overline{RESET}$ line and for the unipolar output ranges the output remains at 0V after $\overline{RESET}$ returns high. For the bipolar output ranges a low pulse on $\overline{RESET}$ causes the output to go to negative full scale. In unipolar applications the $\overline{RESET}$ line can be used to ensure power-up to 0V on the AD7569 DAC output and is also useful when used as a zero override in system calibration cycles. If the $\overline{RESET}$ input is connected to the system

$\overline{RESET}$ line, then the DAC output resets to 0V when the entire system is reset. Figure 7 shows the input control logic for the AD7569 DAC and the write cycle timing diagram is shown in Figure 8.

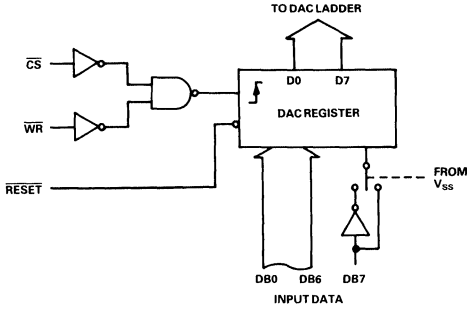


Figure 7. AD7569 DAC Input Control Logic

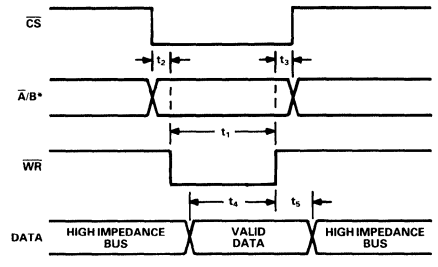


Figure 8. AD7569/AD7669 Write Cycle Timing Diagram

DAC Timing and Control – AD7669

Table III shows the truth table for the dual DAC operation of the AD7669. The part contains two 8-bit DAC registers which are loaded from the data bus under the control of $\overline{CS}$, A/B and $\overline{WR}$. Address line A/B selects which DAC register the data is loaded to. The data contained in the DAC registers determines the analog output from the respective DACs. The $\overline{WR}$ input is an edge-triggered input and data is transferred into the selected DAC register on the rising edge of $\overline{WR}$. Holding $\overline{CS}$ and $\overline{WR}$ low does not make the selected DAC register transparent. The A/B input should not be changed while $\overline{CS}$ and $\overline{WR}$ are low.

$\overline{CS}$	$\overline{WR}$	A/B	$\overline{RESET}$	DAC Function
H	H	X	H	DAC Registers Unaffected
L	↓	L	H	DACA Register Updated
↓	L	L	H	DACA Register Updated
L	↓	H	H	DACB Register Updated
↓	L	H	H	DACB Register Updated
X	X	X	L	DAC Registers Loaded with All Zeros

L = Low State H = High State X = Don't Care

Table III. AD7669 DAC Truth Table

The contents of the DAC registers are reset to all 0s by an active low pulse on the $\overline{RESET}$ line and for the unipolar output ranges the outputs remain at 0V after $\overline{RESET}$ returns high. For the bipolar output ranges a low pulse on $\overline{RESET}$ causes the outputs to go to negative full scale. In unipolar applications the $\overline{RESET}$ line can be used to ensure power-up to 0V on the AD7669 DAC outputs and is also useful when used as a zero override in system calibration cycles. If the $\overline{RESET}$ input is connected to the system $\overline{RESET}$ line, then the DAC outputs reset to 0V when the entire system is reset. Figure 9 shows the DAC input control logic for the AD7669, and the write cycle timing diagram is shown in Figure 8.

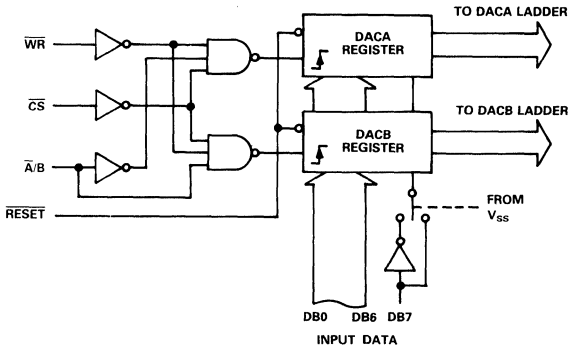


Figure 9. AD7669 DAC Control Logic

ADC Timing and Control

The ADC on the AD7569/AD7669 is capable of two basic operating modes. In the first mode the $\overline{ST}$ line is used to start conversion and drive the track-and-hold into hold mode. At the end of conversion the track-and-hold returns to its tracking mode. The second mode is achieved by hard-wiring the $\overline{ST}$ line high. In this case, $\overline{CS}$ and $\overline{RD}$ start conversion and the microprocessor is driven into a WAIT state for the duration of conversion by $\overline{BUSY}$.

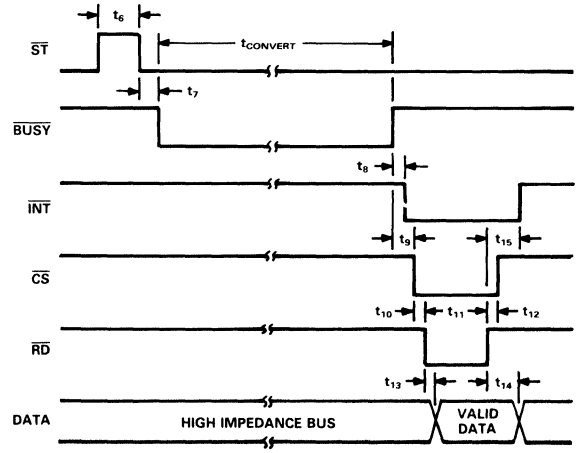


Figure 10. ADC Mode 1 Interface Timing

MODE 1 INTERFACE

The timing diagram for the first mode is shown in Figure 10. It can be used in digital signal processing and other applications where precise sampling in time is required. In these applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases the $\overline{ST}$ line is driven by a timer or some precise clock source.

The falling edge of the $\overline{ST}$ pulse starts conversion and drives the AD7569/AD7669 track-and-hold amplifier into its hold mode. $\overline{BUSY}$ stays low for the duration of conversion and returns high at the end of conversion and the track-and hold amplifier reverts to its tracking mode on this rising edge of $\overline{BUSY}$. The $\overline{INT}$ line can be used to interrupt the microprocessor. A READ to the AD7569/AD7669 address accesses the data and the $\overline{INT}$ line is reset on the rising edge of $\overline{CS}$ or $\overline{RD}$. Alternatively the $\overline{INT}$ can be used to trigger a pulse which drives the $\overline{CS}$ and $\overline{RD}$ and places the data into a FIFO or buffer memory. The microprocessor can then read a batch of data from the FIFO or buffer memory at some convenient time. The $\overline{ST}$ input should not be high when $\overline{RD}$ is brought low otherwise the part will not operate correctly in this mode.

It is important, especially in systems where the conversion start ($\overline{ST}$ pulse) is asynchronous to the microprocessor, that a READ does not occur during a conversion. Trying to read data from the device during a conversion can cause errors to the conversion in progress. Also, pulsing the $\overline{ST}$ line a second time before conversion end should be avoided since it too can cause errors in the conversion result. In applications where precise sampling is not critical the $\overline{ST}$ pulse can be generated from a microprocessor $\overline{WR}$ or $\overline{RD}$ line gated with a decoded address (different to AD7569/AD7669 $\overline{CS}$ address).

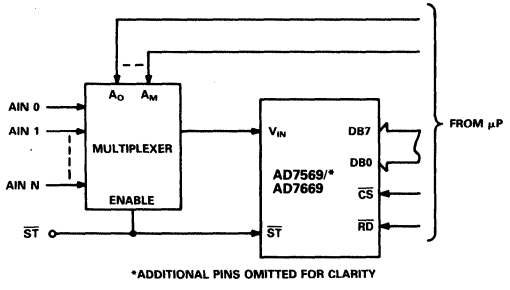


Figure 11. Multichannel Inputs

This interface mode is also useful in applications where a number of input channels are required to be converted by the ADC. Figure 11 shows the circuit configuration for such an application. The signal which drives the $\overline{ST}$ input of the AD7569/AD7669 is also used to drive the ENABLE input of the multiplexer. The multiplexer is enabled on the rising edge of the $\overline{ST}$ pulse while the input signal is held on the falling edge. Therefore, the signal must have settled to within 8 bits over the duration of this $\overline{ST}$ pulse. The settling time, including t_{ON} (ENABLE) of the multiplexer plus the T/H acquisition time (typically 200ns), thus determines the width of the $\overline{ST}$ pulse. This is suited to applications where a number of input channels need to be successively sampled or scanned.

MODE 2 INTERFACE

The second interface mode is intended for use with microprocessors which can be forced into a WAIT state for at least 2µs. The $\overline{ST}$ line of the AD7569/AD7669 must be hard-wired high to achieve this mode. The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7569/AD7669 address, bringing $\overline{CS}$ and $\overline{RD}$ low. $\overline{BUSY}$ subsequently goes low (forcing the microprocessor READY or WAIT input low), placing the microprocessor into a WAIT state. The input signal is held on the falling edge of $\overline{RD}$ (assuming $\overline{CS}$ is already low or is co-incident with $\overline{RD}$). When the conversion is complete ($\overline{BUSY}$ goes high), the processor completes the memory READ and acquires the newly converted data. While conversion is in progress, the ADC places old data (from the previous conversion) on the data bus. The timing diagram for this interface is shown in Figure 12.

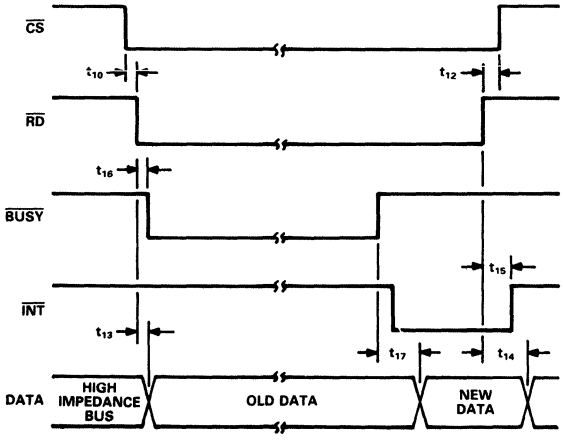


Figure 12. ADC Mode 2 Interface Timing

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then READ data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid reading during conversion. The fast conversion time of the ADC ensures that for many microprocessors, the processor is not placed in a WAIT state for an excessive amount of time.

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (SNR, Harmonic Distortion, Intermodulation Distortion) of both the ADC and DAC are critical. The AD7569/AD7669 is specified dynamically as well as with standard dc specifications. Because the track/hold amplifier has a wide bandwidth, an anti-aliasing filter should be placed on the V_{IN} input to avoid aliasing of high-frequency noise back into the band of interest.

The dynamic performance of the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input which is sampled at a 409.6kHz sampling rate. A Fast Fourier Transform (FFT) plot or Histogram plot is then generated from which SNR, harmonic distortion and dynamic differential nonlinearity data can be obtained. For the DAC, the codes for an ideal sine wave are stored in PROM and loaded down to the DAC. The output spectrum is analyzed, using a spectrum analyzer to evaluate

SNR and harmonic distortion performance. Similarly, for intermodulation distortion, an input (either to V_{IN} or DAC code) consisting of pure sine waves at two frequencies is applied to the AD7569/AD7669.

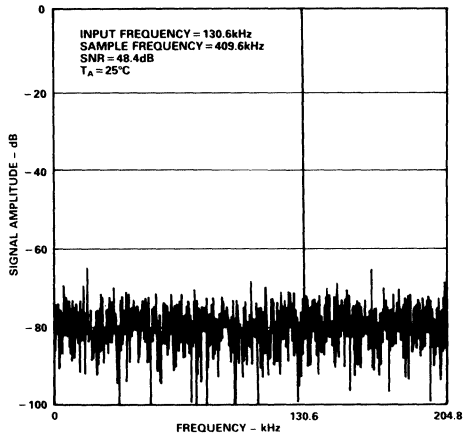


Figure 13. ADC FFT Plot

Figure 13 shows a 2048 point FFT plot of the ADC with an input signal of 130kHz. The SNR is 48.4dB. It can be seen that most of the harmonics are buried in the noise floor. It should be noted that the harmonics are taken into account when calculating the SNR. The relationship between SNR and resolution(N) is expressed by the following equation:

$$SNR = (6.02N + 1.76)dB$$

This is for an ideal part with no differential or integral linearity errors. These errors will cause a degradation in SNR. By working backwards from the above equation, it is possible to get a measure of ADC performance expressed in effective number of bits (N). This effective number of bits is plotted versus frequency in Figure 14. The effective number of bits typically falls between 7.7 and 7.8 corresponding to SNR figures of 48.1 and 48.7dB.

Figure 15 shows a spectrum analyzer plot of the output spectrum from the DAC with an ideal sine-wave table loaded to the data inputs of the DAC. In this case, the SNR is 46dB.

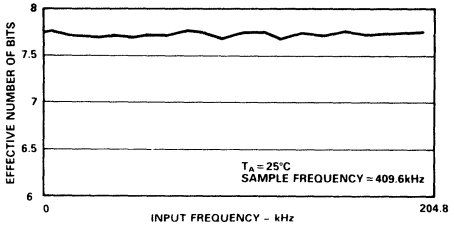


Figure 14. Effective Number of Bits vs. Frequency

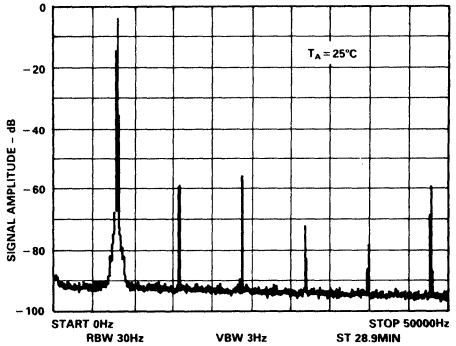


Figure 15. DAC Output Spectrum

HISTOGRAM PLOT

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7569/AD7669 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. If a particular step is wider than the ideal 1LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 16 shows a histogram plot for the ADC indicating very small differential nonlinearity and no missing codes for an input frequency of 204kHz. For a sine-wave input, a perfect ADC would produce a cusp probability density function described by the equation

$$p(V) = \frac{1}{\pi (A^2 - V^2)^{1/2}}$$

where A is the peak amplitude of the sine wave and p(V) the probability of occurrence at a voltage V.

The histogram plot of Figure 16 corresponds very well with this cusp shape.

Further typical plots of the performance of the AD7569/AD7669 are shown in the Typical Performance Graphs section of the data sheet.

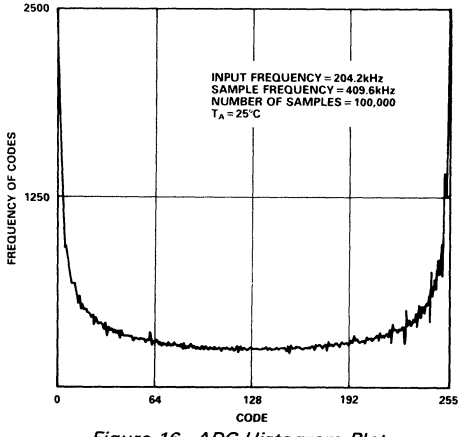


Figure 16. ADC Histogram Plot

INTERFACING THE AD7569/AD7669

AD7569/AD7669 – Z80 INTERFACE

Figure 17 shows a typical interface to the Z80 microprocessor. The ADC is configured for operation in the Mode 1 interface mode. A precise timer or clock source starts conversion in applications requiring equidistant sampling intervals. The scheme used, whereby $\overline{INT}$ of the AD7569/AD7669 generates an interrupt on the Z80, is limited in that it does not allow the ADC to be sampled at the maximum rate. This is because the time between samples has to be long enough to allow the Z80 to service its interrupt and read data from the ADC. To overcome this, some buffer memory or FIFO could be placed between the AD7569/AD7669 and the Z80. Writing data to the relevant AD7569/AD7669 DAC simply consists of a <LD (nn), A> instruction where nn is the decoded address for that DAC. Reading data from the ADC, after an $\overline{INT}$ has been received, consists of a <LDA, (nn)> instruction.

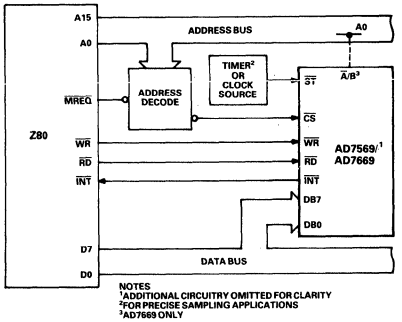


Figure 17. AD7569/AD7669 to Z80 Interface

AD7569/AD7669 – 68008 INTERFACE

A typical interface to the 68008 is shown in Figure 18. In this case the ADC is configured in the Mode 2 interface mode. This means that the one read instruction starts conversion and reads the data. The read cycle is stretched out over the entire conversion period by taking the $\overline{INT}$ line back into the $\overline{DTACK}$ input of the 68008. The additional gates are required so that the 68008 gets a $\overline{DTACK}$ when the processor is writing data to the AD7569/AD7669. In this case there are no wait states introduced into the write cycle. Writing data to the relevant AD7569/AD7669 DAC consists of a <MOVE.B Dn, addr> where Dn is the data register which contains the data to be loaded to that DAC and addr is the decoded address for the DAC. Data is read from the ADC using a <MOVE.B addr,Dn> with the conversion result placed in register Dn.

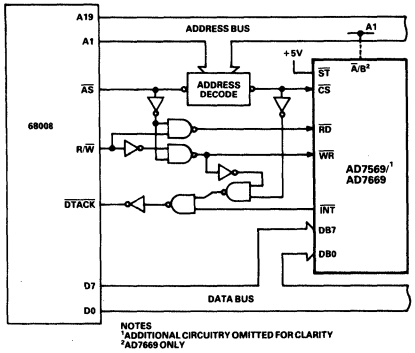


Figure 18. AD7569/AD7669 to 68008 Interface

AD7569/AD7669 – ADSP-2100 INTERFACE

Figure 19 shows a typical interface to the DSP processor, the ADSP-2100. The ADC is in the Mode 2 interface mode which means that the ADSP-2100 is halted during conversion. This is achieved using the decoded address output. This is gated with $\overline{DMWR}$ to ensure that it halts the processor for READ instructions only. $\overline{INT}$ going low at the end of conversion releases the processor and allows it to finish off the READ instruction.

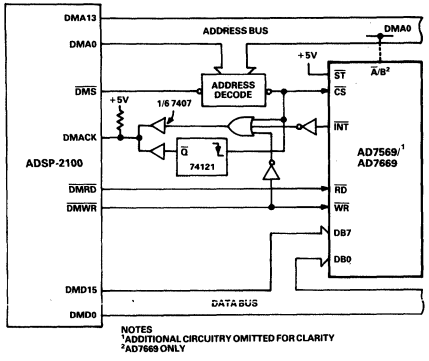


Figure 19. AD7569/AD7669 to ADSP-2100 Interface

Because the instruction cycle of the ADSP-2100 is so fast (125ns cycle) the $\overline{DMWR}$ pulse has to be stretched also for write cycles. This is achieved using the 74121 which generates a pulse which is fed back to DMACK. The duration of this pulse determines how long the ADSP-2100 write cycle is stretched. The buffers which drive the DMACK line must have open-collector outputs. Writing data to the relevant AD7569/AD7669 DAC is achieved using a single instruction, <DM (addr) = MRO> where addr is the decoded address of that DAC and MRO contains the data to be loaded to the DAC register. Data is read from the ADC using a single instruction also, <MRO = DM (addr)>where the conversion result is placed in the MRO data register.

AD7569/AD7669 – IBM PC* INTERFACE

The AD7569/AD7669 is ideal for implementing an analog input/output port for the IBM PC. Figure 20 shows an interface which realizes this function. The ADC is configured in the Mode 1 interface mode and conversions are initiated using a precise clock source for equidistant sampling intervals. At the end of

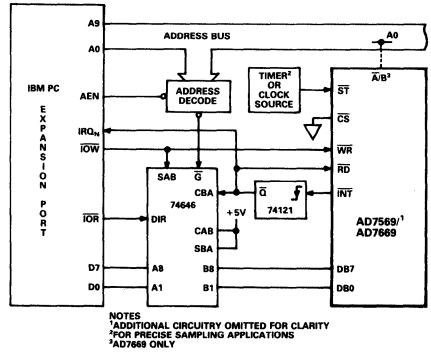


Figure 20. AD7569/AD7669 to IBM PC Interface

***IBM PC is a trademark of International Business Machines Corp.**

conversion the $\overline{INT}$ line goes low, and the 74121 generates a $\overline{RD}$ pulse for the AD7569/AD7669. This $\overline{RD}$ pulse accesses data from the ADC and places the conversion result into a register on the 74646. The rising edge of this pulse generates an interrupt request to the processor. The conversion result is read from the 74646 register by performing an I/0 read to the decoded address of the 74646. Writing data to the relevant AD7569/AD7669 DAC involves an I/0 write to the 74646 which transfers the data to the data inputs of the AD7569/AD7669. Data is latched into the selected DAC register on the rising edge of $\overline{IOW}$.

APPLYING THE AD7569/AD7669 DAC

An internal gain/offset network on the AD7569/AD7669 allows several output voltage ranges. The part can produce unipolar output ranges of 0 to +1.25V or 0 to +2.5V and bipolar output ranges of −1.25V to +1.25V or −2.5V to +2.5V. Connections for these various output ranges are outlined below.

UNIPOLAR (0 to +1.25V) CONFIGURATION

The first of the configurations provides an output voltage range of 0 to +1.25V. This is achieved by tying the V_{SS} and RANGE inputs to $AGND_{DAC}$(=0V). Figure 21 shows the configuration of the AD7569 to achieve this output range. A similar configuration of the AD7669 gives the same output range. The table for output voltage versus the digital code in the DAC register is shown in Table IV.

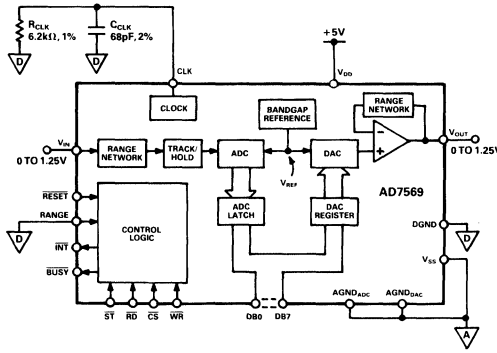


Figure 21. AD7569 Unipolar (0 to +1.25V) Operation

DAC Register Contents MSB LSB	Analog Output, V_{OUT}
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +V_{REF}/2$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

NOTE: 1LSB = $(V_{REF})(2^{-8}) = V_{REF}$ (1/256); V_{REF} = +1.25V Nominal

Table IV. Unipolar (0 to +1.25V) Code Table

UNIPOLAR (0 to +2.5V) CONFIGURATION

The 0 to +2.5V output voltage range is achieved by tying V_{SS} to $AGND_{DAC}$(=0V) and the RANGE input to V_{DD}. The table for output voltage versus digital code is as in Table IV, with $2.V_{REF}$ replacing V_{REF}. Note that for this range

$$1LSB = 2.V_{REF}(2^{-8}) = V_{REF}\frac{1}{128}$$

BIPOLAR (−1.25V to +1.25V) CONFIGURATION

The first of the bipolar configurations is achieved by tying the RANGE input to $AGND_{DAC}$(=0V) and V_{SS} to −5V. The V_{SS} voltage level at which the AD7569/AD7669 changes to bipolar operation is approximately −1V. When the part is configured for bipolar outputs the input coding becomes 2s complement. The table for output voltage versus the digital code in the DAC register is shown in Table V. Note that, as with the unipolar configuration, a digital input code of all 0s produces an output of 0V. It should be noted, however, that a low pulse on the $\overline{RESET}$ line for the bipolar ranges sets the ouput voltage to negative full scale.

DAC Register Contents MSB LSB	Analog Output, V_{OUT}
0111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
0000 0000	0V
1111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
1000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
1000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

NOTE: 1LSB = $(V_{REF})(2^{-7}) = V_{REF}$ (1/128)

Table V. Bipolar (−1.25V to +1.25V) Code Table

BIPOLAR (−2.5V to +2.5V) CONFIGURATION

The −2.5V to +2.5V bipolar output range is achieved by tying the RANGE input to V_{DD} and the V_{SS} input to −5V. Once again, the input coding is 2s complement. The table for output voltage versus digital code is as in Table V with $2.V_{REF}$ replacing V_{REF}. Note that for this range

$$1LSB = 4.V_{REF}(2^{-8}) = V_{REF}\frac{1}{64}$$

APPLYING THE AD7569/AD7669 ADC

The analog input on the AD7569/AD7669 accepts the same four input ranges as the output ranges on the DAC. Whatever output range is selected for the DAC also applies to the input range of the ADC.

Although separate AGNDs exist for both the DAC and ADC to minimize crosstalk, writing data to the DAC while the ADC is performing a conversion may result in an incorrect conversion from the ADC due to an interaction of currents between the DAC and ADC. Therefore, to ensure correct operation of the ADC, the DAC register should not be updated while the ADC is converting.

UNIPOLAR OPERATION

The circuit of Figure 21 shows the AD7569 configured for both an input and output range of 0 to +1.25V (the AD7669 configuration is similar). The nominal transfer characteristic for this range is shown in Figure 22. The output code is Natural Binary with 1LSB = (1.25/256)V = 4.88mV.

As before, to achieve the unipolar 0 to +2.5V input range V_{SS} is connected to 0V and the RANGE input is tied to a logic high. The nominal transfer characteristic is as in Figure 22 but in this case 1LSB = (2.5/256)V = 9.76mV.

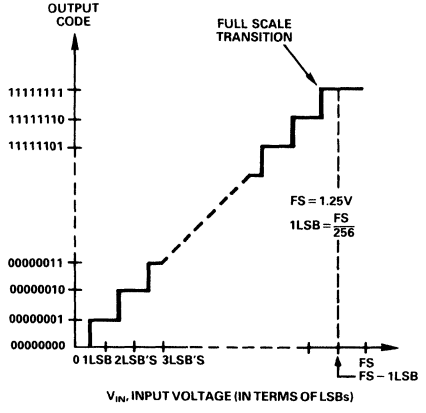


Figure 22. Nominal Transfer Characteristic for Unipolar (0 to +1.25V) Operation

BIPOLAR OPERATION

The analog input of the AD7569/AD7669 ADC is configured for bipolar inputs when V_{SS} = −5V. The output code provided by the part is 2s complement. Figure 23 shows the transfer function for bipolar (−1.25V to +1.25V) operation. The LSB size for this range is (2.5/256)V = 9.76mV.

The transfer function for the −2.5V to +2.5V range is identical to that of Figure 23 but now FS = 5V and the LSB size is (5/256)V = 19.5mV.

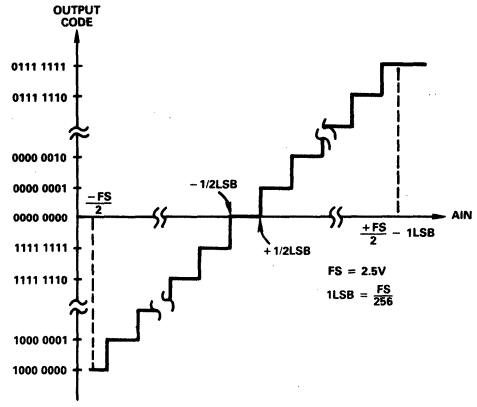


Figure 23. Nominal Transfer Characteristic for Bipolar (−1.25V to +1.25V) Operation

ADC OFFSET AND FULL-SCALE ERROR ADJUSTMENT

In most Digital Signal Processing (DSP) applications, offset and full-scale error have little or no effect on system performance. A typical example is a digital filter, where an ac analog signal is quantized by the ADC, digitally processed and recreated using the DAC. In these type of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important parameter in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

In applications where absolute accuracy is important then ADC offset and full-scale error can be adjusted to zero. Figure 24 shows the additional components required for offset and full-scale error adjustment. Offset error must be adjusted before full-scale error. Zero offset is achieved by adjusting the offset of the op amp driving V_{IN} (i.e., A1 in Figure 23). In unipolar applications, for zero offset error, apply 1/2LSB at the analog input and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 and 0000 0001. For zero full-scale error apply an analog input of FS – 3/2LSBs and adjust R1 until the ADC output code flickers between 1111 1110 and 1111 1111.

In bipolar applications, to adjust for bipolar zero offset apply −1/2LSB at the analog input and adjust the op amp offset voltage until the output code flickers between 1111 1111 and 0000 0000. For zero full-scale error apply +FS/2 – 3/2LSB at the analog input and adjust R1 until the ADC output code flickers between 01111110 and 0111 1111.

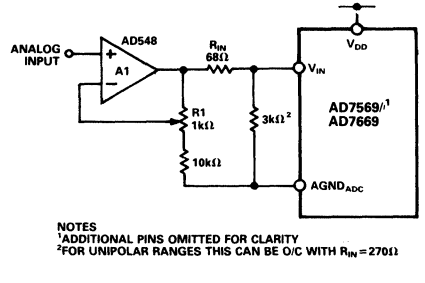


Figure 24. ADC Error Adjust Circuit

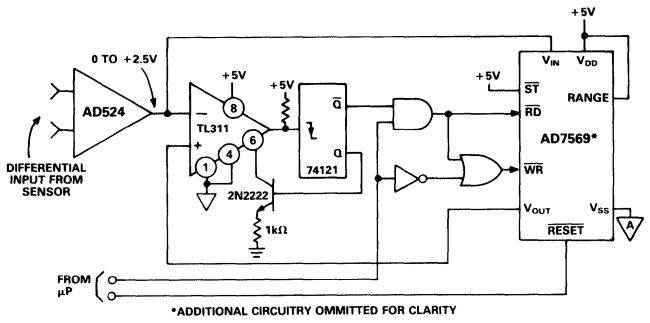


Figure 25. Peak-Reading A/D Converter

PEAK DETECTION – AD7569

The circuit of Figure 25 shows a peak-reading A/D converter which is useful in such applications as monitoring flow rates, temperature, pressure, etc. The circuit ensures that a peak will not be missed while at the same time does not require the microprocessor to frequently monitor the data. The peak value is stored in the A/D converter and can be read at any time.

The gain on the AD524 is adjusted to yield a 0 to +2.5V output. When the input signal exceeds the current stored value, the output of the TL311 goes low, triggering the $\overline{Q}$ output of the 74121. This low-going pulse starts a conversion on the AD7569 ADC and at the end of conversion latches the result into the DAC. This pulse must be at least 120ns greater than the conversion time of the ADC. The Q output is used to drive the strobe input of the TL311, resetting the TL311 output high in readiness for another conversion.

The additional gates on the $\overline{RD}$ and $\overline{WR}$ inputs are to allow the data to be read by the microprocessor while at the same time ensuring that the DAC is not updated when the microprocessor reads the data. It may be necessary to monitor the AD7569 $\overline{BUSY}$ line to ensure that a processor READ is not attempted while the AD7569 is in the middle of a conversion. The READ pulse width from the processor must be less than 1μs to ensure correct data is read from the ADC. A low-going pulse on the $\overline{RESET}$ line resets the DAC output to 0V and starts a new "peak-detection" period. This $\overline{RESET}$ pulse must also be less than 1μs.

DISK DRIVE APPLICATION – AD7669

Closed-Loop Microstepping

Microstepping is a popular technique in low density disk drives (both floppy and hard disk) which allows higher positional resolution of the disk drive head over that obtainable from a full-step driven stepper motor. Typically, a two-phase stepper motor has its phase currents driven with a sine-cosine relationship. These cosinusoidal signals are generated by two DACs driven with the appropriate data. The resolution of the DACs determines the number of microsteps into which each full step can be divided. For example, with a 1.8° full-step motor and a 4-bit DAC, a microstep size of 0.11° (1.8°/(2^n) is obtainable.

The microstepping technique improves the positioning resolution possible in any control application. However, the positional accuracy can be significantly worse than that offered by the original full-step accuracy specification due to load torque effects.

To ensure that the increased resolution is useable, it is therefore necessary to use a closed-loop system where the position of the disk drive head (or motor) is monitored. The closed-loop system allows an error between the desired position and the actual position to be monitored and corrected. The correction is achieved by adjusting the ratio of the phase currents in the motor windings until the required head position is reached.

The AD7669 is ideally suited for the closed-loop microstepping technique with its on-chip dual DACs for positioning the disk drive head and on-board ADC for monitoring the position of the head. A generalized circuit for a closed-loop microstepping system is shown in Figure 26. The DAC waveforms are shown in Figure 27 along with the direction information for clockwise rotation supplied by the controller.

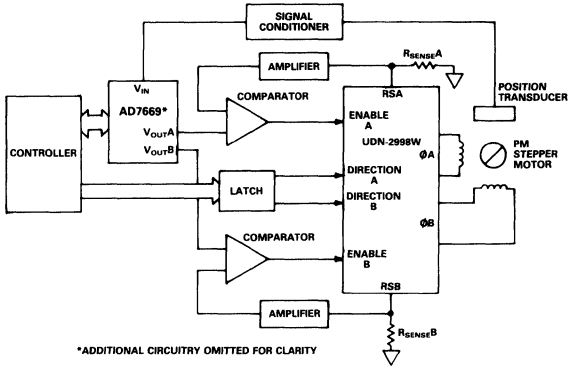


Figure 26. Typical Closed-Loop Microstepping Circuit with the AD7669

The AD7669 is used in the unipolar 0 to +2.5V configuration. This allows the circuit of Figure 26 to be completely unipolar (+5V, +12V supplies); no negative power supplies are required. The power output stage is a dual H-Bridge device such as the UDN-2998W from Sprague Electric. The phase currents in both windings are detected by means of the small value sense resistors, R_SA and R_SB, in series with the windings. The voltage developed across these resistors is amplified and compared with the respective DAC output voltage. The comparators in turn chop the phase winding current. The ADC completes the feedback path by converting information from a suitable transducer for analysis by the controller.

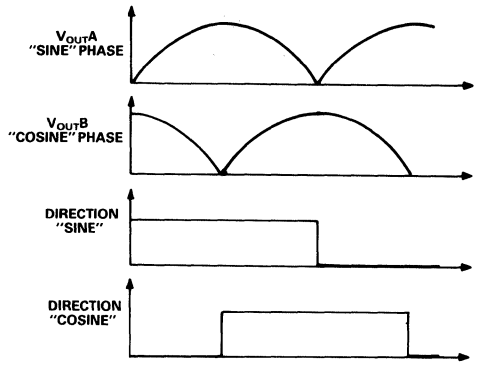


Figure 27. Typical DAC Output Voltages for Microstepping and Direction Signals for Clockwise Rotation with the UDN-2998W

ANALOG DELAY LINE – AD7569

In many applications, especially in audio systems, it is necessary to provide a delay on the input signal. The circuit of Figure 28 shows how a simple analog delay line can be implemented based on the AD7569. The input signal is sampled using the AD7569 ADC and converted data is loaded into the 6116 (2K × 8 static ram). The inverted input clock drives a counter which selects the address for the 6116. The delay is selected by choosing one of the output lines of the HCT4040 counter to reset the counter. This can be done using a simple switch in a manual system or by a multiplexer in a programmable delay application. Data is written to the DAC using the inverted input clock signal.

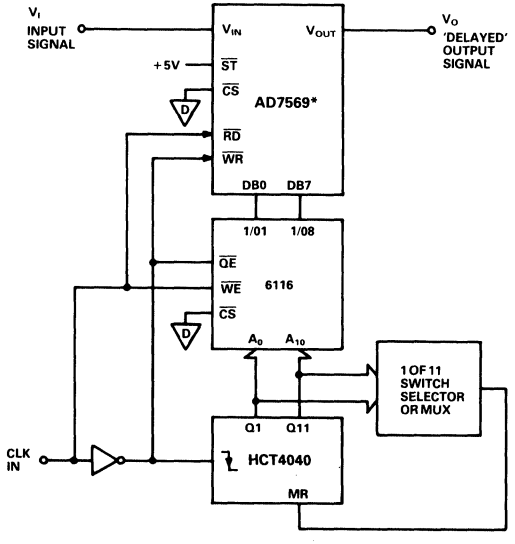


Figure 28. Analog Delay Line

On initial start-up the output voltage, V_O, will be invalid until the length of the delay is reached (i.e., until the counter is reset). From here on the delayed data is read from the 6116 and loaded to the DAC before the newly converted data is written into the same memory location. The input clock to the system can be a square wave of maximum input frequency 200kHz (assuming 2μs conversion time for the ADC). The mark/space ratio of the input clock can be varied to maximize the sampling frequency if required. The clock low time has to be equal to the conversion time and access time of the ADC plus the setup time required for the 6116. The clock high time has only to be equal to the setup time for the DAC plus the delay time through the counter and the access time of the 6116.

The amount of memory used, as well as the sampling frequency, determines the maximum possible delay. Using the HCT4040 and the 6116 with an input clock frequency of 200kHz, the maximum delay is 5ms on a maximum input frequency of 100kHz. Using 64K memory, with an 8kHz input clock frequency the maximum delay is 8 seconds on a maximum input frequency of 4kHz.

TRANSIENT RECORDER – AD7569

The scheme just outlined can also form the basis for a transient recorder. In this case transients on the input signal are converted and stored in memory. The transient can then be recalled from memory at a later time and the transient waveform can be recreated using the AD7569 DAC.

INFINITE SAMPLE-AND-HOLD – AD7569

The AD7569 is ideal for implementing a single-chip infinite sample-and-hold function. Basically, the ADC samples and converts the input signal into an 8-bit digital word. The 8 bits of data are then loaded to the DAC and the sampled value is restored to analog form. The sampled value is held until the DAC register is updated. The full-scale matching between the ADC and the DAC on the AD7569 ensures a typical error of less than 1% between the analog input voltage and the "held" output voltage. Figure 29 shows the connections required on the AD7569 to achieve this infinite sample-and-hold function.

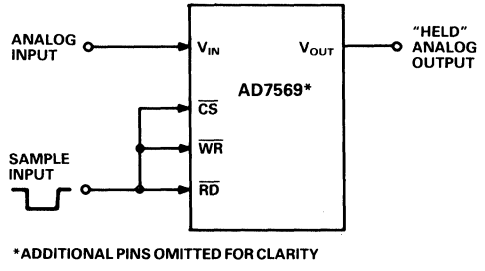


Figure 29. Infinite Sample-and-Hold

TARE FUNCTION FOR WEIGH SCALE – AD7569

The infinite sample-and-hold just outlined can also form the basis of a circuit to provide a tare function for a weigh scale system. Figure 30 shows a circuit for a weigh scale system. It incorporates a tare function using a simple circuit based on the AD7569.

The AD587 along with the 2N6285 provides a buffered +10V reference to supply the low impedance load cell transducer. The load cell output is amplified by the AD624 precision instrumentation amplifier with gain adjustment provided by R1. The output of the AD624 is applied to the noninverting input of a unity gain differential summing amplifier which uses the AD707, a high precision op amp with low drift. The AD707 feeds a 3 1/2 digit panel meter module which converts the signal for digital readout. The input signal to the panel meter is also applied to the analog input of the AD7569 for the tare function. When the tare switch (S1) is closed, a tare cycle commences and V_{IN} is sampled and held infinitely at V_{OUT} until the next tare cycle. V_{OUT} drives the inverting input of the differential amplifier and forces its output to zero. Thus, the tare function is used to give a readout of zero for any undesired weight, such as a box, when only the item placed in it is to be weighed. The tare function can also be used in calibrating the system, to cancel out offset errors due to the load cell, AD624 and differential amplifier.

The AD7569 offers many advantages in the system outlined, such as: simple, low cost circuit – no need for microprocessor, software, etc. – and low power consumption.

3

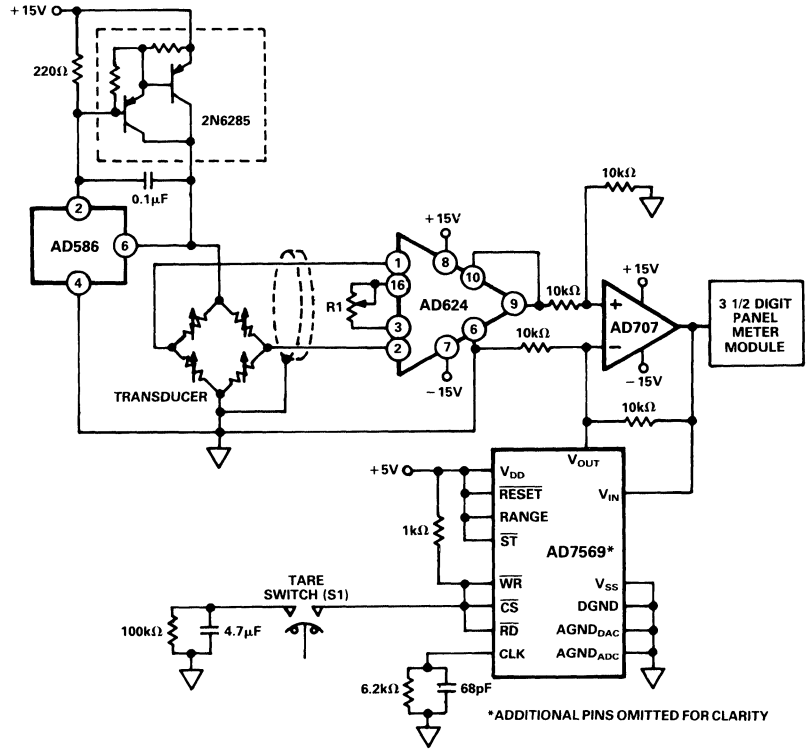


Figure 30. Weigh Scale System with Tare Function

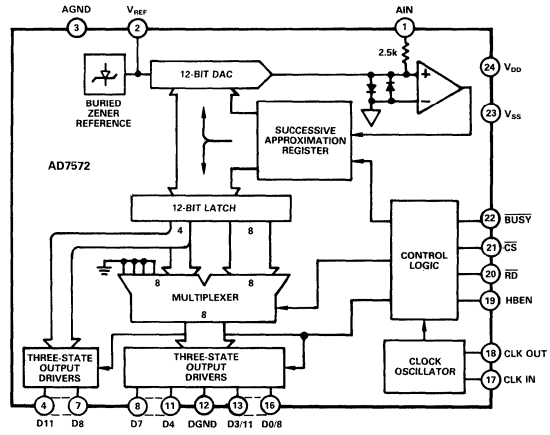
ANALOG DEVICES

LC²MOS Complete, High Speed 12-Bit ADC

AD7572

FEATURES
12-Bit Resolution and Accuracy
Fast Conversion Time
AD7572XX05: 5μs
AD7572XX12: 12.5μs
Complete with On-Chip Reference
Fast Bus Access Time: 90ns
Low Power: 135mW
Small, 0.3", 24-Pin Package and 28-Terminal Surface Mount Packages

AD7572 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7572 is a complete, 12-bit ADC that offers high speed performance combined with low, CMOS power levels. The AD7572 uses an accurate, high speed DAC and comparator in a successive-approximation loop to achieve a fast conversion time. An on-chip, buried Zener diode provides a stable reference voltage to give low drift performance over the full temperature range and the specified accuracy is achieved without any user trims. An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation, or the clock input may be driven from an external clock source such as a divided-down microprocessor clock. The only other external components required for basic operation of the AD7572 are decoupling capacitors for the supply voltages and reference output.

The AD7572 has a high speed digital interface with three-state data outputs and can operate under the control of standard microprocessor Read ($\overline{RD}$) and decoded address ($\overline{CS}$) signals. Interface timing is sufficiently fast to allow the AD7572 to operate with most popular microprocessors, with three-state enable times of only 90ns and bus relinquish times of 75ns.

The AD7572 is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

The AD7572 is available in both 0.3" wide , 24-pin DIPs and in a 28-terminal plastic leaded chip carrier (PLCC) and leadless ceramic chip carrier (LCCC).

PRODUCT HIGHLIGHTS

1. Fast, 5μs and 12.5μs conversion times make the AD7572 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any wideband data acquisition system.
2. On-chip buried-Zener reference has temperature coefficient as low as 25ppm/°C, giving low full-scale drift over the operating temperature range.
3. Stable DAC and comparator give excellent linearity and low zero error over the full temperature range.
4. Fast, easy-to-use digital interface has three-state bus access times of 90ns and bus relinquish times of 75ns, allowing the AD7572 to interface to most popular microprocessors.
5. LC²MOS circuitry gives low power drain (135mW) from +5, −15 volt supplies.
6. 24-pin 0.3" package offers space saving over parts in 28-pin 0.6" DIP.

SPECIFICATIONS (V_{DD} = 5V ±5%, V_{SS} = −15V ±5%, f_{CLK}: 2.5MHz for AD7572XX05, 1MHz for AD7572XX12. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode.)

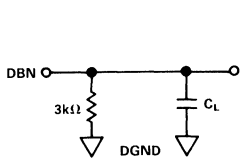
Parameter	J, A, S Versions[1]	K, B, T Versions	L Version	C, U Versions	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1	±1/2	±1/2	LSB max	
T_{min} to T_{max}	±1	±1	±1/2	±3/4	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	
Minimum Resolution for which no Missing Codes are Guaranteed	12	12	12	12	Bits	
Offset Error @ +25°C	±4	±3	±3	±3	LSB max	
T_{min} to T_{max}	±6	±5	±4	±4	LSB max	Typical Change over Temp Is ±1LSB
Full Scale (FS) Error[2] @ +25°C	±15	±10	±10	±10	LSB max	V_{DD} = 5V; V_{SS} = −15V; FS = 5V
Full Scale TC[3,4]	45	25	25	25	ppm/°C max	Ideal Last Code Transition = FS − 3/2LSBs
ANALOG INPUT						
Input Voltage Range	0 to +5	0 to +5	0 to +5	0 to +5	Volts	For Bipolar Operation See
Input Current	3.5	3.5	3.5	3.5	mA max	Figures 10 & 12
INTERNAL REFERENCE VOLTAGE						
V_{REF} Output @ +25°C	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	V min/V max	−5.25V ±1%
V_{REF} Output TC	40	20	20	20	ppm/°C typ	
Output Current Sink Capability	550	550	550	550	µA max	External Load Should Not Change During Conversion
POWER SUPPLY REJECTION						
V_{DD} Only	±1/2	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{SS} = −15V V_{DD} = +4.75V to +5.25V
V_{SS} Only	±1/2	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{DD} = 5V V_{SS} = −14.25V to −15.75V
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN						
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	+2.4	V min	
C_{IN},[5] Input Capacitance	10	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$, HBEN						
I_{IN}, Input Current	±10	±10	±10	±10	µA max	V_{IN} = 0 to V_{DD}
CLK IN						
I_{IN}, Input Current	±20	±20	±20	±20	µA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS						
D11–D0/8, $\overline{BUSY}$, CLK OUT						
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200µA
D11–D0/8						
Floating State Leakage Current	±10	±10	±10	±10	µA max	
Floating State Output Capacitance[5]	15	15	15	15	pF max	
CONVERSION TIME						
AD7572XX05						
Synchronous Clock	5	5	5	5	µs max	f_{CLK} = 2.5MHz. See Under
Asynchronous Clock	4.8/5.2	4.8/5.2	4.8/5.2	4.8/5.2	µs min/max	Control Inputs Synchronization
AD7572XX12						
Synchronous Clock	12.5	12.5	12.5	12.5	µs max	f_{CLK} = 1MHz
Asynchronous Clock	12/13	12/13	12/13	12/13	µs min/µs max	
POWER REQUIREMENTS						
V_{DD}	+5	+5	+5	+5	V NOM	±5% for Specified Performance
V_{SS}	−15	−15	−15	−15	V NOM	±5% for Specified Performance
I_{DD}[6]	7	7	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V
I_{SS}[6]	12	12	12	12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V
Power Dissipation	135	135	135	135	mW typ	
	215	215	215	215	mW max	

NOTES
[1]Temperature range as follows: J, K, L Versions; 0 to +70°C.
A, B, C Versions; −25°C to +85°C.
S, T, U Versions; −55°C to +125°C.
[2]Includes internal voltage reference error.
[3]Full-Scale TC = ΔFS/ΔT, where ΔFS is Full-Scale change from T_A = +25°C to T_{min} or T_{max}.
[4]Includes internal voltage reference drift.
[5]Sample tested to ensure compliance.
[6]Power supply current is measured when AD7572 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.
Specifications subject to change without notice.

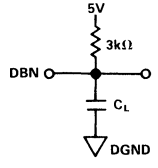
TIMING CHARACTERISTICS[1] (V_{DD} = 5V, V_{SS} −15V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, L, A, B, C Grades)	Limit at T_{min}, T_{max} (S, T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	90	110	120	ns max	Data Access Time after $\overline{RD}$, C_L = 20pF
	125	150	170	ns max	Data Access Time after $\overline{RD}$, C_L = 100pF
t_4	t_3	t_3	t_3	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
t_7[3]	20	20	20	ns min	Bus Relinquish Time
	75	85	90	ns max	
t_8	0	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	200	200	200	ns min	Delay Between Successive Read Operations

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

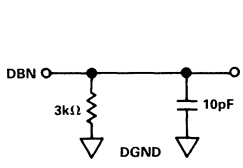


a. *High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)*

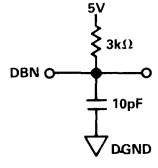


b. *High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)*

Figure 1. Load Circuits for Access Time



a. *V_{OH} to High-Z*



b. *V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V to +7V
V_{SS} to DGND	+0.3V to −17V
AGND to DGND	−0.3V, V_{DD} + 0.3V
AIN to AGND	−15V to +15V
Digital Input Voltage to DGND (CLK IN, HBEN, $\overline{RD}$, $\overline{CS}$)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (D11–D0/8, CLK OUT, $\overline{BUSY}$)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
Commercial (J, K, L Versions)	0 to +70°C
Industrial (A, B, C Versions)	−25°C to +85°C
Extended (S, T, U Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	1,000mW
Derates above +75°C by	10mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION[1]

CONVERSION TIME = 5μs

Full-Scale TC	Accuracy Grade	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (D-24A)	**Hermetic[3] DIP (Q-24)**	**Hermetic[3] DIP (Q-24)**
45ppm/°C	±1LSB	AD7572JN05	AD7572AQ05	AD7572SQ05
25ppm/°C	±1LSB	AD7572KN05	AD7572BQ05	AD7572TQ05
25ppm/°C	±1/2LSB	AD7572LN05	AD7572CQ05	AD7572UQ05
		PLCC[4] (P-28A)		**LCCC[5] (E-28A)**
45ppm/°C	±1LSB	AD7572JP05		AD7572SE05
25ppm/°C	±1LSB	AD7572KP05		AD7572TE05
25ppm/°C	±1/2LSB	AD7572LP05		AD7572UE05

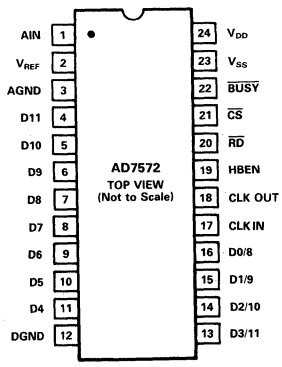
CONVERSION TIME = 12.5μs

Full-Scale TC	Accuracy Grade	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (D-24A)	**Hermetic[3] DIP (Q-24)**	**Hermetic[3] DIP (Q-24)**
45ppm/°C	±1LSB	AD7572JN12	AD7572AQ12	AD7572SQ12
25ppm/°C	±1LSB	AD7572KN12	AD7572BQ12	AD7572TQ12
25ppm/°C	±1/2LSB	AD7572LN12	AD7572CQ12	AD7572UQ12
		PLCC[4] (P-28A)		**LCCC[5] (E-28A)**
45ppm/°C	±1LSB	AD7572JP12		AD7572SE12
25ppm/°C	±1LSB	AD7572KP12		AD7572TE12
25ppm/°C	±1/2LSB	AD7572LP12		AD7572UE12

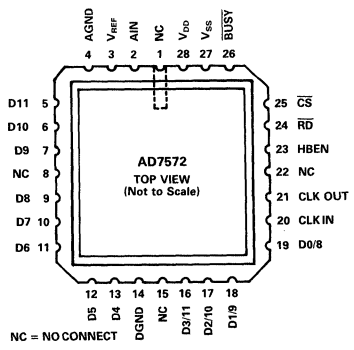
NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC Drawing #5962-87591.
[2]See Section 14 for package outline information.
[3]Analog Devices reserves the right to ship either ceramic (package outline D-24A) or cerdip hermetic (package outline Q-24) packages.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

PIN CONFIGURATIONS

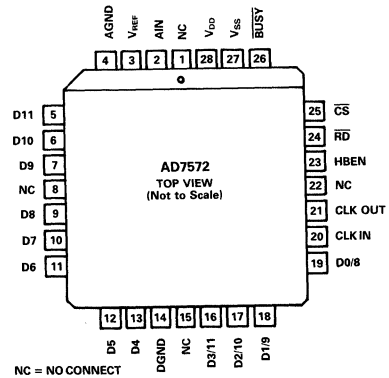
DIP



LCCC



PLCC



PIN FUNCTION DESCRIPTION

DIP Pin No.	Mnemonic	Description
1	AIN	Analog Input.
2	V_{REF}	Voltage Reference Output. The AD7572 has its own internal −5.25V reference.
3	AGND	Analog Ground.
4 . . . 11	D11 . . .D4	Three State data outputs. They become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
13 . . . 16	D3/11 . . . D0/8	Individual pin function is dependent upon High Byte Enable (HBEN) Input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

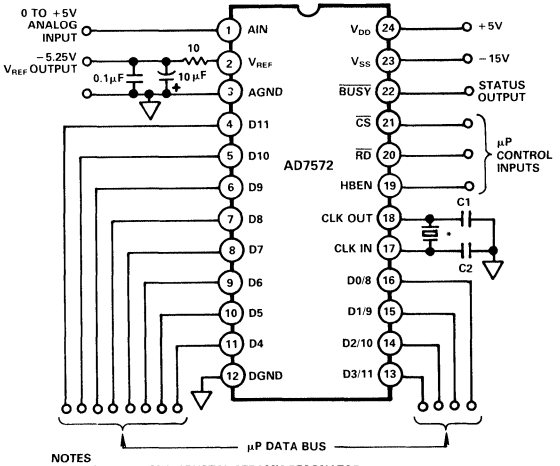
	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

NOTE
*D11 . . . D0/8 are the ADC data output pins.
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB.

12	DGND	Digital Ground.
17	CLK IN	Clock Input pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output Pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description for crystal (resonator).
19	HBEN	High Byte Enable input. Its primary function is to multiplex the 12-bits of conversion data onto the lower D7 . . . D0/8 outputs (4MSBs or 8 LSBs). See Pin description 4 . . . 11 and 13 . . . 16. It also disables conversion start when HBEN is high.
20	$\overline{RD}$	READ input. This active LOW signal, in conjunction with $\overline{CS}$ is used to enable the output data three state drivers and initiate a conversion if $\overline{CS}$ and HBEN are low.
21	$\overline{CS}$	CHIP SELECT Input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three state drivers and initiate a conversion if $\overline{RD}$ and HBEN are low.
22	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
23	V_{SS}	Negative Supply, −15V.
24	V_{DD}	Positive Supply, +5V.

OPERATIONAL DIAGRAM

An operational diagram for the AD7572 is shown in Figure 3. The AD7572 is a 12-bit successive approximation A/D converter. The addition of just a crystal/ceramic resonator and a few capacitors enables the device to perform the analog-to-digital function.



NOTES
AD7572XX05 – 2.5MHz CRYSTAL/CERAMIC RESONATOR.
AD7572XX12 – 1.0MHz CRYSTAL/CERAMIC RESONATOR.
C1 and C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30 to 100pF.

Figure 3. AD7572 Operational Diagram

CONVERTER DETAILS

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be re-started.

During conversion, the internal 12-bit voltage mode DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 4, the AIN input connects to the comparator input via 2.5kΩ. The DAC which has a similar 2.5kΩ output impedance connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output. The MSB decision is made 80ns (typically) after the second falling edge of CLK IN following a conversion start. Similarly, the succeeding bit decisions are made approximately 80ns after a CLK IN edge until conversion is finished. At the end of conversion, the DAC output current balances the AIN input current. The SAR contents (12-bit data word) which represent the AIN input signal is loaded into a 12-bit latch.

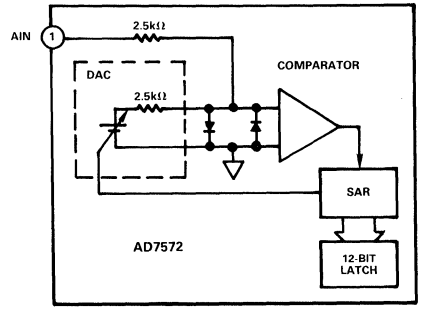


Figure 4. AD7572 AIN Input

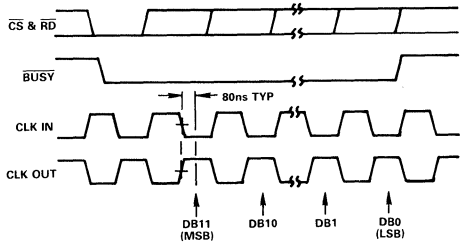


Figure 5. Operating Waveforms Using an External Clock Source for CLK IN

CONTROL INPUTS SYNCHRONIZATION

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach ensures a fixed 5μs conversion time for the AD7572XX05 and 12.5μs for the AD7572XX12: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT.

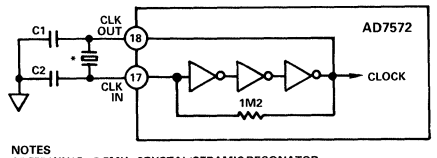
DRIVING THE ANALOG INPUT

During conversion, the AIN input current is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 2.5MHz when CLK IN = 2.5MHz). The analog input voltage must remain fixed during this period and as a result must be driven from an op amp or sample hold with a low output impedance. The output impedance of an op amp is equal to the open loop output impedance divided by the loop gain at the frequency of interest.

Suitable devices capable of driving the AD7572 AIN input are the AD OP-27 and AD711 op amps or the AD585 sample hold.

INTERNAL CLOCK OSCILLATOR

Figure 6 shows the AD7572 internal clock circuit. A crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18) to provide a clock oscillator for the ADC timing. Alternatively the crystal/resonator may be omitted and an external clock source may be connected to CLK IN. For an external clock the mark/space ratio must be 50/50. An inverted CLK IN signal will appear at the CLK OUT pin as shown in the operating waveforms of Figure 5.



NOTES
AD7572XX05 – 2.5MHz CRYSTAL/CERAMIC RESONATOR.
AD7572XX12 – 1.0MHz CRYSTAL/CERAMIC RESONATOR.
C1 and C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30 to 100pF.

Figure 6. AD7572 Internal Clock Circuit

INTERNAL REFERENCE

The AD7572 has an on-chip, buffered, temperature-compensated, buried Zener reference, which is factory trimmed to −5.25V ±1%. It is internally connected to the DAC and is also available at Pin 2 to provide up to 550μA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter out wideband noise from the reference diode (10μF of tantalum in parallel with 100nF ceramic). However, large values of decoupling capacitor can affect the dynamic response and stability of the reference amplifier. A 10Ω resistor in series with the decoupling capacitors will eliminate this problem without adversely affecting the filtering effect of the capacitors. A simplified schematic of the reference with its recommended decoupling components is shown in Figure 7.

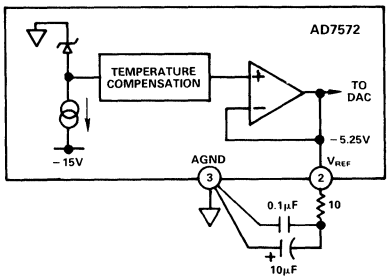


Figure 7. AD7572 Internal −5.25V Reference

UNIPOLAR OPERATION

Figure 8 shows the ideal input/output characteristic for the 0 to 5 volt input range of the AD7572. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, 5/2LSBs . . . FS-3/2LSBs). The output code is natural binary with 1LSB = FS/4096 = (5/4096)V = 1.22mV.

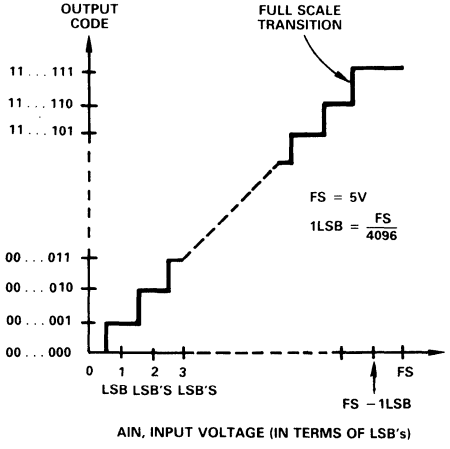


Figure 8. AD7572 Ideal Input/Output Transfer Characteristic

UNIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

In applications where absolute accuracy is important then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 9 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving AIN (i.e., A1 in Figure 9.). For zero offset error apply 0.61mV (i.e., 1/2LSB) at V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

For zero full-scale error apply an analog input of 4.99817V (i.e., FS-3/2LSBs or last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

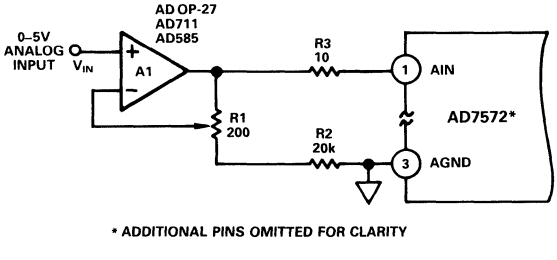


Figure 9. Unipolar 0 to +5V Operation with Gain Error Adjust

BIPOLAR OPERATION

Figures 10 and 12 show how bipolar operation can be achieved with the AD7572. Both circuits use an op-amp to offset the analog signal (V_{IN}) by 2.5V. Alternatively, the op amp (A1) can be replaced by a sample hold as shown in Figure 24. The op amp transfer functions are given below:

Figure 10: AIN = (V_{IN} + 2.5) volts
Figure 12: AIN = (−V_{IN} + 2.5) volts

Both circuits have an analog input range of ±2.5V and an LSB size of 1.22mV. The output codes are offset binary for Figure 10 and complementry offset binary for Figure 12. Their ideal input/output transfer characteristics after offset and full scale adjustment are shown in Figures 11 and 13.

Signal ranges other than ±2.5V are easily accommodated using different values of R3 and R4 for Figure 10, and a different R2 value for Figure 12. These resistors should be chosen such that the voltage range at AIN covers the full dynamic range (i.e., 0V to 5V) of the ADC. All resistors should be the same type and from the same manufacturer so that their temperature coefficients match.

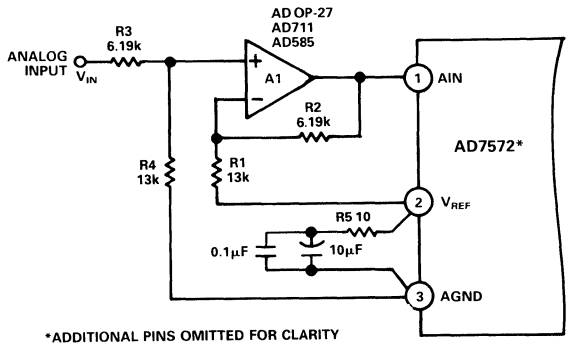


Figure 10. AD7572 Bipolar Operation – Output Code is Offset Binary

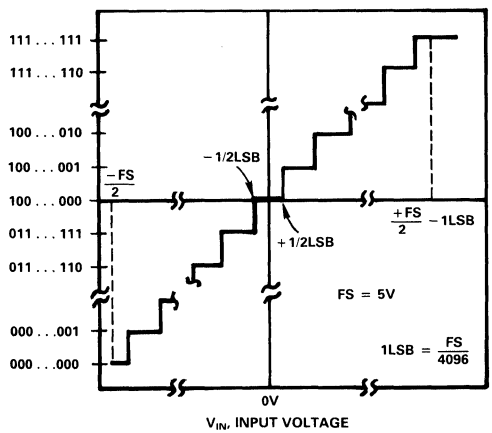


Figure 11. Ideal Input/Output Transfer Characteristic for the Bipolar Circuit of Figure 10

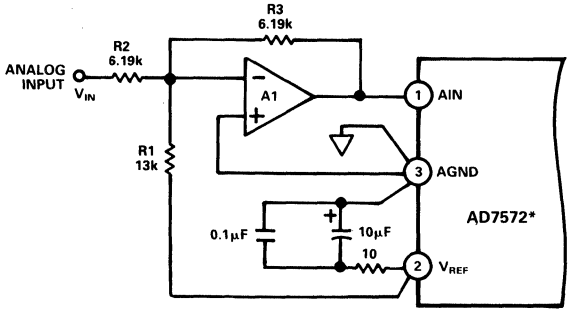


Figure 12. AD7572 Bipolar Operation – Output Code is Complementary Offset Binary

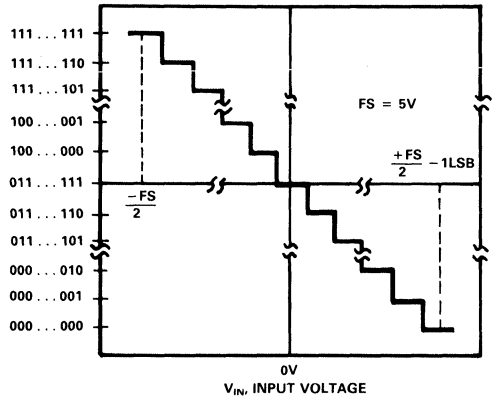


Figure 13. Ideal Input/Output Transfer Characteristic for the Bipolar Circuit of Figure 12

OFFSET AND FULL-SCALE ERROR

In most Digital Signal Processing (DSP) applications offset and full-scale error have little or no effect on system performance. A typical example is a digital filter, where an analog signal is quantized, digitally processed and recreated using a DAC. In these type of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important parameter in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

In measurement applications where absolute accuracy is required, offset and full-scale error can be adjusted to zero as in Figure 14.

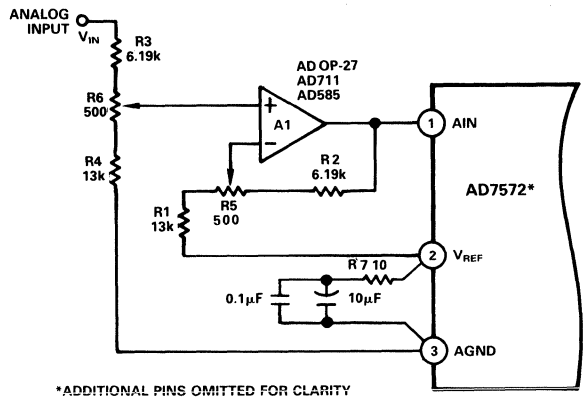


Figure 14. AD7572 Bipolar Operation with Offset and Gain Error Adjust

BIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

The bipolar circuit of Figure 10 can be adjusted for offset and full-scale errors, by including two potentiometers R5 and R6, as shown in Figure 14. Offset must be adjusted before full-scale error. This is achieved by applying an analog input of 0.61mV (1/2LSB) at V_{IN} and adjusting R5 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

For full-scale error adjustment, the analog input must be at 2.49817 volts (i.e., FS/2 – 3/2LSBs or last transition point). Then R6 is adjusted until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

A similar offset and full-scale error adjustment procedure may be employed for Figure 12 by making R1 and R2 variable. Offset must again be adjusted before full scale error. This is achieved by applying an analog input of 0.61mV at V_{IN} and adjusting R1 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

For full-scale error adjust, apply a signal source of 2.49817V at V_{IN} and adjust R2 until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

APPLICATION HINTS

Wire wrap boards are not recommended for high resolution or high-speed A/D converters. To obtain the best performance from the AD7572 a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the AD7572. The analog input should be screened by AGND.

A single point analog ground (STAR ground) separate from the logic system ground should be established at Pin 3 (AGND) or as close as possible to the AD7572 as shown in Figure 15. Pin 12 (AD7572 DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to AIN and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the AD7572 data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the AD7572 data bus.

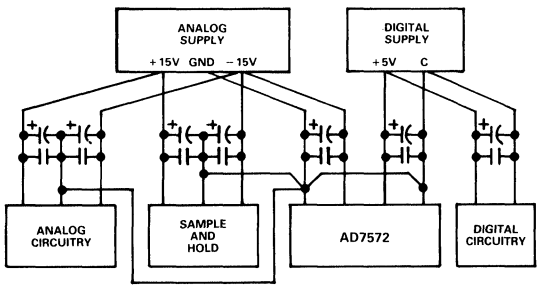


Figure 15. Power Supply Grounding Practice

TIMING AND CONTROL

Conversion start and data read operations are controlled by three AD7572 digital inputs; HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 16 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic "0" is required on all three inputs to initiate a conversion. Once initiated it cannot be re-started until conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

There are two modes of operation as outlined by the timing diagrams of Figures 17 to 20. Slow Memory Mode is designed for microprocessors which can be driven into a WAIT state, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete.
The second is the ROM Mode which does not require microprocessor WAIT states, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.

DATA FORMAT

The output data format can either be a complete parallel load (DB11..DB0) for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word. For a two byte read, only data outputs D7 . . . D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7 . . . D0/8 outputs (4 MSBs or 8 LSBs) where it can be read in two read cycles. The 4 MSB's always appear on D11 . . . D8 whenever the three-state output drives are turned on.

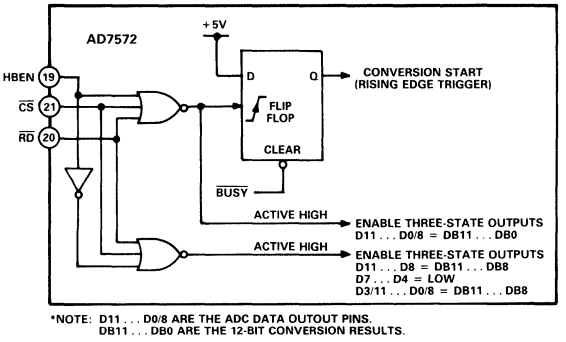


Figure 16. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN

SLOW MEMORY MODE, PARALLEL READ (HBEN = LOW)

Figure 17 and Table I shows the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the AD7572 acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11 . . . D0/8.

SLOW MEMORY MODE, TWO BYTE READ

For a two byte read only 8 data outputs D7 . . . D0/8 are used. Conversion start procedure and data output status for the first read operation is identical to Slow Memory Mode, Parallel Read. See Figure 18 timing diagram and Table II data bus status. At the end of conversion the low data byte (DB7 . . . DB0) is read from the ADC. A second READ operation with HBEN high, places the high byte on data outputs D3/11 . . . D0/8 and disables conversion start. Note the 4MSB's appear on data outputs D11 . . . D8 during the two READ operations above.

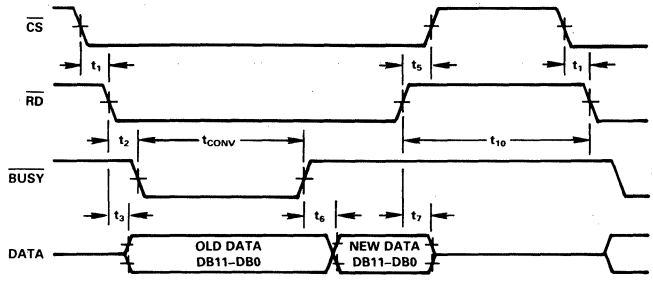


Figure 17. Slow Memory Mode, Parallel Read Timing Diagram

AD7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table I. Slow Memory Mode, Parallel Read Data Bus Status

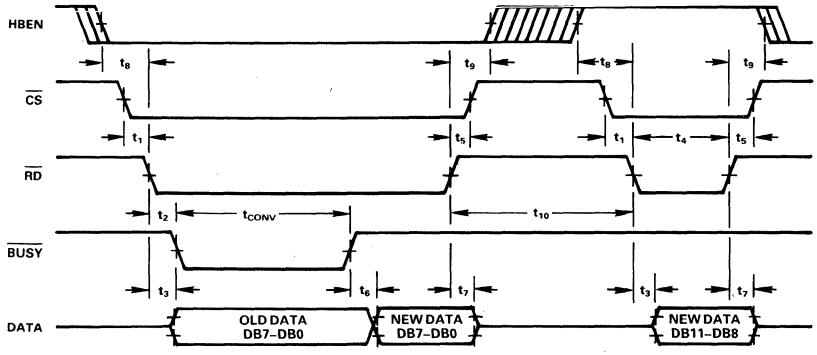


Figure 18. Slow Memory Mode, Two Byte Read Timing Diagram

AD7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Table II. Slow Memory Mode, Two Byte Read Data Bus Status

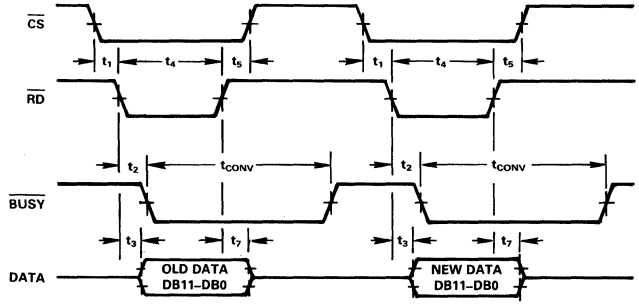


Figure 19. ROM Mode, Parallel Read Timing Diagram

AD7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table III. ROM Mode, Parallel Read Data Bus Status

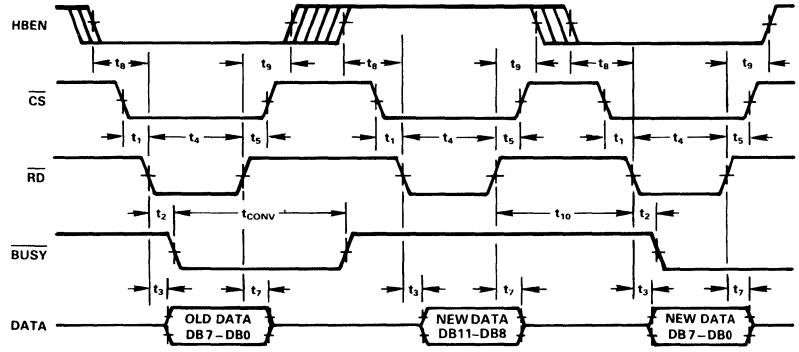


Figure 20. ROM Mode, Two Byte Read Timing Diagram

AD7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table IV. ROM Mode, Two Byte Read Data Bus Status

ROM MODE, PARALLEL READ (HBEN = LOW)

The ROM Mode avoids placing a microprocessor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion is available on data outputs D11 . . . D0/8 (see Figure 19 and Table III). This data may be disregarded if not required. A second READ operation reads the new data (DB11 . . . DB0) and starts another conversion. A delay at least as long as the AD7572 conversion time must be allowed between READ operations.

ROM MODE, TWO BYTE READ

As previously mentioned for a two byte read, only data outputs D7 . . . D0/8 are used. Conversion is started in the normal way with a READ operation and the data output status is the same as the ROM Mode, Parallel Read. See Figure 20 timing diagram and Table IV data bus status. Two more READ operations are required to access the new conversion result. A delay equal to the AD7572 conversion time must be allowed between conversion start and the second data READ operation. The second READ operation, with HBEN high, disables conversion start and places the high byte (4MSBs) on data outputs D3/11 . . . D0/8. A third READ operation accesses the low data byte (DB7 . . . DB0) and starts another conversion. The 4MSB's appear on data outputs D11 . . . D8 during all three read operations above.

MICROPROCESSOR INTERFACING

The AD7572 is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally connected to the microprocessor address bus.

MC68000 Microprocessor

Figure 21 shows a typical interface for the 68000. The AD7572 is operating in the Slow Memory Mode. Assuming the AD7572 is located at address C000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result.

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$, so that the 68000 is forced into a WAIT state. At the end of conversion $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the UP.

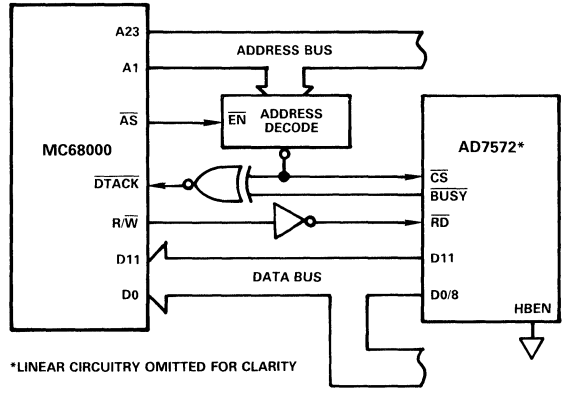


Figure 21. AD7572 – MC68000 Interface

8085A, Z80 MICROPROCESSOR

Figure 22 shows an AD7572 interface for the Z80 and 8085A. The AD7572 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN, so that an even address (HBEN = LOW) to the AD7572 will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit LOAD instruction below.

For the 8085A	LHLD (B000)
For the Z80	LD HL, (B000)

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, $\overline{BUSY}$ forces the microprocessor to WAIT for the AD7572 conversion. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

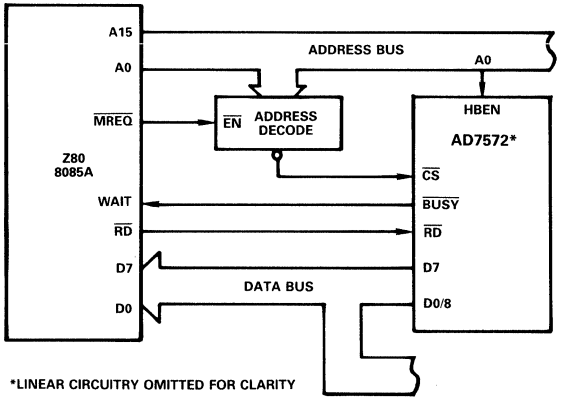


Figure 22. AD7572 – 8085A/Z80 Interface

TMS32010 MICROCOMPUTER

Figure 23 shows an AD7572–TMS32010 interface. The AD7572 is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The AD7572 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into data memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

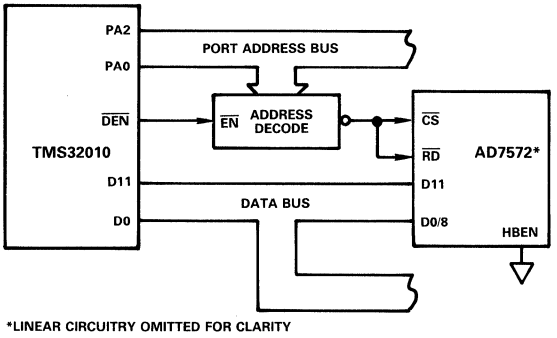


Figure 23. AD7572 – TMS32010 Interface

AD7572-AD585 SAMPLE-HOLD INTERFACE

Figure 24 shows an AD585 sample-hold amplifier driving the AIN input of the AD7572. The interface contains resistors R1, R2, R3 and R4 to allow a bipolar input signal range of ±2.5 volts. The maximum sampling frequency is 125kHz for the AD7572XX05 (5μs conversion) and 64.5kHz for the AD7572XX12 (12.5μs conversion). This includes the sample-hold amplifier acquisition time (3μs).

When an AD7572 conversion is initiated, the converter $\overline{BUSY}$ output goes low indicating conversion is in progress. The falling edge of this $\overline{BUSY}$ output signal places the sample-hold amplifier into the HOLD mode "freezing" the input signal to the AD7572. When conversion is finished, the $\overline{BUSY}$ output returns HIGH allowing the sample-hold to track the input signal. To achieve the maximum sampling rate, the AD7572 output data must be read within 3μs immediately after conversion while the sample-hold amplifier is acquiring the next sample.

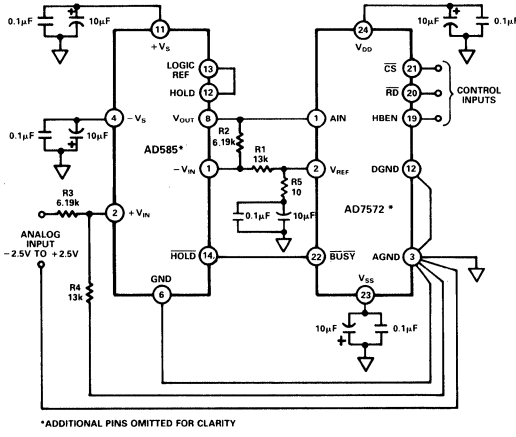


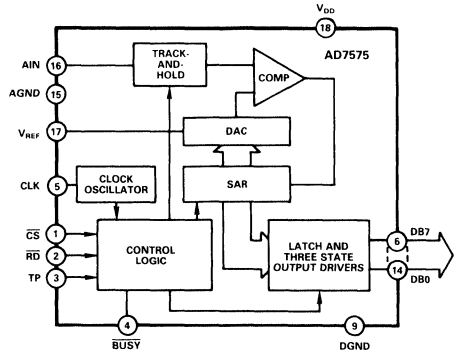
Figure 24. AD7572 – AD585 Sample-and-Hold Interface

ANALOG DEVICES

LC²MOS
5μs 8-Bit ADC with Track/Hold
AD7575

FEATURES
- **Fast Conversion Time: 5μs**
- **On-Chip Track/Hold**
- **Low Total Unadjusted Error: 1LSB**
- **Full Power Signal Bandwidth: 50kHz**
- **Single +5V Supply**
- **100ns Data Access Time**
- **Low Power (15mW typ)**
- **Low Cost**
- **Standard 18-Pin DIPs or 20-Terminal Surface Mount Packages**

AD7575 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7575 is a high-speed 8-bit ADC with a built-in track/hold function. The successive approximation conversion technique is used to achieve a fast conversion time of 5μs, while the built-in track/hold allows full-scale signals up to 50kHz (386mV/μs slew rate) to be digitized. The AD7575 requires only a single +5V supply and a low-cost, 1.23V bandgap reference in order to convert an input signal range of 0 to $2V_{REF}$.

The AD7575 is designed for easy interfacing to all popular 8-bit microprocessors using standard microprocessor control signals ($\overline{CS}$ and $\overline{RD}$) to control starting of the conversion and reading of the data. The interface logic allows the AD7575 to be easily configured as a memory mapped device and the part can be interfaced as SLOW-MEMORY or ROM. All data outputs of the AD7575 are latched and three-state buffered to allow direct connection to a microprocessor data bus or I/O port.

The AD7575 is fabricated in an advanced, all ion-implanted high-speed linear compatible CMOS (LC^2MOS) process and is available in either a small, 0.3" wide 18-pin DIP or in 20-terminal surface mount packages.

ORDERING INFORMATION[1]

Relative Accuracy (LSB)	Temperature Range and Package Options[2]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-18)	**Hermetic DIP (Q-18)**	**Hermetic DIP (Q-18)**
±1	AD7575JN	AD7575AQ	AD7575SQ
±1/2	AD7575KN	AD7575BQ	AD7575TQ
	PLCC[3] (P-20A)		**LCCC[4] (E-20A)**
±1	AD7575JP		AD7575SE
±1/2	AD7575KP		AD7575TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-87762.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time/Low Power
   The fast, 5μs conversion time of the AD7575 makes it suitable for digitizing wideband signals at audio and ultrasonic frequencies, while retaining the advantage of low CMOS power consumption.
2. On-Chip Track/Hold
   The on-chip track/hold function is completely self-contained and requires no external hold capacitor. Signals with slew rates up to 386mV/μs (e.g., 2.46V peak-to-peak 50kHz sine waves) can be digitized with full accuracy.
3. Low Total Unadjusted Error
   The zero, full-scale and linearity errors of the AD7575 are so low that the total unadjusted error at any point on the transfer function is less than 1LSB and offset and gain adjustments are not required.
4. Single Supply Operation
   Operation from a single +5V supply with a low-cost +1.23V bandgap reference allows the AD7575 to be used in 5V microprocessor systems without any additional power supplies.
5. Fast Digital Interface
   Fast interface timing allows the AD7575 to interface easily to the fast versions of most popular microprocessors such as the Z80H, 8085A-2, 6502B, 68B09 and the DSP processor, the TMS32010.

SPECIFICATIONS (V_{DD} = +5V; V_{REF} = +1.23V; AGND = DGND = 0V; f_{CLK} = 4MHz external; All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A Versions[1]	K, B Versions	S Version	T Version	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±½	±1	±½	LSB max	
Minimum Resolution for which						
No Missing Codes is Guaranteed	8	8	8	8	Bits max	
Full Scale Error						
25°C	±1	±1	±1	±1	LSB max	Full Scale TC is typically 5ppm/°C
T_{min} to T_{max}	±1	±1	±1	±1	LSB max	
Offset Error[2]						
25°C	±½	±½	±½	±½	LSB max	Offset TC is typically 5ppm/°C
T_{min} to T_{max}	±½	±½	±½	±½	LSB max	
ANALOG INPUT						
Voltage Range	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	Volts	1LSB = $2V_{REF}$/256; See Figure 4
DC Input Impedance	10	10	10	10	MΩ min	
Slew Rate, Tracking	0.386	0.386	0.386	0.386	V/μs max	
SNR[3]	45	45	45	45	dB min	V_{IN} = 2.46V p-p @ 10kHz; See Figure 1
REFERENCE INPUT						
V_{REF} (For specified Performance)	1.23	1.23	1.23	1.23	Volts	±5%
I_{REF}	500	500	500	500	μA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
25°C	±1	±1	±1	±1	μA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	μA max	V_{INL} = 0V
I_{INH}, Input High Current	700	700	800	800	μA max	V_{INH} = V_{DD}
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40μA
DB0 to DB7						
Floating State Leakage Current	±1	±1	±10	±10	μA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	5	5	5	5	μs	f_{CLK} = 4MHz
With Internal Clock, T_A = 25°C	5	5	5	5	μs min	Using recommended clock
	15	15	15	15	μs max	components shown in Figure 3.
POWER REQUIREMENTS[5]						
V_{DD}	+5	+5	+5	+5	Volts	±5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3mA with V_{DD} = +5V
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	±¼	±¼	±¼	±¼	LSB max	4.75V≤V_{DD}≤5.25V

NOTES

[1]Temperature Ranges are as follows:
J, K Versions; 0 to +70°C
A, B Versions; −25°C to +85°C
S, T Versions; −55°C to +125°C

[2]Offset error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

[3]Sample tested at 25°C to ensure compliance.

[4]Accuracy may degrade at conversion times other than those specified.

[5]Power supply current is measured when AD7575 is inactive i.e. when $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = logic HIGH.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} TO AGND	−0.3V, +7V
V_{DD} TO DGND	−0.3V, +7V
AGND TO DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND	−0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD}
AIN TO AGND	−0.3V, V_{DD}
Operating Temperature Range	
Commercial, (J, K Versions)	0 to +70°C
Industrial (A, B Versions)	−25°C to +85°C
Extended (S, T Versions)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

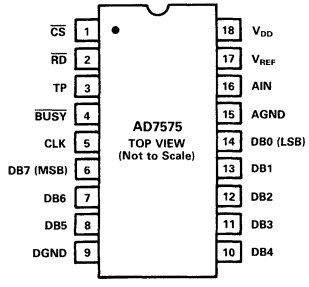
3

CAUTION

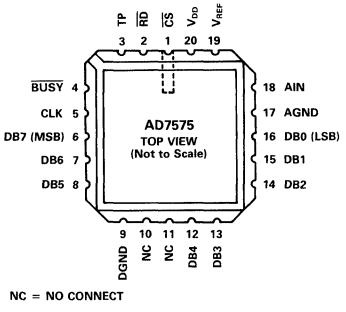
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP

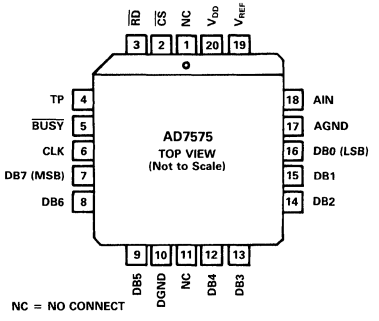


LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

TRACK-AND-HOLD

The on-chip track-and-hold on the AD7575 means that input signals with slew rates up to 386mV/μs can be converted without error. This corresponds to an input signal bandwidth of 50kHz for a 2.46V peak-to-peak sine wave. Figure 1 shows a typical plot of signal-to-noise ratio versus input frequency, over the input bandwidth of the AD7575. The SNR figures are generated using a 200kHz sampling frequency and the reconstructed sine wave passes through a filter with a cutoff frequency of 50kHz.

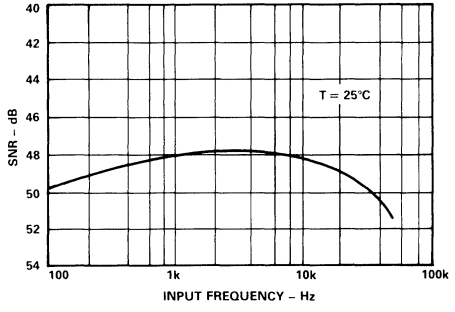


Figure 1. SNR vs. Input Frequency

The improvement in the SNR figures seen at the higher frequencies is due to the sharp cut-off of the filter (50kHz, 8th order Chebyshev) used in the test circuit.

The input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ go LOW. This is indicated in Figure 2 for the Slow Memory Interface. In between conversions the input signal is tracked by the AD7575 track-and-hold. Since the sampled signal is held on a small, on-chip capacitor it is advisable that the data bus be kept as quiet as possible during a conversion.

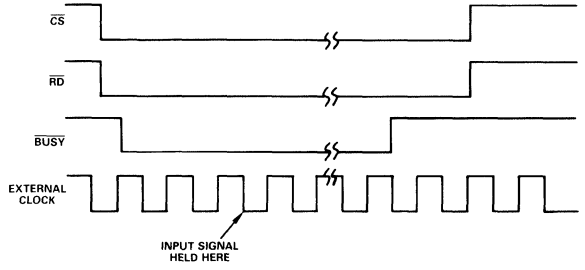


Figure 2. Track-and-Hold (Slow Memory Interface) with External Clock

Unipolar/Bipolar Considerations

UNIPOLAR OPERATION

The basic operation for the AD7575 is in the unipolar single supply mode. Figure 3 shows the circuit connections to achieve this while the nominal transfer characteristic for unipolar operation is given in Figure 4. Since the offset and full-scale errors on the AD7575 are very small, in many cases it will not be necessary to adjust out these errors. If calibration is required the procedure is as follows:

Offset Adjust

Offset error adjustment in single-supply systems is easily achievable by means of the offset null facility of an op-amp when used as a voltage follower for the analog input signal, AIN. The op-amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0V (e.g., TLC271). To adjust for zero offset the input signal source is set to +4.8mV (i.e., 1/2LSB) while the op-amp offset is varied until the ADC output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

The full scale or gain adjustment is made by forcing the analog input AIN to +2.445V (i.e., Full-Scale Voltage −3/2LSB). The magnitude of the reference voltage is then adjusted until the ADC output code flickers between 111 . . . 10 and 111 . . . 11.

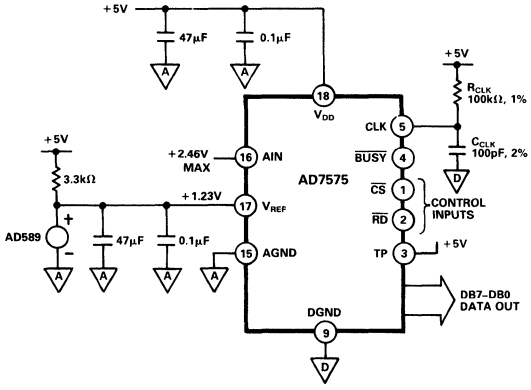


Figure 3. AD7575 Unipolar Configuration

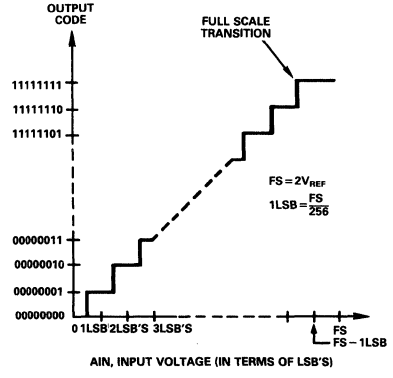


Figure 4. Nominal Transfer Characteristic for Unipolar Operation

BIPOLAR OPERATION

The circuit of Figure 5 shows how the AD7575 can be configured for bipolar operation. The output code provided by the AD7575 is offset binary. The analog input voltage range is ±5V, although the voltage appearing at the AIN pin of the AD7575 is in the range 0V to +2.46V. Figure 6 shows the transfer function for bipolar operation. The LSB size is now 39.06mV. Calibration of the bipolar operation is outlined below. Once again, because the errors are small it may not be necessary to adjust them. To maintain specified performance without the calibration all resistors should be 0.1% tolerance with R4 and R5 replaced by one 3.3kΩ resistor and R2 and R3 replaced by one 2.5kΩ resistor.

Offset Adjust

Offset error adjustment is achieved by applying an analog input voltage of −4.9805V (−FS/2 +1/2LSB). Resistor R3 is then adjusted until the output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

Full scale or gain adjustment is made by applying an analog input voltage of +4.9414V (+FS/2 −3/2LSB). Resistor R4 is then adjusted until the output code flickers between 111 . . . 10 and 111 . . . 11.

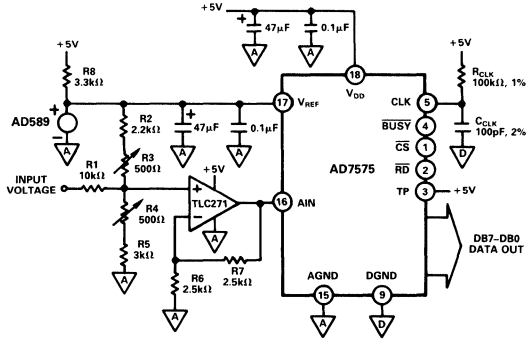


Figure 5. AD7575 Unipolar Configuration

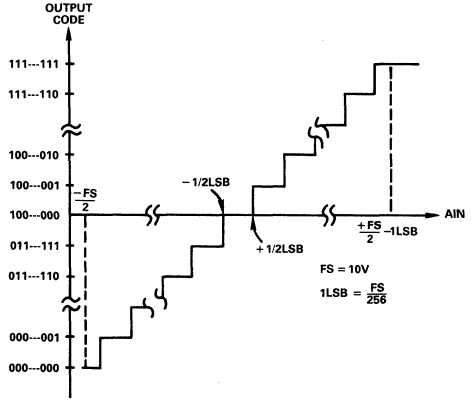


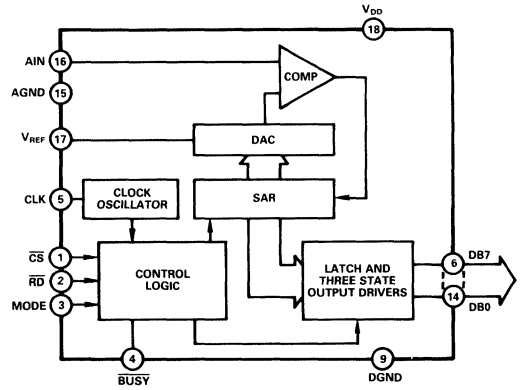
Figure 6. Nominal Transfer Characteristic for Unipolar Operation

LC²MOS
10μs μP Compatible 8-Bit ADC
AD7576

FEATURES

- **Single +5V Operation with External Positive Reference**
- **Fast Conversion Time: 10μs**
- **No Missed Codes Over Full Temperature Range**
- **Microprocessor Compatible**
- **Low Cost**
- **Low Power (15mW)**
- **100ns Data Access Time**

AD7576 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7576 is a low cost, low power, microprocessor compatible 8-bit analog-to-digital converter, which uses the successive approximation technique to achieve a fast conversion time of 10μs. The device is designed to operate with an external reference of +1.23V (standard bandgap reference) and converts input signals from 0V to $2V_{REF}$.

The part is designed for ease of microprocessor interface with three control inputs ($\overline{CS}$, $\overline{RD}$ and MODE) controlling all ADC operations such as starting conversion and reading data. The interface logic allows the part to be easily configured as a memory mapped device. All data outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. The output latches serve to make the conversion process transparent to the microprocessor.

The part is designed for single +5V operation, has on-board comparator, interface logic, and internal/external clock option. This makes the AD7576 ideal for most ADC/μP interface applications.

The AD7576 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process and is available in either a small, 0.3" wide, 18-pin DIP or in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Single Supply Operation
   Operation from a single +5V supply with a +1.23V reference allows operation of the AD7576 with microprocessor systems without any additional power supplies.
2. Low Power
   CMOS fabrication of the AD7576 results in a very low power dissipation figure of 15mW typical.
3. Versatile Interface Logic
   The AD7576 can be configured to perform continuous conversions or to convert on command. It can be interfaced as SLOW-MEMORY or ROM, allowing versatile interfacing to most microprocessors.
4. Fast Conversion Time
   The fabrication of the AD7576 on Analog Devices' Linear Compatible CMOS (LC²MOS) process enables fast conversion times of 10μs, eliminating the need for expensive Sample-and-Holds in many low frequency applications.

ORDERING INFORMATION[1]

Relative Accuracy (LSB)	Temperature Range and Package Options[2]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-18)	**Hermetic DIP (Q-18)**	**Hermetic DIP (Q-18)**
±1	AD7576JN	AD7576AQ	AD7576SQ
±1/2	AD7576KN	AD7576BQ	AD7576TQ
	PLCC[3] (P-20A)		**LCCC[4] (E-20A)**
±1	AD7576JP		AD7576SE
±1/2	AD7576KP		AD7576TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS (V_{DD} = +5V; V_{REF} = +1.23V; AGND = DGND = 0V; f_{CLK} = 2MHz external; All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A[1] Versions	K, B Versions	S Version	T Version	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±½	±1	±½	LSB max	
Minimum Resolution for which						
No Missing Codes is Guaranteed	8	8	8	8	Bits max	
Full Scale Error						
25°C	±1	±1	±1	±1	LSB max	Full Scale TC is typically 5ppm/°C
T_{min} to T_{max}	±1	±1	±1	±1	LSB max	
Offset Error[2]						
25°C	±½	±½	±½	±½	LSB max	Offset TC is typically 5ppm/°C
T_{min} to T_{max}	±½	±½	±½	±½	LSB max	
ANALOG INPUT						
Voltage Range	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	Volts	1LSB = $2V_{REF}$/256; See Figure 4
DC Input Impedance	10	10	10	10	MΩ min	
REFERENCE INPUT						
V_{REF} (For specified Performance)	1.23	1.23	1.23	1.23	Volts	±5%
I_{REF}	500	500	500	500	µA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, MODE						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
25°C	±1	±1	±1	±1	µA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	µA max	V_{INL} = 0V
I_{INH}, Input High Current	700	700	800	800	µA max	V_{INH} = V_{DD}
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40µA
DB0 to DB7						
Floating State Leakage Current	±1	±1	±10	±10	µA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	10	10	10	10	µs	f_{CLK} = 2MHz
With Internal Clock, T_A = 25°C	10	10	10	10	µs min	Using recommended clock
	30	30	30	30	µs max	components shown in Figure 3.
POWER REQUIREMENTS[5]						
V_{DD}	+5	+5	+5	+5	Volts	±5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3mA with V_{DD} = +5V
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	±¼	±¼	±¼	±¼	LSB max	4.75V≤V_{DD}≤5.25V

NOTES
[1]Temperature Ranges are as follows:
J, K Versions; 0 to +70°C
A, B Versions; −25°C to +85°C
S, T Versions; −55°C to +125°C
[2]Offset error is measured with respect to an ideal first code transition which occurs at 1/2LSB.
[3]Sample tested at 25°C to ensure compliance.
[4]Accuracy may degrade at conversion times other than those specified.
[5]Power supply current is measured when AD7576 is inactive i.e. when $\overline{CS}$ = $\overline{RD}$ = MODE = $\overline{BUSY}$ = logic HIGH.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

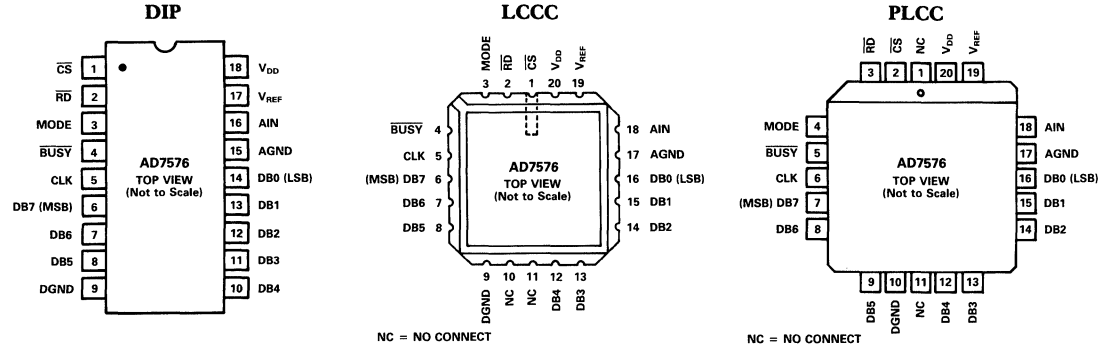
V_{DD} TO AGND	−0.3V, +7V
V_{DD} TO DGND	−0.3V, +7V
AGND TO DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND	−0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD}
AIN TO AGND	−0.3V, V_{DD}
Operating Temperature Range	
Commercial (J, K Version)	0 to +70°C
Industrial (A, B Version)	−25°C to +85°C
Extended (S, T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 secs)	300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS



A SAMPLED-DATA INPUT

The AD7576 makes use of a sampled-data comparator. The equivalent input circuit is shown in Figure 1. When a conversion starts, switch S1 is closed and the equivalent input capacitance is charged to V_{IN}. With a switch resistance of typically 500Ω and an input capacitance of typically 2pF the input time constant is 1ns. Thus C_{IN} becomes charged to within ±¼ LSB in 6.9 time constants or about 7ns. Since the comparator switches are operating at one half the input clock frequency of 2MHz, there is ample time for the input voltage to settle before the comparator decision is made (at the end of a clock period). Increasing the source resistance increases the settling time required. Input bypass capacitors placed directly at the analog input act to average the input charging currents. This average current flowing through any source impedance can cause full-scale errors.

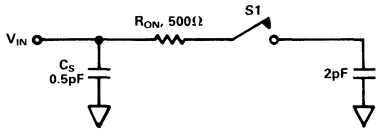


Figure 1. AD7576 Equivalent Input Circuit

REFERENCE INPUT

The reference input impedance on the AD7576 is code dependent and varies by a ratio of approximately 3-to-1 over the digital code range. The typical resistance range is from 6kΩ to 18kΩ. As a result of the code dependent input impedance, the V_{REF} input must be driven from a low impedance source. Figure 2 shows how an AD589 can be configured to produce a nominal reference voltage of +1.23V.

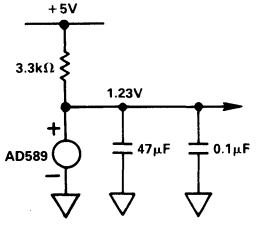


Figure 2. Reference Circuit

Unipolar/Bipolar Considerations

UNIPOLAR OPERATION

The basic operation for the AD7576 is in the unipolar single supply mode. Figure 3 shows the circuit connections to achieve this while the nominal transfer characteristic for unipolar operation is given in Figure 4. Since the offset and full-scale errors on the AD7576 are very small, in many cases it will not be necessary to adjust out these errors. If calibration is required the procedure is as follows:

Offset Adjust

Offset error adjustment in single-supply systems is easily achievable by means of the offset null facility of an op-amp when used as a voltage follower for the analog input signal, AIN. The op-amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0V (e.g., TLC271). To adjust for zero offset the input signal source is set to +4.8mV (i.e., 1/2LSB) while the op-amp offset is varied until the ADC output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

The full scale or gain adjustment is made by forcing the analog input AIN to +2.445V (i.e., Full-Scale Voltage −3/2LSB). The magnitude of the reference voltage is then adjusted until the ADC output code flickers between 111 . . . 10 and 111 . . . 11.

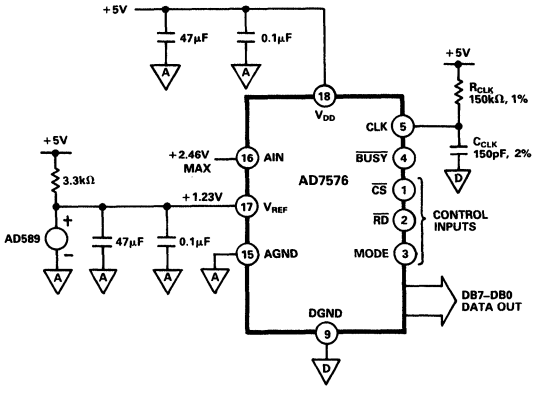


Figure 3. AD7576 Unipolar Configuration

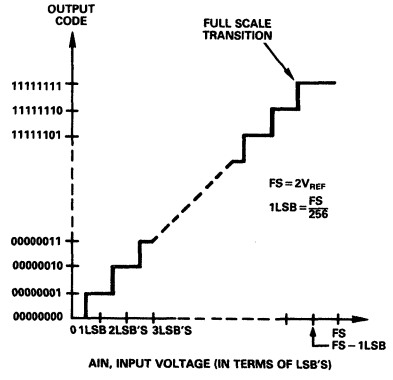


Figure 4. Nominal Transfer Characteristic for Unipolar Operation

BIPOLAR OPERATION

The circuit of Figure 5 shows how the AD7576 can be configured for bipolar operation. The output code provided by the AD7576 is offset binary. The analog input voltage range is ±5V, although the voltage appearing at the AIN pin of the AD7576 is in the range 0V to +2.46V. Figure 6 shows the transfer function for bipolar operation. The LSB size is now 39.06mV. Calibration of the bipolar operation is outlined below. Once again, because the errors are small it may not be necessary to adjust them. To maintain specified performance without the calibration all resistors should be 0.1% tolerance with R4 and R5 replaced by one 3.3kΩ resistor and R2 and R3 replaced by one 2.5kΩ resistor.

Offset Adjust

Offset error adjustment is achieved by applying an analog input voltage of −4.9805V (−FS/2 + 1/2LSB). Resistor R3 is then adjusted until the output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

Full scale or gain adjustment is made by applying an analog input voltage of +4.9414V (+FS/2 −3/2LSB). Resistor R4 is then adjusted until the output code flickers between 111 . . . 10 and 111 . . . 11.

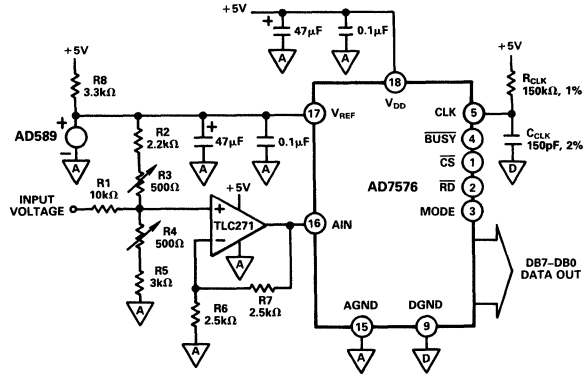


Figure 5. AD7576 Bipolar Configuration

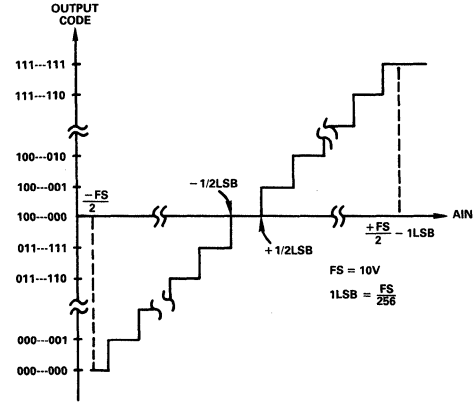


Figure 6. Nominal Transfer Characteristic for Bipolar Operation

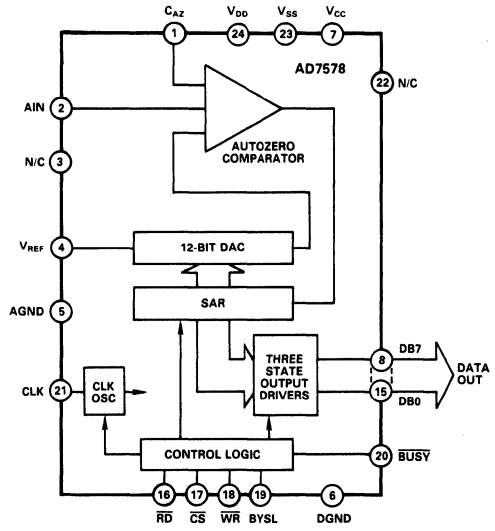
CMOS 12-Bit Successive Approximation ADC

AD7578

FEATURES

- 12-Bit Successive Approximation ADC
- No Missed Codes Over Full Temperature Range
- Low Total Unadjusted Error ±1LSB max
- High Impedance Analog Input
- Autozero Cycle for Low Offset Voltage
- Low Power, 75mW typ
- Small Size: 0.3", 24-Pin Package
- Conversion Time of 100μs

AD7578 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7578 is a medium speed, monolithic 12-bit CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 100μs. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100μV. The device is designed for easy microprocessor interfacing using standard control signals; $\overline{CS}$ (decoded device address), $\overline{RD}$ ($\overline{READ}$) and $\overline{WR}$ ($\overline{WRITE}$).

Conversion results are available in two bytes, 8LSBs and 4MSBs, over an 8-bit three state output bus. Either byte can be read first. Two converter busy flags are available to facilitate polling of the converter's status.

The analog input voltage range is 0V to +5V when using a reference voltage of +5V.

PRODUCT HIGHLIGHTS

1. The AD7578 is a complete 12-bit A/D converter in a 24-pin package requiring only a few passive components and a voltage reference.
2. Autozero cycle realizes very low offset voltages, typically 100μV.
3. Standard microprocessor control signals to allow easy interfacing to most popular 8- and 16-bit microprocessors.
4. Monolithic construction for increased reliability and small 0.3", 24-pin DIP.

ORDERING INFORMATION[1]

Total Unadjusted Error	Temperature Range and Package Options[2]		
$T_{min}-T_{max}$	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic (N-24)	Hermetic[3] (D-24A)	Hermetic[3] (D-24A)
±1LSB	AD7578KN	AD7578BD	AD7578TD

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.

SPECIFICATIONS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5.0V f_{CLK} = 140kHz external, all specifications T_{min} to T_{max} unless otherwise noted).

Parameter	K Version[1]	B Version[1]	T Version[1]	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Total Unadjusted Error[2]	±1	±1	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	No missing codes guaranteed
Full Scale Error (Gain Error)	±1/4	±1/4	±1/4	LSB max	Full Scale TC is typically 1ppm/°C
Offset Error	±1/4	±1/4	±1/4	LSB max	Offset Error TC is typically 1ppm/°C
ANALOG INPUT					
Analog Input Range	0 to +5	0 to +5	0 to +5	V	V_{REF} = +5.0V
C_{AIN}, Input Capacitance	8	8	8	pF typ	
I_{AIN}, Input Leakage Current					AIN; 0 to +5V
+25°C	10	10	10	nA max	
T_{min} to T_{max}	100	100	100	nA max	
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+5	+5	+5	V	±5%
V_{REF} Range	+4 to +6	+4 to +6	+4 to +6	V	Degraded transfer accuracy
V_{REF} Input Reference Current	1.0	1.0	1.0	mA max	V_{REF} = +5.0V
POWER SUPPLY REJECTION					
V_{DD} Only	±1/8	±1/8	±1/8	LSB typ	V_{DD} = +14.25V to +15.75V V_{SS} = −5V
V_{SS} Only	±1/8	±1/8	±1/8	LSB typ	V_{SS} = −4.75V to −5.25V V_{DD} = +15V
LOGIC INPUTS					
$\overline{RD}$ (Pin 16), $\overline{CS}$ (Pin 17), $\overline{WR}$ (Pin 18)					
BYSL (Pin 19)					
V_{IL} Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH} Input High Voltage	+2.4	+2.4	+2.4	V min	
I_{IN} Input Current					
+25°C	±1	±1	±1	μA max	V_{IN} = 0 to V_{CC}
T_{min} to T_{max}	+10	+10	+10	μA max	
C_{IN} Input Capacitance[3]	10	10	10	pF max	
CLK (Pin 21)					
V_{IL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH}, Input High Voltage	+3.0	+3.0	+3.0	V min	
I_{IL}, Input Low Current	±10	±10	±10	μA max	
I_{IH}, Input High Current	+1.5	+1.5	+1.5	mA max	
LOGIC OUTPUTS					
DB0–DB7 (Pins 8–15), $\overline{BUSY}$ (Pin 20)[4]					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA[4]
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	V_{CC} = +5V ±5%, I_{SOURCE} = 200μA
Floating State Leakage Current					
(Pins 8–15)	±1	±1	±1	μA max	V_{OUT} = 0V to V_{CC}
Floating State Output Capacitance	15	15	15	pF max	
CONVERSION TIME[5]					
With External Clock	100	100	100	μs min	f_{CLK} = 140kHz
With Internal Clock, T_A = +25°C	100/150	100/150	100/150	μs min/max	Using recommended clock components as shown in Figure 6.
POWER REQUIREMENTS[6]					
V_{DD}	+15	+15	+15	V NOM	±5% for specified performance
V_{SS}	−5	−5	−5	V NOM	±5% for specified performance
V_{CC}	+5	+5	+5	V NOM	±5% for specified performance
I_{DD}	7.5	7.5	7.5	mA max	Typically 4mA with V_{DD} = +15V
I_{SS}	7.5	7.5	7.5	mA max	Typically 3mA with V_{SS} = −5V
I_{CC}	100	100	100	μA typ	V_{IN} = V_{IL} or V_{IH}
	1.0	1.0	1.0	mA max	
Power Dissipation	75	75	75	mW typ	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH

NOTES

[1]Temperature Range as follows: K Version; 0 to +70°C
B Version; −25°C to +85°C
T Version; −55°C to +125°C

[2]Includes Full Scale Error, Offset Error and Relative Accuracy.

[3]Sample tested to ensure compliance.

[4]I_{SINK} for $\overline{BUSY}$ (pin 20) is 1.0 milliamp.

[5]Conversion Time includes autozero cycle time.

[6]Power supply current is measured when AD7578 is inactive i.e., $\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K & B Grades)	Limit at T_{min}, T_{max} (T Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2 (INT)[2]	200	240	280	ns min	$\overline{WR}$ Pulse Width (Internal Clock Operation)
t_2 (EXT)[2]	10	10	10	µs min	$\overline{WR}$ Pulse Width (External Clock Operation)
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	130	160	200	ns typ	
	200	250	300	ns max	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay
t_5	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_6	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_7	200	240	280	ns min	$\overline{RD}$ Pulse Width
t_8	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9	50	50	50	ns min	BYSL to $\overline{RD}$ Setup Time
t_{10}	0	0	0	ns min	BYSL to $\overline{RD}$ Hold Time
t_{11}[3]	150	180	200	ns typ	
	200	240	280	ns max	$\overline{RD}$ to Valid Data (Bus Access Time)
t_{12}[4]	20	20	20	ns min	$\overline{RD}$ to Three State Output
	130	160	180	ns max	(Bus Relinquish Time)

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_r = t_f$ = 20ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is timed from V_{OH}, V_{OL}.
[2]When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10µs. See "External Clock Operation".
[3]t_{11} is measured with the load circuits of Figure 3 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]t_{12} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
Specifications subject to change without notice.

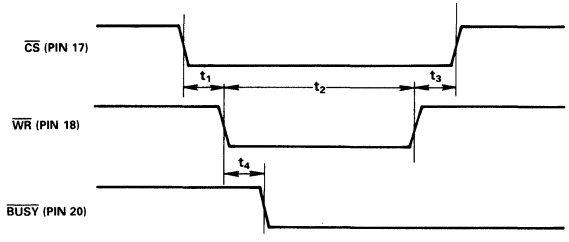
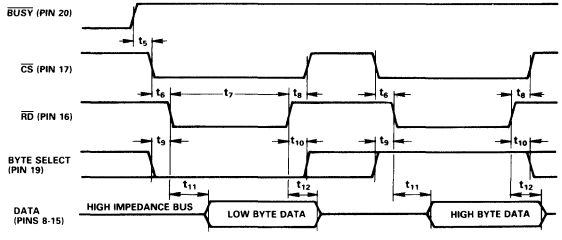
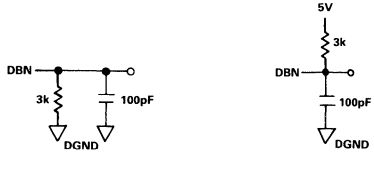


Figure 1. Start Cycle Timing



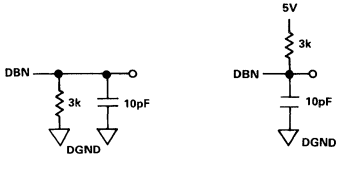
NOTES
THE TWO-BYTE CONVERSION RESULT CAN BE READ IN EITHER ORDER. FIGURE IS FOR LOW BYTE, HIGH BYTE ORDER.
IF BYSL CHANGES WHILE CS & RD ARE LOW THE DATA WILL CHANGE TO REFLECT THE BYSL INPUT.

Figure 2. Read Cycle Timing



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 3. Load Circuits for Access Time Test (t_{11})



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 4. Load Circuits for Output Float Delay Test (t_{12})

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

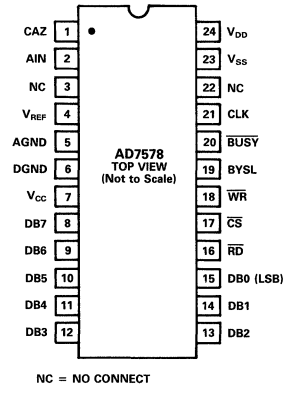
V_{DD} to DGND	−0.3V, +17V
V_{SS} to DGND	+0.3V, −7V
AGND to DGND	−0.3V, V_{REF} +0.3V
V_{CC} to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD} +0.3V
AIN to AGND	−0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND (Pins 16-19, 21)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (Pins 8-15, 20)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
Commercial (K Version)	0 to +70°C
Industrial (B Version)	−25°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package)	
to +75°C	1,000mW
Derate above +75°C by	10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

DIP PIN CONFIGURATION



NC = NO CONNECT

READING DATA

The 12-bit conversion data plus a converter status flag are available over an 8-bit wide data bus. Data is transferred from the AD7578 in right-justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the Byte Select (BYSL) input determining which byte–8 least significant bits or 4 most significant bits plus status flag–is to be read first.

Since the AD7578 uses the successive approximation register (SAR) to hold conversion results (refer to Functional Diagram), it is necessary to wait until a conversion is finished before reading valid 12-bit data. Executing a READ instruction (HIGH or LOW byte) to the AD7578 while a conversion is in progress will place the existing contents of the SAR onto the data bus. Three different approaches can ensure valid 12-bit data is available for reading.

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. At user-defined intervals after a conversion start instruction, poll the internal converter status flag, BUSY. This signal is available on pin 10 during a HIGH byte READ instruction and is the most left-hand bit in a 16-bit right-justified word. The status bit can be shifted into a microprocessor's accumulator-carry position for testing (BUSY is HIGH during conversion).
3. Use the externally available $\overline{BUSY}$ (pin 20) signal as an interrupt to the microprocessor. This signal is LOW during a conversion and returns HIGH at conversion end.

Executing a WRITE instruction to the AD7578 while a conversion is in progress will restart the conversion.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	CAZ	Autozero Capacitor Input. Connect other side of capacitor to AGND.
2	AIN	Analog Input
3	N/C	No Connect pin
4	V_{REF}	Voltage reference input. The AD7578 is specified with $V_{REF} = +5.0V$.
5	AGND	Analog Ground
6	DGND	Digital Ground
7	V_{CC}	Logic Supply. For $V_{CC} = +5V$ digital inputs and outputs are TTL compatible.
8-15		Three state data outputs. They become active when $\overline{CS}$ & $\overline{RD}$ are brought low. Individual pin function is dependent upon the Byte Select (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	BYSL = HIGH	BYSL = LOW
Pin 8	BUSY[1]	DB7
Pin 9	LOW[2]	DB6
Pin 10	LOW[2]	DB5
Pin 11	LOW[2]	DB4
Pin 12	DB11 (MSB)	DB3
Pin 13	DB10	DB2
Pin 14	DB9	DB1
Pin 15	DB8	DB0 (LSB)

[1]BUSY (Pin 8) is a converter status flag and is HIGH during a conversion.
[2]Pins 9-11 output a logic LOW when BYSL is HIGH.
DB11–DB0 are the 12-bit conversion results, DB11 is the MSB.

16	$\overline{RD}$	READ input. This active LOW signal, in combination with $\overline{CS}$, is used to enable the output data three-state drivers.
17	$\overline{CS}$	CHIP SELECT Input. Decoded device address, active LOW. Used in combination with either $\overline{RD}$ or $\overline{WR}$ for control.
18	$\overline{WR}$	WRITE Input. This active LOW signal, in combination with $\overline{CS}$, is used to start a new conversion. When the AD7578 internal clock is used, the minimum $\overline{WR}$ pulse width is t2 (INT). When an external clock source is used, the minimum $\overline{WR}$ pulse width must be extended to include the autozero cycle time. For external clock operation, the minimum $\overline{WR}$ pulse width is t2 (EXT).
19	BYSL	BYTE SELECT. This control input determines whether the high or low byte of data is placed on the output data bus during a data READ operation ($\overline{CS}$ & $\overline{RD}$ LOW). See description of pins 8-15.
20	$\overline{BUSY}$	$\overline{BUSY}$ indicates converter status. $\overline{BUSY}$ is LOW during conversion, otherwise $\overline{BUSY}$ is held at a logic HIGH.
21	CLK	CLOCK Input for internal/external clock operation. Internal : Connect R_{CLK} and C_{CLK1}/C_{CLK2} timing components. See Figure 6 and Figure 7. External : Connect external 74HC compatible clock source as shown in Figure 8.
22	N/C	No connect pin.
23	V_{SS}	Negative supply, −5V.
24	V_{DD}	Positive supply, +15V.

Operating Information

OPERATIONAL DIAGRAM

An operational diagram for the AD7578 is shown in Figure 5. The only passive components required are the autozero capacitor C_{AZ} and timing components R_{CLK}, C_{CLK1} & C_{CLK2} for the internal clock oscillator. If the AD7578 is to be used with an external clock source, then only C_{AZ} is required. Individual pin functions are described in detail on the previous page.

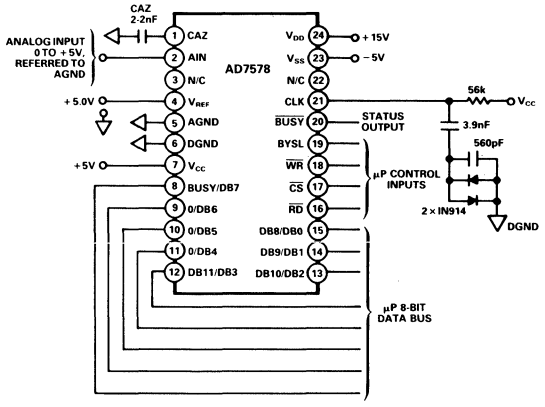


Figure 5. AD7578 Operational Diagram

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 6 and the AD7578 operating waveforms are shown in Figure 7.

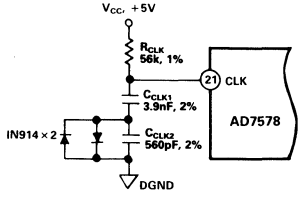
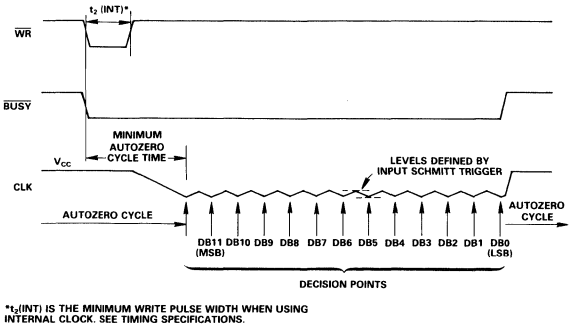


Figure 6. Circuitry Required for Internal Clock Operation



*t_2(INT) IS THE MINIMUM WRITE PULSE WIDTH WHEN USING INTERNAL CLOCK. SEE TIMING SPECIFICATIONS.

Figure 7. Operating Waveforms – Internal Clock

Between conversions ($\overline{BUSY}$ = HIGH) the AD7578 is in the autozero cycle. When $\overline{WR}$ goes LOW (with $\overline{CS}$ LOW) to start a new conversion, the autozero capacitor C_{AZ} charges to AIN – V_{OS} where V_{OS} is the input offset voltage of the autozero comparator.

A minimum time of 10μs is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{WR}$ to remain LOW for this period of time since it is automatically provided by the AD7578. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2}, causing the voltage at the CLK input pin to slowly decay from V_{CC}. This occurs after $\overline{WR}$ returns HIGH. The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK}. When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2}. The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 6 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

EXTERNAL CLOCK OPERATION

For external clock operation R_{CLK}, C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The AD7578 $\overline{WR}$ pulse width must now be extended to provide the minimum autozero cycle time of 10μs since this is no longer provided automatically by the AD7578. Referring to the operating waveforms of Figure 9, the minimum $\overline{WR}$ pulse width when using an external clock source is t_2 (EXT). The $\overline{CS}$ input must now remain valid for the extended $\overline{WR}$ pulse width. It is not necessary to synchronize the external clock source with the extended $\overline{WR}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{WR}$ input returns HIGH.

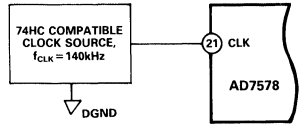
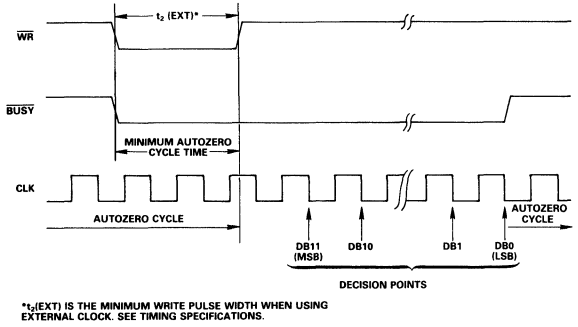


Figure 8. External Clock Operation



*t_2(EXT) IS THE MINIMUM WRITE PULSE WIDTH WHEN USING EXTERNAL CLOCK. SEE TIMING SPECIFICATIONS.

Figure 9. Operating Waveforms – External Clock

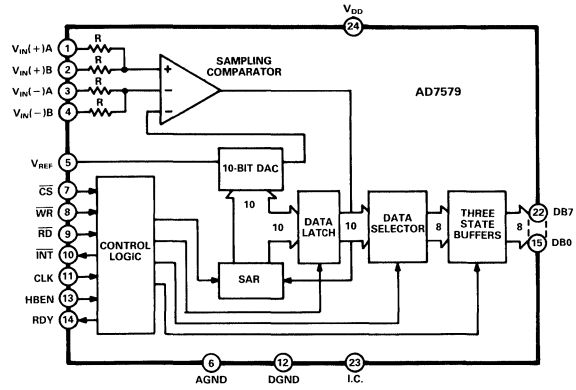
ANALOG DEVICES

LC²MOS
10-Bit Sampling A/D Converters

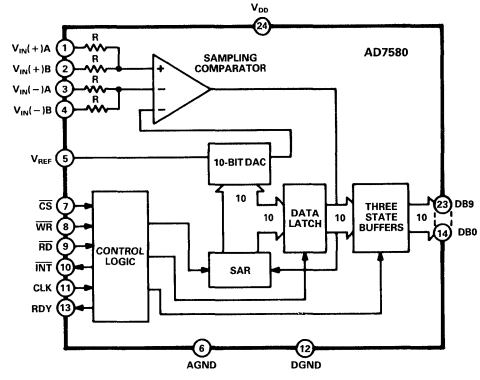
AD7579/AD7580

FEATURES
20μs Conversion Time
On-Chip Sample-Hold
50kHz Sampling Rate
25kHz Full-Power Input Bandwidth
Choice of Data Formats
Single +5V Supply
Low Power (50mW)
Skinny 24-Pin DIP and 28-Terminal Surface Mount Packages

AD7579 FUNCTIONAL BLOCK DIAGRAM



AD7580 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7579 and AD7580 are 10-bit, successive approximation ADCs. They have differential analog inputs that will accept unipolar or bipolar input signals while operating from only a single +5V supply. Input ranges of 0 to +2.5V, 0 to +5V and ±2.5V are possible with no external signal conditioning. Only an external 2.5V reference and clock and control signals are required to make them operate.

With conversion time of less than 20μs and an on-chip sample-hold amplifier, the devices are ideally suited for digitizing ac signals. The maximum sampling rate is 50kHz, giving an input bandwidth of 25kHz. The parts are specified not only with traditional static specifications such as linearity and offset but also with dynamic specifications (SNR, Harmonic Distortion, IMD).

The AD7579 and AD7580 are microprocessor-compatible with standard microprocessor control inputs ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and data outputs capable of interfacing to high-speed data buses. There is a choice of data formats, with the AD7579 offering an (8+2) read and the AD7580 offering a 10-bit parallel word.

Space saving and low power are also features of these devices. They dissipate less than 50mW from a single +5V supply and are offered in a 0.3", 24-pin package and in 28-terminal plastic/ ceramic chip carriers for surface mounting.

PRODUCT HIGHLIGHTS

1. 20μs conversion time with on-chip sample-hold makes the AD7579 and AD7580 ideal for audio and higher bandwidth signals, e.g., modem applications.
2. Differential analog inputs can accept unipolar or bipolar input signals, but only a single, +5V power supply is needed.
3. Versatile and easy-to-use digital interface has fast bus access/ relinquish times, allowing connection to most popular microprocessors.

SPECIFICATIONS[1] (V_{DD} = +5V ±5%; V_{REF} = +2.5V, AGND = DGND = 0V; f_{CLK} = 2.5MHz; All specifications T_{min} to T_{max} unless otherwise noted. Test conditions as in Figure 12 unless otherwise stated).

Parameter	J, A Versions	K, B Versions	S Version	Units	Conditions/Comments
STATIC CHARACTERISTICS					These specifications apply for the
Resolution	10	10	10	Bits	three Analog Input Ranges. See Differential Applications.
Integral Nonlinearity	±1	±1/2	±1	LSB max	No missing codes guaranteed over the
Differential Linearity Error	±0.9	±0.9	±0.9	LSB max	full temperature range[2].
Full-Scale Error	±5	±5	±5	LSB max	
Zero Code Error[3]	±2	±1	±2	LSB max	Connected as in Figure 12.
	±3	±2	±3	LSB max	Connected as in Figure 14 or 15.
Power Supply Rejection	±0.5	±0.5	±0.5	LSB max	4.75V<V_{DD}<5.25V
DYNAMIC CHARACTERISTICS[4,5]					
Conversion Time[6]	16.9	16.9	16.9	µs min	f_{CLK} = 2.5MHz, t_{WR} = 100ns.
	18.5	18.5	18.5	µs max	See Functional Description.
Sampling Rate	50	50	50	kHz max	
Clock Range	250/2.5	250/2.5	250/2.5	kHz min/MHz max	
Signal-to-Noise Ratio	55	55	55	dB min	See Terminology. T_A = 25°C.
	58	60	58	dB typ	
Total Harmonic Distortion	−58	−58	−58	dB max	T_A = 25°C.
	−64	−68	−64	dB typ	
Intermodulation Distortion	−67	−67	−67	dB typ	This is characterized to both SMPTE and CCITT standards. T_A = 25°C.
Slew Rate	160	160	160	mV/µs max	See Terminology
ANALOG INPUT RANGES[7]					
Figure 12					AD7579/AD7580 connected as in Figure 12
Span	V_{REF}	V_{REF}	V_{REF}	V max	
Common-Mode Range	0 to V_{DD}	0 to V_{DD}	0 to V_{DD}	V max	
CMRR	0.5	0.5	0.5	LSB/V typ	
Figure 14					AD7579/AD7580 connected as in Figure 14
Span	$2V_{REF}$	$2V_{REF}$	$2V_{REF}$	V max	
Common-Mode Range	0 to $2V_{DD}$	0 to $2V_{DD}$	0 to $2V_{DD}$	V max	
CMRR	0.5	0.5	0.5	LSB/V typ	
Figure 15					AD7579/AD7580 connected as in Figure 15
Span	$2V_{REF}$	$2V_{REF}$	$2V_{REF}$	V max	
Common-Mode Range	$-V_{REF}$ to ($2V_{DD}-V_{REF}$)	$-V_{REF}$ to ($2V_{DD}-V_{REF}$)	$-V_{REF}$ to ($2V_{DD}-V_{REF}$)	V max	
CMRR	0.5	0.5	0.5	LSB/V typ	
ATTENUATOR INPUT RESISTANCE	5/15	5/15	5/15	kΩ min/kΩ max	10kΩ typical. Resistance measured between $V_{IN}(+)A$, $V_{IN}(+)B$ or $V_{IN}(-)A$, $V_{IN}(-)B$
COMPARATOR INPUT RESISTANCE	10	10	10	MΩ min	AD7579/AD7580 connected as in Figure 12
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+2.5	+2.5	+2.5	V	±5%
I_{REF}	1.5	1.5	1.5	mA max	
LOGIC INPUTS					
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, HBEN, CLK					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
I_{IN}, Input Current					
25°C	±1	±1	±1	µA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[4]	10	10	10	pF max	
LOGIC OUTPUTS					
DB0 to DB7 (DB9)					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	V min	I_{SOURCE} = 400µA
Floating State Leakage Current	±1	±1	±10	µA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[4]	10	10	10	pF max	
RDY, $\overline{INT}$					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
POWER REQUIREMENT					
V_{DD}	+5	+5	+5	V	±5% for Specified Performance
I_{DD}	10	10	10	mA max	Typically 5mA with V_{DD} = +5V
Power Dissipation	50	50	50	mW max	

NOTES
[1]Temperature Ranges as follows:
J, K Versions; 0 to +70°C
A, B Versions; −25°C to +85°C
S Version; −55°C to +125°C
[2]Zero code error and gain error adjusted to zero.
[3]Zero code error is measured with respect to an ideal first code transition which occurs at 1/2LSB.
[4]Sample tested at 25°C to ensure compliance.
[5]These specifications apply for full-scale input signals up to 20kHz.
[6]Accuracy may degrade at conversion times other than those specified.
[7]$V_{IN}(+)$ must always be equal to or more positive than $V_{IN}(-)$, in Figures 12, 14, 15.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5V ±5%, V_{REF} = +2.5V, AGND = DGND = 0V)

Parameter[2,3,4]	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S Grade)	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	40	50	50	ns min	$\overline{WR}$ Pulse Width
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	100	100	120	ns max	$\overline{WR}$ to $\overline{INT}$ Propagation Delay
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_6	t_{12}	t_{12}	t_{12}	ns min	$\overline{RD}$ Pulse Width
t_7	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_8	20	20	30	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	10	10	10	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	110	135	150	ns min	RDY Access Time
t_{11}	100	100	120	ns max	$\overline{RD}$ to $\overline{INT}$ Propagation Delay
t_{12}	110	135	150	ns max	Data Access Time After $\overline{RD}$
t_{13}	10	10	10	ns min	Data Hold Time, RDY Hold Time
	65	80	90	ns max	

NOTES
1. Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F = 20$ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
2. t_4, t_{10}, t_{11} and t_{12} are measured with the load circuits of Figures 3 and 5 and defined as the time required for an output to cross 0.8V or 2.4V.
3. t_{13} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
4. $\overline{INT}$ and RDY are open-drain outputs and need 3kΩ external pull-up resistors for operation.

Specifications subject to change without notice.

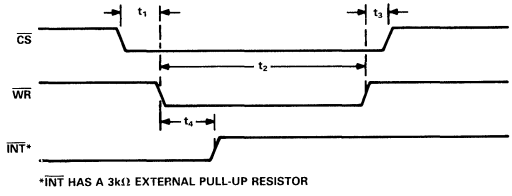


Figure 1. AD7579/AD7580 Start Cycle Timing

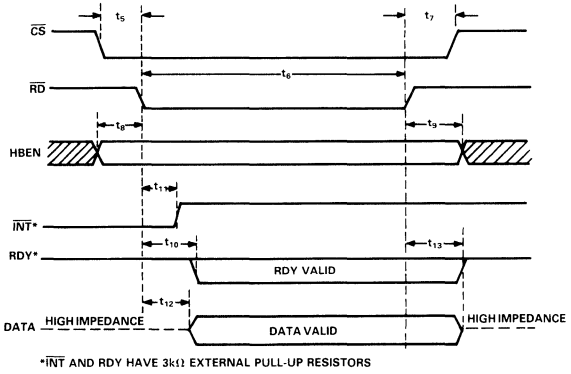
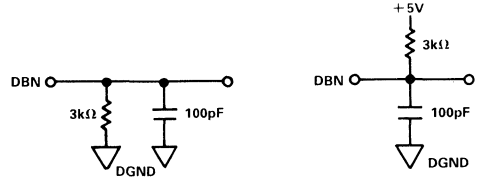
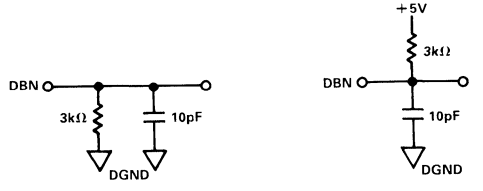


Figure 2. AD7579/AD7580 Read Cycle Timing



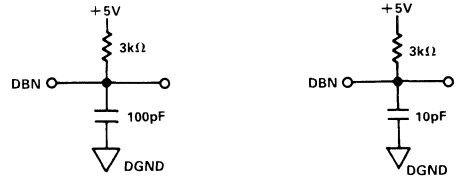
a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 3. Load Circuits for Access Time Tests (t_{12})



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 4. Load Circuits for Output Float Delay (t_{13})



a. High-Z to V_{OL} *b. V_{OL} to High-Z*

Figure 5. Load Circuit for $\overline{INT}$ Propagation Delays

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V to +7V
V_{DD} to DGND . . . . . +0.3V to +7V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND . . . −0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{REF} to AGND . . . . . −0.3V, V_{DD}
$V_{IN}(+)$A, $V_{IN}(+)$B to AGND
(Figure 12) . . . . . −0.3V, V_{DD} +0.3V
$V_{IN}(-)$A, $V_{IN}(-)$B to AGND
(Figure 12) . . . . . −0.3V, V_{DD} +0.3V
$V_{IN}(+)$A to AGND (Figure 14) . . . . . −0.6V, $2V_{DD}$ +0.6V
$V_{IN}(-)$A to AGND (Figure 14) . . . . . −0.6V, $2V_{DD}$ +0.6V
$V_{IN}(+)$A to AGND
(Figure 15) . . . . . $-V_{REF}$ −0.6V, $2V_{DD}$ $-V_{REF}$ +0.6V
$V_{IN}(-)$A to AGND
(Figure 15) . . . . . $-V_{REF}$ −0.6V, $2V_{DD}$ $-V_{REF}$ +0.6V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Industrial (A, B Versions) . . . . . −25°C to +85°C
Extended (S Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (soldering, 10sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates Above +75°C by . . . . . 6mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 10-bit resolution can resolve one part in 2^{10} (1/1024 of full scale). For the AD7579/AD7580 operating in the unipolar range with 2.5V span, one LSB is 2.44mV.

ZERO CODE ERROR

This is a measure of the difference between the ideal (0.5LSB) and the actual differential analog input level required to produce the first positive LSB code transition (00 . . . 00 to 00 . . . 01).

FULL-SCALE ERROR

The ideal difference between the first transition voltage and last transition voltage for an ADC is (F.S. − 2LSB). AD7579/AD7580 Full-Scale Error is defined as the deviation between this ideal difference and the measured difference.

COMMON-MODE RANGE

The voltage at both inputs to the AD7579/AD7580 can be raised above or lowered below analog ground potential, providing $V_{IN}(+)$ is equal to or more positive than $V_{IN}(-)$. Figures 12, 14, and 15 show circuits for various Analog Input Ranges. The Common-Mode Range represents the voltage extremes which can be applied to the circuits of Figure 12, 14 or 15. For example, when the AD7579/AD7580 is connected as in Figure 15, the Common-Mode Range is −2.5V to +7.5V.

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error. The Slew Rate performance of AD7579/AD7580 allows sampling of an input full-scale (2.5V pk-pk) sine wave up to 20kHz.

SIGNAL-TO-NOISE RATIO

Signal-to-Noise Ratio (SNR) is measured signal to noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine-wave input is given by:

$$SNR = (6.02N + 1.76)\ dB,$$

where N is the number of bits in the ADC. Thus for an ideal 10-bit ADC, SNR = 62dB.

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m,n = 0,1,2,3,----. Intermodulation terms are those for which m or n is not equal to zero.

HARMONIC DISTORTION

Harmonic distortion is the ratio of the square root of the sum-of-the-squares of the rms values of the harmonics to the rms value of the fundamental. For the AD7579/AD7580, Harmonic Distortion is:

$$20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}\ dB,$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6 are the rms amplitudes of the individual harmonics.

ORDERING INFORMATION[1, 2]

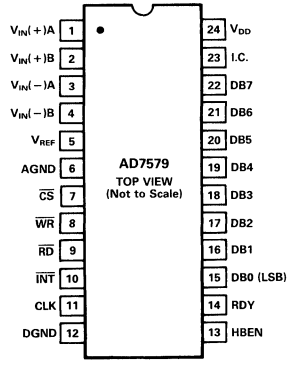
INL	Temperature Range and Package Options[3] Plastic DIP (N-24) 0 to +70°C	Hermetic DIP (Q-24) −25°C to +85°C	Hermetic DIP (Q-24) −55°C to +125°C	PLCC[4] (P-28A) 0 to +70°C	LCCC[5] (E-28A) −55°C to +125°C
±1LSB	AD7579JN	AD7579AQ	AD7579SQ	AD7579JP	AD7579SE
±1/2LSB	AD7579KN	AD7579BQ		AD7579KP	

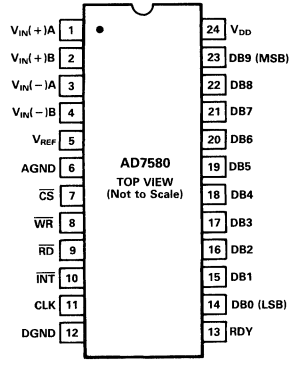
INL	Temperature Range and Package Options[3] Plastic DIP (N-24) 0 to +70°C	Hermetic DIP (Q-24) −25°C to +85°C	Hermetic DIP (Q-24) −55°C to +125°C	PLCC[4] (P-28A) 0 to +70°C	LCCC[5] (E-28A) −55°C to +125°C
±1LSB	AD7580JN	AD7580AQ	AD7580SQ	AD7580JP	AD7580SE
±1/2LSB	AD7580KN	AD7580BQ		AD7580KP	

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]Analog Devices reserves the right to ship ceramic (package outline D-24A) packages in lieu of cerdip (package outline Q-24) packages.
[3]See Section 14 for package outline information.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

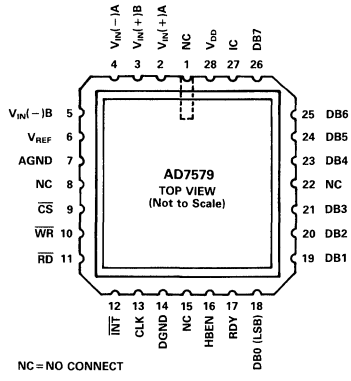
PIN CONFIGURATIONS

DIP

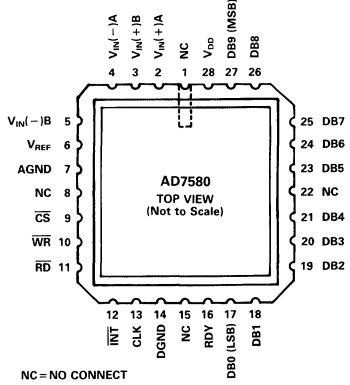




LCCC

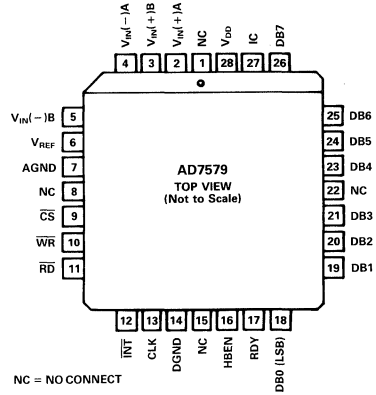


NC = NO CONNECT

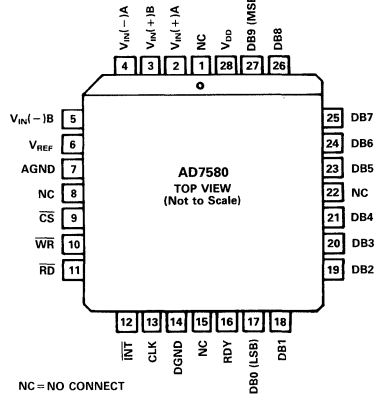


NC = NO CONNECT

PLCC



NC = NO CONNECT



NC = NO CONNECT

PIN FUNCTION DESCRIPTION (DIP PACKAGE)

Mnemonic	Pin Number AD7579	Pin Number AD7580	Description
$V_{IN}(+)A$	1	1	Analog Input Pin.
$V_{IN}(+)B$	2	2	Analog Input Pin.
$V_{IN}(-)A$	3	3	Analog Input Pin.
$V_{IN}(-)B$	4	4	Analog Input Pin. The four analog input pins connect to the on-chip input attenuator (see Figure 6) and may be configured as in Table I for various input ranges.
V_{REF}	5	5	V_{REF} Input. This is nominally +2.5V.
AGND	6	6	Analog Ground
$\overline{CS}$	7	7	Chip Select Input.
$\overline{WR}$	8	8	Write Input. Used with $\overline{CS}$ to start conversion. See Tables II, III.
$\overline{RD}$	9	9	Read Input. Used with $\overline{CS}$ to read data. See Tables II, III.
$\overline{INT}$	10	10	Open Drain Output. High impedance during conversion. Goes low when conversion is complete.
CLK	11	11	Clock Input.
DGND	12	12	Digital Ground.
HBEN	13	–	High Byte Enable Input. Used in AD7579 for 2 Byte Reading. See Tables II, IV. Either the High Byte or the Low Byte may be read first.
RDY	14	13	Open Drain Output. This is accessed during Read Cycle. When accessed, it is low during conversion and high impedance when conversion is complete.
DB0-DB7	15-22	–	Three-State Data Outputs on AD7579. The data format is right justified.
DB0-DB9	–	14-23	Three-State Data Outputs on AD7580.
I.C.	23	–	Internal connection. This pin is connected internally on the AD7579. It should be left open and not used as a feed-through pin in double-sided printed circuit boards.
V_{DD}	24	24	Positive Power Supply. This is +5V nominal.

Analog Input Range	Connections $V_{IN}(+)A$	$V_{IN}(+)B$	$V_{IN}(-)A$	$V_{IN}(-)B$	Analog Input Span	Common-Mode Range
Figure 12	$V_{IN}(+)$	$V_{IN}(+)$	$V_{IN}(-)$	$V_{IN}(-)$	2.5V	0V to +5V
Figure 14	$V_{IN}(+)$	AGND	$V_{IN}(-)$	AGND	5V	0V to +10V
Figure 15	$V_{IN}(+)$	V_{REF}	$V_{IN}(-)$	V_{REF}	5V	−2.5V to +7.5V

Table I. Analog Input Ranges

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	HBEN	Function
1	X	X	X	Not Selected
0	1	1	X	Selected, WAIT for $\overline{WR}$, $\overline{RD}$
0	↓	1	X	Start Conversion on ↓ of $\overline{WR}$
0	1	0	0	Enable ADC Data (8 LSBs)*
0	1	0	1	Enable ADC Data (2 MSBs)*

*Data is Right Justified.

Table II. AD7579 Truth Table

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Function
1	X	X	Not Selected
0	1	1	Selected, WAIT for $\overline{WR}$, $\overline{RD}$
0	↓	1	Start Conversion on ↓ of $\overline{WR}$
0	1	0	Enable ADC data (10 Bits)

Table III. AD7580 Truth Table

HBEN	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HIGH	$\overline{EOC}$*	0	0	0	0	0	DB9	DB8

*$\overline{EOC}$ is an internal End of Conversion flag.

Table IV. AD7579 Output Data Format

CIRCUIT INFORMATION

ANALOG INPUT CIRCUITRY

The AD7579 is a 10-bit ADC with an (8+2) output bus structure designed for 8-bit microprocessor systems. The AD7580 is a 10-bit ADC with a 10-bit parallel output bus structure. The ADC circuitry is identical in both parts. Block diagrams are shown on the first page of this data sheet.

Figure 6 shows the input circuitry to the ADC comparator. This comparator has differential inputs which are accessed through the attenuator networks made up of resistors R. The attenuators can be used to scale and offset analog input voltages, and this is done in Figures 14 and 15 to alter the basic ADC input range. The analog inputs to the comparator are differential with the provisos that V+ is always greater than or equal to V−, V− is greater than or equal to AGND and that V+ is less than or equal to V_{DD}. These conditions must be satisfied when using the ADC in any of the voltage ranges.

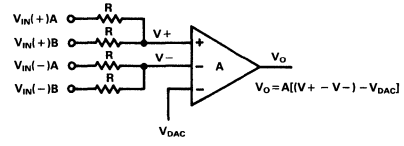


Figure 6. AD7579/AD7580 Input Circuit

Figure 7 shows an ac equivalent input circuit for the AD7579/AD7580 when used in the 2.5V Unipolar Mode of Figure 12. The ADC comparator is a sampled data comparator and the input circuitry for this is represented by S_A, Req and C_A. Req is a combination of the switch-on resistance and the input impedance of the comparator. When conversion starts, $V_{IN}(+)$ is sampled for at least ($2t_{CLK}$ + t_{WR} + 200ns) before the comparator goes into the hold mode. This means that the analog input has a minimum of 1.1μs (f_{CLK} = 2.5MHz, t_{WR} = 100ns) to settle before the comparator makes a decision. By using the typical values in Figure 7 for R, Req and C_A, the input time constant is 50ns. Settling to ±1/4LSB in a 10-bit system takes 8.3 time constants or 415ns in this case. This means that $V_{IN}(+)$ has plenty of time to settle before the ADC comparison cycle begins. It is important to remember that any source resistance or source capacitance appearing at the input will also increase the settling time and this should be kept to a minimum in all cases.

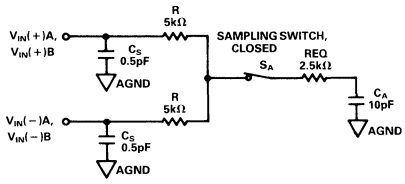


Figure 7. AD7579/AD7580 Equivalent Input Circuit During Sampling

With a 2.5MHz clock, the AD7579/AD7580 has a maximum conversion time of 18.5μs. If 1μs is allowed for reading the data outputs, the maximum sampling rate for the device is 50kHz. This means that the maximum analog input frequency is 25kHz according to the Nyquist theory. The ADC input impedance in the Unipolar Configuration of Figure 12 is 10MΩ. A medium bandwidth op amp will drive this at 25kHz. When the input attenuators are used for signal conditioning, the input impedance is 10kΩ. The drive requirements on the amplifier will now be greater but any errors resulting will be gain errors only. Suitable op amps for driving the AD7579/AD7580 in any of the input configurations are the AD711, AD OP-27, AD544. These will deliver specified device performance over the input bandwidth.

REFERENCE INPUT

The AD7579/AD7580 V_{REF} input is connected to the on-chip DAC. The input impedance of this is code dependent and the greatest variation occurs when the DAC resistors are at their lower limit. In this case, the impedance changes from 1.75kΩ to 5.25kΩ as the DAC is switched. To ensure that the error during conversion is less than 1/2LSB, the Reference output impedance should be less than 1Ω. References which satisfy this are the AD580 (shown in Figure 8) and the AD1403 from Analog Devices. If a trimmable reference such as the AD584 is used, it is possible to trim out the ADC full-scale error by adjusting the reference output.

INTERNAL SAMPLE-AND-HOLD

When an ADC without sample-and-hold is used to digitize ac signals, the analog input must not change by more than 1/2LSB during the conversion. This puts severe limitations on the allowable input signal bandwidth to such devices. A sample-and-hold amplifier must be used in front of the ADC if increased bandwidth is required. The charge balanced comparator used in the AD7579/AD7580 for the A/D conversion provides the user with an inherent sample-and-hold function. The ADC is specified to work with sampling rates up to 50kHz. This rate allows time to do a conversion and read the result into memory. Since at least two samples are needed to define an input sine wave according to the Nyquist theory, the analog input signal bandwidth for the AD7579/AD7580 is 25kHz. Figures 20, 21 and 22 show the performance of the ADC when digitizing ac signals.

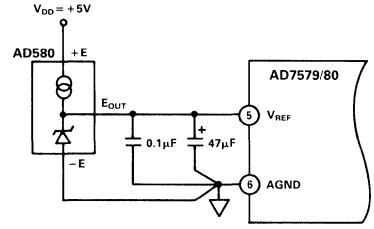


Figure 8. Using the AD580 as the Reference for the AD7579/AD7580

While the AD7579/AD7580 is converting, V+ (see Figure 6) is held and V− is being tracked. This limits the rate of change, $^{dv}/_{dt}$, on $V_{IN}(-)$. For example, if the Common-Mode frequency is 60Hz, then the allowable amplitude of this to introduce no more than 1/2LSB linearity error is 160mV pk-pk. As the Common-Mode frequency increases, this allowable amplitude decreases. Figure 9 shows how a 100mV pk-pk Common-Mode signal affects linearity error as its frequency is increased up to 1kHz.

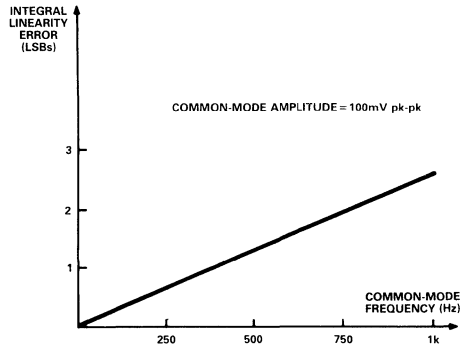


Figure 9. AD7579/AD7580 Error vs. Common-Mode Frequency

CLOCK INPUT

The AD7579/AD7580 is specified to operate with a 2.5MHz clock on the CLK input pin. This pin may be driven directly by CMOS or TTL buffers. The mark/space ratio on the clock can vary from 40/60 to 60/40. As the clock frequency is slowed down, it can result in slightly degraded accuracy performance. This is due to leakage effects on the hold capacitor in the internal sample-and-hold. Figure 10 is a typical plot of accuracy versus clock frequency for the ADC.

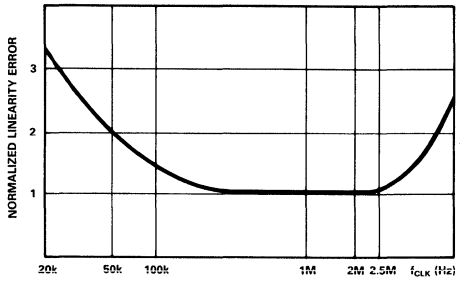


Figure 10. Normalized Linearity Error vs. Clock Frequency

FUNCTIONAL DESCRIPTION

Figure 11 shows the events sequence when the AD7579/AD7580 is converting. The device is selected when $\overline{CS}$ goes low and the first phase of conversion begins when $\overline{WR}$ goes low. This is an initializaton phase and causes the internal DAC to be set to full scale, comparators set to auto-zero and V+ (see Figure 6) to be sampled. The second phase begins some time after $\overline{WR}$ goes back high. This time can vary between 0 and 4 clock periods and depends on the state of an on-chip divide-by-4 counter which is used for internal synchronization. This is the start of the successive approximation procedure. V+ is held after 2-1/2 clock periods have elapsed. V− is sampled and the DAC output is switched into the comparator. There is (1-1/2 × t_{CLK}) left for comparison and then the MSB result is latched. The MSB test takes 4 clock cycles as do each of the succeeding bit tests. Thus, the successive approximation always takes 40 clock cycles.

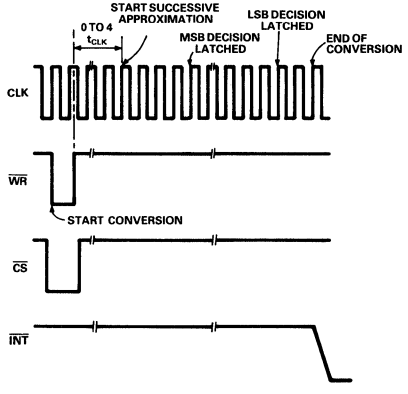


Figure 11. AD7579/AD7580 Conversion Sequence

When all the bits have been tested, the SAR holds a 10-bit word representing the input signal. After a further 2 clock cycles this is transferred to a three state output latch, and three internal flag bits (RDY, $\overline{INT}$, $\overline{EOC}$) are set. The user can access the data outputs by bringing $\overline{RD}$ and $\overline{CS}$ low. RDY and $\overline{INT}$ are both open drain outputs with RDY accessed by $\overline{RD}$ and $\overline{INT}$ being permanently available. When $\overline{INT}$ is loaded with the circuit of Figure 5(a), it typically takes 60ns to reach V_{OL}. $\overline{EOC}$ is only available on the AD7579 (see Table V). It appears on DB7, when reading the high Byte.

When the ADC is finished the conversion, the conditions of V+, V− and the comparators are maintained and the ADC is now ready to start a new conversion. If $\overline{WR}$ and CLK are asynchronous, the total time from start to end of conversion is variable. Minimum conversion time is (t_{WR} + 42 t_{CLK}), and maximum conversion time is (t_{WR} + 46 t_{CLK}).

APPLYING THE AD7579/AD7580

The AD7579/AD7580 has a flexible input stage consisting of two input attenuators. It is possible to realize various analog input ranges by reconfiguring these attenuators. The following diagrams show the ADC connected in the most popular configurations.

DIFFERENTIAL APPLICATIONS

Figure 12 shows the AD7579/AD7580 connected in the standard unipolar mode. Figure 13 and Table V show the ideal input/output

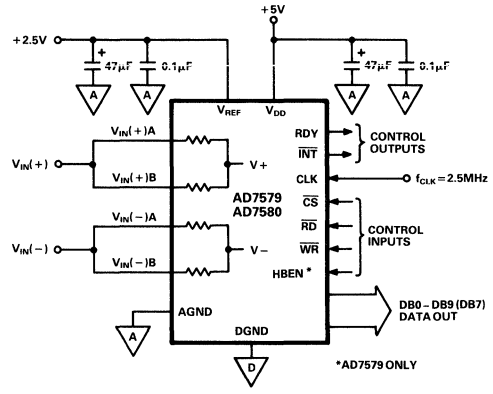


Figure 12. Unipolar 2.5V Operational Diagram

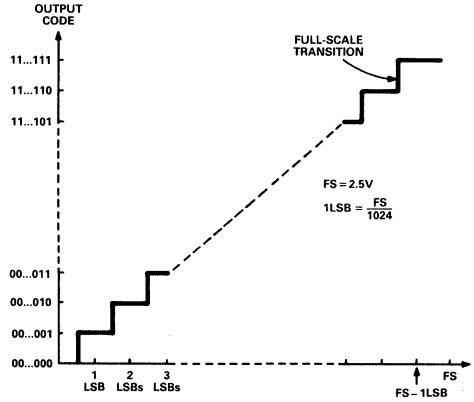


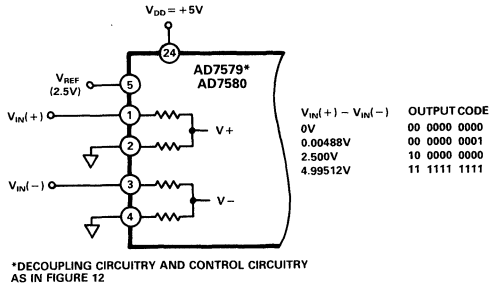
Figure 13. Ideal Input/Output Transfer Characteristic

Differential Analog Input, Volts	Digital Output DB9	DB0
+0.000	00 0000	0000
+0.00244	00 0000	0001
+1.24756	01 1111	1111
+1.25	10 0000	0000
+1.25244	10 0000	0001
+2.49512	11 1111	1110
+2.49756	11 1111	1111

Table V. Input/Output Code Table for Figure 12

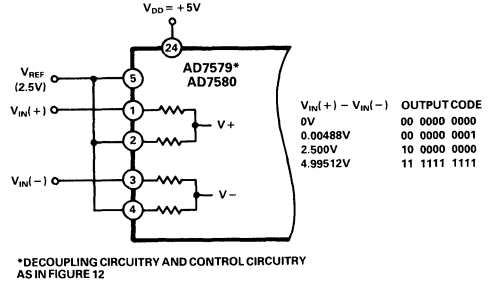
transfer characteristic and the input/output code table respectively. Code transitions occur between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, etc.). The output code is straight binary with 1LSB = FS/1024 = 2.5/1024V = 2.4mV. The input voltage span is 2.5V and the common-mode range is 0V to +5V, when V_{DD} = 5V. This means that the lowest voltage which can be tolerated at any of the analog inputs is 0V, and the highest voltage which can be tolerated is +5V.

Figures 14 and 15 show the input attenuators on the AD7579/AD7580 configured to change the basic range of the device. A 5V range can be configured by grounding one end of each attenuator and applying the differential input to the other ends. This is shown in Figure 14. The span is 5V and the common-mode range is 0 to +10V. In Figure 15, one end of each attenuator is tied to V_{REF} (2.5V), and this allows each of the other legs to go to −2.5V without causing the comparator input to go negative. Assuming V_{REF} is 2.5V, the span of this circuit is 5V and the common-mode range is −2.5V to +7.5V. Note that reducing V_{DD} below 5 volts causes a corresponding reduction in CMR. See Specifications page for full details.



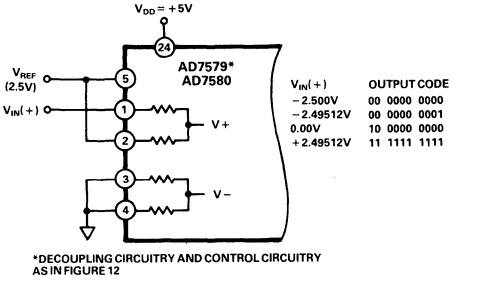
$V_{IN}(+) - V_{IN}(-)$	OUTPUT CODE
0V	00 0000 0000
0.00488V	00 0000 0001
2.500V	10 0000 0000
4.99512V	11 1111 1111

Figure 14. 5V Span with 0 to 10V CMR



$V_{IN}(+) - V_{IN}(-)$	OUTPUT CODE
0V	00 0000 0000
0.00488V	00 0000 0001
2.500V	10 0000 0000
4.99512V	11 1111 1111

Figure 15. 5V Span with −2.5V to +7.5V CMR



$V_{IN}(+)$	OUTPUT CODE
−2.500V	00 0000 0000
−2.49512V	00 0000 0001
0.00V	10 0000 0000
+2.49512V	11 1111 1111

Figure 16. Single-Ended Bipolar Operation, −2.5V to +2.5V

SINGLE-ENDED APPLICATIONS

In many cases, users of the AD7579/AD7580 will want to measure single-ended input voltages (i.e., ground referred signals). The circuits of Figures 12, 14 and 15 can be easily adapted to accept such signals. If $V_{IN}(-)$ in Figure 12 is tied to AGND, then the analog input range is 0V to +2.5V. By connecting $V_{IN}(-)$ of Figure 14 to AGND, the analog input range becomes 0V to +5V. Figure 15 can be modified as in Figure 16 to accept input voltages in the range −2.5V to +2.5V. Each of these circuits are special cases of the Differential Input circuits and are achieved by making the negative input to the internal comparator equal to AGND.

OFFSET AND FULL-SCALE ADJUSTMENT

Figure 17 shows the AD7579/AD7580 connected in the single-ended Unipolar 2.5V range with offset and full-scale calibration circuitry. The zero error of the ADC is the deviation of the actual LSB transition from the ideal LSB transition. In many cases, the zero of the ADC will not need adjustment. When it does, R1 in Figure 17 provides 25mV of adjustment which is sufficient to null out both the op amp and ADC offset error. Resistors R3 and R4 bias $V_{IN}(-)$ to approximately 8mV and ensure that the offset error is never positive. This allows the error to be nulled in the single supply system of Figure 17. Apply +0.5LSB to V_{IN} and adjust R1 until the ADC output code flickers between 00 ..... 000 and 00 ..... 001.

For full-scale calibration, apply a voltage of (2.5V − 1.5LSB) to V_{IN}. Then adjust R2 until the output code flickers between 11 ..... 110 and 11 ..... 111. When the full-scale calibration is complete, return to the offset adjustment procedure and check that further adjustment is not necessary.

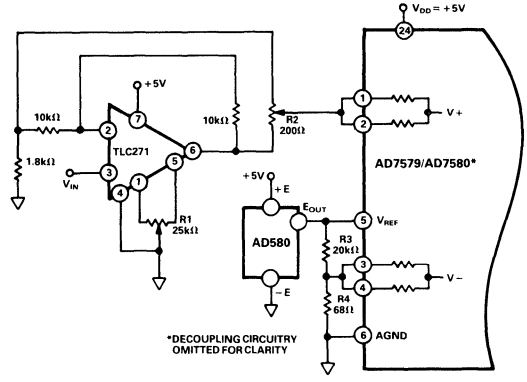


Figure 17. Offset and Full-Scale Calibration for Single-Ended Circuit

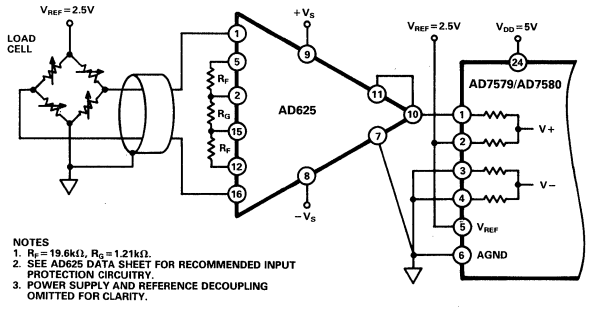


Figure 18a. AD7579/AD7580 and AD625 in a Data Acquisition System

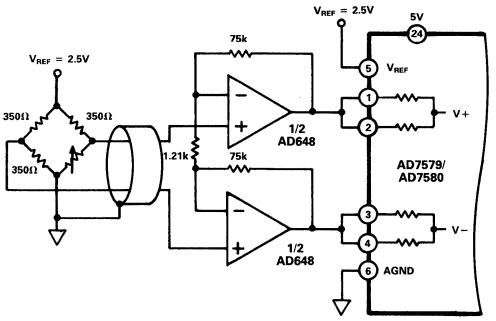


Figure 18b. AD7579/AD7580 and AD648 in a Data Acquisition System

AD7579/AD7580 IN DATA ACQUISITION SYSTEMS

The AD7579/AD7580 is suitable for many data acquisition circuits. Figure 18a shows one such circuit in which a load cell is used to produce a signal in response to an applied force. Typically these transducers produce 30mV full scale per volt of excitation. Since the excitation in this case is 2.5V, the output from the load cell is ±75mV when the maximum specified force is applied. The AD625 Instrumentation Amplifier is set for a gain of 33.33 which means that the input signal to the ADC is ±2.5V. Thus, the AD7579/AD7580 is configured in the single-ended, ±2.5V range of Figure 16. When no force is applied to the load cell, the ADC output will sit at mid-scale. With maximum negative force applied the ADC output will be all zeros; whereas, with maximum positive force the output will be all 1s. Offset and gain calibration of this system can be accomplished by trimming the offsets and gain of the instrumentation amplifier.

Figure 18b shows a differential transducer unbalanced by ≈10Ω supplying a 0 to 20mV maximum signal. The resistors are chosen for a gain of 125, and the ADC is configured to accept 0 to 2.5V differential signal. This is a lower-cost alternative to using an instrumentation amplifier.

Note that in the circuits of Figure 18, V_{REF} for the ADC and the excitation voltage for the load cell are both +2.5V. If the same reference drives both these points, then the ADC operation is ratiometric which eliminates system errors due to reference drift. The main reason why the same reference would not be used to drive both load cell and ADC is physical location. When the load cell is remote from the ADC circuitry, it might not be practical to have the same drive for both circuits.

APPLICATIONS HINTS

Layout: To obtain the best performance from the AD7579/AD7580, lay it out on a printed circuit board. Digital and analog lines on the board should be separated as much as possible. In particular, take care not to run any digital track adjacent to an analog signal track or underneath the AD7579/AD7580. The analog inputs should be screened by AGND.

Grounding: Establish a single-point analog ground (STAR ground) at Pin 6 (AGND) or as close as possible to the AD7579/AD7580. This is shown in Figure 19. Pin 12 (AD7579/AD7580 DGND) and all other analog grounds should be connected to this single analog ground point. However, do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply returns are essential to low noise operation of the ADC and these tracks should be kept as wide as possible.

Noise: Input signal leads to $V_{IN}(+)A$, $V_{IN}(+)B$, $V_{IN}(-)A$, $V_{IN}(-)B$ and signal return leads from AGND (Pin 6) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible a shielded cable between source and ADC is recommended.

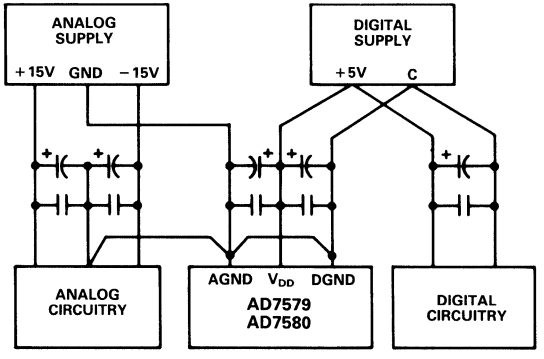


Figure 19. Power Supply Grounding Practice

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (SNR, Harmonic Distortion, Intermodulation Distortion) of ADCs are critical. For this reason, the AD7579/AD7580 is specified dynamically as well as with standard D.C. specifications (linearity error, offset error, etc.).

Figure 20 shows a 2048 point FFT plot of an AD7579/AD7580 with an input signal of 3.58kHz. The SNR is 60.1dBs. The largest harmonic appears at $2f_O$ (7.16kHz) and is 70dB down from the fundamental. Harmonics above $3f_O$ are in the noise floor. Note that when SNR is calculated, it includes harmonics.

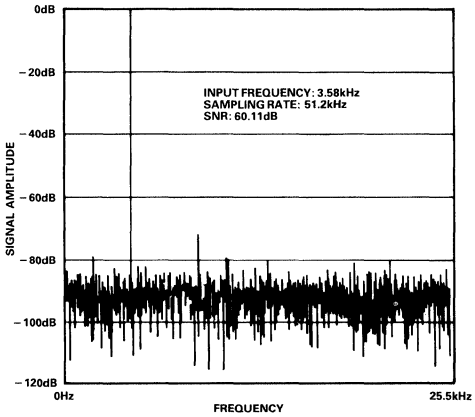


Figure 20. AD7579/AD7580 Spectral Response

If these were excluded the SNR figure would be closer to the ideal of 62dB for a 10-bit ADC. The relationship between Signal-to-Noise Ratio (SNR) and ADC resolution is expressed in the following equation:

$$SNR = (6.02N + 1.76)dB$$

This is for an ideal ADC with no differential or integral linearity errors. These errors will cause a degradation in SNR. By working backwards in the above equation it is possible to get a measure of ADC performance expressed in effective number of bits. This is shown over frequency in Figure 21 for the AD7579/AD7580. The effective number of bits typically falls between 9.7 and 9.8 corresponding to SNRs of 60.0 and 60.6dBs.

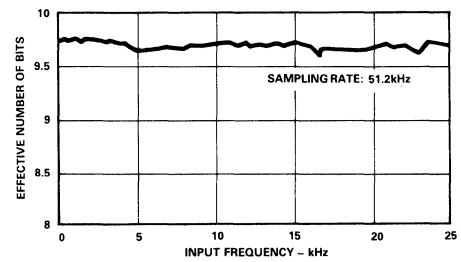


Figure 21. AD7579/AD7580 Effective Number of Bits

When a sine wave of specified frequency is applied to the AD7579/AD7580 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of 1024 ADC codes. A perfect ADC would produce a cusp probability density function described by the equation

$$p(V) = \frac{1}{(A^2 - V^2)^{1/2}}$$

A is the peak amplitude of the sine wave and p(V) the probability of occurrence at the voltage V. If a particular step is wider than the ideal width, then the code associated with that step will accumulate more counts than the code for an ideal step. Likewise, a step narrower than ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the histogram indicates small differential nonlinearity. The actual histogram obtained is shown in Figure 22 and corresponds very well with the ideal cusp shape. It shows that the AD7579/AD7580 has very small differential nonlinearity and no missing codes with an input frequency of 25kHz.

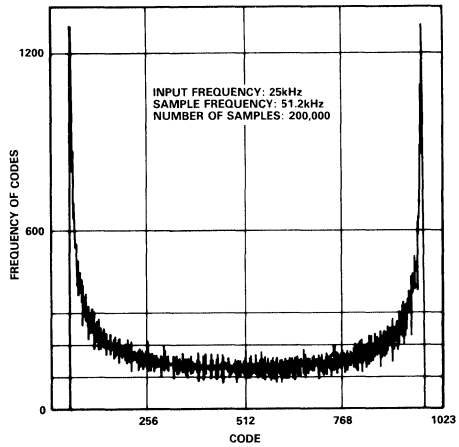


Figure 22. Histogram Plot for AD7579/AD7580

Whenever the AD7579/AD7580 is used to sample ac signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. The $\overline{WR}$ command for the AD7579/AD7580 needs to be synchronized with the CLK input to ensure equal interval sampling.

Two conditions must be satisfied to ensure proper synchronization: 1) The time interval between successive $\overline{WR}$ signals needs to be long enough to allow a conversion to finish and the data to be read into memory. 2) Because of the internal operation of the ADC, the number of clock pulses between successive write signals must be a multiple of four.

The conversion time for the AD7579/AD7580 has a maximum value of (t_{WR} + 46 t_{CLK}). If 4 t_{CLK} is allowed for reading the data outputs into a buffer then the interval between successive $\overline{WR}$ signals must be at least 50 t_{CLK}. The easiest way to satisfy both this requirement and number 2 above is to divide f_{CLK} by 64 to produce the $\overline{WR}$ signal. Alternatively, if a programmable timer/counter on a processor board is available, then it will be possible to easily divide f_{CLK} by 52.

MICROPROCESSOR INTERFACING

Reading Data

Conversion is started in the AD7579/AD7580 by bringing $\overline{WR}$ low. It is recommended that the user wait until conversion is complete before reading data. This can be achieved in any of the following ways:

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. Use the externally available $\overline{INT}$ signal to interrupt the microprocessor. This is an open drain output which goes low at the end of conversion.
3. On the AD7579, it is possible to interrogate the $\overline{EOC}$ status flag (See Table IV) to determine when conversion is complete. Reading may then proceed.

MC68000 Interface

Figure 23 shows an interface diagram for the AD7580 and the MC68000. The address decoding means that the AD7580 is a memory mapped device. For example, if the AD7580 is memory mapped as address COOOH, then a write instruction to this address will start a conversion, i.e.,

MOVE.W DO COOO

starts a conversion. When the conversion is complete, the MC68000 acquires the result by reading from COOOH, i.e.,

MOVE.W COOO, DO.

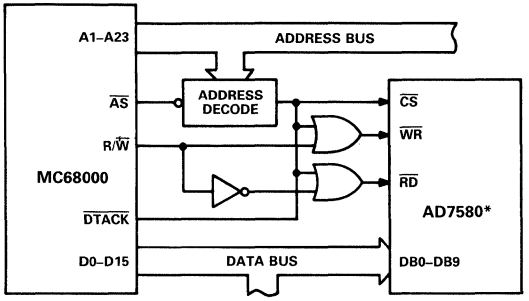


Figure 23. MC68000 to AD7580 Interface

8088 Interface

The AD7579, with its (8 + 2) data format, is ideal for use with the 8088 microprocessor. Figure 24 is the interface diagram. Again, a write instruction is required to start a conversion and a read at the end of conversion reads data into the processor. For the 8088 the appropriate instructions are:

MOV COOO, AX	Start a conversion
MOV AX, COO1	Read 2 MSBs of data
MOV AX, COOO	Read 8 LSBs of data

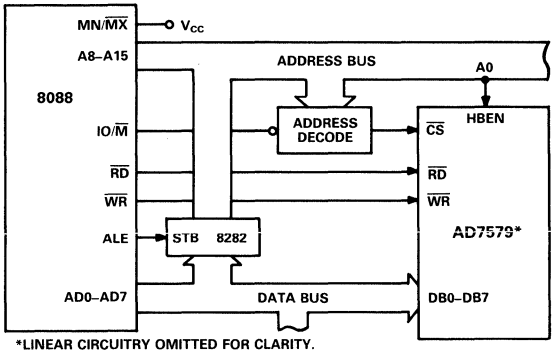


Figure 24. 8088 to AD7579 Interface

TMS32020 Interface

Figure 25 shows the AD7580 to TMS32020 interface. OUTA,PA starts a conversion and INA,PA reads data from the ADC when conversion is complete. PA is the Port Address.

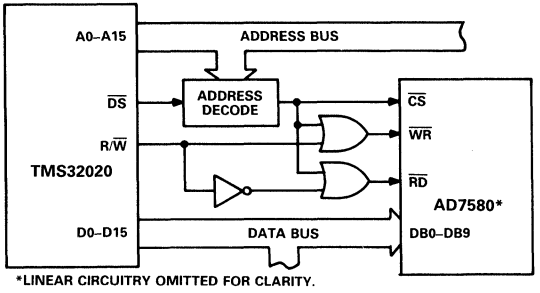


Figure 25. TMS32020 to AD7580 Interface

PRINTED CIRCUIT BOARD LAYOUT

Figure 26 is a circuit diagram showing the AD7579 or AD7580 being used to digitize an analog signal. The circuit board contains the ADC, reference, and a grid where the user can add additional circuitry. If the AD7580 is used, then links L6 and L8 should be inserted; and if AD7579 is used, L7 should be inserted with L6 and L8 omitted. Note that Pins 13 to 23 are not labelled. Depending on which ADC is used the function of these pins changes. See the Pin Function Description section for full details.

Links L1 to L5 at the analog input allow the user to choose various analog input ranges. With L1, L2 and L3 in place and the others omitted, the input range is 0V to +2.5V. Omitting L3 allows the user to measure input voltages which have a common-mode signal. The 0V to +5V range is achieved by inserting L2, L3 and L4 and omitting L1 and L5. With L2, L3 and L5 in place and L1, L4 omitted, the Analog input range is −2.5V to +2.5V.

IC2 (AD580) provides the +2.5V reference for the ADC. All the input and output control signals enter and leave the board through J1, which can be a Eurocard connector or a standard edge connector. Resistors R1 and R2 are the pull-ups required for the RDY and $\overline{INT}$ open-drain outputs. Note that the complete circuit operates from a +5V power supply.

The printed circuit board layout is shown in Figures 27 and 28. Figure 27 is the component side layout and Figure 28 is the solder side layout. The component overlay is shown in Figure 29.

In the layout, the AD580 is kept as close to the AD7579/AD7580 as possible. The STAR ground point is located at Pin 6 (AGND) of the ADC. Pin 12 (DGND), reference ground and the analog ground plane are connected to this point.

To ensure optimum performance, the AD7579/AD7580 power supply is decoupled with C1 and C2. The V_{REF} input to the ADC is decoupled with C3 and C4. Note how all the decoupling capacitors are placed as close as possible to the ADC.

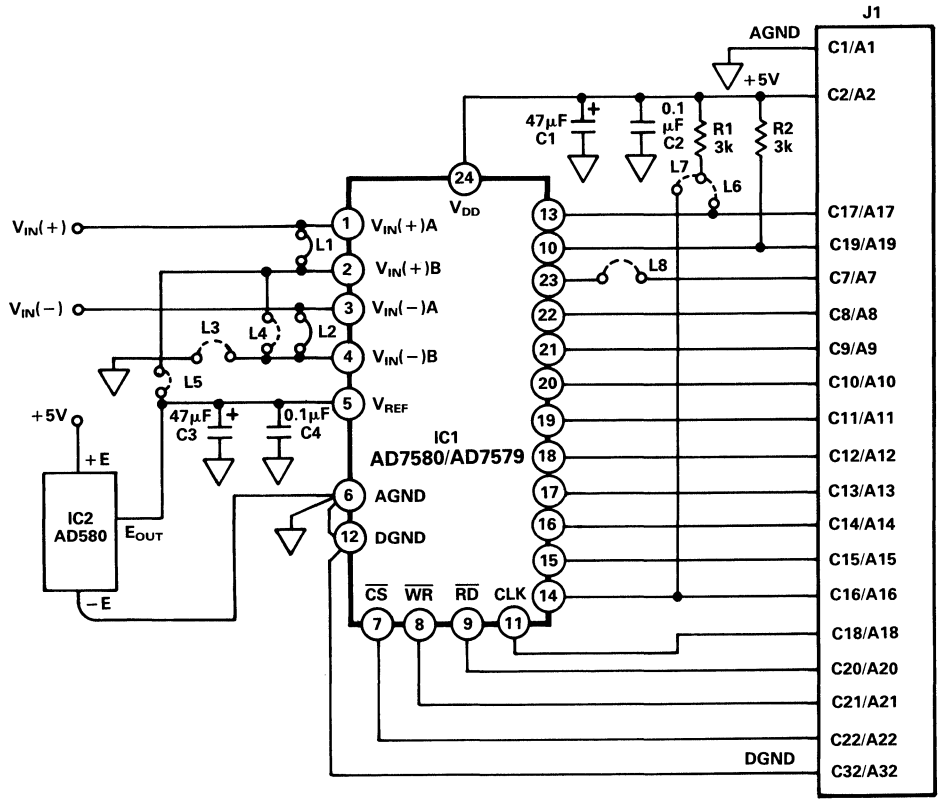


Figure 26. Schematic for AD7579/AD7580 Board

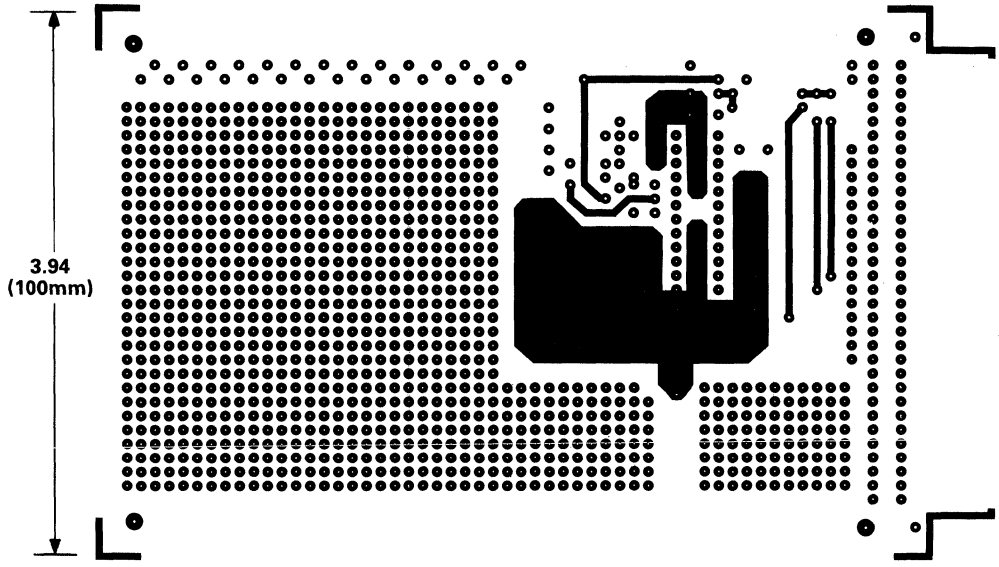


Figure 27. PCB Component Side Layout for Figure 26

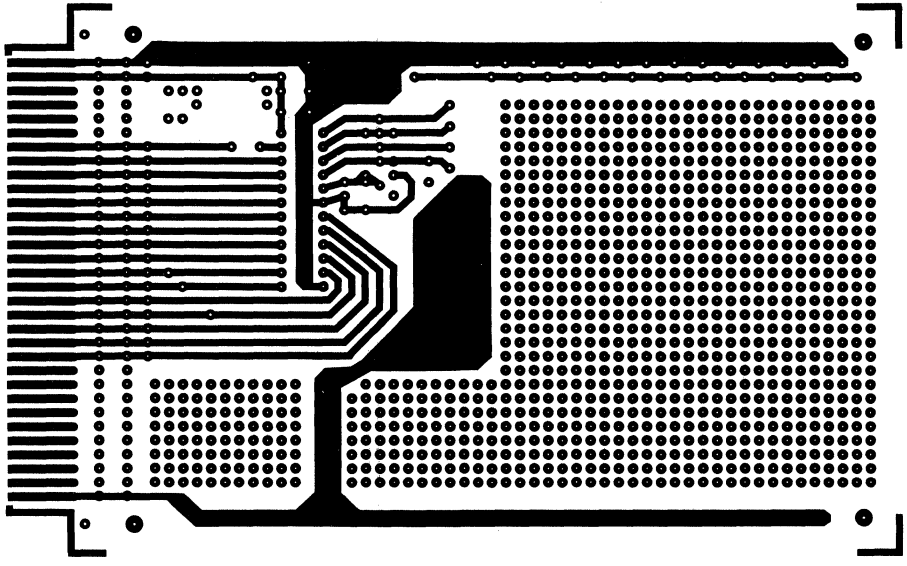


Figure 28. PCB Solder Side Layout for Figure 26

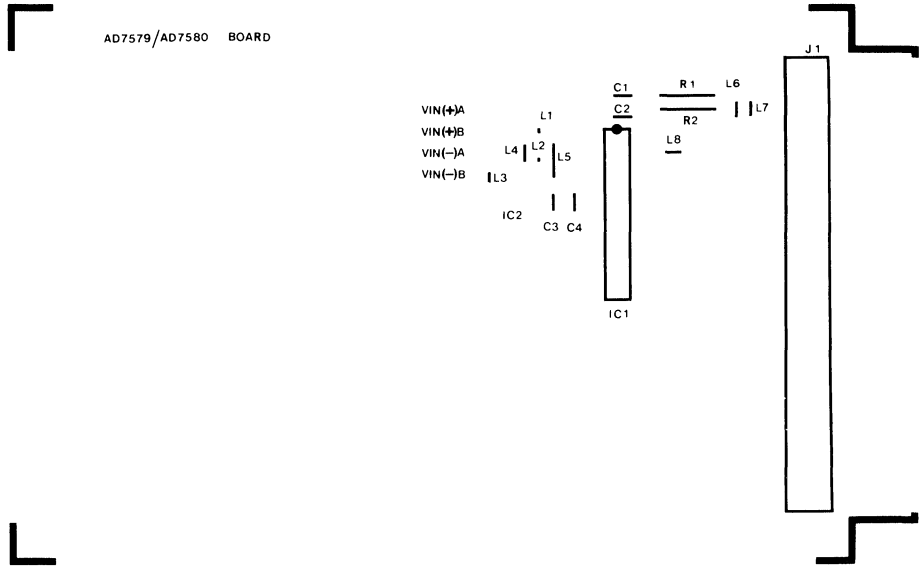


Figure 29. Component Overlay for Circuit of Figure 26

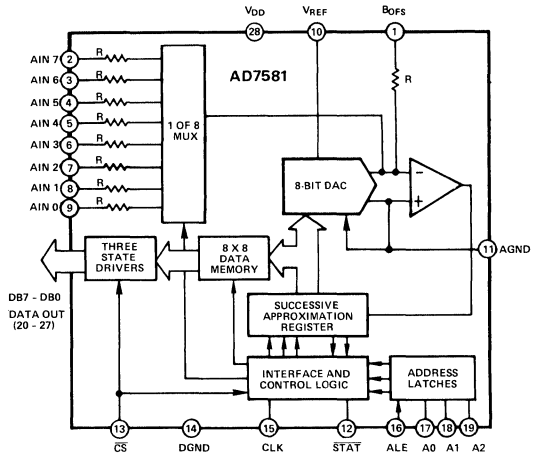
CMOS µP-Compatible 8-Bit, 8-Channel DAS

AD7581

FEATURES

- 8-Bit Resolution
- On-Chip 8 X 8 Dual-Port Memory
- No Missed Codes Over Full Temperature Range
- Interfaces Directly to Z80/8085/6800
- CMOS, TTL Compatible Digital Inputs
- Three-State Data Drivers
- Ratiometric Capability
- Interleaved DMA Operation
- Fast Conversion
- A/D Process Totally Transparent to µP
- Low Cost

AD7581 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7581 is a microprocessor compatible 8 bit, 8 channel, memory buffered, data-acquisition system on a monolithic CMOS chip. It consists of an 8 bit successive approximation A/D converter, an 8 channel multiplexer, 8 X 8 dual-port RAM, three-state DATA drivers (for interface), address latches and microprocessor compatible control logic. The device interfaces directly to 8080, 8085, Z80, 6800 and other microprocessor systems.

The successive approximation conversion takes place on a continuous, channel sequencing, basis using microprocessor control signals for the clock. Data is automatically transferred to its proper location in the 8 X 8 dual-port RAM at the end of each conversion. When under microprocessor control, a READ DATA operation is allowed at any time for any channel since on-chip logic provides interleaved DMA. The facility to latch the address inputs (A_0 - A_2) with ALE enables the AD7581 to interface with µP systems which feature either shared or separate address and data buses.

ORDERING INFORMATION

Differential Nonlinearity	Temperature Range and Package Options*	
	Plastic (N-28) 0 to +70°C	Hermetic (D-28) -25°C to +85°C
±1 7/8LSB	AD7581JN	AD7581AD
±7/8LSB	AD7581KN	AD7581BD
±3/4LSB	AD7581LN	AD7581CD

*See Section 14 for package outline information.

DC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = −10V, Unipolar Operation, unless otherwise stated)

Parameter	Version[1]	Typical at +25°C	Limit Over Temperature	Units	Conditions/Comments
ACCURACY					
Resolution	All	8	8	Bits	
Relative Accuracy	JN, AD	±1 7/8	±1 7/8 max	LSB	
	KN, BD	±3/4	±3/4 max	LSB	
	LN, CD	±1/2	±1/2 max	LSB	
Differential Nonlinearity	JN, AD	±1 7/8	±1 7/8 max	LSB	
	KN, BD	±7/8	±7/8 max	LSB	
	LN, CD	±3/4	±3/4 max	LSB	
Offset Error[2]	JN, AD	200	200 max	mV	Adjustable to zero, see Figure 7a.
	KN, BD	80	80 max	mV	
	LN, CD	50	50 max	mV	
Gain Error					
Worst Channel	JN, AD	±3	±6 max	LSB	Adjustable to zero, see Figure 7a.
	KN, BD	±2	±4 max	LSB	Gain Error is Measured After Offset
	LN, CD	±1	±2 max	LSB	Calibration. Max Full Scale Change for Any Channel from +25°C to T_{min} or T_{max} is ±2LSB.
Gain Match Between Channels	JN, AD	2	3 max	LSB	Adjustable to zero, see Figure 7a.
	KN, BD	1 1/2	2 max	LSB	
	LN, CD	1	1 max	LSB	
B_{OFS} Gain Error	All	−2 1/2	—	LSB	
ANALOG INPUTS					
Input Resistance					
At V_{REF} (pin 10)	All	10/20/30	10/20/30	kΩ min/typ/max	
At B_{OFS} (pin 1)[3]	All	10/20/30	10/20/30	kΩ min/typ/max	
At Any Analog Input (pins 2–9)	All	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (For Specified Performance)	All	−10	−10	V	±5%
V_{REF} Range[4]	All	−5 to −15	−5 to −15	V	
Nominal Analog Input Range					
Unipolar Mode	All	0 to $+V_{REF}$, 0 to $-V_{REF}$	0 to $+V_{REF}$ 0 to $-V_{REF}$	V V	See Figure 7 and 8.
Bipolar Mode	All	$-VB_{OFS} \leq VA_{IN} \leq \lvert V_{REF} \rvert - VB_{OFS}$			See Figure 9
DIGITAL INPUTS					
$\overline{CS}$ (pin 13), ALE (pin 16), A_0 – A_2 (pins 17–19), CLK (pin 15)					
V_{INH} Logic HIGH Input Voltage	All	+2.2	+2.4 min	V	
V_{INL} Logic LOW Input Voltage	All	+1.2	+0.8 max	V	
I_{IN} Input Current	All	0.01	1 max	μA	V_{IN} = 0V, V_{DD}
C_{IN} Input Capacitance[5]	All	4	5 max	pF	
DIGITAL OUTPUTS					
$\overline{STAT}$ (pin 12), DB_7 to DB_0 (pins 20–27)					
V_{OH} Output HIGH Voltage	All	+4.8	+4.5 min	V	I_{SOURCE} = 40μA
V_{OL} Output LOW Voltage	All	+0.4	+0.6 max	V	I_{SINK} = 1.6mA
I_{LKG} DB_7 to DB_0 Floating State Leakage	All	0.3	10 max	μA	
Floating State Output Capacitance (DB_7 – DB_0)	All	5	10 max	pF	V_{OUT} = 0V to V_{DD}
Output Code	All	Unipolar Binary Figure 7 Complementary Binary Figure 8 Offset Binary Figure 9			
POWER REQUIREMENTS					
V_{DD}	All	+5	+5	V	
I_{DD} – Static	All	3 typ	5 max	mA	
I_{DD} – Dynamic	All	3 typ	8 max	mA	f_{CLK} = 1MHz

NOTES
[1] Temperature range as follows: JN, KN, LN (0 to +70°C), AD, BD, CD (−25°C to +85°C).
[2] Typical offset temperature coefficient is ±150μV/°C.
[3] R_{BOFS}/R_{AIN} (0–7) mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 8a, and Figure 9a.
[4] Typical value, not guaranteed or subject to test.
[5] Guaranteed but not tested.
[6] Typical change in B_{OFS} gain from +25°C to T_{min} or T_{max} is ±2LSBs.
Specifications subject to change without notice.

AC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = −10V, Unipolar Operation, unless otherwise stated)

Symbol	Specification	Typical at +25°C	Limit Over Temperature	Units	Conditions
t_H	ALE pulse width	50	80 min	ns	See "Switching Terminology"
t_{ALS}	Address valid to latch set-up time	45	70 min	ns	on page 5
t_{ALH}	Address valid to latch hold time	10	20 min	ns	
t_{LCS}	Address latch to $\overline{CS}$ set-up time	10	20 min	ns	
t_{ACC}	$\overline{CS}$ to output propagation delay	200	250 max	ns	C_L = 100pF
t_{CW}	$\overline{CS}$ pulse width	250	280 min	ns	
t_{CF}	$\overline{CS}$ to output float propagation delay	50	80 max	ns	
t_{CLZ}	$\overline{CS}$ to low impedance bus	100	150 max	ns	
f_{CLK}	Clock frequency for stated accuracy	1600	1200 max[1]	kHz	

[1] Guaranteed conversion time of 66.6μs/channel with 1200kHz clock.

3

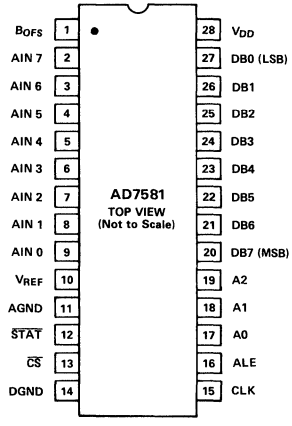
ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND . . . . . +7V
V_{DD} to DGND . . . . . +7V
AGND to DGND . . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND
(Pins 13, 16–19) . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND
(Pins 12, 20–27) . . . . . −0.3V, V_{DD} +0.3V
CLK (Pin 15) Input Voltage to DGND . −0.3V, V_{DD} +0.3V
V_{REF} (Pin 10) to AGND . . . . . ±25V
V_{BOFS} (Pin 1) to AGND . . . . . ±17V
AIN (0–7)(Pin 9–2) . . . . . ±17V
Operating Temperature Range
JN, KN, LN . . . . . 0 to +70°C
AD, BD, CD . . . . . −25°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C
Power Dissipation (Any Package)
to +75°C 1,000mW
Derate above +75°C by . . . . . 10mW/°C

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



GENERAL CIRCUIT INFORMATION

BASIC CIRCUIT DESCRIPTION

The AD7581 accepts eight analog inputs and sequentially converts each input into an eight-bit binary word using the successive approximation technique. The conversion results are stored in an 8 X 8 bit dual-port RAM. The device runs either directly from the microprocessor clock (in 6800 type systems) or from some suitable signal (e.g. ALE in 8085 type systems). Most applications require only a -10V reference and a +5V supply. Start-up logic is included on the device to establish the correct sequences on power-up. A maximum of 800 clock pulses are required for this period. Figure 1 shows the AD7581 functional diagram.

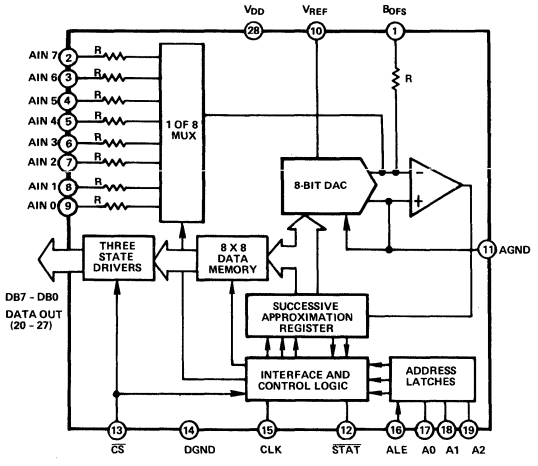


Figure 1. AD7581 Functional Diagram

Conversion of a single channel requires 80 input clock periods and a complete scan through all channels requires 640 input clock periods. When a channel conversion is complete, the successive approximation register contents are loaded into the proper channel location of the 8 X 8 RAM. At this time a status signal output, $\overline{STAT}$ (pin 12), gives a short negative going pulse (8 clock periods). This negative going $\overline{STAT}$ pulse is extended to 72 clock periods when channel 1 conversion is complete. An external pulse-width detector connected to the status pin can be used to derive conversion-related timing signals for microprocessor interrupts (see Channel Identification opposite page). Simultaneous with $\overline{STAT}$ going low, the MUX address is decremented. Eight clock periods later the next conversion is started.

Automatic interleaved DMA is provided by on-chip logic to ensure that memory updates take place at instants when the microprocessor is not addressing memory. Memory locations are addressed by A_0, A_1 and A_2. This address may be latched by ALE for systems which feature a multiplexed address/data bus or alternatively, for systems which have separate address and data buses, the address latches can be made transparent by tying ALE (pin 16) HIGH. $\overline{CS}$ (pin 13) activates three-state buffers to place addressed data on the DB_0 - DB_7 data output pins.

A/D CIRCUIT DETAILS

In the successive approximation technique, successive bits, starting with the most significant bit (DB_7), are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage, A_{IN} (n), using a comparator. If the DAC output is greater than A_{IN}(n), the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than A_{IN}(n), the trial data bit stays in the "1" state, and the next smaller data bit is tried. Each successive bit is tried, compared to A_{IN}(n), and set or reset in this manner until the least significant bit (DB_0) decision is made. The successive approximation register now contains a valid digital representation of A_{IN}(n). A_{IN}(n) is assumed to be stable during conversion.

The current weighting D/A converter is a precision multiplying DAC. Figure 2 shows the functional diagram of the DAC as used in the AD7581. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted i.e., the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the D/A logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to A_{GND} or to the comparator summing point.

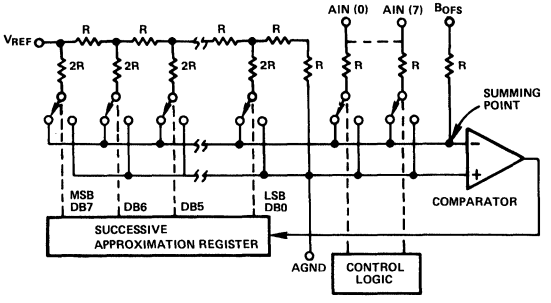


Figure 2. D/A Converter as Used in AD7581

TIMING AND CONTROL OF THE AD7581

CHANNEL SELECTION

Table I shows the truth table for the address inputs. The input address is latched when ALE goes LOW. When ALE is HIGH the address input latch is transparent.

A2	A1	A0	ALE	Channel Data To Be Read
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Table I. Channel Selection Truth Table

TIMING AND CONTROL

A typical timing diagram is shown in Figure 3. When $\overline{CS}$ is HIGH, the three-state data drivers are in the high-impedance state. When $\overline{CS}$ goes LOW the data drivers switch to the low-impedance state (i.e., low impedance to DGND or to V_{DD}). Output data is valid after time t_{ACC}.

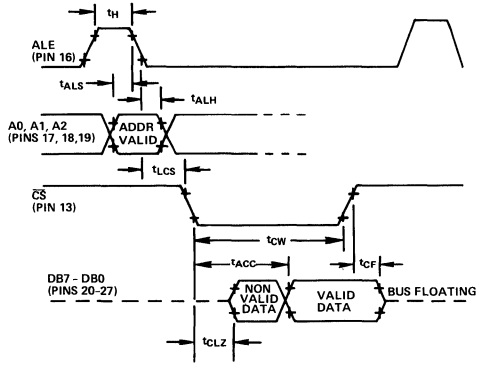


Figure 3. Timing Diagram for the AD7581

SWITCHING TERMINOLOGY

t_H: ALE pulse width requirement.
t_{ALH}: Address Valid to latch hold time.
t_{ALS}: Address Valid to latch set-up time.
t_{LCS}: Address latch to Chip Select set-up time.
t_{CW}: Chip Select pulse width requirement.
t_{ACC}: Chip Select to valid data propagation delay.
t_{CF}: Chip Select to output data float propagation delay.
t_{CLZ}: Chip Select to low impedance data bus.

CHANNEL IDENTIFICATION

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To achieve this, it is necessary to identify which channel is currently under conversion. The $\overline{STAT}$ output provides an identifying signal by staying low for an additional 64 clock periods over normal (8 clock periods) when channel 0 is active. This is illustrated in Figure 4. Memory update takes place on a rising edge of a clock pulse and is completed in 200ns. This occurs 6 clock periods before $\overline{STAT}$ goes low.

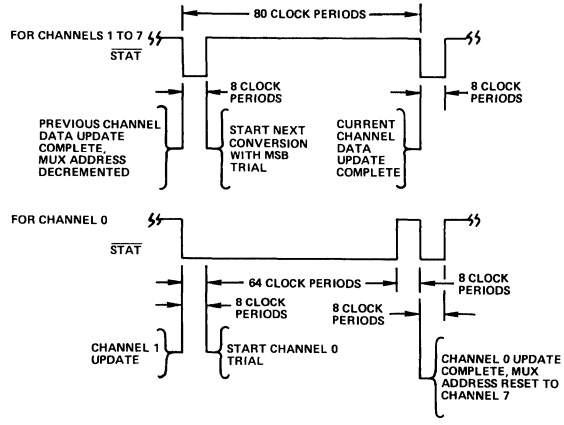


Figure 4. $\overline{STAT}$ Output for Channel Identification

One simple circuit using the $\overline{STAT}$ output is shown in Figure 5. The time constant RC is chosen such that X_2 ignores the normal $\overline{STAT}$ low pulse width (8 clock periods wide) but respond to the much wider $\overline{STAT}$ low pulse width (72 clock periods wide) occurring during channel 0 conversion. Typically for a 1μs clock period C = 0.022μF, R = 1.8kΩ.

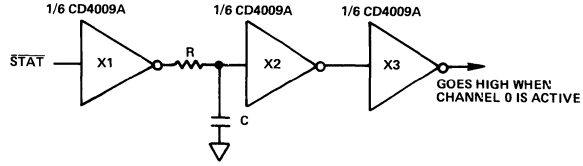


Figure 5. Hardware Channel Identification

Another possibility is to use the microprocessor to interrogate the $\overline{STAT}$ output and hence determine channel identity. A simple routine is shown in Figure 6.

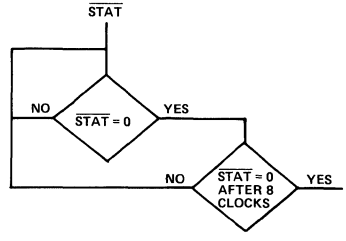


Figure 6. Software Channel Identification

OPERATING THE AD7581

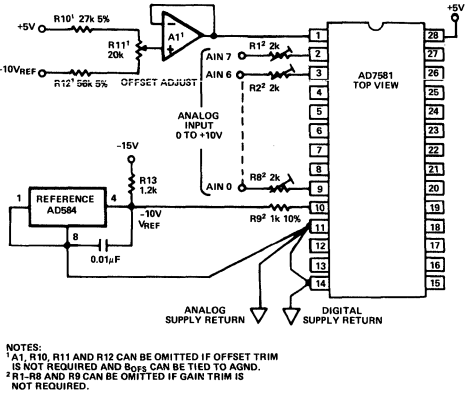
UNIPOLAR BINARY OPERATION

Figures 7a and 7b show the analog circuit connections and typical transfer characteristic for unipolar operation (0V to +10V). An AD584 is used for the -10V reference. Calibration is as follows (device clocked i.e., continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A_0, A_1 and A_2 LOW and and exercise ALE to latch the address.
2. With AIN 0 = 19.5mV (1/2LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until $DB_7 - DB_1$ are LOW and DB_0 (LSB) flickers.



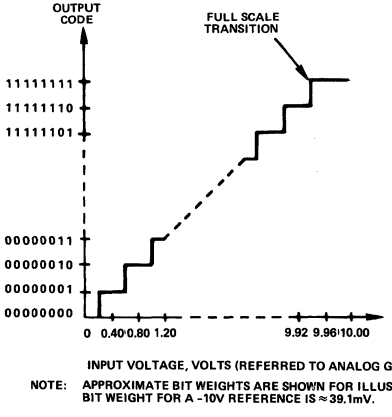
NOTES:
[1]A1, R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED AND B_{OFS} CAN BE TIED TO AGND.
[2]R1-R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.

Figure 7a. AD7581 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1. Apply +9.941V (FS - 3/2LSB) to all input channels AIN (0-7).



NOTE: APPROXIMATE BIT WEIGHTS ARE SHOWN FOR ILLUSTRATION. BIT WEIGHT FOR A -10V REFERENCE IS ≈39.1mV.

Figure 7b. Transfer Characteristic for Unipolar Circuit of Figure 7a

2. Select required channel n via A_0, A_1, A_2 and latch the Address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.

UNIPOLAR (COMPLEMENTARY BINARY) OPERATION

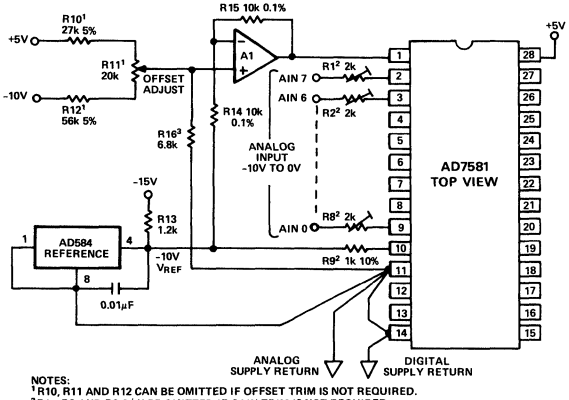
Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar (complementary binary) operation.

Calibration is as follows (continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A_0, A_1 and A_2 LOW and exercise ALE to latch the address.
2. With AIN 0 = -9.98V (-FS + 1/2LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.



NOTES:
[1]R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED.
[2]R1 - R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.
[3]R16/R10/R12 = 5kΩ. IF R10, R11 AND R12 ARE NOT USED, MAKE R16 = 5kΩ.

Figure 8a. AD7581 (0V to -10V) Operation (Output Code is Complementary Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1) Apply -58.6mV (3/2LSB) to all input channels AIN (0-7).
2) Select required channel n via A_0, A_1, A_2 and exercise ALE to latch the address.
3) Adjust trimmer RN of selected channel until $DB_7 - DB1$ are HIGH and the LSB (DB_0) flickers.
4) Select next channel requiring gain trim and repeat step 2 and 3.

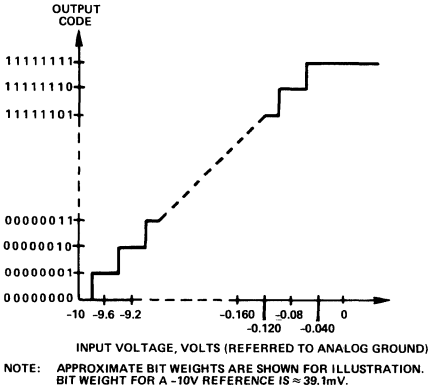


Figure 8b. Transfer Characteristic for Unipolar Circuit of Figure 8a

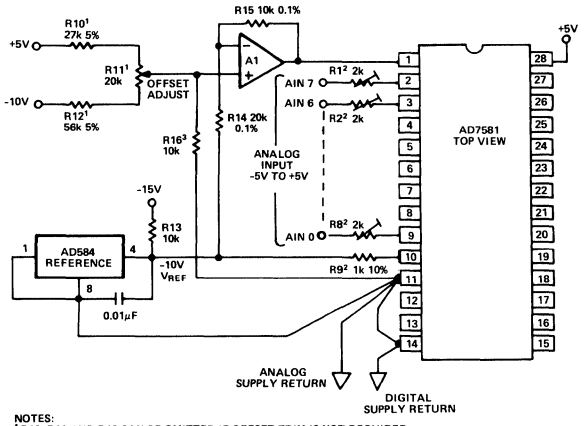


Figure 9a. AD7581 Bipolar (-5V to +5V) Operation (Output Code is Offset Binary)

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for ±5V bipolar operation. Output coding is offset binary. Comparator offset correction is again applied to the B_{OFS} pin.

Calibration is as follows (continuous conversions);

OFFSET:

1. Apply -4.980V (-FS/2 + 1/2LSB) to all input channels, AIN (0-7).
2. Trim R11 of the comparator offset circuit until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.

GAIN (FULL SCALE)

1. Apply +4.941V (+FS/2 -3/2LSB) to all input channels, A_{IN} (0-7).
2. Select required channel n via A_0, A_1, A_2, and latch the address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.
5. Apply -19.5mV to each gain-trimmed channel. If the ADC output code does not flicker between 01111111 and 10000000 repeat the calibration procedure.

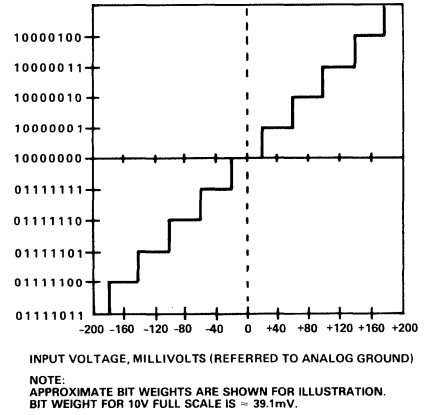


Figure 9b. Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

INTERFACING THE AD7581

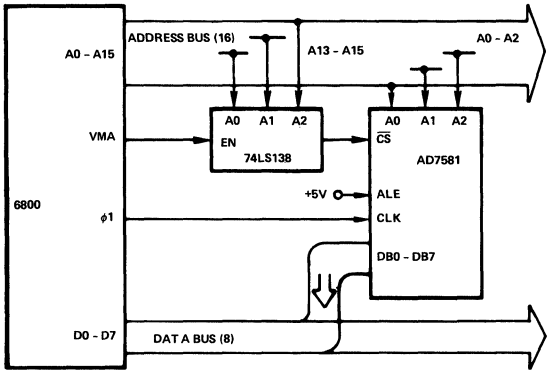


Figure 10. AD7581/6800 Interface

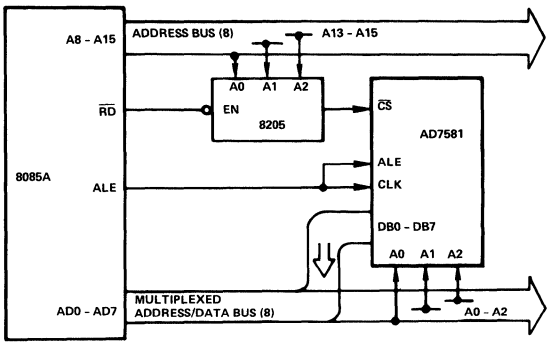


Figure 11. AD7581/8085 Interface

NOTES:

1. ANALOG AND DIGITAL GROUND
   It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7581. In systems where the A_{GND} - D_{GND} intertie is not local, connect back-to-back diodes (1N914 or equivalent) between the AD7581 A_{GND} and D_{GND} pins.
2. LOGIC DEGLITCHING IN μP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7581 $\overline{CS}$ terminal. These glitches can cause unwanted reads. The best way to avoid glitches is to gate the address decoding logic, e.g., with RD (8080), $\overline{RD}$ (8085) or VMA (6800).

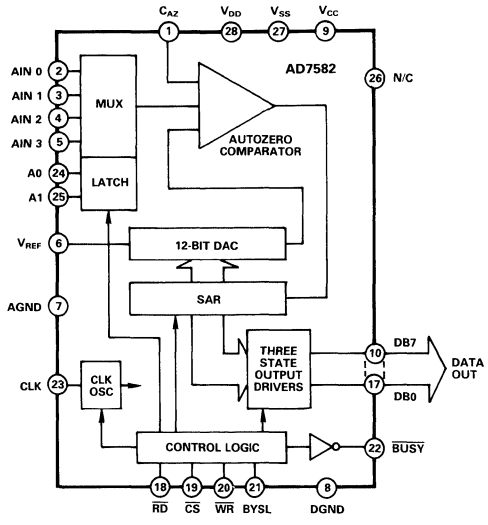
CMOS 12-Bit Successive Approximation ADC

AD7582

FEATURES

12-Bit Successive Approximation ADC
Four High Impedance Input Channels
Analog Input Voltage Range of 0 to +5V with Positive Reference of +5V
Conversion Time of 100μs per Channel
No Missed Codes Over Full Temperature Range
Low Total Unadjusted Error ±1LSB max
Autozero Cycle for Low Offset Voltage
Monolithic Construction

AD7582 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7582 is a medium speed, 4-channel 12-bit CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 100μs per channel. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100μV. The device is designed for easy microprocessor interface using standard control signals; $\overline{CS}$ (decoded device address), $\overline{RD}$ ($\overline{READ}$) and $\overline{WR}$ ($\overline{WRITE}$). The 4-channel input multiplexer is controlled via address inputs A0 and A1.

Conversion results are available in two bytes, 8LSB's and 4MSB's, over an 8-bit three state output bus. Either byte can be read first. Two converter busy flags are available to facilitate polling of the converter's status.

The analog input voltage range is 0V to +5V when using a reference voltage of +5V. The four analog inputs are all high impedance inputs with tight channel-to-channel matching–typically 0.1LSBs.

PRODUCT HIGHLIGHTS

1. The AD7582 is a complete 4 channel 12-bit A/D converter in either a 28-pin DIP or 28-terminal surface mount package requiring only a few passive components and a voltage reference.
2. Autozero cycle realizes very low offset voltages, typically 100μV.
3. The four channel input multiplexer (user addressable) features high input impedance and excellent channel-to-channel matching.
4. Standard microprocessor control signals to allow easy interfacing to most popular 8- and 16-bit microprocessors.

ORDERING INFORMATION[1]

Total Unadjusted Error	Temperature Range and Package Options[2]		
$T_{min}-T_{max}$	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic (N-28)	**Hermetic[3] (D-28)**	**Hermetic[3] (D-28)**
±1LSB	AD7582KN	AD7582BD	AD7582TD
	PLCC[4] (P-28A)		**LCCC[5] (E-28A)**
±1LSB	AD7582KP		AD7582TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Analog Devices reserves the right to ship either ceramic (package outline D-28) or cerdip (package outline Q-28) hermetic packages.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5.0V f_{CLK} = 140kHz external, all specifications T_{min} to T_{max} unless otherwise noted).

Parameter	K Version[1]	B Version[1]	T Version[1]	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Total Unadjusted Error[2]	±1	±1	±1	LSB max	All channels, AIN0–AIN3
Differential Nonlinearity	±1	±1	±1	LSB max	No missing codes guaranteed
Full Scale Error (Gain Error)	±1/4	±1/4	±1/4	LSB max	All channels, AIN0–AIN3 Full Scale TC is typically 5ppm/°C
Offset Error	±1/4	±1/4	±1/4	LSB max	All channels, AIN0–AIN3 Offset Error TC is typically 5ppm/°C
Channel to Channel Mismatch	±1/4	±1/4	±1/4	LSB max	
ANALOG INPUTS					
Analog Input Range	0 to +5	0 to +5	0 to +5	V	V_{REF} = +5.0V
C_{AIN}, On Channel Input Capacitance	8	8	8	pF typ	
I_{AIN}, Input Leakage Current					AIN0–AIN3; 0 to +5V
+25°C	10	10	10	nA max	
T_{min} to T_{max}	100	100	100	nA max	
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+5	+5	+5	V	±5%
V_{REF} Range	+4 to +6	+4 to +6	+4 to +6	V	Degraded transfer accuracy
V_{REF} Input Reference Current	1.0	1.0	1.0	mA max	V_{REF} = +5.0V
POWER SUPPLY REJECTION					
V_{DD} Only	±1/8	±1/8	±1/8	LSB typ	V_{DD} = +14.25V to +15.75V V_{SS} = −5V
V_{SS} Only	±1/8	±1/8	±1/8	LSB typ	V_{SS} = −4.75V to −5.25V V_{DD} = +15V
LOGIC INPUTS					
$\overline{RD}$ (Pin 18), $\overline{CS}$ (Pin 19), $\overline{WR}$ (Pin 20)					
BYSL (Pin 21), A0 (Pin 24), A1 (Pin 25)					
V_{IL} Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH} Input High Voltage	+2.4	+2.4	+2.4	V min	
I_{IN} Input Current					
+25°C	±1	±1	±1	μA max	V_{IN} = 0 to V_{CC}
T_{min} to T_{max}	+10	+10	+10	μA max	
C_{IN} Input Capacitance[3]	10	10	10	pF max	
CLK (Pin 23)					
V_{IL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH}, Input High Voltage	+3.0	+3.0	+3.0	V min	
I_{IL}, Input Low Current	±10	±10	±10	μA max	
I_{IH}, Input High Current	+1.5	+1.5	+1.5	mA max	
LOGIC OUTPUTS					
DB0–DB7 (Pins 10–17), $\overline{BUSY}$ (Pin 22)[4]					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA[4]
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	V_{CC} = +5V ±5%, I_{SOURCE} = 200μA
Floating State Leakage Current (Pins 10–17)	±1	±1	±1	μA max	V_{OUT} = 0V to V_{CC}
Floating State Output Capacitance	15	15	15	pF max	
CONVERSION TIME[5]					
With External Clock	100	100	100	μs min	f_{CLK} = 140kHz
With Internal Clock, T_A = +25°C	100/150	100/150	100/150	μs min/max	Using recommended clock components as shown in Figure 6.
POWER REQUIREMENTS[6]					
V_{DD}	+15	+15	+15	V NOM	±5% for specified performance
V_{SS}	−5	−5	−5	V NOM	±5% for specified performance
V_{CC}	+5	+5	+5	V NOM	±5% for specified performance
I_{DD}	7.5	7.5	7.5	mA max	Typically 4mA with V_{DD} = +15V
I_{SS}	7.5	7.5	7.5	mA max	Typically 3mA with V_{SS} = −5V
I_{CC}	100	100	100	μA typ	V_{IN} = V_{IL} or V_{IH}
	1.0	1.0	1.0	mA max	
Power Dissipation	75	75	75	mW typ	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH

NOTES

[1]Temperature Range as follows: K Version; 0 to +70°C
B Version; −25°C to +85°C
T Version; −55°C to +125°C

[2]Includes Full Scale Error, Offset Error and Relative Accuracy.

[3]Sample tested to ensure compliance.

[4]I_{SINK} for $\overline{BUSY}$ (pin 22) is 1.0 milliamp.

[5]Conversion Time includes autozero cycle time.

[6]Power supply current is measured when AD7582 is inactive i.e., $\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K & B Grades)	Limit at T_{min}, T_{max} (T Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2 (INT)[2]	200	240	280	ns min	$\overline{WR}$ Pulse Width (Internal Clock Operation)
t_2 (EXT)[2]	10	10	10	μs min	$\overline{WR}$ Pulse Width (External Clock Operation)
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	130	160	200	ns typ	
	200	250	300	ns max	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay
t_5	0	0	0	ns min	A0, A1 Valid to $\overline{WR}$ Setup Time
t_6	20	20	20	ns min	A0, A1 Valid to $\overline{WR}$ Hold Time
t_7	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_8	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_9	200	240	280	ns min	$\overline{RD}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{11}	50	50	50	ns min	BYSL to $\overline{RD}$ Setup Time
t_{12}	0	0	0	ns min	BYSL to $\overline{RD}$ Hold Time
t_{13}[3]	150	180	200	ns typ	
	200	240	280	ns max	$\overline{RD}$ to Valid Data (Bus Access Time)
t_{14}[4]	20	20	20	ns min	$\overline{RD}$ to Three State Output
	130	160	180	ns max	(Bus Relinquish Time)

NOTES
[1]Timing Specifications are sample tested at + 25°C to ensure compliance. All input control signals are specified with $t_r = t_f = 20$ns (10% to 90% of + 5V) and timed from a voltage level of + 1.6V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}.
[2]When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10μs. See "External Clock Operation".
[3]t_{13} is measured with the load circuits of Figure 3 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]t_{14} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
Specifications subject to change without notice.

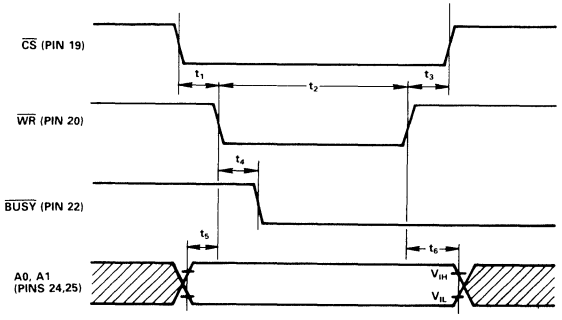


Figure 1. Start Cycle Timing

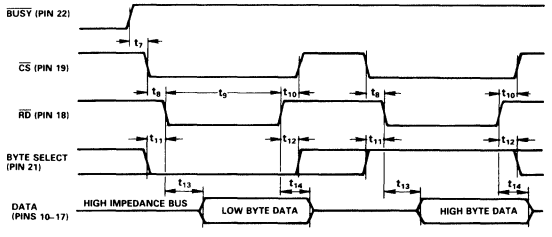
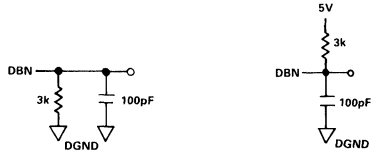
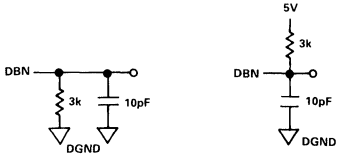


Figure 2. Read Cycle Timing



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 3. Load Circuits for Access Time Test (t_{13})



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 4. Load Circuits for Output Float Delay Test (t_{14})

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND	−0.3V, +17V
V_{SS} to DGND	+0.3V, −7V
AGND to DGND	−0.3V, V_{REF} +0.3V
V_{CC} to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD} +0.3V
AIN (0-3) to AGND	−0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND (Pins 18-21, 23-25)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (Pins 10-17, 22)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
Commercial (K Version)	0 to +70°C
Industrial (B Version)	−25°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (any Package)	
to +75°C	1,000mW
Derate above +75°C by	10mW/°C

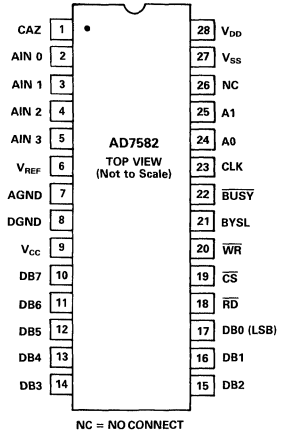
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

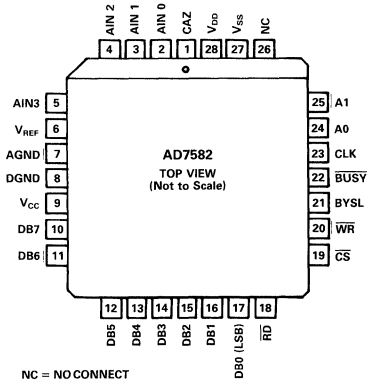
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

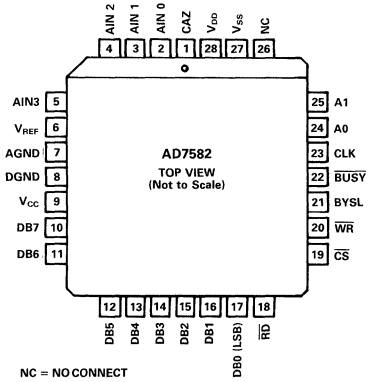
DIP



LCCC



PLCC



READING DATA

The 12-bit conversion data plus a converter status flag are available over an 8-bit wide data bus. Data is transferred from the AD7582 in right-justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the Byte Select (BYSL) input determining which byte–8 least significant bits or 4 most significant bits plus status flag–is to be read first.

Since the AD7582 uses the successive approximation register (SAR) to hold conversion results (refer to Functional Diagram), it is necessary to wait until a conversion is finished before reading valid 12-bit data. Executing a READ instruction (HIGH or LOW byte) to the AD7582 while a conversion is in progress will place the existing contents of the SAR onto the data bus. Three different approaches can ensure valid 12-bit data is available for reading.

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. At user-defined intervals after a conversion start instruction, poll the internal converter status flag, BUSY. This signal is available on pin 10 during a HIGH byte READ instruction and is the most left-hand bit in a 16-bit right-justified word. The status bit can be shifted into a microprocessor's accumulator-carry position for testing (BUSY is HIGH during conversion).
3. Use the externally available $\overline{\text{BUSY}}$ (pin 22) signal as an interrupt to the microprocessor. This signal is LOW during a conversion and returns HIGH at conversion end.

Executing a WRITE instruction while conversion is in progress will restart the conversion.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	CAZ	Autozero Capacitor Input. Connect other side of capacitor to AGND.
2	AIN 0	Analog Input, channel 0
3	AIN 1	Analog Input, channel 1
4	AIN 2	Analog Input, channel 2
5	AIN 3	Analog Input, channel 3
6	V_{REF}	Voltage reference input. The AD7582 is specified with $V_{REF} = +5.0V$.
7	AGND	Analog Ground
8	DGND	Digital Ground
9	V_{CC}	Logic Supply. For $V_{CC} = +5V$ digital inputs and outputs are TTL compatible.
10-17		Three state data outputs. They become active when $\overline{CS}$ & $\overline{RD}$ are brought low. Individual pin function is dependent upon the Byte Select (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	BYSL = HIGH	BYSL = LOW
Pin 10	BUSY[1]	DB7
Pin 11	LOW[2]	DB6
Pin 12	LOW[2]	DB5
Pin 13	LOW[2]	DB4
Pin 14	DB11 (MSB)	DB3
Pin 15	DB10	DB2
Pin 16	DB9	DB1
Pin 17	DB8	DB0 (LSB)

[1]BUSY (Pin 10) is a converter status flag and is HIGH during a conversion.
[2]Pins 11-13 output a logic LOW when BYSL is HIGH.
DB11–DB0 are the 12-bit conversion results, DB11 is the MSB.

18	$\overline{RD}$	READ input. This active LOW signal, in combination with $\overline{CS}$, is used to enable the output data three-state drivers.
19	$\overline{CS}$	CHIP SELECT Input. Decoded device address, active LOW. Used in combination with either $\overline{RD}$ or $\overline{WR}$ for control.
20	$\overline{WR}$	WRITE Input. This active LOW signal, in combination with $\overline{CS}$, is used to start a new conversion on a selected channel. When the AD7582 internal clock is used, the minimum $\overline{WR}$ pulse width is t2 (INT). When an external clock source is used, the minimum $\overline{WR}$ pulse width must be extended to include the autozero cycle time. For external clock operation, the minimum $\overline{WR}$ pulse width is t2 (EXT).
21	BYSL	BYTE SELECT. This control input determines whether the high or low byte of data is placed on the output data bus during a data READ operation ($\overline{CS}$ & $\overline{RD}$ LOW). See description of pins 10-17.
22	$\overline{BUSY}$	$\overline{BUSY}$ indicates converter status. $\overline{BUSY}$ is LOW during conversion, otherwise $\overline{BUSY}$ is held at a logic HIGH.
23	CLK	CLOCK Input for internal/external clock operation. Internal : Connect R_{CLK} and C_{CLK1}/C_{CLK2} timing components. See Figure 6 and Figure 7. External : Connect external 74HC compatible clock source as shown in Figure 8.
24	AO	Address Input AO. See pin 25 description.
25	A1	Address Input A1. Address inputs AO and A1 select the input channel to be converted. The address input latch is transparent when $\overline{CS}$ & $\overline{WR}$ are LOW. The address inputs are latched by $\overline{WR}$ returning HIGH.

A1	A0	CHANNEL SELECTED
0	0	AIN 0
0	1	AIN 1
1	0	AIN 2
1	1	AIN 3

26	N/C	No connect pin.
27	V_{SS}	Negative supply, −5V.
28	V_{DD}	Positive supply, +15V.

Operating Information

OPERATIONAL DIAGRAM

An operational diagram for the AD7582 is shown in Figure 5. The only passive components required are the autozero capacitor C_{AZ} and timing components R_{CLK}, C_{CLK1} & C_{CLK2} for the internal clock oscillator. If the AD7582 is to be used with an external clock source, then only C_{AZ} is required. Individual pin functions are described in detail on the previous page.

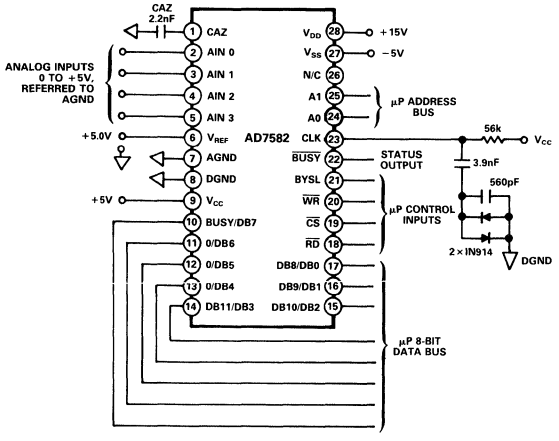


Figure 5. AD7582 Operational Diagram

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 6 and the AD7582 operating waveforms are shown in Figure 7.

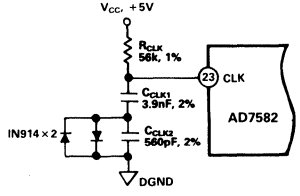


Figure 6. Circuitry Required for Internal Clock Operation

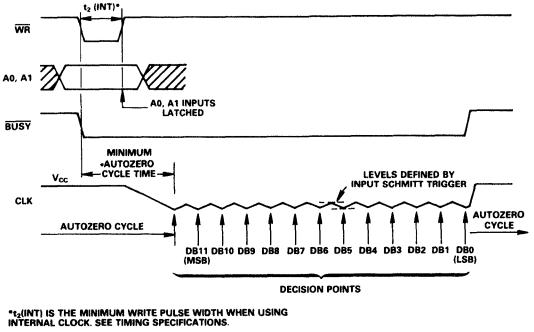


Figure 7. Operating Waveforms – Internal Clock

Between conversions ($\overline{BUSY}$ = HIGH) the AD7582 is in the autozero cycle. When $\overline{WR}$ goes LOW (with $\overline{CS}$ LOW) to start a new conversion, the input multiplexer is switched to the selected channel N, via address inputs A0, A1. The autozero capacitor C_{AZ} now charges to AIN N–V_{OS} where V_{OS} is the input offset voltage of the autozero comparator.

A minimum time of 10μs is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{WR}$ to remain LOW for this period of time since it is automatically provided by the AD7582. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2}, causing the voltage at the CLK input pin to slowly decay from V_{CC}. This occurs after $\overline{WR}$ returns HIGH; $\overline{WR}$ returning HIGH also latches the multiplexer address inputs A0, A1 (see Figure 7). The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK}. When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2}. The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 6 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

EXTERNAL CLOCK OPERATION

For external clock operation R_{CLK}, C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The AD7582 $\overline{WR}$ pulse width must now be extended to provide the minimum autozero cycle time of 10μs since this is no longer provided automatically by the AD7582. Referring to the operating waveforms of Figure 9, the minimum $\overline{WR}$ pulse width when using an external clock source is t_2 (EXT). Multiplexer address inputs A0 and A1, in addition to the $\overline{CS}$ input must now remain valid for the external $\overline{WR}$ pulse width. It is not necessary to synchronize the external clock source with the extended $\overline{WR}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{WR}$ input returns HIGH.

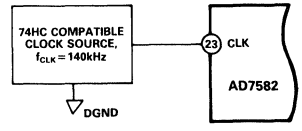


Figure 8. External Clock Operation

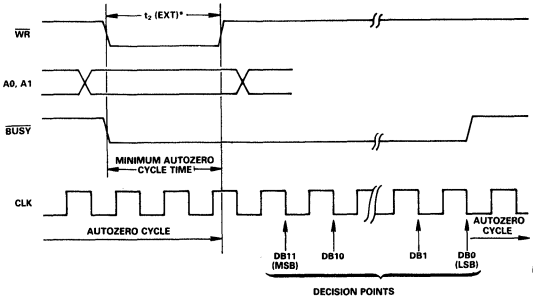


Figure 9. Operating Waveforms – External Clock

LC²MOS High-Speed 12-Bit ADC

AD7672

FEATURES
- **12-Bit Resolution and Accuracy**
- **Fast Conversion Time**
  - **AD7672XX03 – 3μs**
  - **AD7672XX05 – 5μs**
  - **AD7672XX10 – 10μs**
- **Unipolar or Bipolar Input Ranges**
- **Low Power: 110mW**
- **Fast Bus Access Times: 90ns**
- **Small, 0.3″, 24-Pin Package and 28-Terminal Surface Mount Packages**

GENERAL DESCRIPTION

The AD7672 is a high-speed 12-bit ADC, fabricated in an advanced, mixed technology, Linear-Compatible CMOS (LC²MOS) process, which combines precision bipolar components with low-power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3μs while dissipating only 110mW of power.

To allow maximum flexibility the AD7672 is designed for use with an external reference voltage. This allows the user to choose a reference whose performance suits the application or to drive many AD7672s from a single system reference, since the reference input of the AD7672 is buffered and draws little current. For digital signal processing applications where absolute accuracy and temperature coefficients may be unimportant, a low-cost reference can be used. For maximum precision, the AD7672 can be used with a high-accuracy reference, such as the AD588, when absolute 12-bit accuracy can be obtained over a wide temperature range.

An on-chip clock-circuit is provided which may be used with a crystal for accurate definition of conversion time. Alternatively, the clock input may be driven from an external source such as a microprocessor clock.

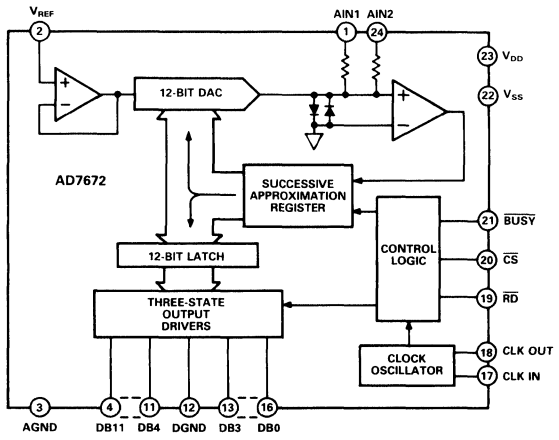
The AD7672 also offers flexibility in its analog input ranges, with a choice of 0 to +5V, 0 to +10V and ±5V.

The AD7672 is also designed to operate from nominal supply voltages of +5V and −12V. This makes it an ideal choice for data acquisition cards in personal computers where the negative supply is generally −12V.

The AD7672 has a high-speed digital interface with three-state data outputs and standard microprocessor control inputs (Chip Select and Read). Bus access time of only 90ns allows the AD7672 to be interfaced to most modern microprocessors.

The AD7672 is available in a variety of space-saving packages; plastic and hermetic 24-pin "skinny" DIP and 28-pin ceramic and plastic chip carrier.

AD7672 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Fast, 3μs, 5μs and 10μs conversion speeds make the AD7672 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any high-speed data acquisition system.
2. LC²MOS circuitry gives high precision with low power drain (110mW typ).
3. Choice of 0 to +5V, 0 to +10V or ±5V input ranges, accomplished by pin-strapping.
4. Fast, simple, digital interface has a bus access time of 90ns allowing easy connection to most microprocessors.
5. Available in space-saving 24-pin, 0.3″ DIP or surface mount package.

SPECIFICATIONS

(V_{DD} = 5V ±5%, V_{SS} = −12V±10%, V_{REF} = −5V unless otherwise noted. f_{CLK}: 4MHz for AD7672XX03, 2.5MHz for AD7672XX05, 1.25MHz for AD7672XX10. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode).

Parameter	K Version[1]	L Version[1]	B Version[1]	C Version[1]	Units	Test Conditions/Comments
ACCURACY[2]						
Resolution	12	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	±1	±1/2	LSB max	Tested Range ±5V
T_{min} to T_{max}	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	±0.9	LSB max	No Missing Codes Guaranteed
Unipolar Offset Error @ +25°C	±5	±3	±5	±3	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±6	±4	±6	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Gain Error @ +25°C	±5	±4	±5	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±7	±6	±7	±6	LSB max	Typical TC is 2ppm/°C
Bipolar Zero Error @ +25°C	±5	±3	±5	±3	LSB max	Input Range: ±5V
T_{min} to T_{max}	±6	±4	±6	±4	LSB max	Typical TC is 2ppm/°C
Bipolar Gain Error @ +25°C	±5	±4	±5	±4	LSB max	Input Range: ±5V
T_{min} to T_{max}	±7	±6	±7	±6	LSB max	Typical TC is 2ppm/°C
ANALOG INPUT						
Unipolar Input Current	3.5	3.5	3.5	3.5	mA max	Input Ranges: 0 to 5V or 0 to 10V
Bipolar Input Current	±1.75	±1.75	±1.75	±1.75	mA max	Input Range: ±5V
REFERENCE INPUT						
V_{REF} (For Specified Performance)	−5	−5	−5	−5	Volts	±1%
Input Reference Current	−3	−3	−3	−3	μA max	
POWER SUPPLY REJECTION						
V_{DD} Only, (FS Change)	±1	±1	±1	±1	LSB typ	V_{SS} = −12V, V_{DD} = +4.75V to +5.25V
V_{SS} Only, (FS Change)	±1	±1	±1	±1	LSB typ	V_{DD} = +5V, V_{SS} = −10.8V to −13.2V
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, CLK IN						
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	+2.4	V min	
C_{IN},[3] Input Capacitance	10	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$						
I_{IN}, Input Current	±10	±10	±10	±10	μA max	V_{IN} = 0 to V_{DD}
CLK IN						
I_{IN}, Input Current	±20	±20	±20	±20	μA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS						
DB11–DB0, $\overline{BUSY}$, CLK OUT						
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200μA
Floating-State Leakage Current						
DB11–DB0	±10	±10	±10	±10	μA max	
Floating-State Output Capacitance[3]	15	15	15	15	pF max	
CONVERSION TIME						
AD7672XX03						Applies to K and B Grades Only
Synchronous Clock	3.125	–	3.125	–	μs max	f_{CLK} = 4MHz. See Under
Asynchronous Clock	3/3.25	–	3/3.25	–	μs min/max	Control Inputs Synchronization
AD7672XX05						
Synchronous Clock	5	5	5	5	μs max	f_{CLK} = 2.5MHz
Asynchronous Clock	4.8/5.2	4.8/5.2	4.8/5.2	4.8/5.2	μs min/max	
AD7672XX10						
Synchronous Clock	10	10	10	10	μs max	f_{CLK} = 1.25MHz
Asynchronous Clock	9.6/10.4	9.6/10.4	9.6/10.4	9.6/10.4	μs min/max	
POWER REQUIREMENTS						
V_{DD}	+5	+5	+5	+5	VNOM	±5% for Specified Performance
V_{SS}	−12	−12	−12	−12	VNOM	±10% for Specified Performance
I_{DD}[4]	7	7	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
I_{SS}[4]	−12	−12	−12	−12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
Power Dissipation	110	110	110	110	mW typ	
	179	179	179	179	mW max	

NOTES

[1]Temperature range as follows: K, L versions; L 0 to +70°C.
B, C versions; −25°C to +85°C.

[2]V_{DD} = 5V, V_{SS} = −12V, 1LSB = FS/4096

[3]Sample tested to ensure compliance.

[4]Power supply current is measured when AD7672 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.

Specifications subject to change without notice.

SPECIFICATIONS

(V_{DD} = 5V ±5%, V_{SS} = −12±10%, V_{REF} = −5V unless otherwise noted. f_{CLK}: 2.5MHz for AD7672XX05, 1.25MHz for AD7672XX10. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode).

Parameter	T Version[1]	U Version[1]	Units	Test Conditions/Comments
ACCURACY[2]				
Resolution	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	LSB max	Tested Range ±5V
T_{min} to T_{max}	±1	±3/4	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	No Missing Codes Guaranteed
Unipolar Offset Error @ +25°C	±5	±3	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±6	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Gain Error @ +25°C	±5	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±7	±6	LSB max	Typical TC is 2ppm/°C
Bipolar Zero Error @ +25°C	±5	±3	LSB max	Input Range: ±5V
T_{min} to T_{max}	±6	±4	LSB max	Typical TC is 2ppm/°C
Bipolar Gain Error @ +25°C	±5	±4	LSB max	Input Range: ±5V
T_{min} to T_{max}	±7	±6	LSB max	Typical TC is 2ppm/°C
ANALOG INPUT				
Unipolar Input Current	3.5	3.5	mA max	Input Ranges: 0 to 5V or 0 to 10V
Bipolar Input Current	±1.75	±1.75	mA max	Input Range: ±5V
REFERENCE INPUT				
V_{REF} (For Specified Performance)	−5	−5	Volts	±1%
Input Reference Current	−3	−3	μA max	
POWER SUPPLY REJECTION				
V_{DD} Only, (FS Change)	±1	±1	LSB typ	V_{SS} = −12V, V_{DD} = +4.75V to +5.25V
V_{SS} Only, (FS Change)	±1	±1	LSB typ	V_{DD} = +5V, V_{SS} = −10.8V to −13.2V
LOGIC INPUTS				
$\overline{CS}$, $\overline{RD}$, CLK IN				
V_{INL}, Input Low Voltage	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	V min	
C_{IN},[3] Input Capacitance	10	10	pF max	
$\overline{CS}$, $\overline{RD}$				
I_{IN}, Input Current	±10	±10	μA max	V_{IN} = 0 to V_{DD}
CLK IN				
I_{IN}, Input Current	±20	±20	μA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$, CLK OUT				
V_{OL}, Output Low Voltage	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	V min	I_{SOURCE} = 200μA
Floating-State Leakage Current				
DB11–DB0	±10	±10	μA max	
Floating-State Output Capacitance[3]	15	15	pF max	
CONVERSION TIME				
AD7672XX05				
Synchronous Clock	5	5	μs max	f_{CLK} = 2.5MHz. See Under
Asynchronous Clock	4.8/5.2	4.8/5.2	μs min/max	Control Inputs Synchronization
AD7672XX10				
Synchronous Clock	10	10	μs max	f_{CLK} = 1.25MHz
Asynchronous Clock	9.6/10.4	9.6/10.4	μs min/max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	VNOM	±5% for Specified Performance
V_{SS}	−12	−12	VNOM	±10% for Specified Performance
I_{DD}[4]	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
I_{SS}[4]	−12	−12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
Power Dissipation	110	110	mW typ	
	179	179	mW max	

NOTES
[1]Temperature range as follows: T, U versions; −55°C to +125°C.
[2]V_{DD} = 5V, V_{SS} = −12V, 1LSB = FS/4096
[3]Sample tested to ensure compliance.
[4]Power supply current is measured when AD7672 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.

Specifications subject to change without notice.

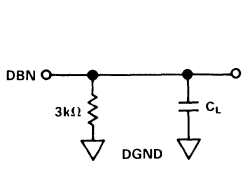
TIMING CHARACTERISTICS[1] (V_{DD} = 5V, V_{SS} = −12V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	90	110	120	ns max	Data Access Time after $\overline{RD}$, C_L = 20pF
	125	150	170	ns max	Data Access Time after $\overline{RD}$, C_L = 100pF
t_4	t_3	t_3	t_3	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
t_7[3]	20	20	20	ns min	Bus Relinquish Time
	75	85	90	ns max	
t_8	200	200	200	ns min	Delay Between Successive Read Operations

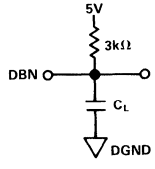
NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

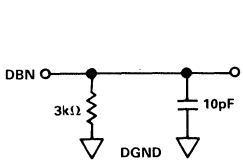


a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

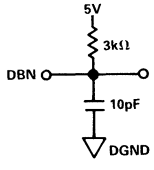


b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V to +7V
V_{SS} to DGND	+0.3V to −17V
AGND to DGND	−0.3V to V_{DD} +0.3V
AIN1, AIN2 to AGND	−15V to +15V
V_{REF} to AGND	V_{SS} −0.3V to V_{DD} +0.3V
Digital Input Voltage to DGND (CLK IN, $\overline{CS}$, $\overline{RD}$)	−0.3V to V_{DD} +0.3V
Digital Output Voltage to DGND (DB11-DB0, $\overline{BUSY}$, CLK OUT)	−0.3V to V_{DD} +0.3V
Operating Temperature Range	
K, L	0 to +70°C
B, C	−25°C to +85°C
T, U	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	1,000mW
Derates above +75°C by	10mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TERMINOLOGY

UNIPOLAR OFFSET ERROR
The ideal first code transition should occur when the analog input is 1/2LSB above AGND. The deviation of the actual transition from that point is termed the offset error.

BIPOLAR ZERO ERROR
The ideal midscale transition (i.e., 0111 1111 1111 to 1000 0000 0000) for the ±5V range should occur when the analog input is 1/2LSB below AGND. Bipolar zero error is the deviation of the actual transition from that point.

GAIN ERROR
The ideal difference between the first code transition and last code transition is FS −2LSBs. The Gain error is defined as the deviation between this ideal difference and the measured difference. Ideal FS corresponds to 5V for the unipolar 0 to 5V range and 10V for both the unipolar 0 to 10V and bipolar ±5V ranges.

ORDERING INFORMATION[1]

CONVERSION TIME = 3μs

Accuracy Grade	Temperature Range and Package Options[2]	
	0 to +70°C	−25°C to +85°C
	Plastic DIP (N-24)	**Hermetic[3] (Q-24)**
±1LSB	AD7672KN03	AD7672BQ03
	PLCC[4] (P-28A)	**LCCC[5] (E-28A)**
±1LSB	AD7672KP03	AD7672BE03

CONVERSION TIME = 5μs

Accuracy Grade	Temperature Range and Package Options[2]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-24)	**Hermetic[3] (Q-24)**	**Hermetic[3] (Q-24)**
±1LSB	AD7672KN05	AD7672BQ05	AD7672TQ05
±1/2LSB	AD7672LN05	AD7672CQ05	AD7672UQ05
	PLCC[4] (P-28A)		**LCCC[5] (E-28A)**
±1LSB	AD7672KP05		AD7672TE05
±1/2LSB	AD7672LP05		AD7672UE05

CONVERSION TIME = 10μs

Accuracy Grade	Temperature Range and Package Options[2]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-24)	**Hermetic[3] (Q-24)**	**Hermetic[3] (Q-24)**
±1LSB	AD7672KN10	AD7672BQ10	AD7672TQ10
±1/2LSB	AD7672LN10	AD7672CQ10	AD7672UQ10
	PLCC[4] (P-28A)		**LCCC[5] (E-28A)**
±1LSB	AD7672KP10		AD7672TE10
±1/2LSB	AD7672LP10		AD7672UE10

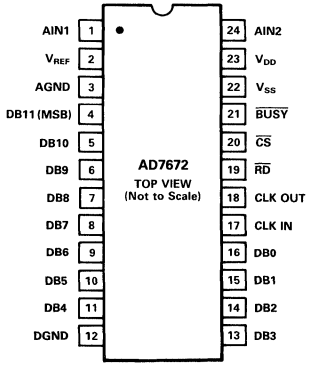
NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Analog Devices reserves the right to ship either ceramic (package outline D-24A) or cerdip hermetic (package outline Q-24) packages.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

DIP PIN FUNCTION DESCRIPTION

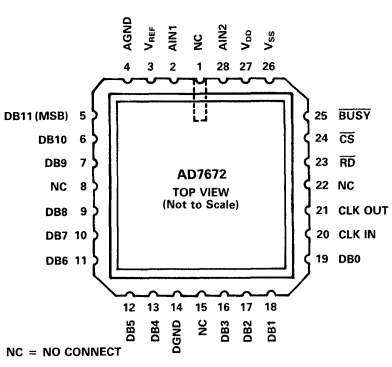
DIP Pin No.	Mnemonic	Description
1	AIN1	Analog Input.
2	V_{REF}	Voltage Reference Input. The AD7672 is specified with $V_{REF} = -5V$.
3	AGND	Analog Ground.
4 . . . 11	DB11 . . .DB4	Three-state data outputs. They become active when $\overline{CS}$ and $\overline{RD}$ are brought low. DB11 is the most significant bit (MSB).
13 . . . 16	DB3 . . . DB0	
12	DGND	Digital Ground.
17	CLK IN	Clock Input pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output Pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description.
19	$\overline{RD}$	READ input. This active LOW signal, in conjunction with $\overline{CS}$ is used to enable the output data three-state drivers and initiate a conversion.
20	$\overline{CS}$	CHIP SELECT Input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three-state drivers and initiate a conversion.
21	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
22	V_{SS}	Negative Supply, −12V.
23	V_{DD}	Positive Supply, +5V.
24	AIN2	Analog Input.

PIN CONFIGURATIONS

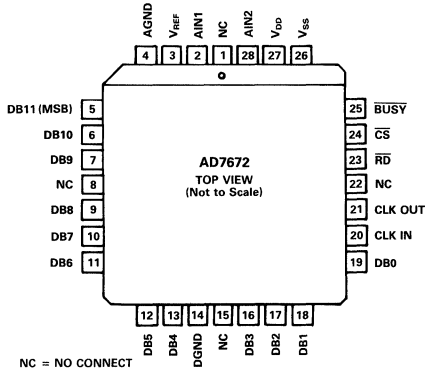
DIP



LCCC



PLCC



OPERATING FROM A NEGATIVE SUPPLY GREATER THAN −12V

The AD7672 is designed to operate with a V_{SS} input of −12V ± 10%. In applications where the negative supply is greater than −12V, then a Zener diode in series with V_{SS} can be used to reduce the supply. The Zener diode should have a dynamic impedance of not greater than 40Ω. An example is given in Figure 3. The diode has a Zener voltage of 3V, which makes it suitable for a negative supply of −15V ± 7%.

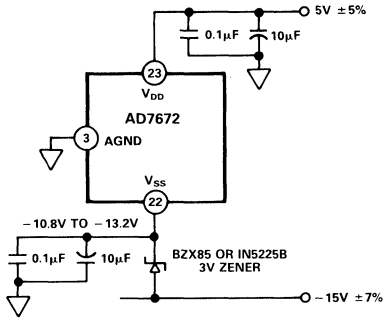


Figure 3. Operation from Nominal Power Supplies of 5V and −15V

CONVERTER DETAILS

Conversion start is controlled by the $\overline{CS}$ and $\overline{RD}$ inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 4, the analog inputs (AIN1 & AIN2) connect to the comparator input via 5kΩ resistors. The DAC which has 2.5kΩ output impedence connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output against the analog inputs. The MSB decision is made 80ns (typically) after the second falling edge of CLK IN following a conversion start (see Figure 5). Similarly, the succeeding bit decisions are made approximately 80ns after a CLK IN falling edge until conversion

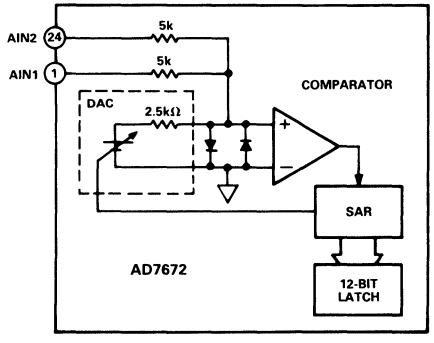


Figure 4. AD7672 AIN Input

is finished. At the end of conversion, the DAC output current balances the current from the analog inputs. The SAR contents (12-bit data word) which represent the analog input signal are loaded into a 12-bit latch.

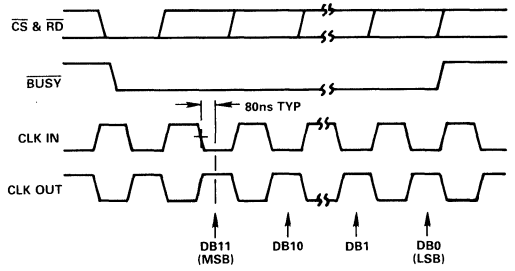


Figure 5. Operating Waveforms Using an External Clock Source for CLK IN

CONTROL INPUTS SYNCHRONIZATION

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach may be used: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT. This ensures a fixed conversion time that is 12.5 times the CLK IN period.

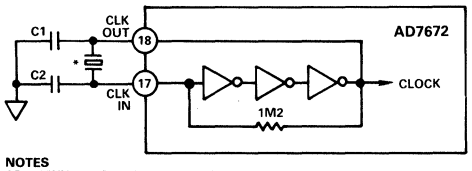
DRIVING THE ANALOG INPUTS

During conversion current from the analog inputs is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 4MHz when CLK IN = 4MHz). This causes voltage spikes (glitches) to appear at the analog inputs. The magnitude and settling time of these glitches depends on the open-loop output impedance and small signal bandwidth of the amplifier or sample and hold driving these inputs. These devices must have sufficient drive to ensure that the glitches have settled within one clock period. An example of a suitable op amp is the AD OP-27. The magnitude of the largest glitch when using this device to drive one of the analog inputs is typically 11mV with a 200ns settling time.

Suitable devices capable of driving the AD7672 analog inputs are the AD OP-27 and AD711 op amps and the AD585 and AD683/681 sample and holds.

INTERNAL CLOCK OPERATION

Figure 6 shows the AD7672 internal clock circuit. A crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18) to provide a clock oscillator for the ADC timing. Alternatively the crystal/ceramic resonator may be omitted and an external clock source may be connected to CLK IN. For an external clock the mark/space ratio must be 50/50. An inverted CLK IN will appear at the CLK OUT pin as shown in the operating waveforms of Figure 5.



NOTES
AD7672XX03 – 4MHz CRYSTAL/CERAMIC RESONATOR.
AD7672XX05 – 2.5MHz CRYSTAL/CERAMIC RESONATOR.
AD7672XX10 – 1.25MHz CRYSTAL/CERAMIC RESONATOR.
C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30pF TO 100pF.

Figure 6. AD7672 Internal Clock Circuit

ANALOG INPUT RANGES

The AD7672 provides three user selectable analog input ranges; 0 to +5V, 0 to +10V and ±5V. Figure 7 shows how to configure the two analog inputs (AIN1 and AIN2) for these ranges.

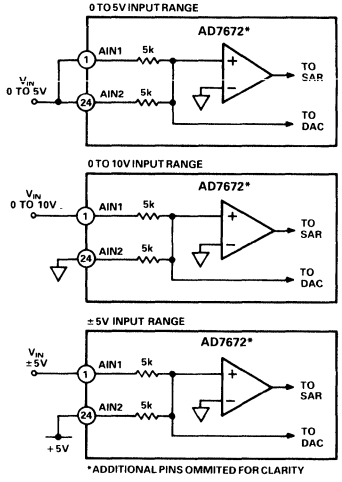


Figure 7. Analog Input Range Configurations

UNIPOLAR OPERATION

Figure 8 shows how to configure an AD584 to produce a reference voltage of −5V for unipolar operation.

The ideal input/output characteristic is shown in Figure 9. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs . . . FS −3/2 LSBs).

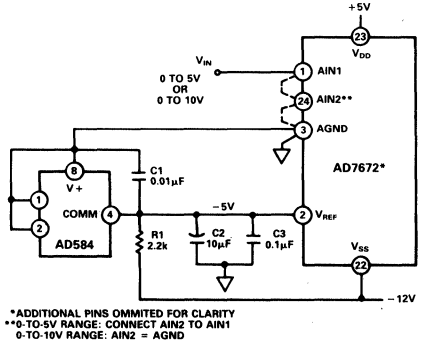


Figure 8. Unipolar Operation Using the AD584 as a Reference

The output code is natural binary with 1LSB = FS/4096. FS is either +5V or +10V depending on the analog inputs configuration.

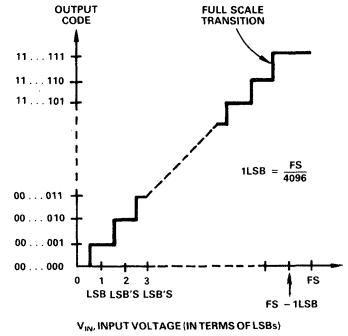


Figure 9. AD7672 Ideal Input/Output Transfer Characteristic for Unipolar Operation.

OFFSET AND FULL-SCALE ERROR

In most Digital Signal Processing (DSP) applications, offset and full-scale error have little or no effect on system performance. A typical example is a digital filter, where an analog input signal is quantized, digitally processed and recreated using a DAC. In these type of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important consideration in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

UNIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

If absolute accuracy is an application requirement then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 10 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving the analog input (i.e., A1 in Figure 10.). For zero offset error apply a voltage equal to 1/2LSB at V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

0 to +5V Range: 1/2LSB = 0.61mV
0 to +10V Range: 1/2LSB = 1.22mV

For zero full-scale error apply an analog input voltage equal to FS-3/2LSBs (last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

0 to +5V Range: FS-3/2LSBs = 4.99817
0 to +10V Range: FS-3/2LSBs = 9.99634

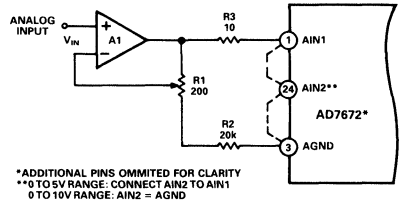
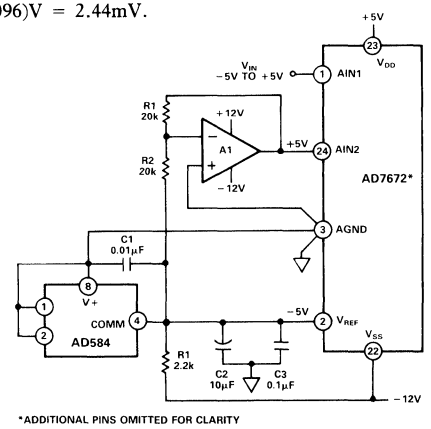


Figure 10. Unipolar Operation with Gain Error Adjust

BIPOLAR OPERATION

Bipolar operation is achieved by providing a +10V span at the AIN1 input which is offset to ±5V by applying +5V at the AIN2 input. This requires two reference voltages; −5V for the V_{REF} input and +5V for the AIN2 input. Figure 11 demonstrates how to produce these voltages from an AD584 and an inverting amplifier configuration. Alternatively, a convenient solution is to use the AD588 voltage reference as in Figure 12. This device generates the required ±5V with a minimum of additional components. It also offers excellent temperature stability with voltage drifts as low as 1.5ppm/°C.

The ideal input/output transfer characteristic after offset and gain adjustment is shown in Figure 13. The LSB size is (10/4096)V = 2.44mV.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 11. Bipolar Operation Using an AD584 and an AD711 Op Amp

BIPOLAR OFFSET AND GAIN ADJUSTMENT

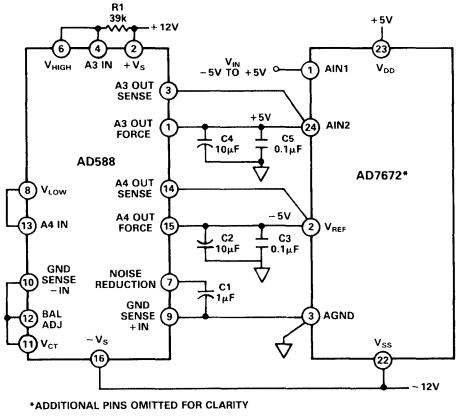
In applications where absolute accuracy is important then offset and gain error can be adjusted to zero. Offset is adjusted by trimming the voltage at the AIN1 or the AIN2 input when the analog input is at −FS/2 +1/2LSB. This can be achieved by adjusting the offset of an external amplifier used to drive either of these analog inputs. Alternatively the AD588 voltage reference contains a balance control input which can be used to trim the offset to zero. An additional potentiometer (R2 in Figure 14) is required. The trim procedure is as follows:

Apply −4.99878V (−FS/2 + 1/2LSB) at V_{IN} and adjust R2 until the ADC ouput code flickers between 0000 0000 0000 and 0000 0000 0001.

Gain error can be adjusted at either the last positive code transition or the mid-scale transition (bipolar zero error adjust). Adjusting the positive end of the transfer function is in keeping with more conventional ADC calibration techniques where the user fixes the two end points as in the unipolar case. Bipolar zero adjustment is required in some applications (e.g., motor control) where the user must be guaranteed that the 0111 1111 1111 to 1000 0000 0000 transition occurs exactly when the analog input is 1/2LSB below AGND. The trim procedures for both cases are as follows. (See Figure 14.)

Last Code Transition Adjust

Apply a voltage of 4.99634 volts (FS/2 – 3/2LSBs) at V_{IN}. Adjust R5 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 12. Bipolar Operation Using an AD588 Voltage Reference

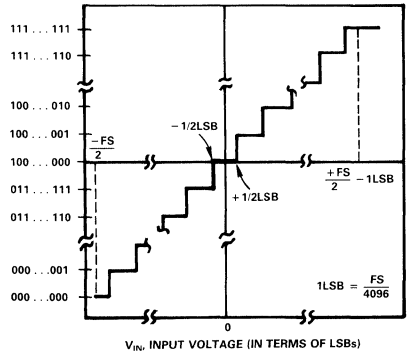
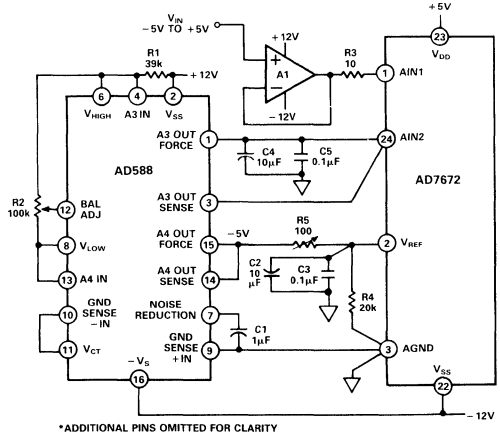


Figure 13. Ideal Input/Output Transfer Characteristic for Bipolar Operation



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 14. Bipolar Operation with Offset and Gain Error Adjust

Bipolar Zero Error Adjust

Apply a voltage of −1.22mV at V_{IN} and adjust R5 until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000.

TIMING AND CONTROL

Conversion start and data read operations are controlled by two of the AD7672 digital inputs; $\overline{CS}$ and $\overline{RD}$. Figure 15 shows the equivalent logic circuit of these inputs. A high-to-low logic transition on $\overline{CS}$ and $\overline{RD}$ initiates a conversion. Once initiated it cannot be restarted until conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

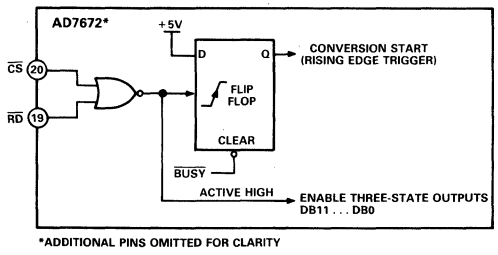


Figure 15. Internal Logic for Control Inputs $\overline{CS}$ and $\overline{RD}$

There are two modes of operation as outlined by the timing diagrams of Figures 16 and 17. Slow Memory Mode is designed for microprocessors that can be driven into a WAIT state, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low, which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode, which does not require microprocessor WAIT states. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result. The data format for both modes is designed for parallel interfacing.

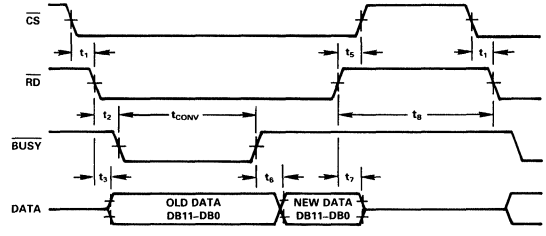


Figure 16. Slow Memory Mode Timing Diagram

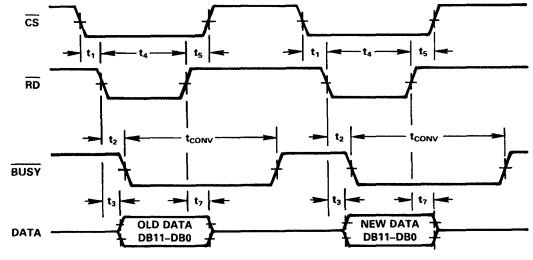


Figure 17. ROM Mode Timing Diagram

SLOW MEMORY MODE

Figure 16 shows the timing diagram for Slow Memory Mode. $\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the AD7672 acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on the output data bus.

ROM MODE

The ROM Mode avoids placing a microprocessor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion are available on the data outputs while $\overline{CS}$ and $\overline{RD}$ are low. This data may be disregarded if not required. A second READ operation reads the new data and starts another conversion. A delay at least as long as the AD7672 conversion time must be allowed between READ operations.

MICROPROCESSOR INTERFACING

The AD7672 is designed to interface to microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ inputs are common control inputs to all peripheral memory interfacing.

MC68000 MICROPROCESSOR

Figure 18 shows a typical interface for the MC68000. The AD7672 is operating in the Slow Memory Mode. Assuming the AD7672 is located at address C000 then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result.

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$, so that the 68000 is forced into a WAIT state. At the end of conversion $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the UP.

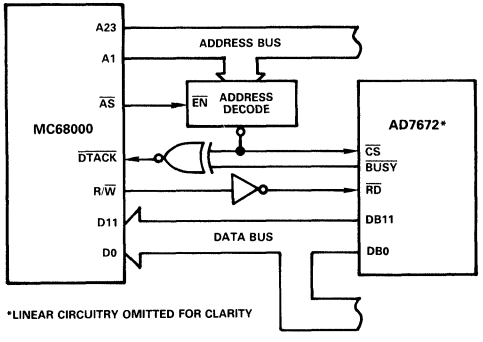


Figure 18. AD7672 –MC68000 Interface

8085A, Z-80 MICROPROCESSORS

Figure 19 shows an AD7672 interface for the Z-80 and 8085A. The AD7672 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the Figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. The following LOAD instruction starts a conversion and reads the conversion result into the HL register pair.

For the 8085A LHLD (B000)
For the Z-80 LDHL (B000)

This is a two byte read instruction. During the first read operation, $\overline{BUSY}$ forces the microprocessor to wait for the AD7672 conversion. At the end of conversion the low byte (DB7-DB0) is loaded into the HL register pair and the high byte (DB11-DB8) is latched into a 74HC374. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

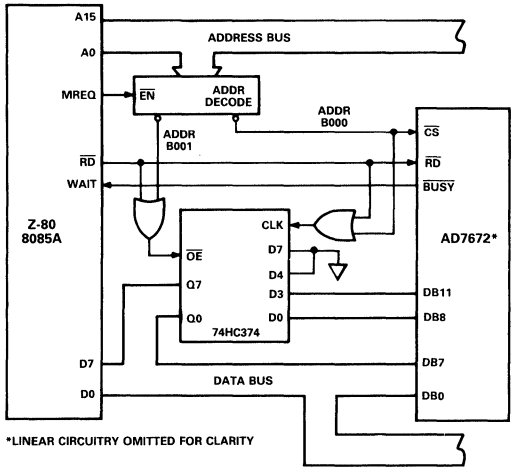


Figure 19. AD7672 – 8085A/Z80 Interface

IBM PC* COMPUTER

The −12V power supply operation of the AD7672 makes it an ideal choice for the IBM PC. A typical interface is shown in Figure 20. The AD7672 is configured in the ROM mode. Two addresses are required to read the 12-bit ADC data over the 8-bit data bus. An I/O read instruction to the ADC address (B000) starts a conversion and reads the low data byte (DB7-DB0). This data is from the previous conversion. The high byte (DB11-DB8) may be read with a similar I/O instruction to the 74HC374 latch (address B001). Alternatively the up-to-date data may be read at the end of conversion. The AD7672 $\overline{BUSY}$ may be used to interrupt the IBM PC as shown in Figure 20. The data is then read with two I/O instructions as before. Note a read instruction to the ADC should not be attempted while conversion is in progress.

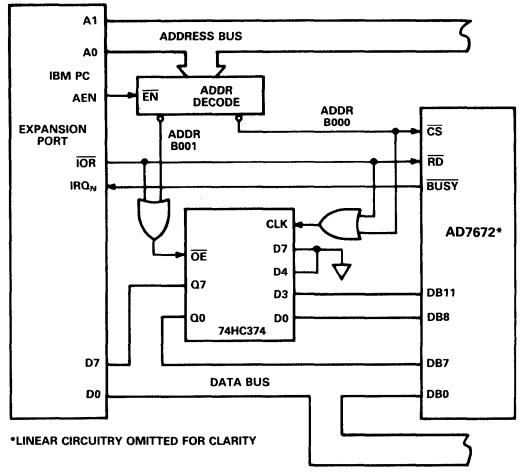


Figure 20. AD7672 – IBM PC Interface

ADSP-2100 DIGITAL SIGNAL PROCESSOR

The ADSP-2100 like other digital signal processors requires very fast data access times beyond the capabilities of the AD7672. This problem is easily overcome by inserting 74HC374 latches in the data bus as in Figure 21. Again for this interface a single instruction is sufficient to read the AD7672 conversion result.

MRO = DM (ADC ADDRESS)

This instruction initiates a conversion and reads the previous conversion result into the MRO register. $\overline{CS}$ and $\overline{RD}$ are gated so that they remain low for the duration of the conversion. Note that no WAIT states are inserted even though the AD7672 is configured for a Slow Memory mode. At the end of conversion, $\overline{BUSY}$ going high latches the new result into the 74HC374 latches. An RC delay is inserted to compensate for the data setup time after $\overline{BUSY}$ (t_6).

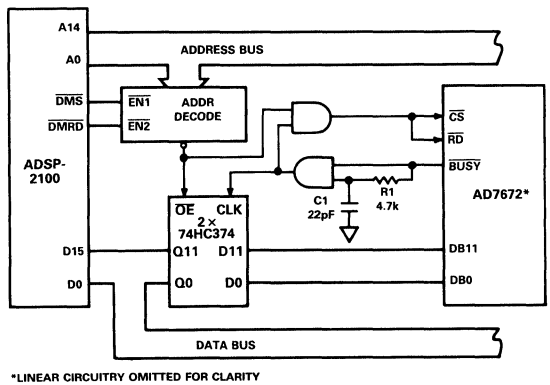


Figure 21. AD7672 – ADSP-2100 Interface

*IBM PC is a trademark of International Business Machines Corp.

TMS32010 MICROCOMPUTER

Figure 22 shows an AD7672-TMS32010 interface. The AD7672 is operating in the ROM mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The AD7672 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into the accumulator and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

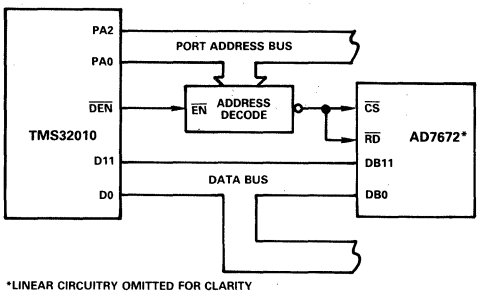


Figure 22. AD7672 – TMS32010 Interface

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. For 12-bit performance the AD7672's comparator is required to make bit decisions to an accuracy of 0.61mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 3 (AGND) or as close as possible to the AD7672 as shown in Figure 23. Connect all other grounds and Pin 12 (AD7672 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths, while guarding the analog circuitry from digital noise. The circuit layout of Figures 29 and 30 have both analog and digital ground planes which are kept separated and only joined together at the AD7672 AGND pin.

NOISE: Keep the input signal leads to AIN and signal return leads from AGND (Pin3) as short as possible to minimize input noise coupling. In applications where this is not possible use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

Microprocessor applications generate noisy environments, making 12-bit performance difficult to achieve, especially when the ADC is connected to a continously active bus. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the AD7672 data bus.

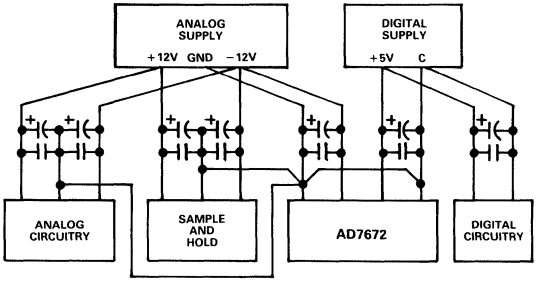


Figure 23. Power Supply Grounding Practice

DATA ACQUISITION APPLICATION

Figure 24 shows a typical data acquisition circuit designed for a microprocessor environment. The corresponding PCB layout and silk screen are shown in Figures 28 to 30. The analog input is applied to a Sample-and-Hold Amplifier (SHA) which can either be an AD683, an AD681 or an AD585. (See Figures 25 and 26.) A voltage reference (AD588) provides the appropriate biasing for any of the three analog input ranges. The data bus outputs are buffered with 74HC374 latches. These provide data bus isolation and improve data access time. Data access time is reduced to under 30ns allowing interfacing to practically any microprocessor including the high-speed DSP processors. Data format can either be a complete parallel load for 16-bit microprocessors or a two byte load for 8-bit microprocesssors.

Bus activity on the AD7672 $\overline{CS}$ and $\overline{RD}$ inputs during conversion can feedthrough to the comparator and cause LSB errors. Ideally these signals should be inactive during conversion. One way of achieving this is to force them into an inactive state by gating them with $\overline{BUSY}$ as shown in Figure 24. R2 and C26 are included to provide a delay of approximately 100ns. This compensates for the data setup time after $\overline{BUSY}$ goes high ensuring valid data gets loaded into IC5 and IC6.

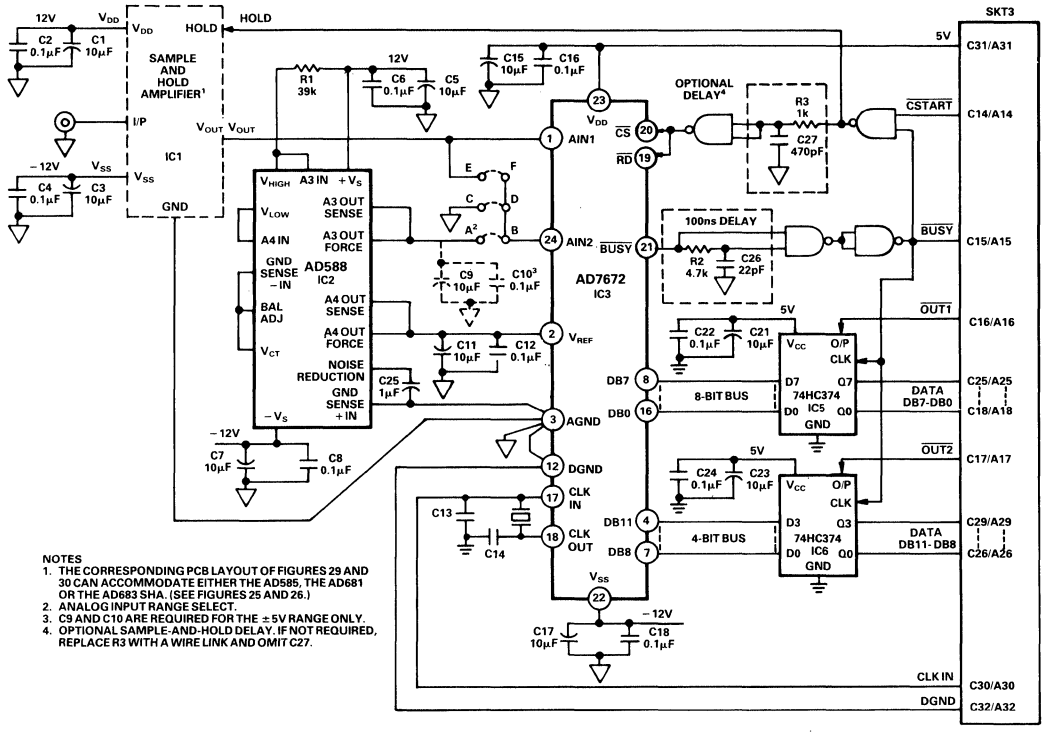


Figure 24. Data Acquisition Circuit Using the AD7672

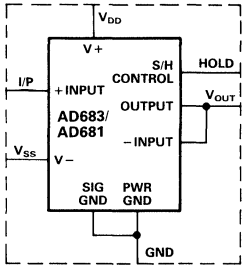


Figure 25. AD683/AD681 SHA Connection Diagram for Figure 24

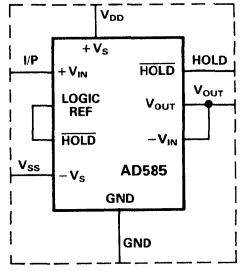


Figure 26. AD585 SHA Connection Diagram for Figure 24

SAMPLE-AND-HOLD OPERATION

The PCB layout of Figures 29 and 30 can accommodate either the AD683, the AD681 or the AD585 sample-and-hold amplifier. The choice of SHA depends mainly on the acquisition time required.

However, another important consideration with sample-and-hold interfacing is settling time. This is the time required by the sample and hold amplifier output to settle after receiving a HOLD command. To allow for this, there must be a delay which is at least as long as the SHA settling time between the HOLD command and the AD7672's first MSB decision. When initiating a conversion, if the SHA's HOLD input and the AD7672 $\overline{CS}$ and $\overline{RD}$ inputs are asserted together, then this delay can vary from one to two clock periods. This corresponds to a delay of 800ns to 1600ns for the AD7672XX10, 400ns to 800ns for the AD7672XX05 and 250ns to 500ns for the AD7672XX03. Under these conditions a settling time of less than 200ns is required by the SHA to satisfy all speed grades of the AD7672. This figure allows an additional 50ns for the AD7672XX03 internal comparator. Both the AD683 and AD681 meet this condition. However, since the AD585 is specified with a settling time of 500ns, the 10μs version of the AD7672 is the only one of the three-speed grades guaranteed to meet this timing requirement. This settling time requirement may be met with the higher speed grades by using either an additional circuit delay or by synchronizing the control inputs with the clock. Both of these methods are discussed below.

AD7672 – AD585 INTERFACE

The 500ns settling time requirement of the AD585 must be allowed for, at the start of conversion when interfacing to the 3μs and 5μs versions of the AD7672. It may be achieved for the 5μs version by using either one of two methods. The first is to synchronize the control inputs with the ADC clock as follows; when initiating a conversion $\overline{CS}$ and $\overline{RD}$ ($\overline{CSTART}$ in Figure 24) should go low on a falling CLK IN edge. This guarantees two clock periods between conversion start and the first MSB decision.

The second method will work for both the 3μs and 5μs parts. It compensates for settling time by inserting an external delay between the AD7672 $\overline{CS}$ and $\overline{RD}$ inputs and the AD585 HOLD input. The length of this delay should be equal to the sample-and-hold amplifier settling time. It is shown as an optional RC delay in Figure 24 which must be bypassed if not used. Note it is not required for the slower 10μs, AD7672XX10 or when either the AD683 or the AD681 is used with any speed grade of the AD7672.

INPUT RANGE SELECT OPTIONS

There are three analog input ranges which are user selectable by placing links on the PCB as shown in Table I below. These options are located between IC2 and IC3.

Range (Volts)	Links Required		
0 to 5	Connect E to F	:	A–B, C–D = Open Circuit
0 to 10*	Connect C to D	:	A–B, E–F = Open Circuit
−5 to +5	Connect A to B	:	C–D, E–F = Open Circuit

*Due to headroom limitations at 12V power supplies, the AD585 sample-and-hold amplifier is not suitable for the 0–10V range.

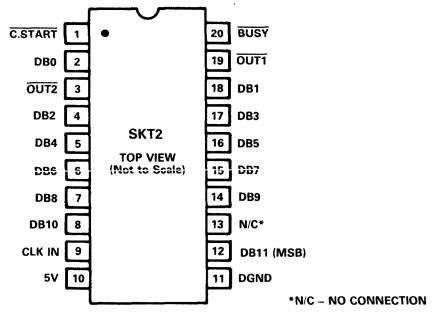
Table I. Input Range Link Options

EXTERNAL CONNECTIONS

The PCB layout is designed so that all external connections except the V_{DD} and V_{SS} power supplies can be made by any of three ways:

1. 32 way single sided edge connector,
2. Euro card connector, SKT3
3. 20-pin DIP socket. (SKT2 on the silk screen).

The pinout for the 20-pin DIP socket is shown below and the other pinouts are shown in Figures 24 and 30. The V_{DD} and V_{SS} power supplies are connected at the top of the board (see Figure 28, Silk Screen).



PIN FUNCTION DESCRIPTION

$\overline{C.START}$	Conversion Start going low initiates a conversion.
$\overline{OUT1}$	Active Low, three-state control for DB7-DB0.
$\overline{OUT2}$	Active Low, three-state control for DB11-DB8.
$\overline{BUSY}$	AD7672 Status Output. $\overline{BUSY}$ is low during conversion.
CLK IN	AD7672 CLK IN input. Note the board has a facility for an on-board crystal oscillator or a ceramic resonator.
DB11-DB0	Three-State data outputs.
5V	5V power supply.
DGND	Digital Ground

COMPONENT LIST

IC1	Sample and hold, IC1 can occupy one of two positions depending on the sample-and-hold model. These positions are outlined in Figure 27. The plated-through holes denoted by "1" are configured for the AD683/AD681 and the plated-through holes denoted by "2" are configured for the AD585.

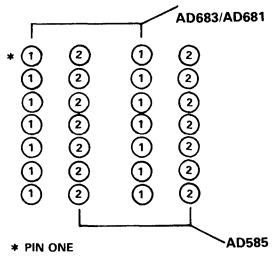


Figure 27. PCB Sample-and-Hold Amplifier Options

IC2	AD588 Voltage Reference.
IC3	AD7672 Analog-to-Digital Converter.
IC4	74HC00 Quad NAND Gate.
IC5, IC6	74HC374 Ocatal Latches with Three-State Outputs.
C1, C3, C5, C7, C11, C15, C17, C19, C21, C23	10μF Capacitors.
C2, C4, C6, C8, C12, C16, C18, C20, C22, C24	0.1μF Capacitors.
C25	1μF
C9	10μF Capacitor, Required for ±5V Range Only.
C10	0.1μF Capacitor, Required for ±5V Range Only.
C13, C14	Crystal/Ceramic Resonator Capacitors Values Depend on the Manufacturer. For example: 4MHz XTAL (HC – 18/U) from IQD; C13, C14 = 30pF; 2.5MHz (HC 18/U) and 1.2288MHz (HC 33/U) from Anderson; No Capacitors Required.
C26	22pF.
C27	470pF, Sample-and-Hold Delay (See Sample-and-Hold Operation) Omit C27 if this delay is not required.
R1	39k.
R2	4.7k.
R3	1k, Sample-and-Hold Delay (See Sample-and-Hold Operation) Replace with a wire link if this delay is not required.
SKT1	Subminiature Connector from Greenpar.

TEST POINTS

TP1 – Analog Input
TP2 – Analog Ground
TP3 – CLK IN
TP4 – AD7672 $\overline{\text{BUSY}}$ Output

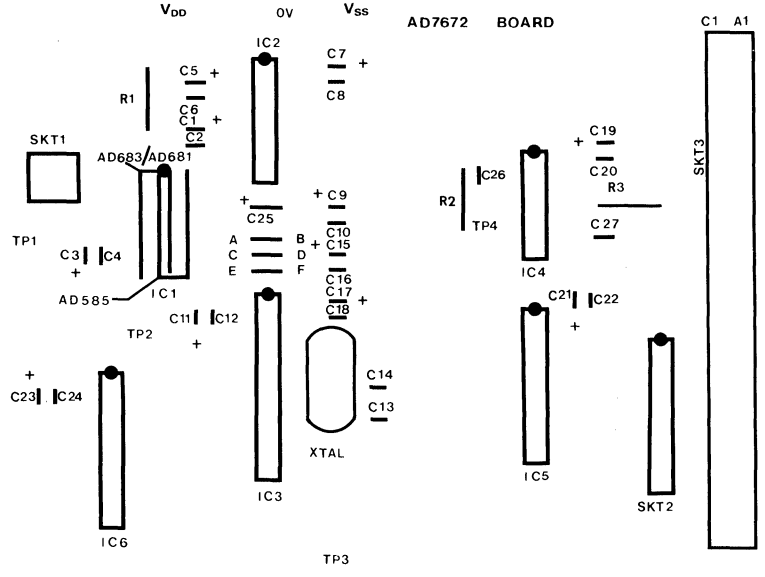


Figure 28. PCB Silk Screen for Figure 24

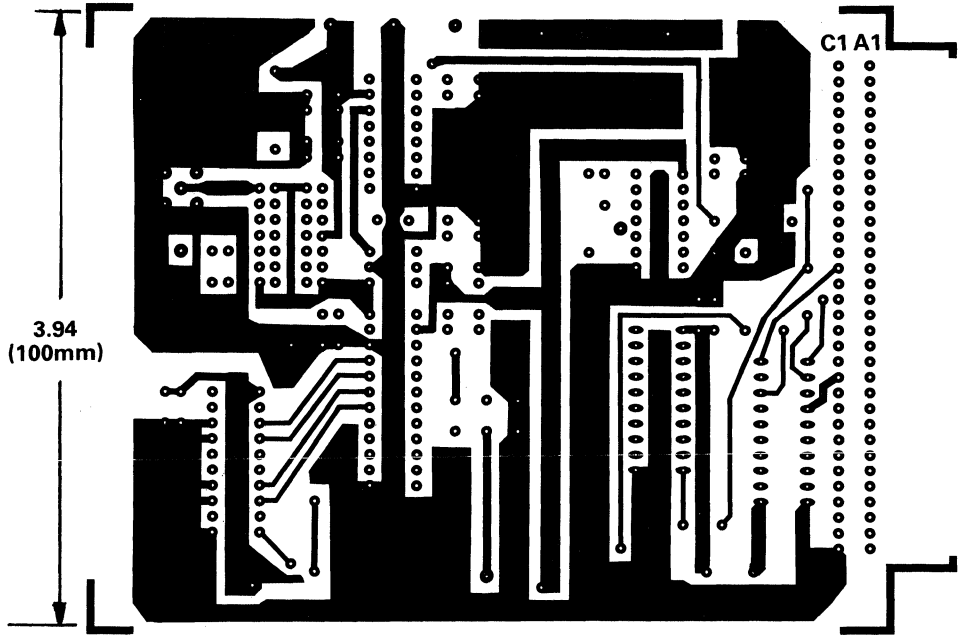


Figure 29. PCB Component Side Layout for Figure 24

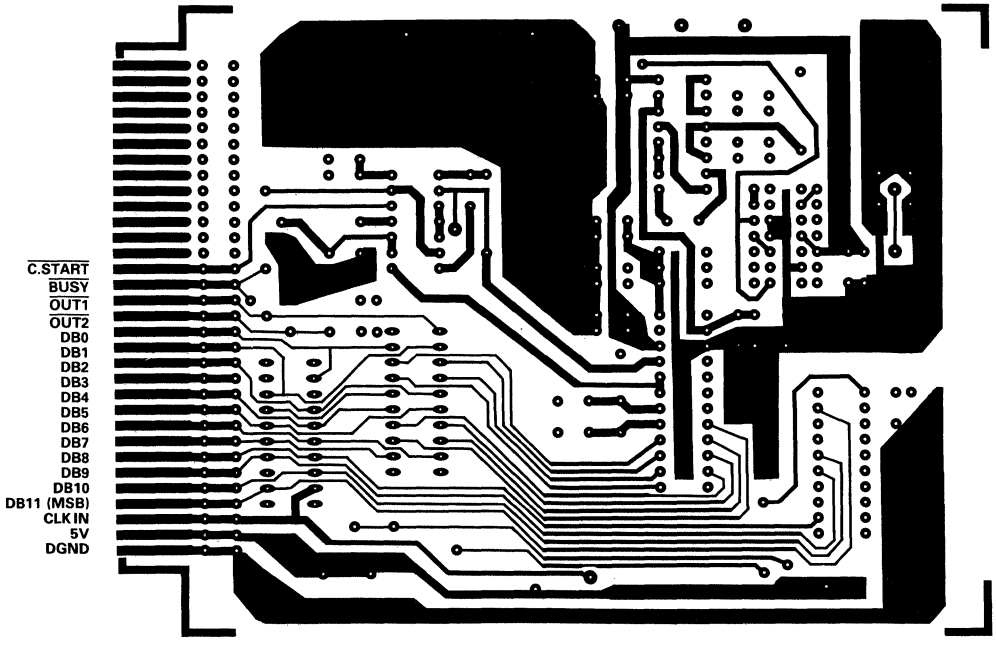


Figure 30. PCB Solder Side Layout for Figure 24

LC²MOS Analog I/O Port

AD7769

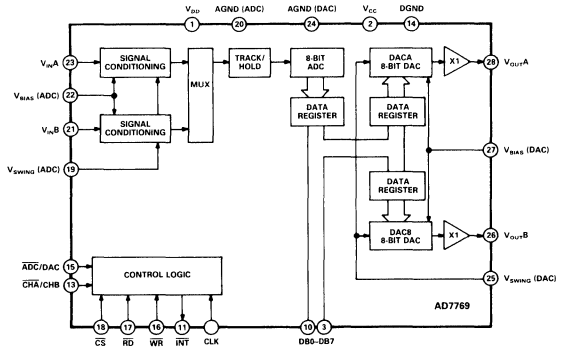
FEATURES

Two-Channel, 8-Bit 2.5 μs ADC
Two 8-Bit, 2.5 μs DACs with Output Amplifiers
Span and Offset of ADC and DAC Independently Adjustable
Low Power

APPLICATIONS

Winchester Disk Servo Controllers
Floppy Disk Microstepping
Closed Loop Servo Systems

AD7769 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7769 is a complete, two-channel, 8-bit, analog I/O port. It has versatile input and output signal conditioning features (patent pending) that make it ideal for use in head-positioning servos in Winchester disk systems. It is equally suitable for floppy disk microstepping head positioning, other closed loop digital servo systems and general purpose 8-bit data acquisition.

The AD7769 contains a high speed successive approximation ADC, preceded by a two-channel multiplexer and signal conditioning circuits. The input span of the ADC and the offset of the zero point from ground can be independently set by applying ground referenced voltages. The AD7769 also contains two independent, fast settling, 8-bit DACs with output amplifiers. The output span and offset voltage of the DACs can be set independently of those of the ADC. This makes the AD7769 especially useful in disk drives, where only a positive supply rail is available and the ranges of the ADC and DACs must be referenced to some positive voltage less than the supply.

The AD7769 is easily interfaced to a standard 8-bit mpu bus via an 8-bit data port and standard microprocessor control lines.

The AD7769 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-pin plastic DIP and 28-terminal PLCC package.

PRODUCT HIGHLIGHTS

1. Two-Channel, 8-Bit Analog I/O port on a Single Chip.
   The AD7769 contains a two-channel, high speed ADC with input signal conditioning and two, fast settling 8-bit DACs with output amplifiers, on a single chip.
2. Independent Control of Span and Offset.
   The input voltage span of the ADC and the midpoint of the transfer function, the output voltage swing of the two DACs and the half-scale output voltage, can be set independently by applying ground referenced control voltages.
3. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications, the AD7769 is specified with ac parameters including signal-to-noise ratio, distortion and signal bandwidth.
4. Fast Microprocessor Interface.
   The AD7669 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 65 ns and a Write pulse width less than 90 ns.

SPECIFICATIONS

ADC SPECIFICATIONS

(V_{DD} = +12 V ±10%; V_{CC} = +5 V ±5%; AGND [ADC] = AGND [DAC] = DGND = 0 V; V_{BIAS} [ADC] = +5 V; V_{SWING} [ADC] = +2.5 V; f_{CLK} = 5 MHz external. All specifications T_{min} to T_{max}[1] unless otherwise stated.)

Parameter	J Version	K Version	Units	Conditions/Comments
DC ACCURACY				
Resolution	8	*	Bits	
Relative Accuracy	±1	*	LSB max	See Terminology
Differential Nonlinearity	±1	*	LSB max	No Missing Codes. See Terminology.
Bias Offset Error				See Terminology
+25°C	±3.0	±2.5	LSB max	
T_{min} to T_{max}	±3.5	±3.0	LSB max	
Bias Offset Match				Channel A to Channel B
+25°C	±2.5	*	LSB max	
T_{min} to T_{max}	±3.5	*	LSB max	
Plus or Minus Full-Scale Error				See Terminology
+25°C	±2.0	*	LSB max	
T_{min} to T_{max}	±2.5	*	LSB max	
Plus or Minus Full-Scale Match				Channel A to Channel B
+25°C	±3.5	*	LSB max	
T_{min} to T_{max}	±4	*	LSB max	
ADC TO DAC MATCHING				Channel A/B to V_{OUT} A/B
Bias Offset Match				V_{BIAS} (DAC) = +5 V, V_{SWING} (DAC) = +2.5 V.
+25°C	±3.5	±2.5	LSB max	
T_{min} to T_{max}	±4.0	±3.5	LSB max	
Plus or Minus Full-Scale Match				
+25°C	±3.5	*	LSB max	
T_{min} to T_{max}	±4.0	*	LSB max	
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio (SNR)	44	*	dB min	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 400 kHz
Total Harmonic Distortion (THD)	48	*	dB max	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 400 kHz
Intermodulation Distortion (IMD)	60	*	dB typ	f_a = 99 kHz, f_b = 96.7 kHz with $f_{SAMPLING}$ = 400 kHz
Frequency Response	0.1	*	dB typ	V_{IN} = Full-Scale, dc to 200 kHz Sine Wave
ANALOG INPUTS				
Input Voltage Ranges, $V_{IN}A$, $V_{IN}B$	$V_{BIAS} - V_{SWING}$ or 0		V min	Whichever Is the Higher
	$V_{BIAS} + V_{SWING}$ or 9.8		V max	Whichever Is the Lower
Input Currents, $I_{IN}A$, $I_{IN}B$	±0.4	*	mA max	
ADC REFERENCE INPUTS				
Input Voltage Levels				
V_{BIAS} (ADC)	2/6.8	*	V min/max	With Respect to AGND (ADC). For Specified Performance.
V_{SWING} (ADC)	2.0/3.0	*	V min/max	With Respect to AGND (ADC). For Specified Performance.
Input Currents				
V_{BIAS} (ADC) Input	±800	*	µA max	
V_{SWING} (ADC) Input	±1	*	µA max	
LOGIC OUTPUTS				
DB0–DB7, $\overline{INT}$				
V_{OL}, Output Low Voltage	0.4	*	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	*	V min	I_{SOURCE} = 200 µA
DB0–DB7				
Floating State Leakage Current	±10	*	µA max	
Floating State Capacitance[2]	10	*	pF max	
Output Coding	Offset Binary			
POWER REQUIREMENTS				
V_{CC} Range	4.75/5.25	*	V min/Vmax	For Specified Performance. The Part Will Function with V_{CC} = 5 V ±10% with Degraded Performance.
V_{DD} Range	10.8/13.2	*	V min/V max	For Specified Performance
I_{DD} @ +25°C	20	*	mA max	For ADC and DAC: V_{BIAS} = 5.0 V; V_{SWING} = 3.0 V; $V_{IN}A$, $V_{IN}B$ = V_{BIAS}; DAC Code = FF (Hex); DACA and DACB Load = 5 kΩ to AGND (DAC). Typically I_{DD} = 14 mA.
T_{min} to T_{max}	22	*	mA max	
I_{CC} @ +25°C	5	*	mA max	Logic Inputs = 2.4 V, CLK Input = 0.8 V. Typically I_{CC} = 1.5 mA.
T_{min} to T_{max}	6	*	mA max	

NOTES

[1]Temperature range as follows: J, K Versions; 0 to +70°C.

[2]Sample tested at +25°C to ensure compliance.

*Specification same as J Version.

Specifications subject to change without notice.

DACA, DACB SPECIFICATIONS

(V_{DD} = +12 V ±10%; V_{CC} = +5 V ±5%; AGND [DAC] = AGND [ADC] = DGND = 0 V; V_{BIAS} [DAC] = +5 V; V_{SWING} [DAC] = +2.5 V; V_{OUT}A, V_{OUT}B load to AGND [DAC], R_L = 5 kΩ, C_L = 100 pF. All specifications T_{min} to T_{max}[1] unless otherwise stated.)

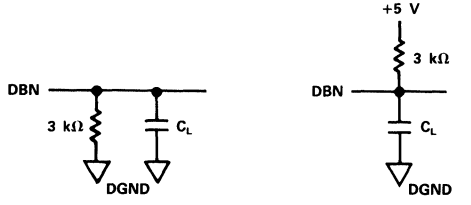
Parameter	J Version	K Version	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	*	Bits	
Relative Accuracy	±1	*	LSB max	See Terminology
Differential Nonlinearity	±1	*	LSB max	Guaranteed Monotonic. See Terminology.
Bias Offset Error				See Terminology
+25°C	±2.0	*	LSB max	
T_{min} to T_{max}	±2.5	*	LSB max	
Bias Offset Match				V_{OUT} A to V_{OUT} B
+25°C	±2.5	*	LSB max	
T_{min} to T_{max}	±3.5	*	LSB max	
Plus or Minus Full-Scale Error				See Terminology
+25°C	±2.0	±1.5	LSB max	
T_{min} to T_{max}	±2.0	*	LSB max	
Plus or Minus Full-Scale Match				V_{OUT} A to V_{OUT} B
+25°C	±3.5	*	LSB max	
T_{min} to T_{max}	±4.0	*	LSB max	
ADC to DAC MATCHING	As Per ADC Specifications			
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio (SNR)	44	*	dB min	V_{OUT} = 20 kHz Full-Scale Sine Wave With $f_{SAMPLING}$ = 400 kHz
Total Harmonic Distortion (THD)	48	*	dB max	V_{OUT} = 20 kHz Full-Scale Sine Wave With $f_{SAMPLING}$ = 400 kHz
Intermodulation Distortion (IMD)	55	*	dB typ	f_a = 18.4 kHz, f_b = 14.5 kHz with $f_{SAMPLING}$ = 400 kHz
ANALOG OUTPUTS				
Output Voltage Ranges				
V_{OUT}A, V_{OUT}B	V_{BIAS} − V_{SWING} or 0.5		V min	Whichever Is the Higher
	V_{BIAS} + V_{SWING} or V_{DD} −2.0		V max	Whichever Is the Lower
DC Output Impedance	0.5	*	Ω typ	
Short-Circuit Current	20	*	mA typ	
DAC REFERENCE INPUTS				
Input Voltage Levels				
V_{BIAS} (DAC)	3/6.8	*	V min/max	With Respect to AGND (DAC). For Specified Performance.
V_{SWING} (DAC)	2.0/3.0	*	V min/max	With Respect to AGND (DAC). For Specified Performance.
Input Currents				
V_{BIAS} (DAC) Input	±2	*	μA max	
V_{SWING} (DAC) Input	±1	*	μA max	
AC CHARACTERISTICS[2]				
Voltage Output Settling Time	4	*	μs max	Settling Time to Within ±1/2 LSB of Final Value. Typically 2.5 μs.
Digital-to-Analog Glitch Impulse	30	*	nV sec typ	See Terminology
Digital Feedthrough	1	*	nV sec typ	See Terminology
LOGIC INPUTS				
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ADC/$\overline{DAC}$, $\overline{CHA}$/CHB, DB0–DB7				
Input Low Voltage, V_{INL}	0.8	*	V max	
Input High Voltage, V_{INH}	2.4	*	V min	
Input Leakage Current	±10	*	μA max	
Input Capacitance	10	*	pF max	
CLK				
Input Low Voltage	0.8	*	V max	External Clock. For Internal Clock Operation Connect
Input High Voltage	2.4	*	V min	the CLK Pin to V_{DD}.
Input Leakage Current	±10	*	μA max	
DB0–DB7				
Input Coding	Offset Binary			
POWER REQUIREMENTS	As per ADC Specifications			

NOTES
[1]Temperature range as follows: J, K Versions; 0 to +70°C.
[2]Sample tested at +25°C to ensure compliance.
*Specifications same as J Version.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{CC} = +5 V ±5%; V_{DD} = +12 V ±10%; AGND [ADC] = AGND [DAC] = DGND = 0 V. For ADC and DAC, V_{BIAS} = +5 V, V_{SWING} = +2.5 V.)

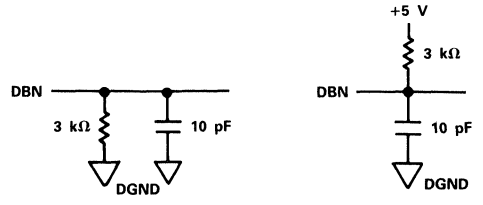
Parameter	Label	Limit at +25°C	Limit at T_{min}, T_{max}	Units	Test Conditions/Comments
ADC/DAC CONTROL TIMING					
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1	0	0	ns min	
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2	0	0	ns min	
$\overline{ADC}$/DAC to $\overline{WR}$ Setup Time	t_3	0	0	ns	
$\overline{ADC}$/DAC to $\overline{WR}$ Hold Time	t_4	0	0	ns min	
$\overline{CHA}$/CHB to $\overline{WR}$ Setup Time	t_5	0	0	ns min	
$\overline{CHA}$/CHB to $\overline{WR}$ Hold Time	t_6	0	0	ns min	
$\overline{WR}$ Pulse Width	t_7	80	80	ns min	
ADC CONVERSION TIMING					
Using External Clock					Load Circuit of Figure 3, C_L = 20 pF
$\overline{WR}$ to $\overline{INT}$ Low Delay	t_8	2.6	2.6	µs max	
Using Internal Clock					Load Circuit of Figure 3, C_L = 20 pF
$\overline{WR}$ to $\overline{INT}$ Low Delay	t_8	1.9/3.0	1.9/3.0	µs min/max	Typically 2.5 µs
$\overline{WR}$ to $\overline{INT}$ High Delay	t_9	85	85	ns max	Load Circuit of Figure 3, C_L = 20 pF
	t_9	120	120	ns max	Load Circuit of Figure 3, C_L = 100 pF
$\overline{WR}$ to Data Valid Delay[3]	t_{10}	t_8+70	t_8+70	ns max	Load Circuit of Figure 1, C_L = 20 pF
	t_{10}	t_8+110	t_8+110	ns max	Load Circuit of Figure 1, C_L = 100 pF
ADC READ TIMING					
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{11}	0	0	ns min	
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{12}	0	0	ns min	
$\overline{RD}$ to Data Valid Delay[3]	t_{13}	15/65	15/65	ns min/max	Load Circuit of Figure 1, C_L = 20 pF
	t_{13}	30/100	30/100	ns min/max	Load Circuit of Figure 1, C_L = 100 pF
Bus Relinquish Time after $\overline{RD}$ High[4]	t_{14}	15/65	15/65	ns min/max	Load Circuit of Figure 2
$\overline{RD}$ to $\overline{INT}$ High Delay	t_{15}	80	80	ns max	Load Circuit of Figure 3, C_L = 20 pF
	t_{15}	110	110	ns max	Load Circuit of Figure 3, C_L = 100 pF
$\overline{RD}$ Pulse Width	t_{16}	t_{13}	t_{13}	ns min	Determined by t_{13}
DAC WRITE TIMING					
Data Valid to $\overline{WR}$ Setup Time	t_{17}	65	65	ns min	
Data Valid to $\overline{WR}$ Hold Time	t_{18}	15	20	ns min	
$\overline{WR}$ to DAC Output Settling Time	t_{19}	4	4	µs max	Load Circuit of Figure 4

NOTES
[1]See Figures 11, 12 and 13.
[2]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[3]t_{10} and t_{13} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_{14} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Bus Relinquish Time Test

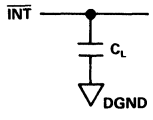


Figure 3. Load Circuit for $\overline{RD}$ and $\overline{WR}$ to $\overline{INT}$ Delay Test

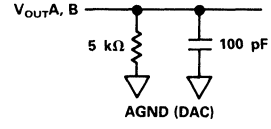


Figure 4. Load Circuit for DAC Settling Time Test

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND or DGND . . . . . −0.3 V, +15 V
V_{CC} to DGND . . . . . −0.3 V, V_{DD} +0.3 V or 7 V (Whichever is Lower)
AGND to DGND . . . . . −0.3 V, V_{DD} +0.3 V
Digital Inputs to DGND
(Pins 12, 13, 15–18) . . . . . −0.3 V, V_{DD} +0.3V
Digital Outputs to DGND
(Pins 3–10, 11) . . . . . − 0.3 V, V_{CC} + 0.3 V
Analog Inputs to AGND . . . . . −0.3 V, V_{DD} +0.3 V
Analog Outputs to AGND . . . . . −0.3 V, V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . 0 to +70°C
Power Dissipation (Any Package)
to +75°C . . . . . 500 mW
Derates Above +75°C by . . . . . 6 mW/°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

3

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

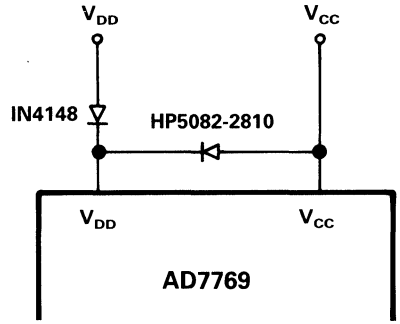
ORDERING INFORMATION

Temperature Range and Package Options[1]
0 to +70°C

Plastic DIP (N-28)	PLCC (P-28A)[2]
AD7769JN	AD7769JP
AD7769KN	AD7769KP

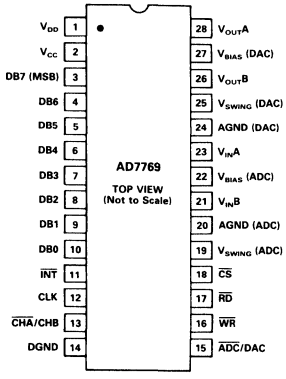
NOTES
[1]See Section 14 for package outline information.
[2]PLCC:Plastic Leaded Chip Carrier.

NOTE
Do not allow V_{CC} to exceed V_{DD} by more than 0.3 V. In cases where this can happen the diode protection scheme shown below is recommended.

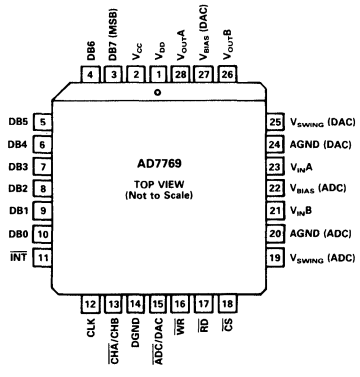


PIN CONFIGURATION

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{DD}	+12 V Power Supply. This powers the analog circuitry.
2	V_{CC}	+5 V Power Supply. This powers the logic circuitry.
3–10	DB7–DB0	Input/Output Data Bus. A bidirectional data port from which ADC output data may be read and to which DAC input data may be written. DB7 is the Most Significant Bit.
11	$\overline{INT}$	Interrupt Output (active low). $\overline{INT}$ is set high on the falling edge of $\overline{RD}$ or $\overline{WR}$ to the ADC and goes low at the end of a conversion.
12	CLK	Clock input. A clock is required for the ADC. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{DD} enables the internal clock oscillator. With an external clock, the mark-space ratio can vary from 30/70 to 70/30.
13	$\overline{CHA}$/CHB	Channel A/Channel B Select Input. Selects Channel A or Channel B of the DAC or ADC. Used in conjunction with $\overline{WR}$, $\overline{RD}$, $\overline{CS}$ and $\overline{ADC}$/DAC for read or write operations.
14	DGND	Digital Ground.
15	$\overline{ADC}$/DAC	ADC or DAC Select Input. Selects either the ADC or the DAC for read or write operations in conjunction with $\overline{WR}$, $\overline{RD}$, $\overline{CS}$ and $\overline{CHA}$/CHB.
16	$\overline{WR}$	Write Input (edge triggered). This is used in conjunction with the $\overline{ADC}$/DAC, $\overline{CHA}$/CHB and $\overline{CS}$ control inputs to start an ADC conversion or write data to the DAC. An ADC conversion starts on the rising edge of $\overline{WR}$.
17	$\overline{RD}$	Read Input (active low). This input must be low to access data from the ADC.
18	$\overline{CS}$	Chip Select Input (active low). The device is selected when this input is low.
19	V_{SWING} (ADC)	ADC Reference Input. The voltage applied to this pin with respect to AGND (ADC) sets the input voltage Full-Scale Range (FSR) of the ADC. V_{IN} (FSR) = 2 V_{SWING} (ADC).
20	AGND (ADC)	ADC Analog Ground.
21	V_{IN}B	Analog Input for Channel B. See V_{IN}A description.
22	V_{BIAS} (ADC)	ADC Reference Input. The voltage applied to this pin with respect to AGND (ADC) sets the midpoint of the ADC transfer function.
23	V_{IN}A	Analog Input for Channel A. The input voltage range of both ADC channels is given by: V_{IN} A/B = V_{BIAS} (ADC) ±V_{SWING} (ADC).
24	AGND (DAC)	DAC Analog Ground.
25	V_{SWING} (DAC)	DAC Reference Input. The voltage applied to this pin with respect to AGND (DAC) sets the output voltage Full-Scale Range (FSR) of the DACs. V_{OUT} (FSR) = 2 V_{SWING} (DAC).
26	V_{OUT}B	Analog Output Voltage from DAC B. See V_{OUT}A description.
27	V_{BIAS} (DAC)	DAC Reference Input. The voltage applied to this pin with respect to AGND (DAC) sets the midpoint output voltage of the DACs.
28	V_{OUT}A	Analog Output Voltage from DAC A. The output voltage range of both DACs is given by: V_{OUT} A/B = V_{BIAS} (DAC) ± V_{SWING} (DAC).

TERMINOLOGY

Relative Accuracy

For an ADC, Relative Accuracy or endpoint nonlinearity is the maximum deviation, in LSBs, of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function, i.e., the 00 to 01 and FE to FF Hex (01111111 to 11111111 Binary) code transitions.

For a DAC, Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function, i.e., those voltages which correspond to codes 00 and FF Hex.

For the specified input and output ranges, 1 LSB = 19.5 mV, but will vary with V_{SWING}. For both DACs and ADC, 1 LSB = 2 V_{SWING} / 256 = FSR / 256.

Differential Nonlinearity

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max ensures monotonicity (DAC) or no missed codes (ADC).

Bias Offset Error

For an ideal ADC, the output code for an input voltage equal to V_{BIAS} (ADC), should be 80 Hex (10000000 binary). The ADC Bias Offset Error is the difference between the actual midpoint voltage for code 80 Hex and V_{BIAS} (ADC), expressed in LSBs.

For an ideal DAC, the output voltage for code 80 Hex should be equal to V_{BIAS} (DAC). The DAC Bias Offset Error is the difference between the actual output voltage and V_{BIAS} (DAC), expressed in LSBs.

Plus and Minus Full-Scale Error

The ADC and DACs in the AD7769 can be considered as devices with bipolar (plus and minus) input ranges, but referred to V_{BIAS} instead of AGND. Plus Full-Scale Error for the ADC is the difference between the actual input voltage at the FE to FF code transition and the ideal input voltage (V_{BIAS} + V_{SWING} −1.5 LSB), expressed in LSBs. Minus Full-Scale Error is similarly specified for the 01 to 00 code transition, relative to the ideal input voltage for this transition (V_{BIAS} − V_{SWING} +0.5 LSB). Plus Full-Scale Error for the DACs is the difference, expressed in LSBs, between the actual output voltage for input code FF and the ideal voltage (V_{BIAS} + V_{SWING} − 1 LSB). Minus Full-Scale Error is similarly specified for code 00, relative to the ideal output voltage (V_{BIAS} − V_{SWING}). Note that Plus and Minus Full-Scale errors for the ADC and the DAC outputs are measured after their respective Bias Offset errors have been adjusted out.

Digital-to-Analog Glitch Impulse

Digital-to-Analog Glitch Impulse is the impulse injected into the analog outputs when the digital inputs change state with either DAC selected. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough

Digital Feedthrough is also a measure of the impulse injected into the analog outputs from the digital inputs but is measured when the DACs are not selected. It is essentially feedthrough across the die and package. It is important in the AD7769 since it is a measure of the glitch impulse transferred to the analog outputs when data is read from the ADC register. It is specified in nV secs and is measured with $\overline{WR}$ high and a digital code change from all 0s to all 1s.

Signal-to-Noise Ratio (SNR)

SNR is the measured Signal-to-Noise Ratio at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for an ideal 8-bit converter, SNR = 49.92 dB.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7769, Total Harmonic Distortion is defined as

$$20\ log\ \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion (IMD)

With inputs consisting of sine waves at two frequencies, f_a and f_b, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mf_a+nf_b, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (f_a+f_b) and (f_a-f_b) and the third order terms include ($2f_a+f_b$), ($2f_a-f_b$), (f_a+2f_b) and (f_a-2f_b).

LOGIC TRUTH TABLE

ADC CHANNEL SELECT AND START CONVERSION

$\overline{CS}$	ADC/$\overline{DAC}$	CHA/$\overline{CHB}$	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	0	X	↓	Note 1	Note 1	1	$\overline{INT}$ Is Set on Falling Edge of $\overline{WR}$.
0	0	0	↓	Note 1	Note 1	1	Select ADC Channel A and Start Conversion.
0	0	1	↓	Note 1	Note 1	1	Select ADC Channel B and Start Conversion.
						0	$\overline{INT}$ Goes Low at End of Conversion.

READ ADC DATA

$\overline{CS}$	ADC/$\overline{DAC}$	CHA/$\overline{CHB}$	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	X	X	X	↓	ADC Data	1	$\overline{INT}$ Is Set High on Falling Edge of $\overline{RD}$.
0	X	X	X	0	ADC Data	1	ADC Data on Data Bus.
0	X	X	X	↓	High-Z	1	Data Outputs High Impedance.

WRITE TO DACA OR DACB

$\overline{CS}$	ADC/$\overline{DAC}$	CHA/$\overline{CHB}$	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	1	0	↓	1	µP Data	N/C	µP Writing Data to DACA.
0	1	1	↓	1	µP Data	N/C	µP Writing Data to DACB.
0	1	0	↓	0	ADC Data	N/C	Data from Last ADC Conversion Will Be Written to DACA.
0	1	1	↓	0	ADC Data	N/C	Data from Last ADC Conversion Will Be Written to DACB.
1	X	X	X	X	High-Z	N/C	No Operation.

NOTES
[1]If $\overline{RD}$ = 1, DB0–DB7 will remain high impedance. If $\overline{RD}$ = 0, DB0–DB7 will output previous ADC data. The $\overline{RD}$ input should not change during a conversion.
[2]X = Don't Care.
[3]N/C = No Change.

CIRCUIT DESCRIPTION

Analog Inputs and Outputs

The AD7769 provides the analog-to-digital and digital-to-analog conversion functions required between the microcontroller and the servo power amplifier in digital servo systems. It is intended primarily for closed loop head positioning in Winchester disk drives but may also be used for microstepping in drives with stepper motor head positioning or other servo applications. The AD7769 contains a high speed, 8-bit, sampling ADC with two input channels and two 8-bit DACs with output buffer amplifiers. A unique feature of the AD7769 is the input and output signal conditioning circuitry which allows the analog input and output voltages to be referred to a point other than analog ground. The input range and offset of the ADC, the output swing and offset of the DACs may be adjusted independently by the application of ground-referenced, positive control voltages, V_{BIAS} (ADC), V_{SWING} (ADC), V_{BIAS} (DAC) and V_{SWING} (DAC). Thus, for example, the peak-to-peak output swing of the DACs could be set to 3 V above and 3 V below a bias voltage of 5 V.

Figures 5 and 6 show the transfer functions of the ADC and DACs and their relationship to V_{BIAS} and V_{SWING}. The midpoint code of the ADC, 80 Hex (10000000 Binary), occurs at an input voltage equal to V_{BIAS}. The input FSR of the ADC is equal to 2 V_{SWING}, so that the Plus Full-Scale code transition (FE to FF Hex) occurs at a voltage equal to V_{BIAS} + V_{SWING} −1.5 LSBs and the Minus Full-Scale code transition (01 to 00 Hex) occurs at a voltage V_{BIAS} − V_{SWING} +0.5 LSBs. The transfer function of the DACs bears a similar relationship to V_{BIAS} and V_{SWING}. The DAC output voltage for code 80 Hex (10000000 binary) is equal to V_{BIAS}, whilst FF Hex (11111111 binary) gives an output voltage of V_{BIAS} + V_{SWING} −1 LSB (Plus Full-Scale) and 00 Hex gives an output voltage of V_{BIAS} − V_{SWING} (Minus Full-Scale).

The ability to refer input and output signals to some voltage other than ground is of particular importance in disk drive applications. Typically, only +5 V digital and +12 V analog supply voltages are available, and the analog signals are often referred to a voltage around half the analog supply.

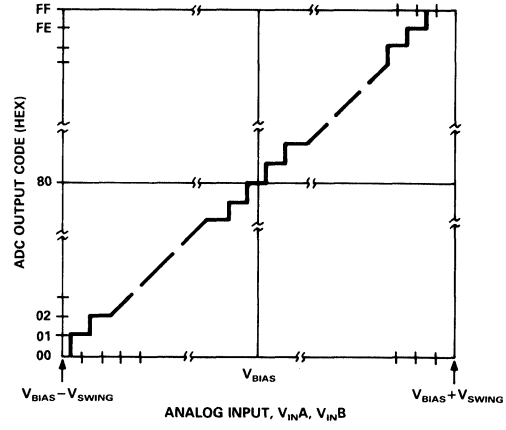


Figure 5. ADC Transfer Function

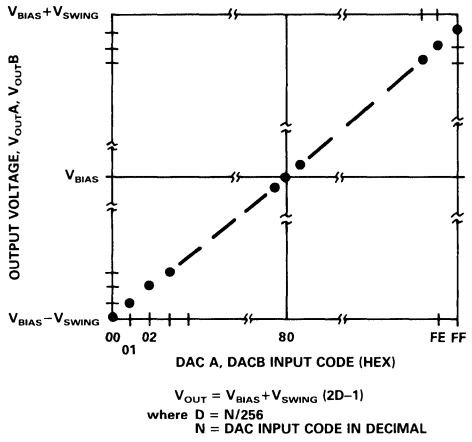


Figure 6. DAC Transfer Function

Driving the Analog Inputs and Reference Inputs

The analog inputs, $V_{IN}A$ and $V_{IN}B$, must be driven from low output impedance sources, such as from op amps. In addition, V_{BIAS} (ADC) must be driven from a similar type low impedance source (e.g., voltage reference).

Op amps are not required to drive the V_{SWING} (ADC), V_{BIAS} (DAC) and V_{SWING} (DAC) inputs as these are high impedance inputs (200 nA typical input current) that feed into on-chip buffer amplifiers. The reference voltages for these inputs can be derived using suitable resistor divider networks.

The analog reference available in the disk drive system can be used to set the bias voltage of the AD7769, and could also be attenuated to provide the reference for the input and output swing as shown in Figure 7. The same bias voltage would generally (though not necessarily) be used for the ADC and the DACs, though the input and output ranges might be different.

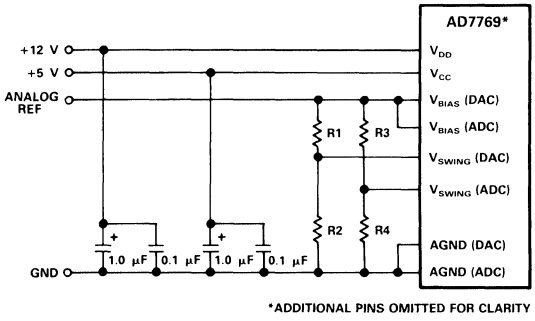


Figure 7. Typical Analog Connections to the AD7769

ADC Conversion Cycle

Figure 8 shows the operating waveforms for a conversion cycle. On the rising edge of $\overline{WR}$, the conversion cycle starts with the acquisition and tracking of the selected ADC channel, $V_{IN}A$ or $V_{IN}B$. The analog input voltage is held 50 ns (typically) after the fourth falling edge of the input CLK following a conversion start. If t_D in Figure 8 is greater than 150 ns, then the falling edge of the input CLK will be seen as the first falling clock edge. If t_D is less than 150 ns, the first falling clock edge to be recognized will not occur until one cycle later.

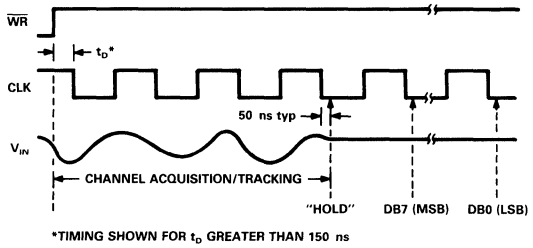


Figure 8. Operating Waveforms Using External Clock

Following the "hold" on the analog input, the MSB decision is made approximately 50 ns after the next falling edge of the input CLK. The succeeding bit decisions are made approximately 50 ns after a CLK edge until conversion is complete. At the end of conversion, the $\overline{INT}$ line goes low 100 ns (typically) after the LSB decision and the SAR contents are transferred to the output latch. The SAR is then reset in readiness for a new conversion.

Track-and-Hold

The track-and-hold (T/H) amplifier on the analog input to the ADC of the AD7769 allows the ADC to accurately convert an input sine wave of 5 V peak-to-peak amplitude up to a frequency of 200 kHz, the Nyquist frequency of the ADC when operated at its maximum throughput rate of 400 kHz. This maximum rate of conversion includes conversion time and time between conversions. Because the input bandwidth of the track-and-hold is much greater than 200 kHz, the input signal should be band limited to avoid folding unwanted signals into the band of interest.

DAC Outputs

The D/A converter outputs are buffered with on-board, high speed op amps that are capable of driving 5 kΩ and 100 pF loads to AGND (DAC). Each output amplifier settles to within 1/2 LSB of its final output value in typically less than 2.5 µs. See Figures 9 and 10 for waveforms of the typical output settling time performance.

The output noise from the amplifiers with full scale on the DACs is typically 200 µV peak-to-peak.

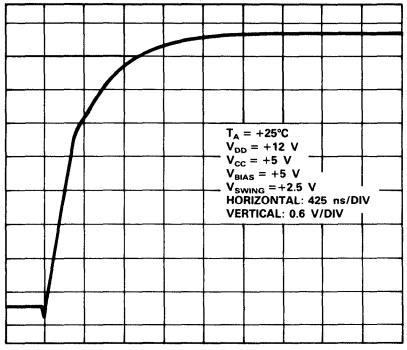


Figure 9. Positive-Going Settling Time

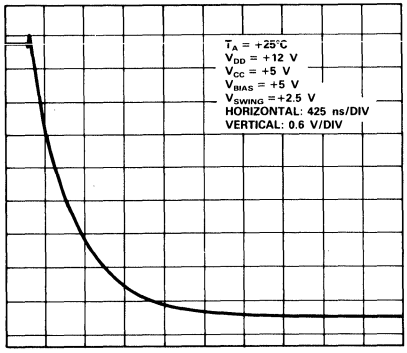


Figure 10. Negative-Going Settling Time

Internal / External Clock Operation

The AD7769 can be operated on either its own internal clock or with an externally applied clock signal . For internal clock operation the CLK input must be tied to V_{DD}. No external components are required. The internal clock typically runs at 5 MHz giving a typical conversion time of 2.5 μs. For external clock operation the CLK input must be driven with a TTL/HCMOS compatible input. The mark/space ratio of the clock signal can vary from 30/70 to 70/30. For an input frequency of 5 MHz, the conversion time is 2.5 μs.

Digital Inputs and Outputs

The AD7769 communicates over a standard, 8-bit microprocessor data bus and is controlled by standard mpu control lines, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{INT}$, plus two address lines, $\overline{ADC}$/DAC and $\overline{CHA}$/CHB, which select the DAC or ADC function and Channel A or Channel B input/output channel. The Chip Select ($\overline{CS}$) line selects the device, Write ($\overline{WR}$) is used to initiate ADC conversions or to write data to the DAC, depending on the state of $\overline{ADC}$/DAC. $\overline{INT}$ is a status flag that indicates completion of a conversion, while $\overline{RD}$ is used to read ADC output data. The 8-bit data port (DB0-DB7) is a bidirectional port into which data can be written to the two DAC registers, and from which data can be read from the ADC register. ADC output data may also be written directly into either of the DAC registers.

These logical operations are detailed in Table I and in the timing diagrams, Figures 11 to 13. Figures 12 and 13 show the fairly straightforward operations of reading ADC data and writing data to the DACs, and need little explanation. Figure 11 shows the timing for ADC channel selection and conversion start. This is more complicated as the state of the data outputs during a conversion depends on $\overline{CS}$ and $\overline{RD}$.

To initiate a conversion (or any other operation) the device must be selected by taking $\overline{CS}$ low. A conversion is started by taking $\overline{WR}$ low, then high again (conversion starts on rising edge of $\overline{WR}$). There are three possibilities for the state of the data outputs during the conversion.

1. If $\overline{RD}$ is held high, the data outputs will be high impedance throughout the conversion.
2. If $\overline{RD}$ and $\overline{CS}$ are both held low until after $\overline{INT}$ goes low, then DB0–DB7 will initially output data from the last conversion. After $\overline{INT}$ goes low the new conversion data will appear on DB0–DB7.
3. If $\overline{RD}$ is held low but $\overline{CS}$ is taken high during the conversion, the device will be de-selected and DB0–DB7 will revert to their high impedance state. This will not affect completion of the conversion, but the data cannot be read, or any other operation performed, until $\overline{CS}$ is taken low again.
4. Note that the state of $\overline{RD}$ should not be changed during a conversion.

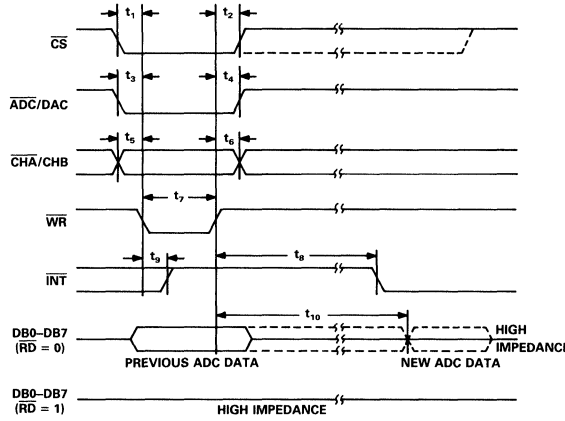


Figure 11. Timing for ADC Channel Select and Conversion Start

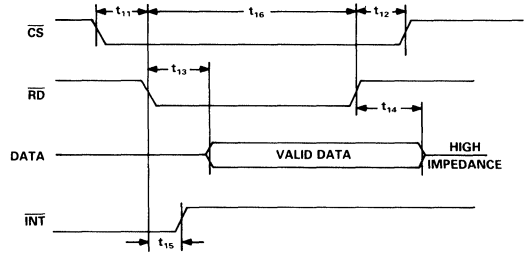
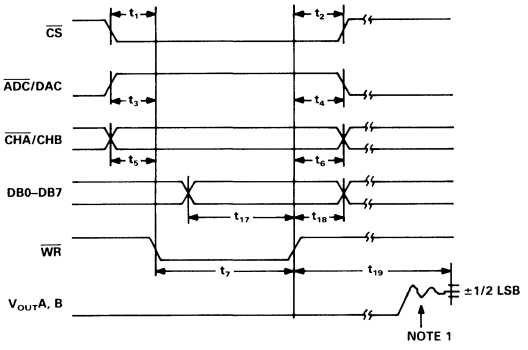


Figure 12. Timing for ADC Data Read



NOTE 1. THE TIME AXIS IS COMPRESSED FOR THIS SECTION OF THE DIAGRAM

Figure 13. Timing for DAC Channel Select and Data Write

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (SNR, Harmonic Distortion, Intermodulation Distortion) of both the ADC and DACs are critical. The AD7769 is specified dynamically as well as with standard dc specifications. Because the track/hold amplifier has a wide bandwidth, an antialiasing filter should be placed on the $V_{IN}A$ and $V_{IN}B$ inputs to avoid aliasing of high frequency noise back into the bands of interest.

The dynamic performance of the ADC is evaluated by applying a sine wave signal of very low distortion to the $V_{IN}A$ or $V_{IN}B$ input which is sampled at a 409.6 kHz sampling rate. A Fast Fourier Transform (FFT) plot or Histogram plot is then generated from which SNR, harmonic distortion and dynamic differential nonlinearity data can be obtained. For the DACs, the codes for an ideal sine wave are stored in PROM and loaded down to the DAC. The output spectrum is analyzed, using a spectrum analyzer to evaluate SNR and harmonic distortion performance. Similarly, for intermodulation distortion, an input (either to VIN or DAC code) consisting of pure sine waves at two frequencies is applied to the AD7769.

Figure 14 shows a 2048 point FFT plot of the ADC with an input signal of 130 kHz. The SNR is 49.2 dB. It can be seen that most of the harmonics are buried in the noise floor. It should be noted that the harmonics are taken into account when calculating the SNR. The relationship between SNR and resolution (N) is expressed by the following equation:

$$SNR = (6.02N + 1.76)\ dB$$

This is for an ideal part with no differential or integral linearity errors. These errors will cause a degradation in SNR. By working backwards from the above equation, it is possible to get a measure of ADC performance expressed in effective number of bits (N). The effective number of bits is plotted versus frequency in Figure 15. The effective number of bits typically falls between 7.7 and 7.9, corresponding to SNR Figures 48.1 and 49.7 dB.

Figure 16 shows a spectrum analyzer plot of the output spectrum from one of the DACs with an ideal sine wave table loaded to the data inputs of the DAC. In this case, the SNR is 47 dB.

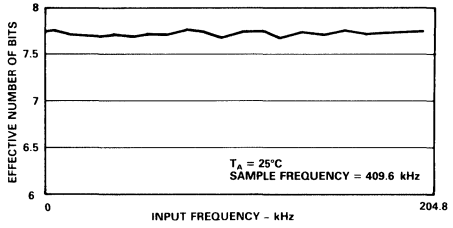


Figure 15. Effective Number of Bits vs. Frequency

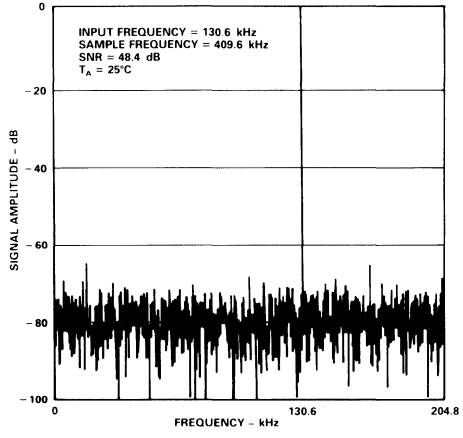


Figure 14. ADC FFT Plot

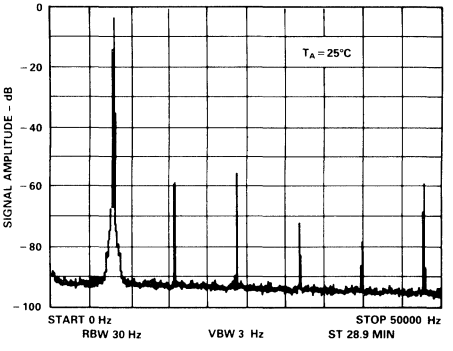


Figure 16. DAC Output Spectrum

Histogram Plot

When a sine wave of specified frequency is applied to the $V_{IN}A$ or $V_{IN}B$ input of the AD7769 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 17 shows a histogram plot for the ADC indicating very small differential nonlinearity and no missing codes for an input frequency of 204 kHz. For a sine wave input, a perfect ADC would produce a probability density function described by the equation:

$$p(V) = \frac{1}{\pi (A^2 - V^2)^{1/2}}$$

where A is the peak amplitude of the sine wave and p (V) the probability of occurrence at a voltage V. The histogram plot of Figure 17 corresponds very well with this shape.

In digital signal processing applications, where the AD7769 is used to sample AC signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. A precise timer or clock source, to start the conversion process, is the best method of generating equidistant sampling intervals.

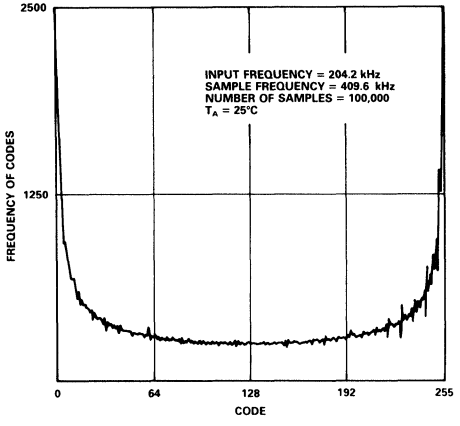


Figure 17. ADC Histogram Plot

MICROPROCESSOR / MICROCOMPUTER INTERFACING

The AD7769 is designed for easy interfacing to microprocessors and microcomputers as a memory mapped peripheral or an I/O device. In addition, the AD7769 high speed bus timing allows direct interfacing to many DSP processors such as the TMS320C10 and ADSP-2101.

AD7769 – TMS320C10 Interface

A typical interface to the TMS320C10 is shown in Figure 18. The AD7769 is mapped at a port address, and the interface is designed for the maximum TMS320C10 clock frequency of 20 MHz.

Conversion is initiated on the selected AD7769 ADC channel using a single I/O instruction, <OUT ADC, A>. The processor then polls $\overline{INT}$ until it goes low before reading the conversion result using an <IN A, ADC> instruction. Writing data to the relevant AD7769 DAC consists of an <OUT DAC, A> instruction.

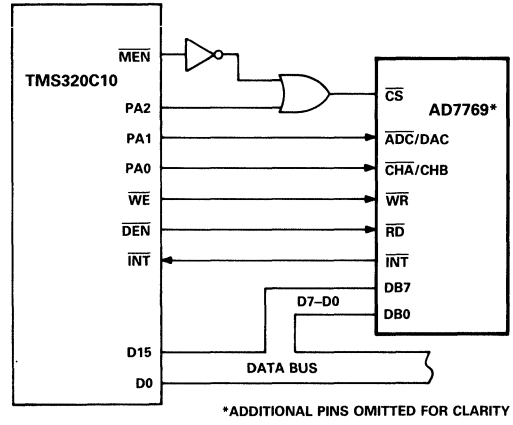


Figure 18. AD7769 to TMS320C10 Interface

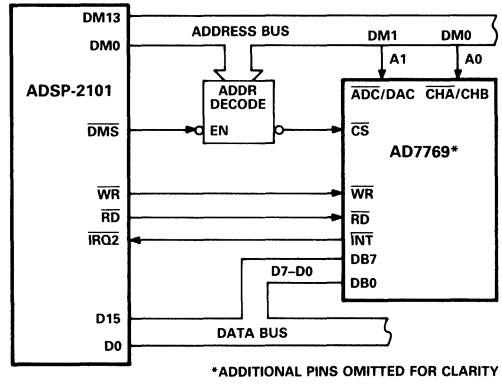


Figure 19. AD7769 to ADSP-2101 Interface

AD7769 – ADSP-2101 Interface

Figure 19 shows a typical interface to the DSP microcomputer, the ADSP-2101. The ADSP-2101 is optimized for high speed numeric processing tasks.

Because the instruction cycle of the ADSP-2101 is very fast (80 ns cycle), the $\overline{WR}$ and $\overline{RD}$ pulses must be stretched out to suit the AD7769. This is easily achieved as the ADSP-2101 memory interface supports slower memories and memory-mapped peripherals (i.e., AD7769) with a programmable wait state generation capability. A number of wait states, from 0 to 7, can be specified for each memory interface. One wait state is sufficient for the interface to the AD7769.

AD7769 – 8051 Interface

A choice of two interface modes are available to the 8051 microcomputer.

Figure 20 shows a typical interface to the 8051 processor bus. It is suitable for the maximum 8051 clock frequency of 12 MHz. In this interface mode, Port 0 provides the multiplexed low order address and data bus and Port 2 provides the high order address bus (A_8–A_{15}).

Figure 21 shows the AD7769 interfaced to the 8051 parallel I/O ports. This interface circuit is simpler to implement than the previous interface to the processor bus, but, in general, the maximum data throughput rate is much slower (for the same clock frequencies). In addition to its simplicity, the interface to the parallel I/O ports versus the processor bus allows independent control of both the $\overline{WR}$ and $\overline{RD}$ inputs to the AD7769.

For example, the 8051 can set both $\overline{WR}$ and $\overline{RD}$ low at the same time. This permits data from the last ADC conversion to be written directly from the ADC register into the selected DAC register (see Logic Truth Table). This allows very fast transfer of data from the ADC to the DAC and is a useful feature for some applications such as a fast, programmable, infinite sample-and-hold function.

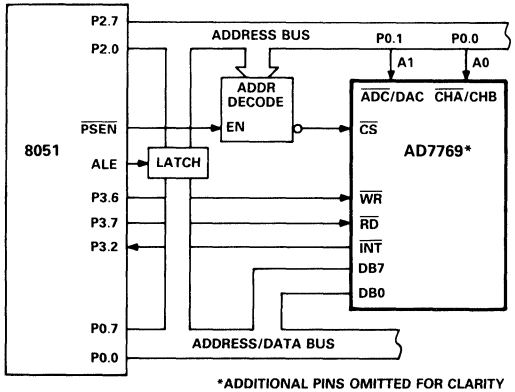


Figure 20. AD7769 to 8051 (Processor Bus) Interface

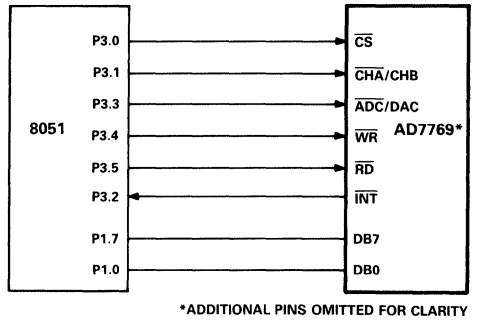


Figure 21. AD7769 to 8051 (Parallel I/O Ports) Interface

AD7769 – MC68HC11 Interface

Figure 22 shows a typical interface between the AD7769 and the MC68HC11 microcomputer. This interface is designed for the maximum MC68HC11 clock speed of 8.4 MHz. The microcomputer is operated in the expanded multiplexed mode, with the AD7769 as a memory mapped peripheral. The expansion bus is made up of Ports B and C, and control signals AS and R/$\overline{W}$.

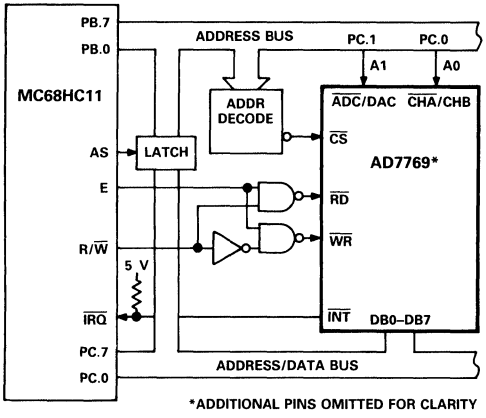


Figure 22. AD7769 to MC68HC11 Interfaced

APPLICATIONS

The AD7769 analog I/O port is used to convert servo related signals between the analog and digital domains. The input structure of the two-channel ADC makes it very easy to convert the typical output signals provided by a servo demodulator.

In a magnetic disk drive employing a dedicated servo surface, the servo demodulator produces two, positive-only, quadrature signals, generally sinusoidal or triangular, from the di-bit patterns read from the servo surface. The quadrature signals have the form of $V_{BIAS} \pm V_{SWING}$. The very fast conversion time of the AD7769 ADC allows sequential conversion of these

quadrature signals without introducing significant phase delay errors. These converted signals provide the servo microcontroller with position and track crossing information from which velocity information can be derived. In optical disk drives, analogous servo signals can be derived from the quad photodiode detector to provide position and focus information for the microcontroller.

The two DACs in the AD7769 accept servo data from the microcontroller to position the head assembly. The DACs provide positive-only output signals of the form $V_{BIAS} \pm V_{SWING}$, which are ideal for driving voice coil motors. In magnetic disk drives, a single voice coil motor is used to position the head assembly and one DAC is usually sufficient to drive the motor in both the seek and track modes. In the seek mode, the DAC can be used to generate directly the desired analog velocity trajectory which the head must travel in order to achieve minimum access times. Alternatively, the DAC can generate a servo error value (computed by the microcontroller) between the actual head velocity and the desired head velocity. In the track mode, the DAC can be used to provide a position error signal to keep the head over the track or to detent the head off track, for such purposes as thermal compensation and soft error retrys. The second DAC in the AD7769 may be employed in this fine positioning loop. Alternatively, the second DAC can be used to control the speed of the spindle motor via a pulse width modulator. In optical disk drives two voice coil motors are used, requiring both DACs of the AD7769—one for the focus servo loop and one for the radial positioning servo loop.

A typical servo control loop using the AD7769 is shown in Figure 23. In this dedicated servo drive, the servo demodulator converts the servo information bit patterns from the disk into the standard N and Q (normal and quadrature) servo signals. The voice coil motor current, I_L, is bidirectional and is supplied by the power transconductance amplifier. One input to this amplifier is held at V_{BIAS} (DAC), while the other input is driven from a DAC output, V_{OUT} A/B. Typical input/output waveforms for this power stage are shown in Figure 24. The transconductance, G_O, of the power stage is determined by external sense resistors.

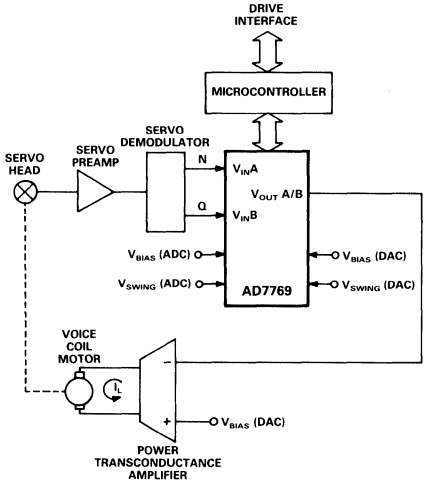


Figure 23. Typical Dedicated Servo Control Loop Using the AD7769

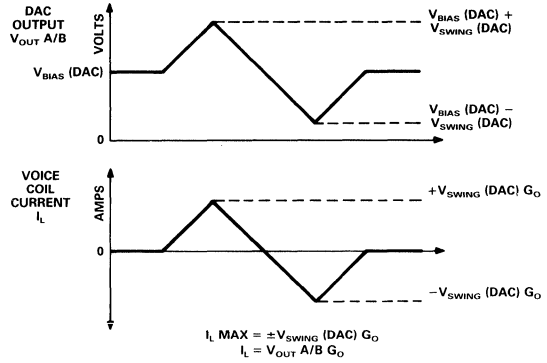


Figure 24. Typical Relationship Between Input Voltage and Output Current for Transconductance Amplifier

Increased Resolution DAC Output

Since both V_{BIAS} (DAC) and V_{SWING} (DAC) are common to both output channels, the full-scale output voltages of both channels are nominally identical. However, by adding an external op amp and scaling resistors, it is possible to attenuate the full-scale output voltage of one (or both) of the DAC outputs to effectively increase the output voltage resolution. Figure 25 shows channel A being attenuated using a resistor scaling of 10:1. The attenuated output voltage, $V_{OUT}A'$, is

$$V_{OUT}A' = V_{BIAS} + (V_{SWING}/10)(2D_A - 1).$$

The output voltage of Channel B remains at

$$V_{OUT}B = V_{BIAS} + V_{SWING}\,(2D_B - 1).$$

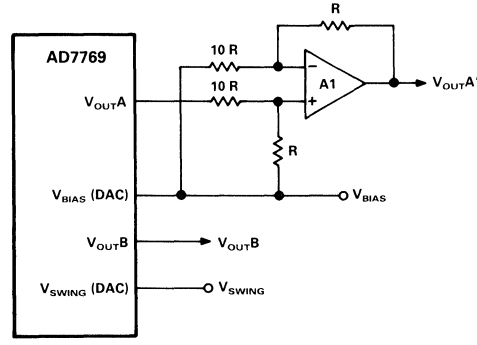


Figure 25. Increasing the DAC Output Voltage Resolution

D_A and D_B are fractional representations of the DAC input codes, e.g., $D_A = N_A/256$ and $D_B = N_B/256$. For example, with a V_{SWING} voltage level of 2 V, the Channel B output span is 4 V with an LSB size of 15.6 mV and (attenuated) Channel A output span is 400 mV with an LSB size of 1.56 mV. Changing the resistor scaling in Figure 25 obviously changes the attenuated full-scale output.

A single change to the circuit Figure 25 allows the two DAC outputs to be combined to provide a single analog output with resolution beyond the standard 8-bits. Figure 26 shows the rearranged circuit. The composite output, V_{OUT}, is

$$V_{OUT} = V_{OUT}B + (V_{SWING}/10)(2D_A - 1)$$

or

$$V_{OUT} = V_{BIAS} + V_{SWING}\,(2D_B - 1) + (V_{SWING}/10)\,(2D_A - 1).$$

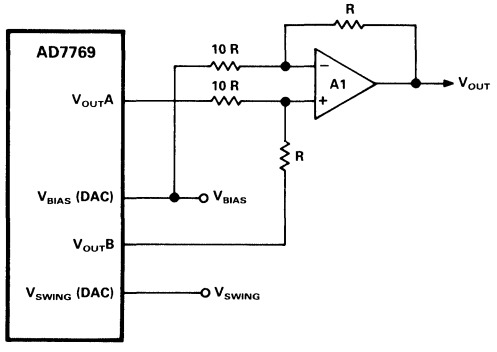


Figure 26. Combined $V_{OUT}A$, $V_{OUT}B$ Circuit

DAC A can be programmed to produce an interpolation function between the 8-bit steps of DAC B to allow, for example, very smooth velocity profile waveforms to be generated.

Servo Offset Facility

Most dedicated servo disk drives offer an offset facility whereby some small voltage is injected into the track-following loop. The purpose of the offset is to move the head to the right or left of its current on-track position to permit reading of off-track data. The circuit is shown in Figure 27. With the 10:1 resistor scaling used in the circuit the output voltage, V_{OUT}, is

$$V_{OUT} = V_{PE} + (V_{SWING}/10)\,(2D_A - 1).$$

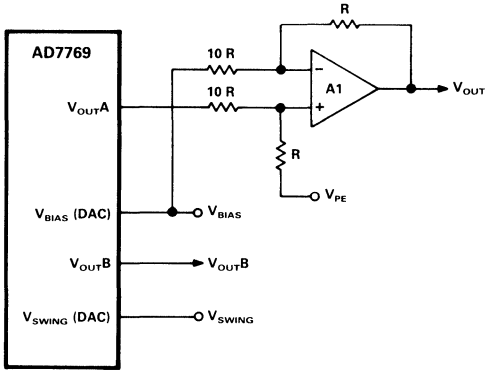


Figure 27. Servo Offset Facility

With no offset added, $V_{OUT} = V_{PE}$, where V_{PE} is the position error voltage which the servo loop normally drives to its zero level, V_{BIAS}. When an offset voltage is supplied by DAC A, the action of the servo is to move the head away from its current on-track position until the position error voltage is equal and opposite to the offset voltage. The position of the head about the track centre is thus programmable.

Programmable Full-Scale Range

The output voltage span of both DACs is determined by the V_{SWING} (DAC) voltage level. This is normally supplied from some fixed voltage source. However, is is possible to use one of the DAC channels to generate a programmable V_{SWING} voltage level. The remaining channel will thus have a full-scale range and LSB size which is software programmable. This circuit is shown in Figure 28 where $V_{OUT}B$ is used in an implicit feedback loop to generate a programmable swing voltage, V_{SWING} (DAC), for the AD7769 from an external fixed input swing voltage, V_{SWING}. Using the 5:1 resistor scaling shown in Figure 28, the expression for the AD7669 input swing voltage is

$$V_{SWING}\,(DAC) = \frac{V_{SWING}}{1 - \frac{(2D_B - 1)}{5}}.$$

For example, with a fixed input swing voltage of 2.5 V, the programmable span via DAC B is as follows:

D_B = 0: V_{SWING} (DAC) = 2.08

D_B = 1/2: V_{SWING} (DAC) = 2.5 V = V_{SWING}

$D_B \approx 1$: V_{SWING} (DAC) = 3.125 V

The AD7769 is specified for a V_{SWING} (DAC) voltage range from 2 V to 3 V, although in practice this range can be extended while still maintaining monotonic operation.

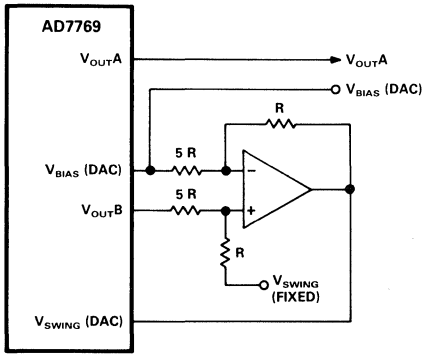


Figure 28. Generating a Software Programmable V_{SWING} (DAC)

Closed Loop Microstepping

Microstepping is a popular technique in low density disk drives (both floppy and hard disk) which allows higher positional resolution of the disk drive head over that obtainable from a full-step driven stepper motor. Typically, a two-phase stepper motor has its phase currents driven with a sine-cosine relationship. These cosinusoidal signals are generated by two DACs driven with the appropriate data. The resolution of the DACs determines the number of microsteps into which each full step can be divided. For example, with a 1.8° full-step motor and a 4-bit DAC, a microstep size of 0.11° ($1.8°/2^n$) is obtainable.

The microstepping technique improves the positioning resolution possible in any control application. However, the positional accuracy can be significantly worse than that offered by the original full-step accuracy specification due to load torque effects. To ensure that the increased resolution is useable, it is therefore necessary to use a closed-loop system where the position of the disk drive head (or motor) is monitored. The closed-loop system allows an error between the desired position and the actual position to be monitored and corrected. The correction is achieved by adjusting the ratio of the phase currents in the motor windings until the required head position is reached.

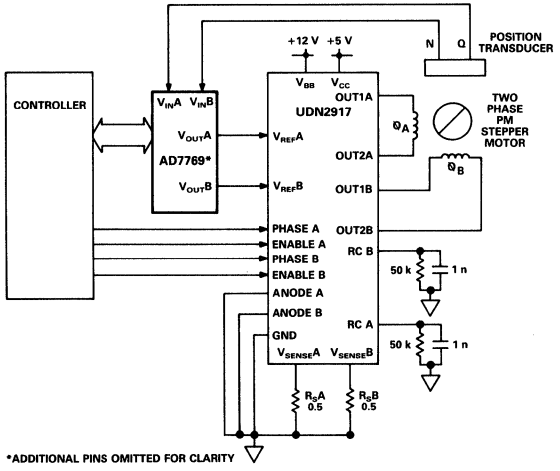


Figure 29. Typical Closed-Loop Microstepping Circuit with the AD7769

The AD7769 is ideally suited for the closed-loop microstepping technique with its dual DACs for positioning the disk drive head and dual channel ADC for monitoring the position of the head. A typical circuit for a closed-loop microstepping system is shown in Figure 29. The DAC waveforms are shown in Figure 30 along with the direction information of clockwise rotation supplied by the controller.

A typical transducer would be a moire-fringe transducer which consists of two gratings, one fixed and one moveable. The relative positions of these two gratings will modulate the amount of light from a LED which can pass through. In order to derive head direction information the stationary grating has two sets of bars, with a 90° phase relationship, and two photo-transistors. The quadrature sinusoidal output waveforms (N & Q) can be converted directly by the AD7769.

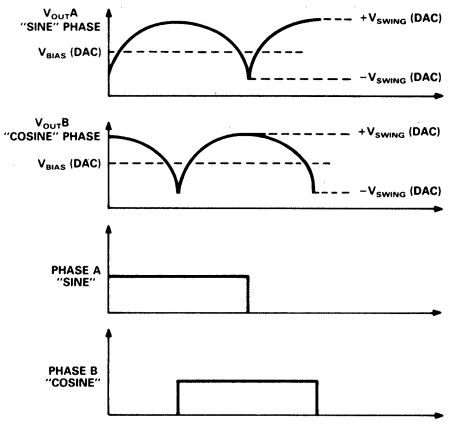


Figure 30. Typical Control Waveforms for the Microstepping Circuit of Figure 29

Multichannel Expansion

In some applications, more than two analog input channels are required to be converted by the ADC. Figure 31 shows a circuit configuration for such an application. The ADG528A is a latched, 8-channel analog multiplexer that is ideally suited for this application since it is specified for single supply operation (+12 V ±10%).

The $\overline{CS}$, $\overline{ADC}$/DAC and $\overline{WR}$ inputs of the AD7769 are gated to drive the $\overline{WR}$ input of the ADG528A. The multiplexer input signal is selected on the falling edge of the $\overline{WR}$ pulse while the signal is latched on the rising edge of $\overline{WR}$, the AD7769 ADC starts conversion. Therefore, the output signal of the multiplexer must have settled to within 8-bits over the duration of the $\overline{WR}$ pulse (see ADC Conversion Cycle section for details). The t_{ON} ($\overline{WR}$) and settling time of the ADG528A thus determines the width of the $\overline{WR}$ pulse.

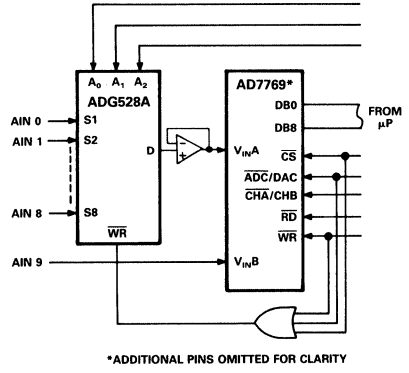


Figure 31. Multichannel Inputs

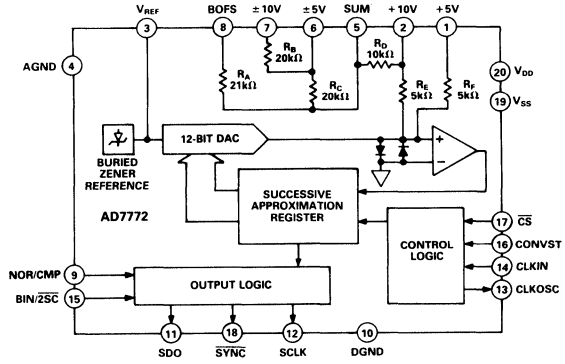
ANALOG DEVICES

LC²MOS Serial Output 12-Bit ADC

AD7772

FEATURES
12-Bit Resolution and Accuracy
Fast Conversion Time: 10μs
Serial Output
Complete with On-Chip Reference
Low Power
Unipolar or Bipolar Input Ranges
Small 0.3", 20-Pin DIPs and 20-Terminal Surface Mount Package

AD7772 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD7772 is a complete 12-bit ADC that offers high speed performance combined with low, CMOS power levels. It uses an accurate, high speed DAC and comparator in a successive approximation loop to achieve a fast conversion time. An on-chip, buried Zener diode provides a stable reference voltage to give low drift performance over the full temperature range, and the specified accuracy is achieved without any user trims. The AD7772 can be configured to have analog input ranges of 0 to +5V, 0 to +10V, ±5V or ±10V.

An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation. Alternatively, the clock input may be driven from an external clock source such as a divided-down microprocessor clock.

The AD7772 serial interface is compatible with digital signal processors such as the TMS32020, μPD7720 and DSP56000. It can also be used with general purpose serial to parallel converters such as shift registers. The device outputs the conversion result with one leading zero and the twelve data bits following. When using the AD7772 at top speed (CLKIN = 1.28MHz) with a 3μs sample-and-hold amplifier like the AD585, it is possible to achieve throughput rates of 76kHz. With this 76kHz sample rate signals with spectral contents up to 38kHz can be digitized.

The AD7772 is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

PRODUCT HIGHLIGHTS

1. Fast, 10μs conversion time makes the AD7772 ideal for a wide range of applications in telecommunications, sonar and radar signal processing and industrial data acquisition systems requiring optical isolation.
2. Where space saving is important, the small package and serial interface of the AD7772 minimize the amount of board space needed to realize 12-bit data acquisition.
3. The versatile serial interface on the AD7772 makes it simple to interface to the serial ports of DSPs as well as other microprocessor systems.
4. On-chip buried Zener reference has temperature coefficient as low as 25ppm/°C, giving low full-scale drift over the operating temperature range.
5. Stable DAC and comparator give excellent linearity and low zero error over the full temperature range.
6. LC²MOS circuitry gives low power drain (135mW) from +5V, −15V supplies.

SPECIFICATIONS (V_{DD} = +5V ±5%, V_{SS} = −15V ±5%, f_{CLK} = 1.28MHz. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	K, B Versions[1]	L Version[1]	C Version[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity @ 25°C	±1	±1/2	±1/2	LSB max	Tested Range: 0 to +5V
T_{min} to T_{max}	±1	±1/2	±3/4		
Differential Nonlinearity	±1	±1	±1	LSB max	No Missing Codes Guaranteed T_{min} to T_{max}
Unipolar Offset Error @ +25°C	±8	±4	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±8	±4	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Full Scale Error[2] @ +25°C	±15	±10	±10	LSB max	Input Range: 0 to 5V or 0 to 10V
Bipolar Zero Error @ +25°C	±9	±5	±5	LSB max	Input Range: ±5V or ±10V
T_{min} to T_{max}	±15	±9	±9	LSB max	
Bipolar Full Scale Error[2] @ +25°C	±10	±7	±7	LSB max	Input Range: ±5V or ±10V
Full Scale TC[3,4]	±45	±35	±35	ppm/°C max	
ANALOG INPUTS					
Input Ranges					
Unipolar	0 to +5	0 to +5	0 to +5	Volts	
	0 to +10	0 to +10	0 to +10	Volts	
Bipolar	−5 to +5	−5 to +5	−5 to +5	Volts	
	−10 to +10	−10 to +10	−10 to +10	Volts	
Input Current					
Unipolar	3	3	3	mA max	Input Range: 0 to 5V or 0 to 10V
Bipolar	±0.4	±0.4	±0.4	mA max	Input Range: ±5V to ±10V
INTERNAL REFERENCE VOLTAGE					
V_{REF} Output @ +25°C	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	V_{min}/V_{max}	−5.25V ±1%
V_{REF} Output TC	±40	±25	±25	ppm/°C typ	
Output Current Sink Capability[5]	550	550	550	µA max	(External Load Should Not Change During Conversion.)
POWER SUPPLY REJECTION					
V_{DD} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{SS} = −15V V_{DD} = +4.75V to +5.25V
V_{SS} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{DD} = +5V V_{SS} = −14.25V to −15.75V
LOGIC INPUTS					
$\overline{CS}$, NOR/CMP, BIN/$\overline{2SC}$					
CONVST, CLKIN					
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{DD} = 5V ± 5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	V min	
C_{IN}[5], Input Capacitance	10	10	10	pF max	
$\overline{CS}$, NOR/CMP, BIN/$\overline{2SC}$					
CONVST					
I_{IN}, Input Current	±10	±10	±10	µA max	V_{IN} = 0 to V_{DD}
CLKIN					
I_{IN}, Input Current	±20	±20	±20	µA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS					
SDO, SCLK, CLKOSC, $\overline{SYNC}$					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200µA
Floating State Leakage Current	±10	±10	±10	µA max	
SDO					
Floating State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME	10.2	10.2	10.2	µs max	f_{CLK} = 1.28MHz. See Control Inputs Synchronization.
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	VNOM	±5% for Specified Performance
V_{SS}	−15	−15	−15	VNOM	±5% for Specified Performance
I_{DD}[6]	7	7	7	mA max	$\overline{CS}$ = CONVST = V_{DD}, AIN = 5V
I_{SS}[6]	12	12	12	mA max	$\overline{CS}$ = CONVST = V_{DD}, AIN = 5V
Power Dissipation	135	135	135	mW typ	
	215	215	215	mW max	

NOTES
[1]Temperature range as follows: K, L versions: 0 to +70°C
B, C versions: −25°C to +85°C
[2]Includes internal voltage reference error.
[3]Full Scale TC = △FS/△T, where △FS is Full Scale change from T_A = +25°C to T_{min} or T_{max}.
[4]Includes internal voltage reference drift.
[5]Sample tested to ensure compliance.
[6]Power supply current is measured when AD7772 is inactive, i.e., $\overline{CS}$ = CONVST = $\overline{SYNC}$ = HIGH.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V, V_{SS} = −15V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Units	Conditions/Comments
t_1[2]	780	780	ns min	CLKIN Cycle Time
t_2	40	50	ns max	Propagation Delay between CLKIN and CLKOSC
t_3[3]	545	560	ns max	Propagation Delay between CLKIN and SCLK
t_4[3]	780	780	ns min	SCLK Cycle Time
t_5	45	45	ns min	$\overline{CS}$ to CONVST Setup Time
t_6[3]	0	0	ns min	$\overline{CS}$ to $\overline{SYNC}$ Hold Time
t_7	40	50	ns min	CONVST Pulse Width
t_8	50	50	ns max	SCLK ↓ to $\overline{SYNC}$ ↓ Delay
t_9	60	65	ns max	SCLK ↓ to $\overline{SYNC}$ ↑ Delay
t_{10}[4]	50	50	ns max	SCLK ↓ to SDO ↓ Delay, C_L = 20pF
	100	125	ns max	SCLK ↓ to SDO ↓ Delay, C_L = 100pF
t_{11}[4]	115	145	ns max	SCLK ↓ to Data Valid, C_L = 20pF
	190	235	ns max	SCLK ↓ to Data Valid, C_L = 100pF
t_{12}[5]	10	10	ns min	SCLK ↓ to SDO High Impedance
	65	80	ns max	

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]CLKIN Mark/Space Ratio Range is 55/45 to 45/55.
[3]SCLK and $\overline{SYNC}$ are loaded with the circuit of Figure 1.
[4]t_{10} and t_{11} are measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.
[5]t_{12} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 3.
Specifications subject to change without notice.

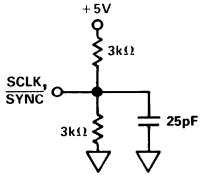
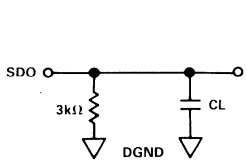
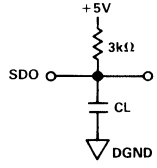


Figure 1. SCLK, $\overline{SYNC}$ Load Circuit

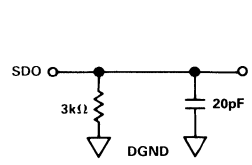


a. To V_{OH} (t_{11})

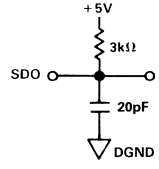


b. To V_{OL} (t_{10}, t_{11})

Figure 2. Load Circuits for t_{10}, t_{11} Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 3. Load Circuits for Bus Relinquish Time Test (t_{12}).

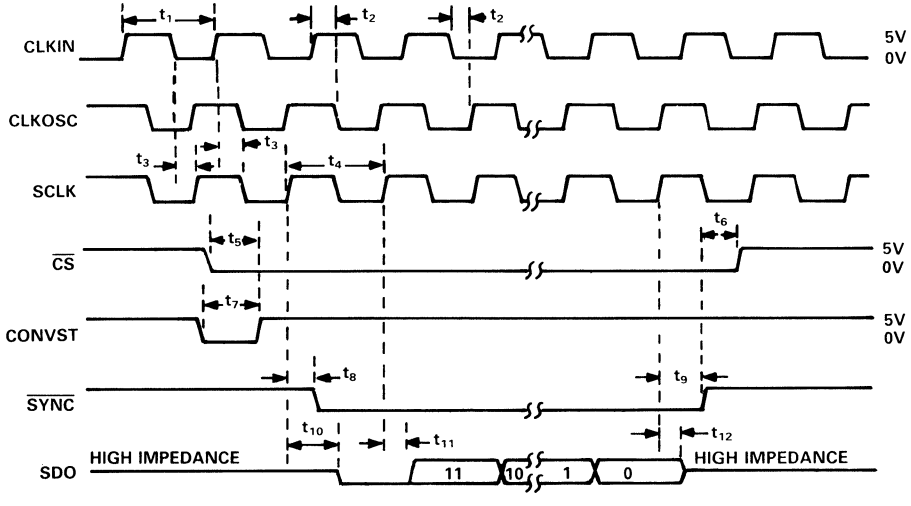


Figure 4. AD7772 Timing Diagram.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3V to +7V
V_{SS} to DGND . . . . . +0.3V to −17V
AGND to DGND . . . . . −0.3V to V_{DD} +0.3V
Analog Input Voltage to AGND
(BOFS, ±10V, ±5V, SUM,
+10V, +5V) . . . . . −15V to +15V
Digital Input Voltage to DGND
(CLK IN, $\overline{CS}$, CONVST, NOR/CMP,
BIN/$\overline{2SC}$) . . . . . −0.3V to V_{DD} +0.3V
Digital Output Voltage to DGND
(SDO, SCLK, $\overline{SYNC}$, CKOSC) . . . −0.3V to V_{DD} +0.3V

Operating Temperature Range
Commercial (K, L Versions) . . . . . 0 to +70°C
Industrial (B, C Versions) . . . . . −25°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

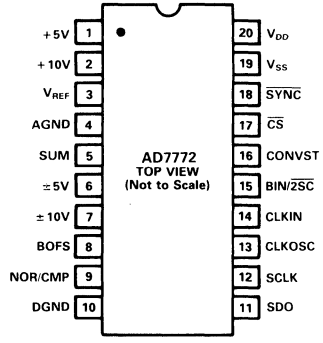
ORDERING INFORMATION[1]

Full Scale TC	Accuracy Grade	0 to +70°C	−25°C to +85°C
		Plastic DIP[2] (N-20)	**Hermetic[2] (Q-20)**
45ppm/°C	±1LSB	AD7772KN	AD7772BQ
35ppm/°C	±1/2LSB	AD7772LN	AD7772CQ
		PLCC (P-20A)[2,3]	
45ppm/°C	±1LSB	AD7772KP	
35ppm/°C	±1/2LSB	AD7772LP	

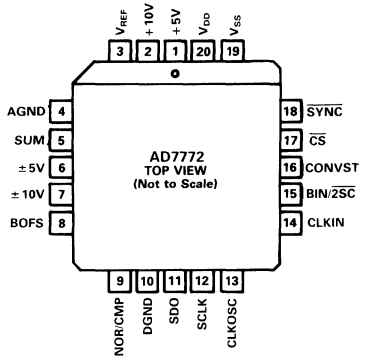
NOTES
[1]Analog Devices reserves the right to ship either ceramic or cerdip hermetic packages.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	+5V	Analog Input Pin. This is connected as in Figure 9 to provide a +5V analog input range.
2	+10V	Analog Input Pin. This is connected as in Figure 11 to provide a +10V analog input range.
3	V_{REF}	Voltage Reference Output. The AD7772 has its own internal −5.25V reference.
4	AGND	Analog Ground
5	SUM	Analog Input Pin. This is connected to the inverting terminal of an op amp for ±5V to ±10V analog input ranges. See Figure 13.
6	±5V	Analog Input Pin. Figure 13 shows how this is connected for a ±5V analog input range.
7	±10V	Analog Input Pin. For ±10V analog input range see Figure 13.
8	BOFS	Bipolar Offset Pin. This is tied to V_{REF} for either of the bipolar analog input ranges. See Figure 13.
9	NOR/CMP	NOR/CMP and BIN/$\overline{2SC}$ determine the format of the output data. See Table I.
10	DGND	Digital Ground
11	SDO	Serial Data Output
12	SCLK	Continuously running Serial Clock Output.
13	CLKOSC	Clock Oscillator Pin. An inverted CLKIN signal appears at CLKOSC when external clock is used. See CLKIN (Pin 14) description for crystal (resonator).
14	CLKIN	Clock Input Pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be applied between CLKIN and CLKOSC. See Figure 7.
15	BIN/$\overline{2SC}$	BIN/$\overline{2SC}$ and NOR/CMP determine the output data format. See Table I.
16	CONVST	Conversion Start Input. This signal starts a conversion on its rising edge when $\overline{CS}$ is low.
17	$\overline{CS}$	Chip Select Input. This active low signal, in conjunction with CONVST, starts a conversion.
18	$\overline{SYNC}$	This is the framing signal for the serial data output. It goes low on the first rising edge of SCLK after conversion begins and goes high when conversion is complete.
19	V_{SS}	Negative Supply, −15V
20	V_{DD}	Positive Supply, +5V

NOR/CMP	BIN/$\overline{2SC}$	Unipolar Data Format	Bipolar Data Format
0	0	2s Complement	Complementary 2s Complement
0	1	Straight Binary	Complementary Offset Binary
1	0	Complementary 2s Complement	2s Complement
1	1	Complementary Binary	Offset Binary

Table I. AD7772 Output Coding

TERMINOLOGY

LEAST SIGNIFICANT BIT
An ADC with 12-bit resolution can resolve one part in 2^{12} (1/4096 of full scale). For the AD7772 operating in the 0 to +5V range, 1LSB is 1.22mV.

NO MISSING CODES
A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For all grades of the AD7772, all 4096 codes are present over the entire operating temperature ranges.

UNIPOLAR OFFSET ERROR
For the unipolar analog input range, the first transition should occur at a level 1/2LSB above AGND. Unipolar offset error is defined as the deviation of the actual transition from that point. This error can be adjusted as explained further on in this data sheet.

BIPOLAR ZERO ERROR
In the bipolar analog input ranges, bipolar zero is defined as the middle of code 2048. Bipolar zero error is the actual deviation from that point. The circuit diagram on page 9 shows how to adjust this.

UNIPOLAR FULL SCALE ERROR
The last transition in the ADC (from 111 . . .110 to 111 . . .111 when using straight binary coding) should occur for an analog value 1 1/2LSB below the nominal full scale (4.99816 for 5.000 volts full scale). The full scale error is the deviation of the actual level at the last transition from the ideal level with unipolar offset error adjusted to zero. This error can be trimmed out as shown in Figure 12. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal −5.25 volts reference.

BIPOLAR FULL SCALE ERROR
In the bipolar mode, the ADC has a positive full scale error and a negative full scale error. Positive full scale error is the deviation of the actual level at the last transition from the ideal level, with bipolar zero error adjusted to zero. Negative full scale error is the deviation of the actual level at the first transition from the ideal level, with bipolar zero error adjusted to zero. Full scale error is defined as either positive full scale error or negative full scale error, whichever is largest.

CIRCUIT INFORMATION

CONVERTER DETAILS

Conversion start on the AD7772 is controlled by the $\overline{CS}$ and CONVST inputs. Figure 5 shows the operating signals of interest. With $\overline{CS}$ held permanently low, a positive-going edge on CONVST starts the conversion cycle. The successive approximation register (SAR) is reset at this stage. On the next rising edge of SCLK, the $\overline{SYNC}$ output goes low and the three-state data output (SDO) is enabled.

During conversion, the internal 12-bit DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output against the analog input. The MSB decision is made and latched to the serial data output 90ns (typically) after the second rising edge of SCLK following the conversion start. Similarly, the succeeding bit decisions are made and latched approximately 90ns after the SCLK rising edges. When conversion is complete, the SDO output is latched to the high impedance state and the $\overline{SYNC}$ output goes high.

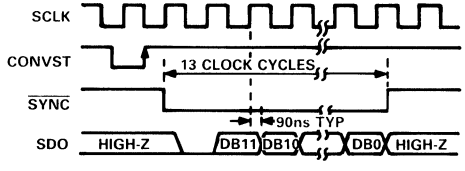


Figure 5. Operating Waveforms Using an External Clock Source for CLKIN

CONTROL INPUTS SYNCHRONIZATION

Conversion time for the AD7772 is defined as the time for which the $\overline{SYNC}$ output is low. This is always 13 clock cycles. However, there is a delay between CONVST going high and $\overline{SYNC}$ going low. Without synchronization this delay can vary from zero to an entire clock period. If a constant delay is required here, then the following approach can be used: when starting a conversion CONVST must go high on either the rising edge of CLKIN or the falling edge of CLKOSC.

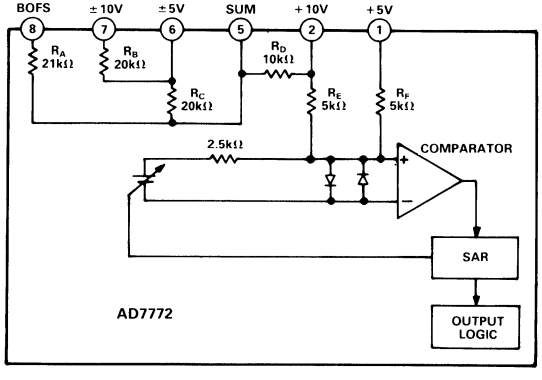


Figure 6. AD7772 Analog Input Stage

DRIVING THE ANALOG INPUT

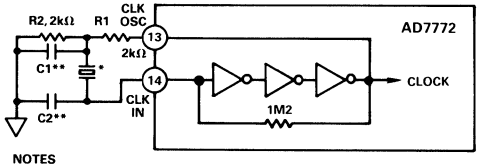
Figure 6 shows the analog input stage for the AD7772. There are four application resistors (R_A, R_B, R_C and R_D). These can be used with one external op amp to implement ±5V and ±10V analog input ranges. R_A is always connected to V_{REF} for these ranges and offsets the input signal by +2.5V. R_C and R_D provide an attenuation of 2 for the ±5V input while R_B, R_C and R_D attenuate the ±10V input by 4. The external op amp is connected as an inverting amplifier with its output driving Pins 1 and 2 and R_D as the feedback resistor. Figure 13 shows the circuit configuration.

The +5V and +10V inputs on the AD7772 connect to the comparator input via the 5kΩ resistors R_E and R_F. The DAC which has 2.5kΩ output impedance also connects to this point. During conversion, current from the analog input is modulated by the DAC output current at a rate equal to the CLKIN frequency (1.28MHz maximum). This causes voltage spikes (glitches) to appear at the analog input. The magnitude and settling time of these glitches depends on the open-loop output impedance and small signal bandwidth of the amplifier or sample-and-hold driving the input. These devices must have sufficient drive to ensure that the glitches have settled within one clock period. An example of a suitable op amp is the AD OP-27. The magnitude of the largest glitch when using this device to drive the analog input is typically 11mV with a 200ns settling time.

Suitable devices capable of driving the AD7772 analog inputs are the AD OP-27 and AD711 op amps and the AD585 sample-and-hold.

INTERNAL CLOCK OSCILLATOR

Figure 7 shows the AD7772 internal clock circuit. A crystal or ceramic resonator may be connected as in Figure 7 to provide a clock oscillator for the ADC timing. Resistors R1 and R2 ensure that the CLKIN mark/space ratio stays between 45/55 and 55/45. Alternatively, the crystal/resonator may be omitted and an external clock source connected to CLKIN. The mark/space ratio of the external clock must be in the range 45/55 to 55/45. An inverted CLKIN signal will appear at the CLKOSC output pin.



NOTES
*1.28MHz CRYSTAL/CERAMIC RESONATOR.
**C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30pF TO 100pF.

Figure 7. AD7772 Internal Clock Circuit

INTERNAL REFERENCE

The AD7772 has an on-chip, buffered, temperature compensated, buried Zener reference, which is factory trimmed to −5.25V ±1%. It is internally connected to the DAC and is also available at Pin 3 to sink up to 550μA current from an external load.

For minimum code transition noise, the reference output should be decoupled with a capacitor to filter out wideband noise from the reference diode (10μF tantalum in parallel with 100nF ceramic). However, large values of decoupling capacitors can affect the dynamic response and stability of the reference amplifier. A 10Ω resistor in series with the decoupling capacitors will eliminate this problem without adversely affecting the filtering effect of the capacitors. A simplified schematic of the reference with its recommended decoupling components is shown in Figure 8.

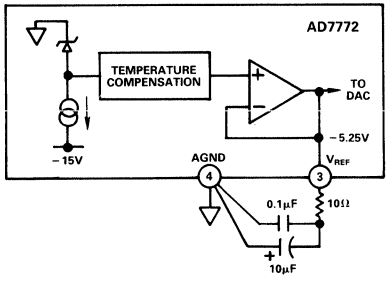


Figure 8. AD7772 Internal −5.25V Reference

APPLYING THE AD7772

The AD7772 has a flexible input stage with application resistors which can be configured for various analog input ranges. The following sections show the AD7772 configured for these ranges.

UNIPOLAR OPERATION

Figure 9 shows the AD7772 connected for the unipolar 0 to +5V input range. The ideal input/output characteristic for this range is given in Figure 10. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, 5/2LSBs . . .FS − 3/2LSBs). The output code is straight binary (see Table I) with an LSB size of FS/4096 = 5/4096V = 1.22mV. To change to complementary binary coding, NOR/CMP should be tied to +5V.

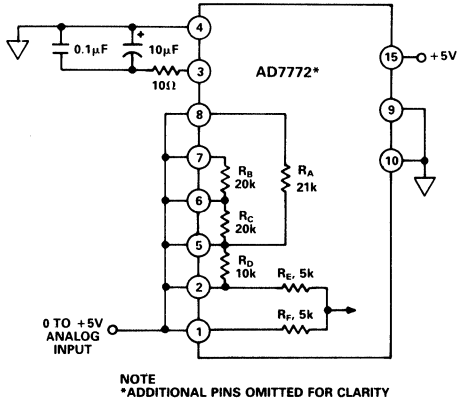


Figure 9. Unipolar 0 to +5V Input Range

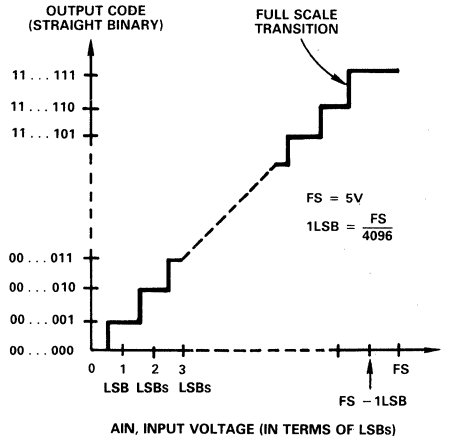


Figure 10. Ideal Input/Output Transfer Characteristic for Figure 9

Figure 11 shows how the AD7772 can be connected for a 0 to +10V input range. The +5V pin is now connected to 0V, thereby attenuating the input by 2 and effectively doubling the analog input range. The analog input is applied to the +10V pin. For this circuit, the LSB size is FS/4096 = 10/4096V = 2.44mV and the coding is straight binary.

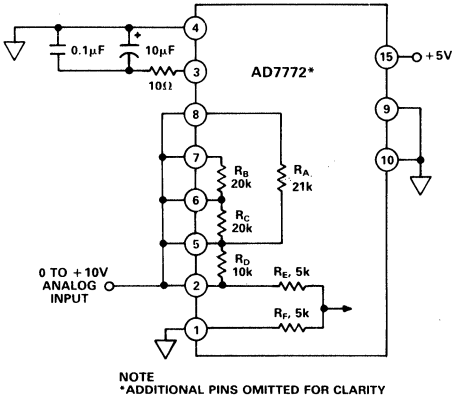


Figure 11. AD7772 in 0 to +10V Analog Input Range

UNIPOLAR OFFSET AND FULL SCALE ERROR ADJUSTMENT

If absolute accuracy is an application requirement, then offset and full scale error can be adjusted to zero. Offset error must be adjusted before full scale error. Figure 12 shows the extra components required for full scale error adjustment. The analog input range is 0 to +5V and the coding is straight binary. Zero offset is achieved by adjusting the offset of the op amp driving the analog input (i.e., A1 in Figure 12). For zero offset error apply 0.61mV (+1/2LSB) to V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 . . . 0000 and 000 . . . 0001.

To adjust the full scale error, apply an analog input of 4.99817V (FS − 3/2LSBs) to V_{IN} and adjust R1 until the ADC output code flickers between 1111 . . . 1110 and 1111 . . . 1111.

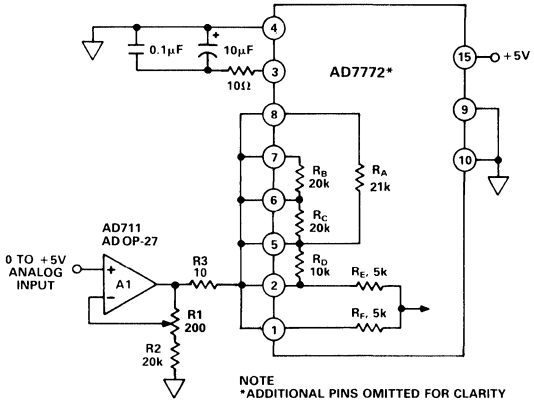


Figure 12. Unipolar 0 to +5V Operation with Full-Scale Error Adjust

BIPOLAR OPERATION

Figure 13 shows the circuit configuration for implementing ±5V and ±10V analog input voltages on the AD7772. R_A and R_D offset the input signal by a constant +2.5V while R_C and R_D provide attenuation for the ±5V input. R_B, R_C and R_D provide attenuation for the ±10V input. If a ±5V input range is needed, the input signal should be applied to Pin 6 (±5V) and Pin 7 left unconnected. For a ±10V input range, apply the signal to Pin 7 (±10V) and leave Pin 6 open circuit. The output code format is offset binary. Figure 14 shows the ideal input/output characteristic for the ±5V input range.

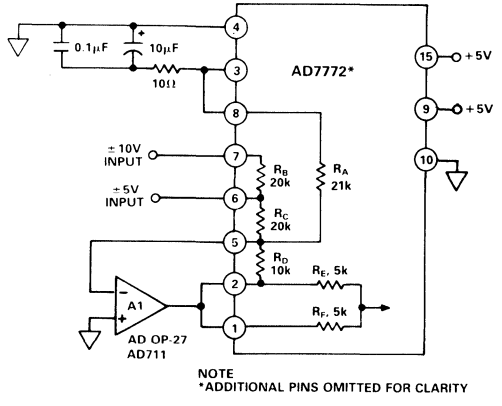


Figure 13. AD7772 Connected for ±5V/±10V Input Range

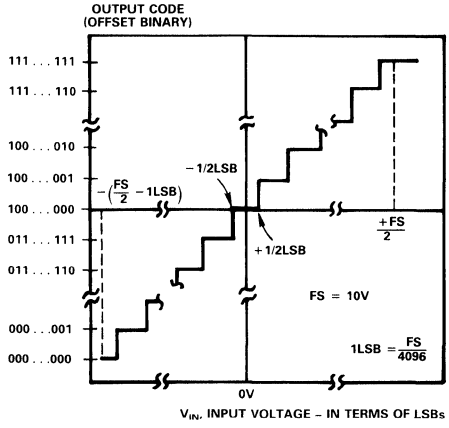


Figure 14. Ideal Input/Output Transfer Characteristic for the Bipolar Circuit of Figure 13

BIPOLAR OFFSET AND FULL SCALE ERROR ADJUSTMENT

In measurement applications where absolute accuracy is required, offset and full scale error can be adjusted to zero. Figure 15 shows how the ±5V input range circuit is modified to do this. By placing R3 in parallel with the op amp feedback resistance R_D and the R1, R2 combination in parallel with R_C, an adjustment range of ±16LSBs is possible.

Bipolar zero error must be adjusted before full scale error. This is achieved by applying an analog input of +1.22mV (+1/2LSB) at the ±5V input pin and adjusting the op amp offset until the ADC output code flickers between 1000 . . . 0000 and 1000 . . . 0001.

For full scale error adjustment, the analog input must be at 4.99878 volts (i.e., FS/2 – 1/2LSB or last transition point). Then R1 is adjusted until the output code flickers between 1111 . . . 1110 and 1111 . . . 1111.

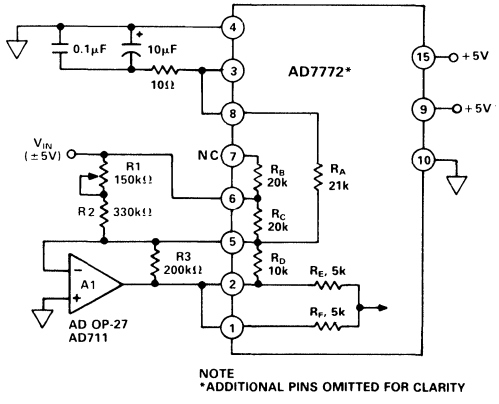


Figure 15. AD7772 Connected for ±5V Input Range with Full-Scale Error Adjust

INTERFACING

The AD7772 is a serial output device, making it suitable for use with digital signal processors which have a serial port (TMS32020, DSP56000, etc.) as well as microcontrollers (8051, 6803) and shift registers. See Figure 4 for the timing diagram. The serial data is placed on the SD0 pin as conversion is taking place. Each data bit is valid on the falling edge of SCLK, and the complete word is framed by the $\overline{SYNC}$ pulse.

TMS32020/TMS320C25 INTERFACE

Figure 16 shows the circuit for interfacing the AD7772 to the TMS32020/TMS320C25 Serial Port. The AD7772 has $\overline{CS}$ tied permanently low. In a sampling system, the SAMPLE TIMER would control the start of conversion. When the system is non-sampling, this CONVST pulse could be software-controlled by the processor. When conversion begins, the $\overline{SYNC}$ output goes low. This enables the serial input of the TMS32020/TMS320C25 which now accepts the data appearing at DR on each negative-going edge of CLKR. After sixteen CLKR pulses the internal interrupt (RINT) is automatically set. The service routine for this interrupt then reads the conversion result from the DRR (data receive register) into the accumulator or memory. Note that the word in the DRR must be shifted right three times in order to get the

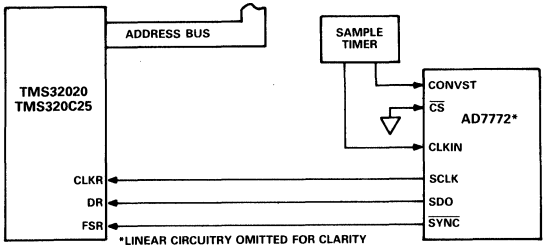


Figure 16. AD7772 to TMS32020/TMS320C25 Interface

standard right-justified data format. This is also the case in the other processor interfaces which follow.

NEC μPD7720/μPD77230 INTERFACE

Figure 17 shows an interface circuit for the NEC μPD7720 digital signal processor. Unlike the FSR input on the TMS320 processors, the $\overline{SIEN}$ input on the μPD7720/μPD77230 is level sensitive rather than edge sensitive. Because the processor can only be configured for either 8-bit or 16-bit data transfers, the $\overline{SIEN}$ input to the μPD7720/μPD77230 must be at least 16 clock pulses wide to receive the 12-bit conversion result from the AD7772. The circuitry of Figure 17 accomplishes this by using the CONVST and $\overline{SYNC}$ signals as the set and reset controls on an S-R flip-flop.

In Figure 17 the processor controls the start of conversion. $\overline{CS}$ is tied low, and the output of the address decoder drives CONVST.

Data bits are shifted into the μPD7720 on the rising edge of SCK when $\overline{SIEN}$ is asserted. This means that SCLK from the AD7772 must be inverted before connecting to the SCK input. The internal shift register converts the serial data to parallel and transfers it to the SI register when 16 bits have been received. The internal acknowledge flag, SIACK, is also set at this time. When the parallel data is read from the SI register, this SIACK flag is reset. It is important to read the data from the SI register before the next conversion is complete and the data bits transferred; otherwise the original data will be lost.

When interfacing to the μPD77230, the inverter for SCLK shown in Figure 17 is not needed, since data on SI is synchronized with the falling edge of SICK (the serial input clock). Thus, SCLK from the AD7772 is connected directly to SICK on the μPD77230. All other connections are as in Figure 17.

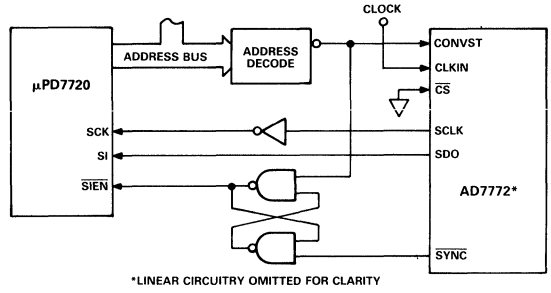


Figure 17. AD7772 to NEC μPD7720 Interface

DSP56000 INTERFACE

The DSP56000 has a very versatile serial interface which can be configured to suit various applications. Figure 18 shows an interface circuit for the AD7772 to DSP56000. The DSP56000 is configured for normal mode, asynchronous operation. This means that the DSP56000 serial transmitter and receiver have their own separate clock and synchronization signals. The processor is set up for 16-bit word and continuous clock with SCO and SCI configured as inputs. The FSL control bit, which selects the type of frame synchronization to be recognized, should be set to 0. All of these conditions are programmable in the DSP56000.

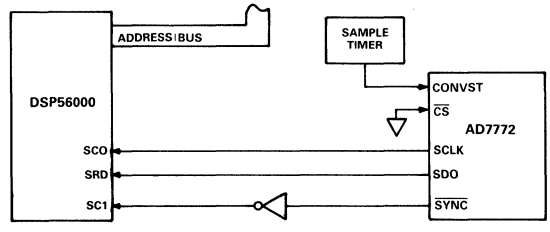


Figure 18. AD7772 to DSP56000 Interface

When the receiver is enabled, a 16-bit data word will be clocked in each time the frame synchronization signal is detected. Once received, the data word will be transferred from the SSI receive shift register to the receive data register (RX). The RDF flag (receive data register full flag) will be set to indicate that the receiver is full and the receive interrupt will occur if it has been enabled. The DSP program should read the data from RX before a new data word is transferred from the receive shift register, otherwise the receive overrun error (ROE) will be set.

AD7772 IN REMOTE CONTROL APPLICATIONS

Figure 19 shows a serial interface between the AD7772 and a remote controller. The digital signals are transmitted differentially along twisted pairs while optocouplers sense the signals at the receiving end. The DS8830 is a dual differential line driver, designed to drive long lengths of coaxial cable, strip line or twisted pair transmission lines. The optocouplers used are HCPL-2601s, which have sufficient speed (1000V/μs slew rate) to handle the maximum data transfer rate of 1.28M bits/sec.

The AD7772 is set up so that only one signal (CONVST) is needed to start conversion. Three twisted pairs are needed to transfer the data back to the controller. These take the SCLK, SDO and $\overline{\text{SYNC}}$ signals.

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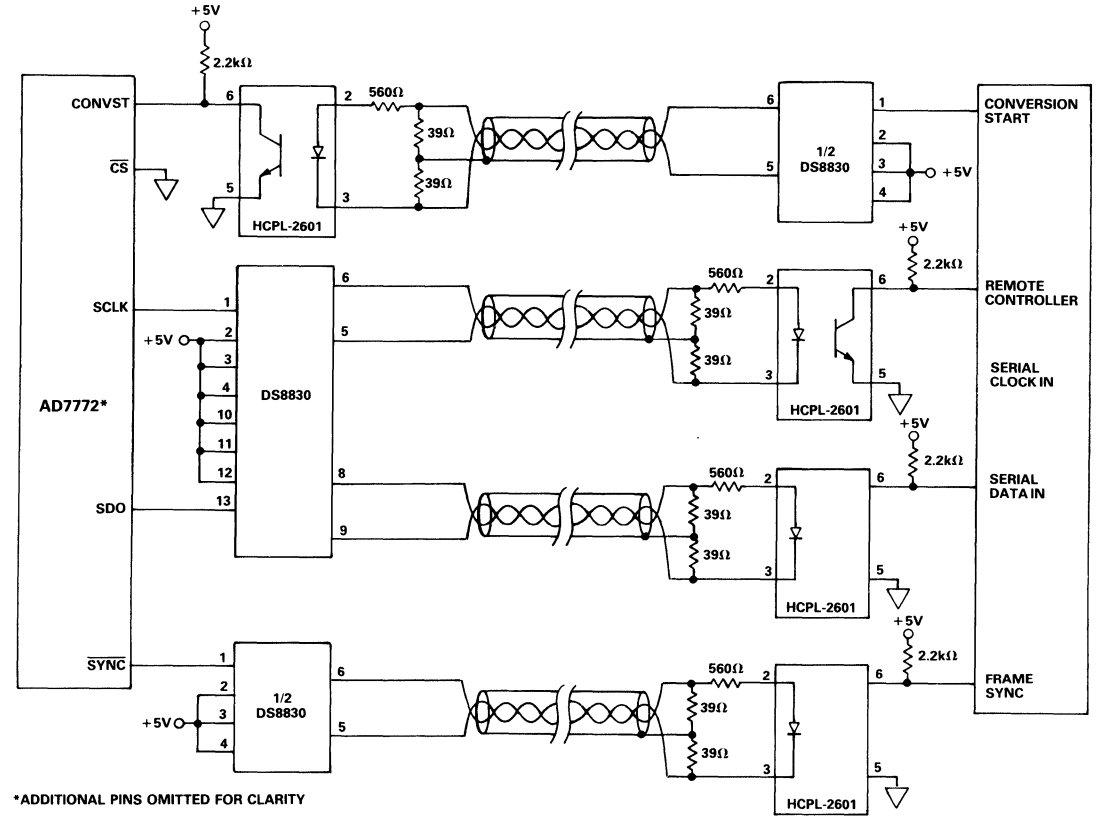


Figure 19. Using Optocouplers with the AD7772

AD7772 – AD585 SAMPLE-HOLD INTERFACE

Figure 20 shows a typical sampling application for the AD7772 with an AD585 sample-and-hold amplifier driving the ADC analog input. The AD585 is configured as a unity gain buffer. The ± 10V input signal is successively sampled and held and this signal is then fed to Pin 7 of the AD7772 which is connected for an analog input range of ± 10V.

For the circuit of Figure 20 to function properly, it is necessary to have the CONVST signal for the ADC synchronized with CLKIN as discussed previously. This ensures that the analog input is always held at a fixed point in time after the CONVST signal goes high and equal interval sampling is achieved. Without this synchronization, the holding point would not be exactly defined and the data acquisition system performance would suffer accordingly.

The maximum throughput rate of the system shown in Figure 20 is 76kHz. 10μs is required for conversion while a further 3μs must be allowed for the AD585 to acquire the signal. This yields a total time of 13μs. Thus, the maximum sampling rate is 76kHz and the analog input bandwidth is 38kHz.

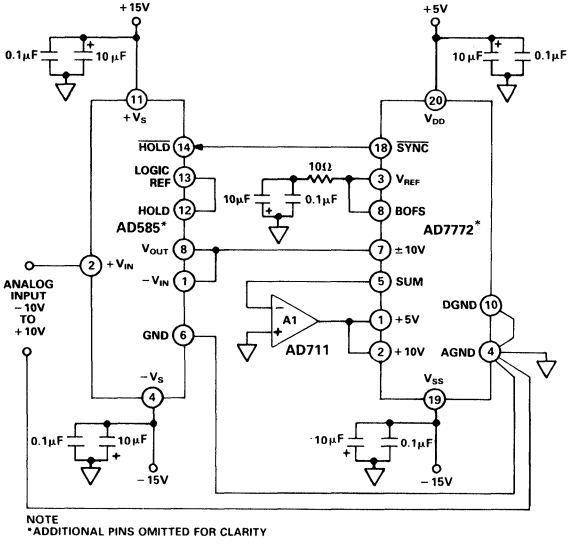


Figure 20. AD7772 Sample-and-Hold Interface

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7772's comparator is required to make bit decisions on an LSB size of 1.22mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 4 (AGND) or as close as possible to the AD7772 as shown in Figure 21. Connect all other grounds and Pin 10 (AD7772 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths while guarding the analog circuitry from digital noise. The circuit layout of Figures 24 and 25 have both analog and digital ground planes which are kept separate and only joined together at the AD7772 AGND pin.

NOISE: Keep the input signal leads to the analog input and signal return leads from AGND (Pin 4) as short as possible to minimize input noise coupling. In applications where this is not possible use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

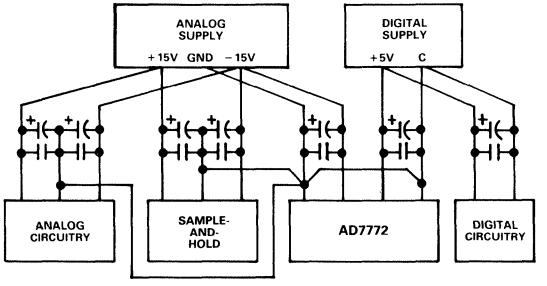


Figure 21. Power Supply Grounding Practice

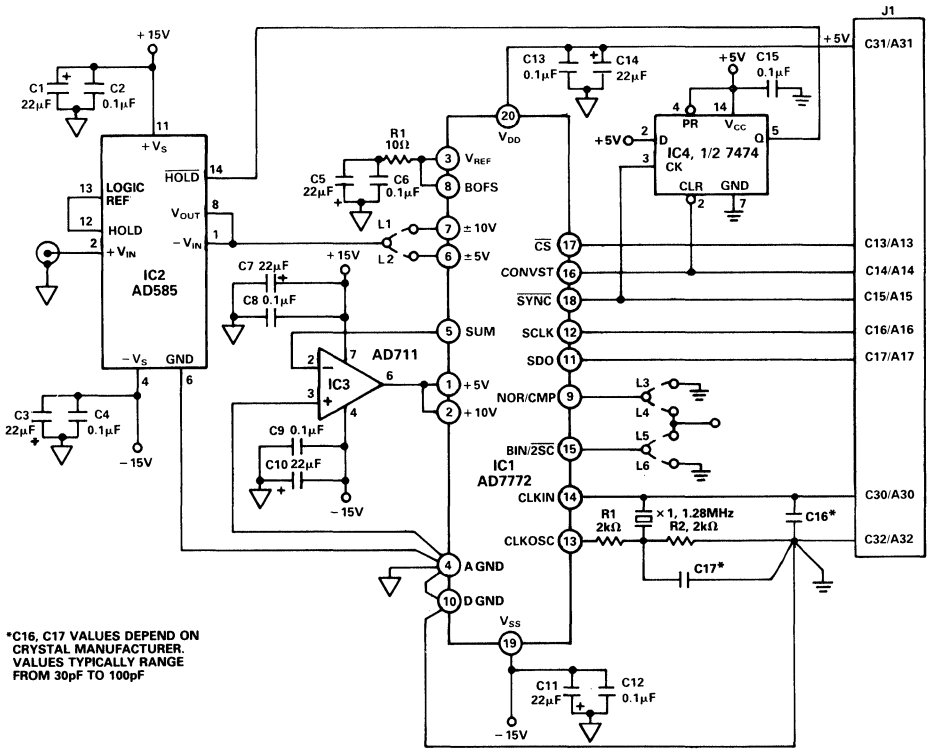


Figure 22. Schematic for AD7772 Board

PRINTED CIRCUIT BOARD LAYOUT

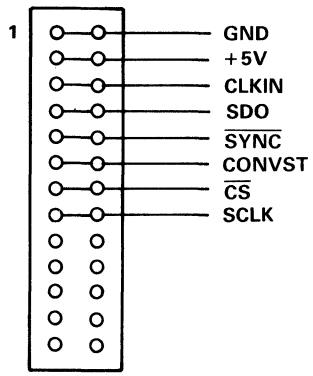
Figure 22 is a circuit diagram showing the AD7772 being used to digitize an analog signal. The circuit board contains the ADC, sample-and-hold and extra op amp necessary to sample a bipolar input signal. Links L1 and L2 allow the user to choose a ±5V or ±10V analog input range. With L1 inserted the range will be ±10V, and with L2 inserted it will be ±5V.

The AD585 is the input sample-and-hold. Its $\overline{\text{HOLD}}$ input is driven from IC4 (1/2 7474 D-type flip-flop). The input signal is sampled at the end of conversion, when $\overline{\text{SYNC}}$ goes high and is held when the CONVST signal goes low. To make sure that the sample-and-hold has enough time to acquire the input signal, the time from sample-and-hold should be at least 3µs. Links L3, L4, L5 and L6 allow the user to choose the output code format for the device. See Table I for the output code truth table.

The PCB layout is designed so that all external connections except the V_{DD} and V_{SS} power supplies can be made in any of three ways:

1. 32-way single-sided edge connector.
2. Eurocard connector, J1.
3. 26-pin plug, J2.

The pinout for the 26-way connector is shown in Figure 23, and the other pinouts are shown in Figure 22. The V_{DD} and V_{SS} power supplies are connected at the top of the board (see Figure 26).



J2: 26-WAY IDC PLUG

Figure 23. J2 Pin Configuration

The printed circuit board layout is shown in Figure 24 and 25. Figure 24 is the component side layout and Figure 25 is the solder side layout. The component overlay is shown in Figure 26. In the layout, the STAR ground point is located at Pin 4 (AGND). Pin 10 (DGND), the AD585 ground, AD711 ground and the ground plane are connected directly to this point.

To ensure optimum performance, the AD7772 power supplies are decoupled as shown. The V_{REF} pin is decoupled with R1, C5 and C6. All ADC decoupling capacitors are placed as close as possible to the device.

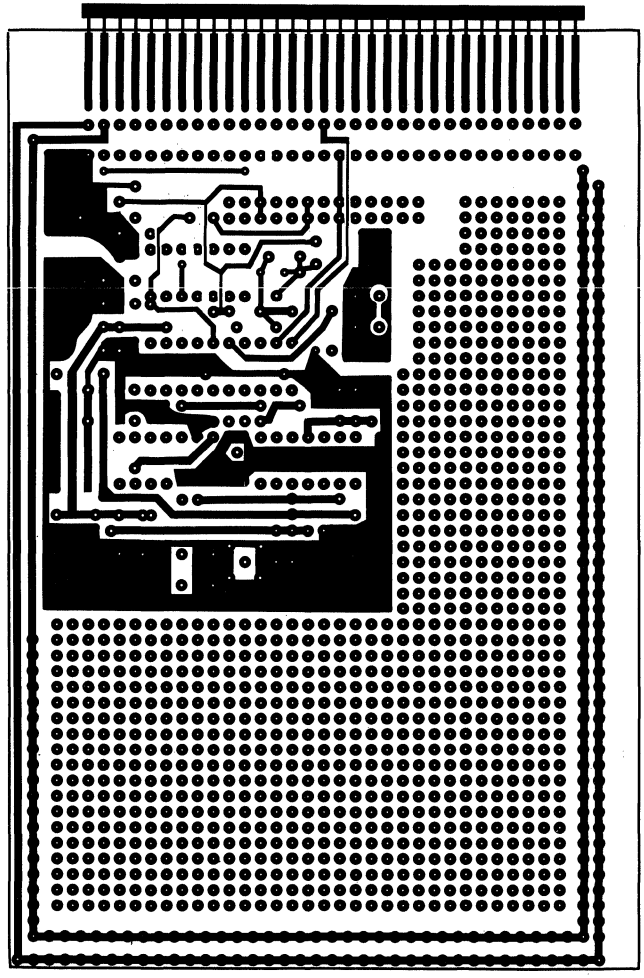


Figure 24. PCB Component Side Layout for Figure 22

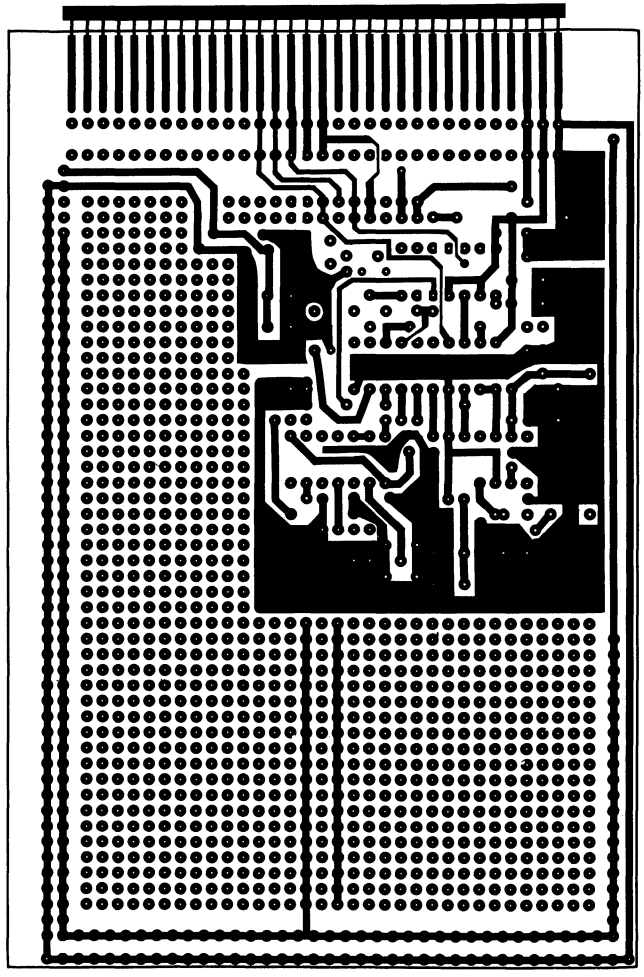


Figure 25. PCB Solder Side Layout for Figure 22

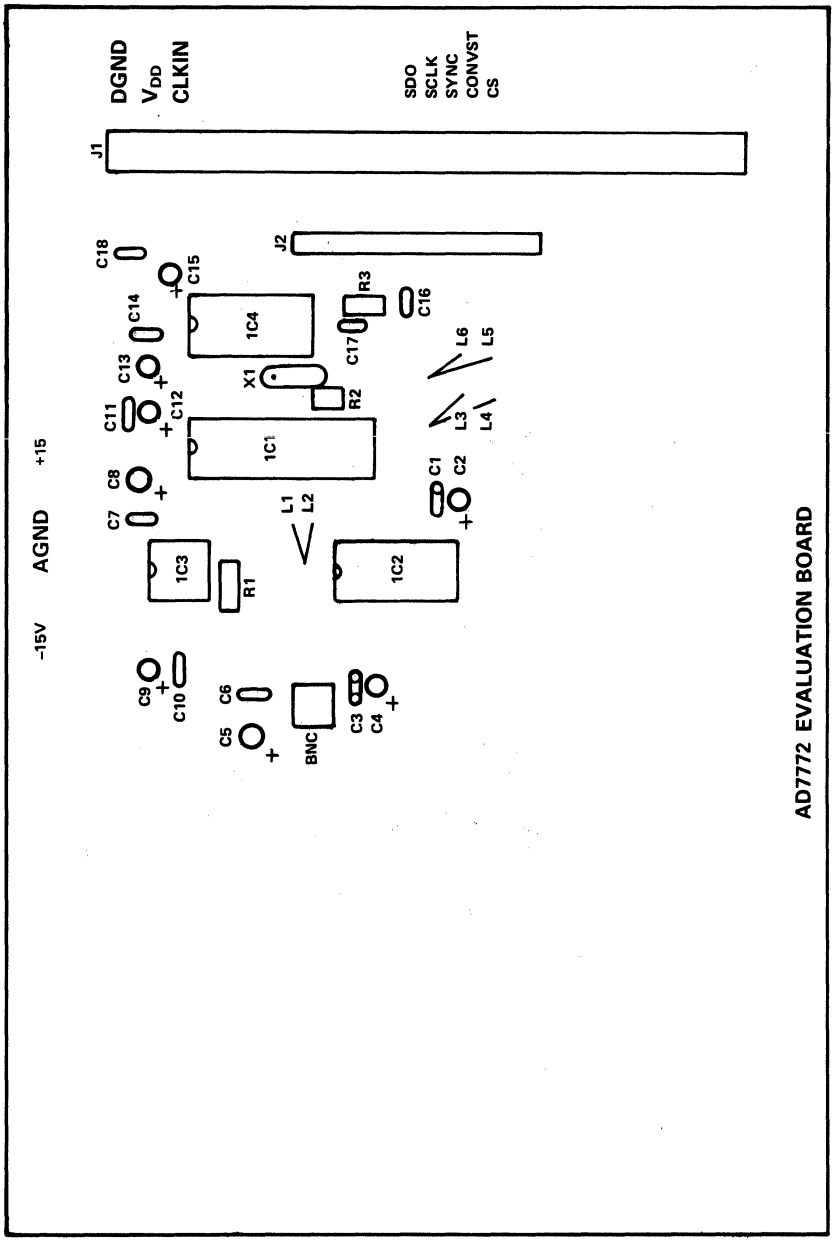


Figure 26. Component Overlay for Circuit of Figure 22

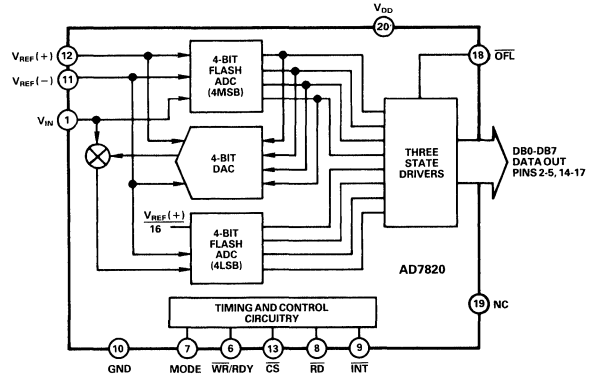
LC² MOS High Speed µP-Compatible 8-Bit ADC with Track/Hold Function

AD7820

FEATURES

Fast Conversion Time: 1.36µs max
Built-In Track-and-Hold Function
No Missed Codes
No User Trims Required
Single +5V Supply
Ratiometric Operation
No External Clock
Skinny 20-Pin DIP and 20-Terminal Surface Mount Packages

AD7820 FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7820 is a high speed, microprocessor-compatible 8-bit analog-to-digital converter which uses a half-flash conversion technique to achieve a conversion time of 1.36µs. The converter has a 0V to +5V analog input voltage range with a single +5V supply.

The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC. The input to the AD7820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals with slew rates less than 100mV/µs.

The part is designed for ease of microprocessor interface with the AD7820 appearing as a memory location or I/O port without the need for external interfacing logic. All digital outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. A non-three state overflow output is also provided to allow cascading of devices to give higher resolution.

The AD7820 is fabricated in an advanced, all ion-implanted, high speed, Linear Compatible CMOS (LC²MOS) process and features a low maximum power dissipation of 75mW. It is available in both 0.3"-wide, 20-pin DIPs and in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC²MOS process, enables very fast conversion times. The maximum conversion time for the WR-RD mode is 1.36µs, with 1.6µs the maximum for the RD mode.
2. Total Unadjusted Error
   The AD7820 features an excellent total unadjusted error figure of less than 1/2LSB over the full operating temperature range. The part is also guaranteed to have no missing codes over the entire temperature range.
3. Built-In Track-and-Hold
   The analog input circuitry uses sampled-data comparators, which by nature have a built-in track-and-hold function. As a result, input signals with slew rates up to 100mV/µs can be converted to 8-bits without external sample-and-hold. This corresponds to a 5V peak-to-peak, 7kHz sine-wave signal.
4. Single Supply
   Operation from a single +5V supply with a positive voltage reference allows operation of the AD7820 in microprocessor systems without any additional power supplies.

SPECIFICATIONS

(V_{DD} = +5V; V_{REF}(+) = +5V; V_{REF}(−) = GND = 0V unless otherwise stated).
All specifications T_{min} to T_{max} unless otherwise specified. Specifications apply for RD Mode (Pin 7 = 0V)

Parameter	K Version[1]	L Version	B, T Versions	C, U Versions	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which No Missing Codes are guaranteed	8	8	8	8	Bits	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
V_{REF}(+) Input Voltage Range	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V min/V max	
V_{REF}(−) Input Voltage Range	GND/V_{REF}(+)	GND/V_{REF}(+)	GND/V_{REF}(+)	GND/V_{REF}(+)	V min/V max	
ANALOG INPUT						
Input Voltage Range	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V min/V max	
Input Leakage Current	±3	±3	±3	±3	μA max	
Input Capacitance[3]	45	45	45	45	pF typ	
LOGIC INPUTS						
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	1	1	μA max	
I_{INH} ($\overline{WR}$)	3	3	3	3	μA max	
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
MODE						
V_{INH}	3.5	3.5	3.5	3.5	V min	
V_{INL}	1.5	1.5	1.5	1.5	V max	
I_{INH}	200	200	200	200	μA max	50 μA typ
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7, $\overline{OFL}$, $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360μA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
I_{OUT} (DB0–DB7)	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
RDY						
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 2.6mA
I_{OUT}	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING[3]	0.2	0.2	0.2	0.2	V/μs typ	
	0.1	0.1	0.1	0.1	V/μs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[4]	15	15	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0V
Power Dissipation	40	40	40	40	mW typ	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16LSB typ V_{DD} = 5V ±5%

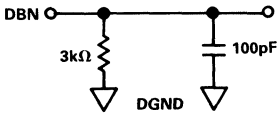
NOTES
[1]Temperature Ranges are as follows:
AD7820K, L Versions; 0 to +70°C
AD7820B, C Versions; −25°C to +85°C
AD7820T, U Versions; −55°C to +125°C
[2]Total Unadjusted Error includes offset, full-scale and linearity errors.
[3]Sample tested at 25°C by Product Assurance to ensure compliance.
[4]See Typical Performance Characteristics.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V; V_{REF}(+) = +5V; V_{REF}(−) = GND = 0V unless otherwise stated)

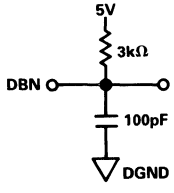
Parameter	Limit at 25°C (All grades)	Limit at T_{min}, T_{max} (K, L, B, C grades)	Limit at T_{min}, T_{max} (T, U grades)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ TO $\overline{RD}$/$\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ TO $\overline{RD}$/$\overline{WR}$ Hold Time
t_{RDY}[2]	70	90	100	ns max	$\overline{CS}$ to Delay. Pull-Up Resistor 5kΩ.
t_{CRD}	1.6	2.0	2.5	μs max	Conversion Time (RD Mode)
t_{ACC0}[3]	t_{CRD} + 20	t_{CRD} + 35	t_{CRD} + 50	ns max	Data Access Time (RD Mode)
t_{INTH}[2]	125	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	175	225	225	ns max	
t_{DH}[4]	60	80	100	ns max	Data Hold Time
t_P	500	600	600	ns min	Delay Time between Conversions
t_{WR}	600	600	600	ns min	Write Pulse Width
	50	50	50	μs max	
t_{RD}	600	700	700	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{ACC1}[3]	160	225	250	ns max	Data Access Time (WR–RD Mode, see Fig. 5b)
t_{R1}	140	200	225	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	700	–	–	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	1000	1400	1700	ns max	
t_{ACC2}[3]	70	90	110	ns max	Data Access Time (WR–RD Mode, see Fig. 5a)
t_{IHWR}[2]	100	130	150	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}	50	65	75	ns max	Data Access Time after $\overline{INT}$ (Stand-Alone Operation)

NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits

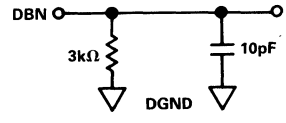


a. High-Z to V_{OH}

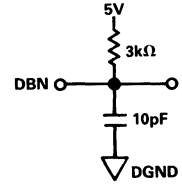


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . 0V, +7V
Digital Input Voltage to GND
Pins 6-8, 13) . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to GND
(Pins 2-5, 9, 14-18) . . . . . −0.3V, V_{DD} +0.3V
V_{REF} (+) to GND . . . . . V_{REF} (−), V_{DD} +0.3V
V_{REF} (−) to GND . . . . . 0V, V_{REF} (+)
V_{IN} to GND . . . . . −0.3V, V_{DD} +0.3V
Operating Temperature Range
Commercial (K, L Versions) . . . . . 0 to +70°C
Industrial (B, C Versions) . . . . . −25°C to +85°C
Extended (T, U Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

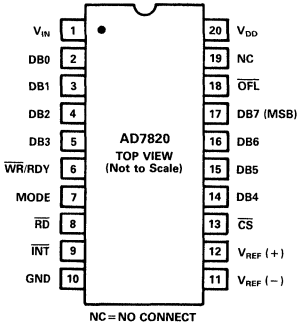
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

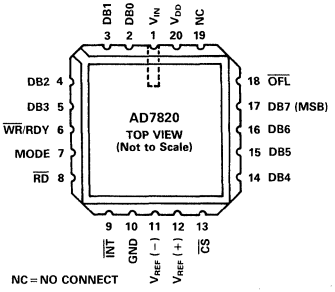
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

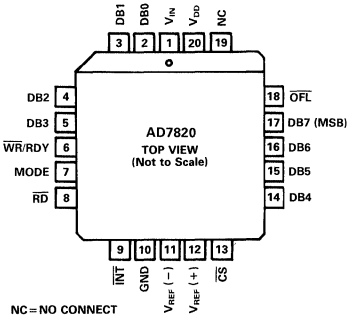
DIP



LCCC



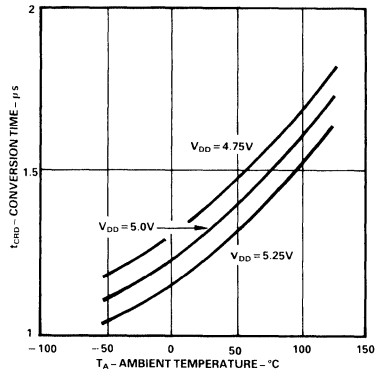
PLCC



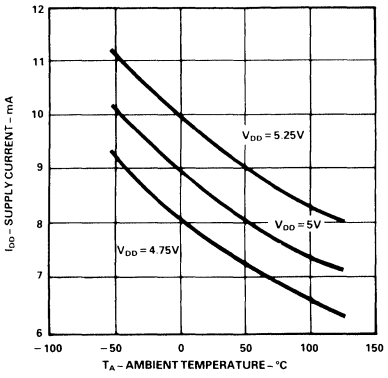
ORDERING INFORMATION[1, 2]

Total Unadjusted Error	Temperature Range and Package Options[3, 4] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-20)	**Hermetic (Q-20)**	**Hermetic (Q-20)**
±1LSB	AD7820KN	AD7820BQ	AD7820TQ
±1/2LSB	AD7820LN	AD7820CQ	AD7820UQ
	PLCC[5] (P-20A)		**LCCC[6] (E-20A)**
±1LSB	AD7820KP		AD7820TE
±1/2LSB	AD7820LP		AD7820UE

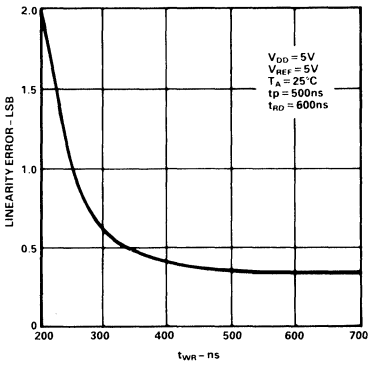
NOTE
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-88650.
[2]Analog Devices reserves the right to ship ceramic packages (package outline D-20) in lieu of cerdip packages (package outline Q-20).
[3]See Section 14 for package outline information.
[4]Also available in SOIC packages (AD7820KR, AD7820LR).
[5]PLCC: Plastic Leaded Chip Carrier.
[6]LCCC: Leadless Ceramic Chip Carrier.



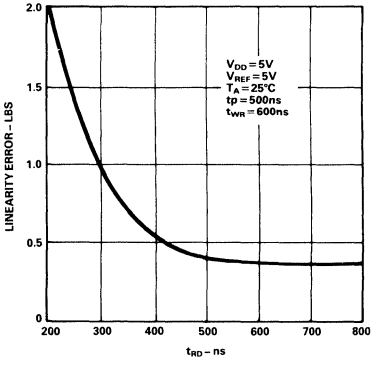
Conversion Time (RD Model) vs. Temperature



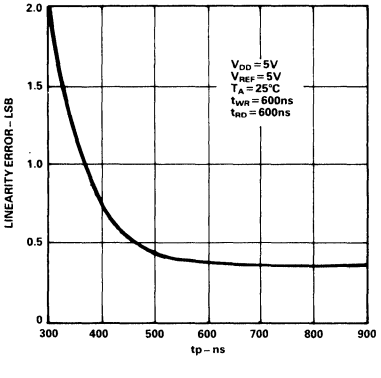
Power Supply Current vs. Temperature (not including reference ladder)



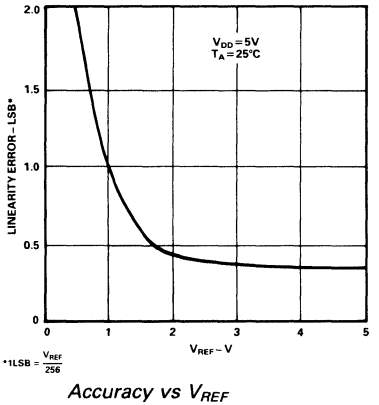
Accuracy vs. t_{WR}



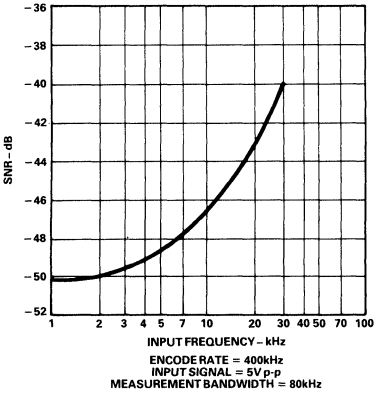
Accuracy vs. t_{RD}



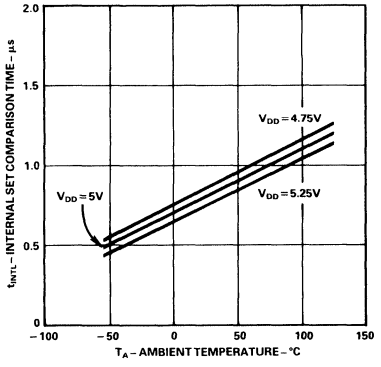
Accuracy vs. tp



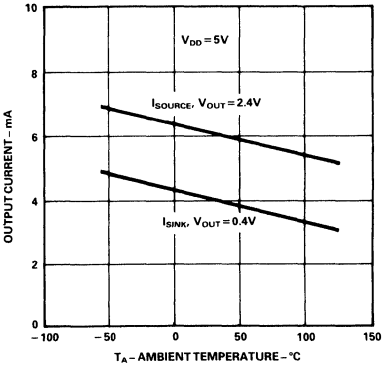
Accuracy vs V_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



Signal-Noise Ratio vs. Input Frequency



t_{INTL}, Internal Time Delay vs. Temperature



Output Current vs. Temperature

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{IN}	Analog Input. Range: $V_{REF}(-)$ to $V_{REF}(+)$.
2	DB0	Data Output. Three State Output, bit 0 (LSB)
3	DB1	Data Output. Three State Output, bit 1
4	DB2	Data Output. Three State Output, bit 2
5	DB3	Data Output. Three State Output, bit 3
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	Mode	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. It is internally tied to GND through a 50μA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{RD}$ or $\overline{CS}$. See Digital Interface section.
10	GND	Ground
11	$V_{REF}(-)$	Lower limit of reference span. Range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{DD}$
13	$\overline{CS}$	Chip Select Input. $\overline{CS}$, the decoded device address, must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	Data Output. Three State Output, bit 4
15	DB5	Data Output. Three State Output, bit 5
16	DB6	Data Output. Three State Output, bit 6
17	DB7	Data Output. Three State Output, bit 7 (MSB)
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+) - 1/2$LSB), $\overline{OFL}$ will be low at the end of conversion. It is a non three state output which can be used to cascade 2 or more devices to increase resolution.
19	NC	No connection.
20	V_{DD}	Power supply voltage, +5V

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7820 uses a half-flash conversion technique whereby two 4-bit flash A/D converters are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. For a full 8-bit reading to be realized, the upper 4-bit flash, the most significant (MS) flash, performs a conversion to provide the 4 most significant data bits. An internal DAC, driven by the 4 MSBs, then recreates an analog approximation of the input voltage. This analog result is subtracted from the input, and the difference is converted by the lower flash ADC, the least significant (LS) flash, to provide the 4 least significant bits of the output data. The MS flash ADC also has one additional comparator to detect input overrange.

OPERATING SEQUENCE

The operating sequence for the AD7820 in the WR-RD mode is shown in Figure 3. A set-up time of 500ns is required prior to the falling edge of $\overline{WR}$. (This 500ns is required between reading data from the AD7820 and starting another conversion). When $\overline{WR}$ is low the input comparators track the analog input signal, V_{IN}. On the rising edge of $\overline{WR}$, the input signal is sampled and the result for the four most significant bits is latched. $\overline{INT}$ goes low approximately 700ns after the rising edge of $\overline{WR}$. This indicates that conversion is complete and the data result is already in the output latch. $\overline{RD}$ going low then accesses the output data. If a faster conversion time is required, the $\overline{RD}$ line can be brought low 600ns after $\overline{WR}$ goes high. This latches the lower 4 bits of data and accesses the output data on DB0–DB7.

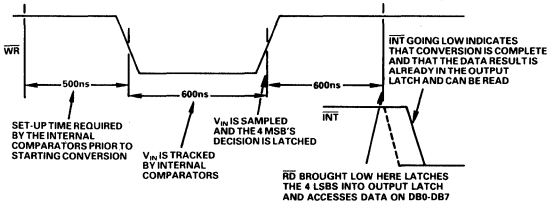


Figure 3. Operating Sequence (WR-RD Mode)

DIGITAL INTERFACE

The AD7820 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low the converter is in the RD mode, with this pin high the AD7820 is set up for the WR-RD mode.

RD Mode

The timing diagram for the RD mode is shown in Figure 4. In the RD mode configuration, conversion is initiated by taking $\overline{RD}$ low. The $\overline{RD}$ line is then kept low until output data appears. It is very useful with microprocessors which can be forced into a WAIT state, with the microprocessor starting a conversion, waiting, and then reading data with a single READ instruction. In this mode, pin 6 of the AD7820 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low at the completion of conversion. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

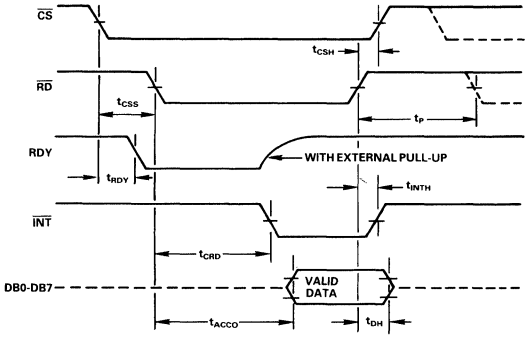


Figure 4. RD Mode

WR-RD Mode

In the WR-RD mode, pin 6 is configured as the WRITE input for the AD7820. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

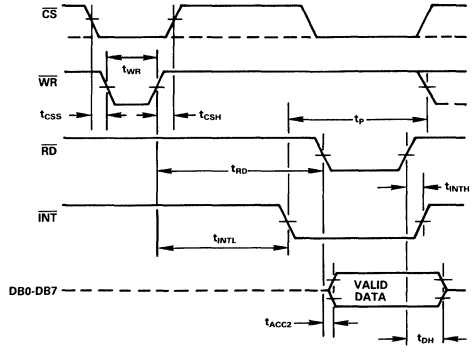


Figure 5a. WR-RD Mode ($t_{RD}>t_{INTL}$)

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 5a). $\overline{INT}$ typically goes low 700ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0-DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

The alternative option can be used to shorten the conversion time. To achieve this, the status of the $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low 600ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data outputs (DB0-DB7). $\overline{INT}$ also goes low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 5b.

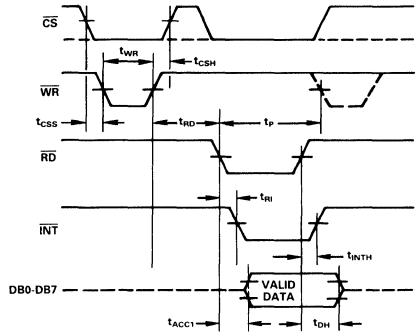


Figure 5b. WR-RD Mode ($t_{RD}<t_{INTL}$)

The AD7820 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid typically 700ns after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 6.

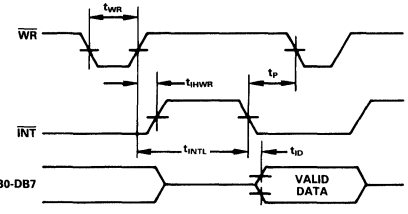


Figure 6. WR-RD Mode Stand-Alone Operation, $\overline{CS}=\overline{RD}=0$

APPLYING THE AD7820

REFERENCE AND INPUT

The two reference inputs on the AD7820 are fully differential and define the zero to full-scale input range of the A/D converter. As a result, the span of the analog input can easily be varied since this range is equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing the reference span, $V_{REF}(+)-V_{REF}(-)$, to less than 5V the sensivity of the converter can be increased (i.e., if $V_{REF}=2V$ then 1LSB = 7.8mV). The input/reference arrangement also facilitates ratiometric operation.

This reference flexibility also allows the input span to be offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Therefore, although V_{IN} is not itself differential, it will have nearly differential-input capability in most measurement applications because of the reference design. Figure 7 shows some of the configurations that are possible.

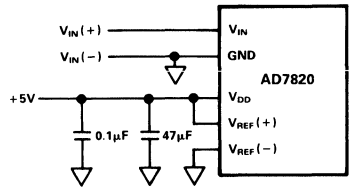


Figure 7a. Power Supply as Reference

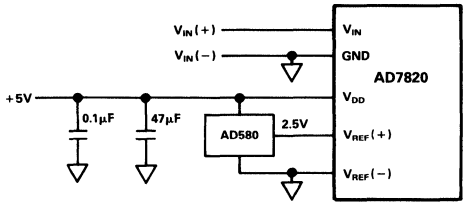


Figure 7b. External Reference 2.5V Full Scale

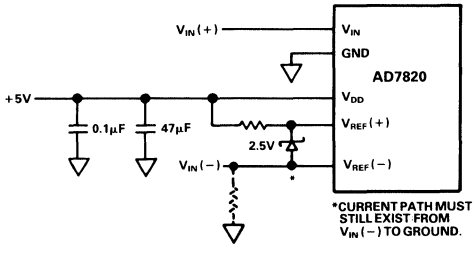


Figure 7c. Input Not Referenced to GND

INPUT CURRENT

Due to the novel conversion techniques employed by the AD7820, the analog input behaves somewhat differently than in conventional devices. The ADC's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the AD7820 is shown in Figure 8a. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, and V_{IN} is connected to the most significant and least significant comparators. Therefore, V_{IN} is connected to thirty one 1pF input capacitors at the same time.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of input stray capacitance must be charged. For large source resistances, the analog input can be modelled as an RC network as shown in Figure 8b. As R_S increases, it takes longer for the input capacitance to charge.

In the RD mode, the time for which the input comparators track the analog input is 600ns at the start of conversion. In the WR-RD mode the input comparators track V_{IN} for the duration of the $\overline{WR}$ pulse. Since other factors cause this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

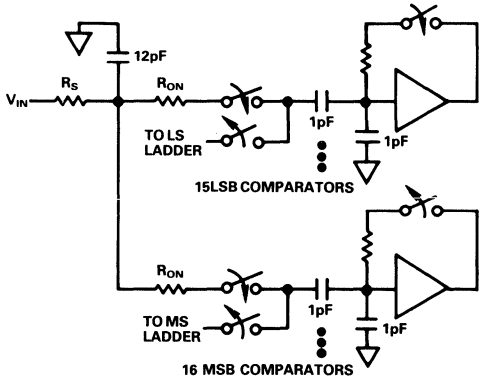


Figure 8a. AD7820 Equivalent Input Circuit

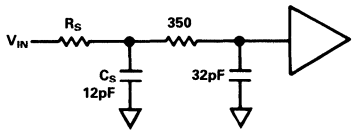


Figure 8b. RC Network Model

INPUT FILTERING

It should be made clear that transients on the analog input signal, caused by charging current flowing into V_{IN} will not normally degrade the ADC's performance. In effect, the AD7820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients with an external capacitor at the V_{IN} terminal.

INHERENT SAMPLE-HOLD

A major benefit of the AD7820's input structure is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain stable to at least ½LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion. The AD7820 input comparators, by nature of their input switching inherently accomplish this sample-and-hold function. Although the conversion time for the AD7820 is 1.36µs, the time through which V_{IN} must be ½LSB stable is much smaller. The AD7820 "samples" V_{IN} only when $\overline{WR}$ is low. The value of V_{IN} approximately 100ns (internal propogation delay) after the rising edge of $\overline{WR}$ is the measured value. This value is then used in the least significant flash to generate the lower 4-bits of data.

Input signals with slew rates typically below 200mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the AD7820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. A SAR type converter with a conversion time as fast as 1μs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The AD7820 with no such help, can typically measure 5V, 10kHz waveforms.

Applications

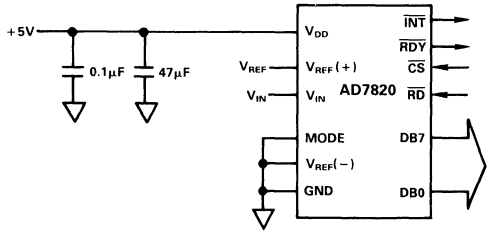


Figure 9a. 8-Bit Resolution

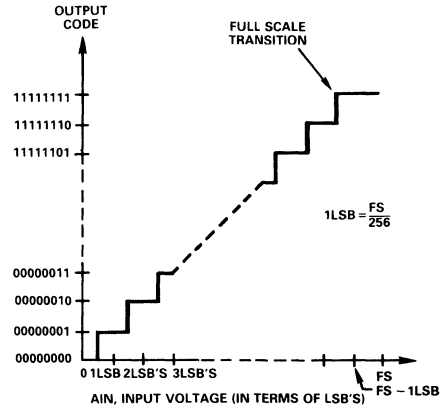


Figure 9b. Nominal Transfer Characteristic for 8-Bit Resolution Circuit

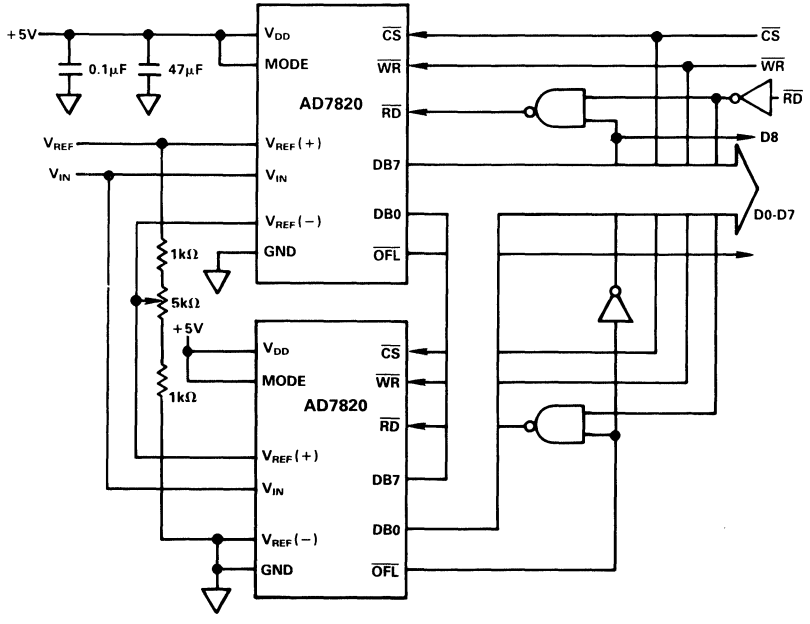


Figure 10. 9-Bit Resolution

Applications

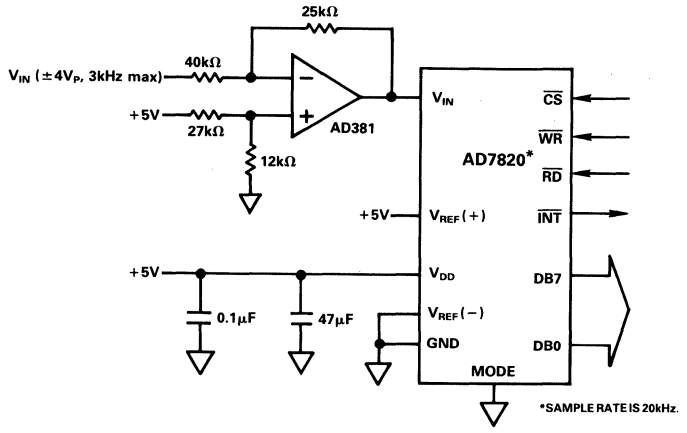


Figure 11. Telcom A/D Converter

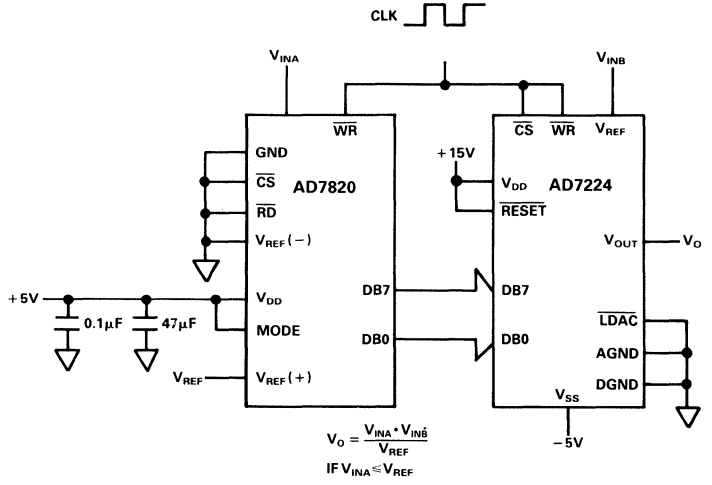


Figure 12. 8-Bit Analog Multiplier

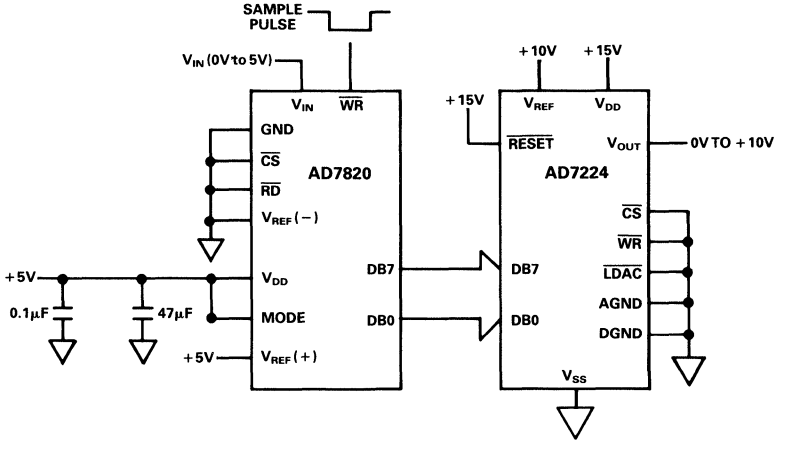


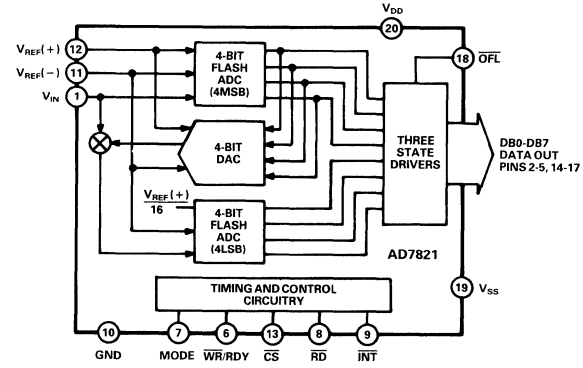
Figure 13. Fast Infinite Sample-and-Hold

LC²MOS High-Speed µP Compatible 8-Bit ADC with Track/Hold Function

AD7821

FEATURES
Fast Conversion Time: 660ns max
100kHz Track-and-Hold Function
1MHz Sample Rate
Unipolar and Bipolar Input Ranges
Ratiometric Reference Inputs
No External Clock
Skinny 20-Pin DIPs and 20-Terminal Surface Mount Packages

AD7821 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7821 is a high-speed, 8-bit, sampling, analog-to-digital converter that offers improved performance over the popular AD7820. It offers a conversion time of 660ns (vs 1.36µs for the AD7820) and 100kHz signal bandwidth (vs 6.4kHz). The sampling instant is better defined and occurs on the falling edge of $\overline{WR}$ or $\overline{RD}$. The provision of a V_{SS} pin (Pin 19) allows the part to operate from ±5V supplies and digitize bipolar input signals. Alternatively, for unipolar inputs, the V_{SS} pin can be grounded and the AD7821 will operate from a single +5V supply, like the AD7820.

The AD7821 has a built-in track-and-hold function capable of digitizing full-scale signals up to 100kHz max. It also uses a half-flash conversion technique which eliminates the need to generate a CLK signal for the ADC.

The AD7821 is designed with standard microprocessor control signals ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and latched, three-state data outputs capable of interfacing to high-speed data buses. An overflow output ($\overline{OFL}$) is also provided for cascading devices to achieve higher resolution.

The AD7821 is fabricated in Linear-Compatible CMOS (LC²MOS), an advanced, mixed technology process combining precision bipolar circuits with low-power CMOS logic. The part features a low power dissipation of 50mW.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC²MOS process, enables a very fast conversion time. The conversion time for the WR-RD mode is 660ns, with 700ns for the RD mode.
2. Built-In Track-and-Hold
   This allows input signals with slew rates up to 1.6V/µs to be converted to 8-bits without an external track-and-hold. This corresponds to a 5V peak-to-peak, 100kHz sine-wave signal.
3. Total Unadjusted Error
   The AD7821 features an excellent total unadjusted error figure of less than ±1LSB over the full operating temperature range.
4. Unipolar/Bipolar Input Ranges
   The AD7821 is specified for single supply (+5V) operation with a unipolar full-scale range of 0 to +5V, and for dual supply (±5V) operation with a bipolar input range of ±2.5V. Typical performance characteristics are given for other input ranges.
5. Dynamic Specifications for DSP Users
   In addition to the traditional ADC specifications, the AD7821 is specified for ac parameters, including signal-to-noise ratio, distortion and slew rate.

SPECIFICATIONS

V_{DD} = +5V ±5%, GND = 0V. Unipolar Input Range: V_{SS} = GND, $V_{REF}(+)$ = 5V, $V_{REF}(-)$ = GND. Bipolar Input Range: V_{SS} = −5V ±5%, $V_{REF}(+)$ = 2.5V, $V_{REF}(-)$ = −2.5V. These test conditions apply unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated. Specifications apply for RD Mode (Pin 7 = 0V).

Parameter	K Version [1]	B, T Version	Units	Comments
UNIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Total Unadjusted Error[3]	±1	±1	LSB max	
Minimum Resolution for which No Missing Codes are Guaranteed	8	8	Bits	
BIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Zero Code Error	±1	±1	LSB max	
Full Scale Error	±1	±1	LSB max	
Signal-to-Noise Ratio (SNR)[3]	45	45	dB min	V_{IN} = 99.85kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500kHz
Total Harmonic Distortion (THD)[3]	−50	−50	dB max	V_{IN} = 99.85kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500kHz
Peak Harmonic or Spurious Noise[3]	−50	−50	dB max	V_{IN} = 99.85kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500kHz
Intermodulation Distortion (IMD)[3]				fa(84.72kHz) and fb(94.97kHz) Full-Scale Sine Waves with $f_{SAMPLING}$ = 500kHz
	−50	−50	dB max	Second order terms
	−50	−50	dB max	Third order terms
Slew Rate, Tracking[3]	1.6	1.6	V/μs max	
	2.36	2.36	V/μs typ	
REFERENCE INPUT				
Input Resistance	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(-)/V_{DD}$	$V_{REF}(-)/V_{DD}$	V min/V max	
$V_{REF}(-)$ Input Voltage Range	$V_{SS}/V_{REF}(+)$	$V_{SS}/V_{REF}(+)$	V min/V max	
ANALOG INPUT				
Input Voltage Range	$V_{REF}(-)/V_{REF}(+)$	$V_{REF}(-)/V_{REF}(+)$	V min/V max	
Input Leakage Current	±3	±3	μA max	$-5V \le V_{IN} \le +5V$
Input Capacitance	55	55	pF typ	
LOGIC INPUTS				
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$				
V_{INH}	2.4	2.4	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	μA max	
I_{INH} ($\overline{WR}$)	3	3	μA max	
I_{INL}	−1	−1	μA max	
Input Capacitance[4]	8	8	pF max	Typically 5pF
MODE				
V_{INH}	3.5	3.5	V min	
V_{INL}	1.5	1.5	V max	
I_{INH}	200	200	μA max	50 μA typ
I_{INL}	−1	−1	μA max	
Input Capacitance[4]	8	8	pF max	Typically 5pF
LOGIC OUTPUTS				
DB0-DB7, $\overline{OFL}$, $\overline{INT}$				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 360μA
V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6mA
I_{OUT} (DB0-DB7)	±3	±3	μA max	Floating State Leakage
Output Capacitance[4] (DB0-DB7)	8	8	pF max	Typically 5pF
RDY				
V_{OL}	0.4	0.4	V max	I_{SINK} = 2.6mA
I_{OUT}	±3	±3	μA max	Floating State Leakage
Output Capacitance[4]	8	8	pF max	Typically 5pF
POWER SUPPLY				
I_{DD}[5]	15	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0V
I_{SS}	100	100	μA max	$\overline{CS}$ = $\overline{RD}$ = 0V
Power Dissipation	50	50	mW typ	
Power Supply Sensitivity	±1/4	±1/4	LSB max	±1/16LSB typ, V_{DD} = 4.75V to 5.25V, ($V_{REF}(+)$ = 4.75V max for Unipolar Mode)

NOTES

[1]Temperature Ranges are as follows:
K Version: 0 to +70°C
B Version: −25°C to +85°C
T Version: −55°C to +125°C

[2]1LSB = 19.53mV for both the unipolar (0 to +5V) and bipolar (−2.5V to +2.5V) input ranges.

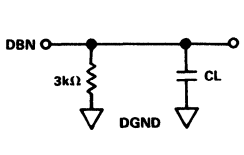
[3]See Terminology.

[4]Sample tested at +25°C to ensure compliance.

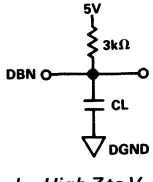
[5]See Typical Performance Characteristics.

Specifications subject to change without notice.

Test Circuits

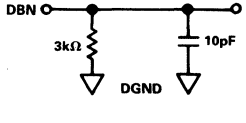


a. High Z to V_{OH}

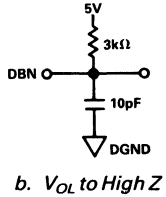


b. High Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High Z



b. V_{OL} to High Z

Figure 2. Load Circuits for Data Hold Time Test

TIMING CHARACTERISTICS[1] (V_{DD} = +5V ±5%, V_{SS} = 0V or −5V ±5%; Unipolar or Bipolar Input Range)

Parameter	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (K, B, Grades)	Limit at T_{min}, T_{max} (T Grade)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time
t_{RDY}[2]	70	85	100	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5k1.
t_{CRD}	700	875	975	ns max	Conversion Time (RD Mode)
t_{ACC0}[3]					Data Access Time (RD Mode)
	t_{CRD} + 25	t_{CRD} + 30	t_{CRD} + 35	ns max	C_L = 20pF
	t_{CRD} + 50	t_{CRD} + 65	t_{CRD} + 75	ns max	C_L = 100pF
t_{INTH}[2]	50	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	80	85	90	ns max	
t_{DH}[4]	15	15	15	ns min	Data Hold Time
	60	70	80	ns max	
t_P	350	425	500	ns min	Delay Time between Conversions
t_{WR}	250	325	400	ns min	Write Pulse Width
	10	10	10	µs max	
t_{RD}	250	350	450	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{READ1}	160	205	240	ns min	$\overline{RD}$ Pulse Width (WR-RD Mode, see Figure 12b)
t_{ACC1}[3]					Determined by t_{ACC1} Data Access Time (WR-RD Mode, see Figure 12b)
	160	205	240	ns max	C_L = 20pF
	185	235	275	ns max	C_L = 100pF
t_{RI}	150	185	220	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	380	–	–	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	500	610	700	ns max	
t_{READ2}	65	75	85	ns max	$\overline{RD}$ Pulse Width (WR-RD Mode, see Figure 12a)
t_{ACC2}[3]					Determined by t_{ACC2} Data Access Time (WR-RD Mode, see Figure 12a)
	65	75	85	ns max	C_L = 20pF
	90	110	130	ns max	C_L = 100pF
t_{IHWR}[2]	80	100	120	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}[3]					Data Access Time after $\overline{INT}$ (Stand-Alone Operation)
	30	35	40	ns max	C_L = 20pF
	45	60	70	ns max	C_L = 100pF

NOTES
[1]Sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . −0.3V, +7V
V_{SS} to GND . . . . . +0.3V, −7V
Digital Input Voltage to GND
(Pins 6-8, 13) . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to GND
(Pins 2-5, 9, 14-18) . . . . . −0.3V, V_{DD} +0.3V
V_{REF} (+) to GND . . . . . V_{SS} −0.3V, V_{DD} +0.3V
V_{REF} (−) to GND . . . . . V_{SS} −0.3V, V_{DD} +0.3V
V_{IN} to GND . . . . . V_{SS} −0.3V, V_{DD} +0.3V
Operating Temperature Range
Commercial (K Version) . . . . . 0 to +70°C
Industrial (B Version) . . . . . −25°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 8-bit resolution can resolve one part in 2^8 (1/256 of full scale). For the AD7821 operating in either the unipolar or bipolar input range with 5V full scale, one LSB is 19.53mV.

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes relative accuracy, offset error and full-scale error.

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error.

TOTAL HARMONIC DISTORTION

Total harmonic distortion is the ratio of the square root of the sum of the squares of the rms value of the harmonics to the rms value of the fundamental. For the AD7821, total harmonic distortion (THD) is defined as

$$20 \log \left[\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^{2)}}}{V_1} \right] \text{dB}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6, are the rms amplitudes of the individual harmonics.

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa+nfb, where m,n = 0, 1, 2, 3, - - - -. Intermodultaion terms are those for which m or n is not equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), and the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb). For the AD7821 intermodulation distortion is calculated separately for both the second and third order terms.

SIGNAL-TO-NOISE RATIO

Signal-to-noise ratio (SNR) is measured signal-to-noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals (excluding dc) up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process. The theoretical SNR for a sine-wave input is given by:

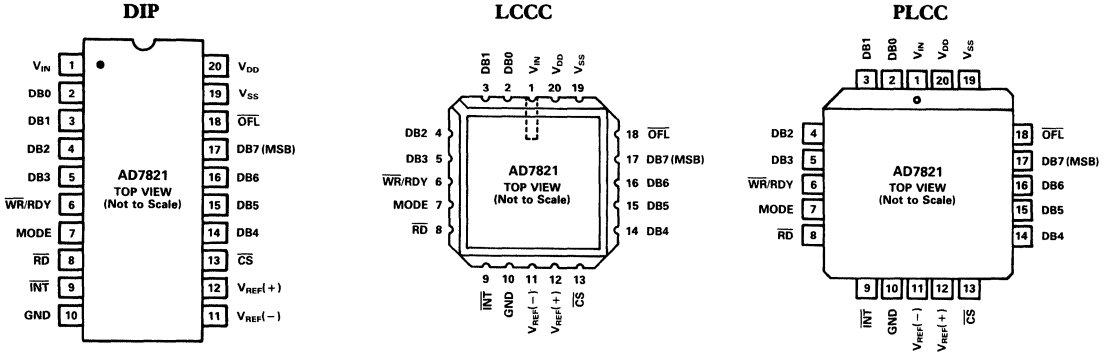
$$\text{SNR} = (6.02N + 1.76)\ \text{dB},$$

where N is the number of bits in the ADC. Thus for an ideal 8-bit ADC, SNR = 50dB.

PEAK HARMONIC OR SPURIOUS NOISE

Peak harmonic or spurious noise is the rms value of the largest nonfundamental frequency (excluding dc) up to half the sampling frequency to the rms value of the fundamental.

PIN CONFIGURATIONS



ORDERING INFORMATION[1]

Temperature Range and Package Options[2]

0 to +70°C	−25°C to +85°C	−55°C to +125°C
Plastic DIP (N-20) AD7821KN	**Hermetic (Q-20)** AD7821BQ	**Hermetic (Q-20)** AD7821TQ
PLCC[3] (P-20A) AD7821KP		**LCCC[4] (E-20A)** AD7821TE

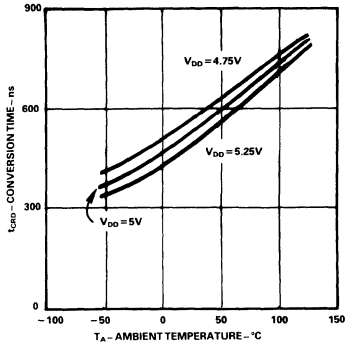
NOTE

[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.

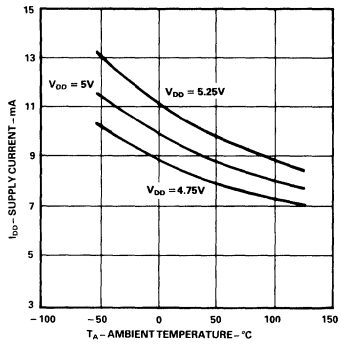
[2]See Section 14 for package outline information.

[3]PLCC: Plastic Leaded Chip Carrier.

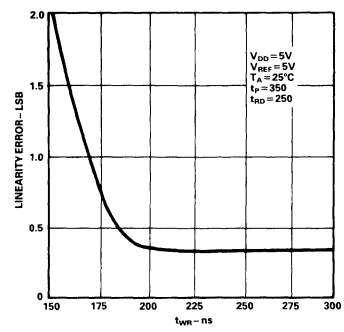
[4]LCCC: Leadless Ceramic Chip Carrier.



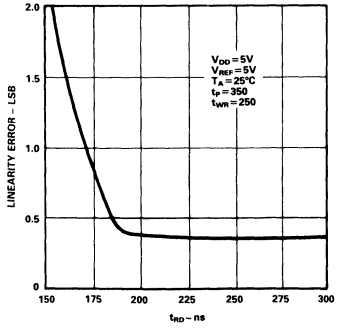
Conversion Time (RD Mode) vs. Temperature



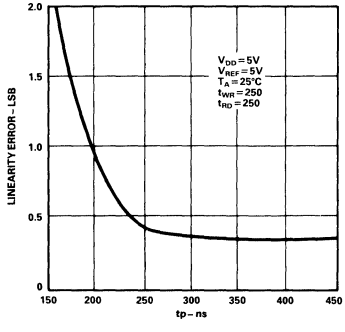
Power Supply Current vs. Temperature (Not Including Reference Ladder)



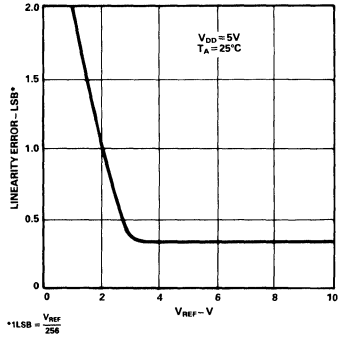
Accuracy vs. t_{WR}



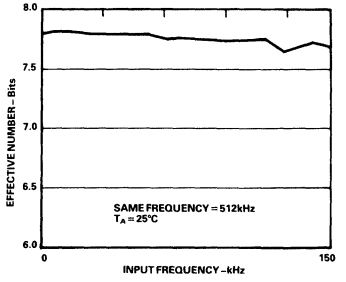
Accuracy vs. t_{RD}



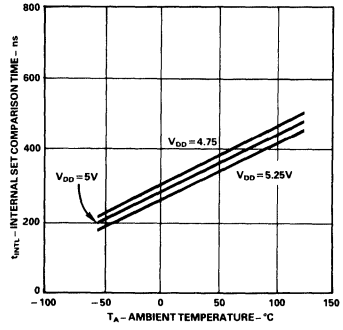
Accuracy vs. t_P



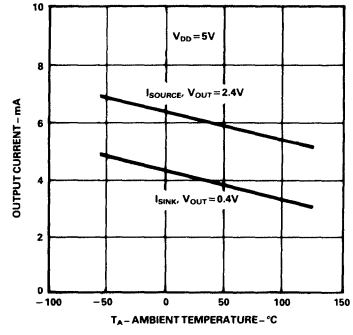
Accuracy vs V_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



Effective Number of Bits vs. Input Signal (±2.5V) Frequency



t_{INTL}, Internal Time Delay vs. Temperature



Output Current vs. Temperature

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{IN}	Analog Input: Range $V_{REF}(-) \leq V_{IN} \leq V_{REF}(+)$.
2	DB0	Three-State Data Output (LSB).
3-5	DB1-DB3	Three-State Data Outputs.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. This input is internally pulled low through a 50μA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$. See Digital Interface section.
10	GND	Ground.
11	$V_{REF}(-)$	Lower limit of reference span. Range: $V_{SS} \leq V_{REF}(-) < V_{REF}(+)$.
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) < V_{REF}(+) \leq V_{DD}$.
13	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
14-16	DB4-DB6	Three-State Data Outputs.
17	DB7	Three-State Data Output (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+) - 1/2LSB$), $\overline{OFL}$ will be low at the end of conversion. It is a non-three-state output which can be used to cascade 2 or more devices to increase resolution.
19	V_{SS}	Negative supply voltage. V_{SS} = 0V; Unipolar Operation. V_{SS} = −5V; Bipolar Operation.
20	V_{DD}	Positive supply voltage, +5V.

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7821 uses a half flash conversion technique (see Functional Block Diagram), whereby two 4-bit flash ADCs are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators, which compare an unknown input voltage to the reference ladder, to achieve a 4-bit result. The MS (most significant) flash ADC converts an unknown analog input voltage (V_{IN}) to provide the 4 MS data bits. An internal DAC, driven by the 4 MS data bits, then recreates an analog approximation of the input voltage. The DAC output voltage is subtracted from the analog input, and the difference is converted by the LS (least significant) ADC to provide the 4 LS data bits. The MS flash ADC also has one additional comparator to detect overrange on the analog input.

OPERATING SEQUENCE

The AD7821 has two operating modes. The RD mode allows a conversion to be started and data to be read with a single, extended, READ operation, i.e., $\overline{CS}$ and $\overline{RD}$ are taken low. The conversion process is timed out by internal one-shots. The WR-RD mode uses $\overline{WR}$ to start a conversion and $\overline{RD}$ to read the data and allows the conversion timing to be externally controlled. The operating sequence for the WR-RD mode is shown in Figure 3.

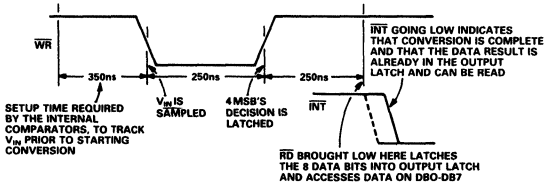


Figure 3. Operating Sequence (WR-RD Mode)

A conversion is initiated and the analog input signal (V_{IN}) sampled on the falling edge of $\overline{WR}$ (falling edge of $\overline{RD}$, RD mode). A setup time (tp, delay time between conversions) of 350ns is required prior to this falling edge. See Digital Interface section for more details. When $\overline{WR}$ is low, the internal MS (most significant) ADC compares the sampled analog input with the reference ladder to provide the 4 MS data bits. A minimum of 250ns is required for this comparison. On the rising edge of $\overline{WR}$, the MS data result is latched internally and the LS (least significant) conversion begins, to yield the 4 LS data bits. $\overline{INT}$ goes low typically 380ns after the rising edge of $\overline{WR}$. This indicates the LS conversion is complete and that both the LS and MS data results are latched into the output buffer. $\overline{RD}$ going low then enables the output data. If a faster conversion time is required, the $\overline{RD}$ line can be brought low 250ns after $\overline{WR}$ goes high. This latches both the LS and MS data bits and outputs the conversion result on DB0-DB7.

REFERENCE AND INPUT

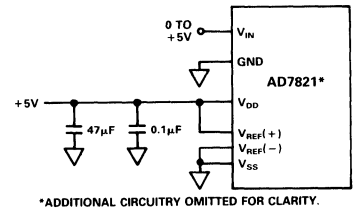
The $V_{REF}(-)$ and $V_{REF}(+)$ reference inputs on the AD7821 are fully differential and define the zero and full-scale input range of the ADC. The transfer characteristic of the part is defined by the integer value of the following expression:

$$\text{Data (LSBs)} = 256\left[\frac{V_{IN} - V_{REF}(-)}{V_{REF}(+) - V_{REF}(-)}\right] + 0.5$$

As a result, the analog input (V_{IN}) of the device can easily be set up to provide both unipolar and bipolar operation. The data output code for unipolar and bipolar operation is Natural Binary and Offset Binary respectively.

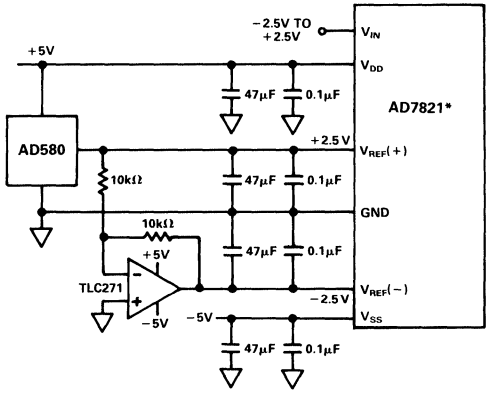
The span of the analog input voltage can easily be varied. By reducing the reference span, $V_{REF}(+) - V_{REF}(-)$, to less than 5V the sensitivity of the converter can be increased (i.e., if V_{REF} = 2V then 1LSB = 7.8mV). The reference flexibility also allows the input span for unipolar operation to be offset from zero ($V_{REF}(-) > GND$). Additionally, the input/reference arrangement facilitates ratiometric operation.

Figures 4 and 5 show some configurations which are possible. For minimum noise a 47μF capacitor in parallel with a 0.1μF capacitor should be connected between the reference inputs and GND.



*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

Figure 4. Power Supply as Reference. Unipolar Operation (0 to +5V)



*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

Figure 5. External Reference. Bipolar Operation (−2.5V to +2.5V)

INPUT CURRENT

The analog input of the AD7821 behaves somewhat differently to conventional A/D converters. This is due to the ADC's sampled-data comparators, which take varying amounts of input current depending on the cycle of the converter.

The equivalent input circuit of the AD7821 is shown in Figure 6. When a conversion ends (e.g., falling edge of $\overline{INT}$, WR-RD mode, $t_{RD} > t_{INTL}$) all the input switches are closed and V_{IN} is connected to the comparators of the internal LS and MS ADCs. Therefore, V_{IN} is connected to thirty-one 1pF input capacitors at the same time.

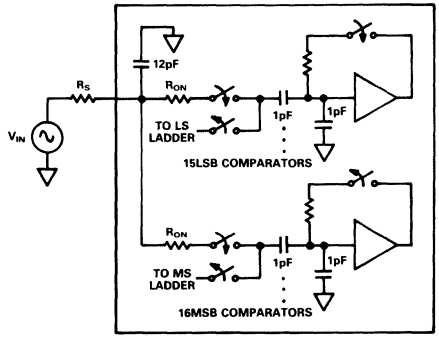


Figure 6. AD7821 Equivalent Input Circuit

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of input stray capacitance must be charged.

The analog input can be modelled as an equivalent RC network as shown in Figure 7. As R_S (source impedance) increases, the input capacitance takes longer to charge.

The comparators track the analog input between conversions. A minimum delay time (t_P) of 350ns is required between conversions to allow for voltage source settling and comparator tracking time. This allows input time constants of 50ns without settling time problems. Typical total input capacitance values of 55pF allow R_S to be 0.9kΩ without lengthening t_P to give V_{IN} more time to settle.

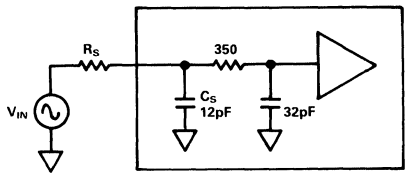


Figure 7. RC Network Model

INPUT TRANSIENTS

Transients on the analog input signal caused by charging current flowing into V_{IN} will not normally degrade the ADC's performance. In effect, the AD7821 does not "look" at the input when these transients occur. The comparators' inputs track V_{IN} and are not sampled until the falling edge of $\overline{WR}$ (WR-RD Mode) or $\overline{RD}$ (RD Mode), so at least 350ns (t_P) is provided to charge the ADC's input capacitance. It is, therefore, not necessary to filter out these transients with an external capacitor at the V_{IN} terminal.

INHERENT TRACK-AND-HOLD

A major benefit of the AD7821's input structure is its ability to measure a variety of high-speed signals without the help of an external track-and-hold. Any ADC which does not have a built-in track-and-hold, regardless of its speed, requires the analog input to remain stable to at least 1/2LSB for the duration of the conversion to maintain full accuracy. This requires the use of a track-and-hold whenever the input is a high-speed signal. The AD7821's sampled-data comparators, by nature of their input switching, inherently accomplish this track-and-hold function. Although the conversion time for the AD7821 is 660ns (WR-RD mode, $t_{WR} + t_{RD} + t_{ACC1}$), the time for which V_{IN} must be stable to 1/2LSB is much smaller. The AD7821 tracks V_{IN} between conversions only, and its value on the falling edge of $\overline{WR}$ or $\overline{RD}$ in the WR-RD or RD modes respectively is the measured value.

SINUSOIDAL INPUTS

The bandwidth of the built-in track-and-hold is 100kHz max (150kHz typ, 5V p-p). This is limited by the analog bandwidth of the comparators and timing skew between the comparator switches. This means that the analog input frequency can be up to 100kHz without the aid of an external track-and-hold. The Nyquist criterion requires that the sampling rate be at least twice the input frequency (i.e., $\geq 2 \times 100$kHz). This requires an ideal antialiasing filter with an inifinite roll-off. To ease the

problem of antialiasing filter design, the sampling rate is usually set much greater than the Nyquist criterion. The maximum sampling rate (f_{max}) for the AD7821 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{0.25E-6+0.25E-6+0.15E-6+0.35E-6}$$

t_{WR} = Write Pulse Width

t_{RD} = Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ Delay

t_P = Delay Time between Conversions

This permits a maximum sampling rate of 1MHz for the AD7821 which is much greater than the Nyquist criterion for sampling a 100kHz analog input signal.

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (Signal-to-Noise Ratio, Harmonic Distortion, Intermodulation Distortion) of an ADC are critical. Since the AD7821 is a very fast ADC with a built-in track-and-hold function, it is specified dynamically as well as with standard dc specifications (Total Unadjusted Error etc.).

SIGNAL-TO-NOISE RATIO AND DISTORTION

The dynamic performance of the AD7821 is evaluated by applying a very low distortion sine-wave signal to the analog input (V_{IN}) which is then sampled at a 512kHz sampling rate. A Fast Fourier Transform (FFT) plot is then generated from which Signal-to-Noise Ratio (SNR) and harmonic distortion data is obtained.

Figure 8 shows a 2048 point FFT plot of the AD7821 with an input signal of 100.25kHz. The SNR is 49.1dB. It should be noted that the harmonics are taken into account when calculating the SNR. The theoretical relationship between SNR and resolution (N) is expressed by the following equation:

SNR = (6.02N + 1.76)db ..... (1)

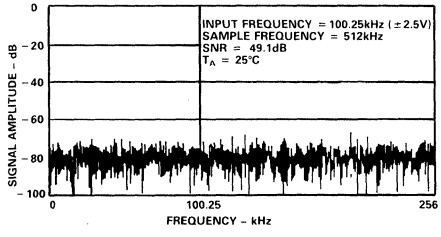


Figure 8. AD7821 FFT Plot

EFFECTIVE NUMBER OF BITS

By working backwards from Equation (1) it is possible to get a measure of ADC performance expressed in effective number of bits (N). A plot of the effective number of bits versus input frequency is given in the Typical Performance Characteristics section. The effective number of bits typically falls between 7.7 and 7.9 corresponding to SNR figures of 48.1 and 49.7dB.

INTERMODULATION DISTORTION

For intermodulation distortion (IMD), an FFT plot is generated by sampling an analog input applied to the ADC consisting of very low distortion sine waves at two frequencies. Figure 9 shows a 2048 point plot for IMD.

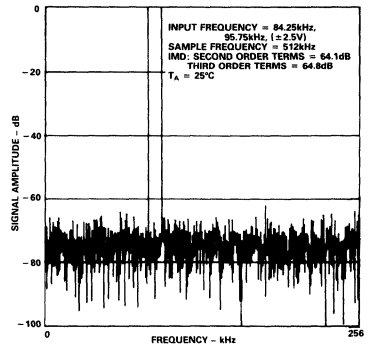


Figure 9. FFT Plot for IMD

HISTOGRAM PLOT

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7821 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. A perfect ADC produces a probability density function described by the equation:

$$P(V) = \frac{1}{\pi(A^2 - V^2)^{1/2}}$$

where A is the peak amplitude of the sine wave and P(V) the probability of occurrence at a voltage V.

If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than the ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 10 shows a histogram plot for the AD7821, which corresponds very well with the ideal shape. The plot indicates very small differential nonlinearity and no missing codes for an input frequency of 100.25kHz.

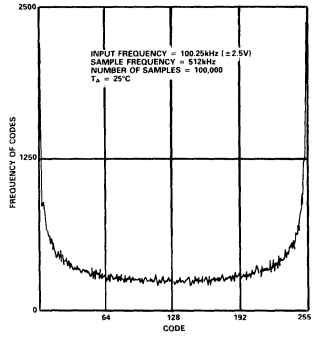


Figure 10. AD7821 Histogram Plot

In digital signal processing applications, where the AD7821 is used to sample ac signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. A precise timer or clock source, to start the ADC conversion process, is the best method of generating equidistant sampling intervals.

The two modes of operation given in the data sheet are suitable for DSP applications because the sampling instant of the AD7821 is well defined. V_{IN} is sampled on the falling edge of $\overline{WR}$ or $\overline{RD}$ in the WR-RD or RD modes respectively.

DIGITAL INTERFACE

The AD7821 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low, the converter is in the RD mode; with this pin high,the AD7821 is set up for the WR-RD mode.

The RD mode is designed for microprocessors which can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when the conversion is complete. The WR-RD mode does not require microprocessor WAIT states. A WRITE operation (i.e., $\overline{CS}$ and $\overline{WR}$ are taken low) initiates a conversion, and a READ operation reads the result when the conversion is complete.

RD Mode (MODE = 0)

The timing diagram for the RD mode is shown in Figure 11. This mode is intended for use with microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A conversion is started by taking $\overline{CS}$ and $\overline{RD}$ low (READ operation). Both $\overline{CS}$ and $\overline{RD}$ are then kept low until output data appears.

In this mode, Pin 6 of the AD7821 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low when a conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

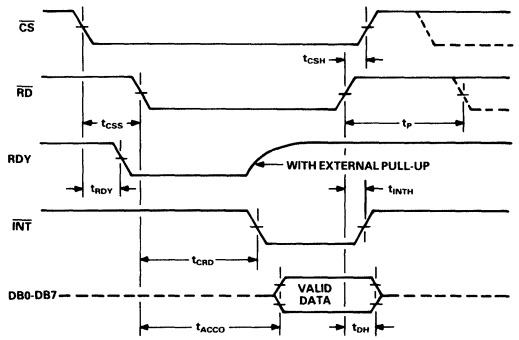


Figure 11. RD Mode

WR-RD Mode (MODE = 1)

In the WR-RD mode, Pin 6 is configured as a WRITE ($\overline{WR}$) input for the AD7821. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 12a). $\overline{INT}$ typically goes low within 380ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0-DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

The alternative option can be used to shorten the conversion time. This is a method for bypassing the internal time-out circuit. The $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low 250ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data output (DB0-DB7). $\overline{INT}$ is driven low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 12b.

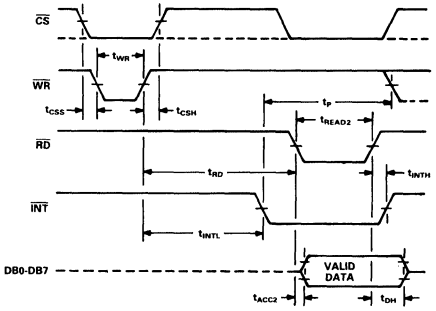


Figure 12a. WR-RD Mode ($t_{RD} > t_{INTL}$)

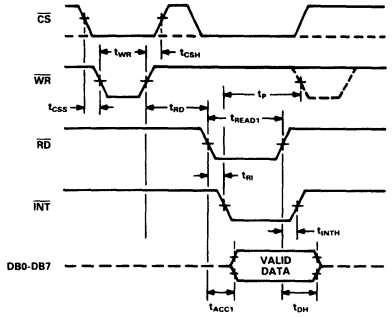


Figure 12b. WR-RD Mode ($t_{RD} < t_{INTL}$)

The AD7821 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low, and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid 530ns (t_{INTL} + t_{ID}) after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 13.

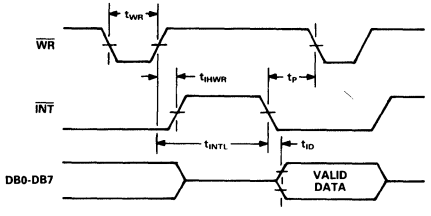


Figure 13. WR-RD Mode Stand-Alone Operation, $\overline{CS} = \overline{RD} = 0$

MICROPROCESSOR INTERFACING

The AD7821 is designed for easy interfacing to microprocessors as a memory mapped perhiperal or an I/O device. This reduces to a minimum the amount of external logic required for interfacing.

AD7821 – 68008 INTERFACE

Figure 14 shows an AD7821 interface to the 68008 microprocessor. The ADC is configured for the RD interface mode. This means that one read instruction starts a conversion and reads the result when the conversion is completed. The read cycle is stretched out over the entire conversion period by taking the $\overline{INT}$ line back to the $\overline{DTACK}$ input of the 68008. Starting a conversion and reading the relevant data consists of a < MOVE B Dn, addr > instruction, where addr is the decoded ADC address and Dn is the data register into which the result is placed.

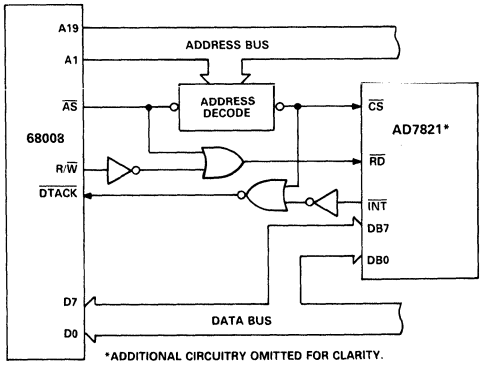


Figure 14. AD7821 to 68008 Interface

AD7821 – 8088 INTERFACE

A typical interface to the 8088 is shown in Figure 15. The AD7821 is configured for the RD interface mode. One read instruction starts a conversion and reads the result. The read cycle is stretched out over the entire conversion period by taking the RDY line back to the READY input of the 8088. Starting a conversion and reading the result consists of a < MOV AX, (addr) > instruction, where addr is the decoded ADC address and AX is the 8088 data register into which the conversion result is placed.

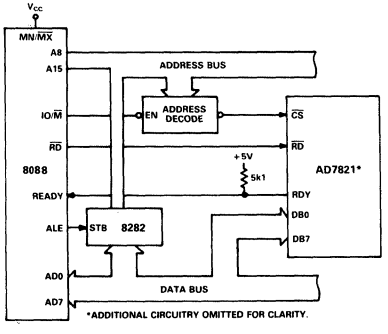


Figure 15. AD7821 to 8088 Interface

AD7821 – TMS32010 INTERFACE

A typical interface to the TMS32010 is shown in Figure 16. The AD7821 is mapped at a port address and the interface is designed for the maximum TMS32010 clock frequency of 20MHz. In this case the AD7821 is configured in the WR-RD interface mode. This means that a write instruction starts a conversion and a read instruction reads the result when the conversion is completed. A precise timer or clock source is used to start a conversion in applications requiring equidistant sampling intervals. The scheme used, whereby the AD7821 generates an interrupt to the TMS32010, is limited in that it does not allow the AD7821 to be sampled at its maximum rate. This is because the time between samples has to be long enough to allow the TMS32010 to service its interrupt and read data from the AD7821. Constant interruption of the TMS32010 by the AD7821, every time the ADC completes a conversion, is not a very efficient use of the processor time. To overcome these problems, some buffer memory or FIFO could be placed between the AD7821 and the TMS32010. The $\overline{INT}$ line of the AD7821 could be used to trigger a pulse which drives its $\overline{CS}$ and $\overline{RD}$ lines and places the AD7821 data into a FIFO or buffer memory. The microprocessor can then read a batch of data from the FIFO or buffer memory at some convenient time. Reading data from the AD7821, after an $\overline{INT}$ has been received, consists of < IN A, PA > instruction (PA is the decoded ADC address).

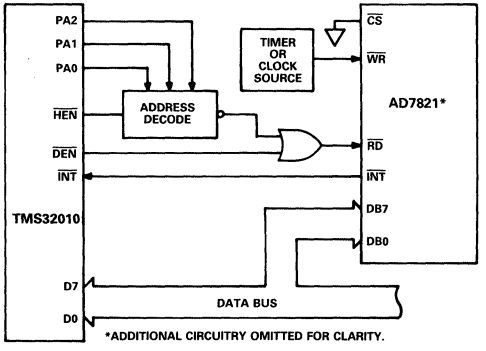


Figure 16. AD7821 to TMS32010 Interface

AD7821 – 8051 INTERFACE

Figure 17 shows the AD7821 interface to the 8051 microcomputer The AD7821 is configured in the WR-RD interface mode and is connected to the 8051 ports. The processor starts conversion and then polls $\overline{INT}$, until it goes low, before reading the conversion result. Data is read from the AD7821 by using the < MOV A, 90H > instruction (90H is the address for Port 1).

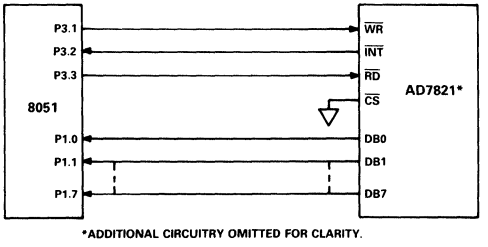
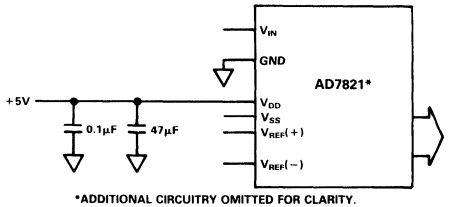


Figure 17. AD7821 to 8051 Interface

APPLYING THE AD7821

The AD7821 is specified for a unipolar input range of 0 to +5V and a bipolar input range of −2.5V to +2.5V. The $V_{REF}(-)$ and $V_{REF}(+)$ voltages required for these input ranges are outlined below. See the Typical Performance Characteristics section for operation with unspecified input voltage ranges.



*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

$V_{REF}(+)$	$V_{REF}(-)$	V_{SS}	V_{IN}	RANGE
+5V	GND	GND	UNIPOLAR	0 to +5V
+2.5V	−2.5V	−5V	BIPOLAR	−2.5V to +2.5V

Figure 18. AD7821 Unipolar/Bipolar Operation

UNIPOLAR OPERATION

Figure 18 gives the configuration and reference voltages required for 0 to +5V operation. The nominal transfer characteristic for this input range is shown in Figure 19. The output code is Natural Binary with 1LSB = (5/256) V = 19.5mV.

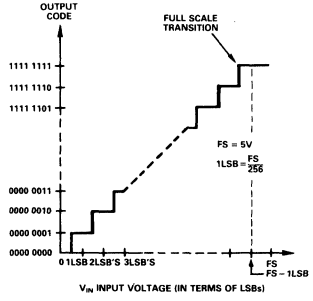


Figure 19. Nominal Transfer Characteristic for Unipolar (0 to +5V) Operation

BIPOLAR OPERATION

Figure 18 gives the configuration and reference voltages required for −2.5V to +2.5V operation. The nominal transfer characteristic for this input range is shown in Figure 20. The output code is Offset Binary with 1LSB = ([+2.5 − (−2.5)]/256)V = 19.5mV.

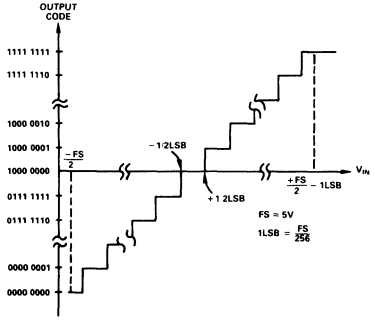


Figure 20. Nominal Transfer Characteristic for Bipolar (−2.5V to +2.5V) Operation

16-CHANNEL TELECOM A/D CONVERTER

The fast sampling rate (1MHz) and bipolar operation of the AD7821 makes it useful in Telecom applications for sampling a number of input channels using a multiplexer. Figure 21 shows a circuit for such an application.

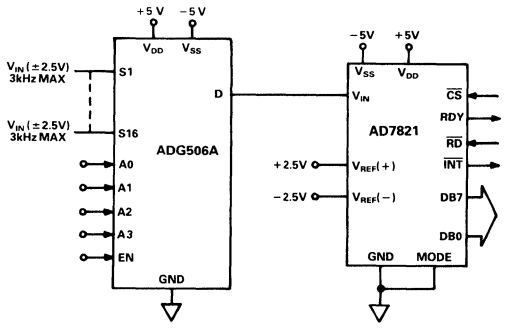


Figure 21. 16-Channel Telecom A/D Converter System

The maximum signal frequency required for acceptable quality in Telecom applications is 3kHz. The circuit given in Figure 21 permits each of the 16-input channels to be sampled at a rate of 16kHz maximum. The sampling rate takes account of such multiplexer parameters as t_{ON}, settling time etc. The circuit also eases the problem of the anti-aliasing filter design by sampling at a rate much greater than that required by the Nyquist criterion.

SIMULTANEOUS SAMPLING A/D CONVERTERS

The AD7821's inherent track-and-hold and well defined sampling instant makes it useful, in such applications as sonar, where a number of input channels are required to be sampled simultaneously. Figure 22 shows a circuit for such an application.

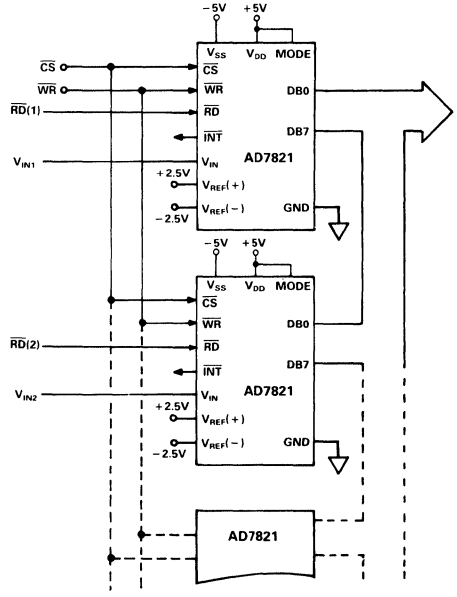


Figure 22. Simultaneous Sampling A/D Converters

The actual sampling instant which is the instant at which V_{IN} is measured, occurs approximately 50ns after the falling edge of $\overline{WR}$ or $\overline{RD}$ in the WR-RD or RD modes, respectively, due to internal logic delays. However, the internal logic delay and, therefore, the sampling instant can vary from device to device, but is typically within ± 5ns. This means that a maximum common input sine wave of ± 2.5V at 32kHz, applied to any number of AD7821s in the circuit of Figure 22, will yield a maximum difference between the converter outputs of typically ± 1/4LSB.

ANALOG DEVICES

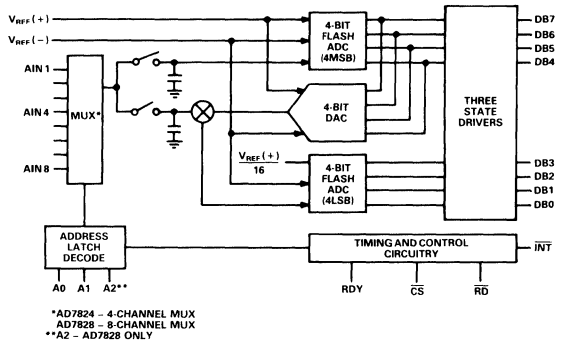
LC²MOS
High Speed 4- & 8-Channel 8-Bit ADCs

AD7824/AD7828

FEATURES

4- or 8-Analog Input Channels
Built-In Track/Hold Function
10kHz Signal Handling on Each Channel
Fast Microprocessor Interface
Single +5V Supply
Low Power: 50mW
Fast Conversion Rate, 2.5μs/Channel
Tight Error Specification: 1/2LSB

AD7824/AD7828 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7824 and AD7828 are high-speed, multichannel, 8-bit ADCs with a choice of 4 (AD7824) or 8 (AD7828) multiplexed analog inputs. A half-flash conversion technique gives a fast conversion rate of 2.5μs per channel and the parts have a built-in track/hold function capable of digitizing full-scale signals of 10kHz (157mV/μs slew rate) on all channels. The AD7824 and AD7828 operate from a single +5V supply and have an analog input range of 0 to +5V, using an external +5V reference.

Microprocessor interfacing of the parts is simple, using standard Chip Select ($\overline{CS}$) and Read ($\overline{RD}$) signals to intitiate the conversion and read the data from the three-state data outputs. The half-flash conversion technique means that there is no need to generate a clock signal for the ADC. The AD7824 and AD7828 can be interfaced easily to most popular microprocessors.

The AD7824 and AD7828 are fabricated in an advanced, all ion-implanted, Linear-Compatible CMOS process (LC²MOS) and have low power dissipation of 40mW (typ). The AD7824 is available in a 0.3" wide, 24-pin "skinny" DIP, while the AD7828 is available in a 0.6" wide, 28-pin DIP and in 28-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. 4- or 8-channel input multiplexer gives cost-effective space-saving multichannel ADC system.
2. Fast conversion rate of 2.5μs/channel features a per channel sampling frequency of 100kHz for the AD7824 or 50kHz for the AD7828.
3. Built-in track-hold function allows handling of 4- or 8-channels up to 10kHz bandwidth (157mV/μs slew rate).
4. Tight total unadjusted error spec and channel-to-channel matching eliminate the need for user trims.
5. Single +5V supply simplifies system power requirements.
6. Fast, easy-to-use digital interface allows connection to most popular microprocessors with minimal external components. No clock signal is required for the ADC.

SPECIFICATIONS (V_{DD} = +5V; $V_{REF}(+)$ = +5V; $V_{REF}(-)$ = GND = 0V unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise specified. Specifications apply for Mode 0.

Parameter	K Version[1]	L Version	B, T Versions	C, U Versions	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which No Missing Codes are guaranteed	8	8	8	8	Bits	
Channel to Channel Mismatch	±1/4	±1/4	±1/4	±1/4	LSB max	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	V min/V max	
$V_{REF}(-)$ Input Voltage Range	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	V min/V max	
ANALOG INPUT						
Input Voltage Range	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	V min/V max	
Input Leakage Current	±3	±3	±3	±3	μA max	Analog Input Any Channel
Input Capacitance[3]	45	45	45	45	pF typ	0 to +5V
LOGIC INPUTS						
$\overline{RD}$, $\overline{CS}$, A0, A1 & A2						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH}	1	1	1	1	μA max	
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7 & $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360μA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
I_{OUT} (DB0-DB7)	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
RDY						
V_{OL}[4]	0.4	0.4	0.4	0.4	V max	I_{SINK} = 2.6mA
I_{OUT}	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING[3]	0.7	0.7	0.7	0.7	V/μs typ	
	0.157	0.157	0.157	0.157	V/μs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[5]	16	16	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 2.4V
Power Dissipation	50	50	50	50	mW typ	
	80	80	100	100	mW max	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16LSB typ V_{DD} = 5V ±5%

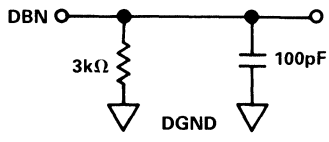
NOTES
[1]Temperature Ranges are as follows:
K, L Versions; 0 to +70°C
B, C Versions; −25°C to +85°C
T, U Versions; −55°C to +125°C
[2]Total Unadjusted Error includes offset, full-scale and linearity errors.
[3]Sample tested at 25°C by Product Assurance to ensure compliance.
[4]RDY is an open drain output.
[5]See Typical Performance Characteristics.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V; V_{REF} (+) = +5V; V_{REF} (−) = GND = 0V unless otherwise stated)

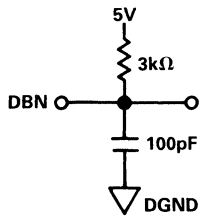
Parameter	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{AS}	0	0	0	ns min	Multiplexer Address Setup Time
t_{AH}	30	35	40	ns min	Multiplexer Address Hold Time
t_{RDY}[2]	40	60	60	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5kΩ.
t_{CRD}	2.0	2.4	2.8	μs max	Conversion Time, Mode 0
t_{ACC1}[3]	85	110	120	ns max	Data Access Time after $\overline{RD}$
t_{ACC2}[3]	50	60	70	ns max	Data Access Time after $\overline{INT}$, Mode 0
t_{INTH}[2]	40	65	70	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay
	75	100	100	ns max	
t_{DH}[4]	60	70	70	ns max	Data Hold Time
t_P	500	500	600	ns min	Delay Time between Conversions
t_{RD}	60	80	80	ns min	Read Pulse Width, Mode 1
	600	500	400	ns max	

NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits

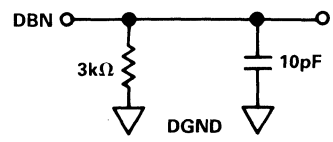


a. High-Z to V_{OH}

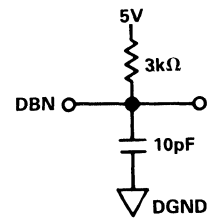


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD}	0V, +7V
Digital Input Voltage to GND ($\overline{RD}$, $\overline{CS}$, A0, A1 & A2)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to GND (DB0, DB7, RDY & $\overline{INT}$)	−0.3V, V_{DD} +0.3V
V_{REF} (+) to GND	V_{REF} (−), V_{DD} +0.3V
V_{REF} (−) to GND	0V, V_{REF} (+)
Analog Input (Any Channel)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
Commercial (K, L Versions)	0 to +70°C
Industrial (B, C Versions)	−25°C to +85°C
Extended (T, U Versions)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

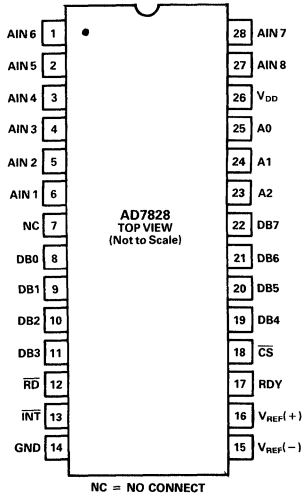
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

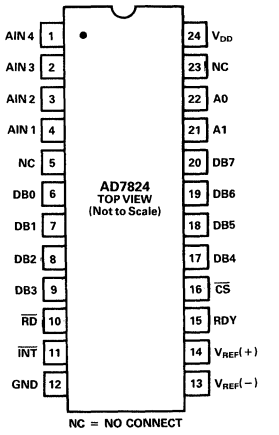
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP

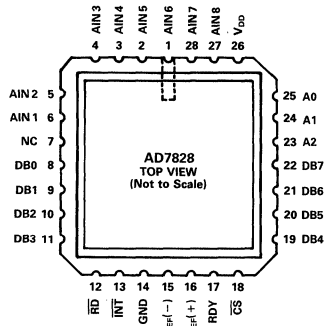


NC = NO CONNECT



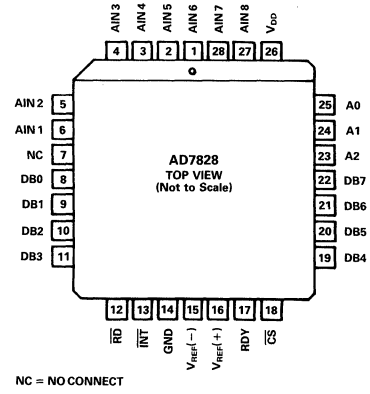
NC = NO CONNECT

LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

ORDERING INFORMATION[1, 2]

Total Unadjusted Error	Temperature Range and Package Options[3]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-28)	**Hermetic[4] (Q-28)**	**Hermetic[4] (Q-28)**
±1LSB	AD7828KN	AD7828BQ	AD7828TQ
±1/2LSB	AD7828LN	AD7828CQ	AD7828UQ
	PLCC[5] (P-28A)		**LCCC[6] (E-28A)**
±1LSB	AD7828KP		AD7828TE
±1/2LSB	AD7828LP		AD7828UE
	Plastic DIP (N-24)	**Hermetic[7] (Q-24)**	**Hermetic[7] (Q-24)**
±1LSB	AD7824KN	AD7824BQ	AD7824TQ
±1/2LSB	AD7824LN	AD7824CQ	AD7824UQ

NOTES

[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.

[2]Analog Devices reserves the right to ship either cerdip or ceramic hermetic packages.

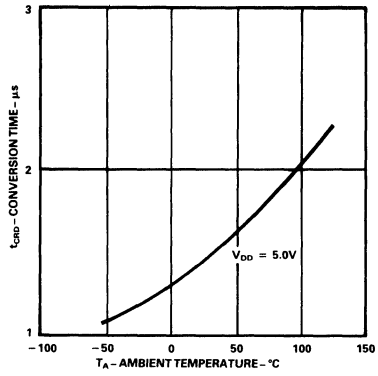
[3]See Section 14 for package outline information.

[4]Package outline cerdip (Q-28) or ceramic (D-28).

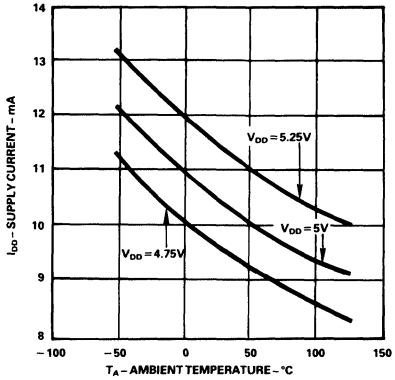
[5]PLCC: Plastic Leaded Chip Carrier.

[6]LCCC: Leadless Ceramic Chip Carrier.

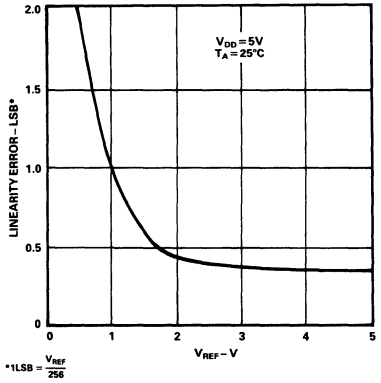
[7]Package outline cerdip (Q-24) or ceramic (D-24A).



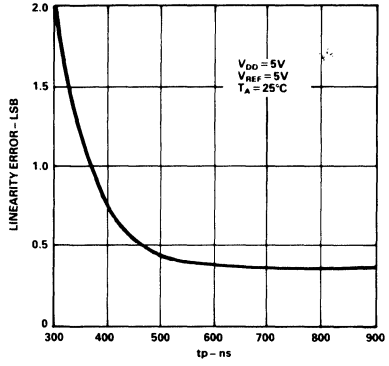
Conversion Time vs. Temperature



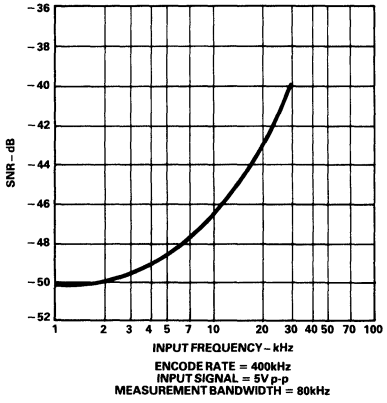
Power Supply Current vs. Temperature (not including reference ladder)



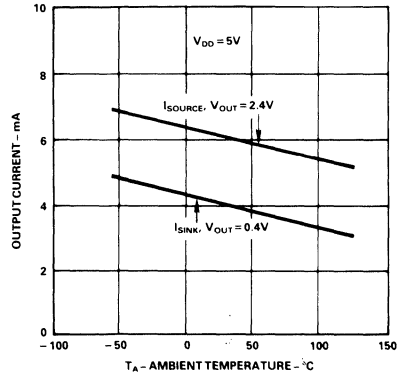
Accuracy vs. V_{REF}
[$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



Accuracy vs. tp



Signal-Noise Ratio vs. Input Frequency



Output Current vs. Temperature

OPERATIONAL DIAGRAM

The AD7824 is a 4-channel 8-bit A/D converter and the AD7828 is an 8-channel 8-bit A/D converter. Operational diagrams for both of these devices are shown in Figures 3 and 4. The addition of just a +5V reference allows the devices to perform the analog-to-digital function.

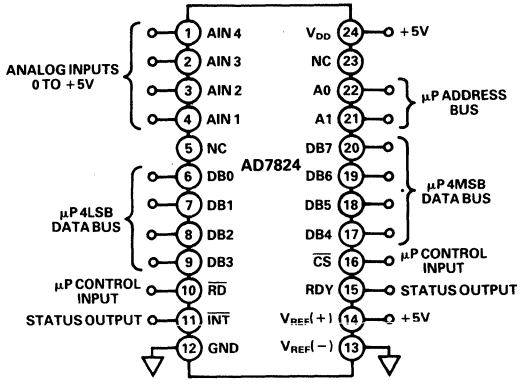


Figure 3. AD7824 Operational Diagram

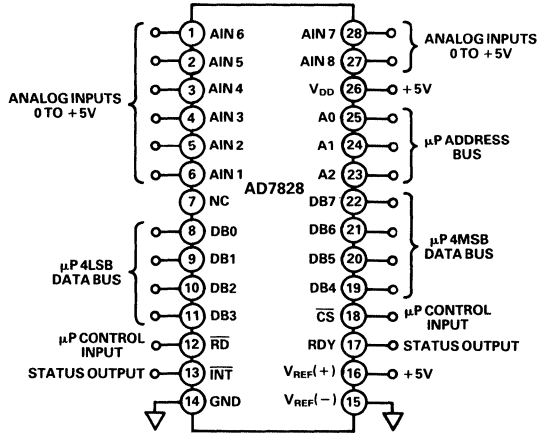


Figure 4. AD7828 Operational Diagram

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7824/AD7828 uses a half-flash conversion technique whereby two 4-bit flash A/D converters are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. For a full 8-bit reading to be realized, the upper 4-bit flash, the most significant (MS) flash, performs a conversion to provide the 4 most significant data bits. An internal DAC, driven by the 4MSBs, then recreates an analog approximation of the input voltage. This analog result is subtracted from the input, and the difference is converted by the lower flash ADC, the least significant (LS) flash, to provide the 4 least significant bits of the output data.

APPLYING THE AD7824/AD7828

REFERENCE AND INPUT

The two reference inputs on the AD7824/AD7828 are fully differential and define the zero to full-scale input range of the A/D converter. As a result, the span of the analog input voltage for all channels can easily be varied. By reducing the reference span, $V_{REF}(+) - V_{REF}(-)$, to less than 5V the sensitivity of the converter can be increased (e.g., if V_{REF} = 2V then 1LSB = 7.8mV). The input/reference arrangement also facilitates ratiometric operation.

This reference flexibility also allows the input channel voltage span to be offset from zero. The voltage at $V_{REF}(-)$ sets the input level for all channels which produces a digital output of all zeroes. Therefore, although the analog inputs are not themselves differential, they have nearly differential-input capability in most measurement applications because of the reference design. Figures 5 to 7 show some of the configurations that are possible.

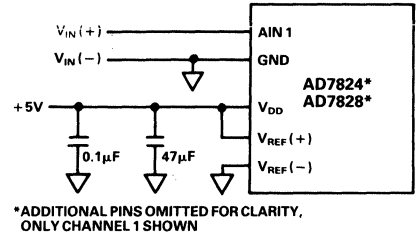


Figure 5. Power Supply as Reference

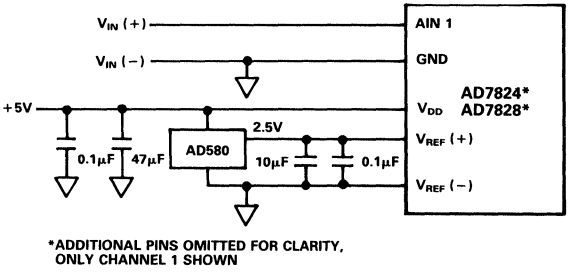


Figure 6. External Reference Using the AD580, Full-Scale Input is 2.5V

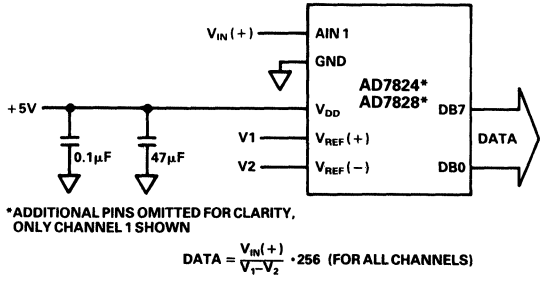


Figure 7. Input Not Referenced to GND

INPUT CURRENT

Due to the novel conversion techniques employed by the AD7824/AD7828, the analog input behaves somewhat differently than in conventional devices. The ADC's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the AD7824/AD7828 is shown in Figure 8. When a conversion starts ($\overline{CS}$ and $\overline{RD}$ going low), all input switches close, and the selected input channel is connected to the most significant and least significant comparators. Therefore, the analog input is connected to thirty-one 1pF input capacitors at the same time.

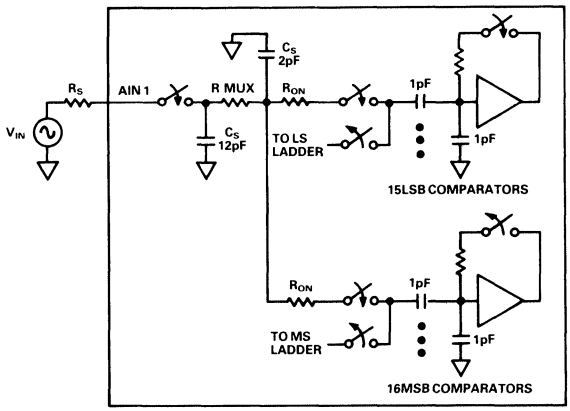


Figure 8. AD7824/AD7828 Equivalent Input Circuit

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 3k to 6k). In addition, about 14pF of input stray capacitance must be charged. The analog input for any channel can be modelled as an RC network as shown in Figure 9. As R_S increases, it takes longer for the input capacitance to charge.

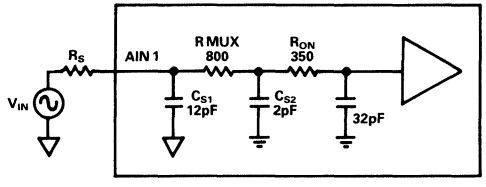


Figure 9. RC Network Model

The time for which the input comparators track the analog input is approximately 1μs at the start of conversion. Because of input transients on the analog inputs, it is recommended that a source impedence of not greater than 100 ohms be connected to the analog inputs. The output impedence of an op-amp is equal to the open loop output impedence divided by the loop gain at the frequency of interest. It is important that the amplifier driving the AD7824/AD7828 analog inputs have sufficient loop gain at the input signal frequency as to make the output impedance low.

Suitable op-amps for driving the AD7824/AD7828 are the AD544 or AD644.

INHERENT SAMPLE-HOLD

A major benefit of the AD7824's and AD7828's analog input structure is its ability to measure a variety of high-speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain stable to at least 1/2LSB throughout the conversion process if rated accuracy is to be maintained. Consequently, for many high-speed signals, this signal must be externally sampled and held stationary during the conversion. The AD7824/AD7828 input comparators, by nature of their input switching inherently accomplish this sample-and-hold function. Although the conversion time for AD7824/ AD7828 is 2μs, the time for which any selected analog input must be 1/2LSB stable is much smaller. The AD7824/AD7828 tracks the selected input channel for approximately 1μs after conversion start. The value of the analog input at that instant (1μs from conversion start) is the measured value. This value is then used in the least significant flash to generate the lower 4-bits of data.

SINUSOIDAL INPUTS

The AD7824/AD7828 can measure input signals with slew rates as high as 157mV/μs to the rated specifications. This means that the analog input frequency can be up to 10kHz without the aid of an external sample and hold. Furthermore, the AD7828 can measure eight 10kHz signals without a sample and hold. The Nyquist criterion requires that the sampling rate be twice the input frequency (i.e., 2×10kHz). This requires an ideal anti-aliasing filter with an infinite roll-off. To ease the problem of anti-aliasing filter design, the sampling rate is usually much greater than the Nyquist criterion. The maximum sampling rate (F_{max}) for the AD7824/AD7828 can be calculated as follows:

$$F_{max} = \frac{1}{t_{CRD} + t_p}$$

$$F_{max} = \frac{1}{2E-6+0.5E-6} = 400\text{kHz}$$

t_{CRD} = AD7824/AD7828 Conversion Time
t_P = Minimum Delay Between Conversion

This permits a maximum sampling rate of 50kHz for each of the 8 channels when using the AD7828 and 100kHz for each of the 4 channels when using the AD7824.

UNIPOLAR OPERATION

The analog input range for any channel of the AD7824/AD7828 is 0 to 5V as shown in the unipolar operational diagram of Figure 10. Figure 11 shows the designed code transitions which occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSB, 5/2LSB, FS-3/2LSBs). The output code is Natural Binary with 1LSB = FS/256 = (5/256)V = 19.5mV.

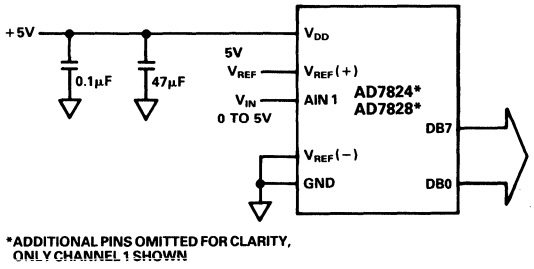


Figure 10. AD7824/AD7828 Unipolar 0 to 5V Operation

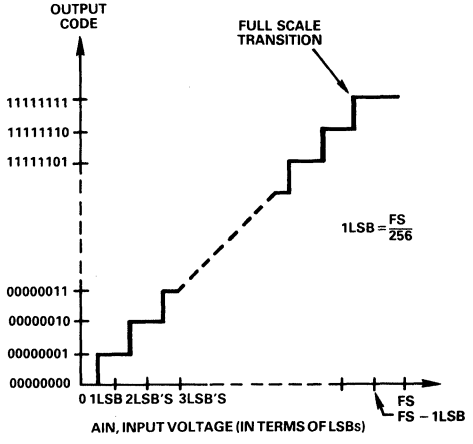


Figure 11. Ideal Input/Output Transfer Characteristic for Unipolar 0 to +5V Operation

BIPOLAR OPERATION

The circuit of Figure 12 is designed for bipolar operation. An AD544 op-amp conditions the signal input (V_{IN}) so that only positive voltages appear at AIN 1. The closed loop transfer function of the op-amp for the resistor values shown is given below:

$$AIN\ 1 = (2.5 - 0.625\ V_{IN})\ Volts$$

The analog input range is ±4V and the LSB size is 31.25mV. The output code is complementary offset binary. The ideal input/output characteristic is shown in Figure 13.

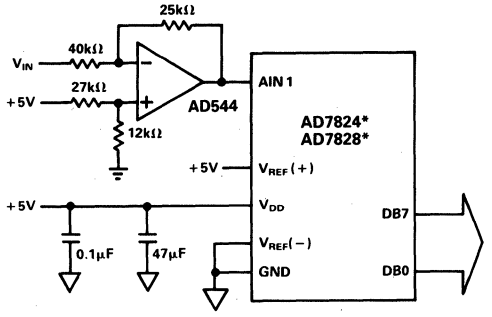


Figure 12. AD7824/AD7828 Bipolar ±4V Operation

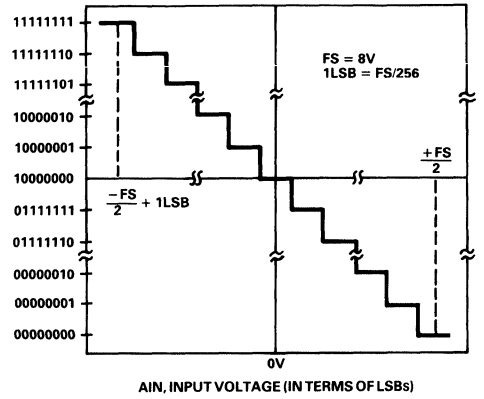


Figure 13. Ideal Input/Output Transfer Characteristic for ±4V Operation

TIMING AND CONTROL

The AD7824/AD7828 has two digital inputs for timing and control. These are Chip Select ($\overline{CS}$) and Read ($\overline{RD}$). A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which starts a conversion on the channel selected by the multiplexer address inputs (see Table I). There are two modes of operation as outlined by the timing diagrams of Figures 14 and 15. Mode 0 is designed for microprocessors which can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when conversion is complete. Mode 1 does not require microprocessor WAIT states. A READ operation initiates a conversion and reads the previous conversion results.

AD7824		AD7828			CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	AIN 1
0	1	0	0	1	AIN 2
1	0	0	1	0	AIN 3
1	1	0	1	1	AIN 4
		1	0	0	AIN 5
		1	0	1	AIN 6
		1	1	0	AIN 7
		1	1	1	AIN 8

Table I. Truth Table for Input Channel Selection

MODE 0

Figure 14 shows the timing diagram for Mode 0 operation. This mode can only be used for microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which starts a conversion. The analog multiplexer address inputs must remain valid while $\overline{CS}$ and $\overline{RD}$ are low. The data bus (DB7-DB0) remains in the three-state condition until conversion is complete. There are two converter status outputs on the AD7824/AD7828, interrupt ($\overline{INT}$) and ready (RDY) which can be used to drive the microprocessor READY/WAIT input. The RDY is an open drain output (no internal pull-up device) which goes low on the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion, when the 8-bit conversion result appears on the data outputs. If the RDY status is not required, then the external pull-up resistor can be omitted and the RDY output tied to GND. The $\overline{INT}$ goes low when conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

MODE 1

Mode 1 operation is designed for applications where the microprocessor is not forced into a WAIT state. A READ operation takes $\overline{CS}$ and $\overline{RD}$ low which triggers a conversion (see Figure 15). The multiplexer address inputs are latched on the rising edge of $\overline{RD}$. Data from the previous conversion is read from the three-state data outputs (DB7-DB0). This data may be disregarded if not required. Note, the RDY output (open drain output) does not provide any status information in this mode and must be connected to GND. At the end of conversion $\overline{INT}$ goes low. A second READ operation is required to access the new conversion result. This READ operation latches a new address into the multiplexer inputs and starts another conversion. $\overline{INT}$ returns high at the end of the second READ operation, when $\overline{CS}$ or $\overline{RD}$ returns high. A delay of 2.5μs must be allowed between READ operations.

3

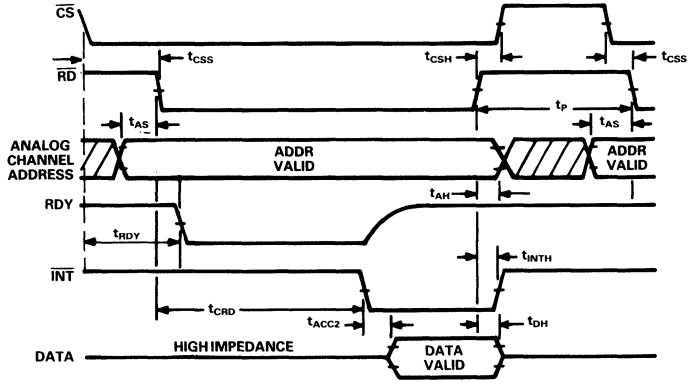


Figure 14. Mode 0 Timing Diagram

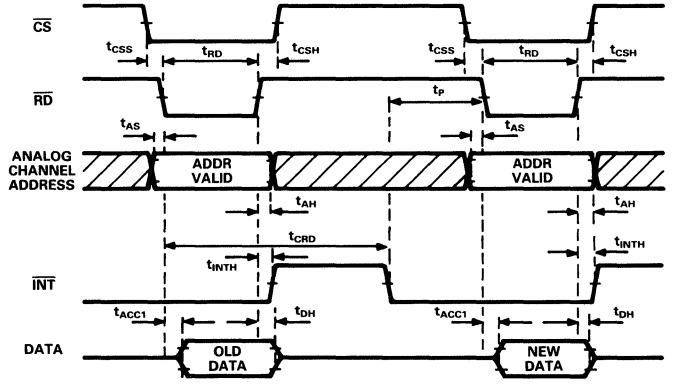


Figure 15. Mode 1 Timing Diagram

MICROPROCESSOR INTERFACING

The AD7824/AD7828 is designed to interface to microprocessors as Read Only Memory (ROM). Analog channel selection, conversion start and data read operations are controlled by $\overline{CS}$, $\overline{RD}$ and the channel address inputs. These signals are common to all memory peripheral devices.

Z80 MICROPROCESSOR

Figure 16 shows a typical AD7824/AD7828 – Z80 interface. The AD7824/AD7828 is operating in Mode 0. Assume the ADC is assigned a memory block starting at address C000. The following LOAD instruction to any of the addresses listed in Table II will start a conversion of the selected channel and read the conversion result.

LD B, (C000)

At the beginning of the instruction cycle when the ADC address is selected, RDY asserts the WAIT input, so that the Z80 is forced into a WAIT state. At the end of conversion RDY returns high and the conversion result is placed in the B register of the microprocessor.

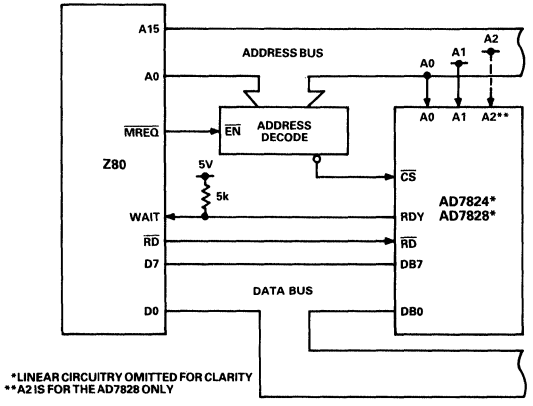


Figure 16. AD7824/AD7828 – Z80 Interface

ADDRESS	AD7824 Channel	AD7828 Channel
C000	1	1
C001	2	2
C002	3	3
C003	4	4
C004	–	5
C005	–	6
C006	–	7
C007	–	8

Table II. Address Channel Selection

MC68000 MICROPROCESSOR

Figure 17 shows a MC68000 interface. The AD7824/AD7828 is operating in Mode 0. Assume the ADC is again assigned a memory block starting at address C000. A MOVE instruction to any of the addresses in Table II starts a conversion and reads the conversion result.

MOVE•B $C000,D0

Once conversion has begun, the MC68000 inserts WAIT states, until INT goes low asserting DTACK at the end of conversion. The microprocessor then places the conversion results in the D0 register.

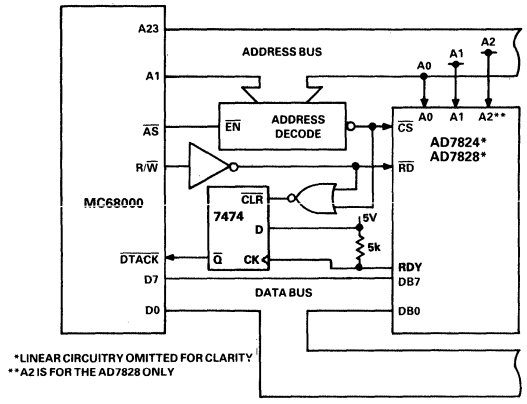


Figure 17. AD7824/AD7828 – MC68000 Interface

TMS32010 MICROCOMPUTER

A TMS32010 interface is shown in Figure 18. The AD7824/AD7828 is operating in Mode 1 (i.e., no μP WAIT states). The ADC is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into the accumulator.

IN, A PA (PA = PORT ADDRESS)

The port address (000 to 111) selects the analog channel to be converted. When conversion is complete a second I/O instruction (IN, A PA) reads the up-to-date data into the accumulator and starts another conversion. A delay of 2.5μs must be allowed between conversions.

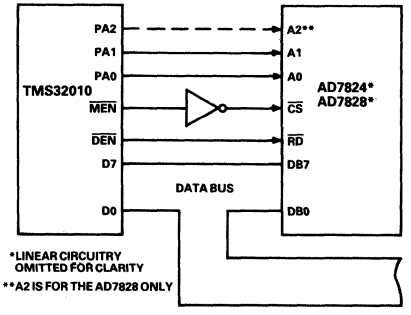


Figure 18. AD7824/AD7828 – TMS32010 Interface

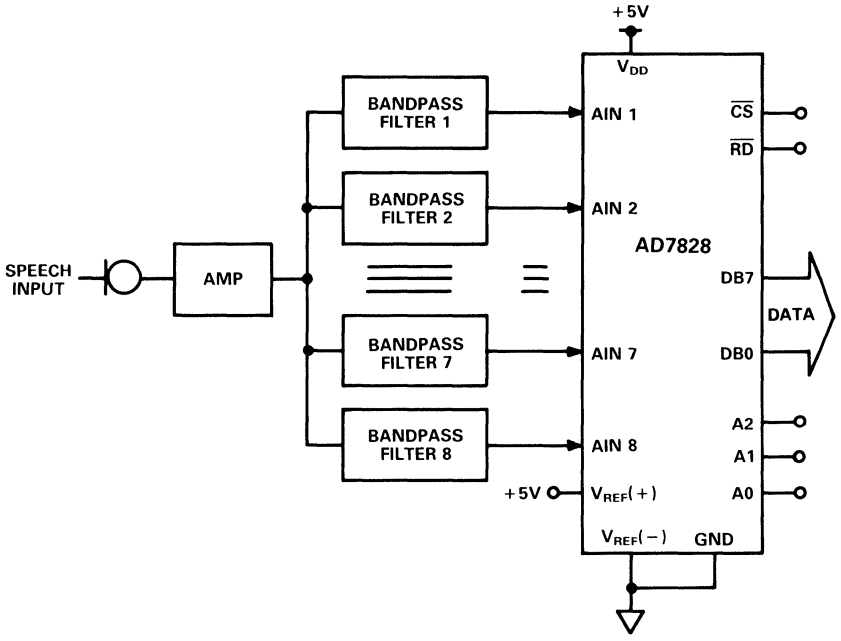


Figure 19. Speech Analysis Using Real-Time Filtering

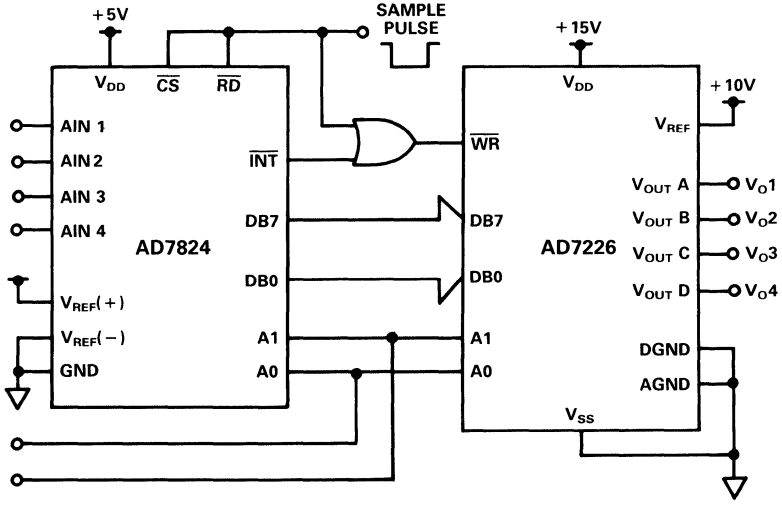


Figure 20. 4-Channel Fast Infinite Sample-and-Hold

ANALOG DEVICES

LC²MOS Complete, 12-Bit, 100kHz, Sampling ADC

AD7870

FEATURES

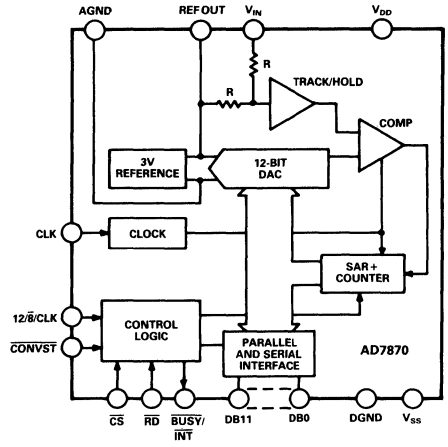
Complete Monolithic 12-Bit ADC with:
- **2μs Track/Hold Amplifier**
- **8μs A/D Converter**
- **On-Chip Reference**
- **Laser-Trimmed Clock**
- **Parallel, Byte and Serial Digital Interface**

72dB SNR at 10kHz Input Frequency
57ns Data Access Time
Low Power – 60mW typ

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

AD7870 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7870 is a fast, complete, 12-bit A/D converter. It consists of a track/hold amplifier, 8μs successive approximation ADC, 3V buried Zener reference and versatile interface logic. The ADC features a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may be overridden by an external clock if required.

The AD7870 offers a choice of three data output formats: a single, parallel, 12-bit word; two 8-bit bytes, or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7870 operates from ±5V power supplies, accepts bipolar input signals of ±3V and can convert full power signals up to 50kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7870 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7870 is fabricated in Analog Devices' linear compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete 12-bit ADC on a chip.
   The AD7870 is the most complete monolithic ADC available and combines a 12-bit ADC with internal clock, track/hold amplifier and reference on a single chip.
2. Dynamic specifications for DSP users.
   The AD7870 is fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and guaranteed over the full operating temperature range.
3. Fast microprocessor interface.
   Data access times of 57ns make the AD7870 compatible with modern 8- and 16-bit microprocessors and digital signal processors.

SPECIFICATIONS (V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V, f_{CLK} = 2.5MHz external, unless otherwise stated. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A[1]	K, B[1]	L, C[1]	S[1]	T[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]							
Signal to Noise Ratio[3] (SNR)							
@ +25°C	70	70	72	70	70	dB min	V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 100kHz
T_{min} to T_{max}	70	70	71	70	70	dB min	Typically 71.5dB for 0 < V_{IN} < 50kHz
Total Harmonic Distortion (THD)	−80	−80	−80	−80	−80	dB max	V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 100kHz Typically −86dB for 0 < V_{IN} < 50kHz
Peak Harmonic or Spurious Noise	−80	−80	−80	−80	−80	dB max	V_{IN} = 10kHz, f_{SAMPLE} = 100kHz Typically −86dB for 0 < V_{IN} < 50kHz
Intermodulation Distortion (IMD)							
Second Order Terms	−80	−80	−80	−80	−80	dB max	fa = 9kHz, fb = 9.5kHz, f_{SAMPLE} = 50kHz
Third Order Terms	−80	−80	−80	−80	−80	dB max	fa = 9kHz, fb = 9.5kHz, f_{SAMPLE} = 50kHz
Track/Hold Acquisition Time	2	2	2	2	2	µs max	
DC ACCURACY							
Resolution	12	12	12	12	12	Bits	
Minimum Resolution for which							
No Missing Codes are Guaranteed	12	12	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/4	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1/2		±1	LSB max	
Differential Nonlinearity		±1	±1		±1	LSB max	
Bipolar Zero Error	±5	±5	±5	±5	±5	LSB max	
Positive Full Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
Negative Full Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
ANALOG INPUT							
Input Voltage Range	±3	±3	±3	±3	±3	Volts	
Input Current	±500	±500	±500	±500	±500	µA max	
REFERENCE OUTPUT							
REF OUT @ +25°C	2.99	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±60	±35	±60	±35	ppm/°C max	
Reference Load Sensitivity							
(ΔREF OUT/ΔI)	±1	±1	±1	±1	±1	mV max	Reference Load Current Change (0-500µA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS							
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	2.4	V min	V_{DD} = 5V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	0.8	V max	V_{DD} = 5V ±5%
Input Current, I_{IN}	±10	±10	±10	±10	±10	µA max	V_{IN} = 0V to V_{DD}
Input Current (12/8/CLK Input Only)	±10	±10	±10	±10	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	10	10	pF max	
LOGIC OUTPUTS							
Output High Voltage, V_{OH}	4.0	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
DB11–DB0							
Floating-State Leakage Current	±10	±10	±10	±10	±10	µA max	
Floating-State Output Capacitance[5]	15	15	15	15	15	pF max	
CONVERSION TIME							
External Clock (f_{CLK} = 2.5MHz)	7.6/8	7.6/8	7.6/8	7.6/8	7.6/8	µs min/µs max	
Internal Clock	7/9	7/9	7/9	7/9	7/9	µs min/µs max	
POWER REQUIREMENTS							
V_{DD}	+5	+5	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	13	13	mA max	Typically 8mA
I_{SS}	6	6	6	6	6	mA max	Typically 4mA
Power Dissipation	95	95	95	95	95	mW max	Typically 60mW

NOTES
[1]Temperature ranges are as follows:
J, K, L Versions: 0 to +70°C
A, B, C Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C
[2]V_{IN} (pk-pk) = ±3V.
[3]SNR calculation includes distortion and noise components.
[4]Measured with respect to internal reference and includes bipolar offset error.
[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1,2] (V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V. See Figures 9, 10, 11 and 12.)

Parameter	Limit at T_{min}, T_{max} (J, K, L, A, B, C Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 1)
t_3	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 1)
t_5	70	70	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[3]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[4]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	**50**	ns max	
t_8	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	100	100	ns min	$\overline{SSTRB}$ to SCLK Falling Edge Setup Time
t_{11}[5]	370	370	ns min	SCLK Cycle Time
t_{12}[6]	135	135	ns max	SCLK to Valid Data Delay. C_L=35pF
t_{13}	100	100	ns min	SCLK Rising Edge to $\overline{SSTRB}$
t_{14}	10	10	ns min	Bus Relinquish Time after SCLK
	100	100	ns max	
t_{15}	60	60	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 2)
t_{16}	120	120	ns max	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay
t_{17}	200	200	ns min	Data Setup Time Prior to $\overline{BUSY}$
t_{18}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 2)
t_{19}	0	0	ns min	HBEN to $\overline{CS}$ Setup Time
t_{20}	0	0	ns min	HBEN to $\overline{CS}$ Hold Time

NOTES

[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.

[2]Serial timing is measured with a 4.7kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2kΩ pull-up on SCLK. The capacitance on all three outputs is 35pF.

[3]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

[4]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

[5]SCLK mark/space ratio (measured from a voltage level of 1.6V) is 40/60 to 60/40.

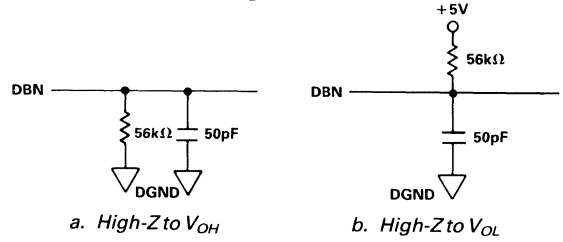
[6]SDATA will drive higher capacitive loads but this will add to t_{12} since it increases the external RC time constant ($4.7k\Omega \| C_L$) and hence the time to reach 2.4V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

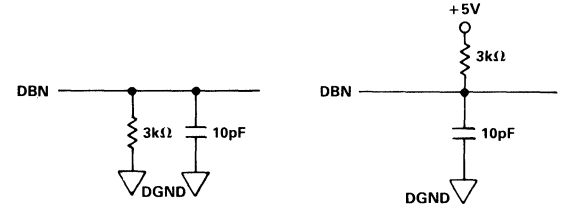
V_{DD} to AGND . . . . . −0.3V to +7V
V_{SS} to AGND . . . . . +0.3V to −7V
AGND to DGND . . . . . −0.3V to V_{DD} +0.3V
V_{IN} to AGND . . . . . −15V to +15V
REF OUT to AGND . . . . . .0V to V_{DD}
Digital Inputs to DGND . . . . . −0.3V to V_{DD} +0.3V
Digital Outputs to DGND . . . . . −0.3V to V_{DD} +0.3V
Operating Temperature Range
Commercial (J, K, L Versions) . . . . . .0 to +70°C
Industrial (A, B, C Versions) . . . . . −25°C to +85°C
Extended (S, T Versions). . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by . . . . . .10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z b. V_{OL} to High-Z

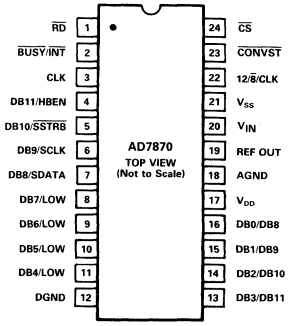
Figure 2. Load Circuits for Output Float Delay

CAUTION:

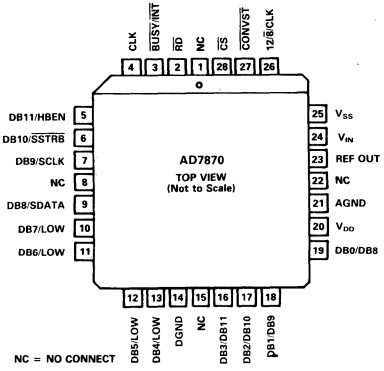
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN CONFIGURATIONS

DIP



PLCC



ORDERING INFORMATION[1]

SNR (dBs)	Relative Accuracy (LSB)	Temperature Range and Package Options[2] 0 to +70°C	−25°C to +85°C	−55°C to +125°C
		Plastic DIP (N-24)	**Hermetic DIP (Q-24)**	**Hermetic DIP (Q-24)**
70 min	±1/2 typ	AD7870JN	AD7870AQ	AD7870SQ[3]
70 min	±1 max	AD7870KN	AD7870BQ	AD7870TQ[3]
72 min	±1/2 max	AD7870LN	AD7870CQ	
		PLCC[4, 5] (P-28A)		
70 min	±1/2 typ	AD7870JP		
70 min	±1 max	AD7870KP		
72 min	±1/2 max	AD7870LP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Available to /883B processing only.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]Contact your local sales office for LCCC availability.

PIN FUNCTION DESCRIPTION

DIP Pin No.	Pin Mnemonic	Function
1	$\overline{RD}$	Read. Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.
2	$\overline{BUSY}/\overline{INT}$	Busy/Interrupt, Active low logic output indicating converter status. See timing diagrams.
3	CLK	Clock input. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed clock oscillator.
4	DB11/HBEN	Data Bit 11 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input (see below). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table I).
5	DB10/$\overline{SSTRB}$	Data Bit 10/Serial Strobe. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{SSTRB}$ is an active low open-drain output that provides a strobe or framing pulse for serial data. An external 4.7kΩ pull-up resistor is required on $\overline{SSTRB}$.
6	DB9/SCLK	Data Bit 9/Serial Clock. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If the 12/$\overline{8}$/CLK input is at −5V, then SCLK runs continuously. If 12/$\overline{8}$/CLK is at 0V, then SCLK is gated off after serial transmission is complete. SCLK is an open-drain output and requires an external 2kΩ pull-up resistor.
7	DB8/SDATA	Data Bit 8/Serial Data. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is an open-drain serial data output which is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low. An external 4.7kΩ pull-up resistor is required on SDATA.
8–11	DB7/LOW–DB4/LOW	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB7-DB4. With 12/$\overline{8}$/CLK low or −5V, their function is controlled by HBEN (see Table I).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	DB3/DB11–DB0/DB8	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With/12/$\overline{8}$/CLK high, they are always DB3-DB0. With 12/$\overline{8}$/CLK low or −5V, their function is controlled by HBEN (see Table I).

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11 (MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)

Table I. Output Data for Byte Interfacing

17	V_{DD}	Positive Supply, +5V ±5%.
18	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
19	REF OUT	Voltage Reference Output. The internal 3V reference is provided at this pin. The external load capability is 500μA.
20	V_{IN}	Analog Input. The analog input range is ±3V.
21	V_{SS}	Negative Supply, −5V ±5%.
22	12/$\overline{8}$/CLK	Three Function Input. Defines the data format and serial clock format. With this pin at +5V, the output data format is 12-bit parallel only. With this pin at 0V, either byte or serial data is available and SCLK is not continuous. With this pin at −5V, byte or serial data is again available but SCLK is now continuous.
23	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. This input is asynchronous to the CLK and independent of $\overline{CS}$ and $\overline{RD}$.
24	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.

CONVERTER DETAILS

The AD7870 is a complete 12-bit A/D converter, requiring no external components apart from power supply decoupling capacitors. It is comprised of a 12-bit successive approximation ADC based on a fast settling voltage-output DAC, a high speed comparator and SAR, a track/hold amplifier, a 3V buried Zener reference, a clock oscillator and control logic.

The conversion cycle normally consists of 19 clock periods, corresponding to a 7.6μs conversion time. The conversion time for both external and internal clock can vary from 19 to 20 clock cycles depending on the conversion start to ADC clock synchronization. If a conversion is initiated within 30ns prior to a rising edge of the ADC clock, the conversion time will consist of 20 clock cycles i.e., 8μs conversion time.

INTERNAL REFERENCE

The AD7870 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 3V ±10mV. Internally it provides both the DAC reference and the dc bias required for bipolar operation. The reference output is available (REF OUT) and is capable of providing up to 500μA to an external load.

The maximum recommended capacitance on REF OUT for normal operation is 50pF. If the reference is required for use external to the AD7870 it should be decoupled with a 200Ω resistor in series with a parallel combination of a 10μF tantalum capacitor and a 0.1μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the AD7870's internal operation.

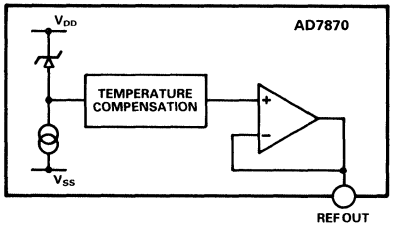


Figure 3. AD7870 Reference Circuit

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7870 allows the ADC to accurately convert an input sine wave of 6V peak-peak amplitude to 12-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate. The 0.1dB cutoff frequency occurs typically at 500kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2μs. The overall throughput rate is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.5MHz input clock the throughput rate is 10μs max.

The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion. If the $\overline{\text{CONVST}}$ input is used to start conversion then the track to hold transition occurs on the rising edge of $\overline{\text{CONVST}}$. If $\overline{\text{CS}}$ starts conversion, this transition occurs on the falling edge of $\overline{\text{CS}}$.

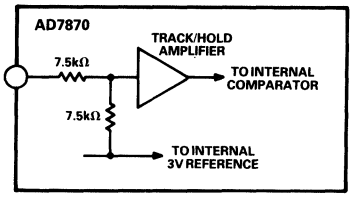


Figure 4. AD7870 Analog Input

ANALOG INPUT

Figure 4 shows the AD7870 analog input. The analog input range is ±3V into an input resistance of typically 15kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, 5/2LSBs . . . FS−3/2LSBs). The output code is 2s complement binary with 1LSB = FS/4096 = 6V/4096 = 1.46mV. The ideal input/output transfer function is shown in Figure 5.

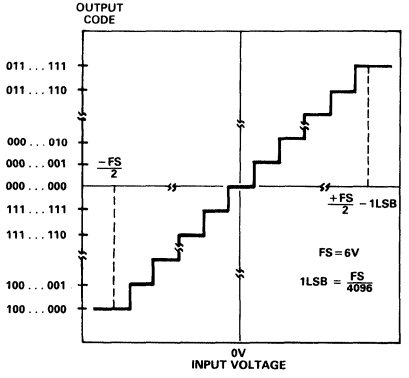


Figure 5. Bipolar Input/Output Transfer Function

BIPOLAR OFFSET AND FULL SCALE ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications will require that the input signal span the full analog input dynamic range. In such applications, offset and full-scale error will have to be adjusted to zero.

Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7870 while the input voltage is 1/2LSB below ground. The trim procedure is as follows: apply a voltage of −0.73mV(−1/2LSB) at V_1 in Figure 6 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000. Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 6).

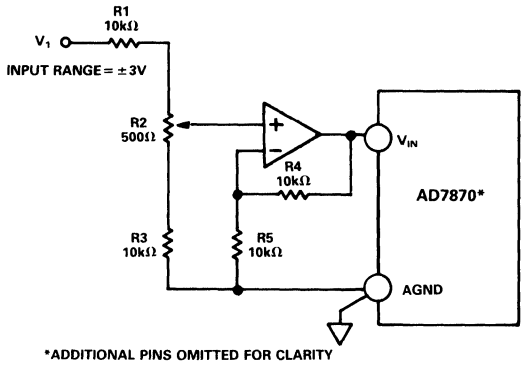


Figure 6. AD7870 Full-Scale Adjust Circuit

Positive Full-Scale Adjust
Apply a voltage of 2.9978V (FS/2 – 3/2LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust
Apply a voltage of −2.9993V (−FS/2 +1/2LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

UNIPOLAR OPERATION

A typical unipolar circuit is shown in Figure 7. The AD7870 REF OUT is used to offset the analog input by 3V. The analog input range is determined by the ratio of R3 to R4. The minimum range with which the circuit will work is 0 to +3V (R3 = 0, R4 = O/C). The resistor values are given in Figure 7 for input ranges of 0 to +5V and 0 to +10V. R5 and R6 are included for offset and full scale adjust only and should be omitted if adjustment is not required.

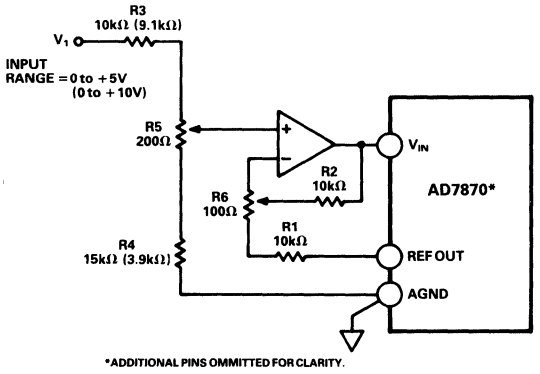


Figure 7. AD7870 Unipolar Circuit

The ideal input/output transfer function is shown in Figure 8. The output can be converted to natural binary by inverting the MSB.

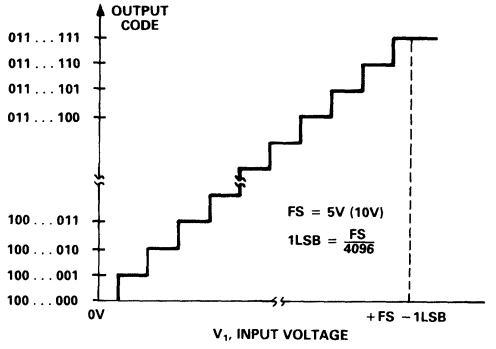


Figure 8. Unipolar Transfer Function

UNIPOLAR OFFSET AND FULL-SCALE ADJUSTMENT

When absolute accuracy is required, offset and full-scale error can be adjusted to zero. Offset must be adjusted before full scale. This is achieved by applying an input voltage of (1/2LSB) to V_1 and adjust R6 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001. For full-scale adjustment apply an input voltage of (FS−3/2LSBs) to V_1 and adjust R5 until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

TIMING AND CONTROL

The AD7870 is capable of two basic operating modes. In the first mode (Mode 1), the $\overline{\text{CONVST}}$ line is used to start conversion and drive the track/hold into its hold mode. At the end of conversion the track/hold returns to its tracking mode. It is intended principally for digital signal processing and other applications where precise sampling in time is required. In these applications, it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. For these cases, the $\overline{\text{CONVST}}$ line is driven by a timer or some precise clock source.

The second mode is achieved by hard-wiring the $\overline{\text{CONVST}}$ line low. This mode (Mode 2) is intended for use in systems where the microprocessor has total control of the ADC, both initiating the conversion and reading the data. $\overline{\text{CS}}$ starts conversion and the microprocessor will normally be driven into a WAIT state for the duration of conversion by $\overline{\text{BUSY/INT}}$.

DATA OUTPUT FORMATS

In addition to the two operating modes, the AD7870 also offers a choice of three data output formats, one serial and two parallel. The parallel data formats are a single, 12-bit parallel word for 16-bit data buses and a two-byte format for 8-bit data buses. The data format is controlled by the 12/$\overline{8}$ /CLK input. A logic high on this pin selects the 12-bit parallel output format only. A logic low or −5V applied to this pin allows the user access to either serial or byte formatted data. Three of the pins previously assigned to the four MSBs in parallel form are now used for serial communications while the fourth pin becomes a control input for the byte-formatted data. The three possible data output formats can be selected in either of the modes of operation.

Parallel Output Format

The two parallel formats available on the AD7870 are a 12-bit wide data word and a two-byte data word. In the first, all 12 bits of data are available at the same time on DB11 (MSB) through DB0 (LSB). In the second, two reads are required to access the data. When this data format is selected, the DB11/HBEN pin assumes the HBEN function. HBEN selects which byte of data is to be read from the AD7870. When HBEN is low, the lower 8 bits of data are placed on the data bus during a read operation; with HBEN high, the upper 4 bits of the 12-bit word are placed on the data bus. These 4 bits are right justified and thereby occupy the lower nibble of data while the upper nibble contains four zeros.

Serial Output Format

Serial data is available on the AD7870 when the 12/$\overline{8}$/CLK input is at 0V or −5V and in this case the DB10/$\overline{\text{SSTRB}}$, DB9/SCLK and DB8/SDATA pins assume their serial functions. Serial data is available during conversion with a word length of 16 bits; four leading zeros, followed by the 12-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (SCLK) and is framed by the serial strobe ($\overline{\text{SSTRB}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{SSTRB}}$ output is low. $\overline{\text{SSTRB}}$ goes low within three clock cycles after $\overline{\text{CONVST}}$, and the first serial data bit (which is the first leading zero) is valid on the first falling edge of SCLK. All three serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC clock source which may be internal or external. Normally, SCLK is required during the serial transmission only. In these cases, it can be shut down at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a serial clock which runs continuously. Both options are available on the AD7870 using the 12/$\overline{8}$/CLK input. With this input at −5V, the serial clock (SCLK) runs continuously; when 12/$\overline{8}$/CLK is at 0V, SCLK is turned off at the end of transmission.

MODE 1 INTERFACE

Conversion is initiated by a low going pulse on the $\overline{\text{CONVST}}$ input. The rising edge of this $\overline{\text{CONVST}}$ pulse starts conversion and drives the track/hold amplifier into its hold mode. The $\overline{\text{BUSY}}$/$\overline{\text{INT}}$ status output assumes its $\overline{\text{INT}}$ function in this mode. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. This $\overline{\text{INT}}$ line can be used to interrupt the microprocessor. A read operation to the AD7870 accesses the data and the $\overline{\text{INT}}$ line is reset high on the falling edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$. The $\overline{\text{CONVST}}$ input must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low for the AD7870 to operate correctly in this mode. Trying to read parallel data during a conversion can cause errors to the conversion in progress. In applications where precise sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from a microprocessor $\overline{\text{WR}}$ line OR-gated with a decoded address.

Figure 9 shows the Mode 1 timing diagram for a 12-bit parallel data output format (12/$\overline{8}$/CLK = +5V). A read to the AD7870 at the end of conversion accesses all 12 bits of data at the same time. Serial data is not available for this data output format.

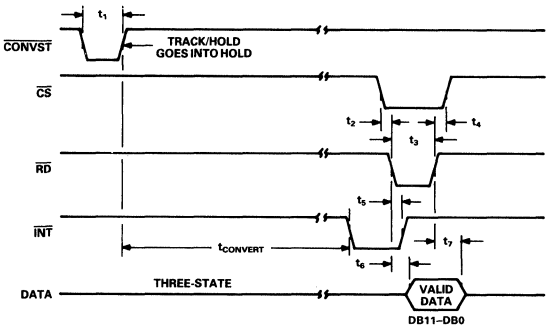
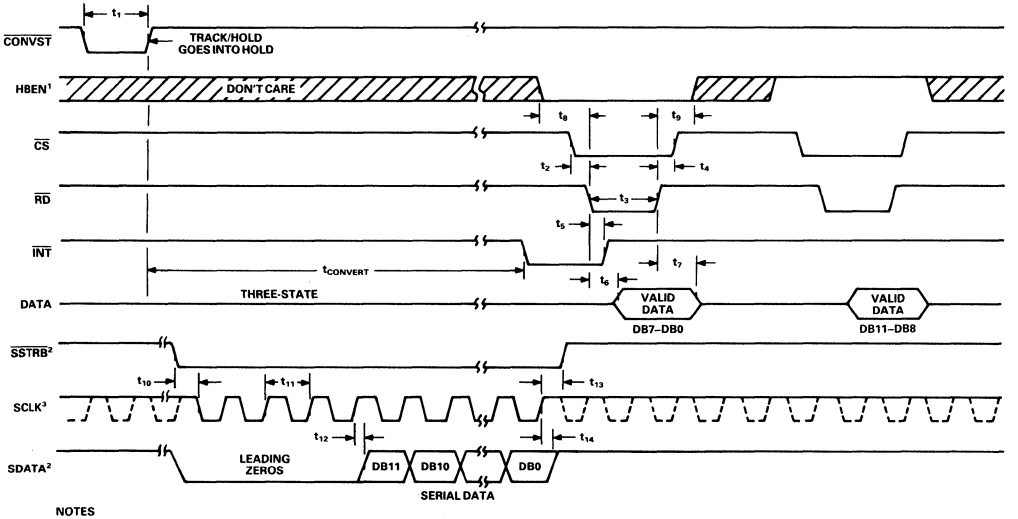


Figure 9. Mode 1 Timing Diagram, 12-Bit Parallel Read



NOTES
[1]TIMES t_2, t_3, t_4, t_8, and t_9 ARE THE SAME FOR A HIGH BYTE READ AS FOR A LOW BYTE READ.
[2]EXTERNAL 4.7kΩ PULL-UP RESISTOR.
[3]EXTERNAL 2kΩ PULL-UP RESISTOR
CONTINUOUS SCLK (DASHED LINE) WHEN 12/$\overline{8}$/CLK = −5V
NONCONTINUOUS WHEN 12/$\overline{8}$/CLK=0V.

Figure 10. Mode 1 Timing Diagram, Byte or Serial Read

The Mode 1 timing diagram for byte and serial data is shown in Figure 10. $\overline{INT}$ goes low at the end of conversion and is reset high by the first falling edge of $\overline{CS}$ and $\overline{RD}$. This first read at the end of conversion can either access the low byte or high byte of data depending on the status of HBEN (Figure 10 shows low byte only for example). The diagram shows both a noncontinuously and a continuously running clock (dashed line).

MODE 2 INTERFACE

The second interface mode is achieved by hard wiring $\overline{CONVST}$ low and conversion is initiated by taking $\overline{CS}$ low while HBEN is low. The track/hold amplifier goes into the hold mode on the falling edge of $\overline{CS}$. In this mode, the $\overline{BUSY}/\overline{INT}$ pin assumes its $\overline{BUSY}$ function. $\overline{BUSY}$ goes low at the start of conversion, stays low during the conversion and returns high when the conversion is complete. It is normally used in parallel interfaces to drive the microprocessor into a WAIT state for the duration of conversion.

Figure 11 shows the Mode 2 timing diagram for the 12-bit parallel data output format (12/$\overline{8}$/CLK = +5V). In this case, the ADC behaves like slow memory. The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then read data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid reading during conversion.

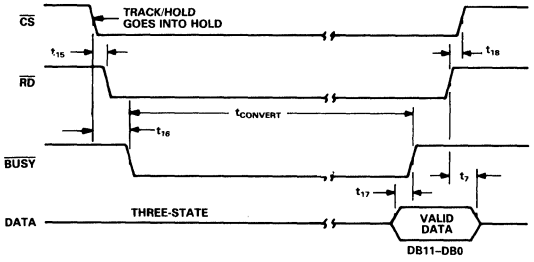


Figure 11. Mode 2 Timing Diagram, 12-Bit Parallel Read

The Mode 2 timing diagram for byte and serial data is shown in Figure 12. For two-byte data read, the lower byte (DB0–DB7) has to be accessed first since HBEN must be low to start conversion. The ADC behaves like slow memory for this first read, but the second read to access the upper byte of data is a normal read. Operation of the serial functions is identical between Mode 1 and Mode 2. The timing diagram of Figure 12 shows both a noncontinuously and a continuously running SCLK (dashed line).

AD7870 DYNAMIC SPECIFICATIONS

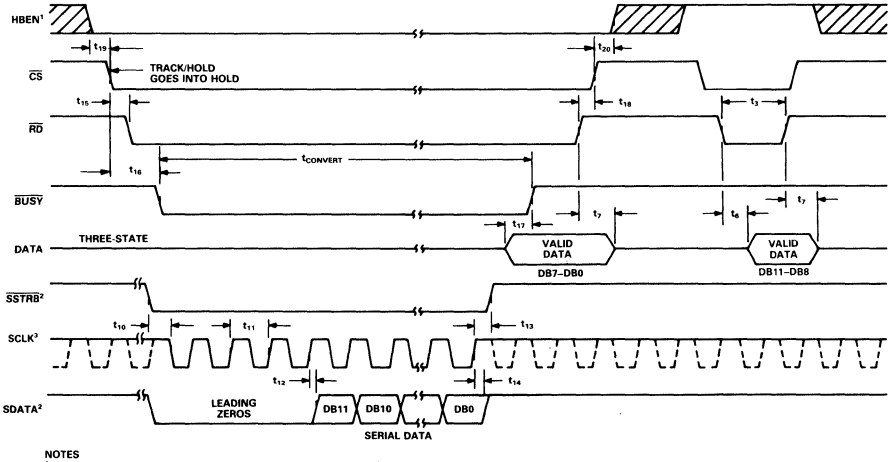
The AD7870 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7870 is specified include SNR, harmonic dsistortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74dB.



NOTES
1TIMES t_{19}, t_{18}, and t_{20} ARE THE SAME FOR A HIGH BYTE READ AS FOR A LOW BYTE READ.
2EXTERNAL 4.7kΩ PULL-UP RESISTOR.
3EXTERNAL 2kΩ PULL-UP RESISTOR
CONTINUOUS SCLK (DASHED LINE) WHEN 12/$\overline{8}$/CLK = –5V
NONCONTINUOUS WHEN 12/8/CLK = 0V.

Figure 12. Mode 2 Timing Diagram, Byte or Serial Read

The output spectrum from the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input which is sampled at a 100kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 13 shows a typical 2048 point FFT plot of the AD7870KN with an input signal of 25kHz and a sampling frequency of 100kHz. The SNR obtained from this graph is 72.6dB. It should be noted that the harmonics are taken into account when calculating the SNR.

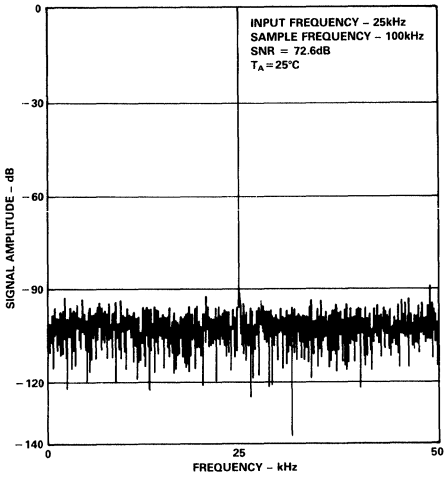


Figure 13. AD7870 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \qquad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 14 shows a typical plot of effective number of bits versus frequency for an AD7870KN with a sampling frequency of 100kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 and 73.1dB.

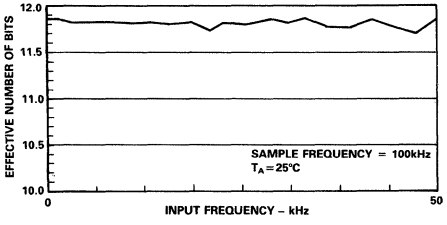


Figure 14. Effective Number of Bits vs. Frequency

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7870, total harmonic distortion (THD) is defined as

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa± nfb where m,n = 0,1,2,3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa - fb) while the third order terms include (2fa + fb), (2fa - fb), (fa + 2fb) and (fa - 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 15 shows a typical IMD plot for the AD7870.

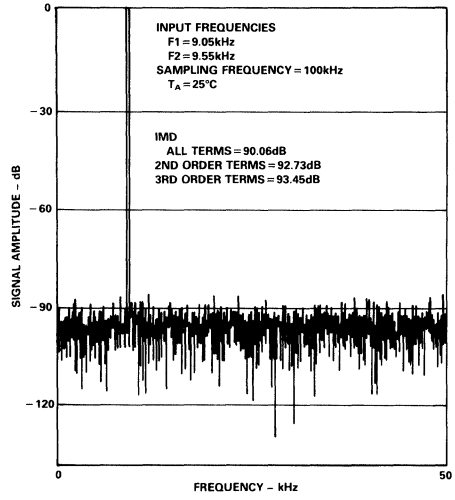


Figure 15. AD7870 IMD Plot

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be

determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

AC Linearity Plot

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7870 and several million samples are taken, a histogram showing the frequency of occurrence of each of the 4096 ADC codes can be generated. From this histogram data it is possible to generate an ac integral linearity plot as shown in Figure 16. This shows very good integral linearity performance from the AD7870 at an input frequency of 25kHz. The absence of large spikes in the plot shows good differential linearity. Simplified versions of the formulae used are outlined below.

$$INL(i) = \left[\frac{V(i) - V(o)}{V(fs) - V(o)} \cdot 4096\right] - i$$

where INL(i) is the integral linearity at code i. V(fs) and V(o) are the estimated full scale and offset transitions and V(i) is the estimated transition for the i^{th} code.

V(i) the estimated code transition point is derived as follows:

$$V(i) = -A \cdot Cos\frac{[\pi \cdot cum(i)]}{N}$$

where A is the peak signal amplitude,

N is the number of histogram samples

and cum(i) = $\Sigma_{n=0}^{i} V(n)$ occurrences

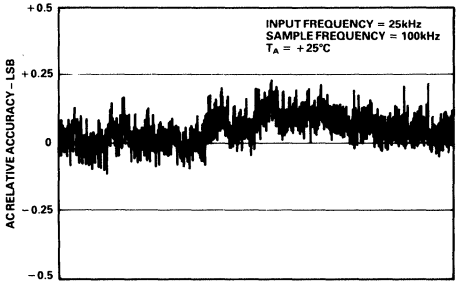


Figure 16. AD7870 ac INL Plot

MICROPROCESSOR INTERFACE

The AD7870 has a wide variety of interfacing options. It offers two operating modes and three data-output formats. Fast data access times allow direct interfacing to most microprocessors including the DSP processors.

Parallel Read Interfacing

Figures 17 to 19 show interfaces to the ADSP-2100, TMS32010 and the TMS32020 DSP processors. The AD7870 is operating in Mode 1, parallel read for all three interfaces. An external timer controls conversion start asynchronously to the microprocessor. At the end of each conversion the ADC $\overline{BUSY/INT}$ interrupts the microprocessor. The conversion result is read from the ADC with the following instruction:

ADSP-2100: MR0 = DM(ADC)

TMS32010: IN D,ADC

TMS32020: IN D,ADC

MR0 = ADSP-2100 MR0 Register

D = Data Memory Address

ADC = AD7870 Address

Some applications may require that conversions be initiated by the microprocessor rather than an external timer. One option is to decode the AD7870 $\overline{CONVST}$ from the address bus so that a write operation to the ADC starts a conversion. Data is read at the end of conversion as described earlier. Note, a read operation must not be attempted during conversion.

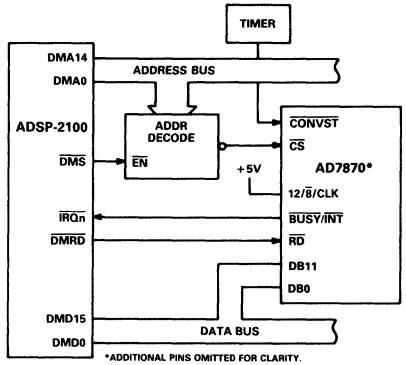


Figure 17. AD7870-ADSP-2100 Parallel Interface

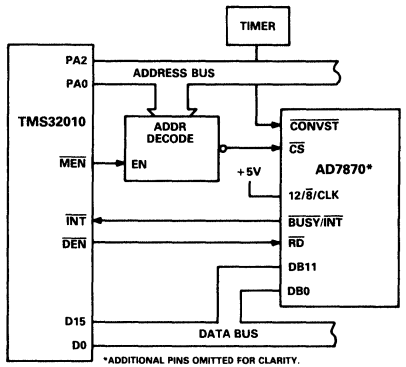


Figure 18. AD7870-TMS32010 Interface

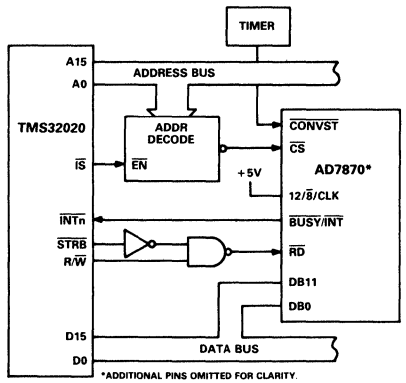


Figure 19. AD7870-TMS32020 Interface

Two Byte Read Interfacing

AD7870-68008 Interface

Figure 20 shows an 8-bit bus interface for the MC68008 microprocessor. For this interface, the AD7870 12/$\overline{8}$/CLK input is tied to 0V and DB11/HBEN pin is driven from the microprocessor least significant address bit. Conversion start control is provided by the microprocessor. In this interface example, a Move

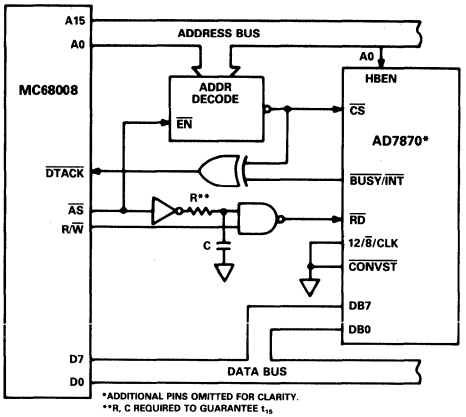


Figure 20. AD7870-MC68008 Byte Interface

instruction from the ADC address both starts a conversion and reads the conversion result.

MOVEW ADC,DO

ADC = AD7870 address

D0 = 68008 D0 register

This is a two byte read instruction. During the first read operation, $\overline{BUSY}$ in conjunction with $\overline{CS}$ forces the microprocessor to WAIT for the AD7870 conversion. At the end of conversion the ADC low byte (DB7–DB0) is loaded into D15–D8 of the D0 register and the ADC high byte (DB15–DB7) is loaded into D7–D0 of the D0 register. The following Rotate instruction to the D0 register swops the high and low bytes to the correct format.

R0L = 8, D0.

Note, while executing the two byte read instruction above, WAIT states are inserted during the first read operation only and not for the second.

Serial Interfacing

Figures 21 to 24 show the AD7870 configured for serial interfacing. In all four interfaces, the AD7870 is configured for Mode 1 operation. The interfaces show a timer driving the $\overline{CONVST}$ input, but this could be generated from a decoded address if required.

AD7870 - DSP56000 Serial Interface

Figure 21 shows a serial interface between the AD7870 and the DSP56000. The interface arrangement is two-wire with the AD7870 configured for noncontinuous clock operation (12/$\overline{8}$/CLK = 0V). The DSP56000 is configured for normal mode synchronous operation with gated clock. It is also set up for a 16-bit word with SCK and SC2 as inputs and the FSL control bit set to a 0. In this configuration, the DSP56000 assumes valid data on the first falling edge of SCK. Since the AD7870 provides valid data on this first edge, there is no need for a strobe or framing pulse for the data. SCLK and SDATA are gated off when the AD7870 is not performing a conversion. During conversion, data is valid on the SDATA output of the AD7870 and is clocked into the receive data shift register of the DSP56000. When this register has received 16 bits of data, it generates an internal interrupt on the DSP56000 to read the data from the register.

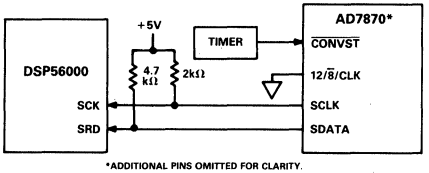


Figure 21. AD7870–DSP56000 Serial Interface

The DSP56000 and AD7870 can also be configured for continuous clock operation (12/$\overline{8}$/CLK = −5V). In this case, a strobe pulse is required by the DSP56000 to indicate when data is valid. The $\overline{SSTRB}$ output of the AD7870 is inverted and applied to the SC2 input of the DSP56000 to provide this strobe pulse. All other conditions and connections are the same as for gated clock operation.

AD7870-NEC7720/77230 Serial Interface

A serial interface between the AD7870 and the NEC7720 is shown in Figure 22. In the interface shown, the AD7870 is configured for continuous clock operation. This can be changed to a noncontinuous clock by simply tying the 12/$\overline{8}$/CLK input of the AD7870 to 0V with all other connections remaining the same. The NEC7720 expects valid data on the rising edge of its SCK input and therefore an inverter is required on the SCLK output of the AD7870. The NEC7720 is configured for a 16-bit data word. Once the 16 bits of data have been received by the SI register of the NEC7720, an internal interrupt is generated to read the contents of the SI register.

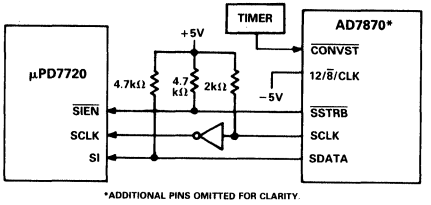


Figure 22. AD7870-NEC7720 Serial Interface

The NEC77230 interface is similar to that just outlined for the NEC7720. However, the clock input of the NEC77230 is SICLK. Additionally, no inverter is required between the AD7870 SCLK output and this SICLK input since the NEC77230 assumes data is valid on the falling edge of SICLK.

AD7870-TMS32020 Serial Interface

Figure 23 shows a serial interface between the AD7870 and the TMS32020. The AD7870 is configured for continuous clock operation. Note, the AD7870 will not interface correctly to the TMS32020 if the AD7870 is configured for a noncontinuous clock. Data is clocked into the data receive register (DRR) of the TMS32020 during conversion. As with the previous interfaces, when a 16-bit word is received by the TMS32020 it generates an internal interrupt to read the data from the DRR.

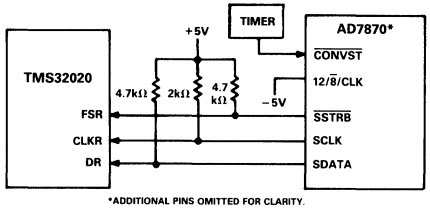


Figure 23. AD7870-TMS32020 Serial Interface

AD7870-ADSP-2101/ADSP-2102 Serial Interface

Figure 24 shows a serial interface between the AD7870 and the ADSP-2101/ADSP-2102. The AD7870 is configured for continuous clock operation. Data is clocked into the serial port register of the ADSP-2101/ADSP-2102 during conversion. As with the previous interfaces, when a 16-bit data word is received by the ADSP-2101/ADSP-2102 an internal microprocessor interrupt is generated and the data is read from the serial port register.

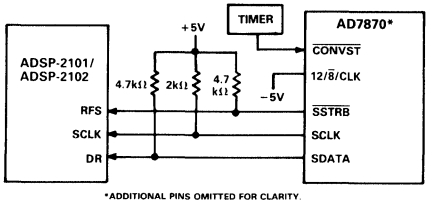


Figure 24. AD7870–ADSP–2101/ADSP–2102 Serial Interface

STAND-ALONE OPERATION

The AD7870 can be used in its Mode 2, parallel interface mode for stand-alone operation. In this case, conversion is inititated with a pulse to the AD7870 $\overline{CS}$ input. This pulse must be longer than the conversion time of the ADC. The $\overline{BUSY}$ output is used to drive the $\overline{RD}$ input. Data is latched from the AD7870 DB0–DB11 outputs to an external latch on the rising edge of $\overline{BUSY}$.

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high speed A/D performance. The AD7870 is required to make bit decisions on an LSB size of 1.465mV. Thus, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7870 AGND pin or as close as possible to the AD7870. Connect all other grounds and the AD7870 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 29 and 30 have both analog and digital ground planes which are kept separated and only joined together at the AD7870 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

DATA ACQUISITION BOARD

Figure 27 shows the AD7870 in a data acquisition circuit. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 28 to 30. The board layout has three interface ports: one serial and two parallel. One of the parallel ports is directly compatible with the ADSP-2100 evaluation board expansion connector.

The only additional component required for a full data acquisition system is an antialiasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other input conditioning circuitry. To facilitate this option there is a shorting plug (labelled LK1 on the PCB) on the analog input track. If this shorting plug is used, the analog input connects to the buffer amplifier driving the AD7870; if this shorting plug is omitted, a wire link can be used to connect the analog input to the PCB component grid.

INTERFACE CONNECTIONS

There are two parallel connectors labeled SKT4 and SKT6 and one serial connector labeled SKT5. A shorting plug option (LK3 in Figure 27) on the AD7870 12/$\overline{8}$/CLK input configures the ADC for the appropriate interface (see Pin Function Description).

SKT6 is a 96-contact (3-ROW) Eurocard connector which is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded chip enable outputs labeled $\overline{ECE1}$ to $\overline{ECE8}$. $\overline{ECE6}$ is used to drive the AD7870 $\overline{CS}$ input on the data acquisition board. To avoid selecting on board RAM sockets at the same time, LK6 on the ADSP-2100 board must be removed. In addition, the ADSP-2100 expansion connector has four interrupts labelled $\overline{EIRQ0}$ to $\overline{EIRQ3}$. The AD7870 $\overline{BUSY/INT}$ output connects to $\overline{EIRQ0}$. There is a single wait state generator connected to EDMACK to allow the AD7870 to interface to the faster versions of the ADSP-2100.

SKT4 is a 26-way (2-ROW) IDC connector. This connector contains all the signal contacts as SKT6 with the exception of EDMACK which is connected to SKT6 only. It also contains

decoded R/$\overline{W}$ and $\overline{STRB}$ inputs which are necessary for TMS32020 interfacing. The SKT4 pinout is shown in Figure 25.

SKT5 is a 9 way D-type connector which is meant for serial interfacing only. An inverted DB9/SCLK output is also provided on this connector for systems which accept data on a rising clock edge. The SKT5 pinout is shown in Figure 26.

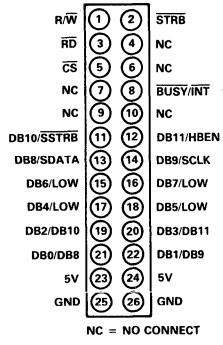


Figure 25. SKT4, IDC Connector Pinout

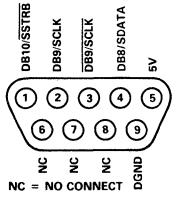


Figure 26. SKT5, D-Type Connector Pinout

SKT1, SKT2 and SKT3 are three BNC connectors which provide input connections for the analog input, the $\overline{CONVST}$ input and an external clock input. The use of an external clock source is optional, there is a shorting plug (LK2) on the AD7870 CLK input which must be connected to either −5V (for the ADCs own internal clock) or to SKT3.

POWER SUPPLY CONNECTIONS

The PCB requires two analog power supplies and one 5V digital supply . The analog supplies are labelled V+ and V−, and the range for both supplies is 12V to 15V (see silkscreen in Figure 28). Connection to the 5V digital supply is made through any of the connectors (SKT4 to SKT6). The −5V supply required by the AD7870 is generated from a voltage regulator on the V− power supply input (IC3 in Figure 26).

SHORTING PLUG OPTIONS

There are seven shorting plug options which must be set before using the board. These are outlined below:

LK1 Connects the analog input to a buffer amplifier. The analog input may also be connected to a component grid for signal conditioning.

LK2 Selects either the AD7870 internal clock or an external clock source.

LK3 Configures the AD7870 12/$\overline{8}$/CLK input for the appropriate serial or parallel interface.

LK4 Connects the AD7870 $\overline{RD}$ input directly to the two parallel connectors or to a decoded $\overline{STRB}$ and R/$\overline{W}$ input. This shorting plug setting depends on the microprocessor e.g., the TMS32010 has a separate $\overline{RD}$ output while the TMS32020 has $\overline{STRB}$ and R/$\overline{W}$ outputs.

LK5–LK7 Connect the pull-up resistors R3, R4 and R5 to $\overline{SSTRB}$, SCLK and SDATA. These shorting plugs should be removed for parallel interfacing.

COMPONENT LIST

IC1	AD711 Op Amp
IC2	AD7870 Analog-to-Digital Converter
IC3	MC79L05 −5V Regulator
IC4	74HC00 Quad NAND Gate
IC5	74HC74 Dual D-Type Flip Flop
C1, C3, C5, C7, C9, C11	10μF Capacitors
C2, C4, C6, C8, C10, C12	0.1μF Capacitors
R1, R2	10kΩ Pull-Up Resistors
R3*, R5*	4.7kΩ Pull-Up Resistors
R4*	2kΩ Pull-Up Resistor
LK1, LK2 LK3, LK4 LK5, LK6, LK7	Shorting Plugs
SKT1, SKT2, SKT3	BNC Sockets
SKT4	26-Contact (2-Row) IDC Connector
SKT5	9-Contact D-Type Connector
SKT6	96-Contact (3-Row) Eurocard Connector

*Required for Serial Communication only.

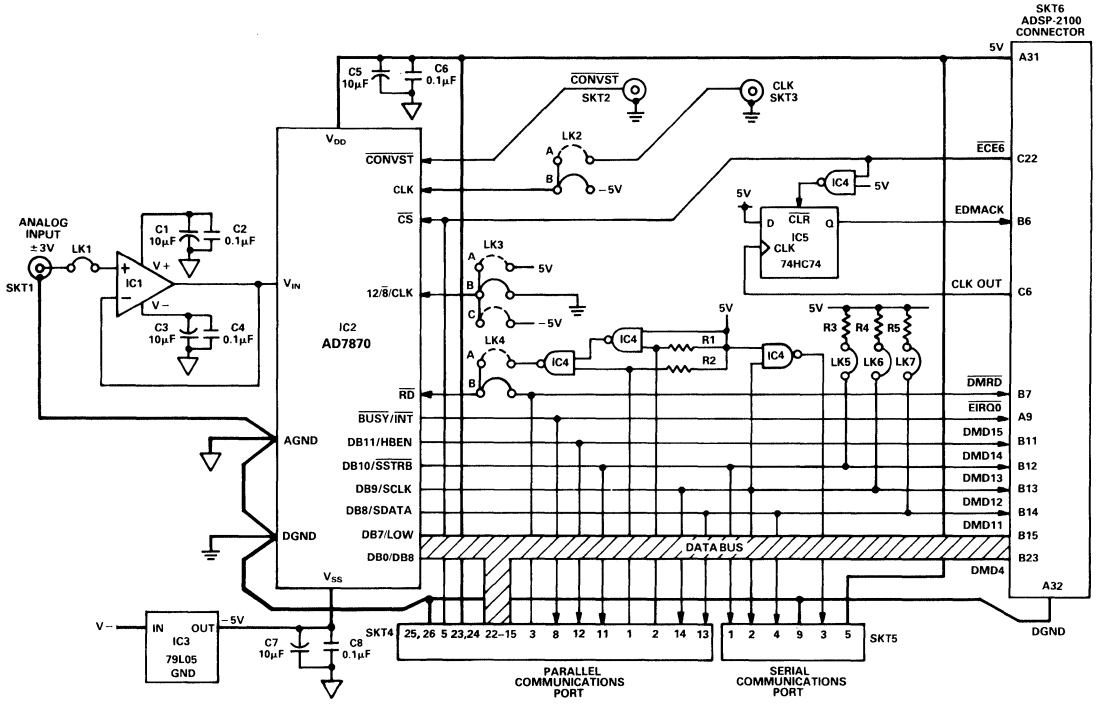


Figure 27. Data Acquisition Circuit Using the AD7870

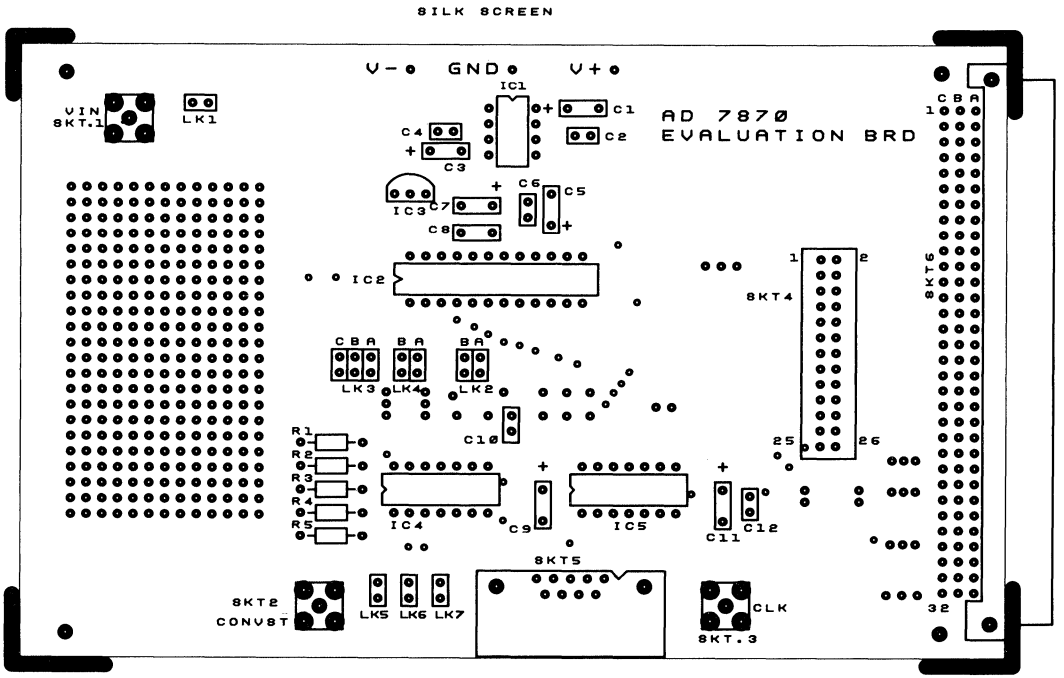


Figure 28. PCB Silkscreen for Figure 27

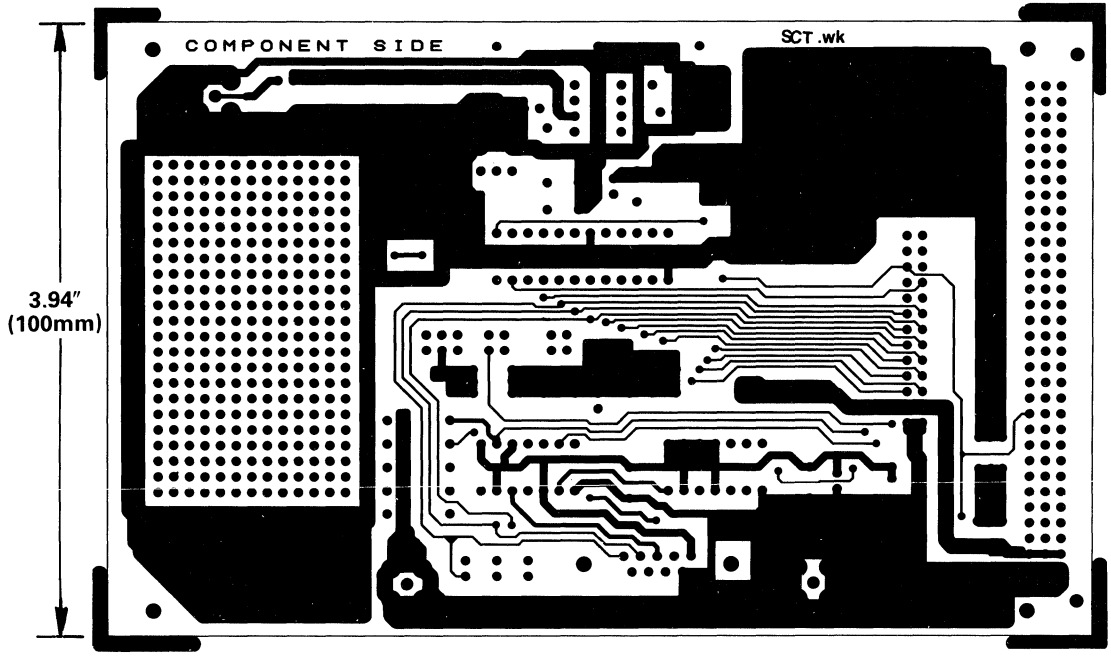


Figure 29. PCB Component Side Layout for Figure 27

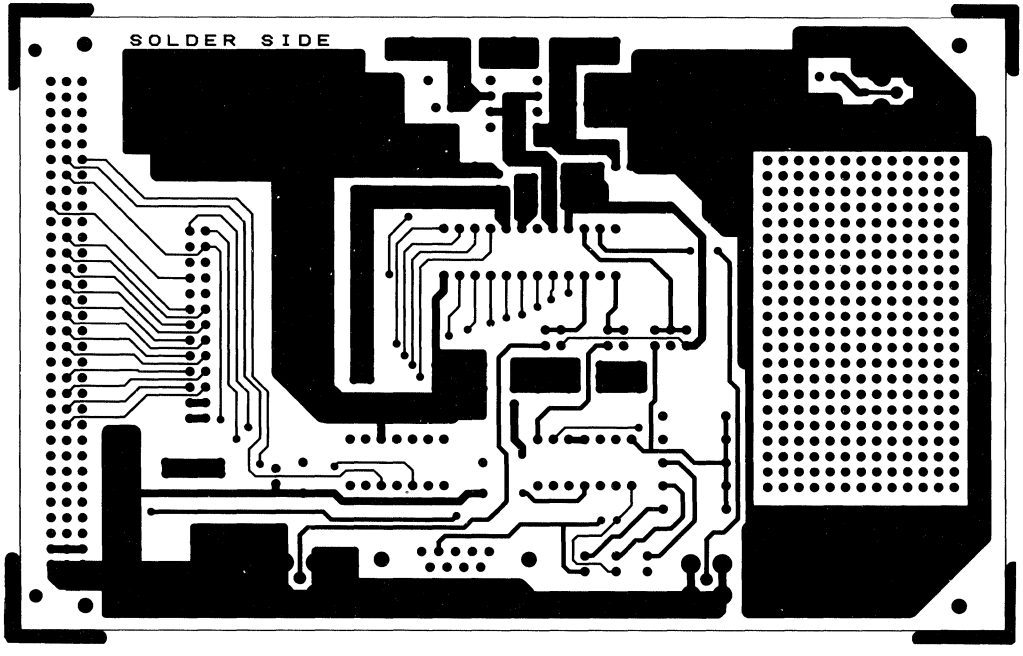


Figure 30. PCB Solder Side Layout for Figure 27

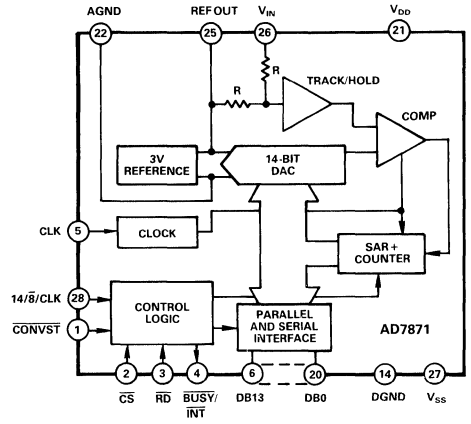
LC²MOS
Complete 14-Bit, Sampling ADC

AD7871/AD7872

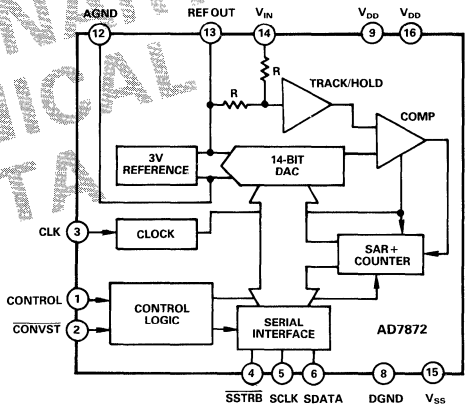
FEATURES
Complete Monolithic 14-Bit ADC
Twos Complement Coding
Parallel, Byte and Serial Digital Interface
82 dB SNR at 10 kHz Input Frequency
57 ns Data Access Time
Low Power – 60 mW typ
83 KSPS Throughput Rate

APPLICATIONS
Digital Signal Processing
High Speed Modems
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control

AD7871 FUNCTIONAL BLOCK DIAGRAM



AD7872 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7871 and AD7872 are fast, complete, 14-bit analog-to-digital converters. They consist of a track/hold amplifier, successive-approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained, laser trimmed internal clock, so no external clock timing components are required. The on-chip clock may be overridden to synchronize ADC operation to the digital system for minimum noise.

The AD7871 offers a choice of three data output formats: a single, parallel, 14-bit word; two 8-bit bytes or a 14-bit serial data stream. The AD7872 is a serial output device only. The two parts are capable of interfacing to all modern microprocessors and digital signal processors.

The AD7871 and AD7872 operate from ±5 V power supplies, accept bipolar input signals of ±3 V and can convert full power signals up to 50 kHz.

In addition to the traditional dc accuracy specifications, the AD7871 and AD7872 are also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

Both devices are fabricated in Analog Devices' LC²MOS mixed technology process. The AD7871 is available in 28-pin plastic DIP, hermetic DIP, LCCC and PLCC packages. The AD7872 is available in 16-pin plastic and hermetic DIP packages.

PRODUCT HIGHLIGHTS

1. Complete 14-Bit ADC on a Chip.
2. Dynamic Specifications for DSP Users.
3. Low Power.

SPECIFICATIONS

(V_{DD}=+5 V ±5%, V_{SS}=−5 V ±5%, AGND=DGND=0 V, f_{CLK}=2 MHz external, F_{SAMPLE}= 83 kHz unless otherwise stated). All Specifications T_{min} to T_{max} unless otherwise noted.

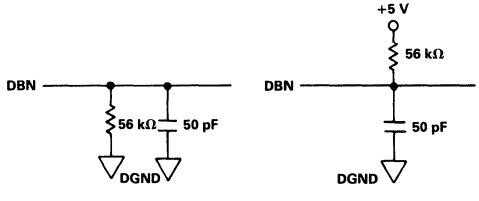
Parameter	J, A Versions[1]	K, B Versions[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR) @ 25°C	78	82	82	dB min	V_{IN}=10 kHz Sine Wave
T_{min} to T_{max}	78	82	82	dB min	
Total Harmonic Distortion (THD)	−84	−86	−86	dB max	V_{IN}=10 kHz Sine Wave THD Is Typically −90 dB for 0 <V_{IN}< 50 kHz.
Peak Harmonic or Spurious Noise	−86	−88	−88	dB max	V_{IN}=10 kHz Peak Harmonic Is Typically −92 dB for 0 <V_{IN}< 50 kHz.
Intermodulation Distortion (IMD)					
Second Order Terms	−85	−85	−85	dB max	fa=9 kHz, fb=9.5 kHz, f_{SAMPLE}=50 kHz
Third Order Terms	−85	−85	−85	dB max	fa=9 kHz, fb=9.5 kHz, f_{SAMPLE}=50 kHz
Track/Hold Acquisition Time	2	2	2	µs max	
DC ACCURACY					
Resolution	14	14	14	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	14	14	14	Bits	
Integral Nonlinearity @ 25°C	±1/2	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Differential Nonlinearity		±1	±1	LSB max	
Bipolar Zero Error	±10	±5	±5	LSB max	
Positive Gain Error[4]	±10	±5	±5	LSB max	
Negative Gain Error[4]	±10	±5	±5	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±500	±500	±500	µA max	
REFERENCE OUTPUT					
REF OUT @ 25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
T_{min} to T_{max}	2.98/3.02	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco		±40	±40	ppm/°C max	The J and A Versions of the AD7871 Have TCs of 60 ppm/°C max.
Reference Load Sensitivity (ΔREF OUT/ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0 – 500 µA). Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD}=5 V±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD}=5 V±5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN}=0 V to V_{DD}
Input Current (14/8/CLK Input Only)	±10	±10	±10	µA max	V_{IN}=V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE}=40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK}=1.6 mA
DB13 – DB0					
Floating-State Leakage Current	10	10	10	µA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
External Clock	9.5/10	9.5/10	9.5/10	µs min/µs max	
Internal Clock	8.5/10.5	8.5/10.5	8.5/10.5	µs min/µs max	The Internal Clock Has a Nominal Value of 2 MHz.
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	mA max	Typically 8 mA
I_{SS}	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	mW max	Typically 60 mW

NOTES
[1]Temperature Ranges are as follows:
J,K Versions; −40°C to +85°C
A,B Versions; −40°C to +85°C
T Version; −55°C to +125°C
[2]V_{IN}=±3V.
[3]SNR calculation includes distortion and noise components.
[4]Measured with respect to internal reference.
[5]Sample tested @25°C to ensure compliance.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1,2] (V_{DD}=+5 V±5%, V_{SS}=−5 V±5%, AGND=DGND=0 V. See Figures 9, 10, 11 and 12.)

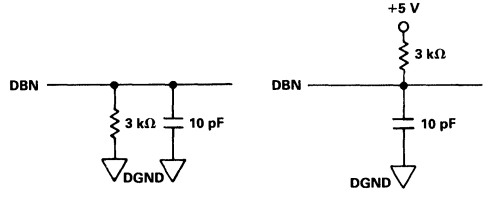
Parameter	Limit at T_{min}, T_{max} (J, K, A, B Versions)	Limit at T_{min}, T_{max} (T Version)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 1)
t_3	**60**	75	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 1)
t_5	70	70	ns min	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[3]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[4]	**5**	**5**	ns min	Bus Relenquish Time after $\overline{RD}$
	50	**50**	ns max	
t_8	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	100	100	ns min	$\overline{SSTRB}$ to SCLK Falling Edge Setup Time
t_{11}[5]	440	440	ns min	SCLK Cycle Time
t_{12}[6]	155	155	ns max	SCLK to Valid Data Delay. CL=35 pF
t_{13}	100	100	ns min	SCLK Rising Edge to $\overline{SSTRB}$
t_{14}	10	10	ns min	Bus Relenquish Time after SCLK
	100	100	ns max	
t_{15}	60	60	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 2)
t_{16}	120	120	ns max	$\overline{CS}$ to BUSY Propagation Delay
t_{17}[3]	200	200	ns min	Data Setup Time Prior to $\overline{BUSY}$
t_{18}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 2)
t_{19}	0	0	ns min	HBEN to $\overline{CS}$ Setup Time
t_{20}	0	0	ns min	HBEN to $\overline{CS}$ Hold Time

NOTES
[1]Timing Specifications in **bold print** are 100% production tested. All other times are sample tested at 25°C to ensure compliance. All input signals are specified with tr=tf=5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and SSTRB and a 2 kΩ pull-up resistor on SCLK. The capacitance on all three outputs is 35 pF.
[3]t_6 and t_{17} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
[5]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
[6]SDATA will drive higher capacitive loads but this will add to t_{12} since it increases the external RC time constant (4.7 kΩ//C_L) and hence the time to reach 2.4 V.
Specifications subject to change without notice.



a. High Z to V_{OH} *b.High Z to V_{OL}*

Figure 1. Load Circuits for Access Time



a. High Z to V_{OH} *b.High Z to V_{OL}*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD}+0.3 V
V_{IN} to AGND . . . . . V_{SS}−0.3 V to V_{DD}+0.3 V
REF OUT to AGND . . . . . 0V to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V to V_{DD}+0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD}+0.3 V
Operating Temperature Range
Commercial (J, K Versions) . . . . . −40°C to +85°C
Industrial (A, B Versions) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION[1]

SNR (dBs)	Relative Accuracy	Temperature Range and Package Options[2]: −40°C to +85°C	−40°C to +85°C	−55°C to +125°C
		Plastic DIP (N-28)	**Cerdip (Q-28)**	**Cerdip (Q-28)**
78 min		AD7871JN	AD7871AQ	
82 min	±1 max	AD7871KN	AD7871BQ	AD7871TQ[3]
		PLCC[4, 5] (P-28A)		
78 min		AD7871JP		
82 min	±1 max	AD7871KP		

SNR (dBs)	Relative Accuracy	Temperature Range and Package Options[2]: −40°C to +85°C	−40°C to +85°C	−55°C to +125°C
		Plastic DIP (N-16)	**Cerdip (Q-16)**	**Cerdip (Q-16)**
78 min		AD7872JN	AD7872AQ	
82 min	±1 max	AD7872KN	AD7872BQ	AD7872TQ[3]

NOTES
[1]To order MIL-STD-883B, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Available to /883B processing only.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]Contact your local sales office for LCCC availability.

AD7871 PIN FUNCTION DESCRIPTION

DIP Pin No.	Pin Mnemonic	Function
1	$\overline{\text{CONVST}}$	Convert Start. A low to high transition on this input puts the track/hold into the hold mode. This input is asynchronous to the CLK. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ must be held high for the duration of this pulse.
2	$\overline{\text{CS}}$	Chip Select. Active low logic input. The device is selected when this input is active. With $\overline{\text{CONVST}}$ tied low, a new conversion is initiated when $\overline{\text{CS}}$ goes low.
3	$\overline{\text{RD}}$	Read. Active low logic input. This input is used in conjunction with $\overline{\text{CS}}$ low to enable the data outputs.
4	$\overline{\text{BUSY}}/\overline{\text{INT}}$	$\overline{\text{Busy}}/\overline{\text{Interrupt}}$. Logic low output indicating converter status. See timing diagrams.
5	CLK	Clock Input. An external TTL-compatible clock may be applied to this input. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed oscillator.
6	DB13/HBEN	Data Bit 13 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the 14/8/CLK input (see Pin 28). When 14-bit data is selected, this pin provides the DB13 output. When either byte or serial data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7 to DB0 is the lower byte of data. With HBEN high, DB7 to DB0 is the upper byte of data (see Table I).

HBEN	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HIGH	LOW	LOW	DB13	DB12	DB11	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table I. Byte Output Format

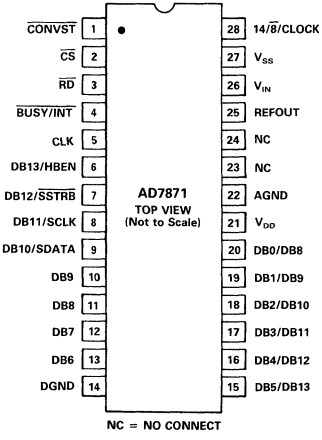
7	DB12/$\overline{\text{SSTRB}}$	Data Bit 12/Serial Strobe. When 14-bit data is selected this pin provides the DB12 data output. Otherwise it is an active low three-state output which provides a framing pulse for serial data.
8	DB11/SCLK	Data Bit 11/Serial Clock. When 14-bit data is selected, this pin provides the DB11 data output. Otherwise SCLK is the gated serial clock output which is derived from the internal or external ADC clock. If the 14/$\overline{8}$ /CLK input is held at −5 V then the SCLK runs continuously. With 14/$\overline{8}$/CLK at 0 V, it is gated off (three-state) after serial transmission is complete.
9	DB10/SDATA	Data Bit 10/Serial Data. When 14-bit parallel data is selected, this pin provides the DB10 data output. Otherwise it is the three-state serial data output used in conjunction with SCLK and $\overline{\text{SSTRB}}$ in serial data transmission. Serial data is valid on the falling edge of SCLK, when $\overline{\text{SSTRB}}$ is low.
10–13	DB9–DB6	Three-State Data Outputs which are controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Their function depends on the state of the 14/$\overline{8}$/CLK and the HBEN inputs. With 14/$\overline{8}$/CLK high, they are always DB9–DB6. With 14/$\overline{8}$/CLK low, their function depends on HBEN (see Table I).
14	DGND	Digital Ground. Ground return for digital circuitry.
15–20	DB5/DB13–DB0/DB8	Three-State Data Outputs which are controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Their function depends on the 14/$\overline{8}$/CLK and HBEN inputs. With 14/$\overline{8}$/CLK high, they are always DB5–DB0. With 14/$\overline{8}$/CLK low or −5 V, their function is controlled by HBEN (see Table I).
21	V_{DD}	Positive Supply, +5 V±5%.
22	AGND	Analog Ground. Ground reference for analog circuitry.
23	NC	No Connect.
24	NC	No Connect.
25	REFOUT	Voltage Reference Output. The internal 3 V referene is provided at this pin. The external load capability is 500 μA.
26	V_{IN}	Analog Input. The input range is ±3 V.
27	V_{SS}	Negative Supply, −5 V±5%.
28	14/$\overline{8}$/CLK	Three-Function Input. Defines both the parallel and serial data formats. With this pin at +5 V, the output data is 14-bit parallel only. With this pin at 0 V, both byte and serial data are available, and the SCLK is noncontinuous. With this pin at −5 V, both byte and serial data are available and the SCLK is continuous.

AD7872 PIN FUNCTION DESCRIPTION

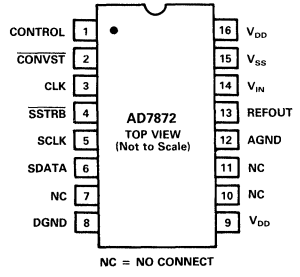
DIP Pin No.	Pin Mnemonic	Function
1	CONTROL	Control Input. With this pin at 0 V, the SCLK is noncontinuous. With this pin at −5 V, the SCLK is continuous.
2	$\overline{\text{CONVST}}$	Convert Start. A low to high transition on this input puts the track/hold into the hold mode. This input is asynchronous to the CLK and is independent of $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
3	CLK	Clock Input. An external TTL-compatible clock may be applied to this input. Alternatively, tying this pin to V_{SS}, enables the internal laser-trimmed oscillator.
4	$\overline{\text{SSTRB}}$	This is an active low three-state output which provides a framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{\text{SSTRB}}$.
5	SCLK	Serial Clock. SCLK is the gated serial clock output which is derived from the internal or external ADC clock. If the 14/$\overline{8}$/CLK input is at −5 V, then the SCLK runs continuously. With 14/$\overline{8}$/CLK at 0 V, it is gated off (three-state) after serial transmission is complete. SCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
6	SDATA	Serial Data. This is the three-state serial data output used in conjunction with SCLK and $\overline{\text{SSTRB}}$ in serial data transmission. Serial data is valid on the falling edge of SCLK, when $\overline{\text{SSTRB}}$ is low. An external 4.7 kΩ pull-up resistor is required on SDATA.
7	NC	No Connect.
8	DGND	Digital Ground. Ground return for digital circuitry.
9	V_{DD}	Positive Supply for digital circuitry, +5 V±5%.
10	NC	No Connect
11	NC	No Connect
12	AGND	Analog Ground. Ground reference for analog circuitry.
13	REFOUT	Voltage Reference Output. The internal 3 V reference is provided at this pin. The external load capability is 500 μA.
14	V_{IN}	Analog Input. The input range is ±3 V.
15	V_{SS}	Negative Supply, −5 V±5%.
16	V_{DD}	Positive Supply for analog circuitry, +5 V±5%.

PIN CONFIGURATIONS

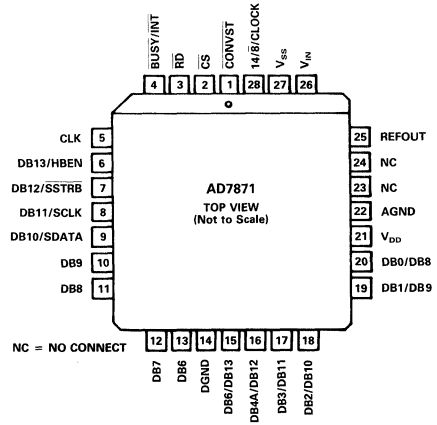
DIP



DIP



PLCC



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

CONVERTER DETAILS

The AD7871/AD7872 is a complete 14-bit A/D converter, requiring no external components apart from power supply decoupling capacitors. It is comprised of a 14-bit successive approximation ADC based on a fast settling voltage-output DAC, a high speed comparator and CMOS SAR, a track/hold amplifier, a 3 V buried Zener reference, a clock oscillator and control logic.

INTERNAL REFERENCE

The AD7871/AD7872 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 3 V ±10 mV. Internally it provides both the DAC reference and the dc bias required for bipolar operation. The reference output is available (REF OUT) and is capable of providing up to 500 μA to an external load.

The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for use external to the AD7871/AD7872, it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the AD7871/AD7872's internal operation.

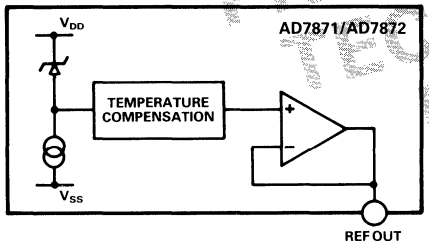


Figure 3. AD7871/AD7872 Reference Circuit

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7871/AD7872 allows the ADC to accurately convert an input sine wave of 6 V peak-peak amplitude to 14-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate. The wide bandwidth of the track/hold allows the high frequency operation. The 0.1 dB cutoff frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 14-bit accuracy in less than 2 μs. The overall throughput rate is determined by the conversion time plus the track/hold amplifier acquisition time. For a 2 MHz input clock the throughput time is 12 μs max.

The operation of the track/hold amplifier is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion. If the $\overline{\text{CONVST}}$ input is used to start conversion, then the track to hold transition occurs on the rising edge of $\overline{\text{CONVST}}$. If $\overline{\text{CS}}$ on the AD7871 starts conversion, this transition occurs on the falling edge of $\overline{\text{CS}}$.

ANALOG INPUT

Figure 4 shows the AD7871/AD7872 analog input. The analog input range is ±3 V into an input resistance of typically 15 kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS −3/2 LSBs). The output code is 2s complement binary with 1 LSB=FS/16384=6 V/16384=366 μV. The ideal input/output transfer function is shown in Figure 5.

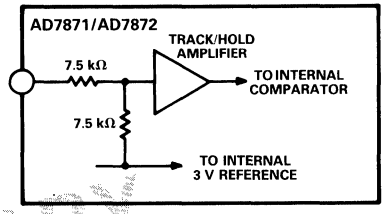


Figure 4. AD7871/AD7872 Analog Input

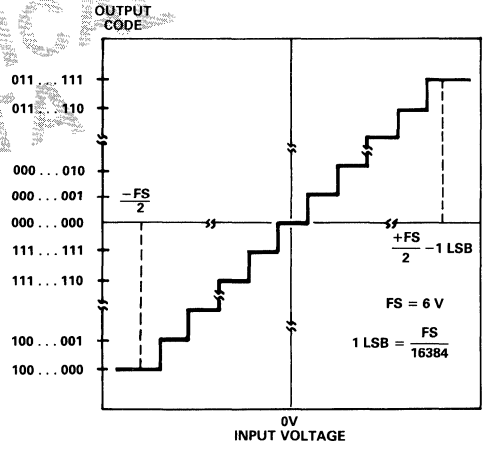


Figure 5. Bipolar Input/Output Transfer Function

BIPOLAR OFFSET AND FULL SCALE ADJUSTMENT

When the AD7871/AD7872's offset and full scale errors need to be adjusted, offset error must be adjusted first. This is achieved by trimming the offset of the op amp driving the analog input of the AD7871/AD7872 while the input voltage is 1/2 LSB below AGND. The trim procedure is as follows: apply a voltage of −0.183 mV (−1/2 LSB) at V_1 in Figure 6 and adjust the op amp offset voltage until the ADC output code flickers between 11 1111 1111 1111 and 00 0000 0000 0000.

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 6).

Positive Full Scale Adjust
Apply a voltage of 2.9995 V (FS/2 −3/2 LSBs) at V_1 and adjust R2 until the ADC output code flickers between 01 1111 1111 1110 and 01 1111 1111 1111.

Negative Full Scale Adjust
Apply a voltage of −2.9998 V (−FS/2+1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 10 0000 0000 0000 and 10 0000 0000 0001.

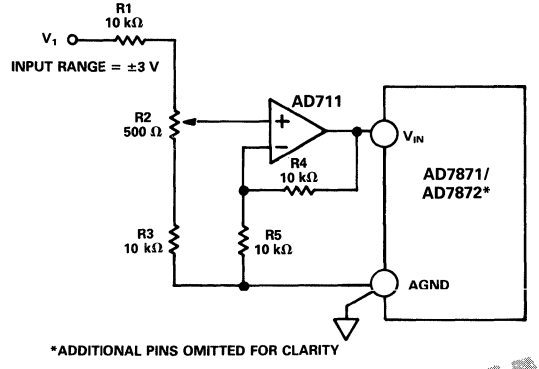


Figure 6. Bipolar Adjust Circuit

UNIPOLAR OPERATION

A typical unipolar circuit is shown in Figure 7. The AD7871/ AD7872 REF OUT is used to offset the analog input by 3 V. The analog input range is determined by the ratio of R3 to R4. The minimum range with which the circuit will work is 0 to +3 V. The resistor values are given in Figure 7 for input ranges of 0 to +5 V and 0 to +10 V. R5 and R6 are included for offset and full scale adjust only and should be omitted if adjustment is not required.

The ideal input/output transfer function is shown in Figure 8. The output can be converted to straight binary by inverting the MSB.

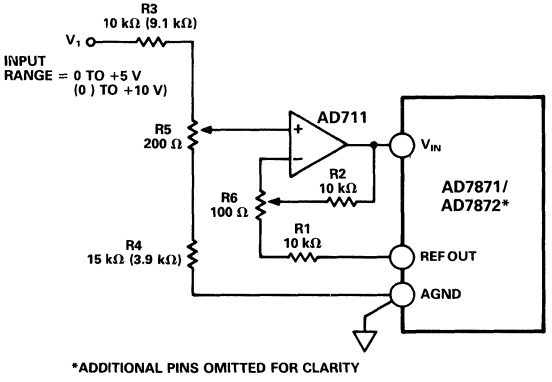


Figure 7. AD7871/AD7872 Unipolar Circuit

UNIPOLAR OFFSET AND FULL-SCALE ADJUSTMENT

When absolute accuracy is required, offset and full scale error can be adjusted to zero. Offset must be adjusted before full scale. This is achieved by applying an input voltage of (1/2 LSB) to V_1 and adjust R6 until the ADC output code flickers between 10 0000 0000 0000 and 10 0000 0000 0001. For full scale adjustment apply an input voltage of (FS-3/2 LSBs) to V_1 and adjust R5 until the output code flickers between 01 1111 1111 1110 and 01 1111 1111 1111.

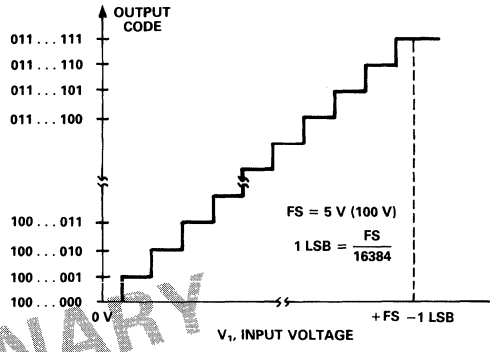


Figure 8. Unipolar Transfer Function

TIMING AND CONTROL

The conversion cycle normally consists of 19 clock periods. The conversion time for both external and internal clock can vary from 19 to 20 clock cycles depending on the conversion start to ADC clock synchronization. If a conversion is initiated within 30 ns prior to a rising edge of the ADC clock, the conversion time will consist of 20 clock cycles.

There are two basic operating modes for the AD7871. In the first mode (Mode 1) the $\overline{\text{CONVST}}$ line is used to start conversion and drive the track/hold into its hold mode. At the end of conversion the track/hold returns to its tracking mode. It is intended principally for digital signal processing and other applications where precise sampling in time is required. In these applications, it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. For these cases the $\overline{\text{CONVST}}$ line is driven by a timer or some precise clock source.

The second mode is achieved by hard-wiring the $\overline{\text{CONVST}}$ line low. This mode (Mode 2) is intended for use in systems where the microprocessor has total control of the ADC, both initiating the conversion and reading the data. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ start conversion and the microprocessor will normally be driven into a WAIT state for the duration of conversion by $\overline{\text{BUSY}}/\overline{\text{INT}}$.

The AD7872 has one operating mode only. This is Mode 1, described above, which uses $\overline{\text{CONVST}}$ to start conversion.

DATA OUTPUT FORMATS

The AD7871 offers a choice of three data output formats, one serial and two parallel. The parallel data formats include a single 14-bit parallel word for 16-bit data buses and a two-byte format for 8-bit data buses. The data format is controlled by the 14/$\overline{8}$/CLK input. A logic high on this pin selects the 14-bit parallel output format only. A logic low or −5 V applied to this pin allows the user access to either serial or byte formatted data.

Three of the pins previously assigned to the four MSBs in parallel form are now used for serial communications while the fourth pin becomes a control input for the byte-formatted data. The three possible data output formats can be selected in either of the modes of operation.

The AD7872 is a serial output device only. The serial data format is exactly the same as the AD7871.

Parallel Output Format

The two parallel formats available on the AD7871 are a 14-bit wide data word and a two-byte data word. In the first, all 14 bits of data are available at the same time on DB13 (MSB) through DB0 (LSB). In the second, two reads are required to access the data. When this data format is selected, the DB13/HBEN pin assumes the HBEN function. HBEN selects which byte of data is to be read from the AD7871. When HBEN is low, the lower 8 bits of data are placed on the data bus during a read operation; with HBEN high, the upper six bits of the 14-bit word are placed on the data bus. These six bits are right justified and thereby occupy the lower six bits of the byte while the upper two bits are zeros.

Serial Output Format

Serial data is available on the AD7871 when the 14/$\overline{8}$/CLK input is at 0 V or −5 V and in this case the DB12/$\overline{\text{SSTRB}}$, DB11/SCLK and DB10/SDATA pins assume their serial functions. The AD7872 is a serial output device only. The serial function on both devices is identical. Serial data is available during conversion with a word length of 16 bits; 2 leading zeros, followed by the 14-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (SCLK) and is framed by the serial strobe ($\overline{\text{SSTRB}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{SSTRB}}$ output is low. $\overline{\text{SSTRB}}$ goes low at the start of conversion and the first serial data bit (which is the first leading zero) is valid on the first falling edge of SCLK. All the serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC master clock source which may be internal or external. Normally, SCLK is required during the serial transmission only. In these cases it can be shut down (i.e., placed into three-state) at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a serial clock which runs continuously. Both options are available on the AD7871 and AD7872. With the 14/$\overline{8}$/CLK input on the AD7871 at −5 V, the serial clock (SCLK) runs continuously; when 14/$\overline{8}$/CLK is at 0 V, SCLK goes into three-state at the end of transmission. The CONTROL pin on the AD7872 performs the same function. When this is at 0 V, SCLK is noncontinuous and when it is at −5 V, SCLK is continuous.

MODE 1 INTERFACE

Conversion is initiated by a low going pulse on the $\overline{\text{CONVST}}$ input. The rising edge of this $\overline{\text{CONVST}}$ pulse starts conversion and drives the track/hold amplifier into its hold mode. Note that $\overline{\text{CS}}$ and $\overline{\text{RD}}$ should be high when $\overline{\text{CONVST}}$ is brought low. The $\overline{\text{BUSY}}$/$\overline{\text{INT}}$ status output assumes its $\overline{\text{INT}}$ function in this mode. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. This $\overline{\text{INT}}$ line can be used to interrupt the microprocessor.

A read operation to the AD7871 accesses the data and the $\overline{\text{INT}}$ line is reset high on the falling edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$. The $\overline{\text{CONVST}}$ input must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low for the AD7871 to operate correctly in this mode. It is important, especially in systems where the conversion start ($\overline{\text{CONVST}}$) pulse is asynchronous to the microprocessor, to ensure that a parallel or byte data read is not attempted during a conversion. Trying to read data during a conversion can cause errors to the conversion in progress. Avoid pulsing the $\overline{\text{CONVST}}$ line a second time before conversion end since it can cause errors in the conversion result. In applications where precise sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from microprocessor $\overline{\text{WR}}$ line OR-gated with the AD7871 $\overline{\text{CS}}$ input.

Figure 9 shows the Mode 1 timing diagram for a 14-bit parallel data output format (14/$\overline{8}$/CLK = +5 V). A read to the AD7871 at the end of conversion accesses all 14 bits of data at the same time. Serial data is not available for this data output format.

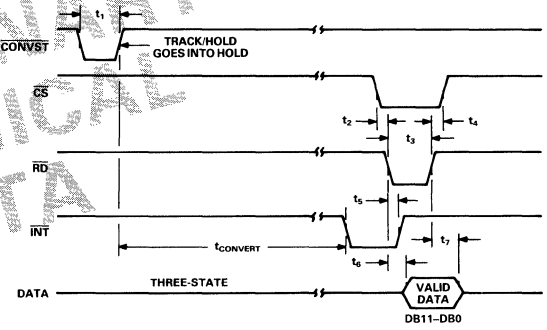


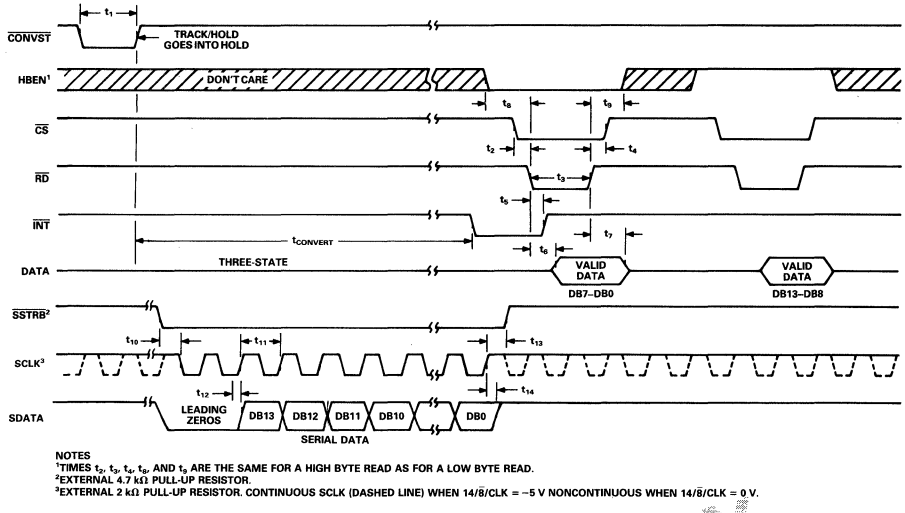
Figure 9. Mode 1 Timing Diagram, 14-Bit Parallel Read

The Mode 1 function timing diagram for byte and serial data is shown in Figure 10. $\overline{\text{INT}}$ goes low at the end of conversion and is reset high by the first falling edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$. This first read at the end of conversion can either access the low byte or high byte of data depending on the status of HBEN (Figure 10 shows low byte for example only). The diagram shows both the SCLK output going into three-state at the end of transmission and a continuously running clock (dashed line).

MODE 2 INTERFACE

The second interface mode is achieved by hard-wiring $\overline{\text{CONVST}}$ low and conversion is initiated by taking $\overline{\text{CS}}$ low while HBEN is low. The track/hold amplifier goes into the hold mode on the falling edge of $\overline{\text{CS}}$. In this mode the $\overline{\text{BUSY}}$/$\overline{\text{INT}}$ pin assumes its $\overline{\text{BUSY}}$ function. $\overline{\text{BUSY}}$ goes low at the start of conversion, stays low during the conversion and returns high when the conversion is complete. It is normally used in parallel interfaces to drive the microprocessor into a WAIT state for the duration of conversion.

Figure 11 shows the Mode 2 timing diagram for the 14-bit parallel data output format (14/$\overline{8}$/CLK = +5 V). In this case the ADC behaves like slow memory. The major advantage of this interface is that it allows the microprocessor to start conversion,



NOTES
¹TIMES t_2, t_3, t_4, t_8, AND t_9 ARE THE SAME FOR A HIGH BYTE READ AS FOR A LOW BYTE READ.
²EXTERNAL 4.7 kΩ PULL-UP RESISTOR.
³EXTERNAL 2 kΩ PULL-UP RESISTOR. CONTINUOUS SCLK (DASHED LINE) WHEN 14/$\overline{8}$/CLK = −5 V NONCONTINUOUS WHEN 14/$\overline{8}$/CLK = 0 V.

Figure 10. Mode 1 Timing Diagram, Byte or Serial Read

WAIT and then read data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid the reading during conversion.

The Mode 2 timing diagram for byte and serial data is shown in Figure 12. For two-byte data read, the lower byte (DB0–DB7) has to be accessed first since HBEN must be low to start conversion. The ADC behaves like slow memory for this first read, but the second read to access the upper byte of data is a normal read. Operation to the serial functions is identical between Mode 1 and Mode 2. Once again, the timing diagram of Figure 12 shows SCLK going into three-state or running continuously (dashed line).

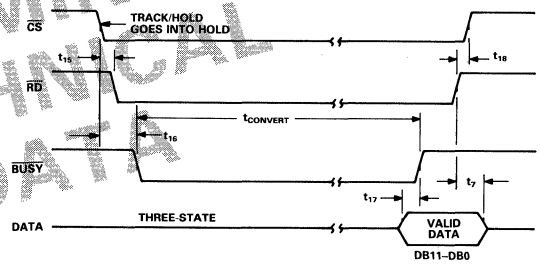
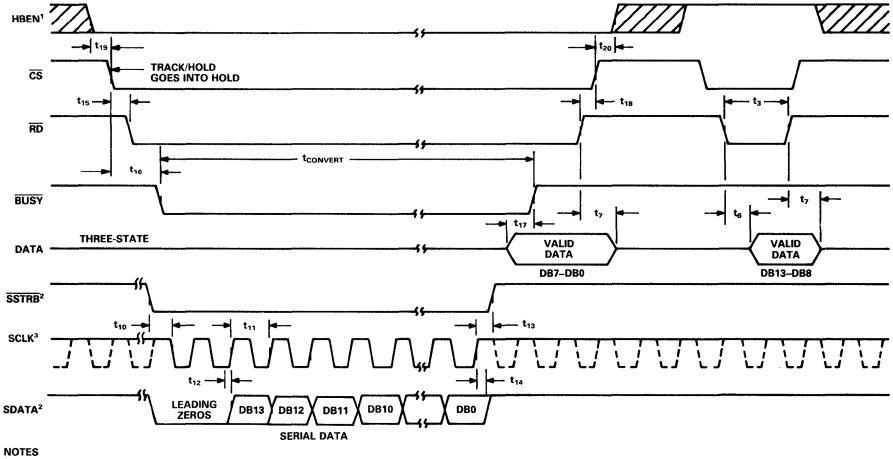


Figure 11. Mode 2 Timing Diagram, 14-Bit Parallel Read



NOTES
¹TIMES t_{15}, t_{18}, t_{19}, AND t_{20} ARE THE SAME FOR A HIGH BYTE READ AS FOR A LOW BYTE READ.
²4.7 kΩ PULL-UP RESISTOR ON SSTRB.
³CONTINUOUS SCLK (DASHED LINE) WHEN 12/$\overline{8}$/CLK = −5 V NONCONTINUOUS WHEN 12/$\overline{8}$/CLK = 0 V. EXTERNAL 2 kΩ PULL-UP RESISTOR.

Figure 12. Mode 2 Timing Diagram, Byte or Serial Read

MICROPROCESSOR INTERFACE

The AD7871 and AD7872 have a wide variety of interfacing options. The AD7871 offers two operating modes and three data-output formats, while the AD7872 is a dedicated serial output device. The fast data access times on the parallel modes of the AD7871 allow interfacing to the very fast DSPs. The serial mode on both the AD7871 and AD7872 is compatible with the serial port structures on all the popular DSPs.

Parallel Read Interfacing

Figures 13 and 14 show interfaces to the ADSP-2100 and the TMS32020/C25 DSP processors. The AD7871 is operating in Mode 1, parallel read for both interfaces. An external timer controls conversion start asynchronously to the microprocessor. At the end of each conversion the ADC $\overline{BUSY/INT}$ interrupts the microprocessor and the conversion result is read from the ADC with the following instruction:

ADSP-2100 MR0 = DM(ADC)

TMS32020/C25: IN D,ADC

MR0 = ADSP-2100 MR0 Register

D = Data Memory Address

ADC = AD7871 Address

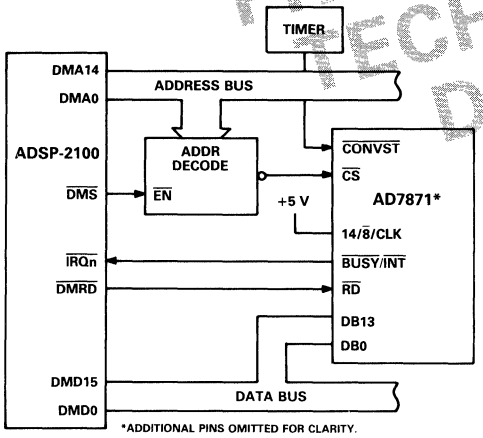


Figure 13. AD7871 to ADSP-2100 Parallel Interface

Some applications may require that conversions be initiated by the microprocessor rather than an external timer. One option is to decode the AD7871 $\overline{CONVST}$ from the address bus so that a write operation to the ADC starts a conversion. Data is read at the end of conversion as described earlier. Note, a read operation must not be attempted during conversion.

Serial Interfacing

Both the AD7871 and the AD7872 have an identical serial interface. The diagrams that follow show the AD7872 interfaces only but the AD7871 could just as easily be used in these circuits. Figures 15, 16 and 17 show the AD7872 connected to three popular DSP's. In all three interfaces, $\overline{CONVST}$ is used to start conversion since this does not activate the parallel bus. Thus,

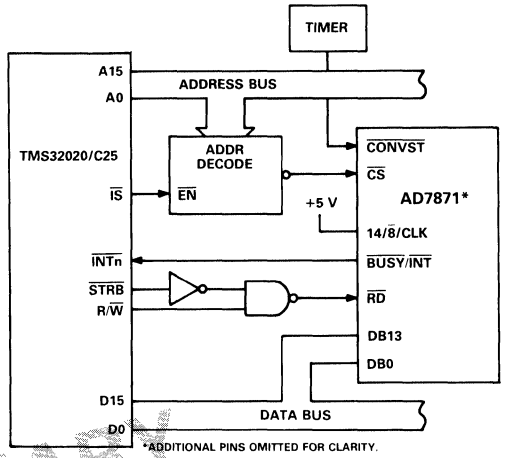


Figure 14. AD7871 to TMS32020/C25 Interface

the microprocessor can continue to use its parallel bus regardless of the state of the AD7872. The interfaces show a timer driving the $\overline{CONVST}$ input but this could be generated from a decoded address if required.

AD7872 – DSP56000 Serial Interface

Figure 15 shows a serial interface between the AD7872 and the DSP56000. The interface arrangement is two-wire with the AD7872 configured for non-continuous clock operation (14/8/CLK=0 V). The DSP56000 is configured for Normal Mode Synchronous Operation with Gated Clock. It is also set up for a 16-bit word with SCK and SC2 as inputs and the FSL control bit set to a 0. In this configuration, the DSP56000 assumes valid data on the first falling edge of SCK. Since the AD7872 provides valid data on this first edge there is no need for a strobe or framing pulse for the data. SCLK and SDATA are three-stated when the AD7872 is not performing a conversion. During conversion data is valid on the SDATA output of the AD7872 and is clocked into the Receive Data Shift Register of the DSP56000. When this register has received 16 bits of data, it generates an internal interrupt on the DSP56000 to read the data from the register.

The DSP56000 and AD7872 can also be configured for continuous clock operation. In this case a strobe pulse is required by the DSP56000 to indicate when data is valid. The $\overline{SSTRB}$ output of the AD7872 is inverted and applied to the SC2 input of the DSP56000 to provide this strobe pulse. All other conditions and connections are the same as for the gated clock operation.

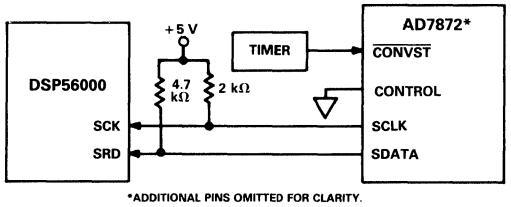


Figure 15. AD7872 to DSP56000 Interface

AD7872 – TMS32020/C25 Serial Interface

Figure 16 shows a serial interface between the AD7872 and the TMS32020/C25. The AD7872 is configured for continuous clock operation. Note, the ADC will not interface correctly to the TMS32020/C25 if it is configured for a non-continuous clock. Data is clocked into the Data Receive Register (DRR) of the TMS32020/C25 during conversion. As with the previous interfaces, when a 16-bit word is received by the DSP it generates an internal interrupt to read the data from the DRR.

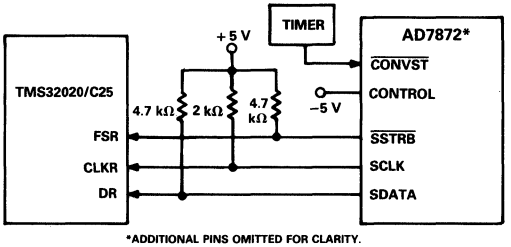


Figure 16. AD7872 to TMS32020/C25 Interface

AD7872 – ADSP-2101/ADSP-2102 Serial Interface

Figure 17 shows a serial interface between the AD7872 and the ADSP-2101/ADSP-2102 DSP Microcomputer. The AD7872 is configured for continuous clock operation. Data is clocked into the serial port register of the microcomputer during conversion. As with the previous interfaces, when a 16-bit data word is received by the ADSP-2101/ADSP-2102 an internal mictoprocessor interrupt is generated and the data is read from the serial port register.

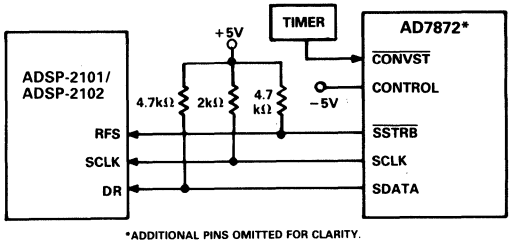


Figure 17. AD7872–ADSP-2101/ADSP-2102 Serial Interface

STAND-ALONE OPERATION

The AD7871 can be used in its Mode 2, parallel mode for stand-alone operation. In this case, conversion is initiated with a pulse to the $\overline{CS}$ input. This pulse must be longer than the conversion time of the ADC. The $\overline{BUSY}$ output is used to drive the $\overline{RD}$ input. Data is latched from the AD7871 DB0 – DB11 outputs to an external latch on the rising edge of $\overline{BUSY}$.

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7871/AD7872 is required to make bit decisions on an LSB size of 366 μV. Thus, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LC²MOS Complete 12-Bit 100kHz Sampling ADC with DSP Interface

AD7878

FEATURES

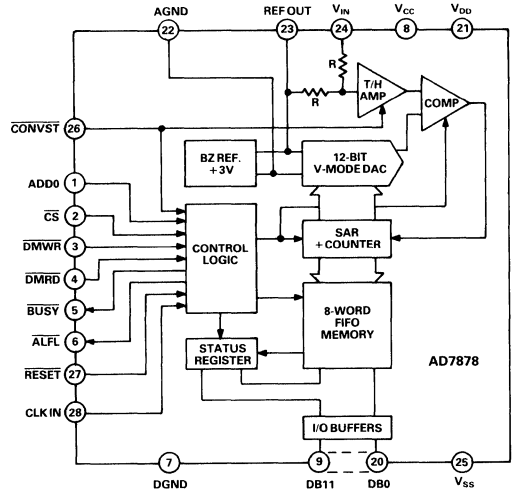
Complete ADC with DSP Interface, Comprising:
- **Track/Hold Amplifier with 2μs Acquisition Time**
- **7μs A/D Converter**
- **3V Zener Reference**
- **8-Word FIFO and Interface Logic**

72dB SNR at 10kHz Input Frequency
Interfaces to High Speed DSP Processors, e.g., ADSP-2100, TMS32010, TMS32020
41ns max Data Access Time
Low Power, 60mW typ

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

AD7878 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7878 is a fast complete 12-bit A/D converter with a versatile DSP interface consisting of an 8-word, first-in, first-out (FIFO) memory and associated control logic.

The FIFO memory allows up to eight samples to be digitized before the microprocessor is required to service the A/D converter. The eight words can then be read out of the FIFO at maximum microprocessor speed. A fast data access time of 41ns allows direct interfacing to DSP processors and high speed 16-bit microprocessors.

An on-chip status/control register allows the user to program the effective length of the FIFO and contains the FIFO out of range, FIFO empty and FIFO word count information.

The analog input of the AD7878 has a bipolar range of ±3V. The AD7878 can convert full power signals up to 50kHz and is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion.

The AD7878 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in four package styles, 28-pin plastic and hermetic dual-in-line package (DIP), leadless ceramic chip carrier (LCCC) or plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete A/D Function with DSP Interface
   The AD7878 provides the complete function for digitizing ac signals to 12-bit accuracy. The part features an on-chip track/hold, on-chip reference and 12-bit A/D converter. The additional feature of an 8-word FIFO reduces the high software overheads associated with servicing interrupts in DSP processors.
2. Dynamic Specifications for DSP Users
   The AD7878 is fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and specified over the full operating temperature range.
3. Fast Microprocessor Interface
   Data access time of 41ns is the fastest ever achieved in a monolithic A/D converter and makes the AD7878 compatible with all modern 16-bit microprocessors and digital signal processors.

SPECIFICATIONS (V_{DD} = +5V ±5%, V_{CC} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V, f_{CLK} = 8MHz. All Specifications T_{min} to T_{max} unless otherwise noted.)

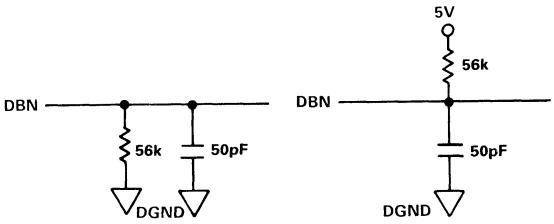
Parameter	J, A Versions[1]	K, L, B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio (SNR)[3] @ 25°C	70	72	70	dB min	V_{IN} = 10kHz sine wave, f_{SAMPLE} = 100kHz
T_{min} to T_{max}	70	71	70	dB min	Typically 71.5dB for 0<V_{IN}<50kHz
Total Harmonic Distortion (THD)	−80	−80	−80	dB max	V_{IN} = 10kHz sine wave, f_{SAMPLE} = 100kHz Typically −86dB for 0<V_{IN}<50kHz
Peak Harmonic or Spurious Noise	−80	−80	−80	dB max	V_{IN} = 10kHz, f_{SAMPLE} = 100kHz Typically −86dB for 0<V_{IN}<50kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−80	dB max	fa = 9kHz, fb = 9.5kHz, f_{SAMPLE} = 50kHz
Third Order Terms	−80	−80	−80	dB max	fa = 9kHz, fb = 9.5kHz, f_{SAMPLE} = 50kHz
Track/Hold Acquisition Time	2	2	2	µs max	See Throughput Rate section.
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for which No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy	±1/2	±1/4	±1/2	LSB typ	
Differential Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Bipolar Zero Error	±6	±6	±6	LSB max	
Positive Full Scale Error[4]	±6	±6	±6	LSB max	
Negative Full Scale Error[4]	±6	±6	±6	LSB max	
ANALOG INPUT					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±550	±550	±550	µA max	
REFERENCE OUTPUT[5]					
REF OUT	3	3	3	V nom	
REF OUT Error @ 25°C	±10	±10	±10	mV max	
T_{min} to T_{max}	±15	±15	±15	mV max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	mV max	Reference Load Current change (0 – 500µA). Reference Load should not be changed during conversion.
LOGIC INPUTS					
Input High Voltage, V_{INH}	+2.4	+2.4	+2.4	V min	V_{CC} = +5V ±5%
Input Low Voltage, V_{INL}	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 to V_{CC}
Input Capacitance, C_{IN}[6]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	+2.7	+2.7	+2.7	V min	I_{SOURCE} = 40µA
Output Low Voltage, V_{OL}	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
DB11 – DB0					
Floating State Leakage Current	±10	±10	±10	±10	µA max
Floating State Output Capacitance[6]	15	15	15	15	pF max
CONVERSION TIME					
	7/7.125	7/7.125	7/7.125	µs min/µs max	Assuming no external Read/Write operations
	7/9.250	7/9.250	7/9.250	µs min/µs max	Assuming 17 external Read/Write operations See Internal Comparator Timing section
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for specified performance
V_{CC}	+5	+5	+5	V nom	±5% for specified performance
V_{SS}	−5	−5	−5	V nom	±5% for specified performance
I_{DD}	13	13	13	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5V
I_{CC}	100	100	100	µA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5V
I_{SS}	6	6	6	mA max	$\overline{CS}$ = $\overline{DMWR}$ = $\overline{DMRD}$ = 5V
Power Dissipation	95.5	95.5	95.5	mW max	Typically 60mW

NOTES
[1]Temperature range as follows:
J, K, L versions: 0 to +70°C
A, B versions: −25°C to +85°C
S version: −55°C to +125°C
[2]V_{IN} = ±3V. See Dynamic Specifications section.
[3]SNR calculation includes distortion and noise components.
[4]Measured with respect to the Internal Reference.
[5]For Capacitive Loads greater than 50pF a series resistor is required (see Internal Reference section).
[6]Sample tested @ 25°C to ensure compliance.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 5V ± 5%, V_{CC} = 5V ± 5%, V_{SS} = −5V ± 5%)

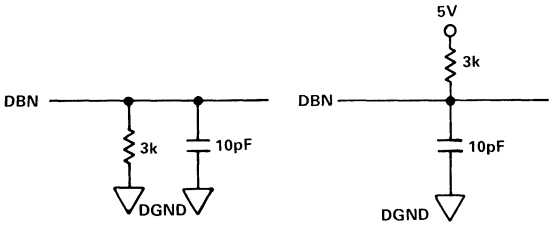
Parameter	Limit at T_{min}, T_{max} (L Grade)	Limit at T_{min}, T_{max} (J,K,A,B Grades)	Limit at T_{min}, T_{max} (S Grade)	Units	Conditions/Comments
t_1	65	65	75	ns max	CLK IN to $\overline{BUSY}$ Low Propagation Delay
t_2	65	65	75	ns max	CLK IN to $\overline{BUSY}$ High Propagation Delay
t_3	2 CLK IN cycles	2 CLK IN cycles	2 CLK IN cycles	min	$\overline{CONVST}$ Pulse Width
t_4	0	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$/REGISTER ENABLE Setup Time
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{DMRD}$/REGISTER ENABLE Hold Time
t_6	**45**	**60**	**60**	ns min	$\overline{DMRD}$ Pulse Width
	50	50	50	µs max	
t_7	**16**	**16**	**16**	ns min	ADD0 to $\overline{DMRD}$/REGISTER ENABLE Setup Time
t_8	0	0	0	ns min	ADD0 to $\overline{DMRD}$/REGISTER ENABLE Hold Time
t_9[2]	**41**	**57**	**57**	ns min	Data Access Time after $\overline{DMRD}$
t_{10}[3]	**5**	**5**	**5**	ns min	Bus Relinquish Time
	45	**45**	**45**	ns max	
t_{11}	**42**	**42**	55	ns min	REGISTER ENABLE Pulse Width
	50	50	50	µs max	
t_{12}	**20**	**20**	**30**	ns min	Data Valid to REGISTER ENABLE Setup Time
t_{13}	10	10	10	ns min	Data Hold Time after REGISTER ENABLE
t_{14}[2]	41	57	57	ns min	Data Access Time after $\overline{BUSY}$

NOTES
[1]Timing Specifications in **bold** print are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
[2]t_9 and t_{14} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_{10} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND	−0.3V to +7V
V_{CC} to DGND	−0.3V to +7V
V_{SS} to DGND	+0.3V to −7V
V_{DD} to V_{CC}	−0.3V to +0.3V
AGND to DGND	−0.3V to V_{DD} +0.3V
V_{IN} to AGND	−15V to +15V
REF OUT to AGND	0 to V_{DD}
Digital Inputs to DGND	
$\overline{CLK\ IN}$, $\overline{DMWR}$, $\overline{DMRD}$, $\overline{RESET}$, $\overline{CS}$, $\overline{CONVST}$, ADD0	−0.3V to V_{DD} +0.3V
Digital Outputs to DGND	
$\overline{ALFL}$, $\overline{BUSY}$	−0.3V to V_{DD} +0.3V
Data Pins	
DB11 – DB0	−0.3V to V_{DD} +0.3V
Operating Temperature Range	
J, K, L Versions	0 to +70°C
A, B Versions	−25°C to +85°C
S Version	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	1000mW
Derates above +75°C by	10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

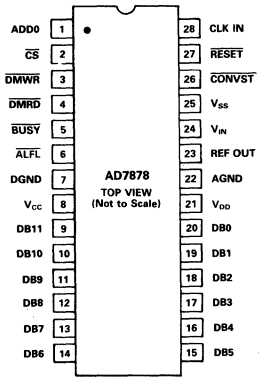
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN FUNCTION DESCRIPTION

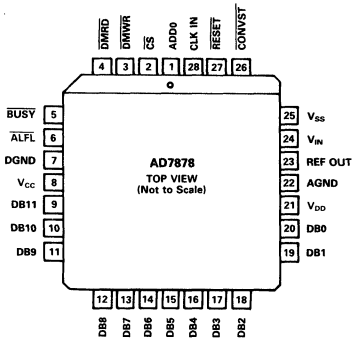
Pin Number	Pin Mnemonic	Function
1	ADD0	Address Input. This control input determines whether the word placed on the output data bus during a read operation is a data word from the FIFO RAM or the contents of the status/control register. A logic low accesses the data word from Location 0 of the FIFO while a logic high selects the contents of the register (see Status/Control Register section).
2	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.
3	$\overline{DMWR}$	Data Memory Write. Active low logic input. $\overline{DMWR}$ is used in conjunction with $\overline{CS}$ low and ADD0 high to write data to the status/control register. Corresponds to $\overline{DMWR}$ (ADSP-2100), R/$\overline{W}$ (MC68000, TMS32020), $\overline{WE}$ (TMS32010).
4	$\overline{DMRD}$	Data Memory READ. Active low logic input. $\overline{DMRD}$ is used in conjunction with $\overline{CS}$ low to enable the three-state output buffers. Corresponds directly to $\overline{DMRD}$ (ADSP-2100), $\overline{DEN}$ (TMS32010).
5	$\overline{BUSY}$	Active low logic output. This output goes low when the ADC receives a $\overline{CONVST}$ pulse and remains low until the track/hold has gone into its hold mode. The three-state drivers of the AD7878 can be disabled while the $\overline{BUSY}$ signal is low (see Extended READ/WRITE section). This is achieved by writing a logic 0 to DB5 ($\overline{DISO}$) of the status/control register. Writing a logic 1 to DB5 of the status/control register allows data to be accessed from the AD7878 while $\overline{BUSY}$ is low.
6	$\overline{ALFL}$	FIFO Almost Full. A logic low indicates that the word count (i.e., number of conversion results) in the FIFO memory has reached the programmed word count in the status/control register. $\overline{ALFL}$ is updated at the end of each conversion. The $\overline{ALFL}$ output is reset to a logic high when a word is read from the FIFO memory. It can also be set high by writing a logic 1 to DB7 ($\overline{ENAF}$) of the status/control register.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	V_{CC}	Digital supply voltage, +5V ±5%. Positive supply voltage for digital circuitry.
9	DB11	Data Bit 11 (MSB). Three-state TTL output. Coding for the data words in FIFO RAM is 2s complement.
10-15	DB10-DB5	Data Bit 10 to Data Bit 5. Three-state TTL input/outputs.
16-19	DB4-DB1	Data Bit 4 to Data Bit 1. Three-state TTL outputs.
20	DB0	Data Bit 0 (LSB). Three-state TTL output.
21	V_{DD}	Analog positive supply voltage, +5V ±5%.
22	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
23	REF OUT	Voltage Reference Output. The internal 3V analog reference is provided at this pin. The external load capability of the reference is 500μA.
24	V_{IN}	Analog Input. Analog input range is ±3V.
25	V_{SS}	Analog negative supply voltage, −5V ±5%.
26	$\overline{CONVST}$	Convert Start. Logic input. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. The $\overline{CONVST}$ input is asynchronous to CLK IN and independent of $\overline{CS}$, $\overline{DMWR}$ and $\overline{DMRD}$.
27	$\overline{RESET}$	Reset. Active low logic input. A logic low sets the words in FIFO memory to 1000 0000 0000 and resets the $\overline{ALFL}$ output and status/control register.
28	CLK IN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark-space ratio of this clock can vary from 35/65 to 65/35.

PIN CONFIGURATIONS

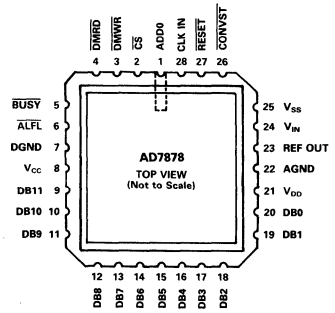
DIP



PLCC



LCCC



STATUS/CONTROL REGISTER

The status/control register serves the dual function of providing control and monitoring the status of the FIFO memory. This register is directly accessible through the data bus (DB11 – DB0) with a read or write operation while ADD0 is high. A write operation to the status/control register provides control for the $\overline{\text{ALFL}}$ output, bus interface and FIFO counter reset. This is normally done on power-up initialization. The FIFO memory address pointer is incremented after each conversion and compared with a preprogrammed count in the status/control register. When this preprogrammed count is reached, the $\overline{\text{ALFL}}$ output is asserted if the $\overline{\text{ENAF}}$ control bit is set to zero. This $\overline{\text{ALFL}}$ can be used to interrupt the microprocessor after any predetermined number of conversions (between 1 and 8). The status of the address pointer along with sample overrange and $\overline{\text{ALFL}}$ status can be accessed at any time by reading the status/control register. Note, reading the status/control register does not cause any internal data movement in the FIFO memory. Status information for a particular word should be read from the status register before the data word is read from the FIFO memory.

STATUS/CONTROL REGISTER FUNCTION DESCRIPTION

DB11 ($\overline{\text{ALFL}}$)

Almost Full Flag, Read only. This the same as Pin 6 ($\overline{\text{ALFL}}$ output) status. A logic low indicates that the word count in the FIFO memory has reached the preprogrammed count in bit locations DB10 – DB8. $\overline{\text{ALFL}}$ is updated at the end of conversion.

DB10 – DB8 (AFC2 – AFC0)

Almost Full Word Count, Read/Write. The count value determines the number of words in the FIFO memory which will cause $\overline{\text{ALFL}}$ to be set. When the FIFO word count equals the programmed count in these three bits, then both the $\overline{\text{ALFL}}$ output and DB11 of the status register are set to a logic low. For example, when a code of 011 is written to these bits, $\overline{\text{ALFL}}$ is set when Location 0 through Location 3 of the FIFO memory contains valid data. AFC2 is the most significant bit of the word count. The count value can be read back if required.

DB7 ($\overline{\text{ENAF}}$)

Enable Almost Full, Read/Write. Writing a 1 to this bit disables the $\overline{\text{ALFL}}$ output and status register bit DB11.

DB6 (FOVR/RESET)

FIFO Overrun/RESET, Read/Write. Reading a 1 from this bit indicates that at least one sample has been discarded because the FIFO memory is full. When the FIFO is full (i.e., contains eight words) any further conversion results will be lost. Writing a 1 to this bit causes a system RESET as per the $\overline{\text{RESET}}$ input (Pin 27).

DB5 (FOOR/$\overline{\text{DISO}}$)

FIFO Out of RANGE/Disable Outputs, Read/Write. Reading a 1 from this bit indicates that at least one sample in the FIFO memory is out of range. Writing a 0 to this bit prevents the data bus from becoming active while $\overline{\text{BUSY}}$ is low regardless of the state of $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$.

DB4 (FEMP)

FIFO Empty, Read Only. Reading a 1 indicates that there are no samples in the FIFO memory. When the FIFO is empty the internal ripple-down effects of the FIFO are disabled and further reads will continue to access the last valid data word in Location 0.

DB3 (SOOR)

Sample out of Range, Read Only. Reading a 1 indicates that the next sample to be read is out of range, i.e., the sample in Location 0 of the FIFO.

DB2 – DB0 (FCN2 – FCN0)

FIFO Word Count, Read Only. The value read from these bits indicates the number of samples in the FIFO memory. For example, reading 011 from these bits indicates that Location 0 through Location 3 contains valid data. Note, reading all 0s indicates that there is either one word or no word in the FIFO memory; in this case the FIFO Empty determines if there is no word in memory. FCN2 is the most significant bit.

BIT LOCATION	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
STATUS INFORMATION (READ)	$\overline{\text{ALFL}}$	AFC2	AFC1	AFC0	$\overline{\text{ENAF}}$	FOVR	FOOR	FEMP	SOOR	FCN2	FCN1	FCN0
CONTROL FUNCTION (WRITE)	X	AFC2	AFC1	AFC0	$\overline{\text{ENAF}}$	RESET	$\overline{\text{DISO}}$	X	X	X	X	X
RESET STATUS	1	0	0	0	0	0	0	1	0	0	0	0

X = DON'T CARE

Table I. Status/Control Bit Function Description

ORDERING INFORMATION[1]

Signal-to-Noise Ratio	Data Access Time	Temperature Range and Package Options[2]		
		0 to +70°C Plastic DIP (N-28)	−25°C to +85°C Hermetic[3] DIP (Q-28)	−55°C to +125°C Hermetic[3] DIP (Q-28)
70 dB	57 ns	AD7878JN	AD7878AQ	AD7878SQ
72 dB	57 ns	AD7878KN	AD7878BQ	
72 dB	41 ns	AD7878LN		
		PLCC[4] (P-28A)		LCCC[5] (E-28A)
70 dB	57 ns	AD7878JP		AD7878SE
72 dB	57 ns	AD7878KP		
72 dB	41 ns	AD7878LP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact our local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]Analog Devices reserves the right to ship either ceramic (D-28) packages or cerdip (Q-28) hermetic packages.
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier. Available to 883B processing only.

INTERNAL FIFO MEMORY

The internal FIFO memory of the AD7878 consists of eight memory locations. Each word in memory contains 13 bits of information – 12 bits of data from the conversion result and one additional bit which contains information as to whether the 12-bit result is out of range or not. A block diagram of the AD7878 FIFO architecture is shown in Figure 3.

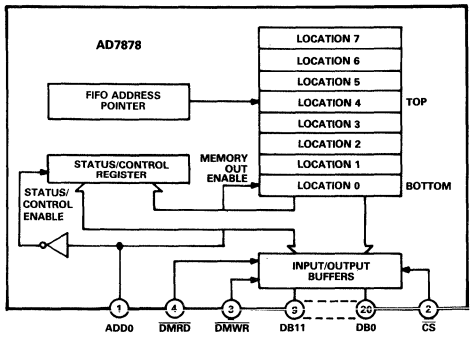


Figure 3. Internal FIFO Architecture

The conversion result is gathered in the successive approximation register (SAR) during conversion. At the end of conversion this result is transferred to the FIFO memory. The FIFO address pointer always points to the top of memory, i.e., the uppermost location which contains valid data. The pointer is incremented after each conversion. A read operation from the FIFO memory accesses data from the bottom of the FIFO, i.e., Location 0. On completion of the read operation each data word moves down one location and the address pointer is decremented by one. Therefore, each conversion result from the SAR enters at the top of memory, propagates down with successive reads until it reaches Location 0 from where it can be accessed by a microprocessor read operation.

The transfer of information from the SAR to the FIFO occurs in synchronization with the AD7878 input clock (CLK IN). The propagation of data words down the FIFO is also synchronous with this clock. As a result, a read operation to obtain data from the FIFO must also be synchronous with CLK IN to avoid Read/Write conflicts in the FIFO (i.e., reading from FIFO Location 0 while it is being updated). This requires that the microprocessor clock and the AD7878 CLK IN are derived from the same source.

INTERNAL COMPARATOR TIMING

The ADC clock, which is applied to CLK IN, controls the successive approximation A/D conversion process. This clock is internally divided by four to yield a bit trial cycle time of 500ns min (CLK IN = 8MHz clock). Each bit decision occurs 25ns after the rising edge of this divided clock. The bit decision is latched by the rising edge of an internal comparator strobe signal. There are 12 bit decisions, as in a normal successive approximation routine, and one extra decision which checks if the input sample is out of range. In a normal successive approximation A/D converter, reading data from the device during conversion can upset the conversion in progress. This is due to on-chip transients, generated by charging or discharging the data bus, concurrent with a bit decision. The scheme outlined below and shown in Figure 4 describes how the AD7878 overcomes this problem.

The internal comparator strobe on the AD7878 is gated with both $\overline{\text{DMRD}}$ and $\overline{\text{DMWR}}$ so that if a read or write operation occurs when a bit decision is about to be made, the bit decision point is deferred by one CLK IN cycle. In other words, if $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ goes low (with $\overline{\text{CS}}$ low) at any time during the CLK IN low-time immediately prior to the comparator strobing edge (t_{LOW} of Figure 4), the bit trial is suspended for a clock cycle. This makes sure that the bit decision is latched at a time when the AD7878 is not attempting to charge or discharge the data bus, thereby ensuring that no spurious transients occur internally near a bit decision point.

The decision point slippage mechanism is shown in Figure 4 for the MSB decision. Normally, the MSB decision occurs 25ns after the fourth rising CLK IN edge after $\overline{\text{CONVST}}$ goes high. However, in the timing diagram of Figure 4, $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ are low in the time period t_{LOW} prior to the MSB decision point on the fourth rising edge. This causes the internal comparator strobe to be slipped to the fifth rising clock edge. The AD7878 will again check during a period t_{LOW} prior to this fifth rising clock edge; and if the $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ or $\overline{\text{DMWR}}$ are still low, the bit decision point will be slipped a further clock cycle.

The conversion time for the ADC normally consists of the 13 bit trials described above and one extra internal clock cycle during which data is written from the SAR to the FIFO. For an 8MHz input clock this results in a conversion time of 7μs. However, the software routine which services the AD7878 has the potential to read 16 times from the device during conversion – 8 reads from the FIFO and 8 reads from the status/control register. It also has the potential to write once to the status/control register. If these 17 (16 read plus 1 write) operations all occur during t_{LOW} time periods, it will cause the conversion time to slip by 17 CLK IN cycles. Therefore, if read or write operations can occur during t_{LOW} periods, it means that the conversion time for the ADC can vary from 7μs to 9.12μs (assuming 8MHz CLK IN). This calculation assumes that there is a slippage of one CLK IN cycle for each read or write operation.

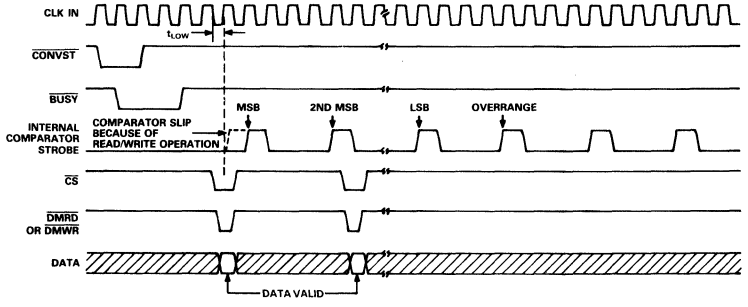


Figure 4. Operational Timing Diagram

INITIATING A CONVERSION

Conversion is initiated on the AD7878 by asserting the $\overline{\text{CONVST}}$ input. This $\overline{\text{CONVST}}$ input is an asynchronous input which is independent of either the ADC or DSP clocks. This is essential for applications where precise sampling in time is important. In these applications the signal sampling must occur at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In these cases the $\overline{\text{CONVST}}$ input is driven from a timer or some precise clock source. On receipt of a $\overline{\text{CONVST}}$ pulse, the AD7878 acknowledges by taking the $\overline{\text{BUSY}}$ output low. This $\overline{\text{BUSY}}$ output can be used to ensure no bus activity while the track/hold goes from track to hold mode (see Extended Read/Write section). The $\overline{\text{CONVST}}$ input must stay low for at least two CLK IN periods. The track/hold amplifier switches from the track to hold mode on the rising edge of $\overline{\text{CONVST}}$ and conversion is also initiated at this point. The $\overline{\text{BUSY}}$ output returns high after the $\overline{\text{CONVST}}$ input goes high and the ADC begins its successive approximation routine. Once conversion has been initiated another conversion start should not be attempted until the full conversion cycle has been completed. Figure 5 shows the timing diagram for the conversion start.

In applications where precise sampling is not critical, the $\overline{\text{CONVST}}$ pulse can be generated from a microprocessor $\overline{\text{WR}}$ or $\overline{\text{RD}}$ line gated with a decoded address (different to the AD7878 $\overline{\text{CS}}$ address). Note that the $\overline{\text{CONVST}}$ pulse width must be a minimum of two AD7878 CLK IN cycles.

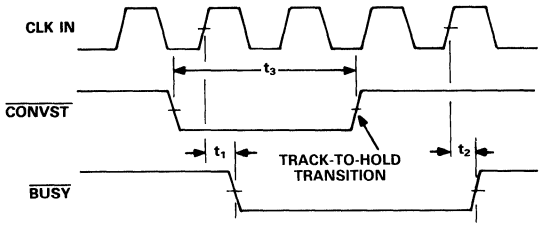


Figure 5. Conversion Start Timing Diagram

READ/WRITE OPERATIONS

The AD7878 read/write operations consist of reading from the FIFO memory and reading and writing from the status/control register. These operations are controlled by the $\overline{\text{CS}}$, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$ and ADD0 logic inputs. A description of these operations is given in the following sections. In addition to the basic read/write operations there is an extended read/write operation. This can occur if a read/write operation occurs during a $\overline{\text{CONVST}}$ pulse. This extended read/write is intended for use with microprocessors which can be driven into a WAIT state and the scheme is recommended for applications where an external timer controls the $\overline{\text{CONVST}}$ input asynchronously to the microprocessor read/write operations.

Basic Read Operation

Figure 6 shows the timing diagram for a basic read operation on the AD7878. $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ going low accesses data from either the status/control register or the FIFO memory. A read operation with ADD0 low accesses data from the FIFO while a read with ADD0 high accesses data from the status/control register.

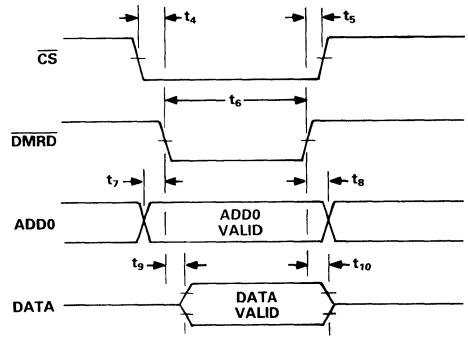


Figure 6. Basic Read Operation

Basic Write Operation

A basic write operation to the AD7878 status/control register consists of bringing $\overline{\text{CS}}$ and $\overline{\text{DMWR}}$ low with ADD0 high. Internally these signals are gated with CLK IN to provide an internal REGISTER ENABLE signal (see Figure 7). The pulse width of this REGISTER ENABLE signal is effectively the overlap between the CLK IN low time and the $\overline{\text{DMWR}}$ pulse. This may result in shorter write pulse widths, data setup times and data hold times than those given by the microprocessor. The timing on the AD7878 timing diagram of Figure 8 is therefore given with respect to the internal REGISTER ENABLE signal rather than the $\overline{\text{DMWR}}$ signal.

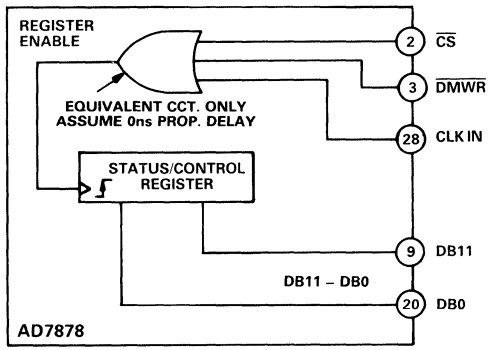
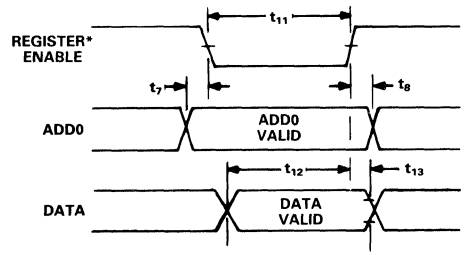


Figure 7. $\overline{\text{DMWR}}$ Internal Logic



*REGISTER ENABLE = $\overline{\text{CS}}$ + $\overline{\text{DMWR}}$ + CLK IN

Figure 8. Basic Write Operation

Extended Read/Write Operation

As described earlier, a read/write operation to the AD7878 can cause spurious on-chip transients. Should these transients occur while the track/hold is going from track to hold mode it may result in an incorrect value of V_{IN} being held by the track/hold amplifier. Because the $\overline{CONVST}$ input has asynchronous capability, a read/write operation could occur while $\overline{CONVST}$ is low. The AD7878 allows the read/write operation to occur but has the facility to disable its three-state drivers so that there is no data bus activity and hence no transients while the track/hold goes from track to hold.

Writing a logic 0 to DB5 ($\overline{DISO}$) of the status/control register prevents the output latches from being enabled while the AD7878 $\overline{BUSY}$ signal is low. If a microprocessor read/write operation can occur during the $\overline{BUSY}$ low time, the $\overline{BUSY}$ should be gated with $\overline{CS}$ of the AD7878 and this gated signal used to stretch the instruction cycle using DMACK (ADSP-2100), READY (TMS32020) or $\overline{DTACK}$ (68000).

When $\overline{CONVST}$ goes low the AD7878 acknowledges by bringing $\overline{BUSY}$ low on the next rising edge of CLK IN. With a logic 0 in DB5, the AD7878 data bus cannot now be enabled. If a read/write operation now occurs, the $\overline{BUSY}$ and $\overline{CS}$ gated signal drives the microprocessor into a WAIT state, thereby extending the read/write operation. $\overline{BUSY}$ goes high on the second rising edge of CLK IN after $\overline{CONVST}$ goes high. The AD7878 data outputs are now enabled and the microprocessor is released from its WAIT state, allowing it to complete its read/write operation to the AD7878.

The microprocessor cycle time for the read/write operation is extended by the $\overline{CONVST}$ pulse width plus two CLK IN periods worst case. This is the maximum length of time for which $\overline{BUSY}$ can be low. Assuming a $\overline{CONVST}$ pulse width of two CLK IN periods and an 8MHz CLK IN, the instruction cycle is extended by 500ns maximum. Figure 9 shows the timing diagram for an extended read operation. In a similar manner, a write operation will be extended if it occurs during a $\overline{CONVST}$ pulse.

For processors which cannot be forced into a WAIT state, writing a logic 1 into DB5 of the status/control register allows the output latches to be enabled while $\overline{BUSY}$ is low. In this case $\overline{BUSY}$ still goes low as before, but it would not be used to stretch the read/write cycle and the instruction cycle continues as normal (see Figures 6 and 8).

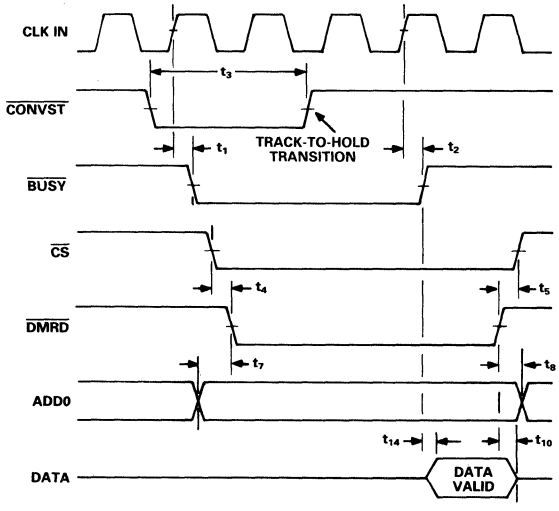


Figure 9. Extended Read Operation

AD7878 DYNAMIC SPECIFICATIONS

The AD7878 is specified and 100% tested for dynamic performance specifications rather than traditional dc specifications such as Integral and Differential Nonlinearity. These ac specifications provide information on the AD7878's effect on the spectral content of the input signal. Hence the parameters for which the AD7878 is specified include SNR, Harmonic Distortion, Intermodulation Distortion and Peak Harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals (excluding dc) up to half the sampling frequency (fs/2). SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)dB \quad \ldots\ldots (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74dB.

The output spectrum from the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input which is sampled at a 100kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 10 shows a typical 2048 point FFT plot of the AD7878KN with an input signal of 25kHz and a sampling frequency of 100kHz. The SNR obtained from this graph is 72.6dB. It should be noted that the harmonics are included in the SNR calculation.

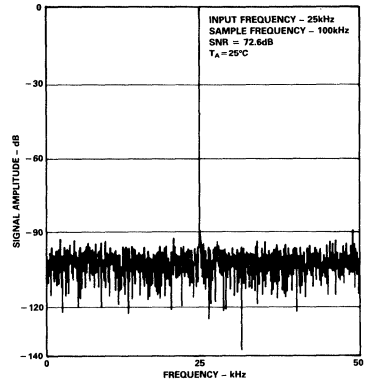


Figure 10. AD7878 FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to get a measure of performance expressed in effective number of bits (N). The effective number of bits for a device can be calculated directly from its measured SNR.

$$N = \frac{SNR - 1.76}{6.02} \quad \ldots (2)$$

Figure 11 shows a typical plot of effective number of bits versus frequency for an AD7878KN with a sampling frequency of 100kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 and 73.1dB.

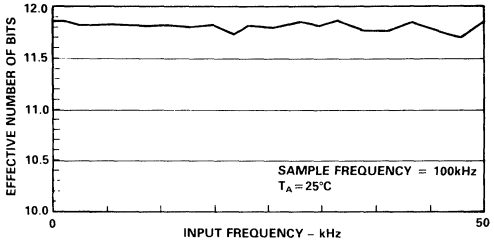


Figure 11. Effective Number of Bits vs. Frequency

Harmonic Distortion

Harmonic Distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7878, Total Harmonic Distortion (THD) is defined as:

$$THD = 20 \text{ Log } \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second to the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m,n = 0,1,2,3 . . . , etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb) while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

Using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Intermodulation distortion is calculated using an FFT algorithm but in this case the input consists of two equal amplitude, low distortion sine waves. Figure 12 shows a typical IMD plot for the AD7878.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fs/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the largest peak will be a noise peak.

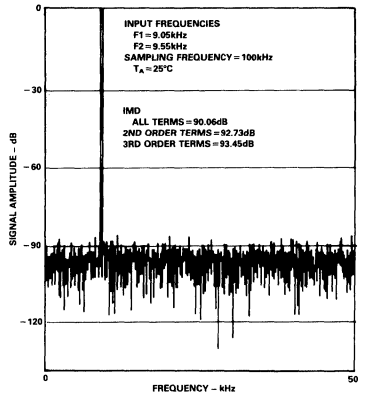


Figure 12. AD7878 IMD Plot

Histogram Plot

When a sine wave of a specified frequency is applied to the V_{IN} input of the AD7878 and several million samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 4096 ADC codes. If a particular step is wider than the ideal 1LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than ideal will have fewer counts. Missing codes are easily seen in the histogram plot because a missing code means zero counts for a particular code. Large spikes in the plot indicate large differential nonlinearity.

Figure 13 shows a histogram plot for the AD7878KN with a sampling frequency of 100kHz and an input frequency of 25kHz. For a sine-wave input, a perfect ADC would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi\sqrt{(A^2 - V^2)}}$$

where A is the peak amplitude of the sine wave and p(V) the probability of occurrence at a voltage V. The histogram plot of Figure 13 corresponds very well with this cusp shape. The absence of large spikes in this plot indicates small dynamic differential nonlinearity (the largest spike in the plot represents less than 1/4 LSB of DNL error). The AD7878 has no missing codes under these conditions since no code records zero counts.

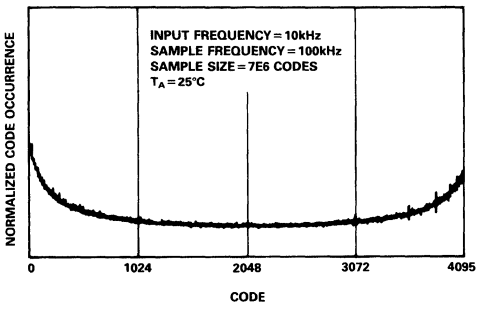


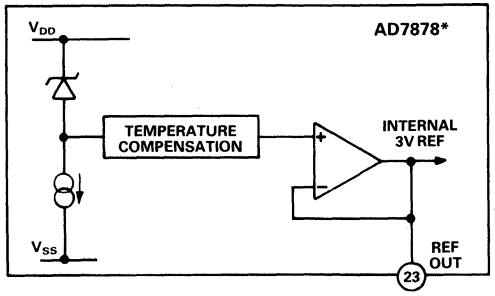
Figure 13. AD7878 Histogram Plot

CONVERSION TIMING

The track-and-hold on the AD7878 goes from track to hold mode on the rising edge of $\overline{CONVST}$ and the value of V_{IN} at this point is the value which will be converted. However, the conversion actually starts on the next rising edge of CLK IN after $\overline{CONVST}$ goes high. If $\overline{CONVST}$ goes high within approximately 30ns prior to a rising edge of CLK IN, that CLK IN edge will not be seen as the first CLK IN edge of the conversion process, and conversion will not actually start until one CLK IN cycle later. As a result, the conversion time (from $\overline{CONVST}$ to FIFO update) will vary by one clock cycle depending on the relationship between $\overline{CONVST}$ and CLK IN. A conversion cycle normally consists of 56 CLK IN cycles (assuming no read/write operations) which corresponds to a 7μs conversion time. If $\overline{CONVST}$ goes high within 30ns prior to a rising edge of CLK IN, the conversion time will consist of 57 CLK IN cycles, i.e., 7.125μs. This effect does not cause track/hold jitter.

INTERNAL REFERENCE

The AD7878 has an on-chip temperature compensated buried Zener reference (see Figure 14) which is factory trimmed to 3V ± 1%. Internally it provides both the DAC reference and the dc bias required for bipolar operation. The reference output is available (REF OUT) and is capable of providing up to 500μA to an external load.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 14. AD7878 Reference Circuit

The maximum recommended capacitance on REF OUT for normal operation is 50pF. If the reference is required for use external to the AD7878 it should be decoupled with a 200Ω resistor in series with a parallel combination of a 10μF tantalum capacitor and a 0.1μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the AD7878's internal operation.

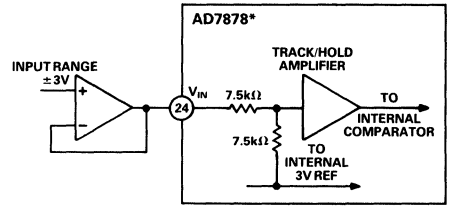
TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7878 allows the ADC to accurately convert an input sine wave of 6V peak-peak amplitude to 12-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when operated at its minimum conversion time. The 0.1dB cutoff frequency occurs typically at 500kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2μs.

The operation of the track/hold amplifier is transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion on the rising edge of $\overline{CONVST}$ and returns to track mode at the end of conversion.

ANALOG INPUT

Figure 15 shows the AD7878 analog input. The analog input range is ±3V into an input resistance of typically 15kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, 5/2LSBs . . . . FS − 3/2LSBs). The output code is 2s complement binary with 1LSB = FS/4096 = 6V/4096 = 1.46mV. The ideal input/output transfer function is shown in Figure 16.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 15. AD7878 Analog Input

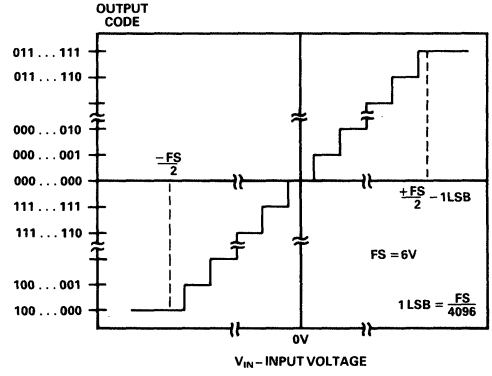


Figure 16. Input/Output Transfer Function

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications offset and full-scale error have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications may require that the input signal span the full analog input dynamic range and accordingly offset and full-scale error will have to be adjusted to zero.

Where adjustment is required offset must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7878 while the input voltage is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of −0.73mV (−1/2 LSB) at V_1 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000.

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows:

Positive Full-Scale Adjust

Apply a voltage of 2.9978V (FS/2 − 3/2LSBs) at V_1. Adjust R2

until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust

Apply a voltage of −2.9993V (−FS/2 + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

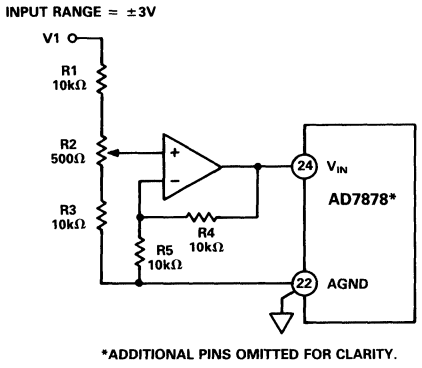


Figure 17. AD7878 Full-Scale Adjust Circuit

MICROPROCESSOR INTERFACING

The AD7878 high speed bus timing allows direct interfacing to DSP processors. Due to the complexity of the AD7878 internal logic, only synchronous interfacing is allowed. This means that the ADC clock must be the same as or a derivative of the processor clock. Suitable processor interfaces are shown in Figures 18 to 21.

AD7878 – ADSP-2100/TMS32010/TMS32020

All three interfaces use an external timer for conversion control. This allows the ADC to sample the analog input asynchronously to the microprocessor. The AD7878 $\overline{ALFL}$ output interrupts the processor when the FIFO preprogrammed word count is reached. The processor then reads the conversion results from the AD7878 internal FIFO memory.

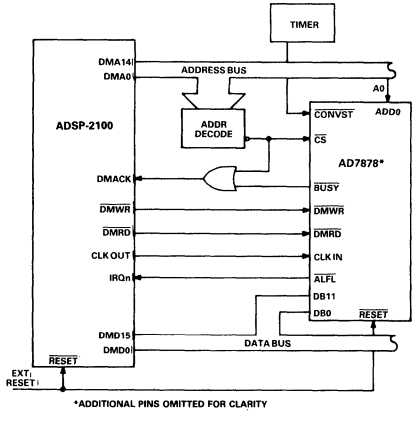


Figure 18. AD7878–ADSP-2100 Interface

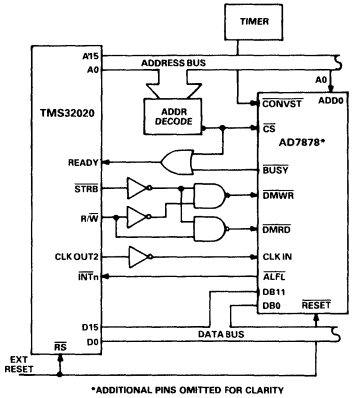


Figure 19. AD7878 – TMS32020 Interface

The interfaces to the ADSP-2100 and the TMS32020 gate the AD7878 $\overline{CS}$ and the $\overline{BUSY}$ to provide a signal which drives the processor into a wait state if a read/write operation to the ADC is attempted while the ADC track/hold amplifier is going from the track to the hold mode. This avoids digital feedthrough to the analog circuitry. The TMS32020 does not have separate $\overline{RD}$ and $\overline{WR}$ outputs to drive the AD7878 $\overline{DMWR}$ and $\overline{DMRD}$ inputs. These are generated from the processor $\overline{STRB}$ and R/$\overline{W}$ outputs with the addition of some logic gates.

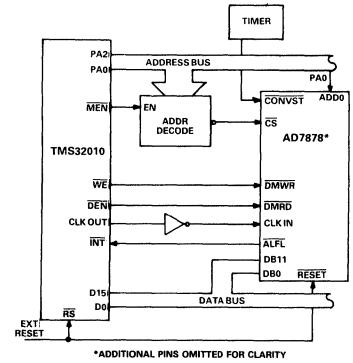


Figure 20. AD7878 – TMS32010 Interface

AD7878 – MC68000

This interface also uses an external timer for conversion control as described for the previous three interfaces. It is discussed separately because it needs extra logic due to the nature of its interrupts. The MC68000 has eight levels of external interrupt. When interrupting this processor one of these levels (0 to 7) has to be encoded onto the $\overline{IPL2}$ – $\overline{IPL0}$ inputs. This is achieved with a 74148 encoder in Figure 21, (interrupt Level 1 is taken for example purposes only). The MC68000 places this interrupt level on address bits A3 to A1 at the start of the interrupt service routine. Additional logic is used to decode this interrupt level on the address bus and the FC2 – FC0 outputs to generate a $\overline{VPA}$ signal for the MC68000. This results in an autovectored interrupt, the start address for the service routine must be loaded into the appropriate auto vector location during initialization. For further information on the 68000 interrupts consult the 68000 users manual.

The MC68000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate separate $\overline{DMWR}$ and $\overline{DMRD}$ inputs for the AD7878. As with the previous three interfaces described earlier, WAIT states are inserted if a read/write operation is attempted while the track/hold amplifier is going from the track to the hold mode.

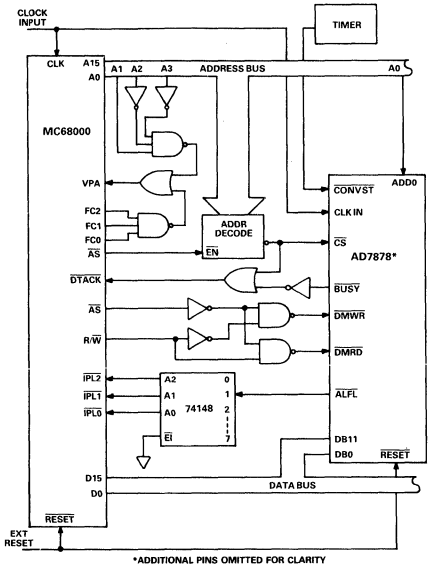


Figure 21. AD7878 – MC68000 Interface

Typical AD7878 Microprocessor Operating Sequence

After power up or reset the status/control register is initialized by writing to the AD7878. This enables the $\overline{ALFL}$ output if required for a microprocessor interrupt and sets the effective word length of the FIFO memory. The processor now executes the main body of the program while waiting for an ADC interrupt. This interrupt will occur when the preprogrammed number of samples are collected in the FIFO memory. The interrupt service routine first interrogates DB5(FOOR) of the status/control register to determine if any sample in the FIFO memory is out of range. If all data samples are valid then the program proceeds to read the FIFO memory. If, on the other hand, at least one sample is out of range then an overrange routine is called.

There are many actions which can be taken by the out of range routine, the selection of which is application dependent. One option is to ignore all the current samples residing in the FIFO memory, reinitialize the status/control register and return to the main body of the program. Another option is to check the individual out of range status of each word in the FIFO memory and discard the invalid ones. The underrange or overrange status of each word can also be determined and the analog input adjusted accordingly before returning to the main program.

Note there is no need to check the out of range status if the analog input is always assured to be within range.

THROUGHPUT RATE

The AD7878 has a maximum specified throughput rate (sample rate) of 100kHz. This is a worst case test condition and specifications apply for reduced sampling rates provided the Nyquist criterion is obeyed. The throughput rate must take into account ADC $\overline{CONVST}$ pulse width, ADC conversion time and the track/hold amplifier acquisition time. The time required for each of these tasks is shown in Table II for a selection of DSP processors. Since the ADC clock has to be synchronized to the microprocessor clock, the conversion time depends on the microprocessor used. In addition, time must be allowed for reading data from the AD7878. If this task is performed during the track/hold amplifier acquisition period then it does not impact on the overall throughput rate. However, if the read operations occur during a conversion, then they may stretch the conversion time and reduce the track/hold amplifier acquisition time. The track/hold amplifier requires a minimum of 2μs to operate to specification. The time required to read from the AD7878 depends on the number of FIFO memory locations to be read and the software organization.

As an example, consider an application using the ADSP-2100 and the AD7878 with a throughput rate of 100kHz. The time required for the $\overline{CONVST}$ pulse and the ADC conversion is 7.375μs. This leaves 2.625μs for the track/hold acquisition time and for reading the ADC (both operations occurring in parallel). The ADSP-2100, when operating from a 32MHz clock, has an instruction cycle of 125ns and an interrupt response time of 500ns. This allows adequate time to perform 16 read operations within the time budget allowed.

	$\overline{CONVST}$ Pulse Width	Conversion Time	T/H Acquisition Time
Number of Clock Cycles	2 min	57 max	Non-Applicable
ADSP-2100[1]	250ns min	7.125μs max	2μs min
TMS32010[2]	400ns min	11.14μs max	2μs min
TMS32020[2]	400ns min	11.14μs max	2μs min

NOTES
[1]ADSP-2100 Clock Freq. = 32MHz
[2]TMS320XX Clock Freq. = 20MHz

Table II. AD7878 Throughput Rate

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high speed A/D performance. The AD7878 is required to make bit decisions on an LSB size of 1.465mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 22 (AGND) or as close as possible to the AD7878 as shown in Figure 22. Connect all other grounds and Pin 7 (AD7878 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout of Figures 25 and 26 have both analog and digital ground planes which are kept separated and only joined together at the AD7878 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND (Pin 22) as short as possible to minimize input noise coupling. In applications where this is not possible use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

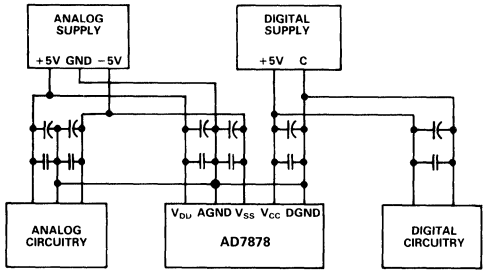


Figure 22. Power Supply Grounding Practice

DATA ACQUISITION BOARD

Figure 23 shows the AD7878 in a data acquisition circuit which will interface directly to either the ADSP-2100, TMS32010 or the TMS32020. The corresponding printed circuit board (PCB) layout and silkscreen are shown in Figures 24 to 26.

The only additional component required for a full data acquisition system is an antialiasing filter. There is a component grid provided near the analog input on the PCB which may be used for such a filter or any other conditioning circuitry. To facilitate this option, a wire link (labelled LK1 on the PCB) is required on the analog input track. This link connects the input signal to either the component grid or directly to the buffer amplifier driving the AD7878 analog input.

Microprocessor connections to the PCB can be made by either of two ways:

1. 96-contact (3 ROW) Eurocard connector.
2. 26-contact (2 ROW) IDC connector.

The 96-contact Eurocard connector is directly compatible with the ADSP-2100 Evaluation Board Prototype Expansion Connector. The expansion connector on the ADSP-2100 has eight decoded chip enable outputs labelled $\overline{ECE8}$ to $\overline{ECE1}$. $\overline{ECE6}$ is used to drive the AD7878 $\overline{CS}$ input on the data acquisition board. To avoid selecting onboard RAM sockets at the same time, LK6 on the ADSP-2100 board must be removed. In addition, the expansion connector on the ADSP-2100 has four interrupts labelled $\overline{EIRQ3}$ to $\overline{EIRQ0}$. The AD7878 $\overline{ALFL}$ output connects to $\overline{EIRQ0}$. The AD7878 and ADSP-2100 data lines are aligned for left justified data transfer.

The 26-way IDC connector contains all the necessary contacts for both the TMS32010 and TMS32020. There are two switches on the data acquisition board that must be set to enable the appropriate interface configuration (see Table III). The interface connections for the TMS32010/32020 and IDC signal contact numbers are shown in Table IV and Figure 23. Note the AD7878 $\overline{CS}$ input must be decoded from the address bus prior to the AD7878 evaluation board for the TMS320XX interfaces.

Connections to the analog input (V_{IN}) and the $\overline{CONVST}$ input are via two BNC sockets labelled SKT1 and SKT2 on the silkscreen. If the $\overline{CONVST}$ input is derived from either the microprocessor or ADC clock, the effects of clock noise coupling will be reduced.

SWITCH SETTING

Microprocessor	SW1	SW2
ADSP-2100	A	A
TMS32010	B	A
TMS32020	B	B

Table III. AD7878 PCB Switch Settings

POWER SUPPLY CONNECTIONS

The PCB requires two analog supplies and one 5V digital supply. Connections to the analog supplies are made directly to the PCB as shown on the silk screen in Figure 24. The connections are labelled V+ and V− and the range for both of these supplies is 12V to 15V. Connection to the 5V digital supply is made through either of the two microprocessor connectors. The +5V and −5V analog power supplies required by the AD7878 are generated from two voltage regulators on the V+ and V− power supply inputs (IC3 and IC4 in Figure 23).

COMPONENT LIST

IC1	AD711 Op Amp
IC2	AD7878 Analog-to-Digital Converter
IC3	MC78L05 5V Regulator
IC4	MC79L05 −5V Regulator
IC5*	74HC00 Quad NAND Gate
IC6*	74HC04 Hex Inverter
IC7	74HC02 Quad NOR Gate
SW1	Single Pole Double Throw
SW2	Double Pole Double Throw
LK1	Wire Link for Analog Input
C1, C3, C5, C7, C9 C11, C13, C15	10μF Capacitors
C2, C4, C6, C8, C10 C12, C14, C16	0.1μF Capacitors
R1*, R2*	10kΩ Resistors
SKT1, SKT2	BNC Sockets
SKT3	26-Contact (2 Row) IDC Connector
SKT4	96-Contact (3 Row) Eurocard Connector

*Not required for ADSP-2100 Interface

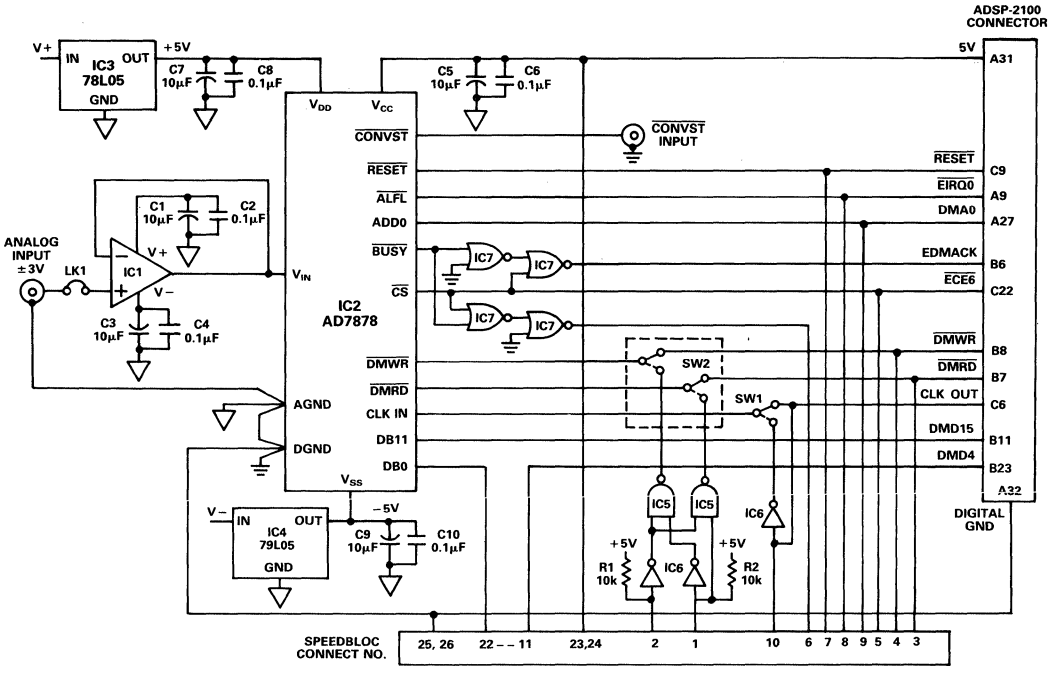


Figure 23. Data Acquisition Circuit Using the AD7878

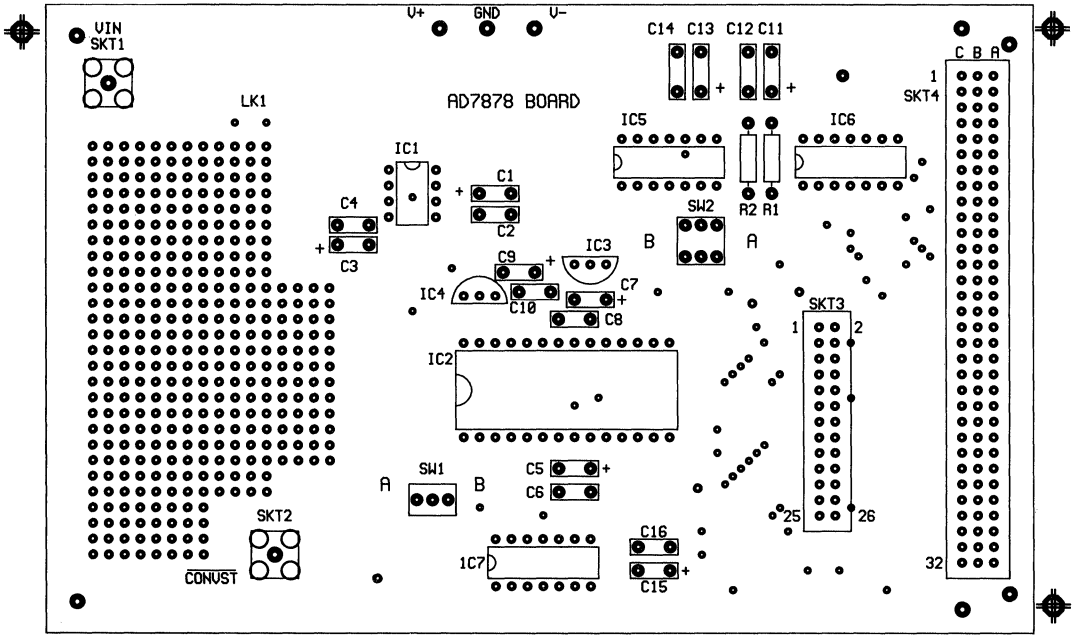


Figure 24. PCB Silkscreen for Figure 23

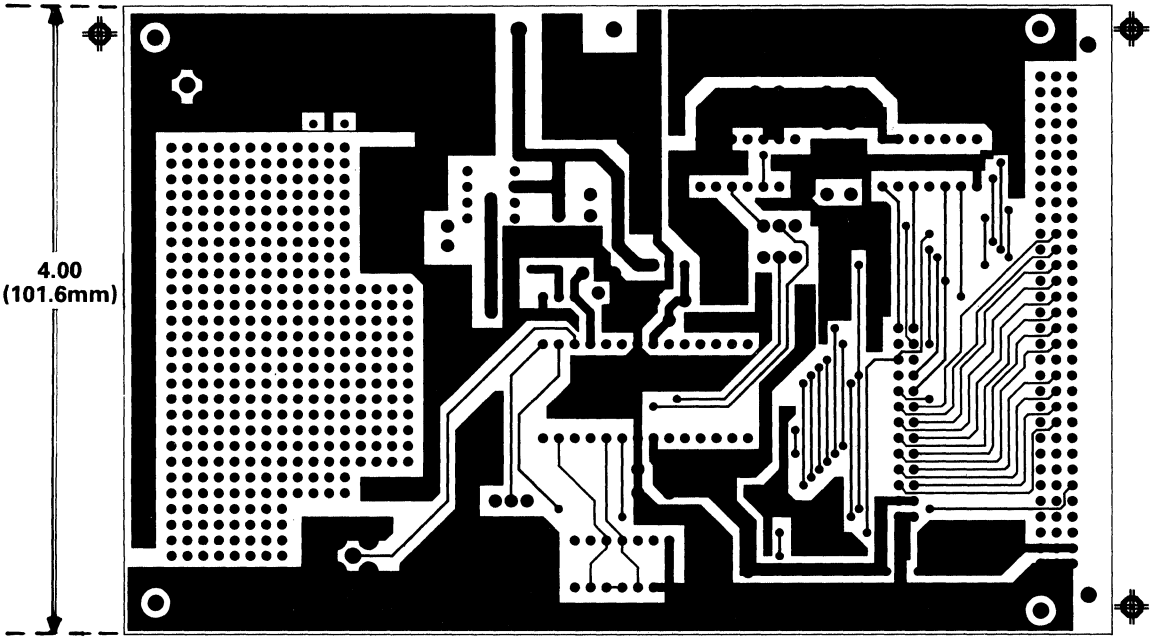


Figure 25. PCB Component Side Layout for Figure 23

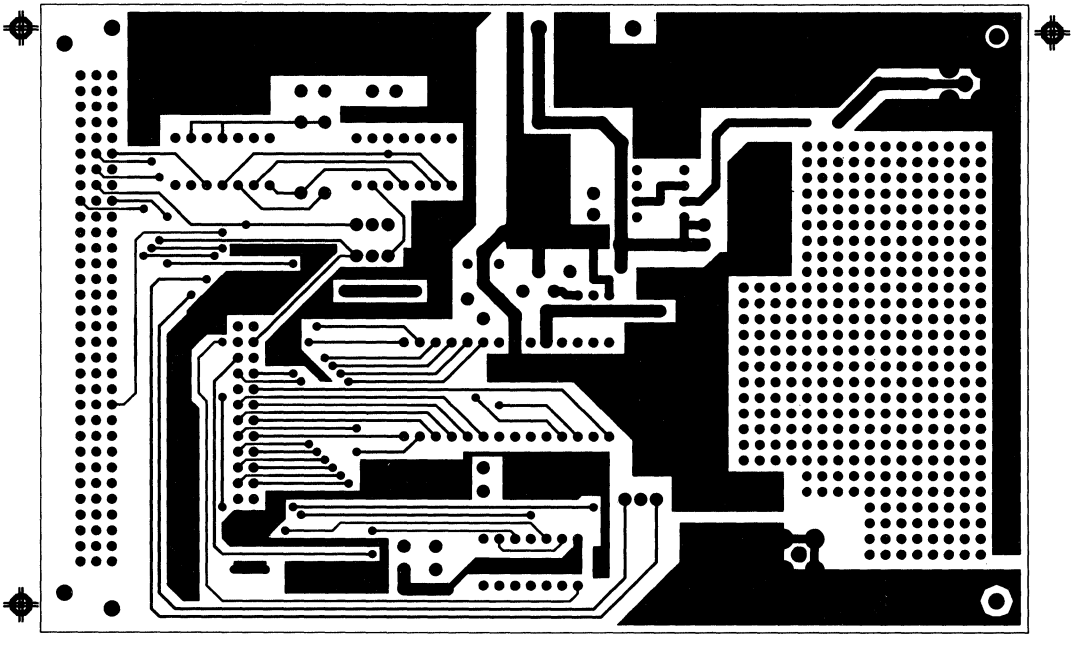


Figure 26. PCB Solder Side Layout for Figure 23

IDC Contact No.	Signal Connect Mnemonic	TMS32010 Signal	TMS32020 Signal
1	R/$\overline{W}$	–	R/$\overline{W}$
2	$\overline{STRB}$	–	$\overline{STRB}$
3	$\overline{DMRD}$	$\overline{DEN}$	–
4	$\overline{DMWR}$	$\overline{WE}$	–
5	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$
6	READY	–	READY
7	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$
8	$\overline{ALFL}$	$\overline{INT}$	$\overline{INT}$
9	ADD0	PA0	A0
10	CLK	CLKOUT	CLKOUT2
11	DB10	D10	D10
12	DB11	D11	D11
13	DB8	D8	D8
14	DB9	D9	D9
15	DB6	D6	D6
16	DB7	D7	D7
17	DB4	D4	D4
18	DB5	D5	D5
19	DB2	D2	D2
20	DB3	D3	D3
21	DB0	D0	D0
22	DB1	D1	D1
23	5V	5V	5V
24	5V	5V	5V
25	GND	GND	GND
26	GND	GND	GND

Table IV. TMS32010/TMS32020 Interface Connections

ANALOG DEVICES

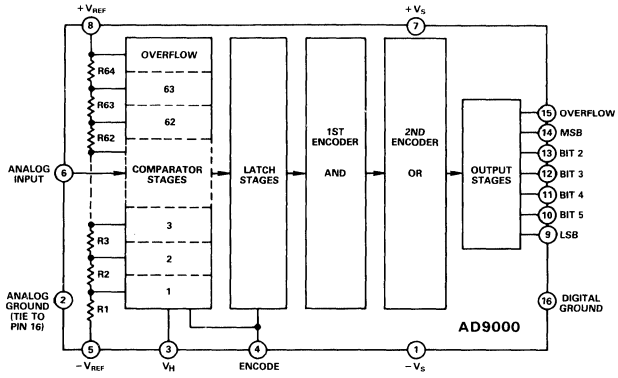
High-Speed 6-Bit A/D Converter

AD9000

FEATURES
77MSPS Encode Rate
Bipolar Input Range
Low Error Rate
Overflow Bit

APPLICATIONS
QAM Telecommunications
Electronic Warfare (ECM, ECCM, ESM)
Radar Guidance Digitizers

AD9000 FUNCTIONAL BLOCK DIAGRAM



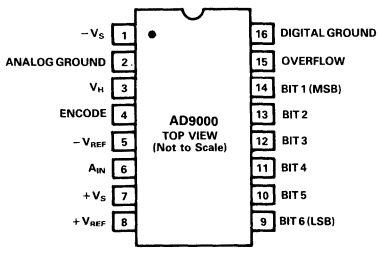
GENERAL DESCRIPTION

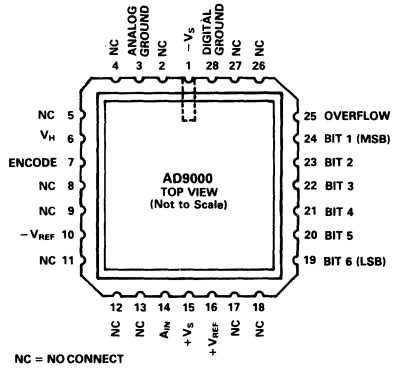
The AD9000 is a 6-bit, high-speed, analog-to-digital converter with ECL compatible outputs and a bipolar input stage. The AD9000 is fabricated in a high-performance bipolar process which allows encode rates up to 77MSPS.

The AD9000 employs the standard flash converter architecture based on 64 individual comparators which simultaneously determine the precise analog signal level. The comparators are followed by two stages of decoding logic, allowing the AD9000 to operate with a very low error rate. The low 35pF input capacitance of the AD9000 greatly simplifies the analog driver stage. Also incorporated into the AD9000 design is an overflow output bit as well as a hysteresis control pin to modify comparator sensitivity.

The AD9000 is offered as both an commercial temperature range device 0 to +70°C, and as an extended temperature range device −55°C to +125°C. Both versions are available packaged in a 16-pin ceramic DIP. The extended temperature range device is also available in a 28-pin ceramic LCC package. The extended temperature range versions are offered as fully compliant MIL-STD-883B devices.

PIN DESIGNATIONS





NC = NO CONNECT

ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9000JD	0 to +70°C	16-Pin DIP, Industrial	D-16
AD9000SD/883C	−55°C to +125°C	16-Pin DIP, MIL-STD-883B, REV. C	D-16
AD9000SE/883C	−55°C to +125°C	28-Pin LCC, MIL-STD-883B, REV. C	E-28A

*See Section 14 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage . . . . . −0.3V to +6V
Negative Supply Voltage . . . . . −6.0V to +0.3V
Analog-to-Digital Ground Voltage Differential 0.5
Analog Input Voltages (A_{IN}, $+V_{REF}$, $-V_{REF}$)[2] . . . . . ±3V
Differential Reference Voltage ($+V_{REF}$ to $-V_{REF}$)[3] 6V
ENCODE Input Voltage . . . . . $-V_S$ to 0V
HYSTERESIS Control Voltage . . . . . 0V to +3.0V
Digital Output Current 20mA

Power Dissipation (+25°C Free Air)[4] 745mW
Operating Temperature Range
AD9000JD . . . . . 0 to +70°C
AD9000SD/SE/883C . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS

(Supply Voltages = −5.2V and +5.0V; Differential Reference Voltage = 2.0V unless otherwise stated)

Parameter	Sub-Group[5]	Temp	AD9000JD Min	AD9000JD Typ	AD9000JD Max	AD9000SD/SE/883B Min	AD9000SD/SE/883B Typ	AD9000SD/SE/883B Max	Units
RESOLUTION			6			6			Bits
DC ACCURACY									
Differential Linearity	7	+25°C		0.25	0.5		0.25	0.5	LSB
	8	Full			1.0			1.0	LSB
Integral Linearity	7	+25°C		0.25	0.5		0.25	0.5	LSB
	8	Full			1.0			1.0	LSB
No Missing Codes	7,8	Full		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR									
Top of Reference Ladder	7	+25°C		0.3	7/8		0.3	7/8	LSB
	8	Full			1.5			1.5	LSB
Bottom of Reference Ladder	7	+25°C		0.25	7/8		0.25	7/8	LSB
	8	Full			1.5			1.5	LSB
Offset Drift Coefficient		Full		145			145		µV/°C
ANALOG INPUT									
Input Voltage Range		Full		±2.0V			±2.0V		V
Input Bias Current (Sampling)[6]	1,2,3	Full			800			800	µA
Input Bias Current (Latched)[6]	1,2,3	Full			20			20	µA
Input Resistance		+25°C		3.0			3.0		kΩ
Input Capacitance	12	+25°C		35	50		35	50	pF
Full Power Bandwidth[7]		+25°C		20			20		MHz
REFERENCE INPUT[2,3]									
Reference Ladder Resistance	1	+25°C	80		200	80		200	Ω
Ladder Temperature Coefficient		Full		0.275			0.275		Ω/°C
Reference Input Bandwidth		+25°C		20			20		MHz
DYNAMIC PERFORMANCE[8]									
Conversion Rate	4	+25°C	50	70		75	77		MHz
Conversion Time (+1 Clock)	4	+25°C			20			13.3	ns
Aperture Delay (t_D)		+25°C		2			2		ns
Aperture Uncertainty (Jitter)		+25°C		25			25		ps
Output Propagation Delay (t_{PD})[9]	9	+25°C	8		12	8		12	ns
Output Hold Time (t_{OH})[10]	9	+25°C	8		14	8		14	ns
Transient Response[11]		+25°C		13			13		ns
Overvoltage Recovery Time[12]		+25°C		11			11		ns
Output Rise Time[13]	9	+25°C			5.0			4.5	ns
Output Fall Time[13]	9	+25°C			5.0			4.5	ns
Output Time Skew		+25°C		0.4			0.4		ns

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Sub-Group[5]	Temp	AD9000JD Min	AD9000JD Typ	AD9000JD Max	AD9000SD/SE/883B Min	AD9000SD/SE/883B Typ	AD9000SD/SE/883B Max	Units
ENCODE INPUT									
Logic "1" Voltage	7,8	Full	−1.1			−1.1			V
Logic "0" Voltage	7,8	Full			−1.5			−1.5	V
Logic "1" Current	7,8	Full			100			100	μA
Logic "0" Current	7,8	Full			100			100	μA
Input Capacitance	12	+25°C		2.5	5.0		2.5	5.0	pF
ENCODE Pulse Width High (t_{PWH})	4	+25°C	6.6			6.6			ns
ENCODE Pulse Width Low (t_{PWL})	4	+25°C	6.6			6.6			ns
AC LINEARITY[14]									
Dynamic Linearity[15]		+25°C		0.5			0.5		LSB
In-Band Harmonics									
(DC to 1MHz)		+25°C		44			44		dBc
(1MHz to 5MHz)		+25°C		42			42		dBc
(5MHz to 8MHz)		+25°C		38			38		dBc
Signal to Noise Ratio[16]	12	+25°C	31	33		31	33		dB
Signal to Noise Ratio[17]	12	+25°C	40	42		40	42		dB
Two Tone Intermodulation Rejection[18]		+25°C		46			46		dBc
Noise Power Ratio (NPR)[19]		+25°C		30			30		dBc
DIGITAL OUTPUTS[8]									
Logic "1" Voltage	1,2,3	Full	−1.1			−1.1			V
Logic "0" Voltage	1,2,3	Full			−1.5			−1.5	V
POWER SUPPLY[20]									
Positive Supply Current (+5.0V)	1	+25°C		60	70		60	70	mA
	2,3	Full			75			75	mA
Negative Supply Current (−5.2V)	1	+25°C		68	80		68	80	mA
	2,3	Full			85			85	mA
Nominal Power Dissipation		+25°C		675			675		mW
Reference Ladder Dissipation		+25°C		20			20		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Under normal operating conditions, the analog input voltages should not exceed nominal ±2V operating range, nor the supply voltages ($+V_S$ and $-V_S$), whichever is smaller.

[3]Under normal operating conditions the differential reference voltage may range from ±0.5V to ±2V; $+V_{REF} \geq -V_{REF}$.

[4]Typical thermal impedances . . .

16-Pin Ceramic $\theta_{ja} = 67°C/W$; $\theta_{jc} = 7°C/W$

28-Pin LCC $\theta_{ja} = 62°C/W$; $\theta_{jc} = 14°C/W$

[5]Subgroups apply to military qualified devices only.

[6]$A_{IN} = +V_{REF}$.

[7]Determined by 3dB reduction in reconstructed output at 75MSPS.

[8]Output terminated with 100Ω resistors to −2.0V.

[9]Measured from the leading edge of ENCODE to data out on Bit 1 (MSB).

[10]Measured from the trailing edge of ENCODE to data out on Bit 1 (MSB).

[11]For full-scale step input, 6-bit accuracy is attained in specified time.

[12]Recovers to 6-bit accuracy in specified time, after 150% full-scale input overvoltage.

[13]Measured on Bit 1 (MSB) only.

[14]Measured at 50MSPS encode rate.

[15]Analog input frequency = 15MHz.

[16]RMS signal to RMS noise, with 540kHz analog input signal.

[17]Peak-to-peak signal to rms noise, with 540kHz analog input signal.

[18]$F_1 = 9.3$MHz; $f_2 = 7.6$MHz; Encode = 42MHz.

[19]DC to 8.2MHz noise bandwidth with 3.886MHz slot.

[20]Supply voltage should remain stable within ±5% for normal operation.

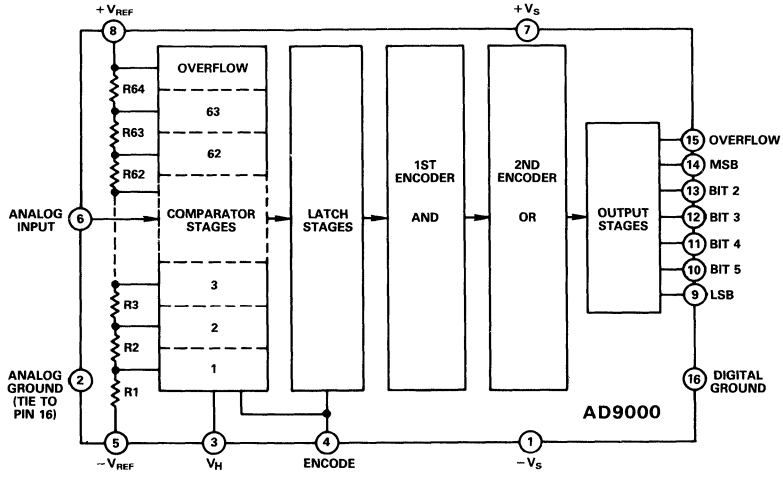
Specifications subject to change without notice.

EXPLANATION OF SUBGROUPS

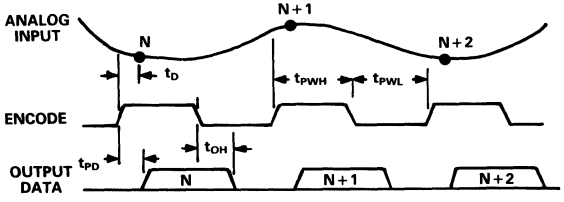
Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
$-V_S$	Negative supply terminal, nominally $-5.2V$.
ANALOG GROUND	Analog ground return. All grounds should be connected together near the the AD9000.
$V_{HYSTERESIS}$	The hysteresis control voltage varies the comparator hysteresis from 15mV to 50mV, for a change of 0V to $+3V$ at the hysteresis control pin.
ENCODE	The ENCODE pin controls the conversion cycle. Encode is rising edge sensitive and should be driven with a 50% duty-cycle waveform under normal conditions.
$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
ANALOG INPUT	Analog input pin.
$+V_S$	Positive supply terminal, nominally $+5.0V$.
$+V_{REF}$	Most positive reference voltage of the internal resistor ladder.
BIT 6 (LSB)	One of six digital outputs. BIT 6 (LSB) is the least-significant-bit of the digital output.
BIT 5 – BIT 2	One of six digital outputs.
BIT 1 (MSB)	One of six digital outputs. BIT1 (MSB) is the most-significant-bit of the digital output.
OVERFLOW	Overflow data output. Logic high indicates an input overvoltage ($A_{IN} \geq +V_{REF}$).
DIGITAL GROUND	Digital ground return. All grounds should be connected together near the AD9000.



AD9000 Functional Block Diagram



t_D APERTURE DELAY
t_{PD} OUTPUT PROPAGATION DELAY
t_{OH} MINIMUM OUTPUT HOLD TIME
t_{PWH} MINIMUM ENCODE PULSE WIDTH HIGH
t_{PWL} MINIMUM ENCODE PULSE WIDTH LOW

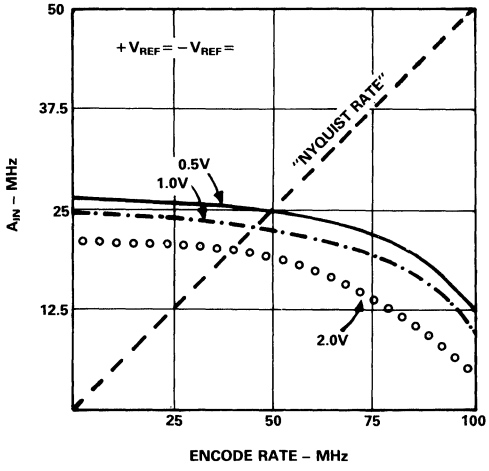
System Timing Diagram

ABOUT THE AD9000

Analog Bandwidth

Quantifying the high-frequency analog performance of the AD9000 is somewhat difficult because of the various criteria that can be applied. At one extreme there is the analog input bandwidth of a single input comparator (which tends to be extremely high). At the other end of the performance criteria is the "no missing codes" restriction, which tends to be the most conservative measure of analog bandwidth.

The "no missing codes" criteria simply means that the converter is capable of generating all 64 output codes for an analog and ENCODE frequency. At higher ENCODE rates to analog frequencies, the converter continues to function, but with reduced resolution. The graph below details the "no missing codes" region of operation for the AD9000 at several reference levels. Note that nearly all analog-to-digital converter applications operate in the oversampled region to avoid generation of indeterminate data (aliasing).

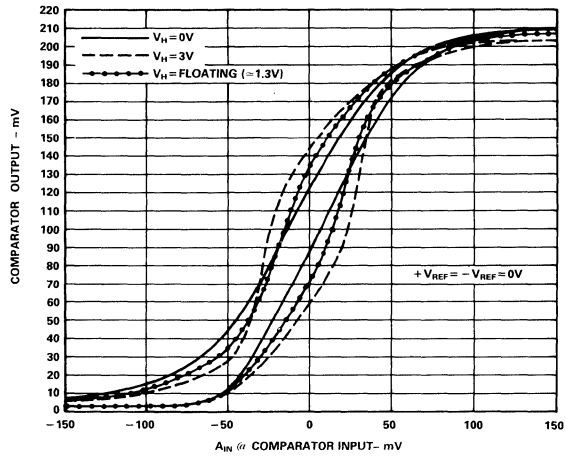


Analog Input vs. Encode Rate "No Missing Codes"

High-Speed Performance Enhancements

The AD9000 employs a hysteresis control pin which affects comparator sensitivity. The error rate (number of full-scale errors in a given period) is directly affected by the comparator sensitivity. By varying the voltage on the hysteresis control pin, the error rate can be reduced. The AD9000 is capable of extremely low error rate operation, which makes it ideal for error sensitive applications like QAM demodulation. If the hysteresis control pin is used, it should be decoupled to ground through a 0.1μF capacitor, otherwise it may be left floating.

At the highest encode rates, overall accuracy can be improved by skewing the ENCODE signal duty-cycle to allow more time in the "latch" mode. Specifically, extending the logic HIGH portion of the ENCODE signal allows the comparators more time to achieve an appropriate logic level prior to the decoding cycle that begins on the rising edge of the ENCODE pulse.



Comparator Switching vs. Hysteresis Voltage

Layout Considerations

The AD9000, like all high-speed circuits, requires certain precautions be taken to insure optimum performance. The foremost of these is the use of a substantial low impedance ground plane around and under the AD9000. Just as important are high quality ground connections to the AD9000 itself. It is probably more effective to keep the analog and digital grounds separate, except at the AD9000 where they should be connected together. Sockets should generally be avoided due to the increased interlead capacitance they induce. If socketing must be used, pin sockets are preferred.

Decoupling is especially important to high-speed analog circuits. Each supply should be decoupled to ground with 0.1μF ceramic and 0.001μF mica capacitors. The ladder reference pins should be treated in a similar manner. In addition to decoupling the reference ladder, the reference ladder should be driven from a low output impedance source for the best noise rejection. In all cases, chip capacitors are recommended, where practical, to reduce the effects of lead inductance associated with standard discrete capacitors.

MIL-STD-883 Compliance Information

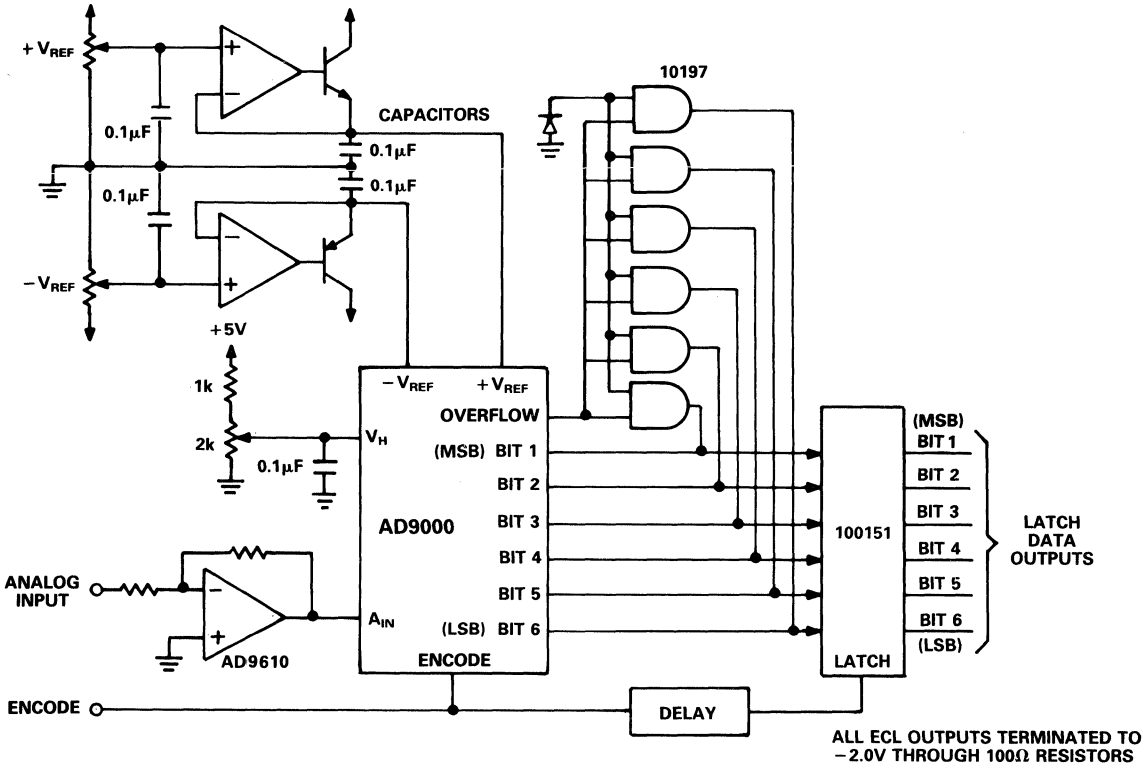
The AD9000SE/SD/883C are classified within microcircuits group 57-technology group D (bipolar A/D converters), and are constructed in accordance with the latest revision of MIL-STD-883. The AD9000 is electrostatic sensitive and falls within electrostatic sensitivity classification Category A. PDA (Percent Defective Allowance) is computed based of Subgroups 1 of the specified Group A test list. QA screening is in accordance with "Alternate Method A" of method 5005. The following apply: Burn-In per 1015, Life Test per 1005, Electrical Testing per 5004. (Note: Group A electrical Testing assumes $T_A = T_C = T_J$.)

TYPICAL APPLICATION

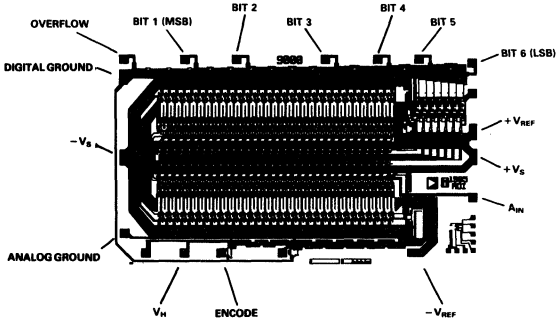
The AD9000 is a relatively flexible device which can be configured in a number of ways. One very useful feature of the AD9000 is the open emitter outputs. The open emitters allow the outputs of several AD9000s to be OR-WIRED in stacking applications for increased resolution. This kind of application depends on the return-to-zero nature of the output bits when $A_{IN} \geq +V_{REF}$ (overflow). In circuits which employ only one AD9000, this is not always an advantage. The circuit below illustrates one method of converting the outputs to nonreturn-to-zero.

The 10197 (standard 10K ECL logic) hex-AND group senses the active OVERFLOW output and forces all other bits to logic HIGH. The 10151 latch is not required for AD9000 applications, but it may ease data transfer sensitivities in asnychronous data collection systems.

The reference driver circuits should provide a low source impedance to prevent noise on the reference inputs from affecting the AD9000's accuracy. This is accomplished to a large extent by adequately decoupling the reference pins to ground. An improved method is employed below. The reference voltages ($+V_{REF}$, $-V_{REF}$) are buffered by a transistor/amplifier combination. This has the advantages of wide bandwidth (hence low impedance over a wide frequency range to eliminate high frequency noise components), and improved temperature stability.

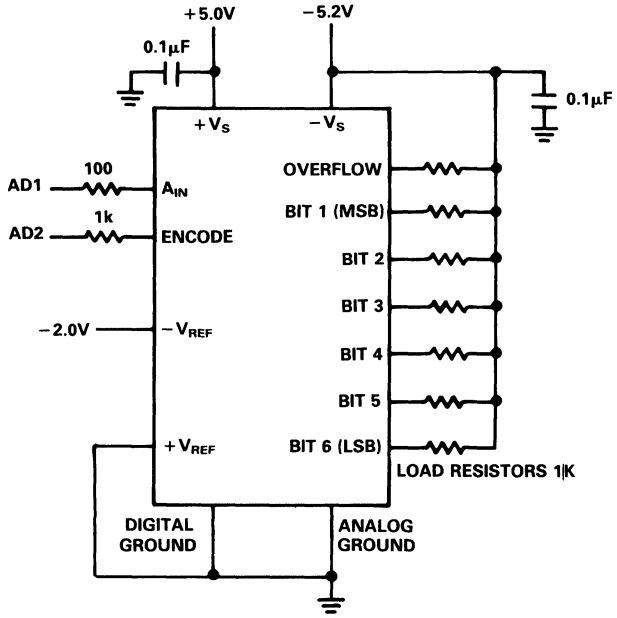


DIE LAYOUT



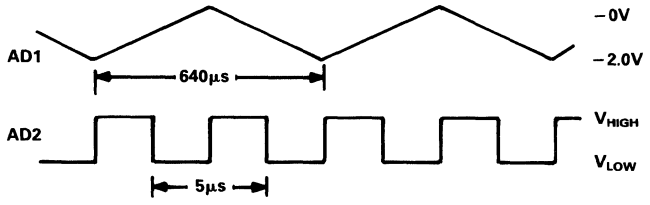
MECHANICAL INFORMATION

Die Dimensions	129 × 217 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	10,000Å Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	10,000Å Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding or 1mil Gold; Gold Ball Bonding



ALL RESISTORS ±5%
ALL CAPACITORS ±20%
ALL SUPPLY VOLTAGES ±5%

OPTION #1: (STATIC) ADI=0.0V, AD2=LOGIC HIGH
OPTION #2: (DYNAMIC) SEE WAVEFORMS



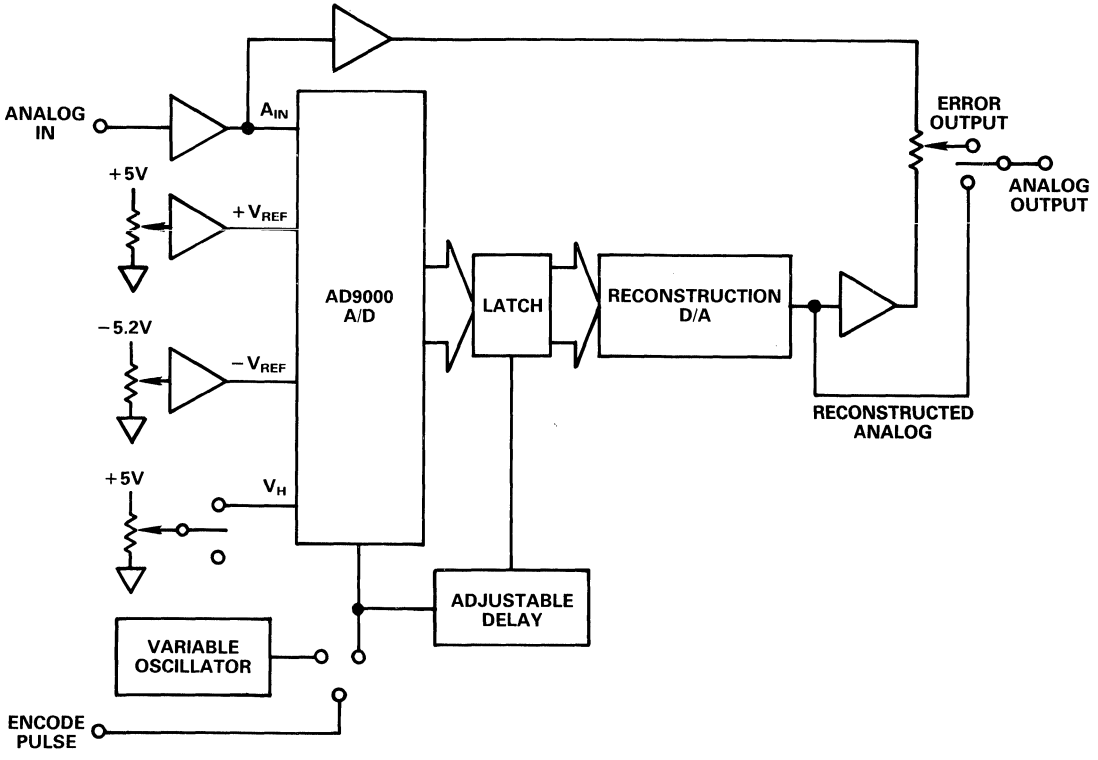
Burn-In Test Circuit

AD9000/PCB EVALUATION AND TEST BOARD

Evaluating and testing the AD9000 is greatly simplified with the AD9000/PCB evaluation board. The printed circuit board contains all of the driver and buffering circuits needed to test and evaluate the AD9000. The board outputs include both a high quality reconstructed representation of the input waveform, and a dc error waveform output which can be used to determine device linearities.

Inputs to the AD9000/PCB evaluation board include the analog signal to be digitized, as well as an optional ENCODE input for high stability measurements. All components, except the AD9000, are soldered onto the 8.5″ × 6.3″ board. The AD9000 is socketed to facilitate moderate volume testing. The evaluation board is offered with either a commercial temperature range AD9000, or an extended temperature range device installed.

The respective ordering numbers are AD9000JD/PCB and AD9000SD/PCB.



AD9000/PCB Block Diagram

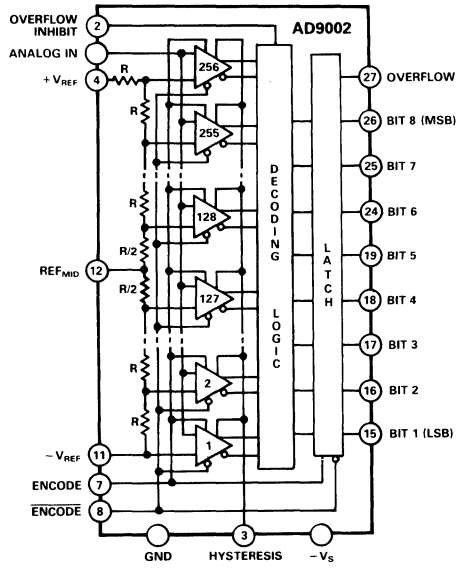
High Speed 8-Bit Monolithic A/D Converter

AD9002

FEATURES
150MSPS Encode Rate
Low Input Capacitance: 17pF
Low Power: 750mW
−5.2V Single Supply

APPLICATIONS
Radar Systems
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

AD9002 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9002 is an 8-bit, high speed, analog-to-digital converter. The AD9002 is fabricated in an advanced bipolar process which allows operation at sampling rates in excess of 150 megasamples/second. Functionally, the AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

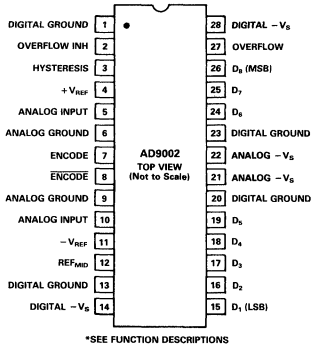
An exceptionally wide large signal analog input bandwidth of 160MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9002 allows very accurate acquisition of high speed pulse inputs, without an external track-and-hold. The comparator output decoding scheme minimizes false codes which is critical to high speed linearity.

The AD9002 provides an external hysteresis control pin which can be used to optimize comparator sensitivity to further improve performance. Additionally, the AD9002's low power dissipation of 750mW makes it usable over the full extended temperature range. The AD9002 also incorporates an overflow bit to indicate overrange inputs. This overflow output can be disabled with the overflow inhibit pin.

The AD9002 is available in two grades, one with 0.5LSB linearity and one with 0.75LSB linearity. Both versions are offered in an industrial grade, −25°C to +85°C, packaged in a 28-pin DIP and a 28-pin PLCC. The military temperature range devices, −55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

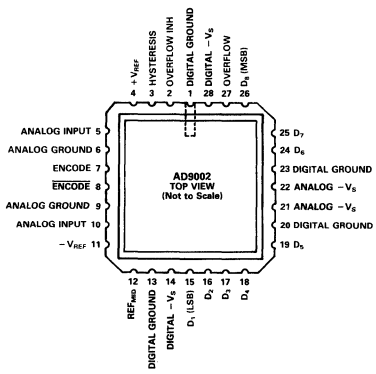
PIN DESIGNATIONS

DIP

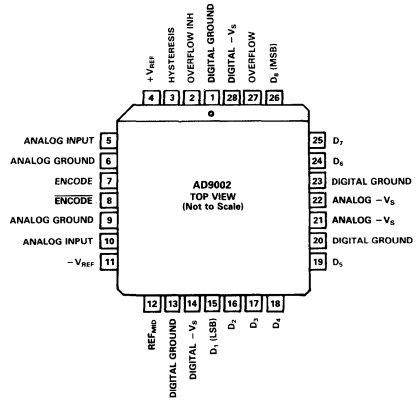


*SEE FUNCTION DESCRIPTIONS

LCC



PLCC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($-V_S$) . . . . . −6V
Analog-to-Digital Supply Voltage Differential 0.5V
Analog Input Voltage . . . . . $-V_S$ to +0.5V
Digital Input Voltage . . . . . $-V_S$ to 0V
Reference Input Voltage ($+V_{REF} - V_{REF}$)[2] . −3.5V to 0.1V
Differential Reference Voltage 2.1V
Reference Midpoint Current . . . . . ±4mA
ENCODE to $\overline{\text{ENCODE}}$ Differential Voltage 4V
Digital Output Current 20mA
Operating Temperature Range
AD9002AD/BD/AN/BN/AP/BP . . . . . −25°C to +85°C
AD9002SE/SD/TD/TE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

Electrical Characteristics ($-V_S = -5.2V$; Differential Reference Voltage = 2.0V, unless otherwise stated)

Parameter	Temp	Test Level	AD9002AD/AP/AN Min	Typ	Max	AD9002BD/BP/BN Min	Typ	Max	Sub-Group[4]	AD9002SD/SE/883B Min	Typ	Max	AD9002TD/TE/883B Min	Typ	Max	Units
RESOLUTION			8			8				8			8			Bits
DC ACCURACY																
Differential Linearity	+25°C	I		0.6	0.75		0.4	0.5	7		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75	8			1.0			0.75	LSB
Integral Linearity	+25°C	I		0.6	1.0		0.4	0.5	7		0.6	1.0		0.4	0.5	LSB
	Full	VI			1.2			1.2	8			1.2			1.2	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			7,8	GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR																
Top of Reference Ladder	+25°C	I		8	14		8	14	7		8	14		8	14	mV
	Full	VI			17			17	8			17			17	mV
Bottom of Reference Ladder	+25°C	I		4	10		4	10	7		4	10		4	10	mV
	Full	VI			12			12	8			12			12	mV
Offset Drift Coefficient	Full	V		20			20				20			20		μV/°C
ANALOG INPUT																
Input Bias Current[5]	+25°C	I		60	100		60	100	1		60	100		60	100	μA
	Full	VI			200			200	2,3			200			200	μA
Input Resistance	+25°C	III	100	200		100	200		12	100	200		100	200		kΩ
Input Capacitance	+25°C	III		17	22		17	22	12		17	22		17	22	pF
Large Signal Bandwidth[6]	+25°C	V		160			160				160			160		MHz
Input Slew Rate[7]	+25°C	V		440			440				440			440		V/μs
REFERENCE INPUT																
Reference Ladder Resistance	+25°C	VI	64	80	110	64	80	110	1	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient		V		0.25			0.25				0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C	V		10			10				10			10		MHz
DYNAMIC PERFORMANCE																
Conversion Rate	+25°C	I	125	150		125	150		4	125	150		125	150		MSPS
Aperture Delay	+25°C	V		1.3			1.3				1.3			1.3		ns
Aperture Uncertainty (Jitter)	+25°C	V		15			15				15			15		ps
Output Delay (t_{PD})[8,9]	+25°C	I	2.5	3.7	5.5	2.5	3.7	5.5	9	2.5	3.7	5.5	2.5	3.7	5.5	ns
Transient Response[10]	+25°C	V		6			6				6			6		ns
Overvoltage Recovery Time[11]	+25°C	V		6			6				6			6		ns
Output Rise Time[8]	+25°C	I			3.0			3.0	9			3.0			3.0	ns
Output Fall Time[8]	+25°C	I			2.5			2.5	9			2.5			2.5	ns
Output Time Skew[8,12]	+25°C	V		0.6			0.6				0.6			0.6		ns
ENCODE INPUT																
Logic "1" Voltage[8]	Full	VI	−1.1			−1.1			7,8	−1.1			−1.1			V
Logic "0" Voltage[8]	Full	VI			−1.5			−1.5	7,8			−1.5			−1.5	V
Logic "1" Current	Full	VI			150			150	7,8			150			150	μA
Logic "0" Current	Full	VI			120			120	7,8			120			120	μA
Input Capacitance	+25°C	V		3			3				3			3		pF
Encode Pulse Width (Low)[13]	+25°C	I	1.5			1.5			4	1.5			1.5			ns
Encode Pulse Width (High)[13]	+25°C	I	1.5			1.5			4	1.5			1.5			ns
OVERFLOW INHIBIT INPUT																
0V Input Current	Full	VI		144	300		144	300	1,2,3		144	300		144	300	μA
AC LINEARITY[14]																
Effective Bits[15]	+25°C	V		7.6			7.6				7.6			7.6		Bits
In-Band Harmonics																
dc to 1.23MHz	+25°C	I	48	55		48	55		4	48	55		48	55		dB
dc to 9.3MHz	+25°C	V		50			50				50			50		dB
dc to 19.3MHz	+25°C	V		44			44				44			44		dB
Signal-to-Noise Ratio[16]	+25°C	I	46	47.6		46	47.6		4	46	47.6		46	47.6		dB
Two Tone Intermod Rejection[17]	+25°C	V		60			60				60			60		dB
DIGITAL OUTPUTS[8]																
Logic "1" Voltage	Full	VI	−1.1			−1.1			1,2,3	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	1,2,3			−1.5			−1.5	V
POWER SUPPLY[18]																
Supply Current (−5.2V)	+25°C	I		145	175		145	175	1		145	175		145	175	mA
	Full	VI			200			200	2,3			200			200	mA
Nominal Power Dissipation	+25°C	V		750			750				750			750		mW
Reference Ladder Dissipation	+25°C	V		50			50				50			50		mW
Power Supply Rejection Ratio[19]	+25°C	I		0.8	1.5		0.8	1.5	7		0.8	1.5		0.8	1.5	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.

[3]Maximum junction temperature (t_J max) should not exceed 175°C for ceramic packages, and 150°C for plastic packages:

$t_J = PD\ (\theta_{JA}) + t_A$

$PD\ (\theta_{JC}) + t_C$

where

PD = power dissipation

θ_{JA} = thermal impedance from junction to ambient (°C/W)

θ_{JC} = thermal impedance from junction to case (°C/W)

t_A = ambient temperature (°C)

t_C = case temperature (°C)

typical thermal impedances are:

Ceramic DIP $\theta_{JA} = 56°C/W$; $\theta_{JC} = 20°C/W$

Plastic DIP $\theta_{JA} = 60°C/W$; $\theta_{JC} = 20°C/W$

Ceramic LCC $\theta_{JA} = 69°C/W$; $\theta_{JC} = 23°C/W$

PLCC $\theta_{JA} = 60°C/W$, $\theta_{JC} = 19°C/W$.

[4]Subgroups apply to military qualified devices only.

[5]Measured with AIN = 0V.

[6]Measured by FFT analysis where fundamental is −3dBc.

[7]Input slew rate derived from rise time (10 to 90%) of full scale input.

[8]Outputs terminated through 100Ω to −2V.

[9]Measured from ENCODE in to data out for LSB only.

[10]For full-scale step input, 8-bit accuracy is attained in specified time.

[11]Recovers to 8-bit accuracy in specified time after 150% full-scale input overvoltage.

[12]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[13]ENCODE signal rise/fall times should be less than 10ns for normal operation.

[14]Measured at 125MSPS encode rate.

[15]Analog input frequency = 1.23MHz.

[16]RMS signal to rms noise, with 1.23MHz analog input signal.

[17]Input signals 1V p-p @1.23MHz and 1V p-p @2.30MHz.

[18]Supplies should remain stable within ±5% for normal operation.

[19]Measured at −5.2V ±5%.

Specifications subject to change without notice.

3

Recommended Operating Conditions

	Input Voltage		
Parameter	**Min**	**Nominal**	**Max**
$-V_S$	−5.46	−5.20	−4.94
$+V_{REF}$	$-V_{REF}$	0.0V	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.

Test Level II – 100% production tested at +25°C, and sample tested at specified temperatures.

Test Level III – Sample tested only.

Test Level IV – Parameter is guaranteed by design and characterization testing.

Test Level V – Parameter is a typical value only.

Test Level VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF SUBGROUPS

Subgroup 1 – Static tests at +25°C (5% PDA calculated against Subgroup 1 for MIL-STD-883 version).

Subgroup 2 – Static tests at maximum rated operating temperature.

Subgroup 3 – Static tests at minimum rated operating temperature.

Subgroup 4 – Dynamic tests at +25°C.

Subgroup 5 – Dynamic tests at maximum rated operating temperature.

Subgroup 6 – Dynamic tests at minimum rated operating temperature.

Subgroup 7 – Functional tests at +25°C.

Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures.

Subgroup 9 – Switching tests at +25°C.

Subgroup 10 – Switching tests at maximum rated operating temperature.

Subgroup 11 – Switching tests at minimum rated operating temperature.

Subgroup 12 – Periodically sample tested.

ORDERING INFORMATION

Device	Linearity	Temperature Range	Description	Package Options*
AD9002AD	0.75LSB	−25°C to +85°C	28-Pin Ceramic DIP, Industrial	D-28
AD9002BD	0.50LSB	−25°C to +85°C	28-Pin Ceramic DIP, Industrial	D-28
AD9002AN	0.75LSB	−25°C to +85°C	28-Pin Plastic DIP, Industrial	N-28
AD9002BN	0.50LSB	−25°C to +85°C	28-Pin Plastic DIP, Industrial	N-28
AD9002AP	0.75LSB	−25°C to +85°C	28-Pin PLCC, Industrial	P-28A
AD9002BP	0.50LSB	−25°C to +85°C	28-Pin PLCC, Industrial	P-28A
AD9002SD/883B	0.75 LSB	−55°C to +125°C	28-Pin Ceramic DIP, Military	D-28
AD9002SE/883B	0.75 LSB	−55°C to +125°C	28-Pin LCC, Military	E-28A
AD9002TD/883B	0.50 LSB	−55°C to +125°C	28-Pin Ceramic DIP, Military	D-28
AD9002TE/883B	0.50 LSB	−55°C to +125°C	28-Pin LCC, Military	E-28A

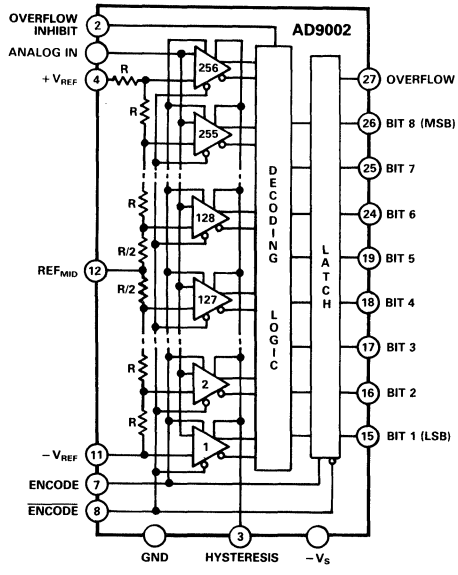
*See Section 14 for package outline information.

FUNCTIONAL DESCRIPTION

Pin #	Name	Description
1	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
2	OVERFLOW INH	OVERFLOW INHIBIT controls the data output polarity for overvoltage inputs.

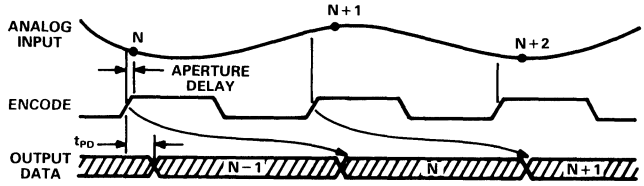
ANALOG INPUT	OVERFLOW ENABLED (FLOATING OR −5.2V) OF	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	OVERFLOW INHIBITED (GND) OF	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8
$V_{IN} > +V_{REF}$	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$V_{IN} \leq +V_{REF}$	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X

3	HYSTERESIS	The Hysteresis control voltage varies the comparator hysteresis from 0mV to 10mV, for a change from −5.2V to −2.2V at the Hysteresis control pin.
4	$+V_{REF}$	The most positive reference voltage for the internal resistor ladder.
5	ANALOG INPUT	One of two analog input pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
7	ENCODE	Noninverted input of the differential encode input. This pin is driven in conjunction with $\overline{\text{ENCODE}}$. Data is latched on the rising edge of the ENCODE signal.
8	$\overline{\text{ENCODE}}$.	Inverted input of the differential encode input. This pin is driven in conjunction with ENCODE.
9	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of two analog input pins. Both analog inputs should be connected together.
11	$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
12	REF_{MID}	The midpoint tap on the internal resistor ladder.
13	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
14	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.
15	D1	Digital data output (LSB).
16-19	D2-D5	Digital data output.
20	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
21, 22	ANALOG $-V_S$	One of two negative analog supply pins (nominally −5.2V). Both analog supply pins should be connected together.
23	DIGITAL GROUND	One of four digital ground pins. All digital ground pins should be connected together.
24, 25	D6, D7	Digital data output.
26	D8	Digital data output (MSB).
27	OVERFLOW	Overflow data output. Logic high indicates an input overvoltage ($V_{IN} > +V_{REF}$) if OVERFLOW INHIBIT is enabled (overflow enabled, −5.2V). See OVERFLOW INHIBIT.
28	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.

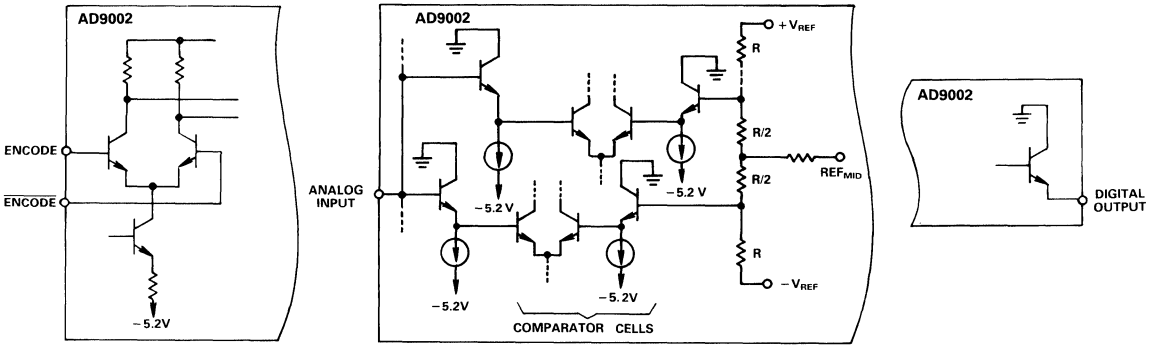


Functional Block Diagram

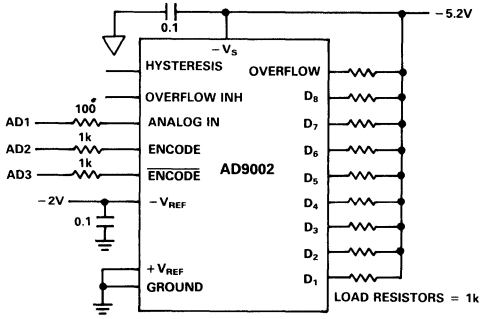
TIMING DIAGRAM



INPUT OUTPUT CIRCUITS



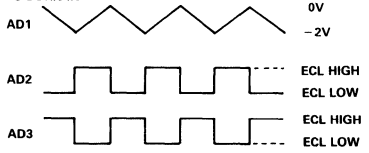
BURN-IN DIAGRAM



STATIC BURN IN

AD1 = 0V AD2 = ECL HIGH AD3 = ECL LOW

DYNAMIC BURN IN



ALL RESISTORS ±5%, Ω

ALL CAPACITORS ±20%, μF

ALL SUPPLIES ±5%

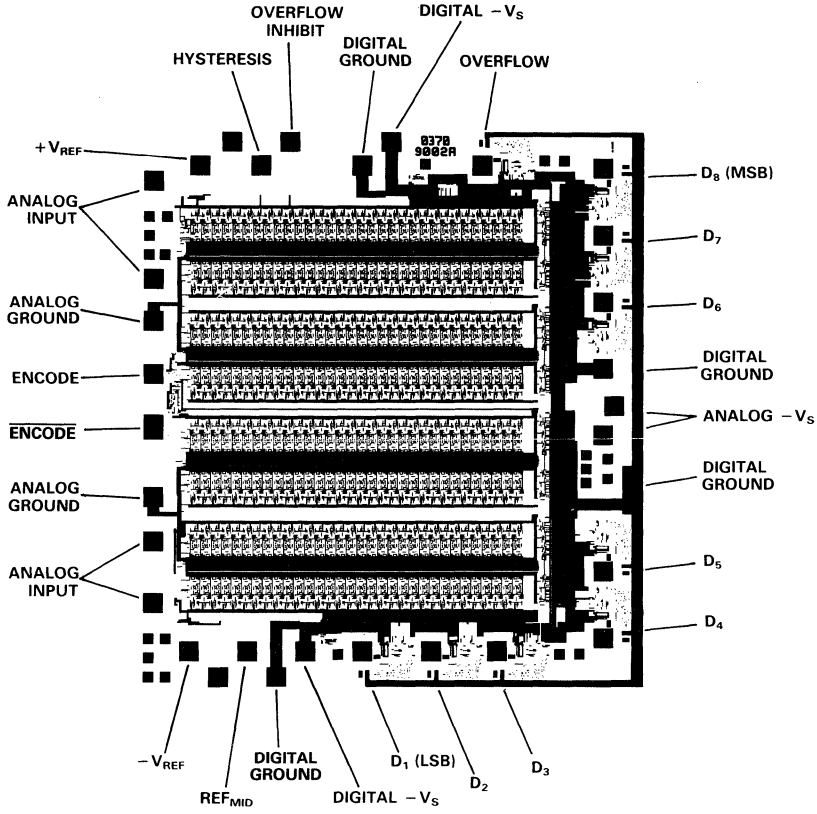
AD9002 BURN IN DIAGRAM

MIL-STD-883 COMPLIANCE INFORMATION

The AD9002 SD/SE/TE/TQ/883B devices are classified within Microcircuits Group 57, Technology Group D (bipolar A/D converters), and are constructed in accordance with MIL-STD-883. The AD9002 is electrostatic sensitive and falls within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $t_a = t_c = t_j$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.

DIE LAYOUT



MECHANICAL INFORMATION

Die Dimensions	106 × 114 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic (Ceramic) Epoxy (Plastic)
Bond Wire	1–1.3 mil Gold; Gold Ball Bonding

APPLICATION INFORMATION

The AD9002 is compatible with all standard ECL logic families, including 10K and 10KH. 100K ECL's logic levels are temperature compensated, and are therefore compatible with the AD9002 (and most other ECL device families) only over a limited temperature range. To operate at the highest encode rates, the supporting logic around the AD9002 will need to be equally fast. Whichever of the ECL logic families is used, special care must be exercised to keep digital switching noise away from the analog circuits around the AD9002. The two most critical items are digital supply lines and digital ground return.

The input capacitance of the AD9002 is an exceptionally low 17pF. This allows the use of a wide range of input amplifiers, both hybrid and monolithic. To take full advantage of the wide input bandwidth of the AD9002, a hybrid amplifier such as the AD9610 will be required. For those applications that do not require the full input bandwidth of the AD9002, more traditional monolithic amplifiers, such as the AD846, will work very well. Overall performance with any amplifier can be improved by inserting a 10Ω resistor in series with the amplifier output.

The output data is buffered through the ECL compatible output latches. All data is delayed by one clock cycle, in addition to the latch propagation delay (t_{PD}), before becoming available at the outputs. Both the analog-to-digital conversion cycle and the data transfer to the output latches are triggered on the rising edge of the differential, ECL compatible ENCODE signal (see timing diagram). In applications where only a single-ended signal is available, the AD96685, a high speed, ECL voltage comparator, can be employed to generate the differential signals. All ECL signals (including the overflow bit) should be terminated properly to avoid ringing and reflection.

The AD9002 also incorporates a HYSTERESIS control pin which provides from 0 to 10mV of additional hysteresis in the comparator input stages. Adjustments in the HYSTERESIS control voltage may help improve noise immunity and overall performance in harsh environments.

The OVERFLOW INHIBIT pin of the AD9002 determines how the converter handles overrange inputs ($AIN \geq +V_{REF}$). In the "enabled" state (floating at $-5.2V$), the OVERFLOW output will be at logic HIGH and all other outputs will be at logic LOW for overrange inputs (return-to-zero operation). In the "inhibited" state (tied to ground), the OVERFLOW output will be at logic LOW, and all other outputs will be at logic HIGH for overrange inputs (nonreturn-to-zero operation).

The AD9002 provides outstanding error rate performance. This is due to tight control of comparator offset matching and a fault tolerant decoding stage. Additional improvements in error rate are possible through the addition of hysteresis (see HYSTERESIS control pin). This level of performance is extremely important in fault-sensitive applications such as digital radio (QAM).

Dramatic improvements in comparator design and construction give the AD9002 excellent dynamic characteristics, especially SNR (signal-to-noise ratio). The 160MHz input bandwidth and low error rate performance give the AD9002 an SNR of 48dB with a 1.23MHz input. High SNR performance is particularly important in wide bandwidth applications, such as pulse signature analysis, commonly performed in advanced radar receivers.

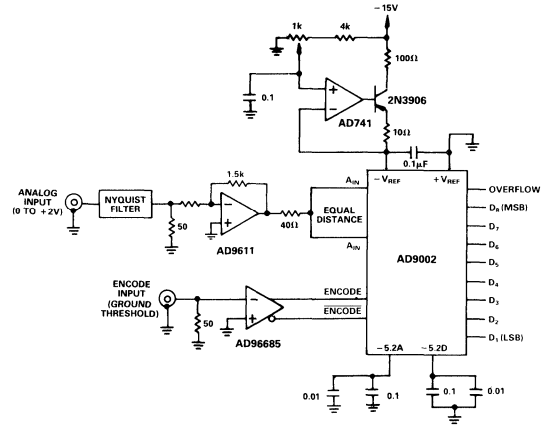
LAYOUT SUGGESTIONS

Designs using the AD9002, like all high speed devices, must follow a few basic layout rules to insure optimum performance. Essentially, these guidelines are meant to avoid many of the problems associated with high speed designs. The first requirement is for a substantial ground plane around and under the AD9002. Separate ground plane areas for the digital and analog components may be useful, but these separate grounds should be connected together at the AD9002 to avoid the effects of "ground loop" currents.

The second area that requires an extra degree of attention involves the three reference inputs, $+V_{REF}$, REF_{MID}, and $-V_{REF}$. The $+V_{REF}$ input and the $-V_{REF}$ input should both be driven from a low impedance source (note that the $+V_{REF}$ input is typically tied to analog ground). A low drift amplifier should provide satisfactory results, even over an extended temperature range. Adjustments at the REF_{MID} input may be useful in improving the integral linearity by correcting any reference ladder skews. The application circuit shown below demonstrates a simple and effective means of driving the reference circuit.

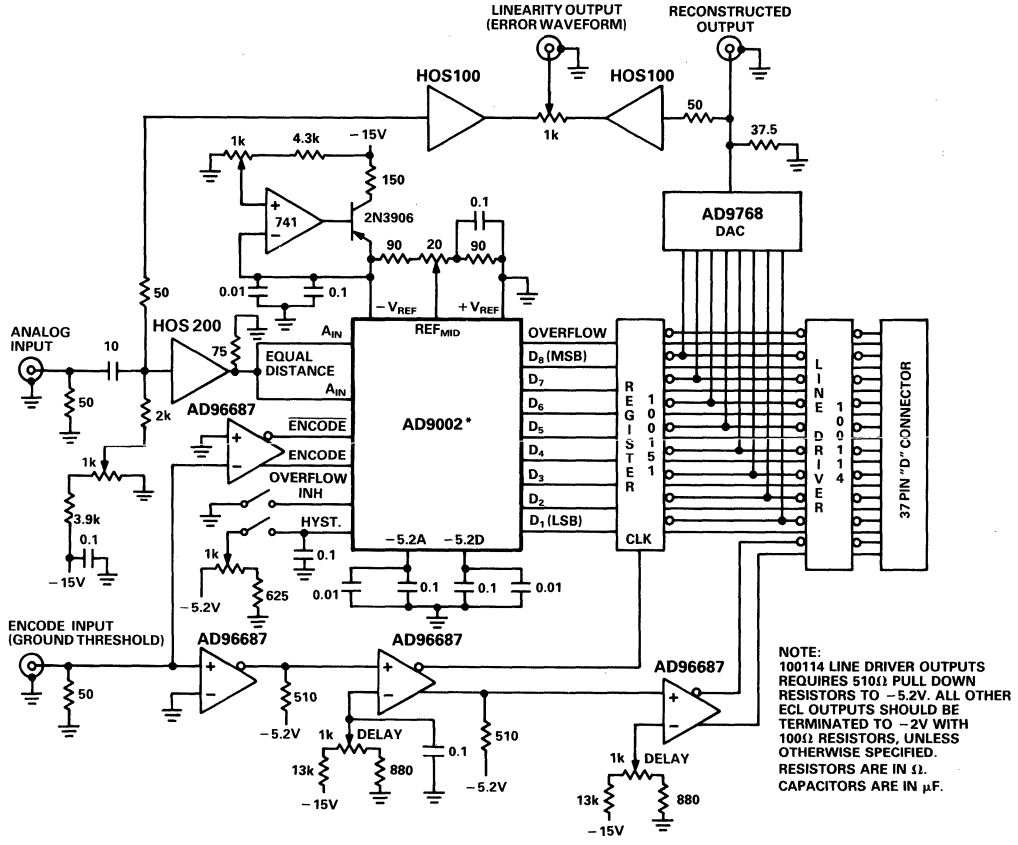
The reference inputs should be adequately decoupled to ground through 0.1μF chip capacitors to limit the effects of system noise on conversion accuracy. The power supply pins must also be decoupled to ground to improve noise immunity; 0.1μF and 0.01μF chip capacitors are recommended.

The analog input signal is brought into the AD9002 through two separate input pins. It is very important that the two input pins be driven symmetrically with equal length electrical connections. Otherwise, aperture delay errors may degrade converter performance at high frequencies.



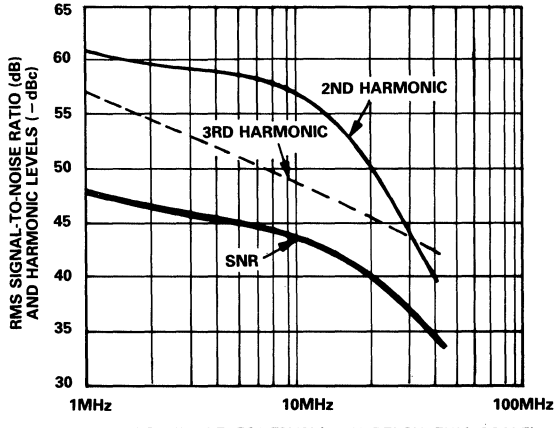
Typical AD9002 Application

AD9002 EVALUATION CIRCUIT



*CONTACT FACTORY ABOUT EVALUATION BOARD AVAILABILITY

AD9002 DYNAMIC PERFORMANCE



ANALOG INPUT FREQUENCY (0.1dB BELOW FULL SCALE)
125 MSPS ENCODE RATE

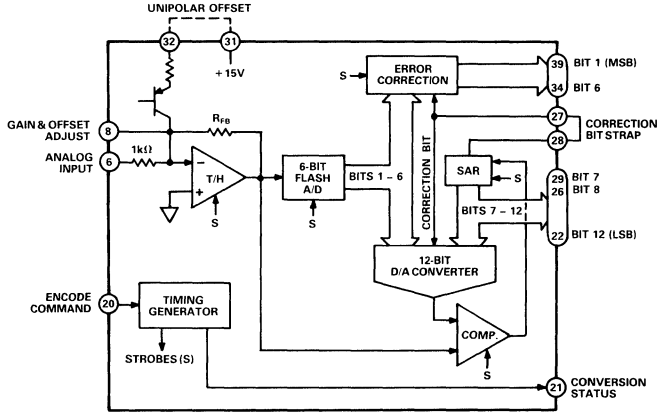
12-Bit, 1MHz A/D Converter

AD9003

FEATURES
12-Bit Resolution
1MHz Word Rates
T/H and Timing Included
Single 40-Pin DIP

APPLICATIONS
Radar Systems
Digital Oscilloscopes
Test Systems
Analytical Instrumentation
Waveform Analyzers

AD9003 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9003 is a complete 12-bit, 1MHz analog-to-digital converter (ADC) which combines low cost and high performance in a single 40-pin DIP. This unique converter includes track-and-hold (T/H), timing, and encoding functions with a power dissipation of only 2.2 watts.

This remarkable unit is capable of converting analog signals to the Nyquist limit at word rates through 1MHz. Its 1μs conversion interval includes acquisition time for the internal T/H, making it a true 1MHz converter.

Proprietary conversion techniques achieve linearity equivalent to the best successive approximation ADC along with subranging conversion speeds. A conversion status signal simplifies transferring output data into system logic. Innovative thick- and thin-film technologies assure excellent performance over temperature without compromising ac characteristics.

The AD9003KM operates at case temperatures from 0 to +70°C; the SM/883B and TM/883B units operate from −25°C to +100°C.

SPECIFICATIONS (Typical with nominal supplies, unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- $\pm V_S$ . . . . . $\pm 18V$
- V_{CC} . . . . . $-0.5V$ to $+7V$

Analog Input . . . . . $\pm 15V$
Digital Inputs . . . . . -0.5 to V_{CC}
Maximum Junction Temperature
- Models AD9003SM/TM/883B . . . . . 165°C
- Model AD9003KM . . . . . 150°C

Operating Temperature Range (Case)
- AD9003KM . . . . . 0 to +70°C
- AD9003SM/TM/883B . . . . . −25C to +100°

Storage Temperature . . . . . −65°C to +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

Parameter[1,2] (Conditions)	Sub-Group	Temp.	AD9003KM[1] Min	AD9003KM[1] Typ	AD9003KM[1] Max	AD9003SM/883B[2] Min	AD9003SM/883B[2] Typ	AD9003SM/883B[2] Max	AD9003TM/883B[2] Min	AD9003TM/883B[2] Typ	AD9003TM/883B[2] Max	Units
RESOLUTION				12			12			12		Bits
				0.024			0.024			0.024		%FS
LSB Weight				1.22			1.22			1.22		mV
STATIC ACCURACY												
√ Gain Error	4	+25°C		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	%FS
# Gain Error		Full			±0.46			±0.6			±0.6	%FS
√ Bipolar Offset	4	+25°C		+5	±10		±5	±10		±5	±10	mV
# Bipolar Offset		Full			±23			±32			±32	mV
√ Unipolar Offset	4	+25°C		±5	±10		±5	±10		±5	±10	mV
# Unipolar Offset		Full			±23			±32			±32	mV
√ Differential Linearity	4	+25°C		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	LSB
√ Differential Linearity	5,6	Full									±1.0	LSB
√ Integral Linearity (Best Fit)	4	+25°C		±0.8	±1.5		±0.8	±1.5		±0.8	±1.5	LSB
√ Integral Linearity (Best Fit)	5,6	Full			±1.5			±2.0			±2.0	LSB
√ Resolution for Which There are No Missing Codes	5,6	Full		12			12			12		Bits
DYNAMIC CHARACTERISTICS (Conversion Rate = 1MHz)[3]												
In-Band Harmonics[4]												
√ dc to 100kHz	4	+25°C	74	80		74	80		74	80		dB
√ dc to 100kHz	5,6	Full	72			72			72			dB
# 100kHz to 500kHz		+25°C		75			75			75		dB
√ Conversion Time[5]	4	+25°C		820	850		820	850		820	850	ns
# Effective Aperture Delay Time		+25°C	6	16	27	6	16	27	6	16	27	ns
# Aperture Uncertainty (Jitter)		+25°C		26			26			26		ps, rms
√ Signal-to-Noise Ratio[6]	4	+25°C	65	69		65	69		65	69		dB
√ Signal-to-Noise Ratio[6]	5,6	Full	65			65			65			dB
# Transient Response[7]		+25°C		200			200			200		ns
# Overvoltage Recovery Time[8]		+25°C			1500			1500			1500	ns
# Two-Tone Intermodulation[9]		+25°C		87			87			87		dB
ANALOG INPUT												
# Voltage Range (Full Scale)[10]		Full		5			5			5		V, p-p
√ Input Impedance	1	+25°C	950	1000	1050	950	1000	1050	950	1000	1050	Ω
√ Input Impedance	2,3	Full	950	1000	1050	950	1000	1050	950	1000	1050	Ω
Input Bandwidth												
# Small Signal, −3dB[11]		+25°C		10			10			10		MHz
# Large Signal, −3dB[12]		+25°C		8			8			8		MHz
TEMPERATURE DRIFT												
Offset Temperature Coefficient												
√ Bipolar	5,6	Full		±10	±35		±10	±40		±10	±40	ppm/°C
√ Unipolar	5,6	Full		±10	±35		±10	±40		±10	±40	ppm/°C
√ Gain Temperature Coefficient	5,6	Full		±15	±40		±15	±40		±15	±40	ppm/°C
# Differential Linearity Tempco		Full		±1.5	±3.5		±1.5	±3.5		±1.5	±3.5	ppm/°C
DIGITAL INPUTS												
# Logic Compatibility		Full		TTL			TTL			TTL		
# Logic "1" Voltage		Full	+2.0		V_{CC}	+2.0		V_{CC}	+2.0		V_{CC}	V
# Logic "0" Voltage		Full	−0.5		+0.8	−0.5		+0.8	−0.5		+0.8	V
Encode Command[13]												
Input Current												
√ Logic "1"	1,2,3	Full			60			60			60	µA
√ Logic "0"	1,2,3	Full			−1.2			−1.2			−1.2	mA
# Width[14]		Full	200		750	200		750	200		750	ns
# Frequency		Full	dc		1.0	dc		1.0	dc		1.0	MHz
# Rise/Fall Times		Full			10			10			10	ns

Parameter[1,2] (Conditions)	Sub-Group	Temp.	AD9003KM[1] Min	Typ	Max	AD9003SM/883B[2] Min	Typ	Max	AD9003TM/883B[2] Min	Typ	Max	Units
DIGITAL OUTPUTS												
# Logic Compatibility		Full		TTL			TTL			TTL		
√ Logic "1" Voltage	1,2,3	Full	+2.4			+2.4			+2.4			V
√ Logic "0" Voltage	1,2,3	Full			+0.4			+0.4			+0.4	V
# Output Drive		Full		1 Standard			1 Standard			1 Standard		TTL Load
Format				Parallel			Parallel			Parallel		
Coding												
Unipolar Mode				Complementary Binary			Complementary Binary			Complementary Binary		
Bipolar Mode				Complementary Offset Binary			Complementary Offset Binary			Complementary Offset Binary		
POWER REQUIREMENTS												
$+V_S$ Voltage		Full	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	+14.5	+15.0	+15.5	V
√ $+V_S$ Current	1,2,3	Full		78	90		78	90		78	90	mA
$-V_S$ Voltage		Full	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	−14.5	−15.0	−15.5	V
√ $-V_S$ Current	1,2,3	Full		44	49		44	49		44	49	mA
V_{CC} Voltage		Full	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
√ V_{CC} Current	1,2,3	Full		75	200		75	200		75	200	mA
√ Power Dissipation	1,2,3	Full		2.2	3.2		2.2	3.2		2.2	3.2	W
# PSRR[15]		+25°C		45			45			45		dB
THERMAL RESISTANCE												
Junction to Air, θ_{ca}[16]				19			19			19		°C/W
Junction to Case, θ_{jc}				3			3			3		°C/W
MTBF[17]												
Mean Time Between Failures							7.84×10^4			7.84×10^4		Hours
PACKAGE OPTIONS[18]												
M-40				AD9003KM			AD9003SM/883B			AD9003TM/883B		

NOTES

√ 100% tested (See Notes 1 and 2).

#Specification guaranteed by design; not tested.

[1]AD9003KM parameters preceded by a check (√) are tested at +25°C ambient temperature; performance is guaranteed over the commercial temperature range (0 to +70°C case temperature).

[2]AD9003SM/883B and TM/883B parameters preceded by a check (√) are tested at −25°C case, +25°C ambient, and +100°C case temperatures. Both grades are manufactured in full compliance to MIL-STD-883, Rev. C.

[3]Converting in excess of 1.0MHz is possible; however, acquisition time is reduced, which may increase distortion of high-frequency analog signals.

[4]In-band harmonics are expressed in dB below FS in terms of spurious in-band signals generated at 1MHz encode rate and single tone analog input in range shown.

[5]Measured from leading edge of encode command to trailing (rising) edge of conversion status signal (see Timing Diagram).

[6]RMS signal to rms noise ratio; analog input 1dB below FS @ 100kHz; 1MHz encode rate.

[7]For full-scale step input, 12-bit accuracy attained in specified time.

[8]Recovers to 12-bit accuracy in specified time after 2 × FS input overvoltage. (See text and Figure 5 for information on overloads.)

[9]Intermodulation measured in dB below FS at 1MHz encode rate with input frequencies of 75kHz and 105kHz; each 7dB below FS.

[10]Voltage Range = ±2.5V or 0V to −5.0V.

[11]With analog input 40dB below FS.

[12]With FS analog input. (Large-signal BW flat within 0.5dB, dc to 500kHz.)

[13]Transition from "0" to "1" initiates conversion.

[14]For 1MHz encode rate. At conversions below 1MHz, max width is conversion period minus 250ns. Optimum linearity at 200 to 250ns widths.

[15]Power Supply Rejection Ratio (PSRR) is sensitivity of offset to V_{CC}. This is parameter which is most sensitive to variations in supply voltage.

[16]The relationship between the device package and outside environment (θ_{ca}) varies with the application. Value shown is based on measuring case temperature with supply voltages applied to a device installed in a ZIF socket mounted on a standard "EJ" burn-in board.

[17]Calculated for SM/TM versions using MIL-HNBK-2i7; Ground Fixed; +80°C case temperature.

[18]See Section 14 for package outline information.

Specifications subject to change without notice.

EXPLANATION OF SUBGROUPS

Subgroup 1 – Static tests at +25°C.
(10% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 – Static tests at maximum rated temperature.
Subgroup 3 – Static tests at minimum rated temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated temperature.
Subgroup 6 – Dynamic tests at minimum rated temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated temperature.
Subgroup 11 – Switching tests at minimum rated temperature.
Subgroup 12 – Periodically sample tested.

PIN DESIGNATIONS
(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
40	DIGITAL GROUND	1	+5V
39	BIT 1	2	REFERENCE BYPASS[1]
38	BIT 2	3	DIGITAL GROUND
37	BIT 3	4	DIGITAL GROUND
36	BIT 4	5	−15V
35	BIT 5	6	ANALOG INPUT
34	BIT 6	7	DO NOT CONNECT
33	+5V	8	GAIN & OFFSET ADJUST
32	UNIPOLAR OFFSET[2]	9	ANALOG GROUND
31	UNIPOLAR OFFSET[1,2]	10	ANALOG GROUND
30	+15V	11	ANALOG GROUND
29	BIT 7	12	ANALOG GROUND
28	CORRECTION BIT[3]	13	ANALOG GROUND
27	CORRECTION BIT[3]	14	ANALOG GROUND
26	BIT 8	15	ANALOG GROUND
25	BIT 9	16	ANALOG GROUND
24	BIT 10	17	+5V
23	BIT 11	18	DIGITAL GROUND
22	BIT 12	19	−15V
21	CONVERSION STATUS	20	ENCODE COMMAND

NOTES
Although Grounds are Designated as Analog or Digital, All Grounds Should Be Connected to a Single Common Low-Impedance Ground Plane for Best Results.

[1]Pins 2 and 31 Must Be Bypassed to Ground with 0.1μF for Optimum Performance.
[2]For Unipolar Operation, Connect Pins 31 and 32; for Bipolar Operation, Ground Pin 32 and Connect Pin 31 Only to 0.1μF.
[3]Pins 27 and 28 Must Always Be Strapped Together with No Other Connections.

THEORY OF OPERATION

Refer to the block diagram of the AD9003.

Basically, the design of the unit is based on successive approximation techniques. However, the AD9003 also uses parallel encoding for the most significant bits (MSBs).

When a TTL-compatible Encode Command signal is applied to Pin 20, it causes the internal Timing Generator to generate strobe pulses used for controlling the timing of the various actions within the device.

The encode command causes the track-and-hold (T/H) to switch from a "track" mode to a "hold" mode; switches the 6-bit flash converter to a tracking mode of operation to allow it to reach the held value from the T/H; and resets the SAR. When the flash converter output has been determined, Bits 1 – 6 become inputs to the 12-bit D/A converter.

If the D/A voltage applied to the comparator is greater than the "held" value being applied to the comparator, a correction bit is turned on. If the D/A voltage is less, there is no correction bit and no change in the signal.

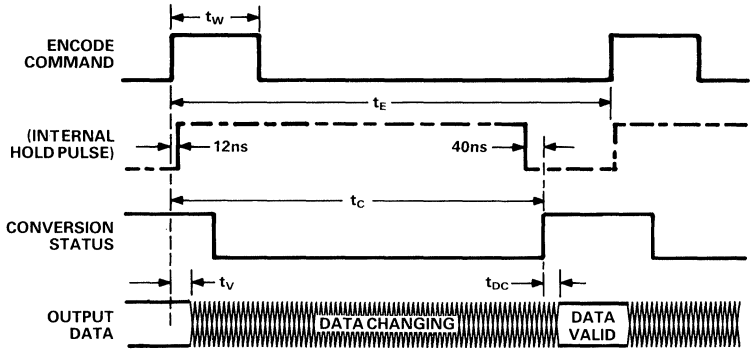
At this point, the D/A output voltage and the correction circuit outputs are 12-bit accurate. Standard successive approximation techniques are used to determine Bits 7 – 12; the end result is a 12-bit parallel output from the AD9003 A/D Converter.

The overall linearity of the AD9003 is independent of the flash converter, which materially enhances the performance of the unit. In addition, the architecture used in the converter makes it less sensitive to nonlinearities caused by D/A and/or comparator settling.

Performance of the AD9003 is equivalent to that of an ultrahigh-speed SAR type of design. But the design techniques which are used relieve the stringent comparator/DAC settling requirements usually associated with SAR designs. Instead, the AD9003 reaps the benefits of combining the best characteristics of flash converters and SARs while avoiding the penalties which are inherent in each individually.

Refer to Figure 1, the timing diagram for the AD9003. In this illustration, spacing between encode commands is shown as it would be for a 1MHz word rate, i.e., 1000ns. The width of the encode pulse is at its minimum value of 200ns.

The period of data validity associated with each encode command appears, in the figure, to be relatively short. Remember, however, each encode command generates the necessary switching to perform the digitizing function, and causes the output data to begin changing.



		MIN	MAX
t_W	ENCODE COMMAND PULSE WIDTH	200ns	750ns
t_E	SPACING BETWEEN ENCODE COMMANDS	1000ns	
t_C	CONVERSION TIME		850ns
t_V	DATA VALID		50ns
t_{DC}	DATA CHANGING		35ns

Figure 1. AD9003 Timing Diagram

In Figure 1, the timing is based on a maximum encode rate, with minimum spacing between encode commands. At lower conversion rates, this spacing would be lengthened correspondingly and the interval when data are valid would become longer.

Internal timing within the AD9003 typically requires 770ns to accomplish the necessary switching and processing of the analog input "frozen" by the encode command. Since the AD9003 is a true 1MHz converter, this leaves 230ns for the T/H to re-establish full accuracy when it returns to the "track" mode at the completion of the digitizing period.

This addition of the required 770ns and the 230ns accuracy increment shows up as a total of 1,000ns minimum between encode commands in Figure 1; any shorter interval will detract from the overall performance of the unit. Higher encode rates, i.e., shorter intervals between encode commands, are possible; but they may cause distortion on high-frequency analog signals because the T/H will not be fully settled when it is switched to the "hold" mode.

SETTING GAIN AND OFFSET

Varying gain and offset for the AD9003 enhances performance of the unit and increases its flexibility in applications. One suggested method of obtaining approximately 5% variation in each is shown in Figure 2.

The AD9003 can be operated in a unipolar mode or a bipolar mode; strap options and adjustments of the external controls shown in Figure 2 determine which is used. When calibrating for either mode, apply an encode command at the word rate frequency of the system to Pin 20.

Connect a precision voltage source between the ANALOG INPUT connection shown in Figure 2 and ground. Set its output for the voltage shown in Table I as being equal to −FS + 1/2LSB for the input range to be used (−0.6mV for unipolar operation and +2.4994V for bipolar operation if using the full-scale 5V input range of the AD9003).

Adjust the OFFSET control for a digital output which "dithers" between 0000 0000 0000 and 0000 0000 0001.

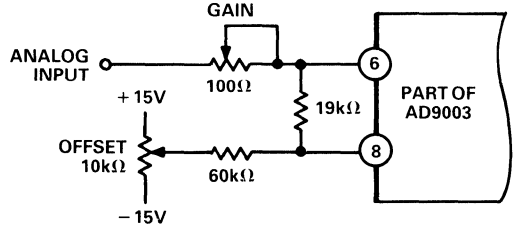


Figure 2. AD9003 Gain and Offset

To set gain, readjust the output of the voltage reference source to the value shown in Table I as being equal to +FS −1-1/2LSB for the input range to be used (−4.9982V for unipolar operation; −2.4982V for bipolar operation with the full-scale 5V range).

Adjust the GAIN control for a digital output which "dithers" between 1111 1111 1110 and 1111 1111 1111.

Figures 3 and 4 provide additional information about the switching points of the LSB when adjusting for either unipolar or bipolar operation using the full-scale 5V input.

AD9003 DRIVER CIRCUIT WITH CLAMP

The choice of the driver amplifier for an A/D can have significant effect on the performance of the converter. The ADI AD9610 Op Amp is the recommended choice for operation with the AD9003. This amplifier has extremely fast settling time and low distortion; these are especially important as the selected word rate frequency approaches the Nyquist limit.

In some applications, the analog input signals to be digitized may be outside the 5V range of the AD9003 converter, which can detract from the performance of the device by driving it into saturation.

At input frequencies greater than 50kHz, overloads larger than approximately 25% will saturate the front-end circuits of the internal track-and-hold. When the overload is removed, the T/H may cause erroneous codes to be generated at the output. Figure 5 shows a suggested circuit to avoid this.

For UNIPOLAR Input	Apply Reference	And Adjust	For "Dither" Between	For BIPOLAR Input	Apply Reference	And Adjust	For "Dither" Between
0 to −5V	−0.6mV	OFFSET	0000 0000 0000 and 0000 0000 0001	0.00	0.00	OFFSET	0111 1111 1111 and 1000 0000 0000
0 to −5V	−4.9982V	GAIN	1111 1111 1110 and 1111 1111 1111	±2.5V	−2.4982V	GAIN	1111 1111 1110 and 1111 1111 1111

Table I.

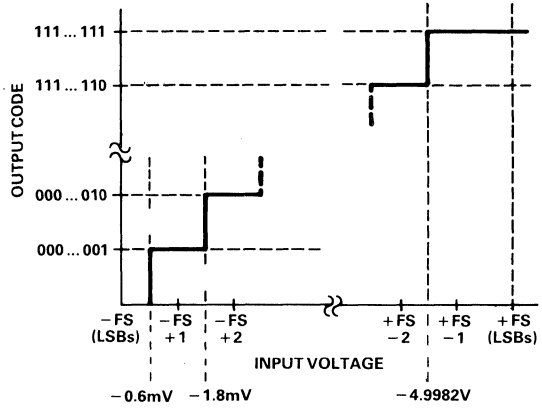


Figure 3. AD9003 Unipolar Adjustment

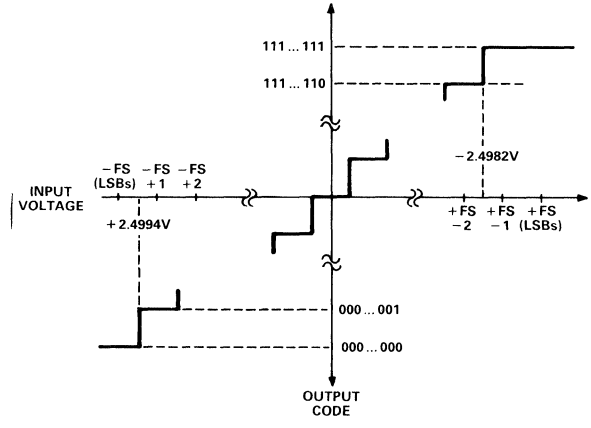


Figure 4. AD9003 Bipolar Adjustment

In this diagram, the value of the feed forward resistor R_{FF} is calculated on the basis of the equation:

$$R_{FF} = |\text{Desired Full-Scale Bipolar Voltage}| \times 500$$

The circuit eliminates saturating the internal T/H of the AD9003. Using an Analog Devices AD9610 ahead of the converter allows ±3x overdrives before the amplifier goes into saturation. Even in those instances in which the input signal exceeds the ±3x limit, the AD9610 comes out of saturation much more quickly than the input circuits of the converter would under the same circumstances.

Bipolar inputs to the AD9003 are held to a maximum of ±2.5V by the clamp circuits made up of 1N2810 Schottky diodes. The Analog Devices AD744 amplifiers and their associated circuits are for the purpose of clamping the Schottky diodes at the desired maximum input levels. As shown, +CLAMP ADJUST and −CLAMP ADJUST are set for +2.530V and −2.530V respectively.

These adjustment values take into account the gain and offset tolerances of the AD9003. If resistors with low temperature coefficients are selected, the clamp circuit will operate over the entire temperature range of the converter.

The bipolar circuit in Figure 5 can also be used for unipolar operation of the A/D with only minor changes. For this mode, the upper op amp (AD744 #1) and its associated reference circuits are removed; the upper 1N2810 clamp is connected, instead, to ground.

With these changes, the unipolar full-scale overdrive limit is 1.5x rather than the 3x of the bipolar connections; but this will prevent saturating the front end circuits of the AD9003. The value of R_{FF} in the unipolar circuit is based on:

$$R_{FF} = |\text{Desired Full-Scale Unipolar Voltage}| \times 250$$

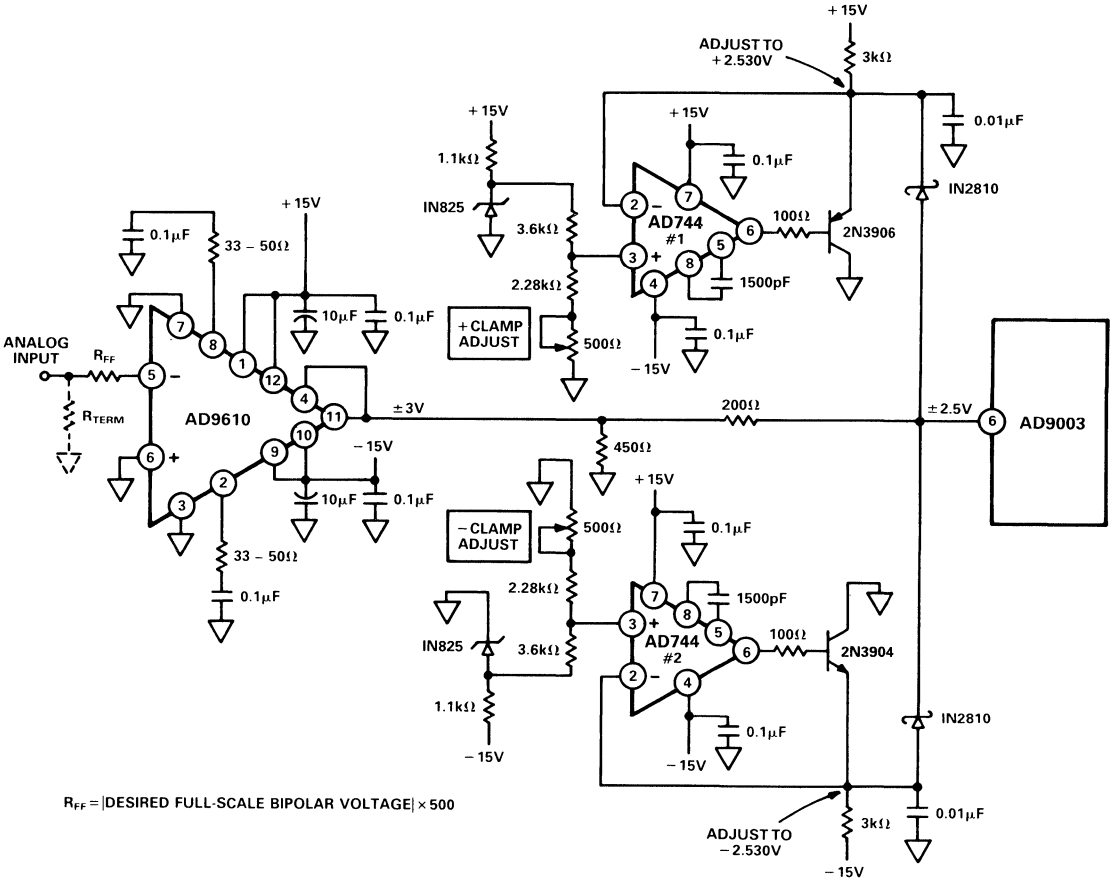


Figure 5. AD9003 Driver Circuit with Clamp

SUGGESTED LAYOUT

To obtain optimum performance from systems using the AD9003 or any other high-speed component, the user must exercise care in laying out the circuit. It is critical to use the shortest possible lead lengths and circuit runs. Construct the circuit on a large, low-impedance ground plane containing the maximum possible amount of copper dedicated as ground surface.

The AD9003 also requires the use of bypass capacitors on the power supplies; these should be connected as closely as possible to the supply pins. A suggested layout for the AD9003 when it is mounted on a printed circuit board is shown in Figure 6.

ORDERING INFORMATION

For operating case temperatures from 0 to +70°C, order part number AD9003KM. Two models are available with military processing and operation at case temperatures betweeen −25°C and +100°C. With the exception of differential linearity, the electrical specifications on these devices are the same. The AD9003SM/883B guarantees no missing codes over temperature; the AD9003TM/883B is screened for differential nonlinearity of ±1LSB maximum.

Both the commercial temperature and extended temperature versions are packaged in 40-pin metal can DIPs.

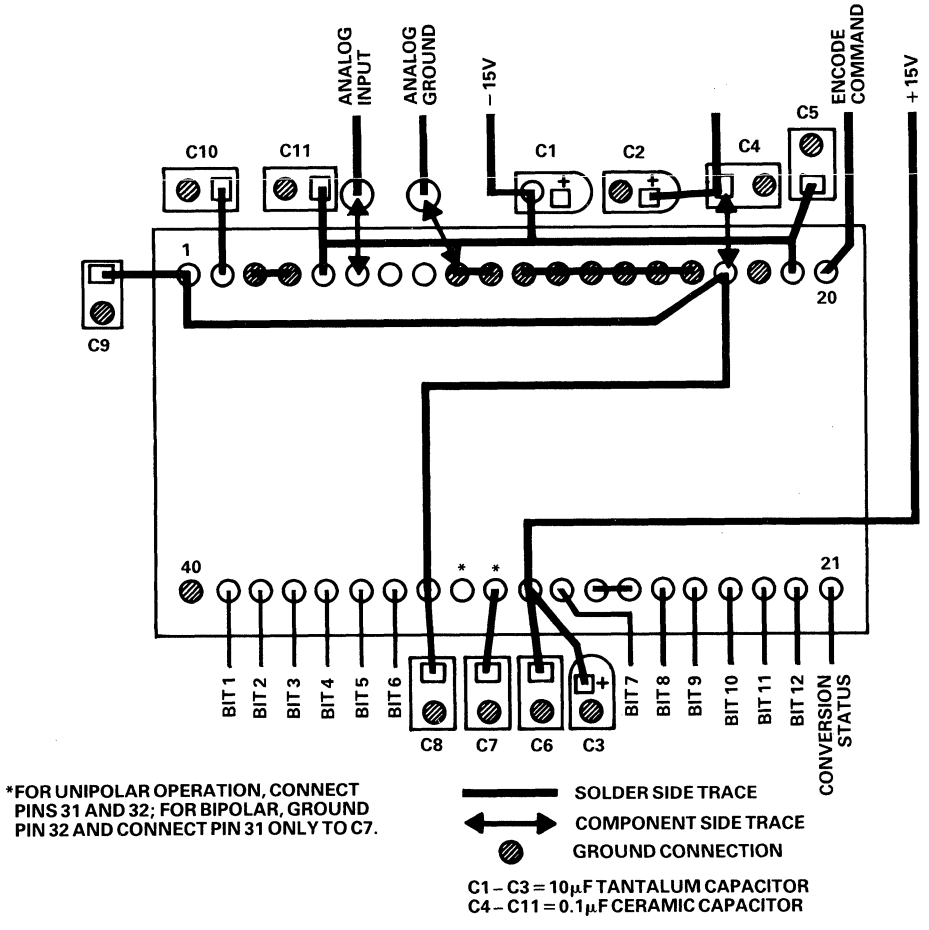


Figure 6. AD9003 Suggested Layout
(As Viewed from Bottom – Not to Scale)

ANALOG DEVICES

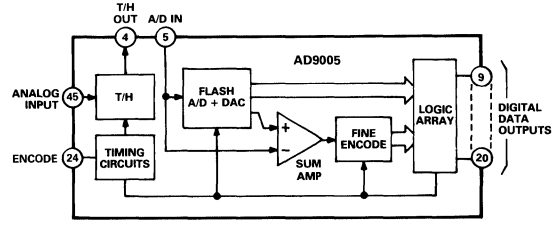
12-Bit, 10MSPS A/D Converter

AD9005

FEATURES
Complete 12-Bit A/D Converter
Includes Track and Hold, Reference and Timing
Bipolar Analog Input (±1.024V)
Up to 10MSPS Sampling Rate
Low Power Dissipation: 3.1W
Low Harmonic Distortion

APPLICATIONS
Radar
Digital Oscilloscopes
Electro-Optics
Medical Scanners
Communication/Signal Intelligence

AD9005 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD9005 is a complete 12-bit A/D converter featuring on-board track-and-hold amplifier, voltage reference and timing circuitry. Featuring sampling rates from dc to 10MSPS, the AD9005 uses a subranging converter architecture to achieve high speed and high resolution. Dynamic performance includes a SNR of 64dB and harmonic distortion of −72dBc with a 4.3MHz analog input.

Critical to this performance is the use of advanced bipolar integrated circuits, custom designed for the AD9005 and manufactured by Analog Devices. The AD9005 is TTL compatible with offset binary outputs. It is available in a 46-pin hermetic metal DIP in two temperature ranges: 0 to +70°C commercial range and −55°C to +125°C military range (case temperature).

ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9005KM	0 to +70°C	46-Pin DIP	M-46
AD9005TM	−55°C to +125°C	46-Pin DIP	M-46

*See Section 14 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_{CC}$) . . . . . +18V
Negative Supply Voltage ($-V_{EE}$) . . . . . −18V
Positive Supply Voltage ($+V_S$) . . . . . +6V
Negative Supply Voltage ($-V_S$) . . . . . −6V
Analog Input Voltage (Pin 45) . . . . . ±3.0V dc
Digital Input Voltage . . . . . −0.5V to $+V_S$
Digital Output Current 4mA

Operating Temperature Range (Case)
AD9005KM . . . . . 0 to +70°C
AD9005TM . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[2] . . . . . +165°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($+V_{CC}$ = +15V, $-V_{EE}$ = −15V, $+V_S$ = +5V, $-V_S$ = −5.2V, unless otherwise stated)

Parameter	Temp	Test Level	AD9005KM Min	AD9005KM Typ	AD9005KM Max	AD9005TM Min	AD9005TM Typ	AD9005TM Max	Units
RESOLUTION	Full	I	12			12			Bits
LSB Weight	Full	V		0.5			0.5		mV
STATIC ACCURACY									
Differential Nonlinearity	+25°C	I	−0.75	±0.5	+0.75	−0.75	±0.5	+0.75	LSB
	Full	VI	−1.0		+1.0	−1.0		+1.25	LSB
Integral Nonlinearity	+25°C	I		±1.0	±2.25		±1.0	±2.25	LSB
	Full	VI			±2.5			±2.75	LSB
No Missing Codes	Full	VI		GUARANTEED			GUARANTEED		
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0	% FS
	Full	VI			±2.0			±2.0	% FS
Offset Error	+25°C	I		±4	±15		±4	±15	mV
	Full	VI			±30			±40	mV
ANALOG INPUT									
Input Voltage Range	Full	V		±1.024			±1.024		V p-p
Input Resistance	Full	VI	950	1000	1050	950	1000	1050	Ω
Input Capacitance	+25°C	V		5			5		pF
Large Signal Input Bandwidth[3]	Full	V		38			38		MHz
DYNAMIC CHARACTERISTICS[5]									
Maximum Conversion Rate	Full	I	10			10			MSPS
Output Data Delay[6,9] (t_{PD})	+25°C	V		90			90		ns
Aperture Delay	+25°C	V		5			5		ns
Aperture Uncertainty	+25°C	IV		10	20		10	20	ps rms
Transient Response (to ±1LSB)[7]	+25°C	IV			120			120	ns
Overvoltage Recovery Time[8] (to ±1LSB)	+25°C	IV			250			250	ns
In-Band Harmonics[10,4]									
F_{IN} = 540kHz	+25°C	IV	−70	−75		−69	−75		dBc
F_{IN} = 2.3MHz	+25°C	I	−68	−72		−67	−72		dBc
	Full	VI	−67			−66			dBc
F_{IN} = 4.3MHz	+25°C	I	−66	−72		−66	−72		dBc
	Full	VI	−65			−63			dBc
Signal to Noise Ratio[11,4]									
F_{IN} = 540kHz	+25°C	IV	65	67		64	67		dB
F_{IN} = 2.3MHz	+25°C	I	63	65		63	65		dB
	Full	VI	63			60			dB
F_{IN} = 4.3MHz	+25°C	I	62	64		62	64		dB
	Full	VI	61			60			
Two-Tone Intermodulation Distortion[12]									
F_{IN} = 2.2MHz+2.3MHz	+25°C	V		−74			−74		dBc

Parameter	Temp	Test Level	AD9005KM Min	AD9005KM Typ	AD9005KM Max	AD9005TM Min	AD9005TM Typ	AD9005TM Max	Units
ENCODE INPUT[14]									
Logic "1" Voltage	Full	IV	2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8	V
Logic "1" Current	Full	IV			150			150	μA
Logic "0" Current	Full	IV			150			150	μA
Input Capacitance	+25°C	V		5			5		pF
Encode Pulse Width (High)	+25°C	IV	25			25			ns
DIGITAL OUTPUTS									
Logic "1" Voltage (2mA Source)	Full	IV	2.4			2.4			V
Logic "0" Voltage (4mA Sink)	Full	IV			0.4			0.4	V
Logic Coding	Full	IV		Offset Binary			Offset Binary		
POWER SUPPLY									
Supply Voltage $+V_{CC}$	Full	VI	+14.25	+15.0	+15.75	+14.25	+15.0	+15.75	V
Supply Current $+V_{CC}$	Full	VI		33	40		23	25	mA
Supply Voltage $-V_{EE}$	Full	VI	−14.25	−15.0	−15.75	−14.25	−15.0	−15.75	V
Supply Current $-V_{EE}$	Full	VI		55	70		45	55	mA
Supply Voltage $+V_S$	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	V
Supply Current Analog $+V_S$	Full	VI		124	140		124	140	mA
Supply Current Digital $+V_S$	Full	VI		55	110		55	110	mA
Supply Voltage $-V_S$	Full	VI	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	V
Supply Current Analog $-V_S$	Full	VI		160	185		160	185	mA
Supply Current Digital $-V_S$	Full	VI		73	115		73	115	mA
Nominal Power Dissipation	Full	VI		3.1	4.1		3.1	4.1	W
PSRR[13, 15]	+25°C	I		0.01	0.02		0.01	0.02	%/%

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute rating conditions for extended periods of time may affect device reliability.

[2]Maximum junction temperature should not be allowed to exceed 165°C. Hybrid thermal model:

$t_{JUNCTION} = t_{AMBIENT} + P_{DISSIPATION} \times (\theta_{CA} + \theta_{JC})$

$= t_{CASE} + P_{DISSIPATION} \times (\theta_{JC})$

46 Pin metal DIP: θ_{CA} = 14°C/W in still air;

θ_{CA} = 6°C/W with 500LFPM air flow

θ_{JC} = 6°C/W

[3]Determined by 3dB reduction in reconstructed output.

[4]Input at 1dB below full scale.

[5]Measured at 10MHz encode rate.

[6]Measured from ENCODE in to data out for LSB only.

[7]For full-scale step input; 12-bit accuracy is attained in the specified time.

[8]Recovers to 12-bit accuracy in specified time following 200% full-scale input voltage.

[9]Excludes pipeline delay of two clock cycles (see timing diagram).

[10]Worst case spurious in-band signal relative to input level.

[11]RMS signal to RMS noise, including harmonics.

[12]Worst case spurious in-band signal relative to level of input tones, which are both −7dB below full scale.

[13]Sensitivity of full scale gain error with respect to power supply variation within supply Min/Max limits.

[14]ENCODE signal rise and fall times should be less than 5ns for normal operation. Transition from "0" to "1" initiates conversion.

[15]PSRR is tested over given voltage range.

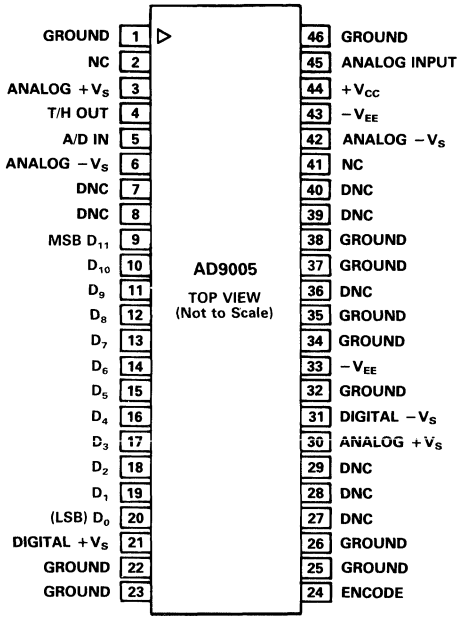
EXPLANATION OF TEST LEVELS

Test Level I	–	100% production tested.
Test Level II	–	100% production tested at +25°C, and sample tested at specified temperatures.
Test Level III	–	Sample tested only.
Test Level IV	–	Parameter is guaranteed by design and characterization testing.
Test Level V	–	Parameter is a typical value only.
Test Level VI	–	All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices. Guaranteed, not tested, for commercial temperature range.

RECOMMENDED OPERATING CONDITIONS

Parameter	Input Voltage Min	Input Voltage Nominal	Input Voltage Max
$-V_S$	−5.45	−5.2	−4.95
$+V_S$	+5.25	+5.0	+4.75
$-V_{EE}$	−15.75	−15.0	−14.25
$+V_{CC}$	+14.25	+15.0	+15.75
Analog Input	−1.024		+1.024

AD9005 PIN DESIGNATIONS



NC = NO CONNECT
DNC = DO NOT CONNECT

PIN DESCRIPTIONS

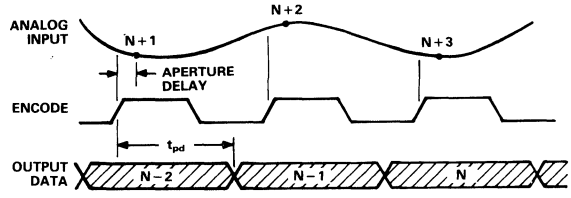
Pin	Name	Description
1	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
2	NC	Not internally connected.
3	ANALOG $+V_S$	Positive analog supply pin. Nominally +5V dc.
4	T/H OUT	Output of internal track-and-hold amplifier. Connect to Pin 5 for normal operation.
5	A/D IN	Input to internal A/D encoder. Connect to Pin 4 for normal operation.
6	ANALOG $-V_S$	Negative analog supply pin. Nominally −5.2V dc.
7, 8	DNC	Do not connect. Internal test point.
9	D_{11} (MSB)	Most significant bit of digital output data.
10-19	D_1-D_{10}	Digital data outputs.
20	D_0 (LSB)	Least significant bit of digital output data.

OUTPUT CODING

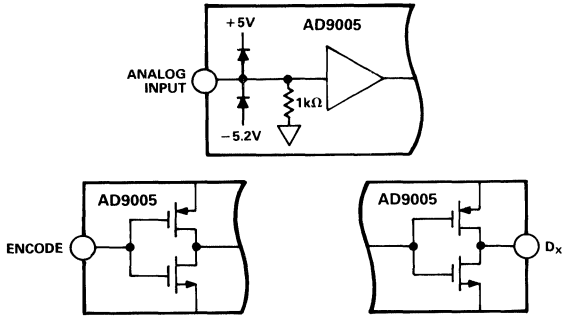
ANALOG INPUT	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
≥+1.024V	1	1	1	1	1	1	1	1	1	1	1	1
≤−1.024V	0	0	0	0	0	0	0	0	0	0	0	0

21	DIGITAL $+V_S$	Positive digital supply pin. Nominally +5V dc.
22, 23	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
24	ENCODE	Convert command. TTL compatible, rising edge triggered.
25, 26	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
27-29	DNC	Do not connect. Internal test point.
30	ANALOG $+V_S$	Positive analog supply pin. Nominally +5V dc.
31	DIGITAL $-V_S$	Negative digital supply pin. Nominally −5.2V dc.
32	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
33	$-V_{EE}$	Negative analog supply pin. Nominally −15V dc.
34, 35	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
36	DNC	Do not connect. Internal test point.
37, 38	GROUND	Circuit ground. All grounds should be connected together near the AD9005.
39, 40	DNC	Do not connect. Internal test point.
41	NC	Not internally connected.
42	ANALOG $-V_S$	Negative analog supply pin. Nominally −5.2V dc.
43	$-V_{EE}$	Negative analog supply pin. Nominally −15V dc.
44	$+V_{CC}$	Positive analog supply pin. Nominally +15V dc.
45	ANALOG INPUT	Analog input. Full scale of ±1.024V.
46	GROUND	Circuit ground. All grounds should be connected together near the AD9005.

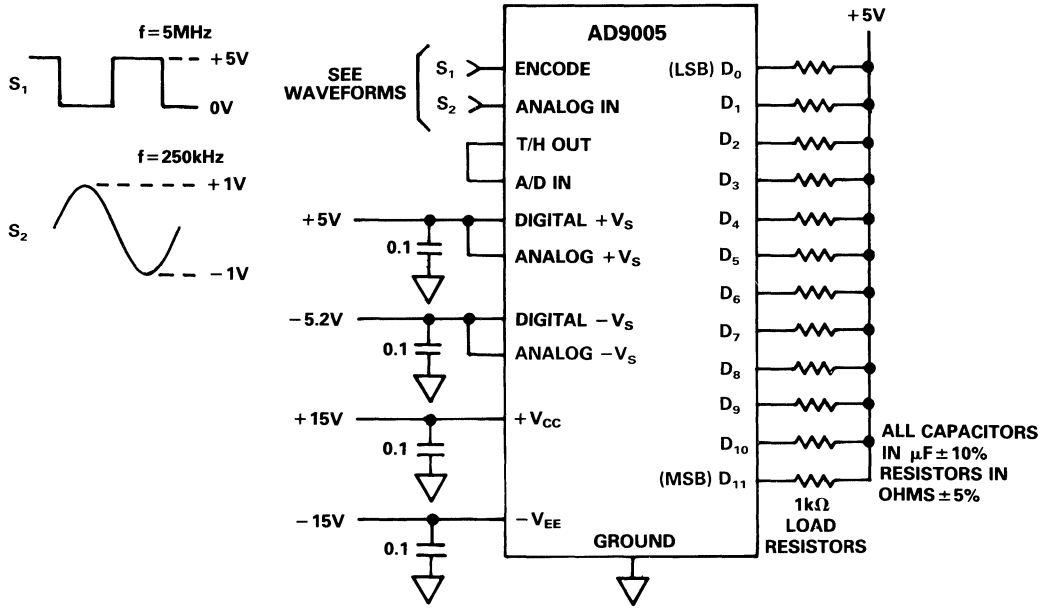
TIMING DIAGRAM



EQUIVALENT INPUT/OUTPUT CIRCUITS



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The AD9005 is a complete analog-to-digital converter. The AD9005 uses a subranging A/D architecture enhanced by hybrid technology. This includes an on-board track-and-hold amplifier, on-board references, timing circuitry and output latches.

The analog input of the AD9005 is fed directly into the internal track-and-hold amplifier, thus eliminating the need for external signal conditioning in many applications. This amplifier provides low input capacitance, and a bipolar (±1.024V) input range. Normally reverse-biased Schottky diodes on the input provide overrange protection. If the amplitude, bandwidth or dc voltage level of the analog input signal calls for external signal conditioning, it is advisable to use an amplifier with low harmonic distortion and low noise characteristics. Selection of such an amplifier is difficult because the performance of the AD9005 will likely exceed that of most commercially available amplifiers. A good choice would be the AD9610, a wideband, low noise, current feedback operational amplifier. It is important to remember that band limiting the analog input signal can avoid aliasing during the A/D conversion process.

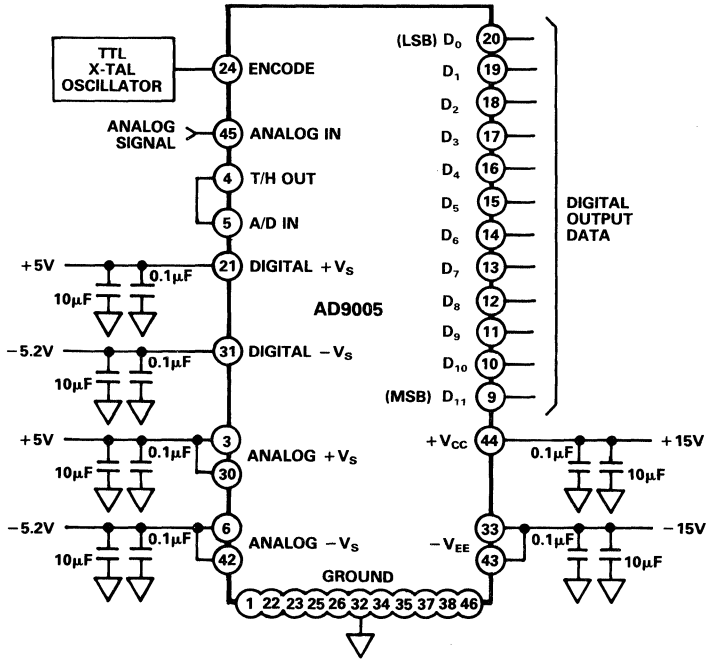
Timing in the AD9005 is critical, and careful measures must be taken to support 12-bit accuracy. One simple way to enhance the performance of the AD9005 is to synchronize the system clock to a crystal oscillator. This will minimize any clock jitter, a must for maintaining the spectral purity of analog signals near Nyquist limits. Because the conversion cycle begins with the rising edge of the encode signal, a fast, clean rising edge will also help to reduce any clock jitter.

When the ENCODE signal of the AD9005 goes HIGH, the internal track-and-hold enters the hold state; after 65ns, it returns to track mode. In applications in which the AD9005 is clocked slowly or intermittently (i.e., in burst mode), the encode signal should be returned to a logic LOW state during the idle periods.

The ENCODE signal pulse width should also be adjusted so that it is in the HIGH (hold) state for a minimum of 25ns. This ensures that the T/H enters the hold mode before the A/D conversion takes place.

The AD9005 has many appealing characteristics for 12-bit A/D converter applications. Its dynamic performance is state-of-the-art in hybrid technology. Typical applications include radar, missile guidance, digital oscilloscopes, waveform analyzers, medical instrumentation, electro-optics, communications and ESM.

TYPICAL AD9005 APPLICATION



Layout Information

The accuracy of a 12-bit converter, especially one with the dynamic performance level of the AD9005, requires that designers pay careful attention to printed circuit board layouts. Analog signal paths should be impedance matched, with termination/load resistors at or near package connections. Analog signal paths should also be isolated from digital signal paths. Otherwise digital signals can be capacitively coupled into the analog section of the circuit, degrading the overall performance of the A/D converter.

Digital switching noise on power supplies can also degrade converter performance. Because of this noise (inherent with TTL logic), the digital power supplies of the AD9005 should be separated from the analog power supplies. In addition, each power supply should be capacitively decoupled to ground. To accomplish this, a single large value capacitor with a high resonant frequency (a 10μF tantalum capacitor for example) should be used on each of the AD9005's power supplies, at or near the package. In addition, a lower value capacitor with good high frequency characteristics (a 0.1μF ceramic chip capacitor is recommended) should be connected to each power supply pin connection.

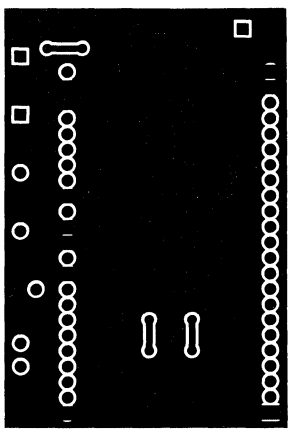
For applications in which only single +5V and/or −5.2V supplies are available, a ferrite bead, placed in series between the analog and digital power pins, can be used to isolate the digital noise from the analog circuits.

Noise on the circuit ground is often the limiting factor in A/D converter performance. Perhaps the most critical concerns of circuit layout are the ground connections. To reduce ground noise, a two-sided printed circuit board is recommended, the component side being reserved (as much as possible) for a single, low impedance ground plane. The other side should be used for all (possible) power and signal connections. Each of the ground connections of the AD9005 should be connected to the ground plane, and most of the area under the AD9005 should be part of this ground plane. The metal case of the AD9005 is connected to ground.

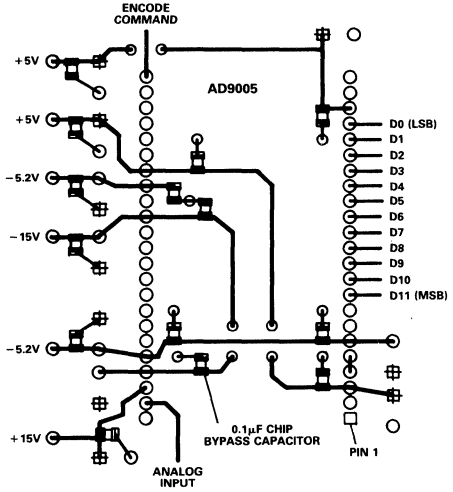
Operation of the AD9005 requires that Pin 4, the output of the internal track-and-hold, be connected to Pin 5, the input to the AD9005's A/D converter circuitry. A suggested layout, showing this connection, is shown below.

A final suggestion regarding circuit layout concerns the use of sockets. Ideally, parts should be soldered into boards in final designs. If sockets must be used, individual pin sockets are recommended to avoid lead inductance and capacitive coupling between adjacent pins. Pin sockets are available from Amp, part #6−330808−0.

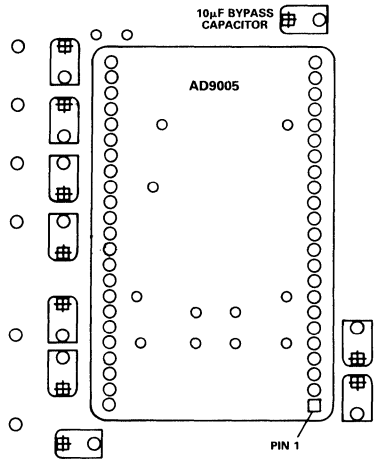
SUGGESTED LAYOUT



GND PLANE SIDE
(As Viewed from Top)

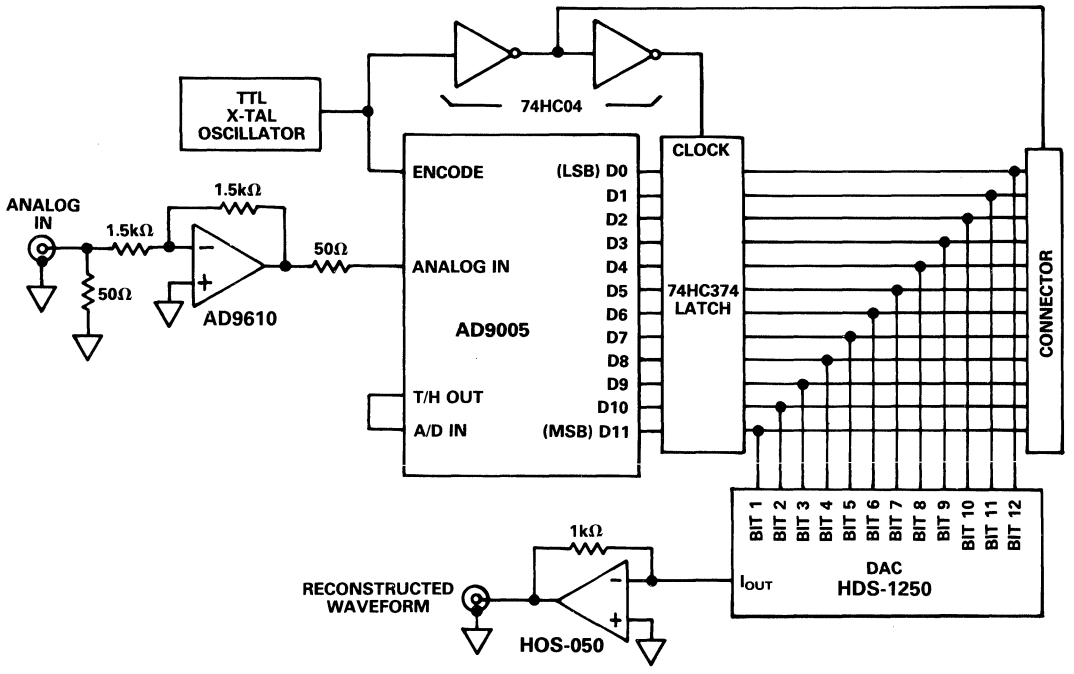


SOLDER SIDE
(As Viewed from Top)



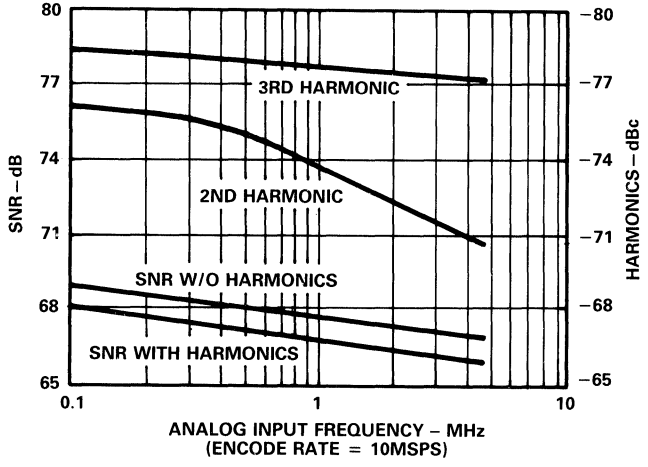
COMPONENT MOUNTING
(As Viewed from Top)

EVALUATION CIRCUIT



Contact factory about evaluation board availability.

AD9005 DYNAMIC PERFORMANCE (@ +25°C)



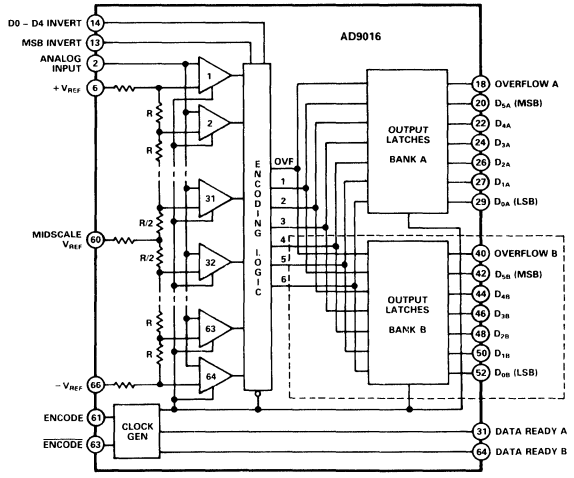
High Speed 6-Bit A/D Converters

AD9006/AD9016

FEATURES
500MSPS Encode Rate
Very Low Input Capacitance: 8pF
30dB SNR @ 200MHz Analog Input
MIL-STD-883 Available
Bipolar Input Range (±1V)
Demultiplexed Outputs (AD9016)

APPLICATIONS
Radar Warning Receivers
Electronic Countermeasures
Transient Recorders
"Smart" Munitions
Digital Oscilloscopes

AD9016 FUNCTIONAL BLOCK DIAGRAM



(Dotted Area Not Included in AD9006)

GENERAL DESCRIPTION

The AD9006 and AD9016 are 6-bit, ultrahigh speed analog-to-digital converters. Both are fabricated in an advanced bipolar process, assuring exceptionally wide analog input bandwidth, and encode rates up to 500MSPS. Functionally, the AD9006 and AD9016 use "flash" architecture; the outputs of 64 parallel comparator stages are decoded to drive a bank of ECL output latches.

The AD9006 features a bipolar analog input range (±1V). Output data is provided in a single 6-bit data bank; the data is ECL compatible and also includes complementary Data Ready signals and an overflow bit. ECL-level control pins allow the user to invert the MSB and/or LSBs. The AD9006 exhibits excellent SNR performance (30dB SNR @ 200MHz input), and requires less than two watts of power.

In the AD9016, the performance and features of the AD9006 are combined with on-board demultiplexing circuits. Output data of the AD9016 are demultiplexed to two 6-bit data banks, each of which includes a Data Ready signal and overflow bit.

The AD9006 and AD9016 are available as commercial temperature range devices: 0 to +70°C; and military temperature range devices: −55°C to +125°C. Both versions are offered in a ceramic 68-pin LCC, and a ceramic 68-pin leaded package. Military temperature range devices comply with MIL-STD-883.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ to Ground . . . . . −0.5V dc to +7.0V dc
AGND to DGND . . . . . −0.5V dc to +0.5V dc
$-V_S$ to Ground . . . . . +0.5V dc to −6.0V dc
ANALOG IN, $+V_{REF}$−V_{REF} . . . . . −1.5V to +1.5V
MIDSCALE V_{REF}[2]
$+V_{REF}$ to $-V_{REF}$ 2.1V
MIDSCALE V_{REF} Current . . . . . ±4mA
Digital Input Voltages . . . . . $-V_S$ to 0V
ENCODE to $\overline{\text{ENCODE}}$ 4V
Digital Output Current 20mA
HYSTERESIS Input . . . . . $-V_S$ to +3V
ANALOG $-V_S$ to DIGITAL $-V_S$ . . . . . ±0.5V
Operating Temperature Range
AD9006/AD9016KE/KZ . . . . . 0 to +70°C
AD9006/AD9016TE/TZ/883 . . . . . −55°C to +125°C
Maximum Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($+V_S = +5.0V$; $-V_S = -5.2V$; $+V_{REF} = +1V$; $-V_{REF} = -1V$, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9006/AD9016KE AD9006/AD9016KZ Min	Typ	Max	Sub-Group[4]	AD9006/AD9016TE/883 AD9006/AD9016TZ/883 Min	Typ	Max	Units
RESOLUTION			6				6			Bits
DC ACCURACY										
Differential Nonlinearity	+25°C	I		0.2	0.25	7		0.2	0.25	LSB
	Full	VI		0.25	0.5	8		0.25	0.5	LSB
Integral Nonlinearity	+25°C	I		0.2	0.25	7		0.2	0.25	LSB
	Full	VI		0.25	0.5	8		0.25	0.5	LSB
No Missing Codes	Full	VI	GUARANTEED			7, 8	GUARANTEED			
INITIAL OFFSET ERROR										
Top of Reference Ladder	+25°C	I		15	20	7		15	20	mV
	Full	VI			20	8			20	mV
Bottom of Reference Ladder	+25°C	I		14	20	7		14	20	mV
	Full	VI			20	8			20	mV
Offset Drift Coefficient	Full	V		20				20		µV/°C
ANALOG INPUT										
Input Voltage Range	Full	V		±1				±1		V
Input Bias Current[5]	+25°C	I		60	100	1		60	100	µA
	Full	VI			130	2, 3			130	µA
Input Resistance	+25°C	III	25	70		12	25	70		kΩ
Input Capacitance	+25°C	III		8	10	12		8	10	pF
Analog Bandwidth[6]	+25°C	V		550				550		MHz
REFERENCE INPUT										
Reference Ladder Resistance	+25°C	I	64	80	110	1	64	80	110	Ω
	Full	VI	50		135	1, 2, 3	50		135	Ω
Ladder Temperature Coefficient	Full	V		0.24				0.24		Ω/°C
Reference Input Bandwidth	Full	V		30				30		MHz
DYNAMIC PERFORMANCE[7]										
Conversion Rate	+25°C	I	470	500		4	470	500		MSPS
Aperture Delay (t_A)	+25°C	V		1.2				1.2		ns
Aperture Uncertainty (Jitter)	+25°C	V		3				3		ps
Output Delay (t_{OD})[8]	+25°C	I	2.7	3.6	4.4	9	2.7	3.6	4.4	ns
Output Rise Time	+25°C	I		1.3	1.5	9		1.3	1.5	ns
Output Fall Time	+25°C	I		1.3	1.5	9		1.3	1.5	ns
Output Time Skew[9]	+25°C	I		0.45	0.7	9		0.45	0.7	ns
Data Ready Output Delay (t_{DR})[10]										
AD9006	+25°C	I	2.7	3.2	4.4	9	2.7	3.2	4.4	ns
AD9016	+25°C	I	3	3.6	4.7	9	3	3.6	4.7	ns
Transient Response[11]	+25°C	V		1				1		ns
Overvoltage Recovery Time[12]	+25°C	V		1				1		ns

Parameter (Conditions)	Temp	Test Level	AD9006/AD9016KE AD9006/AD9016KZ Min	Typ	Max	Sub-Group[4]	AD9006/AD9016TE/883 AD9006/AD9016TZ/883 Min	Typ	Max	Units
ENCODE INPUT										
Logic "1" Voltage	Full	VI	−1.1			7, 8	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	7, 8			−1.5	V
Logic "1" Current	Full	VI			400	7, 8			400	μA
Logic "0" Current	Full	VI			200	7, 8			200	μA
Input Capacitance	+25°C	V		3				3		pF
Encode Pulse Width[13]	+25°C	I	1.0			4	1.0			ns
AC LINEARITY[14]										
Effective Number of Bits (ENOB)										
Analog Input @ 49MHz	+25°C	I	5.2	5.5		4	5.2	5.5		Bits
Analog Input @ 196MHz	+25°C	I	4.4	5.0		4	4.4	5.0		Bits
In-Band Harmonics										
Analog Input @ 9.3MHz	+25°C	I	42	48		4	42	48		dBc
Analog Input @ 49MHz	+25°C	I	38	44		4	38	44		dBc
Analog Input @ 92MHz	+25°C	I	33	36		4	33	36		dBc
Analog Input @ 145MHz	+25°C	I	33	36		4	33	36		dBc
Analog Input @ 196MHz	+25°C	I	31	36		4	31	36		dBc
Signal-to-Noise Ratio[15] (With Harmonics)										
Analog Input @ 9.3MHz	+25°C	I	34	37		4	34	37		dB
Analog Input @ 49MHz	+25°C	I	30	35		4	30	35		dB
Analog Input @ 92MHz	+25°C	I	30	34		4	30	34		dB
Analog Input @ 145MHz	+25°C	I	30	33		4	30	33		dB
Analog Input @ 196MHz	+25°C	I	29	32		4	29	32		dB
Signal-to-Noise Ratio[15] (Without Harmonics)										
Analog Input @ 9.3MHz	+25°C	I	36	37		4	36	37		dB
Analog Input @ 49MHz	+25°C	I	33	36		4	33	36		dB
Analog Input @ 92MHz	+25°C	I	33	36		4	33	36		dB
Analog Input @ 145MHz	+25°C	I	33	35		4	33	35		dB
Analog Input @ 196MHz	+25°C	I	31	34		4	31	34		dB
Two-Tone Intermodulation Distortion Rejection[16]	+25°C	V		50				50		dB
DIGITAL OUTPUTS[7]										
Logic "1" Voltage	Full	VI	−1.1			1, 2, 3	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	1, 2, 3			−1.5	V
POWER SUPPLY (AD9006)										
Positive Supply Current	+25°C	I		25	29	1		25	29	mA
($+V_S = +5.0V$)	Full	VI			30	2, 3			30	mA
Negative Supply Current	+25°C	I		320	380	1		320	380	mA
($-V_S = -5.2V$)	Full	VI			395	2, 3			395	mA
Nominal Power Dissipation	+25°C	V		1.7				1.7		W
Reference Ladder Dissipation	+25°C	V		50				50		mW
Power Supply Rejection Ratio[17]	Full	VI		2	4	7		2	4	mV/V
POWER SUPPLY (AD9016)										
Positive Supply Current	+25°C	I		25	29	1		25	29	mA
($+V_S = +5.0V$)	Full	VI			30	2, 3			30	mA
Negative Supply Current	+25°C	I		375	420	1		375	420	mA
($-V_S = -5.2V$)	Full	VI			450	2, 3			450	mA
Nominal Power Dissipation	+25°C	V		2.0				2.0		W
Reference Ladder Dissipation	+25°C	V		50				50		mW
Power Supply Rejection Ratio[17]	Full	VI		2	4	7		2	4	mV/V

For applications assistance, phone Computer Labs Division at (919) 668-9511.

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]$+V_{REF} > -V_{REF}$ under all circumstances.

[3]Typical thermal impedances:

68-pin leaded ceramic chip carrier $\theta_{JA} = 31°C/W$; $\theta_{JC} = 1.1°C/W$.

68-pin ceramic LCC $\theta_{JA} = 36°C/W$; $\theta_{JC} = 2.6°C/W$.

[4]Subgroups apply only to military qualified devices.

[5]Measured with analog input = 0V.

[6]Measured with use of Fast Fourier Transform (FFT). See Definitions.

[7]Outputs terminated through 100Ω to −2.0V; $C_L < 4pF$

[8]Measured from 50% point of leading edge of ENCODE command to −1.3V point of output data.

[9]Output time skew includes HIGH-to-LOW and LOW-to-HIGH transitions as well as bit-to-bit time skew differences.

[10]Measured from 50% point of trailing edge of ENCODE command to 50% point of Data Ready pulse.

[11]For full scale step input, 6-bit accuracy is attained in the specified time.

[12]Recovers to 6-bit accuracy in specified time after 150% full scale input overvoltage.

[13]ENCODE command rise/fall times should be less than 2.5ns for normal operation.

[14]Measured at 400MSPS encode rate; input level 1.0dB below full scale (FS).

[15]RMS signal to rms noise with analog input signal of 1dB below full scale at specified frequency.

[16]Intermodulation measured with analog input frequencies of 60MHz and 70MHz at 7dB below full scale.

[17]Measured at $+V_S = +5.0V \pm 5\%$ or $-V_S = -5.2V \pm 5\%$; specification shown is for worst case (see Definitions).

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF SUBGROUPS

Subgroup 1 – Static tests at +25°C. (5% PDA calculated against Subgroup 1 for high-rel versions)

Subgroup 2 – Static tests at maximum rated operating temperature.

Subgroup 3 – Static tests at minimum rated operating temperature.

Subgroup 4 – Dynamic tests at +25°C.

Subgroup 5 – Dynamic tests at maximum rated operating temperature.

Subgroup 6 – Dynamic tests at minimum rated operating temperature.

Subgroup 7 – Functional tests at +25°C.

Subgroup 8 – Functional tests at maximum and minimum rated temperatures.

Subgroup 9 – Switching tests at +25°C.

Subgroup 10 – Switching tests at maximum rated operating temperature.

Subgroup 11 – Switching tests at minimum rated operating temperature.

Subgroup 12 – Periodically sample tested.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3dB.

Aperture Delay (t_A)
The delay between the rising edge of the ENCODE command (or falling edge of $\overline{\text{ENCODE}}$) and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Output Delay (t_{DR})
The delay between the 50% point of the falling edge of the ENCODE command (or rising edge of $\overline{\text{ENCODE}}$) and the −1.3V point of the leading edge of the DATA READY pulse.

Differential Nonlinearity
The deviation of any code from an ideal 1LSB step.

Effective Number of Bits (ENOB)
Signal-to-noise ratio (see definition below) is expressed in dB; but can also be expressed in Effective Number of Bits (ENOB) if ENOB is related to full scale inputs as follows:

ENOB = (SNR −1.78)/6.02

ENOB is calculated with a sine wave curve fit method.

In-Band Harmonics
The rms value of the fundamental divided by the rms value of the worst of the first six harmonics.

Integral Nonlinearity
This specification (often called "linearity error") is the deviation of the transfer function from a reference line and is expressed in either % or ppm of full scale range, or in fractions of 1LSB. In the AD9006 and AD9016 devices, this spec is measured in fractions of 1LSB and uses a best-fit straight line determined by a least square curve fit.

Output Delay (t_{OD})
The delay between the 50% point of the rising edge of the ENCODE command (or falling edge of $\overline{\text{ENCODE}}$) and the −1.3V point of output data.

Output Time Skew
Bit-to-bit time variations among Bits D_0 to D_5 and the overflow bit. In the AD9006 and AD9016 specifications, time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 6-bit accuracy after an analog input overvoltage signal of 150% is reduced to the valid range of the converter.

Pipeline Delay
This is equal to one clock cycle and is the delay between the 50% points on the rising edges of two successive ENCODE commands (or falling edges of $\overline{\text{ENCODE}}$ commands).

Power Supply Rejection Ratio
The ratio of the change in power supply voltage to a corresponding change in input offset voltage. In the AD9006 and AD9016 units, $+V_S$ (+5V) or $-V_S$ (−5.2V) are within ±5% of their nominal values for this test. Value shown in SPECIFICATIONS is worst case.

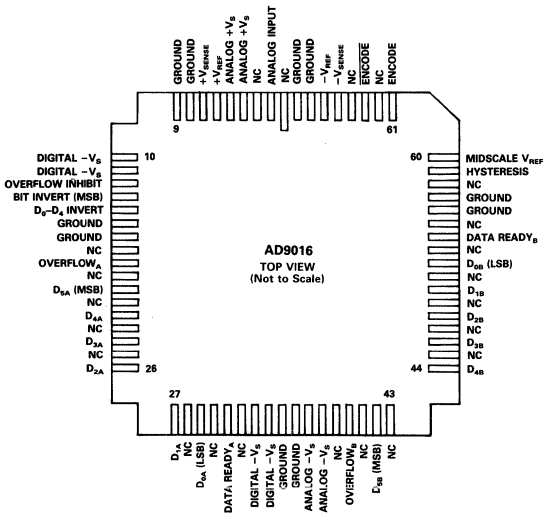
Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise", which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1dB below full scale.

Transient Response
The time required for the converter to achieve 6-bit accuracy when a full scale step function input is applied to the unit.

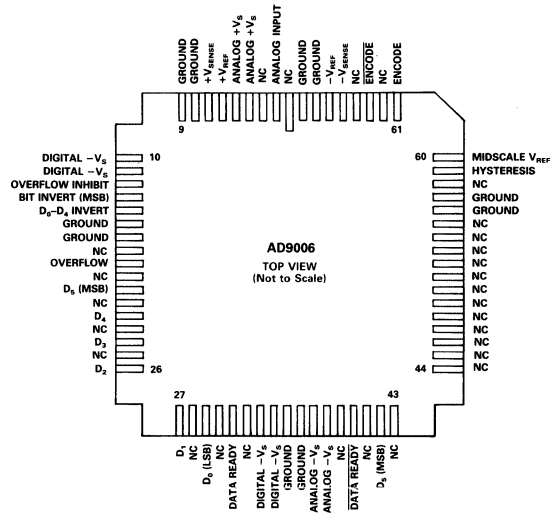
Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of a two-tone signal to the power of the strongest third-order IMD signal.

RECOMMENDED OPERATING CONDITIONS

	Input Voltage		
Parameter	**Min**	**Nominal**	**Max**
$+V_S$	+4.75	+5.00	+5.25
$-V_S$	−5.46	−5.20	−4.94
$+V_{REF}$	$-V_{REF}$	+1.0	+1.1
$-V_{REF}$	−1.1	−1.0	$+V_{REF}$
ANALOG INPUT	−1.0		+1.0



AD9016 Pin Designations



AD9006 Pin Designations

AD9006/AD9016 PIN DESCRIPTIONS

NC — Not internally connected.

ANALOG IN — Analog input connection. Analog input is nominally between −1.0V and +1.0V.

ANALOG $+V_S$ — Positive supply pins; nominally +5.0V.

$+V_{REF}$ — The positive reference voltage applied to the internal resistor ladder.

$+V_{SENSE}$ — Voltage sense line to the most positive reference voltage of the resistor ladder. The sense line is intended for connection to a high impedance node and has limited current capability. It is intended to be used to null offset at the top of the reference ladder.

GROUND — Analog and digital ground connections for the AD9006/AD9016 units. For optimum performance, all grounds should be connected together and to a low impedance ground plane as close to the device as possible. [NOTE: On both the AD9006 and the AD9016, Pins 8, 9, 15, 16, 35, 36, 56 and 57 are digital ground (DGND); pins 67 and 68 are analog ground (AGND).]

OVERFLOW INHIBIT — Overflow bit control pin. OVERFLOW INHIBIT is connected to ground for normal operation (no overflow bit, nonreturn-to- zero operation). When overflow inhibit is connected to −5.2V or allowed to float, OVERFLOW = HIGH and output bits = LOW when the analog input voltage exceeds $+V_{SENSE}$).

BIT INVERT (MSB) — Most significant bit (D_{05}) control pin. BIT INVERT (MSB) is connected to ground for normal operation. When connected to −5.2V or allowed to float, MSB output is inverted.

D_0–D_4 INVERT — Bits D_0–D_4 control pin, connected to ground for normal operation. When connected to −5.2V or allowed to float, D_0–D_4 data outputs are inverted.

$OVERFLOW_A$ — AD9016 only. Overflow data output for Data Bank "A." Logic HIGH indicates the analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).

D_{5A} — AD9016 only. Most significant bit (MSB) digital data output of Data Bank "A."

D_{1A}–D_{4A} — AD9016 only. D_{1A} through D_{4A} digital data outputs from Data Bank "A."

D_{0A} — AD9016 only. Least significant bit (LSB) digital data output of Data Bank "A."

$DATA\ READY_A$ — AD9016 only. Output Data of Bank "A" are valid at the rising edge of the DATA $READY_A$ pulse. Bank "A" carries every other sample of the A/D conversion; Bank "B" carries the remaining samples.

DIGITAL $-V_S$ — Negative digital supply pins, nominally −5.2V.

ANALOG $-V_S$ — Negative analog supply pins, nominally −5.2V.

$OVERFLOW_B$ — AD9016 only. Overflow data output for Data Bank "B." Logic HIGH indicates analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).

D_{5B} — AD9016 only. Most significant bit (MSB) digital data output of Data Bank "B."

D_{1B}–D_{4B} — AD9016 only. D_{1B} through D_{4B} digital data outputs of Data Bank "B."

D_{0B} — AD9016 only. Least significant bit (LSB) digital data output of Data Bank "B."

DATA READY$_B$	AD9016 only. Output data of Bank "B" are valid at the rising edge of the DATA READY$_B$ pulse. Bank "B" carries every other sample of the A/D conversion; Bank "A" carries the remaining samples.
HYSTERESIS	The hysteresis control voltage varies the amount of hysteresis in the internal comparators. This pin normally floats at −3.17V; making pin more positive increases the hysteresis of the internal comparators.
MIDSCALE V_{REF}	The midpoint tap on the internal reference ladder; can be connected to an external voltage to improve integral linearity of the A/D converter.
ENCODE	ECL-compatible noninverted input of the encode command. The conversion cycle begins on the rising edge of the ENCODE signal.
$\overline{\text{ENCODE}}$	ECL-compatible inverted input of the encode command, used when a differential encode signal is used. $\overline{\text{ENCODE}}$ should be tied to a voltage corresponding to the midpoint of the encode signal when a single-ended encode signal is used.
$-V_{SENSE}$	Voltage sense line to the most negative reference voltage of the resistor ladder. The sense line is intended for connection to a high impedance node and has limited current capability. It is intended to be used to null offset at the bottom of the reference ladder.
$-V_{REF}$	The negative reference voltage applied to the internal resistor ladder.
D_0	AD9006 only. Least significant bit (LSB) of the output data.
D_1–D_4	AD9006 only. D_1 through D_4 digital data outputs.
D_5	AD9006 only. Most significant bit (MSB) of digital data output.
OVERFLOW	AD9006 only. Overflow data output. Logic HIGH indicates the analog input is greater than $+V_{SENSE}$ when OVERFLOW INHIBIT pin is LOW (−5.2V).
DATA READY	AD9006 only. Output data are valid at the rising edge of the DATA READY pulse.
$\overline{\text{DATA READY}}$	AD9006 only. Output data valid at the falling edge of the $\overline{\text{DATA READY}}$ pulse.

THEORY OF OPERATION

Refer to the block diagram of the AD9016 A/D converter.

"Flash" architecture used in the AD9006 and AD9016 units makes it unnecessary to use a track-and-hold (T/H) ahead of the converter in many applications. The analog input signal is impressed across 64 parallel comparator stages.

Bias points of these comparators are established by the voltages applied to the reference ladder via $+V_{REF}$, MIDSCALE$_{REF}$ and $-V_{REF}$.

The outputs of the comparators are applied to the decoding logic; from here, the data are applied to output latches as six bits of digital data and an overflow bit. The overflow bit can be used to stack converters to obtain additional bits of resolution and can also be used as a "flag" for indicating positive out-of-range inputs.

Capturing output data at the (guaranteed) encode rates of 470MSPS of the AD9016 is simplified by virtue of using two Data Ready pulses. Output data words alternate between Bank A and Bank B; this allows clocking demultiplexed data from the AD9016 at half the converter's sample rate.

The Data Ready pulses track the propagation delay of the output data and relieve the need to build an external clock circuit for tracking prop delay over the full operating temperature range.

Demultiplexed ports connected to Bank A and Bank B allow the user to capture output data with 100K ECL logic even when the converter is operating at 470MSPS. The AD9016 introduces only one pipeline delay in the processing of these digital output data, thereby reducing the number of clock cycles required to obtain the digital representation of the analog input at the appropriate output port.

The analog input voltage range is determined by the user-supplied voltage references: $+V_{REF}$ and $-V_{REF}$. The references can be adjusted between −1V and +1V. In all cases, $+V_{REF}$ should be greater than $-V_{REF}$; and the differential voltage between the references should not exceed 2.1V. MIDSCALE V_{REF} can be used to improve the integral linearity of the converter.

Another attractive feature of the analog input characteristics of the AD9016 is its low input capacitance of 8pF. In many other flash converters, this value is three or four times larger, making them difficult to drive at high input frequencies.

For those applications in which a single output port is preferred, the recommended choice is the AD9006 A/D converter.

The AD9006 is identical to the AD9016 in performance specifications; it is best suited for systems in which demultiplexing is not performed immediately after the flash converter. As in the AD9016, the AD9006 produces Data Ready pulses on chip; these can be used to clock external latches.

There are two control pins for determining the format of the output data on the AD9006/AD9016. BIT INVERT (MSB) allows the user to invert the most significant bit ($D0_5$); and D_0–D_4 INVERT allows the five least significant bits to be inverted. The AD9006/AD9016 Truth Table elsewhere in the data sheet provides the necessary information to select among binary, inverted binary, twos complement and inverted twos complement coding schemes.

The OVERFLOW INHIBIT pin controls the overflow bit (called out as OVERFLOW BIT in the AD9006, and OVERFLOW$_A$ and OVERFLOW$_B$ in the AD9016). In normal operation, the OVERFLOW INHIBIT is connected to −5.2V, and OVERFLOW will be a digital HIGH whenever the analog input voltage exceeds the most positive comparator reference ($+V_{SENSE}$). The digital outputs (D_0– D_5) will be LOW, i.e., returned-to-zero operation.

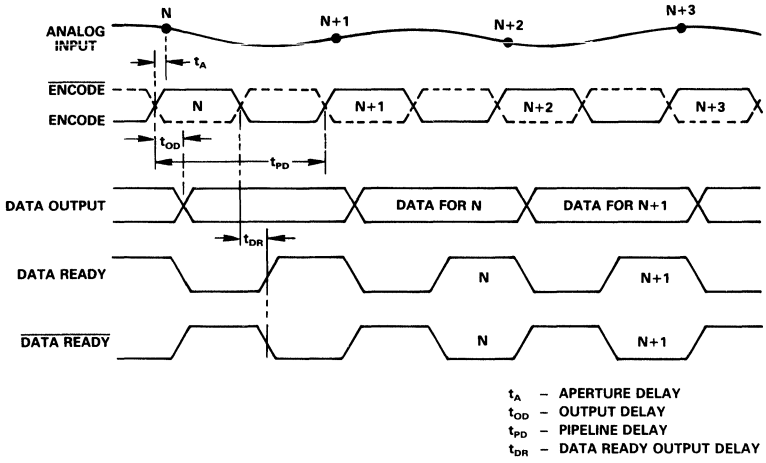
This feature means two AD9006 devices can be cascaded or "stacked" to obtain seven-bit operation, as shown in the diagram below.

Connecting OVERFLOW INHIBIT to ground forces the overflow bit to remain low and disables the return-to-zero operation.

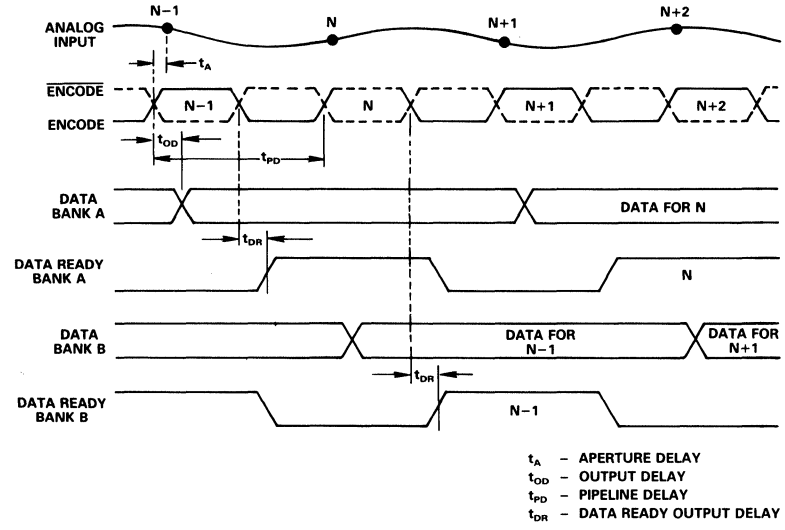
Timing for the AD9006 and AD9016 is shown in their respective timing diagrams. In both illustrations, the complementary encode command is shown in dashed lines.

The DATA READY and $\overline{\text{DATA READY}}$ pulses of the AD9006 correspond, respectively, to the DATA READY BANK A and DATA READY BANK B pulses of the AD9016. As shown in the SPECIFICATIONS table, Data Ready Output Delay is slightly different in the two units: 3.2ns in the AD9006 and 3.6ns in the AD9016.

Availability and timing of a DATA READY pulse help in retrieving data from either the AD9006 or the AD9016. When setting system timing, the user simply takes into account the (single) pipeline delay and the Data Ready Output Delay (3.2ns in the AD9006; 3.6ns in the AD9016) and uses the next DATA READY (or $\overline{\text{DATA READY}}$ in the AD9006) to strobe the desired output into external circuits.



AD9006 Timing Diagram



AD9016 Timing Diagram

APPLYING THE AD9006/AD9016

Setting Reference Levels

The AD9006/AD9016 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$. These two voltages are applied across the internal resistor ladder (nominally 80Ω) and determine the analog input range of the converter.

Care should be taken to assure that these references are driven from stable, low impedance sources. Reference connections should be capacitively coupled to ground to reduce interference generated by noise and/or digital switching.

Resistance between the reference connections and the point at which the first comparator threshold is connected causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled out using the $+V_{SENSE}$ and $-V_{SENSE}$ connections. These sense lines are intended for connection only to high impedance (low current) nodes such as the input of an op amp.

Applying a voltage greater than 2.1V across the internal resistor ladder will cause current densities to exceed rated values and may cause permanent damage to the AD9006/AD9016.The amount of current available at the reference connections must be limited.

One method of nulling the offset errors is shown in Figure 1.

The Analog Devices AD1403 voltage reference supplies a stable 2.5V reference for the circuit, and R_{LIMIT} determines the range over which the reference can be adjusted. R_1 adjusts the voltage at the top of the internal reference ladder through the AD642/2N3904 combination. Feedback from the $+V_{SENSE}$ line causes the op amp to compensate for offset which appears at the top comparator threshold. The transistor limits the amount of current drawn directly from the op amp; resistors at the base and emitter of the transistor stabilize its operation.

Voltage at the bottom of the reference ladder is controlled in essentially the same way, using R_2 to adjust the reference ladder voltage; and using feedback from the $-V_{SENSE}$ connection to null any offset between the reference and the threshold of the bottom comparator.

The midpoint of the comparator reference ladder (MIDSCALE V_{REF}) is shown tied to ground in Figure 1. This allows the user to adjust the voltage reference for minimum integral nonlinearity. This feature becomes important in applications with reduced analog input ranges because integral nonlinearity increases under these conditions.

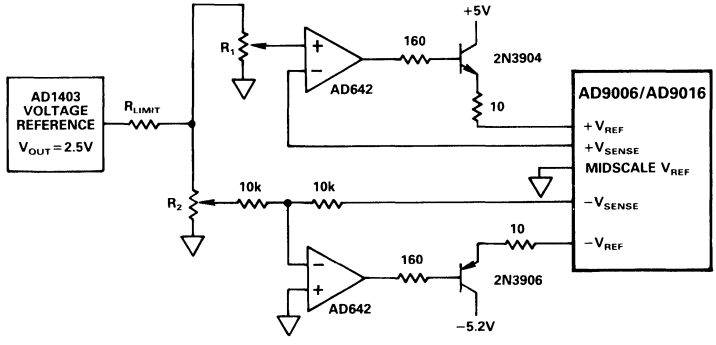


Figure 1. Reference Circuit

Driving the Analog Input

Careful design and layout of the AD9006/AD9016 have resulted in a typical input capacitance of 8pF (9.5pF max). This is low in comparison to most flash converters, but it is still a significant load at high input frequencies and must be taken into account when choosing a drive amplifier.

DC-coupled applications require the performance characteristics of a wide bandwidth, low distortion op amp such as the Analog Devices AD9611. AC-coupled applications at high frequencies may be better served by using a low distortion gain block for the driver.

Figure 2 illustrates possible connections for both approaches.

Regardless of which driving circuit is selected for the application, the overall dynamic performance of the amplifier is enhanced by inserting a small series resistor between the output of the amplifier and the analog input of the converter.

Clocking the Converter

The encode command circuits of the AD9006/AD9016 (ENCODE and $\overline{\text{ENCODE}}$) are designed to be driven by a differential ECL source.

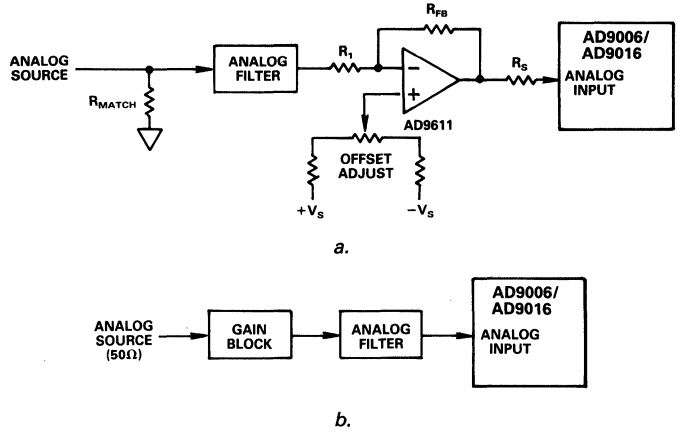


Figure 2. Analog Input Circuits

A differential signal is recommended as the encode command to reduce jitter of the encode signal; increased jitter raises the noise floor of the converter. Full logic levels are preferred for triggering the clock circuits, but reduced levels can also be used. Caution should be exercised when using reduced-level encode commands because their slew rates will be decreased, which can raise the noise floor.

Refer again to the timing diagrams for the AD9006 and AD9016.

The rising edge of the ENCODE signal initiates the conversion process in the AD9006 unit. This same signal, delayed, becomes the DATA READY and complementary $\overline{\text{DATA READY}}$ pulses. Fast rise and fall times (<0.5ns) and "clean" edges are always required for encode commands, but are especially critical for high frequency analog signals.

In the AD9016, the leading edges of the DATA READY_A and DATA READY_B pulses are triggered by the trailing edge of an ENCODE command. Their trailing edges are triggered by the trailing edge of the next ENCODE command.

Although the AD9006/AD9016 is designed and tested to operate with a 50% duty cycle, the dynamic performance at high encode rates can be improved by changing the duty cycle.

Two possible methods of clocking the AD9006/AD9016 are shown in Figure 3. Users planning to implement these circuits need to be aware they may not function over the same temperature ranges possible with the converters.

Both ECL oscillators and saw filter oscillators are available as comercial products, with each type operating at some preselected frequency. The type of oscillator which is selected is a function of the desired operating frequency for the circuit being designed.

Layout and Power Supplies

Correct layout of high speed circuits is always critical, but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as practical, and be properly terminated to avoid reflections and signal distortions. The analog input and voltage references should be kept away from digital signal paths; this reduces the possibility of capacitvely coupling digital switching noise into the analog section of the circuit.

Digital signal paths should also be kept short, and digital run lengths should be matched because propagation delays through digital paths become significant at high data rates. Proper ECL terminations should be used at or near the packages containing successive gates.

Ideally, analog signal paths and digital signal paths should be routed as far away from one another as possible and should never closely parallel one another's paths. If they must cross, they should do so at right angles to avoid interference.

In any layout of high speed circuits, the layout of ground connections is the most important factor. To reduce noise and interference on the circuit ground, a double-sided copper-clad printed circuit board (PCB) is recommended. Every part of the board not used for components or conducting runs should be ground plane. Components are mounted on one side; the opposite side is used for power and signal connections.

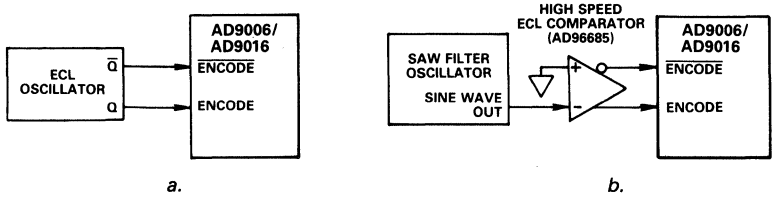


Figure 3. Clock Circuits

It is especially important to retain the continuity of the ground plane under and around the AD9006/AD9016 converter. If the system design separates the digital and analog ground returns, both should be connected together and to ground close to the unit to form a continuous ground plane around the A/D section of the system.

Low noise, low ripple temperature-stable linear power supplies are the preferred choices for high speed circuits. Switching power supplies often seem to meet these criteria, including ripple specifications. *But ripple specs are generally expressed in terms of rms* – and the spikes generated in switchers can produce hard-to-filter, uncontrollable noise peaks with amplitudes of several hundred millivolts. Their high frequency components may be extremely difficult to keep out of the ground system.

If switching power supplies cannot be avoided for high speed designs, they should be *carefully* shielded and their outputs should be well filtered.

Every power supply line leading into a high speed PCB or data acquisition circuit must be carefully bypassed to its ground return to prevent noise from entering the circuit. Ceramic capacitors, ranging in value from 0.01μF to 0.1μF, should be used generously in the layout, mounted as closely as possible to the device or circuit being bypassed.

The capacitors which are used should have a high resonant frequency to insure they maintain their characteristics in the range of frequencies involved in the encoding process. Ceramic surface mount (chip) capacitors meet that requirement and are easily placed near the package connections.

At least one high quality tanatalum capacitor of 3μF– 20μF should be assigned to each power supply voltage, mounted as near as possible to the incoming power pins to minimize low frequency ripple.

Handling the AD9006/AD9016 Package

Several precautions have been included in the design of the AD9006/AD9016 converter to help reduce its sensitivity to electrostatic discharge (ESD). But the user should always use normal ESD precautions to help insure device reliability and avoid degrading the unit's performance.

Package options which are available include both leaded and leadless 68-pin ceramic chip carriers; these are shown in the data sheet as leaded ceramic chip carrier and leadless chip carrier (LC), respectively. Both of these packages have been specially designed to maintain the converter's high frequency parameters while operating over a standard military temperature range.

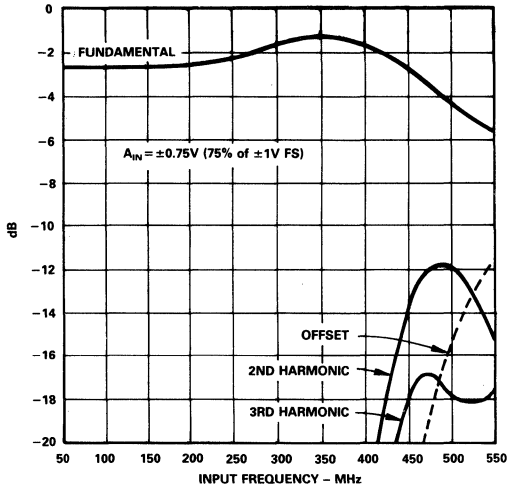
Regardless of package type, the top of the package (containing the model number and the Analog Devices logo) is internally connected to the device substrate and is designed to be used as a heat sink. The substrate is connected to $-V_S$ internally; therefore the top of the package should be allowed to "float" in voltage. The bottom of the package is not connected internally on the device.

High speed devices such as the AD9006/AD9016 converters should be soldered into final applications. There is a temptation to use sockets, but they can limit dynamic performance and should be used only for evaluation or prototype applications.

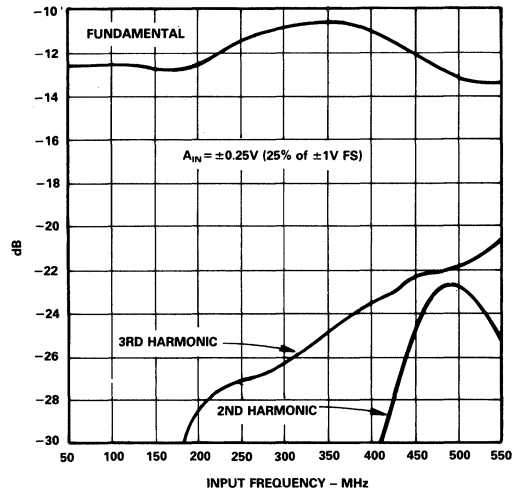
Step	Input Voltage (FS = ±1.0V)	Binary		Offset Twos Complement	
		True	Inverted	True	Inverted
		MSB INVERT = 1 D_0–D_4 INV = 1	MSB INVERT = 0 D_0–D_4 INV = 0	MSB INVERT = 0 D_0–D_4 INV = 1	MSB INVERT = 1 D_0–D_4 INV = 0
00	−1.000	000000	111111	100000	011111
01	−0.968	000001	111110	100001	011110
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
31	−0.031	011111	100000	111111	000000
32	0.000	100000	011111	000000	111111
33	+0.031	100001	011110	000001	111110
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
62	+0.938	111110	000001	011110	100001
63	+0.969	111111	000000	011111	100000
63+	+1.000	(0)111111*	(0)000000*	(0)011111*	(0)100000*
		(1)000000#	(1)111111#	(1)100000#	(1)011111#

*OVERFLOW INHIBIT = "1"; #OVERFLOW INHIBIT = "0."
The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT, D_0–D_4 INVERT and OVERFLOW INHIBIT are considered dc controls. They are tied to ground for logic "1" and $-V_S$ for logic "0"; their "trip point" occurs at approximately −1.3V.

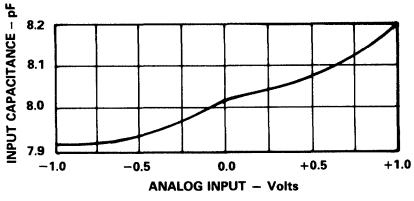
AD9006/AD9016 Truth Table



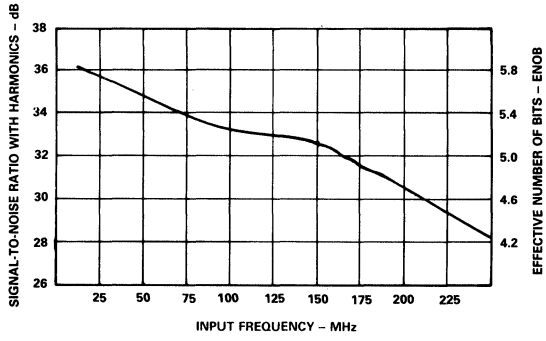
Harmonics vs. Input Frequency – Large Signal



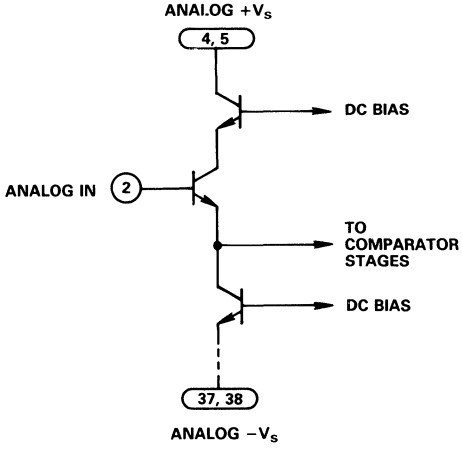
Harmonics vs. Input Frequency – Small Signal



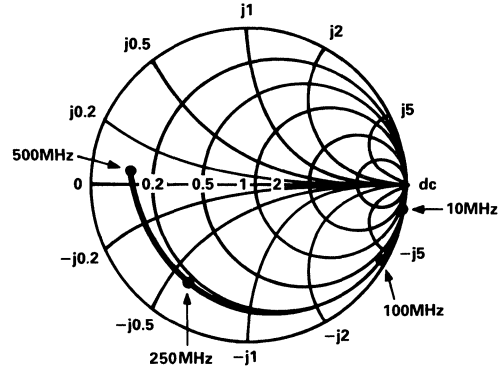
Input Capacitance vs. Input Voltage



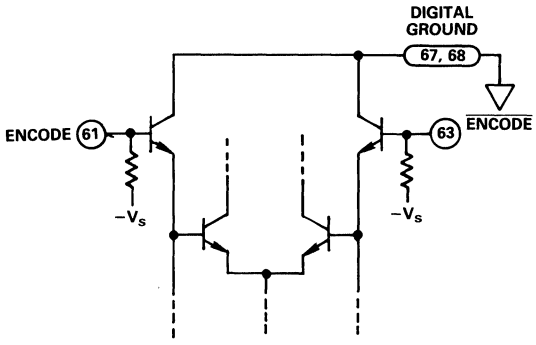
SNR and Effective Number of Bits (ENOB) vs. Input Frequency



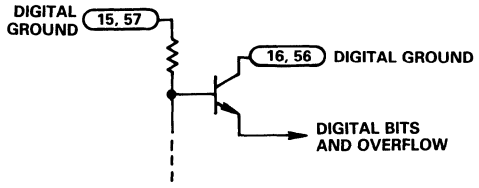
Equivalent Analog Input



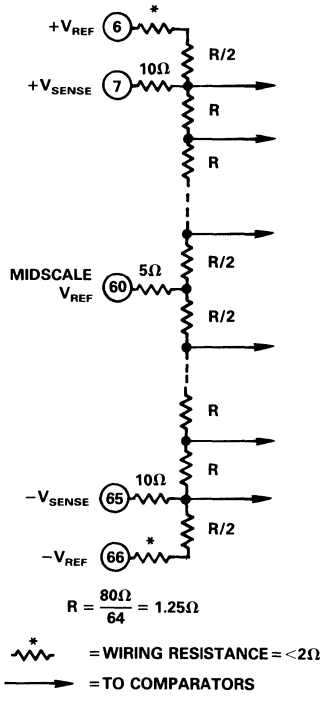
Normalized 50Ω Input Impedance vs. Input Frequency



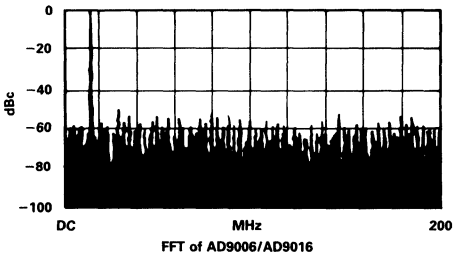
Encode and $\overline{\text{Encode}}$ Equivalent Circuits



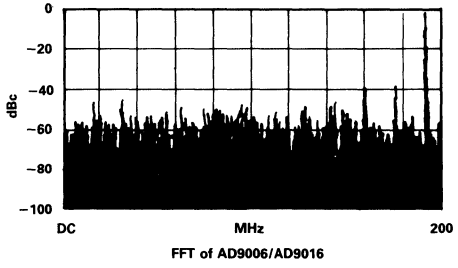
Equivalent Digital Outputs



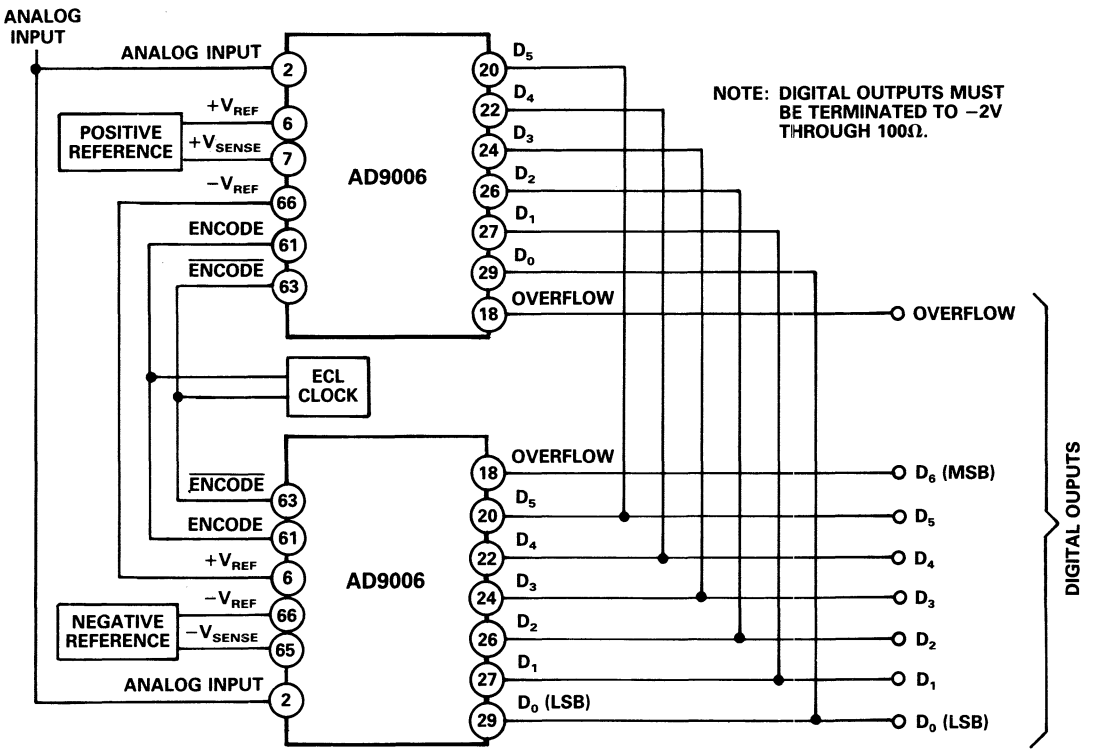
Reference Ladder



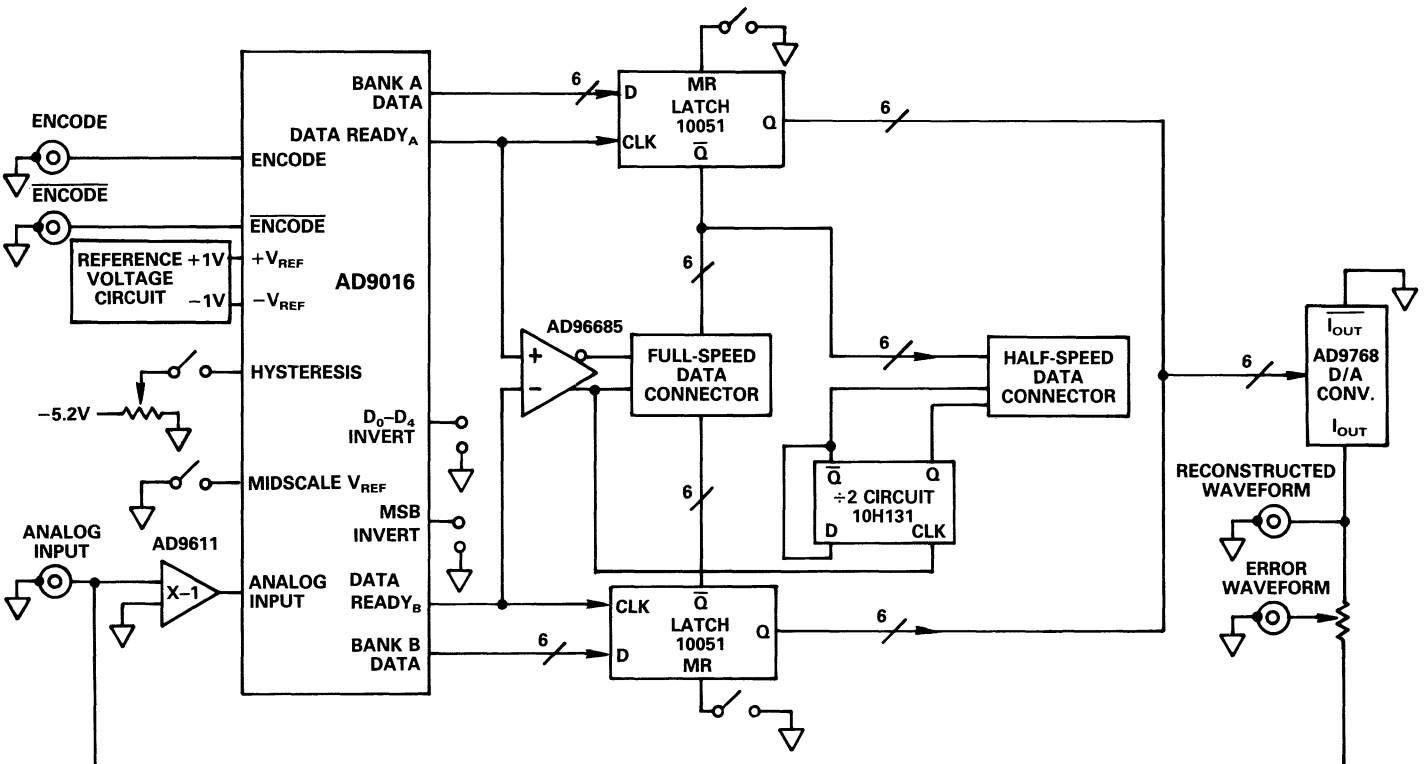
400MSPS: F_{IN} = 14.8MHz; V_{IN} = 1.0dB Below FS



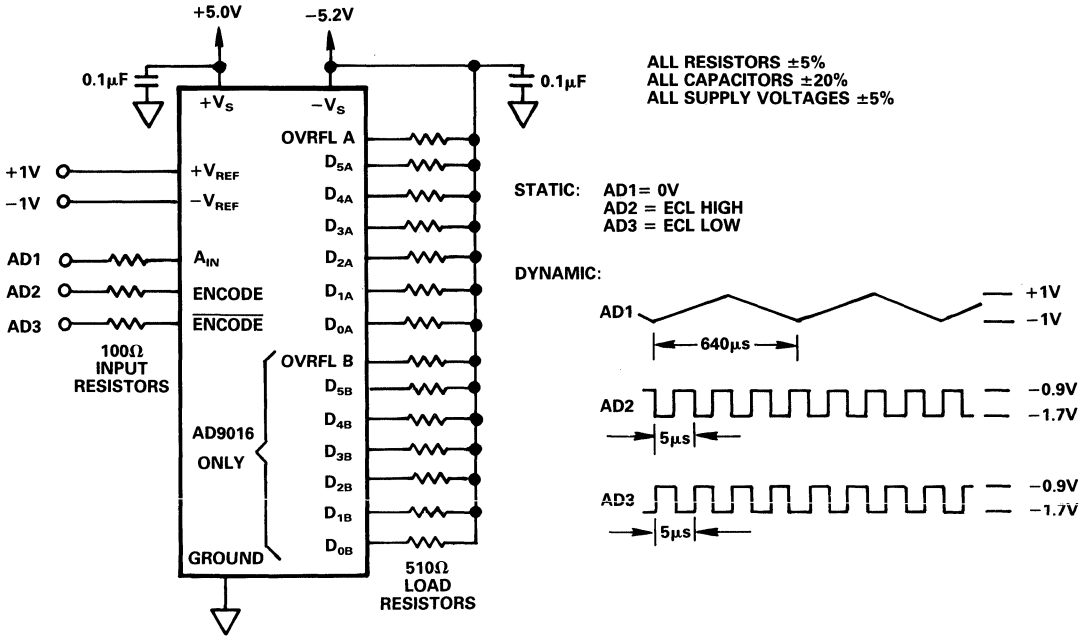
400MSPS: F_{IN} = 192MHz; V_{IN} = 1.0dB Below FS



Connections for 7-Bit Operation



AD9016/PCB Block Diagram



AD9006/AD9016 Burn-In Diagram

MIL-STD-883 Compliance Information

The AD9006/AD9016TE/TZ/883 devices are classified within Microcircuits Group 57, Technology Group D (bipolar A/D converters) and are constructed in accordance with MIL-STD-883. The AD9006/AD9016 are electrostatic sensitive and fall within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.

ORDERING INFORMATION

Model	Temperature	Description	Package Options*
AD9006KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9006KZ	0 to +70°C	68-Pin Leaded Ceramic Chip Carrier	Z-68
AD9016KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9016KZ	0 to +70°C	68-Pin Leaded Ceramic Chip Carrier	Z-68
AD9006TE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9006TZ/883	−55°C to +125°C	68-Pin Leaded Ceramic Chip Carrier	Z-68
AD9016TE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9016TZ/883	−55°C to +125°C	68-Pin Leaded Ceramic Chip Carrier	Z-68
AD9016KE/PCB	0 to +70°C	Evaluation Board; AD9016KE Installed	
AD9016/PCB	0 to +70°C	Evaluation Board; No Converter	

*See Section 14 for package outline information.

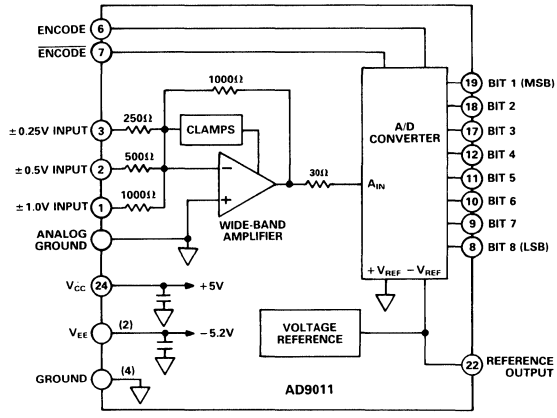
8-Bit, 100MSPS A/D Converter

AD9011

FEATURES
On-Board Amplifier and Reference
100MSPS Encode Rate
Internal Input Clamping Circuit
Multiple Gain Selection
Bipolar Inputs

APPLICATIONS
Radar Guidance
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)

AD9011 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9011 is a high-speed 8-bit A/D converter which includes an amplifier and a voltage reference in the same package. The integration of these functions in one package optimizes dynamic performance while saving board space and design time.

The current-feedback amplifier in the AD9011 features an 80MHz bandwidth at gains of −1, −2 and −4. Voltage gain is selectable by applying the input signal to different pins. Internal clamping circuits protect the input of the A/D converter while still maintaining fast overvoltage recovery times. The AD9011 also includes a voltage reference with a drift of less than 40ppm/°C, providing accurate operation over the full temperature range.

An 8-bit A/D converter performs the high speed digitizing function within the AD9011. Fabricated in an advanced bipolar process, this ADC provides excellent dynamic performance at low power. The digital outputs are ECL compatible.

The AD9011 is available in two grades, one with 0.5LSB linearity and one with 0.75LSB linearity. Both versions are offered as a commercial temperature range device, 0 to +70°C, and as an extended temperature device, −55°C to +125°C. All grades are packaged in a 24-pin metal DIP package.

ORDERING INFORMATION

Device	Linearity	Temperature Range	Description	Package Options*
AD9011JM	0.75LSB	0 to +70°C	24-Pin DIP	M-24A
AD9011KM	0.5LSB	0 to +70°C	24-Pin DIP	M-24A
AD9011SMB	0.75LSB	−55°C to +125°C	24-Pin DIP	M-24A
AD9011TMB	0.5LSB	−55°C to +125°C	24-Pin DIP	M-24A

*See Section 14 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage (V_{CC}) . . . . . +6V
Negative Supply Voltage (V_{EE}) . . . . . −6V
Analog Input Voltage (Pin 1) . . . . . ±3V
Analog Input Voltage (Pin 2) . . . . . ±1.5V
Analog Input Voltage (Pin 3) . . . . . ±0.75V
Digital Input Voltage . . . . . V_{EE} to 0V
ENCODE to $\overline{\text{ENCODE}}$ Differential Voltage 4V
Digital Output Current 20mA
Reference Output Current 20mA
Package Dissipation Limit (+25°C Free Air)[2] 3.3W
Operating Temperature Range
AD9011JM/KM (Case) . . . . . 0 to +70°C
AD9011SMB/TMB (Case) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +165°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{EE} = −5.2V, G = −1, unless otherwise stated)

Parameter	Test Level	Temp	AD9011JM/AD9011KM Min	Typ	Max	AD9011SMB/AD9011TMB Min	Typ	Max	Units
RESOLUTION	IV	Full	8			8			Bits
STATIC ACCURACY									
Differential Nonlinearity AD9011JM/SMB	I	+25°C		0.6	0.75		0.6	0.75	LSB
	VI	Full			1.0			1.0	LSB
AD9011KM/TMB	I	+25°C		0.4	0.5		0.4	0.5	LSB
	VI	Full			0.75			0.75	LSB
Integral Noninearity AD9011JM/SMB	I	+25°C		0.6	1.0		0.6	1.0	LSB
	VI	Full			1.2			1.2	LSB
AD9011KM/TMB	I	+25°C		0.4	0.5		0.4	0.5	LSB
	VI	Full			1.2			1.2	LSB
No Missing Codes	VI	Full	GUARANTEED			GUARANTEED			
Gain Error	I	+25°C		±0.2	±1.0		±0.2	±1.0	%FS
	VI	Full		±0.3	±1.0		±0.5	±2.5	%FS
Offset Error[3]	I	+25°C			±4			±4	mV
	VI	Full		±6	±13		±10	±24	mV
ANALOG INPUT									
Input Voltage Range Pin 1 (G = −1)	V	Full		2			2		V p-p
Input Voltage Range Pin 2 (G = −2)	V	Full		1			1		V p-p
Input Voltage Range Pin 3 (G = −4)	V	Full		0.5			0.5		V p-p
Input Resistance G = −1, −2, −4	V	+25°C		1kΩ/|G|			1kΩ/|G|		Ohms
Input Capacitance	IV	+25°C		2	5		2	5	pF
Large Signal Input Bandwidth (−3dB)[4]	V	+25°C		80			80		MHz
DYNAMIC CHARACTERISTICS[5,6]									
Maximum Conversion Rate	I	+25°C	100			100			MHz
Output Data Delay[7]	V	+25°C		3.7			3.7		ns
Aperture Delay	V	+25°C		−1.6			−1.6		ns
Aperture Uncertainty	V	+25°C		15			15		ps
Transient Response (to ±1LSB)[8]	V	+25°C		11			11		ns
Overvoltage Recovery Time (to ±1LSB)[9]	V	+25°C		20			20		ns
Output Rise Time	IV	+25°C			3.0			3.0	ns
Output Fall Time	IV	+25°C			2.5			2.5	ns
Output Time Skew[10]	V	+25°C		0.6			0.6		ns
In-Band Harmonics[11]									
F_{IN} = 1.248MHz, FS − 1dB	V	+25°C		60			60		dBc
F_{IN} = 2.438MHz, FS − 1dB	V	+25°C		58			58		dBc
F_{IN} = 9.3MHz, FS − 1dB	I	+25°C	46	50		46	50		dBc
Signal-to-Noise Ratio[12]									
F_{IN} = 1.248MHz, FS − 1dB	V	+25°C		47			47		dB
F_{IN} = 2.438MHz, FS − 1dB	V	+25°C		47			47		dB
F_{IN} = 9.3MHz, FS − 1dB	I	+25°C	40	43		40	43		dB
ENCODE INPUT									
Logic "1" Voltage[13]	VI	Full	−1.1			−1.1			V
Logic "0" Voltage[13]	VI	Full			−1.5			−1.5	V
Logic "1" Current	VI	Full			150			150	μA
Logic "0" Current	VI	Full			120			120	μA
Input Capacitance	V	+25°C		3			3		pF
Encode Pulse Width (Low)	IV	+25°C	2			2			ns
Encode Pulse Width (High)	IV	+25°C	2			2			ns

Parameter	Test Level	Temp	AD9011JM/AD9011KM Min	Typ	Max	AD9011SMB/AD9011TMB Min	Typ	Max	Units
DIGITAL OUTPUTS									
Logic "1" Voltage	VI	Full	−1.1			−1.1			V
Logic "0" Voltage	VI	Full			−1.5			−1.5	V
POWER SUPPLY									
Supply Voltage V_{CC}	VI	Full	4.75	5.0	5.25	4.75	5.0	5.25	V
Supply Voltage V_{EE}	VI	Full	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	V
Supply Current V_{CC}	VI	Full		63	72		63	72	mA
Supply Current V_{EE}	VI	Full		240	303		240	303	mA
Nominal Power Dissipation	VI	Full		1.56	1.95		1.56	1.95	W

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute rating conditions for extended periods of time may affect device reliability.

[2]Package dissipation limit . . .

$$\text{PD (watts)} = \frac{t_{J\,max} - t_A}{\theta_{JA}} = \frac{t_{J\,max} - t_C}{\theta_{JC}}$$

Where t_A = ambient; t_C = case; t_J = junction 24-pin metal DIP $\theta_{JA} = 41.7°C/W$; $\theta_{JC} = 7.7°C/W$.

[3]Unused analog inputs floating.

[4]Determined by 3dB reduction in reconstructed output. For under sampled applications only, not meant to imply Nyquist operation.

[5]Outputs terminated with 100Ω resistors to −2.0V.

[6]Measured at 100MHz encode rate.

[7]Measured from ENCODE in to data out for LSB only.

[8]For full-scale step input, 8-bit accuracy is attained in the specified time.

[9]Recovers to 8-bit accuracy in specified time, after 150% full scale input overvoltage.

[10]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[11]Harmonic content below signal.

[12]RMS signal to RMS noise, including harmonics.

[13]ENCODE and $\overline{\text{ENCODE}}$ are differential inputs which must be driven concurrently. ECL inputs within the specified ranges are guaranteed to produce normal switching. ENCODE rise and fall time should be less than 10ns for normal operation.

Specifications subject to change without notice.

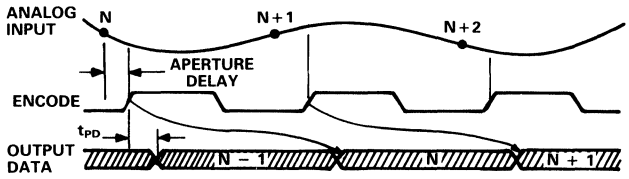
EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.
Test Level II – 100% production tested at +25°C, and sampled tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices.

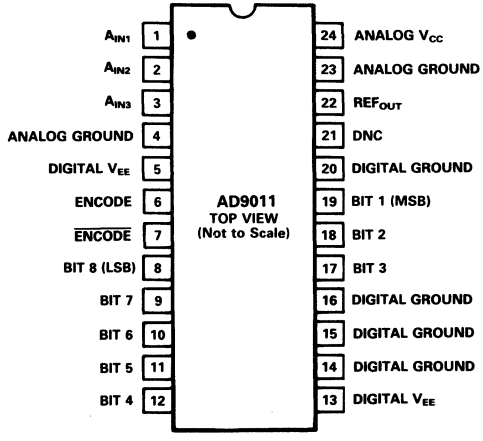
FUNCTIONAL DESCRIPTION

Pin No.	Name	Description
1	ANALOG INPUT	Analog input with internal gain of −1. Input signal should be ≤2V p-p. Unused analog inputs should be grounded.
2	ANALOG INPUT	Analog input with internal gain of −2. Input signal should be ≤1V p-p. Unused analog inputs should be grounded.
3	ANALOG INPUT	Analog input with internal gain of −4. Input signal should be ≤0.5V p-p. Unused analog inputs should be grounded.
4	ANALOG GROUND	One of two analog ground pins. All ground pins should be connected together near the AD9011.
5	V_{EE}	Negative analog supply pin. Nominally −5.2V. Best performance is attained with separate analog and digital supplies.
6	ENCODE	Noninverted input of the differential encode inputs. This pin is driven in conjunction with $\overline{\text{ENCODE}}$.
7	$\overline{\text{ENCODE}}$	Inverted input of the differential encode inputs. This pin is driven in conjunction with ENCODE.
8	BIT 8 (LSB)	Least Significant Bit (LSB) of digital data output.
9 – 12	BIT 7 – BIT 4	Digital data output.
13	V_{EE}	Negative digital supply pin. Nominally −5.2V. Best performance is attained with separate analog and digital supplies.
14 – 16	DIGITAL GROUND	Three of four digital ground pins. All ground pins should be connected together near the AD9011.
17, 18	BIT 3, BIT 2	Digital data output.
19	BIT 1 (MSB)	Most Significant Bit (MSB) of digital data output.
20	DIGITAL GROUND	One of four digital ground pins. All ground pins should be connected together near the AD9011.
21	DNC	Do not connect. Internal test point.
22	REF_{OUT}	Output of internal reference. −2V output @ +12mA (max).
23	ANALOG GROUND	One of two analog ground pins. All ground pins should be connected together near the AD9011.
24	V_{CC}	Positive analog supply pin. Nominally +5.0V.

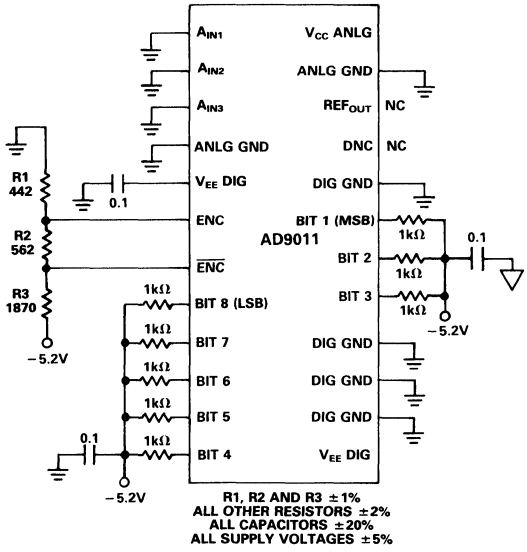
TIMING DIAGRAM



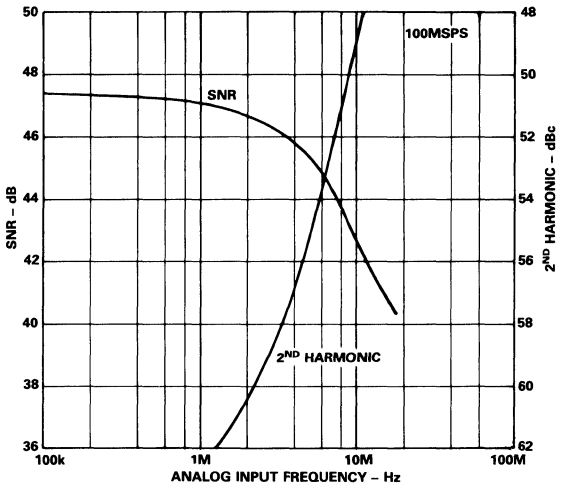
PIN DESIGNATIONS



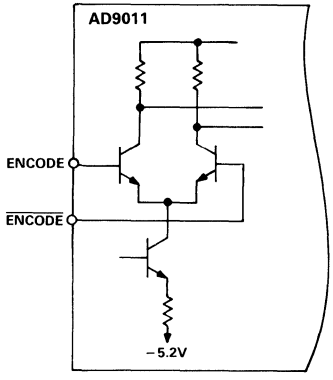
BURN-IN DIAGRAM

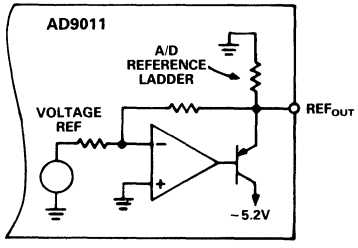


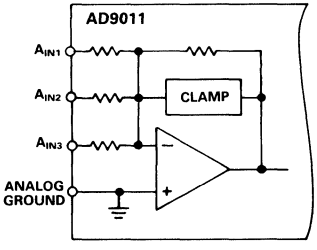
SIGNAL-TO-NOISE RATIO

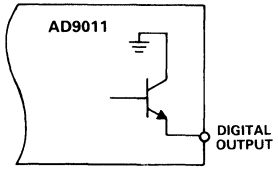


INPUT/OUTPUT CIRCUITS









APPLICATION INFORMATION

Input signals to the AD9011 are buffered through the on-board amplifier/driver. Three separate input pins provide gains of −1, −2 and −4. Only one input pin is used at a time, with the other two pins connected to the analog ground. On-board input clamping circuitry protects the internal flash A/D converter from overvoltage inputs, but the input signal to the AD9011 should not exceed the absolute maximums listed in the specifications.

The AD9011 employs a differential encode input which requires a drive signal to both the ENCODE and the $\overline{\text{ENCODE}}$ pins. All levels are fully ECL compatible, and proper ECL terminations should be used to avoid ringing and reflection.

The output data is buffered through the ECL compatible output latches. All data is delayed by one clock cycle, in addition to the latch propagation delay (t_{PD}), before becoming available at the outputs. Both the analog-to-digital conversion cycle and the data transfer to the output latches, are triggered on the rising edge of the ECL compatible ENCODE signal (see timing diagram).

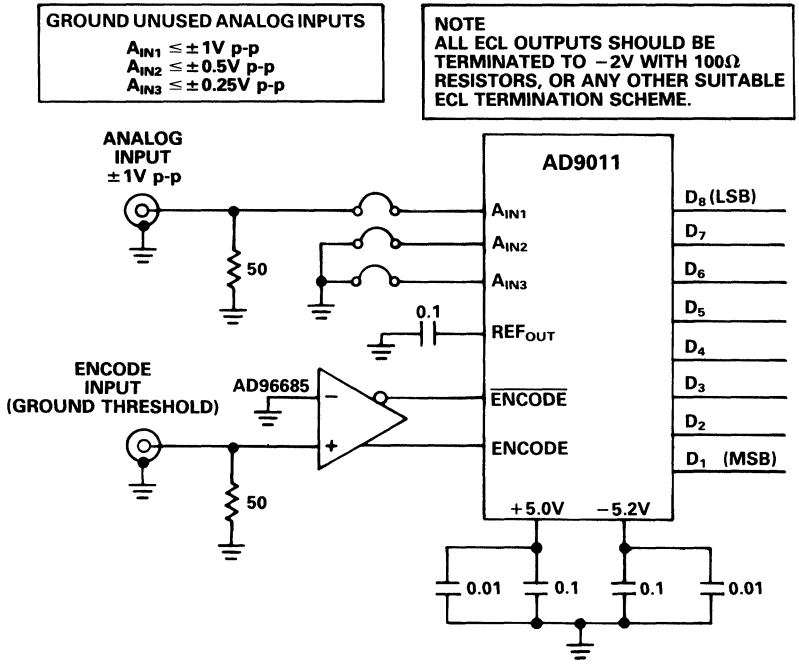
Dramatic improvements in comparator design and construction give the AD9011 excellent dynamic characteristics. The AD9011 provides outstanding error rate performance. Gross error codes occur less than once in every 10^{12} conversion cycles. This is largely due to tight control of comparator offset matching. The 80MHz input bandwidth and low error rate performance give the AD9011 an SNR (signal-to-noise ratio) of 43dB+ with a 9.3MHz input. High SNR performance is particularly important in video bandwidth applications, where signals may pass through the converter several times before the processing is complete. Pulse signature analysis, commonly performed in advanced radar receivers, is another area that is especially dependent on high quality dynamic performance.

LAYOUT SUGGESTIONS

Designs using the AD9011, like all high-speed devices, must follow a few basic layout rules to insure optimum performance. Essentially, these guidelines are meant to avoid many of the problems associated with high speed designs. The first requirement is for a substantial ground plane around and under the AD9011. Separate ground plane areas for the digital and analog components may be useful, but the separate grounds should be connected together at the AD9011 to avoid the effects of "ground loop" currents.

The power supply pins must also be decoupled to ground to improve noise immunity, 0.1μF and 0.01μF chip capacitors should be very effective. The REF_{OUT} pin will provide up to 12mA of current at the −2.0V A/D reference voltage. This pin should also be decoupled to ground through a 0.1μF capacitor.

The analog input signal is brought into the AD9011 through one of three input pins. The other two input pins should be grounded to the analog ground plane. Active switching of the input signal between the input pins is possible, but special care must be taken to see that the unused inputs are grounded through a low impedance, to avoid noise problems.



Typical AD9011 Application

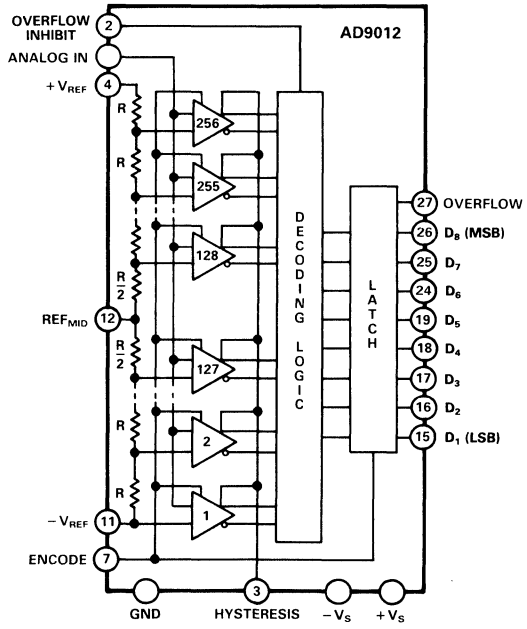
High Speed 8-Bit TTL A/D Converter

AD9012

FEATURES
100MSPS Encode Rate
Very Low Input Capacitance – 16pF
Low Power – 1W
TTL Compatible Outputs

APPLICATIONS
Radar Guidance
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

AD9012 FUNCTIONAL BLOCK DIAGRAM



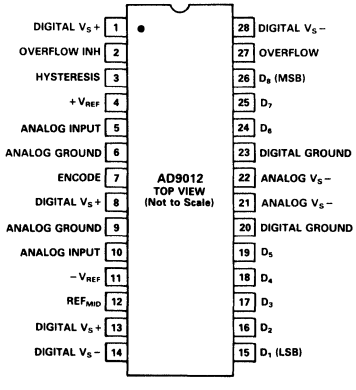
GENERAL DESCRIPTION

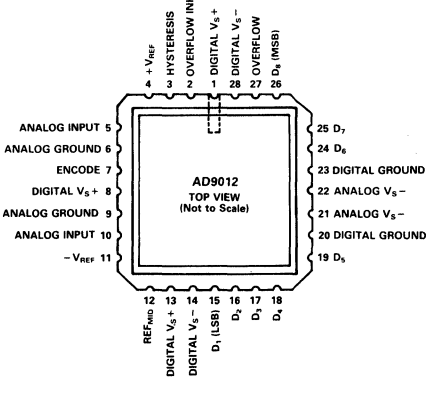
The AD9012 is an 8-bit, ultrahigh speed, analog-to-digital converter. The AD9012 is fabricated in an advanced bipolar process, which allows operation at sampling rates up to 100 megasamples/second. Functionally, the AD9012 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the TTL compatible output latches.

The exceptionally wide large signal analog input bandwidth of 160MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9012 allows very accurate acquisition of high speed pulse inputs without an external track-and-hold. The comparator output decoding scheme minimizes false codes, which is critical to high speed linearity.

The AD9012 is available in two grades, one with 0.5LSB linearity and one with 0.75LSB linearity. Both versions will be offered in an industrial grade, −25°C to +85°C, packaged in a 28-pin DIP and a 28-pin PLCC. The military temperature range devices, −55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

PIN DESIGNATIONS





SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6V
Analog to Digital Supply Voltage Differential ($-V_S$) . . . 0.5V
Negative Supply Voltage ($-V_S$) . . . . . −6V
Analog Input Voltage . . . . . $-V_S$ to +0.5V
ENCODE Input Voltage . . . . . −0.5V to +5V
OVERFLOW INH Input Voltage . . . . . −5.2V to 0V
Reference Input Voltage ($+V_{REF}$ $-V_{REF}$)[2] . −3.5V to +0.1V
Differential Reference Voltage 2.1V
Reference Midpoint Current . . . . . ±4mA
Digital Output Current 30mA
Operating Temperature Range
AD9012AQ/BQ . . . . . −25°C to +85°C
AD9012SE/SQ/TE/TQ/883 . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

Electrical Characteristics ($+V_S = +5.0V$; $-V_S = -5.2V$; Differential Reference Voltage = 2.0V, unless otherwise noted)

Parameter	Temp	Test Level	AD9012AQ/AP/AN Min	Typ	Max	AD9012BQ/BP/BN Min	Typ	Max	Sub-Group[4]	AD9012SQ/SE/883B Min	Typ	Max	AD9012TQ/TE/883B Min	Typ	Max	Units
RESOLUTION			8			8				8			8			Bits
DC ACCURACY																
Differential Linearity	+25°C	I		0.6	0.75		0.4	0.5	7		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75	8			1.0			0.75	LSB
Integral Linearity	+25°C	I		0.6	1.0		0.4	0.5	7		0.6	1.0		0.4	0.5	LSB
	Full	VI			1.2			1.2	8			1.2			1.2	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			7,8	GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR																
Top of Reference Ladder	+25°C	I		6	10		6	10	7		6	10		6	10	mV
	Full	VI			13			13	8			13			13	mV
Bottom of Reference Ladder	+25°C	I		7	15		7	15	7		7	15		7	15	mV
	Full	VI			18			18	8			18			18	mV
Offset Drift Coefficient	Full	V		25			25				25			25		µV/°C
ANALOG INPUT																
Input Bias Current[5]	+25°C	I		60	100		60	100	1		60	100		60	100	µA
	Full	VI			200			200	2,3			200			200	µA
Input Resistance	+25°C	I	150	200		150	200		1	150	200		150	200		kΩ
Input Capacitance	+25°C	III		16	18		16	18	12		16	18		16	18	pF
Large Signal Bandwidth[6]	+25°C	V		160			160				160			160		MHz
Analog Input Slew Rate[7]	+25°C	V		440			440				440			440		V/µs
REFERENCE INPUT																
Reference Ladder Resistance	+25°C	VI	64	80	110	64	80	110	1	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient		V		0.25			0.25				0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C	V		10			10				10			10		MHz
DYNAMIC PERFORMANCE																
Conversion Rate	+25°C	I	75	100		75	100		4	75	100		75	100		MSPS
Aperture Delay	+25°C	V		3.8			3.8				3.8			3.8		ns
Aperture Uncertainty (Jitter)	+25°C	V		15			15				15			15		ps
Output Delay (t_{PD})[8,9]	+25°C	I	3.2	4.9	6.6	3.2	4.9	6.6	9	3.2	4.9	6.6	3.2	4.9	6.6	ns
Transient Response[10]	+25°C	V		8			8				8			8		ns
Overvoltage Recovery Time[11]	+25°C	V		8			8				8			8		ns
Output Rise Time[8]	+25°C	I		6.6	8.0		6.6	8.0	9		6.6	8.0		6.6	8.0	ns
Output Fall Time[8]	+25°C	I		3.3	4.3		3.3	4.3	9		3.3	4.3		3.3	4.3	ns
Output Time Skew[8,12]	+25°C	V		3.0			3.0				3.0			3.0		ns
ENCODE INPUT																
Logic "1" Voltage[8]	Full	VI	2.0			2.0			7,8	2.0			2.0			V
Logic "0" Voltage[8]	Full	VI			0.8			0.8	7,8			0.8			0.8	V
Logic "1" Current	Full	VI			250			250	7,8			250			250	µA
Logic "0" Current	Full	VI			220			220	7,8			220			220	µA
Input Capacitance	+25°C	V		2.5			2.5				2.5			2.5		pF
Encode Pulse Width (Low)[13]	+25°C	I	2.5			2.5			4	2.5			2.5			ns
Encode Pulse Width (High)[13]	+25°C	I	2.5			2.5			4	2.5			2.5			ns
OVERFLOW INHIBIT INPUT																
0V Input Current	Full	VI		200	250		200	250	1,2,3		200	250		200	250	µA
AC LINEARITY[14]																
Effective Bits[15]	+25°C	V		7.5			7.5				7.5			7.5		Bits
In-Band Harmonics																
dc to 1.23MHz	+25°C	I	48	55		48	55		4	48	55		48	55		dBc
dc to 9.3MHz	+25°C	V		50			50				50			50		dBc
dc to 19.3MHz	+25°C	V		44			44				44			44		dBc
Signal-to-Noise Ratio[16]	+25°C	I	46	47.6		46	47.6		4	46	47.6		46	47.6		dBc
Noise Power Ratio[17]	+25°C	V		37			37				37			37		dBc
DIGITAL OUTPUT																
Logic "1" Voltage	Full	VI	2.4			2.4			1,2,3	2.4			2.4			V
Logic "0" Voltage	Full	VI			0.4			0.4	1,2,3			0.4			0.4	V
POWER SUPPLY[18]																
Positive Supply Current (+5.0V)	+25°C	I		33	37.5		33	37.5	1		33	37.5		33	37.5	mA
	Full	VI			38.5			38.5	2,3			38.5			38.5	mA
Supply Current (−5.2V)	+25°C	I		152	179		152	179	1		152	179		152	179	mA
	Full	VI			191			191	2,3			191			191	mA
Nominal Power Dissipation	+25°C	V		955			955				955			955		mW
Reference Ladder Dissipation	+25°C	V		44			44				44			44		mW
Power Supply Rejection Ratio[19]	+25°C	I		0.85	2.5		0.85	2.5	7		0.8	2.5		0.8	2.5	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]$+V_{REF} \geq -V_{REF}$ under all circumstances.

[3]Maximum junction temperature (t_J max) should not exceed +175°C for ceramic packages, and +150°C for plastic packages:

$t_J = PD\ (\theta_{JA}) + t_A$

$PD\ (\theta_{JC}) + t_C$

where

PD = power dissipation

θ_{JA} = thermal impedance from junction to ambient (°C/W)

θ_{JC} = thermal impedance from junction to case (°C/W)

t_A = ambient temperature (°C)

t_C = case temperature (°C)

typical thermal impedances are:

Ceramic DIP $\theta_{JA} = 56°C/W$; $\theta_{JC} = 20°C/W$

Plastic DIP $\theta_{JA} = 60°C/W$; $\theta_{JC} = 20°C/W$

Ceramic LCC $\theta_{JA} = 69°C/W$; $\theta_{JC} = 23°C/W$

PLCC $\theta_{JA} = 60°C/W$; $\theta_{JC} = 19°C/W$.

[4]Subgroups apply to military qualified devices only.

[5]Measured with Analog Input = 0V.

[6]Measured by FFT analysis where fundamental is −3dBc.

[7]Input slew rate derived from rise time (10% to 90%) of full-scale step input.

[8]Outputs terminated with two equivalent 'LS00 type loads. (See load circuit.)

[9]Measured from ENCODE into data out for LSB only.

[10]For full-scale step input, 8-bit accuracy is attained in specified time.

[11]Recovers to 8-bit accuracy in specified time, after 150% full-scale input overvoltage.

[12]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.

[13]ENCODE signal rise/fall times should be less than 30ns for normal operation.

[14]Measured at 75MSPS encode rate. Harmonic data based on worst case harmonics.

[15]Analog input frequency = 1.23MHz.

[16]RMS signal to rms noise, including harmonics with 1.23MHz analog input signal.

[17]NPR measured @ 0.5MHz. Noise Source is 250mW (rms) from 0.5MHz to 8MHz.

[18]Supplies should remain stable within ±5% for normal operation.

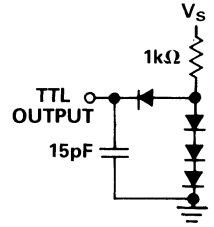
[19]Measured at −5.2V ±5% and +5.0V ±5%.

Specifications subject to change without notice.

Recommended Operating Conditions

Parameter	Input Voltage		
	Min	Nominal	Max
$-V_S$	−5.46	−5.20	−4.94
$+V_S$	+4.75	5.00	+5.25
$+V_{REF}$	$-V_{REF}$	0.0V	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

LOAD CIRCUIT



EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.

Test Level II – 100% production tested at +25°C, and sample tested at specified temperatures.

Test Level III – Sample tested only.

Test Level IV – Parameter is guaranteed by design and characterization testing.

Test Level V – Parameter is a typical value only.

Test Level VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF SUBGROUPS

Subgroup 1 – Static tests at +25°C.

Subgroup 2 – Static tests at maximum rated operating temperature.

Subgroup 3 – Static tests at minimum rated operating temperature.

Subgroup 4 – Dynamic tests at +25°C.

Subgroup 5 – Dynamic tests at maximum rated operating temperature.

Subgroup 6 – Dynamic tests at minimum rated operating temperature.

Subgroup 7 – Functional tests at +25°C.

Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures.

Subgroup 9 – Switching tests at +25°C.

Subgroup 10 – Switching tests at maximum rated operating temperature.

Subgroup 11 – Switching tests at minimum rated operating temperature.

Subgroup 12 – Periodically sample tested.

ORDERING INFORMATION

Device	Linearity	Temperature Range	Description	Package Options*
AD9012AQ	0.75LSB	−25°C to +85°C	28-Pin Ceramic DIP, Industrial	Q-28
AD9012BQ	0.50LSB	−25°C to +85°C	28-Pin Ceramic DIP, Industrial	Q-28
AD9012AN	0.75LSB	−25°C to +85°C	28-Pin Plastic DIP, Industrial	N-28
AD9012BN	0.50LSB	−25°C to +85°C	28-Pin Plastic DIP, Industrial	N-28
AD9012AP	0.75LSB	−25°C to +85°C	28-Pin PLCC, Industrial	P-28A
AD9012BP	0.50LSB	−25°C to +85°C	28-Pin PLCC, Industrial	P-28A
AD9012SQ/883B	0.75 LSB	−55°C to +125°C	28-Pin Ceramic DIP, Military	Q-28
AD9012SE/883B	0.75 LSB	−55°C to +125°C	28-Pin LCC, Military	E-28A
AD9012TQ/883B	0.50 LSB	−55°C to +125°C	28-Pin Ceramic DIP, Military	Q-28
AD9012TE/883B	0.50 LSB	−55°C to +125°C	28-Pin LCC, Military	E-28A

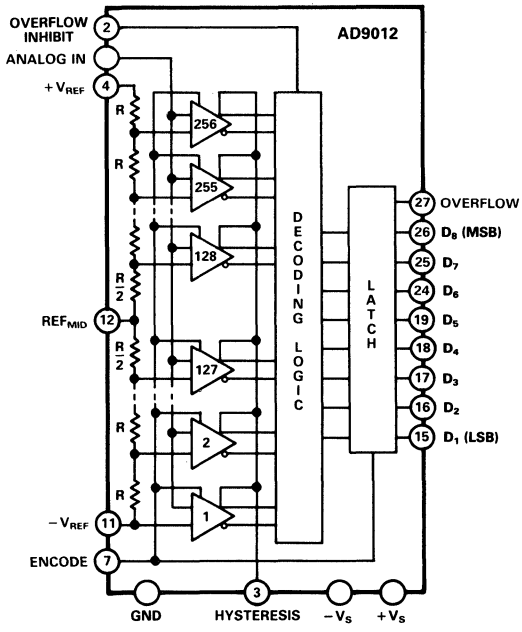
*See Section 14 for package outline information.

FUNCTIONAL DESCRIPTION

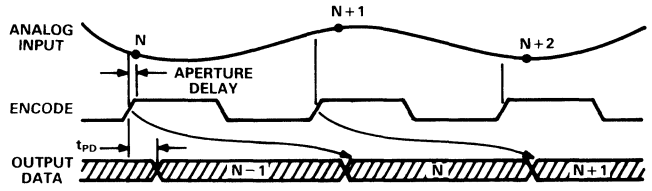
Pin #	Name	Description
1	DIGITAL $+V_S$	One of three positive digital supply pins (nominally +5.0V).
2	OVERFLOW INH	OVERFLOW INHIBIT controls the data output coding for overvoltage inputs (AIN$\geq +V_{REF}$).

ANALOG INPUT	OVERFLOW ENABLED (FLOATING) OF D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8	OVERFLOW INHIBITED (GND) OF D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8
$V_{IN} \geq +V_{REF}$	1 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1
$V_{IN} < +V_{REF}$	0 X X X X X X X X	0 X X X X X X X X

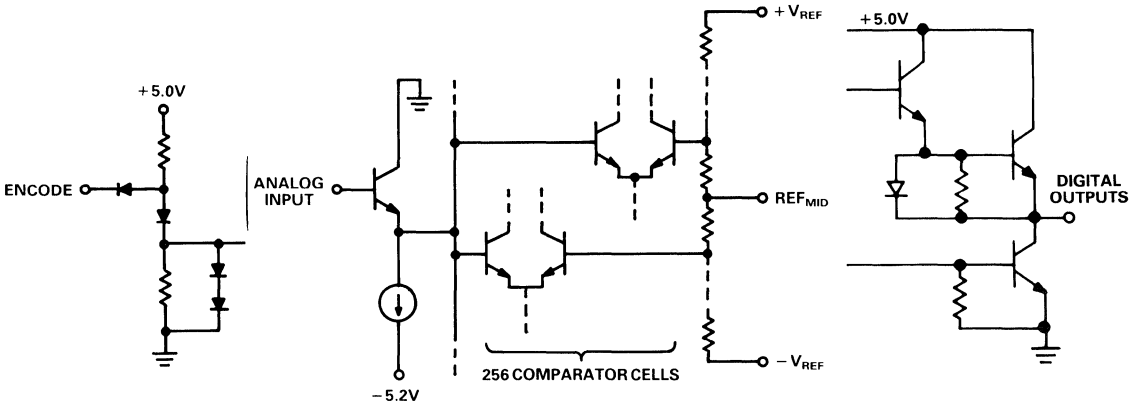
3	HYSTERESIS	The Hysteresis control voltage varies the comparator hysteresis from 0mV to 10mV, for a change from −5.2V to −2.2V at the Hysteresis control pin.
4	$+V_{REF}$	The most positive reference voltage for the internal resistor ladder.
5	ANALOG INPUT	One of two analog input pins. Both analog input pins should be connected together.
6	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
7	ENCODE	TTL level encode command input. ENCODE is rising edge sensitive.
8	DIGITAL $+V_S$	One of three positive digital supply pins (nominally +5.0V).
9	ANALOG GROUND	One of two analog ground pins. Both analog ground pins should be connected together.
10	ANALOG INPUT	One of two analog input pins. Both analog inputs should be connected together.
ii	$-V_{REF}$	The most negative reference voltage for the internal resistor ladder.
12	REF_{MID}	The midpoint tap on the internal resistor ladder.
13	DIGITAL $+V_S$	One of three positive digital supply pins (nominally +5.0V)
14	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.
15	D_1 (LSB)	Digital data output. D_1 (LSB) is the least significant bit of the digital output word.
16-19	D_2-D_5	Digital data output.
20	DIGITAL GROUND	One of two digital ground pins. Both digital grounds pins should be connected together.
21, 22	ANALOG $-V_S$	One of two negative analog supply pins (nominally −5.2V). Both analog supply pins should be connected together.
23	DIGITAL GROUND	One of two digital ground pins. Both digital ground pins should be connected together.
24, 25	D_6, D_7	Digital data output.
26	D_8 (MSB)	Digital data output D_8 (MSB) is the most significant bit of the digital output word.
27	OVERFLOW	Overflow data output. Logic HIGH indicates an input overvoltage ($V_{IN} > +V_{REF}$), if OVERFLOW INHIBIT is enabled (overflow enabled, floating). See OVERFLOW INHIBIT.
28	DIGITAL $-V_S$	One of two negative digital supply pins (nominally −5.2V). Both digital supply pins should be connected together.



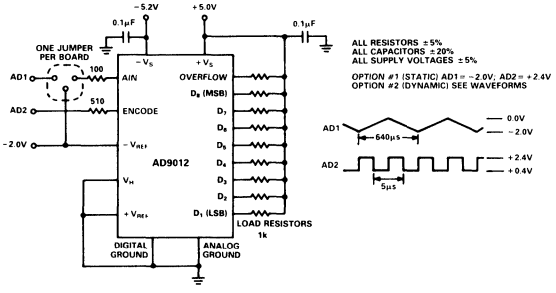
Functional Block Diagram



System Timing Diagram



Input/Output Circuits



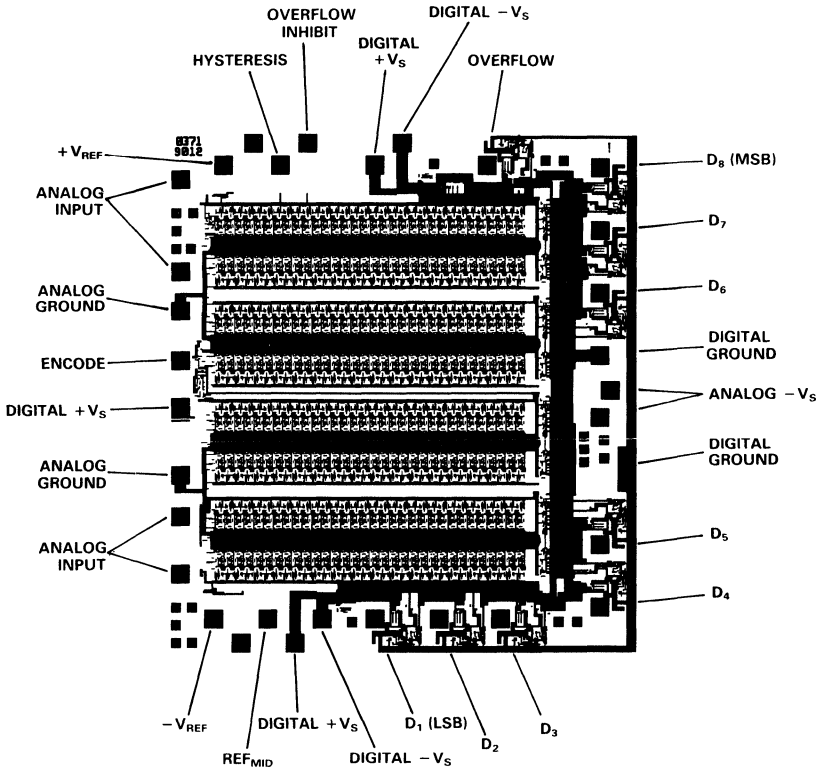
Burn-In Diagram

MIL-STD-883 COMPLIANCE INFORMATION

The AD9012SD/SE/TE/TQ/883B devices are classified within Microcircuits Group 57, Technology Group D (bipolar A/D converters), and are constructed in accordance with MIL-STD-883. The AD9012 is electrostatic sensitive and falls within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $t_a = t_c = t_j$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.

Die Layout and Mechanical Information



Die Dimensions	111 × 123 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic (Ceramic) Epoxy (Plastic)
Bond Wire	1–1.3 mil Gold; Gold Ball Bonding

APPLICATION INFORMATION

The AD9012 is compatible with all standard TTL logic families. However, to operate at the highest encode rates, the supporting logic around the AD9012 will need to be equally fast. Two possible choices are the AS and the ALS families. Whichever of the TTL logic families is used, special care must be exercised to keep digital switching noise away from the analog circuits around the AD9012. The two most critical items are the digital supply lines and the digital ground return.

The input capacitance of the AD9012 is an exceptionally low 16pF. This allows the use of a wide range of input amplifiers, both hybrid and monolithic. To take full advantage of the 160MHz input bandwidth of the AD9012, a hybrid amplifier like the AD9610/AD9611 will be required. For those applications that do not require the full input bandwidth of the AD9012, some of the more traditional monolithic amplifiers, like the AD846, should work very well. Overall performance with monolithic amplifiers can be improved by inserting a 40Ω resistor in series with the amplifier output.

The output data is buffered through the TTL compatible output latches. All data is delayed by one clock cycle, in addition to the latch propagation delay (t_{PD}), before becoming available at the outputs. Both the analog-to-digital conversion cycle and the data transfer to the output latches, are triggered on the rising edge of the TTL compatible ENCODE signal (see timing diagram).

The AD9012 also incorporates a HYSTERESIS control pin which provides from 0 to 10mV of additional hysteresis in the comparator input stages. Adjustments in the HYSTERESIS control voltage may help to improve noise immunity and overall performance in harsh environments.

The OVERFLOW INHIBIT pin of the AD9012 determines how the converter handles overrange inputs (AIN$\geq +V_{REF}$). In the "enabled" state (floating at -5.2V), the OVERFLOW output will be at logic HIGH and all other outputs will be at logic LOW for overrange inputs (return-to-zero operation). In the "inhibited" state (tied to ground), the OVERFLOW output will be at logic LOW for overrange inputs, and all other digital outputs will be at logic HIGH (nonreturn-to-zero operation).

The AD9012 provides outstanding error rate performance. This is due to tight control of comparator offset matching and a fault tolerant decoding stage. Additional improvements in error rate are possible through the addition of hysteresis (see HYSTERSIS control pin). This level of performance is extremely important in fault sensitive applications like digital radio (QAM).

Dramatic improvements in comparator design and construction give the AD9012 excellent dynamic characteristics, namely SNR (signal-to-noise ratio). The 160MHz input bandwidth and low error rate performance give the AD9012 an SNR of 47dB with a 1.23MHz input. High SNR performance is particularly important in broadcast video applications where signals may pass through the converter several times before the processing is complete. Pulse signature analysis, commonly performed in advanced radar receivers, is another area that is especially dependent on high quality dynamic performance.

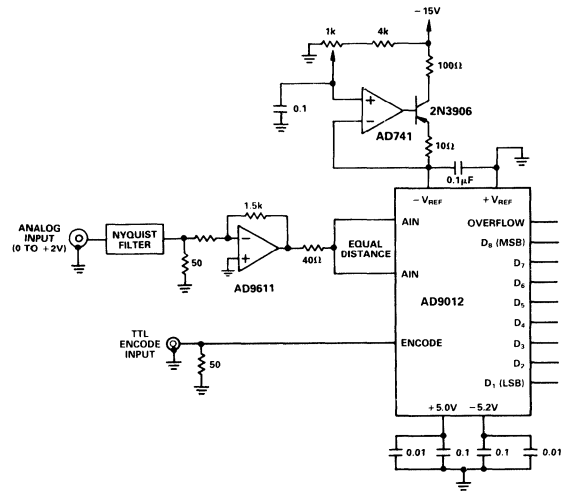
LAYOUT SUGGESTIONS

Designs using the AD9012, like all high-speed devices, must follow a few basic layout rules to insure optimum performance. Essentially, these guidelines are meant to avoid many of the problems associated with high-speed designs. The first requirement is for a substantial ground plane around and under the AD9012. Separate ground plane areas for the digital and analog components may be useful, but the separate grounds should be connected together at the AD9012 to avoid the effects of "ground loop" currents.

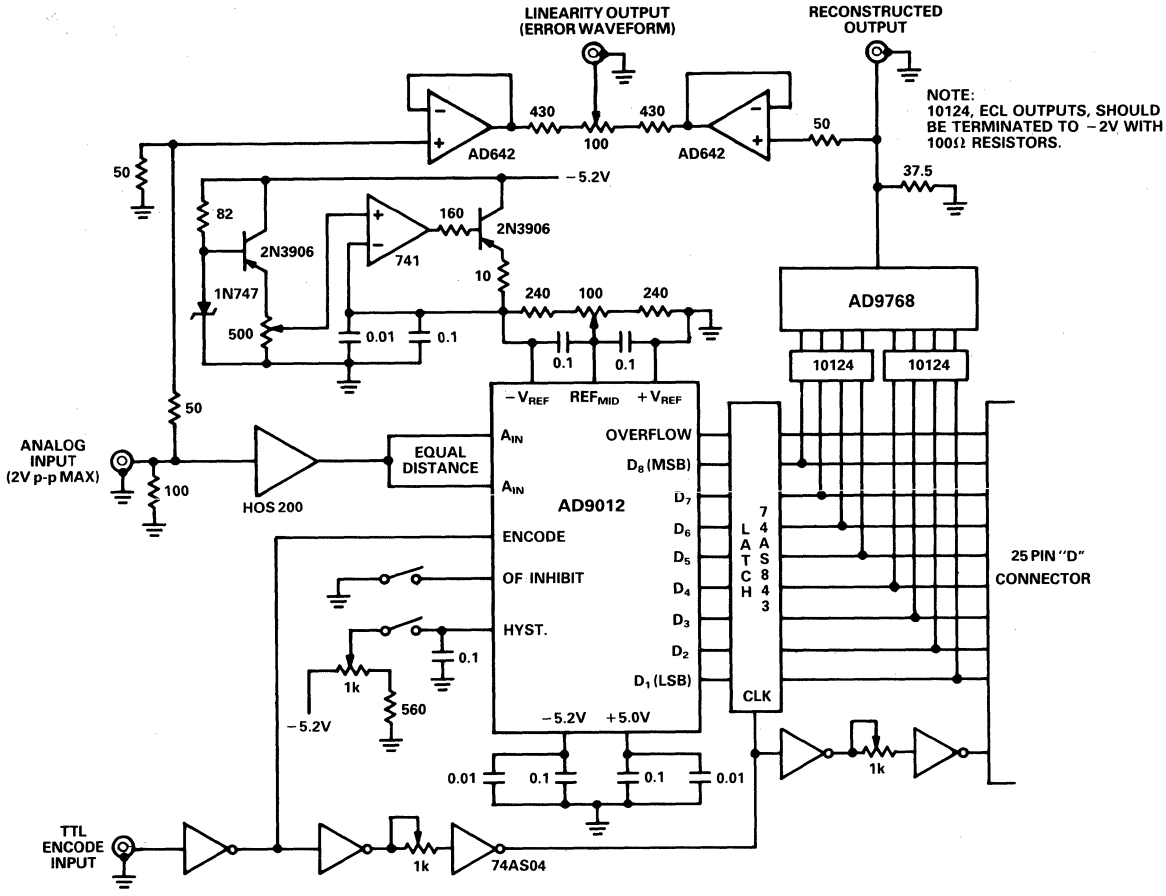
The second area that requires an extra degree of attention involves the three reference inputs, $+V_{REF}$, REF_{MID}, and $-V_{REF}$. The $+V_{REF}$ input and the $-V_{REF}$ input should both be driven from a low impedance source (note that the $+V_{REF}$ input is typically tied to analog ground). A low drift amplifier should provide satisfactory results, even over an extended temperature range. Adjustments at the REF_{MID} input may be useful in improving the integral linearity by correcting any reference ladder skews.

The reference inputs should be adequately decoupled to ground through 0.1μF chip capacitors to limit the effects of system noise on conversion accuracy. The power supply pins must also be decoupled to ground to improve noise immunity; 0.1μF and 0.01μF chip capacitors should be very effective.

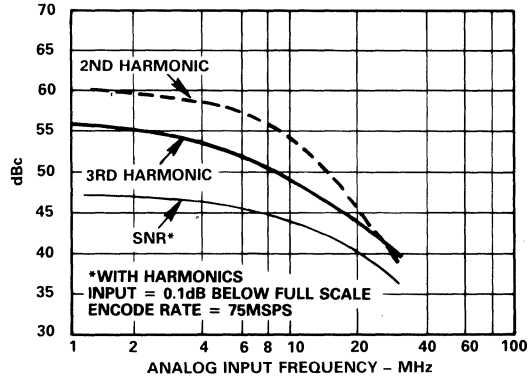
The analog input signal is brought into the AD9012 through two separate input pins. It is very important that the two input pins be driven symetrically with equal length electrical connections. Otherwise, aperture delay errors may degrade converter performance at high frequencies.



Typical AD9012 Application



AD9012 Evaluation Circuit



Dynamic Performance

ANALOG DEVICES

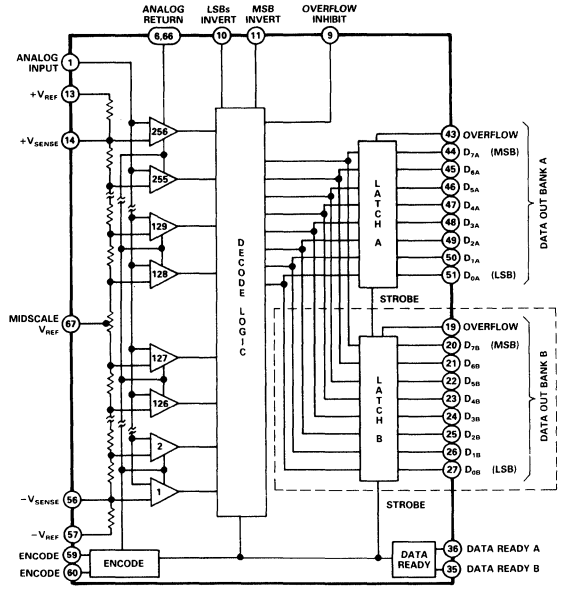
High Speed 8-Bit A/D Converters

AD9028/AD9038

FEATURES
300 MSPS Encode Rate
250 MHz Large Signal Input Bandwidth
Low Input Capacitance: 17 pF
Excellent SNR
Single −5.2 V Power Supply
Overflow Bit & Bit Invert Functions
1:2 Demultiplexed Outputs (AD9038)

APPLICATIONS
Digital Oscilloscopes
Waveform Digitizers
Radar Receivers
Electronic Countermeasures

AD9038 FUNCTIONAL BLOCK DIAGRAM



(Dotted Area Not Included in AD9028)

GENERAL DESCRIPTION

The AD9028 and AD9038 are ECL-compatible 8-bit, high speed flash analog-to-digital converters. Both are fabricated in an advanced bipolar VLSI process which ensures exceptionally wide analog input bandwidth (250 MHz) and encode rates up to 300 MSPS.

Output data for the AD9028 include Overflow and Data Ready signals; control pins allow the user to invert the MSB and/or LSBs. The AD9038 combines the features of the AD9028 with on-board demultiplexing circuits to provide two sets of output data. These ease the task of interfacing the converter by reducing the data rate to half the encode rate.

The analog input is designed for 0 to −2.0 volt operation. Sense pins for the $+V_{REF}$ and $-V_{REF}$ inputs allow full-scale calibration of the input range; a tap at the midpoint of the reference ladder is available to minimize integral nonlinearity. Dynamic performance is enhanced by driving the ANALOG RETURN pins with a buffered analog input; see the Applications section.

There are two linearity grades of each device. Commercial temperature ranges of 0 to +70°C and military temperature ranges of −55°C to +125°C are available. Both components are offered in a ceramic 68-pin LCC, and a ceramic 68-pin leaded package. These packages are specially designed for low thermal impedance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

ANALOG INPUT . . . . . $-V_S$ to +0.5 V
ANALOG RETURN . . . . . .0 V to +2.0 V
$-V_S$ to GROUND . . . . . .+0.5 V dc to −6.0 V dc
$+V_{REF}$, $-V_{REF}$, MIDSCALE V_{REF} . . . . . .−2.1 V to +0.1 V
$+V_{REF}$ to $-V_{REF}$ . . . . . .2.1 V
MIDSCALE V_{REF} , $+V_{SENSE}$, $-V_{SENSE}$ Current . . . . .±4 mA
MSB INVERT, LSBs INVERT, OVERFLOW INHIBIT, ENCODE, $\overline{\text{ENCODE}}$, HYSTERESIS . . . . . .$-V_S$ to 0 V
ENCODE To $\overline{\text{ENCODE}}$ . . . . . .4 V
Digital Output Current . . . . . .20 mA
ANALOG $-V_S$ to DIGITAL $-V_S$ . . . . . .±0.5 V
Operating Temperature Range
AD9028/AD9038KE/KZ/JE/JZ . . . . . .0 to +70°C
AD9028/AD9038TE/TZ/SE/SZ/883 . . . . . .−55°C to +125°C
Maximum Junction Temperature[2] . . . . . .+175°C
Lead Temperature (Soldering, 10sec) . . . . . .+300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($-V_S = -5.2$ V; $+V_{REF} = 0$ V; $-V_{REF} = -2$ V; ANALOG RETURN = 0 V, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	Sub-Group[3]	AD9028JE/JZ SE/SZ/883 Min	Typ	Max	AD9028KE/KZ TE/TZ/883 Min	Typ	Max	AD9038JE/JZ SE/SZ/883 Min	Typ	Max	AD9038KE/KZ TE/TZ//883 Min	Typ	Max	Units
RESOLUTION				8			8			8			8			Bits
DC ACCURACY																
Differential Nonlinearity	+25°C	I	7		0.8	1.0		0.6	0.75		0.8	1.0		0.6	0.75	LSB
	Full	VI	8		1.0	1.2		0.8	1.0		1.0	1.2		0.8	1.0	LSB
Integral NonLinearity	+25°C	I	7		0.8	1.0		0.6	0.75		0.8	1.0		0.6	0.75	LSB
	Full	VI	8		1.0	1.2		0.8	1.0		1.0	1.2		0.8	1.0	LSB
No Missing Codes	Full	VI	7, 8	GUARANTEED			GUARANTEED									
ANALOG INPUT																
Input Bias Current[4]	+25°C	I	1		125	250		125	250		125	250		125	250	µA
	Full	VI	2, 3			400			400			400			400	µA
Input Resistance	+25°C	I	1	50	75		50	75		50	75		50	75		kΩ
Input Capacitance[4]	+25°C	III	12		17	21		17	21		17	21		17	21	pF
Analog Bandwidth[5]	+25°C	V			250			250			250			250		MHz
REFERENCE INPUT																
Reference Ladder Resistance	+25°C	I	1	24	40	60	24	40	60	24	40	60	24	40	60	Ω
	Full	VI	2, 3	20		75	20		75	20		75	20		75	Ω
Ladder Tempco	Full	V			0.13			0.13			0.13			0.13		Ω/°C
Ref. Input Bandwidth	Full	V			30			30			30			30		MHz
Reference Ladder Offset[5]	+25°C	I	7		32	45		32	45		32	45		32	45	mV
(Top)	Full	VI	8			47			47			47			47	mV
Reference Ladder Offset[5]	+25°C	I	7		26	37		26	37		26	37		26	37	mV
(Bottom)	Full	VI	8			39			39			39			39	mV
Offset Drift Coefficient	Full	V			20			20			20			20		µV/°C
SWITCHING PERFORMANCE[5,6]																
Maximum Conversion Rate	+25°C	I	4	300	325		300	325		300	325		300	325		MSPS
Aperture Delay (t_A)	+25°C	V			1.4			1.4			1.4			1.4		ns
Aperture Uncertainty (Jitter)	+25°C	V			3			3			3			3		ps, rms
Output Delay (t_{OD})	+25°C	I	9	4.7	6	7.3	4.7	6	7.3	4.7	6	7.3	4.7	6	7.3	ns
Output Rise Time	+25°C	I	9		1.0	1.6		1.0	1.6		1.0	1.6		1.0	1.6	ns
Output Fall Time	+25°C	I	9		1.0	1.6		1.0	1.6		1.0	1.6		1.0	1.6	ns
Output Time Skew	+25°C	I	9		0.25	0.7		0.25	0.7		0.25	0.7		0.25	0.7	ns
Data Ready Output Delay (t_{DR})	+25°C	I	9	4.1	5.4	6.7	4.1	5.4	6.7	4.8	6.1	7.4	4.8	6.1	7.4	ns
ENCODE INPUT																
Logic "1" Voltage	Full	IV		−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	IV				−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI	7, 8		125	285		125	285		125	285		125	285	µA
Logic "0" Current	Full	VI	7, 8		100	285		100	285		100	285		100	285	µA
Input Capacitance	+25°C	V			3.6			3.6			3.6			3.6		pF
Pulse Width (High)[7]	+25°C	I	4	2			2			2			2			ns
Pulse Width (Low)[7]	+25°C	I	4	1			1			1			1			ns

Parameter (Conditions)	Temp	Test Level	Sub-Group[3]	AD9028JE/JZ SE/SZ/883 Min	Typ	Max	AD9028KE/KZ TE/TZ/883 Min	Typ	Max	AD9038JE/JZ SE/SZ/883 Min	Typ	Max	AD9038KE/KZ TE/TZ//883 Min	Typ	Max	Units
DYNAMIC PERFORMANCE[8]																
Transient Response	+25°C	V			3			3			3			3		ns
Overvoltage Recovery Time	+25°C	V			3			3			3			3		ns
Effective Number of Bits (ENOB)																
Analog Input @ 9.3 MHz	+25°C	I	4	7.0	7.1		7.2	7.5		7.0	7.2		7.2	7.5		Bits
@ 49 MHz	+25°C	I	4	6.5	7.0		6.5	7.0		6.5	7.0		6.5	7.0		Bits
@ 92 MHz	+25°C	I	4	5.4	5.8		5.4	5.8		5.4	5.8		5.4	5.8		Bits
In-Band Harmonics																
Analog Input @ 9.3 MHz	+25°C	I	4	48	53		54	56		48	53		54	56		dBc
@ 49 MHz	+25°C	I	4	41	48		41	48		41	48		41	48		dBc
@ 92 MHz	+25°C	I	4	36	40		36	40		36	40		36	40		dBc
Signal-to-Noise Ratio[9]																
Analog Input @ 9.3 MHz	+25°C	I	4	44	45		45.5	47		44	45		45.5	47		dB
@ 49 MHz	+25°C	I	4	40	43		40	43		40	43		40	43		dB
@ 92 MHz	+25°C	I	4	33	36		33	36		33	36		33	36		dB
Signal-to-Noise Ratio[9] (without harmonics)																
Analog Input @ 9.3 MHz	+25°C	I	4	45.5	48		45.5	48		45.5	48		45.5	48		dB
@ 49 MHz	+25°C	I	4	43	46		43	46		43	46		43	46		dB
@ 92 MHz	+25°C	I	4	38	43		38	43		38	43		38	43		dB
Two-Tone Intermodulation Distortion Rejection[10]	+25°C	I	4	42	49		42	49		42	49		42	49		dB
DIGITAL OUTPUTS[6]																
Logic "1" Voltage	Full	VI	1, 2, 3	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI	1, 2, 3			−1.5			1.5			−1.5			1.5	V
POWER SUPPLY																
Analog Return	+25°C	V			14.4			14.4			14.4			14.4		mA
Negative Supply Current	+25°C	I	1		390	475		390	475		430	495		430	495	mA
($-V_S$ = −5.2 V)	Full	VI	2, 3			515			515			550			550	mA
Power Dissipation	+25°C	V			2.0			2.0			2.2			2.2		W
Ref. Ladder Dissipation	+25°C	V			100			100			100			100		mW
Power Supply Rejection Ratio (PSRR)	+25°C	I	7		1.2	3		1.2	3		1.2	3		1.2	3	mV/V

For applications assistance, phone Computer Labs Division at (919) 668-9511.

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances:
68-pin leaded ceramic chip carrier θ_{JA}=31°C/W; θ_{JC}=1.1°C/W.
68-pin ceramic LCC θ_{JA}=36°C/W; θ_{JC}=2.6°C/W.

[3]Subgroups apply only to military qualified devices.

[4]Measured with analog input = 0 V.

[5]See definitions of specifications.

[6]Outputs terminated through 100 Ω to −2.0 V; C_L<4 pF

[7]ENCODE command rise/fall times should be less than 2.5 ns for normal operation.

[8]Measured at 250 MSPS encode rate; analog return is tied to +1 V dc. (See text and diagrams.)

[9]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[10]Intermodulation measured with analog input frequencies of 60 MHz and 70 MHz at 7 dB below full scale.

Specifications subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Parameter	Input Voltage Min	Nominal	Max
$-V_S$	−5.46	−5.2	−4.94
$+V_{REF}$	$-V_{REF}$	0	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
ANALOG INPUT	$-V_{REF}$		$+V_{REF}$
ANALOG RETURN	Analog In		Analog In +2.0 V

EXPLANATION OF TEST LEVELS

Test Level		
I	–	100% production tested.
II	–	100% production tested at +25°C, and sample tested at specified temperatures.
III	–	Sample tested only.
IV	–	Parameter is guaranteed by design and characterization testing.
V	–	Parameter is a typical value only.
VI	–	All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF SUBGROUPS

Subgroup	1	–	Static tests at +25°C. (5% PDA calculated against Subgroup 1 for high-rel versions.)
Subgroup	2	–	Static tests at maximum rated operating temperature.
Subgroup	3	–	Static tests at minimum rated operating temperature.
Subgroup	4	–	Dynamic tests at +25°C.
Subgroup	5	–	Dynamic tests at maximum rated operating temperature.
Subgroup	6	–	Dynamic tests at minimum rated operating temperature.
Subgroup	7	–	Functional tests at +25°C.
Subgroup	8	–	Functional tests at maximum and minimum rated temperatures.
Subgroup	9	–	Switching tests at +25°C.
Subgroup	10	–	Switching tests at maximum rated operating temperature.
Subgroup	11	–	Switching tests at minimum rated operating temperature.
Subgroup	12	–	Periodically sample tested.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Output Delay
The delay between the 50% point of the falling edge of the ENCODE command and the 50% point of the rising edge of DATA READY A or DATA READY B.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
ENOB is a measure of ac linearity and is calculated from a sine wave curve fit according to the following expression:

$$ENOB = N - LOG_2 [\text{ rms error (actual)/rms error (ideal) }]$$

N is the resolution (number of bits) of the converter. The actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

In-Band Harmonics
The rms value of the fundamental divided by the rms value of the worst harmonic.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Maximum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency tested drops by no more than 3 dB below the guaranteed limit.

Output Delay
The delay between the 50% point of the rising edge of the ENCODE command and the 50% point of output data.

Output Time Skew
Bit-to-bit time variations among D0 to D7 outputs. In the AD9028 and AD9038 specifications, time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 8-bit accuracy after an analog input signal 150% of full scale is reduced to the full scale (0 to −2 V) range of the converter.

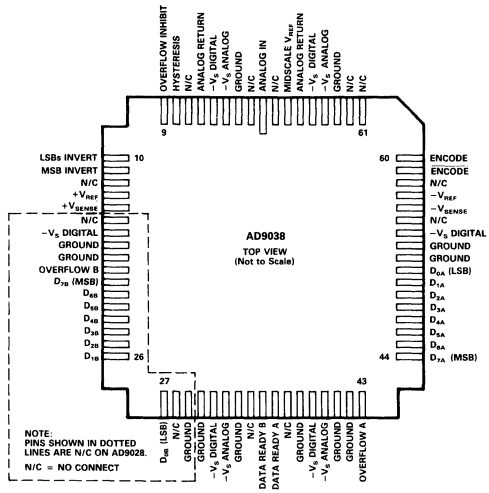
Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage. In the AD9028 and AD9038 units, $-V_S$ (−5.2 V) is within ±5% of its nominal value for this test.

Reference Ladder Offset
The deviation between the top (or bottom) comparator transition voltage as measured at the analog input, and the voltage at the $+V_{REF}$ (or $-V_{REF}$) pin. This is valuable in determining the accuracy and adjustment range for $\pm V_{REF}$ sources.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Transient Response
The time required for the converter to achieve 8-bit accuracy when a step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.



AD9028/AD9038 Pin Designations
(Note: Chip Cavity Opening Is On Bottom of Package.)

AD9028/AD9038 PIN DESCRIPTIONS

Pin No.	Name	Function
1	ANALOG INPUT	Analog input is nominally between 0 and −2 Volts.
6, 66	ANALOG RETURN	Normally grounded; supplies current to input comparator circuits. Pins can be tied to postive potential (+2.0 V max), or buffered version of analog input to reduce capacitance and enhance dynamic performance. (See Applications.)
36	DATA READY A	Rising edge of signal can be used to externally latch D_{0A}–D_{7A}.
35	DATA READY B	Rising edge of signal can be used to externally latch D_{0B}–D_{7B}.
44–51	D_{7A}–D_{0A}	ECL digital data from Data Bank A.
20–27	D_{7B}–D_{0B}	ECL digital data from Data Bank B.
59, 60	ENCODE, ENCODE	Differential ECL convert signals.
3, 17, 18, 29, 30, 33, 38, 41, 42, 52, 53, 63	GROUND	All ground pins should be connected together.
8	HYSTERESIS	Normally grounded; hysteresis control pin.
10	LSBs INVERT	Normally connected to $-V_S$. When grounded, lower order bits are inverted.
67	MIDSCALE V_{REF}	Normally floating; midpoint of reference resistor ladder. Can be adjusted to minimize integral nonlinearity.
11	MSB INVERT	Normally connected to $-V_S$. When grounded, MSB is inverted.
43	OVERFLOW A	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
19	OVERFLOW B	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
9	OVERFLOW INHIBIT	Normally floating or tied to $-V_S$. When grounded, OVERFLOW A and B are disabled; D0–D7 remain at ECL logic "1" when ANALOG IN > $+V_{SENSE}$.
13	$+V_{REF}$	Normally 0 V; sets voltage reference at top of ladder.
57	$-V_{REF}$	Normally −2 V; sets voltage reference at bottom of ladder.
4, 32, 40, 64	$-V_S$ ANALOG	−5.2 Volts; analog supply voltage.
5, 16, 31, 39, 54, 65	$-V_S$ DIGITAL	−5.2 Volts; digital supply voltage.
14	$+V_{SENSE}$	Voltage sense line to most positive comparator reference input.
56	$-V_{SENSE}$	Voltage sense line to most negative comparator reference input.

THEORY OF OPERATION

Refer to the AD9038 Block Diagram. Both units use a "flash," or parallel, A/D architecture. The analog input voltage range is determined by an external voltage reference ($+V_{REF}$ and $-V_{REF}$), nominally 0 to -2 V. An internal resistor ladder divides this reference into 255 levels, each representing a single quantization level.

The A/D conversion, triggered by the ENCODE signal, is performed by 255 comparators. The output of the comparators indicates the appropriate quantization level of the analog input signal. The decoding logic processes the comparator outputs and provides an 8-bit code to the output stage.

Flash architecture has an advantage over other A/D architectures because the conversion occurs in one step, and the performance of the converter is limited primarily by the speed and matching of the individual comparators. A state-of-the-art bipolar process and careful comparator design give the AD9028/AD9038 excellent ac performance. A proprietary decoding scheme minimizes error codes, and control pins allow the user to select among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

APPLICATIONS

Voltage References

The AD9028/AD9038 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$, as shown in Figure 1. These two voltages are applied across an internal resistor ladder (nominally 40 Ω) and set the analog input voltage range of the converter. Each voltage reference should be driven from a stable, low impedance source. The reference connections should be capacitively coupled to ground to bypass noise.

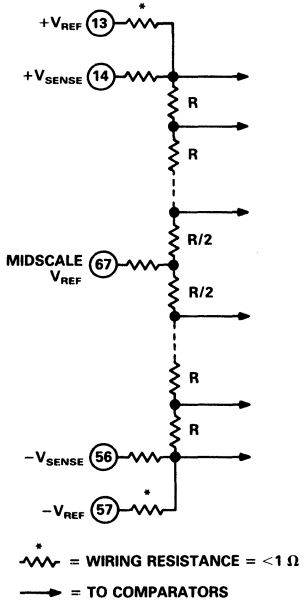


Figure 1. Reference Ladder

Applying a voltage greater than 2.1 V across the internal resistor ladder will cause current densities to exceed rated values, and may cause permanent damage to the AD9028/AD9038. The design of the reference circuit should limit the voltage available to the references.

Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+V_{SENSE}$ and $-V_{SENSE}$, to adjust the reference voltages. Current through the sense lines should be limited to 100 μA.

The voltage at the midpoint of the resistor ladder, MIDSCALE VREF, can be adjusted to improve the integral linearity of individual devices.

A suggested application in Figure 4 shows a reference circuit which nulls out the offset errors using two op amps. Feedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amp; resistors at the base and emitter stabilize their operation.

Analog Input Signal

The analog input circuit of the AD9028/AD9038 consists of 255 comparator inputs and can be represented by a single transistor as shown in Figure 2.

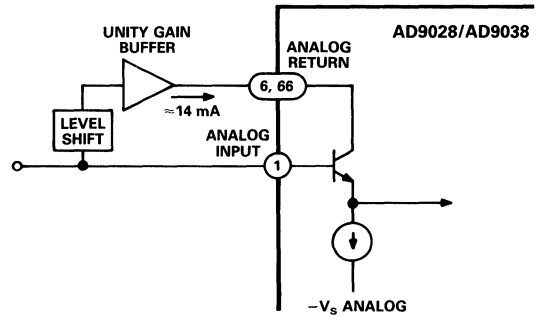


Figure 2. Preferred Analog Input Configuration

Typically, the ANALOG INPUT has an input resistance of 100 kΩ. Input capacitance is characterized in Figure 3.

With ANALOG RETURN (collector of the input transistor) connected to ground, collector base capacitance causes the analog input capacitance to be dependent on the analog input voltage. This varying capacitance is typical of flash converters, and requires that the ANALOG INPUT be driven from a low impedance source. This source must be capable of driving a capacitive load to avoid distorting the analog input signal at high frequencies. In applications where the analog source cannot adequately drive the input capacitance, harmonic distortion will increase; the effect will be greatest on the second harmonic.

AC performance of the AD9028/AD9038 can be improved by connecting the ANALOG RETURN to a dc voltage between ground and +1.5 V. This reduces the analog input capacitance and lessens its dependence on the analog input voltage (see Figure 3).

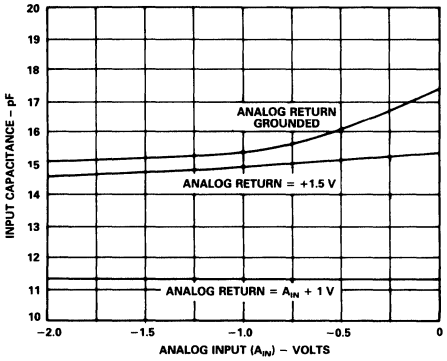


Figure 3. Input Capacitance vs. Input Voltage

The circuits shown in Figure 2 and Figure 4 show the ANALOG RETURN driven by a buffered version of the signal presented to the ANALOG INPUT. The dc level of this signal is 1 V higher than the analog input, and thus reduces the analog input capacitance as described above. In addition, the signal cancels the ac voltage between the ANALOG RETURN and ANALOG INPUT connections, which minimizes the collector-base component of the analog input capacitance. The analog input capacitance characteristics under this condition are also shown in Figure 3.

In any of the configurations described above, the user should drive the analog signal from a low distortion, low noise amplifier. A good choice is the AD9611, a wide bandwidth operational amplifier with excellent ac performance.

Selection of the buffer is also important for applications in which the analog input signal is applied to the ANALOG RETURN. The gain of the buffer should be set as close to 1 as possible, and the buffer should have a low phase shift at the frequencies of interest. It must also be able to supply the current required, typically 14 mA.

Harmonic distortion at the ANALOG RETURN is not as critical as that at the ANALOG INPUT, but should remain less than 40 dB (out to 100 MHz) to maximize converter performance. The input impedance at this node is approximately 6.5 kΩ in parallel with 25 pF. Monolithic wideband operational amplifiers and closed loop buffers should be suitable for driving this input.

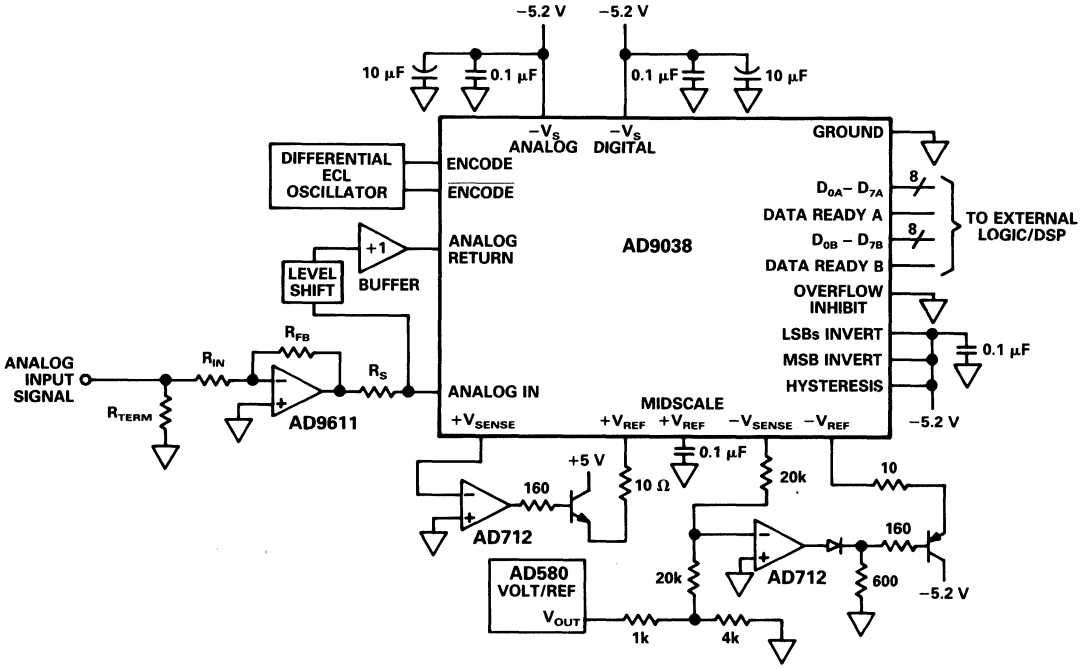


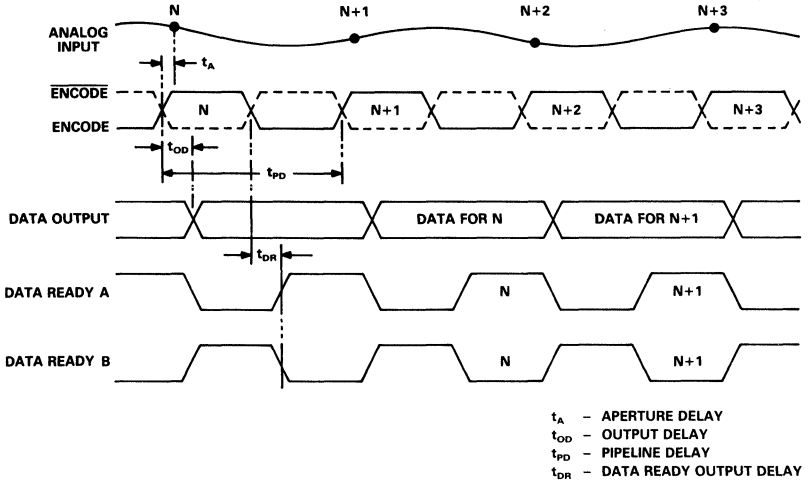
Figure 4. AD9038 Typical Application

Timing

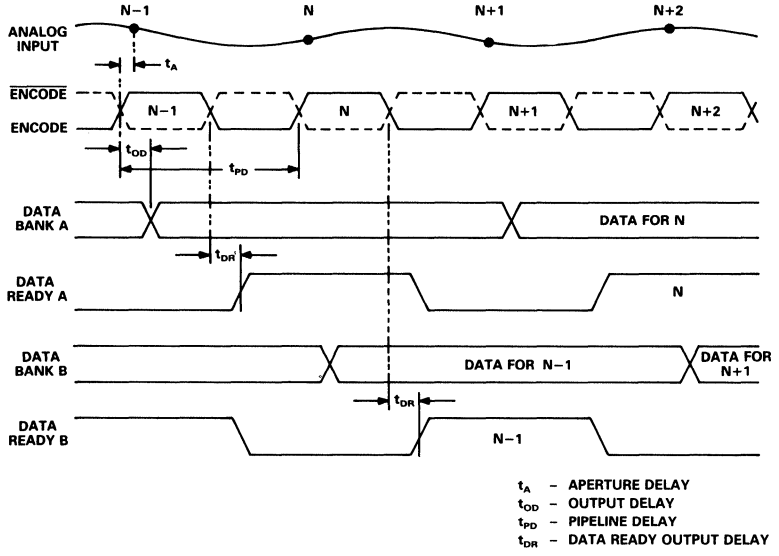
In the AD9028, the rising edge of the ENCODE signal triggers the A/D conversion by latching the comparators. The falling edge of the ENCODE signal returns the comparators to track mode and triggers the Data Ready signal.

ENCODE and $\overline{\text{ENCODE}}$ are ECL compatible and should be driven differentially. Jitter on the ENCODE signal will raise the noise floor of the converter. Differential signals, with fast clean edges, will reduce the jitter in the signal and allow optimum ac performance. In applications with a fixed, high frequency encode rate, converter performance is also improved (jitter reduced) by using a crystal oscillator as the system clock.

The AD9028 is designed to operate with a 50% duty cycle ENCODE signal; adjustment of the duty cycle may improve the dynamic performance of individual devices. Since the ENCODE signal is driven differentially, the logic levels are not critical. Users should remember, however, that reduced logic levels will reduce the slew rate of the edges, and effectively increase the jitter of the signal. ECL terminations for the ENCODE and $\overline{\text{ENCODE}}$ signals should be as close as possible to the AD9028 package to avoid reflections.



AD9028 Timing Diagram



AD9038 Timing Diagram

Output data of the AD9028, D_{0A}–D_{7A} and OVERFLOW A, as well as the data ready signals, are also ECL compatible, and should be terminated through 100 Ω to −2 V (or an equivalent load). The output data can be latched on the rising edge of the DATA READY A output. For the AD9028, the DATA READY B output is simply the complement of DATA READY A.

Timing for the AD9038 is similar to the AD9028, except at the output, where the data is demultiplexed to two separate ports. Successive data samples alternate between the two ports, reducing the output data rate at either port to one-half the encode rate. Data at port A (D_{0A}–D_{7A} and OVERFLOW A) can be latched externally using the rising edge of DATA READY A. The rising edge of DATA READY B can be used to latch the data at port B (D_{0B}–D_{7B} and OVERFLOW B).

The data ready outputs for both the AD9028 and AD9038 are designed to track timing shifts over temperature.

Data Format

The format of the output data is controlled by the MSB INVERT and LSBs INVERT pins. These inputs are dc control inputs and should be connected to GROUND or $-V_S$. The AD9028/AD9038 Truth Table gives information to choose among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

The OVERFLOW INHIBIT pin controls how the converter handles overflow situations (ANALOG INPUT > $+V_{SENSE}$). For normal operation, the OVERFLOW INHIBIT is connected to $-V_S$, and the output data bits (D_{0A}–D_{7A} or D_{0B}–D_{7B}) will be at a logic LOW when ANALOG INPUT > $+V_{SENSE}$ (return to zero operation). The overflow bit (OVERFLOW A or OVERFLOW B) will indicate this condition with a logic HIGH. When the ANALOG INPUT is in range (< $+V_{SENSE}$), the overflow bit will remain at logic LOW.

If the OVERFLOW INHIBIT pin is connected to ground, the overflow bit will be disabled, and the output data will remain at logic high for overflow conditions. The overflow bits are not affected by the bit invert control pins (MSB INVERT and LSBs INVERT).

Layout and Power Supplies

Proper layout of high speed circuits is always critical, but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit.

Digital signal paths should also be kept short, and run lengths matched to avoid propagation delay mismatch. Proper ECL terminations should be located near the packages of successive gates.

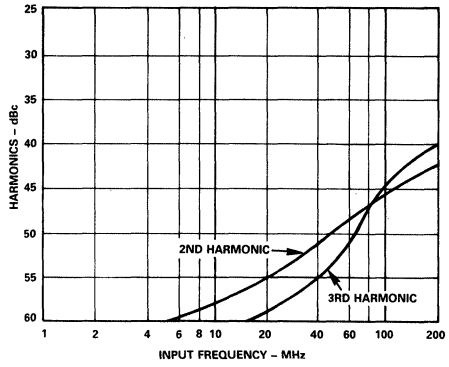
In high speed circuits, layout of the ground circuit is the most important factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground.

Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane.

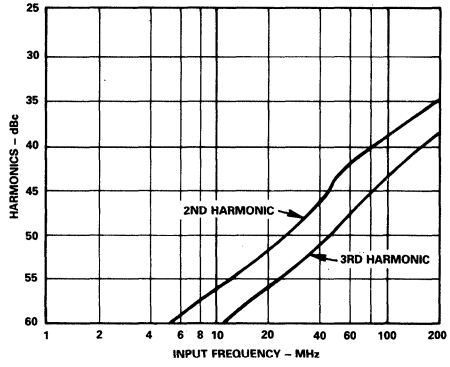
It is especially important to maintain the continuity of the ground plane under and around the AD9028/AD9038. If the system design separates the digital and analog grounds, analog ground is the preferred ground point for the A/D section of the system.

The tops of the AD9028/AD9038 packages are internally connected to the device substrates, and electrically connected to $-V_S$. The top of the package is designed to serve as a heat sink; the bottom of the package is not internally connected.

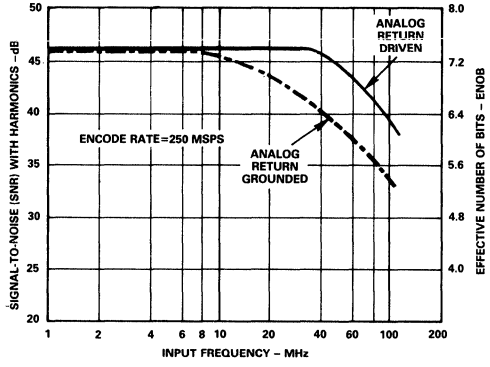
Sockets limit the dynamic performance and should be used only for prototypes or evaluation.



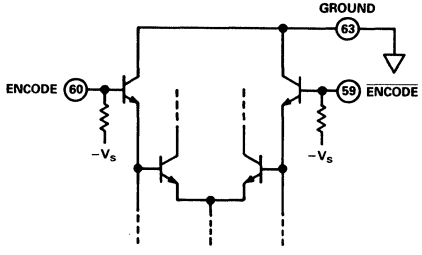
AD9028/AD9038 Harmonics vs. Input Frequency with Analog Return Driven



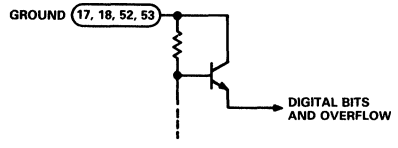
AD9028/AD9038 Harmonics vs. Input Frequency with Analog Return Grounded



AD9028/AD9038 SNR and ENOB vs. Input Frequency



Encode and $\overline{\text{Encode}}$ Equivalent Circuits

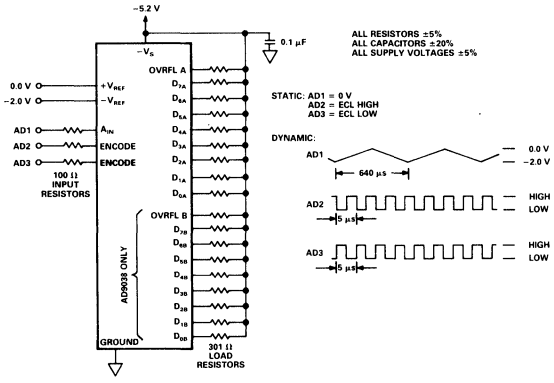


Equivalent Digital Outputs

Step	Range	Ovrfl. Inh.	Offset Binary		Twos Complement	
			True	Inverted	True	Inverted
	0 = −2 V FS = 0 V		MSB INV. = "0" LSBs INV. = "0"	MSB INV. = "1" LSBs INV. = "1"	MSB INV. = "1" LSBs INV. = "0"	MSB INV. = "0" LSBs INV. = "1"
256	≥0.000	"0"	(1)00000000	(1)11111111	(1)10000000	(1)01111111
256	≥0.000	"1"	(0)11111111	(0)00000000	(0)01111111	(0)10000000
255	−0.008	x	11111111	00000000	01111111	10000000
254	−0.016	x	11111110	00000001	01111110	10000001
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
129	−0.992	x	10000000	01111111	00000000	11111111
128	−1.000	x	01111111	10000000	11111111	00000000
127	−1.008	x	01111110	10000001	11111110	00000001
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
02	−1.992	x	00000010	11111101	10000010	01111101
01	−2.000	x	00000001	11111110	10000001	01111110
00	<−2.000	x	00000000	11111111	10000000	01111111

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT, LSBs INVERT, and OVERFLOW INHIBIT are considered dc controls.

AD9028/AD9038 Truth Table

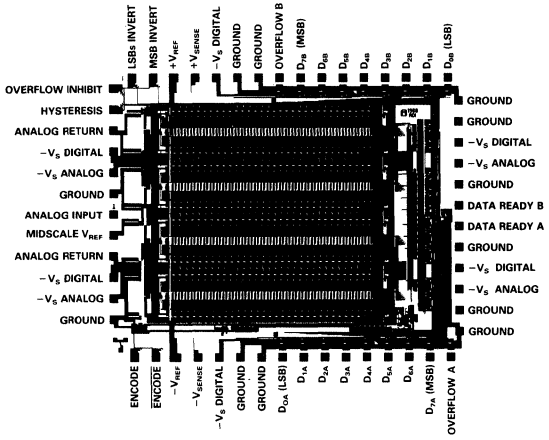


AD9028/AD9038 Burn-In Diagram

MIL-STD-883 Compliance Information

The AD9028/AD9038TE/TZ/SE/SZ/883 devices are classified within Microcircuits Group 57, Technology Group D (bipolar A/D converters) and are constructed in accordance with MIL-STD-883. The AD9028/AD9038 are electrostatic sensitive and fall within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A=T_C=T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.



MECHANICAL INFORMATION

Die Dimensions	178 × 148 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic
Bond Wire	1.3 mil, Gold; Gold Ball Bonding

ORDERING INFORMATION

Model	Temperature	Description	Package Options*
AD9028JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9028KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9028JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9028KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9028SE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9028TE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9028SZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9028TZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9038JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9038KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9038JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9038KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9038SE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9038TE/883	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9038SZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9038TZ/883	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68

*See Section 14 for package outline information.

ANALOG DEVICES

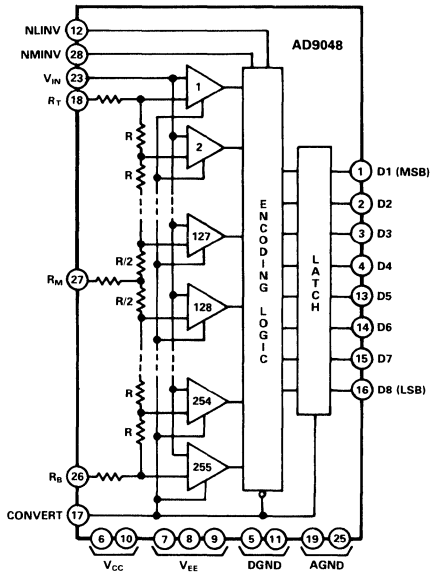
Monolithic 8-Bit Video A/D Converter

AD9048

FEATURES
35MSPS Encode Rate
16pF Input Capacitance
550mW Power Dissipation
Industry-Standard Pinouts

APPLICATIONS
Professional Video Systems
Special Effects Generators
Electro-Optics
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)

AD9048 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9048 is an 8-bit, 35MSPS flash converter, made on a high speed bipolar process, which is an alternate source for the TDC1048 unit but offers enhancements over its predecessor. Lower power dissipation makes the AD9048 attractive for a variety of system designs.

Because of its wide bandwidth, it is an ideal choice for real-time conversion of video signals. Input bandwidth is flat with no missing codes.

Clocked latching comparators, encoding logic and output buffer registers operating at minimum rates of 35MSPS preclude a need for a sample-and-hold (S/H) or track-and-hold (T/H) in most system designs using the AD9048. All digital control inputs and outputs are TTL compatible.

Devices operating over two ambient temperature ranges and with two grades of linearity are available. Linearities of either 0.5LSB or 0.75LSB can be ordered for a commercial range of 0 to +70°C, or extended case temperatures of −55°C to +125°C. Commercial versions are packaged in 28-pin DIPs and plastic leaded chip carriers (PLCCs); extended temperature versions are available in ceramic DIP and ceramic LCC packages. Both commercial units and MIL-STD-883 units are standard products.

SPECIFICATIONS (typical with nominal supplies unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} to DGND . . . . . −0.5V dc to +7.0V dc
AGND to DGND . . . . . −0.5V dc to +0.5V dc
V_{EE} to AGND . . . . . +0.5V dc to −7.0V dc
V_{IN}, V_{RT} or V_{RB} to AGND . . . . . +0.5V to V_{EE}
V_{RT} to V_{RB} . . . . . −2.2V dc to +2.2V dc
CONV, NMINV or NLINV to DGND . −0.5V dc to +5.5V dc
Applied Output Voltage to DGND . −0.5V dc to +5.5V dc[2]
Applied Output Current, Externally Forced
. . . . . −1.0mA to +6.0mA[3,4]
Output Short-Circuit Duration . . . . . 1.0sec[5]
Operating Temperature Range (Ambient)
AD9048JN/KN/JP/KP/JQ/KQ . . . . . 0 to +70°C
AD9048SE/SQ/TE/TQ/883B . . . . . −55°C to +125°C
Maximum Junction Temperature (Plastic) . . . . . +150°C[6]
Maximum Junction Temperature (Hermetic) . . . . . +175°C[6]
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V; V_{EE} = −5.2V; Differential Reference Voltage = 2.0V, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9048JN/JP/JQ Min	Typ	Max	AD9048KN/KP/KQ Min	Typ	Max	Sub-Group[7]	AD9048SE/SQ/883B Min	Typ	Max	AD9048TE/TQ/883B Min	Typ	Max	Units
RESOLUTION			8			8				8			8			Bits
DC ACCURACY																
Differential Nonlinearity	+25°C	I		0.4	0.75		0.3	0.5	7		0.4	0.75		0.3	0.5	LSB
	Full	VI			1.0			0.65	8			1.0			0.5	LSB
Integral Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5	7		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.65	8			1.0			0.5	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			7,8	GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR																
Top of Reference Ladder	+25°C	I		5	12		5	12	7		5	12		5	12	mV
	Full	VI			12			12	8			12			12	mV
Bottom of Reference Ladder	+25°C	I		4	10		4	10	7		4	10		4	10	mV
	Full	VI			10			10	8			10			10	mV
Offset Drift Coefficient	Full	V		20			20				20			20		μV/°C
ANALOG INPUT																
Input Voltage Range	Full	V		−2.1; +0.1			−2.1; +0.1				−2.1; +0.1			−2.1; +0.1		V
Input Bias Current[8,9,10]	+25°C	I		36	60		36	60	1		36	60		36	60	μA
	Full	VI			100			100	2,3			100			100	μA
Input Resistance	+25°C	I	200	300		200	300		1	200	300		200	300		kΩ
	Full	VI	40			40			2,3	40			40			kΩ
Input Capacitance	+25°C	III		16	20		16	20	12		16	20		16	20	pF
Full Power Bandwidth[11]	+25°C	III	10	15		10	15		12	10	15		10	15		MHz
REFERENCE INPUT																
Positive Reference Voltage[12]	Full	V		0.0			0.0				0.0			0.0		V
Negative Reference Voltage[12]	Full	V		−2.0			−2.0				−2.0			−2.0		V
Differential Reference Voltage	Full	V		2.0			2.0				2.0			2.0		V
Reference Ladder Resistance	Full	VI	50	90	125	50	90	125	1,2,3	50	90	125	50	90	125	Ω
Ladder Temperature Coefficient	Full	V		0.22			0.22				0.22			0.22		Ω/°C
Reference Ladder Current[13]	Full	VI		23	40		23	40	1,2,3		23	40		23	40	mA
Reference Input Bandwidth	+25°C	V		10			10				10			10		MHz
DYNAMIC PERFORMANCE[14]																
Conversion Rate[13,15]	+25°C	I	35	38		35	38		4	35	38		35	38		MHz
Aperture Delay	+25°C	III		2.4	5		2.4	5	12		2.4	5		2.4	5	ns
Aperture Uncertainty (Jitter)	+25°C	III		25	50		25	50	12		25	50		25	50	ps
Output Delay (t_{PD})[9,13]	+25°C	I		13	15		9	12	9		9	12		9	12	ns
Output Hold Time (t_{OH})[16]	+25°C	I	5	8		5	8		9	5	8		5	8		ns
Transient Response[17]	+25°C	I		6	20		6	20	4		6	20		6	20	ns
Overvoltage Recovery Time[18]	+25°C	V		8			8				8			8		ns
Rise Time	+25°C	I			9			9	9			9			9	ns
Fall Time	+25°C	I			14			14	9			14			14	ns
Output Time Skew[19]	+25°C	I		4.5	7		4.5	7	9		4.5	7		4.5	7	ns
NMINV and NLINV INPUTS[9,13]																
+0.4V Input Current	Full	VI			200			200	1,2,3			200			200	μA
+2.4V Input Current	Full	VI			10			10	1,2,3			10			10	μA
+5.5V Input Current	Full	VI			10			10	1,2,3			10			10	μA
CONVERT INPUT																
Logic "1" Voltage	Full	VI	2.0			2.0			7,8	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	7,8			0.8			0.8	V
Logic "1" Current (V_I = +2.4V)[9,13]	Full	VI			15			15	1,2,3			15			15	μA
Logic "1" Current (V_I = +5.5V)[9,13]	Full	VI			15			15	1,2,3			15			15	μA
Logic "0" Current[9,13]	Full	VI			400			400	1,2,3			400			400	μA
Input Capacitance	+25°C	III		4	6		4	6	12		4	6		4	6	pF
Convert Pulse Width (LOW)	+25°C	I	18			18			4	18			18			ns
Convert Pulse Width (HIGH)	+25°C	I	10			10			4	10			10			ns

Parameter (Conditions)	Temp	Test Level	AD9048JN/JP/JQ Min	Typ	Max	AD9048KN/KP/KQ Min	Typ	Max	Sub-Group[7]	AD9048SE/SQ/883B Min	Typ	Max	AD9048TE/TQ/883B Min	Typ	Max	Units
AC LINEARITY																
In-Band Harmonics																
dc to 2.438MHz[20]	+25°C	I	47	50		49	55		4	47	50		49	55		dBc
dc to 9.35MHz[21]	+25°C	V		48			48				48			48		dBc
Signal-to-Noise Ratio (SNR)[20]																
1.248MHz Input Frequency[22]	+25°C	I	43.5	44		45	46		4	43.5	44		45	46		dB
2.438MHz Input Frequency[22]	+25°C	I	43	44		44	46		4	43	44		44	46		dB
1.248MHz Input Frequency[23]	+25°C	I	52.5	53		54	55		4	52.5	53		54	55		dB
2.438MHz Input Frequency[23]	+25°C	I	52	53		53	55		4	52	53		53	55		dB
Signal-to-Noise Ratio (SNR)[21]																
1.248MHz Input Frequency[22]	+25°C	I	43.5	44		45	46		4	43.5	44		45	46		dB
9.35MHz Input Frequency[22]	+25°C	V		40.5			40.5				40.5			40.5		dB
Noise Power Ratio (NPR)[24]	+25°C	III	36.5	39		36.5	39		12	36.5	39		36.5	39		dB
Differential Phase[25]	+25°C	III			1			1	12			1			1	Degree
Differential Gain[25]	+25°C	III			2			2	12			2			2	%
DIGITAL OUTPUTS																
Logic "1" Voltage[15]	Full	VI	2.4			2.4			1,2,3	2.4			2.4			V
Logic "0" Voltage[10,15]	Full	VI			0.5			0.5	1,2,3			0.5			0.5	V
Short Circuit Current[5]	Full	VI			30			30	1,2,3			30			30	mA
POWER SUPPLY																
Positive Supply Current (+5.5V)	+25°C	I		34	40		34	40	1		34	40		34	40	mA
(V_{EE} = −5.5V)	Full	VI			40			40	2,3			40			40	mA
Negative Supply Current (−5.5V)	+25°C	I		90	110		90	110	1		90	110		90	110	mA
	Full	VI			120			120	2,3			120			120	mA
Nominal Power Dissipation	+25°C	V		550			550				550			550		mW
Reference Ladder Dissipation	+25°C	V		45			45				45			45		mW

NOTES:
[1]Maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the device may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
[2]Applied voltage must be current-limited to specified range.
[3]Forcing voltage must be limited to specified range.
[4]Current is specified as negative when flowing into the device.
[5]Output High; one pin to ground; one second duration.
[6]Typical thermal impedances (no air flow) are as follows:
Ceramic DIP: θ_{JA} = 49°C/W; θ_{JC} = 15°C/W LCC: θ_{JA} = 69°C/W; θ_{JC} = 21°C/W
Plastic DIP: θ_{JA} = 58°C/W; θ_{JC} = 16°C/W PLCC: θ_{JA} = 59; θ_{JC} = 19
To calculate juntion temperature (T_J), use power dissipation (PD) and thermal impedance:
$T_J = PD(\theta_{JA}) + T_{AMBIENT} = PD(\theta_{JC}) = + T_{CASE}$
[7]Military subgroups apply only to military-grade devices.
[8]Measured with V_{IN} = 0V and CONVERT low (sampling mode).
[9]V_{CC} = +5.5V
[10]V_{EE} = −5.5V
[11]Determined by beat frequency testing for no missing codes.
[12]$V_{RT} \geq V_{RB}$ under all circumstances.
[13]V_{EE} = −4.9V
[14]Outputs terminated with 40pF and 810Ω pull-up resistors.
[15]V_{CC} = +4.5V
[16]Interval from 50% point of leading edge CONVERT pulse to change in output data.
[17]For full scale step input, 8-bit accuracy attained in specified time.
[18]Recovers to 8-bit accuracy in specified time after −3V input overvoltage.
[19]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit time skew differences.
[20]Measured at 20MHz encode rate with analog input 1dB below full scale.
[21]Measured at 35MHz encode rate with analog input 1dB below full scale.
[22]RMS signal to rms noise.
[23]Peak signal to rms noise.
[24]DC to 8MHz noise bandwidth with 1.248MHz slot; four sigma loading; 20MHz encode.
[25]Clock frequency = 4 × NTSC = 14.32MHz. Measured with 40-IRE modulated ramp.
Specifications subject to change without notice.

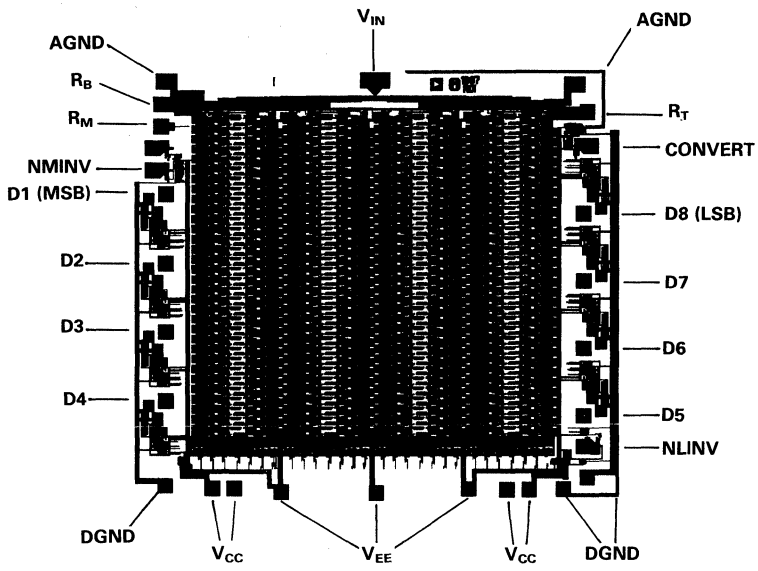
EXPLANATION OF TEST LEVELS

Test Level I – 100% production tested.
Test Level II – 100% production tested at +25°C and sample tested at specified temperatures.
Test Level III – Sample tested only.
Test Level IV – Parameter is guaranteed by design and characterization testing.
Test Level V – Parameter is a typical value only.
Test Level VI – All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF SUBGROUPS

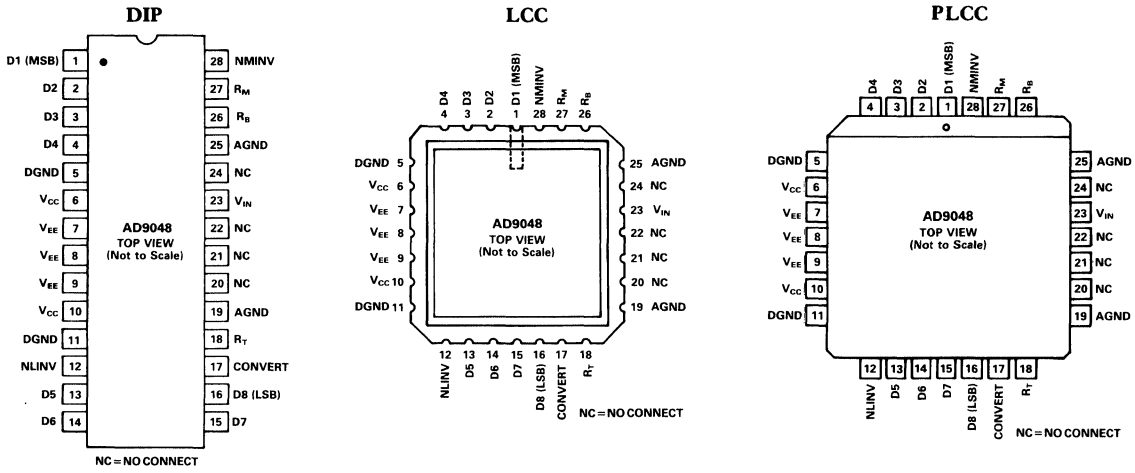
Subgroup 1 – Static tests at +25°C. (5% PDA calculated against Subgroup 1 for MIL-STD-883B versions.)
Subgroup 2 – Static tests at maximum rated operating temperature.
Subgroup 3 –Static tests at minimum rated operating temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated operating temperature.
Subgroup 6 – Dynamic tests at minimum rated operating temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated operating temperature.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated operating temperature.
Subgroup 11 – Switching tests at minimum rated operating temperature.
Subgroup 12 – Periodically sample tested.

MECHANICAL INFORMATION



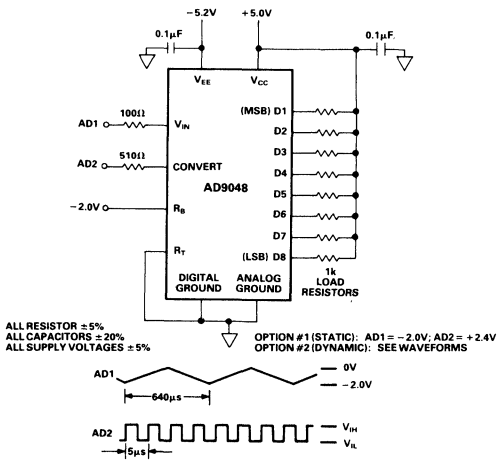
Die Dimensions	127 × 140 × 4 (± 2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	V_{EE}
Passivation	Nitride
Die Attach	Gold Eutectic
Bond Wire	1 mil Gold; Gold Ball Bonding

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

Pin Name	Description
D1 – D8	Eight digital outputs. D1 (MSB) is the most significant bit of the digital output word; D8 (LSB) is the least significant bit.
AGND	One of two analog ground returns. Both grounds should be connected together and to low impedance ground plane near the AD9048.
DGND	One of two digital ground returns. Both grounds should be connected together and to low impedance ground plane near the AD9048.
V_{CC}	Positive supply terminals; nominally +5.0V.
V_{EE}	Negative supply terminals; nominally −5.2V.
CONVERT	Input for conversion signal; sample of analog input signal taken on rising edge of this pulse.
R_B	Most negative reference voltage for internal reference ladder.
R_M	Midpoint tap on internal reference ladder.
R_T	Most positive reference voltage for internal reference ladder.
V_{IN}	Analog input signal pin.
NMINV	"Not Most Significant Bit Invert." In normal operation, this pin floats high; logic LOW at NMINV inverts most significant bit of digital output word [D1 (MSB)].
NLINV	"Not Least Significant Bit Invert." In normal operation, this pin floats high; logic LOW at NLINV inverts the seven least significant bits of the digital output word.



AD9048 Burn-In Diagram

MIL-STD-883 Compliance Information

The AD9048SE/TE/SQ/TQ/883B devices are classified within Microcircuits Group 57, Technology Group D (bipolar A/D converters) and are constructed in accordance with MIL-STD-883. The AD9048 is electrostatic sensitive and falls within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.

THEORY OF OPERATION

Refer to the block diagram of the AD9048. The AD9048 comprises three functional sections: a comparator array, encoding logic, and output latches.

Within the array, the analog input signal to be digitized is compared with 255 reference voltages. The outputs of all comparators whose references are below the input signal level will be high; and outputs whose references are above that level will be low.

The n-of-255 code which results from this comparison is applied to the encoding logic where it is converted into binary coding. When it is inverted with dc signals applied to the NLINV and/or NMINV pins, it becomes twos complement.

After encoding, the signal is applied to the output latch circuits where it is held constant between updates controlled by the application of CONVERT pulses.

The AD9048 uses strobed latching comparators in which comparator outputs are either high or low, as dictated by the analog input level. Data appearing at the output pins have a pipeline delay of one encode cycle.

Input signal levels between the references applied to R_T (Pin 18) and R_B (Pin 26) will appear at the output as binary numbers between 0 and 255, inclusive. Signals outside that range will show up as either full-scale positive or full-scale negative outputs. No damage will occur to the AD9048 as long as the input is within the voltage range of V_{EE} to +0.5V.

The significantly reduced input capacitance of the AD9048 lowers the drive requirements of the input buffer/amplifier and also induces much smaller phase shift in the analog input signal.

Applications which depend on controlled phase shift at the converter input can benefit from using the AD9048 because of its inherently lower phase shift.

The CONVERT, analog input and digital output circuits are shown in Figure 1, AD9048 Input/Output Circuits.

System timing which provides details on delays through the AD9048, as well as the relationships of various timing events, is shown in Figure 2, AD9048 Timing Diagram.

Dynamic performance of the AD9048, i.e., typical signal-to-noise ratio, is illustrated in Figures 3 and 4.

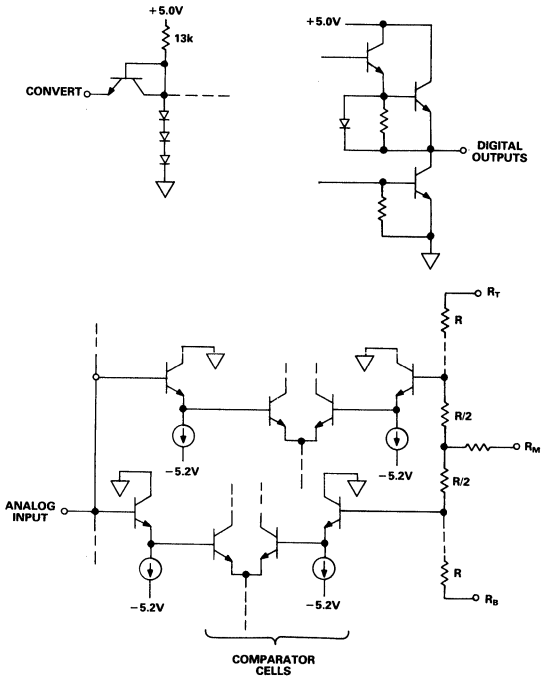


Figure 1. Input/Output Circuits

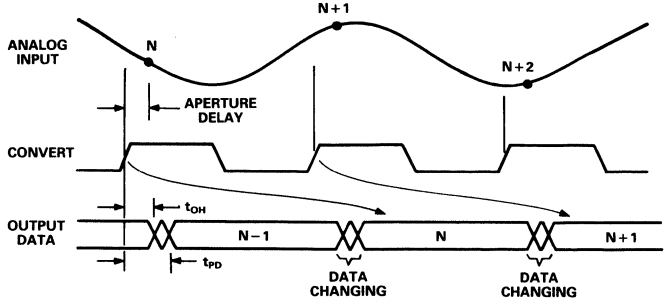


Figure 2. AD9048 Timing Diagram

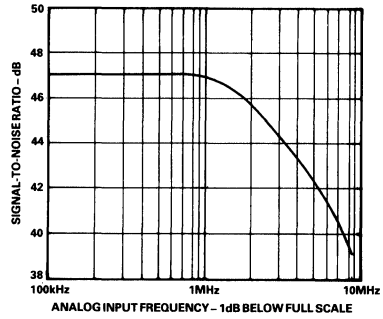


Figure 3. AD9048 Dynamic Performance (20MHz Encode Rate)

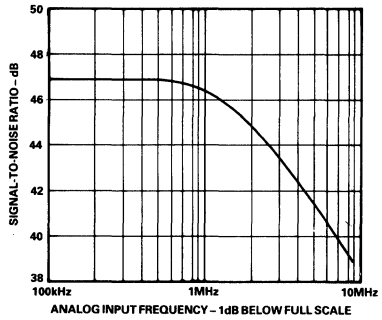


Figure 4. AD9048 Dynamic Performance (35MHz Encode Rate)

LAYOUT SUGGESTIONS

Designs which use the AD9048 or any other high-speed device must follow some basic layout rules to insure optimum performance.

The first requirement is to have a large, low impedance ground plane under and around the converter. If the system uses separate analog and digital grounds, both should be connected solidly together and to the ground plane as close to the AD9048 as practical, to avoid ground loop currents.

Ceramic 0.1μF decoupling capacitors should be placed as close as possible to the supply pins of the AD9048. For decoupling low frequency signals, use 10μF tantalum capacitors, also connected as close as practical to voltage supply pins.

Within the AD9048, reference currents may vary because of coupling between the clock and input signals. Because of this, it is important that the ends of the reference ladder, R_T (Pin 18) and R_B (Pin 28), be connected to low impedances (as measured from ground).

If the AD9048 is being used in a circuit in which the reference is not varied, a bypass capacitor to ground is strongly recommended. In applications which use varying references, they must be driven from a low impedance source.

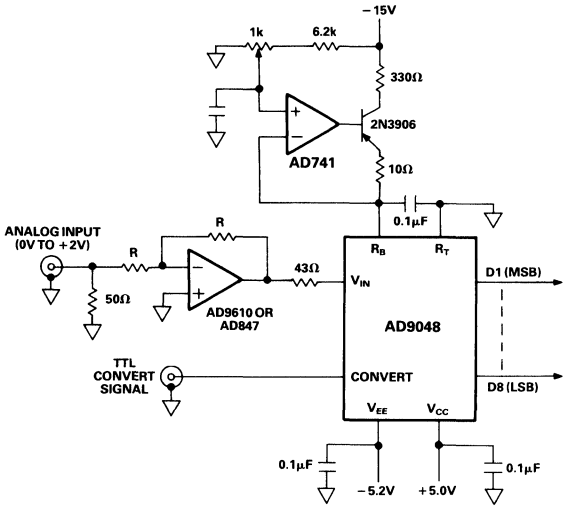


Figure 5. AD9048 Typical Connections

Step	Range		Binary		Offset Twos Complement	
			True	Inverted	True	Inverted
	−2.000V FS	−2.0480V FS	NMINV = 1	0	0	1
	7.8431mV Step	8.000mV Step	NLINV = 1	0	1	0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	−0.0078V	−0.0080V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	−0.9961V	−1.0160V	01111111	10000000	11111111	00000000
128	−1.0039V	−1.0240V	10000000	01111111	00000000	11111111
129	−1.0118V	−1.0320V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	−1.9921V	−2.0320V	11111110	00000001	01111110	10000001
255	−2.0000V	−2.0400V	11111111	00000000	01111111	10000000

AD9048 Truth Table

ORDERING INFORMATION

Model	Linearity	Temperature	Description	Package Options*
AD9048JN	0.75LSB	0 to +70°C	28-Pin Plastic DIP	N–28
AD9048KN	0.5LSB	0 to +70°C	28-Pin Plastic DIP	N–28
AD9048JP	0.75LSB	0 to +70°C	28-Pin PLCC	P–28A
AD9048KP	0.5LSB	0 to +70°C	28-Pin PLCC	P–28A
AD9048JQ	0.75LSB	0 to +70°C	28-Pin Ceramic DIP	Q–28
AD9048KQ	0.5LSB	0 to +70°C	28-Pin Ceramic DIP	Q–28
AD9048SE/883B	0.75LSB	−55°C to +125°C	28-Pin LCC	E–28A
AD9048TE/883B	0.5LSB	−55°C to +125°C	28-Pin LCC	E–28A
AD9048SQ/883B	0.75LSB	−55°C to +125°C	28-Pin Ceramic DIP	Q–28
AD9048TQ/883B	0.5LSB	−55°C to +125°C	28-Pin Ceramic DIP	Q–28

*See Section 14 for package outline information.

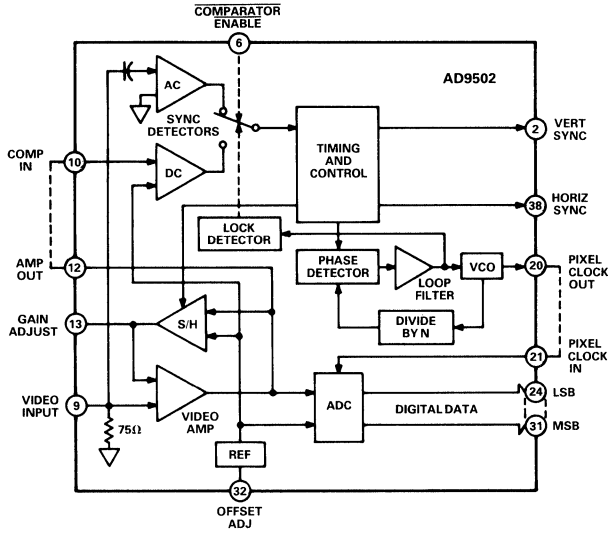
Hybrid RS-170 Video Digitizer

AD9502

FEATURES
8-Bit Gray Scale Resolution
Screen Resolution to 512×512
Phase-Locked Pixel Clock
TTL Compatible

APPLICATIONS
Machine Vision Systems
Automatic Inspection
Image Processing

AD9502 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices' AD9502 is a video digitizer which converts RS-170, NTSC, or PAL camera signals directly into 8-bit digital information and control signals.

All of the analog preprocessing functions needed to move from the analog world of cameras to the digital world of signal processing are contained in this single hybrid component.

Included are a video amplifier with dc restoration, sync detector and separator, phase-locked pixel clock oscillator, and an 8-bit analog-to-digital converter. The AD9502 is also extremely adapatable by virtue of providing for ±3dB gain control and offset variations of 0 to 10 IRE units. These latter characteristics increase the flexibility of the device by making it useable over a wide range of input signal amplitudes and set up level outputs from various types of cameras.

A pixel clock synchronized to the sync portion of the composite signal is generated by the phase-locked oscillator and the sync detector/separator circuit. Depending on model number, the nominal frequency of this clock is 7.31MHz, 9.83MHz, or 12.85MHz. These frequencies correspond to 512 pixels per line or 384 pixels per line, and aspect ratios of 4:3 or 1:1.

In addition to the pixel clock, AD9502 control signals also include horizontal and vertical sync pulses. This combination of outputs allows the user to manage frame memory efficiently; output data can be precisely located for optimum support of complex digital signal processing algorithms.

Six models of the AD9502 are available; all units operate over case temperature ranges of −25°C to +85C. Models AD9502AM, AD9502BM, and AD9502CM with pixel clock frequencies of 7.31MHz, 9.83MHz, and 12.85MHz, respectively, are tested at +25°C. Models AD9502AMB, AD9502BMB, and AD9502CMB, with the same clock frequencies, are tested at temperatures from −25°C to +85°C. During their manufacturing, these latter units also receive additional high-reliability processing.

SPECIFICATIONS (typical @ +25°C with nominal supplies, unless otherwise noted)

Parameter[1,2]	Sub Group	Temp	−25°C to +85°C AD9502AM/BM/CM[1] Min	Typ	Max	−25°C to +85°C AD9502AMB/BMB/CMB[2] Min	Typ	Max	Units
RESOLUTION									
(GS = Gray Scale)				8			8		Bits
(FS = Full Scale)				0.4			0.4		%GS
# LSB WEIGHT[3]				8.4			8.4		mV
				0.39			0.39		IRE Units
ACCURACY									
√ Integral Linearity	4	+25°C		±1.0	±2.5		±1.0	±2.5	%FS
	5,6	Full		±1.5	±3.0		±1.5	±3.0	%FS
√ Differential Linearity[4]	4	+25°C		±2	±3.0		±2	±3.0	LSB
	5,6	Full		±2	±3.0		±2	±3.0	LSB
√ Initial Offset[5]	4	+25°C		±50	±200		±50	±200	mV
# Offset vs. Temperature		Full		±250			±250		µV/°C
√ Gain[6]	4	+25°C	1.91	2.8	4	1.91	2.8	4	V/V
# Gain vs. Temperature[7]		Full		±250			±250		ppm/°C
DYNAMIC CHARACTERISTICS									
Output Data Rate (Pixel Clock)[8]									
√ AD9502AM/AMB	9,10,11	Full		7.31			7.31		MHz
√ AD9502BM/BMB	9,10,11	Full		9.83			9.83		MHz
√ AD9502CM/CMB	9,10,11	Full		12.85			12.85		MHz
# Sampling Jitter		+25°C		1	5		1	5	ns, rms
# Digital Output Delay		+25°C	20	30	50	20	30	50	ns
√ Horizontal Sync Delay	9	+25°C	−0.4	0.3	0.7	−0.4	0.3	0.7	µs
√ Horizontal Sync Delay	10,11	Full	−0.4	0.3	0.7	−0.4	0.3	0.7	µs
√Horizontal Sync Width	9	+25°C	4.5	4.8	5.4	4.5	4.8	5.4	µs
√Horizontal Sync Width	10,11	Full	4.5	4.8	5.4	4.5	4.8	5.4	µs
√Vertical Sync Delay	9	+25°C	5.5	6.0	6.7	5.6	6.0	6.7	µs
√Vertical Sync Delay	10,11	Full	5.5	6.0	6.7	5.6	6.0	6.7	µs
√Sample Delay	9	+25°C	7.9	9.0	9.4	7.9	9.0	9.4	µs
√Sample Delay	10,11	Full	7.9	9.0	9.4	7.9	9.0	9.4	µs
VIDEO INPUT									
Signal Type				RS-170			RS-170		
√ Impedance	1	+25°C	67	75	83	67	75	83	Ω
√ Impedance	2,3	Full	67	75	83	67	75	83	Ω
Input level for rated performance									
# Amplitude		+25°C	0.71	1.0	1.41	0.71	1.0	1.41	Vp-p
# Amplitude		Full	0.71	1.0	1.41	0.71	1.0	1.41	Vp-p
# Dynamic Range									
(back porch ref. to ground)		25°C	−0.83		+1.5	−0.83		+1.5	V
# Dynamic Range		Full	−0.83		+1.5	−0.83		+1.5	V
# Bandwidth (3dB)		+25°C	5	7.5		5	7.5		MHz
# Bandwidth (3dB)		Full	5	7.5		5	7.5		MHz
AUXILIARY SYNC INPUT[9]									
Comparator (Pin 10)									
Width			1		6	1		6	µs
Frequency[8]				15.75			15.75		kHz
# Loading				<1			<1		TTL Load
Input Current									
√ I_{IN} High (V_{IN} = 2.75V)	1	+25°C			50			50	µA
√ I_{IN} Low (V_{IN} = 2.3V)	1	+25°C			50			50	µA
√ Logic Level "1"	1	+25°C	+2.75			+2.75			V
√ Logic Level "0"	1	+25°C			+2.3			+2.3	V
√ I_{IN} High (V_{IN} = 2.75V)	2,3	Full			50			50	µA
√ I_{IN} Low (V_{IN} = 2.3V)	2,3	Full			50			50	µA
√ Logic Level "1"	2,3	Full	+2.75			+2.75			V
√ Logic Level "0"	2,3	Full			+2.3			+2.3	V

Parameter[1,2]	Sub Group	Temp	−25°C to +85°C AD9502AM/BM/CM[1] Min	Typ	Max	−25°C to +85°C AD9502AMB/BMB/CMB[2] Min	Typ	Max	Units
AUXILIARY SYNCH INPUT[9] (Cont.)									
Comparator Enable (Pin 6)									
# Loading				<1			<1		TTL Load
Input Current									
√ I_{IN} Low (V_{IN} = 0.0V)	1	+25°C			±400			±400	µA
√ I_{IN} High (V_{IN} = 5.0V)	1	+25°C			±400			±400	µA
√ Logic Level "1"	1	+25°C	+3.15			+3.15			V
√ Logic Level "0"	1	+25°C			+1.2			+1.2	V
√ I_{IN} High (V_{IN} = 0V)	2,3	Full			±400			±400	µA
√ I_{IN} Low (V_{IN} = 5.0V)	2,3	Full			±400			±400	µA
√ Logic Level "1"	2,3	Full	+3.15			+3.15			V
√ Logic Level "0"	2,3	Full			+0.9			+0.9	V
DIGITAL OUTPUTS									
Coding[10]			Comp. Binary (CBN)			Comp. Binary (CBN)			
Logic Compatibility			TTL			TTL			
√ Logic Level "1"	1	+25°C	+2.4			+2.4			V
√ Logic Level "0"	1	+25°C			+0.5		+0.5		V
√ Logic Level "1"	2,3	Full	+2.4			+2.4			V
√ Logic Level "0"	2,3	Full			+0.5		+0.5		V
√ Drive	1	+25°C	≥2			≥2			TTL Loads
√ Drive	2,3	Full	≥2			≥2			TTL Loads
# Time Skew		+25°C		10		10			ns
# Time Skew		Full		10		10			ns
POWER REQUIREMENTS									
√ +V_S (+12 to +15V dc)	1	+25°C		50	75		50	75	mA
√ −V_S (−12 to −15V dc)	1	+25°C		30	45		30	45	mA
√ +V_{CC} (+5V dc ±5%)	1	+25°C		110	150		110	150	mA
√ Power Dissipation	1	+25°C		1.75	2.55		1.75	2.55	W
√ +V_S (+12 to +15V dc)	2,3	Full		50	75		50	75	mA
√ −V_S (−12 to −15V dc)	2,3	Full		30	45		30	45	mA
√ V_{CC} (+5V dc ±5%)	2,3	Full		110	150		110	150	mA
√ Power Dissipation	2,3	Full		1.75	2.55		1.75	2.55	W
THERMAL RESISTANCE									
# Junction to Air (θ_{JA})				18			18		°C/W
# Junction to Case (θ_{JC})				4			4		°C/W
PACKAGE OPTION[11]			AD9502AM			AD9502AMB			
M-40			AD9502BM			AD9502BMB			
			AD9502CM			AD9502CMB			

NOTES
√ 100% tested (see Notes 1 and 2).
Specification guaranteed by design; not tested.
[1]AD9502AM/BM/CM specifications preceded by a check (√) are tested at +25°C ambient temperature; performance is guaranteed over case temperature range of −25°C to 85°C.
[2]AD9502AMB/BMB/CMB specifications preceded by a check (√) are tested at −25°C case, +25°C ambient, and +85°C case temperatures unless otherwise indicated (See Explanation of Group A Military Subgroups).
[3]Internal ADC reference = 2.15V = 100 IRE units.
[4]Specifications shown guaranteed over temperature on AD9502AMB/BMB/CMB.
[5]Offset is difference between voltage reference at OFFSET ADJUST (Pin 32) and the dc restored voltage value at AMP OUT (Pin 12). Offset is adjustable with external potentiometer to accommodate 0 to 10 IRE units of setup level.
[6]Adjustable with external potentiometer. Compensates for 3dB variation from nominal 1V p-p composite signal.
[7]Gain tempco is equal to the voltage reference at OFFSET ADJUST (Pin 32).
[8]Pixel clock stability is directly related to 15.75kHz input clock stability. Frequency of pixel clock is set at factory for desired aspect ratio and screen resolution; consult Table I for available frequency selections.
[9]Auxiliary sync can be driven from TTL source and can be composite or horizontal only. In horizontal, no output provided at VERTICAL SYNC (Pin 2).
[10]Reference black level output code = 1111 1111; reference white = 0000 0000.
[11]See Section 14 for package outline information.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C. (10% PDA calculated against Subgroup 1 for high-rel versions.)
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

ABSOLUTE MAXIMUM RATINGS

Logic Supply Voltage ($\pm V_S$) . . . . . ±18V
Operating Temperature Range (Case)
AD9502AM/BM/CM . . . . . −25°C to +85°C
AD902AMB/BMB/CMB . . . . . −25°C to +85°C
Junction Temperature . . . . . +165°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Soldering Temperature (Soldering 10sec) . . . . +300°C

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	DO NOT CONNECT*	40	CASE GROUND
2	VERTICAL SYNC	39	GROUND
3	CASE GROUND	38	HORIZONTAL SYNC
4	GROUND	37	+5V dc
5	+5V dc	36	GROUND
6	$\overline{\text{COMPARATOR ENABLE}}$	35	+5V dc
7	DO NOT CONNECT*	34	DO NOT CONNECT*
8	+5 V dc	33	GROUND
9	VIDEO INPUT	32	OFFSET ADJUST
10	COMPARATOR INPUT	31	BIT 1 (MSB)
11	DO NOT CONNECT*	30	BIT 2
12	AMPLIFIER OUTPUT	29	BIT 3
13	GAIN ADJUST	28	BIT 4
14	+V (+12V to +15V)	27	BIT 5
15	−V (−12V to −15V)	26	BIT 6
16	GROUND	25	BIT 7
17	GROUND	24	BIT 8 (LSB)
18	DO NOT CONNECT*	23	+5V dc (ADC)
19	+5V dc (VCO)	22	ANALOG GROUND
20	PIXEL CLOCK OUT	21	PIXEL CLOCK IN

*THESE PINS ARE USED FOR FACTORY TESTING AND SHOULD NOT BE USED AS TIE POINTS OR CONNECTED INTO EXTERNAL CIRCUITS.

THEORY OF OPERATION

The use of analog-to-digital converters (ADCs) for digitizing Gray Scale picture information in a standard RS-170 composite signal is widespread throughout the video industry.

But digitizing only the picture information is not sufficient.

If a complete video frame is to be stored in memory (in a technique generally called "frame grabbing"), the composite signal from the camera must have additional processing steps applied. Among others, these include dc restoration; sync detection and separation; and synchronization to a pixel clock, often "slaved" to a master system clock. Analog circuits for achieving these operations must be combined, and interfaced to digital logic for subsequent processing of the signal.

The principal functions of "front end" video processors which receive the camera signal are to sychronize the frame memory and digitize each pixel (smallest controllable picture element) of video information.

Performing these functions is common in the video industry. But the method of accomplishing them is eased considerably with the AD9502 RS-170 Video Digitizer.

Refer to the AD9502 Functional Block Diagram.

The unit consists of four major parts: a phase-locked loop (PLL), dc restoration circuits, sync detector/timing circuits, and the ADC.

The PLL comprises a phase detector, loop filter/amplifier, voltage-controlled oscillator (VCO), and a digital divider; monolithic ICs are used for each section. The frequency of the pixel clock output (at Pin 20) is an integer multiple of the horizontal line frequency and is phase locked to the sync pulses of the incoming composite signal.

A video amplifier and the sample/hold (S/H) establish a feedback loop for dc restoration of the video input. Sync detection and timing result from the combined actions of the blocks marked AC, Lock Detector, Timing & Control, and the PLL.

Refer to Figure 1, the AD9502 Timing Diagram.

As shown, the leading edge of the sync tip pulse serves as the reference point for timing the actions of the AD9502. As part of the composite signal, these pulses are amplified and inverted by the video amplifier and drive the phase-locked loop within the unit, but only after the pulses are detected and conditioned.

The PLL is unlocked during the power-up phase, or if the input signal is missing. When it is, the comparator and all timing pulses are disabled, creating an ac-coupled signal path for synchronizing the PLL.

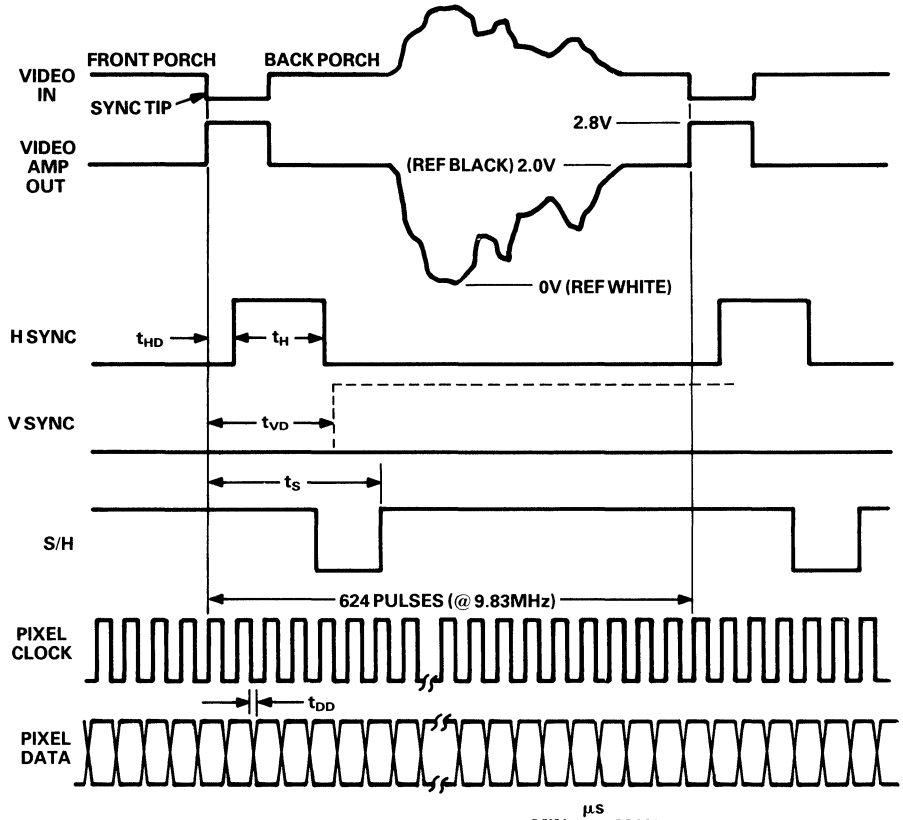
After the lock indicator detects a lock condition, the dc comparator is enabled and the ac-coupled path is disabled. The threshold of the comparator is set at slightly more than half the amplitude of the sync pulse height in the dc-restored RS-170 signal.

When the PLL is operating, the phase detector which is part of the loop generates an error voltage proportional to the timing error between the PLL's input signal (H Sync) and the VCO's divided-by-N output. If a difference exists between the two, the loop filter/amplifier shifts the VCO control voltage in the proper direction to minimize the error. The result of these actions is that the pixel clock output of the VCO is N times the horizontal frequency of the input to the AD9502.

The integer of the Divide by N circuit is set at the factory for the aspect ratio and resolution to be used by the customer and causes the phase detector to operate at a constant frequency. (Refer to ORDERING INFORMATION and Table I for details on specifying the desired frequency of the VCO).

To insure a stable pixel clock, the loop filter must block feed-through from the phase detector and noise. If it does not, the VCO will be unable to provide the required phase-coherent clock.

To some degree, clock stability and loop stability are conflicting requirements. Clock stability can be affected by noise and feed-



		µs MIN	MAX
t_{HD}	H SYNC DELAY	−0.4	+0.7
t_H	H SYNC WIDTH	+4.5	+5.4
t_{VD}	V SYNC DELAY	+5.5	+6.7
t_S	SAMPLE DELAY	+7.9	+9.4
t_{DD}	DATA DELAY	+0.02	+0.05

Figure 1. AD9502 Timing Diagram

through; loop stability can affect the acquisition time of the loop. The design of the unit has been optimized to minimize noise and feedthrough while assuring the PLL will lock during a vertical retrace period.

The vertical sync pulse (VSYNC) which is the other output of the Timing & Control circuit shown in the block diagram is generated whenever the duration of the incoming sync pulse is longer than 6.6µs. These pulses are shown with a dashed line in Figure 1 (and Figure 3) to indicate they are present only after the correct number of lines (containing horizontal sync information) have occurred and the display must be vertically retraced.

The sample-hold (S/H) pulse occurs after every incoming sync pulse except (a) when a vertical sync pulse occurs; or (b) when the PLL is not locked.

As shown, the S/H pulse occurs during the "back porch" of the composite signal. During this sample period, a closed loop formed by the video amplifier and the S/H minimizes the error between the top of the reference for the "flash" A/D converter and the back porch output level of the video amplifier.

When the S/H switches to the "hold" mode of operation during the active picture portion of the composite signal, its output inserts the correct amount of dc offset to position the video signal within the range of the A/D converter. The offset also positions the sync information properly in the range of the sync detector.

Since the RS-170 standard allows for differences in the amplitude and setup level of video signals, the AD9502 includes a capability for changing gain 3dB and varying offset by 200mV. This is illustrated in Figure 2.

Translated into practical terms pertinent to the video input, this ability to vary the input levels means the difference between the Reference Black level and the back porch of the input can be adjusted from 0 to 10 IRE units.

As indicated earlier, the internal A/D converter is a "flash" type; it provides 8 bits of resolution of the video signal. The (+2.15 volt) voltage reference shown in the block diagram is used for the reference ladder of the converter and as a reference for dc restoration. The clock and data circuits are TTL compatible, capable of encode rates as high as 15MHz.

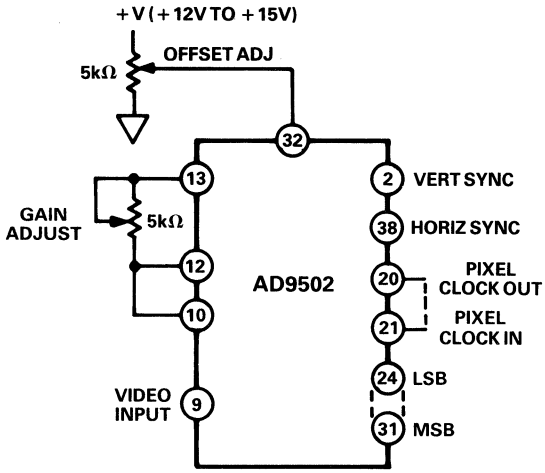


Figure 2. Offset and Gain Adjustments

MONOCHROME APPLICATIONS

The discussion of applying the AD9502 in various applications may be enhanced with a brief summary of the nature of video signals.

A standard RS-170 video signal contains 525 horizontal lines of the type shown at the top of Figure 1 in each "frame." Visible picture information is contained in 485 of these lines; the remainder are used for test and reference information.

To reduce flicker on the screen, these frames of information are divided into two "fields" which are interlaced. For presentation, all odd-numbered horizontal lines are displayed on the screen from top to bottom. During vertical retrace, the electron gun of the cathode-ray tube (CRT) is repositioned from lower right to the upper left corner. When this is completed, even-numbered lines are scanned from top to bottom.

A complete frame of two fields is presented each 1/30 of a second (displaying each 242 1/2-line field at the 60Hz rate of standard power-line frequencies is the key to this technique for reducing flicker in the presentation). This means each line of horizontal information is equal to 63.5μs, i.e., 1/30/525.

The horizontal blanking interval uses 10.9μs of this time, leaving 52.6μs for displaying active picture (more correctly, "intensity") information. The resolution of this 52.6μs line will be determined by the number of pixels (smallest controllable picture element) used to digitize it.

Resolutions of 512 pixels and 384 pixels per line are the two which are generally used for computer-based display applications.

Regardless of the number of pixels, many applications which store the complete useable portion of the line will have a 4:3 aspect ratio. This is the standard ratio for RS-170 signals but non-square pixels which can result may cause problems for certain processing algorithms.

Square pixels are more desirable for these situations, and an aspect ratio of 1:1 is oftentimes preferred. To obtain it, many systems digitize only three quarters of each horizontal line; the image which results represents the center 39.45μs of the line's 52.6μs.

The AD9502 offers pixel rates which can accommodate either 4:3 or 1:1 aspect ratios in densities of either 384 pixels/line or 512 pixels/line, as shown in Table I. The frequencies cited in the first part of the table are those associated with monochrome video signals. For color cameras which supply RGB (red, green, blue) outputs, the frequencies are slightly different because of being based on the frequency of the color burst information.

NOTE: The difference of less than 1% between the theoretical 39.45μs and the 39.8μs of Table I is because of the incremental frequency settings possible with the VCO.

In most of Europe and in many other parts of the world, the PAL standard is used. This differs from NTSC by virtue of using 625 total lines, with 575 active lines; the frame rate is 25Hz instead of 30Hz. As shown in Table I, the AD9502 can also be used for these applications.

Monochrome RS-170
Horizontal Frequency = 15.750kHz

Part No	VCO (MHz)	Aspect Ratio	Active Time (μs)*	Pixels/ Line
AD9502AM	7.308	4:3	52.5	384
AD9502BM	9.828	1:1	39.0	384
AD9502BM	9.828	4:3	52.1	512
AD9502CM	12.85	1:1	39.8	512

NTSC
Horizontal Frequency = 15.734kHz

Part No	VCO (MHz)	Aspect Ratio	Active Time (μs)*	Pixels/ Line
AD9502AM	7.301	4:3	52.6	384
AD9502BM	9.818	1:1	39.1	384
AD9502BM	9.818	4:3	52.1	512
AD9502CM	12.84	1:1	39.9	512

European PAL**
Horizontal Frequency = 15.625kHz

Part No	VCO (MHz)	Aspect Ratio	Active Time (μs)*	Pixels/ Line
AD9502BM	9.750	4:3	44.1	430
AD9502CM	12.75	1:1	44.7	575

*For aspect ratio and VCO frequency shown, this is portion of the horizontal line which will be digitized.
**See ORDERING INFORMATION section.

Table I

Frame grabbers which process the video information generally store either 512 or 256 lines of information, depending upon whether they are designed to operate on a complete frame or only on each field.

In a 256-line memory system, only one of the two fields needs to be digitized; in a 512-line system, each field is stored independently.

The memory system being used must be able to identify each field to assure that each is assigned to the correct address in the memory. Figure 3 illustrates the relationships of the horizontal and vertical sync pulses generated by the AD9502, and the incoming video signal, and makes it easier to visualize how this identification is accomplished.

As shown, the horizontal and vertical sync pulses occur in time coincidence for the first field. For the second field, the start of

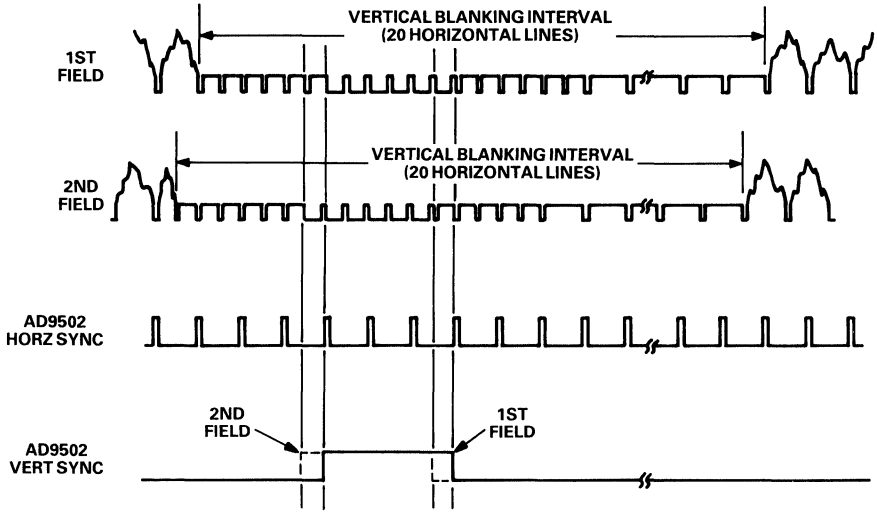


Figure 3. Field/Sync Timing Diagram

each of these two outputs occurs one-half line out of phase. In this way, the system can make a distinction between the two fields when both are to be stored.

Many systems use the pixel clock, horizontal sync, and vertical sync outputs from the AD9502 to address the frame memory for each field by triggering counters. A delay counter, in the horizontal or X axis, can be used to determine the point on the selected line where data storage begins. A second counter would count the pixels needed to obtain the desired pixels/line resolution; the number of counts will be determined by the aspect ratio being used.

Both of these counters are set by the horizontal sync pulse output of the AD9502.

Vertical retrace timing information is obtained in essentially the same way by using Y counters. For these, the counters are set by the vertical sync pulse output. The Y delay counter establishes the time of vertical retrace by counting the number of lines which occur after the vertical sync pulse; it then starts a second (lines/field) counter. The second Y counter establishes the number of lines to be digitized in each field.

Another counter circuit can be used to test for the presence or absence of the vertical sync pulse; the counter output is high if both sync pulses are present, indicating the first field.

The combination of X, Y, and first-field lines acts as address information for correctly routing the digitized picture data into the system memory.

(NOTE: Additional details are included in the Analog Devices application note, "The AD9502 Video Signal Digitizer and Its Application.")

In systems which use a master composite sync, this routing of digital information can be simplified by using the comparator enable function available on the AD9502.

Normally, Pins 10 and 12 are connected externally, as shown in the block diagram. This connection applies the output of the video amplifier to the input of the dc comparator circuit and, as discussed earlier, helps keep the PLL in a locked condition.

Alternatively, a TTL composite sync signal can be used by connecting Pin 6 ($\overline{\text{COMPARATOR ENABLE}}$) to ground. This disables the ac comparator, and the power-up and signal-loss start-up circuits; but they are no longer needed with a master sync.

Using the AD9502 in this way has the advantage of making it unnecessary for the dc comparator to operate with a video signal which may be noisy.

Besides grounding Pin 6, it is also necessary to remove the connection between Pins 10 and 12 and apply the master sync input to Pin 10. Figure 4 shows the difference in the two methods of operating the AD9502.

Note that the camera which is being used must also be locked to the master sync; if it is not, the AD9502 will not be able to sample the back porch of the composite signal for setting the dc reference of the A/D converter.

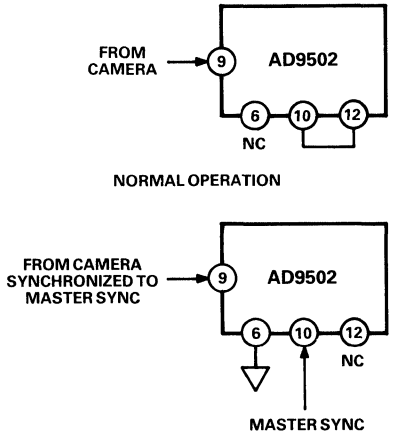


Figure 4. Monochrome Operation

COLOR (RGB) APPLICATIONS

In RGB applications, three monochrome video inputs represent the Red, Green, and Blue outputs of a color camera. Figure 5 illustrates how it is possible to configure three AD9502 units to accept RGB signals.

Generally, the Green input is used as the master sync reference; the other video digitizers are slaved from the Green sync pulses.

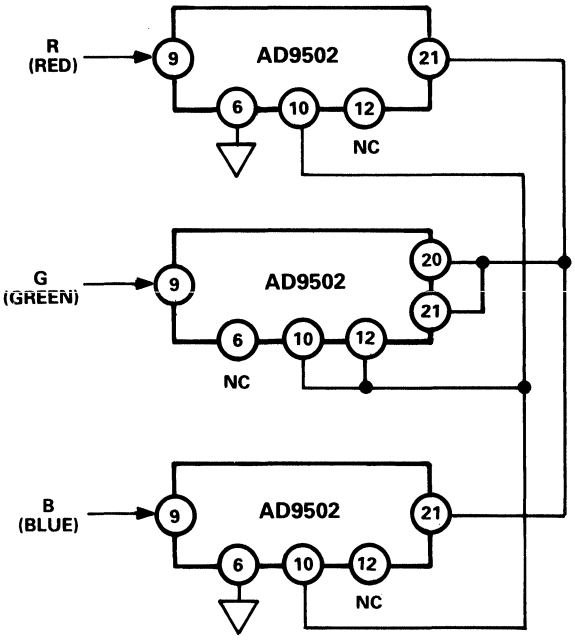


Figure 5. RGB Operation (External Pixel Clock)

When using multiple devices in this way, it is extremely important to use lead lengths which are as short as practical. The drive capability of the Green AD9502 is sufficient to drive the dc comparators in the Red and Blue digitizers, but only so long as the reactive effects of excessive lead lengths do not load the video amplifier in the Green unit.

No attempt should be made to drive low-impedance (<25kΩ) loads with the output (Pin 12) of the Green digitizer. Frame memory management should use the horizontal and vertical sync pulses only from the Green AD9502.

As shown in Figure 5, the connection between Pins 20 and 21 is removed on the Red and Blue units; instead, Pin 21 of each is tied to Pins 20 and 21 of the Green unit.

The Red and Blue digitizers must have Pin 6 grounded, with a master sync (generated by the Green sync tip pulses) applied to Pin 10. Repeating for emphasis: lead lengths need to be as short as practical when applying the high-frequency pixel clock and for all connections among the digitizers.

Variations of the applications described here are possible, depending upon the system configuration and its use. In any application using an external pixel clock, the duty cycle must be set to insure that logic low is maintained for a minimum of 30ns. A shorter interval will have an adverse effect on linearity.

VCR/VTR OPERATION

The AD9502 can be operated with VCR or VTR equipment, but the sync signals which are supplied must be conditioned to insure they are stable in frequency before being applied to the device.

ORDERING INFORMATION

Six models of the AD9502 Video Digitizer are available, with three different pixel clock frequencies. Order model AD9502AM, AD9502BM, or AD9502CM for clock frequencies, respectively, of 7.31MHz, 9.83MHz, or 12.85MHz.

For units with high-rel processing and testing at the temperature extremes of −25°C to 85°C, the model numbers with the same clock frequencies contain an additional "B" suffix, i.e., AD9502AMB, AD9502BMB, or AD9502CMB.

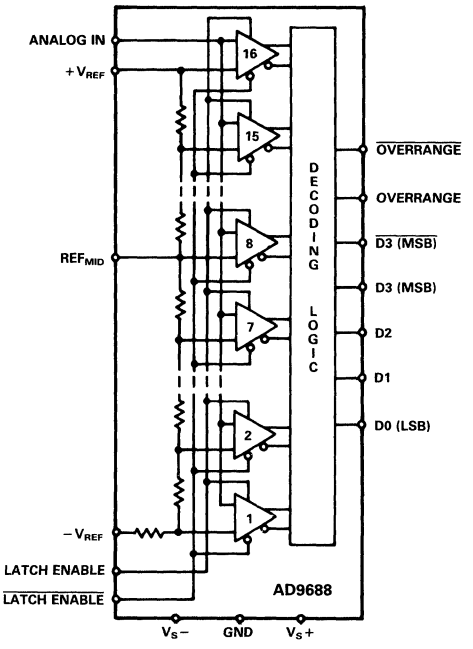
High Speed 4-Bit Monolithic ADC

AD9688

FEATURES
200MSPS Encode Rate
7-Bit Differential Linearity
Bipolar Input Range
Wide Input Range −2.7V to +3.0V

APPLICATIONS
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Radar Guidance Digitizers
Smart Munitions

AD9688 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9688 is a 4-bit, high speed, analog-to-digital converter with ECL compatible outputs. The AD9688 is a pin compatible alternate source for the AM6688. The AD9688 is fabricated in a high-performance, bipolar process which allows full Nyquist operation up to 200MSPS encode rates.

The AD9688 provides 7-bit linearity (0.0625LSB for a 4-bit device) which, when combined with the wide input range, allows several AD9688s to be stacked for higher resolutions. Stacking is aided by the overrange output terminals which can be used to drive decoding logic.

The sixteen high speed input comparators will track input signals up to 200MHz. The comparator sampling is controlled by the differential Latch Enable input. The Latch Enable is designed to be driven by 10K or 100K ECL logic families. The outputs of the AD9688 are open emitter terminals (10K and 10KH compatible) requiring pull-down resistors.

The AD9688 is offered as both an industrial temperature range device −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both versions are available packaged in an 18-pin ceramic DIP. The extended temperature range device is also available in a ceramic LCC package.

ORDERING INFORMATION

Device	Linearity	Temperature Range	Description	Package Options*
AD9688BQ	0.125LSB	−25°C to +85°C	18-Pin Cerdip, Industrial	Q-18
AD9688TE	0.125LSB	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD9688TQ	0.125LSB	−55°C to +125°C	18-Pin Cerdip, Extended Temperature	Q-18

*See Section 14 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±7V
Analog-to-Digital Ground Voltage Differential 0.5V
Analog Input Voltages
(V_{IN}, $+V_{REF}$, V_{REF}, REF_{MID})[2] . . . . . −4.0 to 4.0V
Differential Reference Voltage ($+V_{REF}$ to $-V_{REF}$)[3] . . . 7.0V
Reference Midpoint Current . . . . . ±4mA
LATCH ENABLE Input Voltages . . . . . −5.2V to 0V
Differential LATCH ENABLE Voltage 5.2V
Digital Output Current 20mA
Power Dissipation (+25°C Free Air)[4] 1.3W
Operating Temperature Range
AD9688BQ . . . . . −25°C to +85°C
AD9688TE/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS

(Supply Voltages = −5.2V and +5.0V, Differential Reference Voltage = 2.56V, unless otherwise stated)

Parameter	Temp	AD9688BQ Min	AD9688BQ Typ	AD9688BQ Max	AD9688TE/TQ Min	AD9688TE/TQ Typ	AD9688TE/TQ Max	Units
RESOLUTION		4			4			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.04	0.0625		0.04	0.0625	LSB
	Full			0.125			0.125	LSB
Integral Linearity	+25°C		0.055	0.0625		0.055	0.0625	LSB
	Full			0.0625			0.0625	LSB
Transition Error Voltage	Full			10			10	mV
No Missing Codes	Full		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR								
Top of Reference Ladder	+25°C		13.0	20.0		13.0	20.0	mV
	Full			25.0			25.0	mV
Bottom of Reference Ladder	+25°C		5.0	10.0		5.0	10.0	mV
	Full			15.0			15.0	mV
Offset Drift Coefficient	Full		30			30		µV/°C
ANALOG INPUT								
Input Voltage Range	Full		−2.7, +3.3			−2.7, +3.3		V
Input Bias Current[5]	+25°C		125	175		125	175	µA
	Full			230			230	µA
Input Resistance	+25°C		40			40		kΩ
Input Capacitance	+25°C		10.3	13.0		10.3	13.0	pF
Full Power Bandwidth[6]	+25°C		100			100		MHz
REFERENCE INPUT[2,3]								
Reference Ladder Resistance	+25°C	280	350	420	280	350	420	Ω
Ladder Temperature Coefficient	Full		0.75			0.75		Ω/°C
Reference Input Bandwidth	+25°C		20			20		MHz
DYNAMIC PERFORMANCE[7]								
Conversion Rate	+25°C	175	200		175	200		MHz
Conversion Time	+25°C		5.0	5.7		5.0	5.7	ns
Minimum Output Hold Time (t_{OH})[8]	+25°C	3.0	3.9		3.0	3.9		ns
Output Delay (t_{PD})[9]	+25°C		6.0	6.5		6.0	6.5	ns
Analog Hold Time (t_H)	+25°C		0.8			0.8		ns
Analog Setup Time (t_S)	+25°C		1.5			1.5		ns
Transient Response[10]	+25°C		3.7			3.7		ns
Overvoltage Recovery Time[11]	+25°C		3.9			3.9		ns
Rise Time	+25°C		2.2	3.0		2.2	3.0	ns
Fall Time	+25°C		2.0	3.0		2.0	3.0	ns
Output Time Skew[12]	+25°C		0.6			0.6		ns
Dynamic Linearity	+25°C		0.1			0.1		LSB

Parameter	Temp	AD9688BQ Min	AD9688BQ Typ	AD9688BQ Max	AD9688TE/TQ Min	AD9688TE/TQ Typ	AD9688TE/TQ Max	Units
LATCH ENABLE INPUT[13]								
Logic "1" Voltage	Full			−1.1			−1.1	V
Logic "0" Voltage	Full	−1.5			−1.5			V
Logic "1" Current	Full			75			75	μA
Logic "0" Current	Full			2			2	μA
Input Capacitance	+25°C		3.5	4.0		3.5	4.0	pF
Latch Enable Pulse Width (LATCHED)	+25°C	3.5	2.8		3.5	2.8		ns
Latch Enable Pulse Width (SAMPLED)	+25°C	2.2	1.3		2.2	1.3		ns
DIGITAL OUTPUTS[7]								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
POWER SUPPLY[14]								
Positive Supply Current (+5.0V)	+25°C		65	70		65	70	mA
	Full			75			75	mA
Negative Supply Current (−5.2V)	+25°C		71	80		71	80	mA
	Full			85			85	mA
Nominal Power Dissipation	+25°C		694			694		mW
Reference Ladder Dissipation	+25°C		19			19		mW
Power Supply Rejection Ratio[15]	+25°C		6.5	10		6.5	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

[2]Under normal operating conditions, the analog input voltages should not exceed −3.3V to +2.7V.

[3]Under normal operating conditions, the differential reference voltage may range from 0.16V to 6.0V; $+V_{REF} \geq -V_{REF}$.

[4]Typical thermal impedance . . .

18-Pin Ceramic $\theta_{JA} = 75°C/W; \theta_{JC} = 19°C/W$

20-Pin LCC $\theta_{JA} = 80°C/W; \theta_{JC} = 23°C/W$

[5]Sample mode with $A_{IN} = +V_{REF}$.

[6]Determined by no missing codes in the reconstructed output.

[7]Outputs terminated with 100Ω resistors to −2.0V.

[8]Previous output data will remain valid for specified time after the leading edge of the LATCH ENABLE.

[9]Measured from trailing edge of LATCH ENABLE pulse to data out.

[10]For full-scale step input, 6-bit accuracy is attained in specified time.

[11]Recovers to 6-bit accuracy in specified time, after 150% full-scale input overvoltage.

[12]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit skew differences.

[13]LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ are differential inputs which must be driven concurrently. ECL inputs within the specified ranges are guaranteed to produce normal switching.

[14]Supply voltages should remain stable within ±5% for normal operation.

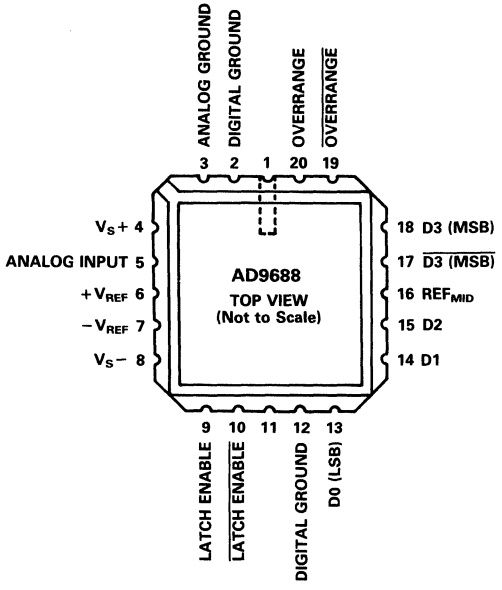
[15]Measured at +5.0V ±5% and −5.2V ±5%.

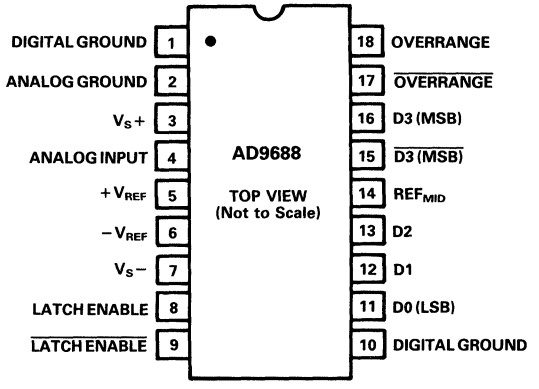
Specifications subject to change without notice.

FUNCTIONAL DESCRIPTION

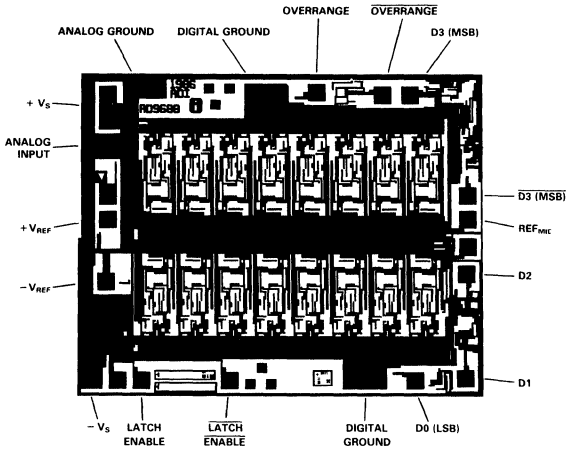
PIN NAME	DESCRIPTION
DIGITAL GROUND	– One of two digital ground returns. All grounds should be connected together near the AD9688.
ANALOG GROUND	– Analog ground return. All grounds should be connected together near the AD9688.
V_S+	– Positive supply terminal, nominally +5.0V.
ANALOG INPUT	– Analog input terminal.
$+V_{REF}$	– Most positive reference voltage for the internal resistor ladder.
$-V_{REF}$	– Most negative reference voltage for the internal resistor ladder.
V_S-	– Negative supply terminal, nominally −5.2V.
LATCH ENABLE	– Noninverting input of differential latch enable input. In the "latch" mode, logic HIGH, the output data reflects the analog input level just prior to the "latched" state. In the "sample" mode, logic LOW, the output data will attempt to track the analog input. The LATCH ENABLE must be driven in conjunction with the $\overline{\text{LATCH ENABLE}}$ input.
$\overline{\text{LATCH ENABLE}}$	– Inverting input of differential latch enable input. In the "latch" mode, logic LOW, the output data reflects the analog input level just prior to the "latched" state. In the "sample" mode logic HIGH, the output data will attempt to track the analog input. The $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with the LATCH ENABLE input.
DIGITAL GROUND	– One of two digital ground returns. All grounds should be connected together near the AD9688.
D0 (LSB)	– One of four digital outputs. D0 (LSB) is the least significant bit of the digital output word.
D1	– One of four digital outputs.
D2	– One of four digital outputs.
REF_{MID}	– The midpoint tap on the internal reference ladder.
$\overline{\text{D3 (MSB)}}$	– One of four digital outputs. $\overline{\text{D3 (MSB)}}$ is the inverted, most significant bit of the digital output word.
D3 (MSB)	– One of four digital outputs. D3 (MSB) is the most significant bit of the digital output word.
$\overline{\text{OVERRANGE}}$	– Inverted overrange data output. Logic LOW indicates an input voltage overrange ($V_{IN} > +V_{REF}$). All other digital outputs return to zero (logic LOW) during overrange conditions.
OVERRANGE	– Overrange data output. Logic HIGH indicates an input voltage overrange ($V_{IN} > +V_{REF}$). All other digital outputs return to zero (logic LOW) during overrange conditions.

PIN CONFIGURATIONS



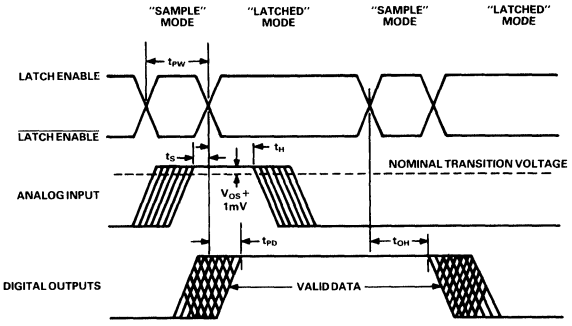


DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	118.5 × 96 × 16 (± 2) mils
Pad Dimensions	4 × 4 mils
Metalization	
1st Level	Copper-Aluminum Alloy
2nd Level	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold; Gold Ball Bonding

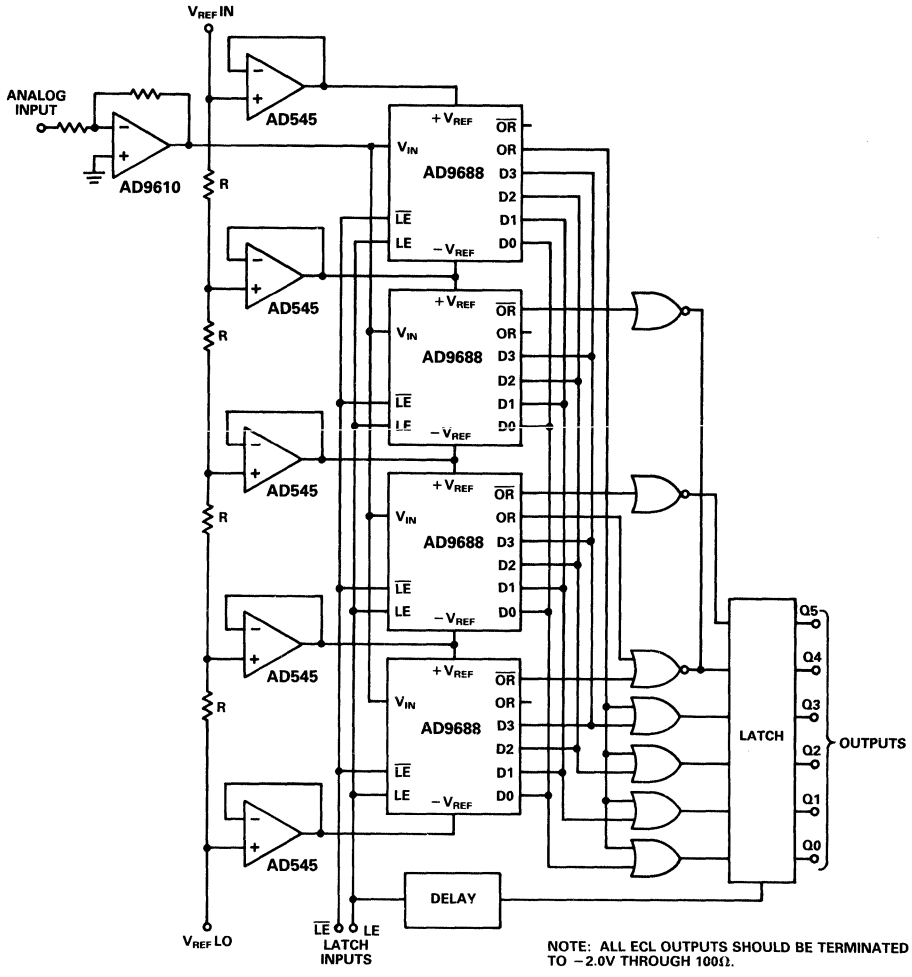
SYSTEM TIMING DIAGRAM



t_{PW}	– Minimum Sample Pulse Width
t_S	– Minimum Setup Time
t_H	– Minimum Hold Time
t_{PD}	– Maximum Output Propagation Delay
t_{OH}	– Minimum Output Hold Time
V_{OS}	– Offset Voltage

NOTE: Comparator outputs are unlatched during "sampling" period. The output may become invalid during this interval as it attempts to track the input signal.

TYPICAL APPLICATION



GENERAL INFORMATION

The AD9688 is a high speed device. The 200MSPS encode rate and analog input frequencies which can reach 200MHz, demand careful layout practice typical of high speed circuit design. One of the most important aspects of any AD9688 design is an effective low impedance ground plane. Special attention should be paid to the actual AD9688 ground connections, particularly if sockets must be used.

The internal reference ladder should be properly biased with some form of low-impedance driving source. This becomes especially important if several AD9688s are stacked for higher resolution. Special transfer functions can be realized when several AD9688s are stacked and the resistor tap point voltages are skewed to approximate the desired response curve.

The AD9688 LATCH ENABLE inputs are differential and must be driven with complementary latch signals. Output stability in the "sampling" mode can be adversely affected by LATCH ENABLE signal quality and precision. The effects of a poor quality waveform can be partially compensated for by adjusting either the average signal value or overall waveform duty cycle.

Best performance will be achieved through the use of proper ECL terminations. The open-emitter outputs of the AD9688 are designed to be terminated through 100Ω resistors to −2.0V. If high speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.

ANALOG DEVICES

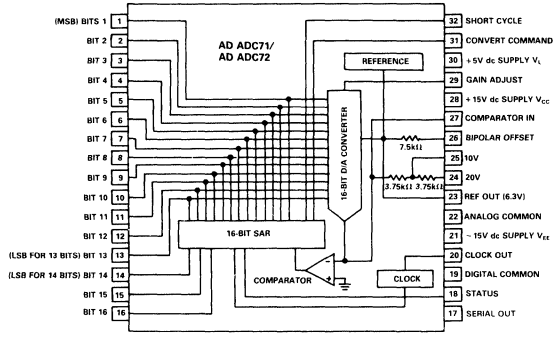
Complete, High Resolution 16-Bit A/D Converters

AD ADC71/AD ADC72

FEATURES

Complete 16-Bit Converter With Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits
Fast Conversion – 35μs (14 Bit)
Short Cycle Capability
Parallel and Serial Logic Outputs
Low Power: 645mW Typical
Industry Standard Pin Out

AD ADC71/AD ADC72 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC71 and AD ADC72 are high resolution 16-bit hybrid IC analog-to-digital converters including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin hermetic ceramic DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR (AD ADC71K, AD ADC72K and B), and maximum conversion time of 50μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD ADC71 and AD ADC72 provide data in parallel form with corresponding clock and status outputs. The AD ADC71 also provides data in serial form. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD ADC71 and AD ADC72 are excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

PRODUCT HIGHLIGHTS

1. The AD ADC71 and AD ADC72 provide 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J and A grades) at 25°C.
2. Conversion time is 35μs typical to 14 bits with short cycle capability.
3. Two binary codes are available on the AD ADC71 and AD ADC72 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 volts unless otherwise noted)

Model	AD ADC71JD/KD	AD ADC72JD/KD	AD ADC72AD/BD	Units
RESOLUTION	16 (max)	*	*	Bits
ANALOG INPUTS				
Voltage Ranges				
Bipolar	±2.5, ±5, ±10	*	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	*	Volts
Impedance (Direct Input)				
0 to +5V, ±2.5V	1.88	*	*	kΩ
0 to +10V, ±5.0V	3.75	*	*	kΩ
0 to +20V, ±10V	7.50	*	*	kΩ
DIGITAL INPUTS[1]				
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion			
Logic Loading	1 (max)	*	*	LSTTL Load
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error	±0.1[2] (±0.2 max)	*	*	%
Offset Error				
Unipolar	±0.05[2] (±0.1 max)	*	*	% of FSR[3]
Bipolar	±0.1[2] (±0.2 max)	*	*	% of FSR
Linearity Error (max)	±0.006 (J)	±0.006 (J)	±0.006 (A)	% of FSR
	±0.003 (K)	±0.003 (K)	±0.003 (B)	% of FSR
Inherent Quantization Error	±1/2	*	*	LSB
Differential Linearity Error	±0.003	*	*	% of FSR
No Missing Codes @ 25°C[4]	To 14 Bits (K Grade)	*	To 14 Bits (B Grade)	Guaranteed
POWER SUPPLY SENSITIVITY				
±15V dc	0.003	*	*	% of FSR/% ΔV_S
+5V dc	0.001	*	*	% of FSR/% ΔV_S
CONVERSION TIME[5] (14 BITS)	35 (50 max)	*	*	µs
WARM-UP TIME	5 (min)	*	*	Minutes
DRIFT				
Gain	±15 (max)	±10 (±20 max)	+7 (±15 max)	ppm/°C
Offset				
Unipolar	±2 (±4 max)	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±8 (±10 max)	±5 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±1.5 (2 max)	±1.0 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code				
Temperature Range[4]				
71JD, 72JD, 72AD (13 Bits)	0 to 70	*	*	°C
71KD, 72KD, 72BD (14 Bits)				
DIGITAL OUTPUT[1]				
(All Codes Complementary)				
Parallel and Serial				
Output Codes[6]				
Unipolar	CSB	*	*	
Bipolar	COB, CTC[7]	*	*	
Output Drive	5	*	*	LSTTL Loads
Status	Logic "1" During Conversion			
Status Output Drive	5 (max)	*	*	LSTTL Loads
Internal Clock				
Clock Output Drive	5 (max)	*	*	LSTTL Loads
Frequency	400	*	*	kHz
INTERNAL REFERENCE VOLTAGE	6.3	*	*	V dc
Error	±5 max	*	*	%
Max External Current Drain				
With no Degradation of Specs	±200 max	*	*	µA
Temperature Coefficient	±10 max	*	*	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Consumption	645 (850 max)	*	*	mW
Rated Voltage, Analog	±15 ±0.5 max	*	*	V dc
Rated Voltage, Digital	+5 ±0.25 max	*	*	V dc
Supply Drain +15V dc	+16	*	*	mA
Supply Drain −15V dc	−21	*	*	mA
Supply Drain +5V dc	+18	*	*	mA
TEMPERATURE RANGE				
Specification	0 to +70	*	−25 to +85	°C
Operating (Derated Specs)	−25 to +85	*	−25 to +125	°C
Storage	−55 to +125	*	*	°C

NOTES
[1] Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
[2] Adjustable to zero.
[3] Full Scale Range.
[4] For definition of "No Missing Codes", refer to Theory of Operation.
[5] Conversion time may be shortened with "Short Cycle" set for lower resolution.
[6] CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Two's Complement.
[7] CTC coding obtained by inverting MSB (Pin 1).
*Specifications same as AD ADC71JD, KD.
Specifications subject to change without notice.

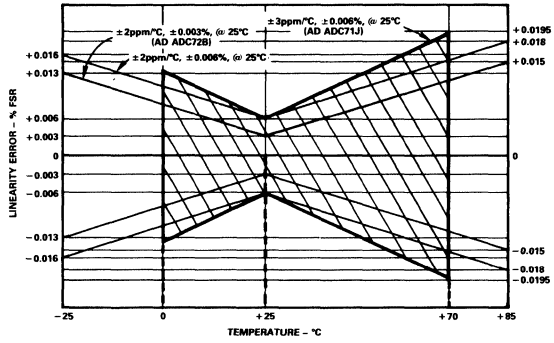


Figure 1. Linearity Error vs. Temperature

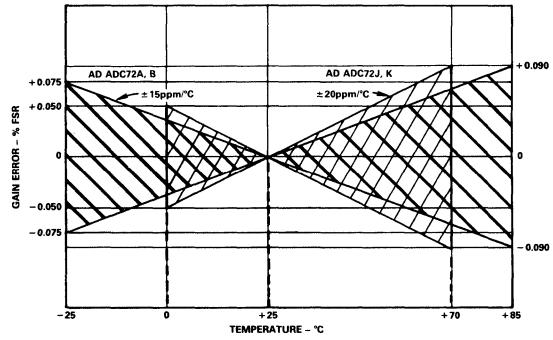


Figure 2. AD ADC72 Gain Drift Error vs. Temperature

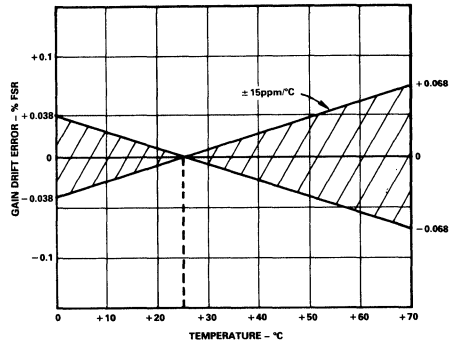


Figure 3. AD ADC71 Gain Drift Error vs. Temperature

ORDERING GUIDE

Model	Linearity Error (Max)	Specification Temp Range	Package Option*
AD ADC71JD	±0.006% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC71KD	±0.003% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72JD	±0.006% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72KD	±0.003% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72AD	±0.006% of FSR	−25°C to +85°C	Ceramic (DH-32E)
AD ADC72BD	±0.003% of FSR	−25°C to +85°C	Ceramic (DH-32E)

*See Section 14 for package outline information.

THEORY OF OPERATION

The analog continuum is partitioned into 2^{16} discrete ranges for 16-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ± 1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.2% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 5 and 6. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC71/AD ADC72 are specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

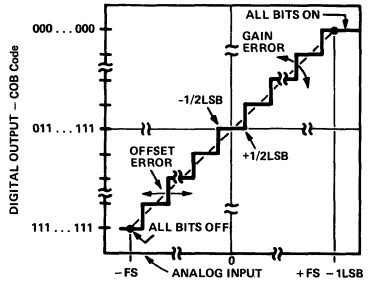


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD ADC71/AD ADC72 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 510kΩ resistor to the gain adjust pin 29 as shown in Figure 5.

If no external trim adjustment is desired, pins 27 (offset adj) and pin 29 (gain adj) may be left open.

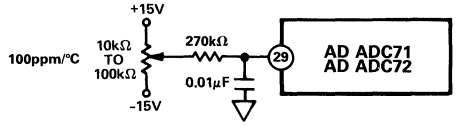


Figure 5. Gain Adjustment Circuit

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 27 for all ranges. As shown in Figure 6, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $32LSB_{14} \times 61ppm/LSB_{14} \times 1200ppm/°C = 2.3ppm/°C$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than $\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

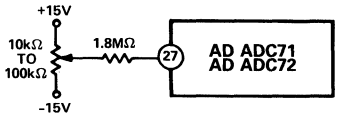


Figure 6. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used, is shown in Figure 7.

In either adjust circuit, the fixed resistor connected to pin 27 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 27 is quite sensitive to external noise pick-up).

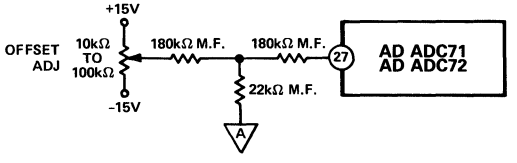


Figure 7. Low Tempco Zero Adjustment Circuit

TIMING

The timing diagram is shown in Figure 8. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

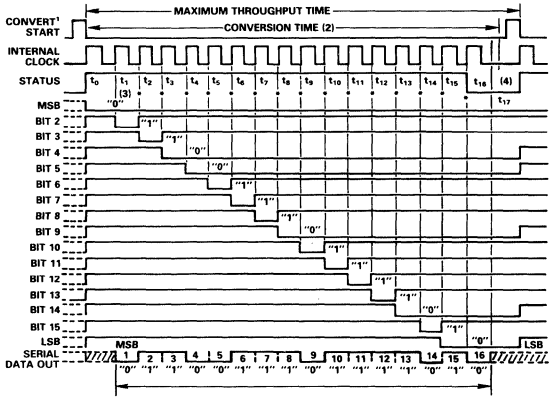


Figure 8. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 9).

Figure 9. LSB Valid to Status Low

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 10. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

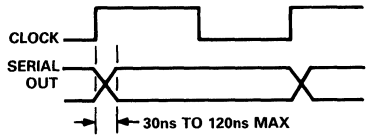


Figure 10. Clock High to Serial Out Valid

Short Cycle Input: A Short Cycle Input, pin 32, permits the timing cycle shown in Figure 8 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, pin 32 is connected to Bit 11 output pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (t_{10} + 40ns in timing diagram of Figure 6). Short cycle connections and associated maximum 8-, 10-, 12-, 13-, 14-, and 15-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 32 to Pin:	Resolution Bits	Resolution (%FSR)	Maximum Conversion Time (μs)	Status Flag Reset
N/C (Open)	16	0.0015	57.0	t_{16} + 40ns
16	15	0.003	53.5	t_{15} + 40ns
15	14	0.006	50.0	t_{14} + 40ns
14	13	0.012	46.5	t_{13} + 40ns
13	12	0.024	42.8	t_{12} + 40ns
11	10	0.100	35.6	t_{10} + 40ns
9	8	0.390	28.5	t_8 + 40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC71 and AD ADC72 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 11 for circuit details.

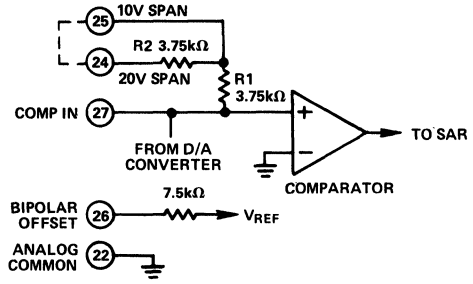


Figure 11. AD ADC71/AD ADC72 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	For Direct Input, Connect Input Signal to
±10V	COB	27	Input Signal	24
±5V	COB	27	Open	25
±2.5V	COB	27	Pin 27	25
0V to +5V	CSB	22	Pin 27	25
0V to +10V	CSB	22	Open	25
0V to +20V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and must be shielded/guarded by analog common.

Table II. AD ADC71/AD ADC72 Input Scaling Connections

Output Code MSB LSB	Range	±10V	±5V	±2.5V	0 to +10V	0 to +5V
000 . . . 000*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0 −1/2LSB	0 −1/2LSB	0 −1/2LSB	+5V −1/2LSB	+2.5V −1/2LSB
111 . . . 110	− Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V +1/2LSB	0V +1/2LSB

*Voltages given are the nominal value for transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	FSR / 2^n	20V / 2^n	10V / 2^n	5V / 2^n	10V / 2^n	5V / 2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n = 13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n = 14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n = 15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Two's Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

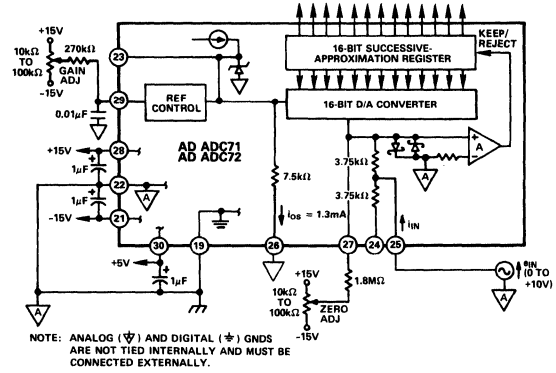


Figure 12. Analog and Power Connections for Unipolar 0 to + 10V Input Range

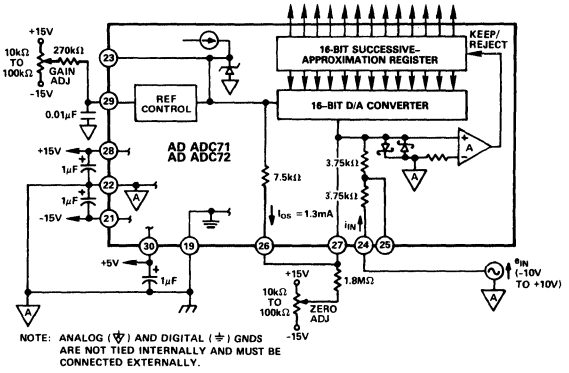


Figure 13. Analog and Power Connections for Bipolar −10V to + 10V Input Range

3

CALIBRATION (14-Bit Resolution Examples)
External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 5 and 6, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to $+1LSB_{14}$ = 0.00061V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2LSB = +9.9987V. Adjust Gain for 00000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

−10V to +10V Range: Set analog input to −9.99878V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

Other Ranges: Representative digital coding for 0 to +10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ± 1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Handbook", D. Sheingold, Analog Devices, Inc., 1986, Part II, Chapter 4.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS
Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (pins 19 and 22) must be tied together at one point for the AD ADC71/AD ADC72 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD ADC71/AD ADC72. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD ADC71/AD ADC72 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC71/AD ADC72's supply terminals should be capacitively decoupled as close to the AD ADC71/AD ADC72s as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

On the ceramic package the metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The AD389 is a companion T/H designed for use with the AD ADC71/AD ADC72 family. The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients, and minimal droop rate.

The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1LSB. The amplitude of 1LSB of the companion A/D converter for a given input range will vary from 610μV for a 14-bit A/D using a 0 to 10V input range to 4.88mV for a 12-bit A/D using a ±10V input range. The hold mode droop rate should produce less than 1LSB of droop in the output during the conversion time of the A/D converter. For 610μV/LSB, as noted in the example above, for a 50μs 14-bit A/D converter, the maximum droop rate will be 610μV/50μs or 12μV/μs during the 50μs conversion period.

Minimal thermal tail effects are another requirement of high resolution applications. The self-heating errors induced by the changing current levels in the output stages of T/H amps may cause more than 1LSB of error due to thermal tail effects.

The linearity error should be less than 1LSB over the transfer function, as set by the resolution of the A/D converter. The T/H acquisition time, T/H settling time along, with the conversion time of the A/D converter determines the highest sampling rate. This in turn will determine the highest input signal frequency that can be sampled at twice a cycle.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, with an ideal brickwall low pass filter placed in the signal path prior to the AD389 and A/D converter to eliminate aliasing.

The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible as with the feedthrough spec. The temperature coefficients for drift should be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more above +70°C (+158°F). For commercial and industrial users, these shifts will only appear above the highest temperatures their equipment will ever expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment. Thus, the AD ADC71 or AD ADC72 used with a companion AD389T/H offers high accuracy sampling in high precision applications.

Spec	14 Bit	AD389KD	Units
Aperture Jitter (max)	2.4	0.4	ns
Slew Rate (max w/20V pk-pk signal)	1.26	30	V/μs
Feedthrough (1LSB max)	−84.3	−86	dB
Droop Rate (1LSB max in 15μs)	40.7	0.1	μV/μs
Droop Rate (1LSB max in 50μs)	12.2	0.1	μV/μs
Acquisition Time (to ±1LSB max) for 20kHz Signal w/15μs ADC	10	3-5	μs
Pedestal Shift (max) with Input Signal	−84.3	−86	dB
Gain Temperature Coefficient (max) for ±10°C Ambient Operation	6.1	2.0	ppm/°C
Thermal Tail (max) within 50μs after Hold	1.2	0.1	mV
Linearity Error (max)	±0.0061	0.003	%FSR

Table V. T/H Amplifier Requirements vs. AD389 Specs

AD389 in Combination With an	Maximum Throughput Rate	Maximum Nyquist Input Frequency Range
AD ADC71 (13 bit)	22.2kHz	dc to 11.1kHz
AD ADC72 (14 bit)	16.7kHz	dc to 8.3kHz

Table VI. T/H & ADC Combinations and Maximum Throughput Rate

Using the AD ADC71/AD ADC72 at Slower Conversion Times

The user may wish to run the AD ADC71/AD ADC72 at slower conversion times in order to synchronize the A/D with an external clock. This is accomplished by running a slower clock than the internal clock into the START CONVERT input. This clock must consist of narrow negative-going clock pulses, as seen in Figure 14. The pulse must be a minimum of 100ns wide but not greater than 700ns. Having a raising edge immediately after a falling edge inhibits the internal clock pulse. This enables the AD ADC71/AD ADC72 to function normally and complete a conversion after 16 clock pulses and serial out in 17 clock pulses. The STATUS command will function normally and switch high after the first clock pulse and will fall low after the 17th clock pulse. In this way an external clock can be used to control the AD ADC71/AD ADC72 at slower conversion times.

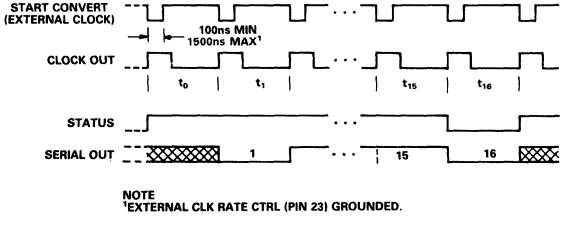


Figure 14. Timing Diagram for Use with an External Clock

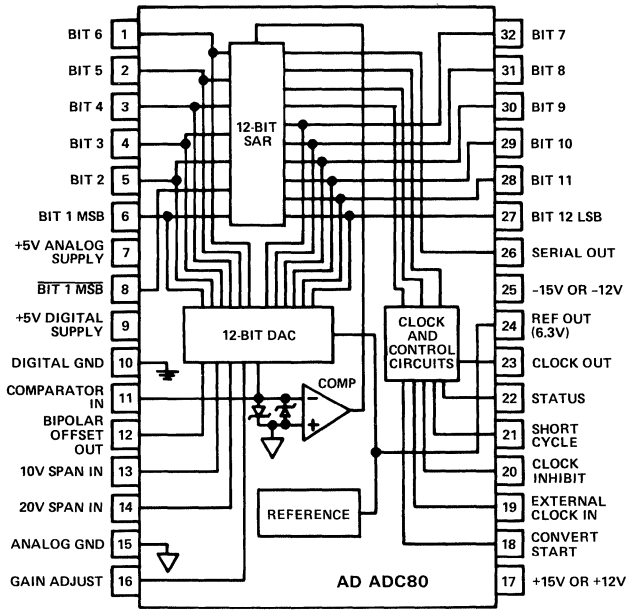
12-Bit Successive Approximation Integrated Circuit A/D Converter

AD ADC80

FEATURES

- True 12-Bit Operation: Max Nonlinearity ±0.012%
- Low Gain T.C.: ±30ppm/°C max
- Low Power: 800mW
- Fast Conversion Time: 25μs
- Precision 6.3V Reference for External Application
- Short-Cycle Capability
- Serial or Parallel Data Outputs
- Monolithic DAC with Scaling Resistors for Stability
- Low Chip Count—High Reliability
- Industry Standard Pinout
- "Z" Models for ±12V Supplies

AD ADC80 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC80 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC80 include a maximum linearity error at +25°C of ±0.012%, max gain T.C. of 30ppm/°C, typical power dissipation of 800mW and max conversion time of 25μs. Monotonic operation of the feedback D/A converter guarantees no missing codes over the temperature range of -25°C to +85°C.

The design of the AD ADC80 includes scaling resistors that provide analog signal ranges of ±2.5, ±5.0, ±10, 0 to +5 or 0 to +10 volts. The 6.3V precision reference may be used for external applications. All digital signals are fully DTL and TTL compatible; output data may be read in both serial and parallel form.

The AD ADC80 is available in two performance grades, the AD ADC80-12 (0.012% of FSR max) and the AD ADC80-10 (0.048% of FSR max). Both grades are specified for use over the -25°C to +85°C temperature range and both are available in a 32-pin ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD ADC80 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The internal buried zener reference is laser trimmed to 6.3 volts. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset current.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The AD ADC80 directly replaces other devices of this type with significant increases in performance.
6. The fast conversion rate of the AD ADC80 makes it an excellent choice for applications requiring high system throughput rates.
7. The short cycle and external clock options are provided for applications requiring faster conversion speeds or lower resolutions.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise specified)

MODEL	AD ADC80-12	AD ADC80-10
RESOLUTION	12 Bits	10 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5V, ±5V, ±10V	
Unipolar	0V to +5V, 0V to +10V	
Impedance (Direct Input)		
0V to +5V, ±2.5V	2.5kΩ	*
0V to +10V, ±5V	5kΩ	*
±10V	10kΩ	*
DIGITAL INPUTS[1]		
Convert Command	Positive Pulse 100ns Wide (min) ("0" to "1" Initiates Conversion)	
Logic Loading	1TTL Load	
External Clock	1TTL Load	
TRANSFER CHARACTERISTICS ERROR		
Gain Error[2]	±0.1% of FSR[3]	*
Offset Error[2]		
Unipolar	±0.05% of FSR	*
Bipolar	±0.1% of FSR	*
Linearity Error (max)[4]	±0.012% of FSR	±0.048% of FSR
Inherent Quantization Error	±1/2LSB	*
Differential Linearity Error	±1/2LSB	*
No Missing Codes Temperature Range	-25°C to +85°C	*
Power Supply Sensitivity		
±15V	±0.0030% of FSR/% V_S	*
+5V	±0.0015% of FSR/% V_S	*
DRIFT		
Specification Temperature Range	-25°C to +85°C	*
Gain (max)	±30ppm/°C	*
Offset		
Unipolar	±3ppm of FSR/°C	*
Bipolar (max)	±15ppm of FSR/°C	*
Linearity (max)	±3ppm of FSR/°C	*
Monotonicity	GUARANTEED	*
CONVERSION SPEED[5]	22μs typ, 25μs max	21μs max
DIGITAL OUTPUT		
(all codes complementary)		
Parallel		
Output Codes[6]		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	2TTL Loads	
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Status Output Drive	2TTL Loads	
Internal Clock		
Clock Output Drive	2TTL Loads	
Frequency[7]	575kHz	
INTERNAL REFERENCE VOLTAGE	6.3V ±10mV	
Max. External Current (with no degradation of specifications)	1.5mA	
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max	
POWER REQUIREMENTS		
Rated Voltages	±15V, +5V	
Range for Rated Accuracy	4.75V to 5.25V and ±14.0V to ±16.0V	
Z Models[8]	4.75V to 5.25V and ±11.4V to ±16.0V	
Supply Drain +15V	+10mA	
-15V	-20mA	
+5V	+70mA	
TEMPERATURE RANGE		
Specification	-25°C to +85°C	
Operating (Derated Specs)	-55°C to +100°C	
Storage	-55°C to +125°C	
PACKAGE OPTION[9]		
DH-32D	AD ADC80-12	AD ADC80-10

NOTES
[1] DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital inputs, Logic "0" = +0.4V max and "1" = 2.4V min digital outputs.
[2] Adjustable to zero with external trimpots.
[3] FSR means Full Scale Range– for example, unit connected for ±10V range has 20V FSR.
[4] Error shown is the same as ±1/2LSB max for resolution of A/D converter.
[5] Conversion time with internal clock.
[6] See Table 1. CSB – Complementary Straight Binary
COB – Complementary Offset Binary
CTC – Complementary Two's Complement
[7] For conversion speeds specified.
[8] For Z models order AD ADC80Z-12 or AD ADC80Z-10.
[9] See Section 14 for package outline information.

*Specifications same as AD ADC80-12.

Specifications subject to change without notice.

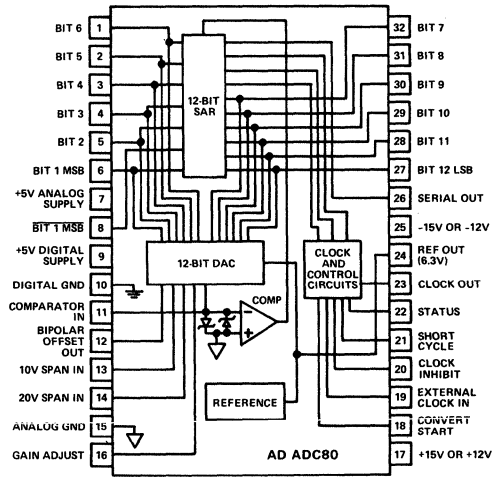


Figure 1. AD ADC80 Functional Diagram and Pinout

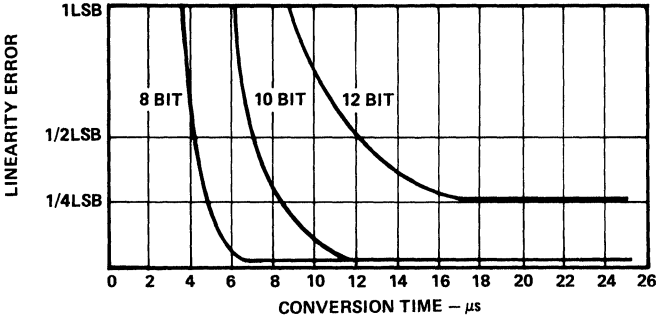


Figure 2. Linearity Error vs. Conversion Time (Normalized)

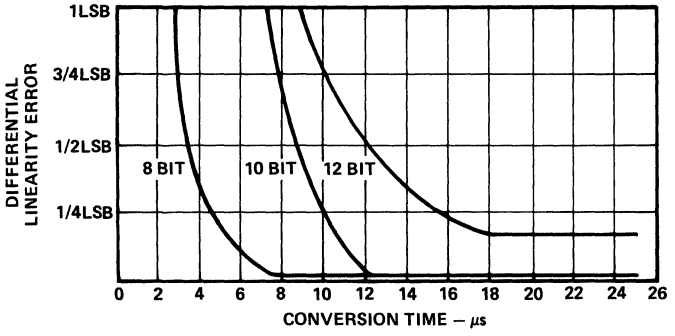


Figure 3. Differential Linearity Error vs. Conversion Time (Normalized)

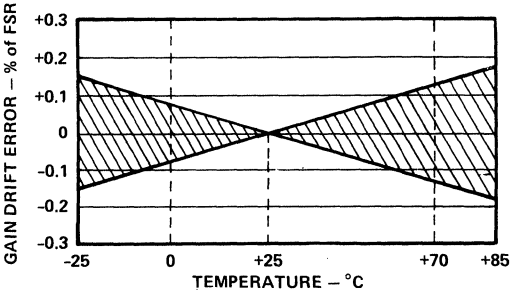


Figure 4. Maximum Gain Drift Error – % of FSR vs. Temperature

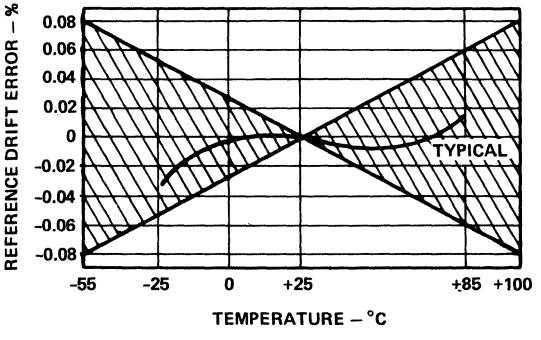


Figure 5. Reference Drift – % Error vs. Temperature

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the AD ADC80 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 7 and 9. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 6).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC80 is specified as having no missing codes over the entire temperature range from -25°C to +85°C.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

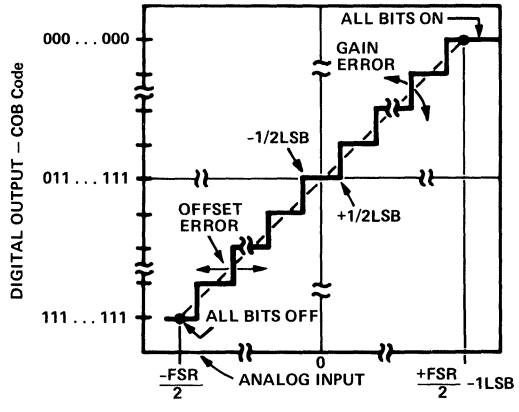


Figure 6. Transfer Characteristic for an Ideal Bipolar A/D

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 11 for all ranges. As shown in Figure 7 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

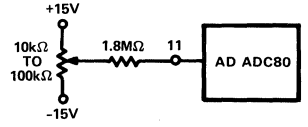


Figure 7. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 8.

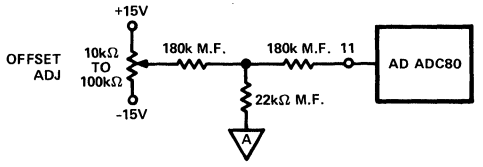


Figure 8. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 11 should be located close to this pin to keep the pin 11 connection runs short (Comparator Input pin 11 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 16 as shown in Figure 9.

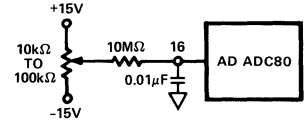


Figure 9. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 10.

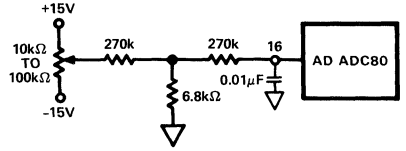


Figure 10. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

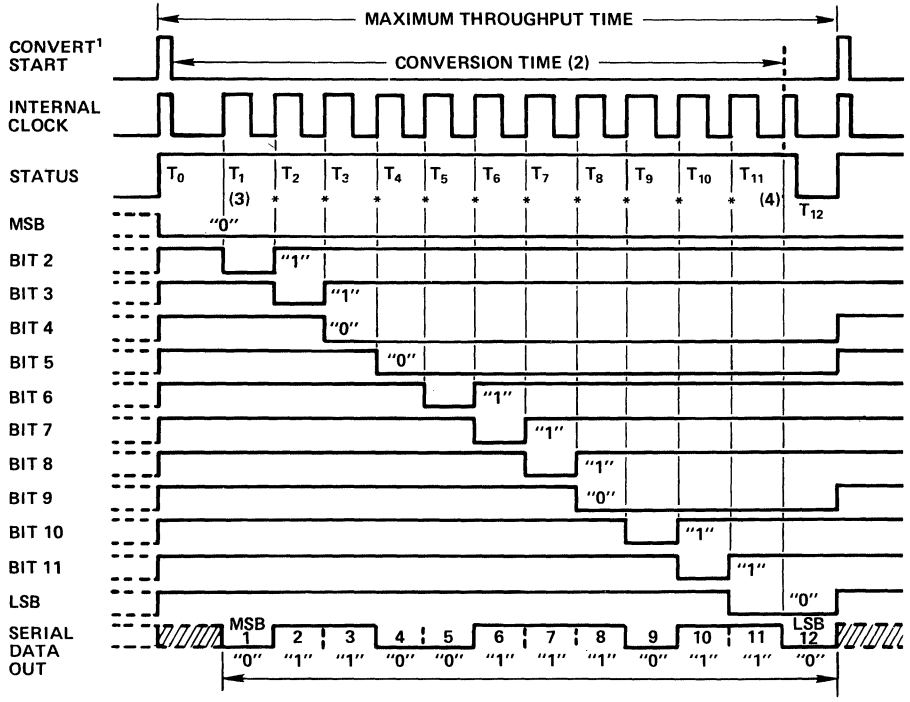
On receipt of a CONVERT START command, the AD ADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 11. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2-B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 11).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "RISING EDGE" OF THE CONVERT COMMAND.
2. 25μs FOR 12 BITS AND 21μs FOR 10 BITS (MAX).
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 11. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 6) or its logical inverse BIT 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 11. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 11. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 21, permits the timing cycle shown in Figure 11 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 10-bit resolution is desired, pin 21 is connected to Bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 11). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I. When 12-bit resolution is required, pin 21 is connected to +5V (pin 9).

Connect Short Cycle Pin 21 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t_{12} +40ns
28	10	0.100	21	t_{10} +40ns
30	8	0.390	17	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 12 for circuit details.

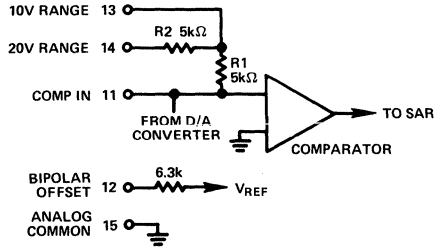


Figure 12. AD ADC80 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0V to +5V	CSB	15	Pin 11	13
0V to +10V	CSB	15	Open	13

Table II. AD ADC80 Input Scaling Connections

Binary (BIN) Output		INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definitions

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC80. Therefore, separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point and the two device grounds should be tied together. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC80's supply terminals should be capacitively decoupled as close to the AD ADC80 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

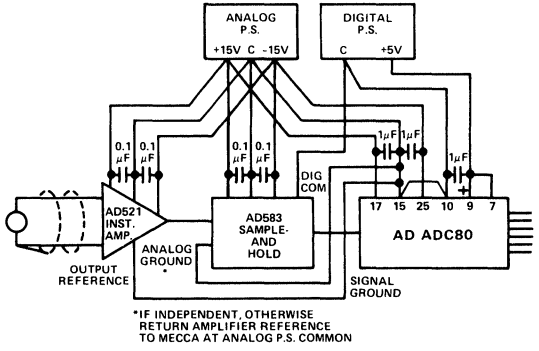


Figure 13. Basic Grounding Practice

CONTROL MODES

The timing sequence of the AD ADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figures 14–16.

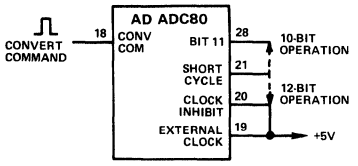


Figure 14. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

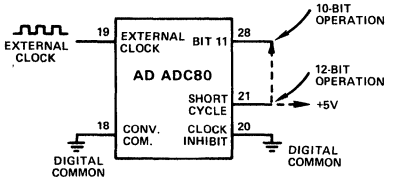


Figure 15. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock Runs Continuously.

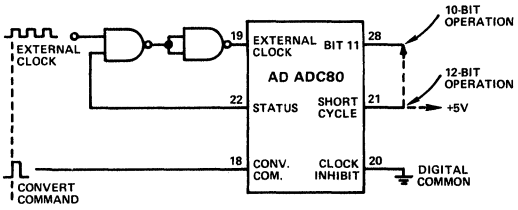


Figure 16. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command must be Synchronized with Clock.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 17 and 18, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, -2.5V to +2.5V and -5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

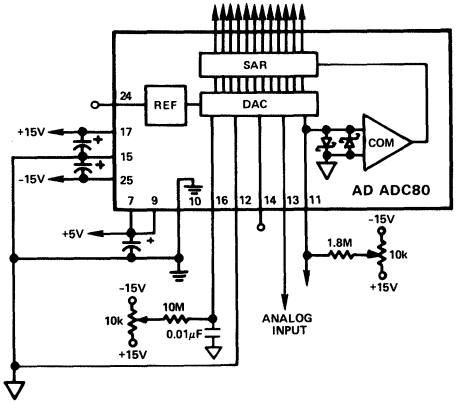


Figure 17. Analog and Power Connections for Unipolar 0-10V Input Range

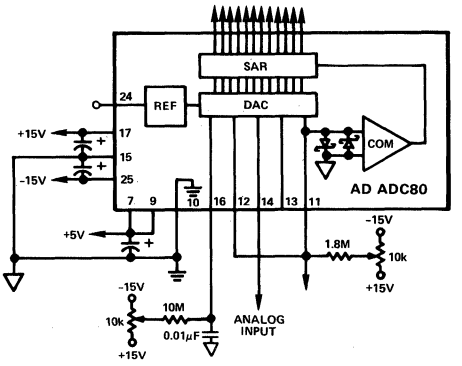


Figure 18. Analog and Power Connections for Bipolar ±10V Input Range

MULTICHANNEL CONVERSION

In multichannel conversion systems, elements of the acquisition chain may be shared by two or more input sources. This sharing may occur in a number of ways, depending on the desired properties of the multiplexed system.

The data acquisition system shown in Figure 19 is a low cost solution to digitizing data from many analog channels. For most efficient use of time, the multiplexer is acquiring the next channel to be converted while the sample-hold is holding the previous output level for conversion. When conversion is complete, the status line from the converter causes the S/H to return to the sample mode and acquire the new data. After the acquisition time is completed, the sample hold can be switched to hold. A conversion can then begin and the multiplexer can be switched to the next channel.

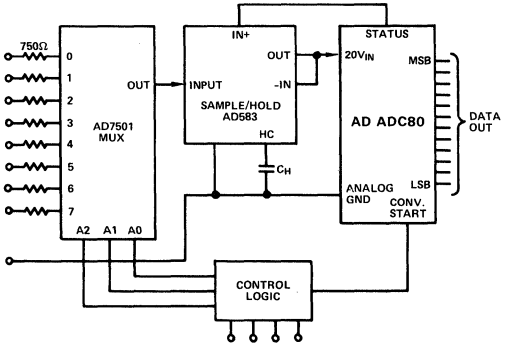


Figure 19. Data Acquisition System

ANALOG DEVICES

Fast, Complete 12-Bit A/D Converters

AD ADC84/AD ADC85/AD5240

FEATURES

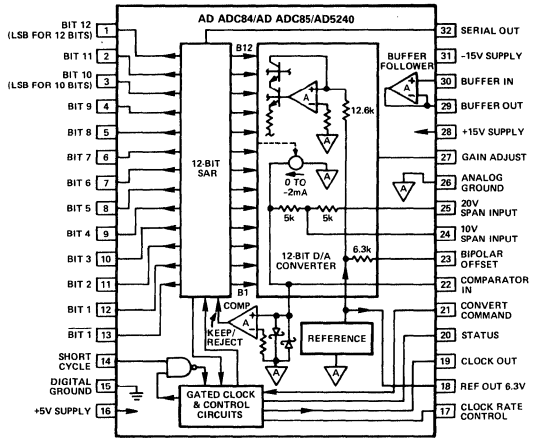
Performance

- Complete 12-Bit A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion: 10μs or 5μs
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
- Max Nonlinearity: <±0.012%
- Low Power: 880mW Typical
- Low Chip Count – High Reliability
- Industry Standard Pin Out
- "Z" Models for ±12V Operation Available
- MIL-STD-883B Processing Available

Versatility

- Negative-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +6.3V Reference for External Applications

AD ADC84/AD ADC85/AD5240
FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC84/AD ADC85/AD5240 series devices are high-speed, low-cost 10- and 12-bit successive approximation analog-to-digital converters that include internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC84/AD ADC85/AD5240 series include a maximum linearity error at +25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 880mW, and conversion time of less than 10μs for the 12-bit versions. Of considerable significance in severe and aerospace applications is the guaranteed performance from -55°C to +125°C of the AD ADC85S which is also available with environmental screening. Monotonic operation of the feedback D/A converter guarantees no missing codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD ADC84/AD ADC85/AD5240 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +6.3V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is negative-true and available in either serial or parallel form.

The AD ADC84/AD ADC85/AD5240 series devices are available in two different performance grades. The devices are specified for either 10-bit accuracy (±0.048% FSR max) or 12-bit accuracy (±0.012% FSR max) with 8.4μs, 10μs (AD ADC84/AD ADC85) and 4.1μs, 5μs (AD5240) max conversion times respectively.

The AD ADC84 and AD ADC85C specified for operation over the 0 to +70°C temperature range. The AD ADC85 and AD ADC85S are specified for the -25°C to +85°C, -55°C to +125°C ranges respectively.

PRODUCT HIGHLIGHTS

1. The AD ADC84/AD ADC85/AD5240 series devices are complete 12-bit A/D converters. No external components are required to perform a conversion.
2. The AD ADC84/AD ADC85/AD5240 directly replaces other devices of this type with significant increases in performance.
3. The fast conversion rates of the AD ADC84/AD ADC85 (10μs) and AD5240 (5μs) make them an excellent choice for applications requiring high system throughput rates.
4. The internal buried zener reference is laser trimmed to 6.3V ±0.1% and ±10ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
5. The integrated package construction provides high quality and reliability with small size and weight.
6. The monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
7. The AD ADC85S/883B and AD524BD/883B come processed to MIL-STD-883, Class B requirements (see ADI Military Products Databook).

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD ADC84	AD ADC85C	AD ADC85	AD ADC85S	AD5249KD/ AD5240BD	UNITS
RESOLUTION	10/12	10/12	10/12	10/12	12	Bits
ANALOG INPUTS						
Voltage Ranges						
Bipolar	±2.5, ±5, ±10	*	*	*	*	Volts
Unipolar	0 to +5, 0 to +10	*	*	*	*	Volts
Impedance (Direct Input)						
0V to +5V, ±2.5V	2.5(±20%)	*	*	*	*	kΩ
0V to +10V, ±5V	5(±20%)	*	*	*	*	kΩ
±10V	10(±20%)	*	*	*	*	kΩ
Buffer Amplifier[1]						
Impedance (min)	100	*	*	*	*	MΩ
Bias Current	50	*	*	*	*	nA
Settling Time						
To 0.01% for 20V Step	2	*	*	*	*	μs
DIGITAL INPUTS[2]						
Convert Command	Positive Pulse 100ns min Trailing Edge Initiates Conversion	*	*	*	*	
Logic Loading	1	*	*	*	*	TTL Load
TRANSFER CHARACTERISTICS ERROR						
Gain Error[3]	±0.1(±0.25% max)	*	*	*	±0.2	%
Offset Error[3]	Adjustable to Zero	*	*	*	*	
Unipolar	±0.05(±0.2% max)	*	*	*	±0.1	% of FSR[4]
Bipolar[5]	±0.1(±0.25% max)	*	*	*	±0.2	% of FSR
Linearity Error (max)[6]	±0.048/±0.012	*	*	*	±0.012	% of FSR
Inherent Quantization Error	±0.5	*	*	*	*	LSB
Differential Linearity Error	±0.5	*	*	*	*	LSB
No Missing Codes Temperature Range	0 to +70	0 to +70	−25 to +85	−55 to +125	0 to +70/−25 to +85	°C
Power Supply Sensitivity						
±15V	±0.004	*	*	*	*	% of FSR/%V
+5V	±0.001	*	*	*	*	% of FSR/%V
DRIFT						
Specification Temperature Range	0 to +70	*	−25 to +85	−55 to +125	0 to +70/−25 to +85	°C
Gain (max)	±30	±40/±25	±20/±15	±25	±30/±25	ppm/°C
Offset						
Unipolar	±3	*	*	±5 max	*	ppm/°C
Bipolar (max)[5]	±15	±20/±12	±10/±7	±10	±15/±7	ppm/°C
Linearity (max)	±3	*	±3/±2	*	±2	ppm/°C
Monotonicity	GUARANTEED	*	*	*	GUARANTEED	
CONVERSION SPEED (MAX)	8.4/10	*	*	*	5	μs
DIGITAL OUTPUT						
(all codes complementary)						
Parallel						
Output Codes[7]						
Unipolar	CSB	*	*	*	*	
Bipolar	COB, CTC	*	*	*	*	
Output Drive	2	*	*	*	*	TTL Loads
Serial Data Codes (NRZ)	CSB, COB	*	*	*	*	
Output Drive	2	*	*	*	*	TTL Loads
Status	Logic "1" during Conversion	*	*	*	*	
Status Output Drive	2	*	*	*	*	TTL Loads
Internal Clock						
Clock Output Drive	2	*	*	*	*	TTL Loads
Frequency	1.9/1.22	*	*	*	2.6	MHz
INTERNAL REFERENCE VOLTAGE	6.3/±15mV max	*	*	*	*	Volts
Max. External Current (with no degradation of specifications)	1.0	*	*	*	*	mA
Tempco of Drift, (max)	±20/max	±10 typ	±5 typ	±5 typ	±10	ppm/°C
POWER REQUIREMENTS						
Rated Voltages	+5, ±15	*	*	*	*	Volts
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	*	Volts
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*	*	*	Volts
Supply Drain +15V	25 max	*	*	*	15 max	mA
−15V	35 max	*	*	*	35 max	mA
+5V	140 max	*	*	*	100 max	mA
Total Power Dissipation	1500 max	*	*	*	1100 max	mW
TEMPERATURE RANGE						
Specification	0 to +70	*	−25 to +85	−55 to +125	0 to +70/−25 to +85	°C
Operating (Derated Specs)	−25 to +85	*	−55 to +125	−55 to +125	−25 to +85	°C
Storage	−55 to +125	*	*	*	−65 to +150	°C
PACKAGE OPTION[9]						
DH-32D	Ceramic	Ceramic	Ceramic	Ceramic	Ceramic	

NOTES

[1] Buffer Settling time adds to conversion speed when buffer is connected to input.

[2] DTL/TTL compatible Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital output, Logic "0" = 0.4V max, Logic "1" = 2.4V min.

[3] Adjustable to zero.

[4] FSR means Full Scale Range.

[5] Guaranteed at V_{IN} = 0 volts.

[6] Error shown is the same as ±1/2LSB max error in % of FSR.

[7] See Table I.

[8] For ±12V operation add "Z" to model number. Input range limited to a maximum of ±5V.

[9] See Section 14 for package outline information.

*Specifications same as AD ADC84.

Specifications subject to change without notice.

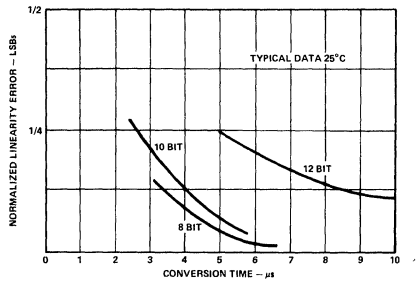


Figure 1a. Linearity Error vs. Conversion Speed (AD ADC84/AD ADC85)

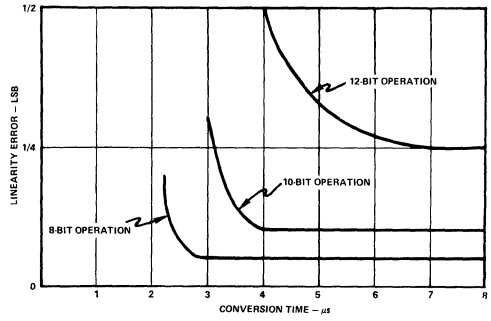


Figure 1b. Linearity Error vs. Conversion Speed (AD5240)

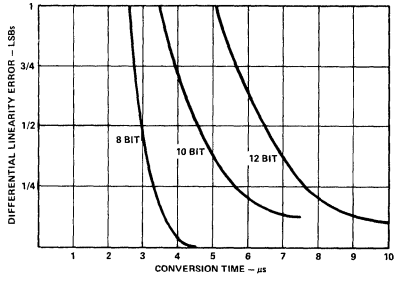


Figure 2a. Change in Differential Linearity vs. Conversion Speed (AD ADC84/AD ADC85)

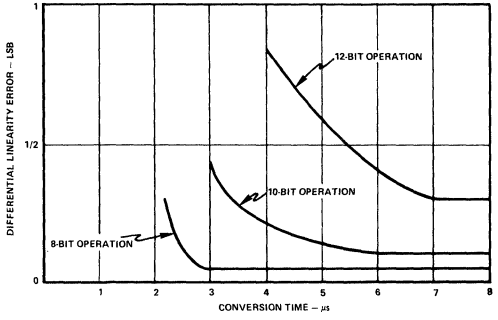


Figure 2b. Change in Differential Linearity vs. Conversion Speed (AD5240)

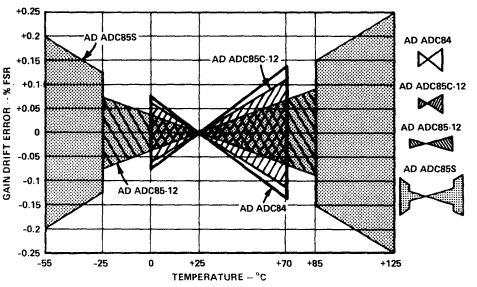


Figure 3a. Gain Drift Error (% FSR) vs. Temperature (AD ADC84/AD ADC85)

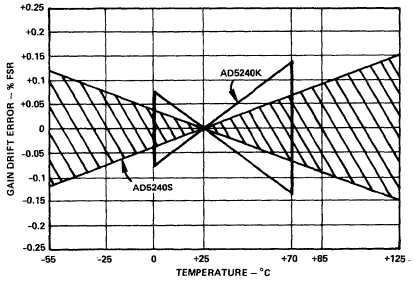


Figure 3b. Gain Drift Error (% FSR) vs. Temperature (AD5240)

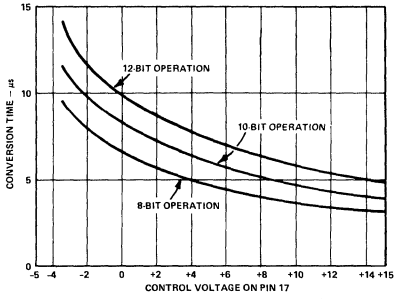


Figure 4a. Conversion Speed vs. Control Voltage (AD ADC84/AD ADC85)

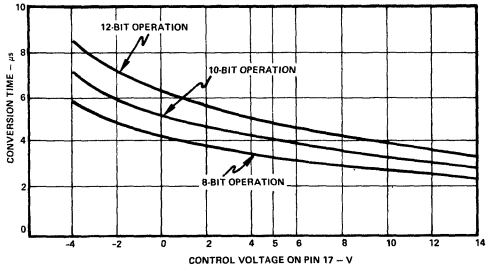


Figure 4b. Conversion Speed vs. Control Voltage (AD5240)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 22 for all ranges. As shown in Figure 5 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

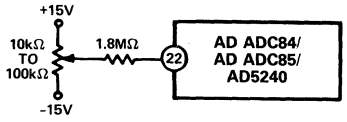


Figure 5. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 5.

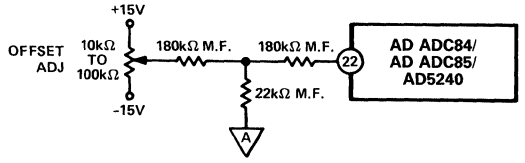


Figure 6. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 22 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 27 as shown in Figure 7.

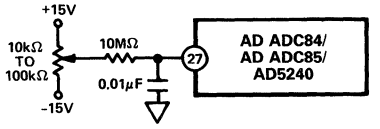


Figure 7. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 8.

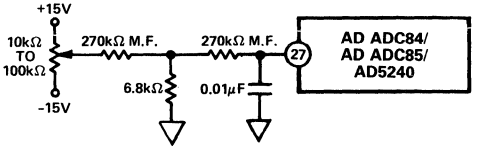


Figure 8. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

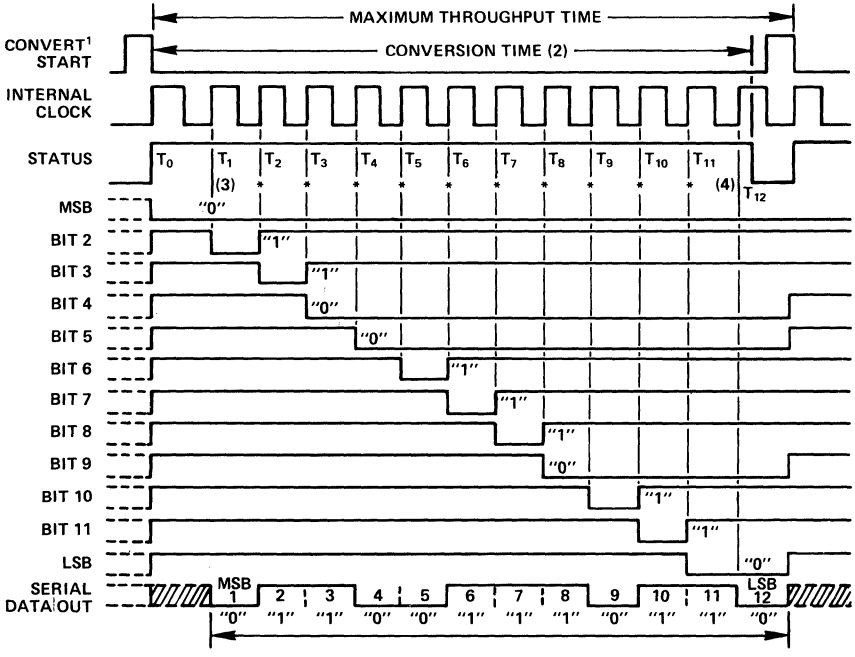
On receipt of a CONVERT START command, the AD ADC84/AD ADC85/AD5240 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 9. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 – B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking into a receiving shift register on these edges (see Figure 9).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES
1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 10μs FOR 12 BITS AND 8.4μs FOR 10 BITS (AD ADC84/AD ADC85) OR 5μs FOR 12 BITS AND 4.1μs FOR 10 BITS (AD5240).
3. MSB DECISION.
4. LSB DECISION 20ns PRIOR TO THE STATUS GOING LOW.
*BIT DECISIONS.

Figure 9. Timing Diagram (Binary Code 0 1 1 0 0 1 1 1 0 1 1 0)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 9. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 9. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 9 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 9). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	AD ADC84/ AD ADC85 (AD5240) Conversion Time (μs)	Status Flag Reset
16	15	12	0.024	10 (5)	t_{12} +40ns
2	16	10	0.100	8.5 (4.1)	t_{10} +40ns
4	28	8	0.390	6.8 (3.3)	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC84/AD ADC85/AD5240 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 10 for circuit detail.

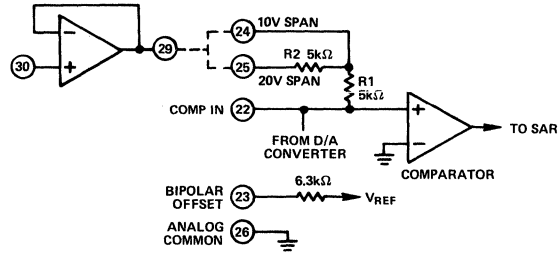


Figure 10. Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table II. Input Scaling Connections

INPUT VOLTAGE RANGE AND LSB VALUES

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{\text{FSR}}{2^n}$	$\frac{20\text{V}}{2^n}$	$\frac{10\text{V}}{2^n}$	$\frac{5\text{V}}{2^n}$	$\frac{10\text{V}}{2^n}$	$\frac{5\text{V}}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definition

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 11 and 12, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

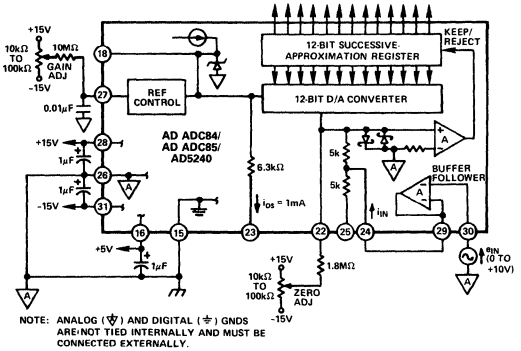


Figure 11. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

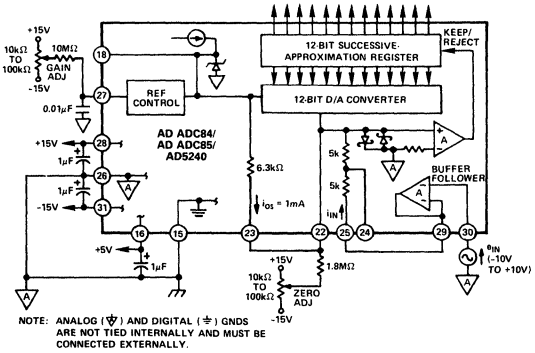


Figure 12. Analog and Power Connections for Bipolar −10V to +10V Input Range with Buffer Follower

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 011111111111.

Other Ranges: Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, -2.5V to +2.5V and -5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC84/AD ADC85/AD5240. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC84/AD ADC85/AD5240's supply terminals should be capacitively decoupled as close to the device as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the CLOCK RATE is desired for faster conversion speeds, the CLOCK RATE CONTROL may be connected to an external multi-turn trim potentiomer with a TCR of ±100ppm/°C or less as shown in Figures 13 and 14. If the potentiometer is connected to -15V, conversion time can be increased as shown in Figure 9. If these adjustments are used, delete the connections shown in Table I for pin 17. See Figures 1a or 1b for nonlinearity error vs. conversion speed and Figures 4a or 4b for the effect of the control voltage on clock speed.

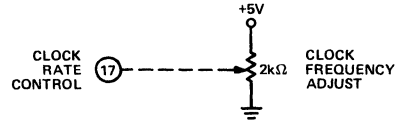


Figure 13. 12-Bit Clock Rate Control Optional Fine Adjust

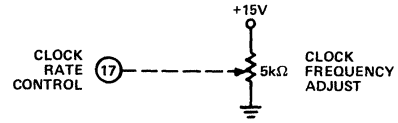


Figure 14. 8-Bit Clock Rate Control Optional Fine Adjust

MICROPROCESSOR INTERFACING

The fast conversion times of the AD ADC84/AD ADC85 and AD5240 suggest several different methods of interface to microprocessors. In systems where the ADC is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSB's reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSB's in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 15 shows a typical connection of an 8085-type bus, using a left-justified data format for unipolar inputs. Status polling is optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD ADC84/AD ADC85/AD5240 should be reversed,

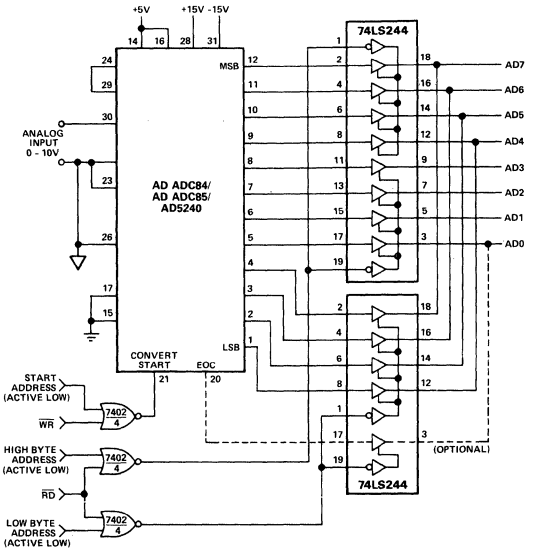


Figure 15. AD ADC84/AD ADC85/AD5240 – 8085A Interface Connections

as well as the connections to the data bus high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields a complementary offset binary-coded output. If complementary two's complement coding is desired, it can be produced by substituting MSB (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Gain T. C. – ppm/°C	Conversion Time
AD ADC84-10	±0.048%	0 to +70°C	±30	10μs
AD ADC84-12	±0.012%	0 to +70°C	±30	10μs
AD ADC85C-10	±0.048%	0 to +70°C	±40	10μs
AD ADC85C-12	±0.012%	0 to +70°C	±25	10μs
AD ADC85-10	±0.048%	-25°C to +85°C	±20	10μs
AD ADC85-12	±0.012%	-25°C to +85°C	±15	10μs
AD ADC85S-10	±0.048%	-55°C to +125°C	±25	10μs
AD ADC85S-12	±0.012%	-55°C to +125°C	±25	10μs
AD5240KD	±0.012%	0 to +70°C	±30	5μs
AD5240BD	±0.012%	-25°C to +85°C	±25	5μs
AD ADC85S-12/883B	±0.012%	-55°C to +125°C	±25	10μs
AD5240BD/883B	±0.012%	-25°C to +85°C	±25	5μs

[1] For complete model number suffixes must be added for "Z" option (±12V operation), linearity. The following guide shows the proper suffix order.
AD ADC (*)(**)-(***)

*Model Number
**"Z" Version Designator
***Linearity

Typical Part Numbers
AD ADC84-12
AD ADC85SZ-12
AD5240ZKD

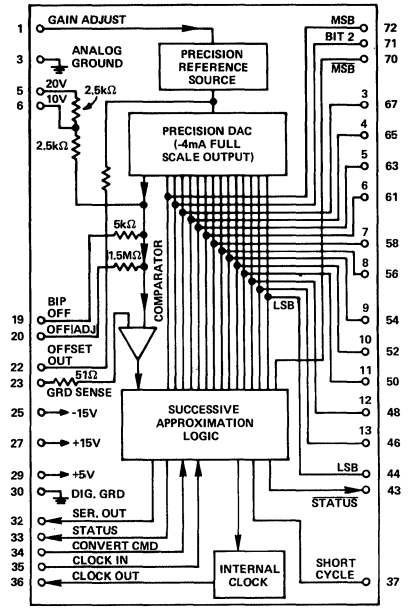
14-Bit High Speed, Analog-to-Digital Converters

ADC1130/ADC1131

FEATURES
- 14-Bit Resolution and Accuracy
- Fast 12μs Conversion Time (ADC1131J/K)
- Low 10ppm/°C Maximum Gain TC
- User Choice of Input Range
- No Missing Codes

APPLICATIONS
- Wide Band Data Digitizing
- Multichannel Computer Interface
- High Accuracy Data Acquisition
- X-Ray Tomography
- Nuclear Accelerator Instrumentation

ADC1130/ADC1131 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADC1130 and ADC1131 are high speed analog-to-digital converters packaged in a small 2" x 4" x 0.4" (51 x 102 x 10mm) module, which perform complete 14-bit conversions in 25μs and 12μs respectively. Using the successive approximations technique, they convert analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V, ±10V, ±5V. The user selects the desired range by making appropriate connections to the module terminals. The ADC1130 and ADC1131 can also be connected so as to perform conversions of less than 14 bit resolution with a proportionate decrease in conversion time.

TIMING

As shown in Figure 1, the leading edge of the convert command set the MSB output to Logic "0" and the CLOCK OUT, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 14 (LSB) comparison is completed. At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the fourteen "0" to "1" clock transitions.

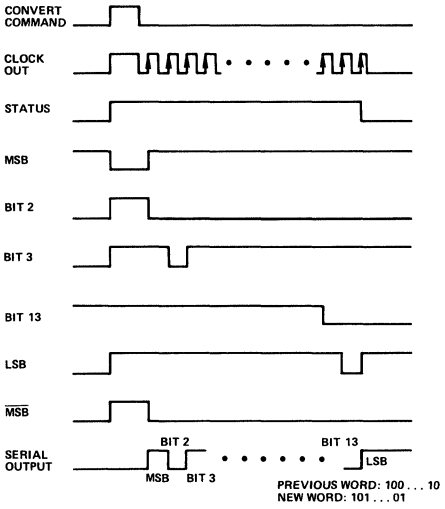


Figure 1. Timing Diagram

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	HIGH SPEED 12μs ADC1131 J	K	MEDIUM SPEED 25μs ADC1130
RESOLUTION, BITS	14	14	14
CONVERSION TIME (max)	12μs	12μs	25μs
ACCURACY			
Integral Nonlinearity Error (LSB)	±1/2 (max)	*	*
Differential Nonlinearity			
Error (LSB)	±1/2 (1 max)	±1/2 (max)	±1/2 (1 max)
Missing Codes	No missing codes	*	*
TEMPERATURE COEFFICIENTS			
Gain ppm/°C	±12 (max)	±7 (+10 max)	±12 max
Unipolar Offset	±0.7 (±3 max)	*	*
Bipolar Offset	±3 (±7 max)	*	*
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V	*	*
INPUT IMPEDANCE (10V RANGE)	2500Ω	*	*
CONVERT COMMAND	Positive Pulse, 200ns min, 400ns max Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible	*	*
PARALLEL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary, Two's Complement	*	*
SERIAL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
STATUS OUTPUT	"1" During Conversion. Complement also available TTL/DTL Compatible.	*	*
LOGIC FANOUTS AND LOADINGS			
Convert Command Input	1TTL Unit Load	*	*
Clock Input	3TTL Unit Loads	*	*
Short Cycle Input	1TTL Unit Load	*	*
Parallel Data Outputs	3TTL Unit Loads/Bit	*	*
Serial Data Output	8TTL Unit Loads	*	*
STATUS Output	2TTL Unit Loads	*	*
$\overline{\text{STATUS}}$ Output	12TTL Unit Loads	*	*
Clock Output	4TTL Unit Loads	*	*
POWER REQUIREMENTS	+15V ±5% @ 40mA	*	*
	-15V ±5% @ 60mA	*	*
	+5V ±5% @ 250mA	*	*
POWER SUPPLY SENSITIVITY			
To ±15V Tracking Supplies			
Gain	±4.5ppm/%Δ V_S	*	*
Zero	±4.5ppm/%Δ V_S	*	*
To ±15V Non-Tracking Supplies			
Gain	±10ppm/%Δ V_S	*	*
Zero	±7ppm/%Δ V_S	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	-55°C to +85°C	*	*

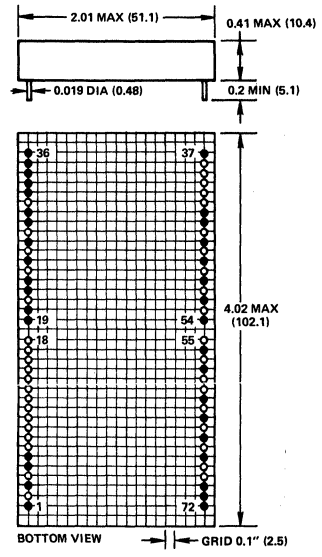
*Same Specifications as ADC1131J.

NOTES:
[1] Offset (zero) and gain errors are adjustable to zero by means of external potentiometers. See Figure 5 for proper connection.
[2] Recommended power supply: Analog Devices model 923.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 3.5 ounces (99.3 grams).
All pins are gold plated half-hard brass (MIL–G–45204), 0.019" ±0.001" (0.48 ±0.03mm) dia.

ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1130 and ADC1131 are shown in block diagram form.

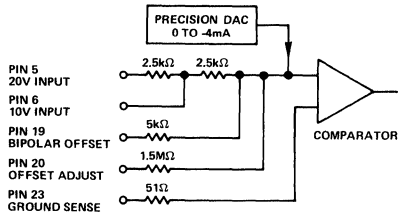


Figure 2. Input Circuit Block Diagram

When the converters are connected as a unipolar device, Pin 19 is left open circuit and, thus, no offset current is applied to the comparator input. The 0 to +10V input signal applied to Pin 6 (or the 0 to +20V input signal applied to Pin 5) develops a 0 to +4mA current which is compared to the 0 to -4mA output of the D/A converter. A voltage between +15V and -15V can be applied to Pin 20 from the wiper of a 100kΩ potentiometer to adjust the zero point by ±40LSB. To reduce the range of this trim padding resistors should be used.

With the offset output, Pin 22, connected to Pin 19, a +2mA offset current is applied to the comparator input. The ADC1130 and ADC1131 will then accept bipolar inputs of ±5V at Pin 6, or ±10V at Pin 5 and compare the 0 to +4mA sum of the offset and input signal currents to the 0 to -4mA D/A converter output. The offset adjustment potentiometer is once again used as described in the preceding paragraph.

Signal ground sense, Pin 23, should normally be jumpered to analog ground, Pin 3. In the event that an offset voltage is developed in the ground wiring, it may be possible to eliminate its effect by connecting Pin 23 directly to the signal or analog ground of the device feeding the analog input signal to the ADC. In any case, Pin 23 must not be left open.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer.

PARALLEL DATA OUTPUT

These converters produce natural Binary Coded outputs when configured as a unipolar device. As a bipolar device, they can produce either Offset Binary or Two's Complement output codes. The most significant bit is represented by Pin 72 (MSB output) for Binary and Offset Binary codes, or by Pin 70 ($\overline{\text{MSB}}$ output) for the Two's Complement code. Tables I and II illustrate the relationship between analog input and digital output for all three codes.

ANALOG INPUT		DIGITAL OUTPUT
0 to +10V Range	0 to +20V Range	Binary Code
+9.9994V	+19.9988V	11111111111111
+5.0000V	+10.0000V	10000000000000
+1.2500V	+2.5000V	00100000000000
+0.0006V	+0.0012V	00000000000001
+0.0000V	+0.0000V	00000000000000

Table I. Nominal Unipolar Input-Output Relationships

±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.9994V	+9.9988V	11111111111111	01111111111111
+2.5000V	+5.0000V	11000000000000	01000000000000
+0.0006V	+0.0012V	10000000000001	00000000000001
+0.0000V	+0.0000V	10000000000000	00000000000000
-5.0000V	-10.0000V	00000000000000	10000000000000

Table II. Nominal Bipolar Input-Output Relationships

SERIAL DATA OUTPUT

The serial data output, available on Pin 32, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the converter.

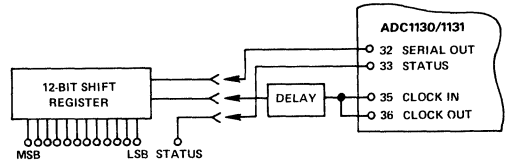


Figure 3. Serial Data Transmission

The timing diagram presented in Figure 4 shows that the converter's clock output must be delayed by an amount of time greater than or equal to the sum of the receiving shift register setup time plus the 20ns clock output to serial output delay.

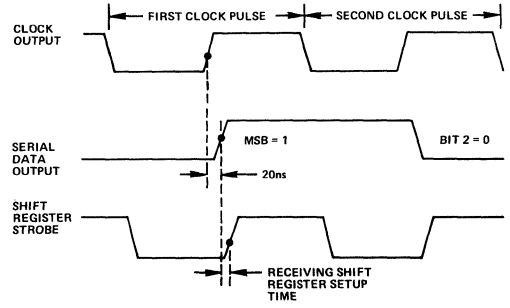


Figure 4. Serial Data Timing Diagram

The 50ns span between the time that the last serial output bit is available and the time that the STATUS output returns to zero insures that the data in the shift register will be valid on the "1" to "0" transition of the STATUS signal.

GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 5. Note that a jumper

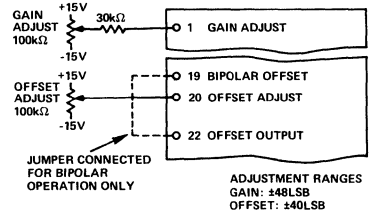


Figure 5. Adjustment Connections

is connected between Pin 19 and Pin 22 for bipolar operation; these pins *must* be left open for unipolar operation.

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment is made first. These adjustments are not made with zero and full scale input signals and it may be helpful to understand why. An A/D converter will produce a given digital output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the output of the converter to be on the verge of switching from one digital value to the adjacent digital value, the unit can be calibrated so that it does change values at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D and D/A converters.

OFFSET CALIBRATION

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V; for 0 to +20V units set it to +0.0006V. Adjust the zero potentiometer until the converter is just on the verge of switching from 00 . . . . 0 to 00 . . . . 1.

For the ±5V bipolar range set the input voltage precisely to -4.9997V; for ±10V units set it to -9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . 0 to 00 . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely to +19.9982V for 0 to +20V units, +9.9991V for 0 to +10V units, +4.9991V for ±5V units, or +9.9982V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11 . . . 0 to 11 . . . 1 and two's complement coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11.

POWER SUPPLY AND GROUNDING CONNECTIONS

These converters do not have an internal connection between analog power ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. One suggested approach is shown in Figure 6.

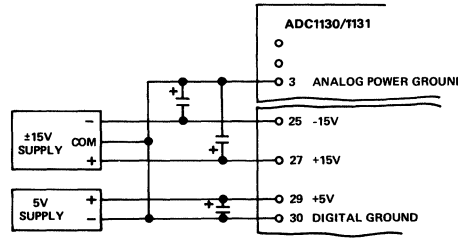


Figure 6. Power Supply and Grounding Connections

The ±15V and +5V power supplies must be externally bypassed with 15μF (+35V tantalum) capacitors. These capacitors should be connected between Pin 27 and Pin 3, between Pin 25 and Pin 3, and between Pin 29 and Pin 30. Capacitor connections should be made as close to the module pins as possible.

CLOCK CONNECTIONS

When the converters are used with their own internal clock, Pin 36 is simply jumpered to Pin 35. When the internal clock is not used, Pin 36 is grounded and an external clock capable of driving three TTL loads is connected to Pin 35. The convert command should be synchronized with the external clock.

REPETITIVE CONVERSIONS

When making repetitive conversions, a new convert command may be initiated any time after the "1" to "0" transition of the STATUS output. The $\overline{\text{STATUS}}$ output may not, however, be connected directly to the CONVERT COMMAND input for the purpose of automatically generating convert command pulses.

SHORT CYCLE CONNECTIONS

When the converters are operated as a 14-bit device, Pin 37 is left open. If, however, it is to perform conversions of less than 14 bits, Pin 37 is connected to the N+1 bit output (where N is the number of bits in the conversion). The conversion time in this mode of operation is T_C x N/14 where T_C is the conversion time of the particular model when operated at 14-bit resolution.

Low Cost, 16-Bit Analog-to-Digital Converter

ADC1140

FEATURES

Guaranteed Nonlinearity: ±0.003% FSR max
35μs Maximum Conversion Time
Small Size 2" X 2" X 0.4"
Wide Power Supply Operation: ±12V to ±17V

APPLICATIONS

Process Control Data Acquisition
Seismic Data Acquisition
Nuclear Instrumentation
Medical Instrumentation
Pulse Code Modulation Telemetry
Industrial Scales
Robotics

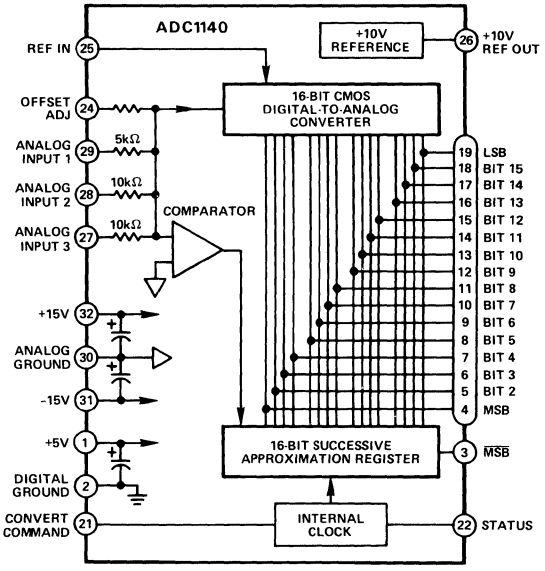
GENERAL DESCRIPTION

The ADC1140 is a low cost 16-bit successive-approximation analog-to-digital converter having a 35μs maximum conversion time. This converter provides high accuracy, high stability and low power consumption all in a 2" X 2" X 0.4" module.

High accuracy performance such as integral and differential nonlinearity of ±0.003% FSR max are both guaranteed. Guaranteed stability such as differential nonlinearity TC of ±2ppm/°C maximum, offset TC of ±30μV/°C maximum, gain TC of ±12ppm/°C maximum and power supply sensitivity of ±0.002% of FSR/% V_S are also provided by the ADC1140.

The ADC1140 makes extensive use of both integrated circuit and thin-film components to obtain excellent performance, small size and low cost. The internal 16-bit DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary CMOS current-steering switches. A low noise reference, low power comparator and low power successive-approximation register are also used to optimize the ADC1140's design (shown in Figure 1).

ADC1140 FUNCTIONAL BLOCK DIAGRAM



The ADC1140 can operate with power supplies ranging from ±12V to ±17V and has provisions for a user supplied external reference. Four analog input voltage ranges are selectable via pin programming: ±5V, ±10V, 0 to +5V and 0 to +10V. Bipolar coding is provided in the offset binary and two's complement formats with unipolar coding displayed in true binary.

SPECIFICATIONS (typical @ +25°C $\pm V_S = \pm 15V$, $V_{CC} = +5V$, $V_{REF} = +10.0V$ unless otherwise specified)

Model	ADC1140
RESOLUTION	16 Bits
CONVERSION TIME	35μs max
ACCURACY[1]	
Nonlinearity Error	±0.003% FSR[2] max
Differential Nonlinearity Error	±0.003% FSR[2] max
STABILITY	
Differential Nonlinearity	±2ppm/°C max
Gain (with internal reference)	±12ppm/°C max
(without internal reference)	±4ppm/°C max
Unipolar Offset	±30μV/°C max
Bipolar Offset	±7ppm/°C max
POWER SUPPLY SENSITIVITY	±0.002% FSR/% V_S
ANALOG INPUT	
Voltage Ranges	
Bipolar	±5V, ±10V
Unipolar	0 to +5V, 0 to +10V
Input Resistance	
0 to +5V	2.5kΩ
0 to +10V, ±5V	5.0kΩ
±10V	10.0kΩ
External Reference Input[3]	
Voltage Range	0 to +12V
Input Resistance	2.5kΩ
DIGITAL INPUT	
Convert Command	Positive Pulse, 100ns Width min Negative Edge Triggered
Logic Loading	1TTL Load
DIGITAL OUTPUT	
Parallel Output Data	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN) Two's Complement
Output Drive	1TTL Load
Status	Logic "1" During Conversion
Output Drive	1TTL Load
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%
External Load Current	
(Rated Performance)	2mA max
Temperature Stability	±8.5ppm/°C max
POWER REQUIREMENTS[4]	
Voltage (Rated Performance)	±15V ±3%, +5V ±3%
Voltage (Operating)	±12V to ±17V, +4.75V to +5.25V
Supply Current Drain ±15V	±25mA
+5V	150mA
TEMPERATURE RANGE	
Specified	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
SIZE	2" X 2" X 0.4" (51 X 51 X 10.4mm)
Weight	1.2 oz (33g)

NOTES

[1] Offset and gain error are adjustable to zero by means of external potentiometers. See Figure 3 for proper connection.

[2] FSR means Full Scale Range.

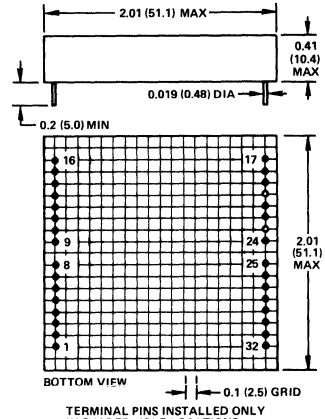
[3] Rated performance is specified with +10.0V reference.

[4] Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

MATING CONNECTORS AC1577 (2 REQUIRED)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	-15V
3	MSB	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	NOT USED
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	NOT USED
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

OTHER HIGH RESOLUTION PRODUCTS FROM ANALOG DEVICES:

- 14-Bit/15-Bit Sampling A/D Converters; DAS1152/53
  - 25kHz (14-Bit)/20kHz (15-Bit) throughput rates
  - Second Source to A/D/A/M824 and A/D/A/M825 Modules
- 14-Bit/15-Bit Low Level Data Acquisition Systems: DAS1155/56
  - 25kHz (14-Bit)/20kHz (15-Bit) throughput rates
  - High Performance PGIA (1V/V–1000V/V), SHA and A/D Converter
- 14-Bit Sample-Hold Amplifier: SHA1144
  - Acquisition Time: 8μs max to ±0.003% (20V step)

OPERATION

For operation, the only connections to the ADC1140 that are necessary are the power supplies, internal or external reference, input voltage pin programming, convert command and digital output. Refer to Table I for input pin programming and Figure 3 for offset and gain calibration.

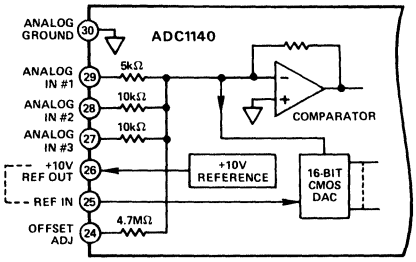


Figure 2. Analog Input Block Diagram

ANALOG INPUT PROGRAMMING

The analog input section consists of three analog input terminals. Analog input range selection is accomplished by pin programming as shown in Table I.

In the unipolar mode, a 0 to +10V or a 0 to +5V input signal develops a 0 to +2mA current that is compared to the 0 to -2mA (shown in Figure 2) current output of the DAC.

In the bipolar mode, a +1mA offset current from the reference is applied to the comparator input via pin programming connections. The ADC1140 can then accept either ±5V or ±10V inputs. These inputs again will be converted to current and compared with the DAC's 0 to -2mA current output.

Input Signal Range	Coding	Connect Input Signal To Pin(s)	Connect Pin 26 To Pin*	Connect Pin 30 To Pin(s)
±10V	OBIN, Two's Comp	28	27	29, 2
±5V	OBIN, Two's Comp	29	27	28, 2
0 to +5V	BIN	27, 28, 29	Open	2
0 to +10V	BIN	27, 28	Open	29, 2

*If Internal Reference is used, Pins 25 and 26 must be connected together through a 50Ω potentiometer or 24.9Ω fixed resistor (see Figure 3 and the gain calibration section).

Table I. Analog Input Voltage Pin Programming

OPTION OFFSET & GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of an accurate and stable voltage reference. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range. The potentiometers selected should be of the good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

By adjusting the offset first, gain and offset adjustments will remain independent of each other.

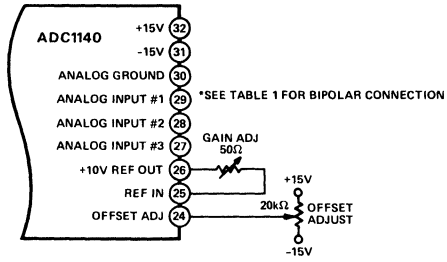


Figure 3. Offset and Gain Calibration

OFFSET CALIBRATION

For 0 to +10V range, set the input voltage precisely to +76μV; for 0 to +5V range, set it at +38μV. Adjust the zero potentiometer until the binary coded converter is just on the verge of switching from 000 . . . 00 to 000 . . . 01.

For ±5V range, set the input voltage precisely to -4.999924V; for ±10V range, set it at -9.999847V. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000 . . . 00 to 000 . . . 01 and the two's comp. coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely at +9.99977V for 0 to +10V input range, +4.99977V for ±5V input range, +9.99954V for ±10V input range, or +4.99988V for 0 to +5V input range, adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 111 . . . 0 to 111 . . . 1 and two's comp. coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11. Note that these values are 1 1/2 LSBs less than nominal full scale.

POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally. The connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1140 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.

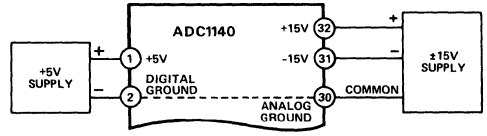


Figure 4. Power Supply and Grounding Techniques

ADC1140 TIMING

Conversion is initiated with the negative going edge of the Convert Command pulse as shown in Figure 5. The Convert Command pulse width must be a minimum of 100ns. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the Convert Command pulse, all internal logic is reset. The MSB is set low with the remaining digitial outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle.

During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 16-bit conversion taking 35μs maximum. At this time, the STATUS line goes low signifying that the low conversion is complete.

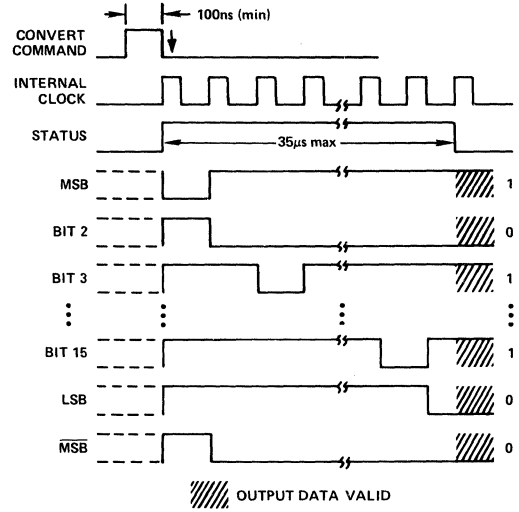


Figure 5. ADC1140 Timing Diagram

ANALOG INPUT/OUTPUT RELATIONSHIPS

The ADC1140 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is displayed on pin 4 for the binary and offset binary codes or on pin 3 for the two's complement code. Table II shows the unipolar analog input/digital output relationships. Table III shows the bipolar analog input/digital output relationships for offset binary code and two's complement codes.

Analog Input 0 to +5V Range	Analog Input 0 to +10V Range	Digital Output Binary Code
+4.999924V	+9.99985V	1111 1111 1111 1111
+2.50000V	+5.00000V	1000 0000 0000 0000
+1.25000V	+2.50000V	0100 0000 0000 0000
+0.62500V	+1.25000V	0010 0000 0000 0000
+0.000076V	+0.000153V	0000 0000 0000 0001
+0.00000V	+0.00000V	0000 0000 0000 0000

Table II. Unipolar Input/Output Relationships

Analog Input ±5V Range	Analog Input ±10V Range	Digital Output Offset Binary Code	Digital Output 2's Complement Code
+4.99985V	+9.99970V	1111 1111 1111 1111	0111 1111 1111 1111
+2.50000V	+5.00000V	1100 0000 0000 0000	0100 0000 0000 0000
+0.000153V	+0.000305V	1000 0000 0000 0001	0000 0000 0000 0001
+0.00000V	+0.00000V	1000 0000 0000 0000	0000 0000 0000 0000
-5.00000V	-10.00000V	0000 0000 0000 0000	1000 0000 0000 0000

Table III. Bipolar Input/Output Relationships

HIGH RESOLUTION DATA ACQUISITION SYSTEM

Shown in Figure 6 is a high resolution data acquisition system. Here the SHA1144, a high resolution sample-hold amplifier, is used to drive the ADC1140. Conversion is initiated by the negative edge of the convert command pulse. At this time the STATUS pulse goes low causing the SHA1144 to go from the sample mode to the hold mode. When the conversion is complete, 35μs later, the STATUS pulse goes low, thus placing the SHA1144 in the sample mode.

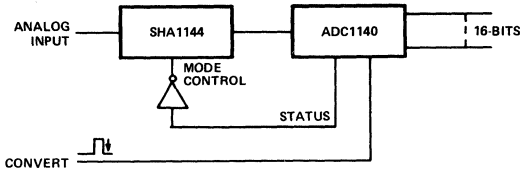


Figure 6. High Resolution Data Acquisition System

EXTERNAL REFERENCE

The ADC1140 is capable of operating with an external +10.0V reference. Simply disconnect the gain trim potentiometer from pin 26 and connect it to the external reference as shown in Figure 7. The external reference output must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained. Gain error is adjusted as previously discussed in the gain calibration section.

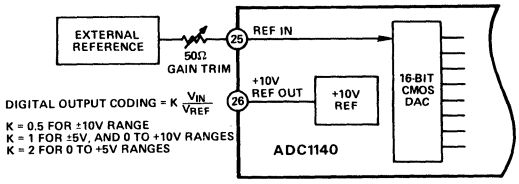


Figure 7. External Reference

The ADC1140 is factory tested and calibrated with the internal +10.0V reference voltage but nonstandard external voltages can be used with the digital output coding being determined by the formula shown in Figure 7.

PIA INTERFACE

The ADC1140 can be used with a PIA to interface directly to a microprocessor. As shown in Figure 8 the 16-bit output of the ADC1140 is split into two 8-bit bytes. Part A of the PIA is programmed to read the eight most-significant-bits while Part B reads the eight least-significant-bits. Output CB2 is used to start the ADC1140 conversion process. CB1, of the PIA, is used to sense the STATUS of the ADC1140 so that the end of conversions can be determined. The control bus, address bus, and data bus are then connected directly to the microprocessor.

With the use of PIAs, control of one or more ADC1140s can be accomplished in many different configurations.

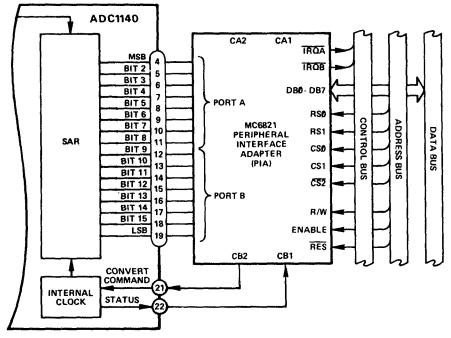


Figure 8. ADC1140 Interface to PIA

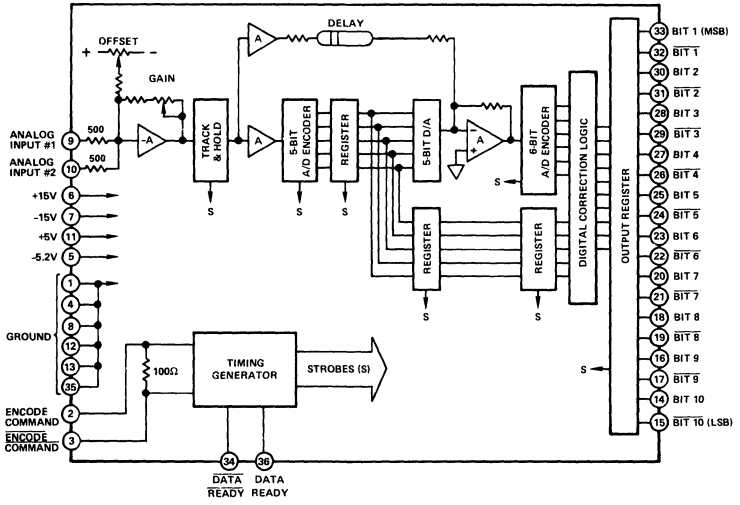
10-Bit Video Analog-to-Digital Converter

CAV-1040

FEATURES
10-Bit Resolution
40MHz Word Rate
Single 35-In² PC Board
ECL Compatible
No External Circuits Required

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis
Transient Analysis

CAV-1040 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices Model CAV-1040 A/D converter is a "system solution" which combines 10-bit resolution, 40MHz word rates, and small size to solve high-speed digitizing problems. Its design is based on proven concepts introduced in the MOD-1020 and MOD-1205 A/D Converters and takes advantage of recent advances in technology to achieve a new level of performance in high-resolution converters.

It is pin-for-pin compatible with the industry's first 10-bit, 20MHz A/D, the MOD-1020. But it *doubles* the word rate of its predecessor, making it possible for system designers to upgrade their systems without new layouts.

This remarkable converter is a complete answer to the question of digitizing radar, video, and/or other high-frequency inputs; it includes a track-and-hold, along with encoding and timing circuits. The CAV-1040 is an ideal choice for the designer who needs state-of-the-art performance in high-resolution, ultra-high-speed A/D conversion.

For applications requiring maximum analog bandwidth, the CAV-1040A is the choice. In this version, the input operational amplifier and its associated offset and gain controls have been eliminated; this effectively doubles the analog input bandwidth.

All inputs and outputs are ECL compatible. Analog input impedance is 250 ohms on 1V range; 500 ohms on 2V range. The A/D requires only an encode command and external power supplies for operation. The CAV-1040 is repairable and backed by Analog Devices' limited one-year warranty.

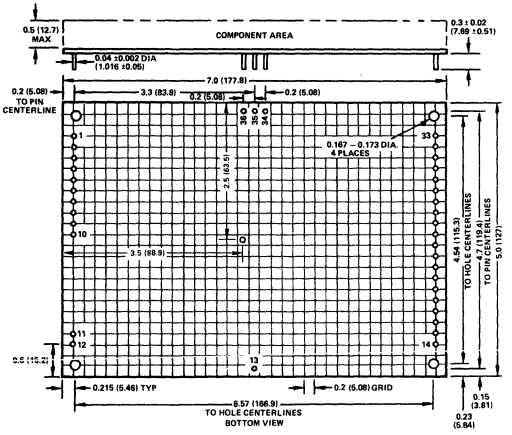
SPECIFICATIONS (typical at +25°C with nominal power supplies unless otherwise noted)

Model	Units	CAV-1040	CAV-1040A
RESOLUTION (FS = Full Scale)	Bits	10	*
	%FS	0.1	*
LSB WEIGHT			
1V p-p FS	mV	1	N/A
2V p-p FS	mV	2	*
ACCURACY			
(Including Linearity) @ dc	% FS ± 1/2LSB	0.05	*
Monotonicity		Guaranteed	
Nonlinearity Vs. Temperature	ppm/°C	10	*
Offset vs. Temperature	ppm/°C (max)	200 (300)	*
Gain vs. Temperature	ppm/°C (max)	50 (100)	*
DYNAMIC CHARACTERISTICS			
In-Band Harmonics[1]			
500kHz input	dB below FS, min	65	*
2.3MHz input	dB below FS, min	55	*
9.3MHz input	dB below FS, min	48	*
Conversion Time[2]	ns	100 + 1 clock period	*
Conversion Rate	MHz, max	40	*
Aperture Uncertainty (Jitter)	ps, rms max	20	*
Effective Aperture Delay Time[3]	ns	−2	8
(± 2ns tolerance unit-to-unit)			
Signal to Noise Ratio (SNR)[4]	dB, min	56	*
Noise Power Ratio (NPR)[5]	dB (min)	50 (47)	*
Transient Response[6]	ns	50	*
Overvoltage Recovery[7]	ns	50	*
Input Bandwidth			
Small Signal, 3dB[8]	MHz	30	60
Large Signal, 3dB[9]	MHz	20	40
Two-Tone Linearity (@Input Frequencies)[10]			
(360kHz; 390kHz)	dB below FS, min	67	*
Differential Phase[11]	°	0.5	*
Differential Gain[11]	%	1	*
ANALOG INPUT			
Voltage Range			
Input Pins 9 & 10 Connected	V, p-p FS	1	N/A
Input Pin 9 or 10	V, p-p FS	2	N/A
	V, max	±4	*
Input Pin 9	V, p-p FS	N/A	2 ± 2%
Input Type		Either Unipolar or Bipolar	Bipolar only
Impedance			
1V Input Range	Ohms	250	N/A
2V Input Range	Ohms	500	*
Offset	mV	Adjustable to Zero with On-Card Potentiometer	±4 (Not adjustable)
vs. Temperature	ppm/°C (max)	200 (300)	*
ENCODE COMMAND INPUT[12]			
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Input)	V	"1" = −0.9	*
Impedance (Line-to-Line)	Ohms, max	100	*
Rise and Fall Times	ns, max	5	*
Width			
Min	ns	10	*
Max		70% of Encode Command period	*
Frequency[13]	MHz	dc to 40	*
DIGITAL OUTPUT			
Format	Bits	10 Parallel; NRZ	*
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Output)	V	"1" = −0.9	*
Drive (Line-to-Line)	Ohms, min	75	*
Time Skew	ns, max	5	*
Coding		Binary (BIN); 2's Complement (2SC)	Compl. Binary (CBIN) Compl. 2's Compl. (C2SC)
DATA READY OUTPUT			
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Output)	V	"1" = −0.9	*
Drive (Line-to-Line)	Ohms, min	75	*
Rise and Fall Times	ns, max	5	*
Duration	ns (max)	10 (± 2)	*
POWER REQUIREMENTS[14]			
+ 15V ± 5%	mA, max	375	*
− 15V ± 5%	mA, max	200	*
+ 5V ± 5%	mA, max	25	*
− 5.2V ± 5%	A, max	2.5	*
Power Consumption	W (max)	20 (22)	*
TEMPERATURE RANGE			
Operating	°C	0 to + 70	*
Storage	°C	−55 to + 85	*
Cooling Air Requirements	LFPM (Linear Feet Per Minute)	500	*
CONSTRUCTION			
Single Printed Circuit Card	Inches	7.0 × 5.0 × 0.5	*
MEAN TIME BETWEEN FAILURES[15]	Hours		3.22×10^4

For applications assistance, call Computer Labs Division at (919) 668-9511.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	19	BIT 8
2	ENCODE COMMAND	20	BIT 7
3	ENCODE COMMAND	21	BIT 7
4	GROUND	22	BIT 6
5	-5.2V	23	BIT 6
6	+15V	24	BIT 5
7	-15V	25	BIT 5
8	GROUND	26	BIT 4
9	ANALOG INPUT #1	27	BIT 4
10	ANALOG INPUT #2	28	BIT 3
11	+5V	29	BIT 3
12	GROUND	30	BIT 2
13	GROUND	31	BIT 2
14	BIT 10	32	BIT 1
15	BIT 10	33	BIT 1
16	BIT 9	34	DATA READY
17	BIT 9	35	GROUND
18	BIT 8	36	DATA READY

ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE ADC.

NOTES

[1]In-Band Harmonics expressed in terms of spurious in-band signals and related harmonics generated at 40MHz encode rate.
[2]Measured from leading edge Encode Command to trailing edge Data Ready; use trailing edge to strobe output data into external circuits (see Text).
[3]See text for Effective Aperture Delay Time description.
[4]Rms signal to rms noise ratio with 500kHz analog input.
[5]Dc to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz, and encode rate of 40MHz.
[6]For full-scale step input, 10-bit accuracy attained in specified time.
[7]Recovers to 10-bit accuracy in specified time after 2 × FS input overvoltage.
[8]With analog input 40dB below FS.
[9]With FS analog input. (Large-signal bandwidth flat within 0.2dB, dc to 8MHz on CAV-1040; dc to 20MHz on CAV-1040A.)
[10]Each input frequency applied at level 7dB below full scale.
[11]Differential phase and differential gain measured with 20-IRE unit reference.
[12]Transition from digital "0" to digital "1" initiates encoding.
[13]For operation at word rates below 500kHz, consult factory.
[14]± 15V must be equal and opposite within 200mV and track over temperature.
[15]Calculated using MIL HNBK-217; + 25°C Ambient; Ground Fixed; 500 LFPM Air Flow.

*Specifications same as CAV-1040.
Specifications subject to change without notice.

THEORY OF OPERATION

Refer to the block diagram of the CAV-1040.

The OFFSET and GAIN controls shown on this diagram are exclusive to the model CAV-1040; they are not included in the model CAV-1040A. In the latter unit, the input operational amplifier is replaced by a buffer amplifier. As shown in the SPECIFICATIONS table, this difference in the front-end design causes the CAV-1040A to have only one input range (2V p-p); and materially increases the bandwidth of the converter.

Analog input signals to be digitized are applied through the input amplifier to a track-and-hold (T/H) amplifier which is normally operating as a buffer amplifier in the "track" mode, following all changes in analog input as they occur. The user of the CAV-1040 determines the point at which the analog signal is to be digitized by applying an Encode Command.

The leading edge of the encode command causes the track-and-hold to switch momentarily to the "hold" mode of operation, "freezing" the analog input signal long enough to begin the digitizing process.

In the CAV-1040, Effective Aperture Delay Time is defined as the interval between the leading edge of the encode command and that instant when the input signal is equal to the sampled value.

Basically, effective aperture delay time is a measure of the difference between the analog and digital delay (t_d-t_a) and can assume a zero, positive, or negative value depending on the comparative lengths of the two delays. In the CAV-1040, the analog delay (t_a) is greater than the switching delay (t_d), and causes the unit to hold an input voltage which occurred before the encode command because the track-and-hold sees a delayed version of the input signal.

Effective aperture delay time is different between the CAV-1040 and the CAV-1040A because the input amplifier of the CAV-1040 adds approximately 10 nanoseconds of analog delay to the signal path.

The "held" value of analog signal at the output of the T/H is applied to a 5-bit encoder. It is also applied through a buffer amplifier to an analog delay circuit, whose time delay is equal to the interval required for the first step of the digitizing/reconstruction process.

After being digitized to 5-bit accuracy, the held value from the T/H is applied through registers to a 5-bit D/A converter which has 12-bit accuracy. Via a second set of registers, the same digital signal is directed to the digital correction logic circuits. The data stored in these latter registers will eventually represent Bits 1-5 of the 10-bit digital output of the CAV-1040.

The inverted, reconstructed output of the D/A converter becomes one input to an operational amplifier, whose other input is the delayed analog signal from the delay line. At the output of the wideband, fast-settling op amp, the resulting signal represents the residue which remains after a 5-bit digital representation of the analog input has been subtracted from that input.

This residue, or error, signal is encoded by a second converter and is applied as 6-bit digital information to the digital correction logic circuits which contain Bits 1-5.

The correction circuits combine the 5-bit and 6-bit bytes of data to compensate for possible nonlinearities and other errors to assure the final 10-bit output of the CAV-1040 is 10-bit accurate.

Expressed in its simplest terms, the digital correction logic circuits use the information in the 6-bit signal to determine what modifications of Bits 1-5 may be necessary. The value of the MSB in the 6-bit byte establishes whether the 5-bit data are passed "as is" or whether they are increased by a value of binary "1". The remaining bits (2-6) of the 6-bit byte become Bits 6-10 of the CAV-1040 digital output.

Digitally corrected subranging (DCS), the innovative technique described here, helps compensate for a wide range of potential errors which could otherwise be avoided only if the CAV-1040 design included expensive, high precision components.

The use of 11 bits to obtain an accurate 10 bits of output cannot prevent gain error, track/hold droop error, linearity error, offset error, or any of the other inherent characteristics of "real world" A/D converters. But DCS can, and does, help nullify their effects and makes it economically feasible to accomplish high-speed, high-resolution digitizing of analog signals.

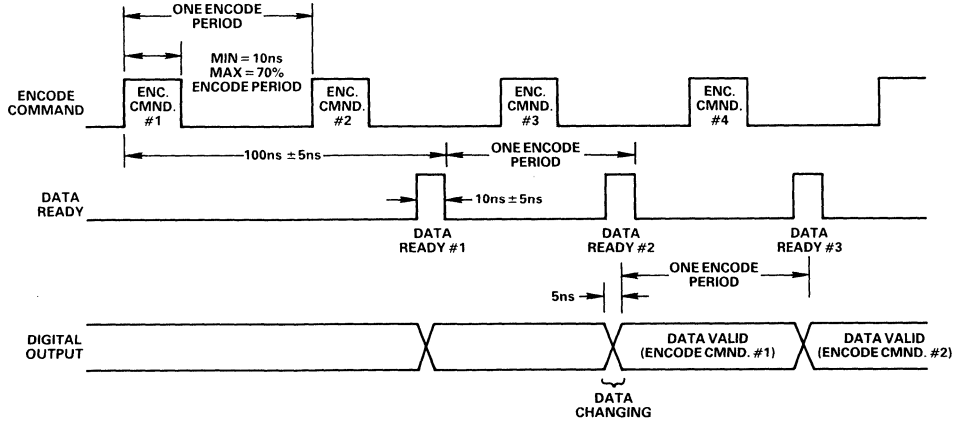


Figure 1. CAV-1040 Timing Diagram

CAV-1040 TIMING

Refer to Figure 1, the CAV-1040 Timing Diagram.

The intervals which are shown represent a continuous update rate of approximately 15.5MHz, which is considerably below the maximum capabilities of the CAV-1040. But that frequency helps to illustrate the "pipeline delay" characteristic of the converter.

At this word rate, spacing between encode commands is approximately 65 nanoseconds; and three encode commands have occurred before the data associated with the first command are valid. In Figure 1, this pipeline delay has a total time of approximately 155 nanoseconds (90ns + 65ns). This interval will be different at other word rates, but will always include 90ns; depending upon the update rate, either more or fewer encode commands may occur before the first data are available.

After the initial delay, valid data will be available at the word rate dictated by encode commands. Note that the spacing between Encode Command #1 and Encode Command #2 is equal to one encode period. This is the same spacing as between Data Ready #1 and Data Ready #2, and is also the spacing between the first and second groups of valid data.

System timing can be adjusted as necessary to take into account the pipeline delay effects and assure that the data of interest are strobed out of the converter at the appropriate time.

Figure 1 also illustrates why the trailing edge of the Data Ready pulse is recommended as the strobe for output data. Typically, data begin changing with the leading (rising) edge of each Data Ready pulse; they will be fully settled at the time of the trailing (falling) edge and available for use in external circuits.

Another possibility for strobing the output data is to use the DATA READY pulse. Its trailing edge occurs at the same time as the trailing edge of the DATA READY signal, but is a rising edge, which may facilitate its use as a strobe.

ANALOG INPUT RANGE OPTIONS

Refer to Figure 2.

The input circuits which are shown apply only to the Model CAV-1040. The Model CAV-1040A does not include OFFSET and GAIN controls; nor is there a resistor connected to Pin 10 in that unit.

For a 1V range on the CAV-1040, connect the analog input to Pin 9, and connect Pins 9 and 10 together. The unterminated input impedance is 250 ohms. For a 2V range, connect the analog input to Pin 9, and leave Pin 10 disconnected. Unterminated impedance under these conditions is 500 ohms.

To obtain the desired input impedance for either a 1V range or a 2V range on the CAV-1040, connect the appropriate external terminating resistor between the analog input pin(s) and ground, as shown in Figure 2. Input impedances greater than 100 ohms will result in loss of input bandwidth and should be avoided.

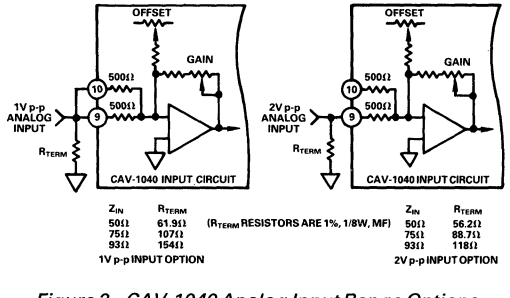


Figure 2. CAV-1040 Analog Input Range Options

The differences in the input circuit of the CAV-1040A preclude an ability to adjust gain and offset on that unit; in addition, there is no 1V input range available. The 2V input range of the CAV-1040A, however, can be terminated in the same way as the 2V range of the CAV-1040.

OFFSET AND GAIN ADJUSTMENTS

The offset and gain of the CAV-1040A are set at the factory and are not adjustable by the user.

Refer to Figure 3, the CAV-1040 Adjustment Controls.

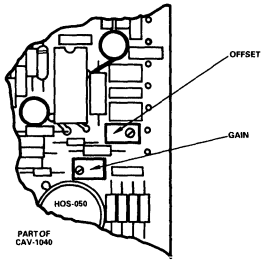


Figure 3. Offset and Gain Controls

When adjusting offset and gain of the CAV-1040 in the system, the OFFSET control should be adjusted first. It has sufficient range to allow the user to operate the CAV-1040 A/D in either the unipolar or bipolar mode. The adjustment sequence is:

1. Apply to the analog input a precise (±0.25mV) dc level corresponding to midscale of the desired input range.
2. Adust OFFSET control while observing MSB (Bit 1); adjust for MSB "toggling" between digital "0" and digital "1".
3. Apply a precise (±0.25mV) dc level corresponding to the most negative excursion of the desired input range.
4. Adjust GAIN control while observing LSB (Bit 10); adjust for output of Bits 1-9 solid "0" with LSB "toggling".
5. Apply a precise (±0.25mV) dc level corresponding to the most positive excursion of the desired input range.
6. Check digital output to assure Bits 1-9 are solid "1" with LSB "toggling".
7. Adjust OFFSET and GAIN controls alternately as necessary to obtain analog input range tolerance of ±1/2LSB.

ORDERING INFORMATION

For standard CAV-1040 units, order model number CAV-1040-400 or CAV-1040A-400. Standard units are set up at the factory to operate for optimum performance at word rates from 35-40MHz.

Converters intended to operate generally at word rates below 35MHz have different model numbers. Order by model number CAV-1040-XXX or CAV-1040A-XXX; in this designation, XXX is specified by the customer to indicate the desired optimized word rate. The decimal place is assumed (but not shown) between the second and third places. CAV-1040-300, for example, indicates final calibration and optimum performance at 30MHz. But the unit will operate over a range of word rates from 500kHz to 40MHz.

Optimum performance will be achieved within a band of frequencies approximately ±12% around the selected word rate. If later applications require word rates beyond the limits of the original optimum frequency, the unit can be returned to the factory for calibration; there is a nominal charge for this service.

Mating sockets for the CAV-1040 converters are model number MSB-2 (thru hole) or MSB-3 (closed end). These are individual solder-type pin sockets for mounting in PC boards; one is required for each of the 36 pins of the converter.

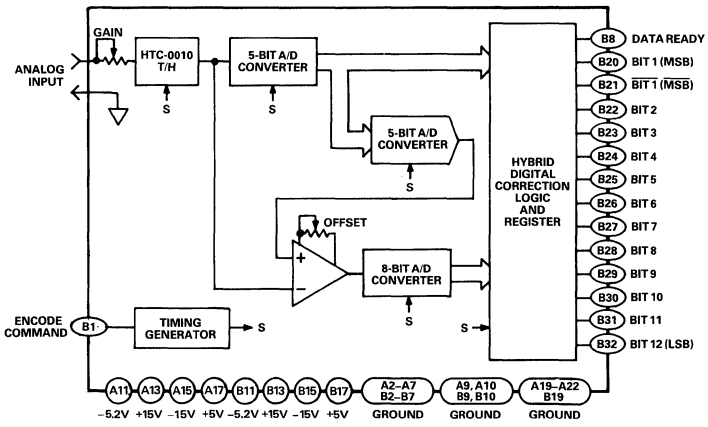
12-Bit, 5MHz Eurocard Analog-to-Digital Converter

CAV-1205

FEATURES
12-Bit Resolution
5MHz Word Rate
Single Eurocard Size
TTL Compatible
Completely Self-Contained

APPLICATIONS
Transient Analysis
Radar Digitizing
Medical Instrumentation

CAV-1205 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices model CAV-1205 A/D converter combines 12-bit resolution, 5MHz conversion speed and self-contained A/D capabilities in a single-width Eurocard size board. These characteristics make the CAV-1205 a natural choice for a variety of high-speed, high-resolution conversion requirements.

Since the complete A/D function is provided on a single card, the unit eases system integration and avoids a need for the user to "match" the characteristics of a track-and-hold to an encoder. Each CAV-1205 is complete with T/H, encoder section, output registers, and all necessary timing circuits to generate 12-bit digital representations of high-frequency analog signals at word rates through 5MHz.

The encode command which initiates the conversion process and the digital outputs of the converter are TTL compatible. All that is needed for converting wideband analog input signals is an encode command and standard power supplies. The analog input is applied via a coaxial SMA connector at the edge of the board to provide isolation from digital switiching noise which may be present; gain and offset of the unit are adjustable with on-board potentiometers.

Like its pin-compatible predecessor, the 2MHz CAV-1202, the CAV-1205 A/D converter is based on the Level 2 requirements for printed circuit board subunits; and meets the standards established by DIN 41494, IEC 48D (sec) 12.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	CAV-1205
RESOLUTION (FS = Full Scale)	Bits	12
LSB WEIGHT		
2.048V FS	mV	0.5
4.096V	mV	1.0
ACCURACY @ dc		
Linearity		
Integral	LSB	±1/2
Differential	LSB (max)	±1/2 (±1)
Monotonicity		Guaranteed
Diff. Nonlinearity vs. Temperature	ppm/°C (max)	5 (10)
Offset vs. Temperature	ppm/°C (max)	50 (150)
Gain vs. Temperature	ppm/°C (max)	75 (150)
DYNAMIC CHARACTERISTICS		
In-Band Harmonics[1]		
dc to 500kHz Input	dB Below FS (min)	78 (70)
500kHz to 2.5MHz Input	dB Below FS (min)	70 (62)
Conversion Time[2]	ns	195 (±25) + 2 Clock Periods
Conversion Rate[3]	MHz (max)	dc to 5 (5.5)
Effective Aperture Delay Time[4]	ns (max)	4 (±4)
Aperture Uncertainty (Jitter)	ps, rms, max	12 (25)
Signal to Noise Ratio (SNR)[5]		
540kHz Input	dB (min)	67 (65)
2.3MHz Input	db (min)	65 (62)
Transient Response[6]	ns	300
Overvoltage Recovery[7]	ns	500
Input Bandwidth (3dB)[8]	MHz	15
Two-Tone Linearity (@ Input Frequencies)[9]		
(500kHz; 540kHz)	dB Below FS	66
ANALOG INPUT		
Voltage Range[10]		
Operating	V, FS	±1.024 and ±2.048
Maximum Without Damage	V, max	±4
Input Type		Bipolar
Impedance		
2V FS	Ω	1,000
4V FS	Ω	2,000
Offset[11]		
Initial	mV	±2
ENCODE COMMAND INPUT[12]		
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4
	V	"1" = +2.5 to +5.0
Impedance	Ω, min	100k
Rise and Fall Times	ns, max	10
Width		
Min	ns	20
Max	70% of Encode Command Period	
Frequency[13]	MHz	dc to 5
DIGITAL OUTPUT		
Format	Data Bits	12 Parallel, Plus $\overline{\text{MSB}}$; NRZ
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.5
		"1" = +2.5 to +5.0
Drive	LS Loads	10
Time Skew	ns, max	10
Coding		Binary (BIN); 2s Complement (2SC)
DATA READY OUTPUT		
Format	RZ	
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.5
		"1" = +2.5 to +4.0
Drive	LSTTL Loads	10
Rise and Fall Times	ns, max	10
Duration	ns (max)	50 (±10)
POWER REQUREMENTS[14]		
+15V ±2%	mA (max)	130 (150)
−15V ±2%	mA (max)	130 (150)
+5V ±5%	mA (max)	300 (400)
−5.2V ±5%	mA (max)	870 (1,000)
Power Consumption	W (max)	9.9 (11.7)
TEMPERATURE RANGE		
Operating	°C	0 to +70
Storage	°C	−55 to +85
Cooling Air Requirements	LFPM (Linear Feet Per Minute)	500
CONSTRUCTION		
Single Printed Circuit Card		
Including Connectors	Millimeters	167.3 × 100 × 13.13
	Inches	6.59 × 3.93 × 0.517
Board Only	Millimeters	160 × 100 × 1.57
	Inches	6.3 × 3.93 × 0.062

For Applications Assistance, Call Computer Labs Division @ (919) 668-9511.

NOTES

[1] In-Band Harmonics expressed in terms of spurious in-band signals and related harmonics generated at 5MHz encode rate. Minimums shown guaranteed over operating temperature range of 0 to +70°C.
[2] Measured leading edge Encode Command to trailing edge of associated Data Ready; use trailing edge to strobe output data into external circuits.
[3] For word rates below 100kHz, consult factory.
[4] See text for description of Effective Aperture Delay Time.
[5] Rms signal to rms noise ratio minimum are guaranteed over the operating temperature range of 0 to +70°C.
[6] For full-scale step input, 1LSB accuracy attained in specified time.
[7] Recovers to 1LSB accuracy in specified time after 2 × FS input overvoltage.
[8] Input bandwidth flat within 0.2dB, dc to 2.5MHz. Unit is optimized for bandwidth shown; wider bandwidth available on special order. Consult factory for details.
[9] Each input frequency applied at level 7dB below full scale.
[10] Gain is adjustable ±5% with on-board potentiometer.
[11] Adjustable ±15mV without performance degradation.
[12] Transition from digital "0" to digital "1" initiates encoding.
[13] For operation at word rates below 500kHz, consult factory.
[14] ±15V must be equal and opposite within 200mV and track over temperature.

Specifications subject to change without notice.

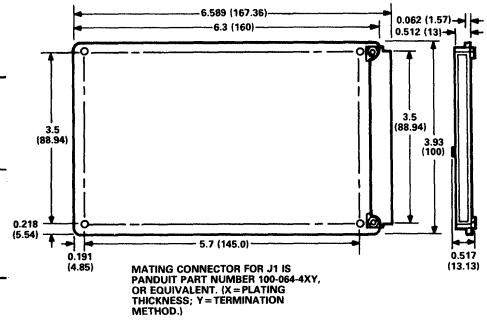
PIN DESIGNATIONS

	ROW A		ROW B
PIN	FUNCTION	PIN	FUNCTION
1	N/C	1	ENCODE COMMAND
2	GROUND	2	GROUND
3	GROUND	3	GROUND
4	GROUND	4	GROUND
5	GROUND	5	GROUND
6	GROUND	6	GROUND
7	GROUND	7	GROUND
8	NO CONNECTION	8	DATA READY
9	GROUND	9	GROUND
10	GROUND	10	GROUND
11	−5.2V	11	−5.2V
12	−5.2V SENSE	12	−5.2V RETURN*
13	+15V	13	+15V
14	+15V SENSE	14	+15V RETURN*
15	−15V	15	−15V
16	−15V SENSE	16	−15V RETURN*
17	+5V	17	+5V
18	+5V SENSE	18	+5V RETURN*
19	GROUND	19	GROUND
20	GROUND	20	BIT 1 (MSB)
21	GROUND	21	$\overline{\text{BIT 1 (MSB)}}$
22	GROUND	22	BIT 2
23	GROUND	23	BIT 3
24	GROUND	24	BIT 4
25	GROUND	25	BIT 5
26	GROUND	26	BIT 6
27	GROUND	27	BIT 7
28	GROUND	28	BIT 8
29	GROUND	29	BIT 9
30	GROUND	30	BIT 10
31	GROUND	31	BIT 11
32	GROUND	32	BIT 12 (LSB)

***CONNECTED INTERNALLY TO GROUND PINS**
ANALOG INPUT IS SMA CONNECTOR LABELED J2

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING CONNECTOR FOR J1 IS PANDUIT PART NUMBER 100-064-4XY, OR EQUIVALENT. (X = PLATING THICKNESS; Y = TERMINATION METHOD.)

ANALOG DEVICES

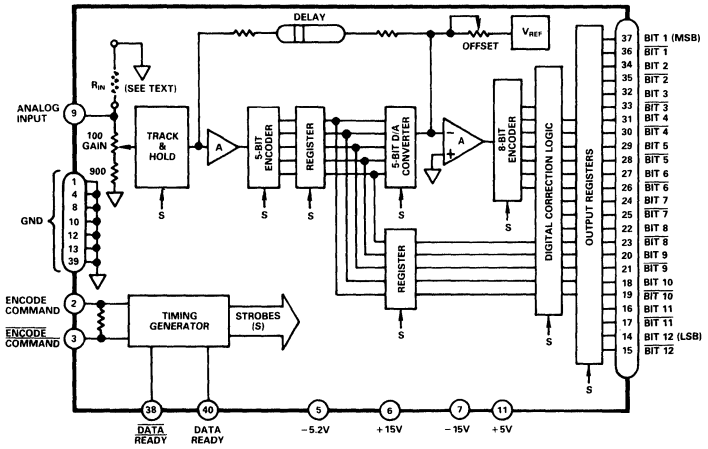
12-Bit Video Analog-to-Digital Converter

CAV-1220

FEATURES
12-Bit Resolution
20MHz Word Rate
Single 35-In² PC Board
ECL Compatible
No External Support Circuits

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Digital Signal Processing
Spectrum Analysis
Transient Analysis

CAV-1220 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices model CAV-1220 A/D converter is an outstanding combination of 12-bit resolution, 20MHz word rates, and small size. The unit is capable of solving a multitude of high-speed digitizing problems. Its design is based on concepts pioneered in the MOD-1020 and MOD-1205 A/D converters; and taken to an even higher level of achievement in the CAV-1210.

It is pin-for-pin compatible with the other units in the MOD and CAV series of A/D converters. But it *doubles* the word rate of its predecessor CAV-1210, making it possible for system designers to offer options or upgrade their high-resolution systems without new layouts.

This remarkable converter includes a track-and-hold, along with encoding and timing circuits. The CAV-1220 is an ideal choice for the designer who needs state-of-the-art performance in high-resolution, ultra-high speed A/D conversion.

For radar applications, 12-bits of resolution increase the dynamic range of the converter, making it possible to detect weaker signals than would be possible with lower resolution characteristics. The high-word rates enhance ranging resolution, thereby increasing system effectiveness.

In imaging applications, the CAV-1220 increases the contrast and/or color resolution of systems in which it is used. Its high-word rates increase spatial resolution; and this combination of high resolution and high speed can materially improve system performance.

All digital inputs and outputs are ECL compatible; optimum analog input impedance can be selected by the user. The unit requires only an encode command and external power supplies for operation. The CAV-1220 is repairable and backed by Analog Devices' limited one-year warranty.

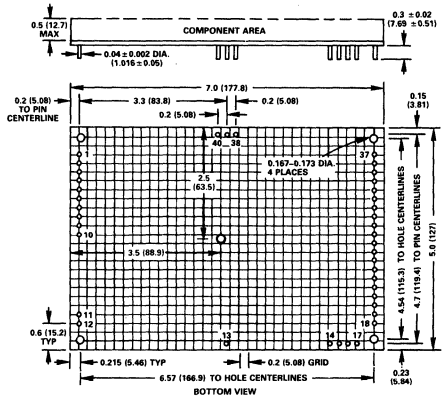
SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	CAV-1220
RESOLUTION (FS = Full Scale)	Bits (% FS)	12 (0.024)
LSB WEIGHT		
2.048V p-p FS	mV	0.5
ACCURACY		
(Including Linearity) @ dc	% FS ± 1/2LSB	0.0125
Monotonicity		Guaranteed
Nonlinearity vs. Temperature	ppm/°C (max)	10 (15)
Offset vs. Temperature	ppm/°C (max)	220 (250)
Gain Error	% FS	2
Adjustable to Zero with On-Card Potentiometer		
Gain vs. Temperature	ppm/°C, max	150
DYNAMIC CHARACTERISTICS		
In-Band Harmonics[1]		
540kHz Input	dB Below FS, min	70
2.3MHz Input	dB Below FS, min	65
9.3MHz Input	dB Below FS, min	50
Conversion Time[2]	ns (max)	1 Clock Period + 155ns (± 10)
Conversion Rate	MHz, max	20
Aperture Uncertainty (Jitter)	ps, rms max	25
Effective Aperture Delay Time[3]	ns (max)	2.5 (± 2.5)
Signal to Noise Ratio (SNR)[4]	dB, (min)	66 (65)
Noise Power Ratio (NPR)[5]	dB	52
Transient Response[6]	ns	100
Overvoltage Recovery[7]	ns	200
Input Bandwidth		
Small Signal, 3dB[8]	MHz	40
Large Signal, 3dB[9]	MHz	35
Two-Tone Linearity (@ Input Frequencies)[10]		
(60kHz; 62kHz)	dB Below FS	70
(2.496MHz; 2.498MHz)	dB below FS	65
(4.996MHz; 4.998MHz)	dB below FS	60
ANALOG INPUT		
Voltage Range[11]		
Operating	V, FS	± 1.024
Maximum Without Damage	V, max	± 2
Input Type		Bipolar
Impedance	Ω	1000
Offset[12]	mV	Adjustable to Zero with On-Card Potentiometer
ENCODE COMMAND INPUT[13]		
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Input)	V	"1" = −0.9
Impedance	Ω, max	100
Rise and Fall Times	ns, max	5
Width		
Min	ns	10
Max	70% of Encode Command Period	
Frequency[14]	MHz	dc to 20
DIGITAL OUTPUT		
Format	Data Bits	12 Parallel; NRZ
	Data Ready and $\overline{\text{Data Ready}}$	2; RZ
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Output)	V	"1" = −0.9
Drive (Line-to-Line)	Ω, min	75
Time Skew	ns, max	5
Coding		Binary (BIN); 2's Complement (2SC)
DATA READY OUTPUT		
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Output)		"1" = −0.9
Drive (Line-to-Line)	Ω, min	75
Rise and Fall Time	ns, max	5
Duration	ns (max)	22 (± 3)
POWER REQUREMENTS[15]		
+15V ± 5%	mA (max)	174 (192)
−15V ± 5%	mA (max)	157 (173)
+5V ± 5%	mA (max)	174 (192)
−5.2V ± 5%	A (max)	2.78 (3.06)
Power Consumption	W (max)	20.3 (22.3)
TEMPERATURE RANGE		
Operating	°C	0 to +70
Storage	°C	−55 to +85
Cooling Air Requirements	LFPM (Linear Feet Per Minute)	500
CONSTRUCTION		
Single Printed Circuit Card	Inches	7.0 × 5.0 × 0.5

For Applications Help, Call Computer Labs Division @ (919) 668-9511.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	40	DATA READY
2	ENCODE COMMAND	39	GROUND
3	$\overline{\text{ENCODE COMMAND}}$	38	$\overline{\text{DATA READY}}$
4	GROUND	37	BIT 1 (MSB)
5	−5.2V	36	$\overline{\text{BIT 1 (MSB)}}$
6	+15V	35	$\overline{\text{BIT 2}}$
7	−15V	34	BIT 2
8	GROUND	33	$\overline{\text{BIT 3}}$
9	ANALOG INPUT	32	BIT 3
10	GROUND	31	BIT 4
11	+5V	30	$\overline{\text{BIT 4}}$
12	GROUND	29	BIT 5
13	GROUND	28	$\overline{\text{BIT 5}}$
14	BIT 12 (LSB)	27	BIT 6
15	$\overline{\text{BIT 12 (LSB)}}$	26	$\overline{\text{BIT 6}}$
16	BIT 11	25	$\overline{\text{BIT 7}}$
17	$\overline{\text{BIT 11}}$	24	BIT 7
18	BIT 10	23	$\overline{\text{BIT 8}}$
19	$\overline{\text{BIT 10}}$	22	BIT 8
20	BIT 9	21	$\overline{\text{BIT 9}}$

NOTES

[1] In-Band Harmonics expressed in terms of spurious in-band signals and harmonics generated at 20MHz encode rate.

[2] Measured from leading edge Encode Command to trailing edge Data Ready; use trailing edge to strobe output data into external circuits (see text).

[3] See text for description of Effective Aperture Delay Time.

[4] Rms signal to rms noise ratio with full-scale 540kHz analog input (see Figure 3).

[5] Dc to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz; and encode rate of 20MHz.

[6] For full-scale step input, 12-bit accuracy attained in specified time.

[7] Recovers to 12-bit accuracy in specified time after 2 × FS input overvoltage.

[8] With analog input 40dB below FS.

[9] With FS analog input. (Large-signal bandwidth flat within 0.2dB, dc to 10MHz).

[10] Both frequencies applied at level 7dB below full scale.

[11] Standard bipolar input is adjustable ± 5% with on-card potentiometer (see text and Figure 2). Unipolar 0 to +2V input range is available on special order; consult factory for details.

[12] Adjustable ± 15mV without performance degradation (see text and Figure 2).

[13] Digital "0" to digital "1" transition initiates encoding.

[14] Encode rate specified by customer; see Ordering Information. Units operated outside ± 10% of specified frequency (up to maximum 20MHz) must be returned to factory for recalibration. For operation at word rates below 500kHz, consult factory.

[15] ± 15V must be equal and opposite within 200mV and track over temperature.

Specifications subject to change without notice.

THEORY OF OPERATION

Refer to the block diagram of the CAV-1220.

Analog input signals to be digitized are applied to a track-and-hold (T/H) amplifier, which is normally operating as a buffer amplifier in the "track" mode, following all changes in analog input as they occur. The user of the CAV-1220 determines the point at which the analog signal is to be digitized by applying an Encode Command.

The leading edge of the ECL-compatible encode command causes the track-and-hold to switch momentarily to the "hold" mode of operation, "freezing" the analog input signal long enough to begin the digitizing process. The instant this switching action occurs is affected by one of the parameters of the CAV-1220, called out as Effective Aperture Delay Time in the Specifications table.

Basically, effective aperture delay time is a measure of the difference between the converter's digital and analog delays (t_d–t_a) and can assume a zero, positive, or negative value depending on the comparative lengths of the two delays. In the CAV-1220, the analog delay (t_a) is less than the digital delay (t_d), and causes effective aperture delay to be typically 2.5ns.

The "held" value of analog signal at the output of the T/H is applied to a 5-bit encoder. It is also applied to an analog delay circuit, whose time delay is equal to the interval required for the first step of the digitizing/reconstruction process.

The digitized signal is applied to a 5-bit D/A converter which has 12-bit accuracy. Via registers, the same digital signal is directed to the digital correction logic circuits. The stored data will represent Bits 1–5 of the 12-bit digital output of the CAV-1220.

The reconstructed output of the D/A converter becomes one input to an operational amplifier; its other input is the delayed analog signal from the delay line. The output of the wideband, fast-settling op amp represents the residue which remains after a 5-bit digital representation of the analog input has been subtracted from that input.

This residue, or error, signal is encoded by a second encoder and is applied as 8-bit digital information to the digital correction logic circuits which contain Bits 1–5.

The correction circuits combine the 5-bit and 8-bit bytes of data to compensate for possible nonlinearities and other errors to assure the final 12-bit output of the CAV-1220 is 12-bit accurate.

Expressed in its simplest terms, the digital correction logic circuits use the information in the 8-bit signal to determine what modifications of Bits 1-5 may be necessary. The value of the MSB in the 8-bit byte establishes whether the 5-bit data are passed "as is" or whether they are increased by a value of binary "1". The remaining bits (2-8) of the 8-bit byte become Bits 6-12 of the CAV-1220 digital output.

Digitally corrected subranging (DCS), the innovative technique described here, helps compensate for a wide range of potential errors which could otherwise be avoided only if the CAV-1220 design included expensive, high precision components.

The use of 13 bits to obtain an accurate 12 bits of output cannot prevent gain error, track/hold droop error, linearity error, offset error, or any of the other inherent characteristics of "real-world" A/D converters. But DCS can, and does, help nullify their effects and makes it economically feasible to accomplish high-speed, high-resolution digitizing of analog signals.

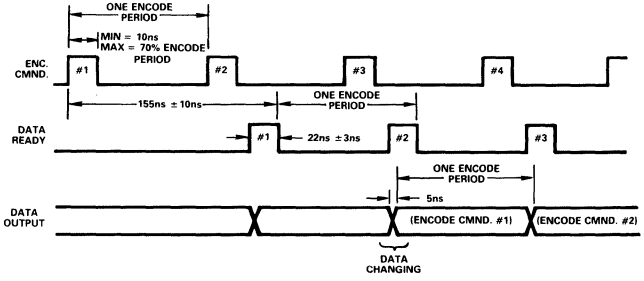


Figure 1. CAV-1220 Timing Diagram

CAV-1220 TIMING

Refer to Figure 1, the CAV-1220 Timing Diagram.

The intervals shown represent a continuous update rate of approximately 10MHz, which is considerably below the maximum capabilities of the CAV-1220. But that frequency helps illustrate the "pipeline delay" characteristic of the converter.

At this word rate, spacing between encode commands is approximately 100 nanoseconds; and three encode commands have occurred before the data associated with the first command are valid. In Figure 1, this pipeline delay has a total time of approximately 255 nanoseconds (155ns + 100ns). This interval will be different at other word rates, but will always include 155ns; depending upon the update rate, either more or fewer encode commands may occur before the first data are available.

After the initial delay, valid data will be available at the word rate dictated by encode commands. Note the spacing between Encode Command #1 and Encode Command #2 is equal to one encode period. This is the same spacing as that between Data Ready #1 and Data Ready #2; and is also the spacing between the first and second groups of valid data.

System timing can be adjusted as necessary to take into account the pipeline delay effects and assure that the data of interest are strobed out of the converter at the appropriate time.

Figure 1 also illustrates why the trailing edge of the Data Ready pulse is recommended as the strobe for output data. Typically, data begin changing 5ns after the leading (rising) edge of each Data Ready pulse; they will be fully settled at the time of the trailing (falling) edge and available for use in external circuits.

Another possibility for strobing the output data is to use the $\overline{\text{DATA READY}}$ pulse. Its leading edge occurs at the same time as the trailing edge of the DATA READY signal, but is a rising edge, which may facilitate its use as a strobe.

ANALOG INPUT IMPEDANCE

Refer again to the block diagram of the CAV-1220 and note the resistor shown in dashed lines and designated as R_{IN}.

This resistor value is chosen by the user to allow the analog input impedance of the CAV-1220 to be matched to the characteristic impedance of the analog signal source.

Without an added resistor, the input impedance of the unit is 1,000Ω; this is the series total of the GAIN control and the 900Ω resistor shown in the block diagram.

When a resistor is added, it is in parallel with the internal impedance of the CAV-1220; various values of resistors can be used to obtain standard impedances:

Desired Input Impedance	Value for R_{IN}
50 ohms	52.3 ohms
75 ohms	80.6 ohms
93 ohms	102 ohms
100 ohms	110 ohms

For an input impedance (Z) different from those shown above, the correct resistor value can be established with the equation:

$$\frac{1}{R_{IN}} = \frac{1}{Z} - \frac{1}{1k}$$

The physical location of R_{IN} is shown in Figure 2.

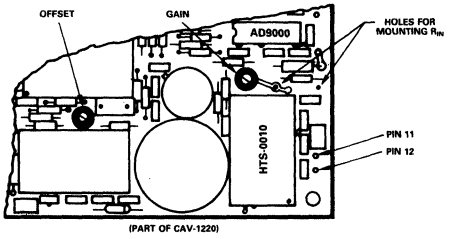


Figure 2. CAV-1220 Adjustment Controls

OFFSET AND GAIN ADJUSTMENTS

The design and manufacture of the CAV-1220 A/D converter are innovative and precise, and have resulted in a high-performance converter which is virtually adjustment-free. This elimination of variable controls helps make the unit less susceptible to performance degradation caused by vibration, shock, or inadvertent and/or incorrect adjustment.

Despite the complexity of the circuits required to obtain high-resolution digitizing at high speeds, there are only two control settings used in the unit. Factory adjustments during final calibration use selected fixed resistors to assure optimum performance without a need for "tweaking" by the user.

Only OFFSET and GAIN controls are available, and even these are sealed at the factory before shipment. In those rare instances where they may require readjustment, the procedure outlined below is one which should be used.

Refer to Figure 2, the CAV-1220 Adjustment Controls.

When adjusting offset and gain of the CAV-1220 in the system, the OFFSET control should be adjusted first. The adjustment sequence is:

1. Apply to the analog input a precise (±0.25mV) dc level corresponding to midscale of the desired input range. (For standard units with ±1V range, this is 0V input.)
2. Adjust OFFSET control while observing MSB (Bit 1); adjust for MSB "toggling" between digital "0" and digital "1".
3. Apply a precise (±0.25mV) dc level corresponding to the most negative excursion of the desired input range. (For standard units, this is −1V input.)
4. Adjust GAIN control while observing LSB (Bit 12); adjust for output of Bits 1–11 solid "0" with LSB "toggling".
5. Apply a precise (±0.25mV) dc level corresponding to the most positive excursion of the desired input range. (For standard units, this is +1V input.)
6. Check digital output to assure Bits 1–11 are solid "1" with LSB "toggling".
7. Adjust OFFSET and GAIN controls alternately as necessary to obtain analog input range to tolerance of ±1/2LSB.

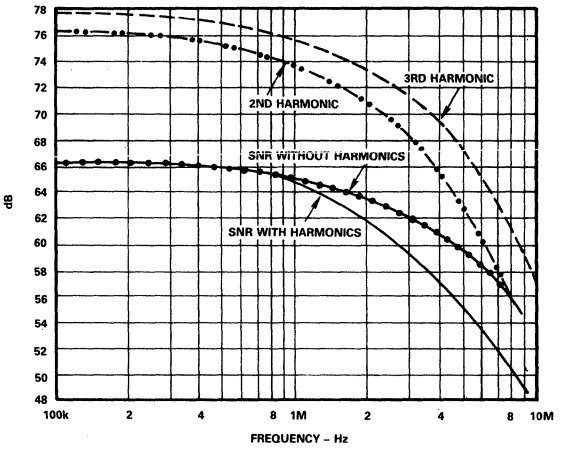


Figure 3. CAV-1220 SNR and Harmonics

DYNAMIC PERFORMANCE

Figure 3 shows typical performance on some of the dynamic characteristics which play an important role in the performance of systems using the CAV-1220 A/D converter.

The A/D was calibrated in final test for an encode rate of 20MHz. As shown, signal-to-noise ratio (SNR) with harmonics is typically 66dB at an input frequency of 100kHz; and remains greater than 50dB for full-scale inputs of 8MHz. As expected, SNR without harmonics is better and is typically 56dB at 8MHz.

The level of 2nd and 3rd harmonics at a word rate of 20MHz is also depicted; in these characteristics, too, the CAV-1220 displays exceptional performance.

ORDERING INFORMATION

For standard CAV-1220 units, order by model number CAV-1220-XXX; XXX is specified by the customer to indicate the desired optimized word rate. The decimal place is assumed (but not shown) between the second and third places. CAV-1220-150, for example, indicates final calibration and optimum performance at 15MHz.

Optimum performance will be achieved within a band of frequencies approximately ±10% around the selected word rate; but the maximum rate of 20MHz must be considered. If later applications require word rates beyond the limits of the original optimum frequency, the unit must be returned to the factory for calibration; there is a nominal charge for this service.

Mating sockets for the CAV-1220 converters are model number MSB-2 (thru hole) or MSB-3 (closed end). These are individual solder-type pin sockets for mounting the A/D on PC boards.

ANALOG DEVICES

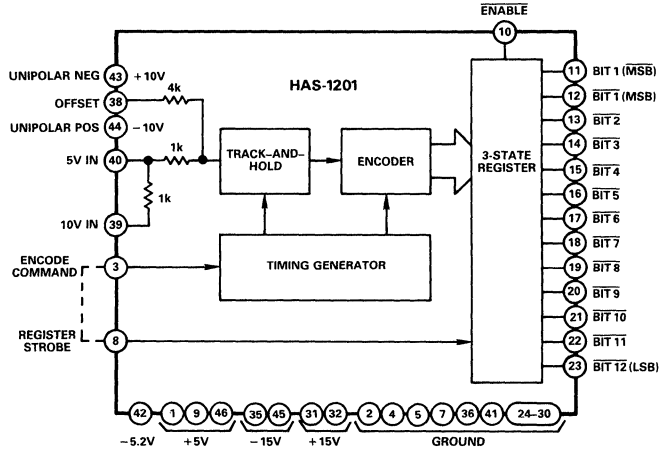
12-Bit, 1MHz Analog-to-Digital Converter

HAS-1201

FEATURES
12-Bit Resolution
1MHz Word Rate
T/H and Timing Circuits Included
Single Hybrid Package

APPLICATIONS
Radar Systems
Medical Instrumentation
Electro-Optics Systems
Test Systems
Digital Oscilloscopes

HAS-1201 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The HAS-1201 A/D Converter combines high resolution and speed in a single hybrid package. This is a *complete* 12-bit, 1MHz unit which includes a track-and-hold and timing circuits. It's a total solution for the system designer who needs to perform the entire analog-to-digital conversion function in the smallest possible space.

This remarkable converter is a full answer to the question of digitizing analog signals into high-resolution data outputs and doing it in the most cost-effective way. The HAS-1201 is the ideal choice for the designer who needs state-of-the-art performance in high-resolution, high-speed A/D conversion.

Full-scale analog inputs are 5 or 10 volts; and the unit can operate with either bipolar or unipolar ranges. Analog input impedance is 1,000 ohms or 2,000 ohms and the three-state digital outputs are TTL compatible. The user needs to supply only an encode command and external power supplies for operation.

All models of the HAS-1201 A/D Converter are housed in 46-pin metal hybrid packages. The HAS-1201KM operates over a temperature range of 0 to +70°C. The HAS-1201SM is rated over an operating temperature range of −25°C to +85°C, but will operate with derated performance over a range of −55°C to +100°C. For units operating from −25°C to +85°C and military screening, order HAS-1201SMB; contact the factory for details about derated performance and military screening.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HAS-1201KM	HAS-1201SM/SMB
RESOLUTION (FS = Full Scale)	Bits	12	*
	% FS	0.025	*
ACCURACY			
Gain	% FS	±3	*
Gain vs. Temperature	ppm/°C	80	*
Linearity @ dc	% FS ± 1/2LSB	0.0125	*
Diff. Nonlinearity vs. Temp.	ppm/°C	10	15
Monotonicity		Guaranteed	*
DYNAMIC CHARACTERISTICS			
In-Band Harmonics[1]			
(dc to 100kHz)	dB below FS (min)	80 (75)	*
(100kHz to 500kHz)	dB below FS	75	*
Conversion Rate	MHz, max	1.05	1.00
Conversion Time[2]	ns, max	950	*
Over Temperature	ns, max	950	1000
Aperture Uncertainty (Jitter)	ps, rms	30	*
Aperture Time (Delay)	ns	25	*
Signal-to Noise Ratio (SNR)[3]	dB (min)	68 (65)	*
Transient Response[4]	ns (max)	600 (1000)	*
Overvoltage Recovery[5]	ns	1000	*
Input Bandwidth			
Small Signal, −3dB[6]	MHz	2	*
Large Signal, −3dB[7]	MHz	2	*
Two-Tone Linearity (@ input frequencies			
(75kHz; 105kHz)	dB below FS	80	*
ANALOG INPUT			
Voltage Ranges	V, p-p FS	5.0/10.0	*
	V, max	±15	*
Impedance (5V/10V Input)	Ω (max)	1000/2000 (±1%)	*
Bipolar Offset[8]			
Initial (5V Input)	mV (max)	±2 (±10)	*
vs. Temperature	FS ppm/°C (max)	50 (200)	*
DIGITAL INPUTS			
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
	V	"1" = +2.4 to +5	*
Impedance	LS TTL Loads	3	*
Rise and Fall Times	ns, max	10	*
Frequency	MHz, max	1.05	1.00
Encode Command Width[9]			
Min	ns	50	*
Max	ns	Encode Period − 350ns	*
Register Strobe Width			
Min	ns	50	*
Max	ns	Encode Period − 350ns	*
$\overline{\text{Enable}}$ Width			
Min	ns	100	*
DIGITAL OUTPUTS			
Format	Bit 1, $\overline{\text{Bit 1}}$ − $\overline{\text{Bit 12}}$	3-State; NRZ	*
Logic Levels, TTL-Compatible[10]	V	"0" = 0 to +0.5	*
		"1" = +2.4 to +5	*
Drive	TTL Loads	1	*
Time Skew	ns, max	10	*
Delay: Register Strobe to			
Output Data Validity	ns	30	*
Coding		Complementary Binary (CBIN)	*
		Complementary Offset Binary (COB)	*
		Complementary 2's Complement (C2SC)	*
POWER REQUIREMENTS			
+15V ±5%	mA (max)	55 (70)	*
−15V ±5%	mA (max)	65 (80)	*
+5V ±5%	mA (max)	195 (235)	*
−5.2V ±5%	mA (max)	35 (40)	*
Power Consumption	W (max)	3.0 (3.6)	*
TEMPERATURE RANGE[11]			
Operating	°C	0 to +70	−25 to +85
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[12]			
Junction to Air, θja (Free Air)	°C/W	12	*
Junction to Case, θjc	°C/W	2.5	*
PACKAGE OPTION[13]			
M-46		HAS-1201KM	HAS-1201SM HAS1201SMB

For applications assistance, phone Computer Labs Division at (919) 668-9511

HAS-1201 PIN DESIGNATION

PIN	FUNCTION	PIN	FUNCTION
46	+5V	1	+5V
45	−15V	2	GROUND
44	UNIPOLAR POSITIVE	3	ENCODE COMMAND
43	UNIPOLAR NEGATIVE	4	GROUND
42	−5.2V	5	GROUND
41	GROUND	6	DO NOT CONNECT*
40	5V RANGE IN	7	GROUND
39	10V RANGE IN	8	REGISTER STROBE
38	OFFSET	9	+5V
37	DO NOT CONNECT*	10	$\overline{\text{ENABLE}}$
36	GROUND	11	BIT 1 ($\overline{\text{MSB}}$)
35	−15V	12	$\overline{\text{BIT 1}}$ (MSB)
34	NO CONNECTION	13	$\overline{\text{BIT 2}}$
33	NO CONNECTION	14	$\overline{\text{BIT 3}}$
32	+15V	15	$\overline{\text{BIT 4}}$
31	+15V	16	$\overline{\text{BIT 5}}$
30	GROUND	17	$\overline{\text{BIT 6}}$
29	GROUND	18	$\overline{\text{BIT 7}}$
28	GROUND	19	$\overline{\text{BIT 8}}$
27	GROUND	20	$\overline{\text{BIT 9}}$
26	GROUND	21	$\overline{\text{BIT 10}}$
25	GROUND	22	$\overline{\text{BIT 11}}$
24	GROUND	23	$\overline{\text{BIT 12}}$ (LSB)

NOTE:
PINS 2, 4, 5, 7, 24-30, 36 and 41 NEED TO BE CONNECTED TO THE SAME COMMON GROUND AS CLOSE TO CASE AS POSSIBLE. POWER SUPPLY VOLTAGES NEED TO BE CONNECTED TO ALL DESIGNATED PINS.
***FOR FACTORY USE ONLY.**

NOTES
[1]In-Band Harmonics expressed in terms of spurious in-band signals generated at 1MHz encode rate at analog inputs shown in ( ).
[2]Measured from leading edge of Encode Command to time associated data are valid.
[3]RMS signal to rms noise ratio with 100kHz analog input.
[4]For full-scale step input, 12-bit accuracy attained in specified time.
[5]Recovers to specified performance in specified time after 2 × FS input overvoltage.
[6]With analog input 40dB below FS.
[7]With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 500kHz.)
[8]Externally adjustable to zero.
[9]Transition from digital "0" to digital "1" initiates encoding.
[10]Output data are TTL-compatible when analog input is within specified range. Negative over-voltage inputs cause tri-state output to drift to "high" condition and may create erroneous output (see text).
[11]Case Temperature. Models HAS-1201SM/SMB will operate with derated performance over temperature range of −55°C to +100°C; contact factory for details.
[12]Maximum junction temperature is +150°C.
[13]See Section 14 for package outline information.

Specifications subject to change without notice.

THEORY OF OPERATION

Refer to the block diagram of the HAS-1201 A/D Converter.

This is a functional illustration of the HAS-1201 A/D Converter. Internally, the converter uses digitally corrected subranging (DCS) pioneered by Analog Devices to generate 14 bits of digital data. The two extra bits are used for digital correction to assure that the 12 bits of parallel output data are an accurate representation of the analog input signal present at the time of the encode command.

The analog signal to be digitized is applied to an internal track-and-hold (T/H), whose change between the "track" and "hold" modes is determined by the HAS-1201 internal timing circuits. Applying an encode command (at Pin 3) triggers these circuits and causes the required timing signals to be generated.

Timing intervals for the various signals involved in the operation of the HAS-1201 A/D Converter are shown in Figure 1.

Understanding the operation of the HAS-1201 is easiest when the timing of events is related to the leading edge of the Encode Command. Minimum width of that signal is 50ns; maximum width is the period of the encode rate less 350ns. A square wave is always an acceptable encode signal for the HAS-1201 converter.

For purposes of illustration, spacing between Encode Commands #1 and #2 in Figure 1 is approximately equal to a word rate of 500kHz.

When the encode command is applied, the unit switches to the hold mode for approximately 670 nanoseconds; the length of the track mode is a function of word rate. When operated at its maximum frequency, the HAS-1201 will remain in "track" 280 nanoseconds, the interval required for internal processing of data.

During the first 50 nanoseconds of each hold period, valid data resulting from the previous encode command continue to be applied to the output register. But then, internal switching within the HAS-1201 causes changes to occur until the conversion cycle initiated by the most recent encode command is completed.

Referenced to the leading edge of the encode command, minimum spacing on the Register Strobe is 950ns; maximum spacing is shown with the Register Strobe in dotted lines.

Output data at Pins 11-23 remain valid until updated by a Register Strobe. As noted, this validity interval is based on having the $\overline{\text{ENABLE}}$ connected to either digital "0" or ground.

In Figure 1, the timing of the signals labeled $\overline{\text{ENABLE}}$ and OUTPUT DATA are not referenced to the ENCODE COMMAND; their timing is related only to each other.

If the $\overline{\text{ENABLE}}$ pulse is used to strobe output data into external circuits, the user must assure its arrival corresponds to the availability of valid data. When the $\overline{\text{ENABLE}}$ is at digital "1", output data present a high impedance to external circuits. Changing $\overline{\text{ENABLE}}$ to a digital "0" causes the three-state logic outputs to become low impedances and makes them available for strobing.

In the block diagram, the external connection of the encode command (Pin 3) to the register strobe (Pin 8) is the connection which might be used if the HAS-1201 were operating at a continuous maximum encode rate of 1.05MHz. Under these circumstances, the output data resulting from Encode Command #1 will be strobed out of the converter with the leading edge of Encode Command #2.

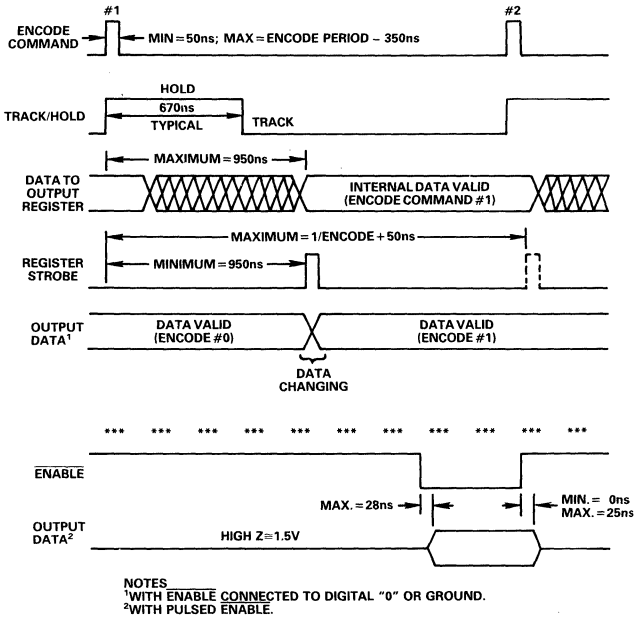


Figure 1. HAS-1201 Timing Diagram

OPERATING HAS-1201 AT WORD RATES LESS THAN MAXIMUM

If encode commands are applied asynchronously, direct connection of these pins results in variations in the times when output data are available, because of pipeline delay through the converter and the differences in intervals between encode commands.

With Pins 3 and 8 connected, the leading edge of each encode command is the signal which strobes output data generated by the *preceding* encode command. There is no separate, designated output signal indicating data are valid.

As an example, assume the HAS-1201 encode rate varies around 500kHz, but with relatively large differences in the times between encode commands. Under these conditions, the availability of output data will vary; it is often preferable to have outputs available a specified interval after each encode command. A method to achieve this is shown in Figure 2.

The insertion of a delay circuit between the encode command input and the strobe input of the HAS-1201 makes it possible to use each digital output word at a precise time after its associated encode command, even when operating the converter asynchronously.

The delay circuit can take any of several forms. The user may opt to use a fixed delay line with a delay of 950ns or more; in other cases, shift registers could be used. Another possibility is a variable delay, such as multivibrators, adjusted to the optimum delay for each application.

In this latter approach, the period of the multivibrators can be set to any desired time between a minimum of 950ns (the period of 1.05MHz) and a maximum determined by the period of the highest word rate to be used.

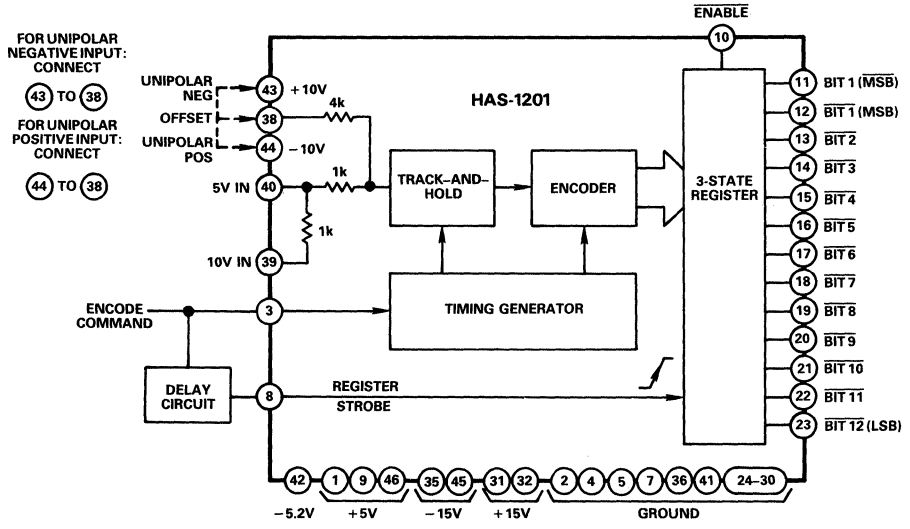


Figure 2. HAS-1201 Connection Diagram

CONNECTING HAS-1201 A/D CONVERTER

At the analog input, the user connects offset (Pin 38) externally to either Pin 43 or Pin 44 to obtain, respectively, unipolar negative or unipolar positive input ranging. The analog signal to be digitized is applied to Pin 39, the 10V input; or to Pin 40, the 5V input, depending upon the application. Examples are shown in Figures 3A-3G.

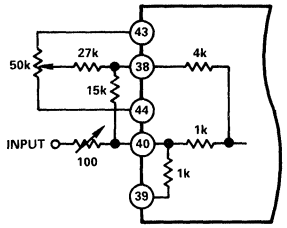


Figure 3A

5V FS Bipolar input
Gain adjustment ± 5% FS
Offset adjustment ± 5% FS
(Adjust offset first)

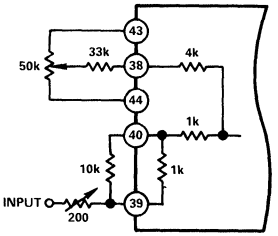


Figure 3B

10V FS Bipolar input
Gain adjustment ± 5% FS
Offset adjustment ± 5% FS
(Adjust offset first)

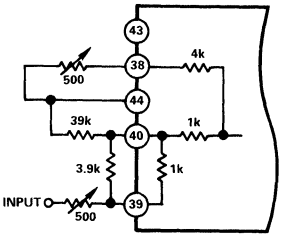


Figure 3C

10V FS Unipolar Positive input
Gain adjustment ± 10% FS
Offset adjustment ± 5%
(Adjust gain first)

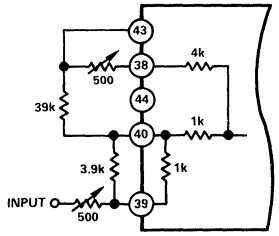


Figure 3D

10V FS Unipolar Negative input
Gain adjustment ± 10% FS
Offset adjustment ± 5%
(Adjust gain first)

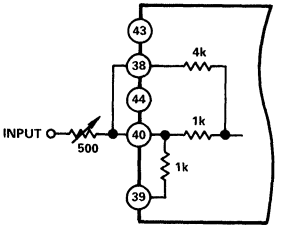


Figure 3E

5V FS Bipolar input
Gain adjustment ± 20% FS
No Offset adjustment

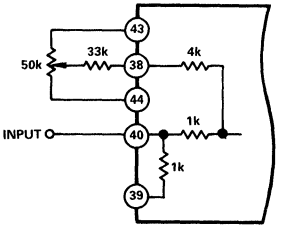


Figure 3F

5V FS Bipolar input
No Gain adjustment
Offset adjustment ± 5% FS

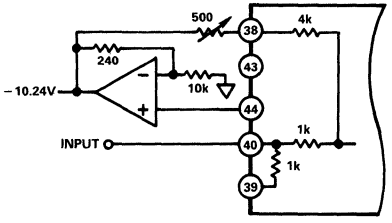


Figure 3G

5V Unipolar Positive input
Offset adjustment ± 5%
No Gain adjustment
(see text)

In Figure 3G, the recommended operational amplifier is an AD741. For 5V Unipolar Negative inputs using this circuit, connect Pin 43 to the positive input of the op amp and leave Pin 44 open.

Various input ranges with fixed gain and offset are shown in Table I.

INPUT RANGE	CONNECT PINS	INPUT PIN
10V Bipolar	None	39
10V Uni. Pos.	38 to 44	39
10V Uni. Neg.	38 to 43	39
5V Bipolar	None	40
5V Uni. Pos.	38 to 44	40
5V Uni. Neg.	38 to 43	40
4V Bipolar (800 ohms impedance)	38 to 40	40

Table I.

Regardless of the input connection being used, certain basic rules of layout should be observed for any high-speed circuit; this is particularly important for high-resolution devices such as the HAS-1201.

Bypass capacitors are used internally, but all power supplies should be bypassed externally, with 0.01μF–0.1μF ceramic capacitors. Electrolytic capacitors of 10-22 microfarads should also be used on each supply; all capacitors should be connected as closely as possible to the supply pins.

A massive ground plane, careful component layout, and physically separating analog and digital signals are among other requirements for assuring the high-speed, high-resolution characteristics of the HAS-1201 A/D Converter.

Supply voltages must be applied to all pins for which they are designated. It is also extremely important to connect all grounds together, and to a solid, low-impedance ground plane.

Cooling air should be passed over the unit when it is being operated; it should be supplied at 300-500 linear feet per minute (LFPM).

The $\overline{\text{ENABLE}}$ signal at Pin 10 can be used for connecting the three-state logic outputs of the HAS-1201 to a bus. A logic "1" at this pin makes the logic outputs "float" at approximately 1.5 volts and causes them to be high impedances during the time other signals are applied to the computer or microprocessor bus.

If the HAS-1201 is not connected to a bus, i.e., it is being used as a system A/D, the $\overline{\text{ENABLE}}$ pin should be connected to logic "0" or ground.

When using the unit as a (free-standing) system A/D, the user should keep in mind the output characteristic noted in the footnotes of the Specifications table on Page 2 of this data sheet.

As a negative-going analog input is increased in value, the digital output of the HAS-1201 follows the changes until all outputs are at logic "1" (unit is operating with Complementary Offset Binary logic), indicating maximum negative analog input. Any further increase in negative input (overranging) will cause the tri-state digital outputs to "float".

The exception to this is the Bit 1 ($\overline{\text{MSB}}$) at Pin 11. Internal pulldown resistors cause it to go to logic "0" and remain.

When they are in an overrange condition, the digital outputs need to look "high". This means the load on the output must pull the open circuits to the "high" state; this requirement normally presents no problem when driving standard TTL or Schottky TTL inputs.

When driving low-power Schottky inputs, the change to "high" will have a slower rise time; it may require up to 100ns. For these, the user should avoid clocking the output data too soon.

CMOS circuits have no provision for pulling up the converter's outputs. In this situation, the recommended procedure is to use 2k pull-up resistors connected to +5 volts.

TESTING HAS-1201 PERFORMANCE

Sophisticated converters of the type represented by the HAS-1201 A/D Converter require sophisticated testing to assure they meet or exceed their specified performance parameters. One of these test methods is a Fast Fourier Transform (FFT) analysis of the converter output.

The results of that testing are shown in Figure 4.

This diagram is an average analysis, based on ten readings. In the test, a 104kHz sine wave is applied as the analog input (f_o), at a level of 1dB below full scale; the HAS-1201 is operated at a word rate of 1.05MHz.

The FFT is based on 512 sample points, with Hanning weighting applied to the digital representations of the analog samples. The resulting spectrum demonstrates the exceptional performance of the converter, particularly in terms of low noise and harmonic distortion.

In Figure 4, the vertical scale is based on a full-scale input referenced as 0dB. In this way, all (frequency) energy cells can be calculated with respect to full-scale rms inputs.

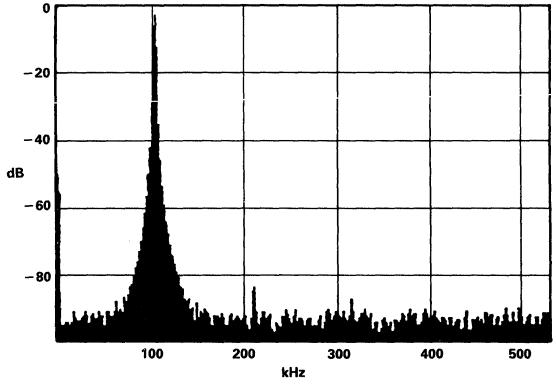


Figure 4. HAS-1201 Output Fast Fourier Transform

Besides the plot shown, the computer testing also supplies numerical data stipulating the precise readings of the second and third harmonics; and the signal-to-noise ratio (SNR). These numbers have been replaced by a horizontal frequency scale for purposes of illustration.

The original numbers indicated the peak amplitude of the second harmonic (208kHz) was at a level of −81dB; the third harmonic (312kHz) was at −85dB. The signal-to-noise ratio was measured at 67.5dB, which corresponds to a noise floor of −68.5dB. All of these numbers, like the plot, are 10-run averages of 512 sample points in each run.

The harmonic distortion numbers include five energy cells on either side of the harmonics of $2 \times f_o$, and $3 \times f_o$. Including these cells helps negate the effects of side lobes caused by the Hanning weighting and non-coherent sampling used for testing.

Hanning, or cosine, weighting is one of several methods of generating FFT data; each method has certain characteristics which make it more or less appropriate for various applications.

ORDERING INFORMATION

Three models of the HAS-1201 A/D Converter are available. For commercial operating temperatures between 0 and +70°C, order model number HAS-1201KM. The HAS-1201SM is rated over an operating temperature range of −25°C to +85°C, but will operate with derated performance over a range of −55°C to +100°C. For units operating from −25°C to +85°C and military screening, order HAS-1201SMB; contact the factory for details about derated performance and military screening.

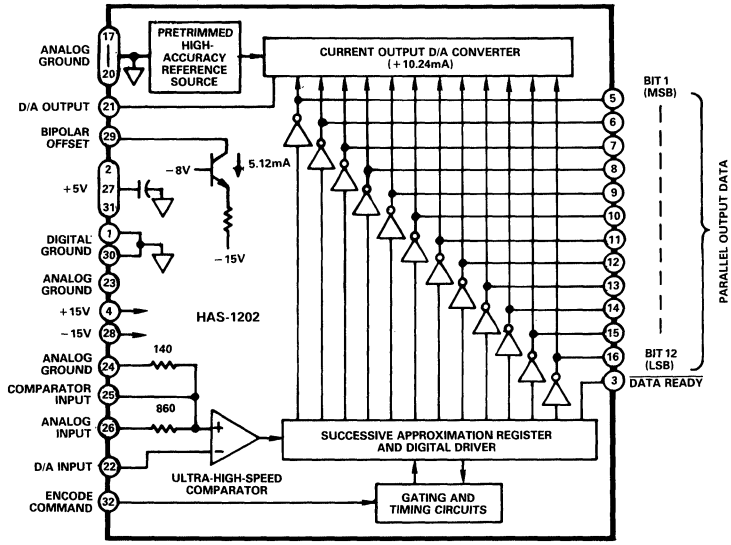
Ultrafast Hybrid Analog-to-Digital Converters

HAS-1202/HAS-1202A

FEATURES
Conversion Time of 1.56μs (HAS-1202A)
12-Bit Resolution
Conversion Rates to 641kHz
Adjustment-Free Operation

APPLICATIONS
Waveform Analysis
Fast Fourier Transforms
Radar Systems

HAS-1202 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HAS-1202 and improved HAS-1202A A/D converters are thick-film hybrid 12-bit converters housed in 32-pin ceramic or metal DIP packages. They can be used with high-performance track-and-hold (T/H) amplifiers to solve high-speed, high-resolution digitizing problems economically and feature conversion times of 2.86μs (HAS-1202) and 1.56μs (HAS-1202A).

These converters and the Analog Devices Model HTC-0300A T/H offer designers an opportunity to go from analog to digital with savings in power, board space, design time, and component costs.

They are ideally suited for applications which require excellent performance with a minimum of adjustments. Included in these potential uses are radar systems, PCM, data acquisition systems, and digital signal processing (DSP) systems of various kinds.

The HAS-1202 and HAS-1202A are rated over an operating temperature range of 0 to +70°C and are packaged in 32-pin DIP ceramic housings. The HAS-1202M and HAS-1202AM are rated over a range of −55°C to +85°C and are packaged in metal cases. For metal case units with an operating range of −55°C to +100°C and military screening, order part numbers HAS-1202MB or HAS-1202AMB. Their performance characteristics are identical except for differences in conversion rates; the HAS-1202 is specified for a maximum rate of 349kHz, while the HAS-1202A is capable of operating up to 641kHz.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

		HAS-1202A	HAS-1202
MAXIMUM RATINGS			
Positive Supply (Pin 4)		+16VDC	*
Negative Supply (Pin 28)		−16VDC	*
Logic Supply (Pins 2, 27, 31)		+7VDC	*
Analog Input (Pin 26)		20V	*
Logic Input (Encode Command @ Pin 32)		+7V	*
Temperature			
Operating (Case)		−55°C to +100°C	*
Storage		−55°C to +125°C	*
Parameter	**Units**	**HAS-1202A**	**HAS-1202**
RESOLUTION (FS = Full Scale)	Bits (%FS)	12 (0.025)	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT	mV	2.5	*
ACCURACY			
Monotonicity		Guaranteed	*
Integral Nonlinearity	LSB	±1/2	*
Differential Nonlinearity	LSB	±1/2	*
Nonlinearity vs. Temperature	ppm/°C	3.5	*
Gain Error	%FS, max	0.08 (0.18)	*
Gain vs. Temperature	ppm/°C	60	*
Gain vs. Power Supply Changes	ppm/mV	2.2	*
DYNAMIC CHARACTERISTICS			
Conversion Rate	kHz, max	641	349
Conversion Time[1]	µs, max	1.56	2.86
vs. Temperature	%/°C	0.08	*
ANALOG INPUT			
Voltage Ranges			
Bipolar	V	±5.12	*
Unipolar	V	0 to +10.24	*
Overvoltage	V, max	20	*
Impedance	Ω, max	1,000 (±20)	*
Offset[2]			
Initial	mV, max	7 (38)	*
vs. Temperature			
Unipolar Input	ppm/°C	7	*
Bipolar Input	ppm/°C	35	*
ENCODE COMMAND INPUT[3]			
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
		"1" = +2.4 to +5	*
Impedance	TTL Loads	1 "S" and 1 "LS"	*
Rise and Fall Times	ns, max	10	*
Width			
Min	ns	50	*
Frequency	kHz	dc to 641	dc to 349
DIGITAL OUTPUT			
Format	Data Bits	12 Parallel; NRZ	
	$\overline{\text{Data Ready}}$	1; RZ	*
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
		"1" = +2.4 to +5	*
Drive	TTL Loads	5 Standard	*
Coding		Binary (BIN) Offset Bin. (OBN)	
POWER REQUIREMENTS			
+15V ±0.5V	mA (max)	48 (60)	*
−15V ±0.5V	mA (max)	30 (46)	*
+5V ±0.25V	mA (max)	150 (232)	*
Power Dissipation	W, max	1.9 (2.75)	*
TEMPERATURE RANGE[4]			
Operating	°C	0 to +70	*
NOTE: For operating range of −25°C to +85°C, specify HAS-1202M or HAS-1202AM; for operating range of −55°C to +100°C and military screening, specify HAS-1202MB or HAS-1202AMB.			
THERMAL RESISTANCE[5]			
Junction to Air, θ_{JA} (Free Air)	°C/W	38	*
Junction to Case, θ_{JC}	°C/W	18	*
PACKAGE OPTION[6]			
M-32		HAS-1202A	HAS-1202

For applications assistance, call Computer Labs Division @ (919) 668-9511.

NOTES
*Specifications same as HAS-1202A.
[1]Measured from leading edge of Encode Command to trailing edge of Data Ready with 50ns encode pulse. Conversion time increases equally with increasing width of Encode Command.
[2]Externally adjustable to zero.
[3]Transition from digital "0" to digital "1" initiates encoding.
[4]Case temperature. Metal case HAS-1202M/HAS-1202AM have operating ranges of −25°C to +85°C; HAS-1202MB/HAS-1202AMB have operating ranges of −55°C to +100°C and military screening.
[5]Maximum junction temperature = 150°C.
[6]See Section 14 for package outline information.

Specifications subject to change without notice.

HAS-1202/HAS-1202A PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
32	ENCODE COMMAND	1	DIGITAL GROUND
31	+5V	2	$\overline{\text{+5V}}$
30	DIGITAL GROUND	3	$\overline{\text{DATA READY}}$
29	BIPOLAR OFFSET	4	+15V
28	−15V	5	BIT 1 (MSB)
27	+5V	6	BIT 2
26	ANALOG INPUT	7	BIT 3
25	COMPARATOR INPUT	8	BIT 4
24	ANALOG GROUND	9	BIT 5
23	ANALOG GROUND	10	BIT 6
22	D/A INPUT	11	BIT 7
21	D/A OUTPUT	12	BIT 8
20	ANALOG GROUND	13	BIT 9
19	ANALOG GROUND	14	BIT 10
18	ANALOG GROUND	15	BIT 11
17	ANALOG GROUND	16	BIT 12

NOTE
Analog Ground (Pins 17-20; 23; 24) and Digital Ground (Pins 1 and 30) Are Electrically Independent of Each Other. Connect Together Externally and to Low-Impedance Ground Plane as Close to Device as Possible.

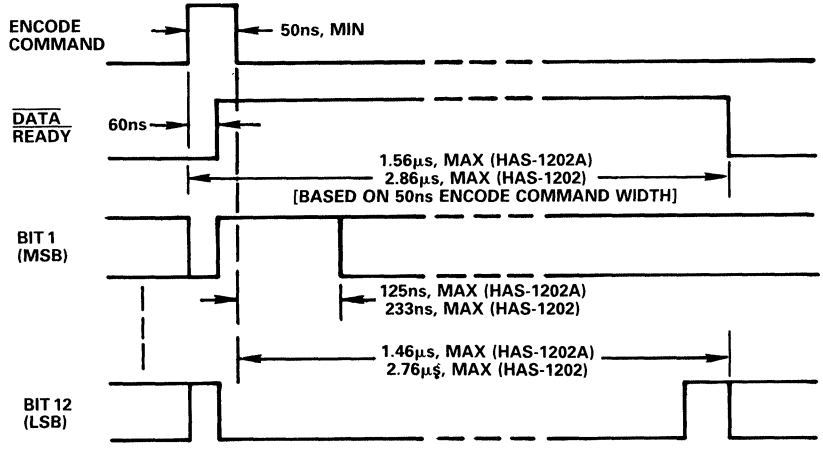


Figure 1. HAS-1202/1202A Timing Diagram

HAS-1202 TIMING

Refer to Figure 1, HAS-1202/1202A Timing Diagram.

The TTL-compatible Encode Command pulse (applied to Pin 32) has a minimum width of 50 nanoseconds. As the width of the Encode Command is increased from this minimum, the width of the Data Ready pulse (and the conversion time) is increased by an equal amount. For the HAS-1202, maximum encode frequency is 349kHz; for the HAS-1202A, maximum encode rate is 641kHz.

When the leading edge of the encode signal arrives, data outputs resulting from the preceding encode command will be at their previous values; the Data Ready pulse, being RZ, will be at a digital "0" logic level.

The Data Ready pulse will typically transition from digital "0" to digital "1" 60 nanoseconds after the leading (positive-going) edge of the Encode Command. It will remain at logic "1" until all data outputs have established levels indicative of the input analog value which is present during the conversion period.

As expected, and as shown in Figure 1, the length of the Data Ready pulse and the corresponding availability of digital output data are different for the two models of HAS-1202 converters because of their differences in speed capabilities.

CALIBRATION PROCEDURE

Input connections for the HAS-1202 and HAS-1202A A/D Converters are shown in Figure 2.

The values for resistors R_A, R1, and R2 in the Gain Adjust portion of Figure 2 are a function of the desired analog input range.

For full-scale inputs ≥10.496 volts:

$R1 = (FS\ p\text{-}p \times 97.66) - 1050$

$R2 = \text{Not used}$

$R_A = 100\Omega$

For full-scale inputs <10.496 volts:

$R1 = 0\Omega$

$$R2 = 860\left[\frac{(FS\ p\text{-}p \times 97.66) - 165}{1025 - (FS\ p\text{-}p \times 97.66)}\right]$$

$R_A = 50\Omega$

The dotted lines between Pins 21 and 29 and ground in Figure 2 are used to show differences in connections for unipolar and bipolar modes. For unipolar, ground Pin 29; for bipolar, connect Pins 21, 22, and 29 together without grounding.

When calibrating for either unipolar or bipolar operation, an encode command at a frequency of 200kHz should be applied to Pin 32. Zero Adjust must always be adjusted before Gain Adjust, no matter which mode of operation is being calibrated.

Connect a precision voltage reference source between the analog input and ground.

If the converter is to be operated in a unipolar mode, adjust the output of the voltage reference to the desired full-scale positive input voltage, as described in Table I. After adjusting the Zero Adjust control per the directions in Table I, reset the reference and calibrate Gain Adjust.

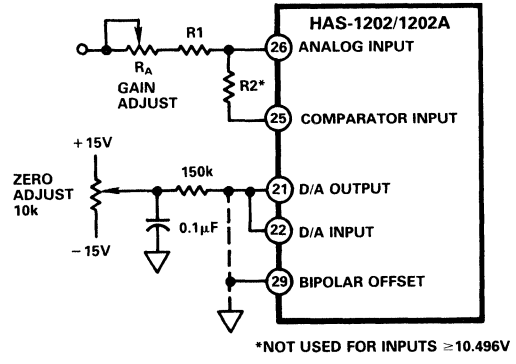


Figure 2. Gain and Offset Adjust

UNIPOLAR INPUT CALIBRATION
(For Analog Input Range 0V to + Full-Scale)

Apply Reference	And Adjust	For "Dither" Between
$+FS \times (1.22 \times 10^{-4})$	Zero	0 000 000 000 and 0 000 000 001
$+FS \times (0.99963)$	Gain	1 111 111 110 and 1 111 111 111

Table I.

If the converter is to be operated in a bipolar mode, refer to Table II.

BIPOLAR INPUT CALIBRATION
(For Analog Input Range − FS to +FS)

Apply Reference	And Adjust	For "Dither" Between
$-FS \times (0.99976)$	Zero	0 000 000 000 and 0 000 000 001
$+FS \times (0.99927)$	Gain	1 111 111 110 and 1 111 111 111

Table II.

Note that Zero Adjust is set using the negative input voltage for bipolar operation, while Gain Adjust is calibrated with the positive bipolar input.

USING HAS-1202 WITH TRACK/HOLD

Figure 3 and Figure 4 illustrate possible combinations of the HAS-1202 or HAS-1202A A/D Converter with the HTC-0300A Track-and-Hold amplifier.

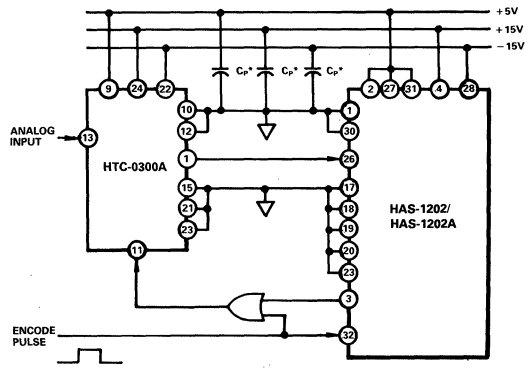
As shown, the upper word rate of the combination will be a function of which converter is used. When comparing the maximum word rates shown in the Specifications Table and the ones shown in the illustrations, there seems to be a disparity in encode rate capabilities.

The word rates shown in Figures 3 and 4, however, are correct and are based on "real-life" circuits using a T/H. The T/H needs sufficient time to acquire and/or settle to 12-bit accuracy. This interval is longer than the conversion time of the HAS-1202, and the result is a lower word rate for the combination than that which is possible with only the converter.

Note in Figure 3 that the encode pulse is applied, via an OR gate, to the ENCODE COMMAND input of the HTC-0300A. In Figure 4, it is applied directly to the $\overline{\text{ENCODE COMMAND}}$ input.

Circuit layout is extremely critical in using a high-speed converter and T/H to accomplish digitizing of analog signals; this is especially true with 12-bit systems of the type shown here.

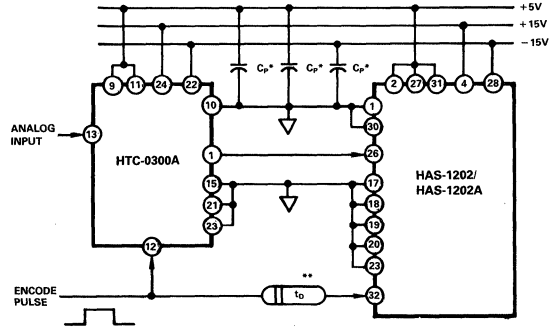
In this context, "circuit layout" encompasses all of the important items which need to be considered. This includes, but is not limited to, precautions such as establishing low-impedance grounds; careful routing of analog and digital signal paths to avoid interference; and keeping all signal paths as short as possible. Bypassing of all power supplies is mandatory for best performance.



*C_P ARE TANTALUM CAPACITORS OF 1-10μF. ALL POWER SUPPLIES SHOULD ALSO BE BYPASSED WITH 0.1μF CERAMIC CAPACITORS CONNECTED DIRECTLY TO PIN.

MODEL	ENCODE PULSE WIDTH (MIN.)	ENCODE FREQ. (MAX.)
HAS-1202	100ns	322kHz
HAS-1202A	100ns	552kHz

Figure 3. 12-Bit A/D Conversion System



*C_P ARE TANTALUM CAPACITORS OF 1-10μF. ALL POWER SUPPLIES SHOULD ALSO BE BYPASSED WITH 0.1μF CERAMIC CAPACITORS CONNECTED DIRECTLY TO PIN.

**t_D CAN BE DECREASED (OR REMOVED) BUT MAY DEGRADE PERFORMANCE. AMOUNT OF DEGRADATION HEAVILY DEPENDENT ON CIRCUIT LAYOUT.

MODEL	**t_D (MIN.)	ENCODE PULSE WIDTH (MIN.)	ENCODE FREQ. (MAX.)
HAS-1202	40ns	250ns	328kHz
HAS-1202A	80ns	250ns	560kHz

Figure 4. 12-Bit A/D Conversion System

For optimum performance in noisy environments, 2k pulldown resistors should be connected to Bits 1 through 4.

ORDERING INFORMATION

With the exception of conversion rates, the specifications are the same for the HAS-1202 and HAS-1202A A/D Converters; both units are housed in 32-pin DIP ceramic packages. For metal case versions with extended temperature ranges of −25°C to +85°C, order model number HAS-1202M or HAS-1202AM. For metal case versions with extended temperature ranges of −55°C to +100°C and military screening, order model number HAS-1202MB or HAS-1202AMB. Consult factory for details.

ANALOG DEVICES

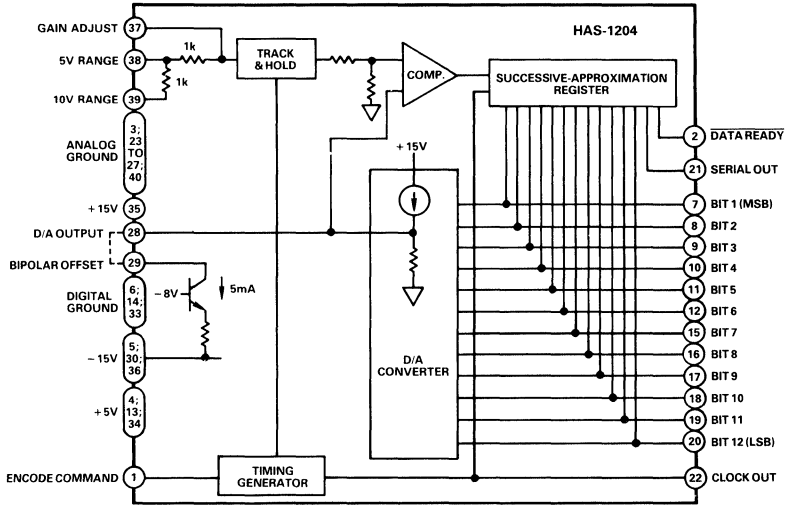
Ultrahigh Speed 12-Bit A/D Converter

HAS-1204

FEATURES
12-Bit Resolution
500kHz Word Rates
Internal Track-and-Hold
Single 40-Pin DIP

APPLICATIONS
Medical Instrumentation
Radar Systems
Test Systems
Waveform Analysis
Fast Fourier Transforms

HAS-1204 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HAS-1204 A/D Converter is a *complete* 12-bit hybrid A/D converter in a single 40-pin metal DIP. In this context, "complete" means the unit includes a track-and-hold (T/H) amplifier, encoder, and all the necessary timing circuits. It is a remarkable, self-contained device ready to perform the conversion function without the need for external circuits.

The maximum conversion time of the HAS-1204 is 2.0 microseconds, including the acquisition time of the internal T/H. The large-signal bandwidth of the T/H is 4MHz and the small-signal bandwidth is 7MHz. This combination of characteristics assures that the HAS-1204 will operate at word rates from dc through 500kHz, digitizing analog signals containing frequency components to 250kHz with minimum attenuation or distortion.

Integrating the T/H, encoder, and timing circuits into a single package allows optimum matching of T/H-encoder parameters to obtain the best possible performance. It also lowers the overall power dissipation to 2.85 watts, making the HAS-1204 an ideal choice for designers who face space and/or power restrictions for their designs.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Model	Units	HAS-1204BM	HAS-1204SM
RESOLUTION (FS = Full Scale)	Bits (%FS)	12 (0.024)	*
LSB WEIGHT			
5V Input Range	mV	1.22	*
10V Input Range	mV	2.44	*
ACCURACY			
Linearity @ dc	%FS ± 1/2LSB	0.0125	*
Monotonicity		Guaranteed	*
Nonlinearity vs. Temperature	ppm/°C	3	*
Gain Error	%FS (max)	0.1 (0.7)	*
Gain vs. Temperature	ppm/°C	35	*
DYNAMIC CHARACTERISTICS			
In-Band Harmonics[1]			
(dc to 60kHz)	dB below FS	75	*
(60kHz to 120kHz)	dB below FS	75	*
(120kHz to 200kHz)	dB below FS	70	*
Conversion Rate	kHz	500	*
Conversion Time	µs, max	2.0	*
Aperture Uncertainty (Jitter)	ps	60	*
Aperture Time (Delay)	ns (min/max)	10 (4/18)	*
Signal to Noise Ratio (SNR)[2]	dB	69	*
Transient Response[3]	ns	400	*
Overvoltage Recovery[4]	ns	900	*
Input Bandwidth			
Small Signal, −3dB[5]	MHz	7	*
Large Signal, −3dB[6]	MHz	4	*
Two-Tone Linearity (@ Input Frequencies)[7]			
(37.5kHz; 52.5kHz)	dB below FS	85	*
ANALOG INPUT			
Voltage Ranges	V, FS	0 to −5; 0 to −10 ±5; ±2.5	*
Overvoltage	V, max	2 × FS	*
Impedance			
5V Ranges	Ω (max)	1,000 (±10)	*
10V Ranges	Ω (max)	2,000 (±20)	*
Offset[8]			
Initial–10V Input	mV (max)	10 (60)	*
vs. Temperature (Unipolar)	FS ppm/°C	15	*
vs. Temperature (Bipolar)	FS ppm/°C	50	*
ENCODE COMMAND INPUT[9]			
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
		"1" = +2.4 to +5	*
Impedance	LS TTL Loads	2	*
Rise and Fall Times	ns, max	10	*
Width			
Min	ns	90	*
Max	ns	160	*
Frequency	kHz	dc to 500	*
DIGITAL OUTPUT[10]			
Format	Data Bits	12 Parallel; NRZ	*
	Data Ready	1; RZ	*
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
		"1" = +2.4 to +5	*
Drive	TTL Loads	1 Standard	*
Coding			
Unipolar Mode		Complementary Binary (CBN)	*
Bipolar Mode		Complementary Offset Binary (COB)	*
POWER REQUIREMENTS			
+15V ±0.5V	mA, max	76	*
−15V ±0.5V	mA, max	55	*
+5V ±0.5V	mA, max	177	*
Power Dissipation[11]	W, max	2.85	*
TEMPERATURE RANGE[12]			
Operating	°C	−25 to +85	−55 to +100
Storage	°C	−65 to +150	*
THERMAL RESISTANCE[13]			
Junction to Air, θ_{JA}			
(Free Air)	°C/W	25	*
Junction to Case, θ_{JC}	°C/W	16	*
PACKAGE OPTION[14]			
M-40		HAS-1204BM	HAS-1204SM

HAS-1204 PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
40	ANALOG GROUND	1	ENCODE COMMAND
39	10V RANGE	2	DATA READY
38	5V RANGE	3	ANALOG GROUND
37	GAIN ADJUST	4	+5V
36	−15V	5	−15V
35	+15V	6	DIGITAL GROUND
34	+5V	7	BIT 1 (MSB)
33	DIGITAL GROUND	8	BIT 2
32	FACTORY USE ONLY	9	BIT 3
31	FACTORY USE ONLY	10	BIT 4
30	−15V	11	BIT 5
29	BIPOLAR OFFSET	12	BIT 6
28	D/A OUTPUT	13	+5V
27	ANALOG GROUND	14	DIGITAL GROUND
26	ANALOG GROUND	15	BIT 7
25	ANALOG GROUND	16	BIT 8
24	ANALOG GROUND	17	BIT 9
23	ANALOG GROUND	18	BIT 10
22	CLOCK OUT	19	BIT 11
21	SERIAL OUT	20	BIT 12 (LSB)

NOTES

*Specification same as HAS-1204BM

[1]In-band harmonics expressed in terms of spurious in-band signals generated at 500kHz encode rate at analog input frequencies shown in ( ).

[2]RMS signal to rms noise ratio with 50kHz analog input and encode rate of 500kHz; input signal at −1.0dB.

[3]For full-scale step input, 12-bit accuracy attained in specified time.

[4]Recovers to specified performance in specified time after 2 × FS input voltage.

[5]With analog input 40dB below FS.

[6]With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 1MHz).

[7]Each input frequency applied at a level 7dB below full scale.

[8]Externally adjustable to zero.

[9]Transition from digital "0" to digital "1" initiates encoding.

[10]Use trailing edge of Data Ready pulse to strobe digital outputs into external circuits (See Figure 2).

[11]Power dissipation shown is at zero input.

[12]T = Case temperature.

[13]Maximum junction temperature = 150°C.

[14]See Section 14 for package outline information.

Specifications subject to change without notice.

THEORY OF OPERATION/TIMING

Refer to the block diagram of the HAS-1204.

Analog input signals to be digitized are applied to either Pin 38 (5V RANGE) or Pin 39 (10V RANGE), depending upon their amplitude. These signals are inputs to the internal track-and-hold (T/H) which is normally operating in the "track" mode as a buffer amplifier, following all changes in analog as they occur.

An external strap, shown between Pin 28 and Pin 29, is used if operating the converter in the bipolar mode; it is important to keep this strap as short as possible. For unipolar operation, connect Pin 29 to ground.

The user determines the point at which the digitizing process is to be initiated by controlling the application of the TTL-compatible Encode Command pulse. Its positive-going leading edge switches the T/H to the "hold" mode of operation, "freezing" the analog input signal and beginning the digitizing process. As shown in the block diagram, the Encode Command applied to Pin 1 generates the required timing signals within the HAS-1204 A/D, making it unnecessary to add external circuits.

The held value of analog input is part of the input to a high-speed comparator within the converter. The other input is the analog output of the internal high-speed, high-accuracy D/A converter. The resulting output of the comparator is applied to the successive approximation register (SAR), also controlled by timing signals initiated by the encode command.

Digital outputs are available in both serial and parallel formats, as shown in Figure 1, HAS-1204 Timing.

Times shown in the timing diagram are typical times, unless noted otherwise. In the illustration, the Track/Hold signal is internal, not available to the user; it is included to help understand the operation of the converter.

Timing intervals are measured from the leading edge of the Encode Command supplied by the user; this makes it easier to establish appropriate system timing.

Note the trailing edge of each clock pulse occurs after its corresponding serial output information has changed. If the serial output of the HAS-1204 converter is the desired signal, the trailing edges of clock pulses should be used as the stobes.

To assure the serial output data are fully established, the user is urged to incorporate a delay of approximately 30 nanoseconds between the trailing clock edge and the latch. This compensates for latch setup time, and slight variations in timing between the clock pulses and their associated data.

The portion of Figure 1 pertaining to Data Ready timing shows it returns to the digital "0" state 10 nanoseconds before the track-and-hold switches from "hold" to "track". The trailing edge of clock pulse #12 and the "track" transition are time-coincident, so this change in Data Ready occurs 10 nanoseconds before the trailing edge of the last clock pulse; and at the same time as the Bit 12 data change.

Time coincidence between the change of the Data Ready pulse and the arrival of Bit 12 (LSB) data might seem to preclude using the Data Ready pulse as a strobe. Despite that initial impression, the trailing (falling) edge of the Data Ready is recommended for strobing the parallel outputs into external circuits. This can be accomplished by using an inverter with a time delay (t_D) of the appropriate amount for the latch which is being used, as illustrated in Figure 2.

The timing relationships discussed above are generated internally because the clock pulses' rising edges control the switching. The 30-nanosecond width of each clock signal helps assure that its serial output data are firmly established by the time the clock's trailing edge arrives.

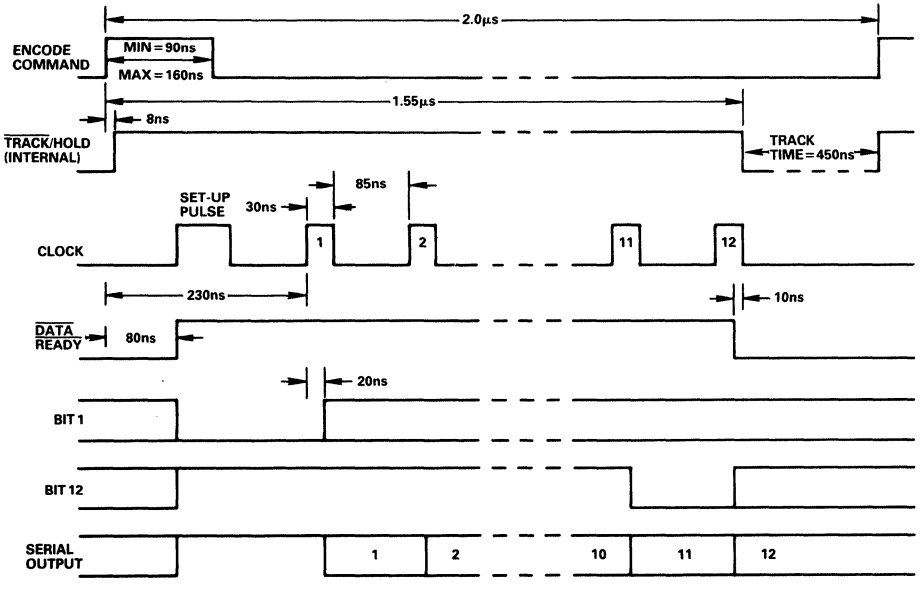


Figure 1. HAS-1204 Timing

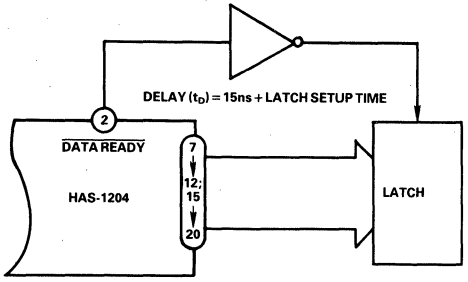
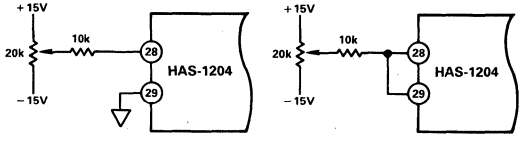


Figure 2. Output Strobe

APPLICATIONS INFORMATION

Figures 3 and 4 provide needed details on the adjustment of controls for setting the amount of offset and gain.

As noted in both illustrations, the OFFSET control must be set first for proper performance of the converter. Since the HAS-1204 is capable of operating in either a unipolar or bipolar mode, OFFSET ADJUST and GAIN ADJUST include information for both.



NOTES
A. ADJUST OFFSET CONTROL BEFORE GAIN CONTROL.
B. FOR UNIPOLAR OPERATION, CONNECT PIN 29 TO GROUND.
C. FOR BIPOLAR OPERATION, CONNECT PINS 28 AND 29 WITH *SHORT* JUMPER.

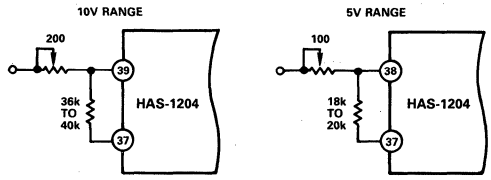
UNIPOLAR	10V RANGE	5V RANGE
APPLY −1/2LSB TO INPUT:	−1.2mV (@ PIN 39)	−0.6mV (@ PIN 38)

ADJUST FOR BIT 12 "DITHER" IN DIGITAL OUTPUT WORD: 000 000 000 00X

BIPOLAR	10V RANGE	5V RANGE
APPLY $\frac{\text{RANGE}}{2}$ − 1/2LSB TO INPUT:	+4.9988V (@ PIN 39)	+2.4994V (@ PIN 38)

ADJUST FOR BIT 12 "DITHER" IN DIGITAL OUTPUT WORD: 000 000 000 00X

Figure 3. Offset Adjust



NOTES
A. ADJUST OFFSET CONTROL BEFORE GAIN CONTROL.
B. FOR UNIPOLAR OPERATION, CONNECT PIN 29 TO GROUND.
C. FOR BIPOLAR OPERATION, CONNECT PINS 28 AND 29 WITH *SHORT* JUMPER.

UNIPOLAR	10V RANGE	5V RANGE
APPLY +1-1/2LSB TO INPUT:	−9.9963V (@ PIN 39)	−4.9982V (@ PIN 38)

ADJUST FOR BIT 12 "DITHER" IN DIGITAL OUTPUT WORD: 111 111 111 11X

BIPOLAR	10V RANGE	5V RANGE
APPLY $\frac{-\text{RANGE}}{2}$ +1-1/2LSB TO INPUT:	−4.9963V (@PIN 39)	−2.4982V (@PIN 38)

ADJUST FOR BIT 12 "DITHER" IN DIGITAL OUTPUT WORD: 111 111 111 11X

Figure 4. Gain Adust

However, careful adjustment of available controls is not the only way to help assure optimum performance. Like all high-speed, high-resolution components, the HAS-1204 is also sensitive to layout constraints. The use of a large, low-impedance ground plane is imperative.

In addition, bypass capacitors on the power supply leads are recommended. For most applications, electrolytic capacitors of 10-22 microfarads in parallel with ceramic capacitors of 0.01μF to 0.1μF will enhance the converter's effectiveness. These should be connected as closely as possible to the power supply pins entering the hybrid.

To prevent cross-coupling of analog and digital signals which may "mask" lower-order bits, analog and digital signal paths should be physically separated as much as possible. The user is urged to pay careful attention to both electrical and mechanical design to obtain best results.

ORDERING INFORMATION

Two versions of HAS-1204 A/D Converters are available as standard products; both are housed in 40-pin hermetically-sealed metal packages. With the exception of operating temperatures, the specifications are the same for both units. For a temperature range of −25°C to +85°C, specify the model HAS-1204BM; for a range of −55°C to +100°C, order model number HAS-1204SM. Units screened to military requirements are also available; contact the factory for details.

ANALOG DEVICES

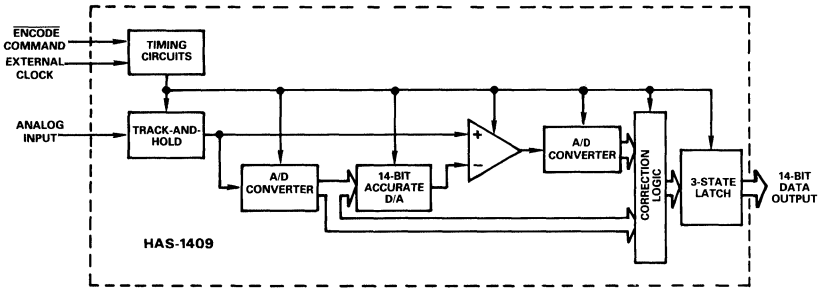
14-Bit, 125kHz Analog-to-Digital Converter

HAS-1409

FEATURES
14-Bit Resolution
125kHz Word Rates
Internal Track-and-Hold
40-Pin DIP

APPLICATIONS
FDM/TDM Transmultiplexers
CAT/NMR Scanners
PCM Systems
Digital Audio
General Instrumentation

HAS-1409 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

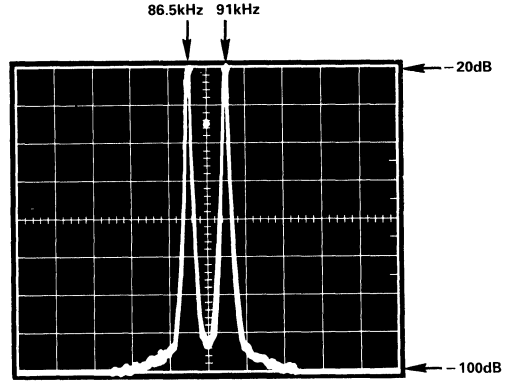
The HAS-1409KM, HAS-1409LM, and HAS-1409AKM hybrid A/D converters offer designers performance characteristics which have never before been available.

Now, for the first time, high resolution and high speed come together in a hybrid package which includes an internal track-and-hold. The HAS-1409 units have resolutions of 14 bits, are capable of word rates up to 125kHz, and are complete with track-and-hold; all of these features are housed in a single 40-pin DIP package which dissipates only two watts.

The HAS-1409KM and HAS-1409LM both include internal clocks, which allow the converters to be operated at any word rate from dc through 120kHz; the HAS-1409AKM is designed for applications which use an external system clock whose frequency establishes the user's optimum word rate, up to 125kHz.

The HAS-1409 A/D has been characterized with a companion D/A converter, the HDD-1409KM, to emphasize the superior ac performance needed for use in Frequency Division Multiplex/Time Division Multiplex (FDM/TDM) transmultiplexer systems. Although specifically designed for these kinds of applications, it can also be used for other digital signal processing such as Computer Aided Tomography (CAT) and Nuclear Magnetic Resonance (NMR) scanners, and Pulse Code Modulation (PCM).

Conventional data converters often display errors at midscale which make them inadequate for use in the types of systems cited above. The unique Digitally Corrected Subranging technique pioneered by Analog Devices, used with other proprietary techniques, virtually cancels midscale errors in the HAS-1409, thereby eliminating a major source of system errors.



10dB/div Vertical; 5kHz/div Horizontal
Spectrum analyzer shows extremely low intermodulation (IM) products of back-to-back HAS-1409 A/D and HDD-1409 D/A

The logic outputs are TTL-compatible and are presented as 14 bits of parallel data. Buffer output registers and a 3-state format provide dual advantages of good drive and bus compatibility.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Model	Units	HAS-1409KM	HAS-1409AKM	HAS-1409LM
RESOLUTION (FS = Full Scale)	Bits (%FS)	14 (0.006)	*	*
LSB WEIGHT	µV	610 or 1221, depending on input range	*	*
ACCURACY				
Linearity @ dc	%FS ± 1/2LSB	0.006	*	*
Monotonicity	°C	Guaranteed 0 to +85	*	*
Nonlinearity vs. Temperature	ppm/°C	5	*	*
Gain Error	%FS	1	*	*
Gain vs. Temperature	ppm/°C	20	*	*
DYNAMIC CHARACTERISTICS[1]				
Harmonics[2]	dB	−100	*	−80
Intermodulation Products[2]	dB	−100	*	−90
Conversion Rate	kHz	120 (112 guaranteed)	125[3]	120 (112 guaranteed)
Aperture Time (Delay)	ns	50	*	*
Signal to Noise Ratio (SNR)[4]	dB	80	*	*
Noise Power Ratio (NPR)[5]	dB	68	*	65
Transient Response[6]	µs	8	*	2
Overvoltage Recovery	µs	8	*	6
Input Bandwidth				
Small Signal, 3dB[8]	kHz	200	*	800
Large Signal, 3dB[9]	kHz	200	*	300
Idle Noise/kHz[10]	dB	−104	*	*
ANALOG INPUT				
Voltage Ranges	V, FS	±5; ±10	*	*
Overvoltage	V, max	±20	*	*
Input Type		Bipolar	*	*
Impedance	kΩ	5; 10	*	*
Offset				
Initial–Set at Factory	mV (max)	2 (10)	*	*
vs. Temperature	µV/°C	100	*	*
ENCODE COMMAND INPUT[11]				
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*	*
		"1" = +2.4 to +5	*	*
Impedance	TTL Loads	1	*	*
Width				
Min	ns	50	1 Clock	*
Max	ns	T–50[12]	Period	*
Frequency	kHz	dc to 125	Synchronous to External Clock	*
CLOCK INPUT				
Logic Levels, TTL-Compatible	V			
		N/A	"0" = 0 to +0.4	N/A
		N/A	"1" = +2.4 to +5	N/A
Impedance	TTL Loads	N/A	2	N/A
Frequency[13]	MHz, max	N/A	4.5	N/A
DIGITAL OUTPUT				
Format	Bits	14 Parallel; 3 State	*	*
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*	*
		"1" = +2.4 to +5	*	*
Drive	TTL Loads	5	*	*
Time Skew	ns, max	20	*	*
Coding		Offset Binary (MSB);	*	*
		2's Complement ($\overline{MSB}$)	*	*
POWER REQUIREMENTS				
+15V ±5%	mA	20	*	*
−15V ±5%	mA	40	*	*
+5V ±5%	mA	220	200	*
Power Dissipation	W (max)	2.0 (2.4)	1.8 (2.2)	*
TEMPERATURE RANGE[14]				
Operating	°C	−25 to +85	*	*
Storage	°C	−55 to +150	*	*
THERMAL RESISTANCE[15]				
Junction to Air, θ_{JA}				
(Free Air)	°C/W	25	*	*
Junction to Case, θ_{JC}	°C/W	16	*	*
MEAN TIME BETWEEN FAILURES[16] (MTBF)	Hours	4.15×10^4	*	*
PACKAGE OPTION[17]				
M-40		HAS-1409KM	HAS-1409AKM	HAS-1409LM

For applications assistance, phone Computer Labs Division at (919) 668-9511

NOTES

[1]AC performance characteristics are based on back-to-back performance with HDD-1409 D/A Converter. All signals are referenced to rms value of full-scale sinewave.

[2]Harmonics and intermodulation products measured at 112kHz encode rate, with input frequencies of 86.5kHz and 91kHz at −21dB (see Figure 5).

[3]Requires external clock.

[4]Full-scale signal to rms noise with 10kHz analog input frequency and encode rate of 112kHz; input signal at −6dB.

[5]60kHz to 108kHz white noise bandwidth with slot frequency of 70kHz; and encode rate of 112kHz (see Figure 6).

[6]For full-scale 10-volt input, ±1LSB attained in specified time.

[7]Recovers to 14-bit accuracy in specified time after 2×FS input overvoltage.

[8]With analog input 40dB below FS.

[9]With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 100kHz).

[10]Idle noise measured at 112kHz encode rate, with input frequency of 84kHz at −41dB (see Figure 7).

[11]HAS-1409KM has pin-selectable positive- or negative-edge triggering. HAS-1409AKM requires negative pulse synchronized to rising clock edge.

[12]T = Encode Command clock period.

[13]Clock frequency shown based on typically using 50% duty cycle and 36:1 division of external clock.

[14]Case Temperature.

[15]Maximum junction temperature = 150°C

[16]Calculated for using MIL-HDBK 217; Ground Benign; Case Temperature = 60°C.

[17]See Section 14 for package outline information.

*Specifications same as HAS-1409KM.

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

HAS-1409 PIN DESIGNATION

PIN	FUNCTION (ALL)	PIN	FUNCTION (AKM)	PIN	FUNCTION (KM & LM)
1	±10V INPUT	21	DIGITAL GROUND	21	DIGITAL GROUND
2	±5V INPUT	22	BIT 1 (MSB)	22	BIT 1 (MSB)
3	ANALOG GROUND	23	BIT 1 (MSB)	23	BIT 1 (MSB)
4	DIGITAL GROUND	24	BIT 2	24	BIT 2
5	+5V	25	BIT 3	25	BIT 3
6	+5V	26	BIT 4	26	BIT 4
7	N/C	27	BIT 5	27	BIT 5
8	N/C	28	BIT 6	28	BIT 6
9	+5V	29	ENABLE HIGH (MSBs)	29	ENABLE HIGH (MSBs)
10	DIGITAL GROUND	30	CLOCK	30	ENCODE
11	ENABLE LOW (LSBs)	31	ENCODE	31	ENCODE
12	BIT 14 (LSB)	32	+5V	32	+5V
13	BIT 13	33	DIGITAL GROUND	33	DIGITAL GROUND
14	BIT 12	34	−15V	34	−15V
15	BIT 11	35	+15V	35	+15V
16	BIT 10	36	DIGITAL GROUND	36	DIGITAL GROUND
17	BIT 9	37	ANALOG GROUND	37	ANALOG GROUND
18	BIT 8	38	ANALOG GROUND	38	ANALOG GROUND
19	BIT 7	39	+5V	39	+5V
20	DIGITAL GROUND	40	ANALOG GROUND	40	ANALOG GROUND

ALL +5V PINS ARE CONNECTED TOGETHER INTERNALLY (5, 6, 9, 32, 39). MUST ALSO BE CONNECTED TOGETHER EXTERNALLY CLOSE TO CASE.
ALL ANALOG GROUND PINS ARE CONNECTED TOGETHER INTERNALLY (3, 37, 38, 40).
ALL DIGITAL GROUND PINS ARE CONNECTED TOGETHER INTERNALLY (4, 10, 20, 21, 33, 36).
FOR BEST PERFORMANCE, ANALOG GROUND AND DIGITAL GROUND PINS MUST ALL BE CONNECTED TOGETHER AND TO GROUND EXTERNALLY AS CLOSE TO THE CASE AS POSSIBLE.

HAS-1409KM/HAS-1409AKM TIMING

Refer to the block diagram of the HAS-1409AKM A/D converter.

In the HAS-1409KM, and HAS-1409LM, signals applied to the timing circuits will be different from those shown. For them, these signals will be ENCODE or $\overline{\text{ENCODE}}$.

In all units, the analog input to be digitized is applied first to a track-and-hold (T/H) circuit, which is normally in "track", following all changes in analog as they occur since the T/H is operating as a buffer amplifier.

Refer to Figure 1, the timing diagram for the HAS-1409KM and HAS-1409LM A/D converters.

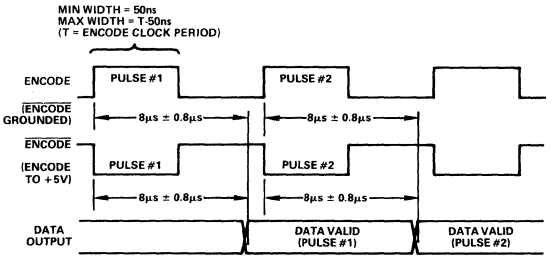


Figure 1. HAS-1409KM and HAS-1409LM A/D Timing Diagram

The user determines the point at which digitizing is to be done by applying an external TTL-compatible signal to the timing circuits; this causes the T/H to switch from the "track" mode to the "hold" mode. In the HAS-1409KM and HAS-1409LM, this "track" to "hold" transition can be accomplished with either positive triggering or negative triggering. As shown, positive-edge triggering is done with an ENCODE command and $\overline{\text{ENCODE}}$ connected to ground. Negative-edge triggering is accomplished with an $\overline{\text{ENCODE}}$ signal and ENCODE connected to +5V. The HAS-1409KM and HAS-1409LM return to "track" automatically approximately 5μs after the encode command.

Output data will be valid after a nominal delay of 8μs from the leading edge of the encode command. Strobing the output data into external circuits might best be accomplished by using a square-wave signal for the encode command and using its negative-going trailing edge as a time reference for the strobing action. Output data will not yet be valid when that trailing edge occurs, but the edge can be used as a known reference point for measuring the 8μs conversion time.

Internal timing circuits within the HAS-1409 generate the necessary control and timing pulses to operate the unit at a word rate of 112kHz. This rate is based on:

KM/LM: The internal clocks are adjusted at the factory for this conversion rate.

AKM: The HAS-1409AKM divides the external clock frequency of 4.032MHz by a factor of 36:1 and provides 14 bits of parallel data at the 112kHz word rate established by this ratio. The 112kHz cited in this example is the minimum guaranteed word rate of the HAS-1409, and is a sample rate commonly used in transmultiplexer applications. (See FDM/TDM Transmultiplexers section of data sheet).

Figure 2 shows the timing relationship of the HAS-1409AKM A/D converter signals when the converter is being operated from an external clock.

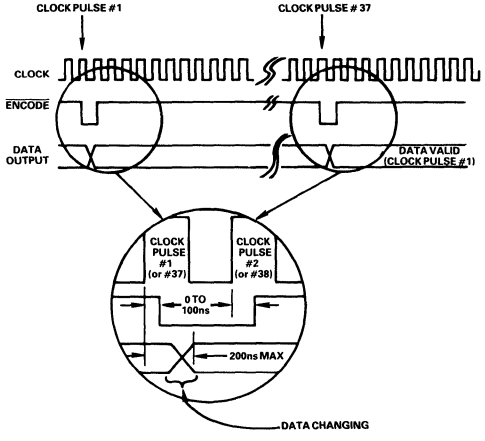


Figure 2. HAS-1409AKM A/D Timing Diagram (External Clock Operating at 4.032MHz)

As shown, the leading edge of the negative-going $\overline{\text{ENCODE}}$ pulse supplied by the user should occur from 0 to 100ns after the leading edge of the clock pulse which is shown (for purposes of illustrating timing relationships) as Clock Pulse #1. The trailing edge of this pulse should occur from 0 to 100ns after the leading edge of the *next* clock pulse (designated here as Clock Pulse #2).

The output data associated with the *preceding* clock pulse and $\overline{\text{ENCODE}}$ pulse will be valid within 200ns of the leading edge of Clock Pulse #1. Data associated with Clock Pulse #1 will be valid within 200ns of the leading edge of Clock Pulse #37. When the HAS-1409AKM is operated from a 4.032MHz clock, the trailing edge of the $\overline{\text{ENCODE}}$ pulse could be used to determine when the output data will be strobed into external circuits.

The $\overline{\text{ENCODE}}$ pulse is used to insure output data will remain in synchronization with the clock pulses. Using the leading edge of the first $\overline{\text{ENCODE}}$ as a reference, the HAS-1409AKM goes into "track" after 21 clock pulses (on Clock Pulse #22); and goes into "hold" after 34 clocks (Clock Pulse #35).

THEORY OF OPERATION

With the exception of the difference in input signals applied to the timing circuits, all converters operate in essentially the same way.

Referring again to the block diagram, the timing circuits "freeze" the analog signal at the output of the track-and-hold. This held value is applied to an A/D converter in the HAS-1409, and the same value is applied to one input of a difference amplifier.

The output of the internal A/D converter is digitized and applied to a D/A converter which is 14-bit accurate and optimized for ac applications; the A/D output is also applied to correction logic circuits.

The D/A output is applied to the second input of the difference amplifier, which generates an error signal indicative of the difference between the "held" analog input and a digital representation of that signal. This residue signal is then converted and is also applied to the digital correction circuits.

The correction circuits combine the two bytes to compensate for nonlinearities and other circuit errors. Basically, the information contained in the second byte is used as the Least Significant Bits (LSBs) and determines what corrective action is needed for the first byte (the MSBs) to insure its accuracy.

APPLICATIONS/TESTING

For FDM/TDM applications, the analog input frequency applied to the HAS-1409 will be in the frequency band of 60-108kHz; the combined HAS-1409/HDD-1409 performance parameters have been optimized for this use.

Refer to Figure 3 HAS-1409 Basic Interface.

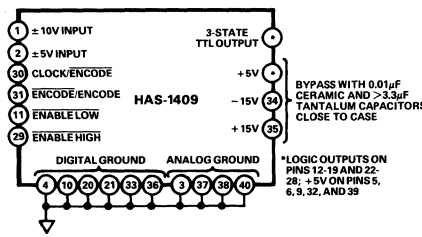


Figure 3. HAS-1409 Basic Interface

As shown, the anlog input is applied to Pin 1 or Pin 2, depending on the amplitude of the signal to be digitized. A TTL-compatible pulse is applied as $\overline{\text{ENCODE}}$; and another TTL-compatible signal is applied as the clock. As indicated earlier in the timing diagram, these signals must be synchronous.

The $\overline{\text{ENABLE HIGH}}$ and $\overline{\text{ENABLE LOW}}$ signals applied to Pins 29 and 11 control the state of the digital outputs. The TTL $\overline{\text{ENABLE HIGH}}$ signal affects $\overline{\text{BIT 1}}$ (MSB), Bit 1 ($\overline{\text{MSB}}$), and Bits 2-6; the $\overline{\text{ENABLE LOW}}$ affects Bits 7-14. When $\overline{\text{ENABLE HIGH}}$ and/or $\overline{\text{ENABLE LOW}}$ inputs are connected

to ground or logical "0", their corresponding bit outputs will be present. When they are connected to a logical "1" voltage, their associated bit outputs will be open.

The 3-state TTL digital output signals will be available at Pins 12-19 and Pins 22-28. Pins 34 and 35 are used for −15V and +15V supplies; +5V is applied to several places–Pins 5, 6, 9, 32, and 39 (all pins should be connected). All three supplies should be bypassed as close as possible to the hybrid case. For best performance, all ANALOG GROUND and DIGITAL GROUND pins *must* be connected together and to ground externally; this should also be done close to the case.

Refer to Figure 4 Basic Test Setup.

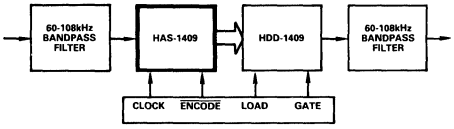


Figure 4. Basic Test Setup

The HAS-1409 A/D converter has been characterized for performance in a back-to-back hook-up with the HDD-1409 D/A converter. The analog signal to be digitized and reconstructed is applied to this test arrangement through a bandpass filter of 60kHz-108kHz; the resulting analog output is also passed through the same kind of filter.

CLOCK and $\overline{\text{ENCODE}}$ signals are generated in synchronization with one another and are timed for correct interaction with the STROBE and GATE signals applied to the D/A. Because of the back-to-back configuration of the two converters, the performance tests are indicative of the baseline characteristics of *both* units.

Refer to Figure 5 Intermodulation (Total Harmonic) Distortion Test Circuit.

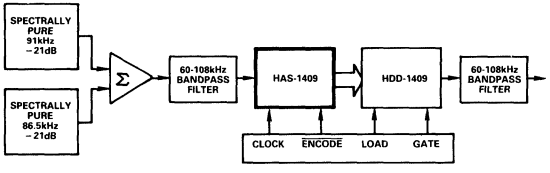


Figure 5. Intermodulation (Total Harmonic) Distortion Test Circuit

Harmonics levels and intermodulation (IM) products are measured in the same way to assure optimum performance in FDM/TDM system applications. The purpose of the testing is to insure that "beat" frequencies generated by the interaction of two signals are sufficiently suppressed to avoid interfering with the carrier frequencies and masking their information contents.

In these tests, the HAS-1409 is operated at a 112kHz word rate, established by the external 4.032MHz clock. Two pure sinewave signals at frequencies of 91kHz and 86.5kHz are applied to a summation amplifier at precise levels 21dB below the rms value of a full-scale sinewave.

These particular input frequencies are selected on the basis that their interaction with one another will generate second and third-order harmonics and IM products which are easily distinguished and measurable. As in any sampling scheme, these signals are "folded" back into the passband of interest and their amplitudes are a measure of A/D and D/A performance.

The output of the summation amplifier is applied through the 60-108kHz filter, digitized, reconstructed, and refiltered. Typically, the levels of harmonics and intermodulation products are −100dB.

Refer to Figure 6 Noise Power Ratio Test Circuit.

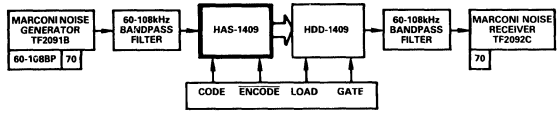


Figure 6. Noise Power Ratio Test Circuit

Noise Power Ratio (NPR) is a critical measure of A/D and D/A performance for FDM/TDM systems and the method of measuring this ratio must replicate the conditions which are present when the units are operating as a part of those systems. In this test, also, the HAS-1409 is operating at 112kHz word rates.

White noise in the frequency band of 60kHz to 108kHz is applied to the A/D, and the total power which is present in a narrow "slot" at a frequency of 70kHz is computed. A narrow bandstop filter whose center frequency is 70kHz is then switched in, and the total power remaining in the "slot" is computed. The ratio of these two readings is the NPR and the result for the HAS-1409 is typically 68dB. CAUTION: The high-performance characteristics of the HAS-1409 stress the measurement capabilities of most NPR test sets.

Refer to Figure 7 Idle Noise Test Circuit. In this test, a spectrally-pure sinewave of 84kHz is applied through a filter to the HAS-1409/HDD-1409 combination at a level of −41dB. An encode rate of 112kHz is used; the combination of input frequency and encode rate cancels all harmonics, leaving only the fundamental input frequency and noise components.

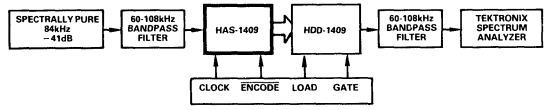


Figure 7. Idle Noise Test Circuit

The results of digitizing and reconstructing this signal are examined with a spectrum analyzer to determine the level of noise components contributed by the converters. Acceptable performance will show average idle noise components to be at −104dB when using a 1kHz-resolution filter.

FDM/TDM TRANSMULTIPLEXERS

There are two standard formats used in telephony for multiplexing voice signals. The older of the two, frequency division multiplex (FDM), is used throughout the world for transmitting long distance telephone calls. In this scheme, voiceband signals are "stacked" into adjacent 4kHz channels in their assigned frequency domain by using single sideband (SSB) amplitude modulation.

Standard FDM hierarchy assembles twelve of these 4kHz channels into units called "groups", and then assembles five groups (60 channels) into "supergroups." The frequencies of group bands range from 60kHz to 108kHz, and the supergroup bands have center frequencies between 312kHz and 552kHz.

In the newer time division multiplex, or TDM, each voice signal is digitized using pulse code modulation (PCM), at an 8kHz sample rate. The resulting pulse streams are then interleaved in time and transmitted.

The assembly of time slots (channels) for TDM is not as universal as it is for FDM. In North America and Japan, the basic unit is 24 time slots, all of which are available to users. In Western Europe, the basic unit is 32 time slots; 30 are active, one is for signaling, and one is for framing.

TDM processing is growing at a rapid pace because the voice signals have good fidelity, and the hardware which is used benefits from the economics of lower and lower prices for digital integrated circuits.

Digital toll switching offices were first installed in the United States in the latter part of the 1970s. One of the major characteristics of these types of telephone offices is that they switch signals exclusively in the TDM format within the office. But their need to operate also with the older FDM format means all incoming and outgoing signals must be converted to and from digital form.

The interface between the two standard signal multiplexing formats used to make this conversion is the FDM/TDM transmultiplexer system. The translation from one format to the other can be accomplished with conventional analog and digital techniques by demultiplexing signals in one format down to baseband, and remultiplexing them again into the other format.

Digital signal processing (DSP) for the interface is attractive, however. The frequency ranges of the signals which are involved make efficient use of available technology; and the stringent interface specifications benefit from the inherent precision of a digital approach. Since the problem is well defined, digital techniques are distinctly viable solutions. An example of these techniques is shown in Figure 8.

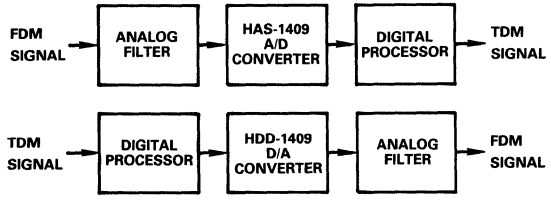


Figure 8. Digital FDM/TDM Translation

Undesirable out-of-band components are removed from the FDM signal by the analog filter. The output of the filter is then applied to the HAS-1409 A/D converter whose output is a digital word stream. The individual channels within this stream are separated via a real-time processing algorithm in the block labeled Digital Processor. The resulting signal is now in the TDM format for switching and/or transmitting.

The lower portion of Figure 8 depicts the process of going from TDM to FDM, using the HDD-1409 D/A converter, in a procedure which is basically an inverse operation. The exception is the analog filter, which performs essentially the same function in both directions.

Interfacing FDM and TDM occurs at two different levels. In North America and Japan, this translation takes place between two 12-channel group bands and a 24-channel TDM unit. In Europe, it is between a 60-channel supergroup and two 30-channel European TDM units.

Theoretically, the minimum word rate for the HAS-1409 A/D is equal to twice the bandwidth of the FDM group signal; that signal, in turn, is equal to the word rate of the TDM signal, i.e., 96kHz for the group band.

This minimum rate falls into the passband of interest because group frequencies occupy the band from 60kHz to 108kHz; as a consequence, the theoretical minimum rate would severely complicate the processing algorithm and introduce aliasing errors into the signal.

Operating at a conversion rate near this minimum is desirable, however, because the cost of the A/D and D/A converters increases as their word rates increase. In addition, a sampling rate which is an even multiple of the basic 8kHz PCM frequency simplifies the algorithm.

Since any sampling rate between the (108kHz) upper band and two times the 60kHz lower band (120kHz) will suffice, the HAS-1409 A/D converter is operated at 112kHz.

This rate provides the benefits enumerated above and prevents overlapping between channels caused by aliasing. A conversion rate of 112kHz also supplies a guard band of 8kHz between signal images; that guard band reduces the complexity of the analog reconstruction filter.

Computer Labs Division of Analog Devices uses this 112kHz word rate when testing the performance of the HAS-1409 A/D and HDD-1409 D/A converters back-to-back to help assure test conditions are a good replication of the operating conditions.

For some of the testing, the word rate interacts with the analog input frequencies to provide additional insight into performance. Harmonics tests and intermodulation products tests are examples.

Another is the test for idle noise, the sum of various noise spectra not influenced by modulation. Thermal noise, oscillator shot noise, baseband amplifier noise, and other sources are examples. Their sum is measured on a power basis because of their uncorrelated nature.

In the test, the input frequency is a spectrally-pure 84kHz. The combination of input frequency and encode rate cancels all harmonics, leaving only the fundamental frequency and the idle noise components.

Evaluating the amount of idle noise generated by the converters helps evaluate their nonlinear distortion, without rigorously testing for that characteristic. In transmultiplexer systems, the converters are the only important sources of this distortion, but converters which meet requirements for idle noise easily meet requirements for nonlinearity.

ANALOG DEVICES

12-Bit Video Analog-to-Digital Converter

MOD-1205

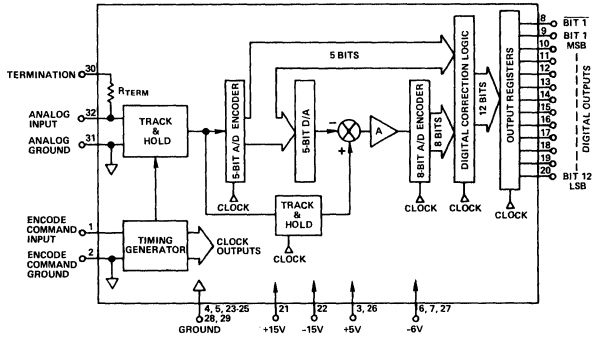
FEATURES

12 Bits @ 5MHz Word Rate
One-27 Sq. In. PC Board
Built-In Track-and-Hold – 25ps Aperture Uncertainty
15MHz Analog Input Bandwidth
TTL Compatible
Low (13-Watt) Power Dissipation
Signal-to-Noise Ratio Greater Than 66dB
Noise Power Ratio Greater Than 56dB
Completely Repairable

APPLICATIONS

Radar Digitizing
Digital Communications
Real Time Spectrum Analysis
Signature Analysis

MOD-1205 FUNCTIONAL BLOCK DIAGRAM



NOTE: WITH PIN 30 OPEN, ANALOG INPUT IMPEDANCE IS 400Ω. WITH PIN 30 GROUNDED, ANALOG IMPEDANCE IS 50Ω.

GENERAL DESCRIPTION

Analog Devices' model MOD-1205 is a very high-speed A/D converter capable of digitizing video input signals to 12-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1205 is truly a breakthrough in high-speed A/D technology. It utilizes the latest state-of-the-art conversion technique called digital correcting subranging (DCS) to effectively eliminate errors normally associated with subranging type ADCs. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

The MOD-1205 is constructed on a single printed circuit card which is intended for mounting on a system mother board and occupies only 27 square inches. Within this A/D is the required sample/track-and-hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. NO external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1205 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1205 is backed by Analog Devices' limited one year warranty.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

MODEL	MOD-1205
RESOLUTION (FS = FULL SCALE)	12 Bits (0.024% FS)
LSB WEIGHT	1mV
ACCURACY (INCLUDING LINEARITY) @ DC	±0.0125% Full Scale ±1/2LSB
Monotonicity	Guaranteed (0 to +70°C)
Nonlinearity vs. Temperature	0.005% of FS/°C, max
Gain vs. Temperature	0.01% of FS/°C, type; 0.03% of FS/°C, max
DYNAMIC CHARACTERISTICS	
AC Linearity[1] (dc to 1MHz)	Spurious Signals >70dB below FS, max
(1MHz to 2.5MHz)	Spurious Signals >65dB below FS, max; >68dB, typ
Conversion Time	See Text and Timing Diagram
Conversion Rate (Word Rate)	5MHz
Aperture Uncertainty (Jitter)	±25ps max
Aperture Time	30ns (±10ns from unit to unit)
Signal to Noise Ratio[2]	66dB min; 68dB, typ
Noise Power Ratio[3]	56dB min, 58dB typ
Transient Response[4]	12-Bit (0.0125%) Accuracy within 200ns
Overvoltage Recovery Time[5]	200ns
Input Bandwidth (small signal, 3dB)	15MHz min
Input Bandwidth (large signal, 3dB)	10MHz min; flat within ±0.1dB, dc through 5MHz
ANALOG INPUT	
Voltage Range	±2.048V FS
	±4V Absolute max
Impedance	400Ω with pin 30 open, 50Ω with pin 30 grounded
Offset Voltage	Adjust to 0 with On Board Potentiometer
Offset vs. Temperature	0.02% FS/°C, type; 0.05% of FS/°C, max
Bias Current	1nA max
ENCODE COMMAND INPUT	
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = +2.4V to +5V
Logic Loading	2 Standard TTL Gates
Rise and Fall Times	10ns max
Duration min/max	25ns/50% of Duty Cycle
Frequency (Random or Periodic)[6]	5MHz
DIGITAL DATA OUTPUT	
Format	12 Parallel Bits, NRZ
Logic Levels, TTL Compatible	"0" = 0 to +0.4V
	"1" = +2.4V to +5V
Drive (Not Short Circuit Protected)	Up to 1 Schottky TTL or
	2 Standard TTL Loads
Time Skew	10ns max
Coding	Offset Binary (OBN) or 2's complement (2SC)
Conversion Time	See Text on the Next Page
POWER REQUIREMENTS[6]	
+15V ±5%	200mA
−15V ±5%	150mA
−6V ±4%	700mA
+5V ±5%	800mA
Power Consumption	13 Watts
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	−55°C to +85°C
Cooling Requirements	500 Linear Feet Per Min (LFPM) @ +70°C
PHYSICAL CHARACTERISTICS	
Construction	Single Printed Circuit Card

NOTES:
[1] AC linearity expressed in terms of spurious in-band signals generated at specified encode rates at analog input frequencies ( ).
[2] rms signal to rms noise at 500kHz analog input.
[3] dc to 2.4MHz white noise bandwidth with slot frequency of 512kHz.
[4] For full-scale step input, attains 12-bit accuracy in time specified.
[5] Recovers to 12-bit accuracy after 2 × FS input overvoltage in time specified.
[6] For operation at word rates below 500kHz, consult factory.

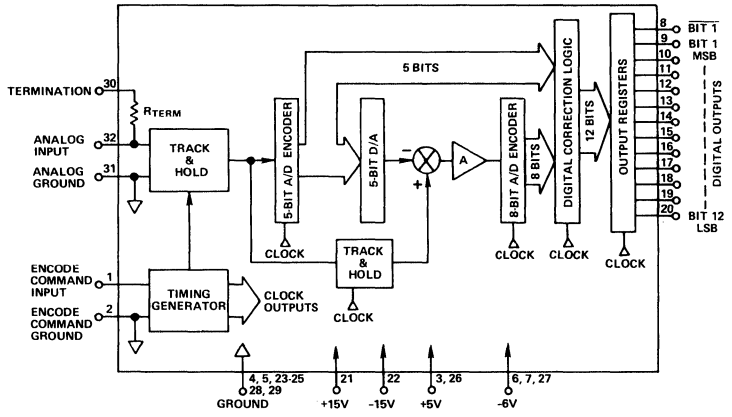
Specifications subject to change without notice.

PIN	FUNCTION
1	ENCODE COMMAND
2	GND*
3	+5V
4	GND*
5	GND*
6	-6V
7	-6V
8	$\overline{\text{BIT 1}}$
9	BIT 1 (MSB)
10	BIT 2
11	BIT 3
12	BIT 4
13	BIT 5
14	BIT 6
15	BIT 7
16	BIT 8

PIN	FUNCTION
17	BIT 9
18	BIT 10
19	BIT 11
20	BIT 12 (LSB)
21	+15V
22	-15V
23	GND*
24	GND*
25	GND*
26	+5V
27	-6V
28	GND*
29	GND*
30	TERMINATION
31	GND*
32	ANALOG INPUT

*ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE MOD-1205

Pin Designations



NOTE: WITH PIN 30 OPEN, ANALOG INPUT IMPEDANCE IS 400Ω. WITH PIN 30 GROUNDED, ANALOG IMPEDANCE IS 50Ω.

MOD-1205 Block Diagram

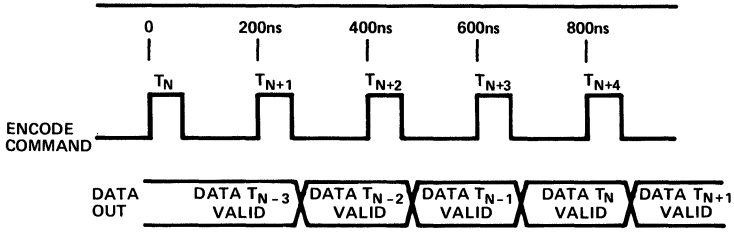
ORDERING INFORMATION

Order model number MOD-1205 A/D converter. Mating pin sockets for the MOD-1205 are model number MSB-2 (32 required per A/D).

CONVERSION TIME

Output data is valid two encode command clock periods plus 275ns ±25ns after application of an initial encode command pulse. Due to the pipeline delay effect of the A/D, a total of three encode command pulses are required to shift the data to the output of the A/D. For example, with a 5MHz encode rate, data is valid 675ns ±25ns after the application of the first encode command pulse—assuming that two pulses occur after the first.

Use of the trailing edge of the encode command is recommended for strobing output data into external register (see Figure 1).



DATA T_N (THE RESULT OF ENCODE COMMAND T_N) OCCURS TWO CONVERSION PERIODS PLUS 275ns ±25ns AFTER ENCODE COMMAND T_N. FOR A 5MHz WORD RATE AS SHOWN, DATA IS VALID 275ns ±25ns AFTER THE THIRD ENCODE COMMAND PULSE OR T_N + 675ns ±25ns. IN ALL CASES, THREE ENCODE COMMAND PULSES ARE REQUIRED FOR TRANSFER OF DATA TO THE OUTPUT, DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D. NO DATA READY PULSE IS SUPPLIED.

Figure 1. MOD-1205 Timing Diagram

GROUND CONNECTIONS

It should be noted that the MOD-1205 PC board has 9 ground pins. These are all connected to the ground plane on the board. For best results it is recommended that ALL of these pins be connected to a massive system or "mother board" ground plane.

CALIBRATION PROCEDURE (MOD-1205)

The MOD-1205 A/D is precisely calibrated at the factory before shipments and should need no further calibration. However, if slight readjustments of the A/D are required in the system, the following procedure should be followed. This procedure refers to a binary output.

Offset Adjustment

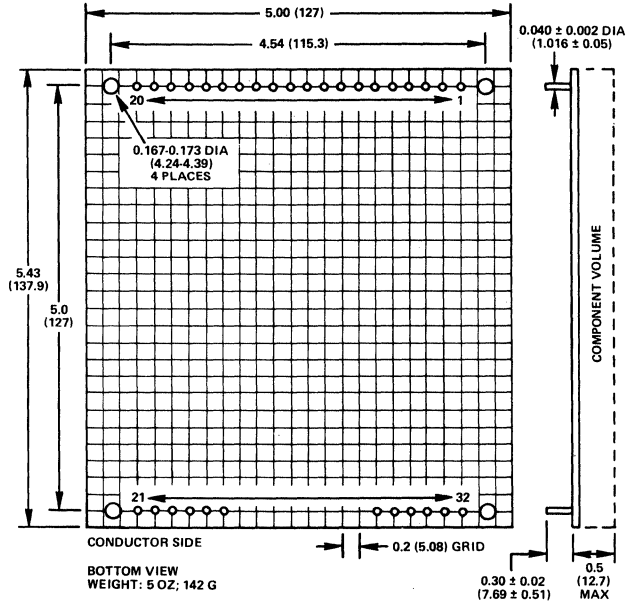
The offset is adjusted by varying potentiometer R22 with 0 volts applied to the analog input. To obtain the proper output code, observe that the digital output is changing between 100000000000 and 011111111111 at this adjustment level. When properly adjusted a digital code of 100000000000 will represent an analog input 1/2LSB above zero volts, and a digital code of 011111111111 will represent an analog input of 1/2LSB below zero volts.

Gain Adjustment

The gain is adjusted by varying potentiometer R2. This adjustment is made by applying +2.0465V (FS -1 1/2LSB) to the analog input and while monitoring the digital output, adjust R2 for the output code varying between 111111111110 and 111111111111 (FS). If the user needs to offset the entire range of the A/D, this can be accomplished by a readjusting R22 as required. However, in this procedure, the offset should always be adjusted first.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



V/F & F/V Converters
Contents

Selection Guide
V/F and F/V Converters

VOLTAGE-TO-FREQUENCY CONVERTERS

Model	Full-Scale Frequency MHz	Linearity % max	FS Calib Error % typ	Output Format	Input Range V	Package Options[1]	Temp Range[2]	Page	Comments
AD652	**2**	**0.005–0.05**	**0.25–0.5**	**Pulse Train**	**0 to 10 0 to −10 ±5**	**Q, P**	**C, I, M**	**4–25**	**Synchronous, Multiple Input Ranges, Low Nonlinearity**
AD650	**1**	**0.005–0.1**	**5–10**	**Pulse Train**	**−10 to 0**	**D, N, P**	**C, I, M**	**4–13**	**Low Nonlinearity**
AD654	**0.5**	**0.1–0.4**	**10**	**Square Wave**	**0 to (V_S–4)**	**N, R**	**C**	**4–41**	**Single Supply, Low Cost**
ADVFC32	0.5	0.01–0.2	5	Pulse Train	0 to 10	H, N	C, I, M	4–49	Industry Standard
AD537	0.15	0.07–0.25	5	Square Wave	$-V_S$ to ($+V_S$–4)	D, H	C, M	4–5	

FREQUENCY-TO-VOLTAGE CONVERTERS

Model	Input Range kHz	Linearity % max	Response Time ms typ	Package Options[1]	Temp Range[2]	Page	Comments
451	0 to 10	0.03–0.008	4	Module	I	N†	Complete, No External Components
453	0 to 100	0.03–0.008	0.8	Module	I	N†	Complete, No External Components

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
†N = Design-In product still available, but not included in catalog. Ask your local sales office for datasheet.
Boldface Type: Product recommended for new design.

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters (VFCs) convert analog voltage or current levels to pulse trains or square waves in a logic-compatible form (usually TTL) at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. V/F converters find applications in analog-to-digital converters with high resolution, long-term high-precision integrators, two-wire high-noise-immunity digital transmission and digital voltmeters.

FREQUENCY-TO-VOLTAGE CONVERTERS

Frequency-to-voltage converters (FVCs) perform the inverse operation; they accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. Combining adjustable threshold, gain and output offset with low linearity error, F/V converters offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage. Examples are motor-speed controllers, power-line frequency monitors and VCO stabilization circuits. In analog-to-analog data transmission, they convert serially transmitted data in the form of pulse streams back to analog voltage.

Applications of both forms of conversion, as appropriate to specific device types, are illustrated with varying degrees of detail on the individual data sheets.

FACTORS IN CHOOSING VFCs AND FVCs

Voltage-to-frequency converters are available from Analog Devices in both pulse train and square wave outputs. The output of the change balance types which can operate up to 1MHz F.S., is a train of pulses of constant height and width, with very low duty cycle for small analog inputs. The output of the AD537 is unique in that its output is square wave, an advantage in some applications.

The most popular VFC designs (Figure 1) contain an integrator which charges at a rate proportional to the value of the input signal. Each time the integrator's charge has been increased by a precisely metered increment, the threshold crossing produces a pulse of accurately known area. The pulse serves both as the output (via a buffer) and as a subtractive charge increment to

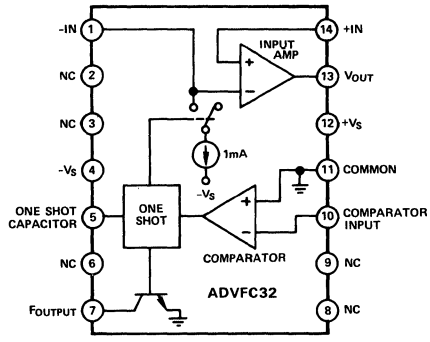


Figure 1. Block Diagram of the ADVFC32

reduce the integrator's net charge. The next pulse is triggered when the net integral has again reached the threshold. The relationship between the pulse rate and the input level is linear. The AD537 operates on a somewhat different principle (Figure 2): an input current charges a capacitor between two threshold levels, first in one direction, then in the other, in an emitter-coupled astable multivibrator circuit. Since the time required to reach the switching threshold is inversely proportional to the analog input, the frequency is directly proportional. For constant analog input, the charging rate and the discharge rate are equal, so the output is a square wave.

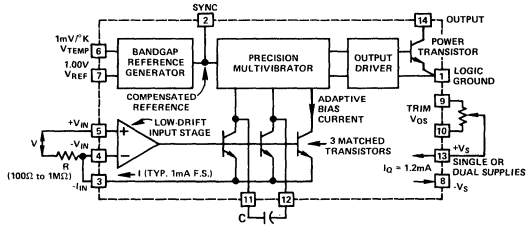
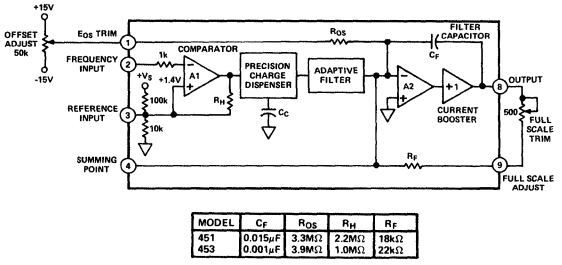


Figure 2. Block Diagram of the AD537



MODEL	C_F	R_{OS}	R_H	R_F
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

Figure 3. Block Diagram – Models 451 & 453 FVCs

Frequency-to-voltage converters (Figure 3) average a train of equal-area pulses that are generated internally by a precision charge dispenser in response to each crossing of an input threshold. The analog output voltage is proportional to the sum of the pulse areas over a given period. F/V conversion can also be obtained by using the ADVFC32.

SPECIFICATIONS

The salient specifications for VFCs are *(non)linearity*, as a percentage of full-scale frequency; *frequency range*, the greater the frequency range, the greater the resolution for a given counting period; *full-scale-calibration error; gain-temperature coefficient*, in ppm of signal per °C, where "gain" is the ratio of full-scale frequency to full-scale voltage; *input-offset temperature coefficient; overrange capability*, within rated specifications, and *step response*, the worst-case time interval required for the frequency to respond to a full-scale-step input change.

For FVCs, important specs, in addition to accuracy specs corresponding to the above, include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated and for versatility in interfacing various types of sensors directly), *hysteresis* (to provide a degree of insensitivity to noise superimposed on a slowly-varying input waveform) and *dynamic response* (important in motor control).

Definitions of some critical specifications, and the conditions for adjusting or measuring them, are detailed on individual data sheets.

ANALOG DEVICES

Integrated Circuit Voltage-to-Frequency Converter

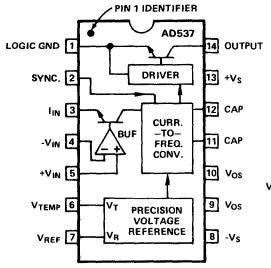
AD537*

FEATURES

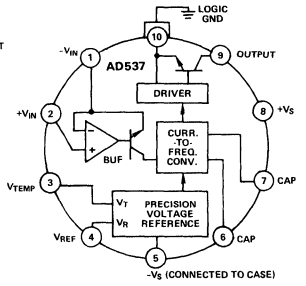
- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity: ±0.05% FS
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output (1mV/K)
- F-V Applications

AD537 PIN CONFIGURATIONS

"D" Package – TO-116



"H" Package – TO-100



4

PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to ±30V. Linearity error is as low as ±0.05% for 10kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±30ppm/°C. The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

A temperature-proportional output, scaled to 1.00mV/K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, offset scales such as 0°C or 0°F can be generated.

The low drift (1μV/°C typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high (250MΩ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0 to +70°C range while the AD537S is specified for operation over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ - 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristic are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 6.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted)

MODEL	AD537JH	AD537JD	AD537KD AD537KH	AD537SD[1] AD537SH[1]
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0 to 150kHz	*	*	*
Nonlinearity[1]				
f_{max} = 10kHz	0.15% max (0.1% typ)	*	0.07% max	**
f_{max} = 100kHz	0.25% max (0.15% typ)	*	0.1% max	**
Full Scale Calibration Error				
C = 0.01μF, I_{IN} = 1.000mA	±10% max	±7% max	±5% max	**
vs. Supply (f_{max} < 100kHz)	±0.1%/V max (0.01% typ)	*	*	*
vs. Temp. (T_{min} to T_{max})	±150ppm/°C max (50ppm typ)	*	50ppm/°C max (30ppm typ)[2]	150ppm/°C max
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0 to (+V_S - 4) Volts (min)	*	*	*
Dual Supply	-V_S to (+V_S - 4) Volts (min)	*	*	*
Input Bias Current				
(Either Input)	100nA	*	*	*
Input Resistance (Non-Inverting)	250MΩ	*	*	*
Input Offset Voltage				
(Trimmable in "D" Package Only)	5mV max	*	2mV max	**
vs. Supply	200μV/V max	100μV/V max	100μV/V max	**
vs. Temp. (T_{min} to T_{max})	5μV/°C	*	1μV/°C	10μV/°C max
Safe Input Voltage[3]	±V_S	*	*	*
REFERENCE OUTPUTS				
Voltage Reference				
Absolute Value	1.00 Volt ±5% max	*	*	*
vs. Temp. (T_{min} to T_{max})	50ppm/°C	*	100ppm/°C max[3]	**
vs. Supply	±0.03%/V max	*	*	*
Output Resistance[4]	380Ω	*	*	*
Absolute Temperature Reference[5]				
Nominal Output Level	1.00mV/K	*	*	*
Initial Calibration @ +25°C	298mV (±5mV)	*	298mV (±5mV max)	**
Slope Error from 1.00mV/K	±0.02mV/K	*	*	*
Slope Nonlinearity	±0.1K	*	*	*
Output Resistance[5]	900Ω	*	*	*
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"				
V_{OUT} = 0.4V max, T_{min} to T_{max})	20mA min	20mA min	20mA min	10mA min
Output Leakage Current in Logic "1"				
(T_{min} to T_{max})	200nA max	*	*	2μA max
Logic Common Level Range	-V_S to (+V_S - 4) Volts	*	*	*
Rise/Fall Times (C_T = 0.01μF)				
I_{IN} = 1mA	0.2μs	*	*	*
I_{IN} = 1μA	1μs	*	*	*
POWER SUPPLY				
Voltage, Rated Performance				
Single Supply	4.5V to 36V	*	*	*
Dual Supply	±5 to ±18V	*	*	*
Quiescent Current	1.2mA (2.5mA max)	*	*	*
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGE OPTIONS[6]				
TO-116 Ceramic DIP (D-14)		AD537JD	AD537KD	AD537SD
TO-100 Header (H-10A)	AD537JH		AD537KH	AD537SH

NOTES

*Specifications same as AD537JH.

**Specifications same as AD537K.

Specifications subject to change without notice.

[1] Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I_{IN} = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[2] Guaranteed not tested.

[3] Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor (see Figure 2).

[4] Loading the 1.0 volt or 1mV/K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the external buffer or an external amplifier.

[5] Temperature reference output performance is specified from 0 to +70°C for "J" and "K" devices, -55°C to +125°C for "S" model.

[6] See Section 14 for package outline information.

CIRCUIT OPERATION

Block diagrams of the AD537 are shown above. A versatile operational amplifier (BUF) serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter. The drive current to the current-to-frequency converter (an astable multivibrator) provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 0.1 to 2000μA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a different level than $-V_S$. The "SYNC" input ("D" package only) allows the oscillator to be slaved to an external master oscillator; this input can also be used to shut off the oscillator.

The reference generator uses a band-gap circuit (this allows single-supply operation to 4.5 volts which is not possible with low T.C. zeners) to provide the reference and bias levels for the amplifier and oscillator stages. The reference generator also provides the precision, low T.C. 1.00 volt output and the V_{TEMP} output which tracks absolute temperature at 1mV/K.

V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

The positive voltage input range is from $-V_S$ (ground in single supply operation) to 4 volts below the positive supply. The connection shown in Figure 1 provides a very high (250MΩ) input impedance. The input voltage is converted to the proper drive current at pin 3 by selecting a scaling resistor. The full scale current is 1mA, so, for example a 10 volt range would require a nominal 10kΩ resistor. The trim range required will depend on capacitor tolerance. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive.

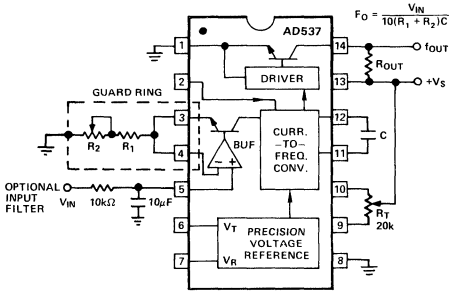


Figure 1. Standard V-F Connection for Positive Input Voltages

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. The maximum frequency is 150kHz. Polystyrene or NPO ceramic capacitors are preferred for T.C. and dielectric absorption; polycarbonate or mica are acceptable; other types will degrade linearity. The capacitor should be wired very close to the AD537.

V-F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

A wide range of negative input voltages can be accommodated with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance since the 1mA F.S. drive current must be supplied by the signal source. However, very large negative voltages beyond the supply can be handled easily; just modify the scaling resistors appropriately. Diode CR1 (HP5082-2811) is necessary for overload and latchup protection for current or voltage inputs.

If the input signal is a true current source, R_1 and R_2 are not used. Full scale calibration can be accomplished by connecting a 200kΩ pot in series with a fixed 27kΩ from pin 7 to $-V_S$ (see calibration section, below).

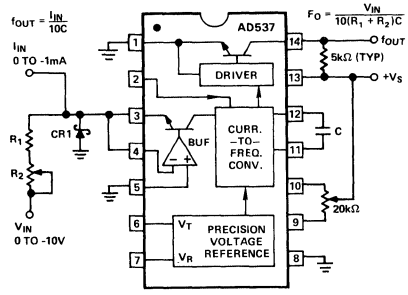


Figure 2. V-F Connections for Negative Input Voltage or Current

CALIBRATION

There are two independent adjustments: scale and offset. The first is trimmed by adjustment of the scaling resistor R and the second by the (optional) potentiometer connected to $+V_S$ and the V_{OS} pins ("D" package only). Precise calibration requires the use of an accurate voltage standard set to the desired FS value and a frequency meter; a scope is useful for monitoring output waveshape. Verification of linearity requires the availability of a switchable voltage source (or a DAC) having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. *Every AD537 is automatically tested for linearity,* and it will not usually be necessary to perform this verification, which is both tedious and time-consuming.

Although drifts are small it is good practice to allow the operating environment to attain stable temperature and to ensure that the supply, source and load conditions are proper. Begin by setting the input voltage to 1/10,000 of full scale. Adjust the offset pot until the output frequency is 1/10,000 of full scale (for example 1Hz for FS of 10kHz). This is most easily accomplished using a frequency meter connected to the output. Then apply the FS input voltage and adjust the gain pot until the desired FS frequency is indicated. In applications where the FS input is small, this adjustment will very slightly affect the offset voltage, due to the input bias current of the buffer amplifier. A change of 1kΩ in R will affect the input by approximately 100μV, which is as much as 0.1% of a 100mV FS range. Therefore, it may be necessary to repeat the offset and scale adjustments for the highest accuracy. The design of the input amplifier is such that the input voltage drift after offset nulling is typically below 1μV/°C.

In some cases the signal may be in the form of a negative current source. This can be handled in a similar way to a negative input voltage. However, the scaling resistor is no longer required, eliminating the capability of trimming full scale in this fashion. Since it will usually be impractical to vary the capacitance, an alternative calibration scheme is needed. This is shown in Figure 3. A resistor-potentiometer connected from the V_R output to $-V_S$ will alter the internal operating conditions in a predictable way, providing the necessary adjustment range. With the values shown, a range of ±4% is available; a larger range can be attained by reducing R1. This technique does not degrade the temperature-coefficient of the converter, and the linearity will be as for negative input voltages. The minimum supply voltage may be used.

Unless it is required to set the input node at exactly ground potential, no offset adjustment is needed. The capacitor C is selected to be 5% below the nominal value; with R2 in its mid-position the output frequency is given by

$$f = \frac{I}{10.5 \times C}$$

where f is in kHz, I is in mA and C is in μF. For example, for a FS frequency of 10kHz at a FS input of 1mA, C = 9500pF. Calibration is effected by applying the full-scale input and adjusting R2 for the correct reading.

This alternative adjustment scheme may also be used when it is desired to present an exact input resistance in the negative-voltage mode. The scaling relationship is then

$$f = \frac{V}{R_{exact}} \cdot \frac{1}{10.5\ C}$$

The calibration procedure is then similar to that used for positive input voltages, except that the scale adjustment is by means of R2.

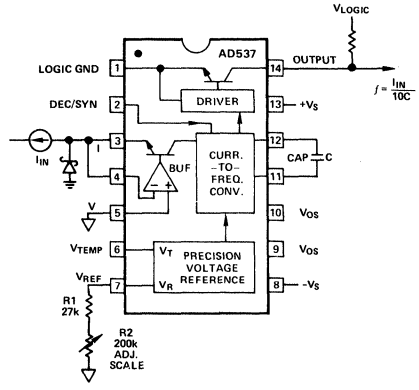


Figure 3. Scale Adjustment for Current Inputs

INPUT PROTECTION

The AD537 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions.

The $-V_{IN}$, $+V_{IN}$ and I_{IN} pins should not be driven more than 300mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. The AD537 can be protected from "below $-V_S$" inputs by a Schottky diode, CR1 (HP5082-2811) as shown in Figure 3. It is also desirable not to drive $+V_{IN}$, $-V_{IN}$ and I_{IN} above $+V_S$. In operation, the converter will become very nonlinear for inputs above ($+V_S$ -3.5V). Control currents above 2mA will also cause nonlinearity.

The 80dB dynamic range of the AD537 guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to the input. For example, when scaled to accept a FS input of 1V, the -80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter and a guard ring around the I_{IN} or $-V_{IN}$ pins. For a FS of 10kHz a single-pole filter with a time-constant of 100ms (Figure 2) will be suitable, but the optimum configuration will depend on the application and type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA (1mV) full integration of additive input noise occurs.

The AD537 is somewhat susceptible to interference from other signals. The most sensitive nodes (besides the inputs) are the capacitor terminals and the SYNC pin. The timing capacitor should be located as close as possible to the AD537 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. The SYNC pin should be decoupled through a 0.005μF (or larger) capacitor to pin 13 ($+V_S$). This minimizes the possibility that the AD537 will attempt to synchronize to a spurious signal. This precaution is unnecessary on the metal can package since the SYNC function is not brought out to a package pin and is thus not susceptible to pickup.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD537.

A decoupling capacitor may also be useful from $+V_S$ to SYNC in those applications where very low cycle-to-cycle period variation (jitter) is demanded. By placing a capacitor across $+V_S$ and SYNC this noise is reduced. On the 10kHz FS range, a 6.8μF capacitor reduces the jitter to one in 20,000 which is adequate for most applications. A tantalum capacitor should be used to avoid errors due to dc leakage.

NONLINEARITY SPECIFICATION

The preferred method for specifying linearity error is in terms of the maximum deviation from the ideal relationship after calibrating the converter at full scale and "zero". This error will vary with the full scale frequency and the mode of operation. The AD537 operates best at a 10kHz full scale frequency with a negative voltage input; the linearity is typically within ±0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicates in the Specifications table. The shape of a typical linearity plot is given in Figure 4.

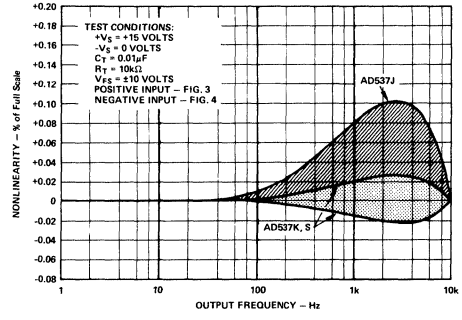


Figure 4a. Typical Nonlinearity Error Envelopes with 10kHz F.S. Output

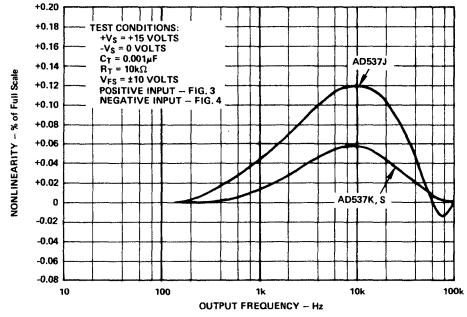
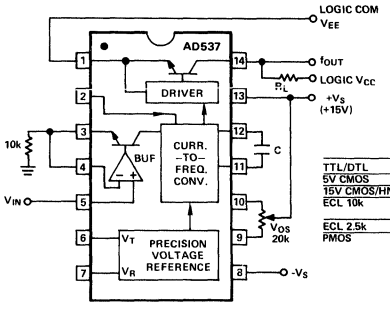


Figure 4b. Typical Nonlinearity Error with 100kHz F.S. Output

OUTPUT INTERFACING CONSIDERATIONS

The design of the output stage allows easy interfacing to all digital logic families. The collector and emitter of the output NPN transistor are both uncommitted; the emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$. The open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can supply up to 20mA (10mA for "H" package) at a maximum saturation voltage of 0.4 volts. The stage limits the output current at 25mA; it can handle this limit indefinitely without damaging the device.

Figure 5 shows the AD537 with a standard 0 to +10 volt input connection and the output stage connections. The values for the logic common voltage, pull-up resistor, positive logic level, and $-V_S$ supply are given in the accompanying chart for several logic forms.



	V_{CC}	V_{EE}	R_L	$-V_S$
TTL/DTL	+5	GND	5k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS/HNIL	+15	GND	10k	GND
ECL 10k	0	-8	5k	-8 to -15
ECL 2.5k	+1.3	-2	5k	-5
PMOS	0	-15	10k	-15

Figure 5. Interfacing Standard Logic Families

APPLICATIONS

The diagrams and descriptions of the following applications are provided to stimulate the discerning engineer with alternative circuit design ideas. "Applications of the AD537 IC Voltage-to-Frequency Converter", available from Analog Devices on request, covers a wider range of topics and concepts in data conversion and data transmission using voltage-to-frequency converters.

TRUE TWO-WIRE DATA TRANSMISSION

Figure 6 shows the AD537 in a true two-wire data transmission scheme. The twisted-pair transmission lines serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation. The PNP circuit at the receiving end represents a fairly simple way for converting the current modulation back into a voltage square wave which will drive digital logic directly. The 0.6 volt square wave which will appear on the supply line at the device terminals does not affect the performance of the AD537 because of its excellent supply rejection. Also, note that the circuit operates at nearly constant average power regardless of frequency.

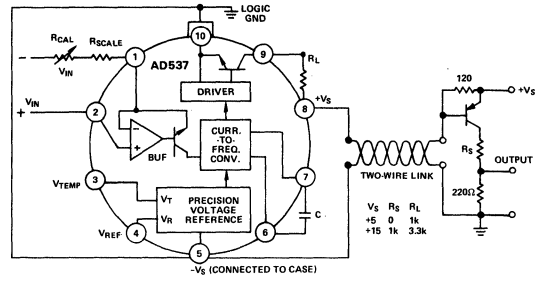


Figure 6. True Two-Wire Operation

F-V CONVERTERS

The AD537 can be used as a high linearity VCO in a phase-locked loop to accomplish frequency-to-voltage conversion. By operating the loop without a low-pass filter in the feedback path (first-order system), it can lock to any frequency from zero to an upper limit determined by the design, responding in three or four cycles to a step change of input frequency. In practice, the overall response time is determined by the characteristics of the averaging filter which follows the PLL.

Figure 7 shows a connection using a low-power TTL quad open-collector nand gate which serves as the phase comparator. The input signal should be a pulse train or square wave with characteristics similar to TTL or 5-volt CMOS outputs. Any duty cycle is acceptable, but the minimum pulse width is 40μs. The output voltage is one volt for a 10kHz input frequency. The output as shown here is at a fairly high impedance level; for many situations an additional buffer may be required.

Trimming is similar to V-F application trimming. First set the V_{OS} trimmer to mid-scale. Apply a 10kHz input frequency and trim the 2kΩ potentiometer for 1.00 volts out. Then apply a 10Hz waveform and trim the V_{OS} for 1mV out. Finally, retrim the full scale output at 10kHz. Other frequency scales can be obtained by appropriate scaling of timing components.

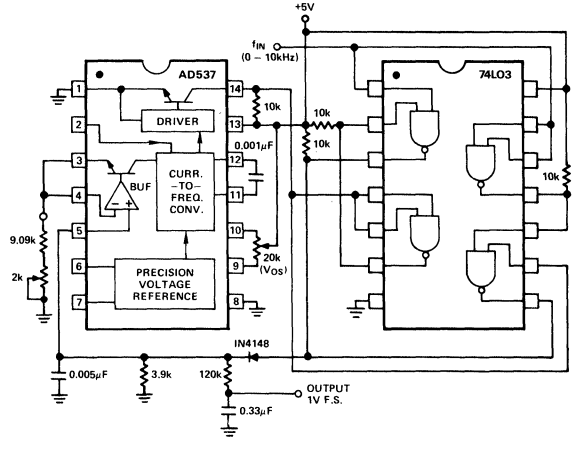


Figure 7. 10kHz F-V Converter

TEMPERATURE-TO-FREQUENCY CONVERSION

The linear temperature-proportional output of the AD537 can be used as shown in these applications to perform various direct temperature-to-frequency conversion functions; it can also be used with other external connections in a temperature sensing or compensation scheme. If the sensor output is used externally, it should be buffered through an op amp since loading that point will cause significant error in the sensor output as well as in the main V-F converter circuitry.

An absolute temperature (Kelvin)-to-frequency converter is very easily accomplished, as shown in Figure 8. The 1mV per K output serves as the input to the buffer amplifier, which then scales the oscillator drive current to a nominal 298μA at +25°C (298K). Use of a 1000pF capacitor results in a corresponding frequency of 2.98kHz. Setting the single 2kΩ trimmer for the correct frequency at a well-defined temperature near +25°C will normally result in an accuracy of ±2°C from -55°C to +125°C (using an AD537S). An NPO ceramic capacitor is recommended to minimize nonlinearity due to capacitance drift.

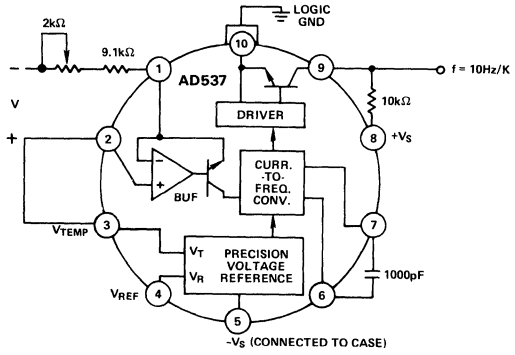


Figure 8. Absolute Temperature to Frequency Converter

OFFSET TEMPERATURE SCALES

Many other temperature scales can be set up by offsetting the temperature output with the voltage reference output. Such a scheme is shown by the Celsius-to-frequency converter in Figure 9. Corresponding component values for a Fahrenheit-to-frequency converter which give 10Hz/°F are given in parentheses.

A simple calibration procedure which will provide ±2°C accuracy requires substitution of a 7.27k resistor for the series combination of the 6.04k with the 2k trimmer; then simply set the 500Ω trimmer to give 250Hz at +25°C.

High accuracy calibration procedure:

1. Measure room temperature in K.
2. Measure temperature output at pin 6 at that temperature.
3. Calculate offset adjustment as follows:

$$\text{Offset Voltage (mV)} = \frac{V_{TEMP}\ (\text{pin 6})\ (\text{mV})}{\text{Room temp (K)}} \times 273.2$$

4. Temporarily disconnect 49Ω resistor (or 500Ω pot) and trim 2kΩ pot to give the offset voltage at the indicated node. Reconnect 49Ω resistor.
5. Adjust slope trimmer to give proper frequency at room temperature (+25°C = 250Hz).
   Adjustment for °F or any other scale is analogous.

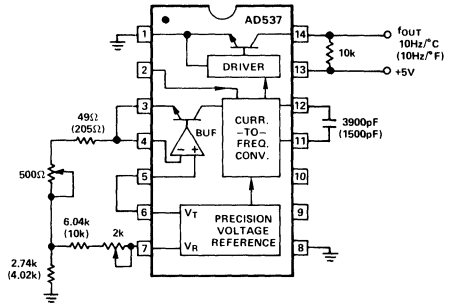


Figure 9. Offset Temperature Scale Converters-Centigrade and (Fahrenheit) to Frequency

SYNCHRONOUS OPERATION

The SYNC terminal at pin 2 of the DIP package can be used to synchronize a free running AD537 to a master oscillator, either at a multiple or a sub-multiple of the primary frequency. The preferred connection is shown in Figure 10. The diodes are used to produce the proper drive magnitude from high level signals. The SYNC terminal can also be used to shut off the oscillator. Shorting the terminal to $+V_S$ will stop the oscillator, and the output will go high (output NPN off).

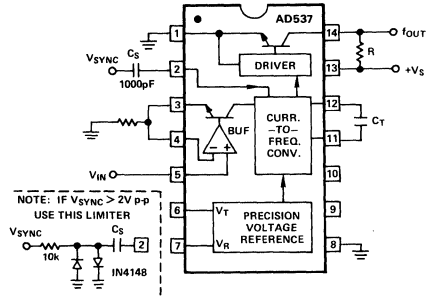


Figure 10. Connection for Synchronous Operation

Figure 11 shows the maximum pull-in range available at a given signal level; the optimum signal is a 0.8 to 1.0 volt square wave; signals below 0.1 volt will have no effect; signals above 2 volts p-p will disable the oscillator. The AD537 can normally be synchronized to a signal which forces it to a higher frequency up to 30% above the nominal free-running frequency, it can only be brought down about 1-2%.

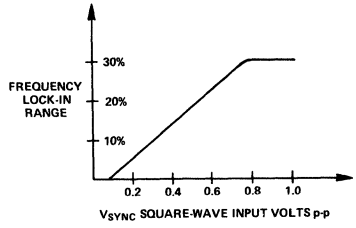


Figure 11. Maximum Frequency Lock-In Range Versus Sync. Signal

LINEAR PHASE LOCKED LOOP

The phase-locked-loop F/V circuit described earlier operates from an essentially noise-free binary input. PLL's are also used to extract frequency information from a noisy analog signal. To do this, the digital phase-comparator must be replaced by a linear multiplier. In the implementation shown in Figure 12, the triangular waveform appearing across the timing capacitor is used as one of the multiplier inputs; the signal provides the other input. It can be shown that the mean value of the multiplier output is zero when the two signals are in quadrature. In this condition, the ripple in the error signal is also quite small. Thus, the voltage at pin 5 is essentially zero, and the frequency is determined primarily by the current in the timing resistor, controlled either manually or by a control voltage.

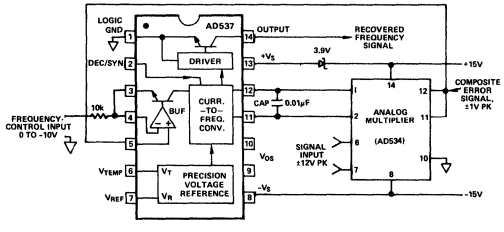


Figure 12. Linear Phase-Locked Loop

Noise on the input signal affects the loop operation only slightly; it appears as noise in the timing current, but this is averaged out by the timing capacitor. On the other hand, if the input frequency changes there is a net error voltage at pin 5 which acts to bring the oscillator back into quadrature. Thus, the output at pin 14 is a noise-free square-wave having exactly the same frequency as the input signal. The effectiveness of this circuit can be judged from Figure 13 which shows the response to an input of 1V rms 1kHz sinusoid plus 1V rms Gaussian noise. The positive supply to the AD537 is reduced by about 4V in order to keep the voltages at pins 11 and 12 within the common-mode range of the AD534.

Since this is also a first-order loop the circuit possesses a very wide capture range. However, even better noise-integrating properties can be achieved by adding a filter between the multiplier output and the VCO input. Details of suitable filter characteristics can be found in the standard texts on the subject.

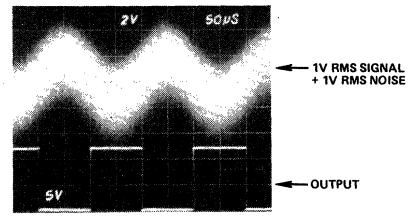


Figure 13. Performance of AD537 Linear Phase-Locked Loop

By connecting the multiplier output to the lower end of the timing resistor and moving the control input to pin 5, a high-resistance frequency-control input is made available. However, due to the reduced supply voltage, this input cannot exceed +6V.

TRANSDUCER INTERFACE

The AD537 was specifically designed to accept a broad range of input signals, particularly small voltage signals, which may be converted directly (unlike many V-F converters which require signal pre-conditioning). The 1.00V stable reference output is also useful in interfacing situations, and the high input resistance allows non-loading interfacing from a source of varying resistance, such as the slider of a potentiometer.

THERMOCOUPLE INPUT

The output of a Chromel-Constantan (Type E) thermocouple, using a reference junction at 0°C, varies from 0 to 53.14mV over the temperature range 0 to +700°C with a slope of 80.678µV/degree over most of its range and some nonlinearity over the range 0 to +200°C. For this example, we assume that it is desired to indicate temperature in Degrees Celsius using a counter/display with a 100ms gate width. Thus, the V-F converter must deliver an output of 7kHz for an input of 53.14mV. If very precise operation down to 0°C is imperative, some sort of linearizing is necessary (see, for example, Analog Devices' Nonlinear Circuits Handbook, pp92-97) but in many cases operation is only needed over part of the range.

The circuit shown in Figure 14 provides good accuracy from +300°C to +700°C. The extrapolation of the temperature-voltage curve back to 0°C shows that an offset of -3.34mV is required to fit the curve most exactly. This small amount of voltage can be introduced without an additional calibration step using the +1.00V output of the AD537. To adjust the scale, the thermocouple should be raised to a known reference temperature near 500°C and the frequency adjusted to value using R1. The error should be within ±0.2% over the range 400°C to 700°C.

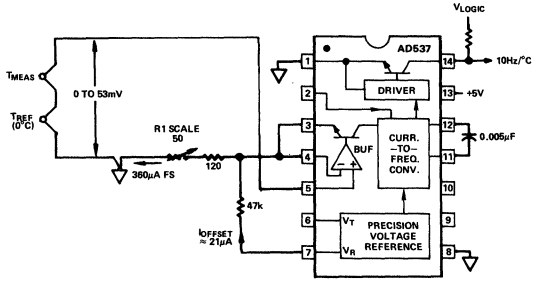


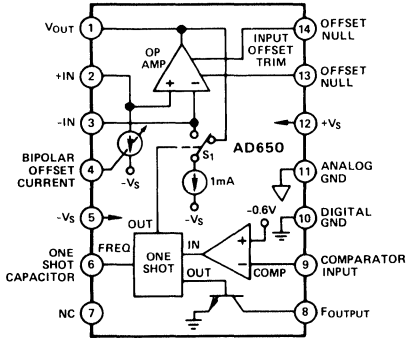
Figure 14. Thermocouple Interface with First-Order Linearization

Voltage-to-Frequency and Frequency-to-Voltage Converter

AD650

FEATURES
- **V/F Conversion to 1MHz**
- **Reliable Monolithic Construction**
- **Very Low Nonlinearity**
  - **0.002% typ at 10kHz**
  - **0.005% typ at 100kHz**
  - **0.07% typ at 1MHz**
- **Input Offset Trimmable to Zero**
- **CMOS or TTL Compatible**
- **Unipolar, Bipolar, or Differential V/F**
- **V/F or F/V Conversion**
- **Available in Surface Mount**

AD650 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD650 V/F/V (voltage-to-frequency or frequency-to-voltage converter) provides a combination of high frequency operation and low nonlinearity previously unavailable in monolithic form. The inherent monotonicity of the V/F transfer function makes the AD650 useful as a high-resolution analog-to-digital converter. A flexible input configuration allows a wide variety of input voltage and current formats to be used, and an open-collector output with separate digital ground allows simple interfacing to either standard logic families or opto-couplers.

The linearity error of the AD650 is typically 20ppm (0.002% of full scale) and 50ppm (0.005%) maximum at 10kHz full scale. This corresponds to approximately 14-bit linearity in an analog-to-digital converter circuit. Higher full-scale frequencies or longer count intervals can be used for higher resolution conversions. The AD650 has a useful dynamic range of six decades allowing extremely high resolution measurements. Even at 1MHz full scale, linearity is guaranteed less than 1000ppm (0.1%) on the AD650KN, KP, BD and SD grades.

In addition to analog-to-digital conversion, the AD650 can be used in isolated analog signal transmission applications, phased-locked-loop circuits, and precision stepper motor speed controllers. In the F/V mode, the AD650 can be used in precision tachometer and FM demodulator circuits.

The input signal range and full-scale output frequency are user-programmable with two external capacitors and one resistor. Input offset voltage can be trimmed to zero with an external potentiometer.

The AD650JN and AD650KN are offered in a plastic 14-pin DIP package. The AD650JP and AD650KP are available in a 20-pin plastic leaded chip carrier (PLCC). Both plastic packaged versions of the AD650 are specified for the commerical (0 to +70°C) temperature range. For industrial temperature range (−25°C to +85°C) applications, the AD650AD and AD650BD are offered in a ceramic package. The AD650SD is specified for the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. In addition to very high linearity, the AD650 can operate at full scale output frequency up to 1MHz. The combination of these two features makes the AD650 an inexpensive solution for applications requiring high resolution monotonic A/D conversion.
2. The AD650 has a very versatile architecture that can be configured to accommodate bipolar, unipolar, or differential input voltages, or unipolar input currents.
3. TTL or CMOS compatibility is achieved using an open collector frequency output. The pullup resistor can be connected to voltages up to +30V, or +15V or +5V for conventional CMOS or TTL logic levels.
4. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the AD650.
5. The AD650 provides separate analog and digital grounds. This feature allows prevention of ground loops in real-world applications.

SPECIFICATIONS (@ +25°C with $V_S = \pm 15V$ unless otherwise noted)

Model	AD650J/AD650A Min	AD650J/AD650A Typ	AD650J/AD650A Max	AD650K/AD650B Min	AD650K/AD650B Typ	AD650K/AD650B Max	AD650S Min	AD650S Typ	AD650S Max	Units
DYNAMIC PERFORMANCE										
Full Scale Frequency Range			1			1			1	MHz
Nonlinearity[1] f_{max} = 10kHz		0.002	0.005		0.002	0.005		0.002	0.005	%
100kHz		0.005	**0.02**		0.005	**0.02**		0.005	**0.02**	%
500kHz		0.02	0.05		0.02	0.05		0.02	0.05	%
1MHz		0.1			0.05	**0.1**		0.05	**0.1**	%
Full Scale Calibration Error[2], 100kHz		±5			±5			±5		%
1MHz		±10			±10			±5		%
vs. Supply[3]	−0.002		**+0.002**	−0.002		**+0.002**	−0.002		**+0.002**	% of FSR/V
vs. Temperature										
A, B, and S Grades										
at 10kHz			±75			±75			**±75**	ppm/°C
at 100kHz			±150			±150			**±150**	ppm/°C
J and K Grades										
at 10kHz		±75			±75					ppm/°C
at 100kHz		±150			±150					ppm/°C
BIPOLAR OFFSET CURRENT										
Activated by 1.24kΩ between pins 4 and 5	0.45	0.5	0.55	0.45	0.5	0.55	0.45	0.5	0.55	mA
DYNAMIC RESPONSE										
Maximum Settling Time for Full Scale										
Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
Overload Recovery Time										
Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
ANALOG INPUT AMPLIFIER (V/F Conversion)										
Current Input Range (Figure 1)	0		+0.6	0		+0.6	0		+0.6	mA
Voltage Input Range (Figure 5)	−10		0	−10		0	−10		0	V
Differential Impedance		2MΩ‖10pF			2MΩ‖10pF			2MΩ‖10pF		
Common Mode Impedance		1000MΩ‖10pF			1000MΩ‖10pF			1000MΩ‖10pF		
Input Bias Current										
Noninverting Input		40	**100**		40	**100**		40	**100**	nA
Inverting Input		±8	**±20**		±8	**±20**		±8	**±20**	nA
Input Offset Voltage										
(Trimmable to Zero)			**±4**			**±4**			**±4**	mV
vs. Temperature (T_{min} to T_{max})		±30				±30			±30	µV/°C
Safe Input Voltage		$\pm V_S$			$\pm V_S$			$\pm V_S$		C
COMPARATOR (F/V Conversion)										
Logic "0" Level	$-V_S$		−1	$-V_S$		−1	$-V_S$		+1	V
Logic "1" Level	0		$+V_S$	0		$+V_S$	0		$+V_S$	V
Pulse Width Range[4]	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	µs
Input Impedance		250			250			250		kΩ
OPEN COLLECTOR OUTPUT (V/F Conversion)										
Output Voltage in Logic "0"										
$I_{SINK} \leq 8mA$, T_{min} to T_{max}			0.4			0.4			0.4	V
Output Leakage Current in Logic "1"			**100**			**100**			**100**	nA
Voltage Range[5]	0		+36	0		+36	0		+36	V
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (1500Ω min load resistance)	0		+10	0		+10	0		+10	V
Source Current (750Ω max load resistance)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
POWER SUPPLY										
Voltage, Rated Performance	±9		**±18**	±9		**±18**	±9		**±18**	V
Quiescent Current			**8**			**8**			**8**	mA
TEMPERATURE RANGE										
Rated Performance – N Package	0		+70	0		+70				°C
D Package	−25		+85	−25		+85	−55		+125	°C
Storage – N Package	−25		+85	−25		+85				°C
D Package	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS[6]										
PLCC (P-20A)		AD650JP			AD650KP					
Plastic DIP (N-14)		AD650JN			AD650KN					
Ceramic DIP (D-14)		AD650AD			AD650BD			AD650SD		

NOTES

[1]Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.
[2]Full scale calibration error adjustable to zero.
[3]Measured at full scale output frequency of 10kHz.
[4]Refer to F/V conversion section of the text.
[5]Referred to digital ground.
[6]See Section 14 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Part Number	Gain Tempco ppm/°C 100kHz	1MHz Linearity	Specified Temperature Range °C	Package
AD650JN	150 typ	0.1% typ	0 to +70	Plastic DIP
AD650KN	150 typ	0.1% max	0 to +70	Plastic DIP
AD650JP	150 typ	0.1% typ	0 to +70	PLCC
AD650KP	150 typ	0.1% max	0 to +70	PLCC
AD650AD	150 max	0.1% typ	−25 to +85	Ceramic
AD650BD	150 max	0.1% max	−25 to +85	Ceramic
AD650SD	150 max	0.1% max	−55 to +125	Ceramic

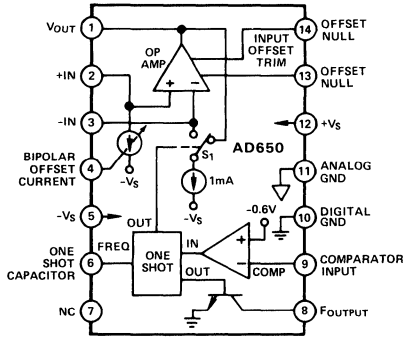
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Storage Temperature Ceramic . . . . . −55°C to +165°C
Plastic . . . . . −25°C to +125°C
Differential Input Voltage (Pins 2 & 3) . . . . . ±10V
Maximum Input Voltage . . . . . $\pm V_S$
Open Collector Output Voltage Above Digital GND . . 36V
Current 50mA
Amplifier Short Ckt to Ground . . . . . Indefinite
Comparator Input Voltage (Pin 9) . . . . . $\pm V_S$

CIRCUIT OPERATION

UNIPOLAR CONFIGURATION

The AD650 is a *charge balance* voltage-to-frequency converter. In the connection diagram shown in Figure 1, or the block diagram of Figure 2a, the input signal is converted into an equivalent current by the input resistance R_{IN}. This current is *exactly* balanced by an internal feedback current delivered in short, timed bursts from the switched 1mA internal current source. These bursts of current may be thought of as precisely defined packets of charge. The required number of charge packets, each producing one pulse of the output transistor, depends upon the amplitude of the input signal. Since the number of charge packets delivered per unit time is dependent on the input signal amplitude, a linear voltage-to-frequency transformation will be accomplished. The frequency output is furnished via an open collector transistor.



AD650 Pin Configuration

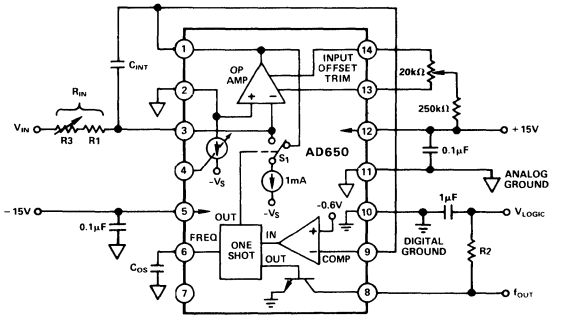


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

A more rigorous analysis demonstrates how the charge balance voltage-to-frequency conversion takes place.

A block diagram of the device arranged as a V to F converter is shown in Figure 2a. The unit is comprised of an input integrator, a current source and steering switch, a comparator and a one-shot. When the output of the one-shot is low, the current steering switch S_1 diverts all the current to the output of the op amp; this is called the Integration Period. When the one-shot has been triggered and its output is high, the switch S_1 diverts all the current to the summing junction of the op amp; this is called the Reset Period. The two different states are shown in Figure 2 along with the various branch currents. It should be noted that the output current from the op amp is the same for either state, thus minimizing transients.

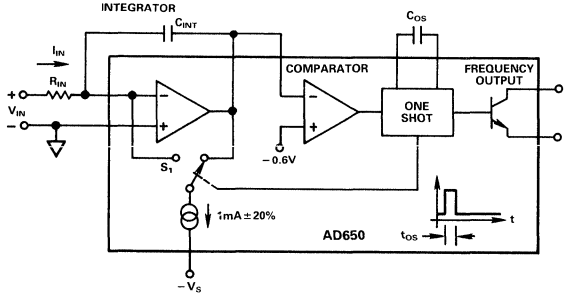


Figure 2a. Block Diagram

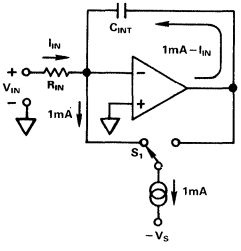


Figure 2b. Reset Mode

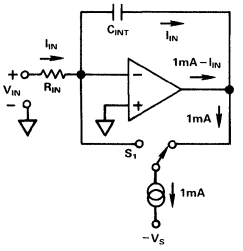


Figure 2c. Integrate Mode

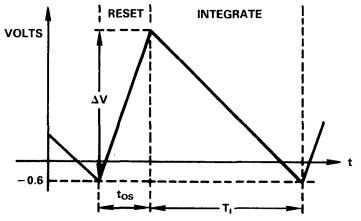


Figure 2d. Voltage Across C_{INT}

The positive input voltage develops a current ($I_{IN} = V_{IN}/R_{IN}$) which charges the integrator capacitor C_{INT}. As charge builds up on C_{INT}, the output voltage of the integrator ramps downward towards ground. When the integrator output voltage (pin 1) crosses the comparator threshold (−0.6 volt) the comparator triggers the one shot, whose time period, t_{OS} is determined by the one shot capacitor C_{OS}.

Specifically, the one shot time period is:

$$t_{OS} = C_{OS} \times 6.8 \times 10^3 \, sec/F + 3.0 \times 10^{-7} sec \quad (1)$$

The Reset Period is initiated as soon as the integrator output voltage crosses the comparator threshold, and the integrator ramps upward by an amount:

$$\Delta V = t_{OS} \cdot \frac{dV}{dt} = \frac{t_{OS}}{C_{INT}} \left(1mA - I_{IN}\right) \quad (2)$$

After the Reset Period has ended, the device starts another Integration Period, as shown in Figure 2, and starts ramping downward again. The amount of time required to reach the comparator threshold is given as:

$$T_I = \frac{\Delta V}{\frac{dV}{dt}} = \frac{t_{OS}/C_{INT}(1mA - I_{IN})}{I_{IN}/C_{INT}} = t_{OS}\left(\frac{1mA}{I_{IN}} - 1\right) \quad (3)$$

The output frequency is now given as:

$$f_{OUT} = \frac{1}{t_{OS} + T_I} = \frac{I_{IN}}{t_{OS} \times 1mA} = 0.15 \frac{F \cdot Hz}{A} \frac{V_{IN}/R_{IN}}{C_{OS} + 4.4 \times 10^{-11} F} \quad (4)$$

Note that C_{INT}, the integration capacitor has no effect on the transfer relation, but merely determines the amplitude of the sawtooth signal out of the integrator.

One Shot Timing

A key part of the preceding analysis is the one shot time period that was given in equation (1). This time period can be broken down into approximately 300ns of propagation delay, and a second time segment dependent linearly on timing capacitor C_{OS}. When the one shot is triggered, a voltage switch that holds pin 6 at analog ground is opened allowing that voltage to change. An internal 0.5mA current source connected to pin 6 then draws its current out of C_{OS}, causing the voltage at pin 6 to decrease linearly. At approximately −3.4V, the one shot resets itself, thereby ending the timed period and starting the V/F conversion cycle over again. The total one shot time period can be written mathematically as:

$$t_{OS} = \frac{\Delta V \, C_{OS}}{I_{DISCHARGE}} + T_{GATE\ DELAY} \quad (5)$$

substituting actual values quoted above,

$$t_{OS} = \frac{-3.4V \times C_{OS}}{-0.5 \times 10^{-3} A} + 300 \times 10^{-9} sec \quad (6)$$

This simplifies into the timed period equation given above.

COMPONENT SELECTION

Only four component values must be selected by the user. These are input resistance R_{IN}, timing capacitor C_{OS}, logic resistor R_2, and integration capacitor C_{INT}. The first two determine the input voltage and full scale frequency, while the last two are determined by other circuit considerations.

Of the four components to be selected, R_2 is the easiest to define. As a pull up resistor, it should be chosen to limit the current through the output transistor to 8mA if a TTL maximum V_{OL} of 0.4V is desired. For example, if a 5V logic supply is used, R_2 should be no smaller than 5V/8mA or 625Ω. A larger value can be used if desired.

R_{IN} and C_{OS} are the only two parameters available to set the full scale frequency to accommodate the given signal range. The

"swing" variable that is affected by the choice of R_{IN} and C_{OS} is nonlinearity. The selection guide of Figure 3 shows this quite graphically. In general, larger values of C_{OS} and lower full scale input currents (higher values of R_{IN}) provide better linearity. In Figure 3, the implications of four different choices of R_{IN} are shown. Although the selection guide is set up for a unipolar configuration with a zero to 10V input signal range, the results can be extended to other configurations and input signal ranges. For a full scale frequency of 100kHz (corresponding to 10V input), you can see that among the available choices, $R_{IN}=20k$ and $C_{OS}=620pF$ gives the lowest nonlinearity, 0.0038%. Also, if you wish to use the highest frequency that will give the 20ppm minimum nonlinearity, it is approximately 33kHz (40.2kΩ and 1000pF).

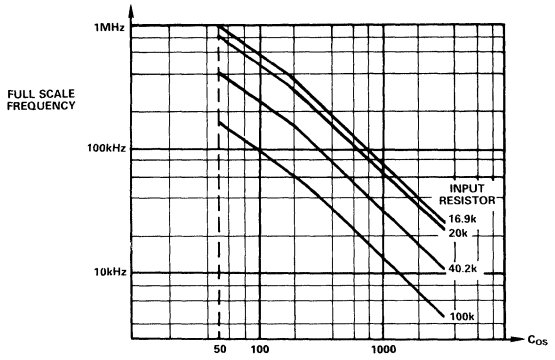


Figure 3a. Full Scale Frequency vs. C_{OS}

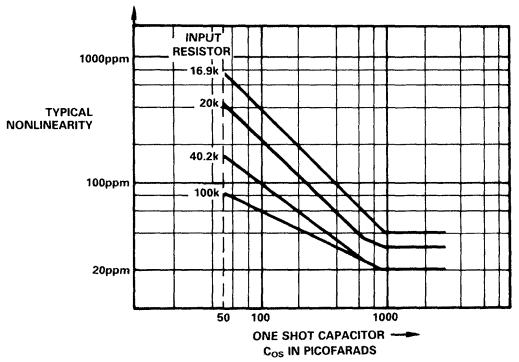


Figure 3b. Typical Nonlinearity vs. C_{OS}

For input signal spans other than 10V, the input resistance must be scaled proportionately. For example, if 100kΩ is called out for a 0–10V span, 10k would be used with a 0–1V span, or 200kΩ with a ±10V bipolar connection.

The last component to be selected is the integration capacitor C_{INT}. In almost all cases, the best value for C_{INT} can be calculated using the equation:

$$C_{INT}=\frac{10^{-4}F/sec}{f_{MAX}} \quad (1000pF \text{ minimum}) \qquad (7)$$

When the proper value for C_{INT} is used, the charge balance architecture of the AD650 provides continuous integration of the input signal, hence large amounts of noise and interference can be rejected. If the output frequency is measured by counting pulses during a constant gate period, the integration provides infinite normal mode rejection for frequencies corresponding to the gate period and its harmonics. However, if the integrator stage becomes saturated by an excessively large noise pulse, the continuous integration of the signal will be interrupted, allowing the noise to appear at the output. If the approximate amount of noise that will appear on C_{INT} is known (V_{NOISE}), the value of C_{INT} can be checked using the following inequality:

$$C_{INT} > \frac{t_{OS}\times 1\times 10^{-3}A}{+V_S-3V-V_{NOISE}} \qquad (8)$$

For example, consider an application calling for a maximum frequency of 75kHz, a 0–1 volt signal range, and supply voltages of only ±9 volts. The component selection guide of Figure 3 is used to select 2.0kΩ for R_{IN} and 1000pF for C_{OS}. This results in a one shot time period of approximately 7μs. Substituting 75kHz into equation 7 yields a value of 1300pF for C_{INT}. When the input signal is near zero, 1mA flows through the integration capacitor to the switched current sink during the reset phase, causing the voltage across C_{INT} to increase by approximately 5.5 volts. Since the integrator output stage requires approximately 3 volts head room for proper operation, only 0.5 volt margin remains for integrating extraneous noise on the signal line. A negative noise pulse at this time might saturate the integrator, causing an error in signal integration. Increasing C_{INT} to 1500 or 2000pF will provide much more noise margin, thereby eliminating this potential trouble spot.

BIPOLAR V/F

Figure 4 shows how the internal bipolar current sink is used to provide a half-scale offset for a ±5V signal range, while providing a 100kHz maximum output frequency. The nominally 0.5mA (±10%) offset current sink is enabled when a 1.24kΩ resistor is connected between pins 4 and 5. Thus, with the grounded 10kΩ nominal resistance shown, a −5V offset is developed at pin 2. Since pin 3 must also be at −5V, the current through R_{IN} is 10V/40kΩ = +0.25mA at V_{IN} = +5V, and 0mA at V_{IN} = −5V.

Components are selected using the same guidelines outlined for the unipolar configuration with one alteration. The voltage

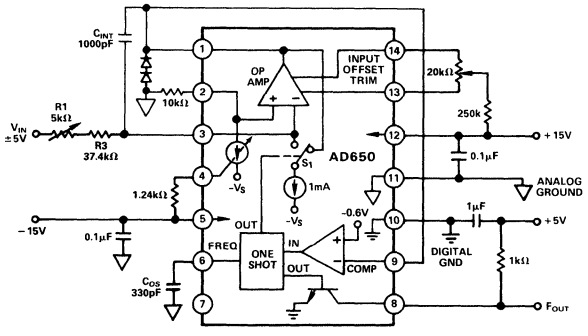


Figure 4. Connections for ±5V Bipolar V/F with 0 to 100kHz TTL Output

across the total signal range must be equated to the maximum input voltage in the unipolar configuration. In other words, the value of the input resistor R_{IN} is determined by the input voltage span, not the maximum input voltage. A diode from pin 1 to ground is also recommended. This is discussed further under "Other Circuit Conditions".

As in the unipolar circuit, R_{IN} and C_{OS} must have low temperature coefficients to minimize the overall gain drift. The 1.24kΩ resistor used to activate the 0.5mA offset current should also have a low temperature coefficient. The bipolar offset current has a temperature coefficient of approximately −200ppm/°C.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 5 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full scale output frequency occurs at negative full scale input, and zero output frequency corresponds with zero input voltage.

A very high impedance signal source may be used since it only drives the noninverting integrator input. Typical input impedance at this terminal is 1GΩ or higher. For V/F conversion of positive input signals using the connection diagram of Figure 1, the signal generator must be able to source the integration current to drive the AD650. For the negative V/F conversion circuit of Figure 5, the integration current is drawn from ground through R1 and R3, and the active input is high impedance.

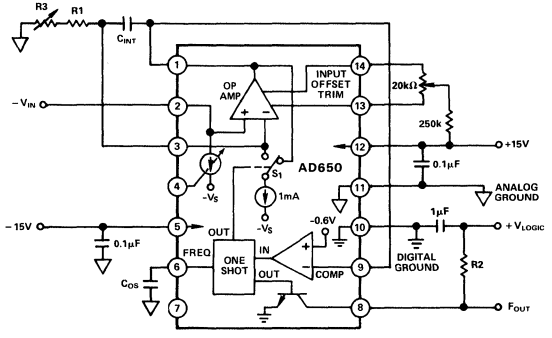


Figure 5. Connection Diagram for V/F Conversion, Negative Input Voltage

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in a previous section. For best operating results use component equations listed in that section.

F/V CONVERSION

The AD650 also makes a very linear frequency-to-voltage converter. Figure 6 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshhold going negative, the one shot is activated and switches 1mA into the integrator input for a measured time period (determined by C_{OS}). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F conversion section.

The circuit of Figure 6 can be biased to accommodate almost any input signal waveform. With a TTL input, the 1000pF coupling capacitor and 2.2kΩ resistor creates a clean negative

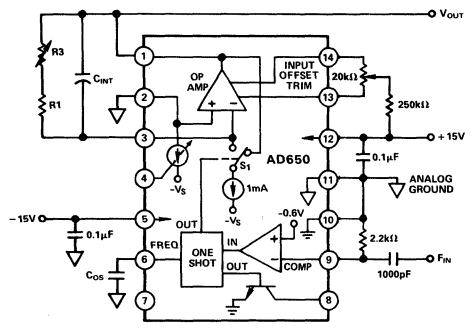


Figure 6. Connection Diagram for F/V Conversion

spike that triggers the one shot on negative going edges. For input signals with slower edges, a larger capacitor and/or resistor may be used as long as the comparator is never exposed to a voltage lower than −0.6V for longer than the one shot time period. If this happens, the one shot will trigger itself more than once per cycle, creating discontinuities in the F/V transfer function. An input pulse greater than 100ns but less than $0.3 \times t_{OS}$ is recommended (t_{OS} is defined by equation 1 in the circuit operation section, unipolar configuration).

HIGH FREQUENCY OPERATION

Proper RF techniques must be observed when operating the AD650 at or near its maximum frequency of 1MHz. Lead lengths must be kept as short as possible, especially on the one shot and integration capacitors, and at the integrator summing junction. In addition, at maximum output frequencies above 500kHz, a 3.6kΩ pulldown resistor from pin 1 to $-V_S$ is required (see Figure 7). The additional current drawn through the pulldown resistor reduces the op amp's output impedance and improves its transient response.

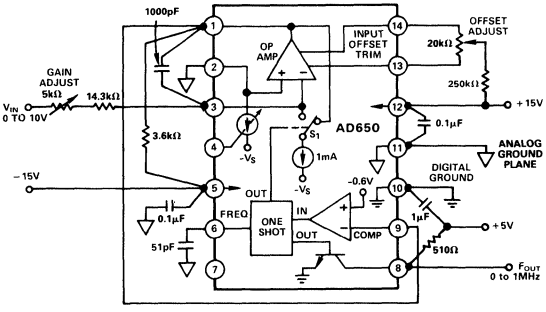


Figure 7. 1MHz V/F Connection Diagram

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD650.

In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the AD650 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to

exploit the full linearity and dynamic range of the AD650. Although some types of circuits may operate satisfactorily with power supply decoupling at only one location on each circuit board, such practice is strongly discouraged in high accuracy analog design.

Separate digital and analog grounds are provided on the AD650. The emitter of the open collector frequency output transistor is the only node returned to the digital ground. All other signals are referred to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. As much as several hundred millivolts of noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At 1MHz full scale, it is necessary to use a pull-up resistor of about 500Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10mA. This much current being switched will surely cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20nH per inch; a current of 10mA being switched in 50ns at the end of 12 inches of 20 gauge wire will produce a voltage spike of 50mV. The separate digital ground of the AD650 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD650 package. A 1μF to 10μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground – pin 10. The pull-up resistor should be connected directly to the frequency output – pin 8. The lead lengths on the bypass capacitor and the pull up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less self-inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (pin 10) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current and cannot radiate RFI. There may also be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause any problem. In fact, the AD650 will tolerate as much as 0.25 volt dc potential difference between the analog and digital grounds. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (pin 11) at the package. All of the signal grounds should be tied directly to pin 11, especially the one-shot capacitor. More information on proper grounding and reduction of interference can be found in reference 1.

TEMPERATURE COEFFICIENTS

The drift specifications of the AD650 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C_{OS} directly affect the overall temperature stability. In the application of Figure 2, a 10ppm/°C input resistor used with a 100ppm/°C capacitor may result in a maximum overall circuit gain drift of:

150ppm/°C (AD650A) + 100ppm/°C (C_{OS}) + 10ppm/°C (R_{IN}) = 260ppm/°C

In bipolar configuration, the drift of the 1.24kΩ resistor used to activate the internal bipolar offset current source will directly affect the value of this current. This resistor should be matched to the resistor connected to the op amp noninverting input (pin 2), see Figure 4. That is, the temperature coefficients of these two resistors should be equal. If this is the case, then the effects of the temperature coefficients of the resistors cancel each other, and the drift of the offset voltage developed at the op amp non-inverting input will be determined solely by the AD650. Under these conditions the TC of the bipolar offset voltage is typically −200ppm/°C and is a maximum of −300ppm/°C. The offset voltage always decreases in magnitude as temperature is increased.

Other circuit components do not directly influence the accuracy of the VFC over temperature changes as long as their actual values are not so different from the nominal value as to preclude operation. This includes the integration capacitor, C_{INT}. A change in the capacitance value of C_{INT} simply results in a different rate of voltage change across the capacitor. During the Integration Phase (refer to Figure 2), the rate of voltage change across C_{INT} has the opposite effect that it does during the Reset Phase. The result is that the conversion accuracy is unchanged by either drift or tolerance of C_{INT}. The net effect of a change in the integrator capacitor is simply to change the peak to peak amplitude of the sawtooth waveform at the output of the integrator.

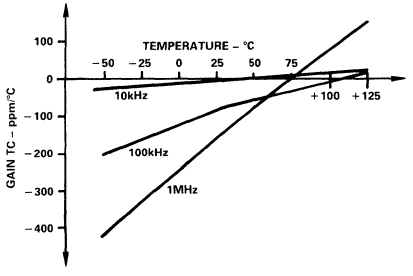


Figure 8. Gain TC vs. Temperature

The gain temperature coefficient of the AD650 is not a constant value. Rather the gain TC is a function of both the full scale frequency and the ambient temperature. At a low full scale frequency, the gain TC is determined primarily by the stability of the internal reference–a buried zener reference. This low speed gain TC can be quite good; at 10kHz full scale, the gain TC near 25°C is typically 0 ± 50ppm/°C. Although the gain TC changes with ambient temperature (tending to be more positive

[1]"Noise Reduction Techniques in Electronic Systems", by H. W. OTT, (John Wiley, 1976).

at higher temperatures), the drift remains within a ±75ppm/°C window over the entire military temperature range. At full scale frequencies higher than 10kHz dynamic errors become much more important than the static drift of the dc reference. At a full scale frequency of 100kHz and above, these timing errors dominate the gain TC. For example, at 100kHz full scale frequency (R_{IN} = 40k and C_{OS} = 330pF) the gain TC near room temperature is typically −80 ±50ppm/°C, but at an ambient temperature near +125°C, the gain TC tends to be more positive and is typically +15 ±50ppm/°C. This information is presented in a graphical form in Figure 8. The gain TC always tends to become more positive at higher temperatures. Therefore it is possible to adjust the gain TC of the AD650 by using a one-shot capacitor with an appropriate TC to cancel the drift of the circuit. For example, consider the 100kHz full scale frequency. An average drift of −100ppm/°C means that as temperature is increased, the circuit will produce a lower frequency in reponse to a given input voltage. This means that the one-shot capacitor must decrease in value as temperature increases in order to compensate the gain TC of the AD650; that is, the capacitor must have a TC of −100ppm/°C. Now consider the 1MHz full scale frequency. It is not possible to achieve very much improvement in performance unless the expected ambient temperature range is known. For example, in a constant low temperature application such as gathering data in an Arctic climate (approximately −20°C), a C_{OS} with a drift of −310ppm/°C is called for in order to compensate the gain drift of the AD650. However, if that circuit should see an ambient temperature of +75°C, the C_{OS} cap would change the gain TC from approximately 0ppm to +310ppm/°C.

The temperature effects of the components described above are the same when the AD650 is configured for negative or bipolar input voltages, and for F/V conversion as well.

NONLINEARITY SPECIFICATION

The linearity error of the AD650 is specified by the end point method. That is, the error is expressed in terms of the deviation from the ideal voltage to frequency transfer relation after calibrating the converter at full scale and "zero". The nonlinearity will vary with the choice of one-shot capacitor and input resistor (see Figure 3). Verification of the linearity specification requires the availability of a switchable voltage source (or a DAC) having a linearity error below 20ppm, and the use of very long measurement intervals to minimize count uncertainties. Every AD650 is automatically tested for linearity, and it will not usually be necessary to perform this verification, which is both tedious and time consuming. If it is required to perform a nonlinearity test either as part of an incoming quality screening or as a final product evaluation, an automated "bench-top" tester would prove useful. Such a system based on the Analog Devices' LTS-2010 is described in Reference 2.

The voltage-to-frequency transfer relation is shown in Figure 9 with the nonlinearity exaggerated for clarity. The first step in determining nonlinearity is to connect the end points of the operating range (typically at 10mV and 10V) with a straight line. This straight line is then the ideal relationship which is desired from the circuit. The second step is to find the difference between this line and the actual response of the circuit at a few points between the end points – typically ten intermediate points will suffice. The difference between the actual and the ideal response is a frequency error measured in hertz. Finally, these frequency errors are normalized to the full scale frequency and expressed either as parts per million of full-scale (ppm) or parts

[2]"V-F Converters Demand Accurate Linearity Testing", by L. DeVito, (Electronic Design, March 4, 1982)

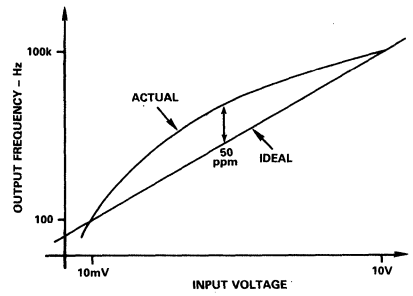


Figure 9a. Exaggerated Nonlinearity at 100kHz Full Scale

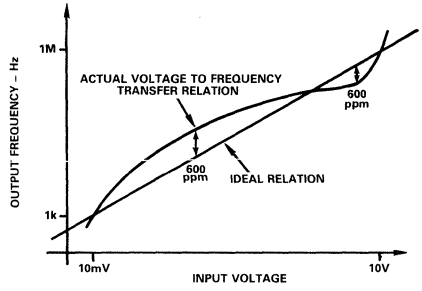


Figure 9b. Exaggerated Nonlinearity at 1MHz Full Scale

per hundred of full scale (%). For example, on a 100kHz full scale, if the maximum frequency error is 5Hz, the nonlinearity would be specified as 50ppm or 0.005%. Typically on the 100kHz scale, the nonlinearity is positive and the maximum value occurs at about midscale (Figure 9a). At higher full scale frequencies, (500kHz to 1MHz), the nonlinearity becomes "S" shaped and the maximum value may be either positive or negative. Typically, on the 1MHz scale (R_{IN} = 16.9k, C_{OS} = 51pF) the nonlinearity is positive below about 2/3 scale and is negative above this point. This is shown graphically in Figure 9b.

PSRR

The power supply rejection ratio is a specification of the change in gain of the AD650 as the power supply voltage is changed. The PSRR is expressed in units of parts-per-million change of the gain per percent change of the power supply – ppm/%. For example, consider a VFC with a 10 volt input applied and an output frequency of exactly 100kHz when the power supply potential is ±15 volts. Changing the power supply to ±12.5 volts is a 5 volt change out of 30 volts, or 16.7%. If the output

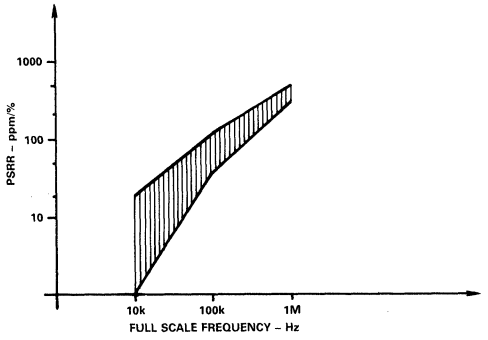


Figure 10. PSRR vs. Full Scale Frequency

frequency changes to 99.9kHz, the gain has changed 0.1% or 1000ppm. The PSRR is 1000ppm divided by 16.7% which equals 60ppm/%.

The PSRR of the AD650 is a function of the full scale operating frequency. At low full scale frequencies the PSRR is determined by the stability of the reference circuits in the device and can be very good. At higher frequencies there are dynamic errors which become more important than the static reference signals, and consequently the PSRR is not quite as good. The values of PSRR are typically 0 ±20ppm/% at 10kHz full scale frequency (R_{IN} = 40k, C_{OS} = 3300pF). At 100kHz (R_{IN} = 40k, C_{OS} = 330pF) the PSRR is typically +80 ±40ppm/%, and at 1MHz (R_{IN} = 16.9kΩ, C_{OS} = 51pF) the PSRR is +350 ±50ppm/%. This information is summarized graphically in Figure 10.

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to pins 1, 2 and 3 is not a standard operational amplifier. Rather, the design has been optimized for simplicity and high speed. The single largest difference between this amplifier and a normal op amp is the lack of an integrator (or level shift) stage. Consequently the voltage on the output (pin 1) must always be more positive than 2 volts below the inputs (pins 2 and 3). For example, in the F to V conversion mode, see Figure 6, the noninverting input of the op amp (pin 2) is grounded, which means that the output (pin 1) will not be able to go below −2 volts. Normal operation of the circuit as shown in the figure will never call for a negative voltage at the output but one may imagine an arrangement calling for a bipolar output voltage (say ±10 volts) by connecting an extra resistor from pin 3 to a positive voltage. This will not work.

Care should be taken under conditions where a high positive input voltage exists at or before power up. These situations can cause a latch up at the integrator output (pin 1). This is a non-destructive latch and, as such, normal operation can be restored by cycling the power supply. Latch up can be prevented by connecting two diodes (e.g., 1N914 or 1N4148) as shown in Figure 4 thereby preventing pin 1 from swinging below pin 2.

A second major difference is that the output will only sink 1mA to the negative supply. There is no pulldown stage at the output other than the 1mA current source used for the V to F conversion. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 3 volts of the positive supply when it is not sourcing external current. When sourcing 10mA the output voltage may be driven to within 6 volts of the positive supply.

A third difference between this op amp and a normal device is that the inverting input, pin 3, is bias current compensated and the noninverting input is not bias current compensated. The bias current at the inverting input is nominally zero, but may be as much as 20nA in either direction. The noninverting input typically has a bias current of 40nA that always flows into the node (an npn input transistor). Therefore, it is not possible to match input voltage drops due to bias currents by matching input resistors.

The op amp has provisions for trimming the input offset voltage. A potentiometer of 20kΩ is connected to pins 13 and 14 and the wiper is connected to the positive supply through a 250kΩ resistor. A potential of about 0.6 volt is established across the 250kΩ resistor, and the 3μA current is injected into the null pins. It is also possible to null the op amp offset voltage by using only one of the null pins and use a bipolar current either into or out of the null pin. The amount of current required will be very small – typically less than 3μA. This technique is shown in the applications section of this data sheet: the auto-zero circuit uses this technique.

The bipolar offset current is activated by connecting a 1.24kΩ resistor between pin 4 and the negative supply. The resultant current delivered to the op amp noninverting input is nominally 0.5mA and has a tolerance of ±10%. This current is then used to provide an offset voltage when pin 2 is tied to ground through a resistor. The 0.5mA which appears at pin 2 is also flowing through the 1.24kΩ resistor and this current may be measured by observing the voltage across the 1.24kΩ resistor. An external resistor is used to activate the bipolar offset current source to provide the lowest tolerance and temperature drift of the resultant offset voltage. It is possible to use other values of resistance between pin 4 and $-V_S$ to obtain a bipolar offset current different than 0.5mA. Figure 11 is a graph of the relationship between the bipolar offset current and the value of the resistor used to activate the source.

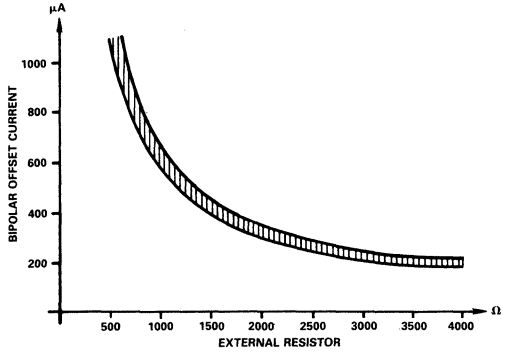


Figure 11. Bipolar Offset Current vs. External Resistor

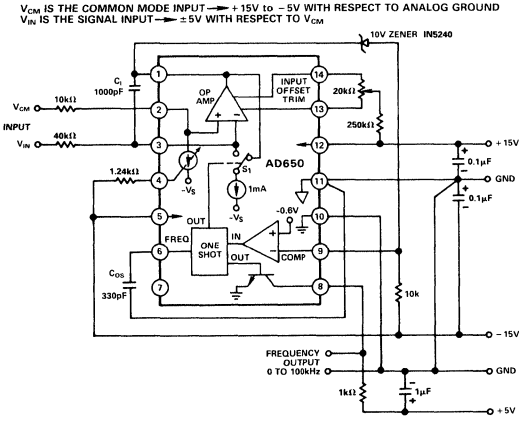


Figure 12. AD650 Differential Input

APPLICATIONS

DIFFERENTIAL VOLTAGE-TO-FREQUENCY CONVERSION

The circuit of Figure 12 accepts a true floating differential input signal. The common mode input, V_{CM}, may be in the range +15 to −5 volts with respect to analog ground. The signal input, V_{IN}, may be ±5 volts with respect to the common mode input. Both inputs are low impedance: the source which drives the common mode input must supply the 0.5mA drawn by the bipolar offset current source and the source which drives the signal input must supply the integration current.

If less common mode voltage range is required, a lower voltage zener may be used. For example, if a 5 volt zener is used, the V_{CM} input may be in the range +10 to −5 volt. If the zener is not used at all, the common mode range will be ±5 volts with repect to analog ground. If no zener is used, the 10k pulldown resistor is not needed and the integrator output (pin 1) is connected directly to the comparator input (pin 9).

AUTO ZERO CIRCUIT

In order to exploit the full dynamic range of the AD650 VFC, very small input voltages will need to be converted. For example, a six decade dynamic range based on a full scale of 10 volts will require accurate measurement of signals down to 10μV. In these situations a well-controlled input offset voltage is imperative. A constant offset voltage will not affect dynamic range but simply shift all of the frequency readings by a few hertz. However, if the offset should change, then it will not be possible to distinguish between a small change in a small input voltage and a drift of the offset voltage. Hence, the useable dynamic range is less. The circuit shown in Figure 13 provides automatic adjustment of the op amp offset voltage. The circuit uses an AD582 sample and hold amplifier to control the offset and the input voltage to the VFC is switched between ground and the signal to be measured via an AD7512DI analog switch. The offset of the AD650 is adjusted by injecting a current into or drawing a current out of pin 13. Note that only one of the offset null pins is used. During the "VFC Norm" mode, the SHA is in the hold mode and the hold capacitor is very large, 0.1μF, to hold the AD650 offset constant for a long period of time.

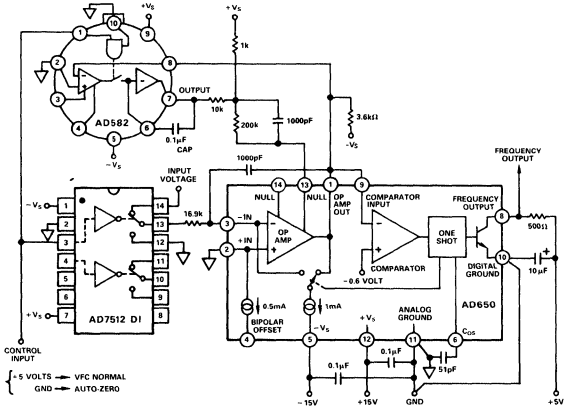


Figure 13. Auto-Zero Circuit for AD650 Voltage-to-Frequency Converter

When the circuit is in the "Auto Zero" mode the SHA is in sample mode and behaves like an op amp. The circuit is a variation of the classical two amplifier servo loop, where the output of the Device Under Test (DUT) – here the DUT is the AD650 op amp – is forced to ground by the feedback action of the control amplifier – the SHA. Since the input of the VFC circuit is connected to ground during the auto zero mode, the input current which can flow is determined by the offset voltage of the AD650 op amp. Since the output of the integrator stage is forced to ground it is known that the voltage is not changing (it is equal to ground potential). Hence if the output of the integrator is constant, its input current must be zero, so the offset voltage has been forced to be zero. Note that the output of the DUT could have been forced to any convenient voltage other than ground. All that is required is that the output voltage be known to be constant. Note also that the effect of the bias current at the inverting input of the AD650 op amp is also nulled in this circuit. The 1000pF capacitor shunting the 200kΩ resistor is compensation for the two amplifier servo loop. Two integrators in a loop requires a single zero for compensation. Note that the 3.6kΩ resistor from pin 1 of the AD650 to the negative supply is *not* part of the auto-zero circuit, but rather it is required for VFC operation at 1MHz.

PHASE LOCKED LOOP F/V CONVERSION

Although the F/V conversion technique shown in Figure 6 is quite accurate and uses only a few extra components, it is very limited in terms of signal frequency response and carrier feedthrough. If the carrier (or input) frequency changes instantaneously, the output cannot change very rapidly due to the integrator time constant formed by C_{INT} and R_{IN}. While it is possible to decrease the integrator time constant to provide faster settling of the F to V output voltage, the carrier feedthrough will then be larger. For signal frequency response in excess of 2kHz, a phase locked F/V conversion technique such as the one shown in Figure 14 is recommended.

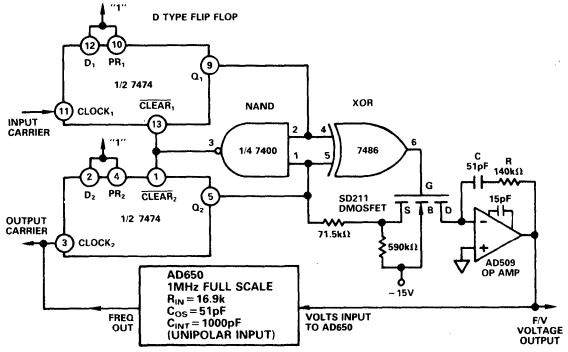


Figure 14. Phase Locked Loop F/V Conversion

In a phase locked loop circuit, the oscillator is driven to a frequency and phase equal to an input reference signal. In applications such as a synthesizer, the oscillator output frequency is first processed through a programmable "divide by N" before being applied to the phase detector as feedback. Here the oscillator frequency is forced to be equal to "N times" the reference frequency and it is this frequency output which is the desired output signal and not a voltage. In this case, the AD650 offers compact size and wide dynamic range.

In signal recovery applications of a PLL, the desired output signal is the voltage applied to the oscillator. In these situations a linear relationship between the input frequency and the output voltage is desired; the AD650 makes a superb oscillator for FM demodulation. The wide dynamic range and outstanding linearity of the AD650 VFC allow simple embodiment of high performance analog signal isolation or telemetry systems. The circuit shown in Figure 14 uses a digital phase detector which also provides proper feedback in the event of unequal frequencies. Such phase-frequency detectors (PFD's) are available in integrated form.

For a full discussion of phase lock loop circuits see Reference 3.

An analysis of this circuit must begin at the 7474 dual D flip flop. When the input carrier matches the output carrier in both phase and frequency, the Q outputs of the flip flops will rise at exactly the same time. With two zero's, then two one's on the inputs of the exclusive or (XOR) gate, the output will remain low keeping the DMOS FET switched off. Also, the NAND gate will go low resetting the flip-flops to zero. Throughout the entire cycle just described, the DMOS integrator gate remained off, allowing the voltage at the integrator output to remain unchanged from the previous cycle. However, if the input carrier leads the output carrier by a few degrees, the XOR gate will be turned on for the small time span that the two signals are mismatched. Since Q_2 will be low during the mismatch time, a negative current will be fed into the integrator, causing its output voltage to rise. This in turn will increase the frequency of the AD650 slightly, driving the system towards synchronization. In a similar manner, if the input carrier lags the output carrier, the integrator will be forced down slightly to synchronize the two signals.

Using a mathematical approach, the ±25μA pulses from the phase detector are incorporated into the phase detector gain, K_d.

$$K_d = \frac{25\mu A}{2\pi} = 4 \times 10^{-6} \quad \textit{amperes/radian} \tag{9}$$

Also, the V/F converter is configured to produce 1MHz in response to a 10 volt input, so its gain K_o is:

$$K_o = \frac{2\pi \times 1 \times 10^6 Hz}{10V} = 6.3 \times 10^5 \quad \frac{\textit{radians}}{\textit{volt} \cdot \textit{sec}} \tag{10}$$

The dynamics of the phase relationship between the input and output signals can be characterized as a second order system with natural frequency ω_n:

$$\omega_n = \sqrt{\frac{K_o K_d}{C}} \tag{11}$$

and damping factor

$$\zeta = \frac{R\sqrt{C\,K_o K_d}}{2} \tag{12}$$

For the values shown in Figure 14, these relations simplify to a natural frequency of 35kHz with a damping factor of 0.8.

For those desiring a simple approach to determining component values for other PLL frequencies and VFC full scale voltage, the following cookbook steps can be used:

1. Determine K_o (in units of radians per volt second) from the maximum input carrier frequency F_{max} (in hertz) and the maximum output voltage V_{max}.

$$K_o = \frac{2\pi \times F_{max}}{V_{max}} \tag{13}$$

2. Calculate a value for C based upon the desired loop bandwidth, f_n. Note that this is the desired frequency range of the output signal. The loop bandwidth (f_n) is *not* the maximum carrier frequency (f_{max}): the signal may be very narrow even though it is transmitted over a 1MHz carrier.

$$C = \frac{K_o}{f_n^2} \cdot 1 \times 10^{-7} \frac{V \cdot F}{Rad \cdot sec} \quad \begin{matrix} \text{C units FARADS} \\ f_n \text{ units HERTZ} \\ K_o \text{ units RAD/VOLT•SEC} \end{matrix} \tag{14}$$

3. Calculate R to yield a damping factor of approximately 0.8 using this equation:

$$R = \frac{f_n}{K_o} \cdot 2.5 \times 10^6 \frac{Rad \cdot \Omega}{V} \quad \begin{matrix} \text{R units OHMS} \\ f_n \text{ units HERTZ} \\ K_o \text{ units RAD/VOLT•SEC} \end{matrix} \tag{15}$$

If in actual operation the PLL overshoots or hunts excessively before reaching a final value, the damping factor may be raised by increasing the value of R. Conversely, if the PLL is overdamped, a smaller value of R should be used.

PLL PERFORMANCE

The performance of the PLL circuit is demonstrated by the system shown in Figure 15; an analog signal is converted into a frequency, and then this frequency is converted back into an analog voltage by the PLL.

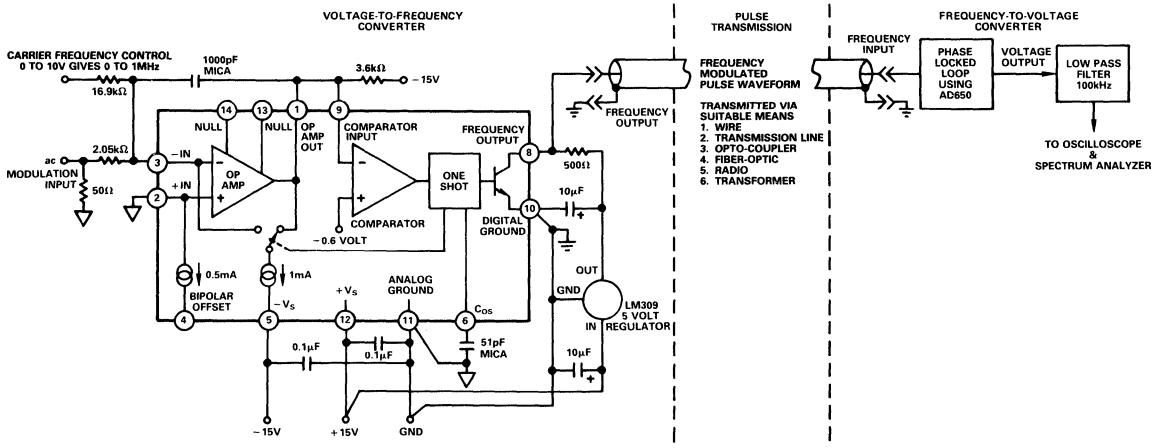


Figure 15.

[3]"Phase lock Techniques", by F.M. Gardner, 2nd Edition, 1979, John Wiley and Sons.

The source of the frequency input signal used to drive the PLL is an AD650 with two separate inputs: one for dc to set the carrier frequency, and one for ac to establish a modulation. Note how the summing junction input to the AD650 allows such flexibility. The output frequency is then relayed to the PLL via a jumper cable. The signal at this point is a 5 volt digital pulse train and as such may be transmitted in any fashion suitable to the application at hand. For example, galvanic isolation is achieved with a simple transformer or opto-isolator; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber-optic link; telemetry can be accomplished with a radio link. The actual method of conveying the pulses is not crucial to the system performance. The PLL is the circuit shown in Figure 14, and the filter shown on the output signal is simply to attenuate carrier feedthrough to allow easy interpretation of the signal with an oscilloscope and spectrum analyzer.

The step response of the system is shown in Figure 16a. The signal output is swinging between 5 volts and 10 volts, for an input step of 500kHz to 1MHz. Note that the AD650 is actually overshooting to 1.1MHz and the response remains well controlled. Note the slight irregularity during the transition: this is caused by cycleslipping during the slew where feedback is lost temporarily and the PLL actually loses phase lock. The frequency response of the system when driven with sinewave excitation is shown in Figure 16b. Here the output level is set to 2 volts peak to peak, and the carrier is 800kHz. Note that the -3dB bandwidth is about 70kHz, which is consistent with a damping factor of 0.8 and a natural frequency of 35kHz[4]. When an unmodulated carrier is applied to the PLL, the noise that appears at the output determines the dynamic range of the system. The spectrum of the noise at the output of the PLL is shown in Figure 16c. By comparing this with Figure 16b, the dynamic range of the system is seen to be 80dB. The harmonic distortion of the system is shown in Figure 16d. The output is a 2V p-p sinewave at 5kHz, and the amplitude of the first harmonic is seen to be 48dB below the fundamental. The harmonic distortion can be improved to the level of 60dB by reducing the amplitude of the modulation, but this is at the expense of dynamic range since the intensity of the noise floor remains constant.

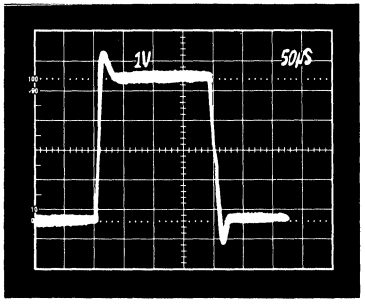


Figure 16a. Step Response

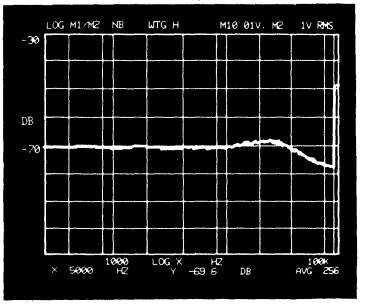


Figure 16c. Noise Output from PLL

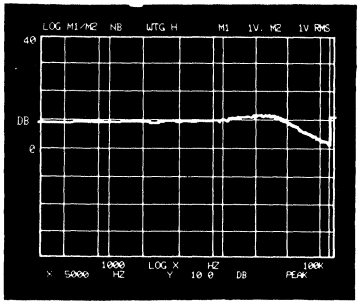


Figure 16b. Frequency Response

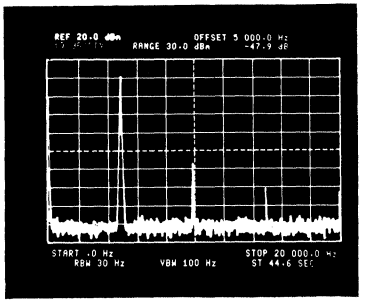


Figure 16d. Harmonic Distortion of PLL System

[4]See page 13 of reference 3.

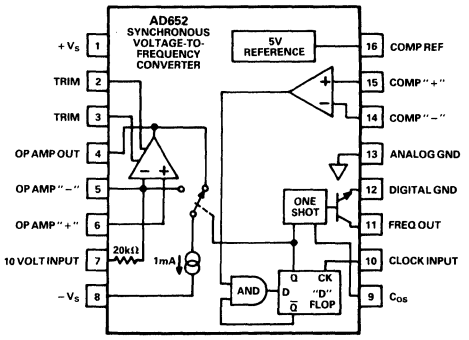
Monolithic Synchronous Voltage-to-Frequency Converter

AD652

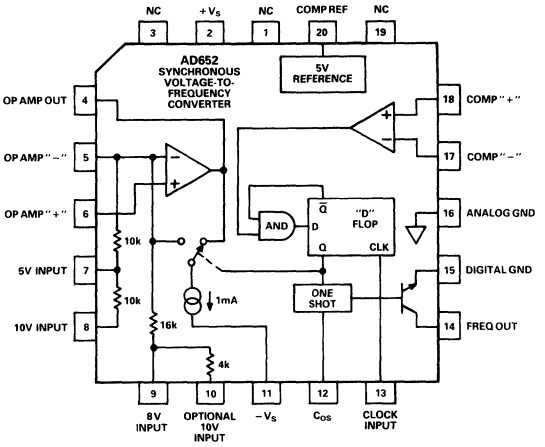
FEATURES

- **Full-Scale Frequency (Up to 2MHz) Set by External System Clock**
- **Extremely Low Linearity Error (0.005% max at 1MHz FS, 0.02% max at 2MHz FS)**
- **No Critical External Components Required**
- **Accurate 5V Reference Voltage**
- **Low Drift (25ppm/°C max)**
- **Dual or Single Supply Operation**
- **Voltage or Current Input**

AD652 PIN CONFIGURATIONS



Cerdip



PLCC

PRODUCT DESCRIPTION

The AD652 Synchronous Voltage-to-Frequency Converter (SVFC) is a powerful building block for precision analog-to-digital conversion, offering typical nonlinearity of 0.002% (0.005% maximum) at a 100kHz output frequency. The inherent monotonicity of the transfer function and wide range of clock frequencies allows the conversion time and resolution to be optimized for specific applications.

The AD652 uses a variation of the popular charge-balancing technique to perform the conversion function. The AD652 uses an external clock to define the full-scale output frequency, rather than relying on the stability of an external capacitor. The result is a more stable, more linear transfer function, with significant application benefits in both single- and multi-channel systems.

Gain drift is minimized using a precision low-drift reference and low-TC on-chip thin-film scaling resistors. Furthermore, the initial gain error is reduced to less than 0.5% by the use of laser-wafer-trimming.

The analog and digital sections of the AD652 have been designed to allow operation from a single-ended power source, simplifying its use with isolated power supplies.

The AD652 is available in five performance grades. The 20-pin PLCC packaged JP and KP grades are specified for operation over the 0 to +70°C commercial temperature range. The 16-pin cerdip-packaged AQ and BQ grades are specified for operation over the −40°C to +85°C industrial temperature range, and the AD652SQ is available for operation over the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. The use of an external clock to set the full-scale frequency allows the AD652 to achieve linearity and stability far superior to other monolithic VFCs. By using the same clock to drive the AD652 and (through a suitable divider) also set the counting period, conversion accuracy is maintained independent of variations in clock frequency.
2. The AD652 Synchronous VFC requires only a single external component (a noncritical integrator capacitor) for operation.
3. The AD652 includes a buffered, accurate 5V reference which is available to the user.
4. The clock input of the AD652 is TTL and CMOS compatible and can also be driven by sources referred to the negative power supply. The flexible open-collector output stage provides sufficient current sinking capability for TTL and CMOS logic, as well as for optical couplers and pulse transformers. A capacitor-programmable one-shot is provided for selection of optimum output pulse width for power reduction.
5. The AD652 can also be configured for use as a synchronous F/V converter for isolated analog signal transmission.

SPECIFICATIONS (typical @ T_A = +25°C, V_S = ±15V, unless otherwise noted)

Parameter	AD652JP/AQ/SQ Min	AD652JP/AQ/SQ Typ	AD652JP/AQ/SQ Max	AD652KP/BQ Min	AD652KP/BQ Typ	AD652KP/BQ Max	Units
VOLTAGE-TO-FREQUENCY MODE							
Gain Error							
f_{CLOCK} = 200kHz		±0.5	±1		±0.25	±0.5	%
f_{CLOCK} = 1MHz		±0.5	**±1**		±0.25	**±0.5**	%
f_{CLOCK} = 4MHz		±0.5	**±1.5**		±0.25	**±0.75**	%
Gain Temperature Coefficient							
f_{CLOCK} = 200kHz		±25	±50		±15	±25	ppm/°C
f_{CLOCK} = 1MHz		±25	**±50**		±15	**±25**	ppm/°C
		±10	**±25**		±10	**±15**	ppm/°C[1]
f_{CLOCK} = 4MHz		±25	**±75**		±15	**±50**	ppm/°C
Power Supply Rejection Ratio		0.001	**0.01**		0.001	**0.01**	%/V
Linearity Error							
f_{CLOCK} = 200kHz		±0.002	±0.02		±0.002	±0.005	%
f_{CLOCK} = 1MHz		±0.002	**±0.02**		±0.002	**±0.005**	%
f_{CLOCK} = 2MHz		±0.01	±0.02		±0.002	±0.005	%
f_{CLOCK} = 4MHz		±0.02	**±0.05**		±0.01	**±0.02**	%
Offset (Transfer Function, RTI)		±1	**±3**		±1	**±2**	mV
Offset Temperature Coefficient		±10	**±50**		±10	**±25**	µV/°C
Response Time	One Period of New Output Frequency Plus One Clock Period.						
FREQUENCY-TO-VOLTAGE MODE							
Gain Error							
f_{IN} = 100kHz FS		±0.5	±1		±0.25	±0.5	%
Linearity Error							
f_{IN} = 100kHz FS		±0.002	±0.02		±0.002	±0.01	%
INPUT RESISTORS							
Cerdip (Figure 1a.) (0 to +10V FS Range)	19.8	20	20.2	19.8	20	20.2	kΩ
PLCC (Figure 1b.)							
Pin 8 to Pin 7	9.9	10	10.1	9.9	10	10.1	kΩ
Pin 7 to Pin 5 (0 to +5V FS Range)	9.9	10	10.1	9.9	10	10.1	kΩ
Pin 8 to Pin 5 (0 to +10V FS Range)	19.8	20	20.2	19.8	20	20.2	kΩ
Pin 9 to Pin 5 (0 to +8V FS Range)	15.8	16	16.2	15.8	16	16.2	kΩ
Pin 10 to Pin 5 (Auxiliary Input)	19.8	20	20.2	19.8	20	20.2	kΩ
Temperature Coefficient (All)		±50	**±100**		±50	**±100**	ppm/°C
INTEGRATOR OP AMP							
Input Bias Current							
Inverting Input (Pin 5)		±5	**±20**		±5	**±20**	nA
Noninverting Input (Pin 6)		20	**50**		20	**50**	nA
Input Offset Current		20	**70**		20	**70**	nA
Input Offset Current Drift		1	3		1	2	nA/°C
Input Offset Voltage		±1	**±3**		±1	**±2**	mV
Input Offset Voltage Drift		±10	±25		±10	±15	µV/°C
Open Loop Gain		86			86		dB
Common-Mode Input Range	$-V_S+5$		$+V_S-5$	$-V_S+5$		$+V_S-5$	V
CMRR	80			80			dB
Bandwidth	14	95		14	95		MHz
Output Voltage Range	**−1**		**(+V_S−4)**	**−1**		**(+V_S−4)**	V
(Referred to Pin 6, R_L >= 5k)							
COMPARATOR							
Input Bias Current		0.5	5		0.5	5	µA
Common-Mode Voltage	$-V_S+4$		$+V_S-4$	$-V_S+4$		$+V_S-4$	V
CLOCK INPUT							
Maximum Frequency	**4**	5		**4**	5		MHz
Threshold Voltage (Referred to Pin 12)		1.2			1.2		V
T_{min}-T_{max}	**0.8**		**2.0**	**0.8**		**2.0**	V
Input Current							
($-V_S<V_{CLK}<+V_S$)		5	**20**		5	**20**	µA
Voltage Range	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Rise Time			2			2	µs

Parameter	AD652JP/AQ/SQ Min	Typ	Max	AD652KP/BQ Min	Typ	Max	Units
OUTPUT STAGE							
V_{OL} (I_{OUT} = 10mA)			**0.4**			**0.4**	V
I_{OL}							
V_{OL}<0.8V			**15**			**15**	mA
V_{OL}<0.4V, T_{min}-T_{max}			**8**			**8**	mA
I_{OH} (Off Leakage)		0.01	**10**		0.01	**10**	µA
Delay Time, Positive Clock Edge to Output Pulse	**150**	200	**250**	**150**	200	**250**	ns
Fall Time (Load = 500pF and I_{SINK} = 5mA)		100			100		ns
Output Capacitance		5			5		pF
OUTPUT ONE-SHOT							
Pulse Width							
C_{OS} = 300pF	**1**	1.5	**2**	**1**	1.5	**2**	µs
C_{OS} = 1000pF	4	5	6	4	5	6	µs
REFERENCE OUTPUT							
Voltage	**4.950**	5.0	**5.050**	**4.975**	5.0	**5.025**	V
Drift			**100**			**50**	ppm/°C
Output Current							
Source T_{min} to T_{max}	**10**			**10**			mA
Sink	**100**	500		**100**	500		µA
Power Supply Rejection							
(Supply Range = ± 12.5V to ± 17.5V)			0.015			0.015	%/V
Output Impedance (Sourcing Current)		0.3	**2**		0.3	**2**	Ω
POWER SUPPLY							
Rated Voltage		± 15			± 15		V
Operating Range							
Dual Supplies	± 6	± 15	± 18	± 6	± 15	± 18	V
Single Supply ($-V_S$ = 0)	+ 12		+ 36	+ 12		+ 36	V
Quiescent Current		± 11	**± 15**		± 11	**± 15**	mA
Digital Common	$-V_S$		$+V_S-4$	$-V_S$		$+V_S-4$	V
Analog Common	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
TEMPERATURE RANGE							
Specified Performance							
JP, KP Grade	0		+ 70	0		+ 70	°C
AQ, BQ Grade	− 40		+ 85	− 40		+ 85	°C
SQ Grade	− 55		+ 125				°C

NOTES
[1]Referred to internal V_{REF}. In PLCC package, tested on 10V input range only.
Specifications in **boldface** are 100% tested at final test and are used to measure outgoing quality levels.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage (Figure 6) 36V
Maximum Output Current (Open Collector Output) . . 50mA
Amplifier Short Circuit to Ground . . . . . Indefinite
Storage Temperature Range: Cerdip . . . . −65°C to + 150°C
PLCC . . . . −65°C to + 150°C

ORDERING GUIDE

Part Number	Gain Drift ppm/°C 100kHz	1MHz Linearity %	Specified Temperature Range °C	Package Options*
AD652JP	50 max	0.02 max	0 to + 70	PLCC (P-20A)
AD652KP	25 max	0.005 max	0 to + 70	PLCC (P-20A)
AD652AQ	50 max	0.02 max	− 40 to + 85	Cerdip (Q-16)
AD652BQ	25 max	0.005 max	− 40 to + 85	Cerdip (Q-16)
AD652SQ	50 max	0.02 max	− 55 to + 125	Cerdip (Q-16)

*See Section 14 for package outline information.

DEFINITIONS OF SPECIFICATIONS

GAIN ERROR – The gain of a voltage-to-frequency converter is that scale factor setting that provides the nominal conversion relationship, e.g. 1MHz full scale. The "gain error" is the difference in slope between the actual and ideal transfer functions for the V-F converter.

LINEARITY ERROR – The "linearity error" of a V-F is the deviation of the actual transfer function from a straight line passing through the endpoints of the transfer function.

GAIN TEMPERATURE COEFFICIENT – The gain temperature coefficient is the rate of change in full-scale frequency as a function of the temperature from + 25°C to T_{min} or T_{max}.

AD652 PIN CONFIGURATIONS

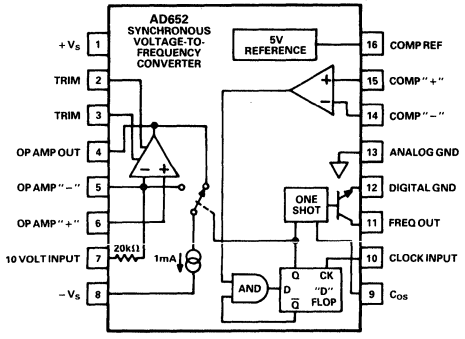
PIN	"Q" CERDIP	"P" PLCC
1	$+V_S$	NC
2	TRIM	$+V_S$
3	TRIM	NC
4	OP AMP OUT	OP AMP OUT
5	OP AMP "−"	OP AMP "−"
6	OP AMP "+"	OP AMP "+"
7	10 VOLT INPUT	5 VOLT INPUT
8	$-V_S$	10 VOLT INPUT
9	C_{OS}	8 VOLT INPUT
10	CLOCK INPUT	OPTIONAL 10V INPUT
11	FREQ OUT	$-V_S$
12	DIGITAL GND	C_{OS}
13	ANALOG GND	CLOCK INPUT
14	COMP "−"	FREQ OUT
15	COMP "+"	DIGITAL GROUND
16	COMP REF	ANALOG GND
17		COMP "−"
18		COMP "+"
19		NC
20		COMP REF

THEORY OF OPERATION

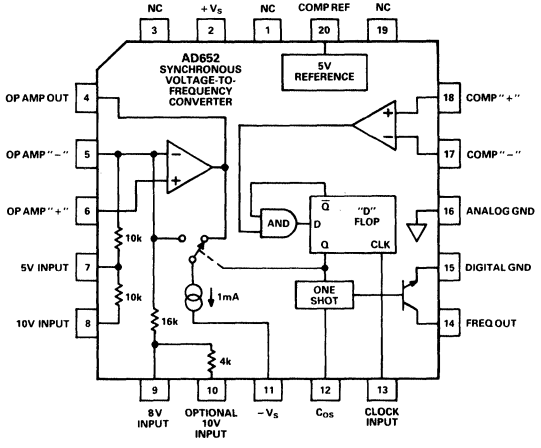
A synchronous VFC is similar to other voltage-to-frequency converters in that an integrator is used to perform a charge-balance of the input signal with an internal reference current. However, rather than using a one-shot as the primary timing element which requires a high quality and low drift capacitor, a synchronous voltage-to-frequency converter (SVFC) uses an external clock; this allows the designer to determine the system stability and drift based upon the external clock selected. A crystal oscillator may also be used if desired.

The SVFC architecture provides other system advantages besides low drift. If the output frequency is measured by counting pulses gated to a signal which is derived from the clock, the clock stability is unimportant and the device simply performs as a voltage controlled frequency divider, producing a high resolution A/D. If a large number of inputs must be monitored simultaneously in a system, the controlled timing relationship between the frequency output pulses and the user supplied clock greatly simplifies this signal acquisition. Also, if the clock signal is provided by a VFC, then the output frequency of the SVFC will be proportional to the product of the two input voltages. Hence, multiplication and A-to-D conversion on two signals are performed simultaneously.

The pinouts of the AD652 SVFC are shown in Figure 1. A block diagram of the device configured as a SVFC, along with various system waveforms, is shown in Figure 2.



a. AD652 Cerdip Pin Configuration



b. AD652 PLCC Pin Configuration

Figure 1.

Figure 2 shows the typical up-and-down ramp integrator output of a charge-balance VFC. After the integrator output has crossed the comparator threshold and the output of the AND gate has gone high, nothing happens until a negative edge of the clock comes along to transfer the information to the output of the D-FLOP. At this point, the clock level is low, so the latch does not change state. When the clock returns high, the latch output goes high and drives the switch to reset the integrator. At the same time the latch drives the AND gate to a low output state. On the very next negative edge of the clock the low output state of the AND gate is transferred to the output of the D-FLOP and then when the clock returns high, the latch output goes low and drives the switch back into the Integrate Mode. At the same time the latch drives the AND gate to a mode where it will truthfully relay the information presented to it by the comparator.

Since the reset pulses applied to the integrator are exactly one clock period long, the only place where drift can occur is in a variation of the symmetry of the switching speed with temperature. Since each reset pulse is identical to every other, the AD652 SVFC produces a very linear voltage to frequency transfer relation. Also, since all of the reset pulses are gated by the clock, there are no problems with dielectric absorption causing the duration of a reset pulse to be influenced by the length of time since the last reset.

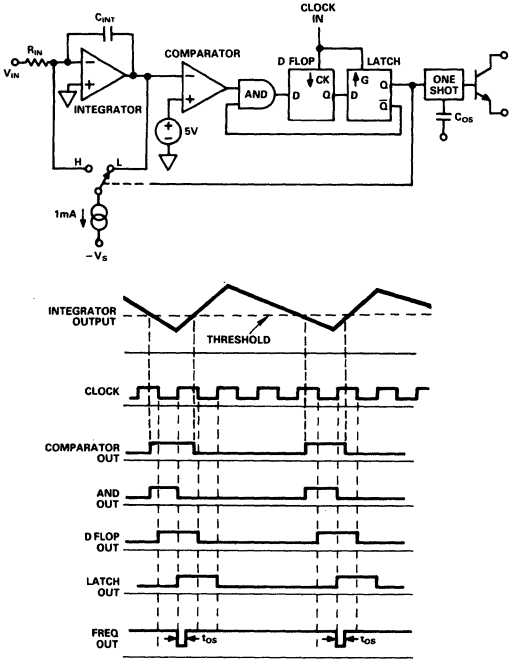


Figure 2. AD652 Block Diagram and System Wafeforms

Referring to Figure 2, it can be seen that the period between output pulses is constrained to be an exact multiple of the clock period. Consider an input current of exactly one quarter of the value of the reference current. In order to achieve a charge balance, the output frequency will equal the clock frequency divided by four; one clock period for reset and three clock periods of integrate. This is shown in Figure 3. If the input current is increased by a very small amount, the output frequency should also increase by a very small amount. Initially, however, no output change is observed for a very small increase in the input current. The output frequency continues to run at one quarter of the clock, delivering an average of 250μA to the summing junction. Since the input current is slightly larger than this, charge accumulates in the integrator and the sawtooth signal starts to drift downward. As the integrator sawtooth drifts down, the comparator threshold is crossed earlier and earlier in each successive cycle, until finally, a whole cycle is lost. When the cycle is lost, the Integrate Phase lasts for two periods of the clock instead of the usual three periods. Thus, among a long string of divide-by-four's an occasional divide-by-three occurs; the average of the output frequency is very close to one quarter of the clock, but the instantaneous frequency can be very different.

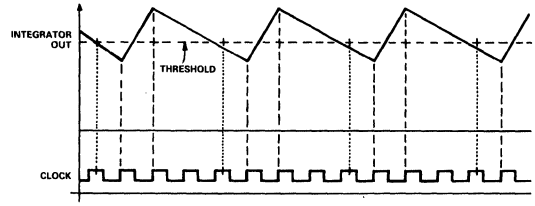


Figure 3. Integrator Output for $I_{IN} = 250\mu A$

Because of this, it is very difficult to observe the waveform on an oscilloscope. During all of this time, the signal at the output of the integrator is a sawtooth wave with an envelope which is also a sawtooth. This is shown in Figure 4.

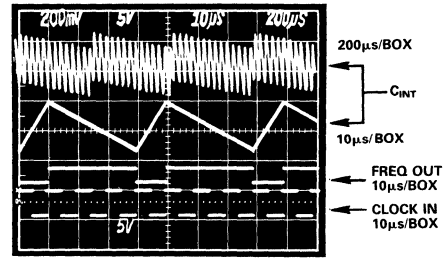


Figure 4. Integrator Output for I_{IN} Slightly Greater than 250μA

Another way to view this is that the output is a frequency of approximately one quarter of the clock that has been phase modulated. A constant frequency can be thought of as accumulating phase linearly with time at a rate equal to $2\pi f$ radians per second. Hence, the average output frequency which is slightly in excess of a quarter of the clock will require phase accumulation at a certain rate. However, since the SVFC is running at exactly one quarter of the clock, it will not accumulate enough phase (see Figure 5). When the difference between the required phase (average frequency) and the actual phase equals 2π, a step in phase is taken where the deficit is made up instantaneously. The output frequency is then a steady carrier which has been phase modulated by a sawtooth signal (see Figure 5). The period of the sawtooth phase modulation is the time required to accumulate a 2π difference in phase between the required average frequency and one quarter of the clock frequency. The amplitude of the sawtooth phase modulation is 2π.

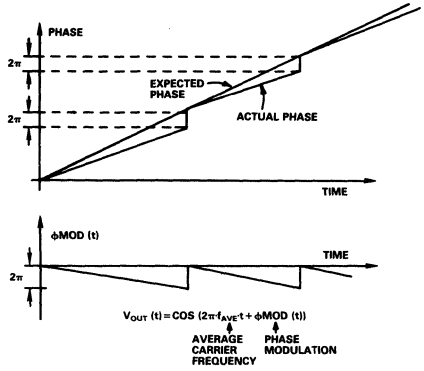


Figure 5. Phase Modulation

The result of this synchronism is that the rate at which data may be extracted from the series bit stream produced by the SVFC is limited. The output pulses are typically counted during a fixed gate interval and the result is interpreted as an average frequency. The resolution of such a measurement is determined by the clock frequency and the gate time. For example, if the clock frequency is 4MHz and the gate time is 4.096ms, then a maximum count of 8,192 is produced by a full-scale frequency of 2MHz. Thus, the resolution is 13 bits.

OVERRANGE

Since each reset pulse is only one clock period in length, the full-scale output frequency is equal to one-half the clock frequency. At full scale the current steering switch spends half of the time on the summing junction; thus, an input current of 0.5mA can be balanced. In the case of an overrange, the output of the integrator op amp will drift in the negative direction and the output of the comparator will remain high. The logic circuits will then simply settle into a "divide-by-two" of the clock state.

SVFC CONNECTION FOR DUAL SUPPLY, POSITIVE INPUT VOLTAGES

Figure 6 shows the AD652 connection scheme for the traditional dual supply, positive input mode of operation. The $\pm V_S$ range is from ± 6 to ± 18 volts. When $+V_S$ is lower than 9.0 volts, it is necessary to short pin 13 to pin 8 (Analog Ground to $-V_S$). Shorting these pins together will ensure proper operation of the 5V reference.

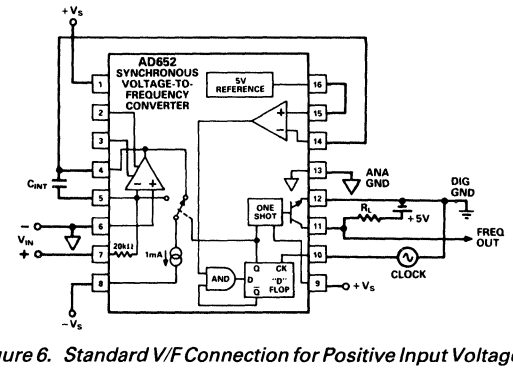


Figure 6. Standard V/F Connection for Positive Input Voltage with Dual Supply

The cerdip packaged AD652 accepts either a 0 to 10V or 0 to 0.5mA full-scale input signal. The temperature drift of the AD652 is specified for a 0 to 10V input range using the internal 20kΩ resistor. If a current input is used, the gain drift will be degraded by a maximum of 100ppm/°C (the TC of the 20kΩ resistor). If an external resistor is connected to pin 5 to establish a different input voltage range, drift will be induced to the extent that the external resistor's TC differs from the TC of the internal resistor. The external resistor used to establish a different input voltage range should be selected as to provide a full-scale current of 0.5mA (i.e., 10kΩ for 0 to 5V).

SVFC CONNECTIONS FOR NEGATIVE INPUT VOLTAGES

Voltages which are negative with respect to ground may be used as the input to the AD652 SVFC. In this case, pin 7 is grounded and the input voltage is applied to pin 6 (see Figure 7). In this mode the input voltage can go as low as 4 volts above $-V_S$. In this configuration the input is a high impedance, and only the 20nA (typical) input bias current of the op amp need be supplied by the input signal. This is contrasted with the more usual positive input voltage configuration, which has a 20kΩ input impedance and requires 0.5mA from the signal source.

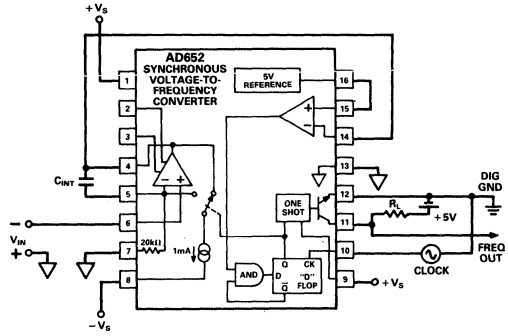


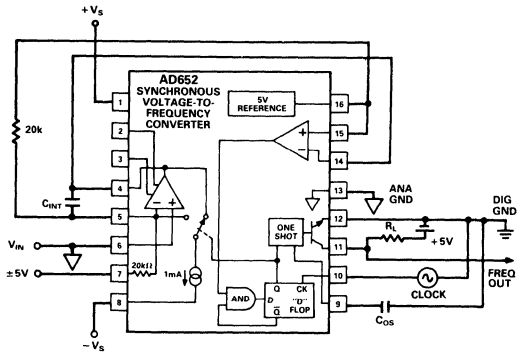
Figure 7. Negative Voltage Input

SVFC CONNECTION FOR BIPOLAR INPUT VOLTAGES

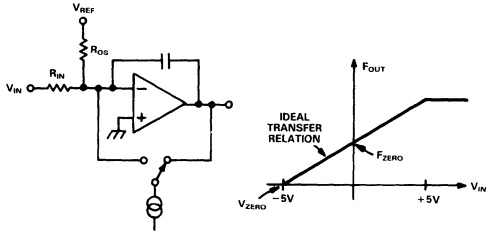
A bipolar input voltage of ± 5V can be accommodated by injecting a 250μA current into pin 5. This is shown in Figure 8a. A -5V signal will then provide a zero sum current at the integrator summing junction which will result in a zero output frequency, while a $+5$V signal will provide a 0.5mA (full- scale) sum current which will result in the full-scale output frequency.

The use of an external resistor to inject the offset current will have some effect on the bipolar offset temperature coefficient. The ideal transfer curve with bipolar inputs is shown in Figure 8b. The user actually has four options to use in injecting the bipolar offset current into the inverting input of the op amp: 1) use an external resistor for R_{OS} and the internal 20k resistor for R_{IN} (as shown in Figure 8a); 2) use the internal 20k resistor as R_{OS} and an external R_{IN}; 3) use two external resistors; 4) use two internal resistors for R_{IN} and R_{OS} (available on PLCC version only).

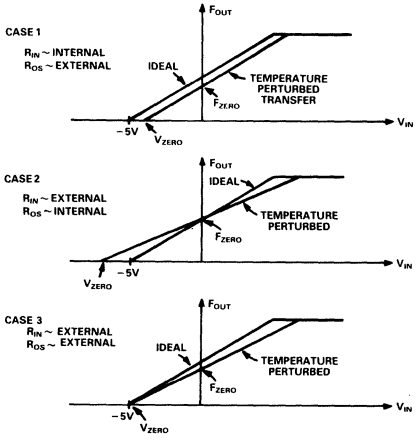
Option #4 provides the closest to the ideal transfer function as diagrammed in Figure 8b. Figure 8c shows the effects on the transfer relation of the other three options. In the first case, the slope of the transfer function is unchanged with temperature. However, V_{ZERO} (the input voltage required to produce an output frequency of 0Hz) and F_{ZERO} (the output frequency when $V_{IN} = 0$V) changes as the transfer function is displaced parallel to the voltage axis with temperature. In the second case, F_{ZERO} remains constant, but V_{ZERO} changes as the transfer function rotates about F_{ZERO} with temperature changes. In the third case, with two external resistors, the V_{ZERO} point remains invariant while the slope and offset of the transfer function change with temperature. If selecting this third option, the user should select low drift, matched resistors.



a. Bipolar Offset



b. Ideal Bipolar Input Transfer Curve Over Temperature



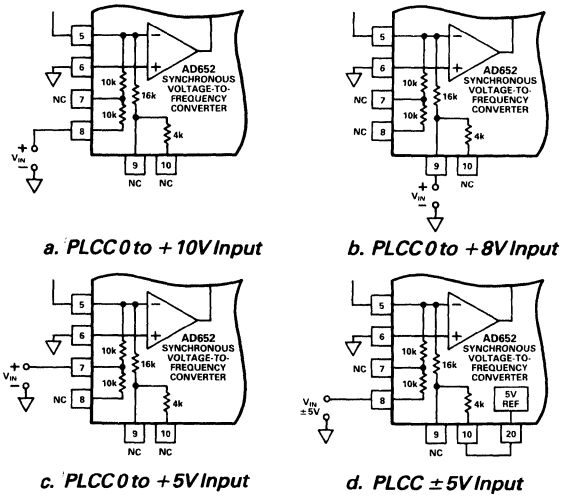
c. Actual Bipolar Input Transfer Over Temperature

Figure 8.

PLCC CONNECTIONS

The PLCC packaged AD652 offers additional input resistors not found on the cerdip-packaged device. These resistors provide the user with additional input voltage ranges. Besides the 10V range available using the on-chip resistor in the cerdip part, the PLCC device also offers 8V and 5V ranges. Figures 9a-9c show the proper connections for these ranges with positive input voltages. For negative input voltages, the appropriate resistor should be tied to analog ground and the input voltage should be applied to pin 6, the "+" input of the op amp.

Bipolar input voltages can be accommodated by injecting a 250μA into pin 5 with the use of the 5V reference and the input resistors. For ±5V or ±2.5V range the reference output, pin 20, should be tied to pin 10. The input signal should then be applied to pin 8 for a ±5V signal and pin 7 for a ±2.5V signal. The input connections for a ±5V range are shown in Figure 9d. For a ±4V range, the input signal should be applied to pin 9, and pin 20 should be connected to pin 8.



a. PLCC 0 to +10V Input

b. PLCC 0 to +8V Input

c. PLCC 0 to +5V Input

d. PLCC ±5V Input

Figure 9.

GAIN AND OFFSET CALIBRATION

The gain error of the AD652 is laser trimmed to within ±0.5%. If higher accuracy is required, the internal 20kΩ resistor must be shunted with a 2MΩ resistor to produce a parallel equivalent which is 1% lower in value than the nominal 20kΩ. Full scale adjustment is then accomplished using a 500Ω series trimmer. See Figures 10a and 10b. When negative input voltages are used, this 500Ω trimmer will be tied to ground and pin 6 will be the input pin.

This gain trim should be done with an input voltage of 9V, and the output frequency should be adjusted to exactly 45% of the clock frequency. Since the device settles into a divide-by-two mode for an input overrange condition, adjusting the gain with a 10V input is impractical; the output frequency would be exactly one-half the clock frequency if the gain were too high and would not change with adjustment until the exact proper scale factor was achieved. Hence, the gain adjustment should be done with a 9V input.

The offset of the op amp may be trimmed to zero with the trim scheme shown in Figures 10a for the cerdip packaged device

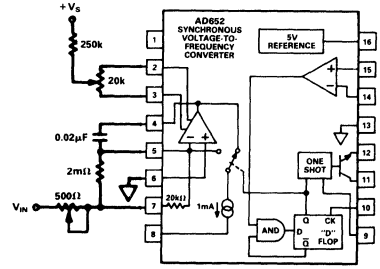


Figure 10a. Cerdip Gain and Offset Trim

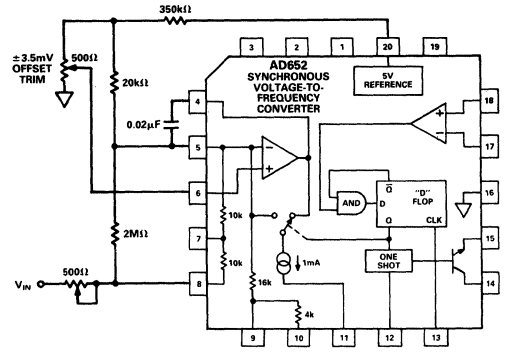


Figure 10b. PLCC Gain and Offset Trim

and Figure 10b for the PLCC packaged device. One way of trimming the offset is by grounding pin 7 (8) of the cerdip (PLCC) packaged device and observing the waveform at pin 4. If the offset voltage of the op amp is positive, then the integrator will have saturated and the voltage will be at the positive rail. If the offset voltage is negative, then there will be a small effective input current that will cause the AD652 to oscillate and a sawtooth waveform will be observed at pin 4. The trimpot should be adjusted until the downward slope of this sawtooth becomes very slow, down to a frequency of 1Hz or less. In an analog-to-digital conversion application, an easier way to trim the offset is to apply a small input voltage, such as 0.01% of the full-scale voltage, and adjust the trimpot until the correct digital output is reached.

GAIN PERFORMANCE

The AD652 gain error is specified as the difference in slope between the actual and the ideal transfer function over the full-scale frequency range. Figure 11 shows a plot of the typical gain error changes vs. the clock input frequency, normalized to 100kHz. If after using the AD652 with a full-scale clock frequency of 100kHz it is decided to reduce the necessary gating time by increasing the clock frequency, this plot shows the typical gain changes normalized to the original 100kHz gain.

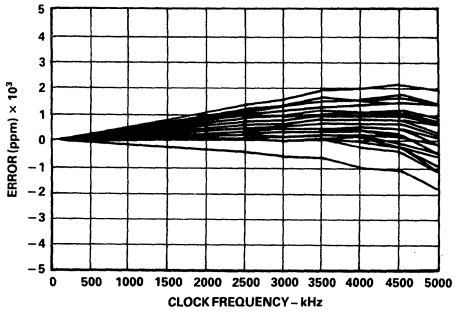


Figure 11. Gain vs. Clock Input

REFERENCE NOISE

The AD652 has on board a precision buffered 5V reference which is available to the user. Besides being used to offset the noninverting comparator input in the voltage-to-frequency mode, this reference can be used for other applications such as offsetting the input to handle bipolar signals and providing bridge excitation. It can source 10mA and sink 100μA, and is short circuit protected. Heavy loading of the reference will not change the gain of the VFC, although it will affect the external reference voltage. For example, a 10mA load interacting with a 0.3Ω typical output impedance will change the reference voltage by 0.06%.

DIGITAL INTERFACING CONSIDERATIONS

The AD652 clock input is a high impedance input with a threshold voltage of two diode voltages with respect to Digital Ground at pin 12 (approximately 1.2 volts at room temp). When the clock input is low, 5-10μA flows out of this pin. When the clock input is high, no current flows.

The frequency output is an open collector pull-down and is capable of sinking 10mA with a maximum voltage of 0.4 volts. This will drive 6 standard TTL inputs. The open collector pull up voltage can be as high as 36 volts above digital ground.

COMPONENT SELECTION

The AD652 integrating capacitor should be 0.02μF. If a large amount of normal mode interference is expected (more than 0.1 volts) and the clock frequency is less than 500kHz, an integrating capacitor of 0.1μF should be used. Mylar, polypropylene, or polystyrene capacitors should be used.

The open collector pull-up resistor should be chosen to give adequately fast rise times. At low clock frequencies (100kHz) larger resistor values (several kΩ) and slower rise times may be tolerated. However, at higher clock frequencies (1MHz) a lower value resistor should be used. The loading of the logic input which is being driven must also be taken into consideration. For example, if 2 standard TTL loads are to be driven then a 3.2mA current must be sunk, leaving 6.8mA for the pull-up resistor if the maximum low level voltage is to be maintained at 0.4 volts. A 680Ω resistor would thus be selected ((5–0.4)V/6.8mA) = 680Ω.

The one-shot capacitor controls the pulse width of the frequency output. The pulse is initiated by the rising edge of the clock signal. The delay time between the rising edge of the clock and the falling edge of the frequency output is typically 200ns. The width of the pulse is 5ns/pF and the minimum width is about 200ns with pin 9 floating. If the one-shot period is accidentally chosen longer than the clock period, the width of the pulse will default to equal the clock period. The one-shot can be disabled by connecting pin 9 to $+V_S$ (Figure 12); the output pulse width will then be equal to the clock period. The one-shot is activated (Figure 13) by connecting a capacitor from pin 9 to $+V_S$, $-V_S$, or Digital Ground($+V_S$ is preferred).

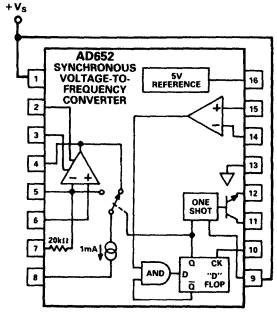


Figure 12. One Shot Disabled

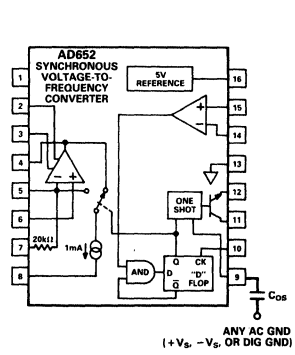


Figure 13. One Shot Enabled

DIGITAL GROUND

Digital Ground can be at any potential between $-V_S$ and ($+V_S$ -4 volts). This can be very useful in a system with derived grounds rather than stiff supplies. For example, in a small isolated power circuit, often only a single supply is generated and the "ground" is set by a divider tap. Such a ground cannot handle the large currents associated with digital signals. With the AD652

SVFC, it is possible to connect the DIG GND to $-V_S$ for a solid logic reference, as shown in Figure 14.

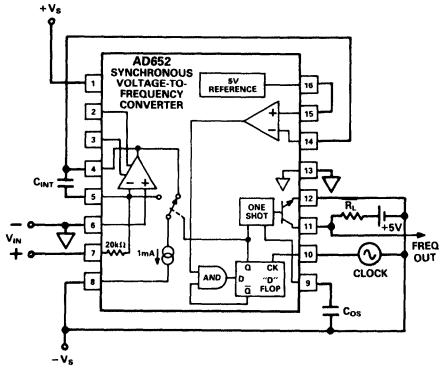


Figure 14. Digital GND at $-V_S$

SINGLE SUPPLY OPERATION

In addition to the Digital Ground being connected to $-V_S$, it is also possible to connect Analog Ground to $-V_S$ of the AD652. Hence, the device is truly operating from a single supply voltage that can range from +12V to +36V. This is shown in Figure 15 for a positive voltage input and Figure 16 for a negative voltage input.

In Figure 15, the comparator reference is used as a derived ground, and the input voltage is referred to this point as well as the op amp common mode (pin 6 is tied to pin 16). Since the input signal source must drive 0.5mA of full-scale signal current into pin 7, it must also draw the exact same current from the input reference potential. This current will thus be provided by the 5V reference.

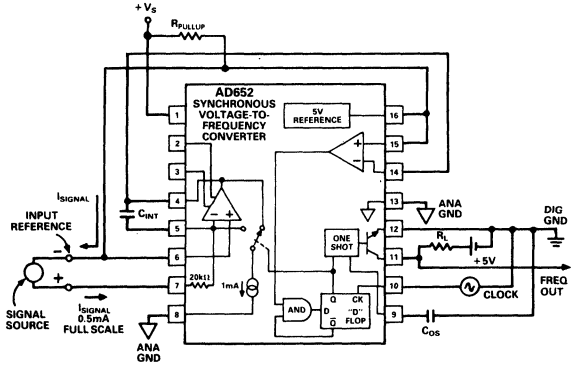


Figure 15. Single Supply Positive Voltage Input

In the single supply operation mode, an external resistor, R_{PULLUP}, is necessary between the power supply, $+V_S$, and the 5V reference output. This resistor should be selected such that a current of approximately 500μA flows during operation. For example, with a power supply voltage of +15V, a 20kΩ resistor would be selected ((15V − 5V)/500μA = 20kΩ).

Figure 16 shows the negative voltage input configuration for use of the AD652 in the single supply mode. In this mode the signal source is driving the "+" input of the op amp which requires only 20nA (typical), rather than the 0.5mA required in the positive input voltage configuration. The voltage at pin 6 may go as low as 4 volts above ground ($-V_S$, pin 8). Since the input reference is 5.0 volts above ground, this leaves a 1V window for the input signal. In order to drive the integrating capacitor with a 0.5mA full-scale current, it is necessary to provide an external 2kΩ resistor. This results in a 2kΩ resistor and a 1V input range. The external 2kΩ resistor should be a low-TC metal-film type for lowest drift degradation.

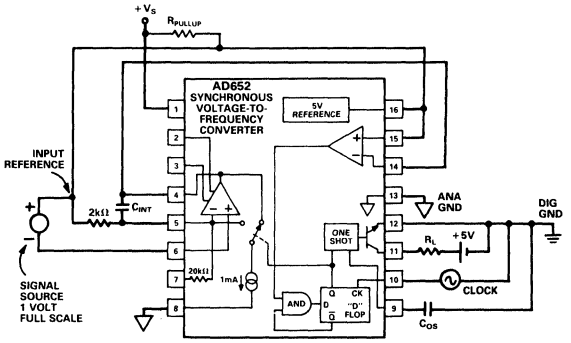


Figure 16. Single Supply Negative Voltage Input

FREQUENCY-TO-VOLTAGE CONVERTER

The AD652 SVFC also works as a frequency-to-voltage converter. Figure 17 shows the connection diagram for F/V conversion. In this case the "−" input of the comparator is fed the input pulses. Either comparator input may be used so that an input pulse of either polarity may be applied to the F/V. In Figure 17 the "+" input is tied to a 1.2V reference and low level TTL pulses are used as the frequency input. The pulse must be low on the falling edge of the clock. On the subsequent rising edge the 1mA current source is switched to the integrator summing junction and ramps up the voltage at pin 4. Due to the action of the AND gate, the 1mA current is switched off after only one clock period. The average current delivered to the summing junction varies from 0 to 0.5mA; using the internal 20kΩ resistor this results in a full-scale output voltage of 10V at pin 4.

The frequency response of the circuit is determined by the capacitor; the −3dB frequency is simply the RC time constant. A tradeoff exists between ripple and response. If low ripple is desired, a large value capacitor must be used (1μF), if fast response is needed, a small capacitor is used (1nF minimum).

The op amp can drive a 5kΩ resistor load to 10V, using a 15V positive power supply. If a large load capacitance (0.01μF) must be driven, then it is necessary to isolate the load with a 50Ω resistor as shown. Since the 50Ω resistor is 0.25% of the full scale, and the specified gain error with the 20kΩ resistor is ±0.5%, this extra resistor will only increase the total gain error to +0.75% max.

The circuit shown is unipolar and only a 0 to +10V output is allowed. The integrator op amp is not a general purpose op amp, rather it has been optimized for simplicity and high speed. The most significant difference between this amplifier and a general purpose op amp is the lack of an integrator (or level shift) stage. Consequently, the voltage on the output (pin 4) must always be more positive than 1 volt below the inputs (pins 6 and 7). For example, in the F-to-V conversion mode, the noninverting input of the op amp (pin 6) is grounded which

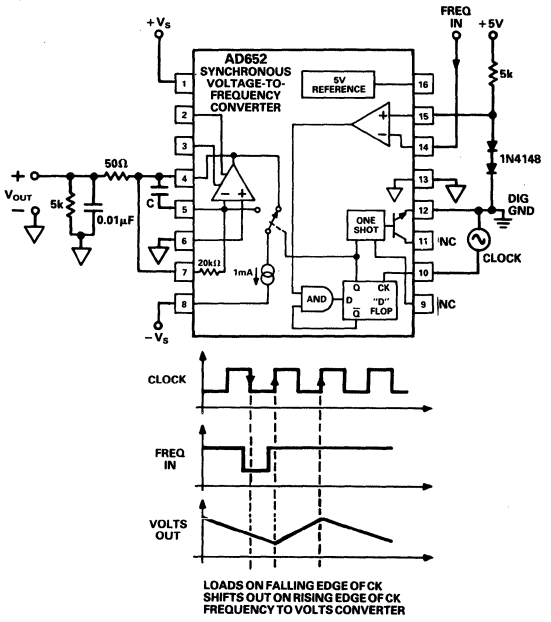


Figure 17. Frequency-to-Voltage Converter

means that the output (pin 4) cannot go below −1 volt. Normal operation of the circuit as shown will never call for a negative voltage at the output.

A second difference between this op amp and a general purpose amplifier is that the output will only sink 1.5mA to the negative supply. The only pulldown other than the 1mA current used for voltage-to-frequency conversion is a 0.5mA source. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 4 volts of the positive supply when not sourcing external current. When sourcing 10mA, the output voltage may be driven to within 6 volts of the positive supply.

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD652.

In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the AD652 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to exploit the full linearity and dynamic range of the AD652.

Separate digital and analog grounds are provided on the AD652. The emitter of the open collector frequency output transistor and the clock input threshold only are returned to the digital ground. Only the 5V reference is connected to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. Much noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At high full-scale frequencies, it is necessary to use a pull-up resistor of about 500Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10mA. This much current being switched will cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20nH per inch; a current of 10mA being switched in 50ns at the end of 12 inches of 20 gauge wire will produce a voltage spike of 50mV. The separate digital ground of the AD652 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD652 package. A 1μF to 10μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground, pin 12. The pull-up resistor should be connected directly to the frequency output, pin 11. The lead lengths on the bypass capacitor and the pull-up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull-up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (pin 12) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current. There may be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause a problem. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (pin 6) at the package. More information on proper grounding and reduction of interference can be found in reference 1.

FREQUENCY OUTPUT MULTIPLIER

The AD652 can serve as a frequency output multiplier when used in conjunction with a standard voltage-to-frequency converter. Figure 18 shows the low cost AD654 VFC being used as the clock input to the AD652. Also shown is a second AD652 in the F/V mode. The AD654 is set up to produce an output frequency of 0-500kHz for an input voltage (V_1) range of 0-10V. The use of R4, C1, and the XOR gate doubles this output frequency from 0-500kHz to 0-1MHz.

This 1MHz full-scale frequency is then used as the clock input to the AD652 SVFC. Since the AD652 full-scale output frequency is one-half the clock frequency, the 1MHz FS clock frequency establishes a 500kHz maximum output frequency for the AD652 when its input voltage (V_2) is +10V. The user thus has an output frequency range from 0-500kHz which is proportional to the product of V_1 and V_2.

[1]"Noise Reduction Techniques in Electronic Systems", by H.W. Ott, (John Wiley, 1976).

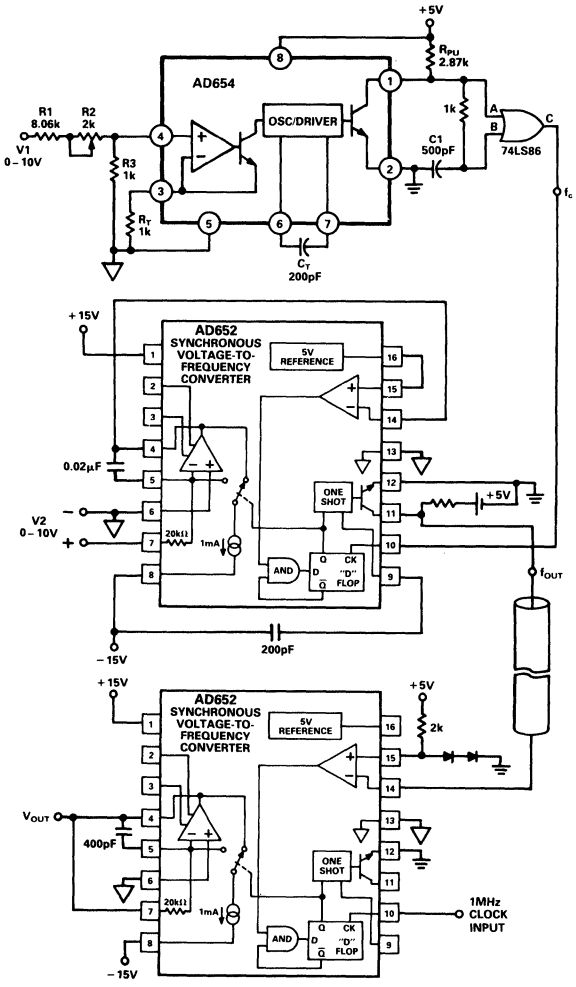


Figure 18. Frequency Output Multiplier

This can be shown in equation form, where f_C is the AD654 output frequency and f_{OUT} is the AD652 output frequency:

$$f_C = V_1 \frac{1MHz}{10V}$$

$$f_{OUT} = V_2 \left(\frac{f_C/2}{10V}\right)$$

$$f_{OUT} = V_1 V_2 \left(\frac{1MHz}{2(10V)\,(10V)}\right)$$

$$f_{OUT} = V_1 \cdot V_2 \cdot 5kHz/V^2$$

The scope photo in Figure 19 shows V_1 and V_2 (top two traces) and the output of the F-V (bottom trace).

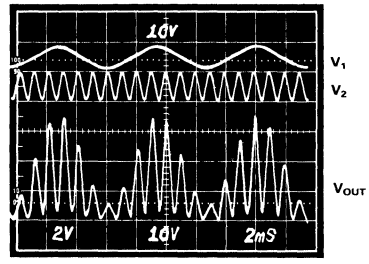


Figure 19. Multiplier Waveforms

SINGLE-LINE MULTIPLEXED DATA TRANSMISSION

It is often necessary to measure several different signals and relay the information to some remote location using a minimum amount of cable. Multiple AD652 SVFC devices may be used with a multiphase clock to combine these measurements for serial transmission and demultiplexing. Figure 20 shows a block diagram of a single-line multiplexed data transmission system with high noise immunity. Figures 21, 22 and 23 show the SVFC multiplexer, a representative means of data transmission, and an SVFC demultiplexer respectively.

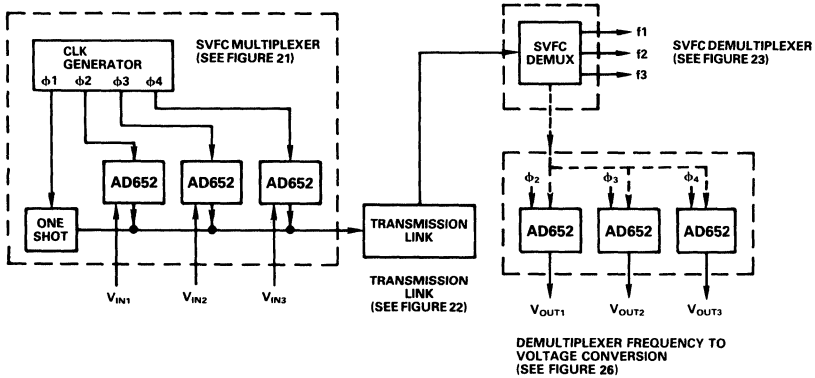


Figure 20. Single Line Multiplexed Data Transmission Block Diagram

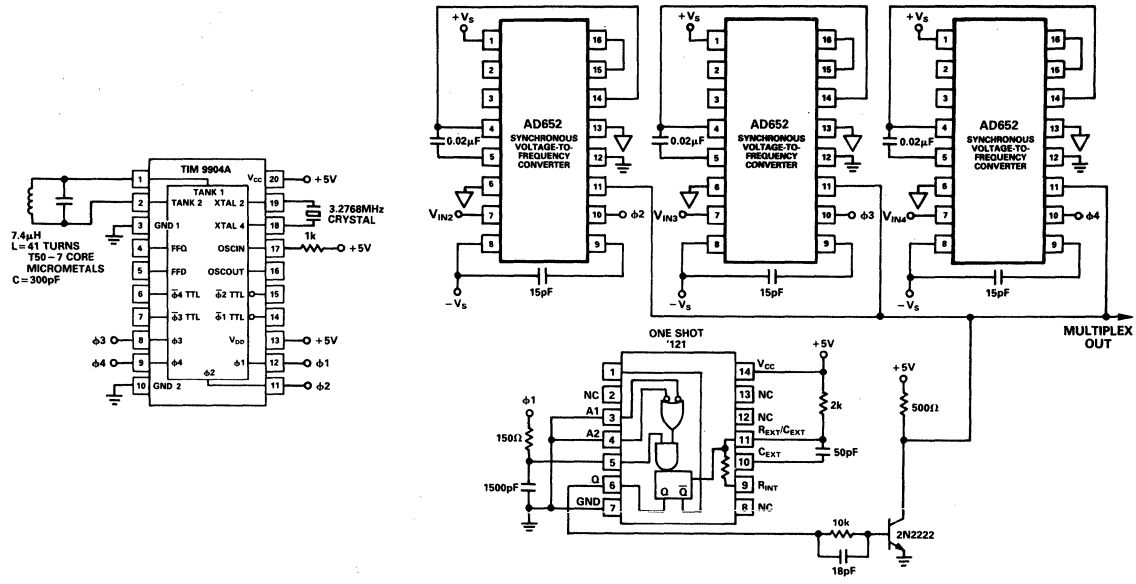


Figure 21. SVFC Multiplexer

Multiplexer

Figure 21 shows the SVFC multiplexer. The clock inputs for the several SVFC channels are generated by a TIM9904A four phase clock driver, and the frequency outputs are combined by strapping all the frequency output pins together (a "wire or" connection). The one-shot in the AD652 sets the pulse width of the frequency output pulses to be slightly shorter than one quarter of the clock period. Synchronization is achieved by applying one of the four available phases to a fixed TTL one-shot ('121) and combining the output with an external transistor. The width of this sync pulse is shorter than the width of the frequency output pulses to facilitate decoding the signal. The RC lag network on the input of the one-shot provides a slight delay between the rising edge of the clock and the sync pulse in order to match the 150ns delay of the AD652 between the rising edge of the clock and the output pulse.

Transmitter

The multiplex signal can be transmitted in any manner suitable to the task at hand. A pulse transformer or an opto-isolator can provide galvanic isolation; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber-optic link; telemetry can be accomplished with a radio link. The circuit shown in Figure 22 uses an EIA RS-422 standard for digital data transmission over a balanced line. Figure 24 shows the waveforms of the four clock phases and the multiplex output signal. Note that the sync pulse is present every clock cycle, but the data pulses are no more frequent than every other clock cycle since the maximum output frequency from the SVFC is half the clock frequency. The clock frequency used in this circuit is 819.2 kHz and will provide more than 16 bits of resolution if 100 millisecond gate time is allowed for counting pulses of the decoded output frequencies.

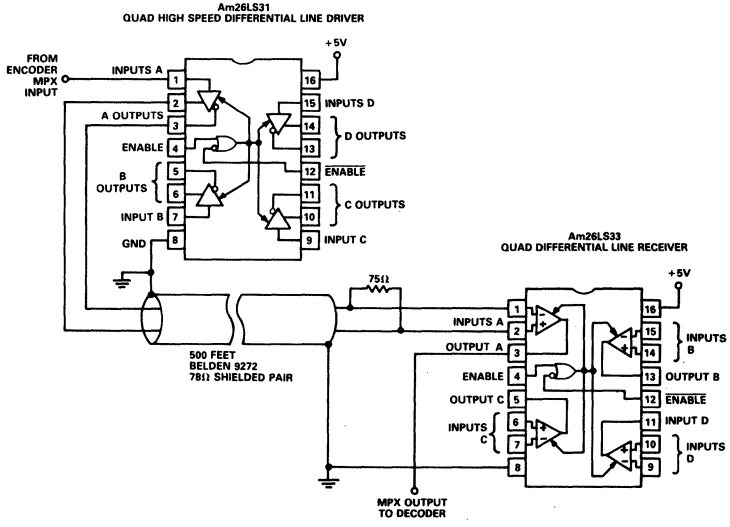


Figure 22. RS-422 Standard Data Transmission

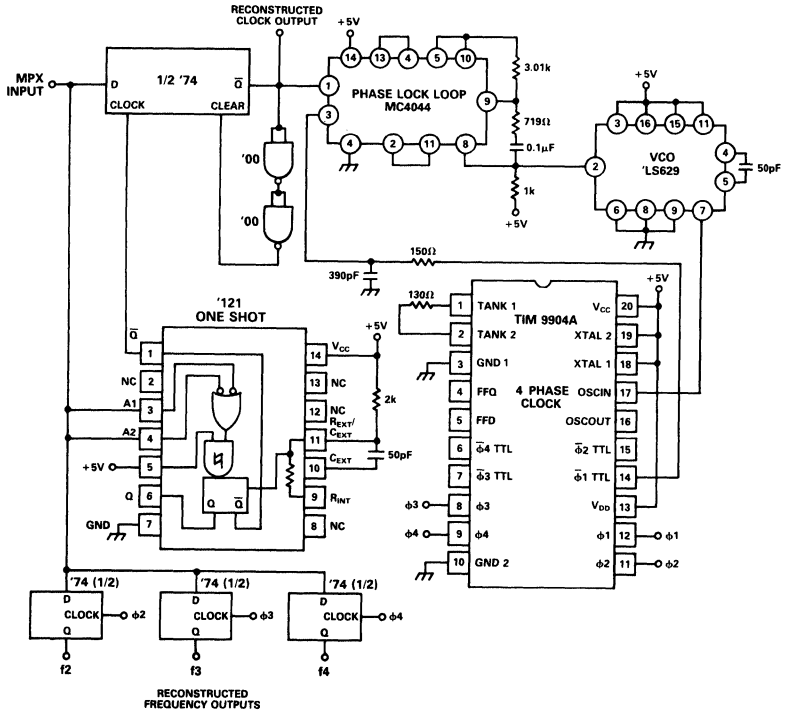


Figure 23. SVFC Demultiplexers

SVFC Demultiplexer

The demultiplexer needed to separate the combined signals is shown in Figure 23. A phase locked loop drives another four phase clock chip to lock onto the reconstructed clock signal. The sync pulses are distinguished from the data pulses by their shorter duration. Each falling edge on the multiplex input signal triggers the one-shot, and at the end of this one-shot pulse the multiplex input signal is sampled by a D-type flip-flop. If the signal is high, then the pulse was short (a sync pulse) and the $\overline{Q}$ output of the D-flop goes low. The D-flop is cleared a short time (two gate delays) later, and the clock is reconstructed as a stream of short, low-going pulses. If the Multiplex input is a data pulse, then when the D-flop samples at the end of the one-shot period, the signal will still be low and no pulse will appear at the reconstructed clock output. These waveforms are shown in Figure 25.

If it is desired to recover the individual frequency signals, then the multiplex input is sampled with a D-flop at the appropriate time as determined by the rising edge of the various phases generated by the clock chip. These frequency signals can be counted as a ratio relative to the reconstructed clock, so it is not even necessary for the transmitter to be crystal controlled as shown here.

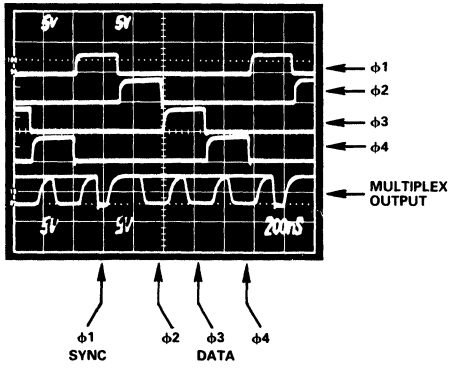


Figure 24. Multiplexer Waveforms

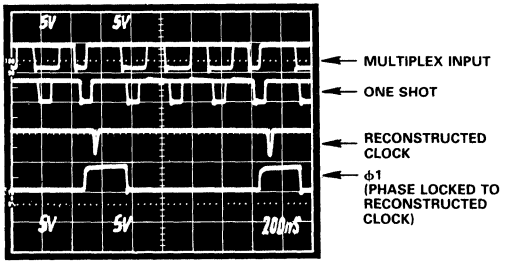
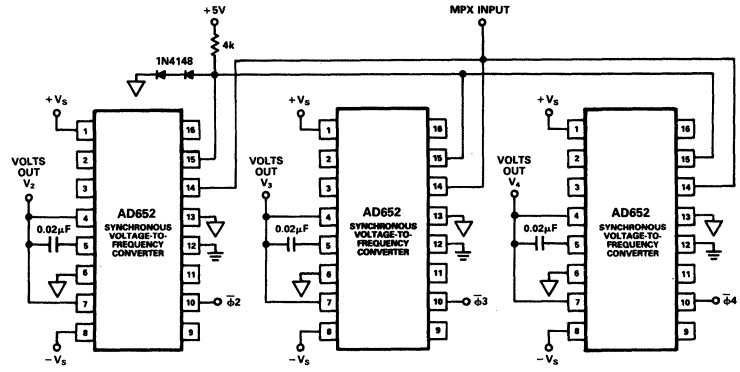


Figure 25. Demultiplexer Waveforms



Φ2, Φ3, Φ4 ARE PINS 15, 7, 6 of TIM9904A FROM DEMUX FIGURE 23

Figure 26. Demultiplexer Frequency-to-Voltage Conversion

Analog Signal Reconstruction

If it is desired to reconstruct the analog voltages from the multiplex signal, then three more AD652 SVFC devices are used as frequency-to-voltage converters, as shown in Figure 26. The comparator inputs of all the devices are strapped together, and the "+" inputs are held at a 1.2 volt TTL threshold, while the "−" inputs are driven by the multiplex input. The three clock inputs are driven by the $\bar{\phi}$ outputs of the clock chip. Remember that data at the comparator input of the SVFC is loaded on the falling edge of the clock signal and shifted out on the next rising edge. Note that the frequency signals for each data channel are available at the frequency output pin of each FVC.

ISOLATED FRONT END

In some applications it may be necessary to have complete galvanic isolation between the analog signals being measured and the digital portions of the circuit. The circuit shown in Figure 27 runs off a single 5 volt power supply and provides a self-contained, completely isolated analog measurement system. The power for the AD652 SVFC is provided by a chopper and a transformer, and is regulated to ±15 volts.

Both the chopper frequency and the AD652 clock frequency are 125kHz, with the clock signal being relayed to the SVFC through the transformer. The frequency output signal is relayed through an opto-isolator and latched into a D-flop. The chopper frequency is generated from an AD654 VFC and is frequency divided by two to develop differential drive for the chopper transistors, and to ensure an accurate 50 percent duty cycle. The pull-up resistors on the D-flop outputs provide a well defined high level voltage to the choppers to equalize the drive in each direction. The 10μH inductor in the +5V lead of the transformer primary is necessary to equalize any residual imbalance in the drive on each half-cycle and thus prevent saturation of the core. The capacitor across the primary resonates the system so that under light loading conditions on the secondary the wave shape will be

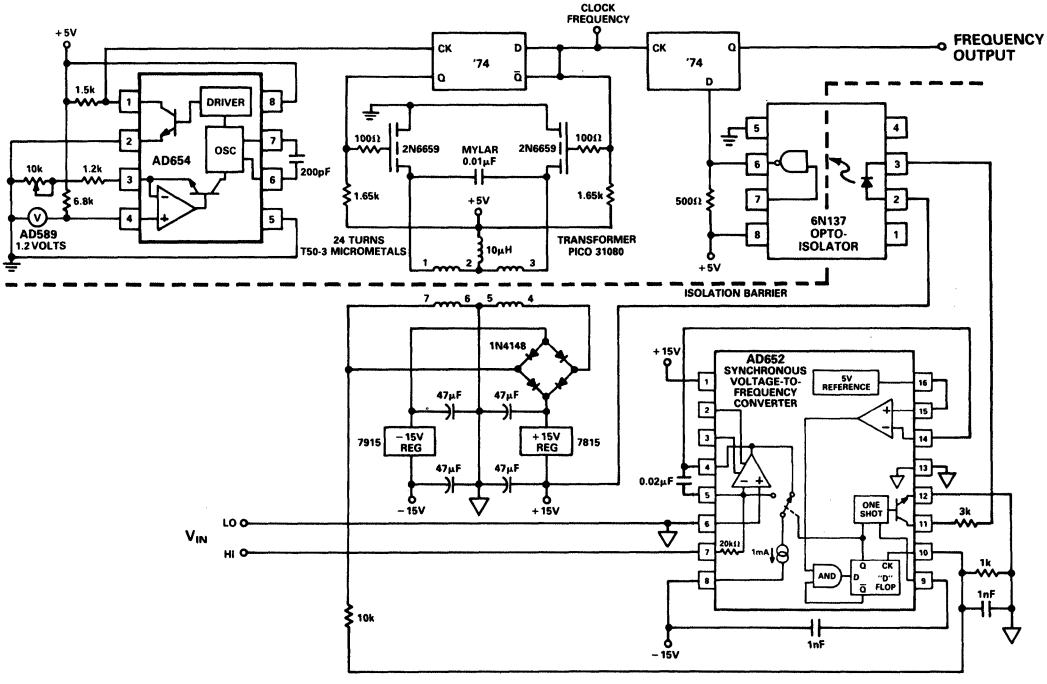


Figure 27. Isolated Synchronous VFC

sinusoidal and the clock frequency will be relayed to the SVFC. To adjust the chopper frequency, disconnect any load on the secondary and tune the AD654 for a minimum in the supply current drawn from the 5 volt supply.

A-TO-D CONVERSION

In performing an A-to-D conversion, the output pulses of a VFC are counted for a fixed gate interval. To achieve maximum performance with the AD652, the fixed gate interval should be generated using a multiple of the SVFC clock input. Counting in this manner will eliminate any errors due to the clock (whether it be jitter, drift with time or temperature, etc.) since it is the ratio of the clock and output frequencies that is being measured.

The resolution of the A-to-D conversion measurement is determined by the clock frequency and the gate time. If, for instance, a resolution of 12 bits is desired and the clock frequency is 1MHz (resulting in an AD652 FS frequency of 500kHz) the gate time will be:

$$\left(\frac{\text{FS Freq}}{N}\right)^{-1} = \left(\frac{1}{2}\frac{\text{Clock Freq}}{N}\right)^{-1} = \left(\frac{1\text{MHz}}{2(4096)}\right)^{-1}$$

$$= \frac{8192}{1\times10^6}\ \text{sec} = 8.192\text{ms}$$: Where N is the total number of codes for a given resolution.

Figure 28 shows the AD652 SVFC as an A-to-D converter in block diagram form.

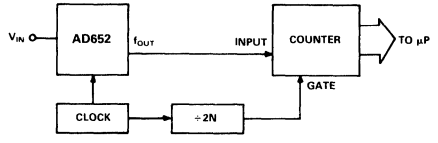


Figure 28. Block Diagram of SVFC A-to-D Converter

To provide the ÷ 2N block a single chip counter such as the 4020B can be used. The 4020B is a 14-stage binary ripple counter which has a clock and master reset for inputs, and buffered outputs from the first stage and the last eleven stages. The output of the first stage is $f_{CLOCK} \div 2^1 = f_{CLOCK}/2$, while the output of the last stage is $f_{CLOCK} \div 2^{14} = f_{CLOCK}/16384$. Hence using this single chip counter as the ÷ 2N block, 13-bit resolution can be achieved. Higher resolution can be achieved by cascading D-type flip-flops or another 4020B with the counter.

Table I shows the relationship between clock frequency and gate time for various degrees of resolution. Note that if the variables are chosen such that the gate times are multiples of 50, 60 or 400Hz, normal-mode rejection (NMR) of those line frequencies will occur.

Resolution	N	Clock	Conversion or Gate Time	Typ Lin	Comments
12 Bits	4096	81.92kHz	100ms	0.002%	50, 60, 400Hz NMR
12 Bits	4096	2MHz	4.096ms	0.01%	
12 Bits	4096	4MHz	2.048ms	0.02%	
4 Digits	10000	200kHz	100ms	0.002%	50, 60, 400Hz NMR
14 Bits	16384	327.68kHz	100ms	0.002%	50, 60, 400Hz NMR
14 Bits	16384	1.966MHz	16.66ms	0.01%	60Hz NMR
14 Bits	16384	1.638MHz	20ms	0.01%	50Hz NMR
4 1/2 Digits	20000	400kHz	100ms	0.002%	50, 60, 400Hz NMR
16 Bits	65536	655.36kHz	200ms	0.002%	50, 60, 400Hz NMR
16 Bits	65536	4MHz	32.77ms	0.02%	

Table I.

DELTA MODULATOR

The circuit of Figure 29 shows the AD652 configured as a delta modulator. A reference voltage is applied to the input of the integrator (pin 7), which sets the steady state output frequency at one-half of the AD652 full-scale frequency (1/4 of the clock frequency). As a 0 to 10V input signal is applied to the comparator (pin 15), the output of the integrator attempts to track this signal. For an input in an idling condition (dc) the output frequency will be one-half full scale. For positive going signals the output frequency will be between one-half full scale and full scale, and for negative going signals the output frequency will be between zero and one-half full scale. The output frequency will correspond to the slope of the comparator input signal.

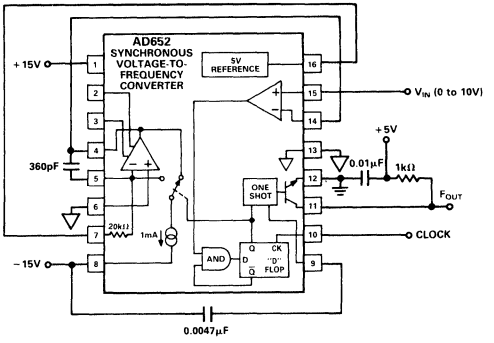


Figure 29. Delta Modulator

Since the output frequency corresponds to the slope of the input signal, the delta modulator acts as a differentiator. A delta modulator is thus a direct way of finding the derivative of a signal. This is useful in systems where, for example, a signal corresponding to velocity exists and it is desired to determine acceleration.

Figure 30 is a scope photo showing a 20kHz, 0 to 10V sine wave used as the input to the comparator and its ramp-wise approximation at the integrator output. The clock frequency used as 2MHz and the integrating capacitor was 360pF. Figure 31 shows the same input signal and its ramp-wise approximation, along with the output frequency corresponding to the derivative of the input signal. In this case the clock frequency was 850kHz.

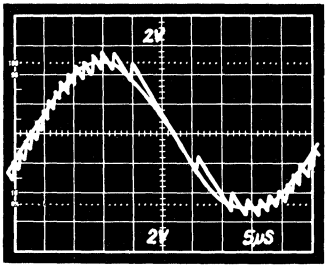


Figure 30. Delta Modulator Input Signal and Ramp-Wise Approximation

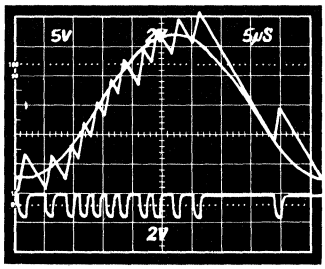


Figure 31. Delta Modulator Input Signal, Ramp-Wise Approximation and Output Frequency

The choice of an integrating capacitor is primarily dictated by the input signal bandwidth. Figure 32 shows this relationship. It should be noted that as the value of C_{INT} is lowered, the ramp size of the integrator approximation becomes larger. This can be compensated for by increasing the clock frequency. The effect of the clock frequency on the ramp size is demonstrated in Figures 30 and 31.

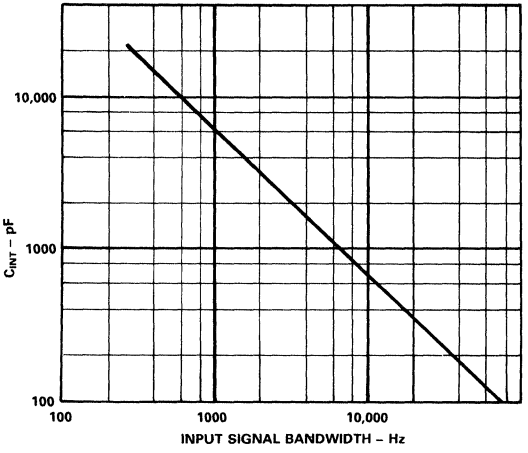


Figure 32. Maximum Integrating Cap Value vs. Input Signal Bandwidth

BRIDGE TRANSDUCER INTERFACE

The circuit of Figure 33 illustrates a simple interface between the AD652 and a bridge-type transducer. The AD652 is an ideal choice because its buffered 5 volt reference can be used as the bridge excitation thereby ratiometrically eliminating the gain drift related errors. This reference will provide a minimum of 10mA of external current, which is adequate for bridge resistance of 600Ω and above. If, for example, the bridge resistance is 120Ω or 350Ω, an external pull-up resistor (R_{PU}) is required and can be calculated using the formula:

$$R_{PU}\ (max) = \frac{+V_S - 5V}{\frac{5V}{R_{BRIDGE}} - 10mA}$$

An instrumentation amplifier is used to condition the bridge signal before presenting it to the SVFC. The AD625, with its high CMRR, minimizes common-mode errors and also can be set to arbitrary gains between 1 and 10,000 via three resistors, simplifying the scaling for the AD652's calibrated 10 volt input range. These resistors should be selected such that the following equation holds:

$$10V = V_{BRIDGE}\left(\frac{2R_F}{R_G} + 1\right)$$

where $10k\Omega \leq R_F \leq 20k\Omega$, and V_{BRIDGE} is the maximum output voltage of the bridge.

The bridge output may be unipolar, as is the case for most pressure transducers, or it may be bipolar as in some strain measurements. If the signal is unipolar, the reference input of the AD625 (pin 7) is simply grounded. If the bridge has a bipolar output, however, the AD652 reference can be tied to pin 7, thereby converting a ±5 volt signal (after gain) into a 0 to +10 volt input for the SVFC.

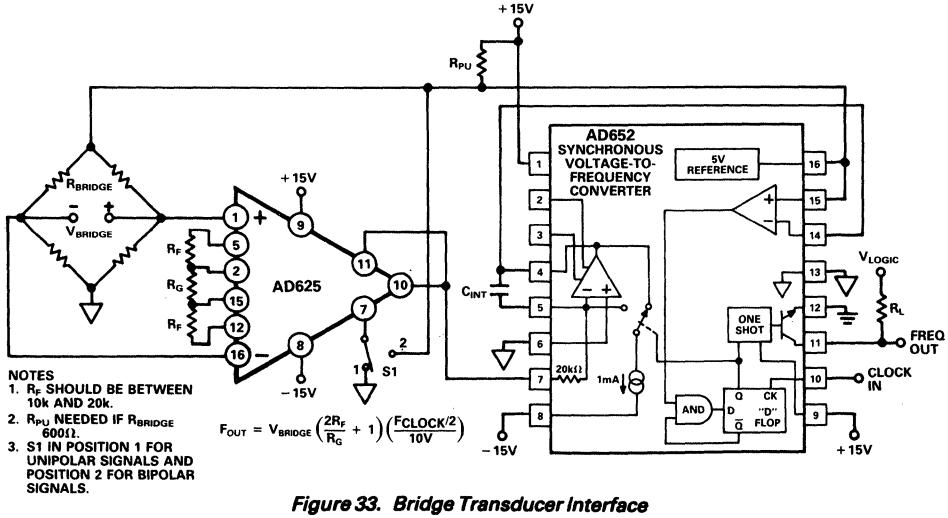


Figure 33. Bridge Transducer Interface

ANALOG DEVICES

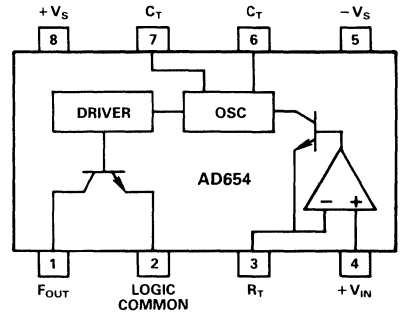
Low Cost Monolithic Voltage-to-Frequency Converter

AD654

FEATURES

- **Low Cost**
- **Single or Dual Supply, 5 to 36 Volts, ±5V to ±18V**
- **Full Scale Frequency Up to 500kHz**
- **Minimum Number of External Components Needed**
- **Versatile Input Amplifier**
  - **Positive or Negative Voltage Modes**
  - **Negative Current Mode**
  - **High Input Impedance, Low Drift**
- **Low Power: 2.0mA Quiescent Current**
- **Low Offset: 1mV**

AD654 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD654 is a monolithic V/F converter consisting of an input amplifier, a precision oscillator system, and a high current output stage. A single RC network is all that is required to set up any full scale (F.S.) frequency up to 500kHz and any F.S. input voltage up to ±30V. Linearity error is only 0.03% for a 250kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±50ppm/°C. The AD654 operates from a single supply of 5 to 36V and consumes only 2.0mA quiescent current.

The low drift (4μV/°C typ) input amplifier allows operation directly from small signals such as thermocouples or strain gauges while offering a high (250MΩ) input resistance. Unlike most V/F converters, the AD654 provides a square-wave output, and can drive up to 12 TTL loads, opto-couplers, long cables, or similar loads.

PRODUCT HIGHLIGHTS

1. Packaged in both an 8-pin mini-DIP and an 8-pin SOIC package, the AD654 is a complete V/F converter requiring only an RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of the timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, $f = V/10RC$.
2. A minimum number of low cost external components are necessary. A single RC network is all that is required to set up any full scale frequency up to 500kHz and any full scale input voltage up to ±30V.
3. Plastic packaging allows low cost implementation of the standard VFC applications: A/D conversion, isolated signal transmission, F/V conversion, phase-locked loops, and tuning switched-capacitor filters.
4. Power supply requirements are minimal; only 2.0mA of quiescent current is drawn from the single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to $(+V_S - 4)$ volts. Negative inputs can easily be connected for below ground operation.
5. The versatile open-collector output stage can sink more than 10mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

SPECIFICATIONS (t_{AMB} = +25°C and V_S (total) = 5 to 16.5V, unless otherwise specified. All testing done @ V_S = +5V).

Model	AD654JN/JR Min	Typ	Max	Units
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0		500	kHz
Nonlinearity[1]				
f_{max} = 250kHz		0.06	**0.1**	%
f_{max} = 500kHz		0.20	0.4	%
Full Scale Calibration Error				
C = 390pF, I_{IN} = 1.000mA	**−10**		**10**	%
vs. Supply ($f_{max} \leq$ 250kHz)				
V_S = +4.75 to +5.25V		0.20	**0.40**	%/V
V_S = +5.25 to +16.5V		0.05	**0.10**	%/V
vs. Temp (0 to 70°C)		50		ppm/°C
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0		(+V_S −4)	V
Dual Supply	−V_S		(+V_S −4)	V
Input Bias Current				
(Either Input)		30	**50**	nA
Input Offset Current		5		nA
Input Resistance (Non-Inverting)		250		MΩ
Input Offset Voltage		0.5	**1.0**	mV
vs. Supply				
V_S = +4.75 to +5.25V		0.1	**0.25**	mV/V
V_S = +5.25 to +16.5V		0.03	**0.1**	mV/V
vs. Temp (0 to 70°C)		4		μV/°C
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"[2]				
V_{OUT} = 0.4V max, 25°C	**10**	20		mA
V_{OUT} = 0.4V max, 0 to 70°C	5	10		mA
Output Leakage Current in Logic "1"		10	**100**	nA
0 to 70°C		50	500	nA
Logic Common Level Range	−V_S		(+V_S −4)	V
Rise/Fall Times (C_T = 0.01μF)				
I_{IN} = 1mA		0.2		μs
I_{IN} = 1μA		1		μs
POWER SUPPLY				
Voltage, Rated Performance	4.5		16.5	V
Voltage, Operating Range				
Single Supply	4.5		36	V
Dual Supply	±5		±18	V
Quiescent Current				
V_S (Total) = 5V		1.5	**2.5**	mA
V_S (Total) = 30V		2.0	**3.0**	mA
TEMPERATURE RANGE				
Operating Range	−40		85	°C
PACKAGE OPTIONS[3]				
SOIC (R-8)		AD654JR		
Plastic DIP (N-8)		AD654JN		

NOTES

[1]At f_{max} = 250kHz; R_T = 1kΩ, C_T = 390pF, I_{IN} = 0-1mA.
f_{max} = 500kHz; R_T = 1kΩ, C_T = 200pF, I_{IN} = 0-1mA.

[2]The sink current is the amount of current that can flow into Pin 1 of the AD654 while maintaining a maximum voltage of 0.4V between Pin 1 and Logic Common.

[3]See Section 14 for package outline information.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage
(Pins 3, 4) to $-V_S$ . . . . . $-300mV$ to $+V_S$
Maximum Output Current
Instantaneous 50mA
Sustained 25mA
Logic Common to $-V_S$ . . . . . $-500mV$ to $(+V_S - 4)$
Storage Temperature Range . . . . . $-65°C$ to $+150°C$

CIRCUIT OPERATION

The AD654's block diagram appears in Figure 1. A versatile operational amplifier serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter (an astable multivibrator). The drive current provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 100nA to 2mA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a level other than $-V_S$.

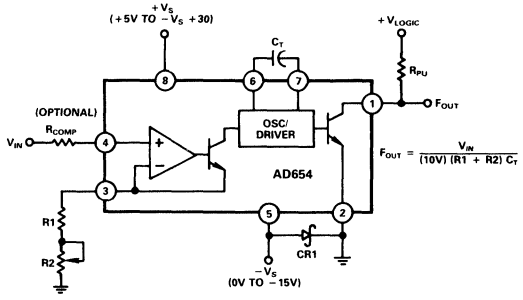


Figure 1. Standard V-F Connection for Positive Input Voltages

V/F CONNECTION FOR POSITIVE INPUT VOLTAGES

In the connection scheme of Figure 1, the input amplifier presents a very high (250MΩ) impedance to the input voltage, which is converted into the proper drive current by the scaling resistors at pin 3. Resistors R1 and R2 are selected to provide a 1mA full scale current with enough trim range to accommodate the AD654's 10% FS error and the components' tolerances. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive. The AD654's positive input voltage range spans from $-V_S$ (ground in single supply operation) to four volts below the positive supply. Power supply rejection degrades as the input exceeds $(+V_S - 3.75V)$ and at $(+V_S - 3.5V)$ the output frequency goes to zero.

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. Good V/F linearity requires the use of a capacitor with low dielectric absorption (DA), while the most stable operation over temperature calls for a component having a small tempco. Polystyrene, polypropylene, or Teflon* capacitors are preferred for tempco and dielectric absorption; other types will degrade linearity. The capacitor should be wired very close to the AD654. In Figure 1, Schottky diode CR1 (MBD101) prevents logic common from dropping more than 500mV below $-V_S$. This diode is not required if $-V_S$ is equal to logic common.

*Teflon is a trademark of E. I. Du Pont de Nemours & Co.

V/F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

The AD654 can accommodate a wide range of negative input voltages with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance because the signal source must supply the 1mA F.S. drive current. However, large negative voltages beyond the supply can be handled easily by modifying the scaling resistors appropriately. If the input is a true current source, R1 and R2 are not used. Again, diode CR1 prevents latch-up by insuring Logic Common does not drop more than 500mV below $-V_S$. The clamp diode (MBD101) protects the AD654 input from "below $-V_S$" inputs.

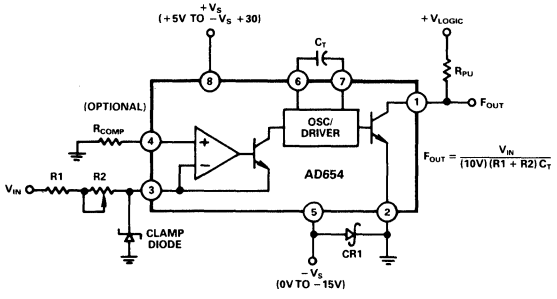


Figure 2. V-F Connections for Negative Input Voltages or Current

OFFSET CALIBRATION

In theory, two adjustments calibrate a V/F: scale and offset. In practice, most applications find the AD654's 1mV max voltage offset sufficiently low to forgo offset calibration. However, the input amplifier's 30nA (typ) bias currents will generate an offset due to the difference in DC source resistance between the input terminals. This offset can be substantial for large values of $R_T = R_1 + R_2$ and will vary as the bias currents drift over temperature. Therefore, to maintain the AD654's low offset, the application may require balancing the DC source resistances at the inputs (pins 3 and 4).

For positive inputs, this is accomplished by adding a compensation resistor nominally equal to R_T in series with the input as shown in Figure 3a. This limits the offset to the product of the 30nA bias current and the mismatch between the source resistance R_T and R_{COMP}. A second, smaller offset arises from the inputs' 5nA offset current flowing through the source resistance R_T or R_{COMP}. For negative input voltage and current connections, the compensation resistor is added at pin 4 as shown in Figure 3b in lieu of grounding the pin directly. For both positive and negative inputs, the use of R_{COMP} may lead to noise coupling at pin 4 and should therefore be bypassed for lowest noise operation.

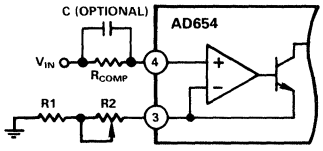


Figure 3a. Bias Current Compensation – Positive Inputs

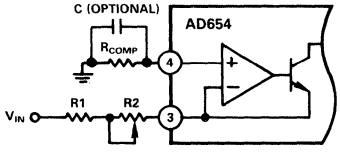


Figure 3b. Bias Current Compensation – Negative Inputs

If the AD654's 1mV offset voltage must be trimmed, the trim must be performed external to the device. Figure 3c shows an optional connection for positive inputs in which R_{OFF1} and R_{OFF2} add a variable resistance in series with R_T. A variable source of ±0.6V applied to R_{OFF1} then adjusts the offset ±1mV. Similarly, a ±0.6V variable source is applied to R_{OFF} in Figure 3d to trim offset for negative inputs. The ±0.6V bipolar source could simply be an AD589 reference connected as shown in Figure 3e.

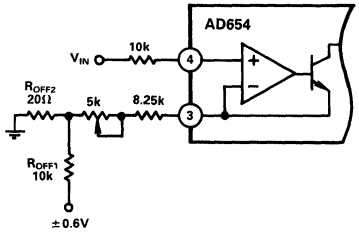


Figure 3c. Offset Trim Positive Input (10V FS)

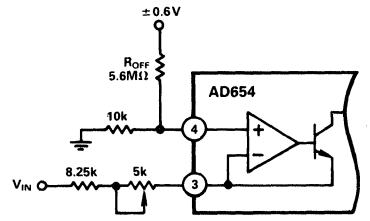


Figure 3d. Offset Trim Negative Input (–10V FS)

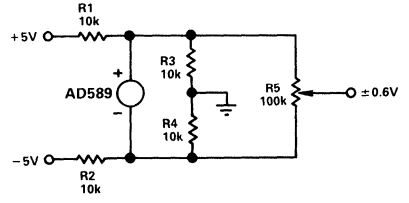


Figure 3e. Offset Trim Bias Network

FULL SCALE CALIBRATION

Full scale trim is the calibration of the circuit to produce the desired output frequency with a full scale input applied. In most cases this is accomplished by adjusting the scaling resistor R_T. Precise calibration of the AD654 requires the use of an accurate voltage standard set to the desired FS value and an accurate frequency meter. A scope is handy for monitoring output waveshape. Verification of converter linearity requires the use of a switchable voltage source or DAC having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. Since each AD654 is factory tested for linearity, it is unnecessary for the end-user to perform this tedious and time consuming test on a routine basis.

Sufficient FS calibration trim range must be provided to accommodate the worst-case sum of all major scaling errors. This includes the AD654's 10% full scale error, the tolerance of the fixed scaling resistor, and the tolerance of the timing capacitor. Therefore, with a resistor tolerance of 1% and a capacitor tolerance of 5%, the fixed part of the scaling resistor should be a maximum of 84% of nominal, with the variable portion selected to allow 116% of the nominal.

If the input is in the form of a negative current source, the scaling resistor is no longer required, eliminating the capability of trimming FS frequency in this fashion. Since it is usually not practical to smoothly vary the capacitance for trimming purposes, an alternative scheme such as the one shown in Figure 4 is needed. Designed for a FS of 1mA, this circuit divides the input into two current paths. One path is through the 100Ω

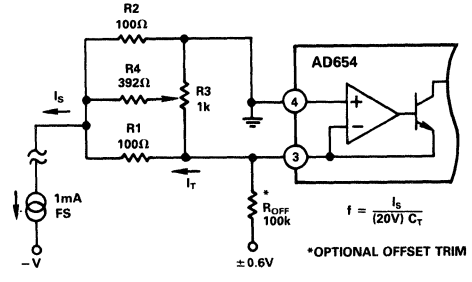


Figure 4. Current Source FS Trim

resistor R1, and flowing into pin 3; it constitutes the signal current I_T to be converted. The second path, through another 100Ω resistor R2, carries the same nominal current. Two equal valued resistors offer the best overall stability, and should be either 1% discrete film units, or a pair from a common array.

Since the 1mA FS input current is divided into two 500μA legs (one to ground and one to pin 3), the total input signal current (I_S) is divided by a factor of two in this network. To achieve the same conversion scale factor, C_T must be reduced by a factor of two. This results in a transfer unique to this hookup:

$$f = \frac{I_S}{(20V)\,C_T}$$

For calibration purposes, resistors R3 and R4 are added to the network, allowing a ±15% trim of scale factor with the values shown. By varying R4's value the trim range can be modified to accommodate wider tolerance components or perhaps the calibration tolerance on a current output transducer such as the AD592 temperature sensor. Although the values of R1 – R4 shown are valid for 1mA FS signals only, they can be scaled upward proportionately for lower FS currents. For instance, they should be increased by a factor of ten for a FS current of 100μA.

In addition to the offsets generated by the input amplifier's bias and offset currents, an offset voltage induced parasitic current arises from the current fork input network. These effects are minimized by using the bias current compensation resistor R_{OFF} and offset trim scheme shown in Figure 3e.

Although device warmup drifts are small, it is good practice to allow the devices operating environment to stabilize before trim, and insure the supply, source and load are appropriate. If provision is made to trim offset, begin by setting the input to 1/10,000 of full scale. Adjust the offset pot until the output is 1/10,000 of full scale (for example, 25Hz for a FS of 250kHz). This is most easily accomplished using a frequency meter connected to the output. The FS input should then be applied and the gain pot should be adjusted until the desired FS frequency is indicated.

INPUT PROTECTION

The AD654 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions. Thus $+V_{IN}$ and R_T pins should not be driven more than 300mV below $-V_S$. Likewise, Logic Common should not drop more than 500mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. In addition to the diode shown in Figures 1 and 2 protecting Logic Common, a second Schottky diode (MBD101) can protect the AD654's inputs from "below $-V_S$" inputs as shown in Figure 5. It is also desirable not to drive $+V_{IN}$ and R_T above $+V_S$. In operation, the converter will exhibit a zero output for inputs above ($+V_S - 3.5V$). Also, control currents above 2mA will increase nonlinearity.

The AD654's 80dB dynamic range guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to input. For example, when scaled to accept an FS input of 1V, the −80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes

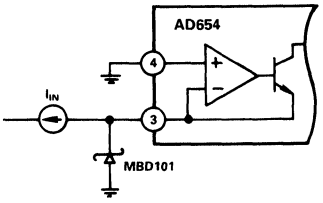


Figure 5. Input Protection

of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter or a guard ring around the R_T pin. The filter can be assembled using the bias current compensation resistor discussed in the previous section. For an FS of 10kHz, a single-pole filter with a time constant of 100ms will be suitable, but the optimum configuration will depend on the application and the type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA full integration of additive input noise occurs. Like the inputs, the capacitor terminals are sensitive to interference from other signals. The timing capacitor should be located as close as possible to the AD654 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in the system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD654. A proper ground scheme appears in Figure 6.

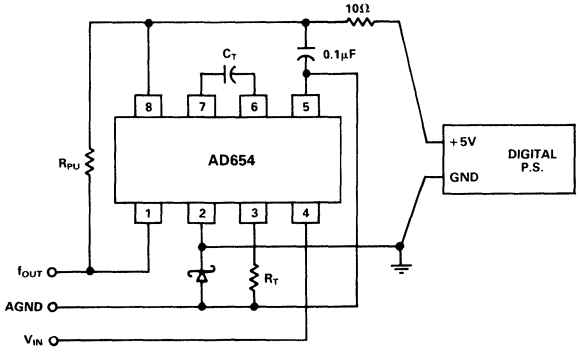


Figure 6. Proper Ground Scheme

OUTPUT INTERFACING CONSIDERATIONS

The output stage's design allows easy interfacing to all digital logic families. The output NPN transistor's emitter and collector are both uncommitted. The emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$, and the open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can sink over 10mA at a maximum saturation voltage of 0.4V. The stage limits the output current at 25mA and can handle this limit indefinitely without damaging the device.

NONLINEARITY SPECIFICATION

The preferred method of specifying nonlinearity error is in terms of maximum deviation from the ideal relationship after calibrating the converter at full scale. This error will vary with the full scale frequency and the mode of operation. The AD654 operates best at a 150kHz full scale frequency with a negative voltage input; the linearity is typically within 0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the Specifications Table. Typical linearity at various temperatures is shown in Figure 7.

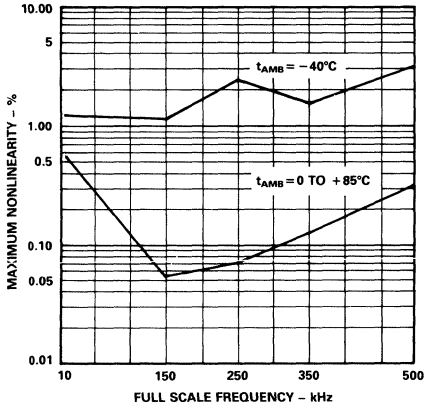


Figure 7. Typical Nonlinearities at Different Full-Scale Frequencies

TWO-WIRE TEMPERATURE-TO-FREQUENCY CONVERSION

Figure 8 shows the AD654 in a two-wire temperature-to-frequency conversion scheme. The twisted pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation.

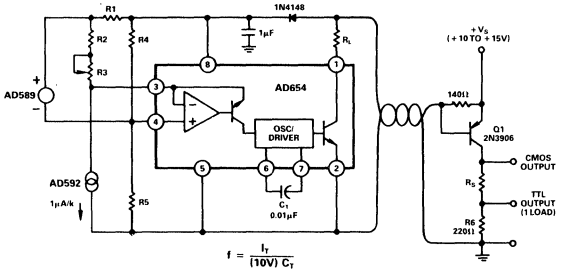


Figure 8. Two-Wire Temperature-to-Frequency Converter

The positive supply line is fed to the remote V/F through a 140Ω resistor. This resistor is selected such that the quiescent current of the AD654 will cause less than one V_{BE} to be dropped. As the V/F oscillates, additional switched current is drawn through R_L when pin 1 goes low. The peak level of this additional current causes Q1 to saturate, and thus regenerates the AD654's output square wave at the collector. The supply voltage to the AD654 then consists of a DC level, less the resistive line drop, plus a one V_{BE} p-p square wave at the output frequency of the AD654. This ripple is reduced by the diode/capacitor combination.

To set up the receiver circuit for a given voltage, the R_S and R_L resistances are selected as shown in Table I. CMOS logic stages can be driven directly from the collector of Q1, and a single TTL load can be driven from the junction of R_S and R6.

$+V_S$	R_S	R_L
10V	270Ω	1.8k
15V	680Ω	2.7k

Table I.

	$(+V_S)$	R1	R2	R3	R4	R5	
K	10V	–	–	–	100k	127k	F = 10Hz/K
	15V	–	–	–	100k	127k	
°C	10V	6.49k	4.02k	1k	95.3k	22.6k	F = 10Hz/°C
	15V	12.7k	4.02k	1k	78.7k	36.5k	
°F	10V	6.49k	4.42k	1k	154k	22.6k	F = 5.55Hz/°F
	15V	12.7k	4.42k	1k	105k	36.5k	

Table II.

At the V/F end, the AD592C temperature transducer is interfaced with the AD654 in such a manner that the AD654 output frequency is proportional to temperature. The output frequency can be scaled and offset from K to °C or °F using the resistor values shown in Table II. Since temperature is the parameter of interest, an NPO ceramic capacitor is used as the timing capacitor for low V/F TC.

When scaling per K, resistors R1 – R3 and the AD589 voltage reference are not used. The AD592 produces a 1μA/K current output which drives pin 3 of the AD654. With the timing capacitor of 0.01μF this produces an output frequency scaled to 10Hz/K. When scaling per °C and °F, the AD589 and resistors R1 – R3 offset the drive current at pin 3 by 273.2μA for scaling per °C and 255.42μA for scaling per °F. This will result in frequencies scaled at 10Hz/°C and 5.55Hz/°F, respectively.

OPTOISOLATOR COUPLING

A popular method of isolated signal coupling is via optoelectronic isolators, or optocouplers. In this type of device, the signal is coupled from an input LED to an output photo-transistor, with light as the connecting medium. This technique allows DC to be transmitted, is extremely useful in overcoming ground loop problems between equipment, and is applicable over a wide range of speeds and power.

Figure 9 shows a general purpose isolated V/F circuit using a low cost 4N37 optoisolator. A +5V power supply is assumed for both the isolated (+5V isolated) and local (+5V local) supplies. The input LED of the isolator is driven from the collector output of the AD654, with a 9mA current level established by R1 for high speed, as well as for a 100% current transfer ratio.

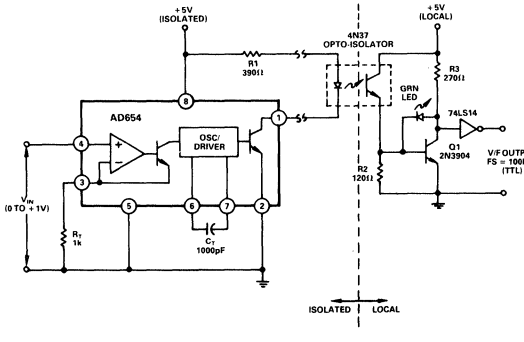


Figure 9. Optoisolator Interface

At the receiver side, the output transistor is operated in the photo-transistor mode; that is with the base lead (pin 6) open. This allows the highest possible output current. For reasonable speed in this mode, it is imperative that the load impedance be as low as possible. This is provided by the single transistor stage current-to-voltage converter, which has a dynamic load impedance of less than 10 ohms and interfaces with TTL at the output.

USING A STAND-ALONE FREQUENCY COUNTER/LED DISPLAY DRIVER FOR VOLTMETER APPLICATIONS

Figure 10 shows the AD654 used with a stand-alone frequency counter/LED display driver. With C_T = 1000pF and R_T = 1kΩ the AD654 produces an FS frequency of 100kHz when V_{IN} = +1V. This signal is fed into the ICM7226A, a universal counter system that drives common anode LED's. With the FUNCTION pin tied to D1 through a 10kΩ resistor the ICM7226A counts the frequency of the signal at A_{IN}. This count period is selected by the user and can be 10ms, 100ms, 1s, or 10 seconds, as shown on pin 21. The longer the period selected, the more resolution the count will have. The ICM7226A then displays the frequency on the LED's, driving them directly as shown. Refreshing of the LED's is handled automatically by the ICM7226. The entire circuit operates on a single +5V supply and gives a meter with 3, 4, or 5 digit resolution.

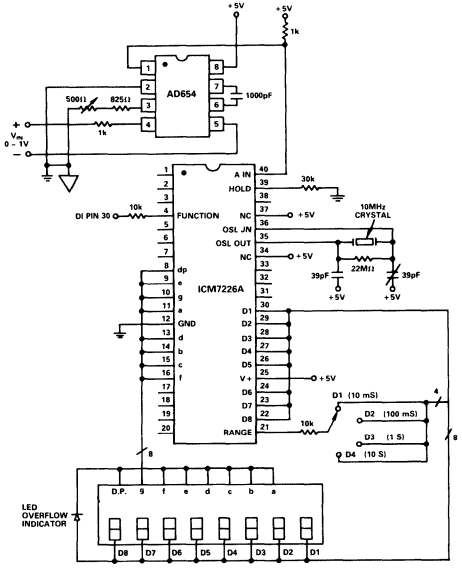


Figure 10. AD654 With Stand-Alone Frequency Counter/LED Display Driver

Longer count periods not only result in the count having more resolution, they also serve as an integration of noisy analog signals. For example, a normal-mode 60Hz sine wave riding on the input of the AD654 will result in the output frequency increasing on the positive half of the sine wave and decreasing on the negative half of the sine wave. This effect is cancelled by selecting a count period equal to an integral number of noise signal periods. A 100ms count period is effective because it not only has an integral number of 60Hz cycles (6), it also has an integral number of 50Hz cycles (5). This is also true of the 1 second and 10 second count period.

AD654-BASED ANALOG-TO-DIGITAL CONVERSION USING A SINGLE CHIP MICROCOMPUTER

The AD654 can serve as an analog-to-digital converter when used with a single component microcomputer that has an interval timer/event counter such as the 8048. Figure 11 shows the AD654, with a full scale input voltage of +1V and a full scale output frequency of 100kHz, connected to the timer/counter input pin T1 of the 8048. Such a system can also operate on a single +5V supply.

The 8748 counter is negative edge triggered; after the STRT CNT instruction is executed subsequent high to low transitions on T1 increment the counter. The maximum rate at which the counter may be incremented is once per three instruction cycles; using a 6MHz crystal, this corresponds to once every 7.5μs, or a maximum frequency of 133kHz. Because the counter overflows every 256 counts (8 bits), the timer interrupt is enabled. Each overflow then causes a jump to a subroutine where a register is incremented. After the STOP TCNT instruction is executed, the number of overflows that have occurred will be the number in this register. The number in this register multiplied by 256 plus the number in the counter will be the total number of negative edges counted during the count period. The count period is handled simply by decrementing a register the number of times necessary to correspond to the desired count time. After the register has been decremented the required number of times, the STOP TCNT instruction is executed.

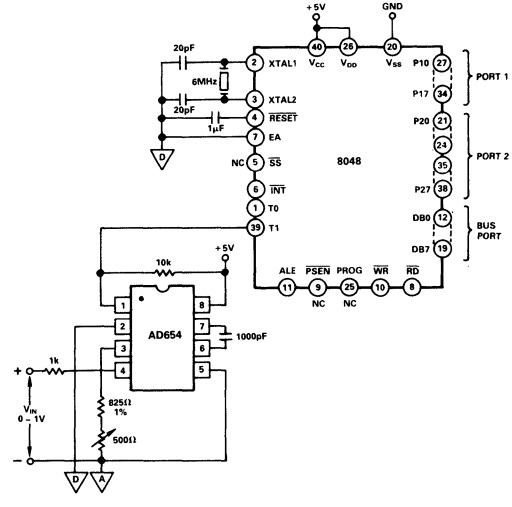


Figure 11. AD654 VFC as an ADC

The total number of negative edges counted during the count period is proportional to the input voltage. For example, if a 1V full-scale input voltage produces a 100kHz signal and the count period is 100ms, then the total count will be 10,000. Scaling from this maximum is then used to determine the input voltage, i.e., a count of 5000 corresponds to an input voltage of 0.5V. As with the ICM7226, longer count times result in counts having more resolution; and they result in the integration of noisy analog signals.

FREQUENCY DOUBLING

Since the AD654's output is a square-wave rather than a pulse train, information about the input signal is carried on both halves of the output waveform. The circuit in Figure 12 converts the output into a pulse train, effectively doubling the output frequency, while preserving the better low frequency linearity of the AD654. This circuit also accommodates an input voltage that is greater than the AD654 supply voltage.

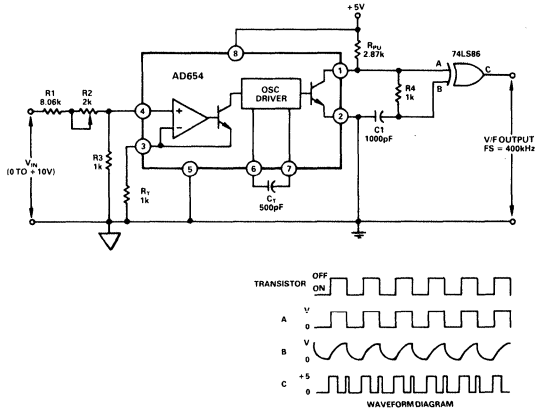


Figure 12. Frequency Doubler

Resistors R1 – R3 are used to scale the 0 to +10V input voltage down to 0 to +1V as seen at pin 4 of the AD654. Recall that V_{IN} must be less than V_{SUPPLY} −4V, or in this case less than 1V. The timing resistor and capacitor are selected such that this 0.to +1V signal seen at pin 4 results in a 0 to 200kHz output frequency.

The use of R4, C1 and the XOR gate doubles this 200kHz output frequency to 400kHz. The AD654 output transistor is basically used as a switch, switching capacitor C1 between a charging mode and a discharging mode of operation. The voltages seen at the input of the 74LS86 are shown in the waveform diagram. Due to the difference in the charge and discharge time constants, the output pulse widths of the 74LS86 are not equal. The output pulse is wider when the capacitor is charging due to its longer rise time than fall time. The pulses should therefore be counted on their rising, rather than falling, edges.

OPERATION AT HIGHER OUTPUT FREQUENCIES

Operation of the AD654 via the conventional output (pins 1 and 2) is speed limited to approximately 500kHz for reasons of TTL logic compatibility. Although the output stage may become speed limited, the multivibrator core itself is able to oscillate to 1MHz or more. The designer may take advantage of this feature in order to operate the device at frequencies in excess of 500kHz.

Figure 13 illustrates this with a circuit offering 2MHz full scale. In this circuit the AD654 is operated at a full scale (FS) of 1mA, with a C_T of 100pF. This achieves a basic device FS frequency of 1MHz across C_T. The P channel JFETs, Q1 and Q2, buffer the differential timing capacitor waveforms to a low impedance level where the push-pull signal is then AC coupled to the high speed comparator A2. Hysteresis is used, via R7, for non-ambiguous switching and to eliminate the oscillations which would otherwise occur at low frequencies.

The net result of this is a very high-speed circuit which does not compromise the AD654 dynamic range. This is a result of the FET buffers typically having only a few pA of bias current. The high end dynamic range is limited, however, by parasitic package and layout capacitances in shunt with C_T, as well as those from each node to AC ground. Minimizing the lead length between A2–6/A2–7 and Q1/Q2 in PC layout will help. A ground plane will also help stability. Figure 14 shows the waveforms V1 – V4 found at the respective points shown in Figure 13.

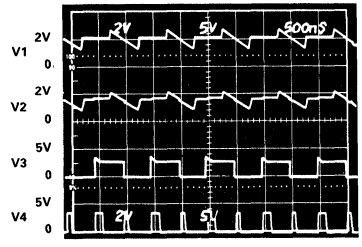


Figure 14. Waveforms of 2MHz Frequency Doubler

The output of the comparator is a complementary square wave at 1MHz FS. Unlike pulse train output V/F converters, each half-cycle of the AD654 output conveys information about the input. Thus it is possible to count edges, rather than full cycles of the output, and double the effective output frequency. The XOR gate following A2 acts as an edge detector producing a short pulse for each input state transition. This effectively doubles the V/F FS frequency to 2MHz. The final result is a 1V full scale input V/F with a 2MHz full-scale output capability; typical nonlinearity is 0.5%.

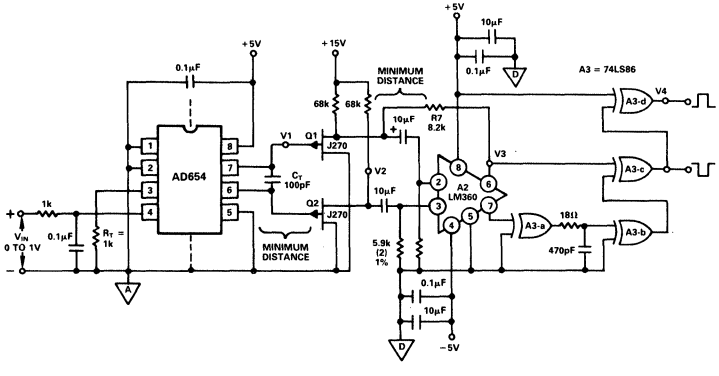


Figure 13. 2MHz, Frequency Doubling V/F

ANALOG DEVICES

Voltage-to-Frequency and Frequency-to-Voltage Converter

ADVFC32

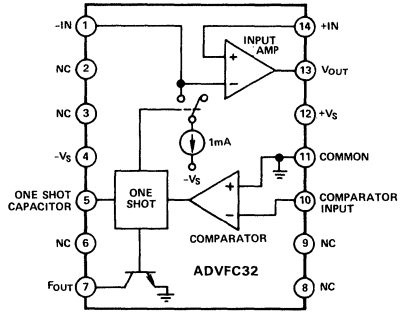
FEATURES

High Linearity
- **±0.01% max at 10kHz FS**
- **±0.05% max at 100kHz FS**
- **±0.2% max at 500kHz FS**

Output TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction

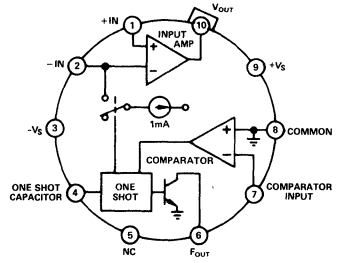
ADVFC32 PIN CONFIGURATION

"N" PACKAGE



TOP VIEW

"H" PACKAGE – TO-100



TOP VIEW

PRODUCT DESCRIPTION

The industry standard ADVFC32 is a low cost monolithic voltage-to-frequency (V/F) converter or frequency-to-voltage (F/V) converter with good linearity (0.01% max error at 10kHz) and operating frequency up to 0.5MHz. In the V/F configuration, positive or negative input voltages or currents can be converted to a proportional frequency using only a few external components. For F/V conversion, the same components are used with a simple biasing network to accommodate a wide range of input logic levels.

TTL or CMOS compatibility is achieved in the V/F operating mode using an open collector frequency output. The pullup resistor can be connected to voltages up to 30 volts, or to +15V or +5V for conventional CMOS or TTL logic levels. This resistor should be chosen to limit current through the open collector output to 8mA. A larger resistance can be used if driving a high impedance load.

Input offset drift is only 3ppm of full scale per °C, and full scale calibration drift is held to a maximum of 100ppm/°C (ADVFC32BH) due to a low T.C. zener diode.

The ADVFC32 is available in commercial, industrial, and extended temperature grades. The commercial grade is packaged in a 14-pin plastic DIP while the two wider temperature range parts are packaged in hermetically sealed TO-100 cans.

ORDERING GUIDE

Part Number	Gain Tempco ppm/°C	Temp Range °C	Package
ADVFC32KN	±75 typ	0 to +70	14-Pin Plastic DIP
ADVFC32BH	±100 max	−25 to +85	TO-100
ADVFC32SH	±150 max	−55 to +125	TO-100

PRODUCT HIGHLIGHTS

1. The ADVFC32 uses a charge balancing circuit technique (see Functional Block Diagram) which is well suited to high accuracy voltage-to-frequency conversion. The full-scale operating frequency is determined by only one precision resistor and capacitor. The tolerance of other support components (including the integration capacitor) is not critical. Inexpensive ±20% resistors and capacitors can be used without affecting linearity or temperature drift.
2. The ADVFC32 is easily configured to satisfy a wide range of system requirements. Input voltage scaling is set by selecting the input resistor which sets the input current to 0.25mA at the maximum input voltage.
3. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the ADVFC32.
4. The ADVFC32 is intended as a pin-for-pin replacement for VFC32 devices from other manufacturers.

SPECIFICATIONS (typical @ +25°C with $V_S = \pm 15V$ unless otherwise noted)

Model	ADVFC32K Min	ADVFC32K Typ	ADVFC32K Max	ADVFC32B Min	ADVFC32B Typ	ADVFC32B Max	ADVFC32S Min	ADVFC32S Typ	ADVFC32S Max	Units
DYNAMIC PERFORMANCE										
Full Scale Frequency Range	0		500	0		500	0		500	kHz
Nonlinearity[1]										
f_{max} = 10kHz	−0.01		±0.01	−0.01		+0.01	−0.01		+0.01	%
f_{max} = 100kHz	**−0.05**		**+0.05**	**−0.05**		**+0.05**	**−0.05**		**+0.05**	%
f_{max} = 0.5MHz	−0.20	±0.05	+0.20	−0.20	±0.05	+0.20	−0.20	±0.05	+0.20	%
Full Scale Calibration Error										
(Adjustable to Zero)		±5			±5			±5		%
vs. Supply										
(Full Scale Frequency = 100kHz)	**−0.015**		**+0.015**	**−0.015**		**+0.015**	**−0.015**		**+0.015**	% of FSR/%
vs. Temperature										
(Full Scale Frequency = 10kHz)		±75		−100		+100	**+150**		**+150**	ppm/°C
DYNAMIC RESPONSE										
Maximum Settling Time for Full Scale										
Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
Overload Recovery Time	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
ANALOG INPUT AMPLIFIER										
(V/F Conversion)										
Current Input Range	0		+0.25	0		+0.25	0		+0.25	mA
Voltage Input Range	0		−10, 0.25 × R_{IN}[3]	0		−10, 0.25 × R_{IN}[3]	0		−10, 0.25 × R_{IN}[3]	V[2] mA
Differential Impedance	300kΩ‖10pF	2MΩ‖10pF		300kΩ‖10pF	2MΩ‖10pF		300kΩ‖10pF	2MΩ‖10pF		
Common-Mode Impedance	300MΩ‖3pF	750MΩ‖3pF		300MΩ‖3pF	750MΩ‖10pF		300MΩ‖3pF	750MΩ‖10pF		
Input Bias Current										
Noninverting Input		40	**250**		40	**250**		40	**250**	nA
Inverting Input	**−100**	±8	**+100**	**−100**	±8	**+100**	**−100**	±8	**+100**	nA
Input Offset Voltage										
(Trimmable to Zero)[2,3]			**4**			**4**			**4**	mV
vs. Temperature (T_{min} to T_{max})			30			30			**30**	µV/°C
Safe Input Voltage		±V_S			±V_S			±V_S		
COMPARATOR (F/V Conversion)										
Logic "0" Level	−V_S		−0.6	−V_S		−0.6	−V_S		−0.6	V
Logic "1" Level	+1		+V_S	+1		+V_S	+1		+V_S	V
Pulse Width Range[4]	0.1		0.15/f_{max}	0.1		0.15/f_{max}	0.1		0.15/f_{max}	µs
Input Impedance	50kΩ‖10pF	250kΩ		50kΩ‖10pF	250kΩ		50kΩ‖10pF	250kΩ		
OPEN COLLECTOR OUTPUT										
(V/F Conversion)										
Output Voltage in Logic "0"										
I_{SINK} = 8mA			**0.4**			**0.4**			**0.4**	V
Output Leakage Current in Logic "1"			**1**			**1**			**1**	µA
Voltage Range	0		+30	0		+30	0		+30	V
Fall Times (Load = 500pF and I_{SINK} = 5mA)			400			400			400	ns
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (0mA≤I_O≤7mA)	0		+10	0		+10	0		+10	V
Source Current (0≤V_O≤7V)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
Closed Loop Output Impedance			1			1			1	Ω
POWER SUPPLY										
Rated Voltage		±15			±15			±15		V
Voltage Range	±9		±18	±9		±18	±9		±18	V
Quiescent Current		6	**8**		6	**8**		6	**8**	mA
TEMPERATURE RANGE										
Specified Range	0		+70	−25		+85	−55		+125	°C
Operating Range	−25		+85	−55		+125	−55		+125	°C
Storage	−25		+85	−65		+150	−65		+150	°C
PACKAGE OPTIONS[5]										
Plastic DIP (N-14)		ADVFC32KN								
TO-100 (H-10A)					ADVFC32BH			ADVFC32SH		

NOTES
[1]Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.
[2]See Figure 3.
[3]See Figure 1.
[4]f_{max} expressed in units of MHz.
[5]See Section 14 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

UNIPOLAR V/F, POSITIVE INPUT VOLTAGE

When operated as a V/F converter, the transformation from voltage to frequency is based on a comparison of input signal magnitude to the 1mA internal current source.

A more complete understanding of the ADVFC32 requires a close examination of the internal circuitry of this part. Consider the operation of the ADVFC32 when connected as shown in Figure 1. At the start of a cycle, a current proportional to the

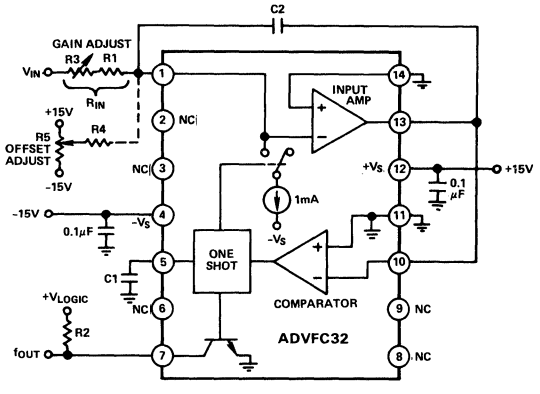


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

input voltage flows through R3 and R1 to charge integration capacitor C2. As charge builds up on C2, the output voltage of the input amplifier decreases. When the amplifier output voltage (pin 13) crosses ground (see Figure 2 at time t_1), the comparator triggers a one shot whose time period is determined by capacitor C1. Specifically, the one shot time period (in nanoseconds) is:

$$t_{OS} \cong (C_1 + 44pF) \times 6.7k\Omega$$

During this period, a current of (1mA $-I_{IN}$) flows out of the integration capacitor. The total amount of charge depleted during one cycle is, therefore (1mA $- I_{IN}$) $\times$ t_{OS}. This charge is replaced during the remainder of the cycle to return the integrator to its original voltage. Since the charge taken out of C2 is equal to the charge that is put on C2 every cycle,

$$(1mA - I_{IN}) \times t_{OS} = I_{IN} \times \left(\frac{1}{F_{OUT}} - t_{OS} \right)$$

or, rearranging terms,

$$F_{OUT} = \frac{I_{IN}}{1mA \times t_{OS}}$$

The complete transfer equation can now be derived by substituting $I_{IN} = V_{IN}/R_{IN}$ and the equation relating C1 and t_{OS}. The final equation describing ADVFC32 operation is:

$$F_{OUT} = \frac{V_{IN}/R_{IN}}{1mA \times (C_1 + 44pF) \times 6.7k\Omega}$$

Components should be selected to optimize performance over the desired input voltage and output frequency range using the equations listed below:

$$C_1 = \frac{3.7 \times 10^7 pF/sec}{F_{OUT\ FS}} - 44pF$$

$$C_2 = \frac{10^{-4}\ Farads/sec}{F_{OUT\ FS}} \text{ (1000pF minimum)}$$

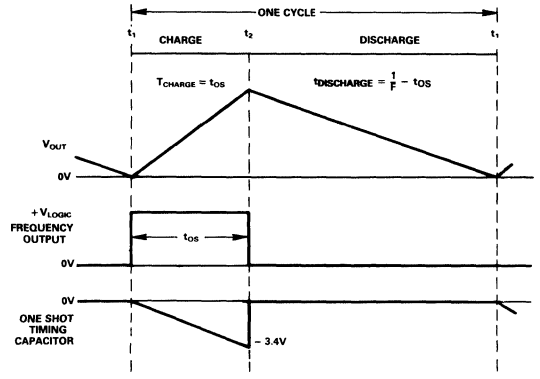


Figure 2. Voltage-to-Frequency Conversion Waveforms

$$R_{IN} = \frac{V_{IN\ FS}}{0.25mA}$$

$$R_2 \geq \frac{+V_{LOGIC}}{8mA}$$

Both R_{IN} and C_1 should have very low temperature coefficients as changes in their values will result in a proportionate change in the V/F transfer function. Other component values and temperature coefficients are not critical.

$V_{IN\ FS}$	$F_{OUT\ FS}$	C_1	R_{IN}	C_2
1V	10kHz	3650pF	4.0kΩ	0.01μF
10V	10kHz	3650pF	40kΩ	0.01μF
1V	100kHz	330pF	4.0kΩ	1000pF
10V	100kHz	330pF	40kΩ	1000pF

Table I. Suggested Values for C_1, R_{IN} and C_2

Input resistance R_{IN} is composed of a fixed resistor (R1) and a variable resistor (R3) to allow for initial gain error compensation. To cover all possible situations, R3 should be 20% of R_{IN}, and R1 should be 90% of R_{IN}. This allows a ±10% gain adjustment to compensate for the ADVFC32 full-scale error and the tolerance of C1.

If more accurate initial offset is required, the circuit of R4 and R5 can be added. R5 can have a value between 10kΩ and 100kΩ, and R4 should be approximately 10MΩ. The amount of current required to trim zero offset will be relatively small, so the temperature coefficients of these resistors are not critical. If large offsets are added using this circuit, temperature drift of both of these resistors is much more important.

BIPOLAR V/F

By adding another resistor from pin 1 (pin 2 of TO-100 can) to a stable positive voltage, the ADVFC32 can be operated with a bipolar input voltage. For example, an 80kΩ resistor to +10V causes an additional current of 0.125mA to flow into the integrator so that the net current flow to the integrator is positive even for negative input voltages. At negative full scale input voltage, 0.125mA will flow into the integrator from V_{IN} cancelling out the 0.125mA from the offset resistor, resulting in an output frequency of zero. At positive full scale, the sum of the two currents will be 0.25mA and the output will be at its maximum frequency.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 3 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full scale output frequency occurs at negative full scale input, and zero output frequency corresponds to zero input voltage.

A very high impedance signal source may be used since it only drive the noninverting integrator input. Typical input impedance at this terminal is 250MΩ or higher. For V/F conversion of positive input signals the signal generator must be able to source 0.25mA to properly drive the ADVFC32, but for negative V/F conversion the 0.25mA integration current is drawn from ground through R1 and R3.

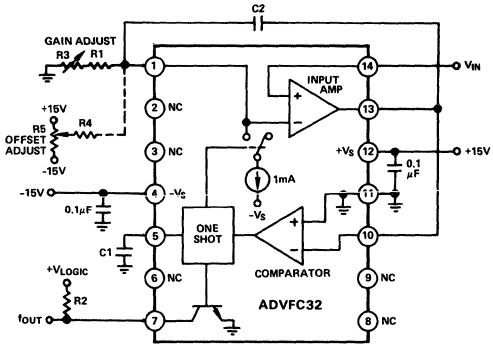


Figure 3. Connection Diagram for V/F Conversion, Negative Input Voltage

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in the previous section. For best operating results use component equations listed in that section.

F/V CONVERSION

Although the mathematics of F/V conversion can be very complex, the basic principle is easy to understand. Figure 4 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshold going negative, the one shot is activated and switches 1mA into the integrator input for a measured time period (determined by C1). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F conversion section.

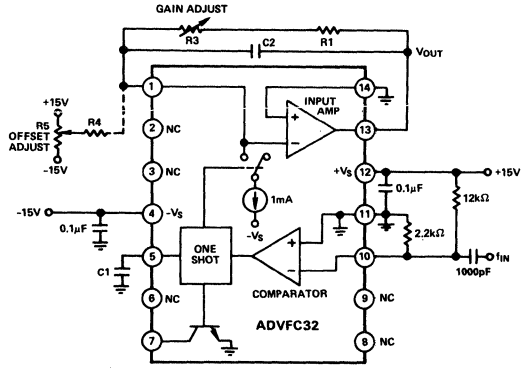


Figure 4. Connection Diagram for F/V Conversion, TTL Input

DECOUPLING

Decoupling power supplies at the device is good practice in any system, but absolutely imperative in high resolution applications. For the ADVFC32, it is important to remember where the voltage transients and ground currents flow. For example, the current drawn through the output pulldown transistor originates from the logic supply, and is directed to ground through pin 11 (pin 8 of TO-100). Therefore, the logic supply should be decoupled near the ADVFC32 to provide a low impedance return path for switching transients. Also, if there is a separate digital ground it should be connected to the analog ground at the ADVFC32. This will prevent ground offsets that could be created by directing the full 8mA output current into the analog ground, and subsequently back to the logic supply.

Although some circuits may operate satisfactorily with the power supplies decoupled at only one location on each board, this practice is not recommended for the ADVFC32. For best results, each supply should be decoupled with 0.1μF capacitor at the ADVFC32. In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the ADVFC32 on each power supply.

COMPONENT TEMPERATURE COEFFICIENTS

The drift specifications of the ADVFC32 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C_1 directly affect the overall temperature stability. In the application of Figure 2, a 10ppm/°C input resistor used with a 100ppm/°C capacitor may result in a maximum overall circuit gain drift of:

100ppm/°C (ADVFC32BH) + 100ppm/°C (C1)
+ 10ppm/°C (R_{IN}) = 210ppm/°C

Although R_{IN} and C_1 have the most pronounced effect on temperature stability, the offset circuit of resistors R4 and R5 may also have a slight effect on the offset temperature drift of the circuit. The offset will change with variations in the resistance of R4 and supply voltage changes. In most applications the offset adjustment is very small, and the offset drift attributable to this circuit will be negligible. In the bipolar mode, however, both the positive reference and the resistor used to offset the signal range will have a pronounced effect on offset drift. A high quality reference and resistor should be used to minimize offset drift errors.

Other circuit components do not directly influence temperature performance as long as their actual values are not so different from nominal value as to preclude operation. This includes integration capacitor C2. A change in the capacitance value of C2 results in a different rate of voltage change across C2, but this is compensated by an equal effect when C2 is discharged by the switched 1mA current source so that no net effect occurs.

The temperature effects of the components described above are the same when the ADVFC32 is configured for negative or bipolar input ranges, or F/V conversion.

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to pins 1, 13, and 14 is not a standard operational amplifier. Although it operates like an op amp in most applications, two key differences should be noted. First, the bias current of the positive input is typically 40nA while the bias current of the inverting input is ±8nA. Therefore, any attempt to cancel input offset voltage due to bias currents by matching input resistors will create worse offsets. Second, the output of this amplifier will sink only 1mA, even though it will source as much as 10mA. When used in the F/V mode, the amplifier must be buffered if large sink currents are required.

MICROPROCESSOR OPERATED A/D CONVERTER

With the addition of a few external components the ADVFC32 can be used as a ±10V A/D microprocessor front end. Although the nonlinearity of the ADVFC32 is only 0.05% maximum (0.01% typ), the resolution is much higher, allowing it to be used in 16-bit measurement and control systems where a monotonic transfer function is essential. The resolution of the circuit shown in Figure 5 is dependent on the amount of time allowed to count the ADVFC32 frequency output. Using a full scale frequency of 100kHz, an 8-bit conversion can be made in about 10ms, and a 2 second time period allows a 16-bit measurement, including offset and gain calibration cycles.

As shown in Figure 5, the input signal is selected via the AD7590 input multiplexer. Positive and negative references as well as a

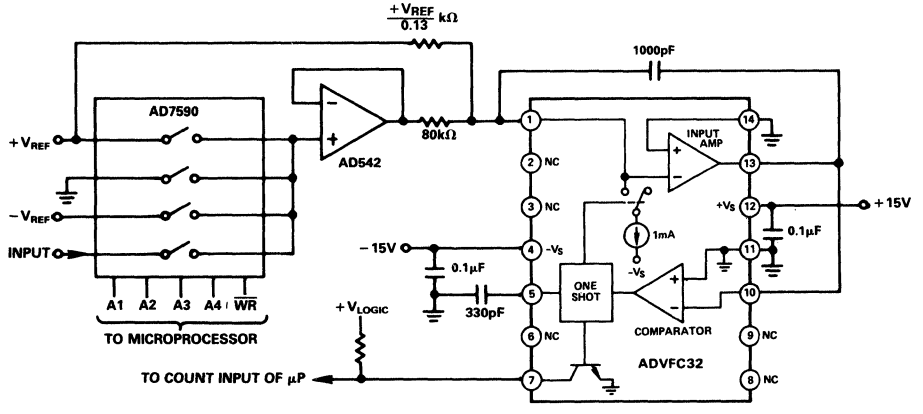


Figure 5. High Resolution, Self-Calibrating, Microprocessor Operated A/D Converter

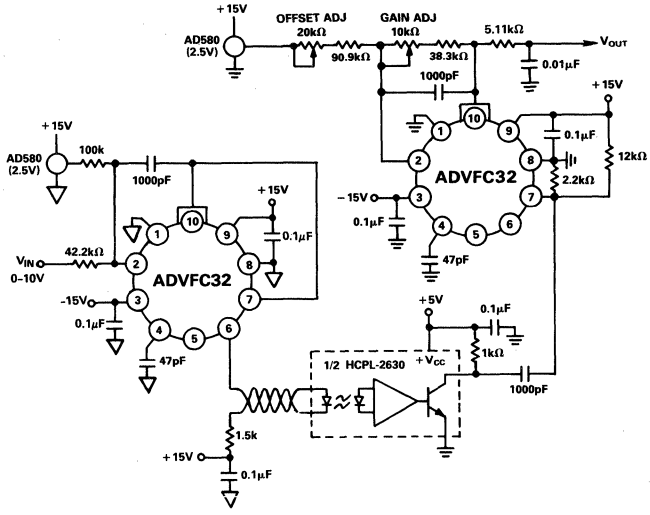


Figure 6. High Noise Immunity Data Link

ground input are provided to calibrate the A/D. This is very important in systems subject to moderate or extreme temperature changes since the gain temperature coefficient of the ADVFC32 is as high as ±150ppm/°C. By using the calibration cycles, the A/D conversion will be as accurate as the references provided. The AD542 following the input multiplexer provides a high impedance input (10^{12} ohms) and buffers the switch resistance from the relatively low impedance ADVFC32 input.

If higher linearity is required, the ADVFC32 can be operated at 10kHz, but this will require a proportionately longer conversion time. Conversely, the conversion time can be decreased at the expense of nonlinearity by increasing the maximum frequency to as high as 500kHz.

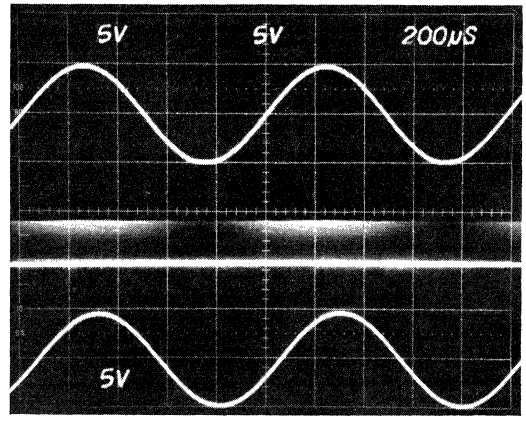
HIGH NOISE IMMUNITY, HIGH CMRR ANALOG DATA LINK

In many applications, a signal must be sensed at a remote site and sent through a very noisy environment to a central location for further processing. In these cases, even a shielded cable may not protect the signal from noise pickup. The circuit of Figure 6 provides a solution in these cases. Due to the optocoupler and voltage-to-frequency conversion, this data link is extremely insensitive to noise and common mode voltage interference. For even more protection, an optical fiber link substituted for the HCPL2630 will provide common mode rejection of more than several hundred kilovolts and virtually total immunity to electrical noise. For most applications, however, the frequency modulated signal has sufficient noise immunity without using an optical fiber link, and the optocoupler provides common mode isolation up to 3000V dc.

The data link input voltage is changed in a frequency modulated signal by the first ADVFC32. A 42.2kΩ input resistor and a 100kΩ offset resistor set the scaling so that a 0V input signal corresponds to 50kHz, and a 10V input results in the maximum output frequency of 500kHz. A high frequency optocoupler is then used to transmit the signal across any common mode voltage potentials to the receiving ADVFC32. The optocoupler is not necessary in systems where common mode noise is either very small or a constant low level dc voltage. In systems where common mode voltage may present a problem, the connection between the two locations should be through the optocoupler; no power or ground connections need to be made.

The output of the optocoupler drives an ADVFC32 hooked up in the F/V configuration. Since the reconstructed signal at pin 10 has a considerable amount of carrier feedthrough, it is desirable to filter out any frequencies in the carrier range of 50kHz to 500kHz. The frequency response of the F/V converter is only 3kHz due to the pole made by the integrator, so a second 3kHz filter will not significantly limit the bandwidth. With the simple one pole filter shown in Figure 6, the input to output 3dB point is approximately 2kHz, and the output noise is less than 15mV. If a lower output impedance drive is needed, a two pole active filter is recommended as an output stage.

Although the F/V conversion technique used in this circuit is quite simple, it is also very limited in terms of its frequency response and output ripple. The frequency response is limited by the integrator time constant and while it is possible to decrease that time constant, either signal range or output ripple must be sacrificed. The performance of the circuit of Figure 6 is shown in the photograph below. The top trace is the input signal, the middle trace is the frequency-modulated signal at the optocoupler's output, and the bottom trace is the recovered signal at the output of the F/V converter.



Synchro & Resolver Converters
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Selection Guide
Synchro & Resolver Converters

SYNCHRO, RESOLVER, INDUCTOSYN† AND LVDT-TO-DIGITAL CONVERTERS

Model	Res Bits	Input Format[1]	Accuracy arc mins	Tracking Rate Options revs/sec[2]	Reference Frequency Options Hz	Input Isol	Package Options[3]	Temp Range[4]	Page	Comments
1S14	10	I, R	±25	680	2k→10k	No	D, M	C, M	5-27	Error, Ripple Carry, Direction and High Quality Tachometer Output
SDC/RDC1741	**12**	**S, R**	**±15.3**	**18**	**400, 2.6 k**	**Yes**	**M**	**C, M**	**5-19**	**Tristate, Latched Output Internal Transformer Isolation**
SDC/RDC1742	**12**	**S, R**	**±8.5**	**18**	**400, 2.6 k**	**Yes**	**M**	**C, M**	**5-19**	**Tristate, Latched Output Internal Transformer Isolation**
1S20	12	I, R	±8.5	50, 90, 170	400→2.6 k, 2.6 k→5 k, 5 k→10 k	No	D, M	C, M	5-35	High Tracking Rate with Velocity, Error, Ripple Carry and Direction Outputs, Latched, Tristate Output. Low Cost
1S24	12	I, R	±8.5	170	2k→10k	No	D, M	C, M	5-27	Error, Ripple Carry, Direction and High Quality Tachometer Output
2S81	**12**	**I, R**	**±30[5]**	**260**	**400→20 k**	**No**	**D**	**C**	**5-77**	**Monolithic, User Selectable Dynamic Characteristics High Tracking Rate, Quality Velocity Output**
SDC/RDC1740	**14**	**S, R**	**±5.3**	**12**	**400, 2.6 k**	**Yes**	**M**	**C, M**	**5-19**	**Tristate, Latched Output Internal Transformer Isolation**
1S40	14	I, R	±5.3	12.5, 22.5, 42.5	400→2.6 k, 2.6 k→5 k, 5 k→10 k	No	D, M	C, M	5-35	High Tracking Rate with Velocity, Ripple Carry and Direction Outputs, Latched, Tristate Output. Low Cost
1S44	14	I, R	±5.3	42.5	2k→10k	No	D, M	C, M	5-27	Error, Ripple Carry, Direction and High Quality Tachometer Output
2S54	14	LVDT	±0.006[6]	360 LSB/ms[7]	360→5 k	No	M	C, M	5-53	Direct Ratiometric Conversion of LVDT Signal, Selectable Input Gain. No External Trims
1S60	16	I, R	±4.0, ±2.6[5]	3, 5.5, 10.5	400→2.6 k, 2.6 k→5 k, 5 k→10 k	No	D, M	C, M	5-35	High Tracking Rate with Velocity, Error, Ripple Carry and Direction Outputs. Latched Tristate Output. Low Cost

SYNCHRO, RESOLVER, INDUCTOSYN† AND LVDT-TO-DIGITAL CONVERTERS

Model	Res Bits	Input Format[1]	Accuracy arc mins	Tracking Rate Options revs/sec[2]	Reference Frequency Options Hz	Input Isol	Package Options[3]	Temp Range[4]	Page	Comments
1S61	16	I, R	±10, ±4.0[5]	3, 5.5, 10.5	400→2.6 k, 2.6 k→5 k, 5 k→10 k	No	D, M	C, M	5–35	Lower Accuracy Version of 1S60. Low Cost
1S64	16	I, R	±4.0, ±2.6[5]	10.5	2k→10k	No	D, M	C, M	5–27	Error, Ripple Carry, Direction and High Quality Tachometer Output
2S56	16	LVDT	±0.006[5]	360 LSB/ms[7]	360→5 k	No	M	M	5–53	Direct Ratiometric Conversion of LVDT Signal, Selectable Input Gain. No External Trims
1S74	10, 12, 14, 16	I, R	±4.0, ±2.6[5]	680[9]	2k→10k	No	D, M	C, M	5–43	High Quality Tachometer Output, Variable Resolution
***2S58**	**16**	**LVDT**	**±0.003[6]**	**680 LSB/ms[7]**	**7k→11k**	**No**	**M**	**C, M**	**5–53**	**Direct Ratiometric Conversion of LVDT Signal, High Gain, Ultra-Linear**
2S80	**16, 14, 12, 10[8]**	**I, R**	**±2, ±4, ±8**	**1040[9]**	**50–20 k**	**No**	**D**	**C, M**	**5–65**	**Monolithic, User Selectable Dynamic Characteristics, and Resolution High Tracking Rate and Quality Velocity Output**
2S82	**16, 14, 12, 10[8]**	I, R	**±2, ±4, ±8**	**1040[9]**	**50–20 k**	**No**	P	**C**	**5–89**	
2S50	11	LVDT	±0.025[6]	200 LSB/ms[7]	400, 1 k→10 k	No	D, M	C, M	5–51	Direct Conversion of LVDT Signal, No External Trims Required, Tristate Output

[1]S = Synchro; R = Resolver; I = Inductosyn.
[2]Revs/sec equivalent to pitches/sec in the case of an Inductosyn; in general higher reference frequency options have higher tracking rates.
[3]Package Options: D–Side-Brazed Dual-In-Line Ceramic; M–Metal Hermetic Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC).
[4]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
[5]Consult data sheet.
[6]LVDT converter accuracy given as % full scale linearity.
[7]Slew Rate (min).
[8]Resolution is user selectable.
[9]Depends on resolution selected.
Boldface type: product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
†Inductosyn is a registered trademark of Farrand Industries, Inc.

Selection Guide
Synchro & Resolver Converters

DIGITAL-TO-SYNCHRO AND RESOLVER CONVERTER

Model	Res Bits	Output Format[1]	Accuracy arc mins	Load Driving Capability	Reference Frequency Options Hz	Reference Input Volt Options V rms	Signal Output Volt Options V rms	Transformer Output Isolations	Package Options[2]	Temp Range[3]	Page	Comments
DR1745	**14**	**R[4]**	**±2, ±4[5]**	**2.0VA[6]**	**dc→2600**	**0→3.4**	**0→6.8**	**Use Ext. STM1680 and STM1683 Transformer**	**M**	**M**	**5–7**	**Digital-to-Resolver Converter with Int. 2VA Power Amplifier. Optional Int. TransZorb‡ Protection. 2 Byte Latched Inputs.**
DR1746	**16**	**R[4]**	**±2, ±4[5]**	**2.0VA[6]**	**dc→2600**	**0→3.4**	**0→6.8**	**Use Ext. STM1680 and STM1683 Transformer**	**M**	**M**	**5–7**	**16-Bit Version of DRC1745**

INPUT TRANSFORMERS

Model	Description	Frequency Hz	Accuracy arc mins	Input Voltage Options V rms[7]	Package Options	Package Size Inches (mm)	Page
5S72	Ref Isolation for 1S14/24/44/64/74 and 1S20/40/60/61	360 to 3000	N/A	11.8, 26, 115	Module	1.12 × 1.12 × 0.4 (28.5 × 28.5 × 10.2)	5–101
5S70	Signal Input for 1S14/24/44/64/74 and 1S20/40/60/61	360 to 3000	±0.33 (typ) ±1.5 (max)	11.8, 26, 90	Module	2.25 × 1.12 × 0.4 (57.0 × 28.5 × 10.2)	5–101

DIGITAL DIRECTOR

Model	Description	Frequency Hz	Output Drive VA	Accuracy Degrees	Output Voltage V rms	Package Size Inches (mm)	Page
6S04	Universal Synchro Simulator and Test Instrument	60 to 400	5 (60 Hz) 15 (400 Hz)	±0.1 (60 Hz) ±0.15 (400 Hz)	90 V Synchro (Coarse/Fine) 4.25 V Slab (Coarse) 11.8 V Slab (Fine)	18.3 × 17 × 7 (466 × 432 × 178)	5–103

[1]R = Resolver.
[2]Package Options: M–Metal Hermetic Dual-In-Line.
[3]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
[4]Synchro format output with external output transformer STM1683.
[5]Depends on option.
[6]Can be used with pulsating power supply for reduced dissipation.
[7]Synchro and resolver format available on all models.
Boldface type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.
‡TransZorb is a trademark of General Semiconductor Industries, Inc.

These products constitute a complete line of devices for the digital measurement and control of angular and linear displacements by means of synchros, resolvers, Inductosyns and LVDTs. All use the tracking conversion technique in which the digital output follows the synchro or resolver shaft automatically without the need for convert commands or wait loops. Apart from producing instantaneous angular data, this inherently ratiometric conversion method is also very tolerant of noise on the signal inputs as well as voltage drops between the transducer and the converter.

In addition to the integrated circuits, hybrids and modules that perform the conversions, the line also includes support components such as power oscillators, transformers and preamplifiers.

The range of synchro processing modules now available covers a wide area of applications. They are widely used in military and radar applications, but there are additional fields in which they could be used to advantage because of the proven ruggedness and high precision of the electromechanical hardware, their standardized specifications and their low cost. They have a number of advantages over potentiometers and optical systems.

In this introductory section, there will be provided a brief set of device definitions. Detailed data and applications information is given in the data sheets. For a complete introduction to synchro/digital conversion, Analog Devices has available a 208-page book, *Synchro and Resolver Conversion*, edited by G. Boyes (1980), $11.50.

In this section and in much of the text, the word "Synchro" appears frequently. In many cases, the word "Resolver" could be used in its place. The modules make use of angular data in resolver form; if the input data is in three-wire synchro form, transformers in "Scott T" configuration convert it to resolver form; analog outputs are available in both forms. There are a number of voltage and frequency options.

Linear Variable displacement Transducer (LVDT) converters such as the 2S50 series provide the LVDT phase-sensitive demodulation and digitization for these extremely rugged transducers, which precisely measure displacement over limited distances.

Digital-to-Synchro Converters (DRC1765, 1746)
Devices that accept parallel binary digital inputs (14 or 16 bits) and an ac reference signal, and provide outputs in 3-wire synchro form.

Inductosyn/Resolver-to-Digital Converter
A device that produces a digital output capable of resolving (to 12 bits) intermediate distances within a single track-pitch of a Farrand linear-Inductosyn stator in displacement- and angle-measuring Inductosyn systems. The moving element is used as though it were a resolver input; hence the device will also convert resolver information to digital.

Synchro-to-Digital Converters (2S80 Family)
Devices that accept either 3-wire synchro or 4-wire resolver inputs, together with a 2-wire ac reference, and outputs angular binary data in a continuously tracking mode employing a Type 2 servo loop. The inputs may be from either remote synchros or from electrically simulated synchros (e.g., DSCs).

Velocity Output
A velocity output is useful when the rate of change of position – the velocity – as well as the absolute position information is needed for monitoring and closed loop control. The 2S80 series of monolithic resolver-to-digital converters provides an analog velocity signal output in addition to the digital output.

Support Devices
Power Oscillators such as the OSC1758 act as the drive oscillator for Inductosyns.

Input Transformers such as the 5S70 and 5S72 isolate the reference input from the converter.

High-Gain Preamps such as the IPA1764 amplify the Inductosyn voltages to converter levels.

REPRESENTATION OF ANGLES IN DIGITAL FORM

Binary
The most commonly used method of representing angles in digital form is simple natural binary weighting, where the most significant bit (MSB) represents 180°, the next represents 90°, etc. The table shows the bit weights in degrees, degrees and minutes, and radians for this coding method.

Bit No.	Degrees	Degrees, Minutes		Radians
1	180	180	0	3.141593
2	90	90	0	1.570796
3	45	45	0	0.785398
4	22.5	22	30	0.392699
5	11.25	11	15	0.196349
6	5.625	5	37.5	0.098175
7	2.8125	2	48.75	0.049087
8	1.40625	1	24.38	0.024544
9	0.70312	0	42.19	0.012272
10	0.35156	0	21.09	0.006136
11	0.17578	0	10.55	0.003068
12	0.08789	0	5.27	0.001534
13	0.04395	0	2.64	0.000767
14	0.02197	0	1.32	0.000383
15	0.01099	0	0.66	0.000192
16	0.00549	0	0.33	0.000096

ANALOG DEVICES

High Power Output, Hybrid Digital-to-Synchro/Resolver Converters

DRC1745/DRC1746

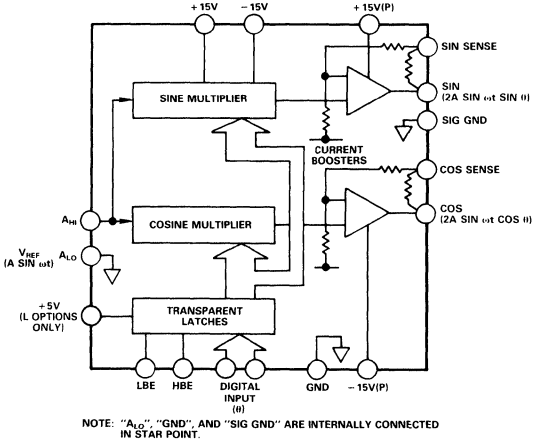
FEATURES

- 14- or 16-Bit Resolution
- 2 or 4 Arc-Minutes Accuracy
- 2VA max Mean Output Drive Capability
- Full Accuracy for dc to 2.6kHz Reference
- Full Accuracy with dc or Pulsating Power Supplies (PPS)
- Guaranteed Operation With 3V dc Pedestal on PPS
- Can Drive Pure Inductive, Resistive or Highly Capacitive Loads
- LS or CMOS Latched Inputs With Separate High/Low Byte Enable
- Low Radius Vector Variation (0.03%)
- Optional TransZorb™ Protection Against Inductive Spikes on Output
- Protected Against +200% Overvoltage on Analog Input
- Remote Output Sensing Facility
- No Trims or External Adjustments
- Full Output Short Circuit Protection
- Single 40-Pin Package
- Hi Rel, MIL-STD 883B Versions Available

APPLICATIONS

- Driving Synchro and Resolver Control Transformers
- Avionic Equipment (e.g., Air Data Computers)
- Interfacing With Servo Systems
- Fire Control System Outputs
- Naval Retransmission Unit Outputs
- Outputs to Radars and Navigational Aids
- Aircraft and Naval Simulators

DRC1745/DRC1746 FUNCTIONAL BLOCK DIAGRAM



NOTE: "A_{LO}", "GND", AND "SIG GND" ARE INTERNALLY CONNECTED IN STAR POINT.

GENERAL DESCRIPTION

The DRC1745 and DRC1746 are hybrid packaged Digital-to-Resolver converters. They accept a 14-bit or 16-bit digital input word representing angle and output sine and cosine voltages multiplied by an analog input. The converters maintain full accuracy when the analog input frequency is in the range dc to 2.6kHz.

The units have internal power amplifiers capable of driving a 2VA load which can be pure inductive, resistive or highly capacitive. The output is fully short-circuit protected against overcurrent. The output of the converter can be used to drive directly into resolver control transformers or in conjunction with an external transformer module to drive synchro control transformers. The power available is more than adequate to drive all standard synchro control transformers.

The separately powered output stage is compatible with conventional ±15V dc power supplies or pulsating power supplies with pedestal components as low as 3V dc.

The use of pulsating power supplies greatly reduces the internal power dissipation in the hybrid package which in turn maximizes the converter's Mean Time Between Failures (MTBF).

A particular feature of the converters is that they have a remote sensing facility which means that output accuracy can be maintained even when long lines have to be driven.

The converter's data inputs are latched and the latches can be CMOS or Low Power Schottky (LS). The former gives advantages in terms of power dissipation and the latter in terms of glitch performance when used in fast dynamic update modes. The latches are transparent and have a separate high and low byte enable.

As an option, the output stage can be fitted with internal TransZorb™ protection. This gives full protection against transient voltages generated by an inductive load in response to an abrupt change in load current. This condition can occur at switch off or as a consequence of external power supply fault conditions.

The units are packaged in 40-pin dual in line hybrid packages and require no external trims or adjustments.

MODELS AVAILABLE

The DRC1745 (14-bit resolution) and DRC1746 (16-bit resolution) are available with accuracies of ±2 or ±4 arc-minutes. Both units have optional TransZorb protection and a choice of either LS or CMOS inputs (see Ordering Information).

Two sets of reference and output transformers are available. The STM1660/STM1663 operates over 47Hz to 440Hz while the STM1680/STM1683 operates over 360Hz to 2.6kHz. The transformers can be Scott T connected to provide a synchro output format.

TransZorb is a registered trademark of General Semiconductor Industries, Inc.

SPECIFICATIONS (typical @ +25°C and ±15V power supplies, unless otherwise noted)

Models	DRC1745	DRC1746
DIGITAL INPUT RESOLUTION	14 Bits (1.32 arc-minutes)	16 Bits (0.33 arc-minutes)
DIGITAL INPUT FORMAT	Parallel natural binary, TTL compatible. Includes internal 27kΩ pull-up resistors.	*
RECOMMENDED ANALOG INPUT (V_{REF})[1]	3.4V rms (single ended input) 3.53V rms (max)	*
OUTPUT WITH RECOMMENDED ANALOG INPUT	6.8V rms 7.07V rms (max)	* *
GAIN (V_{REF} to V_O)	2 ± 0.1%	*
GAIN TEMPERATURE COEFFICIENT	25ppm/°C (max)	*
ANALOG INPUT (V_{REF}) FREQUENCY RANGE	dc to 2.6kHz	*
ANALOG INPUT IMPEDANCE	10.2kΩ	*
ANALOG OUTPUT IMPEDANCE	0.2mΩ max	*
OUTPUT OFFSET VOLTAGE	25mV (max)	*
OUTPUT OFFSET VOLTAGE DRIFT	50μV/°C (max)	*
OUTPUT DRIVE CAPABILITY	2VA (max mean) ± 377mA peak @ 10.6V peak	*
PHASE SHIFT (V_{REF} to V_O)	0.08°@400Hz	*
OUTPUT PROTECTION		
Overvoltage	TransZorb (optional) ± 12V standoff, ± 15V clamp	*
Overcurrent	Limit set@550mA peak. (Case header must be maintained @ 125°C max).	*
RESPONSE TO A STEP INPUT	20μs (max) to within accuracy of converter. Any size digital step input.	*
VECTOR ACCURACY		
Radius Error[2]	0.03%	*
Angular Error	± 2 or ± 4 arc-minutes	*
POWER SUPPLY (NO LOAD)[3,4,5]		
LS Latch Options + 15 Volts	15mA (typ) 22mA (max)	*
− 15 Volts	15mA (typ) 22mA (max)	*
+ 15(P) Volts	20mA (typ) 34mA (max)	*
− 15(P) Volts	20mA (typ) 34mA (max)	*
+ 5 Volts	44mA (typ) 72mA (max)	*
CMOS Latch Options + 15 Volts	24mA (typ) 30mA (max)	*
− 15 Volts	15mA (typ) 22mA (max)	*
+ 15(P) Volts	20mA (typ) 34mA (max)	*
− 15(P) Volts	20mA (typ) 34mA (max)	*
Additional Current (Load Dependent) + 15(P) Volts	400mA Peak (max)	*
− 15(P) Volts	400mA Peak (max)	*
PULSATING POWER SUPPLY PEDESTAL	3V dc (min)	*
POWER DISSIPATION	See Power Dissipation section of this data sheet.	*
CASE TEMPERATURE RANGE[6]	− 55°C to + 125°C Operating − 65°C to + 150°C Storage	* *
SIZE	40-Pin DIL 1.14 × 2.14 × 0.18" (29.0 × 54.4 × 4.6mm)	* *
WEIGHT	0.9 oz (25 grams)	*

Model	Reference Input Transformer STM1680/STM1660	Output Transformer STM1683/STM1663
INPUT VOLTAGE	11.8, 26, 115V rms depending on option R_{HI}, R_{LO}	6.8V rms Sin, Cos
OUTPUT VOLTAGES	3.4V rms ± 1% A_{HI}, A_{LO}	11.8, 26, 90V rms ± 5% S1, S2, S3, (S4)
OUTPUT FORMAT	N/A	Synchro or resolver depending on option
FREQUENCY RANGE		
STM1680	360Hz–2.6kHz	
STM1660	47Hz–440Hz	
STM1683		360Hz–2.6kHz
STM1663		47Hz–440Hz
INPUT IMPEDANCE		
11.8V Input	50kΩ(min)	N/A
26V Input	30kΩ(min)	N/A
115V Input	800kΩ(min)	N/A
ACCURACY		
0.1VA Load	N/A	± 1.0 arc-min (max)
1.4VA Load	N/A	± 2.0 arc-min (max)
2.0VA Load	N/A	± 3.0 arc-min (max)
Temperature Coefficient	N/A	± 0.02 arc-min/°C (max)
OUTPUT IMPEDANCE		
11.8 V Output	N/A	2.9Ω (typ)
26V Output	N/A	13.6Ω (typ)
90V Output	N/A	156Ω (typ)
DC ISOLATION		
Voltage	1000V	1000V
SIZE		
STM1680	1.12 × 1.12 × 0.4" (28.5 × 28.5 × 10.2mm)	
STM1660	1.12 × 1.12 × 1.0" (28.5 × 28.5 × 25.4mm)	
STM1683		2.25 × 1.12 × 0.4" (57.1 × 28.5 × 10.2mm)
STM1663		2.25 × 1.12 × 1.0" (57.1 × 28.5 × 25.4mm)
TEMPERATURE RANGE		
Operating	− 55°C to + 125°C	− 55°C to + 125°C
Storage	− 60°C to + 150°C	− 60°C to + 150°C
WEIGHT (max)		
STM1680	1.5 oz (42 grams)	
STM1660	3.0 oz (84 grams)	
STM1683		2.5 oz (70 grams)
STM1663		5.0 oz (140 grams)

N/A means not applicable.

NOTES
[1] V_{REF} is internally clamped to ± 15V power supplies. Input current should not exceed 10mA.
[2] Worst case error over operating temperature range.
[3] The + 5 volt power supply must never go more than 0.3V below GND potential.
[4] Correct polarity voltages must be maintained on the ± 15V and the ± 15V(P) pins.
[5] Tracking of the ± 15V and ± 15(P) supplies must be maintained.
[6] Adequate heat sinking must be provided to keep the case temperature less than 125°C.
*Specifications same as DRC1745.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS

+15V to GND	+17V
−15V to GND	−17V
+5V to GND	+5.5V, −0.3V
+15(P) to −15(P)	+40V
Digital Inputs GND	+5.5V, −0.3V

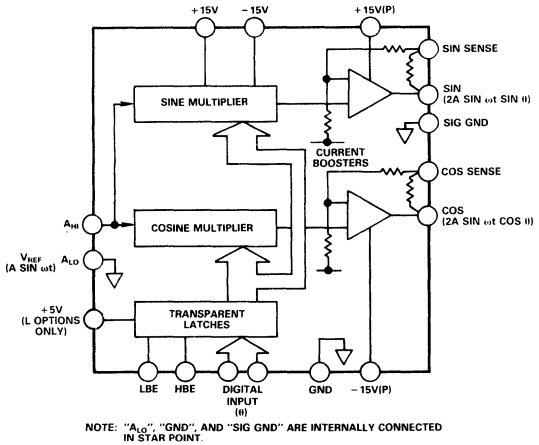
THEORY OF OPERATION

The operation of the DRC1745 and DRC1746 is illustrated in the block diagram shown in Figure 1.

The reference voltage, V_{REF}, (A sin ωt) is multiplied by both Sin θ and Cos θ where θ is the digital angle. The resultant outputs then pass through the current booster output stage to provide the resolver format output voltages viz:

2A Sin ωt Sin θ (Sine output)
and 2A Sin ωt Cos θ (Cos output)

(Note: Converter has a gain of 2 from input to output.)



NOTE: "A_{LO}", "GND", AND "SIG GND" ARE INTERNALLY CONNECTED IN STAR POINT.

Figure 1. Theory of Operation

CONNECTING THE CONVERTER

The connections to the DRC1745 and DRC1746 are very straightforward.

The digital inputs should be connected to the converter using pins 1 (MSB) through 14 (LSB) in the case of the DRC1745 and through 16 (LSB) in the case of the DRC1746. The format of the digital angular input is shown under the "Bit Weight Table" section on this page.

The digital input control lines should be connected as described under the "Digital Data Input" section.

A_{LO} and A_{HI} are for the analog input reference voltage (V_{REF}). It should be noted that this is a single ended input where A_{LO} is grounded internally. If it is desired, the V_{REF} input can be externally isolated using the STM1680 or STM1660 transformer. See the section on "Output and Reference Transformers".

The converters have separate power supply inputs for the output amplifier stage (+15V(P) and −15V(P)) and for the remainder of the converter (+15V and −15V). When dc power supplies are used for the output stage, the supplies may be linked. However, when pulsating power supplies are used for the output stage, a separate dc supply must be provided for the +15V and −15V requirement. The converters have internal capacitive decoupling of 47nF on both power stage and converter supply but it is recommended that 6.8μF capacitors are taken from the +15V and −15V pin to "GND".

The "Case" pin is joined to the case which is isolated and should be connected to a convenient zero potential point in the system.

The sine and cosine outputs are taken from the "Sin" and "Cos" pins with "SIG GND" as the common connection.

The remote sense facility using "Cos Sense" and "Sin Sense" connections should be used as described under the "Remote Output Sensing" heading. If not used, the sense outputs should be connected to the corresponding Sin and Cos outputs.

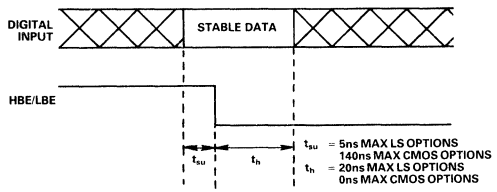
DIGITAL DATA INPUT

The digital input to the converters is internally buffered by transparent latches. The latches will be CMOS (type 54C373) or low power Schottky (LS)(type 54LS373) depending on the option.

The "HBE" input controls the input of the most significant 8 bits and the "LBE" input controls the input of the least significant bits (6 in the case of the DRC1745 and 8 in the case of the DRC1746).

A logic "Hi" on the control lines causes the input to appear transparent and the converter output will follow the changes on the digital input. When "HBE" and "LBE" are taken to a logic "Lo" state, the converter output will be latched at the level of the data present on the input at the low going edge and remains constant until "HBE" and "LBE" are taken to a "Hi" state again. If the latches are not required, "HBE" and "LBE" can be left open circuit. The timing diagram in Figure 2 illustrates the use of "HBE" and "LBE".

Internal resistive pull-ups (to +5V using 27k resistors) are employed on all digital inputs. This ensures full TTL compatibility for either latch option even when sourcing 50μA of leakage current into each external digital driver.



NOTE: INTERNAL LATCHES ARE: 54LS373 (LS) 54C373 (CMOS)

Figure 2. Data Transfer Diagram

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB DRC1745)	0.0220
15	0.0110
16 (LSB DRC1746)	0.0055

POWER DISSIPATION, PULSATING POWER SUPPLIES AND HEAT SINKING

The DRC1745 and the DRC1746 can be used with conventional dc power supplies or a pulsating power supply on the output stage (see Figure 3). The latter gives significant reductions in power dissipation within the hybrid package without any attendant loss of accuracy.

When using a pulsating power supply, full advantage can be taken of the special design which allows the power supply to have a very low dc pedestal voltage. This results in minimized power dissipation. The pedestal voltage can in fact be as low as 3 volts. The combined pedestal plus peak supply voltage must not exceed the absolute maximum rating.

Full accuracy is retained during operation on pulsating power supplies because the output stage employing these supplies is only used to provide current gain. Overall operational loop gain is independently powered. There are no special switch-on/switch-off power supply sequencing requirements, and full internal protection is provided.

The section below demonstrates the power dissipation differences for different load conditions when using dc supplies and pulsating power supplies.

DC Power Supplies:

With inductive loads, the dc resistance is low compared with ac impedance; therefore care should be taken to ensure that no dc offset occurs at the sin and cos outputs. Note that under external current limit conditions asymmetry of the power supplies could occur, forcing a large dc offset to be present at the sin and cos outputs causing heavy power dissipation in the device. Case temperature must be maintained below 125°C.

As the reference input, A_{HI}, is directly coupled, output offset will occur if any dc component is present at this input.

When using dc power supplies, the expression for additional load dependent power dissipation is:

$$P = \frac{2\,V_{dc}I_1}{\pi}\,(|\mathrm{Sin}\theta| + |\mathrm{Cos}\theta|) - \frac{V_oI_1\,\mathrm{Cos}\alpha}{2} \qquad (1)$$

Where V_o is the peak output voltage.
I_1 is the peak value of the output load current.
θ is the digital angle.
α is the load phase angle.
V_{dc} is the dc power supply voltage (usually ± 15 volts).

Pulsating Power Supplies:

When using a pulsating power supply, the expression for additional load dependent power dissipation within the hybrid is:

$$P = \frac{2\,V_pI_1}{\pi}\,(|\mathrm{Sin}\theta| + |\mathrm{Cos}\theta|) + \frac{V_{ac}I_1}{\pi}\,(\mathrm{Sin}\alpha - \alpha\mathrm{Cos}\alpha) \qquad (2)$$

Where V_{ac} is the peak ac component of the pulsating power supply assumed equal to the peak output voltage, V_o.
I_1 is the peak value of the output load current.
θ is the digital angle.
α is the load phase angle.
V_p is the dc pedestal voltage of the pulsating power supply.

Note that $I_1 = \frac{V_o}{|Z|}$ where V_o = Peak output voltage
$= 2 \times V_{REF}$
$|Z|$ = output load

WAVEFORM MUST BE IN PHASE WITH CONVERTER REFERENCE (V_{REF} = A SIN ωt) CONSISTENT WITH MAINTAINING A POWER SUPPLY EXCESS OVER THE OUTPUT WAVEFORM GREATER THAN V_P.

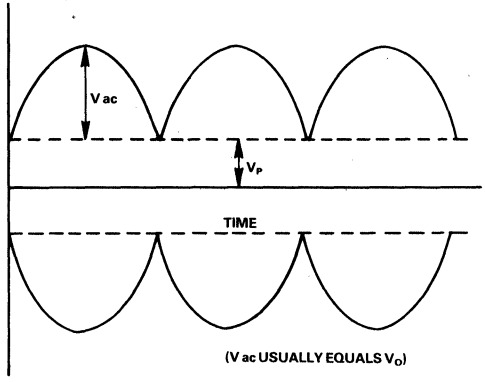


Figure 3. Pulsating Power Supply Format

Examples of Power Dissipation:

Many factors influence the power dissipation within the hybrid. The following two examples, using typical load values and *worst case* digital angle conditions (45 degrees), illustrate the saving in power dissipation which can be achieved by using a pulsating power supply employing a low pedestal voltage.

Note that in the following examples we have chosen:
V_{dc} = ± 15 volts
V_p = 3 volts
V_o = 9.6 volts (6.8 volts rms)
V_{ac} = 9.6 volts (should be chosen to equal V_o)
I_1 = 292mA (equivalent to a 1.4VA mean load)

1) DC power supply, $\theta = 45°$ resistive load.

$$P = \frac{2 \times 15 \times 0.292(\mathrm{Sin}45° + \mathrm{Cos}45°)}{\pi} - \frac{9.6 \times 0.292 \times 1}{2}$$
$$= 3.943 - 1.402$$
$$= \underline{2.54\ \text{Watts}}$$

2) As example (1) but with a 3 volt pedestal pulsating power supply.

From equation (2):

$$P = \frac{2 \times 3 \times 0.292(\mathrm{Sin}45° + \mathrm{Cos}45°)}{\pi} + \frac{9.6 \times 0.292 \times 0}{\pi}$$
$$= \underline{0.79\ \text{Watts}}$$

Thus the pulsating power supply has cut down the internal dissipation by 1.75 watts, a ratio of 3.2:1.

A similar calculation using an inductive load shows a reduction from 3.94 Watts, using a dc power supply, to 1.68 Watts, when a 3 volt pedestal pulsating power supply is used. Thus the pulsating power supply has cut down the internal dissipation by 2.26 Watts, a ratio of 2.3:1.

The graph shown in Figure 4 shows the temperature at the hottest part of the base of the hybrid (in the middle of the base between "+15V(P)" and the opposite "N/C" pin) for resistive loads up to 2VA using dc supplies and pulsating supplies with pedestals of 3 volts and 5 volts.

Figure 5 shows a similar graph for inductive loads up to 1VA.

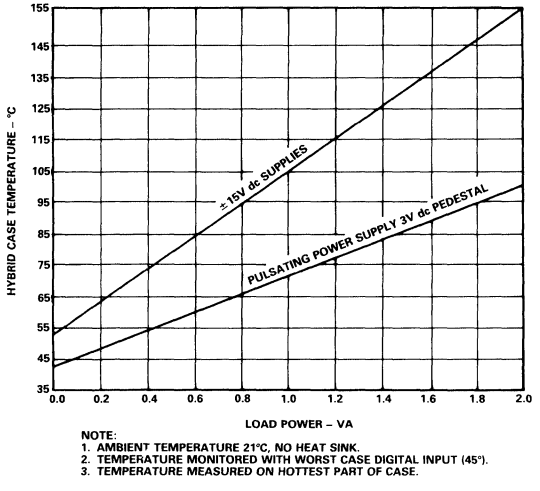


Figure 4. Case Temperature for Resistive Loads

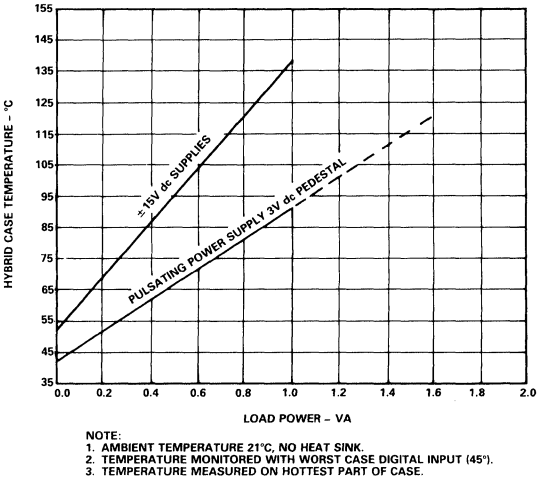


Figure 5. Case Temperature for Inductive Loads

5

As can be seen from Figures 4 and 5, it will be necessary to provide heat sinking when driving significant loads in order to keep the temperature of the case below its 125°C maximum.

The converters have been designed with a flat metal base to facilitate mounting on heat sinking materials. Special thermal management, utilizing direct eutectic bonding, has been employed in the output stage to minimize thermal resistance to:

Angle

0°, 90° θJunction/case = less than 12°C/watt
45°, 135° θJunction/case = less than 6°C/watt

Consequently the internal junction temperatures do not exceed case header temperature by more than 20°C when using pulsating power (even under worst case pure inductive load conditions. The maximum permitted junction temperature is 155°C).

CALCULATING THE LOAD

The following describes how to calculate the load.

In the case of synchro control transformers, first determine the value of Z_{so}. This impedance is normally quoted by the synchro manufacturer.

The load presented by the control transformer will be:

$$\frac{3}{4} \times \frac{V^2}{|Z_{so}|}$$

where V^2 is the rms signal input voltage.

When the STM1683 output transformer pair is used, it is necessary to add 0.25VA to the calculated figure to allow for transformer magnetizing current. For the STM1663 output transformer a figure of 0.30VA should be added.

For example, assume that a 90V rms signal, 400Hz synchro control transformer is to be driven by the DRC1745 in conjunction with the STM1683/412 output transformer pair. (The STM1683/412 boosts the 6.8V rms signal from the DRC1745 to the 90V rms required by the control transformer.)

Z_{so} for the control transformer is quoted as:

700 + j4900

Therefore

$$|Z_{so}| = \sqrt{700^2 + 4900^2} = 4950 \text{ Ohms}$$

Therefore, the load presented by the control transformer is:

$$\frac{90^2}{4950} \times \frac{3}{4} = 1.23\text{VA}$$

Adding to this value 0.25VA for the STM1683 gives a figure of 1.48VA total.

In the case of a resolver control transformer the same exercise must be performed but it is not necessary to multiply by 3/4. Some resolver manufacturers quote rms input current and in this case the load will be the product of the input current and the rms voltage used to drive it. The 0.25VA must be added if the STM1683 transformer pair is used.

DRIVING CAPACITIVE LOADS

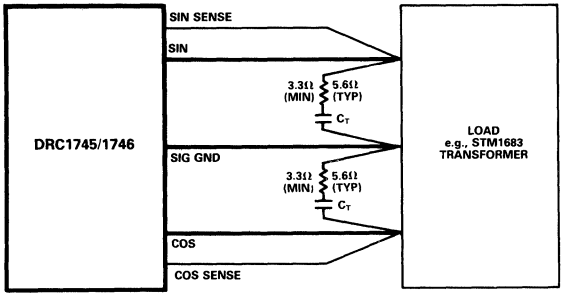
Synchros and resolvers often employ capacitive tuning to minimize power dissipation. This tuning can be on the load itself or (preferably for best accuracy) on the primary of the transformer driving the load. Full tuning modifies the load to appear resistive at the reference frequency, but it appears progressively more capacitive at all frequencies above.

Since the converter is an active negative feedback device, it is essential to include a low value resistor in series with each tuning capacitor to prevent highly dissipative output stage oscillation. This resistor must not be less than 3.3Ω. A value of 5.6Ω is recommended when referred to the output of the DRC1745/DRC1746.

The DRC1745 and DRC1746 can readily drive capacitive inputs up to 100nF at the converter output terminals without special precautions. However, please consult the factory when extreme lengths of screened cable or any other cases of high capacitance are to be driven. For example in the case of step-up transformers where the effective capacitance to be driven is:

$$C_{eff} = n^2 C_L$$

Where C_L is the capacitive load.



NOTE: THE REMOTE SENSE FACILITY IS SHOWN IN THE ABOVE DIAGRAM. C_T IS THE TUNING CAPACITOR.

Figure 6. Incorporating a Resistor in the Tuning Circuit

Care must be taken in tolerancing the tuning capacitors when using secondary tuning since the significant output impedance of typical output transformers can give rise to capacitive balance related angular errors.

The use of these precautions enables the converters to drive fully tuned 2VA loads.

For more information please send for relevant application note.

SHORT CIRCUIT PROTECTION

The short circuit current limit is set at <600mA maximum.

Under short circuit or excessive current conditions, the overcurrent protection circuit will trip and reduce the output current to zero. In order to minimize power dissipated under current limit conditions the device goes into a switching mode, testing the load condition at a high frequency.

When the overload conditions are removed, the output is automatically restored to its normal condition.

VECTOR ERRORS AND EFFECTS

The error law used in the converter has no inherent vector errors. The figure of 0.03% given in the specification is accounted for by tolerances in some of the thin-film resistor networks used in the converter.

These very low vector errors make the converters ideally suited for applications such as displays, or metal cutting control where perfect circles have to be generated.

BANDWIDTH

The open loop gain bandwidth product of the DRC1745 and DRC1746 has been tailored to ensure that the full angular accuracy is maintained over the broadband range of dc to 2.6kHz. This results in a closed loop bandwidth of 300kHz.

REMOTE SENSE FACILITY AND ADDITIONAL OUTPUT ERRORS

A remote sense facility is included in the DRC1745 and DRC1746 in order to reduce errors caused by the output interconnection wiring when driving large loads. The magnitude of this error is illustrated by two examples below.

Assume that the sine and cosine load impedances are perfectly matched and the sine output wiring resistance matches the cosine output wiring resistance to within 5%. Then for a resistive load of 1.4VA (33 ohms) and the worst case angle of 45 degrees, there will be 1.3 arc-minutes of extra error introduced for every 250 milliohms of resistance for the loop wiring between the converter and the load. (AWG22 = 17mΩ/ft, 1 oz PCB copper = 400mΩ/ft.)

In the case of an inductive load under similar conditions, 500 milliohms would produce the same error.

Using the remote sense facility as shown in Figure 7 will half this error or allow twice the distance to be driven for the same additional error.

If the remote sense is not used, then "COS SENSE" should be joined to "COS" and "SIN SENSE" should be joined to "SIN" at the PCB edge connector.

Note also that when output transformers are used with the converters they should be regarded as the load and the remote sense wires taken to the transformer primary inputs.

Sense wiring may employ minimum wire gauge; it does not carry load current.

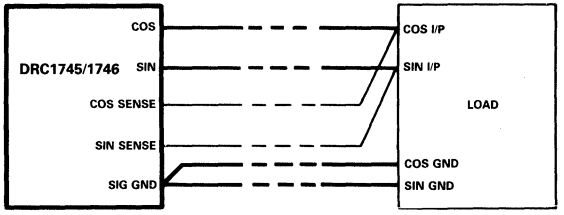


Figure 7. Using the Remote Sense Facility

The ground returns from the load should be individually wired and star-point connected at the converter's signal ground. Any common resistance in the signal returns will produce errors due to the summation of the sin and cos outputs. With a resistive load of 33 ohms at 1.4VA, and at the worst angles of 0 and 90°, there will be 1.3 arc-minutes of extra error introduced for every 12.5 milliohms of common signal return resistance.

TRANSZORB™ OUTPUT PROTECTION

As an option, the output stages of the converter can be internally fitted with TransZorb protection. This form of protection can be advantageous and significantly increase the Mean Time Between Failures when driving inductive loads. The TransZorbs, which are effectively back to back zener diodes, give full protection against transient voltages generated by an inductive load in response to an abrupt change in load current. Such a change can occur at switch off or as a consequence of external power supply fault conditions. The TransZorbs are rated to give protection against worst case transients corresponding to an instantaneous interruption of the converter when driving into a full 2VA pure inductive load with the converter operating at the maximum case temperature of 125°C.

Figure 8 shows a simplified diagram of the converter output stage indicating the action of the TransZorb when the 15 volt supply is interrupted.

It is important to appreciate that destructively high voltages can be generated (given by E = Ldi/dt) even for modest inductive loading, under many fault conditions, since di/dt is effectively uncontrolled. Internal TransZorb protection is a better and more direct solution to the problem than employing a pair of reverse biased diodes to the output stage power supplies. This is because the transient is contained within the specific load disturbed and does not escape into the power supply wiring and hence cause possible damage to other equipments and devices. A domino effect of catastrophic failure is therefore prevented.

Figure 9 shows the nature of transient waveforms where by the very large transient voltage generated by the inductive load is limited to a safe clamp level when it is applied to the output stage.

TransZorb is a registered trademark of General Semiconductor Industries, Inc.

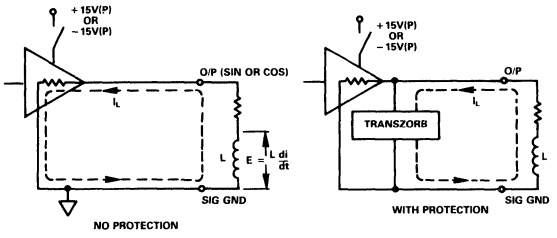


Figure 8. DRC1745/DRC1746 Output Stage Showing TransZorb Protection

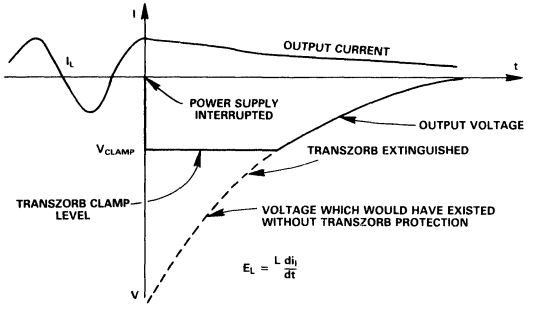


Figure 9. Transient Waveforms and TransZorb Clamping

In addition, there are conventional diode clamps on the ±15V(P) power supplies.

OUTPUT AND REFERENCE TRANSFORMERS

A set of low profile (0.4" high) reference and output transformers (which are capable of handling the full drive capability of the DRC1745 and DRC1746 over a frequency range of 360Hz to 2.6kHz) are available in order to accept the standard voltage formats of synchros and resolvers.

The reference transformer, STM1680, can accept voltages of 11.8 volts, 26 volts or 115 volts depending on the option and its output is 3.4 volts rms which is suitable for connecting to A_{HI} and A_{LO} on the converter.

The output transformer pair, STM1683, accepts the 6.8 volts rms output of the converter and provides a synchro or resolver format depending on the option.

Note: For resolver option for the STM1683 transformer, part number is RTM1683.

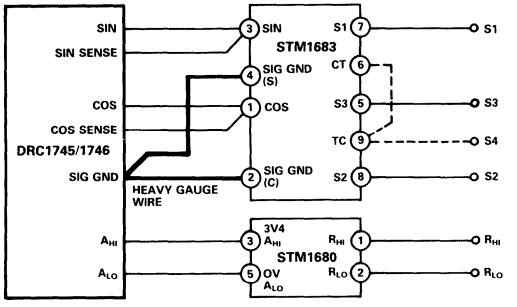
The pin out and dimensions of the STM1680 and STM1683 are shown on the next page, and the connection to the converter in Figure 10.

Note: For operation over the frequency range 47Hz to 440Hz a similar set of transformers are available (1.0" profile height). Part numbers are STM1660 (reference transformer) and STM1663 (output transformer).

RESISTIVE INPUT SCALING

The analog reference input can be externally resistively scaled to cater for a wide range of voltage both when used with or without the reference transformer, STM1680/STM1660.

When the converters are used with the STM1680/STM1660 transformer, a resistance of value 3kΩ per extra volt required should be inserted in the A_{HI} line. Care should be taken to ensure that the voltage on the analog input (A_{HI}, A_{LO}) is 3.4



NOTE: FOR SYNCHRO OUTPUT "CT" MUST BE CONNECTED TO "TC". FOR RESOLVER OUTPUT "TC" IS S4 (NO LINK)

Figure 10. Connecting the DRC1745 to the STM1680 and STM1683 Transformers

volts rms in order to provide a full scale analog output. The maximum output voltage of the converter is proportional to the input voltage (gain of 2) and therefore the resistor tolerance should be chosen so that the correct voltage appears across the A_{HI}, A_{LO} pins. Note that the input to the reference transformer should not exceed the rated max.

Note that the best dc output offset performance is achieved when the STM1680/STM1660 transformer is used. However the use of resistive scaling can never cause an additional offset of greater than 6.5mV (max), 2.6mV (typ).

OTHER PRODUCTS

We manufacture a wide range of hybrid and modular circuits for processing synchro and resolver information. Please ask for our comprehensive literature.

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria
2. Constant Acceleration	3000g
3. Burn-In	160 hrs. at 125°C
4. Gross Leak Test	In-House Criteria
5. Final Electrial Test	Performed at 25°C

HI-REL PROCESSING

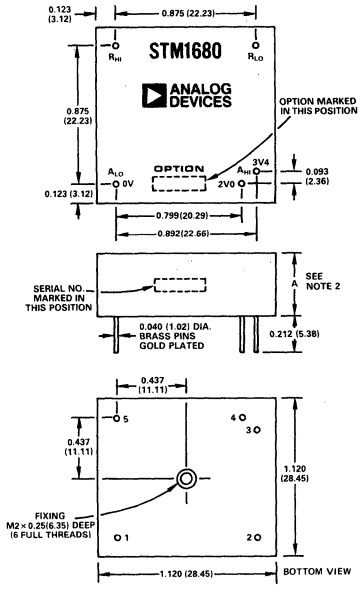
All models ordered to high reliability requirements will be identified with a B suffix, and will have received the following processing:

1. Internal visual inspection
2. Stabilization bake, 24 hours at 150°C
3. Temperature cycling, −65°C to +150°C
4. Constant acceleration, 3000g
5. Powered burn-in, 160 hours at 125°C
6. Final electrical test at T_{MIN} and T_{MAX}
7. Seat test, fine and gross
8. External visual inspection

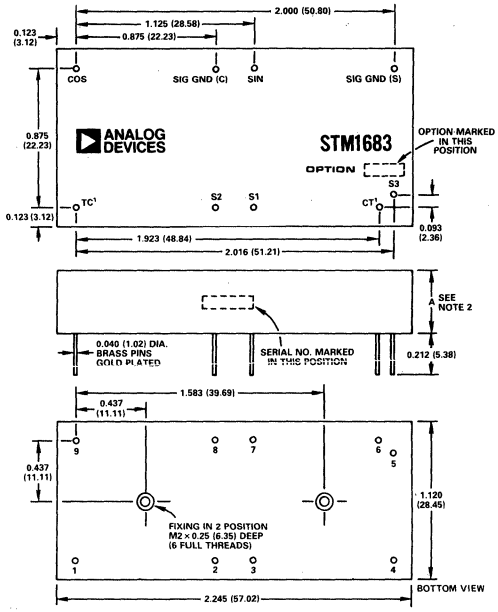
OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).

STM1680/STM1660

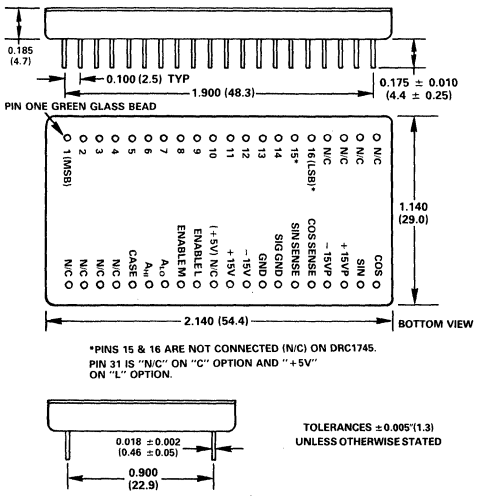


STM1683/STM1663



NOTES
1. "TC" READS "S4" and "CT" READS "NC" ON RESOLVER DEVICE (RTM1683).
2. DIMENSION "A" IS 0.4 (10.2) FOR STM1680 AND STM1683, AND 1.0 (25.4) FOR STM 1660 AND STM 1663. THE TOLERANCES ARE +0.010", −0.005" OR +0.25mm, −0.13mm.

DRC1745/1746



ORDERING INFORMATION

DRC1745/LT4/B

- 1745 = 14-Bit Resolution
- 1746 = 16-Bit Resolution
- Add B after part number if high reliability processing required.
- 2 = ±2 Arc-Mins Accuracy
- 4 = ±4 Arc-Mins Accuracy
- L = Low power Schottky input latches
- C = CMOS input latches
- T = Internal TransZorb protection
- O = Without TransZorb protection

STM1680.A

- 1680 = 360Hz – 2.6kHz
- 1660 = 47Hz – 440Hz
- A = 26V (26V reference, synchro)
- A = 115V (115V reference, synchro)
- A = 11V8 (11.8V reference, resolver)
- A = 26V (26V reference, resolver)

STM1683.4YZ

- STM for synchro output options
- RTM for resolver output options
- Z = 1 (11.8V rms synchro output)
- Z = 2 (90V rms synchro output)
- Z = 3 (11.8V rms resolver output)
- Z = 4 (26V rms resolver output)
- Z = 8 (11.8V rms resolver output)
- 1683 = 360Hz – 2.6kHz
- 1663 = 47Hz – 440Hz
- Y = 1 360Hz to 2.6kHz (STM1683 only)
- Y = 2 47Hz to 440Hz (STM1663 only)
- 4 = −55°C to +125°C operating temperature range.

ANALOG DEVICES

Hybrid Inductosyn Preamplifier

IPA1764

FEATURES
Hybrid Construction
Phase Shift <5°
Phase Match <1°
Load Capacity 10,000pF
Full Military Temperature Range

APPLICATIONS
The IPA1764 is recommended for use with the 1S10/20, 1S14/24 and other 10- and 12-bit Inductosyn*/Resolver-to-Digital Converters.

GENERAL DESCRIPTION

The output signals from an Inductosyn slider are at a low level of the order millivolts and require amplification and buffering before transmission to an Inductosyn-to-digital converter. The IPA1764 provides the necessary gain and output impedance for this purpose.

Any gain mismatch in the two channels amplifying the sine and cosine outputs of the Inductosyn slider contributes to the system error. The IPA1764 with a 0.15% gain match over the temperature range only contributes an error of 0.23 micron using a 2mm pitch Inductosyn. By carefully controlling phase mismatch to less than 1°, the error contribution is only 0.2 micron in a 2mm pitch Inductosyn.

The IPA1764 with an output resistance of less than 3 ohms and a capability of driving a cable capacity of 10,000pF is totally suited to machine tool applications where the Inductosyn-to-digital converter is remote from the measuring Inductosyn.

The IPA1764 is of hybrid manufacturing techniques, and available in two temperature range versions–industrial temperature range (0 to +70°C) and extended temperature range (−55°C to +125°C).

Both versions of the IPA1764 are housed in an 18-pin metal case.

APPLICATION

The diagram below shows a "hookup" with the preamplifier, power oscillator and a 1S60 with an Inductosyn. Precise application information is not possible as the Inductosyn in its application has many variables.

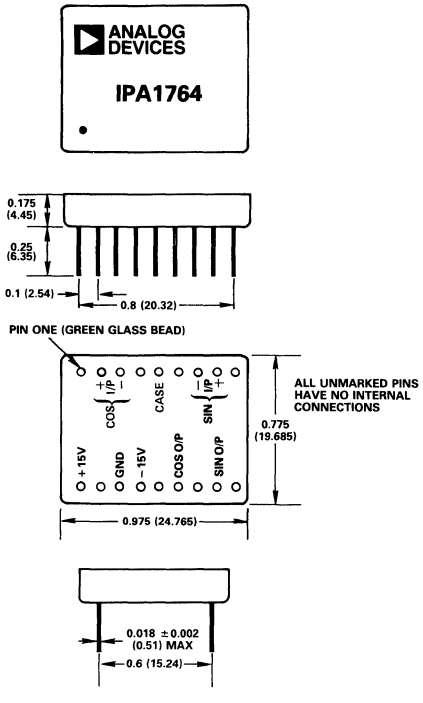
Current Set Resistor
This resistor is used to match the voltage output of the oscillator to the Inductosyn track resistance and provide the manufacturer's recommended current. By variation of the voltage outputs and current resistance, track by this up to approximately 10 feet (3 meters) can be accommodated.

Decoupling
The preamplifier and oscillator have internal high frequency decoupling capacitors on the supply lines, however, it is recommended that electrolytic decoupling capacitors are connected close to the hybrid pins.

*Inductosyn is a registered trademark of Farrand Industries, Inc.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ORDERING INFORMATION

IPA1764 X 60 B

- B — High Reliability Processing
- X = 5 — 0 to +70°C Operating Temperature Range
- X = 4 — −55°C to +125°C Operating Temperature Range

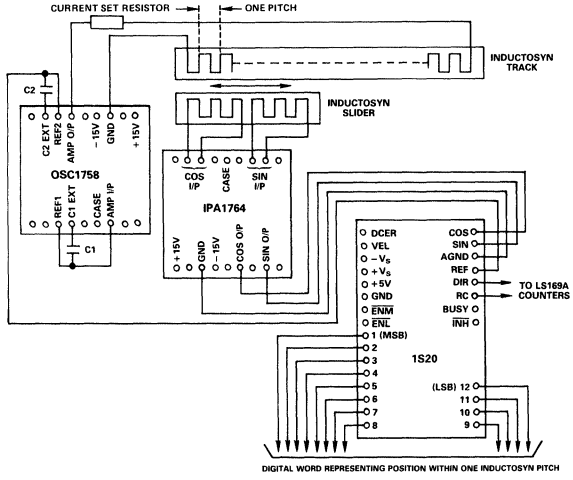
SPECIFICATIONS (typical @ +25°C over full range of power supply inputs unless otherwise noted)

Model	IPA1764/560	IPA1764/460
GAIN	1250 ± 5%	*
GAIN MISMATCH Channel to Channel Over Full Temperature Range	± 0.15% (equivalent to 2.5 arc mins)	± 0.3%
PHASE SHIFT	<5°	*
PHASE MISMATCH Channel to Channel	<1°	*
CROSSTALK	<0.1%	*
OPERATING FREQUENCY	10kHz	*
INPUT RESISTANCE	5kΩ ± 10%	*
OUTPUT RESISTANCE	<5Ω	*
MAX LOAD CAPACITY	10,000pF	*
MAX SIGNAL OUTPUT LEVEL	3V rms	*
POWER SUPPLIES Voltage Current	± 12V to ± 15V 50mA max	* *
TEMPERATURE RANGE Operating	0 to +70°C	−55°C to +125°C
SIZE	0.775" × 0.975" × 0.175" (19.7mm × 24.8mm × 4.5mm)	*
WEIGHT	0.25 ozs (7 grams)	*

NOTES
*Specification same as IPA1764/560.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM VALUES WITH RESPECT TO SUPPLY GROUND

Sin and Cos I/P . . . . . +V
+V Pin . . . . . +17V
−V Pin . . . . . −17V
Sin and Cos O/P 1k Load . . . . . +10V
Indefinite Short Circuit Proof



Use of 1S20 with Inductosyn Preamplifier IPA1764, Hybrid Power Oscillator OSC1758

ANALOG DEVICES

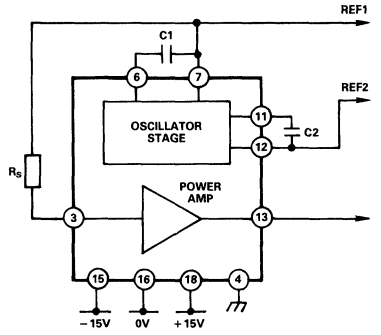
Hybrid Power Oscillator

OSC1758

FEATURES
Full Military Temperature Range
Hybrid Construction
18-Pin DIL Package
0-10kHz Frequency Range
In-Phase and Quadrature Outputs

APPLICATIONS
Synchro Resolver, and Inductosyn® Excitation
LVDT Drive

OSC1758 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts, over 0 to 10kHz.

The device comprises two independent parts–an oscillator and a power amplifier.

The oscillator stage has two signal outputs, one 90° in phase advance with respect to the other.

The oscillator frequency is programmable in the range of 0 to 10kHz by two identical external capacitors.

The power amplifier stage is externally short circuit protected and has a gain of 2.8 ± 1%. The maximum output current this stage can produce is 215mA rms (at 7V rms).

Connecting either of the oscillator stage outputs to the power amplifier input, using an external link, will give a nominal output of 7 volts rms. Lower voltages can be obtained by connecting an external resistor in series with the amplifier's inputs.

The OSC1758 is housed in an hermetically-sealed 18-pin DIL metal case, and operates over full military temperature range (−55°C to +125°C), as well as the industrial (0 to +70°C) temperature range.

MODELS AVAILABLE

The OSC1758 is available in both industrial and military temperature ranges. For details of how to specify the required part, see "Ordering Information".

CONNECTING THE OSC1758

The block diagram shows the output configuration, when using the power amplifier stage. If only the oscillator stage is required, the connection between pin 3 and pin 7 is not included.

The frequency of oscillation for the OSC1758 in the block diagram is determined by the two identical capacitors C1 and C2. For the frequency required, the value of C1 and C2 should be calculated using the following equation.

$$C_1 = C_2 = \frac{1}{F_{OSC} \times 10^5} \quad \text{Farads}$$

Where F_{OSC} = Frequency of oscillation in Hz.

For a reduced output a series resistor, R_S, must be added.

For the required output voltage R_S should be calculated as follows:

$$R_S = \frac{37.5 \times 10^3}{V_{OUT}\,(rms)} - 5350 \text{ Ohms}$$

STABILITY

To ensure stability of both frequency and voltage level outputs it is essential that good quality external capacitors are used, e.g., Silver Mica or Polystyrene.

The tolerance quoted in the specification applies if high grade Silver Mica capacitors, with a temperature coefficient of less than 50ppm/°C, and a low loss factor, are used.

POWER DISSIPATION

The thermal dissipation characteristics for the OSC1758 are as follows:

θ junction – case = 15°C/W
θ junction – ambient = 40°C/W
θ j (max) = 150°C.

Total Power Dissipation =

$(V_{SUPPLY} \times I_{SUPPLY}) - (V_{OUT} \times I_{OUT} \times \text{cosine } \phi)$

where ϕ = load phase angle

NOTE: Although the power amplifier stage has internal short circuit protection, a heat sink should be employed for protection against continuous short circuit conditions.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

Inductosyn® is a registered trademark of Farrand Industries, Inc.

SPECIFICATIONS (typical @ +25°C with ±15V power supplies unless otherwise noted)

Model	OSC1758/500	OSC1758/400
FREQUENCY RANGE	0-10kHz	*
FREQUENCY STABILITY[1,2]	±5%	*
REFERENCE 1 OUTPUT[1]	2.5V rms ±5% @ 3mA rms	*
REFERENCE 2 OUTPUT[1]	2.5V rms ±5% @ 3mA rms 90° Phase Advanced with Respect to Ref. 1 Output	*
AMPLIFIER OUTPUT[3]	7V rms @ 215mA max	*
CAPACITIVE LOAD	10nF (max)	*
AMPLIFIER GAIN[1]	2.8 ±1%	*
AMPLIFIER INPUT RESISTANCE	5.35kΩ ±1%	*
POWER DISSIPATION	4.0 Watts (max)	*
POWER SUPPLY[4]	±15V 60mA (max) No Load 160mA (max) Full Load	* *
TEMPERATURE RANGE Operating Storage	 0 to +70°C −65°C to +150°C	 −55°C to +125°C *
SIZE	0.975" × 0.775" × 0.175" (24.8mm × 19.7mm × 4.5mm)	*
WEIGHT	0.25 ozs. 7 grams	*

NOTES
[1]Over full operating temperature range.
[2]See section on "Stability".
[3]Derated to 5V rms @ 215mA if using ±12 volt power supply.
[4]Will operate with ±12 volt power supply with derated output voltage.
*Specifications same as OSC1758/500
Specifications subject to change without notice.

ABSOLUTE MAXIMUM VALUES WITH RESPECT TO SUPPLY GROUND

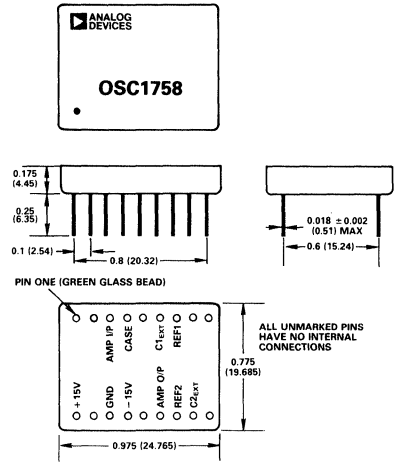
$+V_S$ . . . . . −0.3V to +18V
$-V_S$ . . . . . +0.3V to −18V

ORDERING INFORMATION

OSC1758 X 00 B
- B — High Reliability Processing
- X = 5 — 0 to +70°C Operating Temperature Range
- X = 4 — −55°C to +125°C Operating Temperature Range

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



12- and 14-Bit Hybrid Synchro/ Resolver-to-Digital Converters

SDC/RDC1740/1741/1742

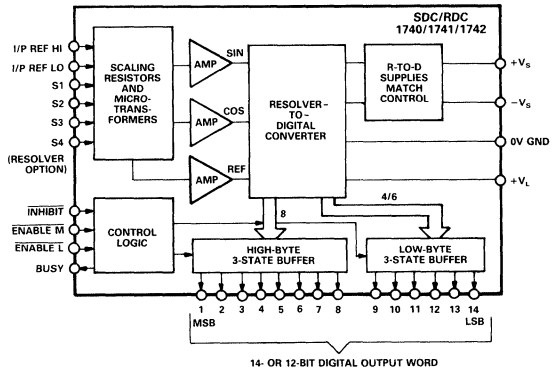
FEATURES
Internal Isolating Transformers
Military Temperature Range
Three Accuracy Options
14-Bit or 12-Bit Resolution
High, Continuous Tracking Rate
32-Pin Welded Metal Package
Hermetically Sealed
Ratiometric Conversion
Laser Trimmed – No External Adjustment
Three-State Latched Outputs

APPLICATIONS
Flight Instrumentation Systems
Military Servo Control Systems
Artillery Fire Control Systems
Avionic Systems
Antenna Monitoring
Robotics
Engine Controllers
Coordinate Conversion
Axis Transformation
CNC Machine Tooling
Process Control

GENERAL DESCRIPTION

The SDC/RDC1740/1741/1742 are hybrid 14- or 12-bit continuous tracking synchro or resolver to digital converters contained in 32-pin welded metal packages. In the core of this hybrid the conversion process is performed by a monolithic IC manufactured in Analog Devices proprietary BiMOS II process that combines the advantages of CMOS logic and bipolar high accuracy linear circuits on the same chip. Internal isolating microtransformers are used to provide true isolation of the signal and reference inputs. The 14- or 12-bit digital word is in a three-state digital form available in two bytes. Using separate $\overline{\text{ENABLE}}$ inputs for the most significant 8 bits and the least significant 6 or 4 bits not only simplifies multiplexing of more than one device onto a single data bus, but also enables the $\overline{\text{INHIBIT}}$ input to be used without interrupting the operation of the tracking loop. The converters are hermetically sealed in a 32-pin welded metal package.

SDC/RDC 1740/1741/1742 FUNCTIONAL BLOCK DIAGRAM



MODELS AVAILABLE

The three synchro/resolver-to-digital converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1740XYZ is a 14-bit converter with an overall accuracy of ±5.3 arc minutes and a resolution of 1.3 arc minutes.

Model SDC1741XYZ is a 12-bit converter with an overall accuracy of ±15.3 arc minutes and a resolution of 5.3 arc minutes.

Model SDC1742XYZ is a 12-bit converter with an overall accuracy of ±8.5 arc minutes and a resolution of 5.3 arc minutes.

Each model has two operating temperature range versions, those covering the industrial temperature range (0 to +70°C) and the military temperature range (−55°C to +125°C). The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage whether it will accept synchro or resolver format. To ensure a high level of reliability each converter receives stringent precap visual inspection, environmental screening and final electrical test.

Military temperature range devices and those processed to high reliability screening standards (suffix B) receive further levels of testing and screening to ensure high levels of reliability. More information about the option codes is given under the heading Ordering Information.

SPECIFICATIONS (typical at 25°C unless otherwise specified)

Parameter	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742	Units	Comments	Notes
CONVERTER PERFORMANCE						
Accuracy	±5.3 max	±15.3 max	±8.5 max	arc min		1, 3
Tracking Rate	27 min	18 min	**	rev/s		4
Resolution	14	12	**	Bits	Output Coding Parallel	
	(1 LSB = 1.3 arc min)	(1 LSB = 5.3 arc min)	**		Natural Binary	
Signal & Reference Frequency	400	*	*	Hz	Option X1Z	
	2.6	*	*	kHz	Option X4Z	
Repeatability of Position Output	1	*	*	LSB		4
Bandwidth	130	150	**	Hz		4
SIGNAL INPUT IMPEDANCE						
90V Signal	200	*	*	kΩ	Resistive Tolerance ±2%	4
26V Signal	57.7	*	*	kΩ		4
11.8V Signal	26	*	*	kΩ		4
REFERENCE INPUTS						
Reference Voltage	11.8, 26, 115	*	*	V rms	See Ordering Information	
Reference Impedance						
115V Ref	120	*	*	kΩ	Resistive Tolerance ±5%	4
26V Ref	27	*	*	kΩ		4
11.8V Ref	12.3	*	*	kΩ		4
ACCELERATION CONSTANT	56000	80000	**	sec^{-2}	Symbol K_a	4
LARGE STEP RESPONSE	85 typ	60 typ	**	ms	179° Step for Settling to	1, 3
	100 max	75 max	**	ms	1 LSB of Error	
POWER LINES						
$+V_S = +15V$	28 typ 35 max	*	*	mA	Quiescent Condition	1, 3
$-V_S = -15V$	28 typ 35 max	*	*	mA	Quiescent Condition	1, 3
$V_L = +5V$	35 typ 56 max	*	*	mA	Quiescent Condition	1, 3
Power Dissipation	1.4 max	*	*	W		
DIGITAL INPUTS ($\overline{\text{INHIBIT}}$, ENABLE $\overline{\text{L}}$, ENABLE M)						
V (Input High)	2 min	*	*	V dc	$V_L = +5V$	1, 3
V (Input Low)	0.7 max	*	*	V dc	$V_L = +5V$	1, 3
I (Input High)	20 max	*	*	μA	$V_{IH} = 2.4V$	1, 3
I (Input Low)	−400 max	*	*	μA	$V_{IL} = 0.4V$	1, 3
ENABLE AND DISABLE TIME	80 max	*	*	ns		2, 4
$\overline{\text{INHIBIT}}$						
Sense	Logic Low	*	*			
	to INHIBIT	*	*			
Time to Data Stable (after Negative-Going Edge of $\overline{\text{INHIBIT}}$)	640 max	*	*	ns		4
BUSY OUTPUT						
Sense	Active Logic High when converter position output changing.					
Timing	Positive going edge 50ns before change in position output.					
Width						
	400 typ	*	*	ns		1, 3
	200 min	*	*	ns		1, 3
	600 max	*	*	ns		1, 3
Load	2 min	*	*	TTL		4
DIGITAL OUTPUTS						
Voltage Levels						
Logic High	2.4 min	*	*	V dc	$V_L = +5V$, $I_{OH} = -240\mu A$	1, 3
Logic Low	0.4 max	*	*	V dc	$V_L = +5V$ $I_{OL} = 9.6mA$	1, 3
Load	6 max	*	*	TTL		

Parameter	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742	Units	Comments	Notes
OPERATING TEMPERATURE RANGE						
Option 5YZ	0 to + 70	*	*	°C		
Option 4YZ	−55 to +125	*	*	°C		
DIMENSIONS	1.74×1.14×0.28	*	*	Inch	See Package	4
	(44.2×28.9×7.1)	*	*	mm	Information	
WEIGHT	0.86 max	*	*	oz		4
	25 max	*	*	grams		

NOTES
[1]Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) ±10% signal and reference harmonic distortion; (c) ±5% power supply variation; (d) ±10% variation in reference frequency.
[2]$\overline{\text{ENABLE M}}$ enables most significant 8 bits.
$\overline{\text{ENABLE L}}$ enables least significant 4 bits (or 6 bits for SDC/RDC1740).
[3]100% tested at nominal values of power supplies, input signal voltages and operating frequency.
[4]Guaranteed by design.

*Specifications same as SDC/RDC1740.
**Specifications same as SDC/RDC1741.
Specifications subject to change without notice.

5

ABSOLUTE MAXIMUM RATINGS

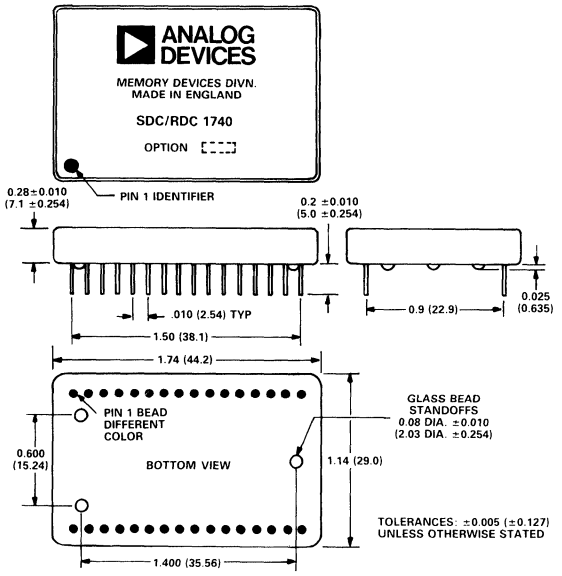
$+V_S$[1] to GND . . . . . +17.25V dc
$-V_S$ to GND . . . . . −17.25V dc
$+V_L$[2] to GND . . . . . +7V dc
Reference Input HI to GND . . . . . ±350V dc
Reference Input LO to GND . . . . . ±350V dc
Common Mode Range . . . . . 175V rms
S1, S2, S3, S4 to GND . . . . . ±350V dc
Any Logical Input to GND . . . . . −0.4V to $+V_L$
Case to GND . . . . . ±20V dc
Storage Temperature Range . . . . . −65°C to +150°C

CAUTION:
[1]Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
[2]The +5V power supply must never go below GND potential.

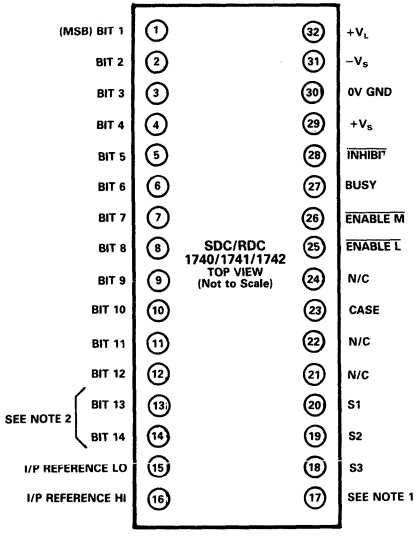
NOTE
Absolute maximum ratings are those values beyond which damage to the device may occur.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN CONFIGURATION



NOTE 1. FOR THE RESOLVER OPTION PIN 17 IS S4. FOR THE SYNCHRO OPTION PIN 17 IS NOT CONNECTED.

NOTE 2. FOR THE 1741 AND 1742 PINS 13 AND 14 ARE NOT CONNECTED.

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB for 1741/1742)	0.0879
13	0.0439
14 (LSB for 1740)	0.0220

Table I. Bit Weight Table

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1-14	Bit 1-14 (1740)	Parallel output data bits.
1-12	Bit 1-12 (1741/1742)	
15	REF LO	Input pins for the reference signal.
16	REF HI	
17	S4 OR N/C	S4 signal input for Resolver option. N/C for Synchro option.
18	S3	
19	S2	Synchro/Resolver input signals.
20	S1	
21	N/C	No Connection.
22	N/C	No Connection.
23	CASE	Should be connected to 0V GND.
24	N/C	No Connection.
25	$\overline{\text{ENABLE L}}$	$\overline{\text{ENABLE L}}$ enables the 6 or 4 least significant bits.
26	$\overline{\text{ENABLE M}}$	$\overline{\text{ENABLE M}}$ enables the 8 most significant bits. Logic High sets the output data bits to a high impedance state; a Logic Low presents the data in the latches to the output pins.
27	BUSY	Converter busy. A Logic High output indicates that the output latches are being updated and data should not be transferred.
28	$\overline{\text{INHIBIT}}$	Logic Low inhibits the data transfer from the counter to the output latches.
29	$+V_S$	Main positive power supply.
30	0V GND	Power supply ground.
31	$-V_S$	Main negative power supply.
32	$+V_L$	Logic power supply.

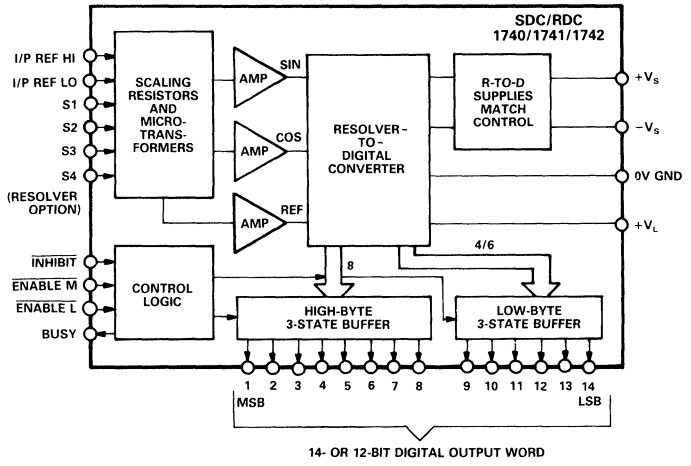


Figure 1. Functional Diagram of the SDC/RDC1740/1741/1742

THEORY OF OPERATION

In the synchro-to-digital converter configuration, the 3-wire synchro output should be connected to S1, S2 and S3 on the unit and the Scott T transformer pair will convert these signals into resolver format, i.e.,

$V_1 = K\ E_O \sin \omega t \sin \theta$ (SIN)
$V_2 = K\ E_O \sin \omega t \cos \theta$ (COS)

where θ is the angle of the synchro shaft.

In the resolver-to-digital converter configuration, the 4-wire resolver output should be connected to S1, S2, S3 and S4 on the unit and the transformers will act purely as isolators.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

V_1 is multiplied by COSϕ and V_2 is multiplied by SINϕ to give:

$K\ E_O \sin \omega t \sin \theta \cos \phi$
and $K\ E_O \sin \omega t \cos \theta \sin \phi$.

These signals are subtracted by the error amplifier to give:

$K\ E_O \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$
or $K\ E_O \sin \omega t \sin (\theta - \phi)$.

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null sin $(\theta - \phi)$. The digital output (counter ϕ), then represents the synchro/resolver shaft angle θ within the specified accuracy of the converter.

$\overline{\text{INHIBIT}}$ INPUT

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a busy pulse to refresh the output data.

$\overline{\text{ENABLE}}$ INPUTS

The $\overline{\text{ENABLE}}$ inputs determine the state of the output data. A Logic High maintains the output data pins in the high impedance condition, and application of a Logic Low presents the data in the latches to the output pins. $\overline{\text{ENABLE M}}$ enables the most significant 8 bits, while $\overline{\text{ENABLE L}}$, enables the least significant 4 bits (6 bits in the SDC/RDC1740). The operation of the $\overline{\text{ENABLE}}$ inputs has no effect on the conversion process.

DATA TRANSFER

Data transfer can be accomplished using either the $\overline{\text{INHIBIT}}$ input or the trailing edge, positive to negative transition of the BUSY pulse output.

The data will be valid 640ns after the application of a Logic Lo to the $\overline{\text{INHIBIT}}$ input. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active busy pulse to clear. By using the $\overline{\text{ENABLE M}}$ and $\overline{\text{ENABLE L}}$ inputs the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a Logic Hi state to enable the output latches to be updated.

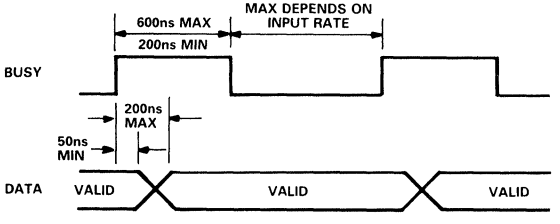


Figure 2. Timing Diagram

5

BUSY OUTPUT

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL levels. A BUSY is initiated each time the input moves by an analog equivalent of an LSB and the internal counter is incremented or decremented or the $\overline{\text{INHIBIT}}$ input is released.

Typically the width of the BUSY pulse is 400ns during the position data output updates. The trailing edge, positive to negative transition, of the BUSY pulse indicates that the position data output has been updated and is ready for transfer (data valid). The maximum load on the BUSY output using the trailing edge of the BUSY pulse is 2 TTL loads.

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be $\pm 15V$ and must not be reversed. The digital logic supply V_L is connected to $+5V$.

It is suggested that a parallel combination of a $0.1\mu F$ ceramic and a $6.8\mu F$ electrolytic capacitor is placed from each of the three supply pins to GND.

The pin marked CASE is connected electrically to the case and should be taken to a convenient zero volt potential in the system.

The digital output is taken from Pin 1 through to Pin 12 for the SDC/RDC1741/1742 and Pin 1 through to Pin 14 for the SDC/RDC1740 where Pin 1 is the MSB.

The reference connections are made to REF HI and REF LO. In the case of a synchro, the signals are connected to S1, S2 and S3 according to the following convention:

$E_{S1\text{-}S3} = E_{RLO\text{-}RHI} \sin \omega t \sin \theta$

$E_{S3\text{-}S2} = E_{RLO\text{-}RHI} \sin \omega t \sin (\theta + 120°)$

$E_{S2\text{-}S1} = E_{RLO\text{-}RHI} \sin \omega t \sin (\theta + 240°)$

For a resolver, the signals are connected to S1, S2, S3 and S4 according to the following convention:

$E_{S1\text{-}S3} = E_{RLO\text{-}RHI} \sin \omega t \sin \theta$
$E_{S2\text{-}S4} = E_{RHI\text{-}RLO} \sin \omega t \cos \theta$

The BUSY, $\overline{\text{INHIBIT}}$ and $\overline{\text{ENABLE}}$ pins should be connected as described under the heading Data Transfer.

RESISTIVE SCALING OF INPUTS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate any change of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

Note: The accuracy of the converter will be affected by the matching accuracies of resistors used for external scaling.

To calculate the values of the external scaling resistors in the case of a synchro converter, add $1.11k\Omega$ per extra volt of signal in series with S1, S2 and S3 and $1k\Omega$ per extra volt of reference in series with RHI. In the case of a resolver-to-digital converter, add $2.22k\Omega$ in series with S1 and S2 per extra volt of signal and $1k\Omega$ per extra volt of reference in series with RHI.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.

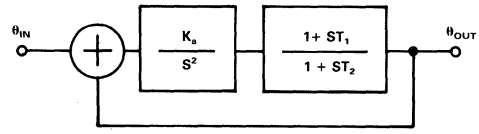


Figure 3. Transfer Function of SDC/RDC1740/1741/1742

Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1+ST_1}{1+ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3T_2}{K_a}}$$

Model SDC/RDC1740

Where $K_a = 56{,}000$
$T1 = 0.01$
$T2 = 0.001525$

The gain and phase diagrams are shown in Figures 4 and 5.

Model SDC/RDC1741/1742

Where $K_a = 80{,}000$
$T1 = 0.0087$
$T2 = 0.001569$

The gain and phase diagrams are shown in Figures 6 and 7.

ACCELERATION ERROR

A tracking converter employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{\text{Input Acceleration}}{\text{Error in Output Angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration, only the error due to acceleration, maximum acceleration is in the region of 5 times the K_a figure. The following is an example using the K_a of the SDC1740.

Acceleration of 50 revolutions sec^{-2} with $K_a = 56000$

$$\text{Error in LSBs} = \frac{50 \times 16384}{56000} = 14.62\text{LSBs}$$

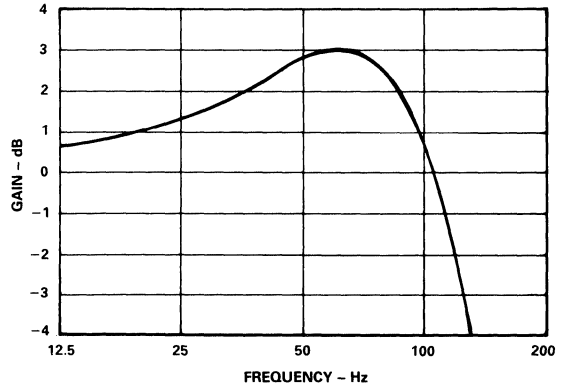


Figure 4. SDC/RDC1740 Gain Plot

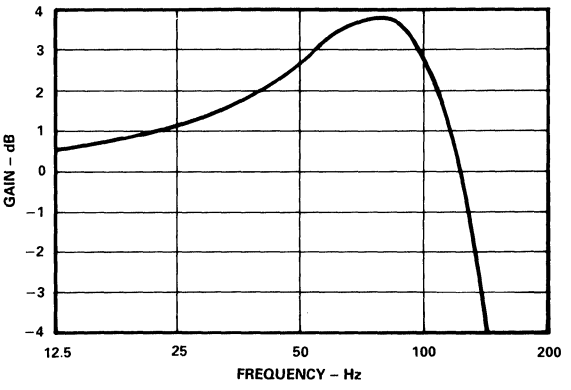


Figure 6. SDC/RDC1741/1742 Gain Plot

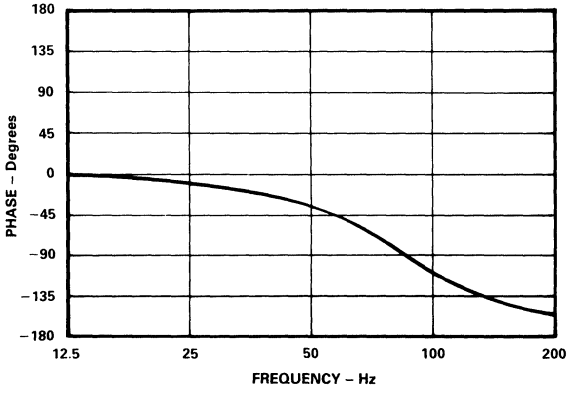


Figure 5. SDC/RDC1740 Phase Plot

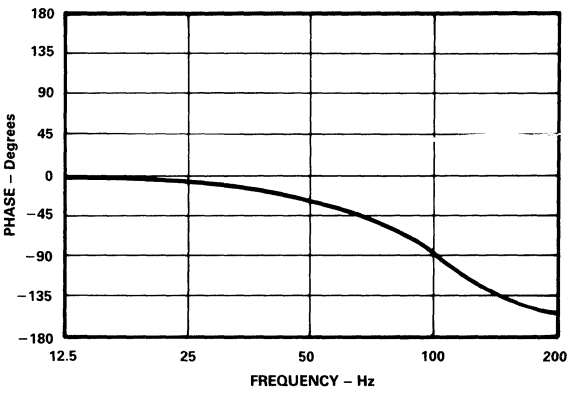


Figure 7. SDC/RDC1741/1742 Phase Plot

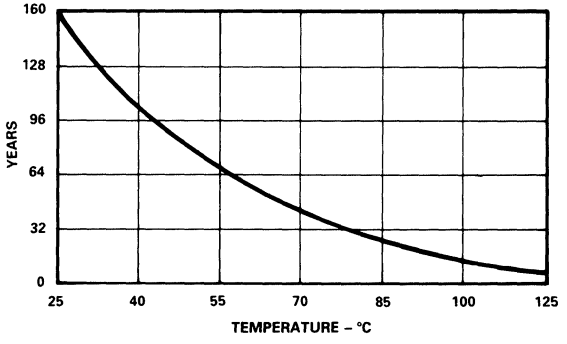


Figure 8. SDC/RDC1740/41/42 MTBF Curve

RELIABILITY

The reliability of these products is very high due to the extensive use of custom chip circuits that decrease the active component count. Calculations of the MTBF figure under various environmental conditions are available on request.

As an example of the Mean Time Between Failures (MTBF) calculated according to MIL-HDBK-217E, Figure 8 shows the MTBF in years versus case temperature in naval sheltered conditions for SDC/RDC1740/41/42.

STANDARD PROCESSING (5YZ OPTION)

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Conditions
1. Preseal Burn In	64 hrs at +125°C
2. Precap Visual Inspection	In-house criteria
3. Seal Test, Fine and Gross	In-house criteria
4. Final Electrical Test	Performed at +25°C
Extended temperature range versions receive additional processing as follows:	
Final Electrical Test	Performed at max and min operating temperatures

PROCESSING FOR HIGH RELIABILITY

Process	Conditions
1. Preseal Burn In	64 hrs at +125°C
2. Precap Visual Inspection	2017
3. Temperature Cycling	10 Cycles, −65°C to +150°C
4. Constant Acceleration	5000G, Y1 Plane
5. Interim Electrical Tests	
6. Operating Burn In	96 hours @ +125°C
7. Seal Test, Fine and Gross	1014
8. Final Electrical Testing (Group A)	Performed at T_{min}, $T_{ambient}$ and T_{max}
9. External Visual Inspection	2009

NOTE
Test and screening data can be supplied. Further information on request.

OTHER PRODUCTS

Many other hybrid products concerned with the conversion of synchro data are manufactured by Analog Devices, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The *SDC/RDC1767* and SDC/RDC1768 are hybrid synchro-to-digital converters with isolating microtransformers similar to the SDC/RDC1740/41/42 described on this data sheet with the additional features of analog velocity output and dc error output.

The *OSC1758* is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts, over a frequency range of 0 to 10kHz.

The *DRC1745* and *DRC1746* are 14- and 16-bit natural binary latched output hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc mins, and the outputs can supply 2VA at 7V rms.

ORDERING INFORMATION

For full definition, the converter part number should be suffixed by an option code. All the standard options and their option codes are shown below. For options not shown, please consult Analog Devices.

SDC 174A X Y Z B

- B — High-Rel Processing
- Z — Signal / Reference / Synchro
  - Z=1 Signal 11.8V Reference 26V Synchro
  - Z=2 Signal 90V Reference 115V Synchro
  - Z=3 Signal 11.8V Reference 11.8V Resolver
  - Z=4 Signal 26V Reference 26V Resolver
  - Z=8 Signal 11.8V Reference 26V Resolver
- Y — Reference Frequency
  - Y=1 400Hz Reference Frequency
  - Y=4 2.6kHz Reference Frequency
- X — Operating Temperature Range
  - X=4 −55°C to +125°C Operating Temperature Range
  - X=5 0 to +70°C Operating Temperature Range
- 174A — Resolution / Accuracy
  - 1740=14-Bit Resolution, ±5.3 arc min Accuracy
  - 1741=12-Bit Resolution, ±15.3 arc min Accuracy
  - 1742=12-Bit Resolution, ±8.5 arc min Accuracy
- SDC — Synchro-to-Digital Converter / RDC=Resolver-to-Digital Converter

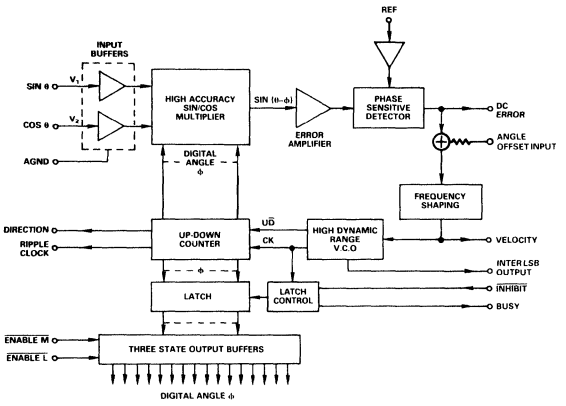
Tachogenerator Output, Hybrid Resolver-to-Digital Converters

1S14/1S24/1S44/1S64

FEATURES
40-Pin Hybrid
Tachogenerator Velocity Output
DC Error Output
Sub LSB Output
Angle Offset Input
Reference Frequency of 2kHz to 10kHz
Logic Outputs for Extension Pitch Counter

APPLICATIONS
Numerical Control of Machine Tools
Feed Forward Velocity Stabilizing Loops
Robotics
Closed Loop Motor Drives
Brushless Tachometry
Single Board Controllers

1S14/1S24/1S44/1S64 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 1SN4* are hybrid devices that convert standard resolver inputs to digital position and analog velocity outputs. All the essential features for multiturn or multipitch operation are included for numerically controlled machine tool and velocity feedback applications.

Typically the input signals would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1SN4 ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway.

A unique feature of the converter is its internally generated tachogenerator velocity output offering a linear voltage-speed relationship. Only one external resistor is required to scale the velocity output to the users chosen volts/rpm relationship.

Repeatability is 1LSB under constant temperature conditions.

Four resolutions are available all operating over a frequency range of 2kHz to 10kHz.

1S14 is 10-bit up to 40,800 revolutions per minute.
1S24 is 12-bit up to 10,200 revolutions per minute.
1S44 is 14-bit up to 2,550 revolutions per minute.
1S64 is 16-bit up to 630 revolutions per minute.

*N is 1, 2, 4 or 6 depending upon resolution of model.

APPLICATIONS

The 1SN4 has been specifically designed for motor position control for the numerically controlled machine and robot industry, using the type 2 servo loop tracking principle that ideally suits these converters to the electrically noisy environment found in these industrial applications.

USER BENEFITS

Allows both velocity and position measurement from a single, low cost, standard, brushless resolver.

80dB dynamic range of velocity output.

0.5% ripple on velocity signal.

0.1% linearity of velocity signal.

Cost effective tachogenerator replacement.

Tracks at 5 to 10 times the rate of equivalent resolution encoders.

Analog output for interpolation between digital codes.

Direction and Ripple Clock (Datum) outputs facilitate revolution counting.

Hybrid construction offering small size and MTBF of >200 years at 50°C GB.

SPECIFICATIONS (typical for both commercial (5Y0) and extended (4Y0) temperature range options @ 25°C and ±15V or ±12V power supplies, unless otherwise noted)

Models / Parameters		1S14	1S24	1S44	1S64	Units
RESOLVER INPUTS						
Signal Voltage		2.0 ± 5%	*	*	*	V rms
Reference Voltage		2.0 + 50%/ – 20%	*	*	*	V rms
Signal & Reference Frequency		2k–10k	*	*	*	Hz
Signal Input Impedance		10(min)	*	*	*	MΩ
Reference Input Impedance		125	*	*	*	kΩ
Allowable Phase Shift (Signal to Reference)		±10	*	*	*	Degrees
POSITION OUTPUT						
Resolution		10	12	14	16	Bits
1LSB		0.35	0.088	0.022	0.0055	Degrees
Accuracy (max error over temp. range)	5Y0	±25.0(0.42)	±8.5(0.14)	±5.3(0.09)	±4.0(0.07)	Arc-mins (degrees)
		±0.12	±0.04	±0.025	±0.019	% F.S.
	4Y0	±25.0(0.42)	±8.5(0.14)	±5.3(0.09)	±2.6(0.04)	Arc-mins (degrees)
		±0.012	±0.04	±0.025	±0.012	% F.S.
Digital Position Output Format		Parallel natural binary	*	*	*	
Load		6(max)	*	*	*	LSTTL
Monotonicity		Guaranteed	*	*	*	
Repeatability		1	*	*	*	LSB
DATA TRANSFER						
Busy Output		Logic "Hi" when Busy	*	*	*	
Load		6(max)	*	*	*	LSTTL
Busy Width		380(min) 530(max)	*	*	*	ns
$\overline{\text{ENABLE}}$ Inputs		Logic "Lo" to Enable	*	*	*	
Load		1	*	*	*	LSTTL
Enable & Disable Times		250(max)	*	*	*	ns
$\overline{\text{INHIBIT}}$ Input		Logic "Lo" to Inhibit	*	*	*	
Load		1	*	*	*	LSTTL
Direction Output (DIR)		Logic "Hi" when counting up, Logic "Lo" when counting down.	*	*	*	
Load		6(max)	*	*	*	LSTTL
Ripple Clock (RC)		Negative pulse indicating when internal counters change from all "1's" to all "0's" or vice versa.	*	*	*	
Load		6(max)	*	*	*	LSTTL
Width		1μ(max) 850n(min)	*	*	*	Secs
DYNAMIC CHARACTERISTICS						
Tracking Rate (min)						
with ±15V supplies		40,800	10,200	2,550	630	rpm
with ±12V supplies		34,680	8,670	2,168	536	rpm
Acceleration Constant Ka		220,000	*	*	*	Sec^{-2}
Settling time (179° step input)		25(max)	35(max)	60(max)	120(max)	ms
Bandwidth		230	*	*	*	Hz
VELOCITY OUTPUT						
Polarity		Positive for increasing angle	*	*	*	
Tachogenerator Voltage Scaling		0.25	1	4	16	V/K rpm
Scale Factor Accuracy		±1(max)	*	*	*	% of output
Scale Factor Tempco		200(max)	*	*	*	ppm/°C
Reversion Error		±0.2(max)	*	*	*	%
Reversion Error Tempco		50(max)	*	*	*	ppm/°C
Linearity		0.1	*	*	*	% of output
Over full temp range		0.25(max)	*	*	*	% of output
Ripple and Noise						
Steady State @10kHz (200Hz b/w)		100	150	300	1300	μV rms
Dynamic Ripple (av-pk)		0.5(max)	*	*	*	% of output
Zero Offset		±500	*	*	*	μV
Zero Offset Tempco		50(max)	*	*	*	μV/°C
Output Load		5(min)	*	*	*	kΩ

Models Parameters	1S14	1S24	1S44	1S64	Units
SPECIAL FUNCTIONS					
DC Error Output Voltage	450	*	*	*	mV/degree
Inter LSB Output	±1 (±20%)	*	*	*	V/LSB
Load	1 (min)	*	*	*	kΩ
Angle Offset Input (over operating temperature range)	320 (±10%)	*	*	*	nA/LSB
Maximum Input	32	*	*	*	LSB
POWER REQUIREMENTS					
Power Supplies					
$\pm V_S$	±15 (±5%) or ±12 (±5%)	*	*	*	V dc
+5V	+4.75 to +5.25	*	*	*	V dc
Power Supply Consumption					
$\pm V_S$	30 (max)	*	*	*	mA
+5V	125 (max)	*	*	*	mA
Power Dissipation	1.5 (max)	*	*	*	W
TEMPERATURE RANGE					
Operating 5Y0 option	0 to +70	*	*	*	°C
4Y0 option	−55 to +125	*	*	*	°C
Storage 5Y0 option	−55 to +125	*	*	*	°C
4Y0 option	−60 to +150	*	*	*	°C
DIMENSIONS					
5Y0 option	2.1″ × 1.1″ × 0.195 (5.3 × 28 × 4.95)	*	*	*	Inches (mm)
4Y0 option	2.14″ × 1.14″ × 0.18 (54.4 × 29 × 4.6)	*	*	*	Inches (mm)
WEIGHT	1 (28)	*	*	*	oz. (grms)

NOTES
*Specifications same as 1S14.
Specifications subject to change without notice.

5

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +17V dc
$-V_S$[1]	0V to −17V dc
+5V[2]	0V to +6.0V dc
Reference	±17V dc
Sine	±17V dc
Cosine	±17V dc
Any Logical Input	−0.4V to +5.5V dc

CAUTION:
1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

OPERATION OF THE CONVERTER

The 1SN4 are tracking converters, this means that the output automatically follows the input for speeds up to the maximum tracking rate for the resolution option. No convert command is necessary as the conversion is initiated by each LSB increment for the input. Each LSB increment of the converter initiates a BUSY pulse.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

The static angular accuracy quoted for each converter type is the worst case error that can occur over the full operating temperature range with the following input conditions:

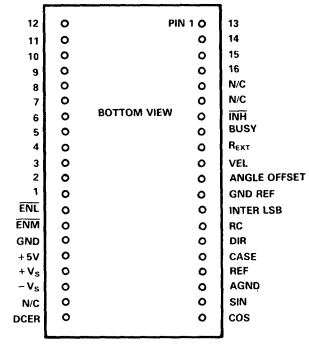
a) Signal input amplitudes within 5% of the nominal values.
b) Signal and reference frequency within the specified operating range.
c) Phase shift between signal and reference less than 10 degrees.
d) Signal and reference waveform harmonic distortion less than 10 percent.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice the converters can be used well outside these operating conditions providing the following points are observed:

Signal Amplitude (Sine and Cosine Inputs)
The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the analog outputs and inputs of the converter such as velocity, inter LSB position and angle offset.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the factor Ka is proportional to signal level.

PIN CONNECTIONS



NOTES
1. "R_{EXT}" SHOULD BE CONNECTED TO "VEL" WHEN NO SCALING REQUIRED.
2. CASE PIN CONNECTED ON 460 OPTION ONLY.

Signal and Reference Frequency
Any frequency within the specified range of the converter may be used. It should be noted that the same frequency must be used on both inputs.

Reference Voltage Level
The amplitude of the reference signal applied to the converter's input is very uncritical, however it is essential that the zero crossing points are maintained in the correct place to drive the converter's phase sensitive detector.

Harmonic Distortion
The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square and triangle waveforms can be used but the input levels should be adjusted so that the average value after rectification is 1.9 volts. (For example – a square wave should be 1.9V peak).

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

Phase Shift (Between Signal and Reference)
See Section on "Dynamic Accuracy vs. Resolver Phase Shift".

DATA TRANSFER

BUSY Output:
The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of an LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input:
The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

Note: With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

$\overline{\text{ENABLE}}$ Inputs:
Two $\overline{\text{ENABLE}}$ inputs are provided, $\overline{\text{ENABLE M}}$ for the most significant 8-bits and $\overline{\text{ENABLE L}}$ for the least significant remainder. These $\overline{\text{ENABLES}}$ determine the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins. The operation of these $\overline{\text{ENABLES}}$ has no effect on the conversion process.

Two methods are available for transferring data, by using the inputs and outputs described.

One method is to transfer data when the BUSY is in a "Lo" state or clock the data out on the trailing edge of the BUSY pulse. Both the $\overline{\text{INHIBIT}}$ and the $\overline{\text{ENABLES}}$ must be in their correct state of "Hi" and "Lo's" respectively.

The alternative method is to use the $\overline{\text{INHIBIT}}$ input. Data will always be valid one microsecond after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied.

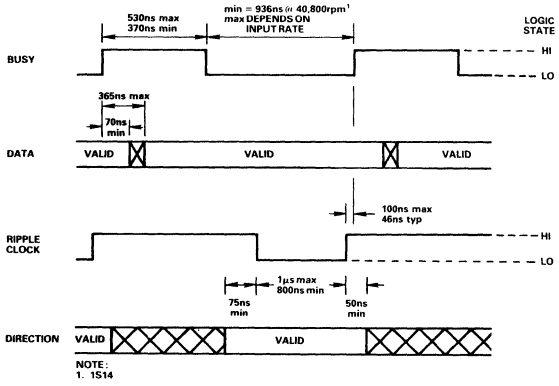


Figure 1. Timing Diagram

RIPPLE CLOCK (RC) and DIRECTION (DIR) Outputs:
As the digital output of the converter passes through the major carry, i.e. all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The DIRECTION (DIR) logic output indicates the direction of input rotation and this data is always valid in advance of the RIPPLE CLOCK pulse, and stays valid until the direction changes (see Timing Diagram – Figure 1).

These two logic outputs are provided so that the user can count the input revolutions or pitches. An external extension counter is required. Figure 7 shows the application circuit which should be used to perform this counting function.

Note: CMOS external counters can be used (see Figure 2) but it is not advisable as great care must be taken to keep stray capacitances low because of the high tracking rate of the converter.

VELOCITY OUTPUT
The tracking conversion technique produces an internal signal at the input to the voltage controlled oscillator (VCO) that is proportional to the rate of the input angle. In the 1SN4 series additional circuitry is included to linearize this signal, which is closely characterized, producing a high quality tachogenerator velocity output at the VELOCITY (VEL) pin.

This analog tachogenerator velocity output is resistively scaled internally to give a full scale output of ±10V dc at the specified tracking rate for the converter.

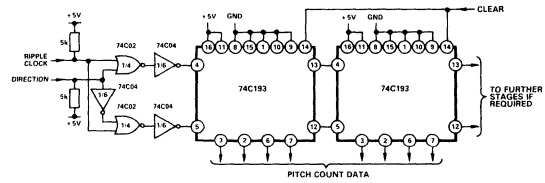


Figure 2. CMOS External Counter

However, a full scale output of ±10V dc can be obtained for lower speeds by changing the gain of the internal scaling amplifier using only one external resistor. The external resistor, R_{EXT}, should be connected between "R_{EXT}" pin and the GND REF pin, and calculated using the following equation.

$$R_{EXT} = \frac{10 \times A}{B - A}\ k\Omega$$

Where A = required rps to be represented by ±10V FS

and B = specified rps for the converter.

Note: A cannot be greater than B and for unity gain "VEL" and "R_{EXT}" pins should be linked (no external resistor required).

When the external resistor facility is used to provide large magnifications there is an additional velocity output offset generated due to the inevitable common ground impedance inherent with a single ground connection point. While these offsets will still be in spec, they can be code dependent. They can be minimized by taking the external scaling resistor from "R_{EXT}" to GND REF instead of "GND". This means that the velocity output will be unaffected by the varying current drawn from the +5V supply as the digital output changes.

Ripple and noise on the velocity signal consists of two components – steady state noise and dynamic noise.

Steady state noise – this is internally generated noise produced by the converter's circuitry and is the only noise signal present under static input conditions.

Dynamic noise – this is the noise produced, in addition to steady state noise, under dynamic operating conditions.

The two main components of the dynamic noise signal are due to the "non-zero" angular error of the resolver/converter combination. The figures given in the specification are typical for a size 11, 7 arc-minutes, brushless resolver.

It should be noted that when operating at low tracking rates it is critical to maintain the signal input voltage at its nominal value in order to keep the noise level on the velocity signal to an absolute minimum. The effect of variation in signal voltage at low tracking rates is to produce low energy spikes on the velocity output on the rising edge of the BUSY pulse. The amplitude of these spikes will be in the region of 30µV per percent variation in signal input voltage level.

Note: The velocity signal output and max tracking rate derates by 15% (max) for operation with ±12 volt power supplies.

SPECIAL FUNCTIONS

DC Error: The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converters are a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason. It is therefore an indication that the input has exceeded the maximum tracking rate of the converter, or, due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test".

INTER LSB Output: In order to overcome the "free play" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of the digital angle output.

The output is therefore proportional to the inter LSB resolved position with a maximum output representing 1LSB.

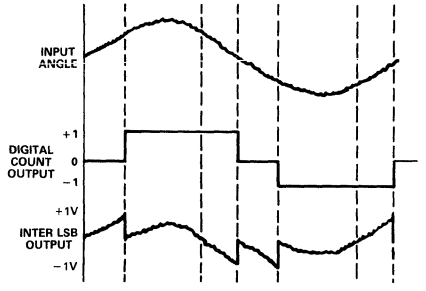


Figure 3

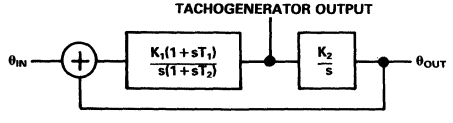
Figure 3 illustrates how the INTER LSB output compensates for the instances where, due to hysteresis, there is no change in the digital count output for 1LSB change in input angle. The sum of the digital count output and INTER LSB output equals the actual input angle.

ANGLE OFFSET Input: A unique feature of the 1SN4 series of converter is their angle offset input which allows the user to electrically "rotate" the input shaft of the resolver.

Injecting a current of 320nA into the angle offset input pin will offset the digital output of the converter by 1LSB relative to the angle defined by the resolver inputs. It is recommended that an offset equivalent to no greater than 30LSB's be applied to this input.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Positional Transfer Function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_1K_2}{s^2} \cdot \frac{1 + sT_1}{1 + sT_2} \text{ Open Loop}$$

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + \frac{s^2}{K_1K_2} + \frac{s^3T_2}{K_1K_2}} \text{ Closed Loop}$$

where $K_1K_2 = K_a$

Tachogenerator Transfer Function:

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{K_1(1 + sT_1)}{s(1 + sT_2)} \text{ Open Loop}$$

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{s(1 + sT_1)}{K_2(1 + sT_1) + \frac{s^2}{K_1} + \frac{s^3T_2}{K_1}}$$

Closed Loop

Where: $K_1 = 3.23$
$K_2 = 68.2 \times 10^3$
$K_a = 220 \times 10^3$
$T_1 = 4.46\text{ms}$
$T_2 = 0.21\text{ms}$

Refer: Figures 4 and 5

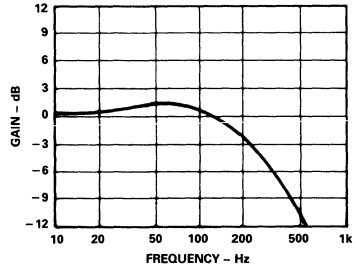


Figure 4. Gain Plot

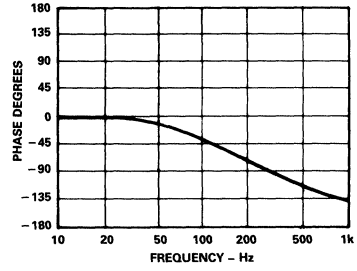


Figure 5. Phase Plot

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Under static operating conditions phase shift between signal and reference lines theoretically does not effect the converter's static accuracy.

However, when rotating, most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

Note: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

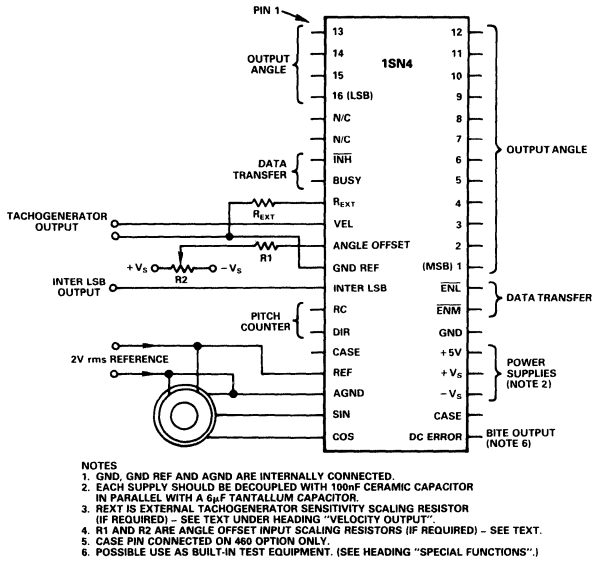


Figure 6. Electrical Connections

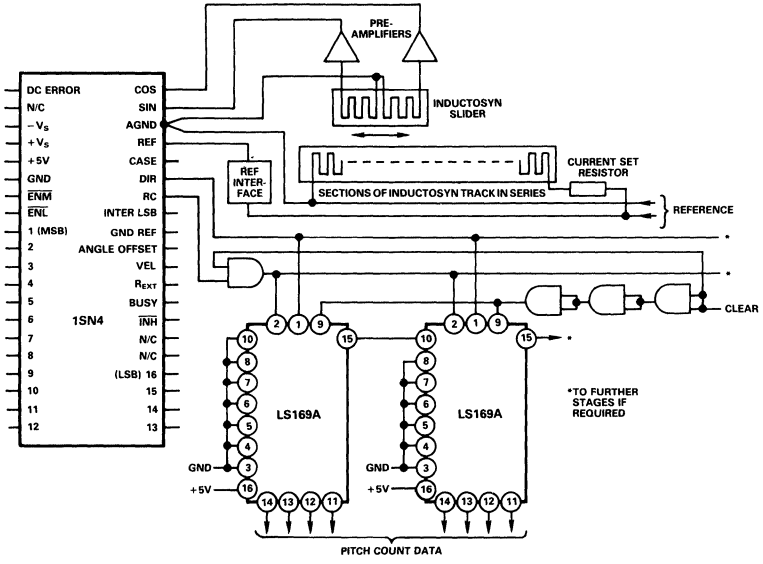


Figure 7. Connections for Use with Inductosyn/"LS" External Counters

CONNECTING THE CONVERTER

The electrical connection of the converter is straight-forward. The power supply voltages connected to $+V_S$ and $-V_S$ pins can be $\pm 12V$ to $\pm 15V$ but must not be reversed. The $+5V$ supply connects to the $+5V$ pin and should not be allowed to become negative with respect to the GND pin.

It is suggested that decoupling capacitors are connected in parallel between the power lines ($+V_S$, $-V_S$ and $+5V$) and GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The converter has some H/F decoupling provided internally, as well as input protection on the signal and reference inputs.

The resolver connections are made to the sine and cosine inputs, reference and analog ground as shown in the electrical connection diagram (Figure 6).

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

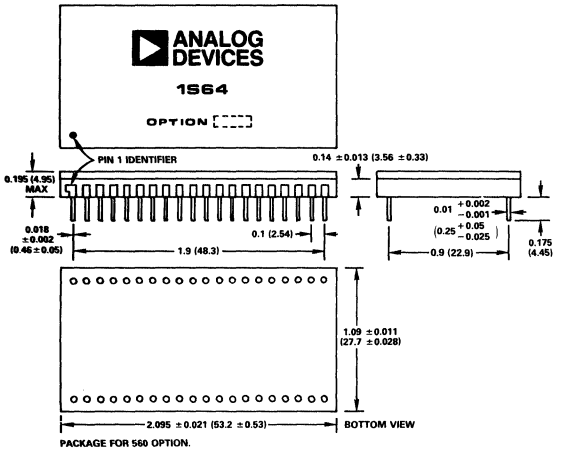
HIGH REL PROCESSING

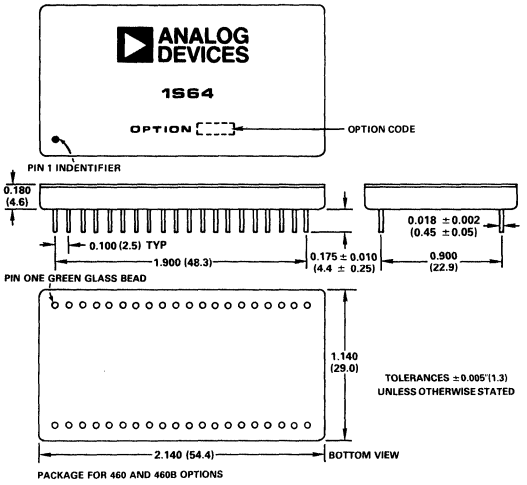
All models ordered to high reliability requirements will be identified with a B suffix, and will have received the following processing:

1. Internal visual inspection
2. Stabilization bake, 24 hours at 150°C
3. Temperature cycling, −65°C to +150°C
4. Constant acceleration, 5000g
5. Powered burn-in, 160 hours at 125°C
6. Final electrical test at T_{MIN} and T_{MAX}
7. Seal test, fine and gross
8. External visual inspection

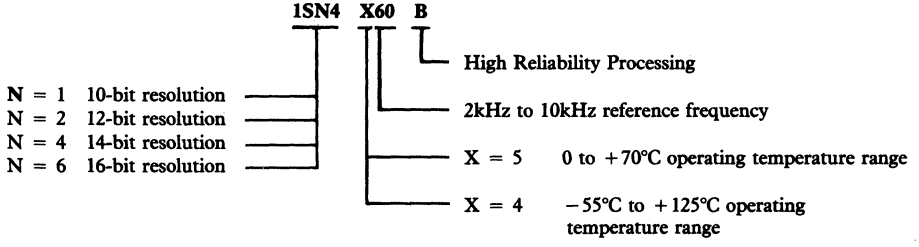
OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).





ORDERING INFORMATION



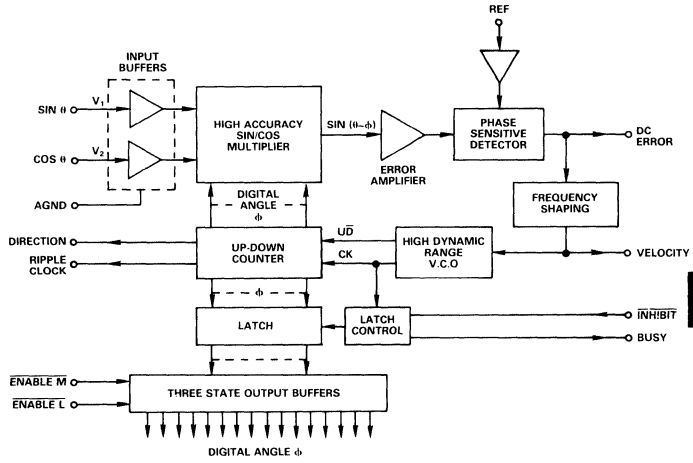
Hybrid, Tracking Resolver-to-Digital Converters

1S20/1S40/1S60/1S61

FEATURES
Low Cost
32-Pin Hybrid
High Tracking Rate 170rps at 12 Bits
Velocity Output
DC Error Output
Logic Outputs for Extension Pitch Counter

APPLICATIONS
Numerical Control of Machine Tools
Robotics

1S20/1S40/1S60/1S61 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The 1S20/40/60/61 are a series of low cost hybrid converters with a high tracking rate and all essential features for numerically controlled machine applications. These converters are housed in a 32-pin triple DIP ceramic package measuring 1.1″ × 1.7″ × 0.205″ (28 × 43.2 × 5.2mm).

The 1S20/40/60/61 convert resolver format input signals into a parallel natural binary digital word. Typically, these signals would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1S20/40/60/61 series ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital* highway. In this series there are 12-, 14- and two 16-bit resolution (±4 arc mins and ±10 arc mins accuracy) models available.

Repeatability is 1LSB for all models under constant temperature conditions.

The 1S20/40/60/61 are available with three frequency options covering the range 400Hz to 10kHz.

Models Available

Four models are available in this range and three frequency options for each model.

1S20 is a 12-bit up to 170 revolutions per second
1S40 is a 14-bit up to 42.5 revolutions per second
1S60 is a 16-bit up to 10.5 revolutions per second
1S61 is a 16-bit up to 10.5 revolutions per second

APPLICATIONS/USER BENEFITS

The 1S20/40/60/61 has been specifically designed for the numerically controlled machine and robot industry. Using the type 2 servo loop tracking principle ideally suits these converters to the electrically noisy environment found in these industrial applications.

By using hybrid construction techniques, small size, low power and high reliability are further benefits offered by these converters. This small size with the three-state digital outputs makes these converters ideal for multichannel operation.

The layout of the connections simplifies the parallel connection to a digital highway.

The provision of the digital outputs of DIRECTION and RIPPLE CLOCK allow simple extension counters for multi-pitch operation to be implemented.

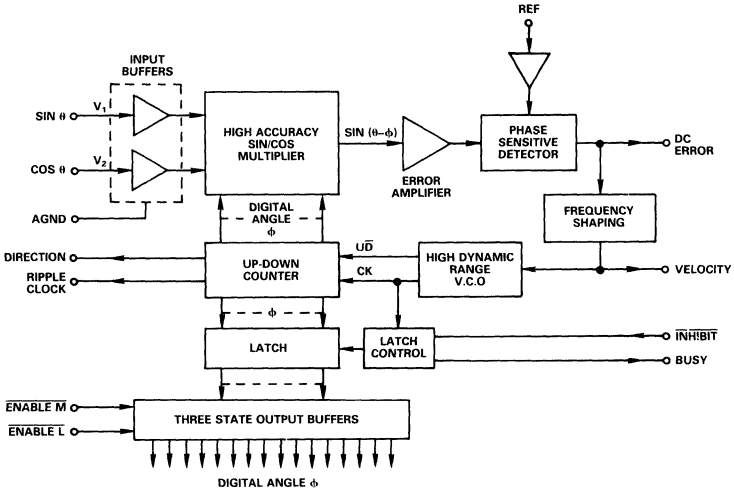
Analog outputs of velocity and dc error for control loop stabilization and bite (built in test) provide two more features required in these applications.

SPECIFICATIONS (typical @ +25°C, unless otherwise specified)

Models	1S20	1S40	1S60	1S61	Units
RESOLUTION	12	14	16	16	Bits
ACCURACY[1]	±8.5	±5.3	±4.0	±10	arc-mins
REPEATABILITY[2]	1	*	*	*	LSB
SIGNAL AND REFERENCE FREQUENCY[3]	400-10k	*	*	*	Hz
DIGITAL OUTPUT	Parallel natural binary				
Max Load	20	*	*	*	LSTTL
TRACKING RATE (min)					
400Hz–2.6kHz	50	12.5	3.0	3.0	rps
2.6kHz–5kHz	90	22.5	5.5	5.5	rps
5kHz–10kHz	170	42.5	10.5	10.5	rps
SETTLING TIME					
400Hz–2.6kHz	150	180	350	350	ms
2.6kHz–5kHz	40	50	130	130	ms
5kHz–10kHz	20	25	60	60	ms
ACCELERATION CONSTANT (K_a)					
400Hz–2.6kHz	9,500	*	*	*	sec^{-2}
2.6kHz–5kHz	144,000	*	*	*	sec^{-2}
5kHz–10kHz	713,000	*	*	*	sec^{-2}
SIGNAL VOLTAGE	2.0	*	*	*	V rms
SIGNAL INPUT IMPEDANCE	>10	*	*	*	MΩ
REFERENCE VOLTAGE	2.0	*	*	*	V rms
REFERENCE INPUT IMPEDANCE	125	*	*	*	kΩ
ALLOWABLE PHASE SHIFT[4]					
(Signal to Reference)	±10	*	*	*	Degrees
BUSY OUTPUT[5]	Logic "Hi" when Busy				
Max Load	20	*	*	*	LSTTL
BUSY WIDTH	430	*	*	*	ns
$\overline{\text{ENABLE}}$ INPUTS	Logic "Lo" to ENABLE				
Load	1	*	*	*	LSTTL
ENABLE AND DISABLE TIMES	120(typ)	*	*	*	ns
	220(max)	*	*	*	ns
$\overline{\text{INHIBIT}}$ INPUT	Logic "Lo" to INHIBIT	*	*	*	
Load	1	*	*	*	LSTTL
DIRECTION OUTPUT (DIR)[5]	Logic "Hi" when counting up Logic "Lo" when counting down				
Max Load	20	*	*	*	LSTTL
RIPPLE CLOCK[5]	Negative pulse indicating when internal counters change from all "1's" to all "0's" or vice versa.				
Max Load	20	*	*	*	LSTTL
VELOCITY OUTPUT[6] (at specified min tracking rate).					
Polarity	positive for increasing angle	*	*	*	–
Output Voltage[7]	±10	*	*	*	V dc
Accuracy	±10	*	*	*	% FSD
Zero Offset	±8	*	*	*	mV
DC ERROR OUTPUT VOLTAGE[6]	40	10	2.5	2.5	mV/LSB
POWER SUPPLIES					
$+V_S$	+11.5 to +16	*	*	*	V
$-V_S$	−11.5 to −16	*	*	*	V
+5V	+4.75 to +5.25	*	*	*	V
POWER SUPPLY CONSUMPTION[7]					
$+V_S$	20, 30 (max)	*	*	*	mA
$-V_S$	20, 30 (max)	*	*	*	mA
+5V	105, 125 (max)	*	*	*	mA
POWER DISSIPATION[7]	1.1, 1.5 (max)	*	*	*	W
TEMPERATURE RANGE					
Operating	0 to +70	*	*	*	°C
Storage	−55 to +125	*	*	*	°C
PACKAGE OPTION[8]	DH-32E	*	*	*	
WEIGHT	1(28)	*	*	*	oz. (grms)

NOTES
[1]Specified over the operating temperature range and for:
a). ±10% signal and reference amplitude variation.
b). 10% signal and reference harmonic distortion.
c). ±10% on frequency range of option.
[2]Specified at constant temperature. Over the operating temperature range, worst case repeatability could be up to 1.5 arc mins for all models.
[3]See frequency range options.
[4]For no additional error with a static input, see "Dynamic Accuracy vs. Resolver Phase Shift"
[5]See timing diagram.
[6]These outputs should be connected via buffers or comparator inputs (max load 100pF).
[7]$\pm V_S = \pm 15$ volts.
[8]See Section 14 for package outline information.
*Specifications same as 1S20.
Specifications subject to change without notice.

FUNCTIONAL DIAGRAM



BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0440
14	0.0220
15	0.0110
16	0.0055

5

THEORY OF OPERATION

The sine and cosine signals are applied to the signal input.

$$V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$$
$$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$$

Where θ is the angle of the resolver shaft or the distance through a particular pitch of the Inductosyn™.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$$
and $$K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$$

These signals are subtracted by the error amplifier to give:

$$K' E_O \text{ Sin } \omega t \text{ (Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$$
or $$K' E_O \text{ Sin } \omega t \text{ Sin } (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ), equals, within the rated accuracy of the converter, the resolver shaft angle θ.

OPERATION OF THE CONVERTER

The 1S20/40/60/61 are tracking converters, this means that the output automatically follows the input for speeds up to the maximum tracking rate for the frequency option specified. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

As the digital output of the converter passes through the major carry; i.e., all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is *always* valid in advance of a RIPPLE CLOCK pulse.

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

Two $\overline{\text{ENABLE}}$ inputs are provided, $\overline{\text{ENABLE M}}$ for the Most Significant 8 bits and $\overline{\text{ENABLE L}}$ for the Least Significant remainder. The operation of these enables has no effect on the conversion process.

The tracking conversion technique produces an internal signal at the input to the VCO that is proportional to the rate of the input angle. This is a bipolar dc analog signal that is made available at the VELOCITY (VEL) pin. As this is an internal control signal it is not closely characterized.

The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converter is a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason, it is therefore an indication that the input has exceeded the maximum tracking rate of the converter or due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test".

NOTE: The DC ERROR voltage has no internal filtering.

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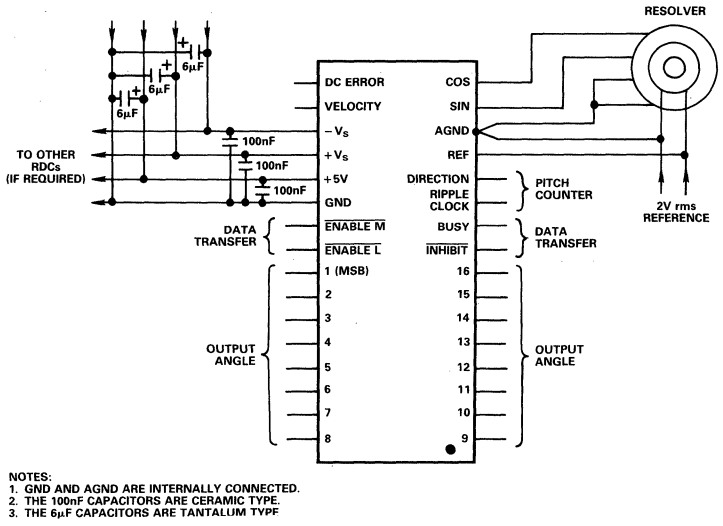


Figure 1. Electrical Connections

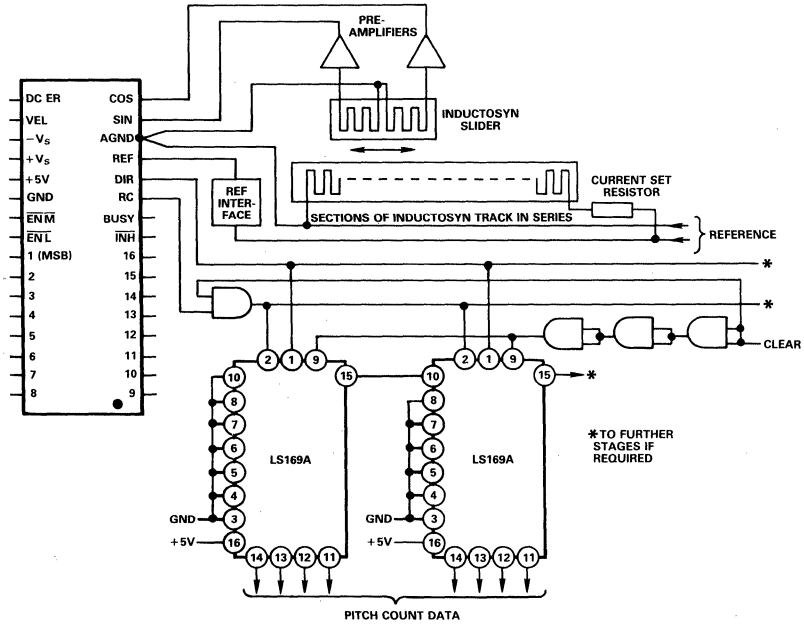


Figure 2. Connections for Use with Industosyn/"LS" External Counters

CONNECTING THE CONVERTER

The electrical connection of the converter is straight-forward. The power supply voltages connected to $+V_S$ and $-V_S$ pins can be $\pm 12V$ to $\pm 15V$ but must not be reversed. The $+5V$ supply connects to the $+5V$ pin and should not be allowed to become negative with respect to the GND pin.

It is suggested that decoupling capacitors of 100nF are connected in parallel between the power lines ($+V_S$, $-V_S$ and $+5V$) and GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter (refer to Figure 1).

The converter has some H/F decoupling provided internally, as well as input protection on the signal and reference inputs.

The resolver connections are made to the sine and cosine inputs, reference and analog ground as shown in the electrical connection diagram (Figure 1).

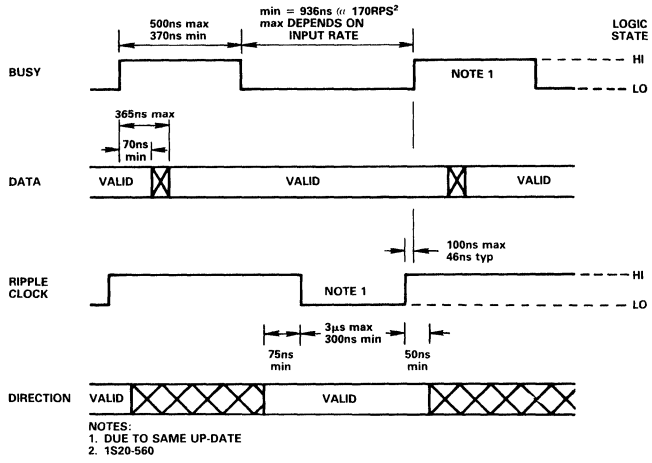


Figure 3. Timing Diagram

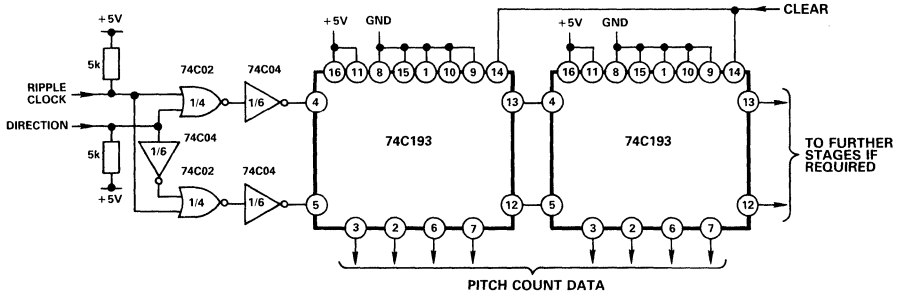


Figure 4. CMOS External Counter

DATA TRANSFER

The readiness of the converter for data transfer is given by the state of the BUSY output. The signal appearing on the BUSY output pin is a series of pulses of TTL levels when the angular input of the converter is changing. A BUSY pulse is initiated each time the input moves by an LSB and the internal counter is incremented or decremented. With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

The $\overline{\text{ENABLE}}$ input pin determines the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins.

From the above it can be seen that there are two methods available for transferring data.

One method is to transfer data when the BUSY is in a "Lo" state or clock the data out on the trailing edge of the BUSY pulse. Both the $\overline{\text{INHIBIT}}$ and the $\overline{\text{ENABLES}}$ must be in their correct state of "Hi" and "Lo's" respectively.

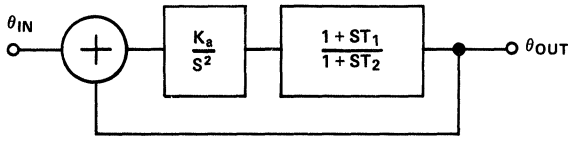
The alternative method is to use the $\overline{\text{INHIBIT}}$ input. Data will always be valid one microsecond after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied.

In order to count input revolutions or pitches, an external extension counter is required. A circuit performing this function is shown in Figure 2.

The DIRECTION (DIR) and RIPPLE CLOCK (RC) logic outputs should always be used in the manner shown in the application circuit. We recommend the circuit in Figure 2 to be used as the circuit in Figure 4 uses CMOS and great care must be taken to keep the stray capacitances low because of the high tracking rate of the converter.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1 + ST_1}{1 + ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3 T_2}{K_a}}$$

1S20/1S40/1S60/1S61 (typical values)

Constant \ Option	510	550	560
K_a	9,500	144,000	713,000
T_1	17.4ms	4.1ms	1.85ms
T_2	2.6ms	0.6ms	0.25ms
Gain Plot	Figure 5	Figure 7	Figure 9
Phase Plot	Figure 6	Figure 8	Figure 10

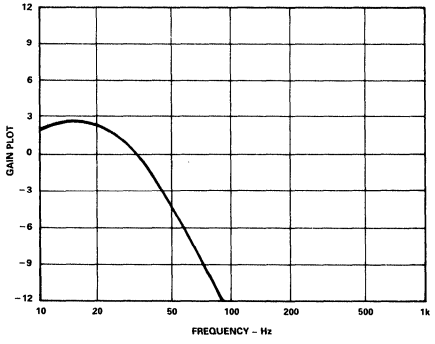


Figure 5

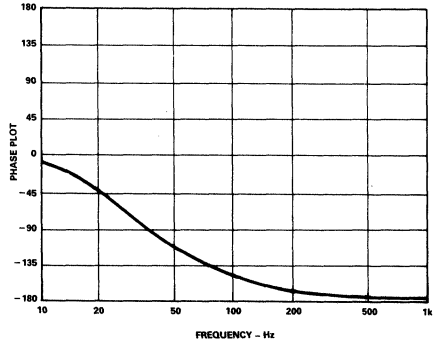


Figure 6

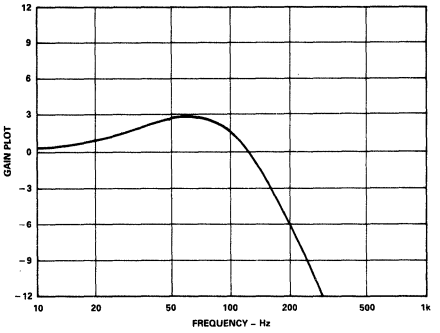


Figure 7

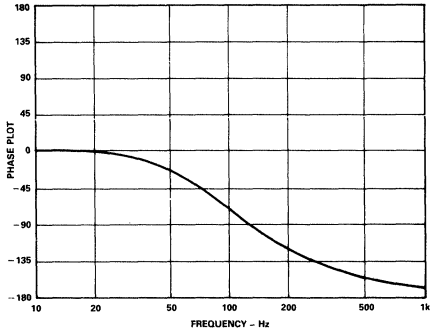


Figure 8

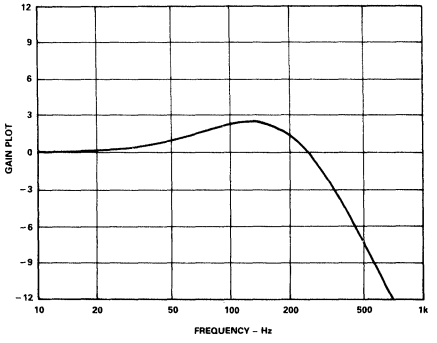


Figure 9

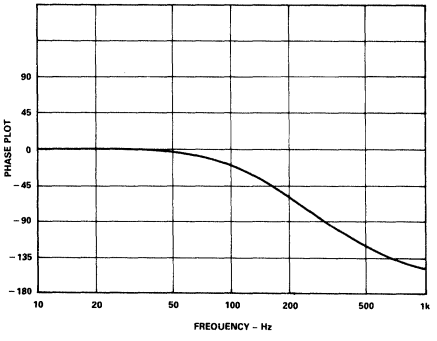


Figure 10

ACCELERATION ERROR

A tracking converter like the 1S20 employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{\text{Input acceleration}}{\text{Error in output angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration only the error due to acceleration, maximum acceleration is in the region of 10 times the K_a figure (deg/sec^2).

An example using the K_a of the 1S60/560

Acceleration of 33 revolutions sec^{-2} with K_a = 713,000

Additional error = 1 arc-min

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

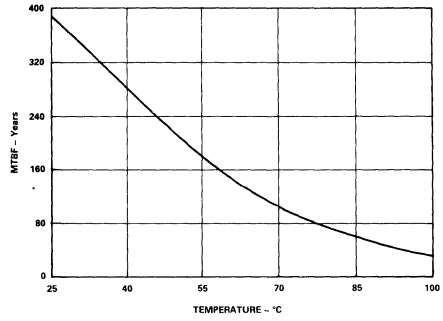
As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

MEAN TIME BETWEEN FAILURES (MTBF)

The reliability of these products is very high due to the extensive use of custom chip circuitry. For details of MTBF figures under particular conditions please consult the factory.

The graph below shows the typical variation of MTBF with temperature for the 1S20, under ground benign environment.



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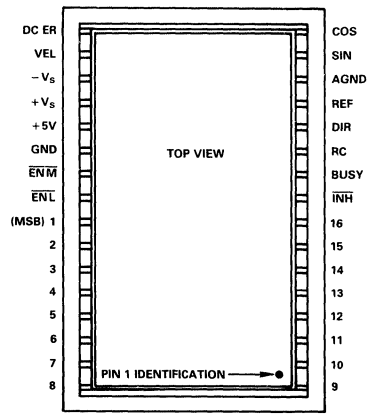
ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +17V dc
$-V_S$[1]	0V to −17V dc
$+5V$[2]	0V to +7.0V dc
Reference	±17V dc
Sine	±17V dc
Cosine	±17V dc
Any Logical Input	−0.4V to +5.5V dc

CAUTION:

1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

PIN CONFIGURATION



OTHER PRODUCTS

IRDC1732–	Inductosyn™/Resolver to Digital Converter (Hybrid)
IPA1751–	Inductosyn™ Pre-Amplifier
OSC1754–	Power Oscillator
OSC1758–	Power Oscillator (Hybrid)
IPA1764–	Inductosyn™ Pre-Amplifier (Hybrid)
MCI1794–	3 Channel Inductosyn™/Resolver to Digital Converter (Multibus Compatible Card)

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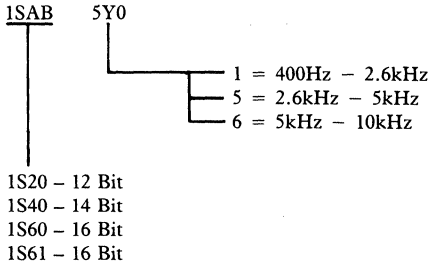
ORDERING INFORMATION



Tachogenerator Output, Variable Resolution, Hybrid, Resolver-to-Digital Converter

1S74

FEATURES
- **40-Pin Hybrid**
- **Tachogenerator Velocity Output**
- **User Selectable Resolution**
- **DC Error Output**
- **Sub LSB Output**
- **Angle Offset Input**
- **Reference Frequency of 2kHz to 10kHz**
- **Logic Outputs for Extension Pitch Counter**

APPLICATIONS
- **Numerical Control of Machine Tools**
- **Feed Forward Velocity Stabilizing Loops**
- **Robotics**
- **Closed Loop Motor Drives**
- **Brushless Tachometry**
- **Single Board Controllers**

GENERAL DESCRIPTION

The 1S74 is a hybrid device that converts standard resolver inputs to digital position and analog velocity outputs. All the essential features of multiturn or multipitch operation are included for numerically controlled machine tool and velocity feedback applications.

Typically, the input signal would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1S74 ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

In conjunction with the IPA1764 preamplifier, the 1S74 is also suitable for use with Inductosyns®.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway.

A unique feature of the converter is its internally generated tachogenerator velocity output offering a linear voltage-speed relationship. Only one external resistor is required to scale the velocity output to the user's chosen volts/rpm relationship.

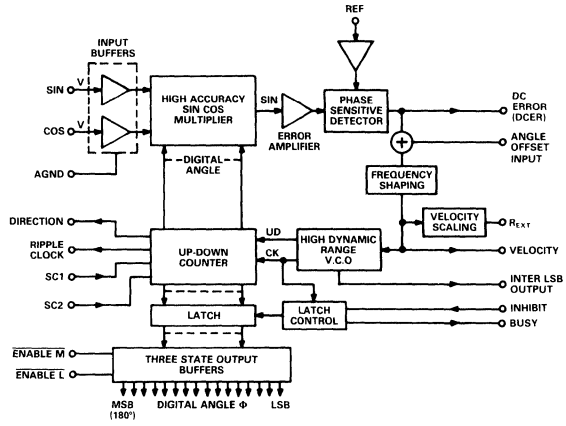
Repeatability is 1LSB under constant temperature conditions.

The resolution of the 1S74 converter is user selectable by means of applying a specific binary code to two of the converter's pins.

Four resolutions can be selected, all operating over a frequency range of 2kHz to 10kHz.

10 bit up to 40,800 revolutions per minute.
12 bit up to 10,200 revolutions per minute.
14 bit up to 2,550 revolutions per minute.
16 bit up to 630 revolutions per minute.

1S74 FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS

The 1S74 has been designed for motor position control in the CNC, robotic and military fields. The use of a type 2 tracking servo loop circuit with high inherent noise immunity, makes the product ideally suited to these applications.

USER BENEFITS

Allows both velocity and position measurement from a single, low cost, standard, brushless resolver.

80dB dynamic range of velocity output.

0.5% ripple on velocity signal.

0.1% linearity of velocity signal.

Cost effective tachogenerator/encoder replacement.

Tracks at 5 to 10 times the rate of equivalent resolution encoders.

Analog output for interpolation between digital codes.

Direction and Ripple Clock (Datum) outputs facilitate revolution counting.

Hybrid construction offering small size and MTBF of >200 years at 50°C GB.

MIL operating temperature range and spec. options available.

Inductosyn® is a registered trademark of Farrand Industries, Inc.

SPECIFICATIONS

(typical for both commercial (5YO) and extended (4YO) temperature range options @ 25°C and ±15V or ±12V power supplies, unless otherwise noted)

Resolution	10 Bits	12 Bits	14 Bits	16 Bits	Units
RESOLVER INPUTS					
Signal Voltage	2.0 (±5%)	*	*	*	V rms
Reference Voltage	2.0 (+50% −20%)	*	*	*	V rms
Signal & Reference Frequency	2k – 10k	*	*	*	Hz
Signal Input Impedance	10 (min)	*	*	*	MΩ
Reference Input Impedance	125	*	*	*	kΩ
Allowable Phase Shift (Signal to Reference)	±10	*	*	*	Degrees
POSITION OUTPUT					
Resolution	10	12	14	16	Bits
1LSB	0.35	0.088	0.022	0.0055	Degrees
Accuracy (maximum error over temperature range)					
5YO	±25.0 (0.42)	±8.5 (0.14)	±5.3 (0.09)	±4.0 (0.07)	arc-mins (degrees)
	±0.12	±0.04	±0.025	±0.019	% F.S.
4YO	±25.0 (0.42)	±8.5 (0.14)	±5.3 (0.09)	±2.6 (0.04)	arc-mins (degrees)
	±0.12	±0.04	±0.025	±0.012	% F.S.
Digital Position Output Format	Parallel natural binary	*	*	*	
Load	6 (max)	*	*	*	LSTTL
Monotonicity	Guaranteed	*	*	*	
Repeatability	1	*	*	*	LSB
DATA TRANSFER					
Busy Output	Logic "Hi" when busy	*	*	*	
Load	6 (max)	*	*	*	LSTTL
Busy Width	380 (min) 530 (max)	*	*	*	ns
ENABLE INPUTS	Logic "Lo" to enable	*	*	*	
Load	1	*	*	*	LSTTL
Enable & Disable Times	250 (max)	*	*	*	ns
INHIBIT INPUT	Logic "Lo" to inhibit	*	*	*	
Load	1	*	*	*	LSTTL
Direction Output (DIR)	Logic "Hi" when counting up, logic "Lo" when counting down.				
Load	6 (max)	*	*	*	LSTTL
Ripple Clock (RC)	Negative pulse indicating when internal counters change from all "1's" to all "0's" or vice versa.				
Load	6 (max)	*	*	*	LSTTL
Width	1μ (max) 850n (min)	*	*	*	secs
DYNAMIC CHARACTERISTICS					
Tracking Rate					
with ±15V Supplies	40,800 (min)	10,200 (min)	2,550 (min)	630 (min)	rpm
with ±12V Supplies	34,680 (min)	8,670 (min)	2,168 (min)	536 (min)	rpm
Acceleration Constant K_a	220,000	*	*	*	sec^{-2}
Settling Time (179° step input)	25 (max)	35 (max)	60 (max)	120 (max)	ms
Bandwidth	230	*	*	*	Hz
VELOCITY OUTPUT					
Polarity	Positive for increasing angle	*	*	*	
Tachogenerator Voltage Scaling	0.25	1.00	4	16	V/K rpm
Scale Factor Accuracy	±1 (max)	*	*	*	% of output
Scale Factor Tempco	200 (max)	*	*	*	ppm/°C
Reversion Error	±0.2 (max)	*	*	*	%
Reversion Error Tempco	50 (max)	*	*	*	ppm/°C
Linearity	0.1	*	*	*	% of output
Over Full Temperature Range	0.25 (max)	*	*	*	% of output
Ripple and Noise					
Steady State (200Hz B/W)	100	150	300	1300	μV rms
Dynamic Ripple (av-pk)	0.5 (max)	*	*	*	% of output
Zero Offset	±500	*	*	*	μV
Zero Offset Tempco	50 (max)	*	*	*	μV/°C
Output Load	5 (min)	*	*	*	KΩ

Resolution	10 Bits	12 Bits	14 Bits	16 Bits	Units
SPECIAL FUNCTIONS					
dc Error Output Voltage	450	*	*	*	mV/deg
Inter LSB Output	±1 (±20%)	*	*	*	V/LSB
Load	1k (min)	*	*	*	Ω
Angle Offset Input (over operating temperature range)	320 (±10%)	*	*	*	nA/LSB
Maximum Input	32	*	*	*	LSB
POWER REQUIREMENTS					
Power Supplies					
$\pm V_S$	±15 (±5%) or ±12 (±5%)	*	*	*	V dc
+5V	+4.75 to +5.25	*	*	*	V dc
Power Supply Consumption					
$+V_S$	30 (max)	*	*	*	mA
$-V_S$	30 (max)	*	*	*	mA
+5V	125 (max)	*	*	*	mA
Power Dissipation	1.5 (max)	*	*	*	W
TEMPERATURE RANGE					
Operating 5YO Option	0 to +70	*	*	*	°C
4YO Option	−55 to +125	*	*	*	°C
Storage 5YO Option	−55 to +125	*	*	*	°C
4YO Option	−60 to +150	*	*	*	°C
DIMENSIONS					
5YO Option	2.1 × 1.1 × 0.195	*	*	*	Inches
	(53.5 × 28 × 4.95)	*	*	*	(mm)
4YO Option	2.14 × 1.14 × 0.18	*	*	*	Inches
	(54.5 × 29 × 4.6)	*	*	*	(mm)
WEIGHT	1 (28)	*	*	*	oz. (grams)

Specifications subject to change without notice.

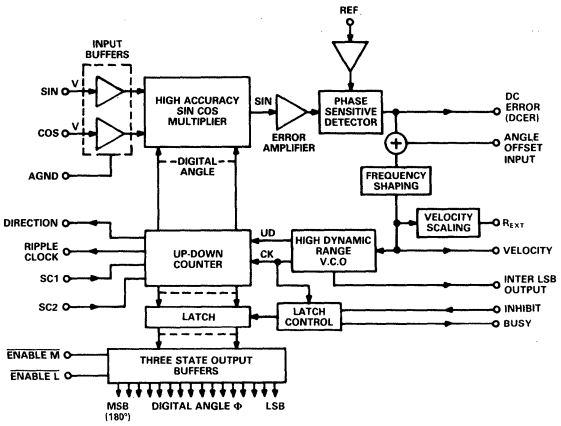
ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1] . . . . . 0V to +17V dc
$-V_S$[1] . . . . . 0V to −17V dc
+5V[2] . . . . . 0V to +6.0V dc
Reference . . . . . ±17V dc
Sine . . . . . ±17V dc
Cosine . . . . . ±17V dc
Any Logical Input . . . . . −0.4V to +5.5V dc

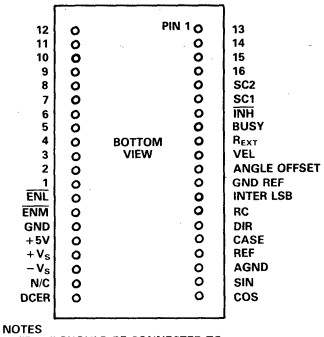
CAUTION:

1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NOTES
1. "R_{EXT}" SHOULD BE CONNECTED TO "VEL" FOR UNITY GAIN.
2. CASE PIN CONNECTED ON 460 OPTION ONLY

OPERATION OF THE CONVERTER

The 1S74 is a tracking converter, this means that the output automatically follows the input for speeds up to the maximum tracking rate for the resolution option. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

The static angular accuracy quoted for each converter type is the worst case error that can occur over the full operating temperature range with the following input conditions:

a) Signal input amplitudes within 5% of the nominal values.

b) Signal and reference frequency within the specified operating range.

c) Phase shift between signal and reference less than 10 degrees.

d) Signal and reference waveform harmonic distortion less than 10 percent.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the converters can be used well outside these operating conditions providing the following points are observed.

SIGNAL AMPLITUDE (SINE AND COSINE INPUTS)

The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the analog outputs and inputs of the converter such as velocity, inter LSB position and angle offset.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value the angular error will increase by an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the K_a is proportional to signal level.

SIGNAL AND REFERENCE FREQUENCY

Any frequency within the specified range of the converter may be used. It should be noted that the signal and reference input voltages must be in resolver format.

REFERENCE VOLTAGE LEVEL

The amplitude and waveform of the reference signal applied to the converter's input is not critical, however it is essential that the zero crossing points are maintained in the correct place to drive the converter's phase sensitive detector.

HARMONIC DISTORTION

The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square and triangle waveforms can be used but the input levels should be adjusted so that the average value after rectification is 1.9 volts. (For example – a square wave should be 1.9V peak.)

NOTE: The figure specified of 10% harmonic distortion is for calibration convenience only.

PHASE SHIFT (BETWEEN SIGNAL AND REFERENCE)

See Section on "Dynamic Accuracy vs. Resolver Phase Shift".

RESOLUTION PROGRAMMING

The 1S74 converter can be programmed for resolutions of 10, 12, 14, and 16 bit by applying a binary code to the pins "SC1" and "SC2".

The dc error output and maximum revolutions per minute for full scale are scaled internally according to the particular resolution selected.

Table I gives the binary code, dc error output and maximum tracking rate for the resolutions available.

Resolution	Binary Code SC1	SC2	DC Error (mV/Bit)	Tracking Rate for FS (±10V) rpm
10 Bit	0	0	160	40,800
12 Bit	0	1	40	10,200
14 Bit	1	0	10	2,550
16 Bit	1	1	2.5	630

Table I.

NOTE: When changing resolution under dynamic conditions, a period of uncertainty will exist before position and velocity data is valid.

For more information ask for the relevant application note.

DATA TRANSFER

BUSY Output:

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of an LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input:

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

NOTE: With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

$\overline{\text{ENABLE}}$ Inputs:

Two $\overline{\text{ENABLE}}$ inputs are provided, $\overline{\text{ENABLE M}}$ for the most significant 8-bits and $\overline{\text{ENABLE L}}$ for the least significant remainder. These $\overline{\text{ENABLES}}$ determine the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins. The operation of these $\overline{\text{ENABLES}}$ has no effect on the conversion process.

Two methods are available for transferring data, by using the inputs and outputs described.

One method is to transfer data when the BUSY is in a "Lo" state or clock the data out on the trailing edge of the BUSY pulse. Both the $\overline{\text{INHIBIT}}$ and the $\overline{\text{ENABLES}}$ must be in their correct state of "Hi" and "Lo's" respectively.

The alternative method is to use the $\overline{\text{INHIBIT}}$ input. Data will always be valid one microsecond after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied.

RIPPLE CLOCK (RC) AND DIRECTION (DIR) OUTPUTS:

As the digital output of the converter passes through the major carry, i.e., all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

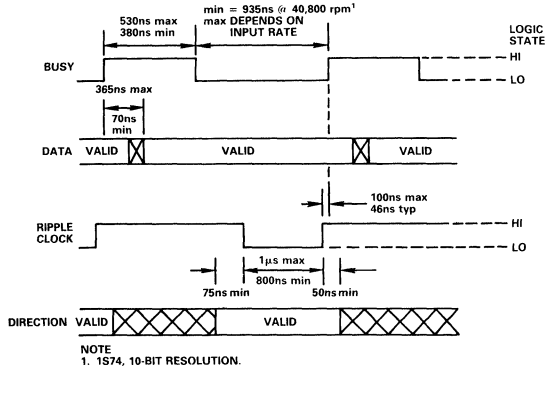


Figure 1. Timing Diagram

The DIRECTION (DIR) logic output indicates the direction of input rotation and this data is always valid in advance of the RIPPLE CLOCK pulse, and stays valid until the direction changes (see Timing Diagram).

These two logic outputs are provided so that the user can count the input revolutions or pitches. An external extension counter is required. Figure 2 shows the application circuit which should be used to perform this counting function.

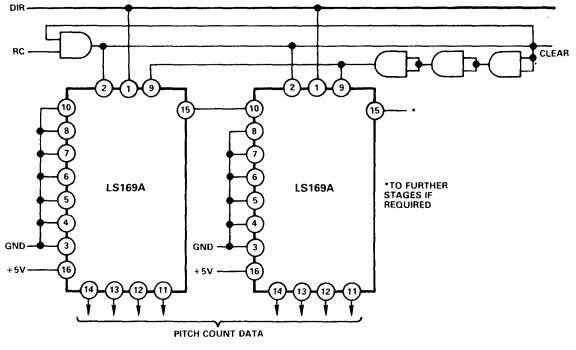


Figure 2. Connections for Use with LS Extension Counters

VELOCITY OUTPUT

The tracking conversion technique produces an internal signal at the input to the voltage controlled oscillator (VCO) that is proportional to the rate of the input angle. In the 1S74 additional circuitry is included to linearize this signal, which is closely characterized, producing a high quality tachogenerator velocity output at the VELOCITY (VEL) pin.

This analog tachogenerator velocity output is resistively scaled internally to give a full scale output of ±10V dc at the specified tracking rate for the converter.

However, a full scale output of ±10V dc can be obtained for lower speeds by changing the gain of the internal scaling amplifier using only an external resistor. The external resistor, R_{EXT}, should be connected between "R_{EXT}" pin and ground, and calculated using the following equation.

$$R_{EXT} = \frac{10 \times A}{B - A} \text{ k ohms}$$

Where A = required rpm to be represented by ±10V FS

B = specified rpm for the converter.

NOTE: A cannot be greater than B and for unity gain "VEL" and "R_{EXT}" pins should be linked.

Ripple and noise on the velocity signal consists of two components—steady state noise and dynamic noise.

Steady state noise—this is internally generated noise produced by the converter's circuitry and is the only noise signal present under static input conditions.

Dynamic noise—this is the noise produced, in addition to steady state noise, under dynamic operating conditions.

The two main components of the dynamic noise signal are due to the "non-zero" angular error of the resolver/converter combination. The figures given in the specification are typical for a size 11, 7 arc-minutes, brushless resolver.

It should be noted that when operating at low tracking rates it is critical to maintain the signal input voltage at its nominal value in order to keep the noise level on the velocity signal to an absolute minimum. The effect of variation in signal voltage at low tracking rates is to produce low energy spikes on the velocity output on the rising edge of the BUSY pulse. The amplitude of these spikes will be in the region of 30μV per percent variation in signal input voltage level.

NOTE: The velocity signal output and max tracking rate derates by 15% (max) for operation with ±12 volt power supplies.

SPECIAL FUNCTIONS

DC ERROR: The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converters are a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason. It is therefore an indication that the input has exceeded the maximum tracking rate of the converter, or due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test".

INTER LSB OUTPUT: In order to overcome the "free play" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of the digital angle output.

The output is therefore proportional to the inter LSB resolved position with a maximum output representing 1LSB.

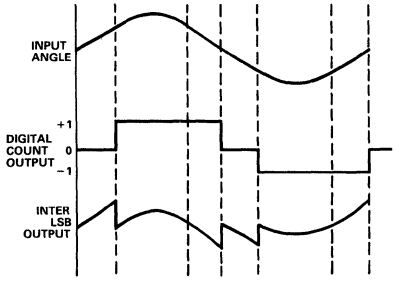


Figure 3.

Figure 3 illustrates how the INTER LSB output compensates for the instances where, due to hysteresis, there is no change in the digital count output for 1LSB change in input angle. The sum of the digital count output and INTER LSB output equals the actual input angle.

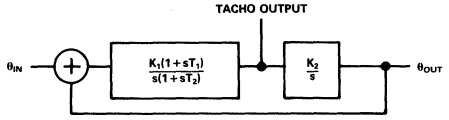
ANGLE OFFSET: A unique feature of the 1S74 converter is the angle offset input which allows the user to electrically "rotate" the input shaft of the resolver.

Injecting a current of 320nA into the angle offset input pin will offset the digital output of the converter by 1LSB relative to the angle defined by the resolver inputs. It is recommended that an offset equivalent to no greater than 30LSB's be applied to this input.

This input is a virtual ground, therefore a current source can be generated by a voltage source connected by a single resistor.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below:



Positional Transfer Function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_1 K_2}{s^2} \cdot \frac{1 + sT_1}{1 + sT_2} \text{ open loop}$$

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + \frac{s^2}{K_1 K_2} + \frac{s^3 T_2}{K_1 K_2}} \text{ closed loop}$$

where $K_1K_2 = K_a$

Tachogenerator Transfer Function:

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{K_1(1 + sT_1)}{s(1 + sT_2)} \text{ open loop}$$

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{s(1 + sT_1)}{K_2(1 + sT_1) + \frac{s^2}{K_1} + \frac{s^3 T_2}{K_1}} \text{ closed loop}$$

Where: $K_1 = 3.23$
$K_2 = 68.2 \times 10^3$
$K_a = 220 \times 10^3$
$T_1 = 4.46\text{ms}$
$T_2 = 0.21\text{ms}$

Refer: Figures 4 and 5

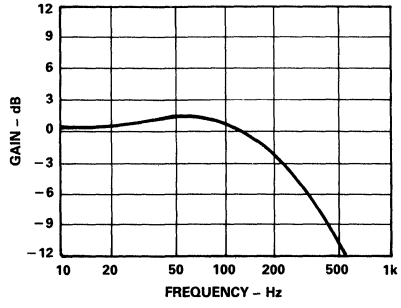


Figure 4. Gain Plot

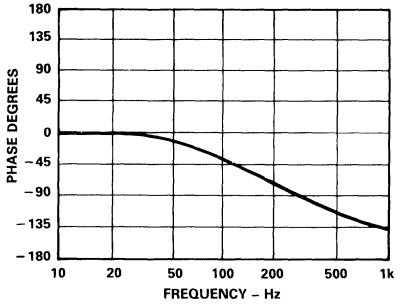


Figure 5. Phase Plot

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Under static operating conditions phase shift between signal and reference lines theoretically does not affect the converter's static accuracy:

However, when rotating, most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions, to an additional error defined by:

$$\frac{\text{SHAFT SPEED (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

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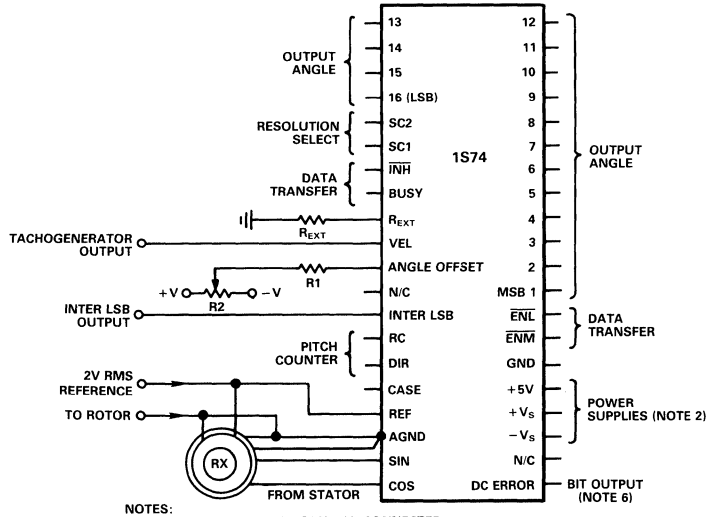


NOTES:
1. GND AND AGND ARE INTERNALLY CONNECTED.
2. EACH SUPPLY SHOULD BE DECOUPLED WITH 100nF CERAMIC CAPACITOR IN PARALLEL WITH A 6μF TANTALLUM CAPACITOR.
3. REXT IS EXTERNAL TACHOGENERATOR SENSITIVITY SCALING RESISTOR (IF REQUIRED) – SEE TEXT UNDER HEADING "VELOCITY OUTPUT".
4. R1 AND R2 ARE ANGLE OFFSET INPUT SCALING RESISTORS (IF REQUIRED) – SEE TEXT.
5. CASE PIN CONNECTED ON 460 OPTION ONLY.
6. POSSIBLE USE AS BUILT-IN TEST EQUIPMENT. (SEE HEADING "SPECIAL FUNCTIONS".)

Figure 6. Electrical Connections

CONNECTING THE CONVERTER

The electrical connection of the converter is straight-forward. The power supply voltages connected to $+V$, and $-V$, pins can be $\pm 12V$ to $\pm 15V$ but must not be reversed. The $+5V$ supply connects to the $+5V$ pin and should not be allowed to become negative with respect to the GND pin.

It is suggested that decoupling capacitors are connected in parallel between the power lines ($+V_s$, $-V_s$ and $+5V$) and GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The converter has some H/F decoupling provided internally, as well as input protection on the signal and reference inputs.

The resolver connections are made to the sine and cosine inputs, reference and analog ground as shown in the electrical connection diagram (Figure 6). The 2V rms reference supply, which can be provided by the OSC1758 oscillator, should be connected to the resolver rotor.

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

HI-REL PROCESSING

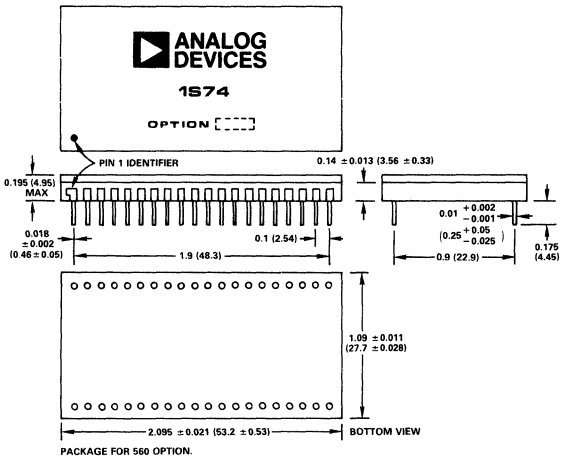
All models ordered to high reliability requirements will be identified with a B suffix, and will have received the following processing:

1. Internal visual inspection
2. Stabilization bake, 24 hours at 150°C
3. Temperature cycling, −65°C to +150°C
4. Constant acceleration, 5000g
5. Powered burn-in, 160 hours at 125°C
6. Final electrical test at T_{min} and T_{max}
7. Seal test, fine and gross
8. External visual inspection

OUTLINE DIMENSIONS

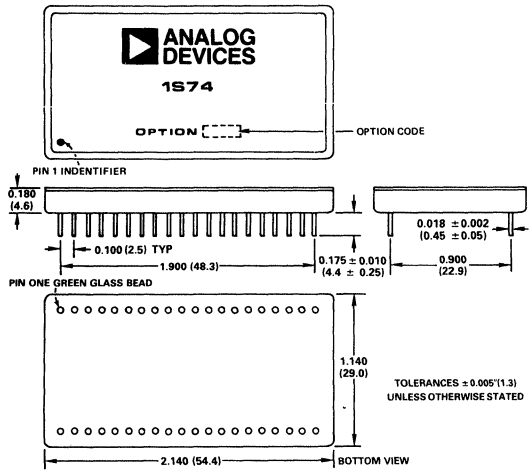
Dimensions Shown in inches and (mm).

PACKAGE FOR 560 OPTION



PACKAGE FOR 560 OPTION.

PACKAGE FOR 460 AND 460B OPTIONS



PACKAGE FOR 460 AND 460B OPTIONS

OTHER PRODUCTS

1S14/1S24/1S44/1S64–	10-, 12-, 14- and 16-Bit Hybrid Resolver-to-Digital Converters with High Specification Tachometer Output.
1S10/1S20/1S40/1S60/1S61–	10-, 12-, 14- and two 16-Bit Inductosyn™/ Resolver-to-Digital Converters (Hybrid)
IRDC1732–	Inductosyn™/Resolver-to-Digital Converter (Hybrid), Low Cost
IPA1751–	Inductosyn™ Pre-Amplifier
OSC1754–	Power Oscillator
OSC1758–	Power Oscillator (Hybrid)
IPA1764–	Inductosyn™ Pre-Amplifier (Hybrid)
MCI1794–	3 Channel Inductosyn™/Resolver-to-Digital Converter (Multibus Compatible Card)

Inductosyn™ is a registered trademark of Farrand Industries, Inc.

ORDERING INFORMATION

1S74 X60 B

- B — High Reliability Processing
- X60 — 2kHz to 10kHz reference frequency
- X = 5 0 to +70°C operating temperature range
- X = 4 −55°C to +125°C operating temperature range.

ANALOG DEVICES

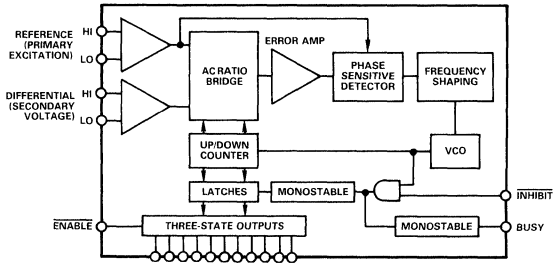
LVDT-to-Digital Converter

2S50

FEATURES
Internal Signal Conditioning
Direct Conversion to Digits
Reference Frequency 400Hz or 1kHz to 10kHz
High MTBF
No External Trims
Absolute Encoding

APPLICATIONS
Industrial Measurement and Gauging
Numerical Control
Avionic Control Systems
Valves and Actuators
Limit Sensing

2S50 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The 2S50 series converters translate the outputs from LVDT and RVDT transducers into digits directly. No signal conditioning, trims, preamplifiers, demodulators or filters are required. The 2S50 series can also be used as general purpose ratiometric A-to-D converters; very compatible with load cells, strain gauge bridges, some pressure transducers and interferometers.

The 2S50 linearly converts ac signals into an 11-bit parallel digital word. The digital output is an offset binary word which is the ratio of the signal and reference inputs. When used with LVDT and RVDT transducers, the digital output represents the linear or rotary displacements of the transducer. The converter is a continuous tracking type using a type 2 servo loop.

PRINCIPLE OF OPERATION

The 2S50 is a tracking converter. This means that the output automatically follows the input without the necessity of a convert command.

A conversion is initiated by a change of input signal equivalent to 1LSB of the output.

Each LSB increment of the output is indicated by a "Busy" pulse.

With an LVDT connected to give a null at center position, the output will track the input from digital "1 + all zeroes" to digital "all ones" for plus full scale, and digital "1 + all zeroes" to digital "all zeroes" for negative full scale.

The 2S50 operates only on the ratio of the two inputs for the conversion process. As such the whole system, consisting of excitation oscillator, LVDT and converter, is insensitive to change in excitation voltage, amplitude, frequency and waveshape.

Since a phase sensitive demodulator is included with the conversion loop of the 2S50, the system has a high rejection to signals that are not phase and frequency coherent with the excitation voltage. This feature, combined with ratiometric conversion gives a very high standard of integrity to digitized LVDT and RVDT systems.

PIN FUNCTION DESCRIPTION

$-V_S$	Main negative power supply -15V dc.
$+V_S$	Main positive power supply $+15$V dc.
$+5$V	Logic supply.
GND	Power supply ground. Digital ground. Reference voltage low.
Bit 1-11	Parallel output data bits.
Ref Hi	Analog reference input (Hi).
Diff Hi	Analog difference input (Hi).
Ref Lo	Analog reference input (Lo).
Diff Lo	Analog difference input (Lo).
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "Lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the output latches are being updated. Data should not be transferred from the converter while BUSY is "Hi".
$\overline{\text{ENABLE}}$	The output data bits are set to a low impedance state by application of a logic "Lo".
CASE	This should normally be grounded. Case can be taken to any voltage with a low impedance up to ± 20V.
N/C	Pins designated N/C not connected internally.

ORDERING INFORMATION

2S50/ X Y 0 B

- B — High Reliability Processing
- Y = 1 400Hz reference frequency
- Y = 6 1kHz to 10kHz reference frequency
- X = 4 −55°C to +125°C operating temperature range (Metal Package)
- X = 5 0 to +70°C operating temperature range (Ceramic Package)

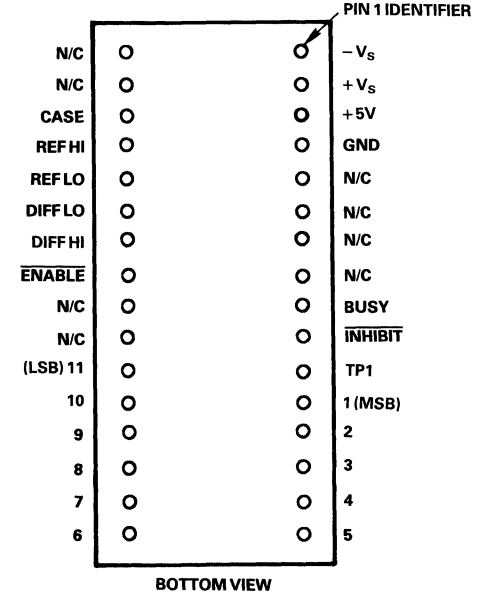
SPECIFICATIONS (typical @ +25°C, unless otherwise noted)

Models	2S50/510	2S50/560	2S50/410	2S50/460
RESOLUTION	11 Bits	*	*	*
ACCURACY[1]	0.1% (Full Scale)	0.1%	0.2%	0.2%
LINEARITY	± 1/2LSB	*	*	*
REFERENCE FREQUENCY	400Hz	1kHz–10kHz	400Hz	1kHz–10kHz
SIGNAL INPUTS[2]	2.5V rms	*	*	*
INPUT IMPEDANCE	5MΩ (min)	*	*	*
SLEW RATE (Min)	200LSB/ms	400LSB/ms	200LSB/ms	400LSB/ms
SETTLING TIME (99% FS Step)	50ms	25ms	50ms	25ms
ACCELERATION CONSTANT (k_a)	70,000	650,000	70,000	650,000
BUSY PULSE	1μs (max) 1 LS TTL Load	* *	* *	* *
INHIBIT INPUT	Logic "Lo" to Inhibit 1 LS TTL Load	* *	* *	* *
POWER DISSIPATION	550mW	*	*	*
POWER SUPPLIES[3]	−15V @ 18mA (typ) 25mA (max) +15V @ 18mA (typ) 25mA (max) +5V @ 3mA (max)	* * *	* * *	* * *
TEMPERATURE RANGE				
Operating	0 to +70°C	*	−55°C to +125°C	**
Storage	−60°C to +150°C	*	*	*
DIMENSIONS	1.72" × 1.1" × 0.205" (43.5 × 28.0 × 5.2mm)	* *	1.74" × 1.14" × 0.28" (44.2 × 28.9 × 7.1mm)	** **
WEIGHT	1 oz. (28g)	*	*	*
PACKAGE OPTIONS[4]	DH-32E	DH-32E	M-32	M-32

NOTES
[1]Accuracy applies over ± 20% signal voltage, ± 20% excitation frequency and full temperature range, and for not greater than 3° phase error between reference and difference inputs.
[2]This is a nominal value.
[3] ± 12 volts to ± 17 volts.
[4]See Section 14 for package outline information.
*Specifications same as 2S50/510.
**Specifications same as 2S50/410.

Specifications subject to change without notice.

PIN CONFIGURATION



BOTTOM VIEW

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$	0V to +17V dc
$-V_S$	0V to −17V dc
+5V	0V to +5.5V dc
Ref, Hi to Lo	±20V dc
Diff, Hi to Lo	±20V dc
Case to GND	±20V dc
Any Logical Input	−0.4V to +5.5V dc

High Resolution LVDT-to-Digital Converters

2S54/2S56/2S58

FEATURES

Direct Conversion of LVDT and RVDT Outputs into Digital Format
Ratiometric Conversion for Extremely High Stability
High Resolution (14-16 Bit) Parallel Digital Output
User Definable Input Gain
Quadrature Rejection
Operation Over 360 Hz to 11 kHz Frequency Range
Linearity Better than ±0.01%
Internal Bridge Completion Resistors
1 LSB Repeatability
75% Overrange Capability
Extended Temperature Range Versions

APPLICATIONS

Direct LVDT/RVDT-to-Digital Conversion
Industrial Measurement and Gauging
Valve and Actuator Control
Limit Sensing
Aircraft Control Systems
Semiconductor Wafer Profiling
AC-to-Digital Conversion

GENERAL DESCRIPTION

The 2S56 series of converters linearly converts the outputs of ac energized Linear and Rotary Variable Differential Transformers (LVDTs, RVDTs) directly into a high resolution digital format. For example, with a ±1 mm stroke LVDT, the least significant bit (LSB) of the 2S56 will represent 0.061 microns.

The 2S58, a high gain variant of the 2S56, can offer even higher positional resolution. Using the same ±1 mm stroke LVDT over a reduced range, the 2S58 can realize an LSB weighting of 1.22 nm.

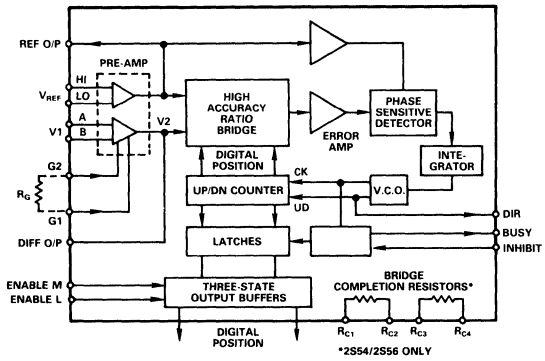
The ratiometric conversion technique employed by the converters obviates the need for high stability oscillators. The performance quoted for the devices can be achieved with as much as a ±10% variation in reference amplitude.

The converters are complete – no signal conditioning, preamplifiers or filters are required. The user need only supply a suitable reference oscillator.

The converters operate on a Type II, tracking, servo loop principle which means that the digital output continuously follows the transducer input without the need for external convert commands as in conventional A-to-D converters. The conversion technique also ensures that there is no lag between digital output and transducer input under constant velocity conditions.

To facilitate interfacing with various types of LVDTs and RVDTs, all inputs are fully differential. In addition, the converters have the flexibility of setting the input gain with a single

2S54, 2S56 AND 2S58 FUNCTIONAL BLOCK DIAGRAM



external resistor or link. In order to simplify the transducer interface, both the output of the gain stage as well as the reference voltage are brought out to enable simplified measurement.

The parallel digital output word is through tri-state drivers to enable direct connection to system data buses. Included is a High/Low byte enable which allows communication on both 8 and 16-bit busses. A separate line is provided to indicate the direction of transducer travel. A BUSY pulse is provided indicating that data is changing and not valid for transfer.

APPLICATIONS/USER BENEFITS

Because the 2S56 series of converters operates on the ratio of the transducer output signal to the excitation (reference) voltage, the entire measurement system is insensitive to changes in reference voltage, frequency and wave shape. The resulting stability makes conversion technique unrivaled, particularly in applications with poor voltage regulation.

The converters can also be connected in a mode which allows the 2S54/56/58 to be galvanically isolated from the excitation source. This configuration has the added benefit of minimizing the effect of phase shifts and signal input quadrature.

Because of the use of a phase sensitive demodulator in the tracking loop, the system has extremely high rejection of signals which are not phase and frequency coherent with the excitation voltage. The resulting noise immunity makes the converters an ideal choice for industrial and airborne applications.

The high precision of the conversion, together with the stability offered by ratiometric conversion, make the 2S56 series good candidates for applications previously beyond the capability of LVDTs. For example, the 2S58 can realize performance competitive with optical interferometric measurement systems.

SPECIFICATIONS[1]

Models	2S54	2S56	2S58	Comments	Units
DIGITAL OUTPUT				Output Coding Parallel	
Format	14-Bit Binary	16-Bit Binary	16-Bit Binary	Natural Binary	
Overrange[2]	75% of FS	*	*		
INPUTS (DIFFERENTIAL)					
V_{REF}	2	*	*		V rms
V_2	2	*	*		V rms
V_1[3]	0.2 (min) 2.0 (max)	*	0.04 (min) 0.2 (max)	See "INPUT GAIN" and	V rms
Input Gain	×1 to ×10	*	×10 to ×50	"SCALING INPUTS"	
Input Impedance (V_{REF}, V_1)[2]	6 (max)	*	*		MΩ
CMRR[2]					
@ ×1 Gain	100 (min)	*	NA		dB
@ ×10 Gain	100 (min)	*	120 (min)		dB
@ ×50 Gain	NA	NA	120 (min)		dB
BRIDGE COMPLETION RESISTORS[2]				(Only in 2S54/2S56)	
Value (XYO Options)	9990 (min) 10010 (max)	*	NA		Ω
Ratio Match	0.025	*	NA		%
Tracking Temperature Coefficient	2	*	NA		ppm/°C
REFERENCE FREQUENCY[2]					
50 Hz Bandwidth Option (2S54, 2S56)	360 (min) 5000 (max)	*	NA		Hz
140 Hz Bandwidth Option (2S54, 2S56)	1000 (min) 5000 (max)	*	NA		Hz
300 Hz Bandwidth Option (2S58 Only)	NA	NA	7000 (min) 11000 (max)		Hz
DIGITAL OUTPUT (BIT 1–BIT 16)					
Output Voltage				V_L = +5 V dc	
(Logic Low I_{OL}=8.0 mA)	0.4 (max)	*	*	Logic Low I_{OL} = 8.0 mA	V dc
(Logic High I_{OH}=−0.4 mA)	2.4 (min)	*	*	Logic High I_{OH} = −0.4 mA	V dc
Tristate Leakage Current				V_L = +5 V dc	
(V_{OZL}=0.4 V dc)	±20 (max)	*	*	Logic Low V_{OZL} = 0.4 V dc	µA
(V_{OZH}=2.4 V dc)	±20 (max)	*	*	Logic High V_{OZH} = 2.4V dc	µA
DIGITAL INPUT					
(INHIBIT, ENABLE M, ENABLE L)					
Low Input Voltage	0.7 (max)	*	*	V_L = +5 V dc	V dc
High Input Voltage	2.0 (min)	*	*	V_L = +5 V dc	V dc
Low Input Current	−400 (max)	*	*	V_{IL} = 0.4 V dc	µA
High Input Current	20 (max)	*	*	V_{IH} = +2.4 V dc	µA
DATA TRANSFER[2]				See Figure 12	
BUSY Pulse Width	380 (min) 530 (max)	*	*		ns
BUSY Pulse Load[4]	6	*	*	BUSY Is "Hi" When Output Is Changing	LSTTL Loads
Enable/Disable Time	120 (typ) 220 (max)	*	*		ns
Data Setup Time	600	*	*		ns
ACCURACY[5]					
Conversion Accuracy	±0.7	±2.5	±1		LSB
Gain Accuracy[6,7]					
@ ×1 Gain					
0 to +70°C (5Y0)	±0.03 (max)	*	NA	2S54/2S56 Only	% FSR
−55°C to +125°C (4Y0)	±0.03 (max)	*	NA		% FSR
@ ×10 Gain					
0 to +70°C (5Y0)	±0.07 (max)	*	*	2S54/2S56 and 2S58	% FSR
−55°C to +125°C (4Y0)	±0.10 (max)	*	*		% FSR
@ ×50 Gain					
0 to +70°C (5Y0)	NA	NA	±0.09 (max)	2S58 Only	% FSR
−55°C to +125°C (4Y0)	NA	NA	±0.12 (max)		% FSR

Models	2S54	2S56	2S58	Comments	Units
Integral Linearity[6,7]					
0° Phase Shift, V_{REF} to V_1	±0.006 (max)	*	±0.00312 (max)	See "PHASE SHIFT	% FSR
1° Phase Shift, V_{REF} to V_1	±0.008 (max)	*	±0.00437 (max)	AND QUADRATURE	% FSR
5° Phase Shift, V_{REF} to V_1	±0.01 (max)	*	±0.00625 (max)	EFFECTS"	% FSR
Differential Linearity[6]	±0.5 (max)	*	*		LSB
Temperature Dependent					
Position Offset[2]	±0.04 (max)	*	*		% FSR
REPEATABILITY[5]					
Over 0 to +70°C[2]	±1	*	*		LSB
Hysterisis	0.5 (min) 1 (max)	*	*		LSB
DYNAMIC CHARACTERISTICS[5]					
Slew Rate[2]					
50 Hz Bandwidth Option (2S54,2S56)	150	*	NA		LSB/ms
140 Hz Bandwidth Option (2S54, 2S56)	360	*	NA		LSB/ms
300 Hz Bandwidth Option (2S58 Only)	NA	NA	688		LSB/ms
Settling Time (Half FS Step)					
50 Hz Bandwidth Option (2S54, 2S56)	160	300	NA	Half FS Step	ms
140 Hz Bandwidth Option (2S54, 2S56)	70	160	NA	Half FS Step	ms
300 Hz Bandwidth Option (2S58 Only)	NA	NA	65	Step From +FSR to −FSR	ms
ANALOG OUTPUTS					
DIFF O/P (Max Allowable Swing)	10	*	*		V p-p
REF O/P (Max Allowable Swing)	10	*	*		V p-p
POWER REQUIREMENTS					
$+V_S$	+15 ±5%	*	*		V dc
$-V_S$	−15 ±5%	*	*		V dc
+5 V	+5 ±5%	*	*		V dc
Supply Currents					
$\pm V_S$	25 (typ) 40 (max)	*	*	Quiescent Condition	mA
+5 V	105 (typ) 125 (max)	*	*		mA
Power Dissipation	1.3 (typ) 1.8 (max)	*	*		Watts
TEMPERATURE RANGE					
Operating	0 to +70 (5Y0 Option)	*	*		°C
	−55 to +125 (4Y0 Option)	*	*		°C
Storage	−55 to +125	*	*		°C
DIMENSIONS	2.14 × 1.14 × 0.18	*	*	See Packaging	Inches
	54.4 × 29.0 × 4.6	*	*	Specifications	mm
WEIGHT	1	*	*		Ounces
	28	*	*		Grams
PACKAGE OPTIONS[8]	M-40	M-40	M-40		

NOTES

[1]Tested with nominal supply (±15 V dc, +5 V dc), reference/signal voltages and frequency.

[2]Guaranteed by design, test not required.

[3]V_1 is the signal input to the converter directly from the transducer. V_2 is the output of the internal gain stage. Because V_2 needs to be maintained at 2 V ±10% in order to meet the converter accuracy (see Note 5), the gain and the maximum value of V_1 should be carefully chosen. Furthermore, because the converter operates on the ratio of V_2 and V_{REF}, care should be taken to see these voltages are matched in order to achieve the full dynamic range of the converter.

[4]Maximum output current is 2.4 mA.

[5]Specified over the operating temperature range of the option and for:

a. ±10% difference in both V_{REF} and V_2 amplitudes

b. 10% harmonic distortion in V_{REF} and V_1.

c. The accuracy is specified for the preset gains of ×1, ×10, and ×50. For accuracy in the intermediate range, see Section "PHASE SHIFT AND QUADRATURE EFFECTS."

[6]Tested with input gains 1, 10 and 50 with V_1 attenuated by 1, 10 and 50, respectively.

[7]Full-Scale Range (FSR) is defined as $V_2 = +V_{REF}$ to $V_2 = -V_{REF}$. This would usually correspond to the utilized LVDT stroke.

[8]See Section 14 for package outline information.

*Specifications the same as the 2S54.

Specifications subject to change without notice.

MODELS AVAILABLE

The 2S56 series is available in three versions:

2S54	14-Bits	Input Gain	1–10
2S56	16-Bits	Input Gain	1–10
2S58	16-Bits	Input Gain	10–50

The 2S54 and 2S56 are available in two bandwidth options. The 50 Hz bandwidth option operates over the reference frequency range of 360 Hz to 5 kHz, while the 140 Hz bandwidth option operates over the range of 1 kHz to 5 kHz. The 2S58 is available only in a 300 Hz bandwidth version which operates with reference frequencies between 7 kHz and 11 kHz.

All three devices are available in both commercial (0 to +70°C) and military (−50°C to +125°C) operating temperature versions.

Full ordering information is given on the back page of this data sheet.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to GND	+17 V dc
$-V_S$ to GND	−17 V dc
V_{REF}	35 V p-p
$+V_L$ to GND	+7 V dc
V1	35 V p-p
Logical Input to GND (max)	+5.5 V dc
Logical Input to GND (min)	−0.4 V dc
Case to GND	±20 V dc
Power Dissipation	1.8 Watts
Junction Temperature	+150°C

CAUTION:

1. Absolute Maximum Ratings are the limits beyond which damage to the device may occur.
2. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
3. The +5 V power supply must never go below GND.

PRINCIPLES OF OPERATION

The principle of operation is shown in Figure 1.

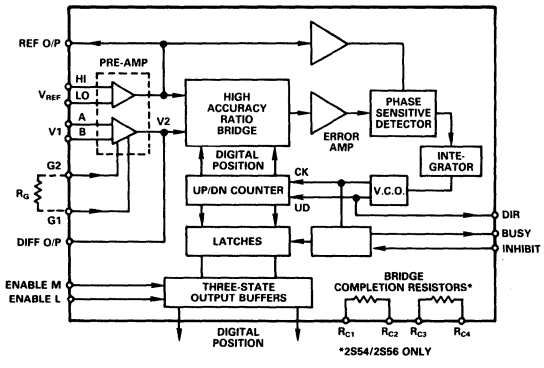


Figure 1. Principle of Operation of the 2S56 Series Converters

USING THE 2S56 SERIES CONVERTERS

The 2S56 series of converters operates on a tracking principle. This means that the output digital word always automatically represents the position of the LVDT or RVDT without the need for external convert commands and status wait loops. As the transducer moves through a position equivalent to 1 Least Significant Bit (LSB) on the output, the output digital word is automatically updated. Each LSB update initiates a BUSY pulse.

INPUT GAIN

Since the transformation ratio of an LVDT or RVDT from excitation voltage to signal voltage is typically in the order of 1:0.15, provision for gain scaling has been provided. The gain can, therefore, be selected to ensure that the full-scale output of the converter represents the maximum stroke position of the transducer.

The gain setting is accomplished by means of Pins 21 and 22 (G1 and G2). A link between the two pins gives a preset gain of ×10 (×50 on the 2S58) whereas no connections between them gives a preset gain of ×1 (×10 on the 2S58).

For intermediate gains a resistor should be connected between the pins (G1 and G2) according to the following equation:

$$G = \frac{R_1}{R_G + R_2} + G\infty$$

where R_G is the value of the external resistor in kΩ and G is the realized gain.

For the 2S54 and 2S56:

$R_1 = 27$ [kΩ]

$R_2 = 3$ [kΩ]

$G\infty = 1$

For the 2S58:

$R_1 = 108$ [kΩ]

$R_2 = 2.7$ [kΩ]

$G\infty = 10$

The internal resistors each have absolute accuracies of 0.02% at 25°C. Their absolute temperature coefficient is ±25 ppm/°C. Therefore, if the temperature coefficient and absolute accuracy of the external gain setting resistor, R_G, is known, the accuracy of the input gain stage can be calculated. This additional inaccuracy must be added to the gain error of the converter.

DIGITAL OUTPUT CODES

The 2S56 series of converters employs an offset binary output code, the null position of the LVDT being represented by the MSB being high and all other bits low. Representative digital output codes are shown in Figure 2. For the 2S54 (14-bit resolution), the two least significant bits are unused.

NOTE: A negative position is defined as being when the V1 and V_{REF} are out of phase. A positive position is when they are in phase.

OVERRANGE

The digital output code format shown in Figure 2 enables the user to determine if the LVDT has exceeded the negative or positive full-scale position and has gone into overrange. An indication of overrange can be obtained by performing an "exclusive OR" on Bits 1 and 2 (MSB and 2nd MSB). Alternatively this function can be performed in software.

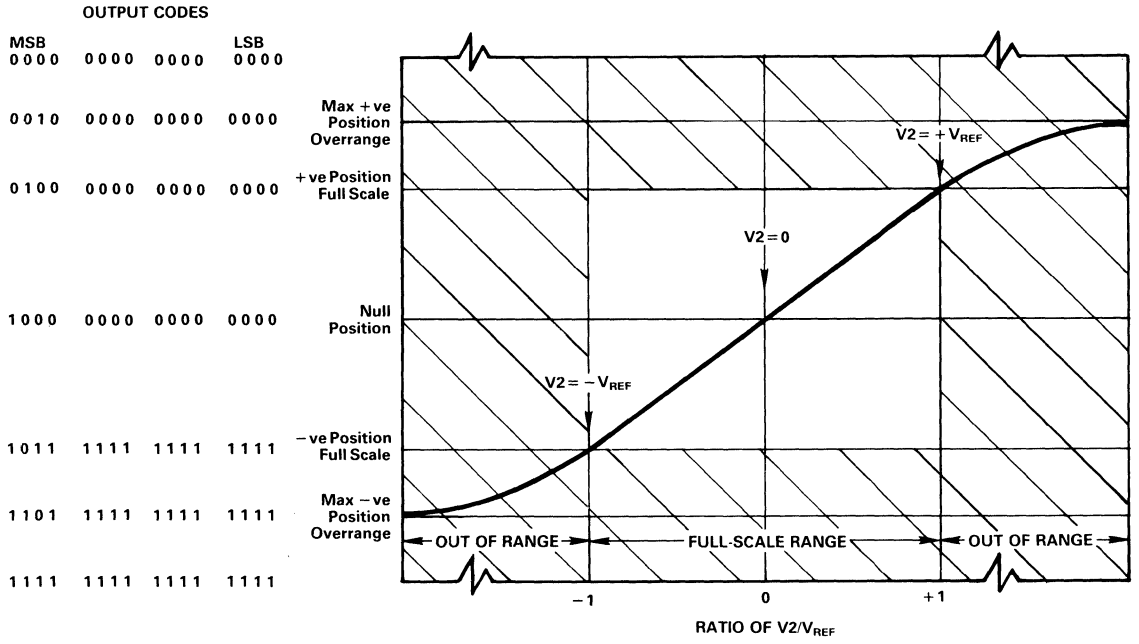


Figure 2. Output Code Format

PHASE SHIFT AND QUADRATURE EFFECTS

Reference to signal phase shift can be high in LVDTs, sometimes in the order of 70 degrees. If the converter is connected as in Figures 3 and 4, any effects due to this phase shift are minimized. This connection method, therefore, provides outstanding benefits.

The additional gain error caused by reference to signal phase shifts is given by:

$$(1 - \cos\theta) \times 100\% \text{ of } FSR$$

where

θ = phase shift between V_{REF} and V1.

When the phase shift between V_{REF} and V1 is zero, additional quadrature on the signal will have no effect on the converter. This is another benefit of the conversion method.

CONNECTING LVDTS

Since all input connections to 2S56 converters are truly differential, there is great flexibility in the input sensor connection configuration. Some of the various methods are shown in Figures 3, 4 and 5.

(It should be noted that a ground reference point should always be included and connected to either the V_{REF} or V1 inputs.)

It is suggested that decoupling capacitors be connected in parallel between the power supply lines ($+V_S$, $-V_S$, +5 V) and GND, adjacent to the converter. Suggested values are: 6.8 µF tantalum and 47 nF disc capacitors connected in parallel. When more than one converter is on a card, separate decoupling should be used for each converter, particularly the 47 nF capacitors.

The $+V_S$ and the $-V_S$ pins should be connected to dc power supplies of the appropriate polarity in the range of ±15 V ±5%. Care should be taken to ensure that the polarity can never become reversed. The +5 V pins should be connected to a +5 V ±5% dc supply. The +5 V supply must never be allowed to go negative with respect to ground.

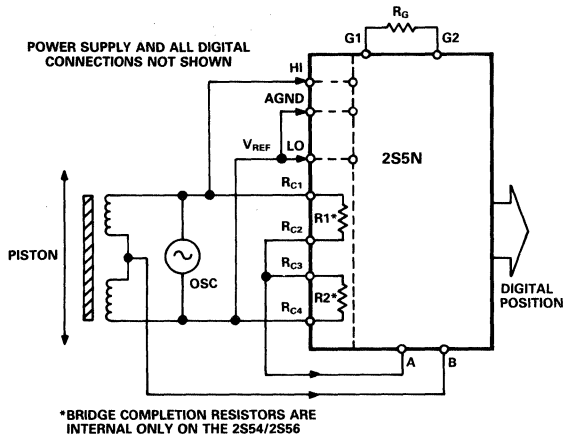


Figure 3. Half Bridge LVDT Connection

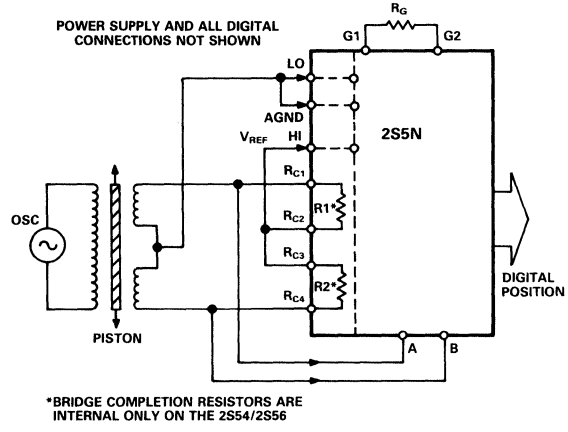


Figure 4. Three- or Four-Wire LVDT Connection

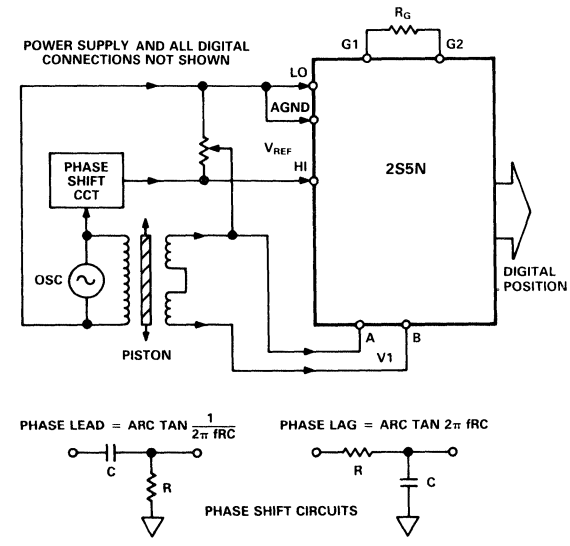


Figure 5. Two-Wire LVDT Connection

Half Bridge Type LVDT Connection

In this method of connection, shown in Figure 3, the internal bridge completion resistors, R1 and R2, in the 2S54 and 2S56 are used. If this configuration is used with the 2S58, external precision resistors must be employed. The "BRIDGE COMPLETION RESISTORS" in the SPECIFICATIONS section details the required precision. The internal resistors in the 2S54 and 2S56 have nominal values of 10 kΩ and are matched sufficiently to ensure that the null position of the LVDT is represented by the correct output code. The common connection between the two resistors (i.e., R_{C2} to R_{C3} on the 2S54, 2S56) can be replaced by a potentiometer if the null needs to be adjusted. For differential measurements, the resistors can be replaced by another LVDT. The system is nonisolated.

Three or Four Wire LVDT Connection

In this method of connection, shown in Figure 4, the converters digital output is proportional to the ratio:

$$\frac{(A-B)}{(A+B)/2}$$

where A and B are the individual LVDT secondary output voltages. Inspection of Figure 4 should demonstrate why this relationship is true. (A−B) is simply the voltage across the series connected secondaries of the LVDT and is applied to the V1 input to the converter. (A+B)/2 is effectively the average of the two secondary voltages as computed by the balanced bridge completion resistors and the grounding of the secondary center-tap.

Note: This method of connection is appropriate only for where (A+B) is a constant, independent of LVDT position. Any lack of constancy in (A+B) will be reflected as an additional non-linearity in the output. It is up to the user to determine if (A+B) is sufficiently constant over the particular stroke length employed. (A+B)/2 can be monitored on the "REF O/P" pin.

This method will usually restrict the usable LVDT range to half of its full range. The restriction can be eliminated, however, by attenuating V1 by a factor of 2 or increasing V_{REF} by a factor of 2.

This connection method has the tremendous advantage of being insensitive to temperature related phase shifts and excitation oscillator instabililty effects usually associated with more conventional LVDT conversion systems.

As in the case of the Half Bridge Type LVDT Connection, R1 and R2 are the bridge completion resistors (internal on the 2S54, 2S56; external on the 2S58) and are matched to a degree sufficient to ensure that the digital output representing the null position does not vary from the LVDT's natural null position. If null adjustment is required, a potentiometer can be used in place of the common connection between the two resistors.

Two-Wire LVDT Connection

This method should be used in cases where the sum of the LVDT secondary output voltages (A+B) is not constant with LVDT displacement over the desired stroke length. The method of connection, shown in Figure 5, still maintains the ratiometric operation and the insensitivity to variations in reference amplitude and frequency. However, the phase shift between V_{REF} and V1 should be minimized to maintain accuracy (see Section "PHASE SHIFT AND QUADRATURE EFFECTS"). Suggested phase compensation circuits are shown in Figure 5.

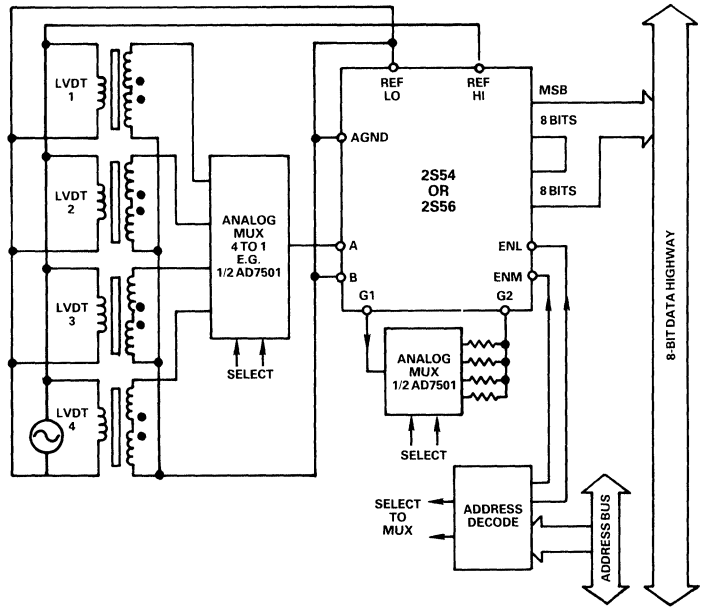


Figure 6. Multiplexing 4 LVDTs into the 2S54/2S56

MULTIPLEXING THE CONVERTERS

Although the 2S56 series of converters are primarily intended for use as single channel, continuous conversion devices, they can also be used in small multiplexed systems as shown in Figure 6. However, when switching between LVDT channels, ample time must be allowed for the converters to settle prior to transferring data.

Using the 2S54/X40 as in Figure 6 and allowing a time between samples of 70 ms, the maximum settling time of the converter can yield four 14-bit results from the 4 LVDTs in 280 ms. The gain can be programmed, as shown, to accommodate various transformation rations of dissimilar LVDTs. Note, however, that the finite "ON" resistance of the analog switch used with the gain setting resistor can introduce gain inaccuracies. This error is minimized for lower gains as the "ON" resistance of the switch will be negligible compared to the gain setting resistor. The error introduced can be calculated from the equation for the preamplifier gain in the "INPUT GAIN" section.

SCALING THE INPUTS

In cases where there is a requirement for a particular LVDT stroke length to correspond to full-scale on the digital output, the input gain must be chosen accordingly. It is important to remember that it is the relationship between V2 and V_{REF}, not V1 and V_{REF}, which determines the full-scale digital output. Furthermore, it should be ensured that these voltages are each 2 V rms ±10%, respectively. For monitoring purposes, V2 is brought to the "DIFF O/P" pin and V_{REF} is brought to the "REF O/P" pin.

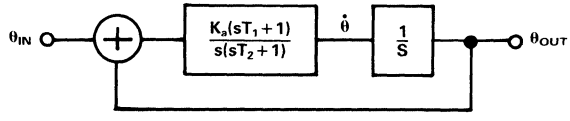


Figure 7. Transfer Function

DYNAMIC PERFORMANCE

The transfer function of the converters, shown in Figure 7 is given by:

Open Loop Gain:

$$\frac{\Delta_{OUT}}{\Delta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1+sT_1}{1+sT_2}$$

Closed Loop Gain:

$$\frac{\Delta_{OUT}}{\Delta_{IN}} = \frac{1+sT_1}{1+sT_1+s^2/K_a+s^3T_2/K_a}$$

where:

	k_a	T1	T2
2S54/56 X10 options	12000 sec^{-2}	14.7 ms	2.3 ms
2S54/56 X40 options	93600 sec^{-2}	5.9 ms	1.0 ms
2S58	450000 sec^{-2}	2.4 ms	0.4 ms

The gain and phase response of each of the three options is shown in Figures 8, 9, 10, 11, 12 and 13.

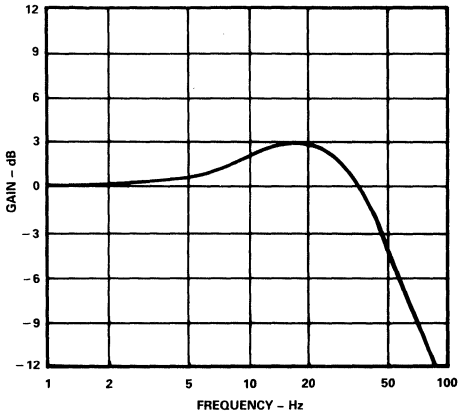


Figure 8. Gain Plot 410 and 510 Options (2S54/2S56)

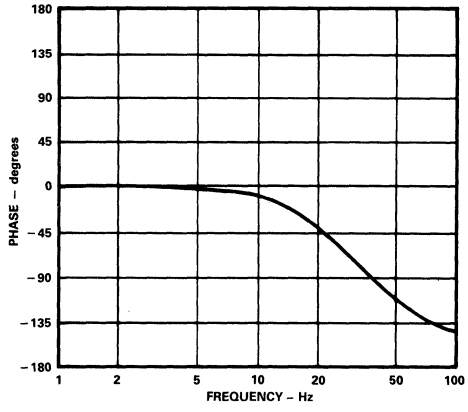


Figure 9. Phase Plot 410 and 510 Options (2S54/2S56)

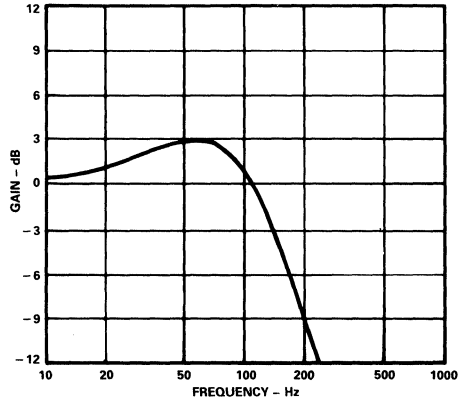


Figure 10. Gain Plot 440 and 540 Options (2S54/2S56)

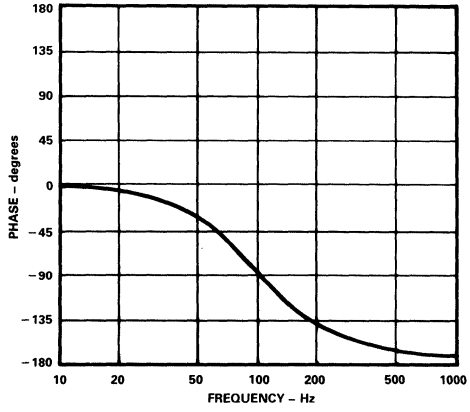


Figure 11. Phase Plot 440 and 540 Options (2S54/2S56)

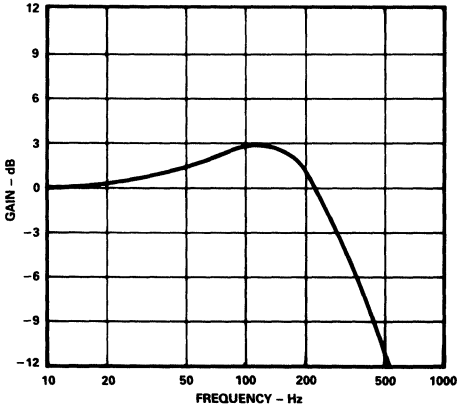


Figure 12. Gain Plot for 2S58

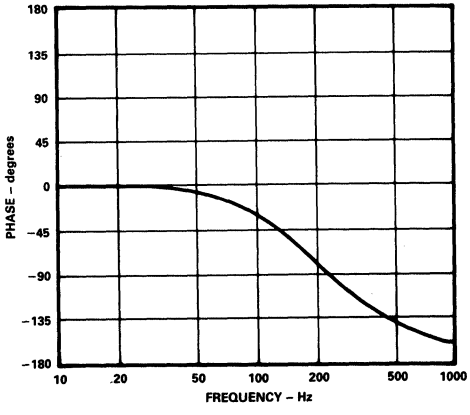


Figure 13. Phase Plot for 2S58

ACCELERATION ERROR

Tracking converters such as the 2S56 series, employing a type 2 servo loop, do not suffer any velocity lag. However, there is an additional error when the LVDT is undergoing periods of acceleration.

The additional error can be defined using the K_a constant of the converter (see DYNAMIC PERFORMANCE section) as follows:

$$K_a = \frac{\textit{Input acceleration}}{\textit{Error in output position}}$$

where the numerator and the denominator are defined in the same units.

K_a does not define the maximum acceleration, only the error due to the acceleration.

DATA TRANSFER

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, due to a change in displacement of the LVDT, the signal appearing on the converter's BUSY output pin is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the equivalent of an LSB and the internal up-down counter is incremented or decremented.

With the INHIBIT input pin in the "Hi" state, data will be transferred automatically to the output latches.

The two three-state enable inputs, ENABLE L and ENABLE M, allow the digital input to be transferred on to a data bus in two separate bytes. ENABLE M enables the most significant 8 bits of the output word while ENABLE L enables the remaining least significant bits.

Figure 14 shows the timing diagram.

There are two methods of transferring the output data. The first is to detect the state of the "BUSY" which is 'Hi" for 1 μs max and then transfer the data when the BUSY is "Lo". Both INHIBIT, ENABLE M and ENABLE L must be in their correct state of "Hi" and "Lo" respectively, in order that the data is presented to the output.

The alternative method is to use the INHIBIT input. Taking this input to a "Lo" state prevents the internal monostable circuits being triggered and consequently the latches being updated. Data will always be valid 1 μs after the application of a logic "Lo" to the INHIBIT. However, if INHIBIT is applied while BUSY is in the "Lo" state (with ENABLE M and ENABLE L also "Lo"), data is valid instantaneously.

The internal tracking operation of the converter cannot in any way be affected by the logic state present on either the INHIBIT or the ENABLE pins.

OTHER INPUTS AND OUTPUTS

Differential Output (DIFF O/P)

This signal is in fact V2 and is brought out to a pin in order to simplify scaling of the V1 signal.

Direction (DIR)

This TTL output signal indicates the direction of the transducer. It is a logic "Hi" when counting up and a logic "Lo" when counting down.

Reference Output (REF O/P)

This is the reference signal after the input buffer stage. It can be used as a single ended measurement point for the V_{REF} input.

It can also be used as a BITE (Built in Test Equipment) signal to detect if the LVDT has become disconnected or the reference supply has failed.

SUPPORT OSCILLATOR

A power oscillator, OSC1758, is available for use as a reference generator for LVDT and RVDT transducers. It is capable of providing up to 7 volts rms at 1.4 VA.

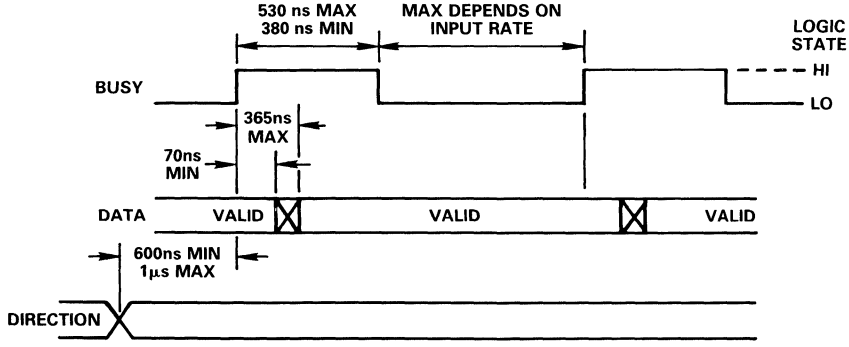
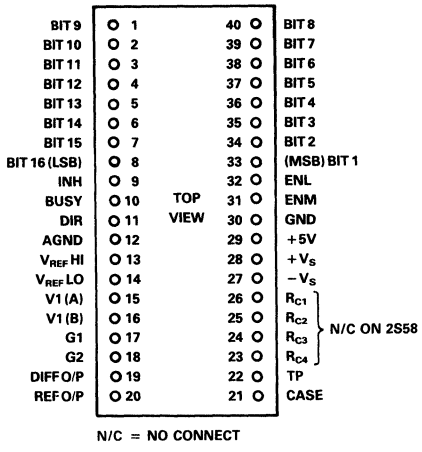


Figure 14. 2S56 Data Transfer Timing Diagram

PIN CONFIGURATIONS



N/C = NO CONNECT

MEAN TIME BETWEEN FAILURES (MTBF)

The predicted reliability of these converters is exceptionally high due to the extensive uses of LSI custom circuitry. Figure 15 shows the MTBF of the 4YZ options as calculated according to MIL HDBK 217D at various temperatures under ground benign environment. For MTBF calculations under other environments, please consult the factory.

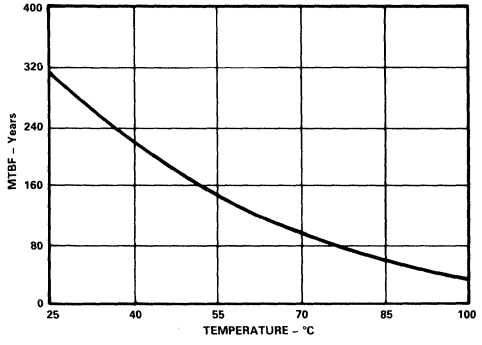


Figure 15.

PIN FUNCTION DESCRIPTION

$-V_S$	Main negative power supply.
$+V_S$	Main positive power supply.
+5 V	Logic power supply.
GND	Power supply ground. Digital ground.
Bit 1–14 (2S54) Bit 1–16 (2S56, 2S58))	Parallel output data bits.
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "Lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the output latches are being updated. Data should not be transferred from the converter while BUSY is "Hi."
$\overline{\text{ENABLE M}}$	The 8 most significant output data bits are set to a high impedance state by application of a logic "Hi."
$\overline{\text{ENABLE L}}$	The 6 least significant bits of a 2S54, or the 8 least significant bits of a 2S56 "and 2S58," are set to a high impedance state by application of a logic "Hi."
R_{C1} R_{C2}	Connections to R1, internal bridge completion resistor (2S54/2S56 only).
R_{C3} R_{C4}	Connections to R2, internal bridge completion resistor (2S54/2S56 only).
DIR	TTL output indicating the direction of movement of the transducer.
AGND	Analog ground.
V_{REF} HI V_{REF} LO	Input pins for the Reference signal.
V1 (A) V1 (B)	Input pins for the Signal.
G1 G2	A gain setting resistor, or a link, can be connected between these pins.
DIFF O/P	This is a V1 after scaling (V2).
REF O/P	This is the reference signal after the input buffer stage.
CASE	This should normally be grounded. Case can be taken to any voltage with a low impedance up to ±20 V.
TP	Test Point. Do not make connections to this pin.

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Preseal Burn In	64 Hours at +125°C
2. Precap Visual Inspection	In-House Criteria
3. Seal Test, Fine and Gross	In-House Criteria
4. Final Electrical Test	

Extended temperature range versions receive additional processing as follows:

4. Final Electrical Test	Performed at Maximum and Minimum Operating Temperatures

PROCESSING FOR HIGH RELIABILITY

All extended temperature range models are available with high reliability screening. The parts are identified with a B suffix, and will receive the following processing.

Process	Conditions
1. Preseal Burn In	64 Hours at +125°C
2. Precap Visual Inspection	MIL-STD-883, Method 2017
3. Temperature Cycling	10 Cycles, −65°C to +150°C
4. Constant Acceleration	5000G, Y1 Plane
5. Interim Electrical Tests	
6. Operating Burn In	96 Hours at +125°C
7. Seal Test, Fine and Gross	MIL-STD-883, Method 1014
8. Final Electrical Testing (Group A)	Performed at T_{min}, T_{AMB}, and T_{max}
9. External Visual Inspection	MIL-STD-883, Method 2009

NOTE: Test and screening data can be supplied. Further information on request.

OTHER TRANSDUCER INTERFACE PRODUCTS

2S80/2S81/2S82	10–16 Bit Variable Resolution Resolver to Digital Converter (Monolithic IC)
2S50	10 Bit + Sign, LVDT to Digital Converter (Hybrid)
OSC1758	Power Oscillator (Hybrid)
1S14/24/44/64	10-, 12-, 14-, and 16-Bit Resolver-to-Digital Converters with High Accuracy Velocity O/P
1S74	Variable Resolution (10 to 16 Bits) Resolver-to-Digital Converter with High Accuracy Velocity Output.
1S10/1S20/1S40/ 1S60/1S61	10-, 12-, 14- and Two 16-Bit Inductosyn* Resolver-to-Digital Converters (Hybrid)
5S70/72	Input Isolation Transformers for the 1S Series of Converters. Also Convert from Synchro Format.
IPA1764	Inductosyn Pre-Amplifier (Hybrid)

***Inductosyn is a trademark of Farrand Industries, Inc.**

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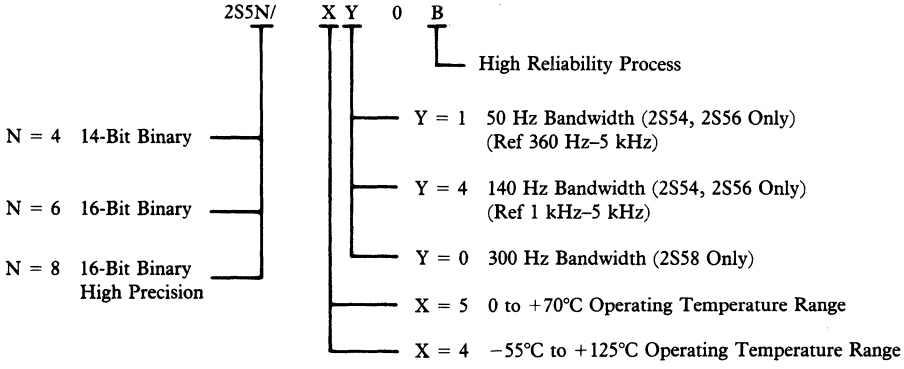
ORDERING INFORMATION



Variable Resolution, Monolithic Resolver-to-Digital Converter

2S80

FEATURES

Monolithic (BiMOS II) Tracking R/D Converter
40-Pin DIL Package
10-, 12-, 14- and 16-Bit Resolution Set by User
Ratiometric Conversion
Low-Power Consumption – 300mW typ
Dynamic Performance Set by User
High Max Tracking Rate 1040 rps (10 Bits)
Velocity Output
Military Temperature Range Version

APPLICATIONS

Brushless Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control
Military Servo Control

GENERAL DESCRIPTION

The 2S80 is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 40-pin, dual-in-line ceramic package. It is manufactured on a BiMOS II process that combines the advantages of CMOS logic and Bipolar high-accuracy linear circuits on the same chip.

The converter allows users **to select their own resolution and dynamic performance with external components.** This allows the users great flexibility in defining the converter that best suits their system requirements. The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

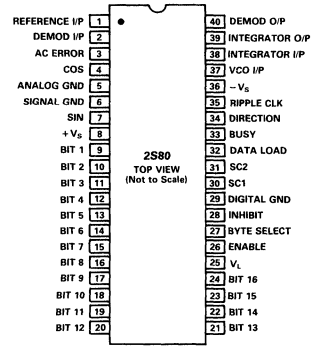
The 2S80 converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high-noise immunity and tolerance of lead length when the converter is remote from the resolver.

The 10-, 12-, 14- or 16-bit output word is in a three-state digital logic form available in 2 bytes on the 16 output data lines. BYTE SELECT, ENABLE and INHIBIT pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available.

The 2S80 operates over 50 to 20,000 Hertz reference frequency.

2S80 PIN CONFIGURATION



PRODUCT HIGHLIGHTS

Monolithic. A one-chip solution reduces the package size required and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the 2S80 to be 10, 12, 14 or 16 bits allowing the user to use the 2S80 with the optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and a tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low-cost preferred value resistors and capacitors and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization and velocity feedback data.

Low-Power Consumption. Typically only 300mW.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Information."

SPECIFICATIONS (typical at 25°C unless otherwise specified)

Model	2S80	Units	Notes
TYPICAL CONVERTER PERFORMANCE (Connected as shown in Figure 1)			
Resolution	10, 12, 14 or 16	bits	
Accuracy JD, SD Options	±8 + 1LSB	arc mins	Accuracy will be affected by the offset at the
KD, TD Options	±4 + 1LSB	arc mins	INTEGRATOR I/P.
LD, UD Options	±2 + 1LSB	arc mins	
Tracking Rate Range			
10-Bit Resolution	0 to 1040	rps	User Selected, max rate limited to 1/16 of the
12-Bit Resolution	0 to 260	rps	reference frequency.
14-Bit Resolution	0 to 65	rps	
16-Bit Resolution	0 to 16.25	rps	
Operating Frequency Range	50 to 20,000	Hz	
Repeatability of Position Output	1	LSB	
Bandwidth	User Selectable		
Velocity Signal			See "Using the Velocity Signal."
Linearity			
Over Full Range	±1	% of output	See VCO spec.
Reversion Error	±1	%	With power supplies adjusted for best performance.
Zero Offset	+6	mV	For max tracking rate range. Depends on VCO I/P resistor (R6).
Zero Offset Tempco	−22	µV/°C	For max tracking rate range. Depends on VCO I/P resistor (R6).
Gain Scaling Accuracy	±10	% FSD	
Output Voltage	±8	V dc	
Noise and Ripple			
at LSB Rate	2	mV	See section "Using the Velocity Output."
Dynamic Ripple (Peak)	1.5	% of mean output	
ANALOG INPUTS			
Protection	All analog inputs are diode protected against overvoltage at ±8V.		
REFERENCE INPUT			
Frequency	50–20,000	Hz	
Voltage Level Nominal	2	V rms	
Max	11	V peak	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
SIGNAL INPUTS (SIN, COS)			
Frequency	50–20,000	Hz	
Allowable Phase Shift			
(Signal to Reference)	10	Degrees	
Voltage Level	2, ±10%	V rms	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Maximum Voltage Nominal	±8	V	
DIGITAL INPUTS	TTL Compatible		Except DATA LOAD and SHORT CYCLE INPUTS.
INHIBIT			
Sense	Logic LO to inhibit		
Time to Data Stable (After Negative Going Edge of INHIBIT)	600	ns	
DATA LOAD			
Sense	Internally pulled up to +12V. Unconnected for normal operation. Logic LO allows data to be loaded into the counters from the data lines.		Connect when multiplexing the 2S80 or when using as a control transformer. Ensure data lines are in high impedance state when loading data.
SHORT CYCLE INPUTS (SC1, SC2)			
			Internally pulled up to $+V_S$.
	SC1	SC2	Used to select the resolution of the converter.
For 10-Bit Resolution	0	0	0 = Digital Ground. Drive low with open collector TTL.
For 12-Bit Resolution	0	1	1 = Open Circuit (internally pulled up through 100kΩ).
For 14-Bit Resolution	1	0	
For 16-Bit Resolution	1	1	
BYTE SELECT			
Sense Logic HI	8 MSBs selected on data lines 1 to 8. LS Byte selected on data lines 9 to 16.		The size of the LS Byte will be between 2 and 8 bits depending on the resolution selected.
Logic LO	LS Byte selected on data lines 1 to 8 and 9 to 16.		
Time to Data Available (After Change in State)	150 (typ), 450 (max)		ns

Model	2S80	Units	Notes
ENABLE			
Sense	Logic LO to enable position outputs. Logic HI position outputs in high impedance state.		
Enable and Disable Times	200 (typ), 550 (max)	ns	
ANALOG OUTPUTS			
Protection	Short-circuit output current limited to ± 8mA, ± 30%.		
Output Voltage Range, typ	+ 9 to − 9	V	With 1mA load.
max	+ 10.5 to − 10.5	V	
min	+ 8 to − 8	V	
DIGITAL OUTPUTS			
Format	V_L = + 5V	TTL Compatible	Voltage on V_L sets the voltage level of the digital outputs.
	V_L = + 12V	CMOS Compatible	
POSITION OUTPUTS			
Format	Three-state natural binary		
Resolution	10, 12, 14 or 16	bits	
Number of Data Lines	16		
Max Load	3	LSTTL	
Monotonicity			
JD, KD, SD, TD Options	Guaranteed to 14 bits		
LD and UD Options	Guaranteed to 16 bits		
DIRECTION			
Sense	Logic HI when counting up. Logic LO when counting down.		
Timing	Only changes, if required, at start of output position data cycle.		
Max Load	3	LSTTL	
RIPPLE CLOCK			
Sense	Positive going edge when counting up from all "1s" and when counting down from all "0s" as data changes.		
Timing	Edge occurs at least 300ns before change in DIR can occur.		
Width	300 (min)	ns	
Reset	By start of next data update.		
Max Load	3	LSTTL	
BUSY			
Sense	Logic HI when converter position output changing.		
Timing	Positive going edge 50ns before change in position output.		
Width typ	300	ns	
min	200	ns	
max	600	ns	
Max Load	3	LSTTL	
POWER SUPPLIES			The 2S80 may latch up if $+V_S$ is applied without $-V_S$.
Voltage Levels			
$+V_S$	+ 12 ± 10%	V	
$-V_S$	− 12 ± 10%	V	
$+V_L$	+ 5 to + 14	V	
Current			Over operating temperature range.
$+V_S$, $-V_S$ at 12V	12 (typ), 23 (max)	mA	
$+V_S$, $-V_S$ at 13.2V	19 (typ), 30 (max)	mA	
$+V_L$	0.5 (typ), 1.5 (max)	mA	
GENERAL			
Operating Temperature Range			
JD, KD, LD Options	0 to + 70	°C	
SD, TD, UD Options	− 55 to + 125	°C	
Storage Temperature Range (All Options)	− 60 to + 150	°C	
Weight	0.2 (5)	oz (grams)	

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CONVERTER CHARACTERISTICS

Model	2S80	Units	Notes
RATIO MULTIPLIER			
Function	AC ERROR output represents the difference between the angle at the SIN and COS inputs compared to the position output angle.		
AC ERROR Output Scaling			
10-Bit Resolution	177.6	mV/bit	
12-Bit Resolution	44.4	mV/bit	
14-Bit Resolution	11.1	mV/bit	
16-Bit Resolution	2.775	mV/bit	
Accuracy			Maximum over temp. range.
JD and SD Options	±8	arc mins	
KD and TD Options	±4	arc mins	
LD and UD Options	±2	arc mins	
Differential Nonlinearity			
JD, KD, SD, TD Options	<1	Bits in 14	Guaranteed monotonic to 14 bits when connected in tracking mode.
LD, UD Options	<1	Bits in 16	Guaranteed monotonic to 16 bits when connected in tracking mode.
PHASE SENSITIVE DETECTOR			Specified over operating frequency range. Tested at 1kHz.
Output Offset Voltage	12 (max)	mV	
Gain of Signal (dc Out, rms In)			
In Phase w.r.t. Reference	−0.9 ±2%		
In Quadrature w.r.t. Reference	±0.02 (max)		
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
INTEGRATOR			
Open Loop Gain at 10kHz	60 ±3	dB	
Dead Zone Current	100	nA/LSB	See section "Integrator."
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	60 (typ), 150 (max)	nA	
Output Voltage Range (min)	+8 to −8	V	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
VCO			
Maximum Rate	1.1	MHz	
VCO Rate	7.4 ±10%	kHz/μA	With ±12V supplies.
VCO Rate Tempco	−0.05	%/°C	
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	120 (typ), 300 (max)	nA	
Input Bias Current Tempco	−0.55	nA/°C	
Input Voltage Range	−8 to +8	V	
Linearity of Absolute Rate			
Over Full Range	±1 (typ), ±3 (max)	%	
Over 0 to 50% of Max Range	+1 (max)	%	
Reversion Error	<3 (max)	%	Symmetrical power supplies.
Sensitivity of Reversion Error to Symmetry of Power Supplies	8	%/V of Asymmetry	See section "Using the Velocity Output."

Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1] . . . . . 0V to +14V dc
$-V_S$ . . . . . 0V to −14V dc
$+V_L$ . . . . . 0V to $+V_S$
Reference . . . . . +14V to $-V_S$
Sin . . . . . +14V to $-V_S$
Cos . . . . . +14V to $-V_S$
Any Logical Input . . . . . −0.4V to $+V_L$ dc
Demodulator Input . . . . . +14V to $-V_S$
Integrator Input . . . . . +14V to $-V_S$
VCO Input . . . . . +14V to $-V_S$

CAUTION:

1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

OPERATION OF THE CONVERTER

When connected in a circuit such as is shown in Figure 1 the 2S80 operates as a tracking resolver-to-digital converter and forms a type 2 closed loop system. This means that the output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

Because the conversion depends on the ratio of the input signals the 2S80 is remarkably tolerant of input amplitude and frequency (there is no need of an accurate, stable oscillator to produce the reference signal). The inclusion of a phase sensitive detector in the conversion loop ensures a high immunity to signals that are not coherent or are in quadrature with the reference signal.

Two major areas of the 2S80 specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the state of the inputs SC1 and SC2 to be 10, 12, 14 or 16 bits and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

Position Output

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

As the digital output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changes with a change in direction.

Both the RIPPLE CLOCK pulse and the DIRECTION data are unaffected by the application of the INHIBIT.

The static accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effect of offset signals at the INTEGRATOR INPUT (which can be trimmed out) and with the following conditions: input signal amplitudes are within 5% of the nominal values; signal and reference frequency is within the specified operating range; phase shift between signal and reference is less than 10 degrees; signal and reference waveform harmonic distortion is less than 10%.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the 2S80 can be used well outside these operating conditions providing the following points are observed.

Signal Amplitude (Sine and Cosine Inputs)

The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The 2S80 will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

Reference Voltage Level

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept below the absolute maximum voltage.

The 2S80 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

Harmonic Distortion

The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9V rms. (For example, a square wave should be 1.9V peak.)

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

Velocity Signal

The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR OUTPUT Pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

DC Error Signal

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is therefore proportional to the error between the input angle and the output digital angle. This is the DC ERROR of the converter; and as the converter is a type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in test".

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be $\pm$ 12V and must not be reversed. If one rail is connected without the other, the converter will not operate and may "latch up". In this case, the removal of both rails is necessary in order for the converter to function correctly again. The voltage applied to V_L can be $+5V$ to $+V_S$.

It is suggested that decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Suggested values of 100nF (ceramic) and 10μF (tantalum). Decoupling capacitors of 100nF and 10μF should also be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and SIGNAL GROUND as shown in Figure 7 and described in section "CONNECTING THE RESOLVER". The two signal ground wires from the resolver should be joined at the SIGNAL GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GROUND and ANALOG GROUND are connected

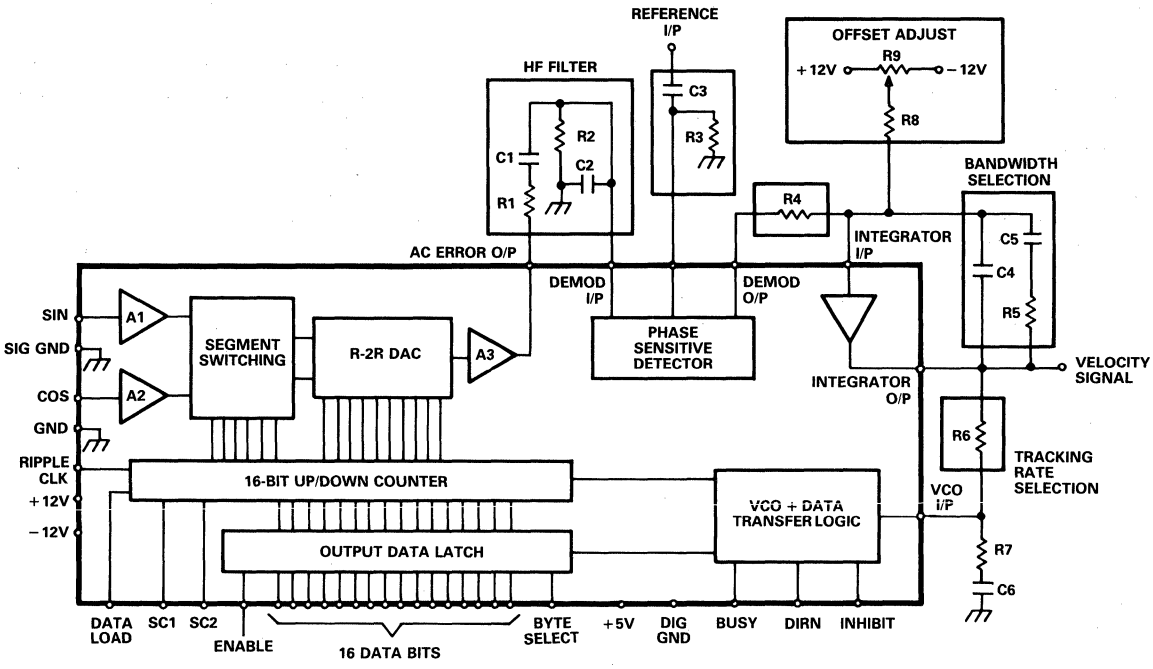


Figure 1. 2S80 Connection Diagram

internally. ANALOG GROUND and DIGITAL GROUND must be connected externally.

The external components required should be connected as shown in Figure 1.

SELECTING THE RESOLUTION

The resolution of the 2S80 can be selected to be 10, 12, 14 or 16 bits by use of the short cycling inputs SC1 and SC2. The required resolution can be selected as shown in the specification section.

The choice of resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO respectively (see section "COMPONENT SELECTION"). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, a period of uncertainty will exist before position and velocity data is valid.

COMPONENT SELECTION

The following instructions describe how to select the external components to the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE".

1. HF Filter (R1, R2, C1, C2)

The function of the HF filter is to reduce the amount of noise present on the signal inputs to the 2S80, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted – in which case R2 = R3 and C1 = C3, calculated below – but their use is particularly recommended if noise from a switch mode motor drive is present.

Values should be chosen so that

$$R1 = R2 \leq 56k\Omega$$

$$C1 = C2 = \frac{1}{2\pi\, R1\, f_{REF}}$$

and f_{REF} = Reference frequency (Hz)

This filter gives an attenuation of 3 times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
If R1, C2 are fitted then:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\,\Omega$$

If R1, C2 are not fitted then:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\,\Omega$$

where E_{DC} = 160×10^{-3} for 10 bits resolution
= 40×10^{-3} for 12 bits
= 10×10^{-3} for 14 bits
= 2.5×10^{-3} for 16 bits
= Scaling at the DC ERROR in volts

3. AC Coupling of Reference Input (R3, C3)
Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

$R3 = 100k\Omega$

$$C3 > \frac{1}{10^5 \times f_{REF}}$$

4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate the velocity output will be 8V.

   Decide on your required maximum tracking rate, "T", in revolutions per second. Note that "T" must not exceed the specified maximum tracking rate or 1/16 of the reference frequency.

$$R6 = \frac{5.92 \times 10^7}{T \times p}\ k\Omega$$

   where p = bit per rev
   = 1,024 for 10 bits resolution
   = 4,096 for 12 bits
   = 16,384 for 14 bits
   = 65,536 for 16 bits

5. Closed Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the Closed Loop 3dB Bandwidth (f_{BW}) required ensuring that

$$f_{REF} > 2.5 \times f_{BW}$$

   Typical values may be 100Hz for 400Hz reference frequency and 500 to 1000Hz for 5kHz reference frequency.

   b. Select C4 so that

$$C4 = \frac{20.2 \times 10^{-3}}{R6 \times f_{BW}^2}$$

   with R6 in kΩ and f_{BW} in Hz selected above.

   c. C5 is given by

$$C5 = 5 \times C4$$

   d. R5 is given by

$$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\ \Omega$$

6. VCO Phase Compensation
   The following values of C6 and R7 should be fitted.

   C6 = 470pF R7 = 68Ω

7. Offset Adjust
   Offset and bias current at the integrator input can cause an additional positional offset at the output of the converter of 1 arc min typical, 5.3 arc mins maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.

   If fitted, the following values of R8 and R9 should be used: R8 = 4.7MΩ, R9 = 1MΩ potentiometer.

   To adjust for zero offset, ensure the resolver is disconnected and all the other external components are fitted. Connect the COS pin to the REFERENCE INPUT and the SIN pin to the SIGNAL GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

   The potentiometer may be replaced by select on test resistors if preferred.

PIN FUNCTIONS

REFERENCE I/P	Input pin for the Reference Signal.
DEMOD I/P	Demodulator input pin.
AC ERROR O/P	Output of Ratio Multiplier.
COS	Input pin for Cosine signal from resolver.
ANALOG GROUND	Power ground.
SIGNAL GROUND	Ground pin for signals from resolver.
SIN	Input pin for Sine signal from resolver.
$+V_S$	Main positive power supply.
BIT 1 – BIT 16	Parallel output data bits.
V_L	Logic power supply.
ENABLE	Logic "HI" sets the output data bits to a high impedance state, a logic "LO" presents the data in the latches to the output pins.
BYTE SELECT	Selects the data output bits presented on data bits 1 to 8. Logic "HI" will present the 8 most significant bits; a logic "LO" will present the least significant byte.
INHIBIT	Logic "LO" inhibits the data transfer from the counter to the output latches.
DIGITAL GROUND	Ground pin for digital circuitry.
SC1, SC2	Logic inputs used for selecting the resolution of the converter.
DATA LOAD	Logic "LO" allows data to be loaded into the counters.
BUSY	Converter BUSY. A logic "HI" indicates that the output latches are being updated and data should not be transferred.
DIRECTION	Logic output indicating the direction of rotation of the input signals.
RIPPLE CLOCK	A negative going pulse whenever the output of the converter changes from all "1s" top all "0s" or the converse.
$-V_S$	Main negative power supply.
VCO I/P	Input pin to VCO.
INTEGRATOR I/P	Input pin of Integrator.
INTEGRATOR O/P	Output pin of Integrator.
DEMOD O/P	Output pin of Demodulator.

DATA TRANSFER

To transfer data the INHIBIT input should be used. The data will be valid 600ns after the application of a logic "Lo" to the INHIBIT. This is regardless of the time when the INHIBIT is applied and allows time for an active BUSY to clear. By using the ENABLE input the two bytes of data can be transferred after which the INHIBIT should be returned to a logic "Hi" state to enable the output latches to be updated.

BUSY Output:

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of an LSB and the internal counter is incremented or decremented.

INHIBIT Input:
The INHIBIT logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the INHIBIT automatically generates a BUSY pulse to refresh the output data.

ENABLE Input:
The ENABLE input determines the state of the output data. A logic "Hi" maintains the output data pins in the high impedance condition, and application of a logic "Lo" presents the data in the latches to the output pins. The operation of the ENABLE has no effect on the conversion process.

BYTE SELECT Input:
The BYTE SELECT input selects the byte of position data to be presented at the data output bits 1 to 8. The least significant byte will be presented on data output bits 9 to 16 (with the ENABLE input taken to a logic "Lo") regardless of the state of the BYTE SELECT pin. Note that when the 2S80 is used with a resolution less than 16 bits the unused data lines are pulled to a logic "Lo". A logic "Hi" on the BYTE SELECT input will present the eight most significant data bits on data output Bits 1 and 8. A logic "Lo" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

RIPPLE CLOCK Output:
As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution, or a pitch, of the input has been completed. The pulse has a minimum width of 300ns and is reset by the start of the next data update cycle.

DIRECTION Output:
The DIRECTION (DIR) logic output indicates the direction of the input rotation, and this data is valid in advance of the RIPPLE CLOCK pulse and stays valid until the direction changes. This is the start of the next data update cycle – if the direction of rotation of the inputs has changed – and will be at least 300ns after the rising edge of the RIPPLE clock (see Figure 2).

The DIR and RC outputs are unaffected by the state of the INHIBIT input.

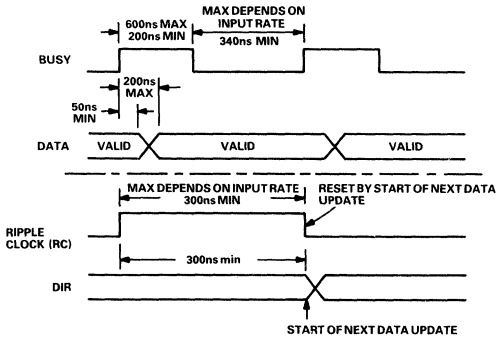


Figure 2. Timing Diagram

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE

The 2S80 allows the user great flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the external components shown in Figure 1, and the section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the 2S80 and the variations in the dynamic performance available to the user.

Loop Compensation
The 2S80 (connected as shown in Figure 1) behaves as a type 2 tracking servo loop where the VCO/counter combination and the Integrator perform the two integration functions inherent in a type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize any type 2 loop to avoid the loop gain characteristic crossing the 0dB axis with 180° of additional phase lag, as shown in Figure 4. This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

The 2S80 does not have to be connected as tracking converter, parts of the circuit can be used independently. This is particularly true of the Ratio Multiplier which can be used as a control transformer.

A block diagram of the 2S80 is given in Figure 3.

Ratio Multiplier
The Ratio Multiplier is the input section of the 2S80 and compares the signal from the resolver inputs, θ, to the digital angle, ϕ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by a mechanical device known by that name.

The AC ERROR signal is given by

$$A1 \sin(\theta - \phi) \sin\omega t.$$

where $\omega = 2\pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage is 14.5 times

So for 2V rms inputs signals
AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{p}\right) \times A1$$

where p = bits per rev
= 1,024 for 10 bits resolution
= 4,096 for 12 bits
= 16,384 for 14 bits
= 65,536 for 16 bits

Giving AC ERROR output
= 178mV rms/bit @ 10 bits resolution
= 44.5mV rms/bit @ 12 bits
= 11.125mV rms/bit @ 14 bits
= 2.78mV rms/bit @ 16 bits

The Ratio Multiplier will operate in exactly the same way whether the 2S80 is connected as a tracking converter or as a control transformer, where data is preset into the counters using the DATA LOAD pin.

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any DC offset at this point. Note, however, that the PSD of the 2S80 is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noisy environments, and the user is advised to fit a simple HF filter R1, C2 prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator.

Values of the components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The Phase Sensitive Demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times \text{(DEMODULATOR INPUT rms voltage)}$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error Scaling = 160mV/bit (10 bits resolution)
= 40mV/bit (12 bits resolution)
= 10mV/bit (14 bits resolution)
= 2.5mV/bit (16 bits resolution)

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the 2S80 to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from "flickering" (i.e., continually toggling by ±1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ) feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 bit. In order to ensure that this feedback "hysteresis" is set to 1LSB the input current to the integrator must be scaled to be 100nA/bit. So,

$$R4 = \frac{\text{DC Error Scaling (mV/bit)}}{100\ (\text{nA/bit})}\ \text{M}\Omega$$

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB of extra error will be added for each 100nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION".

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocked either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the reset period the input continues to be integrated although the reset period is constant at 400ns.

The VCO rate is fixed for a given input current by the VCO scaling factor,

$= 7.4\text{kHz}/\mu\text{A}$

The tracking rate in rps per μA of VCO input current can be found by dividing the VCO scaling factor by the number of LSB changes per rev (i.e., 4096 for 12-bit resolution).

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT pin and the VCO input current. Thus to achieve a 5V output at 100 rps (6000 rpm) and 12-bit resolution the VCO input current must be:

$(100 \times 4096)/(7400) = 55.3\mu\text{A}$

Thus, R6 would be set to: $5/(55.3 \times 10^{-6}) = 90\text{k}\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

Velocity Offset Voltage = R6 × (VCO bias current)

The temperature coefficient of this offset is given by

Velocity Offset Tempco = R6 × (VCO bias current tempco)

where the VCO bias current tempco is typically −0.55nA/°C.

The maximum recommended rate for the VCO is 1.1MHz which sets the maximum possible tracking rate.

Since the maximum voltage swing available at the integrator output is ±8V, this implies that the minimum value for R6 is 54kΩ. As

$$\text{Max Current} = \frac{1.1 \times 10^6}{7.4 \times 10^3} = 149\mu\text{A}$$

$$\text{Min Value } R_6 = \frac{8}{149 \times 10^{-6}} = 54\text{k}\Omega$$

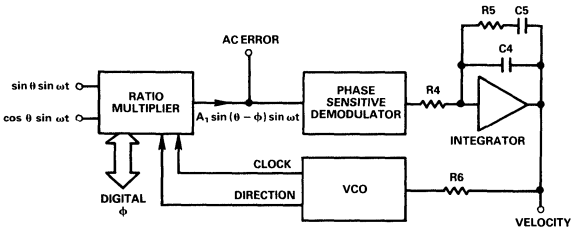


Figure 3. 2S80 Functional Diagram

Transfer Function

By selecting components using the method outlined in the section "Component Selection" the converter will have a critically damped time response and maximum phase margin. The Closed-Loop Transfer Function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\,(1 + s_N)}{(s_N + 2.4)\,(s_N^2 + 3.4\,s_N + 5.8)}$$

where, s_N, the normalized frequency variable is

$$s_N = \frac{2}{\pi}\,\frac{s}{f_{BW}}$$

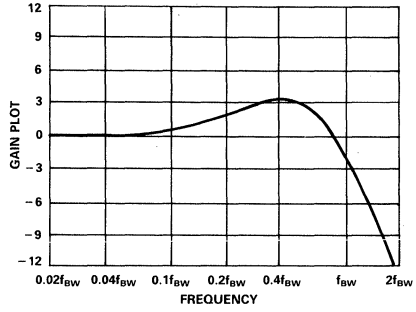


Figure 4. 2S80 Gain Plot

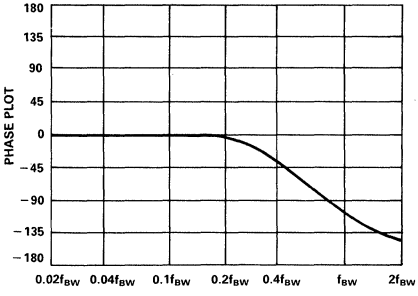


Figure 5. 2S80 Phase Plot

and f_{BW} is the closed-loop 3dB bandwidth (selected by the choice of external components).

The acceleration constant, K_A, is given approximately by

$$K_A = 6 \times (f_{BW})^2 \quad sec^{-2}$$

The normalized gain and phase diagrams are given in Figures 4 and 5.

The small signal step response is shown in Figure 6. The time from the step to the first peak is t_1 and the t_2 is the time from the step until the converter as settled to 1LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}} \times \frac{R}{12}$$

where R = resolution, i.e., 10, 12, 14 or 16.

The large signal step response (for steps greater than 10 degrees) applies when the error voltage will exceed the linear range of the converter. Typically the converter will take 3 times longer to reach the first peak for a 179 degrees step.

The response to a velocity step, the velocity output will exhibit the same time response characteristics as outlined above for the position output.

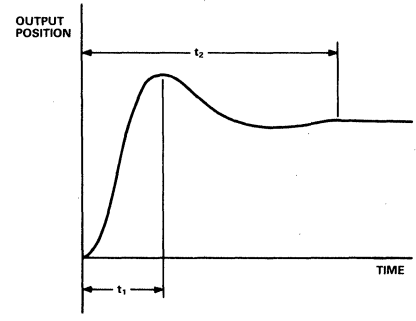


Figure 6. 2S80 Small Step Response

APPLICATIONS

USING THE 2S80 AS A CONTROL TRANSFORMER

The ratio multiplier section of the 2S80 can be used independently to the rest of the converter to perform the function of Control Transformer. In this mode the signal from the resolver inputs, θ, is compared to a digital angle, ϕ, loaded into the counters. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. To use the device in this way the DATA LOAD pin is used.

Applying a logic "Lo" to the DATA LOAD pin will allow data to be loaded into the counters of the converter from the data lines. It is important that the data lines are placed in the high impedance state before loading data.

To operate the 2S80 as a tracking resolver-to-digital converter the DATA LOAD pin should be left unconnected as it is pulled high internally to +12V.

CAUSES OF ADDITIONAL ERROR

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will be typically 1 arc minute over the operating temperature range.

A description of how to adjust for zero offset is given in the section "COMPONENT SELECTION" and the circuit required is shown in Figure 1.

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

$$\text{Error} = 0.53\ a.b \text{ arc minutes}$$

where a = differential phase shift in degrees
and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltge, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section "CONNECTING THE RESOLVER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's static accuracy.

However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (rps)} \times \text{Phase Shift (Degs)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20 degrees, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000} = 0.088 \text{ degrees}$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

USING THE VELOCITY SIGNAL

The signal at the INTEGRATOR OUTPUT pin relative to the ANALOG GROUND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in place of a velocity transducer. Although the conversion loop of the 2S80 includes a digital section there is an additional totally analog feedback loop around the velocity signal. This ensures that there is no digital effects on the output signal and that the loop is closed even when the input signals are such that the digital output does not change.

A better quality velocity signal will be achieved if the following points are considered.

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion Error.
   If necessary, the reversion error can be reduced by a simple trimming circuit. Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO. The reversion error can be nulled by varying one supply rail relative to the other.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using separate screened twisted pair cable for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fitted before the Phase Sensitive Demodulator (as described in the section HF FILTER).

   A resolver is chosen that has a low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the 2S80 with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   The signal voltages are 2V rms to prevent a ripple at the LSB switching rate. This is because the 1LSB of analog feedback that prevents the output from flickering will be incorrectly scaled (see section "INTEGRATOR").

   If the above precautions are taken, a very good noise and ripple performance is obtainable making the 2S80 velocity signal usable in very noisy environments, for instance in motor drive applications with PWM switching noise.

   The positional error curve of the converter and the resolver will result in an apparent acceleration when the resolver is rotating at a constant velocity. The main result of this will be a ripple on the velocity signal twice per revolution.

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 7.

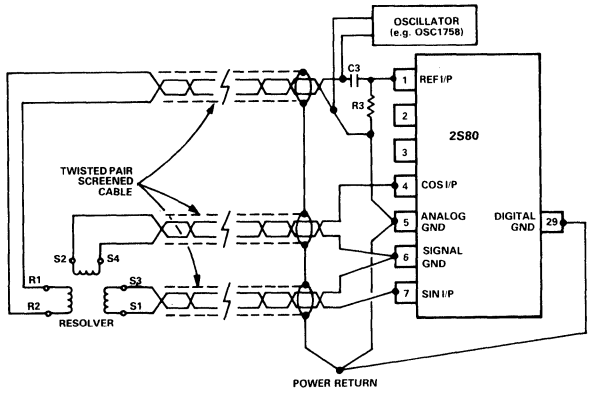


Figure 7. Connecting the 2S80 to a Resolver

In cases where the reference phase relative to the input signals from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency $= \frac{1}{2\pi R C}$

By altering the value of R2 the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

For signal and reference voltages greater than 2V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

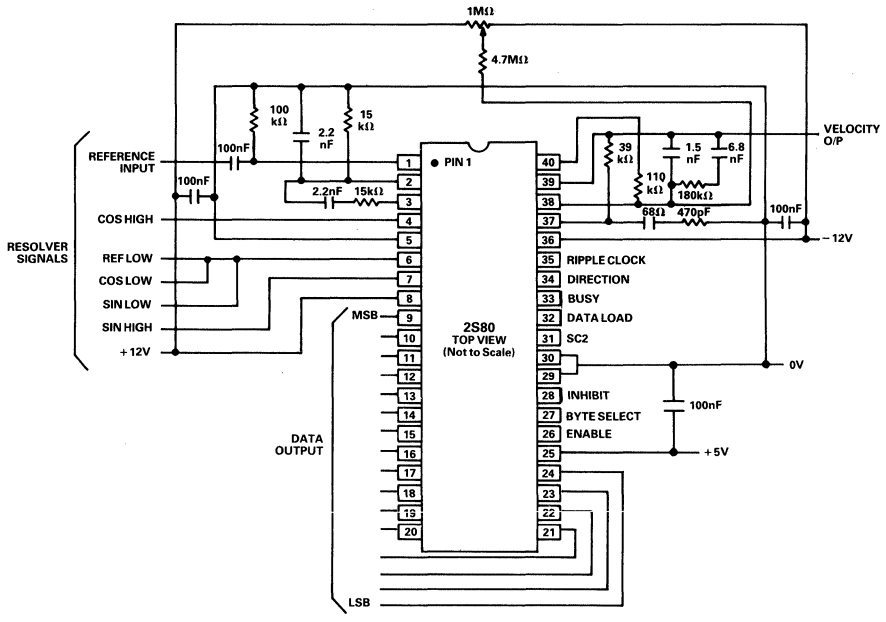


Figure 8.

TYPICAL CIRCUIT CONFIGURATION

Figure 8 shows a typical circuit configuration for the 2S80 in a 12-bit resolution mode. Values of the external components have been chosen for a reference frequency of 5kHz and to give a maximum tracking rate of 260 rps and a bandwidth of 520Hz. The resistors are 0.125W, 5% tolerance preferred values. The capacitors are 100V ceramic, 10% tolerance components.

An offset adjustment potentiometer is included at the integrator input to remove the offset error. Obviously this can be left out of the circuit if the extra inaccuracy can be tolerated.

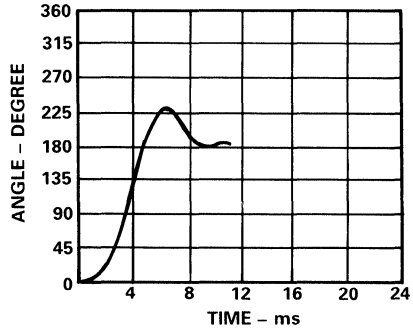


Figure 9. Large Step Response Curves for Typical Circuit Shown in Figure 8

ORDERING INFORMATION

Model	Accuracy (Arc mins)	Operating Temperature Range (°C)	Package Option*
2S80JD	8	0 to +70	D-40
2S80KD	4	0 to +70	D-40
2S80LD	2	0 to +70	D-40
2S80SD	8	−55 to +125	D-40
2S80TD	4	−55 to +125	D-40
2S80UD	2	−55 to +125	D-40

*See Section 14 for package outline information.

ANALOG DEVICES

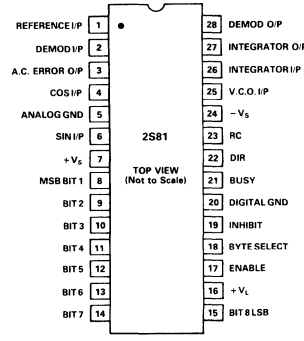
Low-Cost, Monolithic 12-Bit Resolver-to-Digital Converter

2S81

FEATURES
Low Cost
Monolithic Construction
28-Pin DIP Package
Ratiometric Conversion
Low Power Consumption: 300mW typical
Dynamic Performance Set by User
High Tracking Rate: 260 rps max
Velocity Output

APPLICATIONS
Brushless Motor Control
Programmable Limit Switches
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

2S81 PIN CONFIGURATION



5

GENERAL DESCRIPTION

The 2S81 is a monolithic 12-bit tracking resolver-to-digital converter packaged in a 28-pin DIP. It is manufactured in Analog Devices' proprietary BiMOS II process which combines high-density and low-power CMOS logic with high-accuracy bipolar linear circuitry.

The converter can track resolver signals at rates up to 260 revolutions per second (15,600 rpm). Users can set the converter's dynamic performance with external components, providing greater flexibility in tailoring the converter to suit system requirements.

The 2S81 converts resolver format input signals into a 12-bit natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of long lead lengths when the converter is located remotely from the resolver. The 12-bit output word is in a three-state digital logic form, available in 2 bytes on the 8 output data lines. BYTE SELECT and INHIBIT pins ensure easy data transfer. In addition, output pins are available to permit the use of external counters to count cycle or pitch. An analog signal proportional to velocity is also available.

PRODUCT HIGHLIGHTS

Monolithic: The single-chip construction reduces package size and increases inherent reliability.

Low Cost: The use of a single integrated circuit to perform the conversion ensures low cost.

Ratiometric Tracking Conversion: Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerates harmonic distortion in the reference and input signals.

Dynamic Performance Set by User: By selecting external resistor and capacitor values, the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low-cost preferred value resistors and capacitors.

Velocity Output: An analog signal proportional to velocity is linear to 1% (typical). This can be used in place of a velocity transducer in many applications to provide loop stabilization and velocity feedback data.

MODELS AVAILABLE

The 2S81 operates over 0 to +70°C temperature range. The reference frequency can range from 400 to 20,000Hz.

SPECIFICATIONS (typical at 25°C unless otherwise specified)

Model	2S81JD	Units	Notes
OVERALL CONVERTER SPECIFICATIONS (CONNECTED AS SHOWN IN FIGURE 1)			
Resolution	12	Bits	
Accuracy	± 30 + 1LSB	Arc Minutes	Accuracy will be Affected by the Offset at the INTEGRATOR I/P.
Tracking Rate Range	0 to 260 (max)	rps	User Selected, Max Rate Limited at Lower Operating Frequencies.
Operating Frequency Range	400 to 20,000	Hz	
Repeatability of Position Output	1	LSB	
Bandwidth	User Selectable		
Velocity Signal			See "Using the Velocity Signal"
Linearity Over Full Range	± 1 (typ), ± 3 (max)	%	
Over 0 to 6000 rpm	± 1 (max)	%	
Reversion Error	± 5 (max)	%	Symmetry of $-V_S$ and $+V_S$ Power Supplies to be within ± 5%.
	± 2 (max)	%	With $-V_S$ Adjusted for Best Performance.
Zero Offset (for 260 rps Max Tracking Rate)	± 6 (typ) + 16 (max)	mV	Depends on VCO I/P Resistor (R6).
Zero Offset Tempco (for 260 rps Max Tracking Rate)	− 22	μV/°C	Depends on VCO I/PResistor (R6).
Gain Scaling Accuracy	± 10	% FSD	
Output Voltage	± 8	V dc	
Noise and Ripple (av-pk)	1.5	%	See Section "Using the Velocity Signal"
ANALOG INPUTS			
Protection	All Analog Inputs Are Diode Protected Against Overvoltage at ± 8V		
REFERENCE INPUT			
Frequency	400 – 20,000	Hz	
Voltage Level Nominal	2	V rms	
max	11	V peak	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
SIGNAL INPUTS (SIN, COS)			
Frequency	400 – 20,000	Hz	
Allowable Phase Shift (Signal to Reference)	10	Degrees	
Voltage Level	2, ± 10%	V rms	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Maximum Voltage Nominal	± 8	V	
DIGITAL INPUTS	TTL-Compatible		
INHIBIT			
Sense	Logic LO to Inhibit		
Time to Data Stable (After Negative Going Edge of INHIBIT)	1	μs	
BYTE SELECT			
Sense	Logic HI Selects 8MSBs on Pins 8-15 Logic LO Selects 4LSBs on Pins 8-11; Pins 12-15 Are Logic LO		
Data Available (After Change in State)	150 (typ), 450 (max)	ns	
ENABLE			
Sense	Logic LO to Enable Position Outputs Logic HI Position Outputs in High Impedance State		
Enable and Disable Times	200 (typ), 550 (max)	ns	
ANALOG OUTPUTS			
Protection	Short Circuit Output Current Limited to ± 8mA, ± 30% Output Voltage Range Will Be Degraded for Currents >3mA		
Output Voltage Range (typ)	+ 9 to − 9	V	
(max)	+ 10.5 to − 10.5	V	
(min)	+ 8 to − 8	V	
DIGITAL OUTPUTS			
Format	V_L = + 5V TTL Compatible V_L = + 12V CMOS Compatible		Voltage on V_L Sets the Voltage Level of Digital Outputs.

Model	2S81JD	Units	Notes
POSITION OUTPUTS			
Format	Three-State Natural Binary		
Resolution	12	Bits	
Number of Data Lines	8		Pins 8 to 15
Max Load	3	LSTTL	
Monotonicity	Guaranteed		
DIRECTION (DIR)			
Sense	Logic "HI" When Counting Up Logic "LO" When Counting Down		
Timing	Only Changes, if Required, at Start of Output Position Data Update Cycle		
Max Load	3	LSTTL	
RIPPLE CLOCK (RC)			
Sense	Positive Going Edge When Counting Up from All "1s" and When Counting Down from All "0s" as Data Changes		
Timing	Edge Occurs at Least 300ns Before Change in DIR Can Occur		
Width (min)	300	ns	
Reset	By Start of Next Data Update		
Max Load	3	LSTTL	
BUSY			
Sense	Logic "HI" When Converter Position Output Changing		
Timing	Positive Going Edge 50ns Before Change in Position Output		
Width (typ)	300	ns	
(min)	200	ns	
(max)	600	ns	
Load, (max)	3	LSTTL	
POWER SUPPLIES			The Device May Latch Up If $+V_S$ is Applied without $-V_S$.
Voltage Levels			
$+V_S$	$+12 \pm 10\%$	V	
$-V_S$	$-12 \pm 10\%$	V	
$+V_L$[5]	+5 to +14	V	
Current			
$+V_S$	12 (typ), 23 (max)	mA	
$-V_S$	12 (typ), 23 (max)	mA	
$+V_L$	0.5 (typ), 1.5 (max)	mA	
Power Dissipation	300 (typ), 600 (max)	mW	
GENERAL			
Operating Temperature Range	0 to +70	°C	
Storage Temperature Range	−65 to +150	°C	
Weight	0.2 (5)	Oz. (Grams)	

Model	2S81JD	Units	Notes
CONVERTER CHARACTERISTICS			
RATIO MULTIPLIER			
Function	AC ERROR Output Represents the Difference between the Angle at the SIN and COS Inputs Compared to the Position Output Angle		
AC Error Output Scaling	44.4	mV/Bit	
Accuracy	30	Arc Minutes	
Differential Nonlinearity	±0.25 (max)	LSB	
PHASE SENSITIVE DETECTOR			Specified Over the Operating Frequency Range. Tested at 1kHz.
Output Offset Voltage (max)	15	mV	
Gain of Signal (dc out, rms in)			
In Phase w.r.t. Reference	−0.9 ±2%		
In Quadrature w.r.t. Reference	±0.02 (max)		
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
INTEGRATOR			
Open Loop Gain at 10kHz	60 ±3	dB	
Output Impedance at 10kHz (max)	0.5	Ω	
Dead Zone Current	100	nA/LSB	See Section "Integrator"
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	60 (typ), 150 (max)	nA	
Output Voltage Range (min)	+8 to −8	V	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
VCO			
Maximum Rate	1.1	MHz	
VCO Rate	7.4 ±10%	kHz/μA	
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	120 (typ), 300 (max)	nA	
Input Bias Current Tempco	−0.55	nA/°C	
Input Voltage Range	+8 to −8	V	
Reversion Error	±5	%	
Linearity of Absolute Rate	+3	%	
Sensitivity of VCO Rate in "Up Direction" to $-V_S$	−7	%/V	
Sensitivity of VCO Rate in "Down Direction" to $-V_S$	+2	%/V	

NOTE
Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1] . . . . . 0V to +14V dc
$-V_S$ . . . . . 0V to −14V dc
$+V_L$ . . . . . 0V to $+V_S$
Reference . . . . . +14V to $-V_S$
Sin . . . . . +14V to $-V_S$
Cos . . . . . +14V to $-V_S$
Any Logic Input . . . . . −0.4V to $+V_L$ dc
Demodulator Input . . . . . +14V to $-V_S$
Integrator Input . . . . . +14V to $-V_S$
VCO Input . . . . . +14V to $-V_S$

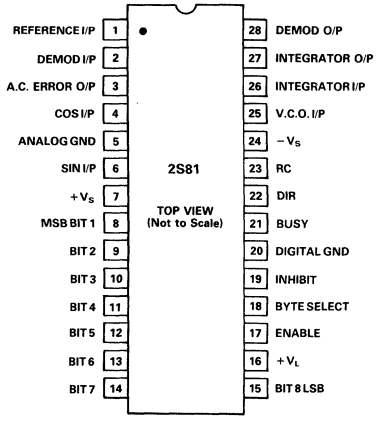
CAUTION:
1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

ORDERING INFORMATION

Model	Package Option*	Temperature Range	Operating Frequency Range
2S81JD	D-28	0 to +70°C	400 to 20,000Hz

*See Section 14 for package outline information.

PIN CONFIGURATION



OPERATION OF THE CONVERTER

When connected in a circuit such as is shown in Figure 1 the 2S81 operates as a tracking resolver-to-digital converter and forms a type 2 closed loop system. This means that the digital output will automatically follow the input for speeds up to the maximum tracking rate, set by the choice of external components. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

As the digital output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is *always* valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changes with a change in direction.

Both the RIPPLE clock pulse and DIRECTION data are unaffected by the application of the $\overline{\text{INHIBIT}}$.

Position Output

The resolver shaft position is represented at the converter output by a natural binary digital word.

The static angular accuracy quoted is the worst case error that can occur over the full operating temperature range with the following input conditions:

a) Signal input amplitudes within 5% of the nominal values.

b) Signal and reference frequency within the specified operating range.

c) Phase shift between signal and reference less than 10 degrees.

d) Signal and reference waveform harmonic distortion less than 10 percent.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the converters can be used well outside these operating conditions providing the following points are observed.

Signal Amplitude (Sine and Cosine Inputs)

The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The 2S81 will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

Reference Voltage Level

The amplitude of the reference signal applied to the converter's input is noncritical; however, it is essential that the zero crossing points are maintained in the correct place to drive the converter's phase sensitive detector.

The 2S81 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

Harmonic Distortion

The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9 volts rms. (For example – a square wave should be 1.9V peak.)

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

Velocity Signal

The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR OUTPUT pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

DC Error Signal

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is therefore proportional to the error between the input angle and the output digital angle. This is the DC ERROR of the converter; and as the converter is a type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators this voltage can be used as a "built-in test".

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be $\pm$ 12V and must not be reversed. If one rail is connected without the other, the converter will not operate and may "latch up". In this case the removal of both rails is necessary in order for the converter to function correctly again. The voltage applied to V_L can be +5V to $+V_S$.

It is suggested that decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Suggested values are 100nF (ceramic) and 10μF (tantalum). Decoupling capacitors of 100nF and 10μF should also be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and ANALOG GROUND as shown in Figure 7 and described in section "CONNECTING THE RESOLVER". The two signal ground wires from the resolver should be joined at the ANALOG GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using twisted pair cables with the sine, cosine and reference signals twisted separately.

The external components required should be connected as shown in Figure 1.

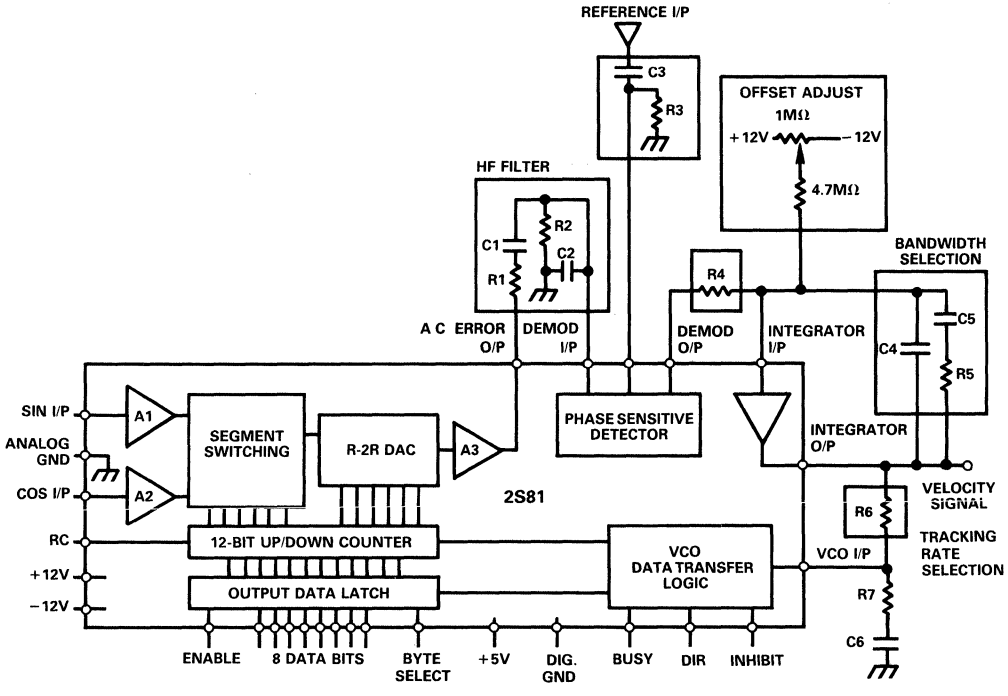


Figure 1. 2S81 Connection Diagram

COMPONENT SELECTION

The following instructions describe how to select the external components to the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used and a 5 percent tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE".

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to reduce the amount of noise present on the signal inputs to the 2S81 reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted – in which case R2 = R3 and C1 = C3, calculated below – but their use is particularly recommended if noise from a switch mode motor drive is present.

   Values should be chosen so that

   $R1 = R2 = 50k\Omega$ (max)

   $$C1 = C2 = \frac{1}{2\pi f_{REF} R1}$$

   and f_{REF} = Reference frequency (Hz)

   This filter gives an attenuation of 3 times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
   If R1, C2 are fitted then: $R4 = 120k\Omega$

   If R1, C2 are not fitted then: $R4 = 390k\Omega$

3. AC Coupling of Reference Input (R3, C3)
   Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

   $R3 = 100k\Omega$

   $$C3 > \frac{1}{10^5 \times f_{REF}}$$

4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate the velocity output will be 8 volts.

   Decide on your required maximum tracking rate, "T" in revolutions per second. Note that "T" must not exceed 260 rps and 1/8 of the reference frequency.

   $$R6 = \frac{14.5 \times 10^3}{T} \ k\Omega$$

   This gives a scale factor of $\frac{T}{8}$ rps/volt

5. Closed-Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the Closed-Loop 3dB Bandwidth (B_{CL}) required ensuring that

      $f_{REF} > 2.5 \times B_{CL}$

      Typical values may be 100Hz for 400Hz reference frequency and 500 to 1000Hz for 5kHz reference frequency.

   b. Select C4 so that

      $$C4 = \frac{20.4 \times 10^{-3}}{R6 \times B_{CL}^{2}}$$

      with R6 in kΩ and B_{CL} in Hz selected above.

   c. C5 is given by

      $C5 = 5 \times C4$

   d. R5 is given by

      $$R5 = \frac{4}{2 \times \pi \times B_{CL} \times C5} \ \Omega$$

6. VCO Phase Compensation
   The following values of C6 and R7 should be fitted.

   C6 = 470pF R7 = 68Ω.

7. Offset Adjust
   Input bias current at the integrator input can cause an additional positional offset at the output of the converter of 4 arc mins typical, 10 arc mins maximum. If this can be tolerated then the 4.7MΩ resistor and the 1MΩ potentiometer can be omitted from the circuit.

   To adjust for zero offset, ensure the resolver is disconnected and all the other external components are fitted. Connect COS to the REFERENCE INPUT and SIN to the ANALOG GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

   The potentiometer may be replaced by select on test resistors if preferred.

DATA TRANSFER

BUSY Output:
The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of an LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input:
The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

NOTE: With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

ENABLE Input:
The ENABLE input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance condition, and application of a logic "LO" presents the data in the latches to the output pins. The operation of the ENABLE has no effect on the conversion process.

BYTE SELECT Input:
The BYTE SELECT input selects the byte of position data to be presented at the data output pins. A logic "HI" on the BYTE SELECT input will present the 8 most significant data bits on pins 8 to 15 when the ENABLE input is taken to a logic "LO". A logic "LO" will present the 4 least significant data bits on pins 8 to 11 and place a logic "LO" on pins 12 to 15 (with the ENABLE input taken to a logic "LO").

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

To transfer data the INHIBIT input should be used. The data will be valid 600ns after the application of a logic "LO" to the INHIBIT. This is regardless of the time when the INHIBIT is applied and allows time for an active BUSY to clear. By using the BYTE SELECT input the two bytes of data can be transferred after which the INHIBIT should be returned to a logic "HI" state to enable the output latches to be updated.

RIPPLE CLOCK (RC) and DIRECTION (DIR) Outputs: As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution or a pitch of the input has been completed. The pulse has a minimum width of 300ns and is reset by the start of the next data update cycle.

The DIRECTION (DIR) logic output indicates the direction of the input rotation, and this data is valid in advance of the RIPPLE CLOCK pulse and stays valid until the direction changes. This is the start of the next data update cycle – if the direction of rotation of the inputs has changed – and will be at least 300ns after the rising edge of the RIPPLE CLOCK (see Figure 2).

The DIR and RC outputs are unaffected by the state of the INHIBIT input.

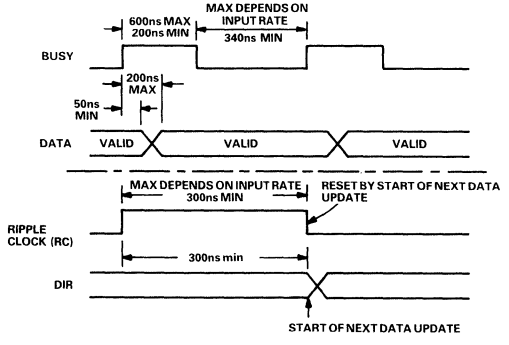


Figure 2. Timing Diagram

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE

The 2S81 allows the user great flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the exernal components shown in Figure 1, and the section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the 2S81 and the variations in the dynamic performance available to the user.

Loop Compensation

The 2S81 (connected as shown in Figure 1) behaves as a type 2 tracking servo loop where the VCO/counter combination and the Integrator perform the 2 integration functions inherent in a type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize any type 2 loop to avoid the loop gain characteristic crossing the 0dB axis with 180 degrees of additional phase lag, as shown in Figure 4. This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

A block diagram of the 2S81 is given in Figure 3.

Ratio Multiplier

The Ratio Multiplier is the input section of the 2S81 and compares the signal from the resolver inputs, θ, to the output digital angle, ϕ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by a mechanical device known by that name.

The AC ERROR signal is given by

AC ERROR OUTPUT = A1 sin $(\theta - \phi)$ sinωt.

where $\omega = 2\pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage, is 14.5 times

So for 2V rms input signals

AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{4096}\right) \times A1$$

$$= 44.5\text{mV/rms/bit}$$

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any DC offset at this point. Note, however, that the PSD of the 2S81 is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noise environments, and the user is advised to fit a simple HF filter (R1, C2) prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator.

Values of the components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The Phase Sensitive Demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times (\text{DEMODULATOR INPUT rms voltage})$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error = 40mV/bit

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the 2S81 to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from 'flickering' (i.e., continually toggling by ± 1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ) feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 bit. In order to ensure that this feedback "hysteresis" is set to 1LSB the input current to the integrator must be scaled to be 100nA/bit. So

$$R4 = \frac{40\text{mV/bit}}{100\text{nA/bit}} = 400\text{k}\Omega$$ (390kΩ is the nearest preferred value).

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB (5.3 arc mins) of extra error will be added for each 100nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION".

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocked either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the reset period the input continues to be integrated although the reset period is constant at 400ns.

The VCO rate is fixed for a given input current by the VCO scaling factor,

$= 7.4\text{kHz}/\mu\text{A}$

This is equivalent to a tracking rate of 7400/4096 = 1.807 rps per μA of VCO input current.

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT pin and the VCO input current. Thus to achieve a 5 volt output at 100 rps (6000 rpm) the VCO input current must be:

$(100 \times 4096)/(7400) = 55.4\mu\text{A}$

Thus R6 would be set to: $5/(55.4 \times 10^{-6}) = 90\text{k}\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

Velocity Offset Voltage = R6 × (VCO bias current)

The temperature coefficient of this offset is given by

Velocity Offset Tempco = R6 × (VCO bias current tempco)

where the VCO bias current tempco is typically −0.55nA/°C.

The maximum recommended rate for the VCO is 1.1MHz which sets the maximum possible tracking rate at

$$1.1 \times \frac{10^6}{4096} \text{ revs/second}$$

Since the maximum voltage swing available at the integrator output is ±8 volts, this implies that the minimum value for R6 is 54kΩ. As

$$\text{Max Current} = \frac{1.1\ 10^6}{7.4 \times 10^3} = 149\mu\text{A}$$

$$\text{Min Value } R_6 = \frac{8}{149 \times 10^{-6}} = 54\text{k}\Omega$$

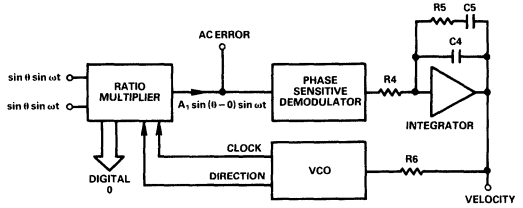


Figure 3. 2S81 Functional Diagram

Transfer Function

By selecting components using the method outlined in the section "Component Selection" the converter will have a critically damped time response and maximum phase margin. The Closed-Loop Transfer Function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\ (1+s_N)}{(s_N+2.4)\ (s_N^2+3.4\ s_N+5.8)}$$

where, s_N, the normalized frequency variable is

$$s_N = \frac{2}{\pi}\ \frac{s}{f_{BW}}$$

and f_{BW} is the closed-loop 3dB bandwidth (selected by the choice of external components).

The acceleration constant, K_A is given approximately by

$$K_A = 6 \times (f_{BW})^2 \quad \text{sec}^{-2}$$

The normalized gain and phase diagrams are given in Figures 4 and 5.

The small signal step response is shown in Figure 6. The time from the step to the first peak is t_1 and the t_2 is the time from the step until the converter has settled to 1LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}}$$

The large signal step response (for steps greater than 10 degrees) applies when the error voltage will exceed the linear range of the converter. Typically the converter will take 3 times longer to reach the first peak for a 179° step.

In response to a velocity step the velocity output will exhibit the same time response characteristics as outlined above for the position output.

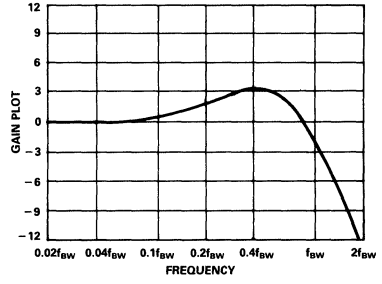


Figure 4. 2S81 Gain Plot

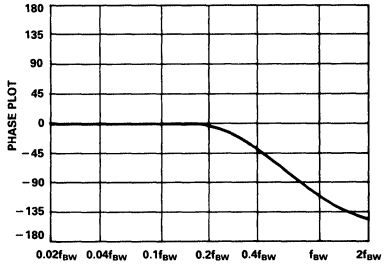


Figure 5. 2S81 Phase Plot

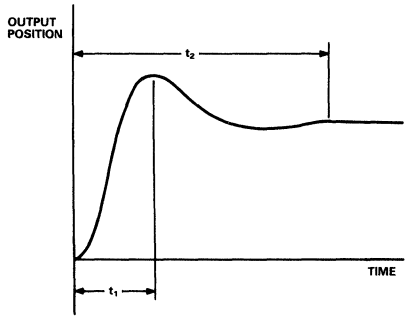


Figure 6. 2S81 Small Step Response

APPLICATIONS

Causes of Additional Error

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will be a maximum of 10 arc minutes over the operating temperature range, and if it can be tolerated in the performance of the converter, then the 4.7MΩ resistor and the 1MΩ potentiometer shown in Figure 1 can be omitted. (An offset of 40mV at the input to the integrator will cause an additional error of 1LSB in the accuracy of the converter.)

A description of how to adjust for zero offset is given in the section "COMPONENT SELECTION" and the circuit required is shown in Figure 1.

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and will cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

$$\text{Error} = 0.53\ a.b \text{ arc minutes}$$

where a = differential phase shift in degrees
and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section "CONNECTING THE RESOLVER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically effect the converter's static accuracy.

However, when rotating, most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

Using the Velocity Signal

The signal at the INTEGRATOR OUTPUT pin relative to the ANALOG GROUND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in place of a velocity transducer. Although the conversion loop of the 2S81 includes a digital section there is an additional totally analog feedback loop around the velocity signal. This ensures that there is no digital effects on the output signal and that the loop is closed even when the input signals are such that the digital output does not change.

A better quality velocity signal will be achieved if the following points are considered.

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion Error.
   If necessary, the reversion error can be reduced by a simple trimming circuit. Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO. Because the sensitivity of the VCO rate to $-V_S$ depends on the direction of rotation, the reversion error can be reduced by varying the magnitude of $-V_S$. By trimming a reversion error of less than 1% is achievable.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using screened separate twisted pair cables for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fitted before the Phase Sensitive Demodulator (as described in the section HF FILTER).

   A resolver is chosen that has a low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the 2S81 with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   The signal voltages are 2V rms to prevent a ripple at the LSB switching rate. This is because the 1LSB of analog feedback that prevents the output from flickering will be incorrectly scaled (see section "INTEGRATOR").

   If the above precautions are taken, a very good noise and ripple performance is obtainable making the 2S81 velocity signal usable in very noisy environments, for instance in motor drive applications with PWM switching noise.

   The positional error curve of the converter and the resolver will result in an apparent acceleration when the resolver is rotating at a constant velocity. The main result of this will be a ripple on the velocity signal twice per revolution.

Connecting the Resolver

The recommended connection circuit is shown in Figure 7.

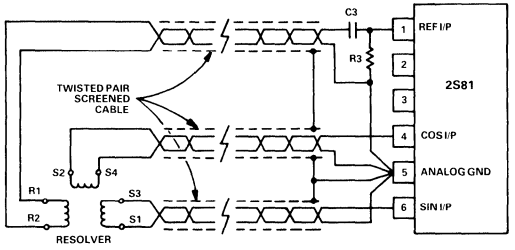


Figure 7. Connecting the 2S81 to a Resolver

In cases where the reference phase relative to the input signals from the resolver requires adjustment this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency $= \frac{1}{2\pi R C}$

By altering the value of R2 the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

For signal and reference voltages greater than 2V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

Typical Circuit Configuration

Figure 8 shows a typical circuit configuration for the 2S81. Values of the external components have been chosen for a reference frequency of 5kHz and to give a maximum tracking rate of 260 rps and a bandwidth of 520Hz. The resistors are 0.25W (except for the 4.7MΩ which is 0.5W) 5 percent tolerance preferred values. The capacitors are 100V ceramic 5 percent tolerance components.

An offset adjustment potentiometer is included at the integrator input to remove the offset error. Obviously this can be left out of the circuit if the extra inaccuracy can be tolerated.

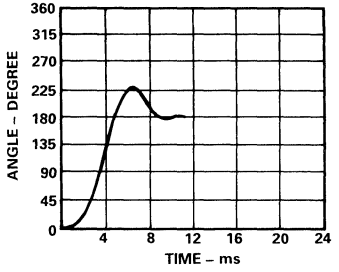


Figure 9. Large Step Response Curves for Typical Circuit Shown in Figure 8

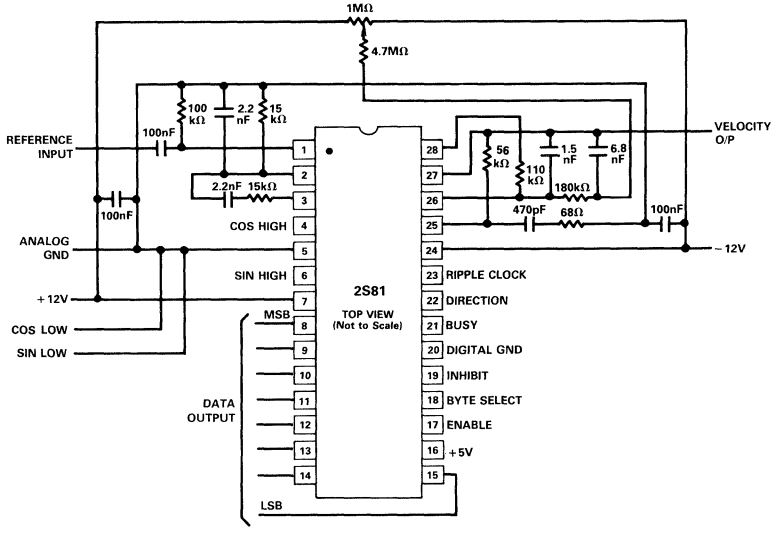


Figure 8. Typical Circuit for the 2S81

ANALOG DEVICES

Variable Resolution, Monolithic Resolver-to-Digital Converter

2S82

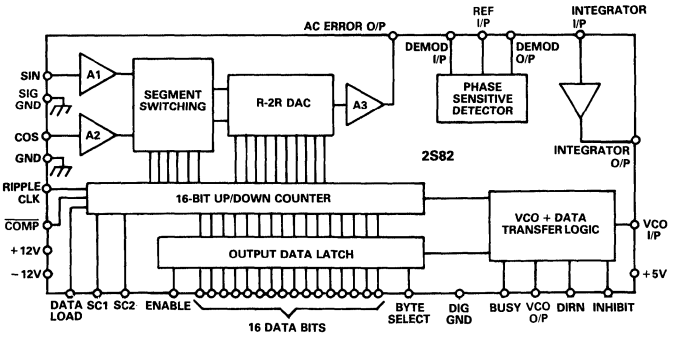
FEATURES

Monolithic (BiMOS II) Tracking R/D Converter
44-Pin J Leaded Chip Carrier (LCC)
10-, 12-, 14- and 16-Bit Resolution Set by User
Ratiometric Conversion
Low Power Consumption – 300mW typ
Dynamic Performance Set by User
High max Tracking Rate 1040 rps (10 Bits)
Velocity Output
VCO Output (Inter LSB Output)
Data Complement Facility
Military Temperature Range Version

APPLICATIONS

Brushless Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

2S82 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 2S82 is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 44-pin J leaded chip carrier package. Two extra functions are provided in the new surface mount package – COMPLEMENT and VCO OUTPUT. All other functions are identical to the 2S80.

The converter allows users to select their own resolution and dynamic performance with external components. This allows the users great flexibility in defining the converter that best suits their system requirements. The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The 2S82 converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of lead length when the converter is remote from the resolver.

The 10-, 12-, 14- or 16-bit output word is tristate available in two bytes on the 16 output data lines. BYTE SELECT, ENABLE and INHIBIT pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available.

Reference frequency operating range for the 2S82 is 50Hz to 20,000Hz.

PRODUCT HIGHLIGHTS

Monolithic. A one-chip surface mount package solution reduces the package size required and increases reliability.

Resolution Set by User. Two control pins are used to select the resolution of the 2S82 to be 10, 12, 14 or 16 bits allowing the user to use the 2S82 with optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and a tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values, the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost, preferred value resistors and capacitors, and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization and velocity feedback data.

Low Power Consumption. Typically only 300mW.

ORDERING INFORMATION

Model	Accuracy (Arc mins)	Operating Temperature Range	Package Options
2S82HP	22 + 1LSB	0 to +70°C	Plastic LCC
2S82JP	8 + 1LSB	0 to +70°C	Plastic LCC
2S82KP	4 + 1LSB	0 to +70°C	Plastic LCC
2S82LP	2 + 1LSB	0 to +70°C	Plastic LCC

SPECIFICATIONS (typical at 25°C unless otherwise specified)

Model	2S82	Units	Notes
TYPICAL CONVERTER PERFORMANCE (Connected as shown in Figure 1)			
Resolution	10, 12, 14 or 16	bits	
Accuracy HP Option	±22 + 1LSB	arc mins	Accuracy will be affected by the offset at the INTEGRATOR I/P.
JP Option	±8 + 1LSB	arc mins	
KP Option	±4 + 1LSB	arc mins	
LP Option	±2 + 1LSB	arc mins	
Tracking Rate Range			
10-Bit Resolution	0 to 1040	rps	User Selected, max rate limited to 1/16 of the reference frequency.
12-Bit Resolution	0 to 260	rps	
14-Bit Resolution	0 to 65	rps	
16-Bit Resolution	0 to 16.25	rps	
Operating Frequency Range	50 to 20,000	Hz	
Repeatability of Position Output	1	LSB	
Bandwidth	User Selectable		
Velocity Signal			See "Using the Velocity Signal."
Linearity			
Over Full Range	±1	% of output	See VCO spec.
Reversion Error	±1	%	With power supplies adjusted for best performance.
Zero Offset	+6	mV	For max tracking rate range. Depends on VCO I/P resistor (R6).
Zero Offset Tempco	−22	μV/°C	For max tracking rate range. Depends on VCO I/P resistor (R6).
Gain Scaling Accuracy	±10	% FSD	
Output Voltage	±8	V dc	
Noise and Ripple			
at LSB Rate	2	mV	See section "Using the Velocity Output."
Dynamic Ripple (Peak)	1.5	% of mean output	
ANALOG INPUTS			
Protection	All analog inputs are diode protected against overvoltage at ±8V.		
REFERENCE INPUT			
Frequency	50–20,000	Hz	
Voltage Level Nominal	2	V rms	
Max	11	V peak	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
SIGNAL INPUTS (SIN, COS)			
Frequency	50–20,000	Hz	
Allowable Phase Shift (Signal to Reference)	10	Degrees	
Voltage Level	2, ±10%	V rms	
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Maximum Voltage Nominal	±8	V	
DIGITAL INPUTS	TTL Compatible		Except DATA LOAD and SHORT CYCLE INPUTS.
INHIBIT			
Sense	Logic LO to inhibit		See section "INHIBIT Input."
Time to Data Stable (After Negative Going Edge of INHIBIT)	600	ns	
DATA LOAD			
Sense	Internally pulled up to +12V. Unconnected for normal operation. Logic LO allows data to be loaded into the counters from the data lines.		Connect when multiplexing the 2S82 or when using as a control transformer. Ensure data lines are in high impedance state when loading data.
SHORT CYCLE INPUTS (SC1, SC2)			Internally pulled up to $+V_S$.
	SC1	SC2	Used to select the resolution of the converter.
For 10-Bit Resolution	0	0	0 = Digital Ground. Drive low with open collector TTL.
For 12-Bit Resolution	0	1	1 = Open Circuit (internally pulled up through 100kΩ).
For 14-Bit Resolution	1	0	
For 16-Bit Resolution	1	1	
BYTE SELECT			
Sense Logic HI	8 MSBs selected on data lines 1 to 8. LS Byte selected on data lines 9 to 16.		The size of the LS Byte will be between 2 and 8 bits depending on the resolution selected.
Logic LO	LS Byte selected on data lines 1 to 8 and 9 to 16.		
Time to Data Available (After Change in State)	150 (typ), 450 (max)		ns

Model	2S82	Units	Notes
$\overline{\text{COMPLEMENT}}$	Internally pulled up to +12V. Unconnected for normal operation. Logic LO to activate.		
$\overline{\text{ENABLE}}$			
Sense	Logic LO to enable position outputs. Logic HI position outputs in high impedance state.		
Enable and Disable Times	200 (typ), 550 (max)	ns	
ANALOG OUTPUTS			
Protection	Short-circuit output current limited to ±8mA, ±30%.		
Output Voltage Range, typ	+9 to −9	V	With 1mA load.
max	+10.5 to −10.5	V	
min	+8 to −8	V	
DIGITAL OUTPUTS			
Format	V_L = +5V	TTL Compatible	Voltage on V_L sets the voltage level of the digital outputs.
	V_L = +12V	CMOS Compatible	
POSITION OUTPUTS			
Format	Three-state natural binary		
Resolution	10, 12, 14 or 16	bits	
Number of Data Lines	16		
Max Load	3	LSTTL	
Monotonicity			
HP, JP, KP Options	Guaranteed to 14 bits		
LP Option	Guaranteed to 16 bits		
DIRECTION			
Sense	Logic HI when counting up. Logic LO when counting down.		
Timing	Only changes, if required, at start of output position data cycle.		
Max Load	3	LSTTL	
RIPPLE CLOCK			
Sense	Positive going edge when counting up from all "1s" and when counting down from all "0s" as data changes.		
Timing	Edge occurs at least 300ns before change in DIR can occur.		
Width	300 (min)	ns	
Reset	By start of next data update.		
Max Load	3	LSTTL	
BUSY			
Sense	Logic HI when converter position output changing.		
Timing	Positive going edge 50ns before change in position output.		
Width typ	300	ns	
min	200	ns	
max	600	ns	
Max Load	3	LSTTL	See Section "BUSY Output."
POWER SUPPLIES			The 2S82 may latch up if $+V_S$ is applied without $-V_S$.
Voltage Levels			
$+V_S$	+12 ±10%	V	
$-V_S$	−12 ±10%	V	
$+V_L$	+5 to +14	V	
Current			Over operating temperature range.
$+V_S$, $-V_S$ at 12V	12 (typ), 23 (max)	mA	
$+V_S$, $-V_S$ at 13.2V	19 (typ), 30 (max)	mA	
$+V_L$	0.5 (typ), 1.5 (max)	mA	
GENERAL			
Operating Temperature Range			
HP, JP, KP, LP Options	0 to +70	°C	
Storage Temperature Range (All Options)	−25 to +85	°C	
Weight	0.2 (5)	oz (grams)	
VCO OUTPUT	±3 (±10%)	V/LSB	The VCO output swings between ±3V depending on the resolver direction.

CONVERTER CHARACTERISTICS

Model	2S82	Units	Notes
RATIO MULTIPLIER			
Function	AC ERROR output represents the difference between the angle at the SIN and COS inputs compared to the position output angle.		
AC ERROR Output Scaling			
10-Bit Resolution	177.6	mV/bit	
12-Bit Resolution	44.4	mV/bit	
14-Bit Resolution	11.1	mV/bit	
16-Bit Resolution	2.775	mV/bit	
Accuracy			Maximum over temp. range.
HP Option	±22	arc mins	
JP Option	±8	arc mins	
KP Option	±4	arc mins	
LP Option	±2	arc mins	
Differential Nonlinearity			
HP, JP, KP Options	<1	Bits in 14	Guaranteed monotonic to 14 bits when connected in tracking mode.
LP Option	<1	Bits in 16	Guaranteed monotonic to 16 bits when connected in tracking mode.
PHASE SENSITIVE DETECTOR			Specified over operating frequency range. Tested at 1kHz.
Output Offset Voltage	12 (max)	mV	
Gain of Signal (dc Out, rms In)			
In Phase w.r.t. Reference	−0.9 ± 2%		
In Quadrature w.r.t. Reference	±0.02 (max)		
Input Bias Current	60 (typ), 150 (max)	nA	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
INTEGRATOR			
Open Loop Gain at 10kHz	60 ± 3	dB	
Dead Zone Current	100	nA/LSB	See section "Integrator."
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	60 (typ), 150 (max)	nA	
Output Voltage Range (min)	+8 to −8	V	
Input Impedance	>1	MΩ	
Input Voltage Range	+8 to −8	V	
VCO			
Maximum Rate	1.1	MHz	
VCO Rate	7.4 ± 10%	kHz/μA	With ± 12V supplies.
VCO Rate Tempco	−0.05	%/°C	
Input Offset Voltage	1 (typ), 5 (max)	mV	
Input Bias Current	120 (typ), 300 (max)	nA	
Input Bias Current Tempco	−0.55	nA/°C	
Input Voltage Range	−8 to +8	V	
Linearity of Absolute Rate			
Over Full Range	±1 (typ), ±3 (max)	%	
Over 0 to 50% of Max Range	+1 (max)	%	
Reversion Error	<3 (max)	%	Symmetrical power supplies.
Sensitivity of Reversion Error to Symmetry of Power Supplies	8	%/V of Asymmetry	See section "Using the Velocity Output."

Specifications subject to change without notice.

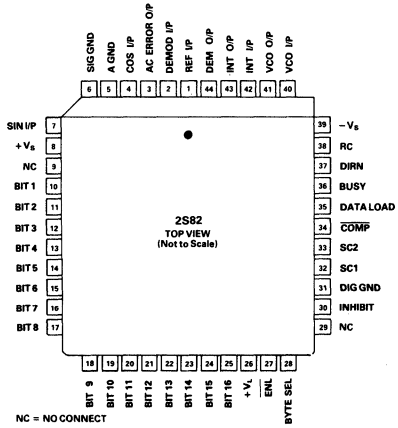
ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +14V dc
$-V_S$	0V to −14V dc
$+V_L$	0V to $+V_S$
Reference	+14V to $-V_S$
Sin	+14V to $-V_S$
Cos	+14V to $-V_S$
Any Logical Input	−0.4V to $+V_L$ dc
Demodulator Input	+14V to $-V_S$
Integrator Input	+14V to $-V_S$
VCO Input	+14V to $-V_S$

NOTE

[1]**CAUTION** – Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.

PIN CONFIGURATION



OPERATION OF THE CONVERTER

When connected in a circuit such as is shown in Figure 1, the 2S82 operates as a tracking resolver-to-digital converter and forms a type 2 closed loop system. This means that the output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

Because the conversion depends on the ratio of the input signals, the 2S82 is remarkably tolerant of input amplitude and frequency (there is no need of an accurate, stable oscillator to produce the reference signal). The inclusion of a phase sensitive detector in the conversion loop ensures a high immunity to signals that are not coherent or are in quadrature with the reference signal.

Two major areas of the 2S82 specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the state of the inputs SC1 and SC2 to be 10, 12, 14 or 16 bits, and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

Position Output

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

As the digital output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changes with a change in direction.

Both the RIPPLE CLOCK pulse and the DIRECTION data are unaffected by the application of the INHIBIT.

The static accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effect of offset signals at the INTEGRATOR INPUT (which can be trimmed out) and with the following conditions: input signal amplitudes are within 5% of the nominal values; signal and reference frequency is within the specified operating range; phase shift between signal and reference is less than 10 degrees; signal and reference waveform harmonic distortion is less than 10%.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the 2S82 can be used well outside these operating conditions providing the following points are observed.

Signal Amplitude (Sine and Cosine Inputs)

The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The 2S82 will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

Reference Voltage Level

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept below the absolute maximum voltage.

The 2S82 will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

Harmonic Distortion

The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9V rms. (For example, a square wave should be 1.9V peak.)

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

Velocity Signal

The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR OUTPUT pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

DC Error Signal

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is therefore proportional to the error between the input angle and the output digital angle. This is the DC ERROR of the converter; and as the converter is a type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in test."

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be $\pm$ 12V and must not be reversed. If one rail is connected without the other, the converter will not operate and may "latch up." In this case, the removal of both rails is necessary in order for the converter to function correctly again. The voltage applied to V_L can be $+5V$ to $+V_S$.

It is suggested that decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Suggested values of 100nF (ceramic) and 10μF (tantalum). Decoupling capacitors of 100nF and 10μF should also be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and SIGNAL GROUND as shown in Figure 7 and described in section "CONNECTING THE RESOLVER". The two signal ground wires from the

resolver should be joined at the SIGNAL GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GROUND and ANALOG GROUND are connected internally. ANALOG GROUND and DIGITAL GROUND must be connected externally.

The external components required should be connected as shown in Figure 1.

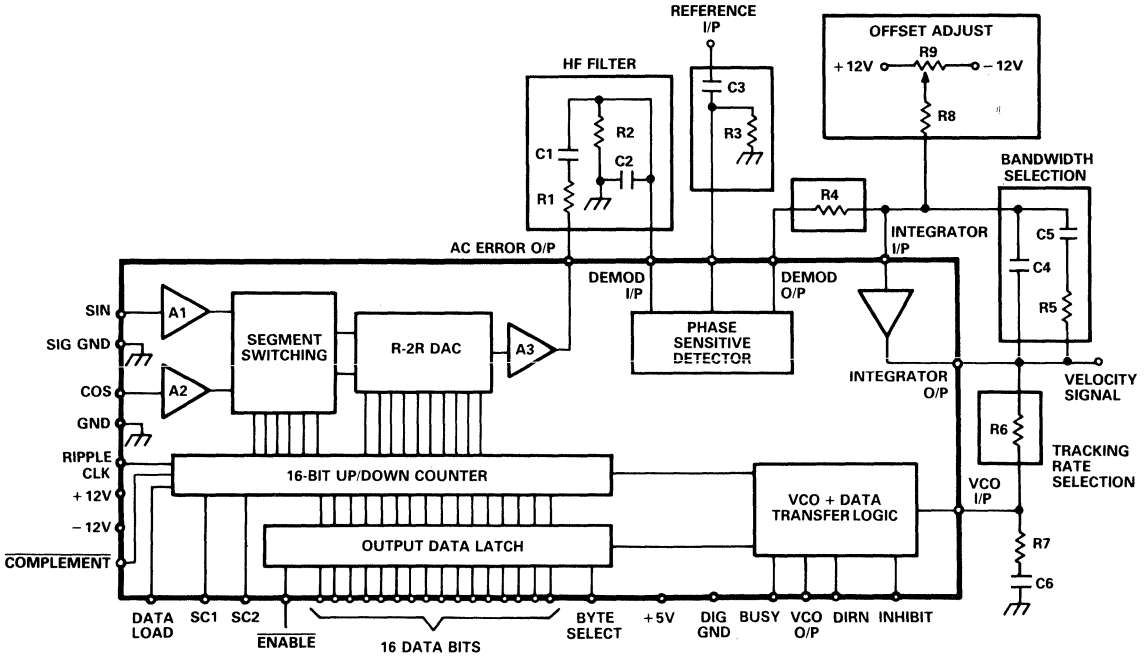


Figure 1. 2S82 Connection Diagram

SELECTING THE RESOLUTION

The resolution of the 2S82 can be selected to be 10, 12, 14 or 16 bits by use of the short cycling inputs SC1 and SC2. The required resolution can be selected as shown in the specification section.

The choice of resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO respectively (see section "COMPONENT SELECTION"). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, a period of uncertainty will exist before position and velocity data is valid.

COMPONENT SELECTION

The following instructions describe how to select the external components to the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE."

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to reduce the amount of noise present on the signal inputs to the 2S82, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted – in which case R2 = R3 and C1 = C3, calculated below – but their use is particularly recommended if noise from a switch mode motor drive is present.

   Values should be chosen so that

   $$R1 = R2 \leq 56k\Omega$$

   $$C1 = C2 = \frac{1}{2\pi\, R1\, f_{REF}}$$

   and f_{REF} = reference frequency. (Hz)

   This filter gives an attenuation of 3 times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
   If R1, C2 are fitted then:

   $$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\,\Omega$$

   If R1, C2 are not fitted then:

   $$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\,\Omega$$

   where E_{DC} = 160×10^{-3} for 10 bits resolution
   = 40×10^{-3} for 12 bits
   = 10×10^{-3} for 14 bits
   = 2.5×10^{-3} for 16 bits
   = Scaling at the DC ERROR in volts

3. AC Coupling of Reference Input (R3, C3)
Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

$$R3 = 100k\Omega$$

$$C3 > \frac{1}{10^5 \times f_{REF}}$$

4. Maximum Tracking Rate (R6)
The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate the velocity output will be 8V.

Decide on your required maximum tracking rate, "T," in revolutions per second. Note that "T" must not exceed the specified maximum tracking rate or 1/16 of the reference frequency.

$$R6 = \frac{5.92 \times 10^7}{T \times p}\ k\Omega$$

where p = bit per rev
= 1,024 for 10 bits resolution
= 4,096 for 12 bits
= 16,384 for 14 bits
= 65,536 for 16 bits

5. Closed Loop Bandwidth Selection (C4, C5, R5)
a. Choose the Closed Loop 3dB Bandwidth (f_{BW}) required ensuring that

$$f_{REF} > 2.5 \times f_{BW}$$

Typical values may be 100Hz for 400Hz reference frequency and 500 to 1000Hz for 5kHz reference frequency.

b. Select C4 so that

$$C4 = \frac{20.2 \times 10^{-3}}{R6 \times f_{BW}^2}$$

with R6 in kΩ and f_{BW} in Hz selected above.

c. C5 is given by

$$C5 = 5 \times C4$$

d. R5 is given by

$$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\ \Omega$$

6. VCO Phase Compensation
The following values of C6 and R7 should be fitted.

C6 = 470pF R7 = 68Ω

7. Offset Adjust
Offset and bias current at the integrator input can cause an additional positional offset at the output of the converter of 1 arc min typical, 5.3 arc mins maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.

If fitted, the following values of R8 and R9 should be used: R8 = 4.7MΩ, R9 = 1MΩ potentiometer.

To adjust for zero offset, ensure the resolver is disconnected and all the other external components are fitted. Connect the COS pin to the REFERENCE INPUT and the SIN pin to the SIGNAL GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

The potentiometer may be replaced by select on test resistors if preferred.

PIN FUNCTIONS

REFERENCE I/P	Input pin for the reference signal.
DEMOD I/P	Demodulator input pin.
AC ERROR O/P	Output of ratio multiplier.
COS	Input pin for cosine signal from resolver.
ANALOG GROUND	Power ground.
SIGNAL GROUND	Ground pin for signals from resolver.
SIN	Input pin for sine signal from resolver.
$+V_S$	Main positive power supply.
BIT 1 – BIT 16	Parallel output data bits.
V_L	Logic power supply.
$\overline{\text{ENABLE}}$	Logic "HI" sets the output data bits to a high impedance state, a logic "LO" presents the data in the latches to the output pins.
BYTE SELECT	Selects the data output bits presented on data bits 1 to 8. Logic "HI" will present the 8 most significant bits; a logic "LO" will present the least significant byte.
INHIBIT	Logic "LO" inhibits the data transfer from the counter to the output latches.
DIGITAL GROUND	Ground pin for digital circuitry.
SC1, SC2	Logic inputs used for selecting the resolution of the converter.
DATA LOAD	Logic "LO" allows data to be loaded into the counters.
BUSY	Converter BUSY. A logic "HI" indicates that the output latches are being updated and data should not be transferred.
DIRECTION	Logic output indicating the direction of rotation of the input signals.
RIPPLE CLOCK	A negative going pulse whenever the output of the converter changes from all "1s" top all "0s" or the converse.
$-V_S$	Main negative power supply.
VCO I/P	Input pin to VCO.
INTEGRATOR I/P	Input pin of integrator.
INTEGRATOR O/P	Output pin of integrator.
DEMOD O/P	Output pin of demodulator.
$\overline{\text{COMPLEMENT}}$	Logic "LO" to activate
VCO O/P	Output pin of VCO.

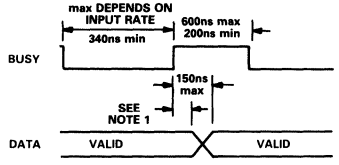
DATA TRANSFER
Data transfer can be accomplished using either the INHIBIT input or the trailing edge of the BUSY pulse output.

INHIBIT Input:
The INHIBIT logic input only inhibits the data transfer from the internal up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the INHIBIT automatically generates a BUSY pulse to refresh the output data.

The output data is valid 350ns after the application of a logic "Lo" to the INHIBIT but the INHIBIT input must remain "Lo" for at least 600ns; otherwise the BUSY pulse generated by the logic "Lo" to "Hi" transition of the INHIBIT input may overlap the BUSY pulse that may have occurred at the time the INHIBIT is applied. The time required to assert the INHIBIT is 100ns.

BUSY Output:
The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL levels. A BUSY pulse is initiated each time the input moves by an analog equivalent of an LSB and the internal counter is incremented or decremented or the INHIBIT input is released.

Typically the width of the BUSY pulse is 350ns during the position data output updates. The trailing edge of the BUSY pulse indicates that the position data output has been updated and is ready for transfer. The maximum load on the BUSY output using the trailing edge of the BUSY pulse is 3 LSTTL loads.



NOTE 1
THE USE OF THE LEADING EDGE OF THE BUSY TO PREDICT DATA UPDATES IS ADVERSELY AFFECTED BY THE CAPACITIVE LOADING ON THE BUSY PULSE. TO ENSURE THAT THE LEADING EDGE OF THE BUSY PULSE OVERLAPS DATA TRANSITIONS, THE MAXIMUM LOAD ON BUSY OUTPUT SHOULD BE 15pF AND IT SHOULD BE PULLED UP TO +5 VOLT SUPPLY VIA A 5kΩ. THIS WILL RESTRICT THE MAXIMUM LOAD ON THE BUSY OUTPUT TO 1 LSTTL LOAD.

Figure 2. Timing Diagram

$\overline{\text{ENABLE}}$ Input:
The ENABLE input determines the state of the output data. A logic "Hi" maintains the output data pins in the high impedance condition, and application of a logic "Lo" presents the data in the latches to the output pins. The operation of the ENABLE has no effect on the conversion process.

BYTE SELECT Input:
The BYTE SELECT input selects the byte of position data to be presented at the data output Bits 1 to 8. The least significant byte will be presented on data output Bits 9 to 16 (with the ENABLE input taken to a logic "Lo") regardless of the state of the BYTE SELECT pin. Note that when the 2S82 is used with a resolution less than 16 bits the unused data lines are pulled to a logic "Lo." A logic "Hi" on the BYTE SELECT input will present the eight most significant data bits on data output Bits 1 and 8. A logic "Lo" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

RIPPLE CLOCK Output:
As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution, or a pitch, of the input has been completed. The pulse has a minimum width of 300ns and is reset by the start of the next data update cycle.

DIRECTION Output:
The DIRECTION (DIR) logic output indicates the direction of the input rotation, and this data is valid in advance of the RIPPLE CLOCK pulse and stays valid until the direction changes. This is the start of the next data update cycle – if the direction of rotation of the inputs has changed – and will be at least 300ns after the rising edge of the RIPPLE clock.

The DIR and RC outputs are unaffected by the state of the INHIBIT input.

$\overline{\text{COMPLEMENT}}$
The $\overline{\text{COMPLEMENT}}$ pin is internally pulled up to +12V in the INACTIVATE STATE. It is pulled down to DIGITAL GROUND (~100μA) to ACTIVATE.

When used in conjunction with the DATA LOAD pin, Strobing Data Load and $\overline{\text{COMPLEMENT}}$ pins "LOW" will set the logic "HIGH" bits of the 2S82 counter to a "LOW" state. Those bits of the applied data which are logic "LOW" will not change the corresponding bits in the 2S82 counter.

For example:

Initial Counter State	– – – 1 0 1 0 1 – – –
Applied Data Word	– – – 1 1 0 0 0 – – –
Counter State after Data Load Only	– – – 1 1 0 0 0 – – –
Initial Counter State	– – – 1 0 1 0 1 – – –
Applied Data Word	– – – 1 1 0 0 0 – – –
Counter State after Data Load and Complement	– – – 0 0 1 0 1 – – –

In order to read the output the following procedure should be followed:
1. Place outputs in high impedance state (ENABLE – "HIGH").
2. Present data to pins.
3. Pull DATA LOAD and COMPLEMENT pins to ground.
4. Wait 100ns.
5. Remove data from pins.
6. Remove outputs from high impedance state (ENABLE – "LOW").
7. Read Outputs.

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE

The 2S82 allows the user great flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the external components shown in Figure 1, and the section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the 2S82 and the variations in the dynamic performance available to the user.

Loop Compensation
The 2S82 (connected as shown in Figure 1) behaves as a type 2 tracking servo loop where the VCO/counter combination and the integrator perform the two integration functions inherent in a type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize any type 2 loop to avoid the loop gain characteristic crossing the 0dB axis with 180° of additional phase lag, as shown in Figure 4. This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

The 2S82 does not have to be connected as tracking converter; parts of the circuit can be used independently. This is particularly true of the ratio multiplier which can be used as a control transformer.

A block diagram of the 2S82 is given in Figure 3.

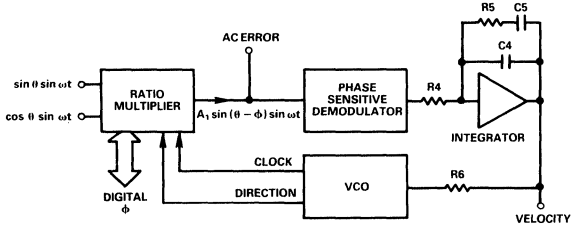


Figure 3. 2S82 Functional Diagram

Ratio Multiplier

The ratio multiplier is the input section of the 2S82 and compares the signal from the resolver inputs, θ, to the digital angle, ϕ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by a mechanical device known by that name.

The AC ERROR signal is given by

$A1 \sin(\theta - \phi) \sin\omega t$.

where $\omega = 2\pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage is 14.5 times.

So for 2V rms inputs signals

AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{p}\right) \times A1$$

where p = bits per rev

= 1,024 for 10 bits resolution

= 4,096 for 12 bits

= 16,384 for 14 bits

= 65,536 for 16 bits

Giving AC ERROR output

= 178mV rms/bit @ 10 bits resolution

= 44.5mV rms/bit @ 12 bits

= 11.125mV rms/bit @ 14 bits

= 2.78mV rms/bit @ 16 bits.

The ratio multiplier will operate in exactly the same way whether the 2S82 is connected as a tracking converter or as a control transformer, where data is preset into the counters using the DATA LOAD pin.

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any dc offset at this point. Note, however, that the PSD of the 2S82 is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noisy environments, and the user is advised to fit a simple HF filter R1, C2 prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator.

Values of the components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The phase sensitive demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times \text{(DEMODULATOR INPUT rms voltage)}$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error Scaling = 160mV/bit (10 bits resolution)

= 40mV/bit (12 bits resolution)

= 10mV/bit (14 bits resolution)

= 2.5mV/bit (16 bits resolution)

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the 2S82 to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from "flickering" (i.e., continually toggling by ±1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ) feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 bit. In order to ensure that this feedback "hysteresis" is set to 1LSB the input current to the integrator must be scaled to be 100nA/bit. So,

$$R4 = \frac{\text{DC Error Scaling (mV/bit)}}{100\ \text{(nA/bit)}}\ \text{MΩ}$$

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB of extra error will be added for each 100nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION."

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocked either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the reset period the input continues to be integrated although the reset period is constant at 400ns.

The VCO rate is fixed for a given input current by the VCO scaling factor,

$= 7.4\text{kHz}/\mu\text{A}$

The tracking rate in rps per μA of VCO input current can be found by dividing the VCO scaling factor by the number of LSB changes per rev (i.e., 4096 for 12-bit resolution).

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT pin and the VCO input current. Thus to achieve a 5V output at 100 rps (6000 rpm) and 12-bit resolution the VCO input current must be:

$(100 \times 4096)/(7400) = 55.3\mu\text{A}$

Thus, R6 would be set to: $5/(55.3 \times 10^{-6}) = 90\text{k}\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

Velocity Offset Voltage = R6 × (VCO bias current)

The temperature coefficient of this offset is given by

Velocity Offset Tempco = R6 × (VCO bias current tempco)

where the VCO bias current tempco is typically −0.55nA/°C.

The maximum recommended rate for the VCO is 1.1MHz which sets the maximum possible tracking rate.

Since the maximum voltage swing available at the integrator output is ±8V, this implies that the minimum value for R6 is 54kΩ. As

$$\text{Max Current} = \frac{1.1 \times 10^6}{7.4 \times 10^3} = 149\mu\text{A}$$

$$\text{Min Value } R_6 = \frac{8}{149 \times 10^{-6}} = 54\text{k}\Omega$$

VCO OUTPUT

VCO OUTPUT: In order to overcome the "free play" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of the digital angle output.

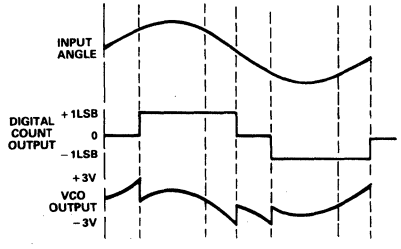


Figure 4.

The converter updates the output if the error is an LSB or greater and the VCO output gives the positional error smaller than 1LSB.

Figure 4 illustrates how the VCO output compensates for the instances where, due to hysteresis, there is no change in the digital count output for 1LSB change in input angle. The sum of the digital count output and VCO output equals the actual input angle.

Transfer Function

By selecting components using the method outlined in the section "Component Selection" the converter will have a critically damped time response and maximum phase margin. The closed-loop transfer function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\,(1 + s_N)}{(s_N + 2.4)\,(s_N^2 + 3.4\,s_N + 5.8)}$$

where, s_N, the normalized frequency variable is

$$s_N = \frac{2}{\pi}\,\frac{s}{f_{BW}}$$

and f_{BW} is the closed-loop 3dB bandwidth (selected by the choice of external components).

The acceleration constant, K_A, is given approximately by

$$K_A = 6 \times (f_{BW})^2 \quad \text{sec}^{-2}$$

The normalized gain and phase diagrams are given in Figures 5 and 6.

The small signal step response is shown in Figure 6. The time from the step to the first peak is t_1, and the t_2 is the time from

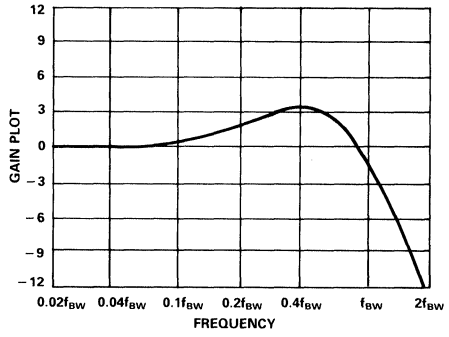


Figure 5. 2S82 Gain Plot

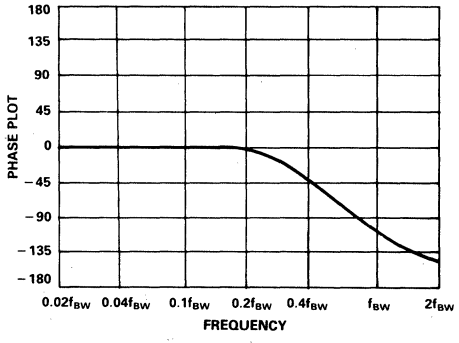


Figure 6. 2S82 Phase Plot

the step until the converter as settled to 1LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}} \times \frac{R}{12}$$

where R = resolution, i.e., 10, 12, 14 or 16.

The large signal step response (for steps greater than 10 degrees) applies when the error voltage will exceed the linear range of the converter. Typically the converter will take 3 times longer to reach the first peak for a 179 degrees step.

The response to a velocity step, the velocity output will exhibit the same time response characteristics as outlined above for the position output.

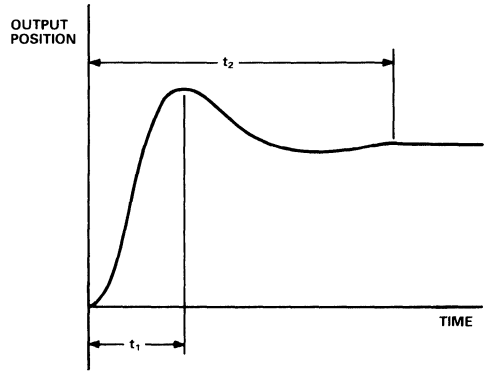


Figure 7. 2S82 Small Step Response

APPLICATIONS

USING THE 2S82 AS A CONTROL TRANSFORMER

The ratio multiplier section of the 2S82 can be used independently to the rest of the converter to perform the function of control transformer. In this mode the signal from the resolver inputs, θ, is compared to a digital angle, ϕ, loaded into the counters. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. To use the device in this way the DATA LOAD pin is used.

Applying a logic "Lo" to the DATA LOAD pin will allow data to be loaded into the counters of the converter from the data lines. It is important that the data lines are placed in the high impedance state before loading data.

To operate the 2S82 as a tracking resolver-to-digital converter the DATA LOAD pin should be left unconnected as it is pulled high internally to +12V.

CAUSES OF ADDITIONAL ERROR

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will be typically 1 arc minute over the operating temperature range.

A description of how to adjust for zero offset is given in the section "COMPONENT SELECTION" and the circuit required is shown in Figure 1.

Differential Phase Shift

Phase shift between the sine and the cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

Error = 0.53 a·b arc minutes

where a = differential phase shift in degrees
and b = signal to reference phase shift in degrees.

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section "CONNECTING THE RESOLVER"). By taking these precautions, the extra error can be made insignificant.

Resolver Phase Shift

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's static accuracy.

However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (rps)} \times \text{Phase Shift (Degs)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20 degrees, a shaft rotation of 22 rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000} = 0.088 \text{ degrees}$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

NOTE: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

USING THE VELOCITY SIGNAL

The signal at the INTEGRATOR OUTPUT pin relative to the ANALOG GROUND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in place of a velocity transducer. Although the conversion loop of the 2S82 includes a digital section there is an additional totally analog feedback loop around the velocity signal. This ensures that there is no digital effects on the output signal and that the loop is closed even when the input signals are such that the digital output does not change.

A better quality velocity signal will be achieved if the following points are considered.

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion Error.
   If necessary, the reversion error can be reduced by a simple trimming circuit. Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO. The reversion error can be nulled by varying one supply rail relative to the other.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using separate screened twisted pair cable for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fitted before the Phase Sensitive Demodulator (as described in the section HF FILTER).

   A resolver is chosen that has a low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the 2S82 with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   The signal voltages are 2V rms to prevent a ripple at the LSB switching rate. This is because the 1LSB of analog feedback that prevents the output from flickering will be incorrectly scaled (see section "INTEGRATOR").

If the above precautions are taken, a very good noise and ripple performance is obtainable making the 2S82 velocity signal usable in very noisy environments, for instance in motor drive applications with PWM switching noise.

The positional error curve of the converter and the resolver will result in an apparent acceleration when the resolver is rotating at a constant velocity. The main result of this will be a ripple on the velocity signal twice per revolution.

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 8.

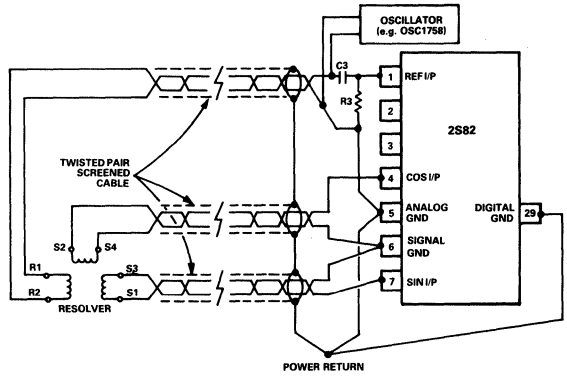


Figure 8. Connecting the 2S82 to a Resolver

In cases where the reference phase relative to the input signals from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency $= \frac{1}{2\pi R C}$

By altering the value of R2 the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

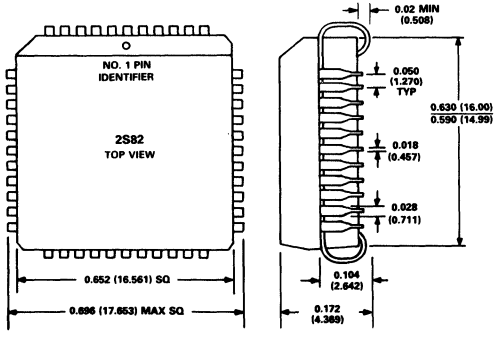
Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.

For signal and reference voltages greater than 2V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic Leaded Chip Carrier



ANALOG DEVICES

Synchro and Resolver Isolation Transformers

5S70/5S72

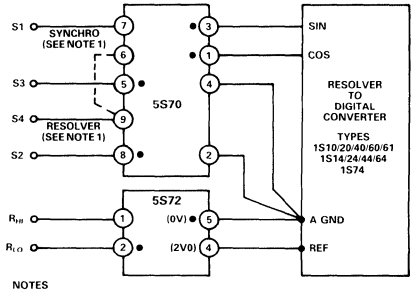
FEATURES

Ultralow Profile – 0.4" (10mm)
1kV Isolation Primary to Secondary
High Accuracy (±1.5 Arc Min Max)

APPLICATIONS

Provides Signal and Reference Isolation for 1S Series Resolver-to-Digital Converters (e.g., 1S10/20/40/60/61, 1S14/24/44/64 and 1S74)
Enables 1S Series Converters to be Used with Synchro Inputs
Allows 1S Series Converters to be Used with Higher Signal and Reference Voltages
External Mounting of the Transformer Eliminates High Voltages from Printed Circuit Boards

5S70/5S72 CONNECTION DIAGRAM



NOTES
FOR SYNCHRO OPTIONS, CONNECT PIN 9 TO PIN 6.
FOR RESOLVER OPTIONS, CONNECT PIN 9 TO S4 TERMINAL OF RESOLVER.
• DENOTES START OF WINDING

5

GENERAL DESCRIPTION

The 5S70 series of miniature transformers provide Resolver-to-Resolver and/or Synchro-to-Resolver format transformations and input isolation for the 1S series of Resolver-to-Digital converters (e.g., 1S10/20/40/60/61, 1S14/24/44/64 and 1S74).

The 5S70 series accept all the standard synchro and resolver signal voltages and give the 2V rms required by the 1S series of converters.

The additional error introduced by the 5S70 is ±1.5 Arc Minute maximum.

The 5S72 transformers enable the reference input of the 1S series converters to be isolated and to accept voltages higher than the standard 2V rms.

All transformers operate over the 360Hz to 3kHz frequency range and have an operating temperature range of −55°C to +125°C.

The units are fitted with ruggedly secured threaded inserts to assist with PCB mounting.

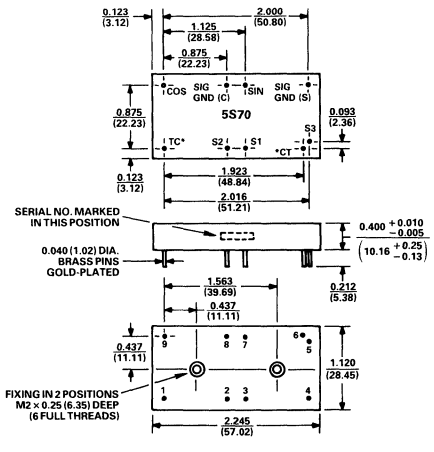
The dc isolation is 1kV from primary to secondary and 5kV between any winding and the threaded insert.

The 5S70 transformers measure only 2.25" × 1.12" × 0.4" (57.0 × 28.5 × 10.2) and the 5S72 transformers 1.12" × 1.12" × 0.4" (28.5 × 28.5 × 10.2).

OUTLINE DIMENSIONS

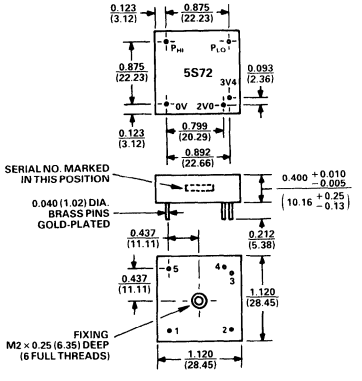
Dimensions shown in inches and (mm).

5S70 Transformers



*'TC' READS 'S4' AND 'CT' READS 'NC' ON 414, 418 OPTIONS.

5S72 Transformers



SPECIFICATIONS (typical @ +25°C, unless otherwise specified)

Model Parameters	5S70 /411	5S70 /412	5S70 /414	5S70 /418	5S72 /11V8	5S72 /26V	5S72 /115V	Units
INPUTS								
Transformation Format[1]	S to R	S to R	R to R	R to R	Ref.	Ref.	Ref.	
Transformation Ratio	0.169	0.022	0.077	1.000	0.169 0.288	0.077 0.131	0.017 0.030	
Input Voltage[2]	11.8	90	26	11.8	11.8	26	115	V rms
Magnetization Energy @ 400Hz	3.0	17.0	17.0	3.0	3.0	3.0	17.0	mW
OUTPUTS								
Output Voltage	2.0	*	*	*	2.0 3.4	**	**	V rms V rms
Output Phase Shift	0.1	*	*	*	*	*	*	Degrees
Output Resistance	7.4	8.6	2.2	5.9	5.1[3] 9.4[4]	6.4[3] 11.3[4]	5.5[3] 9.5[4]	Ω Ω
REFERENCE FREQUENCY	360 to 3,000	*	*	*	*	*	*	Hz
ANGULAR ACCURACY (With 1S Converters as Load)								
Typical	±0.33	*	*	*	N/A	N/A	N/A	arc-mins
Max[5]	±1.5	*	*	*	N/A	N/A	N/A	arc-mins
DC ISOLATION								
Input to Output	1	*	*	*	*	*	*	kV
Primary or Secondary to Threaded Insert	5	*	*	*	*	*	*	kV
TEMPERATURE RANGE								
Operating	−55 to +125	*	*	*	*	*	*	°C
Storage	−60 to +150	*	*	*	*	*	*	°C
DIMENSIONS	2.25 × 1.12 × 0.4 57.0 × 28.5 × 10.2	* *	* *	* *	1.12 × 1.12 × 0.4 28.5 × 28.5 × 10.2	** **	** **	inches mm
WEIGHT	1.8 50	* *	* *	* *	0.9 25	** **	** **	oz g

NOTES
[1]S indicates Synchro.
R indicates Resolver.
N/A indicates Not Applicable.
[2] + 10% voltage overdrive allowed.
[3]2V0 output.
[4]3V4 output.
[5]Over the operating temperature range.
*Specification same as 5S70/411.
**Specification same as 5S72/11V8.
Specifications subject to change without notice.

APPLICATIONS/USER BENEFITS

Apart from providing signal and reference isolation and allowing synchro inputs to be used with the 1S series of converters, high voltages can also be eliminated from the PCB by mounting the transformers externally.

In addition, by using a number of transformers on a PCB with a single converter, it is possible to cater for a number of different synchro and resolver configurations.

MODELS AVAILABLE

The 5S70 and 5S72 transformers are available with a variety of input voltage and format configurations. The transformers operate over the −55°C to +125°C temperature range and accept reference frequencies in the range 360Hz to 3kHz.

ORDERING INFORMATION

The transformers should be ordered by reference to the part numbers shown in the Specifications above.

ANALOG DEVICES

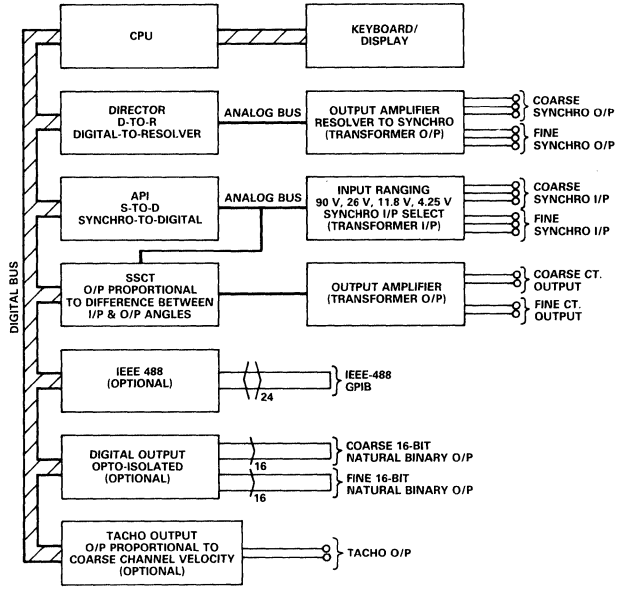
Digital Director

6S04

FEATURES
15 VA Output Drive Capability at 400 Hz
±0.15° Accuracy
Measurement of External Synchro Inputs
Angle Position Indicator
Control Transformer Function
Coarse–Fine Synchro Transmission
User Selectable Output Functions (Motion Patterns)
Internal Isolating Transformers
IEEE (GPIB 488) Interface (Optional)
Isolated 16-Bit Natural Binary Outputs (Optional)
Tachogenerator Output (Optional)

APPLICATIONS
Simulation and Test of:
- **Synchro Transmitters**
- **Synchro Receivers**
- **Gun Mounting Servo Systems**
- **Radar Processing Equipment**
- **Naval Retransmission Systems**
- **Measurement of Backlash in Servo System Gear Boxes**
- **Test of Digitally Controlled Machines**
- **ATE Systems**

6S04 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The 6S04 Digital Director is a microprocessor based **Universal Synchro Simulator and Test Instrument**.

It is designed as a portable Test Instrument and Synchro Simulator (Dummy Director) and its uses are the synchro transmitter electrical output simulation and testing of equipment with synchro inputs such as gun mounting sensors, radar processing and equipment and naval retransmission systems.

The 6S04 can be considered as three autonomous units.

The Director simulates the electrical outputs of a synchro coarse/fine transmitter. An operator can set the output of the director at any fixed angle and also select from a suite of predefined patterns of motion, referred to as "output functions."

The Angle Position Indicator measures and displays synchro format signals from either the director or an external synchro transmitter. The angular position of the selected source is displayed on the front panel of the instrument.

The Solid State Control Transformer simulates the action of a conventional control transformer by generating an analog signal proportional to the angular difference between the director output and the input from an external synchro transmitter.

SPECIFICATIONS (typical at +25°C unless otherwise specified)

Electrical Specification

MAINS POWER SUPPLY (Single Phase)

Voltage Range	115 V ac (90 V ac–132 V ac)
	220 V ac/240 V ac (180 V ac–265 V ac)
Supply Current	
1.4 A (typ)	2 A (max) (115 V ac)
0.7 A (typ)	1 A (max) (230 V ac)
Dissipation 160W (typ)	200 Watts (max)
Supply Frequency	47 Hz to 63 Hz
Fuse	2.5 A Anti-Surge (115 V ac)
	1.25 A Anti-Surge (230 V ac)
	Both 5 mm × 20 mm
Isolation	1000 V dc Input to Output
	1000 V dc Input to Case

DUMMY DIRECTOR

COARSE AND FINE REFERENCE INPUT (User Provided)

Voltage	115 V rms ±10% for Rated O/P
	3 V to 120 V rms for API Function
Frequency	60 Hz ±10% or 400 Hz ±10%
Input Impedance	220 kΩ (Nominal)
Isolation	500 V dc Galvanic Isolation

INTERNAL COARSE OUTPUT

Voltage	(Synchro) 90 V ±2% Line-to-Line at Nominal Reference and 100% Output Level
	(SLAB) 4.25 V ±2% Line-to-Line at Nominal Reference and 100% Output Level
Transformation Ratio	0.782 ±2% (Synchro)
	0.037 ±2% (SLAB)
Voltage Range	50% to 110% of Nominal,
	Resolution 1%, Accuracy ±0.5%
Resolution	0.01% of Output
Angular Accuracy	±0.1° @ 5 VA
	±0.15° @ 15 VA
Radius Vector Error	±0.1%
Energizing Power	15 VA @ 400 Hz Reference
	5 VA @ 60 Hz Reference
Energizing Current	200 mA (max)
Regulation	Better than 5% at 5 VA
	Better than 10% at 15 VA
Protection	Protected Against Open and Short Circuits, and Thermal Overload with Automatic Reset
Isolation	500 V dc Galvanic Isolation
Update Interval	0.977 ms
Effective Stator dc Resistance	20 Ω for 90 V Synchro Output
	1 Ω for SLAB Output

INTERNAL FINE OUTPUT

As Above Except:	
Voltage	(Synchro) 90 V ±2% Line-to-Line at Nominal Reference and 100% Ouput Level
	(SLAB) 11.8 V ±2% Line-to-Line at Nominal Reference and 100% Output Level
Transformation Ratio	0.782 ±2% (Synchro)
	0.037 ±2% (SLAB)
Effective Stator dc Resistance	20 Ω for 90 V Synchro Output
	2.4 Ω for SLAB Output

EXTERNAL COARSE AND FINE INPUT (for API)

Voltage	(a) 90 V ±20%
	(b) 26 V ±20%
	(c) 11.8 V ±20%
	(d) 4.25 V ±20%
Frequency	Same as Reference
Allowable Phase Shift	±30° Under Static Conditions (Signal to Reference)
Input Impedance	(a) 200 kΩ (Nominal)
	(b) 58 kΩ (Nominal)
	(c) 26 kΩ (Nominal)
	(d) 9.5 kΩ (Nominal)
Isolation	500 V dc Galvanic Isolation
Accuracy	±0.1°
Resolution	0.01°

CONTROL TRANSFORMER OUTPUT

Voltage	57.5 V ±5% at Nominal External Synchro Input Level, No Load 90° Angular Difference
Transformation Ratio Tolerance ±5%	(a) 0.638 for 90 V Range Selected
	(b) 2.212 for 26 V Range Selected
	(c) 4.873 for 11.8 V Range Selected
	(d) 13.53 for 4.25 V Range Selected
Load Impedance	∞ to 10 kΩ
Regulation	10%
Angular Accuracy	±9 arc mins @ 0° Difference
Null Voltage	150 mV (max)
Protection	Protected Against Open and Short Circuits
Isolation	500 V dc Galvanic Isolation
Update Interval	0.977 ms
Voltage Gradient	1V Per Degree at Angles <5°
Effective Rotor dc Resistance	330 Ω

DIGITAL OUTPUT (Option 090)

Collector Voltage	30 V dc max
Collector Current (On)	1.6 mA min
Collector Current (Off)	500 nA max
Isolation	500 V dc
Data Strobe Low Duration	20 µs min
Update Interval	0.977 ms

TACHO OUTPUT (Option 900)

Resolution	0.1 deg/sec
Accuracy	±1% of Output
Update Interval	0.977 ms
Voltage	10 V ±1% at Velocity of 90 deg/sec Relative to the Coarse Channel
Scaling Factor	111 mV/deg/sec
Load Impedance	∞ to 10 kΩ
Protection	Protected Against Short Circuits

Specifications subject to change without notice.

DIRECTOR FUNCTIONAL DESCRIPTION

The director consists of two electronically geared transmitters, each capable of providing a synchro transmitter output to an accuracy of ±0.1° under full load conditions. The combined accuracy of the two signals is determined by the gearing employed.

The signals may be selected to be either Synchro 90 V rms on both coarse and fine, or SLAB format, 4.25 V rms on coarse and 11.8V rms on fine.

OUTPUT FUNCTIONS

The user may select from the output functions below.

1. Datum Angle
   The combined coarse/fine output angle may be set at any angle between 0.00° to 359.99° to accuracy of ±0.1° and resolution of 0.01°.
2. Constant Velocity
   The synchro output can be made to rotate at constant rates in either direction at velocities from ±0.01° per second to ±359.99° per second.
3. Square Wave
   The output can be made to oscillate with a square waveform with a period selectable to any integer between 1 and 100 second and a peak-to-peak amplitude of between 0.00° and ±179.99°. The starting datum angle may be set at any angle in the range 0.00° to ±359.99°.
4. Sine Wave
   The output can be made to oscillate sinusoidally with a period selectable to any integer between 1 and 100 second and a peak amplitude of between 0.00° to ±179.99°. The center of oscillation may be set to any angle within the range 0.00° to ±359.99°.
5. Velocity + Square Wave
   This function superimposes the velocity and square wave functions as described above.
6. Manual Control
   Using the control knob, the velocity of the output angle can be varied mannually between 0° and ±90° per second on a logarithimic scale. In this mode, two push buttons are also enabled which allow the output angle to be stepped, either forwards or backwards by a fixed preselected amount between 0.00° to ±179.99°. These "INCH" keys are also enabled with the velocity function thus allowing manual steps to be superimposed on constant velocity.

ANGLE POSITION INDICATOR (API)

The API may be set to measure either the angle output from the Director or the angle input to the to the instrument from an external synchro transmitter. Either the coarse, the fine or the combined coarse and fine angle may be displayed. The display will normally be updated at a rate of approximately three times a second.

SOLID STATE CONTROL TRANSFORMER (SSCT)

The Solid State Control Transformer provides signals from both the coarse and fine channels, which are an indication of the angular difference between the director output, and the input from an external synchro transmitter. When used with 90 V, 26 V, 11.8 V and 4.25 V an error signal is produced which is scaled to give a 1 volt per degree of error. The null voltage is 150 mV maximum, which corresponds to an angular accuracy of 0.15°.

IEEE INTERFACE (Option 009)

The instrument can be provided with an IEEE 488 standard 24 wire General Purpose Interface Bus, which allows any standard IEEE controller to remotely operate the unit.

The IEEE standard 488 is a byte serial bit parallel interface system structured with 16 transmission lines of which 8 are data bus lines, 3 are data byte transfer control lines (handshake) and the remaining 5 are interface management lines.

The controller can set the unit to either Talk or Listen mode. In the Listen mode the controller can operate the various key functions, and in the Talk mode it can read the instruments API display. Please refer to operating manual for operator setup procedure for the IEEE Bus.

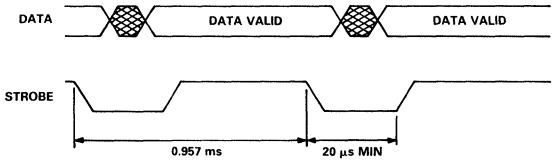
Interconnections

Refer to an IEEE handbook for detailed information and specifications.

DIGITAL OUTPUT (Option 090)

The digital output consists of two 16-bit parallel data channels carrying digital representations of the coarse and fine output angles. These are automatically updated with the coarse and fine output angles. Data is in the form of an unsigned 16-bit binary integer with the most significant bit representing 180 degrees.

BIT NO.	BIT WEIGHT (°)
1 (MSB)	180
2	90
3	45
4	22.5
5	11.25
6	5.625
7	2.812
8	1.406
9	0.703
10	0.352
11	0.176
12	0.088
13	0.044
14	0.022
15	0.011
16 (LSB)	0.005

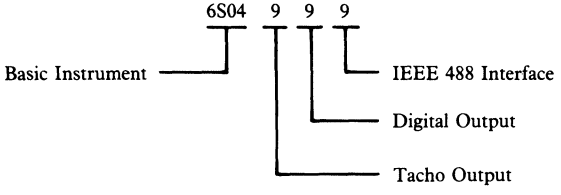


Digital Output Timing

TACHO OUTPUT (Option 900)

The tacho output provides an analogue voltage signal via a BNC output socket which is proportional to the angular velocity of the coarse channel outputs.

ORDERING INFORMATION



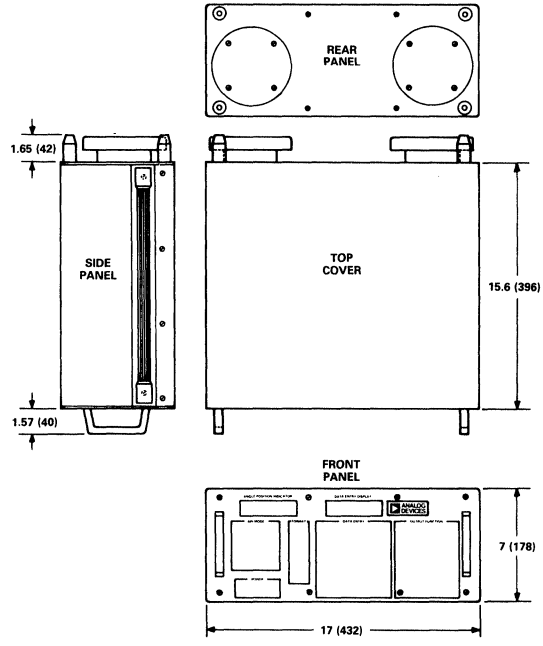
NOTES
Insert 0 in place of 9 if option is not required.
Options are factory fitted only.
An operating manual is available upon request.

PHYSICAL SPECIFICATIONS

Dimensions	Depth = 478 mm (18.8″) Width = 432 mm (17″) Height = 178 mm (7″)
Weight	18.5 kg (40.78 lbs)
Low Temperature	Storage −25°C; Operating 0°C per MIL-STD-810D, Method 502.2, Procedure II
High Temperature	Storage +70°C; Operating +45°C per MIL-STD-810D, Medthod 501.2, Procedure II
Humidity	90% RH at 30°C per MIL-STD-810D, Method 507.2, Procedure III
Moisture Ingress	MIL-STD-810D, Method 507.2 Procedure II
Vibration	DEF STAN 66-31 CAT II
Fusing	1.25 A, 2.5 A Anti-Surge (5 mm × 20 mm)
Dissipation	200 Watts max
Safety	Designed to Comply with BS4743 Class I
Finish	Anodized per BS1615 Painted per BS3900 Part A8 Light Grey

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).
Tolerances ±1 mm unless otherwise stated.



Sample/Track-Hold Amplifiers
Contents

Selection Guide
Sample/Track and Hold Amplifiers

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate µV/µs max	Package Options[1]	Temp Range[2]	Page	Comments
***AD1154**	**0.00076**	**3.5**	**80**	**0.15**	**0.1**	**D**	**C, I**	**6–51**	**16-Bit Accurate Sample-and-Hold Amplifier**
***AD386**	**0.00076**	**4.5**	**12**	**0.040**	**0.1**	**D**	**I, M**	**6–11**	**16-Bit Accurate Sample-and-Hold Amplifier**
AD389	**0.003**	**2.5**	**30**	**0.4**	**0.1**	**D**	**C, I**	**6–25**	**High Resolution Track-and-Hold Amplifier**
HTC-0300A	**0.01**	**0.1**	**6**	**0.05**	**0.5**	**D**	**I, M**	**6–57**	**Ultrahigh Speed Track-and-Hold Amplifier**
***AD684**	**0.01**	**1.0**	**25**	**0.2**	**0.001**	**P, Q**	**C, I, M**	**6–43**	**Quad, Monolithic 1µs SHA**
AD346	0.01	2.0	60	0.4	0.5	D	C, M	6–5	High Speed Sample-and-Hold
AD585	**0.01**	**3.0**	**35**	**0.5**	**1**	**E, P, Q**	**C, I, M**	**6–37**	**High Speed, Precision. On-Board Hold Cap**
AD583	0.01	5.0	50	5		D	C	6–35	5µs SHA
HTS-0010	**0.01**	**0.014**	**2**	**0.005**		**D**	**C, I**	**6–61**	**Ultrahigh Speed Track-and-Hold Amplifier**
HTS-0025	**0.01**	**0.025**	**5**	**0.02**		**D**	**C, I**	**6–67**	**Ultrahigh Speed Track-and-Hold Amplifier**
AD582	0.1	6.0	200	15		D, H	C, M	6–31	Low Cost, 15µs

[1] Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip.
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

Orientation
Sample/Track-Hold Amplifiers

The technical data in this volume embrace high-performance (high-resolution and high-speed) sample/track-holds in the form of monolithic and hybrid ICs. Besides the products in this section (stand-alone devices for performing the sample/track-hold function) similar functions can be found integrated into a variety of component and subsystem products. Component examples: a number of video A/D converters have on-board track-holds (MOD-1205); the monolithic AD7579/7580 A/D converters have integral sample-hold functions; and high-resolution D/A converters have deglitcher options (Deglitcher IV for the DAC1138). Besides these, sample-hold functions are inherent in data-acquisition subsystems and microcomputer analog I/O boards.

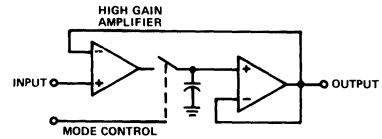
The principal application for sample/track-hold amplifiers is to maintain an analog-to-digital converter's input constant during conversion at a value representing the analog input as of a certain precisely known time. The characteristics of the SHA are crucial to system accuracy and the reliability of the digital data, especially in ≥12-bit and/or high-throughput-rate applications.

A sample/track-hold amplifier (s/h or SHA), as its name indicates, has two modes of operation, programmed by a digital control input. In the *track* or *sample* mode, the output follows the input, usually with a gain of +1. When the mode input switches to *hold*, the output of the SHA ideally retains the last value it had when the command to hold was given, and it retains that value until the logic input dictates *track (sample)*, at which time the output ideally jumps to the input value and follows the input until the next *hold* command is given.

Analog Devices' *track-holds* and *sample-holds* are functionally identical; they are designed to acquire input signals for either immediate hold or for a possibly extended period of tracking. They should not be confused with ac devices termed "sample-hold" that can *only* obtain quick samples and cannot track the input continuously.

SHA CIRCUITRY AND HARDWARE

A sample-hold amplifier usually consists of a storage capacitor, input- and output-buffer amplifiers and a switch and its drive circuitry. During *sample*, the circuit is connected to promote rapid charging of the capacitor. During *hold*, the capacitor is disconnected from its charging source and ideally retains its charge. The following figure shows a typical feedback configuration: the input buffer is a high-gain differential amplifier with a current output that charges the capacitor through the logic-controlled switch. The capacitor is unloaded by a unity-gain buffer-follower. The output is fed back to the negative input (as in an op amp follower configuration), and thus, in *sample* the charge on the capacitor is compelled to follow the input. In *hold*, the input amplifier no longer drives the capacitor; it retains its charge, unloaded by the output follower. In another popular configuration, the capacitor is used as the feedback element of an inside-the-loop integrator (AD346). The highest-speed devices usually run open-loop.

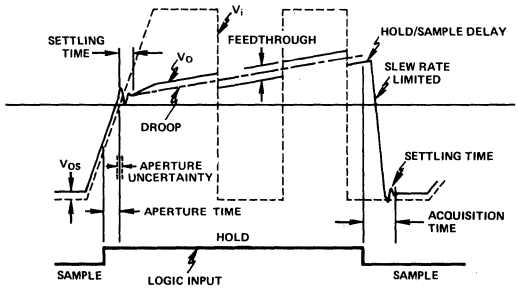


Since drive current is finite and leakage current in *hold* is not zero, the capacitance, if large, limits the slewing rate in *sample* and, if small, converts leakage current to "droop" in *hold*. In s/h *modules*, the capacitance is usually fixed, and the properties of the complete device are optimized for one condition, and so specified. In s/h *monolithic ICs*, the capacitor may be omitted and furnished by the user (both for flexibility and because good capacitors for this purpose are hard to integrate); the AD346 and AD585 have internal hold capacitors. The optimum capacitance can be selected for the specific application.

PERFORMANCE

In the *sample* mode, it is useful to consider that a SHA's performance can be characterized by specifications similar to those of a closed-loop operational amplifier (offset, drift, nonlinearity, gain error, bias current, etc.), but with somewhat slower response (gain-bandwidth, slewing rate, settling time) because of the need to charge the storage capacitor.

However, during the *sample-to-hold*, *hold* and *hold-to-sample* states, the dynamic nature of the mode-switching introduces a number of specifications that are peculiar to SHAs. The most important of these are defined below and illustrated in the adjoining figure. They include the *aperture time* and its *uncertainty*, the *sample-to-hold step*, *feedthrough* and *droop* (in hold) and *acquisition time*.



DEFINITIONS

Acquisition Time is the time required by the output of the device to reach its final value, within a specified error band, after the *sample* command has been given. Included are switch-delay time, the slewing interval and settling time for a specified output-voltage change.

Aperture (Delay) Time is the time required after the *hold* command for the switch to open fully. The sample is, in effect, delayed by this interval, and the *hold* command would have to be advanced by this amount for precise timing.

Aperture Uncertainty – or Aperture (Delay) Jitter – is the range of variation in the *aperture time*. If the *aperture time* is "tuned out" by advancing the *hold* command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution. For example, the HTC-0300A specs are 8ns aperture time and 100ps aperture jitter.

Charge Transfer (or *offset step*), the principal component of *sample-to-hold* offset (or *pedestal*), is the charge transferred to the storage capacitor via stray capacitance when switching to the *hold* mode. It can sometimes be reduced by lightly coupling an appropriate polarity version of the *hold* signal to the capacitor for cancellation. The associated voltage error (ΔQ/C) can be reduced by using greater capacitance for storage, but this increases response time.

Droop is the change of the output voltage during *hold* as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current within a given device. In ICs, it is specified as a (*droop* or *drift*) current, in modules, a dV/dt. [Note: I = C(dV/dt).]

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in *hold*. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Sample-to-Hold Offset, a shift in level between the last value in *sample* and the value settled-to in *hold*, is the residual step error after the *charge transfer* is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as *offset nonlinearity*.

ANALOG DEVICES

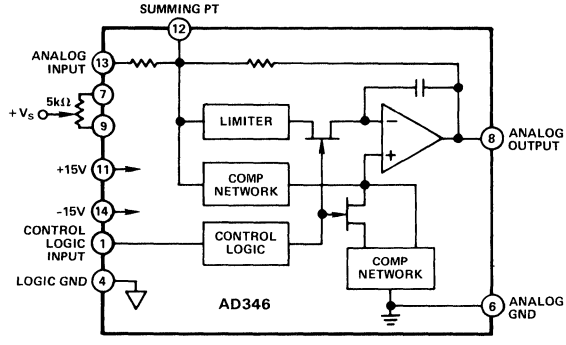
High Speed Sample-and-Hold Amplifier

AD346

FEATURES

Fast 2.0μs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset
Low Glitch: <40mV
Aperture Jitter: 400ps
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor
MIL-STD-883B Processing Available

AD346 FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD346 is a high speed (2μs to 0.01%), adjustment free sample-and-hold amplifier designed for high throughput rate data acquisition applications. The fast acquisition time (2μs to 0.01%) and low aperture jitter (400ps) make it suitable for use with fast A/D converters to digitize signals up to 97kHz.

The AD346 is complete with an internal hold capacitor and it incorporates a compensation network which minimizes the sample to hold charge offset. The AD346 is also laser trimmed to eliminate the need for external trimming potentiometers.

Typical applications for the AD346 include sampled data systems, D/A deglitchers, peak hold functions, strobed measurement systems and simultaneous sampling converter systems.

The device is available in two versions: the "J" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the extended temperature range, −55°C to +125°C.

ORDERING GUIDE

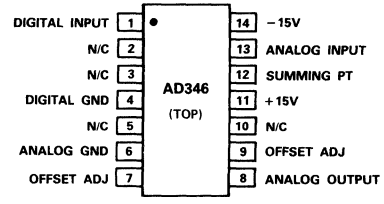
Model	Temperature Range	Package Option*
AD346JD	0 to +70°C	DH-14A
AD346SD	−55°C to +125°C	DH-14A
AD346SD/883B	−55°C to +125°C	DH-14A

*See Section 14 for package outline information.

PRODUCT HIGHLIGHTS

1. The AD346 is an improved second source for other sample and holds of the same pin configuration.
2. The AD346 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
3. The droop rate is only 0.5mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
4. The fast acquisition time and low aperture make it suitable for very high speed data acquisition systems.

PIN CONFIGURATION



SPECIFICATIONS (typical @ +25°C, V_S = ±15V unless otherwise noted)

Model	AD346JD	AD346SD	Units
ANALOG INPUT			
Voltage Range	±10.0	*	Volts
Input Impedance	3.0	*	kΩ
DIGITAL INPUT			
"0" Input Threshold Voltage (Hold)	+0.8 max	*	Volts
"1" Input Threshold Voltage (Sample)	2.0 min	*	Volts
"0" Input Current	−360μA (max)	*	μA
"1" Input Current	20μA (max)	*	μA
TRANSFER CHARACTERISTICS			
Gain	−1.0	*	V/V
Gain Error	±0.02 max (±0.01 typ)	*	% FSR
Gain Error, $T_{min}-T_{max}$	±0.05 max (±0.03 typ)	*	% FSR
Offset Voltage	±3 max (±1 typ)	*	mV
Offset Voltage, $T_{min}-T_{max}$	±20 max (±6 typ)	*	mV
Pedestal	±4 max (±2 typ)	*	mV
Pedestal, $T_{min}-T_{max}$	±20 max (±8 typ)	±20 max (±10 typ)	mV
Droop Rate	0.5 max (0.1 typ)	*	mV/ms
Droop Rate, $T_{min}-T_{max}$	60 max (20 typ)	700 max (200 typ)	mV/ms
DYNAMIC CHARACTERISTICS			
Full Power Bandwidth			
V_{OUT} = +10V, −3dB	1.4	*	MHz
Output Slew Rate	50	*	V/μs
Acquisition Time			
To ±0.01% 10V Step	2.0 max (1.0 typ)	*	μs
To ±0.01% 20V Step	2.5 max (1.6 typ)	*	μs
Aperture Delay	60 max (30 typ)	*	ns
Aperture Jitter	0.4	*	ns
Settling Time			
Sample Mode (10V Step)	2.0 max (1.0 typ)	*	μs
Sample to Hold	500	*	ns
Feedthrough (Hold Mode)			
at 1kHz	0.02 max (0.005 typ)	*	% FSR
Transient Peak Amplitude			
Sample/Hold/Sample	40	*	mV
ANALOG OUTPUT			
Output Voltage Swing[1]	±10.0 min	*	Volts
Output Current	3.0	*	mA
POWER REQUIREMENTS			
Operating Voltage Range	±12 to ±18	*	Volts
Supply Current			
+V	18 max (9 typ)	*	mA
−V	−10 max (−3 typ)	*	mA
Power Supply Rejection Ratio	100	*	μV/V
Power Consumption	500 max (200 typ)	*	mW

NOTES

[1]Maximum output swing is 4V less than $+V_S$.

*Specifications same as AD346JD.

Specifications subject to change without notice.

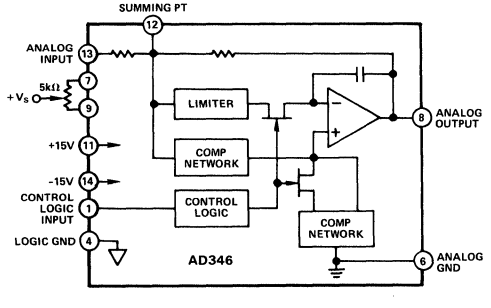


Figure 1. Functional Block Diagram

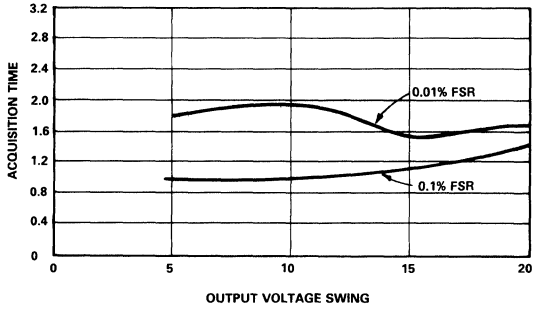


Figure 2. Acquisition Time vs. Output Voltage

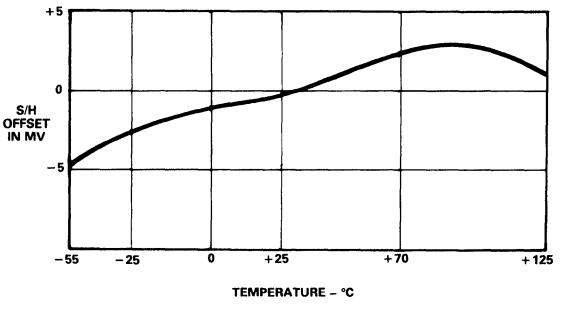


Figure 4. S/H Offset Drift (Typical)

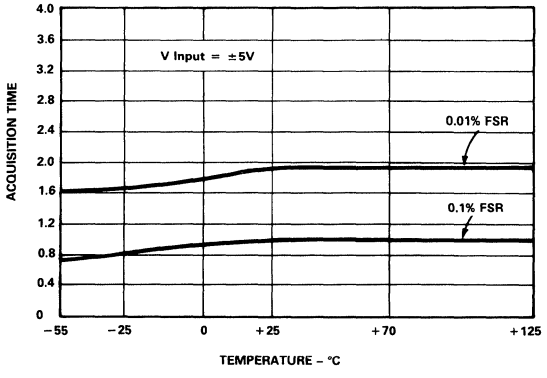


Figure 3. Acquisition Time vs. Temperature

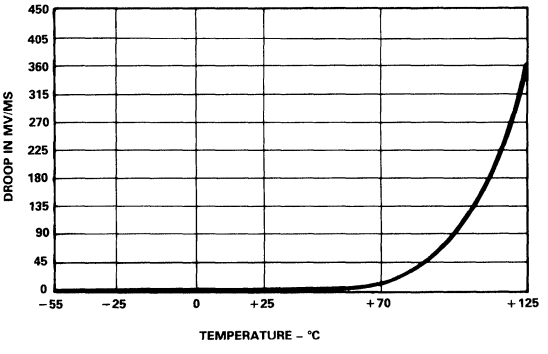


Figure 5. Droop vs. Temperature (±5 Volts)

6

TERMINOLOGY

Aperture Time is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sampling timing.

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the sample-to-hold command with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency.

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage.

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Pedestal during hold is a sample-to-hold offset. This is an offset that occurs from such phenomena as charge dumps when switches are opened, coupling of the logic signal transients.

Transients are the spikes or glitches that occur on the output at the start and end of hold time.

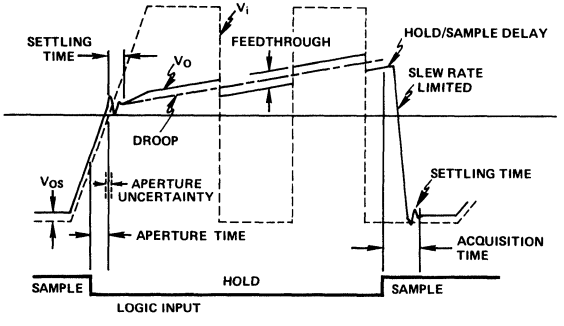


Figure 6. Pictorial Showing Various S/H Characteristics

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pins of the AD346. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

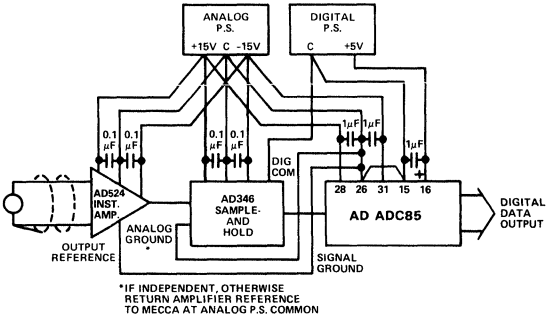


Figure 7. Basic Grounding Practice

SAMPLED DATA SYSTEMS

The fast acquisition time of the AD346 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acqusition systems. The AD346 can be used with a number of different A/D converters to achieve high throughput rates. Figures 8, 9 and 10 show the use of an AD346 with the AD578, AD5240 and AD ADC85.

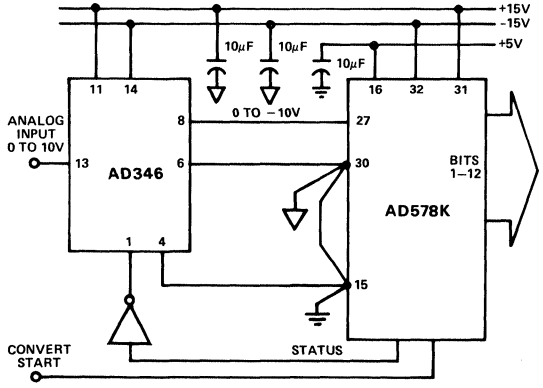


Figure 8. 153kHz–12-Bit, A/D Conversion System

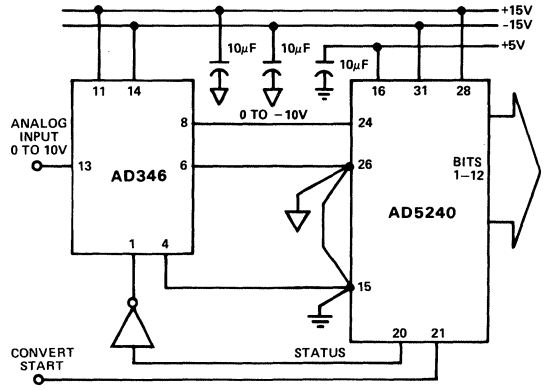


Figure 9. 142.8kHz–12-Bit, A/D Conversion System

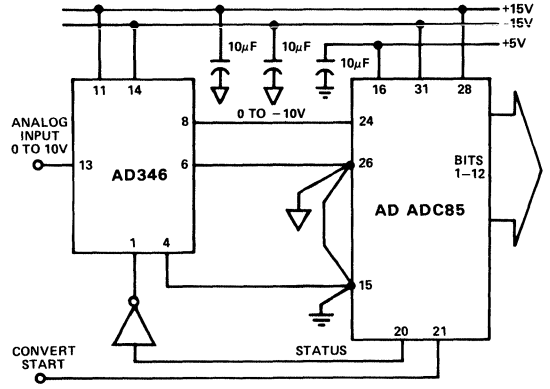


Figure 10. 83.3kHz–12-Bit, A/D Conversion System

In sampled data systems there are two limiting factors in digitizing high frequency signals. The first limitation is the bandwidth and aperture uncertainty of the sample-and-hold amplifier. The second limitation is the maximum update rate for the SHA and A/D converter combination. For high throughput rate data acquisition systems all factors must be understood.

The aperture time is the time required for the sample and hold amplifier to switch from sample to hold. Since this is a constant it can be tuned out by advancing the sample-to-hold command by 60ns with respect to the input signal and, therefore, can be eliminated as an error source. Once the aperture time has been eliminated the aperture jitter which is the variation aperture time from sample-to-sample, remains. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the A/D converter.

$$F_{max} = \frac{(\text{Full Scale Voltage})\ (2^{-N})}{(2)\ (\text{Full Scale Voltage})\ \pi\ (\text{Aperture Jitter})}$$

For an application with a 10-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-10}}{(2)\ (10)\ \pi\ (4 \times 10^{-10}\ \text{sec})}$$

F_{max} = 388.6kHz.

For an application with a 12-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-12}}{2\ (10)\ \pi\ (4 \times 10^{-10}\ \text{sec})}$$

F_{max} = 97.1kHz.

The maximum throughput rate is the sum of the sample-and-hold acquisition time, settling time and the A/D conversion time as shown in Figure 11.

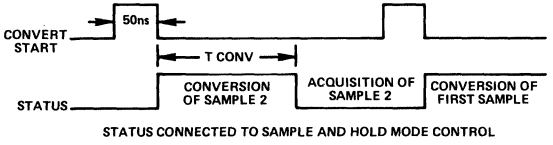


Figure 11. Start/Status Timing for Sampled Data System

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, what has been assumed is that an ideal brickwall filter has been placed in the signal path prior to the AD346 and A/D converter.

AD346 in Combination With an	Throughput Rate	Input Frequency Range
AD578K	153kHz	dc to 76.5kHz
AD5240	143kHz	dc to 71.5kHz
AD ADC85	83.3kHz	dc to 41.6kHz
AD579	263kHz	dc to 131kHz
HAS1202	250kHz	dc to 125kHz

Table I. SHA & ADC Combinations and Maximum Throughput Rate

6

MULTICHANNEL CONVERSION

In multichannel conversion systems, elements of the acquisition chain may be shared by two or more input sources. This sharing may occur in a number of ways, depending on the desired properties of the multiplexed system.

The data acquisition system shown in Figure 12 is one solution to digitizing data from many analog channels. For most efficient use of time, the multiplexer is acquiring the next channel to be converted while the sample-hold is holding the previous output level for conversion. When conversion is complete, the status line from the converter causes the S/H to return to the sample mode and acquire the new data. After the acquisition time is completed, the sample hold can be switched to hold. A conversion can then begin and the multiplexer can be switched to the next channel.

In applications where the AD346 is to be driven from high impedance sources or directly from an analog multiplexer, a fast slewing, fast settling wideband op amp like the ADLH0032 should be used as an input buffer.

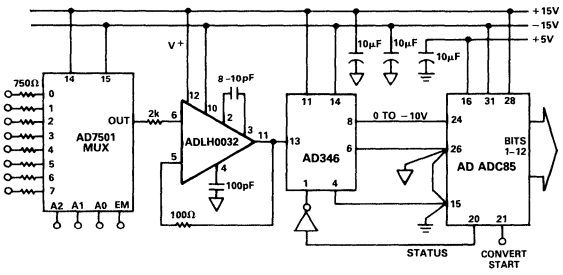


Figure 12. Data Acquisition System

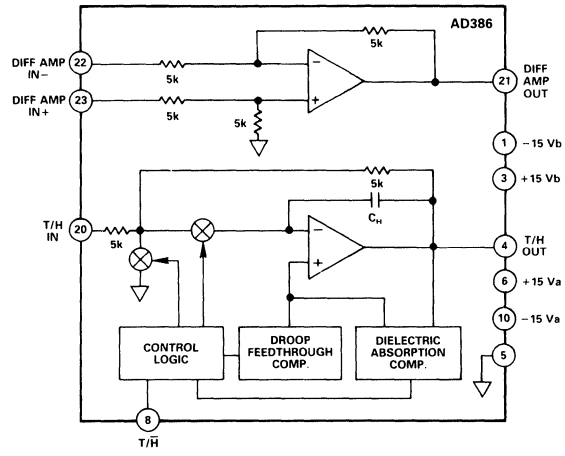
True 16-Bit Track-and-Hold Amplifier

AD386

FEATURES
Companion to True 16-Bit A/D Converters
16-Bit Linear (−40°C to +85°C)
14-Bit Linear (−55°C to +125°C)
Fast Acquisition Time: 3.6 μs to 0.00076%
Low Droop Rate: 20 μV/ms
Differential Amplifier for Ground Sense
Low Aperture Jitter: 40 ps

APPLICATIONS
Medical and Analytical Instrumentation
Signal Processing
Multichannel Data Acquisition Systems
Automatic Test Equipment
Guidance and Control
Sonar

AD386 FUNCTIONAL BLOCK DIAGRAM

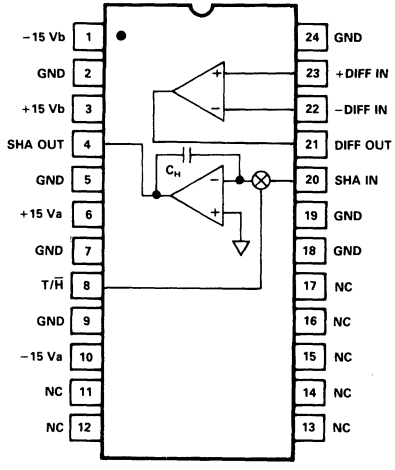


PRODUCT DESCRIPTION

The AD386 is a high accuracy, adjustment free track-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time (3.6 μs to 75 μV) and low aperture jitter (40 ps) make it ideal for use with fast A/D converters.

The AD386 is complete with an internal hold capacitor, and it incorporates a compensation network which minimizes the track-to-hold charge offset and dielectric absorption. The AD386 also includes an internal differential amplifier for very high accuracy applications.

Typical applications for the AD386 include sampled data system, peak hold function, strobe measurement system and simultaneous sampling converter systems. When used with autozero and autocalibration techniques, this T/H combined with a high linearity A/D will offer true 16-bit performance (0.00076% linearity) over the industrial temperature range, and 14-bit performance (0.003% linearity) over the military temperature range.



AD386 Pin Configuration

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Package Option*
AD386BD	0.00076% FSR	−40°C to +85°C	Ceramic (DH-24B)
AD386TD	0.003% FSR	−55°C to +125°C	Ceramic (DH24B)

*See Section 14 for package outline information.

SPECIFICATIONS (@ +25°C unless otherwise noted, V_S = ±15 V ±10%)

Model	Conditions	AD386BD Min	AD386BD Typ	AD386BD Max	AD386TD Min	AD386TD Typ	AD386TD Max	Units
DIFFERENTIAL AMPLIFIER								
INPUT CHARACTERISTICS								
Input Range		±10			±10			V
Common-Mode Range		±10			±10			V
Input Resistance[1]								
Signal			5			5		kΩ
Ground Sense			10			10		kΩ
Offset[2]			0.6	**2.0**		0.6	**2.0**	mV
Offset Drift	T_{min} to T_{max}		10	30		10	30	μV/°C
CMRR	V_{CM} = ±10	**80**	90		**80**	90		dB
PSRR[3]		**76**	85		**76**	85		dB
TRANSFER CHARACTERISTICS								
Gain			−1			−1		V/V
Gain Error				**0.02**			**0.02**	%
Gain Error Drift	T_{min} to T_{max}		1	5		1	5	ppm/°C
Gain Linearity			0.0002	**0.00076**		0.0002	**0.003**	%
Gain Linearity Drift	T_{min} to T_{max}		0.01	0.05		0.01	0.05	ppm/°C
Noise (ENBW = 1.8 MHz)			32	45		32	45	μV rms
DYNAMIC CHARACTERISTICS								
Small Signal Bandwidth			6			6		MHz
Slew Rate			65			65		V/μs
Settling Time[4]								
10 V Step to 1/2 LSB16			2.0	3.0				μs
10 V Step to 1/2 LSB14			0.8	1.5		0.8	1.5	μs
20 V Step to 1/2 LSB16			2.0	**3.0**				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		2.0	3.0				μ s
20 V Step to 1/2 LSB14			0.8	**1.5**		0.8	**1.5**	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		0.8	1.5		0.8	1.5	μs
OUTPUT								
Voltage	R_{LOAD}>3.5 kΩ, T_{min} to T_{max}	±10			±10			V
Current	Short Circuit		15			15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±5		±18	±5		±18	V
Quiescent Current			4.2	**5.0**		4.2	**5.0**	mA
TRACK-AND-HOLD								
INPUT CHARACTERISTICS								
Input Range		±10			±10			V
Input Resistance[1]			5			5		kΩ
Offset[2]			0.6	**2.0**		0.6	**2.0**	mV
Offset Drift	T_{min} to T_{max}		10	30		10	30	μV/°C
TRANSFER CHARACTERISTICS								
Gain			−1			−1		V/V
Gain Error				**0.02**			**0.02**	%
Gain Error Drift	T_{min} to T_{max}		1	5		1	5	ppm/°C
Gain Linearity			0.0002	**0.00076**		0.0002	**0.003**	%
Gain Linearity Drift	T_{min} to T_{max}		0.01	0.05		0.01	0.05	ppm/°C
PSRR[3]		**76**	85		**76**	85		dB
DYNAMIC CHARACTERISTICS								
Small Signal Bandwidth			2			2		MHz
Slew Rate			15			15		V/μs
TRACK-TO-HOLD SWITCHING								
Pedestal + Offset			0.5	**1.5**		0.5	**1.5**	mV
Pedestal + Offset	T_{min} to T_{max}			5.0			7.5	mV
Pedestal Linearity	T_{min} to T_{max}		0.0004	0.00076		0.0004	0.003	%
Aperture Delay			12			12		ns
Aperture Jitter			40			40		ps
Transient Settling[4]								
to 1/2 LSB16	T_{min} to T_{max}		600	**800**				ns
to 1/2 LSB14	T_{min} to T_{max}		400	**500**		400	**500**	ns

Model	Conditions	AD386BD Min	AD386BD Typ	AD386BD Max	AD386TD Min	AD386TD Typ	AD386TD Max	Units
HOLD MODE								
Droop Rate			20	**100**		20	**100**	mV/s
Droop Rate	T_{max}		0.2	1.0		3.6	18	V/s
Feedthrough[5]			−99	**−94**		−99	**−94**	dB
Noise (ENBW = 1.7 MHz)			32	50		32	50	μV rms
PSRR[3]		**60**	66		**60**	66		dB
Dielectric Absorption[6]			7	**10**		7	**10**	ppm
HOLD-TO-TRACK DYNAMICS								
Acquisition Time[4]								
10 V Step to 1/2 LSB16			3.6	4.1				μs
10 V Step to 1/2 LSB14			3.1	3.6		3.1	3.6	μs
20 V Step to 1/2 LSB16			3.6	**4.1**				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		4.0	4.5				μs
20 V Step to 1/2 LSB14			3.1	**3.6**		3.1	**3.6**	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		3.5	4.0		4.0	4.5	μs
DIGITAL INPUTS								
V_{IH}	T_{min} to T_{max}	**2.4**			**2.4**			V
V_{IL}	T_{min} to T_{max}			**0.8**			**0.8**	V
I_{IH}	T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	μA
I_{IL}	T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	μA
OUTPUT								
Voltage	R_{LOAD}>3.5 kΩ, T_{min} to T_{max}	±10			±10			V
Current	Short Circuit		15			15		mA
POWER SUPPLY								
Rated Performance			±15			± 15		V
Operating Range		± 8		±18	± 8		±18	V
Quiescent Current								
Positive Supply			8.0	**12.0**		8.0	**12.0**	mA
Negative Supply		**−6.0**	−5.4		**−6.0**	−5.4		mA
SYSTEM								
Gain Linearity	T_{min} to T_{max}		0.0003	0.00076		0.0003	0.003	%
Acquisition Time[4, 7]								
20 V Step to 1/2 LSB16			4.1	5.1				μs
20 V Step to 1/2 LSB16	T_{min} to T_{max}		4.5	5.4				μs
20 V Step to 1/2 LSB14			3.2	3.9		3.2	3.9	μs
20 V Step to 1/2 LSB14	T_{min} to T_{max}		3.6	4.3		4.1	4.8	μs
Power Dissipation			312	435		312	435	mW
TEMPERATURE RANGE								
Operating		−40		+85	−55		+125	°C
Storage		−60		+150	−60		+150	°C

NOTES
[1]Typical resistance tolerance is ±25%.
[2]After 5 minute warmup at +25°C.
[3]Test conditions: $+V_S$ = +15 V, $-V_S$ = −16 V to −14 V and $+V_S$ = +14 V to +16 V, $-V_S$ = −15 V.
[4]R_{LOAD} = 5 kΩ, C_{LOAD} = 10 pF, settling measured to 1/2 LSB at output.
[5] Measured at 1 kHz.
[6]Dielectric Absorption represents the magnitude of long-term settling artifacts for hold times up to 80 μs as a fraction of the difference in voltages between two successive held samples.
[7]Specifications also apply for 10 V step.
Specifications subject to change without notice.
Specifications in **bold** are 100% production tested.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 800 mW
Input Voltage[2] . . . . . ±18 V
T/$\overline{H}$ Input Voltage . . . . . −0.5 V, + 16 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD386B . . . . . −40°C to +85°C
AD386T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Typical Performance Characteristics

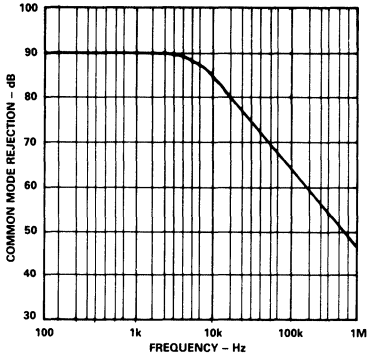


Figure 1. Differential Amplifier Common Mode Rejection vs. Frequency

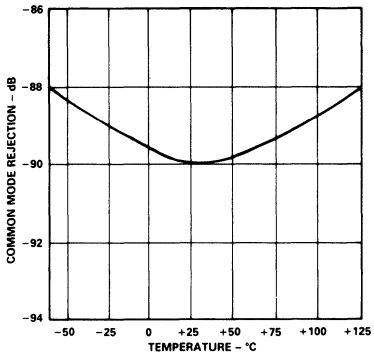


Figure 2. Differential Amplifier Common Mode Rejection vs. Temperature (100 Hz)

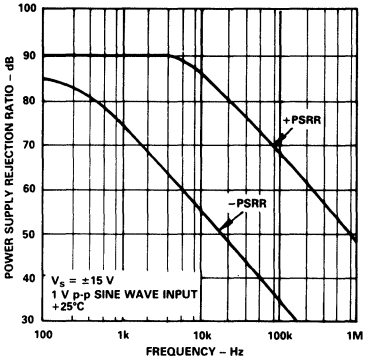


Figure 3. Differential Amplifier Power Supply Rejection vs. Frequency

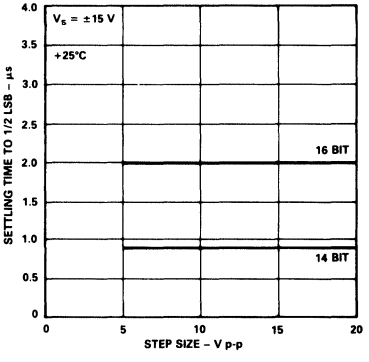


Figure 4. Differential Amplifier Settling Time vs. Step Size

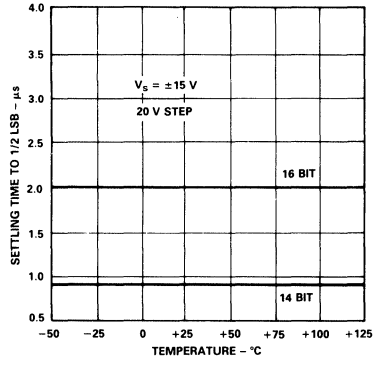


Figure 5. Differential Amplifier Settling Time vs. Temperature

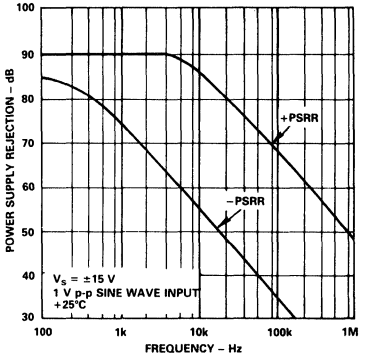


Figure 6. T/H Power Supply Rejection vs. Frequency, Track Mode

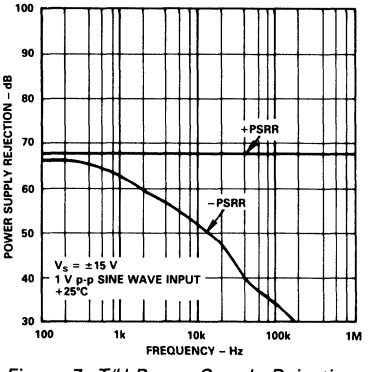


Figure 7. T/H Power Supply Rejection vs. Frequency, Hold Mode

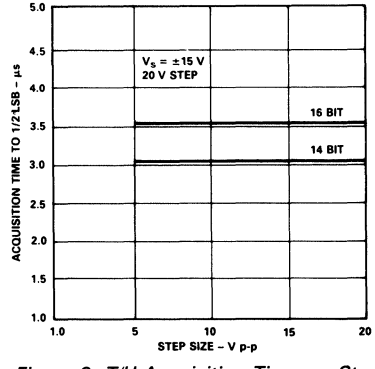


Figure 8. T/H Acquisition Time vs. Step Size

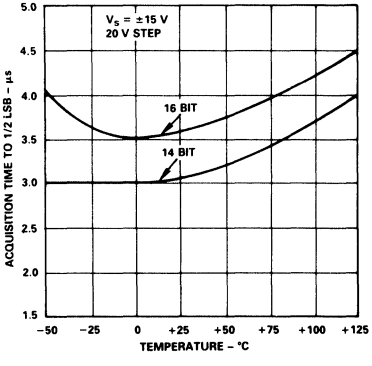


Figure 9. T/H Acquisition Time vs. Temperature

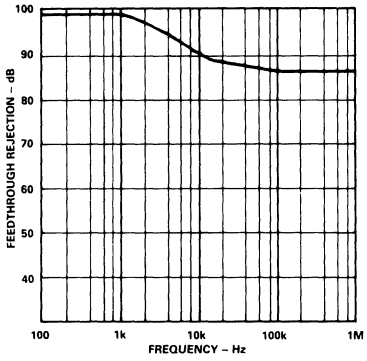


Figure 10. Feedthrough vs. Frequency

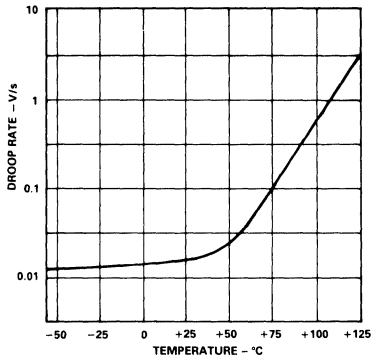


Figure 11. Droop Rate vs. Temperature

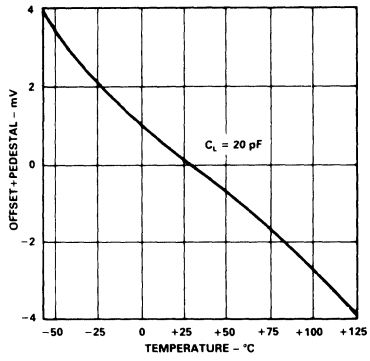


Figure 12. (Pedestal+Offset) vs. Temperature

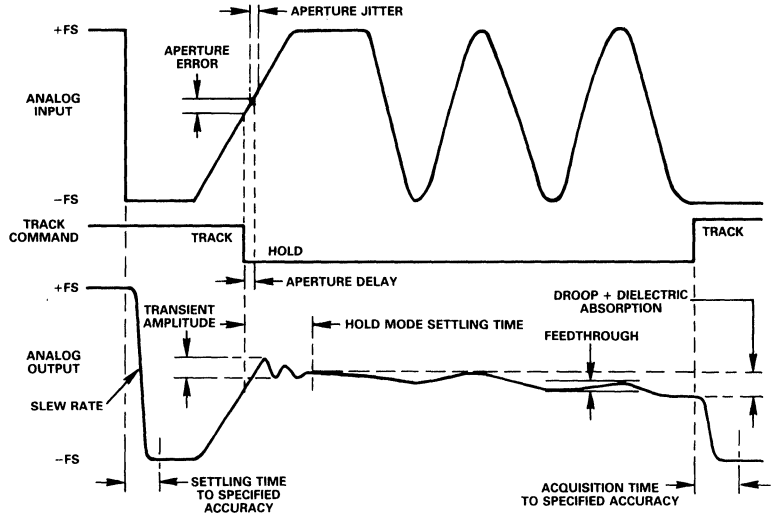


Figure 13. T/H Characteristic Features

TERMINOLOGY

Aperture Delay: the time required by the internal switch(es) to disconnect the hold capacitor from the input, which produces an effective delay in the sample timing.

Aperture Jitter: the uncertainty in Aperture Delay caused by internal noise and the variation of switching thresholds with signal level. The error caused by aperture jitter depends on the rate of change of the input and as such determines the maximum input frequency which can be sampled without error.

Pedestal: a step change in the output voltage which occurs when switching from track mode to hold mode.

Hold Mode Settling Time: the time required for the pedestal to reach its final value to within a specified fraction of full scale.

Droop: the change in the held output voltage resulting from leakage currents.

Feedthrough: the fraction of input signal variation which appears at the output in hold mode as a result of capacitive coupling.

Dielectric Absorption: the tendency of charges within a capacitor to redistribute themselves over time, resulting in "creep" in the voltage of an open circuit capacitor after a large rapid change.

Acquisition Time: the time required after entering track mode for the voltage on the hold capacitor to settle to within a specified fraction of full scale. This is usually specified for a full-scale step change in output voltage.

Settling Time: the time required in track mode for the output to reach its final value within a specified fraction of full scale following a step change in the input voltage.

Nonlinearity: the degree to which a plot of output versus input deviates from the straight line defined by the end points. It is usually specified as a percentage of full scale.

THEORY OF OPERATION

The architecture of the AD386 differs from that usually encountered in inverting Track-and-Hold (T/H) circuits. The hold capacitor in a conventional T/H (Figure 14) is always connected from the amplifier's output to its inverting input. In track mode switch A is open and switch B is closed. Since the summing junction is a virtual ground, the voltage across the capacitor follows the input. The switches change state in hold mode which disconnects the capacitor from the input and holds the output voltage constant. The clamping action of switch A reduces the variations across switch B, improving feedthrough performance.

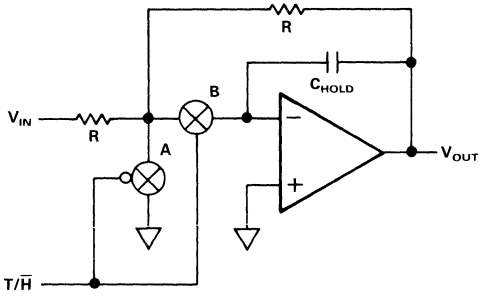


Figure 14. Conventional Inverting Integrator T/H

This circuit forces several tradeoffs. The hold capacitor's charging current is limited by the input resistor. Either the resistor or the capacitor, or both, must be made small to obtain fast acquisition times. A small resistor creates greater demands on the circuit which drives the T/H, while a small capacitor leads to increased pedestal and droop. In addition, the parallel combination of the feedback resistor and the hold capacitor acts as a low pass filter and constrains both bandwidth and acquisition time.

The AD386 uses a four-switch flyback architecture which removes the hold capacitor from the feedback loop during track mode (Figure 15). Switches A and C are open in track mode while switches B and D are closed. This maximizes bandwidth and provides minimum acquisition time because the charging current delivered to the hold capacitor is limited only by the amplifier's output capability. The hold capacitor can be made larger, subject to amplifier stability, since it no longer appears in parallel with the feedback resistor. This helps to reduce droop and pedestal. Switches A and C close in hold mode while switches B and D open, which connects the hold capacitor to the amplifier's inverting input.

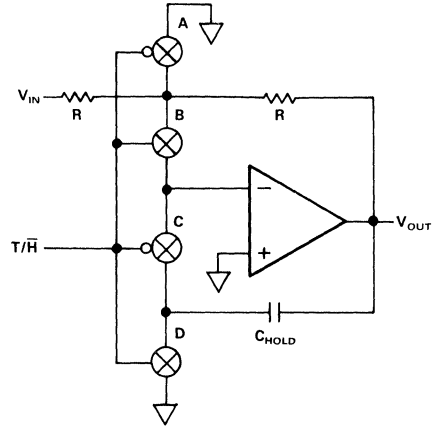


Figure 15. Four-Switch Inverting Flyback T/H

Additional switches and capacitors, not shown in the figure, provide first order cancellation of amplifier and switch leakage currents, switching charge injection, and switch feedthrough. Finally, a small amount of positive feedback is used to reduce dielectric absorption effects.

TRACK-AND-HOLD ERROR CONTRIBUTIONS IN SAMPLED-DATA SYSTEM

Any track-and-hold amplifier imposes performance limits on the system in which it is used. Some of these limits can be derived from the theory of sampled-data systems, some are intrinsic to the T/H, and some depend on details of the system design. Many subtle effects come into play as system resolution increases to 14 or 16 bits, and these can contribute significant errors. Understanding T/H error sources is critical to maintaining signal integrity in a high resolution data acquisition system.

FREQUENCY LIMITATIONS

Three factors set fundamental limits on system performance when digitizing high frequency signals. These are: T/H amplifier bandwidth, aperture uncertainty, and the maximum update rate of the T/H and A/D combination. The track mode bandwidth of the T/H must be significantly greater than the bandwidth of the signals being digitized to prevent the introduction of amplitude and phase errors. The 2 MHz small signal bandwidth of the AD386 attenuates a 35 kHz signal by 0.001 dB and shifts its phase by 1.0 degrees.

There are two different aperture related error terms. The first is aperture delay time, the delay between the HOLD command and the complete opening of internal switches in the T/H. This time amounts to a negative phase delay applied to the input signal because the T/H output can actually continue to track the input for a brief time after the HOLD command. Aperture delay time can be "tuned out" by advancing the assertion of HOLD.

Aperture jitter, the random variations in aperture delay time, causes errors which are directly related to the rate of change of the input signal and which cannot be eliminated by circuit adjustments.

A simple calculation provides the frequency at which aperture jitter produces an error of 1/2 LSB when the input is a full-scale sinusoid. The general result for an N-bit A/D converter is

$$F_{max} = \frac{V_{FS}}{V_{PP}} \times \frac{1}{2^{N+1} \times \pi \times Aperture\ Jitter}$$

where V_{FS} is the A/D converter's input range and V_{PP} is the peak-to-peak value of the input sinusoid. The worst case (minimum) value of F_{max} occurs when V_{PP} is equal to V_{FS}. If the T/H has an aperture jitter of 100 ps and is used with a 16-bit linear A/D, the maximum input frequency is 24.3 kHz.

The same T/H, when used with a 14-bit linear A/D, permits the processing of signals up to 97.1 kHz before aperture jitter-errors become observable. Figure 16 shows these errors as a function of frequency, assuming a full scale input sinusoid, for several values of aperture jitter.

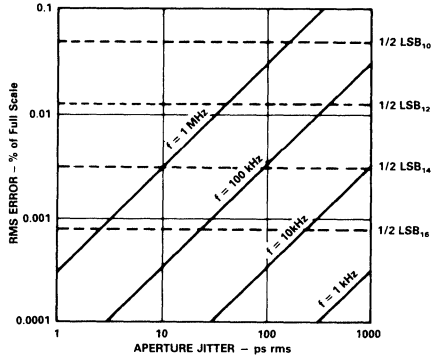


Figure 16. T/H Error vs. Aperture Jitter and Input Frequency

Aperture jitter is often expressed as an rms number. "Peak-to-peak" aperture jitter is usually defined as 6 times this rms value. This comes from probability theory, where 99.7% of the measurements of a random variable will be within 3 standard deviations of the variable's average value. Aperture jitter arises from broadband electrical noise, which is very nearly an ideal random process with a standard deviation equal to its rms value, so multiplication by 6 gives a good approximation to the noise's peak-to-peak value.

A second limit on the input frequency is imposed by the finite time required for signal acquisition and conversion. It is possible to reconstruct any uniformly sampled signal without loss of information provided the sampling rate is at least twice the bandwidth of the input signal; this is the Nyquist criterion, a fundamental result in sampling theory. This limits input frequency to

$$F_{max} = \frac{1}{2 \times (t_{ACQ} + t_{CONV} + t_{AP})}$$

where t_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{AP} is the aperture delay of the T/H. The last term is usually very small and can be ignored. A system composed of a 3.6 μs T/H and a 10 μs A/D can be used successfully to digitize signals with frequency components up to 36.76 kHz. This limit is independent of input signal amplitude. Throughput rates and input frequency ranges for the AD386 in combination with various A/D converters are shown in Table I.

A/D	Conversion Time	Minimum Throughput
ADADC71	50 μs max	18.7 kHz
AD1376/78	17 μs max	48.8 kHz
AD1377	10 μs max	73.5 kHz

Table I. Throughput for AD386 with Various A/D Converters

NONLINEARITIES

Two phenomena directly affect the fidelity of a T/H's transfer function and can degrade system linearity. One of these error sources is track mode nonlinearity. It arises primarily from gain nonlinearity in the T/H's internal amplifier(s). Mismatches in the temperature coefficients of internal resistors may also contribute, but usually do so only for very low frequency signals. The AD386's track mode nonlinearity is about 1/6 16-bit LSB (Figure 17), as is the nonlinearity of the AD386's differential amplifier.

System linearity will also be reduced if the pedestal varies nonlinearly with signal level. Pedestal nonlinearity in the AD386 is below 8 microvolts per volt of input signal, or about 1/2 16-bit LSB.

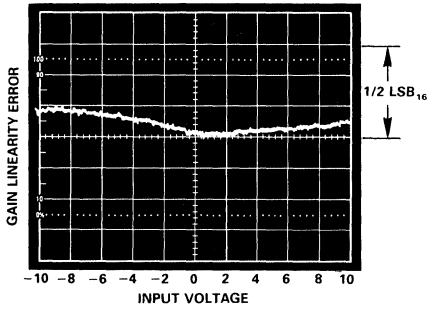


Figure 17. AD386 Track Mode Nonlinearity

FEEDTHROUGH, DROOP, AND DIELECTRIC ABSORPTION

Errors resulting from signal feedthrough and droop must be less than 1/2 LSB in order for the system's linearity to be maintained. The AD386 uses a symmetrical, compensated architecture to minimize both these effects. Feedthrough varies slightly with input frequency from −100 dB below 1 kHz to −86 dB above 100 kHz (Figure 10). This provides 16-bit accuracy for full-scale inputs up to at least 5 kHz and 14-bit performance to beyond 100 kHz.

The circuit's symmetry causes the droop rate to depend on differences in leakage currents between identical junctions under nearly identical bias conditions. The resulting droop is less than 1/2 16-bit LSB (10 V scale) at temperatures up to 85°C and 1/2 14-bit LSB (10 V scale) over the full military temperature range for hold times up to 100 μs.

Capacitors exhibit a memory phenomenon, dielectric absorption (DA), in fast charge, long hold applications. This arises from nonideal behavior of the dielectric material which allows charge storage in the bulk of the dielectric. This bulk charge cannot be removed rapidly because of the long time constant associated with the dielectric's high resistance. A capacitor with dielectric absorption can be modeled as an ideal capacitor in parallel with a series R-C circuit as shown in Figure 18. When such a capacitor is used as the hold capacitor in a T/H the held voltage will tend to creep back towards the voltage held for the previous conversion cycle. The degree and time constant of this behavior depends on the capacitor's dielectric material, as well as on the charge and hold time of the circuit.

Dielectric absorption will cause a variable "offset" if a T/H is used to sample multiple channels with widely varying signals. This causes an apparently nonlinear pedestal because the difference between the currently measured voltage and the previously measured voltage determines the magnitude of the DA error. The AD386 uses a high quality hold capacitor with low intrinsic DA. Residual DA errors are further reduced by laser trimming a compensation network during the manufacturing process. The trimming is performed under typical system timing conditions of 5 μs track, 45 μs hold. The post-trim dielectric absorption error is less than 1/2 16-bit LSB for full-scale changes between samples and hold times between 10 μs and 100 μs.

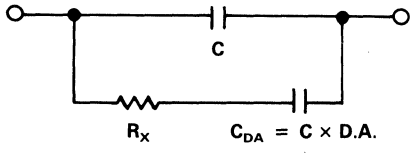


Figure 18. Capacitor Model with Dielectric Absorption

NOISE

Noise generated in a T/H adds to the held signal and causes variations in the output code of an A/D. This noise has two components, one which arises during track mode and another contributed during hold mode. The rms sum of these terms determines the noise performance of the T/H in the system.

Track noise is the noise which gets sampled when entering hold mode. An inverting T/H architecture such as that used in the AD386 has a noise gain of 2. This noise is low pass filtered in the R-C network comprised of the hold capacitor and the switch on resistance (see Figure 19a). The rms value of the track noise is

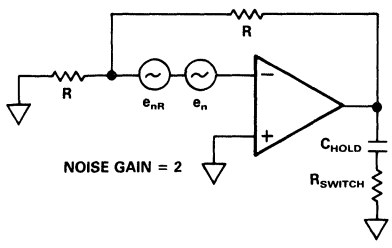
$$\langle e_{nT} \rangle = (op\ amp\ noise) \times (noise\ gain) \times (ENBW)^{1/2}$$

Op amp noise is the rms sum of the amplifier's broadband voltage noise and the thermal noise contributions of the input and feedback resistors, about 17 nV/$\sqrt{\text{Hz}}$. Other noise sources, including amplifier current noise and switch thermal noise, are negligible. ENBW, the equivalent noise bandwidth, is

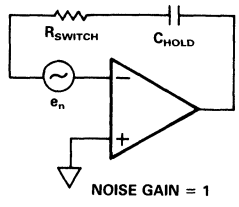
$$ENBW = \frac{\pi}{2} \times \frac{BW1 \times BW2}{BW1 + BW2}$$

where BW1 is the small signal bandwidth of the T/H in track mode (2 MHz for the AD386) and BW2 is the corner frequency of the R_{SWITCH}–C_{HOLD} combination (2.7 MHz). The resulting track noise in the AD386 is at most 46 μV rms.

Noise gain is reduced to 1 in hold mode, and input and feedback resistor thermal noise makes no contribution (Figure 19b). The equivalent noise bandwidth now depends on the T/H's small signal bandwidth and the characteristics of the A/D converter used in the system. This is because the signal at the input



a. Track Mode



b. Hold Mode

Figure 19. Dominant AD386 Noise Sources

of the comparator in a successive approximation A/D converter is filtered by the converter's input resistance and the summing junction capacitance. ENBW is calculated as before, but now BW1 is the T/H's small signal bandwidth in hold mode (4 MHz for the AD386), and BW2 is the bandwidth of the A/D's input R-C. BW2 is about 700 kHz in the AD ADC71 and AD1376 and roughly 1.7 MHz in the AD1377 and AD1378 (assuming a 10 V span). The respective values of ENBW are 940 kHz and 1.9 MHz. The hold noise contribution of the AD386 is about 16 μV rms when used with the AD ADC71 or AD1376 and 22 μV rms when used with the AD1377 or AD1378; this noise is 30% less for a 20 V span and 40% greater for a 5 V span because changes in the A/D's input resistance cause changes in BW2.

The total noise is the rms sum of these two results:

$$\langle e_n \rangle = [\langle e_{nT}^2 \rangle + \langle e_{nH}^2 \rangle]^{1/2}$$

This yields 49 μV rms and 51 μV rms for the two cases. Track noise dominates in both instances.

When the AD386's differential amplifier is used, its noise contribution will be band limited and sampled by the T/H. The equivalent bandwidth for this noise is also 1.8 MHz and the contribution to the track noise is 46 μV rms. The total track noise is the rms sum of 46 μV and 46 μV, or 65 μV rms, and the overall noise for the complete AD386 used with any of the above A/D converters is at most 70 μV rms.

The rms value represents one standard deviation if the noise has a Gaussian distribution, which is usually the case for wideband electrical noise. If a constant noise-free voltage is sampled a large number of times, the held result will be within one standard deviation of the ideal value 32% of the time, within two standard deviations 95% of the time, and within three standard deviations 99.7% of the time. The entries in Table II were calculated using three standard deviations as the definition of the peak-to-peak noise.

Span	No. Bits	rms Noise LSBs	p-p Noise LSBs
10 V	14	0.11	0.66
20 V	14	0.06	0.36
10 V	16	0.45	2.7
20 V	16	0.23	1.4

Table II. AD386 Noise Contribution as a Function of A/D Span and Resolution

POWER SUPPLY REJECTION

Variations on the power supply lines, both dc and ac, can lead to unwanted changes in the voltage acquired by a T/H. Power supply variations in track mode cause the output voltage, and hence the voltage across the hold capacitor, to vary. PSRR decreases with increasing frequency, making well regulated, low noise linear power supplies and proper bypassing essential in a high resolution data acquisition system.

Equally important, but usually forgotten or omitted, is hold PSRR. This is frequently much worse than track PSRR because parasitic capacitances which are not significant in track mode couple into the extremely high impedance nodes which exist in a T/H during hold mode. This specification is essential to the system designer, as hold mode PSRR often determines the performance required from the system's power supplies. The power supply rejection of the AD386 is specified and characterized in both track and hold modes.

Pedestal arises from the transfer of charge from the internal switching circuitry to the hold capacitor during the transition from track mode to hold mode. Pedestal in some T/H circuits is extremely sensitive to changes in the high and low levels of the external control signal. The AD386 uses an internal +5 V supply and logic buffers to prevent this behavior.

GROUNDING

All voltage measurements in a data acquisition system are eventually referenced to ground. Variations in the "ground" potential through the system resulting from resistive drops of power supply and signal return currents as well as from interference from external sources may add to the signal being digitized and produce false results. The grounding scheme in a high resolution system cannot be left to chance and must be planned as carefully as any other aspect of the system's design. Proper grounding and the reduction of externally induced ground noise are discussed at length in the following Applications section.

Applications

GROUNDING. DECOUPLING, AND LAYOUT CONSIDERATIONS

Many data acquisition systems have two or more ground pins which are not connected together within the device(s). These "grounds" may be referred to as Logic Power Return, Digital Return, Analog Ground, Analog Power Return, Signal Ground, etc., and they must be connected together somewhere within the system to establish a measurement reference point. Good grounding practice dictates that these grounds be tied at a single point, sometimes called a star or "Mecca" ground. In high resolution systems the star point is often located at the A/D, with a single, short, low impedance trace leading from there to the analog supply "common" terminal. The ideal is to use a solid analog ground plane beneath the T/H and A/D as the star point.

Because circuit traces have resistance and inductance, currents in the various ground runs can create voltage differences of hundreds of millivolts between "ground" in different parts of the system. Power supply and signal ground traces should be separate to prevent summing power supply return currents with analog signal currents, which would lead to measurement errors. It is also important to avoid closed circuit loops in system ground connections. A loop can act as a very effective antenna, coupling voltages created by stray magnetic fields into the measurement system.

Each of the AD386's power supply terminals should be capacitively bypassed to the ground plane as closely as possible to the device. This is best done using 0.01 μF to 0.1 μF ceramic capacitors. High frequency supply noise rejection may be further improved by placing small (4.7 Ω to 10 Ω) carbon composition resistors in series with the supply leads. These resistors, in combination with the ceramic capacitors, act as local low pass filters and prevent crosstalk between system components. The bypassing scheme should also include solid Tantalum capacitors of 1 μF to 10 μF from each supply to ground in the critical areas of the board. Proper grounding and bypassing techniques are shown in Figure 20.

All AD386 ground pins (Pins 2, 5, 7, 9, 18, 19, and 24) should be connected to the analog ground plane.

WARNING: Improper bypassing can result in poor settling performance or high frequency oscillations.

The metal cover of the AD386 is internally grounded to provide additional shielding. Do not make any external connection to the cover.

DIFFERENTIAL AMPLIFIER

Many high resolution applications require the ability to sense ground at the signal source. This is especially true in systems with physical or thermal constraints that make it necessary to locate the T/H and A/D at some distance from the transducer. Under these conditions stray electromagnetic fields may cause "ground" at the signal source to be at a different potential from "ground" at the A/D despite the designer's best efforts. This will give rise to measurement errors because the potential difference will appear to be added to the true signal. The AD386's differential amplifier may be used to eliminate this type of ground noise as shown in Figure 21.

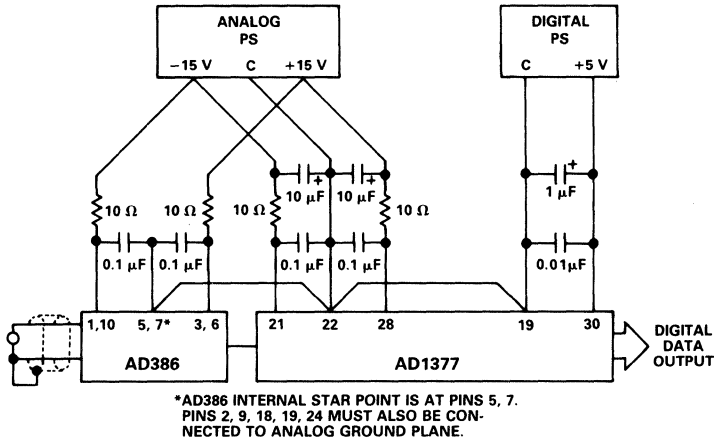
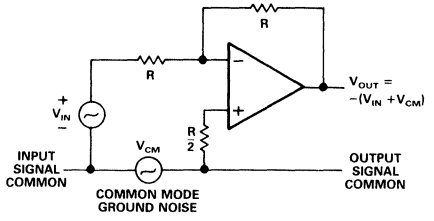
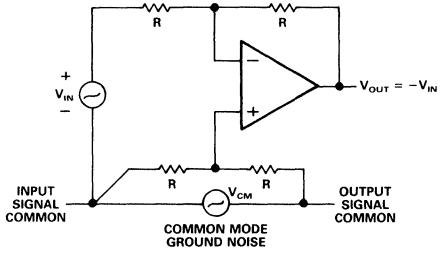


Figure 20. Proper Grounding and Supply Bypassing Techniques for a High Resolution Data Acquisition System



a. Without Differential Amplifier



b. With Differential Amplifier

Figure 21. Effects of Common Mode Noise

In extremely noisy environments it may be necessary to connect the differential amplifier to the signal source with shielded twisted pair cable. The shield should be connected to ground at the transducer and should be left floating at the AD386. This shielding technique is shown in Figure 22. The cable presents a capacitive load, and the signal source must be capable of driving this load without ringing or oscillations. The differential amplifier's noninverting input should be connected to Pin 24 if ground sensing is not required.

Another use of the differential amplifier is to restore signal polarity. Like most high resolution T/H amplifiers, the T/H in the AD386 operates in the inverting mode. The differential amplifier may be used to provide a second inversion so that the T/H output has the same polarity as the sensor output.

The differential amplifier also provides a low dynamic source impedance to the T/H section. This absorbs transients produced when the T/H switches from hold mode to track mode, providing optimal settling performance.

The T/H and differential amplifier have independent power supply connections. This permits a reduction in system power dissipation when the differential amplifier function is not needed.

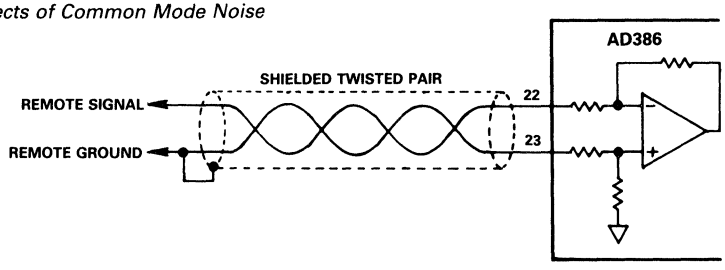


Figure 22. Remote Ground Sensing in a Noisy Environment

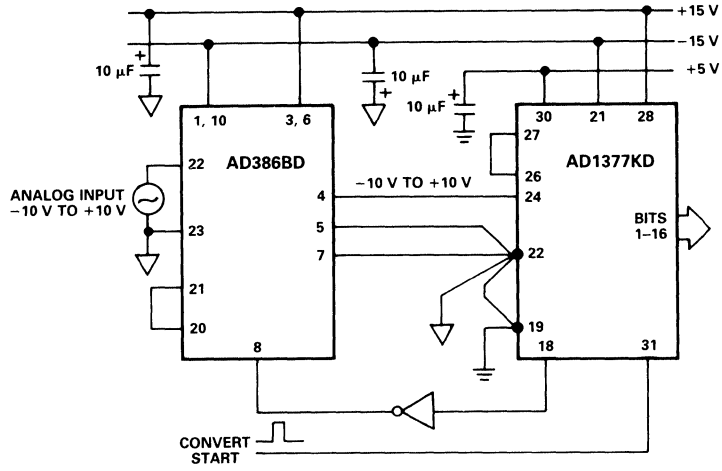


Figure 23. Basic Data Acquisition System (Some Supply Bypassing Omitted for Clarity)

6

GAIN AND OFFSET ADJUSTMENT

The usual practice in the design of data acquisition systems is to incorporate a single system level trim for offsets and a second for gain errors, rather than to trim each element in the signal processing chain. Traditionally these trims involve potentiometers or fixed resistors. The trims should be designed so that nulling static errors does not introduce new errors such as noise, increased thermal drift, or nonlinearity.

The offset, drift, and gain errors of the AD386 are laser trimmed during manufacture and no external adjustment capabilities are provided. This prevents the introduction of noise through offset adjust terminals and preserves the excellent gain linearity and drift performance. Most A/Ds provide for nulling gain and offset errors with a range sufficient to include the contributions of the AD386. Of course, it is also possible to include calibration routines in the system's software to eliminate mechanical adjustments.

HIGH RESOLUTION DATA ACQUISITION SYSTEM

The essential details of a high resolution data acquisition system using the AD386 are shown in Figure 23. Conversion is initiated by the falling edge of the CONVERT START pulse. This edge drives the A/D's STATUS line high. The inverter then drives the AD386 into hold mode. STATUS remains high throughout the conversion and returns low once the conversion is completed. This allows the AD386 to reenter track mode. The throughputs given in Table I were calculated based upon this circuit configuration.

One drawback of this connection becomes apparent if the system's grounding is marginal. The falling edge of CONVERT-START resets the successive approximation register within the A/D, causing transient currents in both the analog and digital return paths. These transients vary depending on the input signal and the prior conversion result. The same edge also drives the T/H into hold mode. The exact timing relationship of these two events depends upon differences in propagation delays. The T/H's held value may be affected if the A/D reset transient begins before the T/H has fully entered hold mode. The end result is system nonlinearity.

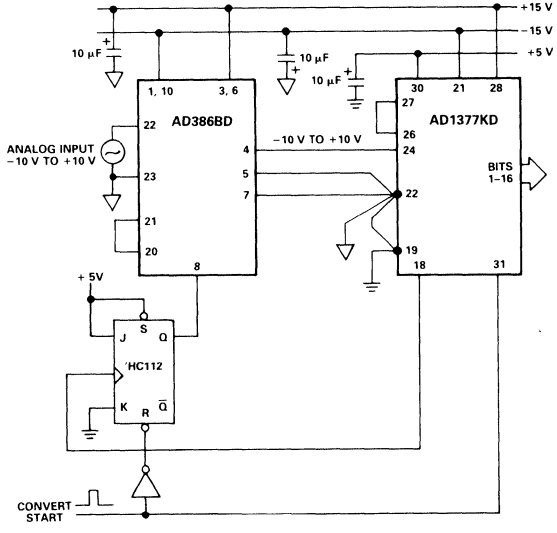


Figure 24. Improved Data Acquisition System (Some Supply Bypassing Omitted for Clarity)

This problem can be avoided with the addition of a flip flop as shown in Figure 24. The rising edge of CONVERT START places the T/H into hold mode before the A/D reset transients begin. The falling edge of STATUS places the AD386 back into track mode. System throughput will be reduced if a long CONVERT START pulse is used. Throughput can be calculated from

$$Throughput = \frac{1}{T_{ACQ} + T_{CONV} + T_{CS}}$$

where T_{ACQ} is the T/H acquisition time, T_{CONV} is the time required for the A/D conversion, and T_{CS} is the duration of CONVERT START. No significant T/H droop error will be introduced provided the width of CONVERT START is small compared with the A/D's conversion time.

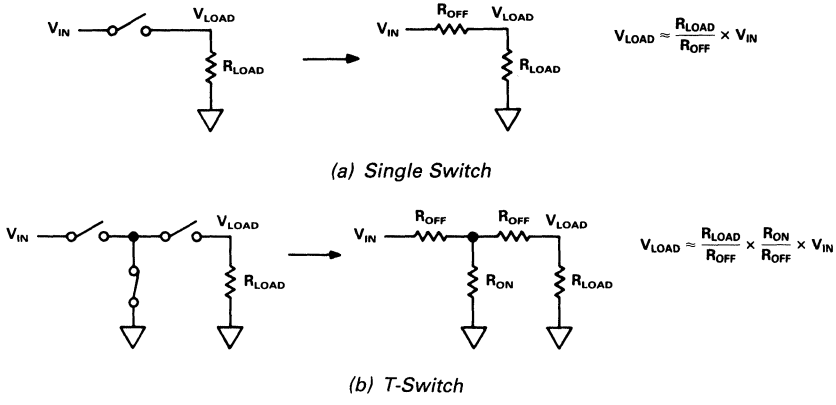


Figure 25. Single and "T" Analog Switches (Shown in OFF Position)

MULTICHANNEL SYSTEMS

The design of multiplexed data acquisition systems which maintain 14- or 16-bit signal fidelity is an extremely demanding task. One of the first difficulties encountered is the lack of adequate analog switches. The specified feedthrough performance of most switches and multiplexers is seldom better than −80 dB. This is an order of magnitude too high for a 16-bit system with its 8 parts-per-million sensitivity. A "T" switch configuration can be used to reduce feedthrough as shown in Figure 25. The improvement in "off" isolation relative to a single switch is substantial.

A few monolithic video T-switch ICs are now available and provide the necessary isolation in the dc-50 kHz frequency range. Unfortunately, these devices have voltage limitations which restrict their utility. It will usually be necessary to design a multiplexer using analog multiplexer and switch ICs. Figure 26 shows a simple 4-channel single-ended T-switch multiplexer and includes a high performance buffer (see below).

The on-resistance of analog switches and multiplexers is a nonlinear function of signal voltage. This will produce severe nonlinearity in a system in which a multiplexer supplies signals

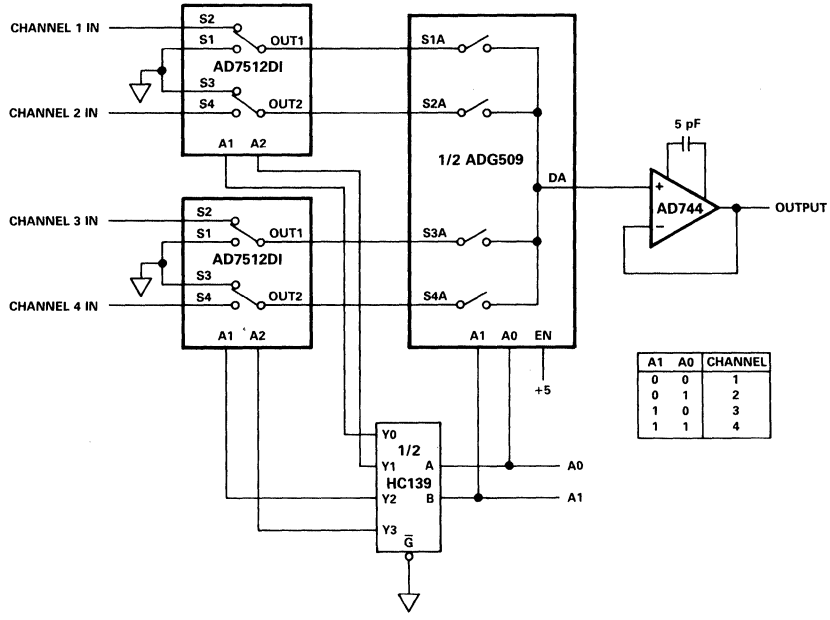


Figure 26. Four-Channel T-Switch Multiplexer(Power Supply Connections Not Shown)

directly to an AD386. A high-impedance buffer between the multiplexer and the T/H's input can solve this problem but may introduce several others.

An op amp in the noninverting gain-of-1 configuration is the obvious candidate for a buffer. The amplifier must settle quickly to maximize system throughput and must be extremely linear to maintain system performance. The linearity of this configuration depends upon the linearity of both the amplifier's open loop gain and common-mode rejection (linear errors in these parameters result only in system gain error, but nonlinear gain and CMRR produce system nonlinearity). Neither of these parameters is specified by most amplifier manufacturers.

A buffer may also increase system noise. Applications which require ground- sensing will require two buffers, resulting in 40% more noise than a one-buffer system.

Finally, a buffer will add its own offset to the signal being measured. Software calibration of the error and its drift is possible using a permanently grounded multiplexer channel.

The AD744 is a nearly ideal buffer for multiplexed systems. This amplifier provides offsets as low as 250 μV and an offset drift of 3 μV/°C while maintaining 16-bit linearity over the −40°C to +85°C temperature range. Typical settling times at room temperature are 2.3 μs (14 bits) and 3.5 μs (16 bits) for the AD744 combined with the AD386's differential amplifier. The increase in noise at the differential amplifier's output will be about 6 μV rms in a one-buffer system and roughly 12 μV rms in a two buffer system (recall that a 16-bit LSB in a 20 volt system is 305 μV). The AD744 is not unity-gain stable, and compensation is required. A 5 pF compensating capacitor is sufficient to ensure stability. The settling times listed above were measured using a 9 pF compensation capacitor which provides greater stability with moderate capacitive loads.

The NE5534 can also be used as a buffer to deliver 16-bit linearity. This amplifier also requires slight compensation to achieve unity-gain stability; 10 pF is sufficient. Settling is somewhat slower than the AD744, about 5 μs to 14 bits and 6 μs to 16 bits, including the AD386's differential amplifier when measured at room temperature. The 5534 has lower voltage noise and will cause only a 1 or 2 μV rms increase in the total noise at the differential amplifier's output. The NE5534 lacks the precision offset and drift performance of the AD744.

Multiplexed throughput can be improved with the proper choice of system timing. If the new input channel is selected while the AD386 is in Hold mode, then multiplexer, buffer, and differential amplifier settling can occur during the A/D conversion. In this case throughput is determined only by the sum of the T/H acquisition and A/D conversion times. The effects of T/H feedthrough must be considered when using this type of overlap in system timing.

There is another solution to many of the problems of multiplexed systems when the speed of channel switching is not critical: relays. Relays should be selected for good shielding, low thermal EMF, and low on-resistance. The only significant drawback of this approach, other than switching speed and size, is power dissipation. In all other respects relays offer a near-perfect solution to the problems of high resolution system design discussed above.

DYNAMIC PERFORMANCE

Dynamic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD) are important in many signal processing applications. SNR and THD are affected by both the T/H and A/D. The errors contributed by the T/H are generally dependent upon the input signal frequency, while those contributed by the A/D converter usually are not. The dynamic performance of a T/H-A/D pair is characterized using Fast Fourier Transform (FFT) techniques.

Figures 27–31 show the results of several 1024-point FFTs which demonstrate the exceptional distortion and noise performance of the AD386 when combined with the AD1377. These FFTs were obtained using a circuit similar to that of Figure 24. The input signal was processed by both the differential amplifier and T/H sections of the AD386 and was sampled at an 83.333 kHz rate. The AD1377's clock was adjusted to yield an 8.0 μs conversion time, which provided 4.0 μs for the AD386 to acquire each new sample. The vertical scale for these figures is based on a full-scale input referenced as 0 dB. The system was configured for a 10 volt span.

Figures 27 and 28 illustrate the system's low frequency noise and distortion performance. The input frequency is 1.546 kHz. When the input is −0.3 dB, nearly full scale, the largest harmonic component is −102.8 dB (Figure 27). Total harmonic distortion, the rms sum of the second through fifth harmonics, is −99.9 dB. The signal to noise ratio is 89.9 dB. The ultimate noise floor can be determined using a lower level input. Reducing the input level about 20 dB, as in Figure 28, decreases the

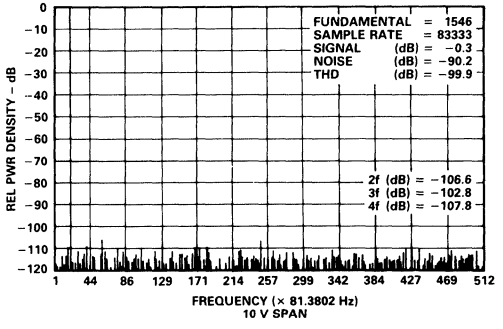


Figure 27.

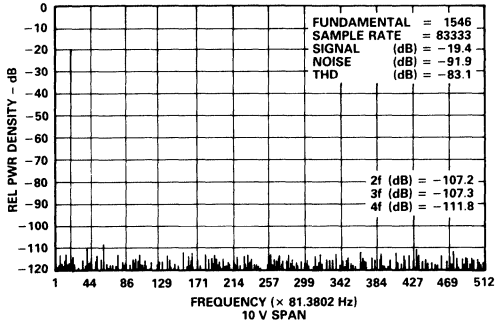


Figure 28.

noise floor by 1.8 dB to −91.9 dB. This corresponds to a total AD386 noise contribution of about 45 μV rms. The FFT noise floor would improve about 2 dB with the system configured for a 20 volt span because the effect of noise contributed by the AD386 is reduced as a result of the increased LSB size.

System performance just beyond the high end of the audio band is shown in Figure 29. Here the input is a −0.3 dB sinusoid at 21.24 kHz. The only significant harmonic component, the second harmonic, is −91.9 dB with respect to the fundamental, and THD is −91.1 dB. The noise floor is 0.5 dB greater than in Figure 27. The additional noise is contributed by higher-order harmonics; the second through fifth harmonics have been excluded from the noise floor calculations, but higher harmonics are considered to be "noise". These harmonics arise from the AD386's aperture jitter. The additional noise is consistent with an rms jitter of 40 ps.

In Figures 30 and 31, −0.3 dB and −20.1 dB inputs at 40.61 kHz show system performance near the Nyquist frequency. Even at this high frequency a full-scale input produces THD of only −84.6 dB, dominated by the second harmonic at −85.1 dB (Figure 31). In Figure 31 the harmonics have been eliminated by reducing the input level by a factor of 10.

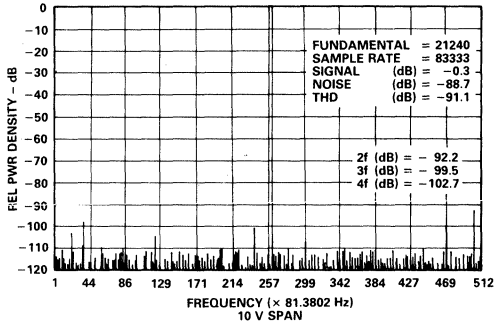


Figure 29.

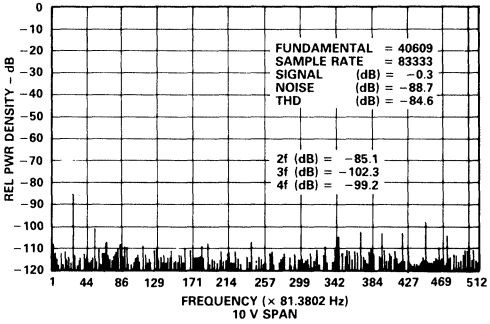


Figure 30.

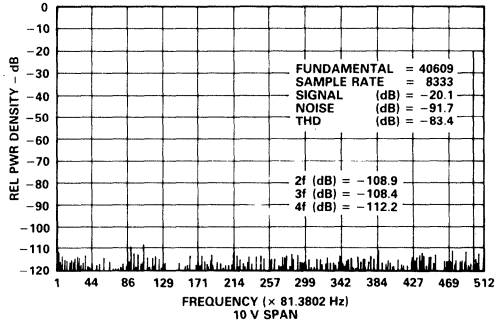


Figure 31.

ANALOG DEVICES

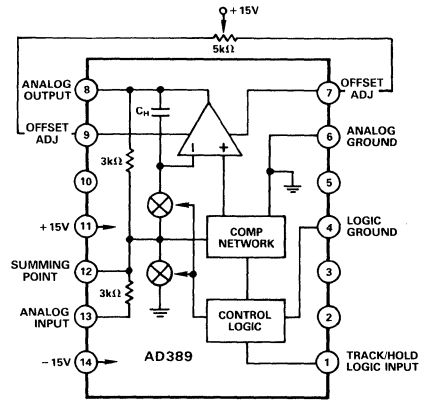
High Resolution Track-and-Hold Amplifier

AD389

FEATURES

Companion to High Resolution A/D Converters
Fast Acquisition Time: 2.5μs to ±0.003%
Low Droop Rate: 0.1μV/μs
Aperture Jitter: 400ps
Internal Hold Capacitor
Unity Gain Inverter
Low Power Dissipation: 300mW

AD389 FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD389 is a high accuracy, adjustment free track-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time (2.5μs to ±0.003%) and low aperture jitter (400ps) make it suitable for use with fast A/D converters to digitize signals up to 40kHz.

The AD389 is complete with an internal hold capacitor and it incorporates a compensation network which minimizes the sample to hold charge offset.

Typical applications for the AD389 include sampled data systems, peak hold functions, strobed measurement systems and simultaneous sampling converter systems. When used with autozero and autocalibration techniques, this T/H combined with a high linearity A/D will offer 14-bit performance over the converter's full no-missing-code temperature range.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "B" specified over the full industrial temperature range, −25°C to +85°C. High reliability processing is available; contact factory for information.

PRODUCT HIGHLIGHTS

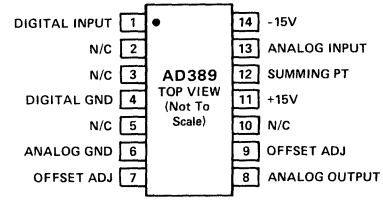
1. The AD389 is the ideal companion track-and-hold amplifier to 14-bit accurate A/D converters.
2. The AD389 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
3. The droop rate is only 0.1μV/μs so that it may be used in slower high resolution systems without the loss of accuracy.
4. The fast acquisition time and low aperture make it suitable for high speed data acquisition systems and digital audio recording.
5. The AD389 T/H amplifier is ideal for applications requiring wide dynamic range.
6. Clever circuit design eliminates any measurable thermal tail (see Figures 11a and 11b).

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD389KD	0 to +70°C	DH-14A
AD389BD	−25°C to +85°C	DH-14A

*See Section 14 for package outline information.

PIN CONFIGURATION



SPECIFICATIONS (typical @ +25°C and nominal power supply voltage of ±15V unless otherwise noted)

Model	AD389KD	AD389BD	Units
ANALOG INPUT			
Voltage Range	±10 min	*	V
Overvoltage, no damage	±15 max	*	V
Impedance	3000	*	Ω
DIGITAL INPUT (TTL Compatible)			
Track Mode, Logic "1"	2 to 5.5V	*	V
Hold Mode, Logic "0"	0 to 0.8V	*	V
Logic "1" Current	20 (max)	*	μA
Logic "0" Current	−360 (max)	*	μA
ANALOG OUTPUT			
Voltage	±10 min	*	V
Current	3	*	mA
Short Circuit Current	20	*	mA
Impedance	1	*	Ω
DC ACCURACY/STABILITY			
Gain	−1.00	*	V/V
Gain Error	±0.01 (±0.02 max)	*	%
Gain Nonlinearity (±10V Output Track)	±0.001	*	%
Gain Temperature Coefficient	1 (5 max)	*	ppm/°C
Offset Voltage	±3 max, adjustable to zero	*	mV
Output Offset @ T_{min}, T_{max} (Track)	±6	*	mV
TRACK MODE DYNAMICS			
Frequency Response			
Small Signal (−3dB)	1.5	*	MHz
Full Power Bandwidth	0.5	*	MHz
Slew Rate	30	*	V/μs
Noise in Track Mode, dc to 1.0MHz	200	*	μV rms
TRACK-TO-HOLD SWITCHING			
Aperture Time	30	*	ns
Aperture Uncertainty (Jitter)	0.4	*	ns
Offset Step (Pedestal)	±2 (4 max)	*	mV
Pedestal with Temperature	±4	±6	mV
Switching Transient			
Amplitude	200	*	mV
Settling to 1mV	0.5 (2 max)	*	μs
Settling to 0.3mV	1.0 (3 max)	*	μs
HOLD MODE DYNAMICS			
Droop Rate	0.1 (1 max)	*	μV/μs
Droop Rate at T_{max}	10 max	40 max	μV/μs
Feedthrough Rejection (10V p-p @ 20kHz)	86 (74 min)	*	dB
HOLD-TO-TRACK DYNAMICS			
Acquisition Time to ±0.01% of 20V	1.5 (3 max)	*	μs
Acquisition Time to ±0.003% of 20V	2.5 (5 max)	*	μs
POWER REQUIREMENTS			
Nominal Voltages for Rated Performance	±15 (±3%)	*	V
Operating Range[1]	±11 to ±18	*	V
Power Supply Rejection	100	*	μV/V
Supply Current			
$+V_S$	15 (20 max)	*	mA
$-V_S$	−4 (10 max)	*	mA
Power Dissipation	300 (500 max)	*	mW
TEMPERATURE RANGE			
Operating	0 to +70	−25 to +85	°C
Storage	−55 to +125	*	°C
THERMAL RESISTANCE			
Junction to Air, θ_{JA} (free air)	60	*	°C/W
Junction to Case, θ_{JC}	20	*	°C/W

NOTES

[1]Operating to derated performance with $|V_{IN}| < |V_S - 5V|$.

*Specifications same as AD389KD.

Specifications subject to change without notice.

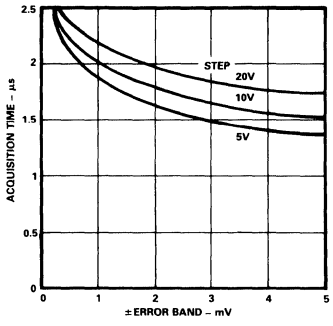


Figure 1. Acquisition Time vs. Final Error Band

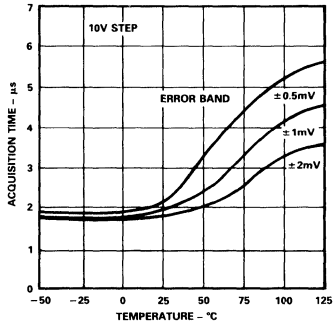


Figure 2. Acquisition Time vs. Temperature

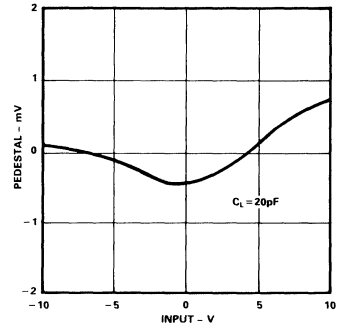


Figure 3. Pedestal vs. Input Voltage

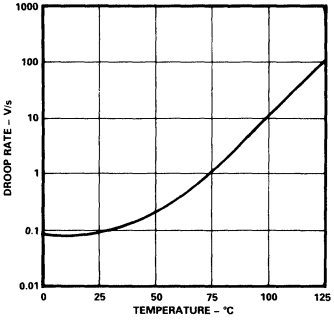


Figure 4. Droop Rate vs. Temperature

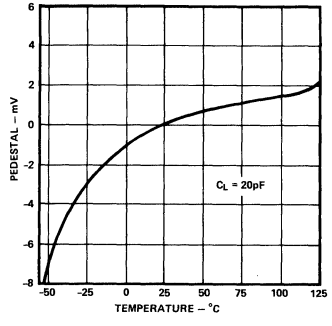


Figure 5. Pedestal vs. Temperature

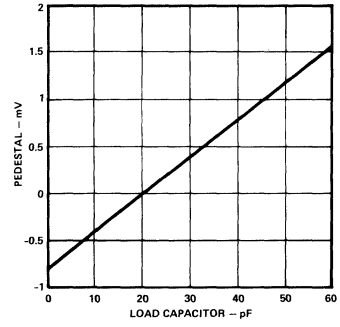


Figure 6. Pedestal vs. Load Capacitor

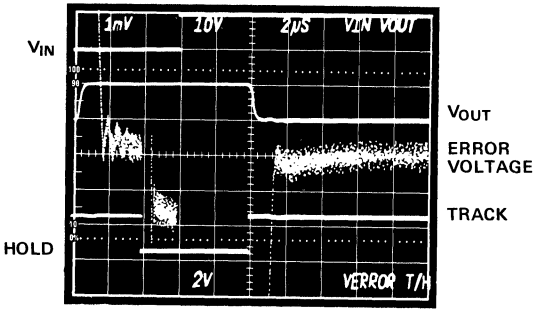


Figure 7. Hold to Track Acquisition Time

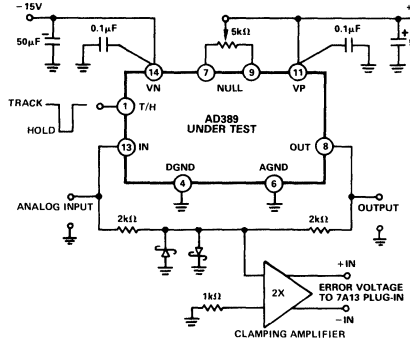


Figure 8. Pedestal and Acquisition Time Test Circuit

TERMINOLOGY

Aperture Time is the time required after the "hold" command until the switch is fully open and it produces a delay in the effective sampling timing.

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the track-to-hold command with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency.

Acquisition Time is the time required by the device to reach its final value within a given error band after the track command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage.

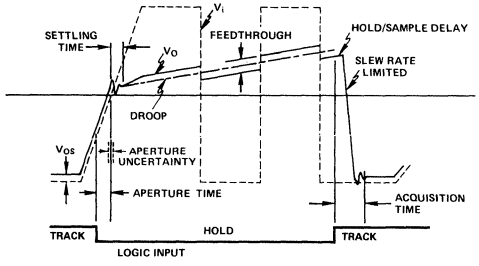


Figure 9. Pictorial Showing Various T/H Characteristics

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Pedestal during hold is a track-to-hold offset. This is an offset that occurs from such phenomena as charge dumps when switches are opened, and coupling of the logic signal transients.

Thermal Tail is the slow drift of the output stage as it settles to the final value with a thermally induced offset due to self-heating; see Figures 11a and 11b.

Transients are the spikes or glitches that occur on the output at the start and end of hold time.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, preferably as close to the A-to-D converter as possible. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pins of the AD389. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

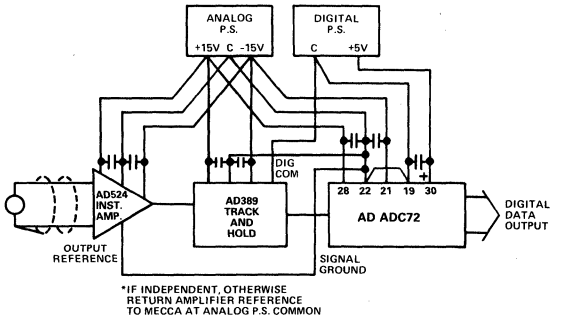


Figure 10. Basic Grounding and Decoupling Practice

DECOUPLING

The AD389 can only settle accurately and fast if the power supplies do not change during transients. Therefore, it is necessary to put 0.1 microfarad (0.1μF) decoupling capacitors right between the supply and analog ground pins and to have 50μF tantalum caps close by.

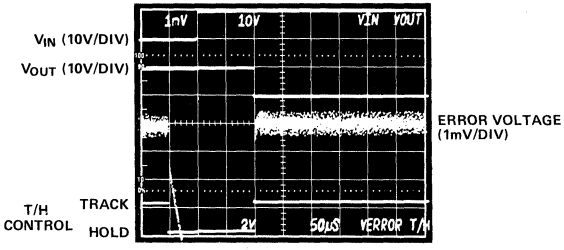


Figure 11a. Acquisition Time after 100μs in the Hold Mode. The AD389 Shows no "Thermal Tail".

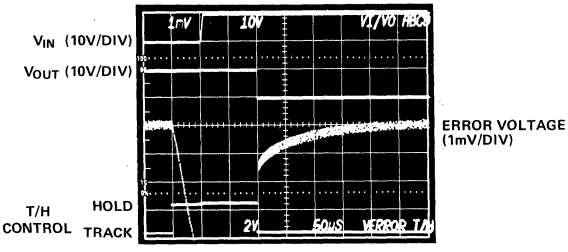


Figure 11b. Typical Thermal Tail and Acquisition Time of Other 12-Bit T/Hs Make them Unsuitable for High Resolution Applications

SAMPLED DATA SYSTEMS

The fast acquisition time of the AD389 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. Figures 12 and 13 show the use of an AD389 with the ADC72 and AD376.

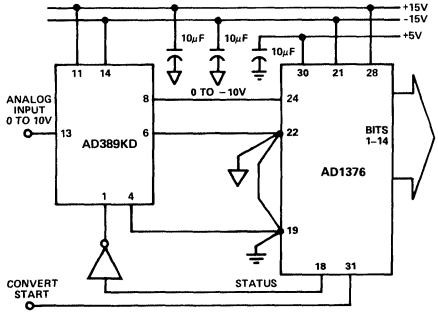


Figure 12. 20kHz–14-Bit, A/D Conversion System

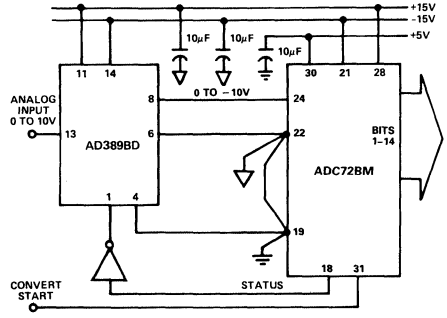


Figure 13. 8.3kHz–14-Bit, A/D Conversion System for −25°C to +85°C Operation

In sampled data systems there are two limiting factors in digitizing high frequency signals. The first limitation is the bandwidth and aperture uncertainty of the sample-and-hold amplifier. The second limitation is the maximum update rate for the T/H and A/D converter combination. For high throughput rate data acquisition systems all factors must be understood.

The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input which is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the A/D converter.

$$F_{max} = \frac{(\text{Full Scale Voltage})\ (2^{-N})}{(\text{Full Scale Voltage})\ (2\pi)\ (\text{Aperture Jitter})}$$

For an application with a 14-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-14}}{(10)\ (2\pi)\ (4 \times 10^{-10}\ \text{sec})} = 24\text{kHz}$$

For an application with a 12-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-12}}{(10)\ (2\pi)\ (4 \times 10^{-10}\ \text{sec})} = 97\text{kHz}$$

Note that some additional aperture delay and jitter are added if the AD389 is not driven directly from the convert start line, but from the status line, which from some converters is delayed.

The maximum throughput rate is the sum of the sample-and-hold acquisition time, settling time and the A/D conversion time.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, with an ideal brickwall low pass filter has been placed in the signal path prior to the AD389 and A/D converter to eliminate aliasing.

AD389 in Combination With an	Throughput Rate	Input Frequency Range
ADC71 (13 bit)	22.2kHz	dc to 11.1kHz
ADC72 (14 bit)	16.7kHz	dc to 8.3kHz
AD1376 (14 bit)	40.0kHz	dc to 20kHz

Table I. T/H & ADC Combinations and Maximum Throughput Rate

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients, and minimal droop rate.

For sampling a 20kHz signal to 14 bit and 16 bits for example, the following specs are required:

Spec	14 Bit	16 Bit	AD389KD	Units
Aperture Jitter (max)	2.4	0.6	0.4	ns
Slew Rate (max w/20V pk-pk signal)	1.26	1.26	30	V/μs
Feedthrough (1LSB max)	−84.3	−96.3	−86	dB
Droop Rate (1LSB max in 15μs)	40.7	10.2	0.1	μV/μs
Droop Rate (1LSB max in 50μs)	12.2	3.0	0.1	μV/μs
Acquisition Time (to ± 1LSB max) for 20kHz Signal w/15μs ADC	10	10	3-5	μs
Pedestal Shift (max) with Input Signal	−84.3	−96.3	−86	dB
Gain Temperature Coefficient (max) for ± 10°C Ambient Operation	6.1	1.5	2.0	ppm/°C
Thermal Tail (max) within 50μs after Hold	1.2	0.3	0.1	mV
Linearity Error (max)	±0.0061	0.0015	0.003	%FSR

Table II. T/H Amplifier Requirements vs. AD389 Specs

Aperture Jitter will affect exactly when the switch closes, even though the T/H control line is driven by a very precise clock. All high speed sampled data systems are very dependent on low aperture jitter for digitizing high frequency signals for spectrum analysis and accurate signal reconstruction.

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1LSB. The amplitude of 1LSB of the companion A/D converter for a given input range will vary from 610μV for a 14-bit A/D using a 0 to 10V input range to 4.88mV for a 12-bit A/D using a ±10V input range. The hold mode droop rate should produce less than 1LSB of droop in the output during the conversion time of the A/D converter. For 610μV/LSB, as noted in the example above, for a 50μs 14-bit A/D converter, the maximum droop rate will be 610μV/50μs or 12μV/μs during the 50μs conversion period.

The linearity error should be less than 1LSB over the transfer function, as set by the resolution of the A/D converter. The T/H acquisition time, T/H settling time along, with the conversion time of the A/D converter determines the highest sampling rate. This in turn will determine the highest input signal frequency that can be sampled at twice a cycle per the Nyquist criteria. The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible as with the feedthrough spec. The temperature coefficients for drift should be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more over temperature above +70°C (+158°F). For commercial and industrial users, these shifts will only appear above the highest temperatures their equipment will ever expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment.

Minimal thermal tail effects are another requirement of high resolution applications. The self-heating errors induced by the changing current levels in the output stages of T/H amps may cause more than 1LSB of error due to thermal tail effects. The performance of a typical AD389 in contrast to a typical 12-bit T/H circuit is shown in Figures 11a. and 11b. The test circuit is shown in Figure 8.

OFFSET ADJUST TRIM

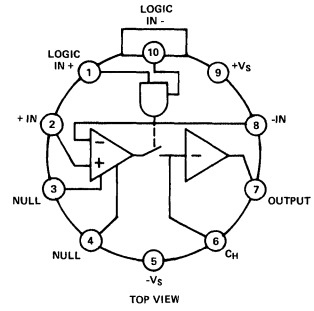
In most data acquisition systems only one offset adjustment is made. In many cases it is the offset adjust of the ADC that is used to cancel all other accumulated system offsets. The offset or pedestal of the AD389 can be nulled by means of 5kΩ potentiometer between pins 7, 9, and 11. If the offset of the AD389 is not adjusted, then connect pins 7 and 9 to pin 14, the negative supply. Otherwise the high impedance of the null pin together with parasitic capacitances can cause tail effects.

Low-Cost Sample-and-Hold Amplifier

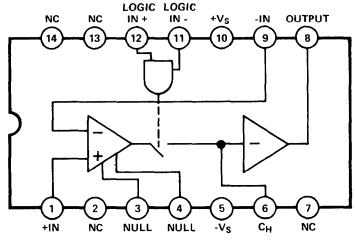
AD582

FEATURES
Suitable for 12-Bit Applications
High Sample/Hold Current Ratio: 10^7
Low Acquisition Time: 6μs to 0.1%
Low Charge Transfer: <2pC
High input Impedance in Sample-and-Hold Modes
Connect in Any Op Amp Configuration
Differential Logic Inputs

AD582 PIN CONFIGURATIONS



10-Pin TO-100



14-Pin DIP TO-116

PRODUCT DESCRIPTION

The AD582 is a low-cost integrated circuit sample-and-hold amplifier consisting of a high performance operational amplifier, a low leakage analog switch and a JFET integrating amplifier – all fabricated on a single monolithic chip. An external holding capacitor, connected to the device, completes the sample-and-hold function.

With the analog switch closed, the AD582 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its last level, regardless of input voltage.

Typical applications for the AD582 include sampled data systems, D/A deglitchers, analog de-multiplexers, auto null systems, strobed measurement systems and A/D speed enhancement.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the extended temperature range, -55°C to +125°C. All versions may be obtained in either the hermetic sealed, TO-100 can or the TO-116 DIP.

PRODUCT HIGHLIGHTS

1. The specially designed input stage presents a high impedance to the signal source in both sample and hold modes (up to ±12V). Even with signal levels up to $\pm V_S$, no undesirable signal inversion, peaking or loss of hold voltage occurs.
2. The AD582 may be connected in any standard op amp configuration to control gain or frequency response and provide signal inversion, etc.
3. The AD582 offers a high, sample-to-hold current ratio: 10^7. The ratio of the available charging current to the holding leakage current is often used as a figure of merit for a sample and hold circuit.
4. The AD582 has a typical charge transfer less than 2pC. A low charge transfer produces less offset error and permits the use of smaller hold capacitors for faster signal acquisition.
5. The AD582 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	*
Aperture Delay, 20V p-p Input, Hold 0V	200ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*
Droop Current, Steady State, ±10V_{OUT}	100pA max	*
Droop Current, T_{min} to T_{max}	1nA	150nA max
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	*
Common Mode Rejection V_{CM} = 20V p-p	60dB min (70dB typ)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 100pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 100pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 100pF	3V/μs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	*
Offset Voltage, T_{min} to T_{max}	4mV	8mV max (5mV typ)
Bias Current	3μA max (1.5μA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_{min} to T_{max}	100nA	400nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	±V_S	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage		
Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	*
-Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	±V_S	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	4.5mA max (3mA typ)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	*
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*
Lead Temperature (Soldering, 15 sec)	+300°C	*
PACKAGE OPTION[1]		
TO-100 (H-10A)	AD582KH	AD582SH
TO-116 (D-14)	AD582KD	AD582SD

NOTES
*Specifications same as AD582K.
[1]See Section 14 for package outline information.
Specifications subject to change without notice.

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

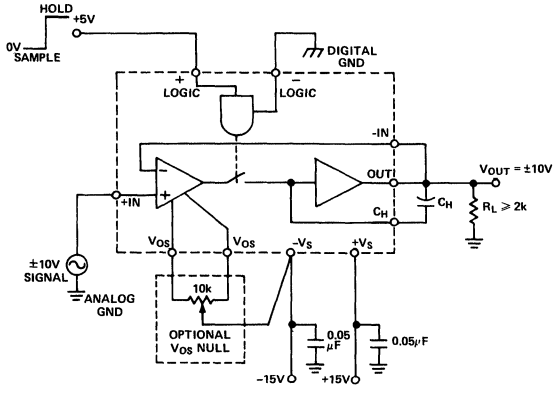


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

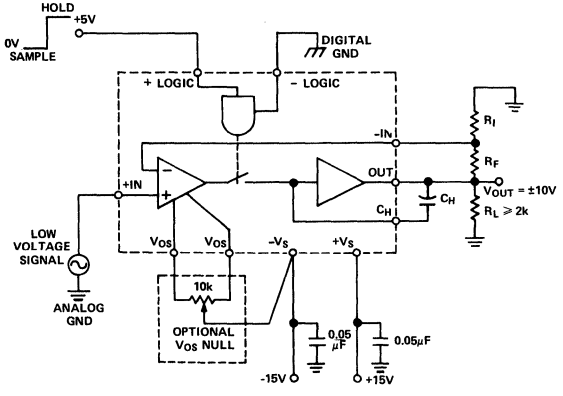


Figure 2. Sample and Hold with A = (1 + R_F/R_I)

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic Input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and ($+V_S$ - 3V). The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

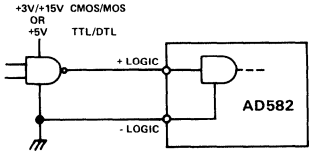


Figure 3A. Standard Logic Connection

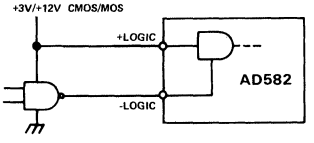


Figure 3B. Inverted Logic Sense Connection

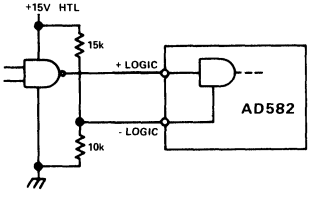


Figure 3C. High Threshold Logic Connection

DEFINITION OF TERMS

Figure 4 illustrates various dynamic characteristics of the AD582.

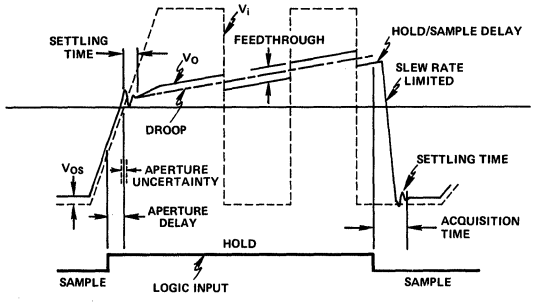


Figure 4. Pictorial Showing Various S/H Characteristics

Aperture Delay is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. The Aperture Time can be eliminated by advancing the sample-to-hold command 200ns with respect to the input signal. The Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\ (\text{Volts/sec}) = \frac{I(\text{pA})}{C_H(\text{pF})}$$

(See also Figure 6.)

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Sample-to-Hold Offset is an output shift or step caused by charge injection into the hold capacitor as the device is switched from sample to hold. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H\ (\text{pF})}$$

This offset also has a dc component as shown in Figure 6.

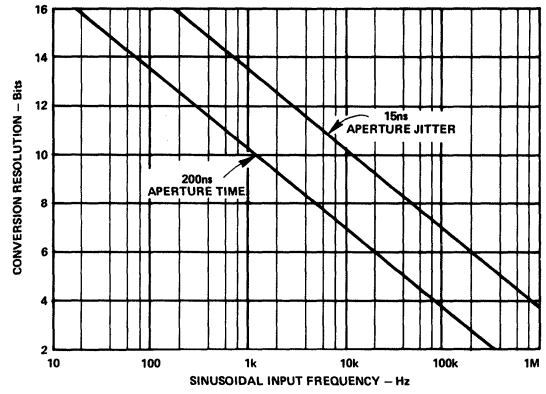


Figure 5. Maximum Frequency of Input Signal for ½LSB Sampling Accuracy

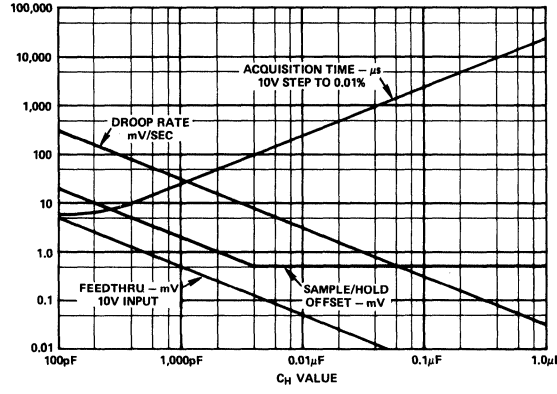


Figure 6. Sample-and-Hold Performance as a Function of Hold Capacitance

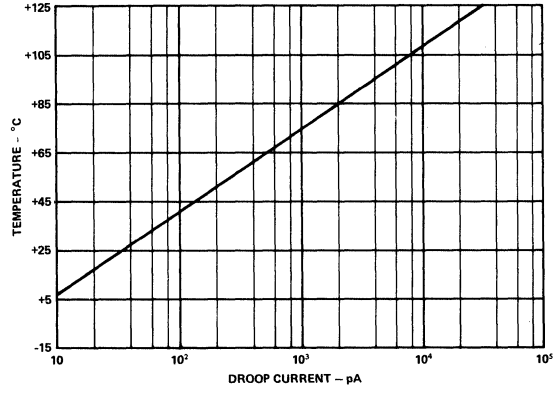


Figure 7. Droop Current vs. Temperature

ANALOG DEVICES

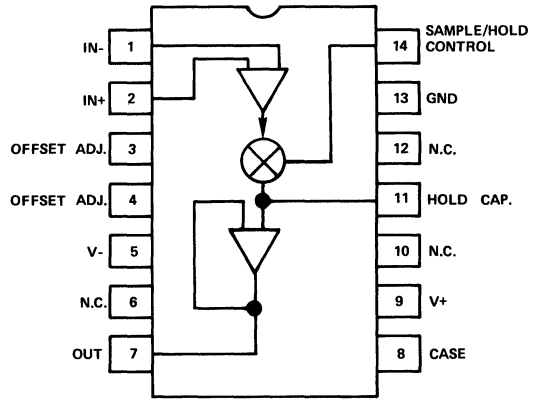
Sample-and-Hold Amplifier

AD583

FEATURES

High Sample-to-Hold Current Ratio: 10^6
High Slew Rate: 5V/μs
High Bandwidth: 2MHz
Low Aperture Time: 50ns
Low Charge Transfer: 10pC
DTL/TTL Compatible
May Be Used as Gated Op Amp

AD583 PIN CONFIGURATION



PRODUCTION DESCRIPTION

The AD583 is a monolithic sample-and hold circuit consisting of a high performance operational amplifier in series with a low leakage analog switch and unity gain amplifier. An external hold capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

PRODUCT HIGHLIGHTS

1. Sample-and-hold operation is obtained with the addition of one external capacitor.
2. Low charge transfer (10pC) and high sample-to-hold current ratio insure accurate tracking.
3. Any gain or frequency response is available using standard op amp feedback networks.
4. High slew rate and low aperture time permit sampling of rapidly changing signals.
5. Output, gated through a low leakage analog switch, also makes the AD583 useful for applications such as analog switches, peak holding circuits, etc.

6

SPECIFICATIONS (typical @ +25°C, hold capacitor of 1000pF and ±15V dc unless otherwise specified)

MODEL	AD583KD
OPEN LOOP GAIN R_L = 2kΩ, T_{min} to T_{max}	25k min (50k typ)
OUTPUT VOLTAGE SWING R_L = 2kΩ, T_{min} to T_{max}	±10V min
OUTPUT CURRENT	±10mA min
OUTPUT RESISTANCE	5Ω
OFFSET VOLTAGE T_{min} to T_{max}	6mV max (3mV typ) 8mV max (4mV typ)
BIAS CURRENT T_{min} to T_{max}	200nA max (50nA typ) 400nA max
OFFSET CURRENT T_{min} to T_{max}	50nA max (10nA typ) 100nA max
INPUT RESISTANCE	5MΩ min (10MΩ typ)
COMMON MODE RANGE	±10V min
COMMON MODE REJECTION T_{min} to T_{max}	74dB min (90dB typ)
GAIN BANDWIDTH PRODUCT	2MHz
SLEW RATE Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = ±10V p-p	5V/μs
RISE TIME Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	100ns
OVERSHOOT Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	20%
DIGITAL INPUT CURRENT V_{in} = 0, T_{min} to T_{max} V_{in} = +5.0V, T_{min} to T_{max}	 0.8mA max (Logic "Sample") 20μA max (Logic "Hold")
DIGITAL INPUT VOLTAGE Low T_{min} to T_{max} High T_{min} to T_{max}	 0.8V max 2.0V min
ACQUISITION TIME Av = +1, R_L = 2kΩ, C_L = 50pF to 0.1% of final value: to 0.01% of final value:	 4μs 5μs
APERTURE TIME	50ns
APERTURE JITTER	5ns
DRIFT CURRENT[1] T_{min} to T_{max}	50pA max (5pA typ) 1.0nA max (0.05nA typ)
CHARGE TRANSFER	20pC max (10pC typ)
SUPPLY CURRENT	5.0mA max (2.5mA typ)
POWER SUPPLY REJECTION[2]	74dB min (90dB typ)
OPERATING TEMP	0 to +70°C
STORAGE TEMP	-65°C to +150°C
PACKAGE OPTION[3] D-14	 AD583KD

NOTES
[1] Voltage on hold is zero.
[2] Sample mode only.
[3] See Section 14 for package outline information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- Terminals	40V
Differential Input Voltage	±30V
Digital Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Internal Power Dissipation	30mW (Derate power dissipation by 4.3mW/°C above +150°C ambient temperature)

ANALOG DEVICES

High Speed, Precision Sample-and-Hold Amplifier

AD585

FEATURES
3.0μs Acquisition Time to ±0.01% max
Low Droop Rate: 1.0mV/ms max
Sample/Hold Offset Step: 3mV max
Aperture Jitter: 0.5ns
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor
Internal Application Resistors
±12V or ±15V Operation
Available in Surface Mount

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements

PRODUCT DESCRIPTION

The AD585 is a complete monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultralow leakage analog switch and a FET input integrating amplifier. An internal holding capacitor and matched applications resistors have been provided for high precision and applications flexibility.

The performance of the AD585 makes it ideal for high speed 10- and 12-bit data acquisition systems, where fast acquisition time, low sample-to-hold offset, and low droop are critical. The AD585 can acquire a signal to ±0.01% in 3μs maximum, and then hold that signal with a maximum sample-to-hold offset of 3mV and less than 1mV/ms droop, using the on-chip hold capacitor. If lower droop is required, it is possible to add a larger external hold capacitor.

The high-speed analog switch used in the AD585 exhibits aperture jitter of 0.5ns, enabling the device to sample full-scale (20V peak-to-peak) signals at frequencies up to 78kHz with 12-bit precision.

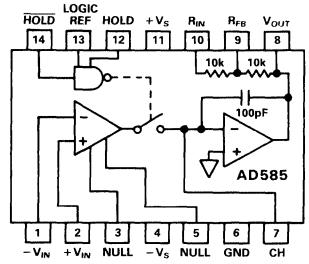
The AD585 can be used with any user-defined feedback network to provide any desired gain in the sample mode. On-chip precision thin-film resistors can be used to provide gains of +1, −1, or +2. Output impedance in the hold mode is sufficiently low to maintain an accurate output signal even when driving the dynamic load presented by a successive-approximation A/D converter. However, the output is protected against damage from accidental short circuits.

The control signal for the HOLD command can be either active high or active low. The differential HOLD signal is compatible with all logic families, if a suitable reference level is provided. An on-chip TTL reference level is provided for TTL compatibility.

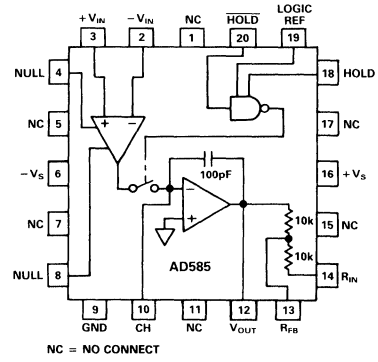
The AD585 is available in three performance grades. The JP grade is specified for the 0 to +70°C commercial temperature range and packaged in a 20-pin PLCC. The AQ grade is specified for the −25°C to +85°C industrial temperature range and is packaged in a 14-pin cerdip. The SQ and SE grades are specified for the −55°C to +125°C military temperature range and are packaged in a 14-pin cerdip and 20-pin LCC.

AD585 FUNCTIONAL BLOCK DIAGRAMS

DIP



LCC/PLCC PACKAGE



NC = NO CONNECT

PRODUCT HIGHLIGHTS

1. The fast acquisition time (3μs) and low aperture jitter (0.5ns) make it the first choice for very high speed data acquisition systems.
2. The droop rate is only 1.0mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
3. The low charge transfer of the analog switch keeps sample-to-hold offset below 3mV with the on-chip 100pF hold capacitor, eliminating the trade-off between acquisition time and S/H offset required with other SHAs.
4. The AD585 has internal pretrimmed application resistors for applications versatility.
5. The AD585 is complete with an internal hold capacitor for ease of use. Capacitance can be added externally to reduce the droop rate when long hold times and high accuracy are required.
6. The AD585 is recommended for use with 10- and 12-bit successive-approximation A/D converters such as AD573, AD574A, AD674A, AD7572 and AD7672.

SPECIFICATIONS (typical @ +25°C and V_S = ±12V or ±15V, and C_H = Internal, A = +1, $\overline{HOLD}$ active unless otherwise specified)

Model	AD585J Min	AD585J Typ	AD585J Max	AD585A Min	AD585A Typ	AD585A Max	AD585S Min	AD585S Typ	AD585S Max	Units
SAMPLE/HOLD CHARACTERISTICS										
Acquisition Time, 10V Step to 0.01%			3			3			3	µs
20V Step to 0.01%			5			5			5	µs
Aperture Time, 20V p-p Input, $\overline{HOLD}$ 0V		35			35			35		ns
Aperture Jitter, 20V p-p Input, $\overline{HOLD}$ 0V		0.5			0.5			0.5		ns
Settling Time, 20V p-p Input, $\overline{HOLD}$ 0V, to 0.01%		0.5			0.5			0.5		µs
Droop Rate			1			1			1	mV/ms
Droop Rate T_{min} to T_{max}		Doubles Every 10°C			Doubles Every 10°C			Doubles Every 10°C		
Charge Transfer			0.3			0.3			0.3	pC
Sample-to-Hold Offset	−3		3	−3		3	−3		3	mV
Feedthrough 20V p-p, 10kHz Input		0.5			0.5			0.5		mV
TRANSFER CHARACTERISTICS[1]										
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k		200,000			200,000			200,000		V/V
Application Resistor Mismatch			0.3			0.3			0.3	%
Common Mode Rejection V_{CM} = ±10V	80			80			80			dB
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p		2.0			2.0			2.0		MHz
Full Power Bandwidth V_{OUT} = 20V p-p		160			160			160		kHz
Slew Rate V_{OUT} = 20V p-p		10			10			10		V/µs
Output Resistance (Sample Mode) I_{OUT} = ±10mA			0.05			0.05			0.05	Ω
Output Short Circuit Current		50			50			50		mA
Output Short Circuit Duration		Indefinite			Indefinite			Indefinite		
ANALOG INPUT CHARACTERISTICS										
Offset Voltage			5			2			2	mV
Offset Voltage, T_{min} to T_{max}			6			3			3	mV
Bias Current			2			2			2	nA
Bias Current T_{min} to T_{max}			5			5		20	50[2]	nA
Input Capacitance, f = 1MHz		10			10			10		pF
Input Resistance, Sample or Hold 20V p-p Input, A = +1		10^{12}			10^{12}			10^{12}		Ω
DIGITAL INPUT CHARACTERISTICS										
TTL Reference Output	1.2	1.4	1.6	1.2	1.4	1.6	1.2	1.4	1.6	V
Logic Input High Voltage T_{min} to T_{max}	2.0			2.0			2.0			V
Logic Input Low Voltage T_{min} to T_{max}			0.8			0.8			0.7	V
Logic Input Current (Either Input)			50			50			50	µA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	+5, −10.8		±18	+5, −10.8		±18	+5, −10.8		±18	V
Supply Current, R_L = ∞	6		10	6		10	6		10	mA
Power Supply Rejection, Sample Mode	70			70			70			dB
TEMPERATURE RANGE Specified Performance	0		+70	−25		+85	−55		+125	°C
PACKAGE OPTIONS[3]										
Cerdip (Q-14)					AD585AQ			AD585SQ		
LCC (E-20A)								AD585SE		
PLCC (P-20A)		AD585JP								

NOTES

[1]Maximum input signal is the minimum supply minus a headroom voltage of 2.5V.

[2]Not tested at −55°C.

[3]See Section 14 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supplies ($+V_S$, $-V_S$)	±18V
Logic Inputs	$\pm V_S$
Analog Inputs	$\pm V_S$
R_{IN}, R_{FB} Pins	$\pm V_S$
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering)	300°C
Output Short Circuit to Ground	Indefinite
TTL Logic Reference Short Circuit to Ground	Indefinite

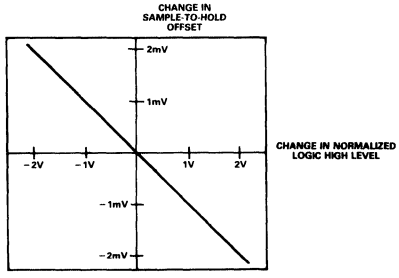


Figure 1. Sample-to-Hold Offset vs. Logic Level (HOLD Active)

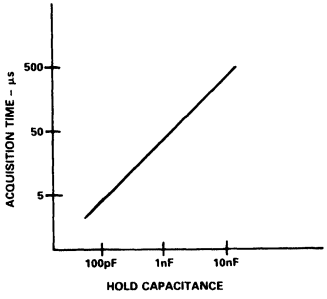


Figure 2. Acquisition Time vs. Hold Capacitance (10V Step to 0.01%)

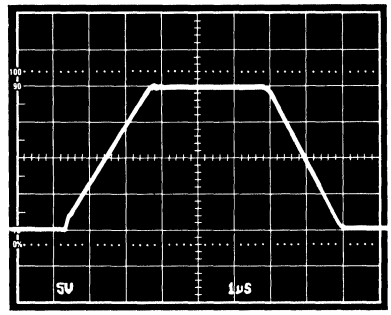


Figure 3. Large Signal Response, Sample Mode

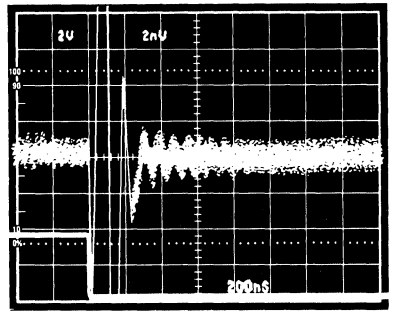


Figure 4. Sample-to-Hold Settling Time (HOLD Active)

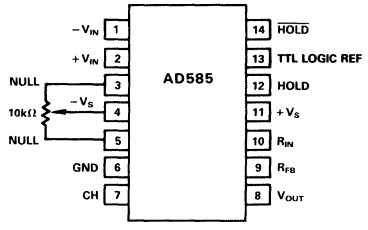


Figure 5. DIP Pin Configuration

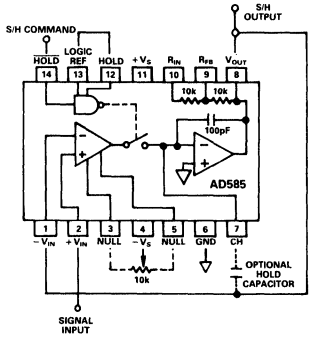


Figure 6. Connection Diagram, Gain = +1, HOLD Active

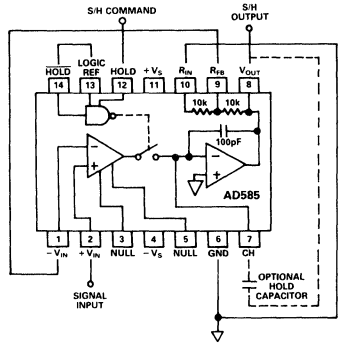


Figure 7. Connection Diagram, Gain = +2, HOLD Active

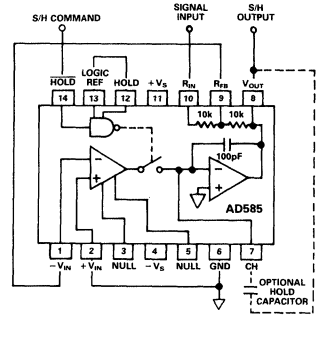


Figure 8. Connection Diagram, Gain = −1, HOLD Active

SAMPLED DATA SYSTEMS

In sampled data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 9 shows pictorially the sample-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Sample-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Sample Transition.

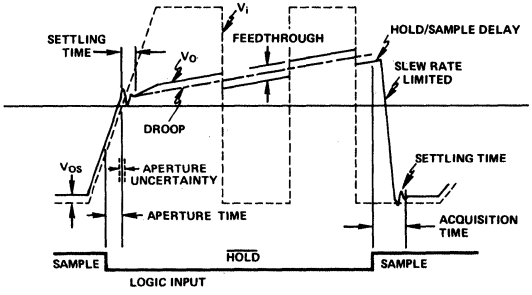


Figure 9. Pictorial Showing Various S/H Characterstics

SAMPLE-TO-HOLD TRANSITION

The aperture delay time is the time required for the sample-and-hold amplifier to switch from sample to hold. Since this is effectively a constant then it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 10 will result.

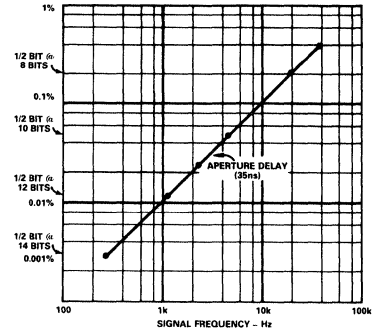


Figure 10. Aperture Delay Error vs. Frequency

To eliminate the aperture delay as an error source the sample-to-hold command may be advanced with respect to the input signal.

Once the aperture delay time has been eliminated as an error source then the aperture jitter which is the variation in aperture delay time from sample-to-sample remains. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dT of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the N-bit A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi \text{ (Aperture Jitter)}}$$

For an application with a 10-bit A/D converter with a 10V full scale to a 1/2LSB error maximum.

$$F_{max} = \frac{2^{-(10+1)}}{\pi\ (0.5 \times 10^{-9})}$$

$$F_{max} = 310.8\text{kHz}.$$

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\ (0.5 \times 10^{-9})}$$

$$F_{max} = 77.7\text{kHz}.$$

Figure 11 shows the entire range of errors induced by aperture jitter with respect to the input signal frequency.

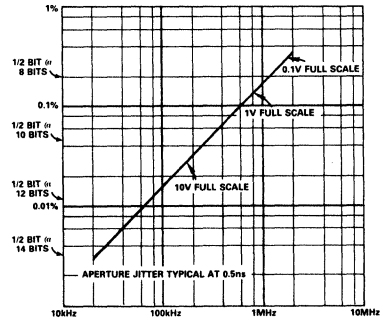


Figure 11. Aperture Jitter Error vs. Frequency

Sample-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting sample-to-hold offset is a function of the logic level.

The logic inputs were designed for application flexibility and, therefore, a wide range of logic thresholds. This was achieved by using a differential input stage for HOLD and $\overline{\text{HOLD}}$. Figure 1 shows the change in the sample-to-hold offset voltage based upon an independently programmed reference voltage. Since the input stage is a differential configuration, the offset voltage is a function of the control voltage range around the programmed threshold voltage.

The sample-to-hold offset can be reduced by adding capacitance to the internal 100pF capacitor and by using $\overline{\text{HOLD}}$ instead of HOLD. This may be easily accomplished by adding an external capacitor between Pins 7 and 8. The sample-to-hold offset is then governed by the relationship:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H \text{ Total (pF)}}$$

For the AD585 in particular it becomes:

$$\text{S/H Offset (V)} = \frac{0.3 \text{ pC}}{100\text{pF} + (C_{EXT})}$$

The addition of an external hold capacitor also affects the acquisition time of the AD585. The change in acquisition time with respect to the C_{EXT} is shown graphically in Figure 2.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a sample and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dT is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dT}\ (\text{Volts/Sec}) = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD585 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF} + (C_{EXT})}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion. The hold-mode droop rate can be traded-off with acquisition time to provide the best combination of droop error and acquisition time. The tradeoff is easily accomplished by varying the value of C_{EXT}.

Since a sample and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (T_{CONV}) is required to calculate the maximum allowable dV/dT.

$$\frac{dV \text{ max}}{dt} = \frac{\Delta V \text{ max}}{T_{CONV}}$$

The maximum $\frac{dV \text{ max}}{dT}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) $= \Delta T$.

$$\frac{dV\ 25°C}{dT} \times 2^{\frac{(\Delta T°C)}{10°C}} \leq \frac{dV \text{ max}}{dT}$$

HOLD-TO-SAMPLE TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD585 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD585 can be used with a number of different A/D converters to achieve high throughput rates. Figures 12 and 13 show the use of an AD585 with the AD578 and AD574A.

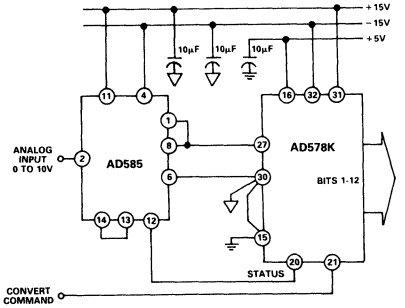


Figure 12. A/D Conversion System, 117.6kHz Throughput 58.8kHz max Signal Input

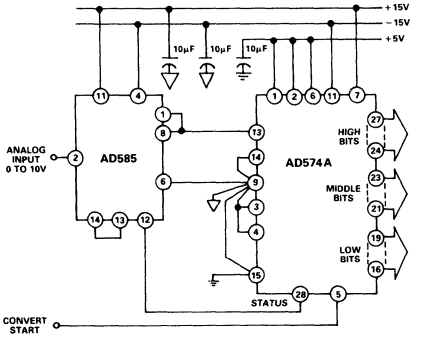


Figure 13. 12 Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz max Signal Input

LOGIC INPUT

The sample-and-hold logic control was designed for versatile logic interfacing. The HOLD and $\overline{\text{HOLD}}$ inputs may be used with both low and high level CMOS, TTL and ECL logic systems. Logic threshold programmability was achieved by using a differential amplifier as the input stage for the digital inputs. A predictable logic threshold may be programmed by referencing either HOLD or $\overline{\text{HOLD}}$ to the appropriate threshold voltage. For example, if the internal 1.4V reference is applied to $\overline{\text{HOLD}}$ an input signal to HOLD between $+1.8$V and $+V_S$ will place the AD585 in the hold mode. The AD585 will go into the sample mode for this case when the input is between $-V_S$ and $+1.0$V. The range of references which may be applied is from $(-V_S + 4V)$ to $(+V_S - 3V)$.

OPTIONAL CAPACITOR SELECTION

If an additional capacitor is going to be used in conjunction with the internal 100pF capacitor it must have a low dielectric absorption. Dielectric absorption is just that; it is the charge absorbed into the dielectric that is not immediately added to or removed from the capacitor when rapidly charged or discharged. The capacitor with dielectric absorption is modeled in Figure 14.

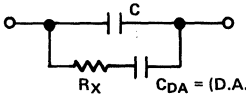


Figure 14. Capacitor Model with Dielectric Absorption

If the capacitor is charged slowly, C_{DA} will eventually charge to the same value as C. But unfortunately, good dielectrics have very high resistances, so while C_{DA} may be small, R_X is large and the time constant $R_X C_{DA}$ typically runs into the millisecond range. In fast-charge, fast-discharge situations the effect of dielectric absorption resembles "memory". In a data acquisition system where many channels with widely varying data are being sampled the effect is to have an ever changing offset which appears as a very nonlinear sample-to-hold offset since the difference between the voltage being measured and the voltage previously measured determines the fraction by which the dielectric absorption figure is multiplied. It is impossible to readily correct for this error source. The only solution is to use a capacitor with dielectric absorption less than the maximum tolerable error. Capacitor types such as polystyrene, polypropylene or Teflon are recommended.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD585. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

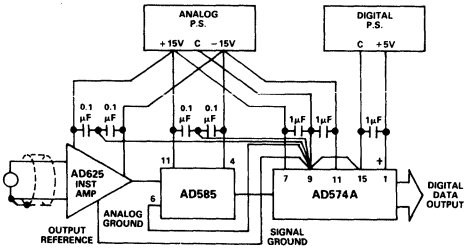


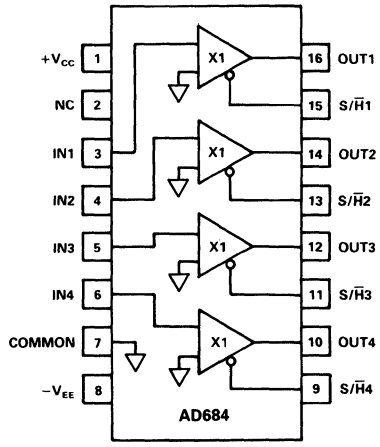
Figure 15. Basic Grounding Practice

Four-Channel Sample-and-Hold Amplifier

AD684

FEATURES
Four Matched Sample-and-Hold Amplifiers
Independent Inputs, Outputs and Control Pins
500ns Hold Mode Settling
1μs Maximum Acquisition Time to 0.01%
Low Droop Rate: 0.01μV/μs
Internal Hold Capacitors
200ps Maximum Aperture Jitter
Low Power Dissipation: 360 mW
0.3" Skinny DIP Package

AD684 FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD684 is a monolithic quad sample-and-hold amplifier (SHA). It features four complete sampling channels, each controlled by an independent hold command. Each SHA is complete with an internal hold capacitor. The high accuracy SHA channels are self-contained and require no external components or adjustments. The AD684 is manufactured on a BiMOS process which provides a merger of high performance bipolar circuitry and low power CMOS logic.

The AD684 is ideal for high performance, multichannel data acquisition systems. Each SHA channel can acquire a signal in less than 1μs and retain the held value with a droop rate of less than 0.01μV/μs. Excellent linearity and ac performance make the AD684 an ideal front end for high speed 12- and 14-bit ADCs.

The AD684 has a self-correcting architecture that minimizes hold mode errors and insures accuracy over temperature. Each channel of the AD684 is capable of sourcing 5mA and incorporates output short circuit protection.

The AD684 is specified for three temperature ranges. The J grade device is specified for operation from 0 to 70°C, the A grade from −40°C to +85°C and the S grade from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Fast acquisition time (1μs) and low aperture jitter (200ps) make the AD684 the best choice for multiple channel data acquisition systems.
2. Monolithic construction insures excellent interchannel matching in terms of timing and accuracy, as well as high reliability.
3. Independent inputs, outputs and sample-and-hold controls allow user flexibility in system architecture.
4. Low droop (0.01μV/μs) and internally compensated hold mode error results in superior system accuracy.
5. The AD684's fast settling time and low output impedance make it ideal for driving high speed analog to digital converters such as the AD578, AD674, AD7572 and the AD7672.

SPECIFICATIONS (typical @ +25°C, V_{CC} = +12V, V_{EE} = −12V, unless otherwise specified)

Parameter	AD684J Min	AD684J Typ	AD684J Max	AD684A Min	AD684A Typ	AD684A Max	AD684S Min	AD684S Typ	AD684S Max	Units
SAMPLING CHARACTERISTICS										
Acquisition Time (T_{min} to T_{max})										
10V Step to 0.01%		0.75	1.0		0.75	1.0		0.75	1.0	µs
10V Step to 0.1%		0.5	0.6		0.5	0.6		0.5	0.6	µs
Small Signal Bandwidth		4			4			4		MHz
Full Power Bandwidth		1			1			1		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay	−30	−20	−10	−30	−20	−10	−30	−20	−10	ns
Aperture Jitter		100	200		100	200		100	200	ps
Hold Settling Time (to 1mV)		250	500		250	500		250	500	ns
Droop Rate (T_{min} to T_{max})[1]		0.01	**1**		0.01	5		0.01	7	µV/µs
Feedthrough										
(V_{IN} = ±5V, 100kHz)		−90			−90			−90		dB
ACCURACY CHARACTERISTICS (T_{min} to T_{max})[1]										
Hold Mode Offset	−7	−4	+3	−7	−4	+3	−7	−4	+3	mV
Hold Mode Offset Drift		10			10			10		µV/°C
Track Mode Offset		50	**200**		50	**200**		50	**200**	mV
Nonlinearity		±0.002	±0.003		±0.002	±0.003		±0.003	±0.005	% FS
Gain Error		±0.03	**±0.05**		±0.03	**±0.05**		±0.03	**±0.05**	% FS
INTERCHANNEL CHARACTERISTICS										
Interchannel Isolation										
(V_{IN} = ±5V, 100kHz)	80	86		80	86		80	86		dB
Interchannel Aperture Offset		150	300		150	300		150	300	ps
Interchannel Offset		0.1	**1.2**		0.1	**1.2**		0.1	**1.2**	mV
OUTPUT CHARACTERISTICS										
Output Drive Current[2]										
(T_{min} to T_{max})	−5		+5	−5		+5	−5		+5	mA
Output Resistance, dc		0.3	0.5		0.3	0.5		0.3	0.5	Ω
Total Output Noise										
(dc to 5MHz)		150			150			150		µV rms
Sampled dc Uncertainty		85			85			85		µV rms
Hold Mode Noise										
(dc to 5MHz)		125			125			125		µV rms
Short Circuit Current[3]										
Source		20			20			20		mA
Sink		10			10			10		mA
INPUT CHARACTERISTICS (T_{min} to T_{max})										
Input Voltage Range	−5		+5	−5		+5	−5		+5	V
Bias Current		100	**200**		100	**200**		100	**200**	nA
Input Impedance		50			50			50		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS (T_{min} to T_{max})										
Input Voltage Low			**0.8**			**0.8**			**0.8**	V
Input Voltage High	**2.0**			**2.0**			**2.0**			V
Input Current (V_{IN} = 5V)		2	**20**		2	**20**		2	**20**	µA
POWER SUPPLY CHARACTERISTICS										
(T_{min} to T_{max})										
Operating Voltage Range (V_{CC}, V_{EE})	±10.8	±12	±13.2	±10.8	±12	±13.2	±10.8	±12	±13.2	V
Supply Current		15	**22**		15	**22**		15	**24**	mA
+ PSRR (+12V, ±10%)	**65**	70		**65**	70		**65**	70		dB
−PSRR (−12V, ±10%)	**60**	65		**60**	65		**60**	65		dB
Power Consumption		360	530		360	530		360	580	mW
TEMPERATURE RANGE										
Specified Performance	0		+70	−40		+85	−55		+125	°C

NOTE

[1]Specified and tested over an input range of ±5V.

[2]Maximum current the AD684 can source (or sink). Testing guarantees that the accuracy of the held signal remains within 2.5mV of its initial value.

[3]The output is protected for a short circuit to common, $+V_{CC}$ and $-V_{EE}$.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

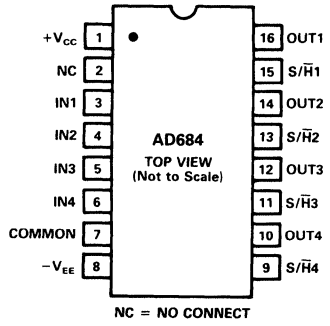
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Unit
V_{CC}	Common	−0.3	+15	V
V_{EE}	Common	−15	+0.3	V
Control Inputs	Common	−0.5	+7	V
Analog Inputs	Common	−12	+12	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Max Junction Temperature			+175	°C
Storage		−65	+150	°C
Lead Temperature (10sec max)			+300	°C
Power Dissipation			640	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

PIN CONFIGURATION



CAUTION

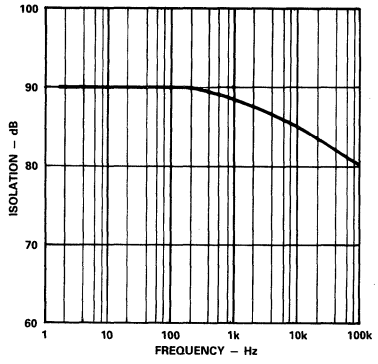
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

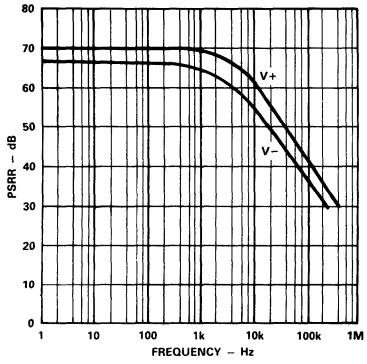
Model	Temperature Range	Package Options*
AD684JQ	0 to +70°C	Q-16
AD684AQ	−40°C to +85°C	Q-16
AD684SQ	−55°C to +125°C	Q-16

*See Section 14 for package outline information.

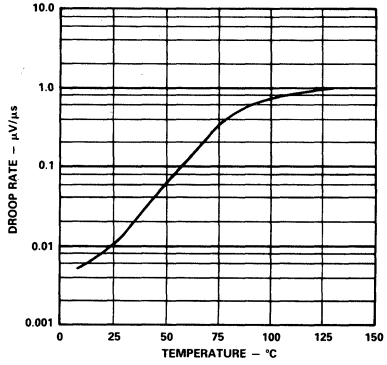
Typical Characteristics



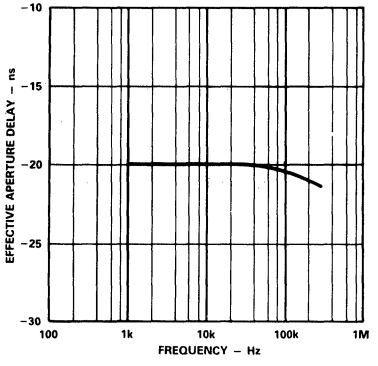
Interchannel Isolation vs. Frequency



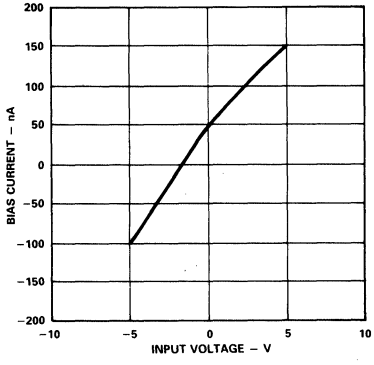
Power Supply Rejection Ratio vs. Frequency



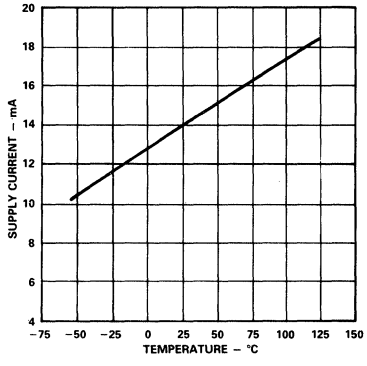
Droop Rate vs. Temperature, V_{IN} = 0V



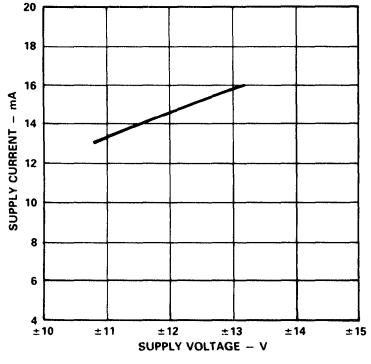
Effective Aperture Delay vs. Frequency



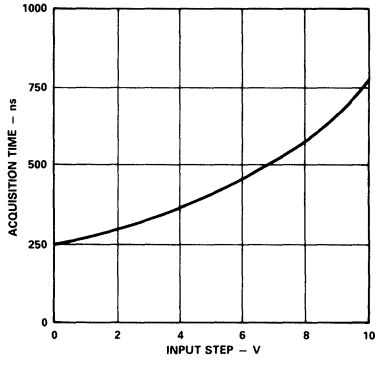
Bias Current vs. Input Voltage



Supply Current vs. Temperature



Supply Current vs. Supply Voltage



Acquisition Time (to 0.01%) vs. Input Step Size

DEFINITIONS OF SPECIFICATIONS

Acquisition Time — The length of time that the SHA must remain in the sample mode in order to acquire a full scale input step to a given level of accuracy.

Small Signal Bandwidth — The frequency at which the held output amplitude is 3dB below the input amplitude, under an input condition of a 100mV p-p sine wave.

Full Power Bandwidth — The frequency at which the held output amplitude is 3dB below the input amplitude, under an input condition of a 10V p-p sine wave.

Effective Aperture Delay — The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

Aperture Jitter — The variations in aperture delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

Hold Settling Time — The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

Droop Rate — The drift in output voltage while in the hold mode.

Feedthrough — The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

Hold Mode Offset — The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. It is specified for an input of 0V.

Tracking Mode Offset — The difference between the input and output signals when the SHA is in the track mode.

Nonlinearity — The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between endpoints, over an input range of −5V and +5V.

Gain Error — Deviation from a gain of +1 on the transfer function of input vs. held output.

Interchannel Isolation — The level of crosstalk between adjacent channels while in the sample (track) mode with a full scale 100kHz input signal.

Interchannel Aperture Offset — The variation in aperture time between the four channels for a simultaneous hold command.

Differential Offset — The difference in hold mode offset between the four SHA channels.

Power Supply Rejection Ratio — A measure of change in the held output voltage for a specified change in the positive or negative supply.

Sampled dc Uncertainty — The internal rms SHA noise that is sampled onto the hold capacitor.

Hold Mode Noise — The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

Total Output Noise — The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

Output Drive Current — The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5mV.

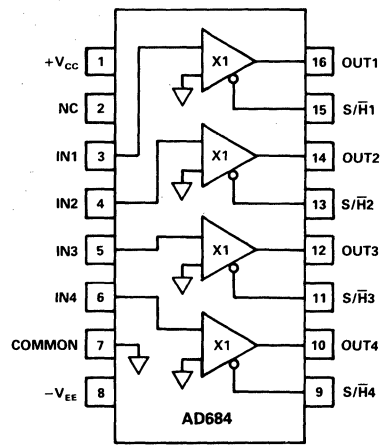
6

FUNCTIONAL DESCRIPTION

The AD684 is a complete quad sample-and hold amplifier that provides high speed sampling to 12-bit accuracy in less than 1μs.

The AD684 is completely self-contained, including on-chip hold capacitors, and requires no external components or adjustments to perform the sampling function. Each SHA channel can operate independently, having its own input, output and sample/hold command. Both inputs and outputs are treated as single ended signals, referred to common.

The AD684 utilizes a proprietary circuit design which includes a self-correcting architecture. This sample-and-hold circuit corrects for internal errors after the hold command has been given, by compensating for amplifier gain and offset errors, and charge injection errors. Due to the nature of the design, the SHA output in the sample mode is not intended to provide an accurate representation of the input. However, in hold mode, the internal circuitry is reconfigured to produce an accurately held version of the input signal. To the right is a block diagram of the AD684.



Functional Block Diagram

DYNAMIC PERFORMANCE

The AD684 is compatible with 12-bit A-to-D converters in terms of both accuracy and speed. The fast acquisition time, fast hold settling time and good output drive capability allow the AD684 to be used with high speed, high resolution A-to-D converters like the AD674 and AD7672. The AD684's fast acquisition time provides high throughput rates for multichannel data acquisition systems. Typically, the sample and hold can acquire a 10V step in less than 750ns. Figure 1 shows the settling accuracy as a function of acquisition time.

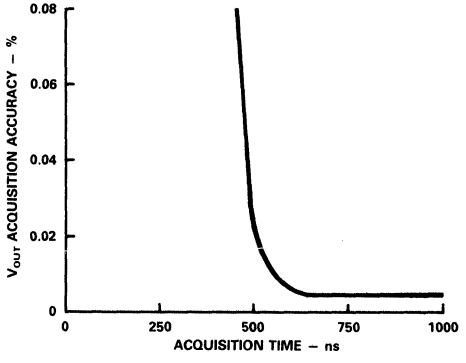


Figure 1. V_{OUT} Settling vs. Acquisition Time

The hold settling determines the required time, after the hold command is given, for the output to settle to its final specified accuracy. The typical settling behavior of the AD684 is shown in Figure 2. The settling time of the AD684 is sufficiently fast to allow the SHA, in most cases, to directly drive an A-to-D converter without the need for an added "start convert" delay.

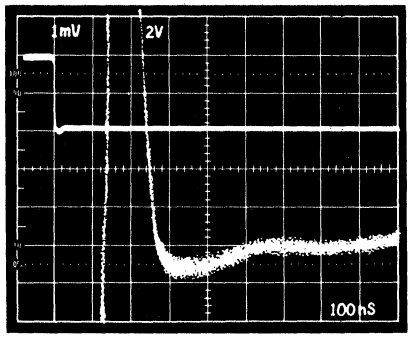


Figure 2. Typical AD684 Hold Mode

HOLD MODE OFFSET

The dc accuracy of the AD684 is determined primarily by the hold mode offset. The hold mode offset refers to the difference between the final held output voltage and the input signal at the time the hold command is given. The hold mode offset arises from a voltage error introduced onto the hold capacitor by charge injection of the internal switches. The nominal hold mode offset is specified for a 0V input condition. Over the input range of −5V to +5V, the AD684 is also characterized for an effective gain error and nonlinearity of the held value, as shown in Figure 3. As indicated by the AD684 specifications, the hold mode offset is very well matched between channels and stable over temperature.

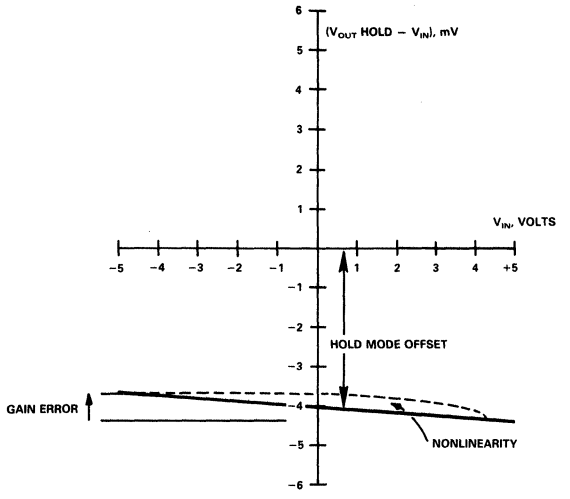


Figure 3. Hold Mode Offset, Gain Error and Nonlinearity

For applications where it is important to obtain zero offset, the hold mode offset may be nulled externally at the input to the A-to-D converter. Adjustment of the offset may be accomplished through the A-to-D itself or by an external amplifier with offset nulling capability (e.g., AD711). Only a single adjustment of the offset is necessary for the four SHA channels as a result of the excellent matching among them. The offset will change less than 0.5mV over the specified temperature range.

SUPPLY DECOUPLING AND GROUNDING CONSIDERATIONS

As with any high speed, high resolution data acquisition system, the power supplies should be well regulated and free from excessive high frequency noise (ripple). The supply connection to the AD684 should also be capable of delivering transient currents to the device. To achieve the specified accuracy and dynamic performance, decoupling capacitors must be placed directly at both the positive and negative supply pins to common. Ceramic type 0.1μF capacitors should be connected from V_{CC} and V_{EE} to common.

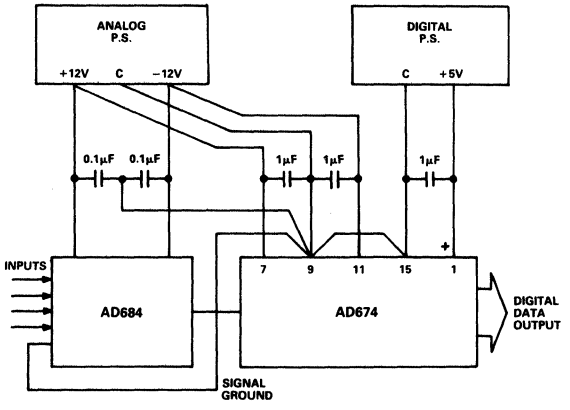


Figure 4. Basic Grounding and Decoupling Diagram

The AD684 does not provide separate analog and digital ground leads as is the case with most A-to-D converters. The common pin is the single ground terminal for the device. It is the reference point for the sampled input voltage and the held output voltage and also the digital ground return path. The common pin should be connected to the reference (analog) ground of the A-to-D converter with a separate ground lead. Since the analog and digital grounds in the 684 are connected internally, the common pin should also be connected to the digital ground, which is usually tied to analog common at the A-to-D converter. Figure 4 illustrates the recommended decoupling and grounding practice.

NOISE CHARACTERISTICS

Designers of data conversion circuits must also consider the effect of noise sources on the accuracy for the data acquisition system. A sample-and-hold amplifier that precedes the A-to-D converter introduces some noise and represents another source of uncertainty in the conversion process. The noise from the AD684 is specified as the total output noise, which includes both the sampled wideband noise of the SHA in addition to the band limited output noise. The total output noise is the rms sum of the sampled dc uncertainty and the hold mode noise. A plot of the total output noise vs. the equivalent input bandwidth of the converter being used is given in Figure 5.

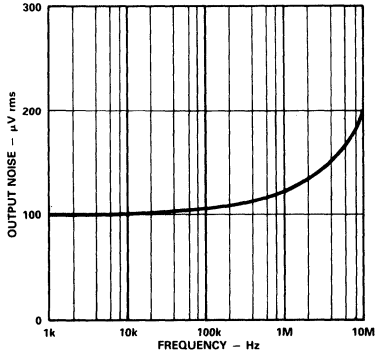


Figure 5. RMS Noise vs. Input Bandwidth of ADC

DRIVING THE ANALOG INPUTS

For best performance, it is important to drive the AD684 analog inputs from a low impedance signal source. This enhances the sampling accuracy by minimizing the analog and digital crosstalk. Signals which come from higher impedance sources (e.g., over 5k ohms) will have a relatively higher level of crosstalk. For applications where signals have high source impedance, an operational amplifier buffer in front of the AD684 is required. The AD713 (precision quad BiFET op amp) is recommended for these applications.

HIGH FREQUENCY SAMPLING

Aperture jitter and distortion are the primary factors which limit frequency domain performance of a sample-and-hold amplifier. Aperture jitter modulates the phase of the hold command and produces an effective noise on the sampled analog input. The magnitude of the jitter induced noise is directly related to the frequency of the input signal.

A graph showing the magnitude of the jitter induced error vs. frequency of the input signal is given in Figure 6.

The accuracy in sampling high frequency signals is also constrained by the distortion and noise created by the sample-and-hold. The level of distortion increases with frequency and reduces the "effective number of bits" of the conversion.

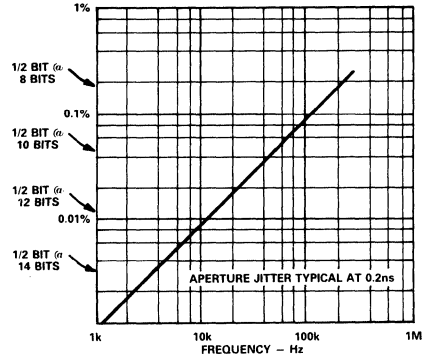


Figure 6. Error Magnitude vs. Frequency

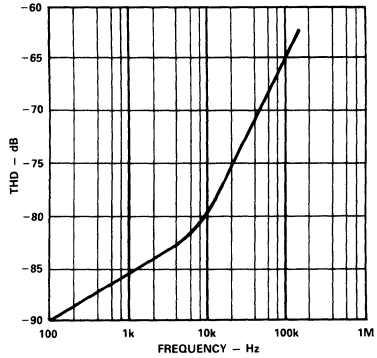


Figure 7. Total Harmonic Distortion vs. Frequency

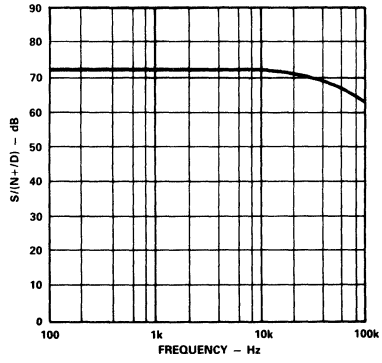


Figure 8. Signal/(Noise and Distortion) vs. Frequency

Measurements of Figures 7 and 8 were made using a 14-bit A-to-D converter with V_{IN} = 10V p-p and a sample frequency of 100KSPS.

DATA ACQUISITION APPLICATIONS

Figure 9 shows a typical data acquisition circuit using the AD684 and the high speed 12-bit A-to-D converter, the AD7672. Four input signals are simultaneously sampled by the AD684 as the $\overline{\text{HOLD}}$ command is given. One of the four held outputs is selected by the ADG201, quad CMOS switch, and buffered by the AD711. The AD588 provides the reference voltage with switches A–B and C–D selecting a −5V to +5V or 0 to +5V input range.

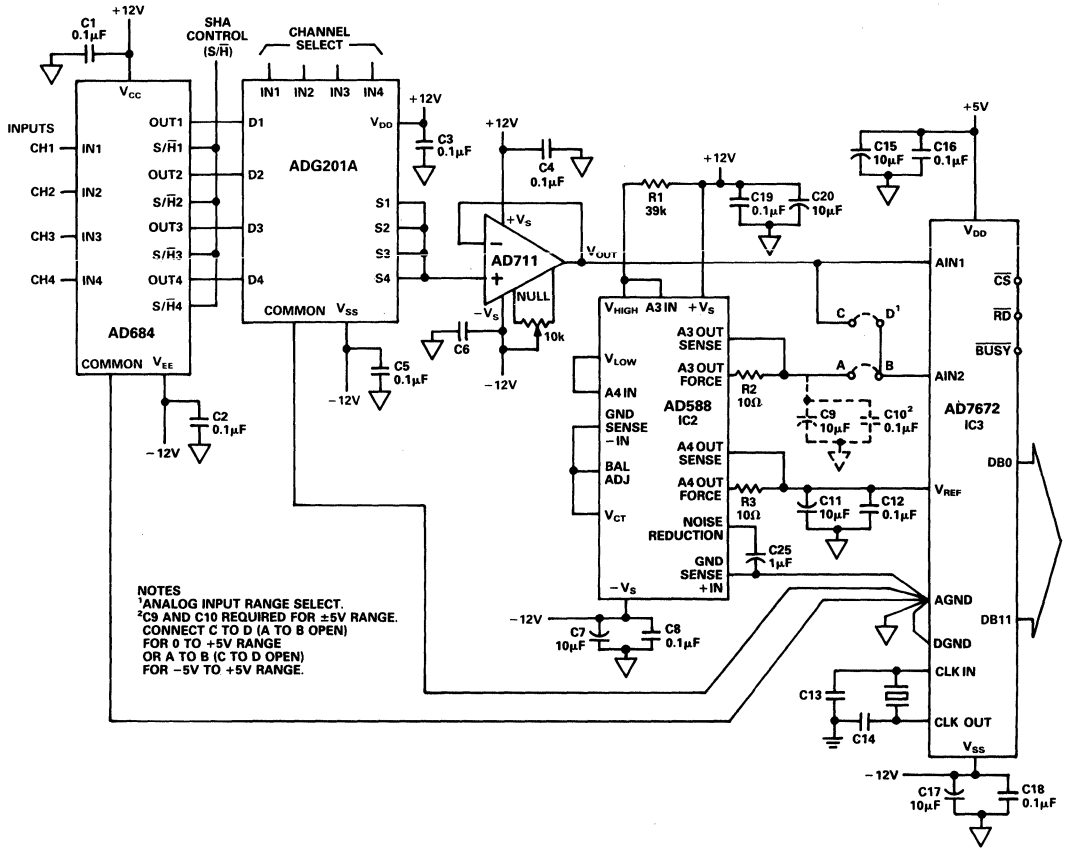


Figure 9. Data Acquisition System Using the AD684 and the AD7672

ANALOG DEVICES

Low Cost 16-Bit Accurate Sample-and-Hold Amplifier

AD1154

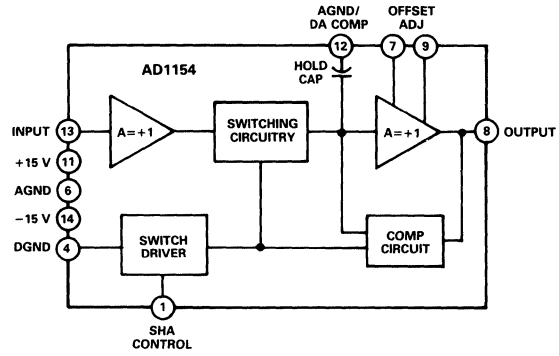
FEATURES

Low Nonlinearity: ±7.6 ppm max (1/2 LSB @ 16-Bit Accuracy)
Fast Acquisition Time to ±0.00076%: 3.5 μs
Low Droop Rate: 0.02 μV/μs
Aperture Jitter: 150 ps
±10 V Input Range
Hold Mode Feedthrough Rejection of −106 dB
14-Pin Metal DIP
Gain of +1 V/V
Low Cost

APPLICATIONS

Medical and Analytical Instrumentation
Automatic Test Equipment
Data Acquisition for Signal Processing
Simultaneous Sample-and-Hold
Peak Measurement Detection
Event Analysis

AD1154 FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The AD1154 is a high accuracy, low cost sample-and-hold amplifier (SHA) designed to be used in high resolution data acquisition systems. It is complete with internal hold capacitor and proprietary capacitor trimmed compensation circuitry. Its accuracy (0.00076% of full scale range) and dynamic performance allow it to be used with high speed 16-bit A/D converters. The AD1154's low price enables users to upgrade the front end performance of 14-bit systems without increasing system cost. Its gain accuracy and droop rate in "hold" mode also allow accurate conversion by slower 16-bit A/D converters having conversion times of up to 7.6 ms.

The AD1154 is a hybrid noninverting sample-and-hold amplifier (SHA) with a gain of +1 V/V. It can be utilized in most inverting SHA applications by inverting the digital data. The AD1154 is packaged in a compact 14-pin metal DIP.

Typical applications for the AD1154 include data acquisition systems, strobed measurement systems, peak hold circuits and simultaneous sample-and-hold functions. The AD1154 is available in two grades, both operating over the −25°C to +85°C temperature range. The "A" grade is specified for 15-bit accurate systems, while the "B" grade offers superior performance for true 16-bit applications.

PRODUCT HIGHLIGHTS

1. Fast acquisition and low jitter make it the right choice for high speed, high accuracy data acquisition.
2. Its low droop rate (0.02 μV/μs) allows it to be used in slower systems without noticeable performance degradation.
3. The AD1154 is ideal for systems requiring wide dynamic range.
4. Low price reduces overall system cost.
5. Unity gain buffer architecture allows ease of use.

SPECIFICATIONS (typical @ 25°C and nominal power supply of ±15V unless otherwise noted)

Model	AD1154AW	AD1154BW	Units
ANALOG INPUT			
Voltage Range	±10 min	*	V
Overvoltage (No Damage)	$\pm V_S$	*	V
Input Impedance	10^{12}	*	Ω
Input Capacitance	10	*	pF
DIGITAL INPUT (TTL COMPATIBLE)			
Sample Mode Logic "1"	2.0 min	*	V
Hold Mode Logic "0"	0.8 max	*	V
Logic "1" Current	1	*	μA
Logic "0" Current	3	*	μA
ANALOG OUTPUT			
Voltage ($R_{LOAD} \geq 2$ kΩ)	±10 min	*	V
Short Circuit Current	20	*	mA
Impedance	0.1	*	Ω @ 1kHz
DC ACCURACY/STABILITY			
Gain	+1	*	V/V
Gain Error	±0.003 (±0.01 max)	*	%
Gain Temperature Coefficient	±0.1 (±1 max)	*	ppm/°C
Nonlinearity			
Sample Mode[1]	±0.0015	*	%
Hold Mode	±0.0015 max	±0.00076 max	%
Per mV of Offset Adjust (Hold Mode)	±0.3	*	ppm/mV
Offset Error (Adjustable to Zero)	±3 (±20 max)	*	mV
Offset Error @ T_{min}, T_{max}[2]	±0.6	*	mV
Offset Tempco per mV of Offset Adjust	±0.5	*	μV/°C/mV
SAMPLE MODE DYNAMICS			
Small Signal Bandwidth (−3 dB)	1	*	MHz
Full Power Bandwidth	120	*	kHz
Slew Rate	10	*	V/μs
Noise (dc to 1 MHz)	40	*	μV rms
SAMPLE-TO-HOLD SWITCHING			
Aperture Delay	80	*	ns
Aperture Uncertainty (Jitter)	150	*	ps
Offset Step (Pedestal)	±8	*	mV
Switching Transient			
Amplitude	±75	*	mV
Settling to ±0.003%	0.4	*	μs
Settling to ±0.00076%	1	*	μs
Dielectric Absorption Error (Uncompensated)	0.003	*	%
HOLD MODE DYNAMICS			
Droop Rate	0.05 (0.1 max)	0.02 (0.05 max)	μV/μs
Droop Rate @ T_{max}	1	*	μV/μs
Feedthrough Rejection (20 V p-p @ 10 kHz)	−106 (−96 max)	*	dB
HOLD-TO-TRACK SWITCHING			
Acquisition Time to ±0.00076% of 20 V[3]	5 (8 max)	3.5 (5 max)	μs
POWER REQUIREMENTS			
Nominal Voltage for Rated Performance (V_S)	±15 (±3%)	*	V
Power Supply Rejection	20	*	μV/V
Supply Current			
$+V_S$	10	*	mA
$-V_S$	10	*	mA
Power Dissipation	300	*	mW
TEMPERATURE RANGE			
Rated Performance	−25 to +85	*	°C
Storage	−40 to +125	*	°C
PACKAGE	14-Pin DIP	*	

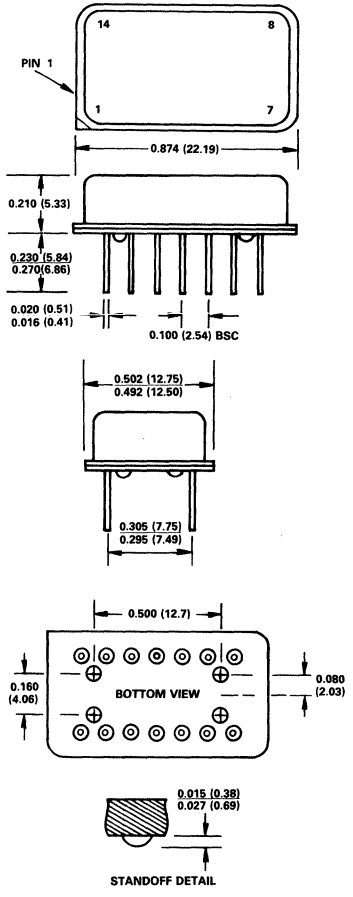
NOTE
[1]The AD1154 was designed specifically for 16-bit accurate sample/hold applications (tailored for hold mode performance), but it may be used as a track-and-hold amplifier with 15-bit accurate tracking performance.
[2]Error at +25°C adjusted to zero.
[3]Tested with 5 kΩ load.

*Specification same as AD1154AW
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions are shown in inches and (mm).

14-LEAD METAL PLATFORM DIP



PIN DESIGNATIONS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	SHA CONTROL	8	SHA OUTPUT
2	NO CONNECTION	9	OFFSET ADJUST
3	NO CONNECTION	10	NO CONNECTION
4	DIGITAL GROUND	11	+15 V
5	NO CONNECTION	12	ANA GND/DA COMP
6	ANALOG GROUND	13	SHA INPUT
7	OFFSET ADJUST	14	−15 V

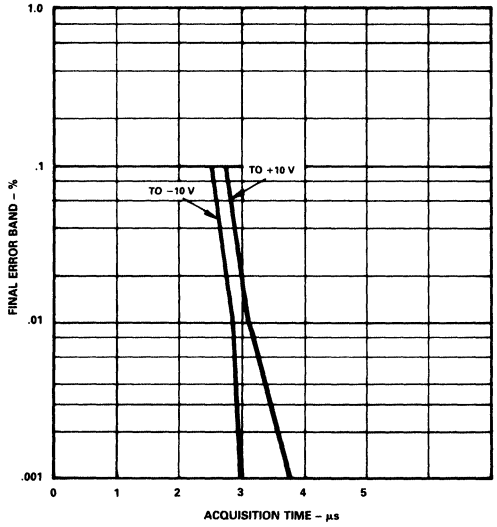


Figure 1. Acquisition Time vs. Final Error Band for 20 Volt Step

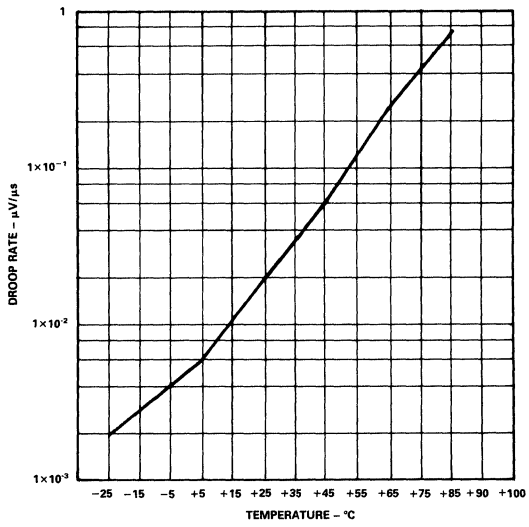


Figure 2. Droop Rate vs. Temperature

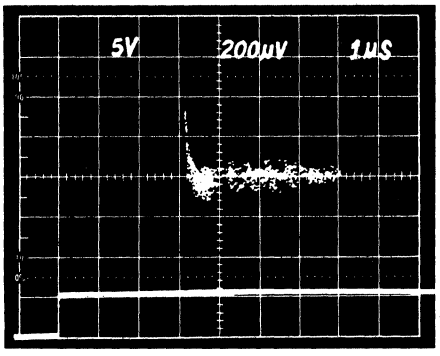


Figure 3. Hold-to-Sample Acquisition Time

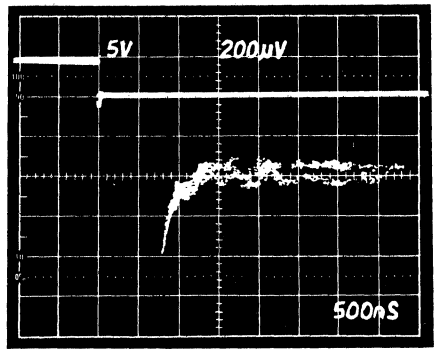


Figure 4. Sample-to-Hold Settling Time

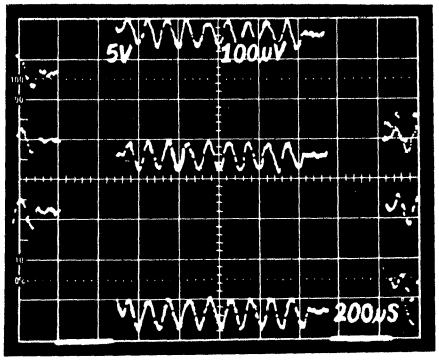


Figure 5. Input Feedthrough

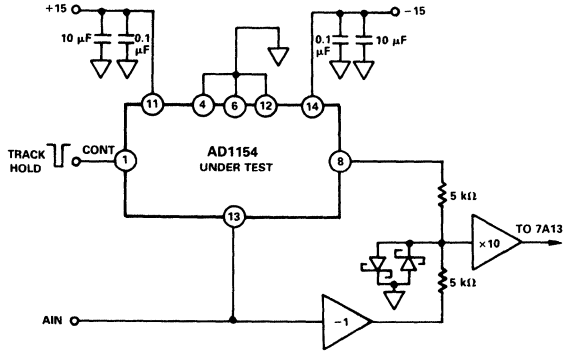


Figure 6. Acquisition Time Test Circuit

TERMINOLOGY

Accuracy is the peak deviation of the output from a straight line through the endpoints of the transfer function. It is expressed as a percentage of the full scale output range. Note that this parameter is measured in hold mode because the actual voltage to be converted is the voltage present at the output of the device during the hold mode.

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample/track command has been given assuming that the input amplifier has settled. This includes switch delay time, slewing time and settling time for a given output voltage change.

Aperture Time is the time required after the hold command for the switch to open fully. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

Aperture Jitter is the range of variation in the aperture time. If the aperture time is "tuned out" by advancing the hold command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution.

Charge Transfer (or offset step or pedestal) is the charge transferred to the storage capacitor when switching to the hold mode.

Droop Rate is the rate of change in output voltage over time while in the hold mode. The droop rate will determine how long a signal can be accurately held before it changes more than 1 LSB.

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in hold. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Small Signal Bandwidth is the maximum analog signal frequency that can be tracked before the gain is reduced by 3 dB. This assumes the signal amplitude is small enough so as not to be slew rate limited.

Switching Transient Settling Time is the time required for the device to stabilize in the hold mode to within specified limits of its final value after the hold mode signal has been given.

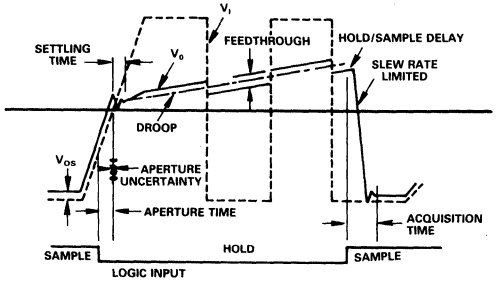


Figure 7. T/H Characteristics

INVERTING VS. NONINVERTING ARCHITECTURE

The AD1154 has a gain of +1 V/V. Many S/H amplifiers use an inverting architecture and hence have a gain of −1 V/V. The AD1154, because of its noninverting architecture, does not have an externally accessible summing point. This pin is found on most inverting S/Hs and is typically not used. In applications where the summing junction is not connected, the AD1154 can be used as a direct hardware replacement by tying Pin 12 to ground, but the output is of opposite polarity.

GROUNDING CONSIDERATIONS

The AD1154 is a true 16-bit performance sample/hold amplifier. In order to insure proper operation of the device, great care must be taken in managing the ground tracks. It is recommended that Pins 4, 6 and 12 of the AD1154 be tied together directly outside of the package. This point should then be tied to the analog ground of the A/D converter, as shown in Figure 8. This track should be as short and wide as possible to minimize voltage drops. Also note from the figure that any other analog grounds in the signal path should be joined to the A/D converter analog ground.

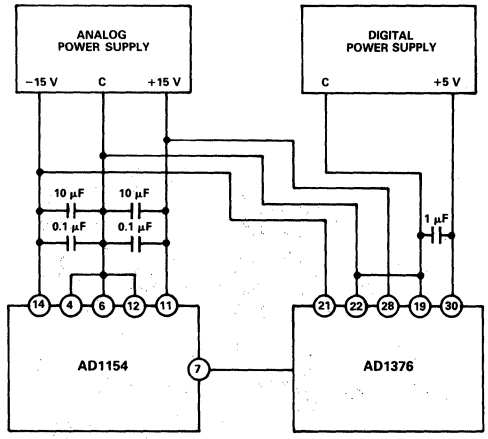


Figure 8. Basic Grounding and Power Supply Bypassing Practice

DIELECTRIC ABSORPTION COMPENSATION

The hold capacitor used in the AD1154 is a high quality ceramic chip capacitor. This capacitor's dielectric absorption characteristics are typically better than high quality film capacitors. In addition, the AD1154 provides a means for compensating for the dielectric absorption of the capacitor if better performance is required. If dielectric absorption compensation is not used, Pin 12 should be tied to ground. Please refer to the section titled "DISCUSSION OF DIELECTRIC ABSORPTION" for more detailed information.

POWER SUPPLY BYPASSING

The AD1154 utilizes high speed amplifiers in its design. These amplifiers require quiet power supplies that are free from spikes. For maximum performance it is recommended that both power supplies be bypassed with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors located as close to the device as possible (see Figure 8).

DISCUSSION OF DIELECTRIC ABSORPTION

The hold capacitor of the AD1154 was chosen for its low dielectric absorption (D.A.) characteristics. D.A. is directly affected by the sample/hold mode switching durations and input levels. The AD1154 provides the user with a pin for external D.A. compensation circuitry. The AD1154's uncompensated D.A. performance is inherently superior, and in most applications the D.A. compensation pin should be connected to ground. Where additional compensation is desired to tailor the AD1154 to a specific user's application, only three resistors and a capacitor are required to optimize the AD1154's D.A. performance (see Figure 11).

If a capacitor is charged to a voltage, discharged for a moderate period of time, and then open circuited, the voltage on the capacitor will begin to creep back towards its initial value. This creep voltage is known as dielectric absorption. Dielectric absorption occurs because the dielectric material doesn't polarize instantly, the molecules need time to align themselves. As a result, not all of the energy stored in a capacitor can be quickly recovered upon discharge.

A first order model of the hold capacitor to include dielectric absorption effects is shown in Figure 9. In addition to the main capacitance, C_M, and the insulation resistance, R_I, there is an

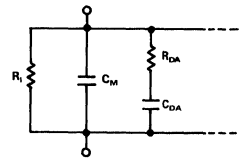


Figure 9. First Order Model of D. A. Effects

R_{DA} and a C_{DA}. When the capacitor is charged to some value, C_{DA} is also charged. When the capacitor is discharged, C_{DA} also discharges. But it must discharge through R_{DA}, and, if the capacitor is not discharged for a long enough period of time, C_{DA} will not completely discharge. As a result, when the capacitor is open circuited, C_{DA} will discharge into C_M causing the voltage across it to creep back towards its initial value. The actual model of the capacitor should contain additional R_{DA}s and C_{DA}s with increasing time constants in parallel with the one shown.

Figure 10 shows a circuit suitable for measuring the dielectric absorption of sample/hold amplifiers. The circuit operates as follows: R1 and C1 set the frequency of the SHA control; R2 and C2 set the amount of acquisition time allowed for the SHA. See the timing diagram of Figure 10.

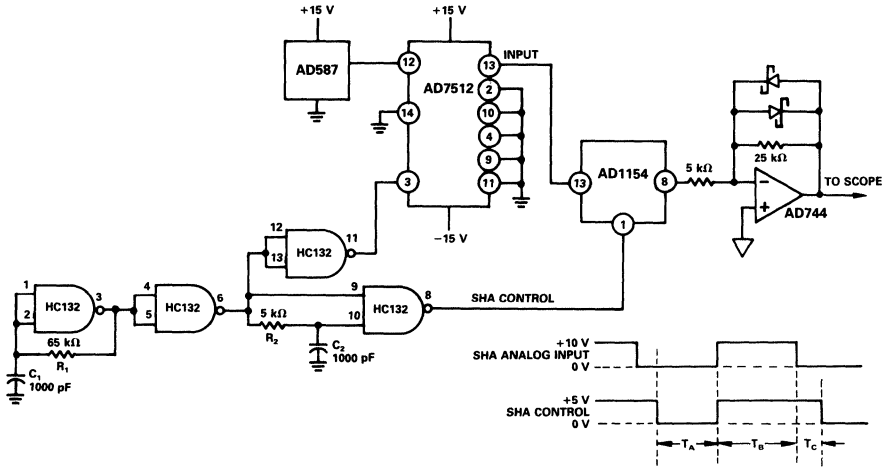


Figure 10. Dielectric Absorption Measurement Circuit

During T_B, the CONTROL line is high, the AD1154 is in the sample mode and the analog input charges the hold capacitor to +10 V. During T_C the analog input to the SHA is switched to ground, effectively shorting the hold capacitor for the remainder of the sample period. During T_A, the SHA is switched into hold mode and the hold capacitor is open circuited. The dielectric rebound can be observed on the oscilloscope during T_A. Refer to Figure 12.

Note that the dielectric absorption error is dependent on several factors: it is a function of how long the capacitor is charged (T_B), how long it is discharged (T_C) and how long it is observed while open circuited (T_A). These parameters can be modified by changing R1, R2, C1 and C2.

The AD1154 provides a pin to compensate for dielectric absorption. To use it, the circuit of Figure 11 must be employed.

To find the optimum values for R1, R2, R3 and C1 follow this procedure:

1. Adjust the D.A. measurement circuit (see Figure 10) to represent a typical sampling rate.
2. Observe the dielectric absorption error on the oscilloscope.
3. Pick (R1‖R2) • C1 to be equal to the approximate time constant (T_{const}) of the dielectric rebound on the oscilloscope (see photo in Figure 12).

4. R3 is used to adjust the magnitude of the compensation. To find an initial approximation for R3, the following relationship can be used:
   $R3 = [\text{Magnitude of D.A. error} \times (R1+R2)]/10 \times 1/(e^{-T_C/T_{CONST}} - e^{-T_A/T_{CONST}})$
5. R3 can then be fine trimmed for the flattest output during hold.

Using this method it is possible to reduce the effect of dielectric absorption by a factor of four or five. The typical values for resistors and capacitor given in Figure 11 are for a sample time of 20 μs, acquisition time of 5 μs and a hold time of 20 μs. When determining the values, R3 should be less than 10 Ω, and C1 should be as small as possible.

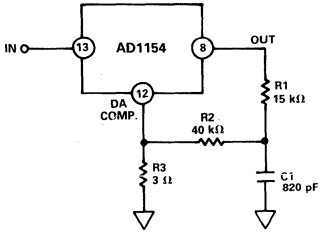


Figure 11. D/A Compensation Circuit with Typical Values

DYNAMIC SIGNALS

The primary purpose of using a sample/hold in front of an A/D converter is to hold the input constant while the A/D performs its conversion. Without a sample/hold, a 16-bit A/D converter would not be able to accurately digitize any signal whose slew rate exceeded 1 LSB divided by the conversion time. Or, for a 15 μs A/D with an input range of ±10 V this says:

$\text{Input Signal Slew Rate}_{MAX} = 1 \text{ LSB} \div \text{Conversion Time} = 20.3 \text{ V/S}$

Since the maximum slew rate of a sinusoid is defined as:

$\text{Slew Rate}_{MAX} = 2 \cdot \pi \cdot \text{Amplitude} \cdot \text{Frequency}$

This translates into a maximum input frequency of:

$F_{IN\ MAX} = \text{Slew Rate}_{MAX} \div (2 \cdot \pi \cdot \text{Amplitude}) = 0.32 \text{ Hz}$

By using a sample/hold, however, the maximum slew rate of the input signal is now limited by the aperture jitter of the sample/hold, which is usually orders of magnitude better than a conversion time. Specifically, for an AD1154 the analysis is:

$\text{Input Signal Slew Rate}_{MAX} = 1 \text{ LSB} \div \text{Aperture Jitter} = 2.035 \text{ V/μs}.$

Now the maximum input frequency becomes:

$F_{IN\ MAX} = \text{Slew Rate}_{MAX} \div (2 \cdot \pi \cdot \text{Amplitude}) = 32.4 \text{ kHz}.$

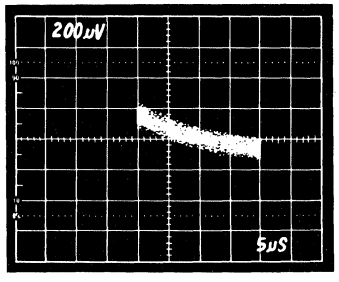


Figure 12. Dielectric Absorption

This represents a dramatic improvement over using the A/D converter by itself. The AD1154's 222 kHz throughput ($1/(T_{ACQ} + T_{SETT})$) and 150 ps aperture jitter allow it to digitize input signals of up to 32 kHz to 16-bit accuracy or up to a 128 kHz signal to 14-bits.

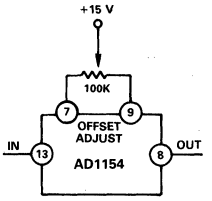


Figure 13. Offset Adjust Circuit

OPERATING INSTRUCTIONS

Offset Adjust

In most data acquisition systems only one offset adjustment is made. Usually the offset adjust of the A/D converter is used to null the combined system offsets. However, the offset or pedestal of the AD1154 can be nulled by connecting a trim potentiometer between Pins 7 and 9, and tying the wiper to +15 V (refer to Figure 13.) To null the pedestal, ground the input of the SHA and toggle the SHA CONTROL. Then adjust the pot until the output of the SHA in hold mode reads 0 V. Please note that each millivolt of offset adjust adjustment degrades linearity by 0.3 ppm.

APPLICATIONS

50kHz Sampling A/D System

Figure 14 shows a typical connection of the AD1154 to the AD1376 (16-bit 15.5 μs A/D converter). This combination will result in an A/D conversion system capable of sampling a 25 kHz signal at a 50 kHz throughput rate. (Where Throughput Rate = $T_{ACQ} + T_{SETTLE} + T_{CONV}$ = 3.5 μs + 1 μs + 15.5 μs = 20 μs.) This example has an input range of ±10 V, power consumption of < 1 W and 16-bit resolution. The accuracy of this system is limited to the AD1376's 14-bit performance.

Track-and-Hold

The AD1154's design is optimized for sample-and-hold applications and is internally compensated to guarantee 16-bit (0.00076%) hold mode gain nonlinearity. Even though the AD1154 is tailored specifically as a SHA, it may be used as a track-and-hold amplifier providing 15-bit (0.0015%) track mode gain nonlinearity.

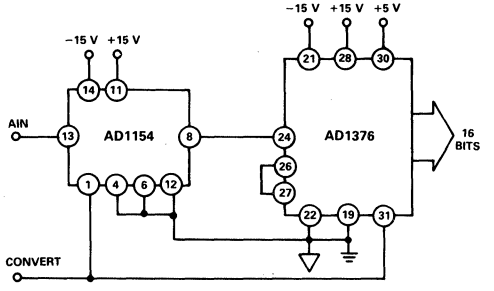


Figure 14. 50 kHz Sampling A/D Conversion System

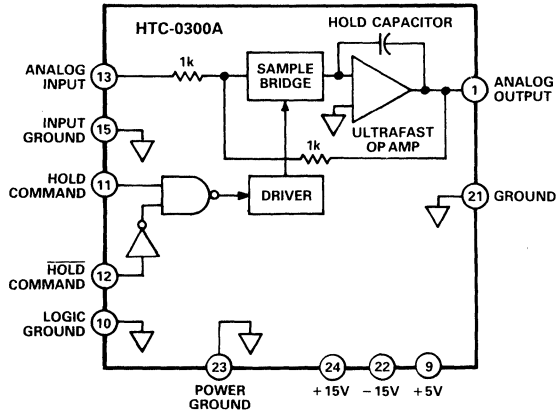
Ultrahigh-Speed Hybrid Track-and-Hold Amplifier

HTC-0300A

FEATURES
Aperture Jitter of 50ps
Input Range ±10V
Output Current ±50mA
Max Droop Rate 5μV/μs
Max 200ns Acquisition Time (0.01%; 10V Step)

APPLICATIONS
Data Acquisition Systems
Peak Measurement Systems
Simultaneous Sample & Hold
Analog Delay

HTC-0300A FUNCTIONAL BLOCK DIAGRAM



NOTES: WHEN APPLYING HOLD COMMAND TO PIN 11, CONNECT HOLD COMMAND (PIN 12) TO GROUND.
WHEN APPLYING HOLD COMMAND TO PIN 12, CONNECT HOLD COMMAND (PIN 11) TO +5V.

GENERAL DESCRIPTION

The HTC-0300A is a hybrid microcircuit track-and-hold amplifier useful in a wide range of signal processing applications, including waveform measurements, analog signal delay, and signal sampling.

The unit has a typical aperture jitter of only 50 picoseconds rms; wide dynamic input range of ±10 volts; and laser-trimmed gain and offset which preclude a need for external adjustments. Its speed and precision are the result of innovative design techniques using a high-speed op amp and DMOSFET switches. These techniques also enhance device performance in feedthrough rejection, linearity, harmonic distortion, droop rate, and output voltage swing.

ORDERING INFORMATION

For a case temperature range of −25°C to +85°C, order the HTC-0300A; it is packaged in a 24-pin hermetically-sealed ceramic DIP.

A case temperature range of −55°C to +125°C is available with the HTC-0300AM, HTC-0300AM/883B, and the HTC-0300ATD/883B. The first two units are housed in 24-pin metal packages, and the latter unit is packaged in a hermetic 24-pin ceramic DIP.

All versions of the HTC-0300A are manufactured in a facility which has been certified to MIL-STD-1772.

SPECIFICATIONS (Typical with nominal supplies, unless otherwise noted)

Parameter[1,2] (Conditions)	Sub-Group	Temp.	HTC-0300A[1] Min	Typ	Max	HTC-0300AM ATD/883B AM/883B[2] Min	Typ	Max	Units
ANALOG INPUT									
(FS = Full Scale = 10V; FSR = Full-Scale Range = 20V)									
# Voltage Range		+25°C			±10			±10	V
# Overvoltage, No Damage		+25°C			±15			±15	V
√ Input Impedance (V_{IN} = 10V; Pins 11 & 12 = "0")	1,2,3	Full	950	1000	1050	950	1000	1050	Ω
# Initial Offset Voltage (V_{IN} = 0V; Pins 11 & 12 = "0")	1	+25°C		±0.5	±5.0		±0.5	±5.0	mV
DIGITAL INPUT MODE CONTROL (TTL Compatible)									
√ Logic "0" Input Voltage	1,2,3	Full	0.0		0.8	0.0		0.8	V
√ Logic "0" Input Current	1,2	+25°C/ +125°C			±1.0			±1.0	µA
# Logic "0" Input Current		−55°C			±1.0			±1.0	µA
√ Logic "1" Input Voltage	1,2,3	Full	2.0		5.5	2.0		5.5	V
√ Logic "0" Input Current	1,2	+25°C/ +125°C			±1.0			±1.0	µA
# Logic "0" Input Current		−55°C			±1.0			±1.0	µA
ANALOG OUTPUT									
# Voltage		+25°C	±10			±10			V
# Current (Not Short Circuit Protected)		+25°C	±50			±50			mA
# Impedance		+25°C		0.1	1.0		0.1	1.0	Ω
Capacitive Load (See text)		+25°C		250			250		pF
# Noise in Track Mode[3]		+25°C							
dc to 100kHz				15			15		µV rms
dc to 1MHz				34			34		µV rms
dc to 5MHz				0.1			0.1		mV rms
DC ACCURACY/STABILITY									
# Gain		+25°C	−1.0			−1.0			V/V
√ Gain Error	1	+25°C		±0.05	±0.1		±0.05	±0.1	%
	2,3	Full						±0.15	%
√ Gain Nonlinearity	1	+25°C		±0.005	±0.01		±0.005	±0.01	%
	2,3	Full						±0.01	%
√ Gain Temperature Coefficient	2,3	Full		±0.5	+5		±0.5	±5	ppm FS/°C
√ Input Offset Temperature Coefficient	2,3	Full		±3	±15		±3	±15	ppm FSR/°C
TRACK (SAMPLE) MODE DYNAMICS									
Frequency Response (V_{IN} = 1V p-p; Pins 11 & 12 = "0")									
√ Small Signal (−3dB)	4	+25°C	8	16		8	16		MHz
Full Power (−3dB)		+25°C		8			8		MHz
√ Slew Rate (V_{IN} = 10V p-p; Pins 11 & 12 = "0")	4	+25°C	220	300		220	300		V/µs
	5,6	Full	180	300		180	300		V/µs
# Harmonic Distortion[4]		+25°C		80			80		dB
TRACK (SAMPLE)-TO-HOLD DYNAMICS									
# Aperture Time		+25°C	4	6	8	4	6	8	ns
Aperture Uncertainty (Jitter)		+25°C		50			50		ps, rms
√ Pedestal (Offset Step)	4	+25°C		±2.5	±20		±2.5	±20	mV
√ Pedestal Temp. Coeff.	5,6	Full						±8	ppm FS/°C
# Pedestal Sensitivity to +5V Supply Changes		+25°C		5			5		mV/V
Switching Transient									
√ Amplitude	4	+25°C		180	380		180	380	mV p-p
	5,6	Full		180	380		180	380	mV p-p
√ Settling Time									
To 0.1%	7	+25°C		40	85		40	85	ns
To 0.1%	8	Full		40	85		40	85	ns
To 0.01%	7	+25°C		60	100		60	100	ns
To 0.01%	8	Full		60	100		60	100	ns
HOLD MODE DYNAMICS									
√ Droop Rate	4	+25°C		±0.5	±5		±0.5	±5	µV/µs
	5	+125°C						±1.8	mV/µs
	6	−55°C						±5	µV/µs
√ Feedthrough Rejection (V_{IN} = 20V p-p@2.5MHz)	7	+25°C	64	74		64	74		dB
HOLD (SAMPLE)-TO-TRACK DYNAMICS									
√ Acquisition Time to 0.1%	7	+25°C		100	170		100	170	ns
(10V p-p Step)	8	Full		100	170		100	170	ns
√ Acquisition Time to 0.01%	7	+25°C		160	200		160	200	ns
(10V p-p Step)	8	Full		160	200		160	200	ns
Acquisition Time to 0.1% (20V p-p Step)		+25°C		110			110		ns

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- $\pm V_S$ . . . . . ±18V
- V_{CC} . . . . . −0.5, +7V

Storage Temperature . . −65°C to +150°C
Junction Temperature . . +150°C (A & AM)
Junction Temperature . . . . . +165°C (/883B units)
Lead Soldering (10sec) . . . . . +300°C
Digital Inputs . . . . . −0.5V to V_{CC}
Analog Input . . . . . ±15V

TRACK/HOLD FUNCTION TRUTH TABLE

With logic levels shown at		
HOLD (Pin 11)	$\overline{\text{HOLD}}$ (Pin 12)	Operating Mode of HTC-0300A is
0	0	Track
0	1	Track
1	0	Hold
1	1	Track

PIN DESIGNATIONS
(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
24	+15V	1	ANALOG OUTPUT
23	POWER GROUND	2	N/A
22	−15V	3	N/A
21	GROUND	4	N/A
20	N/A	5	N/A
19	N/A	6	N/A
18	N/A	7	N/A
17	N/A	8	N/A
16	N/A	9	+5V
15	INPUT GROUND	10	LOGIC GROUND
14	N/A	11	$\overline{\text{HOLD}}$ COMMAND
13	ANALOG INPUT	12	$\overline{\text{HOLD}}$ COMMAND

Parameter[1,2] (Conditions)	Sub-Group	Temp.	HTC-0300A[1] Min	Typ	Max	HTC-0300AM ATD/883B AM/883B[2] Min	Typ	Max	Units
POWER REQUIREMENTS									
Supply Voltages									
$\pm V_S$		±25°C	±14.25	±15	±15.75	±14.25	±15	±15.75	V
V_{CC} (Logic Supply)		+25°C	+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
Supply Currents (V_{IN} = 0V; Pins 11 & 12 = "0")									
✓ $\pm V_S$	1	+25°C		±21	±25		±21	±25	mA
	2,3	Full		±21	±25		±21	±25	mA
✓ V_{CC} (Logic Supply)	1	+25°C		+4	+5		+4	+5	mA
	2,3	Full		+4	+5		+4	+5	mA
✓ Power Dissipation	1	+25°C		650	775		650	775	mW
	2,3	Full		650	775		650	775	mW
✓ $\pm V_S$ POWER SUPPLY REJECTION RATIO (PSSR)	1	+25°C		±0.3	±0.5		±0.3	±0.5	mV/V
(V_{IN} = 10V; Pins 11 & 12 = "0")	2,3	Full		±0.3	±0.5		±0.3	±0.5	mV/V
THERMAL RESISTANCE									
Case to Air, θ_{ca}[5]				34			34		°C/W
Junction to Case, θ_{jc}				28			28		°C/W
MEAN TIME BETWEEN FAILURES (MTBF)[6]						2.1×10^6			Hours
PACKAGE OPTIONS[7]									
DH-24B				HTC-0300A			HTC-0300ATD/883B		
M-24A							HTC-0300AM		
							HTC-0300AM/883B		

NOTES
✓100% tested (See Notes 1 and 2).
#Specification guaranteed by design; not tested.
[1]HTC-0300A parameters preceded by a check (✓) are tested at +25°C ambient temperature; performance is guaranteed over the industrial temperature range (−25°C to +85°C) case temperature.
[2]HTC-0300AM, ATD/883B, AM/883B parameters preceded by a check (✓) are tested at −55°C case, +25°C ambient, and +125°C case temperatures.
[3]Noise level increases with increasing duty cycle of Hold Command. Noise figures shown for Track mode are measured with input grounded and filters for frequencies shown on output.
[4]V_{IN} = 20V p-p, 200kHz sine wave; R_L = 1kΩ; Mode Control = Track.
[5]The relationship between the device package and outside environment (θ_{ca}) varies with the application. Value shown is based on measuring case temperature with supply voltages applied to a device installed in a ZIF socket mounted on a standard "EJ" burn-in board.
[6]MTBF calculated for /883B unit using MIL-HNBK 217D; Ground Fixed; Temperature (Ambient) = +25°C.
[7]See Section 14 for package outline information.
Specifications subject to change without notice.

Explanation of Subgroups

Subgroup 1 – Static tests at +25°C.
(10% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 – Static tests at maximum rated temperature.
Subgroup 3 – Static tests at minimum rated temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated temperature.
Subgroup 6 – Dynamic tests at minimum rated temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated temperatures.
Subgroup 11 – Switching tests at minimum rated temperatures.
Subgroup 12 – Periodically sample tested.

APPLICATIONS

Track-and-hold (T/H) amplifiers can be used in a wide variety of ways, but the most common application for these units is to place them ahead of an A/D converter. The combination of a T/H and converter is used when the bandwidth of the signal to be digitized is wider than the converter can handle by itself, i.e., the analog input is changing more than one LSB during the converter's conversion interval.

In applications of this type, the HTC-0300A "freezes" the incoming signal on command to present a nonchanging signal at the input stage of the converter.

The HTC-0300A T/H can reduce the aperture window to 100 picoseconds when used with the appropriate A/D. It can also be used for peak-holding functions, simultaneous sampling A/Ds (when combined with analog multiplexers), and other high-speed analog signal processing applications.

THEORY OF OPERATION

When operated in the "track" mode, the HTC-0300A functions as an operational amplifier with a gain of −1, following all changes in the analog input signal as they occur.

When a TTL-compatible digital logic "1" is applied to the Hold Command input of the T/H, the inverted analog output of the HTC-0300A is "held" at the value which was present at the time of the Hold Command, plus the aperture time. If the change from the "track" mode to the "hold" mode is accomplished via Pin 11, $\overline{\text{Hold}}$ Command input (Pin 12) must be connected to ground.

For applications which require an inverted Hold Command, this "freezing" of the inverted analog output can be accomplished with a digital "0" applied to the $\overline{\text{Hold}}$ Command (Pin 12) input. In this case, a digital "1" establishes the "track" mode of operation. For these, the Hold Command input (Pin 11) must be connected to +5V.

Refer to Figure 1, the HTC-0300A Track/Hold Waveforms.

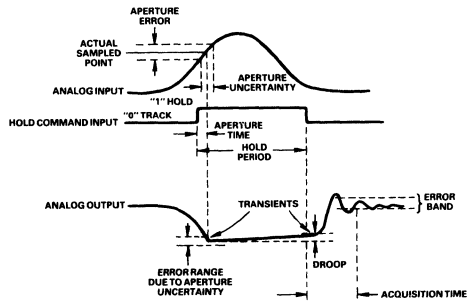


Figure 1. Track/Hold Waveforms – HTC-0300A

Two different intervals of time can affect the point on the analog input which is sampled when the T/H is switched from "track" to "hold". There is no major difference in operation whether this change in state is accomplished via the Hold Command or $\overline{\text{Hold}}$ Command; the functioning of the HTC-0300A is essentially the same, with only a slight difference in timing because of an additional logic package in the $\overline{\text{Hold}}$ Command signal path.

The delay interval, aperture time, is a constant and should not be regarded as an error source. The design of the HTC-0300A assures that aperture time is within its spec from unit to unit; and is also repeatable from one "hold" command to the next in any given unit. In this way, aperture time can be compensated with system timing to assure an optimum sampling point.

Aperture uncertainty, or "jitter", is the other interval affecting the held value. It is the result of noise signals which modulate the phase of the hold command and shows up as sample-to-sample variations in the value of the analog signal being "frozen."

As expected, the error resulting from jitter is directly related to the dV/dt of the analog input. If very-high-speed inputs are sampled, any given value of jitter will result in larger errors in the held value at the output as dV/dt increases. See Figure 2.

The high feedthrough rejection of the HTC-0300A in the hold mode is an important characteristic; it precludes errors being introduced during the conversion interval of the digitizer.

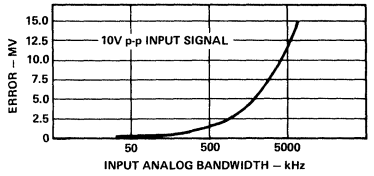


Figure 2. HTC-0300A Error Due to Aperture Uncertainty

As shown in Figure 1, droop is the amount the output changes during the hold period; this is the result of loading on the internal hold capacitor. Low droop rates are important in T/H amplifiers to insure they are appropriate for high-resolution digitizing. Excessive droop rates can negate the effectiveness of having converters of 10 or 12 bits or more. Lower-order bits may be in error because of changes in the held value during the conversion cycle, especially for successive-approximation converters.

The return to the "track" mode is accomplished by changing the digital logic level of the hold command; Figure 1 shows the hold command as it would appear at the (Pin 11) Hold Command input.

Acquisition Time is the interval required for the analog output to re-establish accurate tracking of the changing input and remain within a specified error band around its final value. The greater the change in the input value during the hold period, the longer this interval is. Nyquist sampling is the most stringent application.

Transients shown in Figure 1 are "spikes" which occur at the output of the T/H at the beginning and end of each "hold" period because of switching transients within the unit. When a T/H is used at the output of a D/A converter for "deglitching" discontinuities in the output of the converter, these transients occur at the update rate and can be filtered.

SAMPLE-AND-HOLD (S/H) MODE

Although it is generally used in the track-and-hold mode, the HTC-0300A can also be used as a sample-and-hold device. In the S/H mode, the output of the unit is usually in the "hold" mode, but is switched briefly to the "sample" (track) mode.

The width of the the sample pulse applied to the $\overline{\text{Hold}}$ Command input (or, if using inverted logic, the Hold Command input) is determined by (1) the acquisition time of the HTC-0300A, and (2) the desired accuracy of the sampled output. Output accuracy will also be a function of the amount of change which has occurred since the preceding sample.

This latter phenonmenon is illustrated in Figure 3. Note the analog input has changed drastically between the first and second hold commands. There is a considerably smaller change between the third and fourth pulses; as a consequence, movement in the held value of the output is correspondingly smaller.

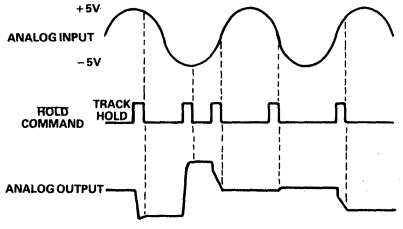


Figure 3. Sample/Hold Operation

Figure 4 illustrates settling accuracy versus acquisition time; closer accuracies require more time. The relationship approaches an asymptotic curve and is not a linear function.

The HTC-0300A is a "closed loop" T/H and is suitable for most applications requiring a track-and-hold for update rates up to 5–10MHz. (Note: 5MHz conversion rates are only a guide and are based on system acquisition time, not logic speed. Higher rates are possible with trade-offs in acquisition time.)

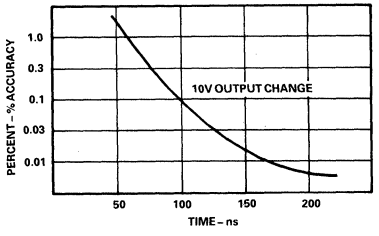


Figure 4. Settling Accuracy vs. Acquisition Time

For optimum performance, the HTC-0300A must have external bypass capacitors connected to the power supply pins close to the device. Electrolytic capacitors of 10 – 22μF and ceramic capacitors of 0.01 – 0.1μF on each supply will enhance performance of the unit.

Output loading has some restrictions. To avoid oscillations, limit capacitive loads to 250pF; the recommended resistive loading is 500Ω. Acquisition and settling times are relatively unaffected by capacitive loads up to 50pF and resistive loads down to 250Ω.

A massive ground plane, careful component layout, and physically separating digital and analog signals as much as possible are also among the multitude of items which can affect the operation of circuits that include the HTC-0300A T/H.

Cross coupling of analog and digital signals is often a major problem at high frequencies. Relatively low levels of ground plane noise can "mask" lower-order bits when the HTC-0300A is used in high-resolution digitizing. The user must exercise care in electrical and mechanical design to assure satisfactory performance.

ANALOG DEVICES

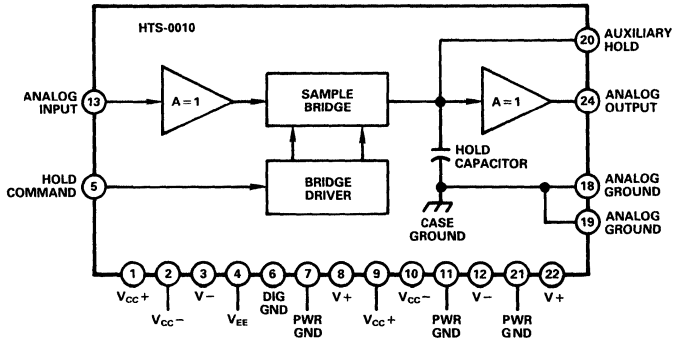
Ultrahigh-Speed Hybrid Track-and-Hold Amplifiers

HTS-0010

FEATURES
Aperture Jitter of 2ps rms
Acquisition Time 10ns
Output Current ±40mA
Slew Rate 300V/μs

APPLICATIONS
Data Acquisition Systems
Radar Systems
Instrumentation Systems
Medical Electronics

HTS-0010 FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The Analog Devices HTS-0010 Track-and-Hold is another example of Analog's continuing efforts to advance the state of the art in high-speed circuits.

The HTS-0010 adds breadth to a line of devices which offers designers the industry's widest range of track-and-hold and sample-and-hold units.

Its pinouts are similar to its predecessor HTS-0025 Track-and-Hold, but it provides enchanced performance in many of the characteristics established by that device. Two pins which are unused on the HTS-0025 are used on the HTS-0010, but with those exceptions, the two devices have identical pin assignments. This plug-in compatibility gives designers remarkable flexibility in selecting those parameters which are optimum for their applications.

The HTS-0010 Track-and-Hold (T/H) uses many of the proven design concepts which have made the HTS-0025 T/H the standard of comparison for high-speed circuits of this type. A dc-coupled Schottky diode bridge is driven by a high impedance buffer amplifier and followed by a low impedance output amplifier to achieve the best possible combination of speed and drive capabilities.

All models of the HTS-0010 are housed in a standard 24-pin metal DIP. The unit operating over a temperature range of 0 to +70°C is HTS-0010KD; the unit for a range of −55°C to +100°C is HTS-0010SD.

SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

Parameter	Units	HTS-0010KD	HTS-0010SD
ANALOG INPUT			
Voltage Range			
For Rated Performance	V p-p	2	*
Maximum Without Damage	V	±3	*
Impedance	Ω	10^5	*
Capacitance	pF (max)	7	*
Bias Current	μA (max)	20	*
DIGITAL INPUT (ECL Compatible)			
Mode Control			
Hold Command Input			
"0" = Track	V	−1.5 to −1.8	*
"1" = Hold	V	−0.8 to −1.1	*
ANALOG OUTPUT			
Current (Not Short Circuit Protected)	mA (max)	±40	*
Impedance	Ω (max)	9 (12)	*
Noise in Track Mode			
@ 5.0MHz Bandwidth	μV rms (max)	20 (40)	*
DC ACCURACY/STABILITY (FS = Full Scale)			
Gain (No Load)[1]	V/V (min)	0.96 (0.93)	*
Gain Nonlinearity; 2V FS Input	% (max)	0.1	*
Gain Nonlinearity; 1V FS Input	% (max)	0.01	*
Gain Temperature Coefficient	ppm/°C (max)	30 (40)	30 (50)
Initial Offset Voltage	mV (max)	±2 (±5)	*
Offset vs. Temperature	μV/°C (max)	125 (175)	*
TRACK (SAMPLE) MODE DYNAMICS			
Frequency Response			
Full Power Bandwidth	MHz (min)	40	*
Small Signal (−3dB) Bandwidth	MHz (min)	60	*
Slew Rate	V/μs (min)	300 (250)	*
Harmonic Distortion (Track Mode;			
4MHz, 2V p-p Input)			
R_L = 1kΩ	dB (max)	−68	*
R_L = 500Ω	dB (max)	−65	*
R_L = 200Ω	dB (max)	−64	*
R_L = 75Ω	dB (max)	−50	*
TRACK (SAMPLE)-TO-HOLD SWITCHING			
Effective Aperture Delay Time[2]	ns (max)	−2 (±1)	*
Aperture Uncertainty (Jitter)	ps (rms max)	2	*
Offset Step (Pedestal)	mV (max)	±2 (±10)	*
Sensitivity to Temperature	μV/°C (max)	50	250[3]
Sensitivity to −5.2V	mV/V (max)	10	*
Switch Delay Time	ns	1.5	*
Switching Transient			
Amplitude	mV (max)	±15 (30)	*
Settling to ±5mV	ns (max)	5 (14)	*
HOLD MODE DYNAMICS			
Droop Rate (@ +25°C)	mV/μs (max)	0.1	*
Droop Rate (@ Temperature Extremes)	mV/μs (max)	3.0	*
Feedthrough Rejection			
(2V p-p Input)			
@ 1MHz	dB (min)	62	*
@ 10MHz	dB (min)	52	*
HOLD-TO-TRACK (SAMPLE) DYNAMICS[4]			
Acquisition Time (1V Step)			
to ±1%	ns (max)	10 (16)	*
to ±0.1%	ns (max)	14 (19)	*
Acquisition Time (2V Step)			
to ±1%	ns (max)	13 (16)	*
to ±0.1%	ns (max)	16 (22)	*
Switch Delay Time	ns	1.5	*

Parameter	Units	HTS-0010KD	HTS-0010SD
POWER REQUIREMENTS			
V+ (+15V ±0.5V)	mA (max)	36	*
V− (−15V ±0.5V)	mA (max)	48	*
V_{CC}+ (+5.0V ±0.25)	mA (max)	22	*
V_{CC}− (−5.0V ±0.25)[5]	mA (max)	25	*
V_{EE} (−5.2V ±0.25)[5]	mA (max)	45	*
Power Dissipation	W (max)	1.73	*
Power Supply Rejection Ratio[6] (dc to 10kHz)	mV/V (max)	10	*
TEMPERATURE RANGE			
Operating (Case)	°C	0 to +70	−55 to +100
Storage	°C	−55 to +125	*
THERMAL RESISTANCE[7]			
Junction to Air, θ_{JA} (Free Air)	°C/W	42	*
Junction to Case, θ_{JC}	°C/W	12	*
MTBF[8]			
Mean Time Between Failures	Hours		6.83×10^5
PACKAGE OPTION[9]			
M-24A		HTS-0010KD	HTS-0010SD

For applications assistance, call (919) 668-9511.

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NOTES

[1]Gain = $\frac{R_L \times 0.96}{R_L + 9}$

[2]Effective Aperture Delay Time is delay between Hold strobe and held value of analog output, referenced to analog input (see text).

[3]Pedestal temperature variation on HTS-0010SD is same as HTS-0010KD below +70°C, but increases between +70°C and +100°C.

[4]For acquisition time measurements, $R_L = 200\Omega$; $C_L = 3pF$.

[5]V_{CC}− may be tied to V_{EE} with adequate bypass capacitors (see text).

[6]Variations in V− (−15V) have greater effect on unit performance than variations in other supplies; PSRR shown is for V−.

[7]Maximum junction temperature is +150°C.

[8]Calculated using MIL-HNBK 217; Ground; Fixed; +70°C case temperature.

[9]See Section 14 for package outline information.

*Specifications same as HTS-0010KD.

Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION
1	V_{CC}+ (+5V)
2	V_{CC}− (−5V)
3	V− (−15V)
4	V_{EE} (−5.2V)
5	HOLD COMMAND
6	DIGITAL GROUND
7	POWER GROUND
8	V+ (+15V)
9	V_{CC}+ (+5V)
10	V_{CC}− (−5V)
11	POWER GROUND
12	V− (−15V)
13	ANALOG INPUT
14	N/A
15	N/A
16	N/A
17	N/A
18	ANALOG GROUND
19	ANALOG GROUND
20	AUXILIARY HOLD
21	POWER GROUND
22	V+ (+15V)
23	N/A
24	ANALOG OUTPUT

POWER GROUND (PINS 7, 11 AND 21), ANALOG GROUND (PINS 18 AND 19), AND DIGITAL GROUND (PIN 6) MUST BE CONNECTED TOGETHER AND TO A LOW-IMPEDANCE GROUND FOR PROPER OPERATION. MAKE CONNECTIONS AS CLOSE TO DEVICE AS POSSIBLE. HYBRID CASE IS CONNECTED TO ANALOG GROUND INTERNALLY.

Applications

One of the main uses for track-and-hold (T/H) units is ahead of analog-to-digital (A/D) converters to allow digitizing signals with bandwidths higher than the A/D can handle by itself. The use of an appropriate T/H allows the converter to become a true "Nyquist converter", i.e., capable of digitizing analog signals whose maximum bandwidth is one-half the encoding rate.

The characteristics of the HTS-0010 T/H make it useful in multiple other applications beside this "standard" use of devices of this kind. It can be used in sample and hold circuits, peak holding applications, simultaneous sampling A/Ds (with appropriate analog multiplexing), and for many other data processing needs.

Refer to Figure 1, HTS-0010 Interconnection Diagram.

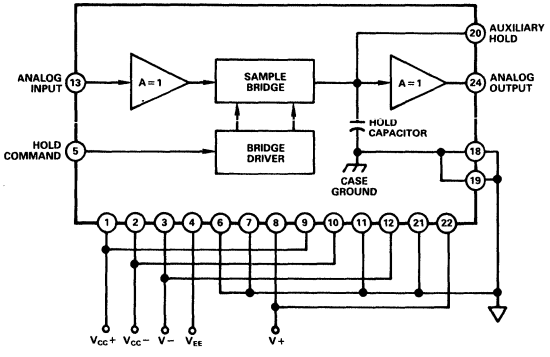


Figure 1. HTS-0010 Interconnection Diagram

Bypass capacitors are used internally on all power supply leads on the HTS-0010 track-and-hold. External bypassing of all power supplies with 0.01μF–0.1μF ceramics will help performance. In addition, electrolytic capacitors of 10-22 microfarads on each supply will also enhance the HTS-0010's operation

A massive ground plane, careful component layout, and physically separating analog and digital signals are among the other considerations which can have major effects in improving the high-speed characteristics of the HTS-0010 track-and-hold.

As shown in Figure 1, supply voltages must be applied to all pins for which they are designated. In addition, it is extremely important to connect all grounds together, and to a solid, low-impedance ground plane. These connections must be made as close to the hybrid as physically possible.

Five different voltages are shown for powering the HTS-0010. These are the voltages which are used in final test and calibration and are the recommended voltages for best performance, but minor variations from these recommendations are possible.

For best performance, the amplifier supplies, $V_{CC}-$ and $V_{CC}+$ should be equal and opposite, as shown. If desired, the ECL logic supply ($V_{EE} = -5.2V$) can be used also for $V_{CC}-$, to eliminate the need for a separate power supply voltage. If it is, bypass capacitors should be used at each supply pin to decrease the possibility of logic switching noise introducing extraneous signals.

TRACK-AND-HOLD MODE

When operated in the "track" mode, the HTS-0010 T/H functions as a buffer amplifier, following all changes in analog input as they occur. The user selects the point at which digitizing is to be done by applying an external ECL-compatible HOLD COMMAND to Pin 5.

Refer to Figure 2, Track/Hold Waveforms.

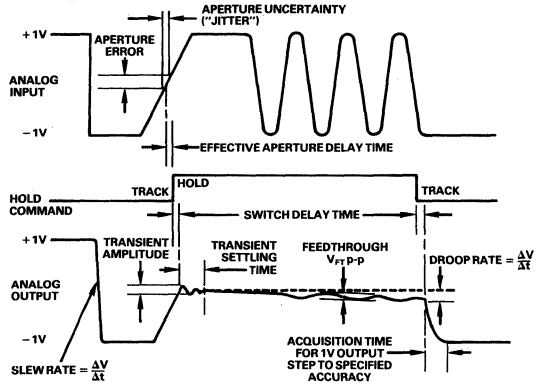


Figure 2. Track/Hold Waveforms

A varying, ideal analog input is shown at the top of Figure 2 for purposes of illustrating the response of the HTS-0010 to various types of inputs. This method of presentation helps show some of the critical, and often misleading, parameters of high-speed track-and-hold devices.

During the track mode, the unit operates as a high-speed buffer amplifier, with the output following input changes as they occur. In this mode, the response of the HTS-0010 is limited primarily by the slew rate characteristics of the device. As a result, the analog output is a faithful reproduction of the input as long as the highest frequency component of the input signal does not exceed the bandwidth of the unit.

The analog output shown on the bottom of Figure 2 tracks the input until a HOLD COMMAND is applied to Pin 5. When this pulse arrives, the sample bridge of the HTS-0010 disconnects the hold capacitor from the input. The short, but finite, interval required for this action is called aperture time.

Two other delay intervals combine with aperture time. One is delay in the hold command caused by propagation delay in the bridge driver; for purposes of discussion, this is a digital delay (t_d) because it is the time required for logic switching to occur. The other is propagation delay through the input buffer amplifier, which is an analog delay (t_a) because it affects the analog input signal being applied to the hold capacitor (see HTS-0010 Block Diagram).

Each of these three components is critical in the design of track-and-hold circuits, but the user needs to be concerned only with their combined overall effect. The combination is specified here as Effective Aperture Delay Time and is defined as the interval between the leading edge of the hold command and that instant when the input signal is equal to the held value.

Basically, effective aperture delay time is a measure of the difference between the analog and digital delay (t_d–t_a) and can assume a zero, positive, or negative value depending upon the comparative lengths of the two delays. In the HTS-0010, the analog delay (t_a) is greater than the switching delay (t_d), and causes the unit to hold an input voltage which occurred before the hold command because the hold capacitor sees a delayed version of the input signal.

The specification for Effective Aperture Delay Time is a more useful measurement for assessing T/H performance than is the measurement of only aperture time because it includes all three

of the components which have an effect on how quickly the device can make the change from the track mode to the hold mode.

The time intervals discussed above help explain what happens when the HTS-0010 makes the change from the track mode to the hold mode. In normal operation, however, they become academic discussions since most users of the T/H are more interested in when the held value has reached its steady state.

Aperture uncertainty or "jitter," is the result of noise signals of various kinds which modulate the phase of the hold command. This jitter shows up as a sample-to-sample variation in the value of the analog signal which is being "frozen."

Aperture uncertainty manifests itself as an aperture error, as shown in Figure 2. The amplitude of the error is related to the dV/dt of the analog input. For any given value of aperture uncertainty, aperture error will increase as the input dV/dt increases.

The design characteristics of the HTS-0010 insure that effective aperture delay time is within its specification from unit to unit; and is also repeatable from one "hold" command to the next within any unit. Therefore, it should not be regarded as an error source the way aperture uncertainty is. Effective aperture delay time can be compensated with system timing which correctly establishes the beginning of the hold period.

Referring again to Figure 2, a switching transient appears in the analog output as a result of this transition from "track" to "hold." The Specifications table includes the maximum amplitude and duration of this transient; and also includes information on the switch delay time which precedes it. The held output is settled to within 1mV 6-15ns after the leading edge of the hold signal.

Feedthrough rejection is a measure of the amount of leakage from input to output during the hold interval after the HTS-0010 has settled to its specified accuracy. High feedthrough rejection is important because it assures no errors will be introduced during the conversion interval of the converter used at the output of the T/H.

In the illustration, V_{FT} is the small amount of "ripple" voltage on the held value of analog output. The ratio of output feedthrough to input signal is measured in dB and is equal to:

$$20 \log \left[\frac{V_{FT\ p\text{-}p}}{V_{IN\ p\text{-}p}} \right]$$

As shown, droop is that amount of change in the analog output which occurs during the hold interval. Improving (lessening) the droop rate can be accomplished by adding capacitance in parallel with the internal hold capacitor, but at the expense of slowing down the T/H and its ability to handle high-speed signals.

Applications which require longer hold times than the standard HTS-0010 provides may require external capacitance in parallel with the internal hold capacitor. For these, the user can parallel extra capacitance by connecting it between pin 20 and ground. The droop rate will be improved, but the overall speed and bandwidth of the T/H will be reduced. This extra connection should be made close to the hybrid case or it may introduce small amounts of electrical noise.

Switch delay time shown in Figure 2 is the interval between the end of the hold command and the start of movement in the analog output as it begins to retrack the analog input. This delay occurs at both the beginning and the end of the hold interval and is primarily the result of propagation delay through the output buffer amplifier.

Acquisition time is the time required for the output of the T/H to reacquire and begin tracking accurately the analog input after the T/H has returned to the "track" mode. The acquisition time "clock" starts when the output begins moving and stops when the output has settled to its specified accuracy. As might be expected, longer acquisition times are required for larger signals and/or greater accuracy.

High slew rates are also important during acquisition time, but the desire for speed must be tempered with practical considerations. If the design of the unit achieves only speed without regard for overshoot, the acquisition time will be lengthened. Excessive "ringing" around the signal being acquired precludes applying successive hold commands at MHz update rates.

SAMPLE-AND-HOLD (S/H) MODE

Although generally used in the track-and-hold mode, the HTS-0010 can also be used as a sample-and-hold device for applications where this capability is needed.

The operation of the unit is essentially a "mirror" of the T/H operation, in that the output is usually in the "hold" mode but is switched to the "sample" (track) mode for brief intervals.

The width of the sample pulse which is used will be based on factors which are different for each application. Basically, the user establishes the width of this pulse by taking into account:

1. The acquisition time of the HTS-0010.
2. The desired accuracy of the sampled output.
3. The maximum amount of change which has occurred since the preceding sample.

This latter phenomenon is illustrated in Figure 3 Sample/Hold Operation.

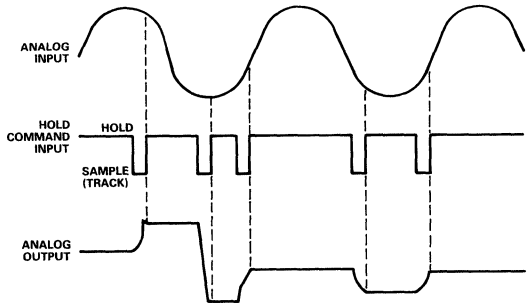


Figure 3. Sample/Hold Operation

When operating as a S/H, the signal applied to the HOLD COMMAND input (Pin 5) is usually a digital logic "1" which holds the HTS-0010 output at the input value present at the time of the sample/hold pulse.

Figure 3 shows asynchronous pulses applied to cause the output to reslew to new values. The trailing edge establishes the sample (track) mode; the leading edge returns the output to "hold".

In Figure 3, the analog input applied to the unit has changed drastically between the first and second sample (track) pulses. Smaller differences in the input values are present at the times of the second and third pulses. These differences in input show

up as differences in the amount of movement of the analog output.

The exceptional acquisition time of the HTS-0010 makes it extremely attractive for sample-hold applications because of its ability to acquire new output values quickly. This characteristic of the device allows the use of a narrow sample pulse and an inherently faster sample rate, limited only by the factors enumerated earlier.

Refer to Figure 4 Settling Accuracy vs. Acquisition Time.

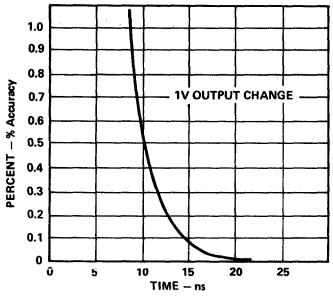


Figure 4. Settling Accuracy vs. Acquisition Time

This graph illustrates that closer accuracies require correspondingly longer amounts of time to acquire the signal. As shown, the accuracy/time relationship approaches an asymptotic curve, as opposed to being a linear function.

Another point to consider in Figure 4 is the output change which is illustrated is for a 1V change. If the output is required to change less than one volt (as it is between the second and third pulses in Figure 3, for example), the amount of time required to acquire the new value will be less than that which is shown.

When using the HTS-0010 or any other high-speed track-and-hold in the real world of data acquisition for fast-changing signals, the line between the device operating as a T/H or a S/H tends to "blur."

The designer using it as a T/H ahead of an A/D converter will generally vary the amount of "hold" time to obtain optimum operation for his particular application. When that performance is achieved, the HTS-0010 may, in the strictest sense of the word, be operating as a sample-and-hold. But it is useful to regard the two modes of operation separately when discussing the theory of operation of the unit.

DIFFERENCES: HTS-0010 VS. HTS-0025

As noted earlier, pin designations for the HTS-0010 T/H are similar to the predecessor HTS-0025 T/H. Two pins not used on the HTS-0025 are used for HTS-0010 functions, and attempts to use it as a "drop-in" replacement for the HTS-0025 need to take this into account.

Pins 20 and 21 on the HTS-0010 are used for auxiliary hold and power ground, respectively. These pins are not used on the HTS-0025 because that unit does not have a capability for accepting external capacitance in parallel with the hold capacitor; nor does it have as many ground connections. If circuits using the HTS-0025 are using those pin locations as tie points, it may preclude the possibility of substituting a model HTS-0010 unit in the circuit.

Current drive on the HTS-0010 is slightly less than it is on the HTS-0025 ($\pm$40mA vs. $\pm$50mA) but 3dB bandwidth is higher (60MHz vs. 30MHz).

The user of the HTS-0010 can reasonably expect higher speeds because of improvements in aperture uncertainty (5ps rms vs. 20ps rms); switching transient amplitude (15mV vs. 30mV); and acquisition time (10ns vs. 20ns for 1% settling). Noise levels in the track mode are also improved (40μV vs. 0.1mV maximum).

Voltage supplies for the internal amplifiers ($V_{CC}+$ and $V_{CC}-$) have a wider range on the HTS-0025 than they do on the HTS-0010 but $V_{CC}-$ can be connected to V_{EE} if desired, as explained elsewhere in the data sheet.

ORDERING INFORMATION

All versions of the HTS-0010 track/hold are housed in 24-pin metal dual in-line hybrid packages. For commercial applications operating over a temperature range of 0 to +70°C, specify model HTS-0010KD. For a temperature range of −55°C to +100°C, specify model HTS-0010SD. A temperature range of −55°C to +100°C and processing to MIL-STD-883, Method 5008, are available in the model HTS-0010SD/883.

Mating individual pin sockets are available from AMP. Knockout end type are part number 6-330808-0; open end type are 6-330808-3.

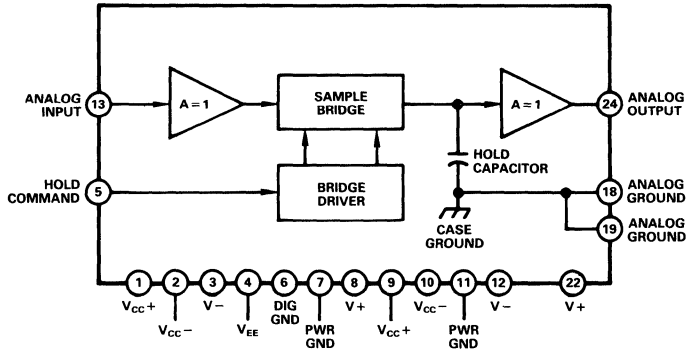
Ultrahigh Speed Hybrid Track-and-Hold Amplifier

HTS-0025

FEATURES
Aperture Jitter of 10ps
Acquisition Time 25ns
Output Current ±50mA
Slew Rate 250V/μs

APPLICATIONS
Data Acquisition Systems
Radar Systems
Instrumentation Systems
Medical Electronics
High Resolution Displays

HTS-0025 FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The Analog Devices HTS-0025 Track-and-Hold is another in Analog's range of track-and-hold (T/H) amplifiers useable in a variety of high-speed circuits. The HTS-0025 is part of a line of devices which offers designers the industry's widest range of track-and-hold and sample-and-hold units.

Design concepts used in the HTS-0025 T/H have made it the standard of comparison for high-speed circuits of this type. A dc-coupled Schottky diode bridge is driven by a high-impedance buffer amplifier and followed by a low impedance output amplifier. This achieves the best possible combination of speed and drive capabilities.

The pinouts of the HTS-0025 are similar to the HTS-0010 Track-and-Hold, so designers can select either the HTS-0025 or HTS-0010 for their particular applications. This kind of flexibility makes it possible to choose those parameters which are optimum for each application.

All models of the HTS-0025 are housed in a standard 24-pin metal DIP. The unit operating over a temperature range of 0 to +70°C is HTS-0025; the unit for a range of −55°C to +100°C is HTS-0025M.

SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

Parameter	Units	HTS-0025	HTS-0025M
ANALOG INPUT			
Voltage Range			
For Rated Performance	V p-p	2	*
Maximum Without Damage	V	±4	*
Impedance	Ω	10^{10}	*
Capacitance	pF max	7	*
Bias Current	nA max	15	*
DIGITAL INPUT (ECL Compatible)			
Mode Control			
Hold Command Input			
"0" = Track	V	−1.5 to −1.8	*
"1" = Hold[1]	V	−0.8 to −1.1	*
ANALOG OUTPUT			
Current (Not Short Circuit Protected)	mA max	±50	*
Impedance	Ω(max)	3 (10)	*
Noise in Track Mode			
@ 5.0MHz Bandwidth	mV rms max	0.1	*
DC ACCURACY/STABILITY (FS = Full Scale)			
Gain (No Load)	V/V (min)	0.97 (0.92)	*
Gain Nonlinearity; 2V FS Input	% max	0.1	*
Gain Nonlinearity; 1V FS Input	% max	0.01	*
Gain Temperature Coefficient	ppm/°C (max)	30 (40)	*
Output Offset Voltage	mV (max)	±5 (±20)	*
(Track Mode)			
vs. Temperature	μV/°C (max)	100 (150)	200 (300)
TRACK (SAMPLE) MODE DYNAMICS			
Frequency Response			
Full Power Bandwidth	MHz min	20	15
Small Signal (−3dB) Bandwidth	MHz min	30	20
Slew Rate	V/μs (min)	250 (140)	250 (120)
Harmonic Distortion (Track Mode;			
4MHz, 2V p-p Input)			
R_L = 1kΩ	dB max	−68	*
R_L = 500Ω	dB max	−65	*
R_L = 200Ω	dB max	−64	*
R_L = 75Ω	dB max	−50	*
TRACK (SAMPLE)-TO-HOLD SWITCHING			
Effective Aperture Delay Time[2]	ns	5	*
Aperture Uncertainty (Jitter)	ps (rms) max	10	*
Offset Step (Pedestal)	mV (max)	±5 (±20)	*
Sensitivity to Temperature	μV/°C max	100	150
Sensitivity to −5.2V	mV/V max	30	*
Switch Delay Time	ns	5	*
Switching Transient			
Amplitude	mV (max)	25 (35)	*
Settling to 5mV	ns (max)	20 (30)	*
HOLD MODE DYNAMICS			
Droop Rate	mV/μs (max)	0 (0.8)	*
Variation with Temperature		Doubles/10°C Change	
Feedthrough Rejection			
(2V p-p Input)			
@ 1MHz	dB min	70	*
@ 10MHz	dB min	65	*
HOLD-TO-TRACK (SAMPLE) DYNAMICS[3]			
Acquisition Time (1V Step)			
to ±1%	ns (max)	20 (30)	20 (40)
to ±0.1%	ns (max)	25 (35)	25 (40)
Acquisition Time (2V Step)			
to ±1%	ns (max)	25 (35)	25 (40)
to ±0.1%	ns (max)	30 (40)	30 (45)
Switch Delay Time	ns	1.5	*
POWER REQUIREMENTS			
V+ (+15V ±0.5V)	mA max	45	*
V− (−15V ±0.5V)	mA max	45	*
V_{CC}+ (+5.0V to +15.5V)[4]	mA max	15	*
V_{CC}− (−5.0V to −15.5V)[4]	mA max	15	*
V_{EE} (−5.2V ±0.25)[4]	mA max	40	*
Power Dissipation[5]	W max	2.3	*
Power Supply Rejection Ratio[6]	mV/V max	18	*
(dc to 10kHz)			
TEMPERATURE RANGE			
Operating (Case)	°C	0 to +70	−55 to +100
Storage	°C	−55 to +125	*
THERMAL RESISTANCE[7]			
Junction to Air, θja (Free Air)	°C/W	42	*
Junction to Case, θjc	°C/W	12	*
MTBF[8]			
Mean Time Between Failures	Hours		3.45×10^5
PACKAGE OPTION[9]			
M-24A		HTS-0025	HTS-0025M

For applications assistance, call (919) 668-9511.

POWER SEQUENCE FOR HTS-0025 T/H

1. V_{CC}+ and V_{CC}− must be applied simultaneously with, or ahead of, V+ and V− 15-volt supplies.
2. If V_{CC}+ and V_{CC}− are present, either V+ or V− can be applied first.
3. Output goes to V_{CC}+ if V+ is applied first in presence of V_{CC}+ and V_{CC}−.
4. Output goes to V_{CC}− if V− is applied first in presence of V_{CC}+ and V_{CC}−.
5. Recommended procedure is to use a single switch between source of ac power and all power supplies connected to HTS-0025 T/H. Operation of that switch then applies all dc supplies to T/H, which is a preferred way to power up unit.

NOTES

[1] One ECL 10k Gate, no resistor; requires 1kΩ to −5.2V
[2] Effective Aperture Delay Time is delay between Hold strobe and held value of analog output, referenced to analog input (see text).
[3] For acquisition time measurements, R_L = 200Ω; C_L = 13pF.
[4] V_{CC}+ may be tied to V+; V_{CC}− may be tied to V− or V_{EE} with adequate bypass capacitors (see text).
[5] Maximum power shown based on V_{CC}+ = V+; V_{CC}− = V−. Power is reduced to 2.0W maximum with V_{CC}+ = +5V and V_{CC}− = −5V.
[6] Variations in V− (−15V) have greater effect on unit performance than variations in other supplies; PSRR shown is for V−.
[7] Maximum junction temperature is +150°C.
[8] Calculated using MIL-HNBK 217.
[9] See Section 14 for package outline information.

*Specifications same as HTS-0025.
Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION
1	$V_{CC}+$ (+5V TO +15.5V)
2	$V_{CC}-$ (−5V TO −15.5V)
3	V− (−15V)
4	V_{EE} (−5.2V)
5	HOLD COMMAND
6	DIGITAL GROUND
7	POWER GROUND
8	V+ (+15V)
9	$V_{CC}+$ (+5V TO +15.5V)
10	$V_{CC}-$ (−5V TO −15.5V)
11	POWER GROUND
12	V− (−15V)
13	ANALOG INPUT
14	N/A
15	N/A
16	N/A
17	N/A
18	ANALOG GROUND
19	ANALOG GROUND
20	N/A
21	N/A
22	V+ (+15V)
23	N/A
24	ANALOG OUTPUT

POWER GROUND (PINS 7 AND 11), ANALOG GROUND (PINS 18 AND 19), AND DIGITAL GROUND (PIN 6) MUST BE CONNECTED TOGETHER AND TO A LOW-IMPEDANCE GROUND FOR PROPER OPERATION. MAKE CONNECTIONS AS CLOSE TO DEVICE AS POSSIBLE. HYBRID CASE IS CONNECTED TO ANALOG GROUND INTERNALLY.

6

Applications

One of the main uses for Track-and-Hold (T/H) units is ahead of analog-to-digital (A/D) converters to allow digitizing signals with bandwidths higher than the A/D can handle by itself. The use of an appropriate T/H allows the converter to become a true "Nyquist converter", i.e., capable of digitizing analog signals whose maximum bandwidth is one-half the encoding rate.

The characteristics of the HTS-0025 T/H make it useful in multiple other applications besides this "standard" use of devices of this kind. It can be used in sample and hold circuits, peak holding applications, simultaneous sampling A/Ds (with appropriate analog multiplexing), and for many other data processing needs.

Refer to Figure 1, HTS-0025 Interconnection Diagram.

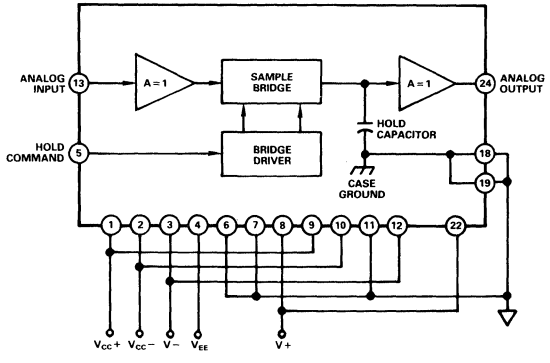


Figure 1. HTS-0025 Interconnection Diagram

Bypass capacitors are used internally on all power supply leads on the HTS-0025 Track-and-Hold. External bypassing of all power supplies with 0.01μF–0.1μF ceramics will help performance. In addition, electrolytic capacitors of 10-22 microfarads on each supply will also enhance the HTS-0025's operation.

A massive ground plane, careful component layout, and physically separating analog and digital signals are among the other considerations which can have major effects in improving the high-speed characteristics of the HTS-0025 Track-and-Hold.

As shown, supply voltages must be applied to all pins for which they are designated; it is extremely important to connect all grounds together, and to a solid, low-impedance ground plane as close to the hybrid as physically possible.

The five different voltages shown are the voltages used in final test and calibration, and are the recommended voltages for best performance; minor variations are possible.

For best performance, amplifier supplies, $V_{CC}-$ and $V_{CC}+$ should be equal and opposite. The ECL logic supply (V_{EE} = −5.2V) can be used also for $V_{CC}-$; if it is, bypass capacitors should be used at each supply pin to decrease the possibility of logic switching noise introducing extraneous signals.

TRACK-AND-HOLD MODE

When operated in the "track" mode, the HTS-0025 T/H functions as a buffer amplifier, following all changes in analog input as they occur. The user selects the point at which digitizing is to be done by applying an external ECL-compatible HOLD COMMAND to Pin 5.

Refer to Figure 2, Track/Hold Waveforms.

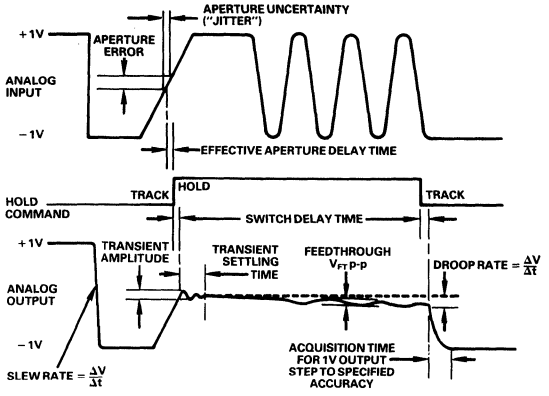


Figure 2. Track/Hold Waveforms

A varying, ideal analog input is shown at the top of Figure 2 for purposes of illustrating the response of the HTS-0025 to various types of inputs. This method of presentation shows many of the critical, and sometimes confusing, parameters of high-speed track-and-hold devices.

In the track mode, the response of the HTS-0025 is limited primarily by the slew rate characteristics of the device. As a result, the analog output is a faithful reproduction of the input as long as the highest frequency component of the input signal does not exceed the bandwidth of the unit.

The analog output shown on the bottom of Figure 2 tracks the input until a HOLD COMMAND is applied to Pin 5. When this pulse arrives, the sample bridge of the HTS-0025 disconnects the hold capacitor from the input. The short, but finite, interval required for this action is called aperture time (t_{sa}).

Other delay intervals combine with aperture time. One is delay in the hold command caused by propagation delay in the bridge driver; for purposes of discussion, this is a digital delay because it is the time required for logic switching to occur. Another is propagation delay through the input buffer amplifier, which is an analog delay because it affects the analog input signal being applied to the hold capacitor (see HTS-0025 Block Diagram).

Each of these three components is critical in the design of track-and-hold circuits, but user concern is limited only to their combined effect. The combination is specified here as Effective Aperture Delay Time and is defined as the interval between the leading edge of the hold command and that instant when the input signal is equal to the held value.

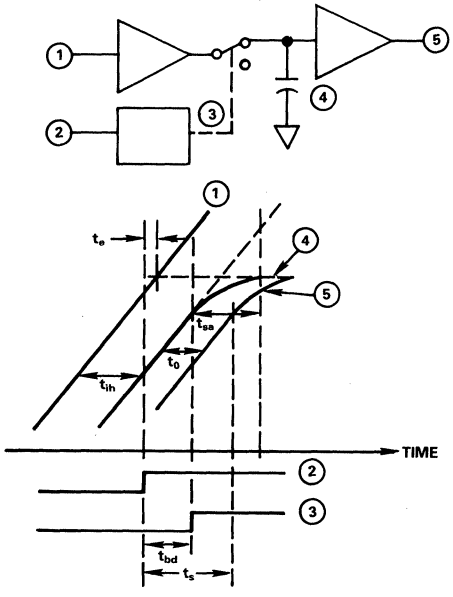
Additional details on the timing intervals in T/H circuits are shown in Figure 3.

The model T/H shown at the top of Figure 3 contains the basic elements of the HTS-0025, shown in their simplest form. The lower portion of the figure calls out multiple intervals of incremental time involved in switching from "track" to "hold" but no attempt is made to assign numerical values to them. Their definitions are intended solely to help understand the theory of T/H operation.

Effective aperture delay time (t_e) is digital delay plus averaging of the switch delay, minus analog delay. Depending on the comparative lengths of these combined delays, the value of t_e can be zero, positive, or negative.

The specification for Effective Aperture Delay Time is a more useful measurement for assessing T/H performance than aperture time because it includes all three of the components which have an effect on how quickly the device can make the change from the track mode to the hold mode.

In normal operation, these time intervals become academic discussions since users of the T/H are more interested in when the held value has reached its steady state.



(1) ANALOG INPUT
(2) ENCODE COMMAND INPUT
(3) SWITCH CONTROL
(4) HOLD CAPACITOR
(5) ANALOG OUTPUT

t_{ih} = ANALOG DELAY INPUT TO HOLD CAPACITOR = (DELAY FROM (1) TO (4))

t_{bd} = DIGITAL DELAY THROUGH BRIDGE DRIVER (DELAY (2) TO (3)).

t_{sa} = APERTURE TIME OF SWITCH

t_e = EFFECTIVE APERTURE DELAY TIME = $t_{bd} + \frac{t_{sa}}{2} - t_{ih}$ (DELAY (2) TO (1)).

t_s = SWITCH DELAY TIME = $t_{bd} + t_o$ (DELAY (2) TO (5)).

t_o = OUTPUT BUFFER DELAY (DELAY (4) TO (5))

Figure 3. T/H Timing Intervals

The waveforms in Figure 3 are idealized and based on an analog input which has a constant dV/dt. Other phenomena which are involved, such as transients, "jitter," etc. are illustrated in Figure 2.

Aperture uncertainty, or "jitter," is the result of noise signals of various kinds which modulate the phase of the hold command. This jitter shows up as a sample-to-sample variation in the value of the analog signal which is being "frozen".

Aperture uncertainty manifests itself as an aperture error, as shown in Figure 2. The amplitude of the error is related to the dV/dt of the analog input. For any given value of aperture uncertainty, aperture error will increase as the input dV/dt increases.

The design of the HTS-0025 insures that effective aperture delay time is within its specification from unit to unit; and is also repeatable from one "hold" command to the next within any unit. Therefore, it should not be regarded as an error source the way aperture uncertainty is. Effective aperture delay time can be compensated with system timing which correctly establishes the beginning of the hold period.

A switching transient appears in the analog output as a result of the transition from "track" to "hold." The Specifications table includes the maximum amplitude and duration of this transient; and also includes information on the switch delay time which precedes it. The held output is settled to within 5mV 20-25ns after the leading edge of the hold signal.

Feedthrough rejection is a measure of the amount of leakage from input to output during the hold interval after the HTS-0025 has settled to its specified accuracy. High feedthrough rejection is important because it assures no errors will be introduced during the conversion interval of the converter used at the output of the T/H.

In the illustration, V_{FT} is the small amount of "ripple" voltage on the held value of analog output. The ratio of output feedthrough to input signal is measured in dB and is equal to:

$$20 \log \left[\frac{V_{FT\ p\text{-}p}}{V_{IN\ p\text{-}p}} \right]$$

As shown, droop is that amount of change in the analog output which occurs during the hold interval.

Switch delay time shown in Figure 2 is the interval between the edges of the hold command and the start of movements in the analog output. This delay occurs at both the beginning and the end of the hold interval and is primarily the result of propagation delay through the output buffer amplifier.

Acquisition time is the time required for the output of the T/H to reacquire and begin accurate tracking of the analog input after the T/H has returned to the "track" mode. The acquisition time "clock" starts when the output begins moving and stops when the output has settled to its specified accuracy. As might be expected, longer acquisition times are required for larger signals and/or greater accuracy.

High slew rates are also important during acquisition time, but the desire for speed must be tempered with practical considerations. If the design of the unit achieves only speed without regard for overshoot, the acquisition time will be lengthened. Excessive "ringing" around the signal being acquired precludes applying successive hold commands at MHz update rates.

SAMPLE-AND-HOLD (S/H) MODE

Although generally used in the track-and-hold mode, the HTS-0025 can also be used as a sample-and-hold device for applications where this capability is needed.

The operation of the unit is essentially a "mirror" of the T/H operation, in that the output is usually in the "hold" mode but is switched to the "sample" (track) mode for brief intervals.

The width of the sample pulse which is used will be based on factors which are different for each application. Basically, the user establishes the width of this pulse by taking into account:

1. The acquisition time of the HTS-0025.
2. The desired accuracy of the sampled output.
3. The maximum amount of change which has occurred since the preceding sample.

This latter phenomenon is illustrated in Figure 4 Sample/Hold Operation.

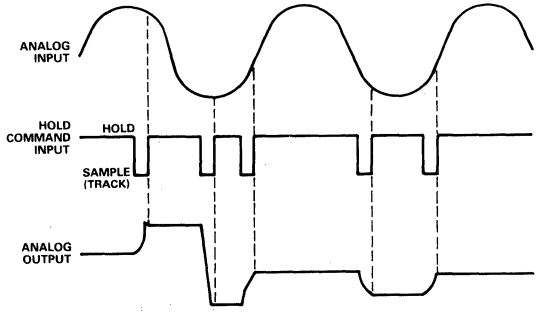


Figure 4. Sample/Hold Operation

When operating as a S/H, the signal applied to the HOLD COMMAND input (Pin 5) is usually a digital logic "1" which holds the HTS-0025 output at the input value present at the time of the sample/hold pulse.

Figure 4 shows asynchronous pulses applied to cause the output to reslew to new values. The trailing edge establishes the sample (track) mode; the leading edge returns the output to "hold".

In Figure 4, the analog input applied to the unit has changed drastically between the first and second sample (track) pulses. Smaller differences in the input values are present at the times of the second and third pulses. These differences in input show up as differences in the amount of movement of the analog output.

The acquisition time of the HTS-0025 makes it extremely attractive for sample-hold applications because of its ability to acquire new output values quickly. This characteristic of the device allows the use of a narrow sample pulse and an inherently faster sample rate, limited only by the factors enumerated earlier.

Refer to Figure 5 Settling Accuracy vs. Acquisition Time.

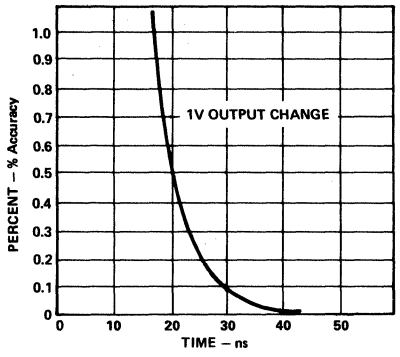


Figure 5. Settling Accuracy vs. Acquisition Time

This graph illustrates that closer accuracies require correspondingly longer amounts of time to acquire the signal. As shown, the accuracy/time relationship approaches an asymptotic curve, rather than being a linear function.

Another point to consider in Figure 5 is the illustrated output change is for a 1V change. If the output is required to change less than one volt (as it is between the second and third pulses in Figure 4, for example), the amount of time required to acquire the new value will be less than that shown.

When using the HTS-0025 or any other high-speed track-and-hold in the real world of data acquisition for fast-changing signals, the line between the device operating as a T/H or a S/H tends to "blur."

The designer using it as a T/H ahead of an A/D converter will generally vary the amount of "hold" time to obtain optimum operation for his particular application. When that performance is achieved, the HTS-0025 may, in the strictest sense of the word, be operating as a sample-and-hold. But it is useful to regard the two modes of operation separately when discussing the theory of operation of the unit.

ORDERING INFORMATION

All versions of the HTS-0025 track/hold are housed in 24-pin metal dual in-line hybrid packages. For commercial applications operating over a temperature range of 0 to +70°C, specify model HTS-0025. For a temperature range of −55°C to +100°C, specify model HTS-0025M. A temperature range of −55°C to +100°C and processing to MIL-STD-883, Method 5008, are available in the model HTS-0025MB.

Mating individual pin sockets are available from AMP. Knockout end type are part number 6-330808-0; open end type are 6-330808-3.

Typical HTS-0025 Operation

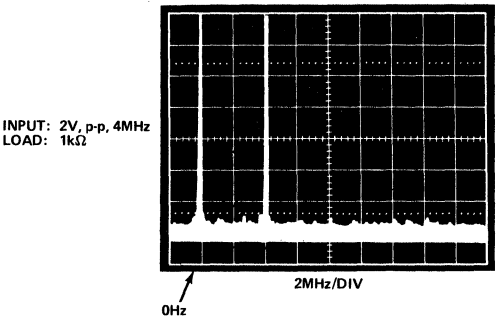


Figure 6a. Harmonic Distortion – Track Mode

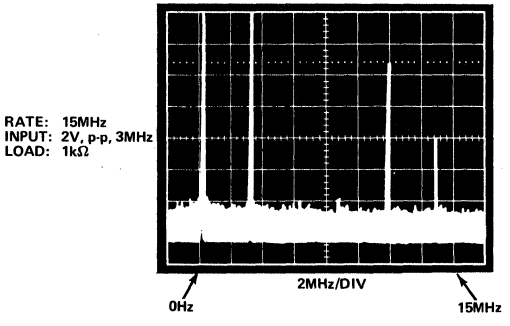


Figure 6b. Frequency Domain Outputs

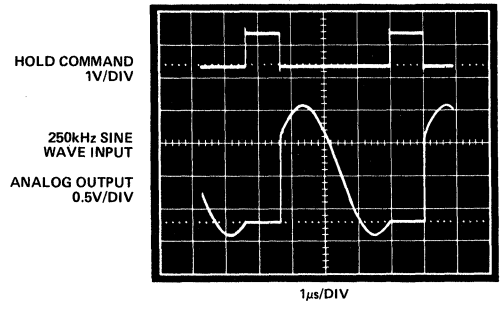


Figure 6c. Track/Hold Operation

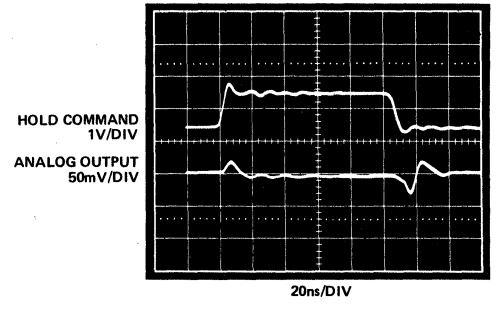


Figure 6d. Expanded View of Output Signal Showing Switching Transients and Pedestal with dc Input

CMOS Switches & Multiplexers
Contents

Selection Guide
Analog Switches & Multiplexers

CMOS SWITCHES

Model	Function	Leakage Current nA max	R_{ON} Ω max	Latched	Package Options[1]	Temp Range[2]	Page	Comments
*ADG201HS	Quad SPST	1	50		E, N, P, Q, R	C, I, M	7–29	CMOS, High-Speed Quad Switch. 44 V Supply Maximum Ratings
ADG201A	Quad SPST	1–2	90		E, N, P, Q, R	C, I, M	7–25	CMOS, 44 V Supply Maximum Ratings
ADG202A	Quad SPST	1–2	90		E, N, P, Q, R	C, I, M	7–25	CMOS, 44 V Supply Maximum Ratings
ADG221	Quad SPST	1–2	90	X	E, N, P, Q, R	C, I, M	7–41	CMOS, Latched Input, 44 V Supply Maximum Ratings
ADG222	Quad SPST	1–2	90	X	E, N, P, Q	C, I, M	7–41	CMOS, Latched Input, 44 V Supply Maximum Ratings
AD7510DI	Quad SPST	5–10	100		E, N, P, Q	C, M	7–9	DiCMOS, Dielectrically Isolated
AD7511DI	Quad SPST	5–10	100		E, N, P, Q	C, M	7–9	DiCMOS, Dielectrically Isolated
AD7590DI	Quad SPST	5	90	X	E, N, P, Q	C, I, M	7–13	DiCMOS, Latched, Dielectrically Isolated
AD7591DI	Quad SPST	5	90	X	E, N, P, Q	C, I, M	7–13	DiCMOS, Latched, Dielectrically Isolated
ADG211A	Quad SPST	5	115		N, P, R	C	7–37	CMOS, Low Cost, 44 V Supply Maximum Ratings
ADG212A	Quad SPST	5	115		N, P	C	7–37	CMOS, Low Cost, 44 V Supply Maximum Ratings
AD7512DI	Dual SPDT	5–10	100		E, N, P, Q	C, M	7–9	DiCMOS, Dielectrically Isolated
AD7592DI	Dual SPDT	5	90	X	E, N, P, Q	C, M	7–13	DiCMOS, Latched, Dielectrically Isolated

ANALOG CMOS MULTIPLEXERS

Model	Function	Leakage Current nA max	R_{ON} Ω max	Latched	Package Options[1]	Temp Range[2]	Page	Comments
ADG506A	16:1	1	280		E, N, P, Q	C, I, M	7–45	Superior Second Source to DG506A
ADG526A	16:1	1	280	X	E, N, P, Q	C, I, M	7–57	Superior Second Source to DG526A
ADG507A	Dual 8:1	1	280		E, N, P, Q	C, I, M	7–45	Superior Second Source to DG507A
ADG527A	Dual 8:1	1	280	X	E, N, P, Q	C, I, M	7–57	Superior Second Source to DG527A
ADG508A	8:1	1	300		E, N, P, Q, R	C, I, M	7–53	Superior Second Source to DG508A
ADG528A	8:1	1	300	X	E, N, P, Q, R	C, I, M	7–65	Superior Second Source to DG528A
AD7501	8:1	1-5	300		E, N, Q	C, M	7–7	
AD7503	8:1	1–5	300		E, N, Q	C, M	7–7	
ADG509A	Dual 4:1	1	300		E, N, P, Q, R	C, I, M	7–53	Superior Second Source to DG509A
ADG529A	Dual 4:1	1	300	X	E, N, P, Q, R	C, I, M	7–65	Superior Second Source to DG529S
AD7502	Dual 4:1	1–5	300		E, N, Q	C, M	7–7	

VIDEO MULTIPLEXERS

Model	Function	Full Power BW MHz min	Crosstalk Rejection F = 10 MHz dB	Package Options[1]	Temp Range[2]	Page	Comments
***AD9300**	**4:1**	**30**	**75**	**E, Q**	**C, M**	**7–17**	**Wideband Video Mux**

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

Orientation
CMOS Switches & Multiplexers

Analog Devices offers a complete line of monolithic CMOS analog multiplexers and switches, which utilize a high-breakdown CMOS process, in conjunction with a double-layer interconnect for high density. Both 8- and 16-channel multiplexers are available in one-line and two-line (4- and 8-channel differential) versions. The switches are dielectrically isolated duals and quads available in a variety of contact forms. Both direct and inverted logic options are available for the most popular types. The popular AD7510/11/12DI (quad SPST/dual SPDT), which utilize dielectric isolation, are latchup-proof and can withstand overrange to ±25V beyond the supplies.

CMOS switches have extremely low quiescent power dissipation, require little drive or supply current while switching and are low in cost. Their R_{ON} is low and is, to a first order, independent of applied voltage; in the off condition, leakage is quite small, both across the gate and to the drive and supply circuits. Most types respond to TTL/DTL as well as CMOS logic.

Definitions for terminal nomenclature used in the data sheets are given below, and a summary of device functions appears on the preceding page. General information on the nature of CMOS, its advantages, its applications and its protection, is to be found in the *Analog CMOS Switches and Multiplexers*, available from Analog Devices upon request.

MULTIPLEXER TERMINOLOGY

R_{ON}: Ohmic resistance between the output and an addressed input.

R_{ON} vs. Temperature: R_{ON} drift over the temperature range.

ΔR_{ON} between Switches: Difference between the R_{ON}s of any two switches.

R_{ON} vs. Temperature between Switches: Difference between the R_{ON} drifts of any two switches.

I_S: Current at any switch input, S1 through S_N. This is a leakage current when the switch is open.

I_{OUT}: Current at the output. This is a leakage current when all switches are open.

$I_{OUT} - I_S$: Difference between the current going into terminal "S" and the current going out of terminal "out" when terminal "S" is addressed.

V_{INL}: Digital threshold voltage for the low state.

V_{INH}: Digital threshold voltage for the high state.

C_S: Capacitance between any open terminal "S" and ground.

C_{OUT}: Capacitance between the output terminal and ground with all switches open.

C_{S-OUT}: Capacitance between any open terminal "S" and the output terminal.

C_{SS}: Capacitance between any two "S" terminals.

$t_{TRANSITION}$: Delay time when switching from one address state to another.

t_{OPEN}: "OFF" time of both switches when switching from one address state to another.

t_{ON}(En): Delay time between the 50% points of the enable input and the switch "ON" condition.

t_{OFF}(En): Delay time between the 50% points of the enable input and the switch "OFF" condition.

V_{DD}: Most positive voltage supply.

V_{SS}: Most negative voltage supply.

I_{DD}: Positive supply current.

I_{SS}: Negative supply current.

SWITCH TERMINOLOGY

R_{DS}: Ohmic resistance between terminals D and S.

$I_D(I_S)$: Current at terminals D or S. This is a leakage current when the switch is OFF.

I_{DS}: Current flowing through the closed switch.

$I_D - I_S$: Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)

$V_D(V_S)$: Analog voltage on terminal D (S).

$C_S(C_D)$: Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)

C_{DS}: Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)

$C_{DD}(C_{SS})$: Capacitance between terminals D (S) of any 2 switches. (This will determine the cross coupling between switches vs. frequency.)

t_{ON}: Delay time between the 50% points of the digital input and switch "ON" condition.

t_{OFF}: Delay time between the 50% points of the digital input and switch "OFF" condition.

V_{INL}: Threshold voltage for the low state.

V_{INH}: Threshold voltage for the high state.

$I_{INL}(I_{INH})$: Input current of the digital input.

C_{IN}: Input capacitance to ground of the digital input.

V_{DD}: Most positive voltage supply.

V_{SS}: Most negative voltage supply.

I_{DD}: Positive supply current.

I_{SS}: Negative supply current.

CMOS
4/8 Channel Analog Multiplexers
AD7501/AD7502/AD7503

FEATURES
DTL/TTL/CMOS Direct Interface
Power Dissipation: 30μW
R_{ON}: 170Ω
Standard 16-Pin DIPs and 20-Terminal Surface Mount Packages

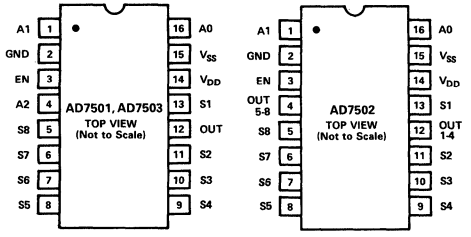
GENERAL DESCRIPTION

The AD7501 and AD7503 are monolithic CMOS, 8-channel analog multiplexers which switches one of 8 inputs to a common output depending on the state of three binary address lines and an "enable" input. The AD7503 is identical to the AD7501 except its "enable" logic is inverted. All digital inputs are TTL/DTL and CMOS logic compatible.

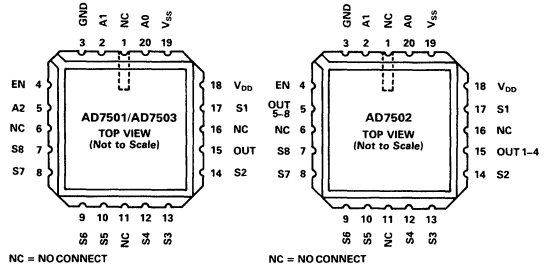
The AD7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of 2 binary address inputs and an "enable", it switches two output buses to two of 8 inputs.

PIN CONFIGURATIONS

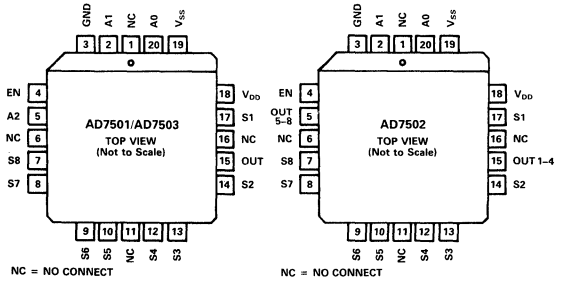
DIP



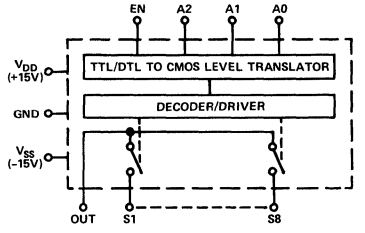
LCCC



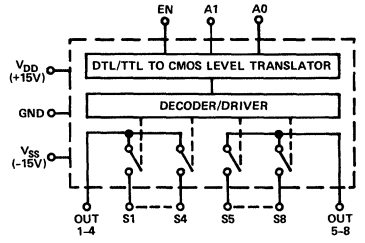
PLCC



AD7501/AD7503 FUNCTIONAL BLOCK DIAGRAM



AD7502 FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION[1]

Temperature Range and Package Options[2]		
0 to +70°C	−25°C to +85°C	−55°C to +125°C
Plastic DIP (N-16)	Hermetic (Q-16)	Hermetic (Q-16)
AD7501JN	AD7501JQ	AD7501SQ
AD7501KN	AD7501KQ	AD7502SQ
AD7502JN	AD7502JQ	AD7503SQ
AD7502KN	AD7502KQ	
AD7503JN	AD7503JQ	
AD7503KN	AD7503KQ	
PLCC[3] (P-20A)		LCCC[4] (E-20A)
AD7501JP		AD7501SE
AD7501KP		AD7501SE
AD7502JP		AD7503SE
AD7502KP		
AD7503JP		
AD7503KP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. See Analog Devices' 1987 Military Databook for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

TRUTH TABLES

AD7501				
A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

AD7502			
A_1	A_0	E_N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

AD7503				
A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

PARAMETER	VERSION[1]	SWITCH CONDITION	@25°C AD7501, AD7503	@25°C AD7502	OVER SPECIFIED TEMP. RANGE AD7501, AD7503	OVER SPECIFIED TEMP. RANGE AD7502	TEST CONDITIONS
ANALOG SWITCH							
R_{ON}	All	ON	170Ω typ, 300Ω max	*			−10V ≤ V_S ≤ +10V
R_{ON} vs. V_S	All	ON	20% typ	*			I_S = 1.0mA
R_{ON} vs. Temperature	All	ON	0.5%/°C typ	*			V_S = 0V, I_S = 1.0mA
ΔR_{ON} Between Switches	All	ON	4% typ	*			
R_{ON} vs. Temperature Between Switches	All	ON	±0.01%/°C	*			
I_S	J, K	OFF	0.2nA typ, 2nA max	*	50nA max	*	V_S = −10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = −10V
	S	OFF	0.5nA max	*	50nA max	*	
I_{OUT}	J, K	OFF	1nA typ, 10nA max	0.6nA typ, 5nA max	250nA max	125nA max	V_S = −10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = −10V
	S	OFF	5nA max	3nA max	250nA max	125nA max	AD7501/02: Enable LOW AD7503: Enable HIGH
$\lvert I_{OUT} - I_S \rvert$	J, K	ON	12nA max	7nA max	300nA max	175nA max	V_S = 0
	S	ON	5.5nA max	3.5nA max	300nA max	175nA max	
DIGITAL CONTROL							
V_{INL}	All				0.8V max	*	
V_{INH}	J				3.0V min	*	Note 2
	K, S				2.4V min	*	
I_{INL} or I_{INH}	All		10nA typ	*			
C_{IN}	All		3pF typ	*			
DYNAMIC CHARACTERISTICS							
t_{ON}	All		0.8μs typ	*			V_{IN} = 0 to +5.0V (See Test Circuit 2)
t_{OFF}	All		0.8μs typ	*			
C_S	All	OFF	5pF typ	*			
C_{OUT}	All	OFF	30pF typ	15pF typ			
C_{S-OUT}	All	OFF	0.5pF typ	*			
C_{SS} Between Any Two Switches	All	OFF	0.5pF typ	*			
POWER SUPPLY							
I_{DD}	All		500μA max	*	500μA max	*	All Digital Inputs Low
I_{SS}	All		500μA max	*	500μA max	*	
I_{DD}	All		800μA max	*	800μA max	*	All Digital Inputs High
I_{SS}	All		800μA max	*	800μA max	*	

NOTES
*Same specifications as AD7501 and AD7503.
[1] JN, KN, JP, KP versions specified for 0 to +70°C; JQ, KQ versions for -25°C to +85°C; and SQ, SE versions for -55°C to +125°C.
[2] A pullup resistor, typically 1-2kΩ is required to make the AD7501J, AD7502J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . −17V
V Between Any Switch Terminals (see Note 1) 25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Overvoltage at V_{OUT} (V_S) . . . . . V_{SS}, V_{DD}
Switch Current (I_S, Continuous One Channel) 20mA
Switch Current (I_S, Surge One Channel)
1ms Duration, 10% Duty Cycle 35mA
Power Dissipation (Any Package)
Up to +50°C 1000mW
Derates above +50°C by . . . . . 10mW/°C
Operating Temperature
Commercial (JN, KN, JP, KP Versions) . . . . 0 to +70°C
Industrial (JQ, KQ Versions) . . . . . −25°C to +85°C
Extended (SQ, SE Versions) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

CAUTION

1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control linputs are diode protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ANALOG DEVICES

DI CMOS Protected Analog Switches

AD7510DI/AD7511DI/AD7512DI

FEATURES
Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Silicon-Nitride Passivated
Monolithic Dielectrically Isolated CMOS
Standard 14-/16-Pin DIPs and 20-Terminal Surface Mount Packages

GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (500pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged either in a 14-pin DIP or a 20-terminal surface mount package.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

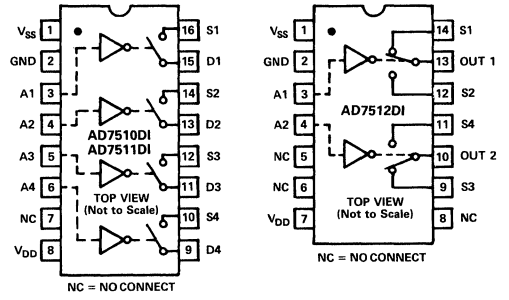
ORDERING INFORMATION[1]

Temperature Range and Package[2]		
0 to +70°C	−25°C to +85°C	−55°C to +125°C
Plastic DIP[3]	**Hermetic[4]**	**Hermetic[4]**
AD7510DIJN	AD7510DIJQ	AD7510DISQ
AD7510DIKN	AD7510DIKQ	AD7510DITQ
AD7511DIJN	AD7511DIJQ	AD7511DITQ
AD7511DIKN	AD7511DIKQ	AD7512DISQ
AD7512DIJN	AD7512DIJQ	AD7512DITQ
AD7512DIKN	AD7512DIKQ	
PLCC[5] (P-20A)		**LCCC[6] (E-20A)**
AD7510DIJP		AD7510DISE
AD7510DIKP		AD7511DISE
AD7511DIJP		AD7511DITE
AD7511DIKP		AD7512DISE
AD7512DIJP		AD7512DITE
AD7512DIKP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]For AD7510DIJN/KN and AD7511DIJN/KN package outline N-16; for AD7512DIJN/KN package outline N-14.
[4]For AD7510DIJQ/KQ/SQ and AD7511DIJQ/KQ/SQ/TQ package outline Q-16; for AD7512DIJQ/KQ/SQ/TQ package outline Q-14.
[5]PLCC: Plastic Leaded Chip Carrier.
[6]LCCC: Leadless Ceramic Chip Carrier.

AD7510DI/AD7511DI/AD7512DI FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS

DIP



CONTROL LOGIC

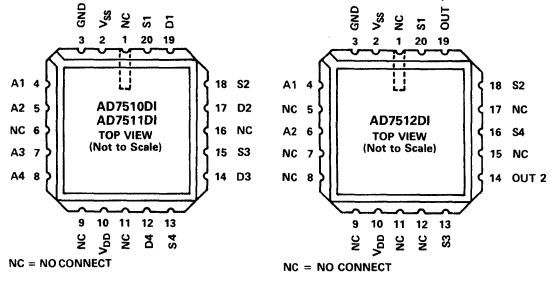
AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

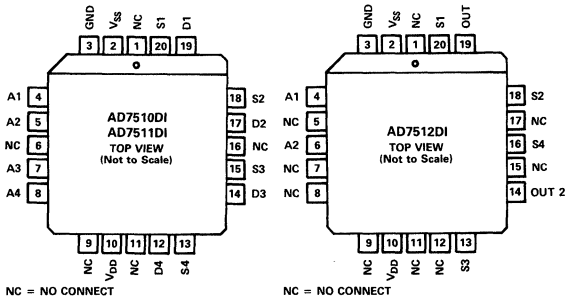
AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

PIN CONFIGURATIONS

LCCC



PLCC



SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

COMMERCIAL AND INDUSTRIAL VERSIONS (J, K)

PARAMETER	MODEL	VERSION	+25°C (N, P, Q, E)	0 to +70°C (N, P) -25°C to +85°C (Q)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	J, K	75Ω typ, 100Ω max	175Ω max	$-10V \leq V_D \leq +10V$
R_{ON} vs V_D (V_S)	All	J, K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	J, K	+0.5%/°C typ		
R_{ON} Match	All	J, K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S)$_{OFF}$[1]	All	J, K	0.5nA typ, 5nA max	500nA max	V_D = −10V, V_S = +10V and V_D = +10V, V_S = −10V
I_D (I_S)$_{ON}$[1]	All	J, K	10nA max		V_S = V_D = +10V V_S = V_D = −10V
I_{OUT}[1]	AD7512DI	J, K	15nA max	1500nA max	V_{S1} = V_{OUT} = ±10V, V_{S2} = ∓10V and V_{S2} = V_{OUT} = ±10V, V_{S1} = ∓10V
DIGITAL CONTROL					
V_{INL}[1]	All	J, K		0.8V max	
V_{INH}[1]	All	J		3.0V min	
	All	K		2.4V min	
C_{IN}	All	J, K	7pF typ		
I_{INH}[1]	All	J, K	10nA max		V_{IN} = V_{DD}
I_{INL}[1]	All	J, K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		V_{IN} = 0 to +3.0V
	AD7511DI	J, K	350ns typ		
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D)$_{OFF}$	All	J, K	8pF typ		V_D (V_S) = 0V
C_S (C_D)$_{ON}$	All	J, K	17pF typ		
C_{DS} (C_{S-OUT})	All	J, K	1pF typ		
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to −10V
POWER SUPPLY					
I_{DD}[1]	All	J, K	800μA max	800μA max	All digital inputs = V_{INH}
I_{SS}[1]	All	J, K	800μA max	800μA max	
I_{DD}[1]	All	J, K	500μA max	500μA max	All digital inputs = V_{INL}
I_{SS}[1]	All	J, K	500μA max	500μA max	
PACKAGE OPTIONS[2]					
Plastic (N-14)	AD7512DIJN/KN				
Plastic (N-16)	AD7510DIJN/KN				
	AD7511DIJN/KN				
Cerdip (Q-14)	AD7512DIJQ/KQ				
Cerdip (Q-16)	AD7510DIJQ/KQ				
	AD7511DIJQ/KQ				
PLCC (P-20A)	AD7510DIJP/KP				
	AD7511DIJP/KP				
	AD7512DIJP/KP				

NOTES
[1] 100% tested.
[2] See Section 14 for package outline information.

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

EXTENDED VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	S, T	100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ I_{DS} = 1mA
I_D $(I_S)_{OFF}$[1]	All	S, T	3nA max	200nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D $(I_S)ON$[1]	All	S, T	10		$V_S = V_D$ = +10V and $V_S = V_D$ = -10V
I_{OUT}[1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL}[1]	All	S, T		0.8V max	
V_{INH}[1,2]	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH}[1]	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL}[1]	All	S, T	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}[3]	AD7510DI	S,	1.0μs max		V_{IN} = 0 to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF}[3]	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}$[3]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD}[1]	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS}[1]	All	S, T		800μA max	
I_{DD}	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS}[1]	All	S, T		500μA max	
PACKAGE OPTIONS[4]					
Cerdip (Q-16)	AD7510DISQ				
	AD7511DISQ/TQ				
Cerdip (Q-14)	AD7512DISQ/TQ				
LCCC (E-20A)	AD7510DISE				
	AD7511DISE/TE				
	AD7512DISE/TE				

NOTES
[1] 100% tested.
[2] A pullup resistor, typically 1-2kΩ is required to make AD7511DISQ and AD7512DISQ TTL compatible.
[3] Guaranteed, not production tested.
[4] See Section 14 for package outline information.
Specifications subject to change without notice.

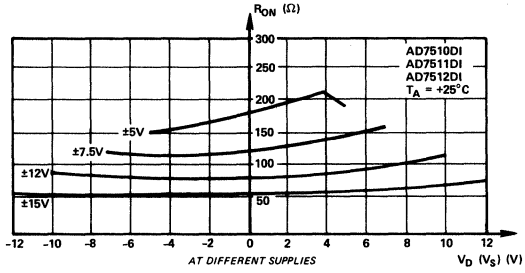
ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . -17V
Overvoltage at V_D (V_S)
(1 second surge) . . . . . V_{DD} +25V
or V_{SS} -25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} -20V
or 20mA, Whichever Occurs First
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . 0V to V_{DD} +0.3V
Power Dissipation (Any Package)
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

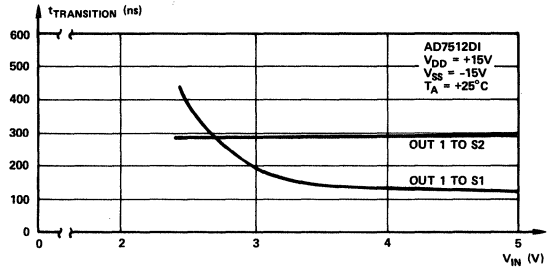
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature
Commercial (JN, KN, JP, KP Versions) . . . . 0 to +70°C
Industrial (JQ, KQ Versions) . . . . . -25°C to +85°C
Extended (SQ, TQ, SE, TE Versions) . . -55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

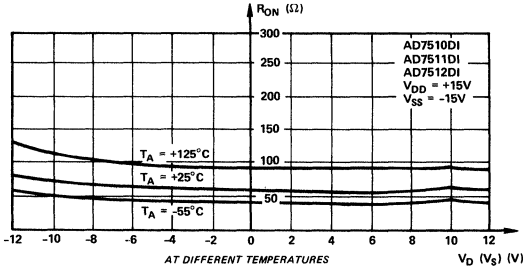
Typical Performance Characteristics



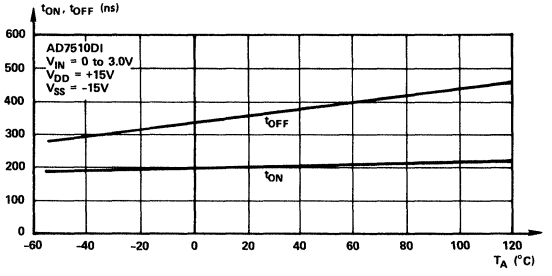
R_{ON} as a Function of V_D (V_S)



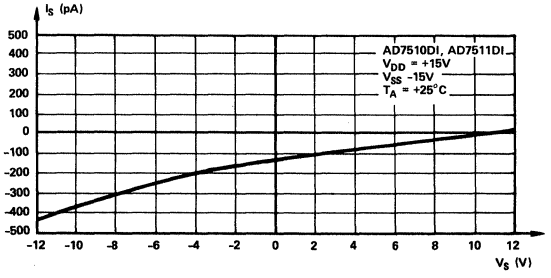
$t_{TRANSITION}$ as a Function of Digital Input Voltage



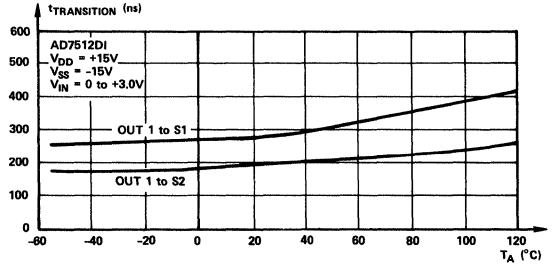
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature



I_S, $(I_D)_{OFF}$ vs V_S



$t_{TRANSITION}$ as a Function of Temperature

DI CMOS
Analog Switches with Data Latches

AD7590DI/AD7591DI/AD7592DI

FEATURES
SCR Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 60Ωtyp
Buffered Switch Logic
TTL, CMOS Compatible
Monolithic Dielectrically-Isolated CMOS
Pin Compatible with AD7510DI Series
Standard 14/16-Pin DIPs and 20-Terminal Surface Mount Packages

GENERAL DESCRIPTION

The AD7590DI, AD7591DI and AD7592DI are a family of protected (latch-proof) dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. Microprocessor interfacing is facilitated by the provision of on-chip data latches.

The AD7590DI and AD7591DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the switch control logic is inverted. The AD7592DI has two independent SPDT switches packaged in either a 14-pin DIP or a 20-terminal surface mount package.

ORDERING INFORMATION[1]

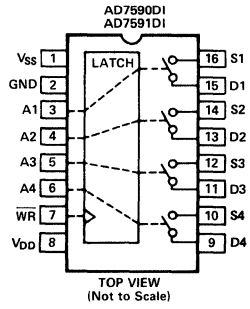
Temperature Range and Package Options[2]

0 to +70°C	−25°C to +85°C	−55°C to +125°C
Plastic DIP[3]	**Hermetic[4]**	**Hermetic[4]**
AD7590DIKN	AD7590DIBQ	AD7590DITQ
AD7591DIKN	AD7591DIBQ	AD7591DITQ
AD7592DIKN	AD7592DIBQ	AD7592DITQ
PLCC[5] (P-20A)		**LCCC[6] (E-20A)**
AD7590DIKP		AD7590DITE
AD7591DIKP		AD7591DITE
AD7592DIKP		AD7592DITE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]For AD7590DIKN and AD7591DIKN package outline N-16; for AD7592DIKN package outline N-14.
[4]For AD7590DIBQ/TQ and AD7591DIBQ/TQ package outline Q-16; for AD7592DIBQ/TQ package outline Q-14.
[5]PLCC: Plastic Leaded Chip Carrier.
[6]LCCC: Leadless Ceramic Chip Carrier.

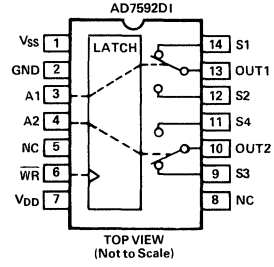
AD7590DI/AD7591/AD7592DI FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS FOR DIP

16-PIN DIP



TOP VIEW
(Not to Scale)

14-PIN DIP



TOP VIEW
(Not to Scale)

NC = NO CONNECT

CONTROL LOGIC ($\overline{WR}$ HELD LOW)

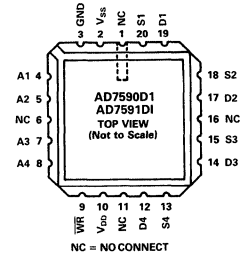
AD7590DI: Switch "ON" for Address "HIGH"

AD7591DI: Switch "ON" for Address "LOW"

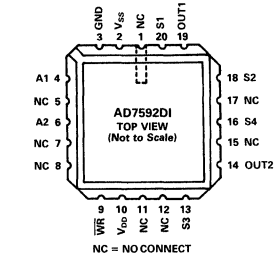
AD7592DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

PIN CONFIGURATIONS

LCCC

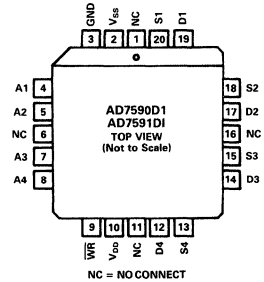


NC = NO CONNECT

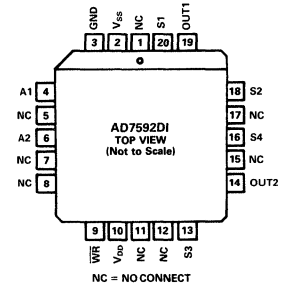


NC = NO CONNECT

PLCC



NC = NO CONNECT



NC = NO CONNECT

SPECIFICATIONS (V_{DD} = 15V, V_{SS} = −15V unless otherwise noted)

Parameter	Model	T_A = +25°C All Versions[1]	K, B Versions	T Version	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range	All	±10	±10	±10	Volts	
R_{ON}[2]	All	60			Ω typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA;
	All	90	120	150	Ω max	Test Circuit 1
R_{ON} Match[3]	All	2			Ω typ	V_S = 0, I_{DS} = 1mA
R_{ON} Match Drift[3]	All	0.01			Ω/°C typ	V_S = 0, I_{DS} = 1mA
I_D OFF[2]	AD7590DI	0.5			nA typ	Test Circuit 2
	AD7591DI	5	50	200	nA max	
I_S OFF[2]	All	0.5			nA typ	Test Circuits 2 & 3
		5	50	200	nA max	
I_D (I_S) ON[2]	All	0.5			nA typ	Test Circuit 4
		5	50	200	nA max	
I_{OUT}[2]	AD7592DI	1			nA typ	Test Circuit 3
		10	100	400	nA max	
C_S (C_D) OFF[4]	All	10			pF typ	
C_S (C_D) ON[4]	All	30			pF typ	
C_{DS} (C_{S-OUT})[4]	All	1			pF typ	
C_{DD} (C_{SS})[4]	All	0.5			pF typ	
C_{OUT}[4]	AD7592DI	40			pF typ	
DIGITAL CONTROL						
V_{INL}[2]	All	0.8	0.8	0.8	V max	
V_{INH}[2]	All	2.4	2.4	2.4	V min	
C_{IN}[4]	All	7	7	7	pF typ	
I_{INL} or I_{INH}[2,5]	All	1	1	1	μA max	V_{IN} = 0 or V_{DD}
DYNAMIC CHARACTERISTICS						
t_{ON}[3]	AD7590DI	250	380	380	ns max	Test Circuit 5
	AD7591DI	400	500	500	ns max	
t_{OFF}[3]	AD7590DI	400	500	500	ns max	Test Circuit 5
	AD7591DI	250	380	380	ns max	
$t_{TRANSITION}$[3]	AD7592DI	350	450	450	ns max	Test Circuit 6
Write Pulse-Width (t_{WR})[3]	All	250	300	400	ns min	See Figure 1
Address Setup Time (t_{AS})[3]	All	300	300	400	ns min	See Figure 1
Address Hold Time (t_{AH})[3]	All	20	30	40	ns min	See Figure 1
Off Isolation[4]						
(Analog Input to Analog Output)	All	−85			dB typ	A, $\overline{WR}$ = 0.8V; V_S = 10V (Pk-Pk); f = 1kHz, R_L = 10kΩ
Crosstalk[4]						
(Digital Input to Analog Output)	All	5			mV peak, typ	R_L = 1MΩ, C_L = 15pF; V_{INH} = 3V, V_{INL} = 0V; t_{RISE} = t_{FALL} = 20ns; $\overline{WR}$ held HIGH
Q_{INJ}[4]						
(Charge Injection)	All	55			pC typ	Test Circuit 7
POWER SUPPLY						
I_{DD}[2]	All	1	1.5	2	mA max	Digital Inputs = V_{INL} or V_{INH}
I_{SS}[2]	All	1	1	1	mA max	

NOTES

[1]Temperature Ranges as follows: K Version; 0 to +70°C
B Version; −25°C to +85°C
T Version; −55°C to +125°C

[2]100% tested.

[3]Guaranteed, not production tested.

[4]Typical values for information only, not subject to test.

[5]Inputs are MOS gates typical current less than 10nA.

Specifications subject to change without notice.

TIMING AND CONTROL SEQUENCE

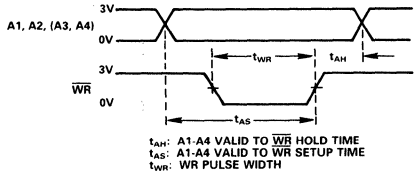


Figure 1. Timing and Control Sequence

TIMING AND CONTROL SEQUENCE

Figure 1 shows the timing sequence for latching the switch address inputs. The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the address inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

NOTE: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F$ = 20ns.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . −17V
Overvoltage at V_D (V_S), One Switch Only
(1sec surge) . . . . . V_{DD} +25V
or V_{SS} −25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} −20V
or 20mA, Whichever Occurs First
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . −0.3V to V_{DD} +0.3V

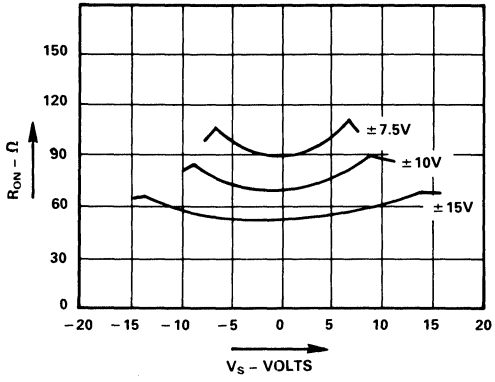
Power Dissipation (Any Package)
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature
Commercial (K Version) . . . . . 0 to +70°C
Industrial (B Version) . . . . . −25°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

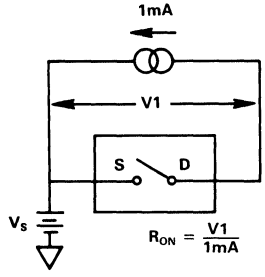
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Typical Performance Characteristics and Test Circuits

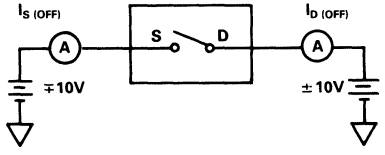


R_{ON} AS A FUNCTION OF V_D (V_S)
FOR DIFFERENT SUPPLY VOLTAGES

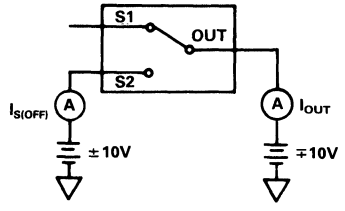
TEST CIRCUIT 1



TEST CIRCUIT 2
(AD7590DI, AD7591DI)

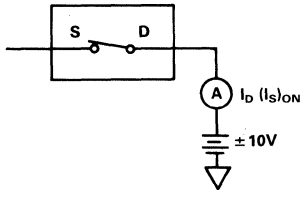


TEST CIRCUIT 3
(AD7592DI ONLY)

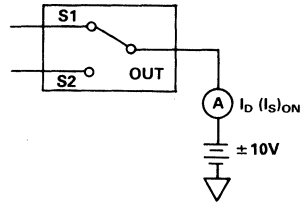


Typical Performance Characteristics and Test Circuits Cont'd

TEST CIRCUIT 4

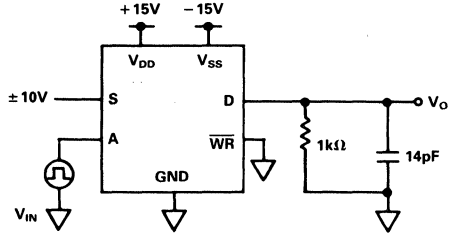


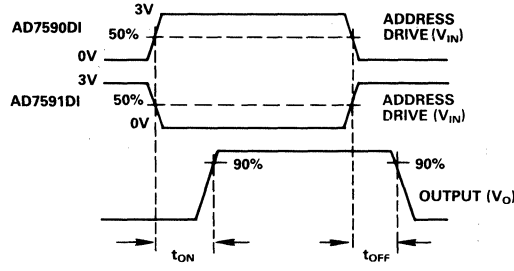
a. AD7590DI, AD7591DI



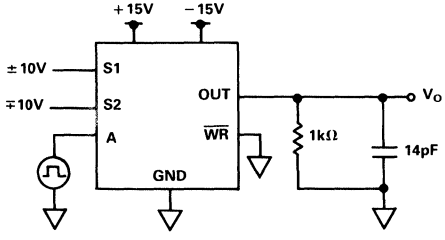
b. AD7592DI

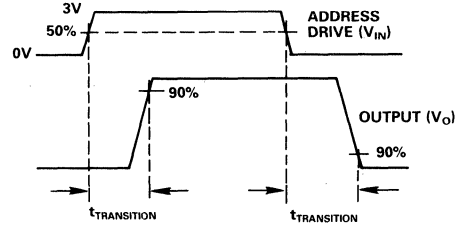
TEST CIRCUIT 5
SWITCHING TIME OF AD7590DI AND AD7591DI, t_{ON}, t_{OFF}



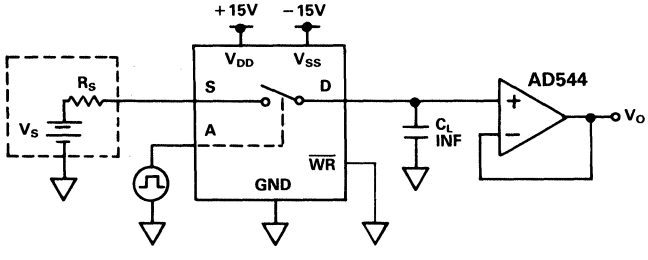


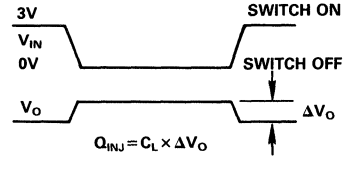
TEST CIRCUIT 6
SWITCHING TIME OF AD7592DI, $t_{TRANSITION}$





TEST CIRCUIT 7
CHARGE INJECTION





ANALOG DEVICES

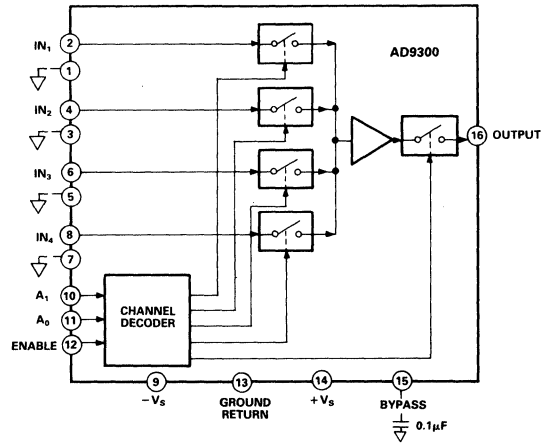
4 × 1 Wideband Video Multiplexer

AD9300

FEATURES
34MHz Full Power Bandwidth
±0.1dB Gain Flatness to 8MHz
75dB Crosstalk Rejection @ 10MHz
0.05°/0.05% Differential Phase/Gain
Cascadable for Switch Matrices

APPLICATIONS
Video Routing
Medical Imaging
Electro-Optics
ECM Systems
Radar Systems
Data Acquisition

AD9300 FUNCTIONAL BLOCK DIAGRAM
(Based on Cerdip)



GENERAL DESCRIPTION

The AD9300 is a monolithic high-speed video signal multiplexer useable in a wide variety of applications.

Its four channels of video input signals can be randomly switched at megahertz rates to the single output. In addition, multiple devices can be configured in either parallel or cascade arrangements to form switch matrices. This flexibility in using the AD9300 is possible because the output of the device is in a high-impedance state when the chip is not enabled; when the chip is enabled, the unit acts as a buffer with a high input impedance and low output impedance.

An advanced bipolar process provides fast, wideband switching capabilities while maintaining crosstalk rejection of 75dB at 10MHz. Full power bandwidth is a minimum 30MHz. The device can be operated from ± 10V to ± 15V power supplies.

The AD9300KQ is packaged in a 16-pin ceramic DIP, and the AD9300KP is packaged in a 20-pin PLCC; both are designed to operate over the commercial temperature range of 0 to +70°C. For military temperatures of −55°C to +125°C, order part number AD9300TQ, which is also a 16-pin ceramic DIP. In addition, the AD9300 is available in a 20-pin LCC as the model AD9300TE, which operates over a temperature range of −55°C to +125°C.

ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9300KQ	0 to +70°C	16-Pin Cerdip, Commercial	Q-16
AD9300TQ	−55°C to +125°C	16-Pin Cerdip, Military Temperature	Q-16
AD9300TE	−55°C to +125°C	20-Pin LCC, Military Temperature	E-20A
AD9300KP	0 to +70°C	20-Pin PLCC, Commercial	P-20A

*See Section 14 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±16V
Analog Input Voltage Each Input
(IN_1 thru IN_4) . . . . . ±3.5V
Differential Voltage Between Any Two
Inputs (IN_1 thru IN_4) 5V
Digital Input Voltages (A_0, A_1, ENABLE) . −0.5V to +5.5V
Output Current
Sinking 6.0mA
Sourcing 6.0mA
Operating Temperature Range
AD9300KQ/KP . . . . . 0 to +70°C
AD9300TQ/TE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 12V \pm 5\%$; $C_L = 10pF$; $R_L = 2k\Omega$, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0 to +70°C AD9300KQ/KP Min	Typ	Max	Military Subgroup[2]	MILITARY −55°C to +125°C AD9300TQ/TE Min	Typ	Max	Units
INPUT CHARACTERISTICS										
Input Offset Voltage	+25°C	I		3	10	1		3	10	mV
Input Offset Voltage	Full	VI			14	2,3			18	mV
Input Offset Voltage Drift[3]	Full	V		75				83		µV/°C
Input Bias Current	+25°C	I		15	37	1		15	37	µA
Input Bias Current	Full	VI			55	2,3			55	µA
Input Resistance	+25°C	V		3.0				3.0		MΩ
Input Capacitance	+25°C	V		2				2		pF
Input Noise Voltage (dc to 8MHz)	+25°C	V		16				16		µV rms
TRANSFER CHARACTERISTICS										
Voltage Gain[4]	+25°C	I	0.990	0.994		1	0.990	0.994		V/V
Voltage Gain[4]	Full	VI	0.985			2,3	0.985			V/V
DC Linearity[5]	+25°C	V		0.01				0.01		%
Gain Tolerance (V_{IN} = ±1V)										
dc to 5MHz	+25°C	I		0.05	0.1	4		0.05	0.1	dB
5MHz to 8MHz	+25°C	I		0.1	0.3	4		0.1	0.3	dB
Small-Signal Bandwidth (V_{IN} = 100mV p-p)	+25°C	V		350				350		MHz
Full Power Bandwidth[6] (V_{IN} = 2V p-p)	+25°C	I	30	34		4	30	34		MHz
Output Swing	Full	VI	±2			1,2,3	±2			V
Output Current (Sinking @ = 25°C)	+25°C	V		5				5		mA
Output Resistance	+25°C	III		9	15	12		9	15	Ω
DYNAMIC CHARACTERISTICS										
Slew Rate[7]	+25°C	I	190	215		4	190	215		V/µs
Settling Time (to 0.1% on ±2V Output)	+25°C	III		70	100	12		70	100	ns
Overshoot										
To T-Step[8]	+25°C	V		<0.1				<0.1		%
To Pulse[9]	+25°C	V		<10				<10		%
Differential Phase[10]	+25°C	III		0.05	0.1	12		0.05	0.1	°
Differential Gain[10]	+25°C	III		0.05	0.1	12		0.05	0.1	%
Crosstalk Rejection										
Three Channels[11]	+25°C	IV	70	75			70	75		dB
One Channel[12]	+25°C	IV	78(75)	80			78(75)	80		dB
SWITCHING CHARACTERISTICS[13]										
A_X Input to Channel HIGH Time[14] (t_{HIGH})	+25°C	I		40	50	9		40	50	ns
A_X Input to Channel LOW Time[15] (t_{LOW})	+25°C	I		35	45	9		35	45	ns
Enable to Channel ON Time[16] (t_{ON})	+25°C	I		30	40	9		30	40	ns
Enable to Channel OFF Time[17] (t_{OFF})	+25°C	I		20	30	9		20	30	ns
Switching Transient[18]	+25°C	V		60				60		mV

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0 to +70°C AD9300KQ/KP Min	Typ	Max	Military Subgroup[2]	MILITARY −55°C to +125°C AD9300TQ/TE Min	Typ	Max	Units
DIGITAL INPUTS										
Logic "1" Voltage	Full	VI	2			1,2,3	2			V
Logic "0" Voltage	Full	VI			0.8	1,2,3			0.8	V
Logic "1" Current	Full	VI			5	1,2,3			5	μA
Logic "0" Current	Full	VI			1	1,2,3			1	μA
POWER SUPPLY										
Positive Supply Current (+12V)	+25°C	I		13	16	1		13	16	mA
Positive Supply Current (+12V)	Full	VI		13	16	2,3		13	16	mA
Negative Supply Current (−12V)	+25°C	I		12.5	15	1		12.5	15	mA
Negative Supply Current (−12V)	Full	VI		12.5	16	2,3		12.5	16	mA
Power Supply Rejection Ratio ($\pm V_S = \pm 12V \pm 5\%$)	Full	VI	67	75		1,2,3	67	75		dB
Power Dissipation (±12V)[19]	+25°C	V		306				306		mW

NOTES

For applications assistance, phone Computer Labs Division at (919) 668-9511

[1]Permanent damage may occur if any one absolute maximum rating is exceeded. Functional operation is not implied, and device reliability may be impaired by exposure to higher-than-recommended voltages for extended periods of time.

[2]Military Subgroups apply to military-qualified devices only.

[3]Measured at extremes of temperature range.

[4]Measured as slope of V_{OUT} versus V_{IN} with $V_{IN} = \pm 1V$.

[5]Measured as worst deviation from end-point fit with $V_{IN} = \pm 1V$.

[6]Full Power Bandwith (FPBW) based on Slew Rate (SR). $FPBW = SR/2\pi V_{PEAK}$

[7]Measured between 20% and 80% transition points of ±1V output.

[8]T-Step = Sin^2X Step, when Step between 0V and +700mV points has 10%-to-90% risetime = 125ns.

[9]Measured with a pulse input having slew rate >250V/μs.

[10]Measured at output between 0.28Vdc and 1.0Vdc with V_{IN} = 284mV p-p at 3.58MHz and 4.43MHz.

[11]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p-p signal applied to remaining three channels. If selected channel is grounded through 75Ω, value is approximately 6dB higher.

[12]This specification is critically dependent on circuit layout. Value shown is measured with selected channel grounded and 10MHz 2V p-p signal applied to one other channel. If selected channel is grounded through 75Ω, value is approximately 6dB higher. Minimum specification in ( ) applies to DIPs.

[13]Consult system timing diagram.

[14]Measured from address change to 90% point of −2V to +2V output LOW-to-HIGH transition.

[15]Measured from address change to 10% point of +2V to −2V output HIGH-to-LOW transition.

[16]Measured from 50% transition point of ENABLE input to 90% transition of 0V to −2V output.

[17]Measured from 50% transition point of ENABLE input to 10% transition of +2V to 0V output.

[18]Measured while switching between two grounded channels.

[19]Maximum power dissipation is a package-dependent parameter related to the following typical thermal impedances:

16-Pin Ceramic $\theta_{JA} = 87°C/W$; $\theta_{JC} = 25°C/W$

20-Pin LCC $\theta_{JA} = 74°C/W$; $\theta_{JC} = 10°C/W$

Specifications subject to change without notice.

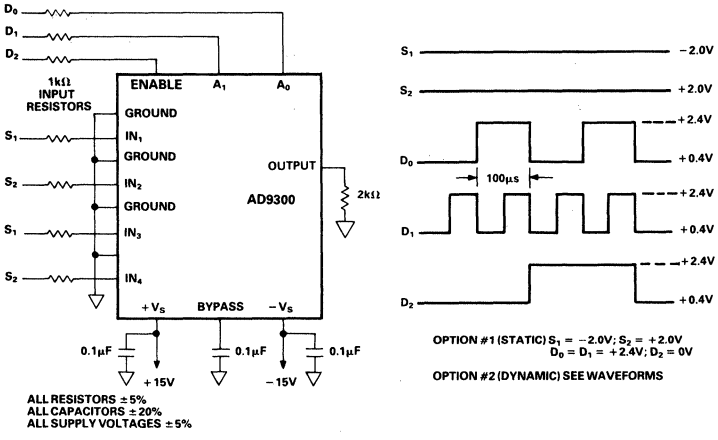
EXPLANATION OF TEST LEVELS

Test Level I	–	100% production tested.
Test Level II	–	100% production tested at +25°C, and sample tested at specified temperatures.
Test Level III	–	Sample tested only.
Test Level IV	–	Parameter is guaranteed by design and characterization testing.
Test Level V	–	Parameter is a typical value only.
Test Level VI	–	All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

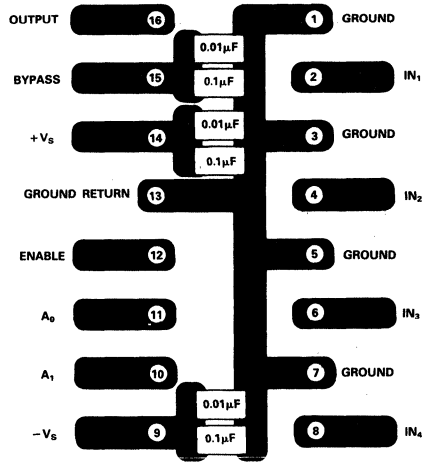
Subgroup 1	–	Static tests at +25°C. (5% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2	–	Static tests at maximum rated temperature.
Subgroup 3	–	Static tests at minimum rated temperature.
Subgroup 4	–	Dynamic tests at +25°C.
Subgroup 5	–	Dynamic tests at maximum rated temperature.
Subgroup 6	–	Dynamic tests at minimum rated temperature.
Subgroup 7	–	Functional tests at +25°C.
Subgroup 8	–	Functional tests at maximum and minimum rated temperatures.
Subgroup 9	–	Switching tests at +25°C.
Subgroup 10	–	Switching tests at maximum rated temperature.
Subgroup 11	–	Switching tests at minimum rated temperature.
Subgroup 12	–	Periodically sample tested.

AD9300 BURN-IN DIAGRAM



ALL RESISTORS ±5%
ALL CAPACITORS ±20%
ALL SUPPLY VOLTAGES ±5%

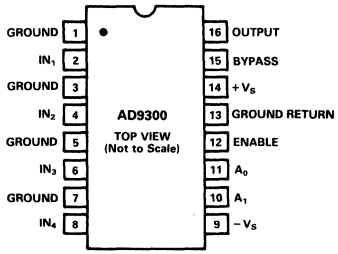
SUGGESTED LAYOUT OF AD9300 PC BOARD



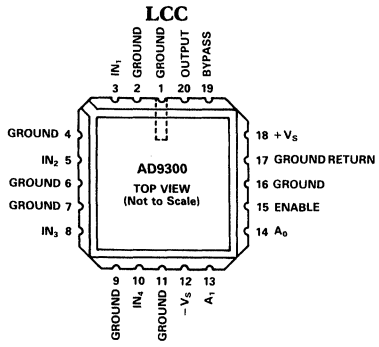
(Bottom View – Not to Scale)
Component Side Should be Ground Plane

PIN DESIGNATIONS

DIP

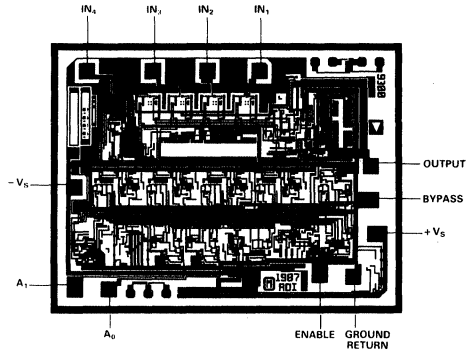


LCC



(PLCC PINOUTS SAME AS LCC)

METALIZATION PHOTOGRAPH



MECHANICAL INFORMATION

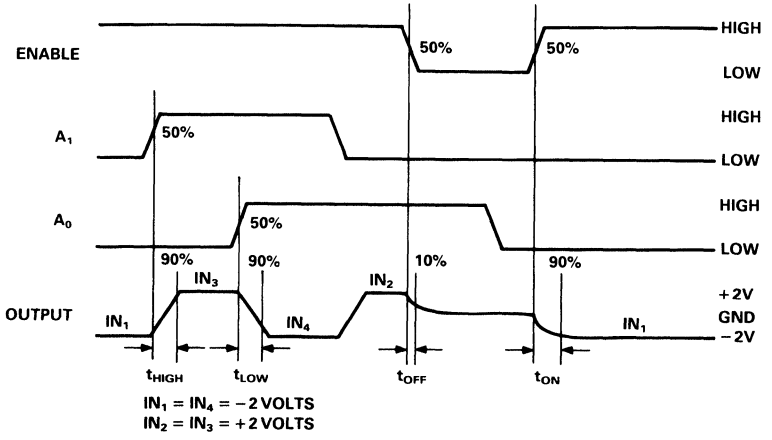
Die Dimensions	84 × 104 × 18 (max) mils
Pad Dimensions	4 × 4 (min) mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding

FUNCTIONAL DESCRIPTION

$IN_1 - IN_4$	Four analog input channels.
GROUND	Analog input shielding grounds, not internally connected. Connect each to external low-impedance ground as close to device as possible.
A_0	One of two TTL decode control lines required for channel selection. See Logic Truth Table.
A_1	One of two TTL decode control lines required for channel selection. See Logic Truth Table.
ENABLE	TTL-compatible chip enable. In enabled mode (logic HIGH), output signal tracks selected input channel; in disabled mode (logic LOW), output is high impedance and no signal appears at output.
$-V_S$	Negative supply voltage; nominally -10V dc to -15V dc.
$+V_S$	Positive supply voltage; nominally $+10$V dc to $+15$V dc.
OUTPUT	Analog output. Tracks selected input channel when enabled.
BYPASS	Bypass terminal for internal bias line; must be decoupled externally to ground through 0.1μF capacitor.
GROUND RETURN	Analog signal and power supply ground return.

LOGIC TRUTH TABLE

ENABLE	A_1	A_0	OUTPUT
0	X	X	High Z
1	0	0	IN_1
1	0	1	IN_2
1	1	0	IN_3
1	1	1	IN_4



AD9300 Timing

THEORY OF OPERATION

Refer to the functional block diagram of the AD9300.

As shown on the drawing, this diagram is based on the pinouts of the DIP packaging of the models AD9300KQ and AD9300TQ. The AD9300TE is packaged in a 20-pin leadless chip carrier (LCC), but the extra pins are used for ground connections; the theory of operation remains the same.

The AD9300 Video Multiplexer allows the user to connect any one of four analog input channels ($IN_1 - IN_4$) to the output of the device, and to switch between channels at megahertz rates.

The input channel which is connected to the output is determined by a 2-bit TTL digital code applied to A_0 and A_1. The selected input will not appear at the output unless a digital "1" is also applied to the ENABLE input pin; unless the output is enabled, it is a high impedance. Necessary combinations to accomplish channel selection are shown in the Logic Truth Table.

Bipolar construction used in the AD9300 insures that the input impedance of the device remains high, and will not vary with power supply voltages. This characteristic makes the AD9300, in effect, a switchable-input buffer. An on-board bias network makes the performance of the AD9300 independent of applied supply voltages, which can have any nominal value from ±10V dc to ±15V dc.

Although the primary application for the AD9300 is the routing of video signals, the harmonic and dynamic attributes of the device make it appropriate for other applications. The AD9300 has exceptional performance when switching video signals, but can also be used for switching other analog signals requiring greater dynamic range and/or precision than those in video.

As shown in Figure 1, Input and Output Equivalent Circuits, each analog input is connected to the base of a bipolar transistor. If Channel 1 is selected, a current switch is closed and routes current through the input transistor for Channel 1.

If Channel 2 is then selected by the digital inputs, the current switch for Channel 1 is opened and the current switch for Channel 2 is closed. This causes current to be routed away from the Channel 1 transistor and into the Channel 2 input transistor. Whenever a channel's input device is carrying current, the analog input applied to that channel is passed to the output stage.

The operation of the output stage is similar to that of the input stages. Whenever the output stage is enabled with a HIGH digital "1" signal at the ENABLE pin, the output transistor will carry current and pass the selected analog input.

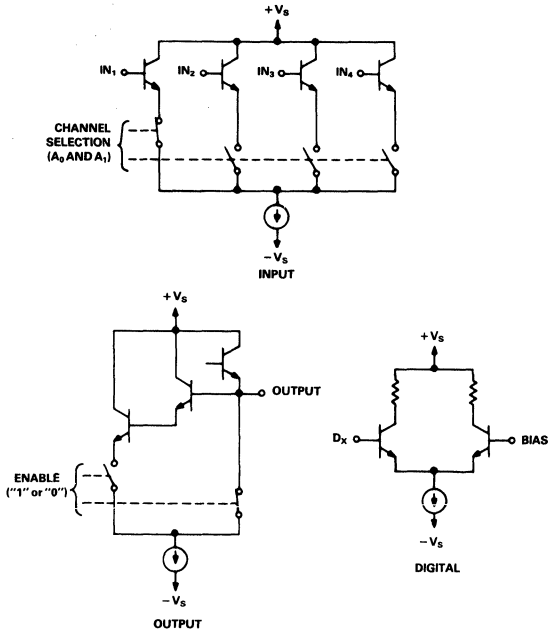


Figure 1. Input and Output Equivalent Circuits

When the output stage is disabled (by virtue of the ENABLE pin being driven LOW with a digital "0"), the output current switch is opened. This routes the current to other circuits within the AD9300 which keep the output transistor biased "off". These circuits require approximately 1μA of bias current from the load connected to the output of the multiplexer. In the absence of a terminating load and the resulting dc bias, the output of the AD9300 "floats" at −2.5V.

In summary, when the AD9300 is enabled by the ENABLE pin being driven HIGH with a digital "1", the selected analog input channel acts as a buffer for the input; and the output of the multiplexer is a low impedance. When the AD9300 is disabled with a digital "0" LOW signal, the selected channel acts as an open switch for the input; and the output of the unit becomes a high impedance. This characteristic allows the user to wire-or several AD9300 Analog Multiplexers together to form switch matrices.

AD9300 APPLICATIONS

To ensure optimum performance from circuits using the AD9300, it is important to follow a few basic rules which apply to all high-speed devices.

A large, low-impedance ground plane under the AD9300 is critical. Generally, GROUND and GROUND RETURN connections should be connected solidly to this plane. GROUND pin connections are signal isolation grounds which are not connected internally; they can be left unconnected, but there may be some degradation in crosstalk rejection. GROUND RETURN, on the other hand, serves as the internal ground reference for the AD9300 and should be connected to the ground plane *without exception.*

It is recommended that the AD9300 be soldered directly into circuit boards, rather than using socket assemblies. If sockets must be used, individual pin sockets are the preferred choice, rather than a socket assembly. A second requirement for proper high-speed design involves decoupling the power supply and internal bias supply lines from ground to improve noise immunity. Chip capacitors are recommended for connecting 0.1μF and 0.01μF capacitors between ground and the $\pm V_S$ supplies (Pins 9 and 14), and the BYPASS connection (Pin 15).

The output stage of the unit is capable of driving a 2kΩ‖10pF load. Larger capacative loads may limit full power bandwidth and increase t_{OFF} (the interval between the 50% point of the ENABLE high-to-low transition and the instant the output becomes a high impedance.)

For applications such as driving cables (See Figure 2), output buffers are recommended.

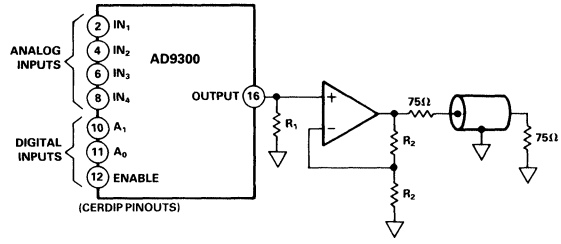


Figure 2. 4×1 AD9300 Multiplexer with Buffered Output Driving 75Ω Coaxial Cable

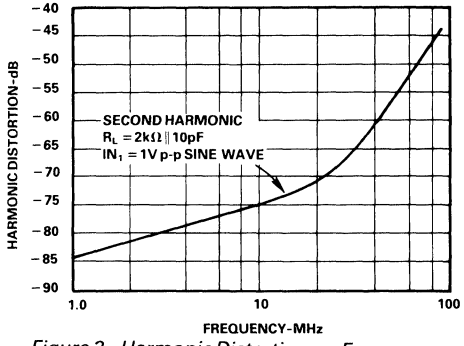


Figure 3. Harmonic Distortion vs. Frequency

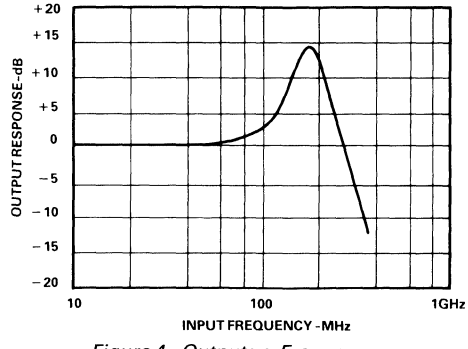


Figure 4. Output vs. Frequency

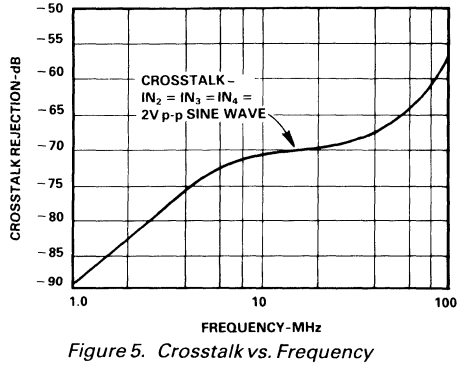


Figure 5. Crosstalk vs. Frequency

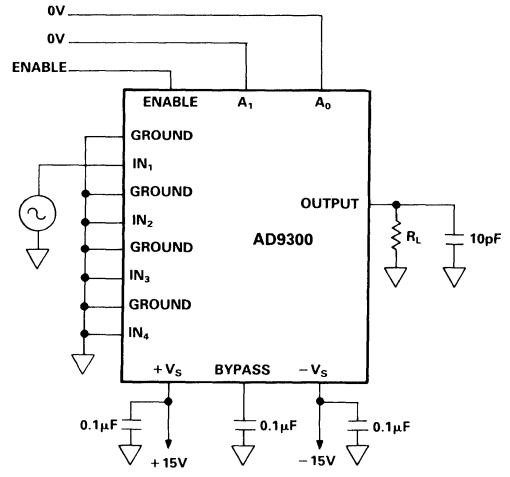


Figure 6. Test Circuit for Harmonic Distortion, Pulse Response, T-Step Response and Disable Characteristics

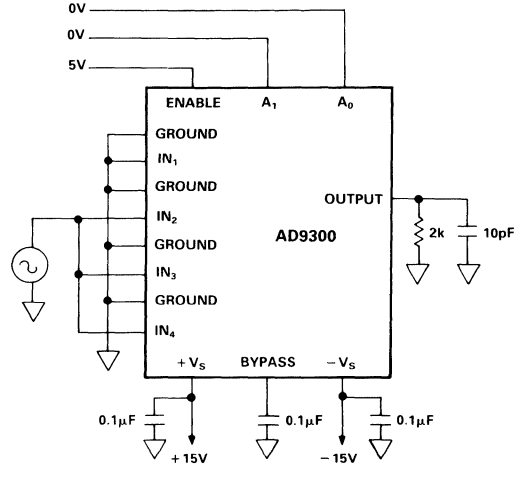


Figure 7. Crosstalk Rejection Test Circuit

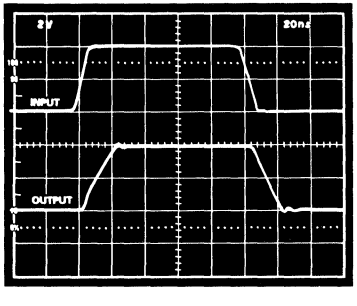


Figure 8. Pulse Response

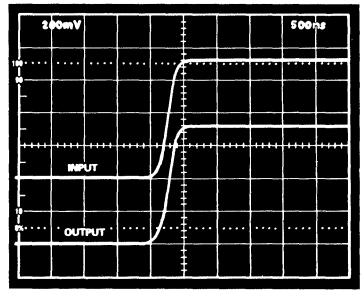


Figure 9. T-Step Response

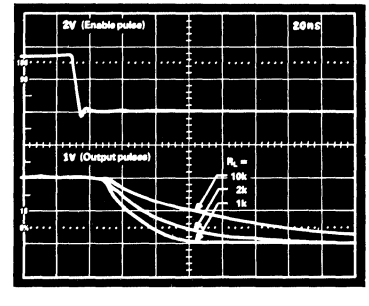


Figure 10. Enable to Channel "Off" Response

CROSSPOINT CIRCUIT APPLICATIONS

Four AD9300 multiplexers can be used to implement an 8 × 2 crosspoint, as shown in Figure 11. The circuit is modular in concept, with each pair of multiplexers (#1 and #2; #3 and #4) forming an 8 × 1 crosspoint. When the inputs to all four units are connected as shown, the result is an 8 × 2 crosspoint circuit.

D_2 or D_5	D_1 or D_4	D_0 or D_3	OUT_1 or OUT_2
0	0	0	S_1
0	0	1	S_2
0	1	0	S_3
0	1	1	S_4
1	0	0	S_5
1	0	1	S_6
1	1	0	S_7
1	1	1	S_8

8 × 2 Crosspoint Truth Table

The truth table describes the relationships among the digital inputs ($D_0 - D_5$) and the analog inputs ($S_1 - S_8$); and which signal input is selected at the outputs (OUT_1 and OUT_2). The number of crosspoint modules that can be connected in parallel is limited by the drive capabilities of the input signal sources. High input impedance (3MΩ) and low input capacitance (2pF) of the AD9300 help minimize this limitation.

Adding to the number of inputs applied to each crosspoint module is simply a matter of adding AD9300 multiplexers in parallel to the module. Eight devices connected in parallel result in a 32 × 1 crosspoint which can be used with input signals having 30MHz bandwidth and 1V peak-to-peak amplitude. Even more AD9300 units can be added if input signal amplitude and/or bandwidth are reduced; if they are not, distortion of the output signals can result.

When an AD9300 is enabled, its low output impedance causes the "off" isolation of disabled parallel devices to be greater than the crosstalk rejection of a single unit.

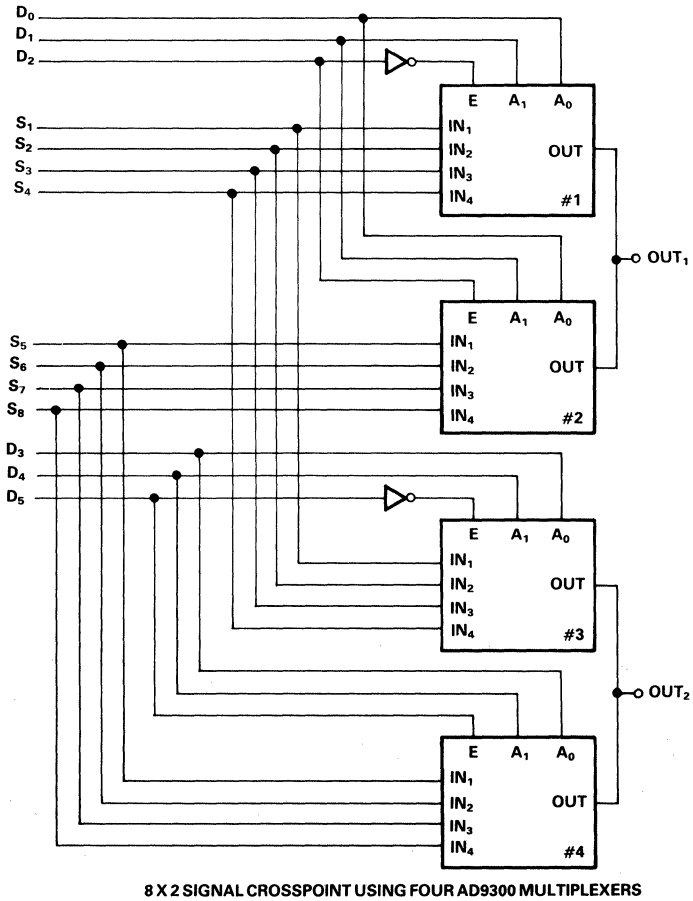


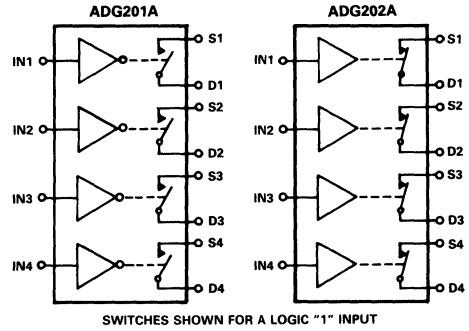
Figure 11. 8 × 2 Signal Crosspoint Using Four AD9300 Multiplexers

CMOS Quad SPST Switches

ADG201A/ADG202A

FEATURES
44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (60Ω)
Low Leakage (0.5nA)
Extended Plastic Temperature Range (−40°C to +85°C)
Low Power Dissipation (33mW)
Standard 16-Pin Dips and 20-Terminal Surface Mount Packages
Superior Second Source:
ADG201A Replaces DG201A, HI-201
ADG202A Replaces DG202

ADG201A/ADG202A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

ORDERING INFORMATION[1]

Temperature Range and Package Options[2, 3]		
−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP (N-16)	**Hermetic (Q-16)**	**Hermetic (Q-16)**
ADG201AKN	ADG201ABQ	ADG201ATQ
ADG202AKN	ADG202ABQ	ADG202ATQ
PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
ADG201AKP		ADG201ATE
ADG202AKP		ADG202ATE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. See Analog Devices Military Products Data Book (1987) for military data sheet.
[2]See Section 14 for package outline information.
[3]Also available in SOIC packages (ADG201AKR, ADG202AKR)
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG201A IN	ADG202A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

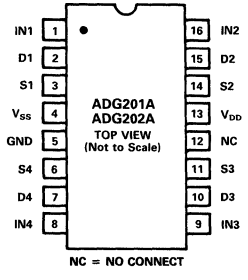
SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, unless otherwise noted)

Parameter	K Version 25°C	K Version −40°C to +85°C	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}	60		60		60		Ω typ	−10V≤V_S≤+10V
	90	145	90	145	90	145	Ω max	I_{DS} = 1.0mA Test Circuit 1
R_{ON} vs. V_D(V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	V_S = 0V, I_{DS} = 1mA
I_S(OFF)	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S ∓14V; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D(OFF)	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D(ON)	0.5		0.5		0.5		nA typ	V_D = ±14V; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[1]	300		300		300		ns max	Test Circuit 4
t_{OFF}[1]	250		250		250		ns max	Test Circuit 4
OFF Isolation	80		80		80		dB typ	V_S = 10V(p-p); f = 100kHz R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S(OFF)	5		5		5		pF typ	
C_D(OFF)	5		5		5		pF typ	
C_D, C_S(ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		2		2		2	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		33		33		33	mW max	

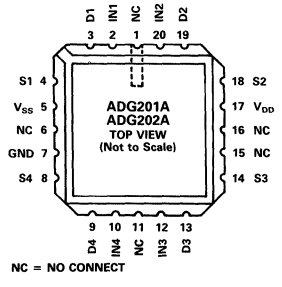
NOTES
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

PIN CONFIGURATIONS

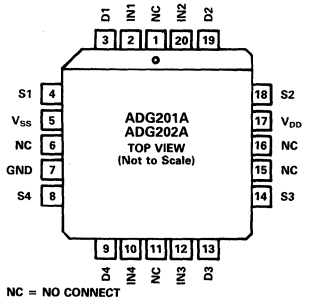
DIP



LCCC



PLCC



ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise stated)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −0.3V to V_{DD} +0.3V
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[1]	
Voltage at IN	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commercial (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

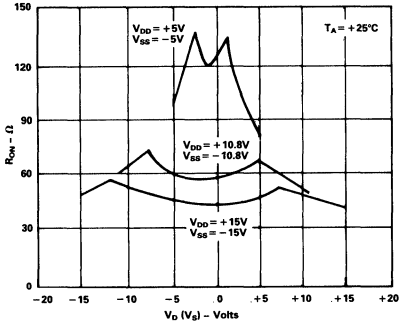
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

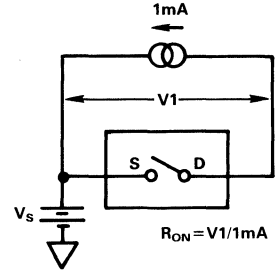
7

Typical Performance Characteristics and Test Circuits

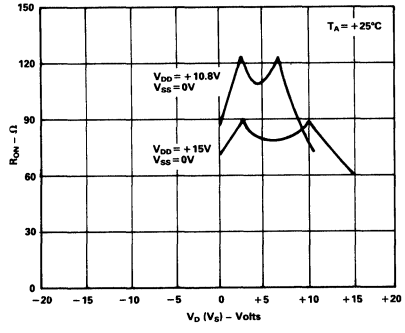
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



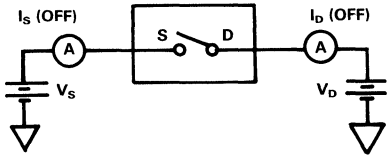
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



Test Circuit 1

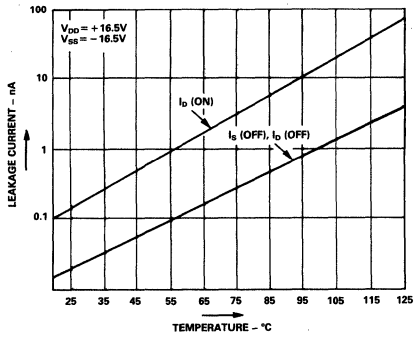


R_{ON} as a Function of V_D (V_S): Single Supply Voltage

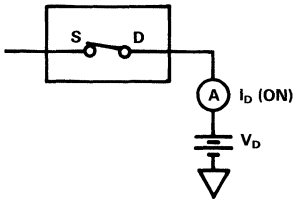


Test Circuit 2

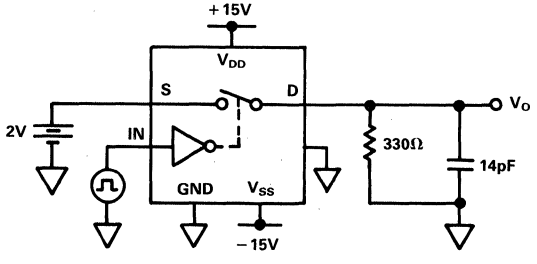
Typical Performance Characteristics and Test Circuits Cont'd

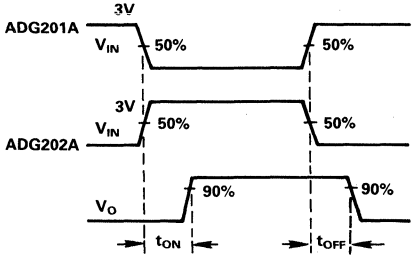


Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

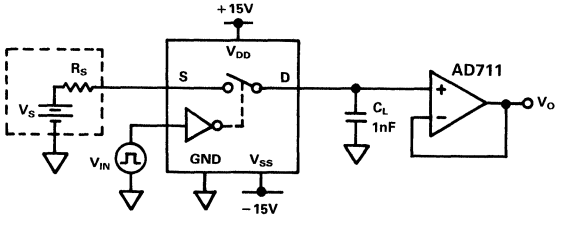


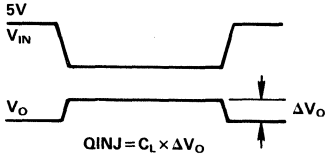
Test Circuit 3



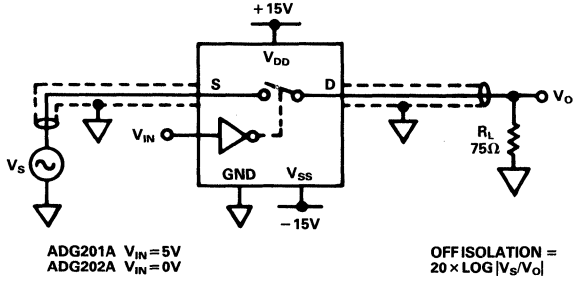


Test Circuit 4

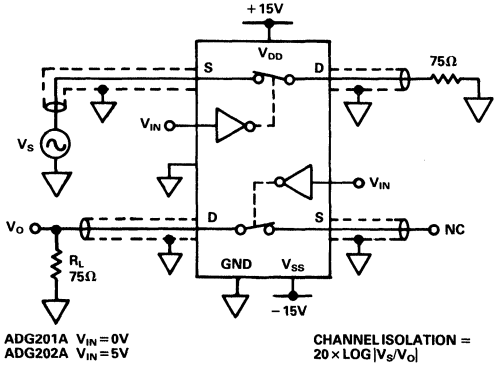




Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation



Test Circuit 7. Channel to Channel Isolation

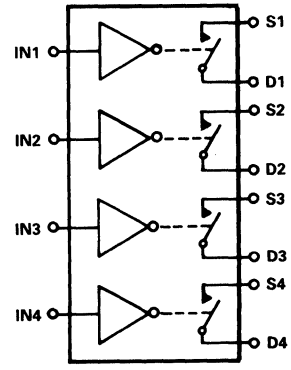
LC²MOS
High Speed, Quad SPST Switch

ADG201HS

FEATURES

50ns max Switching Time Over Full Temperature Range
Low R_{ON} (30Ω typ)
Single Supply Specifications for +10.8V to +16.5V Operation
Extended Plastic Temperature Range (−40°C to +85°C)
Break-Before-Make Switching
Low Leakage (100pA typ)
44V Supply max Rating
ADG201HS (K,B,T) Replaces HI-201HS
ADG201HS (J,A,S) Replaces DG271

ADG201HS FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG201HS is a monolithic CMOS device comprising four independently selectable SPST switches. It is designed on an enhanced LC²MOS process which gives very fast switching speeds and low R_{ON}.

The switches also feature break-before-make switching action for use in multiplexer applications and low charge injection for minimum transients on the output when switching the digital inputs.

ORDERING INFORMATION[1]

Temperature Range and Package Options[2,3]

−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP (N-16)	**Hermetic (Q-16)**	**Hermetic (Q-16)**
ADG201HSJN	ADG201HSAQ	ADG201HSSQ
ADG201HSKN	ADG201HSBQ	ADG201HSTQ
PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
ADG201HSJP		ADG201HSTE
ADG201HSKP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing 5962-86716.
[2]See Section 14 for package outline information.
[3]Also available in SOIC package (ADG201HSKR).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

PRODUCT HIGHLIGHTS

1. 50ns max t_{ON} and t_{OFF}:
   The ADG201HS top grades (K, B, T) have guaranteed 50ns max turn-on and turn-off times over the full operating temperature range. The lower grades (J,A,S) have guaranteed 75ns switching times over the full operating temperature range.
2. Single Supply Specifications:
   The ADG201HS is fully specified for applications which require a single positive power supply in the +10.8V to +16.5V range.
3. Low Leakage:
   Leakage currents in the range of 100pA make these switches suitable for high precision circuits. The added feature of break-before-make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

IN	Switch Condition
0	ON
1	OFF

Truth Table

SPECIFICATIONS

Dual Supply

(V_{DD} = +13.5V to +16.5V, V_{SS} = −13.5V to −16.5V, GND = 0V, V_{IN} = 3V (Logic High Level) or 0.8V (Logic Low Level) unless otherwise noted)

Parameter	Version	+25°C	T_{min}–T_{max}[1]	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	Vmin	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	30	–	Ω typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA; Test Circuit 1
	All	50	75	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
R_{ON} Match	All	3	–	% typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage[2]	All	0.1		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[2]	All	0.1		nA typ	$V_D = \pm 14V$; $V_S = \mp 14V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S,T	1	60	nA max	
I_D (ON), On Channel Leakage[2]	All	0.1		nA typ	$V_D = \pm 14V$; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S,T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF1}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	t_{ON}–t_{OFF1}; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
I_{SS}	All	6	6	mA max	
Power Dissipation	All	240	240	mW max	V_{DD} = +15V, V_{SS} = −15V

NOTES

[1]Temperature ranges are as follows: ADG201HSJ, K; −40°C to +85°C
ADG201HSA, B; −40°C to +85°C
ADG201HSS, T; −55°C to +125°C

[2]Leakage specifications apply with a V_D (V_S) of ±14V or with a V_D (V_S) of 0.5V within the supply voltages (V_{DD}, V_{SS}), whichever is the minimum.

Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V, V_{IN} = 3V [Logic High Level] or 0.8V [Logic Low Level] unless otherwise noted)

Parameter	Version	+25°C	T_{min}–T_{max}	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	V min	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	65	–	Ω typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA; Test Circuit 1
	All	90	120	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA
R_{ON} Match	All	3	–	% typ	$0V \leq V_S \leq +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage[1]	All	0.1		nA typ	V_D = +10V/+0.5V; V_S = +0.5V/+10V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[1]	All	0.1		nA typ	V_D = +10V/+0.5V; V_S = +0.5V/+10V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (ON), On Channel Leakage[1]	All	0.1		nA typ	V_D = +10V/+0.5V; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF1}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	t_{ON}–t_{OFF1}; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
Power Dissipation	All	150	150	mW max	V_{DD} = +15V

NOTE
[1]The leakage specifications degrade marginally (typically 1nA at 25°C) with V_D (V_S) = V_{SS}.
Specifications subject to change without notice.

7

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	−0.3V, 25V
V_{SS} to GND[1]	+0.3V, −25V
Analog Inputs[2]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[2]	
Voltage at IN	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First

Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commerical (J, K Version)	−40°C to +85°C
Industrial (A, B Version)	−40°C to +85°C
Extended (S, T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

NOTES

[1]If V_{SS} is open circuited with V_{DD} and GND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to GND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

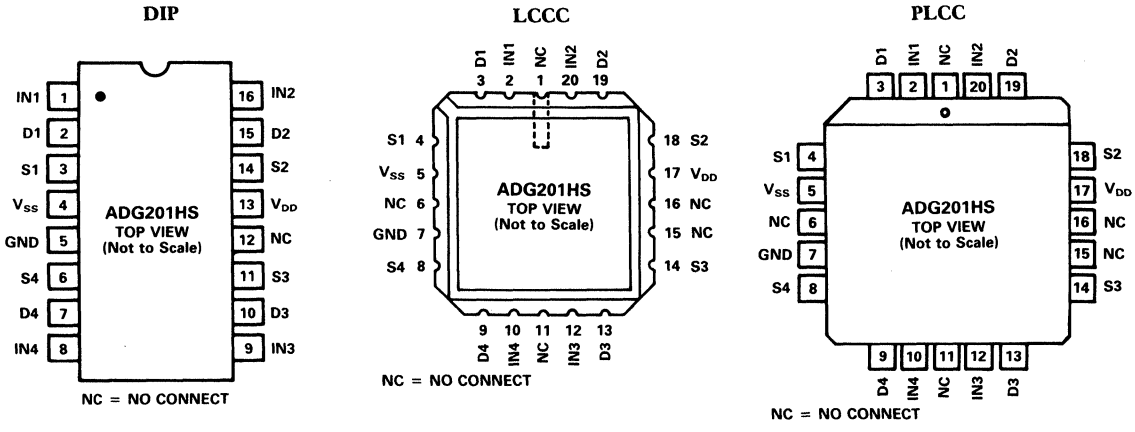
[2]Overvoltage at IN, S or D, will be clamped by diodes. Current should be limited to the maximum rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

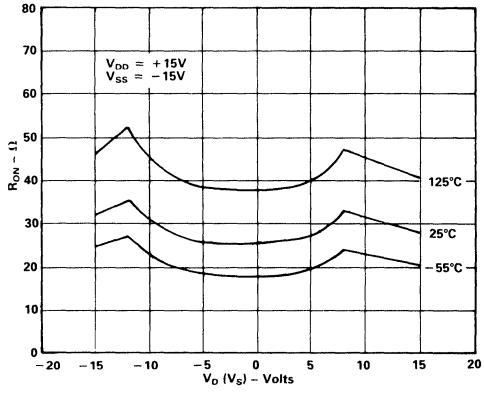
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

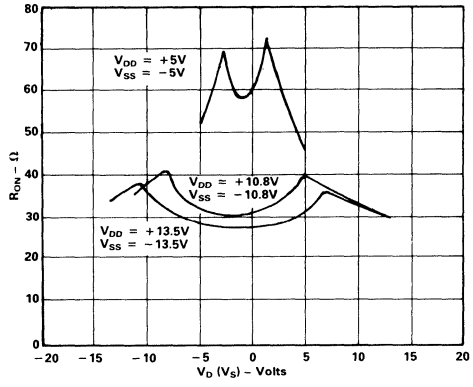
PIN CONFIGURATIONS



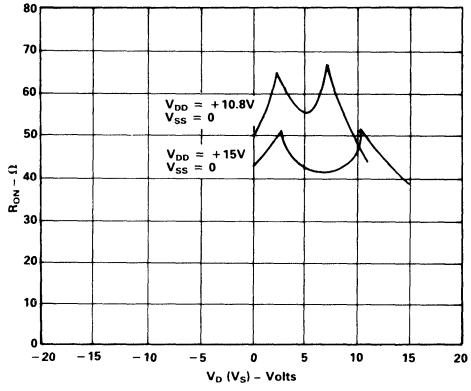
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



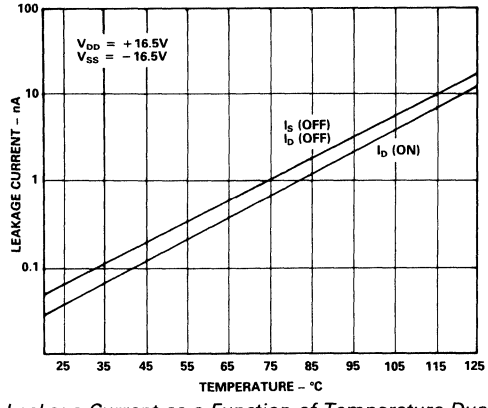
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



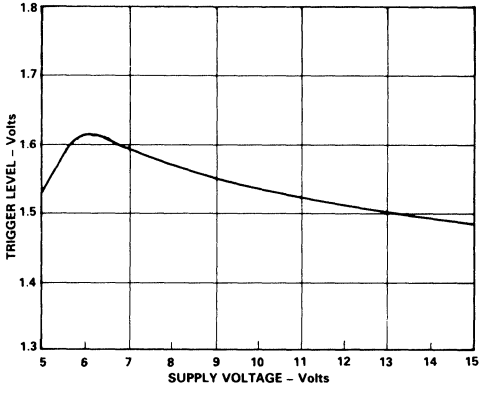
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage, T_A = +25°C



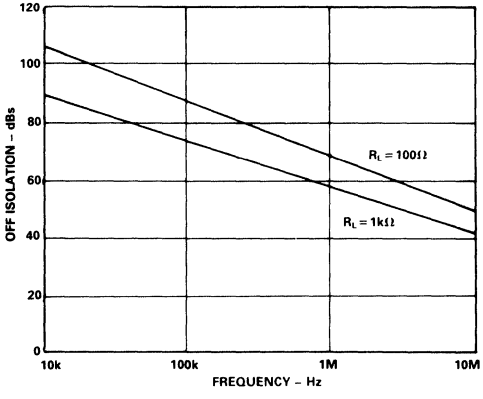
R_{ON} as a Function of V_D (V_S): Single Supply Voltage, T_A = +25°C



Leakage Current as a Function of Temperature Dual Supply Voltage. (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

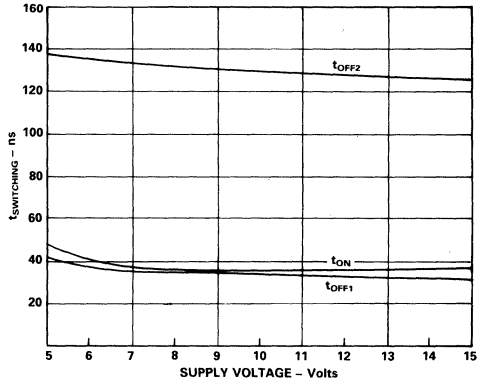


Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C

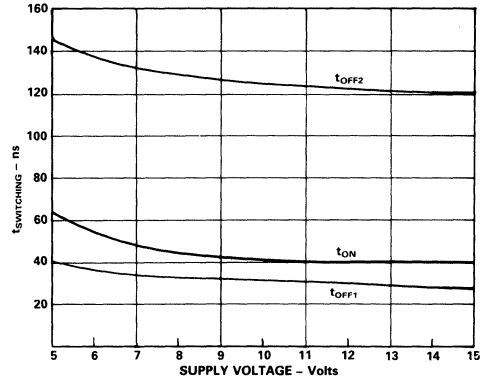


Off Isolation vs. Signal Frequency; Dual or Single 15V Supplies, T_A = +25°C

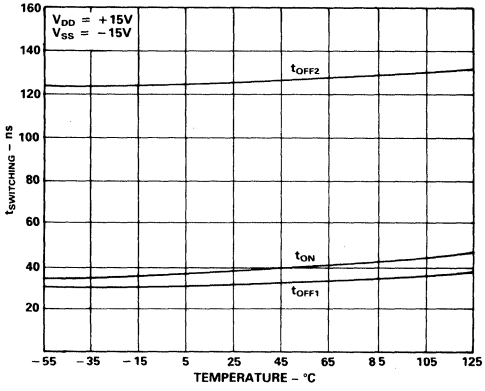
Typical Performance Characteristics (Continued)



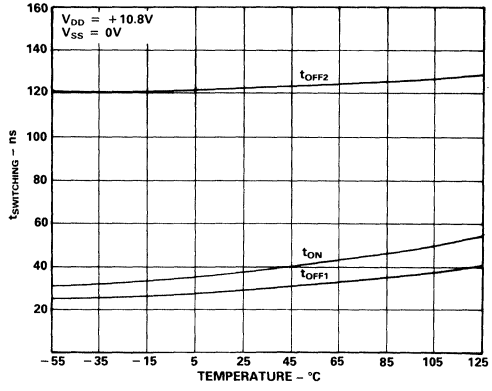
Switching Time vs. Supply Voltage (Dual Supply): T_A = +25°C. (Note: See Test Circuit 4. For V_{DD} <10V, V_S = V_{DD})



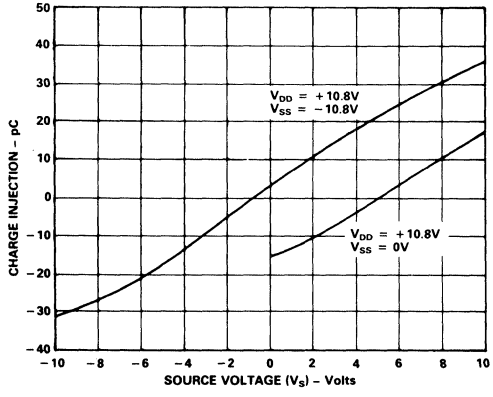
Switching Time vs. Supply Voltage (Single Supply): T_A = +25°C. (Note: See Test Circuit 4. For V_{DD} <10V, V_S = V_{DD})



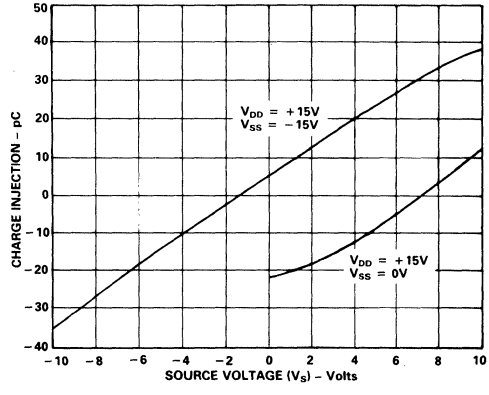
Switching Time vs. Temperature: Dual Supply Voltage



Switching Time vs. Temperature: Single Supply Voltage



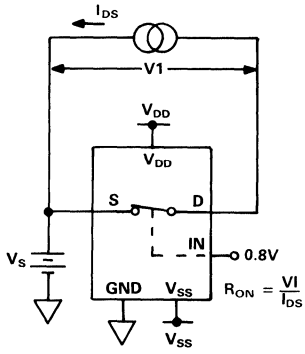
Charge Injection vs. Source Voltage (V_S) for Dual and Single 10.8V Supplies: T_A = +25°C



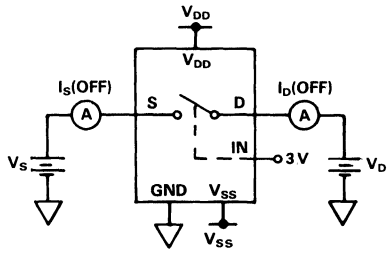
Charge Injection vs. Source Voltage (V_S) for Dual and Single 15V Supplies: T_A = +25°C

Note: All digital input signal rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 5ns$. Decoupling capacitors (0.01μF min) from V_{DD} and V_{SS} to GND are recommended to achieve specified performance.

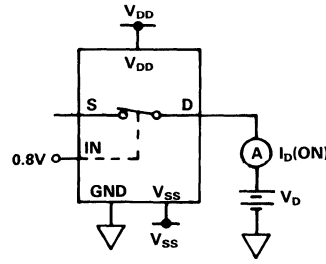
TEST CIRCUIT 1
R_{ON}



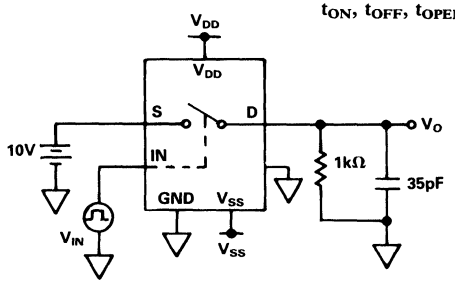
TEST CIRCUIT 2
I_S(OFF), I_D(OFF)

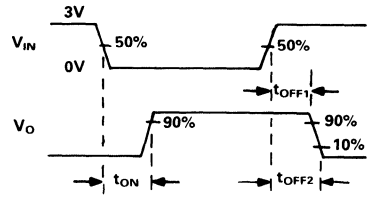


TEST CIRCUIT 3
I_D (ON)

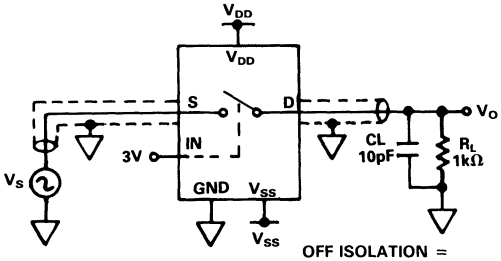


TEST CIRCUIT 4
t_{ON}, t_{OFF}, t_{OPEN}, SETTLING TIME



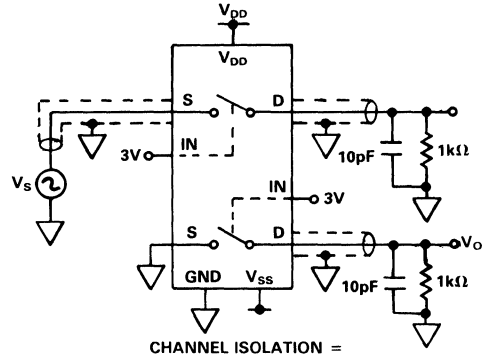


TEST CIRCUIT 5
OFF ISOLATION



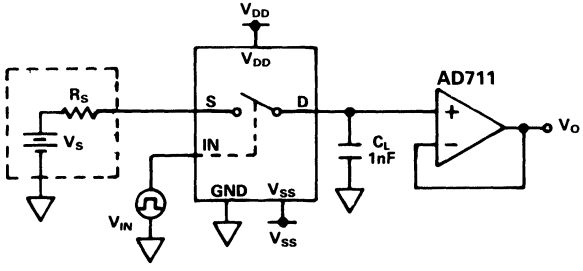
OFF ISOLATION =
$20 \times LOG|V_S/V_O|$

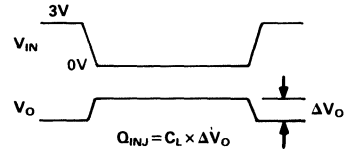
TEST CIRCUIT 6
CHANNEL-TO-CHANNEL CROSSTALK



CHANNEL ISOLATION =
$20 \times LOG|V_S/V_O|$

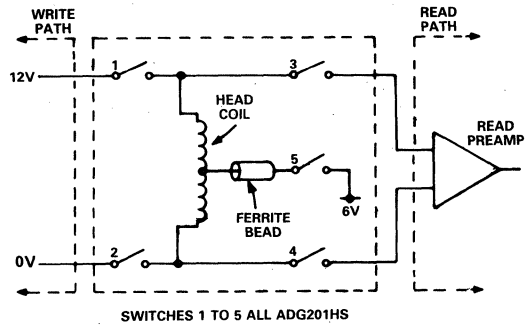
TEST CIRCUIT 7
CHARGE INJECTION





SINGLE SUPPLY DISK DRIVE APPLICATION

The excellent performance of the ADG201HS with single supply operation makes it suitable in applications such as disk drives where only positive power supply voltages are normally available. The accompanying circuit shows a typical application for the ADG201HS in the read/write head switching section of a disk drive. The circuit allows data (0s and 1s) to be written to and read from a disk. The principal advantage offered by the ADG201HS is that it retains very fast switching speed with single supply operation (see Single Supply Specifications). This allows disk drives to run at higher data rates.



SWITCH STATES/FUNCTION

SWITCH NUMBER	WRITE "0"	WRITE "1"	READ
1	OFF	ON	OFF
2	ON	OFF	OFF
3	OFF	OFF	ON
4	OFF	OFF	ON
5	ON	ON	OFF

ADG201HS in the Read/Write Head Switching Circuit of a Disk Drive

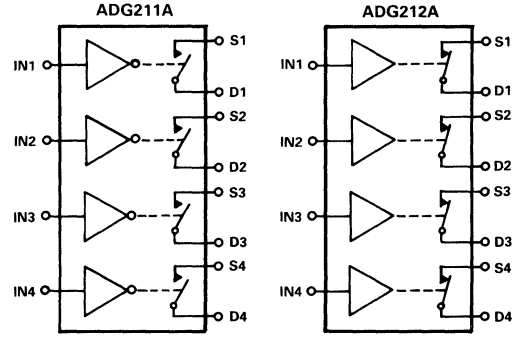
ANALOG DEVICES

LC²MOS Quad SPST Switches

ADG211A/ADG212A

FEATURES
- **44V Supply Maximum Rating**
- **±15V Analog Signal Range**
- **Low R_{ON} (115Ω max)**
- **Low Leakage (0.5nA typ)**
- **Single Supply Operation Possible**
- **Extended Plastic Temperature Range (−40°C to +85°C)**
- **TTL/CMOS Compatible**
- **Standard 16-Pin DIPs and 20-Terminal PLCC Packages**
- **Superior Second Source:**
  - **ADG211A Replaces DG211**
  - **ADG212A Replaces DG212**

ADG211A/ADG212A FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG211A and ADG212A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG211A and ADG212A consist of four SPST switches. They differ only in that the digital control logic is inverted. In multiplexer applications, all switches exhibit break-before-make switching action when driven simultaneously. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

ORDERING INFORMATION

Temperature Range and Package[1, 2]

Plastic DIP (N-16) −40°C to +85°C	PLCC[3] (P-20A) −40°C to +85°C
ADG211AKN	ADG211AKP
ADG212AKN	ADG212AKP

NOTE
[1]See Section 14 for package outline information.
[2]Also available in SOIC packages (ADG211AKR, ADG212AKR).
[3]PLCC: Plastic Leaded Chip Carrier.

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC²MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG211A IN	ADG212A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

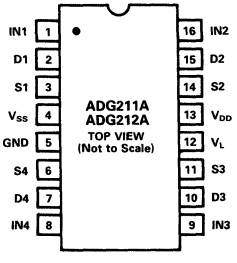
SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, V_L = 5V, unless otherwise noted)

	K Version			
Parameter	**25°C**	**−40°C to +85°C**	**Units**	**Test Conditions**
ANALOG SWITCH				
Analog Signal Range	±15	±15	Volts	
R_{ON}	115	175	Ωmax	−10V≤V_S≤+10V, I_{DS} = 1mA, Test Circuit 1
R_{ON} vs. V_D (V_S)	20		% typ	
R_{ON} Drift	0.5		%/°C typ	
R_{ON} Match	5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)	0.5		nA typ	V_D = ±14V; V_S ∓14V; Test Circuit 2
OFF Input Leakage	5	100	nA max	
I_D (OFF)	0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Output Leakage	5	100	nA max	
I_D (ON)	0.5		nA typ	V_D = ±14V; Test Circuit 3
ON Channel Leakage	5	200	nA max	
DIGITAL CONTROL				
V_{INH}, Input High Voltage		2.4	V min	TTL Compatibility is Independent of V_L
V_{INL}, Input Low Voltage		0.8	V max	
I_{INL} or I_{INH}		1	µA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS				
t_{OPEN}[1]	30		ns typ	Test Circuit 4
t_{ON}[1]	600		ns max	Test Circuit 5
t_{OFF}[1]	450		ns max	Test Circuit 5
OFF Isolation	80		dB typ	V_S = 10V(p-p); f = 100kHz R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		dB typ	Test Circuit 7
C_S (OFF)	5		pF typ	
C_D (OFF)	5		pF typ	
C_S, C_D (ON)	16		pF typ	
Q_{INJ}, Charge Injection	20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V Test Circuit 8
POWER SUPPLY				
I_{DD}	0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}	1		mA max	
I_{SS}	0.1		mA typ	
I_{SS}	0.2		mA max	
I_L	0.9		mA max	

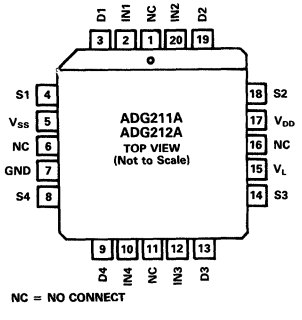
NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

PIN CONFIGURATIONS

DIP



PLCC



NC = NO CONNECT

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise stated)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
V_L to GND	−0.3V, 25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −0.3V to V_{DD} +0.3V
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[1]	
Voltage at IN	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

7

Typical Performance Characteristics

The switches can comfortably operate and are TTL compatible anywhere in the 10V to 15V single or dual supply range, with only a slight degradation in performance. The following graphs show some relevant performance curves. The test circuit is given in the following section, "Test Circuits."

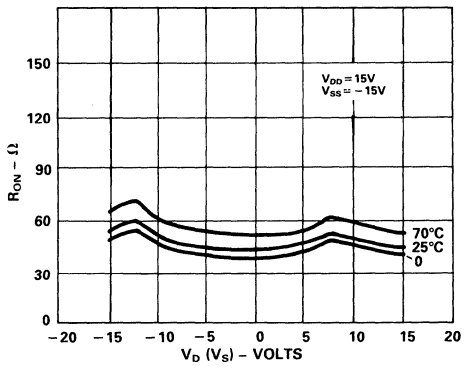


Figure 1. R_{ON} as a Function of V_D (V_S): Dual ± 15 Supplies

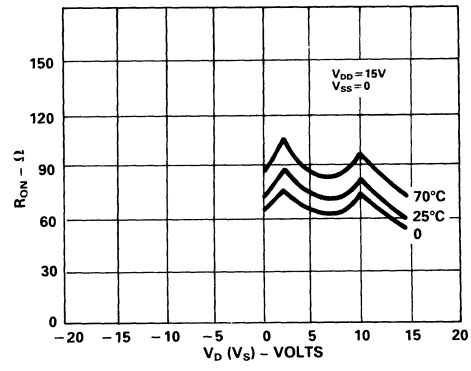
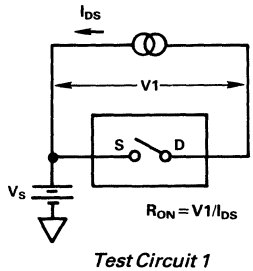
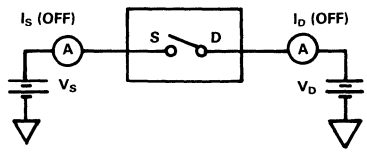


Figure 2. R_{ON} as a Function of V_D (V_S): Single + 15V Supply

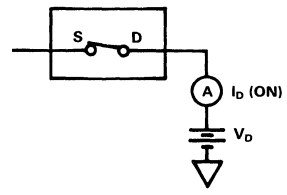
Test Circuits



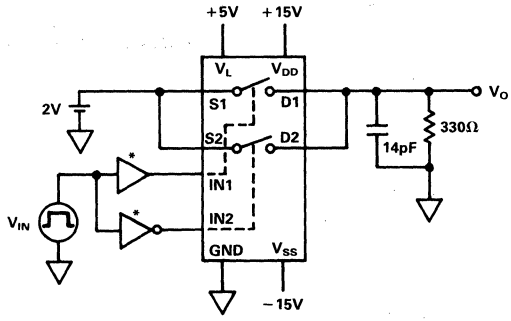
Test Circuit 1



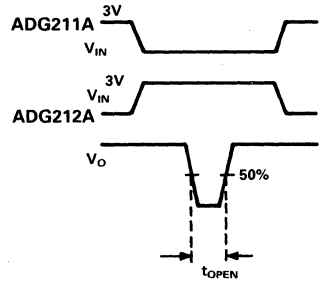
Test Circuit 2



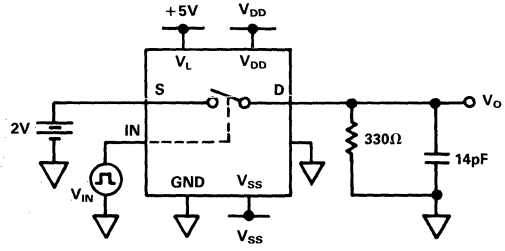
Test Circuit 3

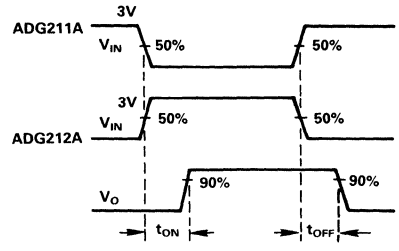


*BOTH THE BUFFER AND INVERTER SHOULD HAVE THE SAME PROPAGATION DELAY.

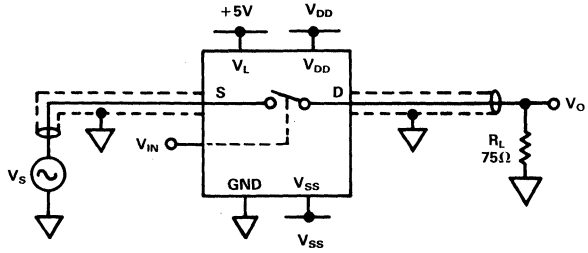


Test Circuit 4

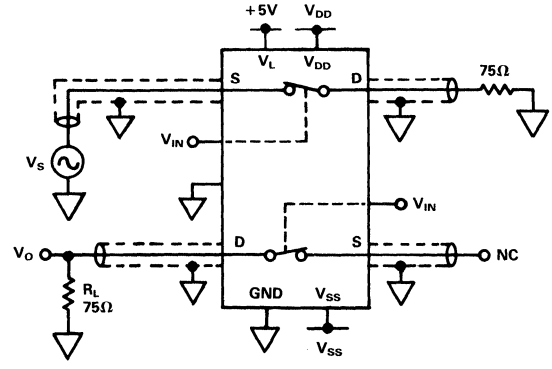




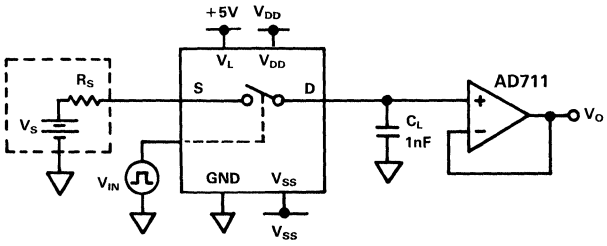
Test Circuit 5

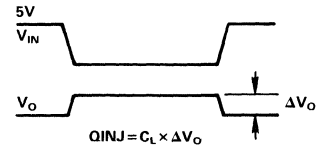


Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk





Test Circuit 8. Charge Injection

ANALOG DEVICES

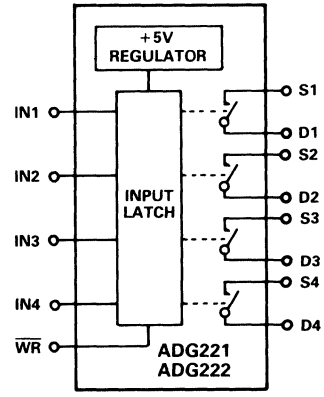
CMOS Quad SPST Switches

ADG221/ADG222

FEATURES

- 44V Supply Maximum Rating
- ± 15V Analog Signal Range
- Low R_{ON} (60Ω)
- Low Leakage (0.5nA)
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (25.5mW)
- µP, TTL, CMOS Compatible
- Standard 16-Pin DIPs and 20-Terminal Surface Mount Packages
- Superior DG221 Replacement

ADG221/ADG222 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG221 and ADG222 are monolithic CMOS devices comprising four independently selectable switches. On-chip latches facilitate microprocessor interfacing. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ± 15V. These switches also feature high switching speeds and low R_{ON}.

The ADG221 and ADG222 consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

ORDERING INFORMATION[1]

Temperature Range and Package Options[2, 3]		
−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP (N-16)	**Hermetic (Q-16)**	**Hermetic (Q-16)**
ADG221KN	ADG221BQ	ADG221TQ
ADG222KN	ADG222BQ	ADG222TQ
PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
ADG221KP		ADG221TE
ADG222KP		ADG222TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See Analog Devices Military Products Data Book (1987) for military data sheet.
[2]See Section 14 for package outline information.
[3]Also available in SOIC packages (ADG221KR, ADG222KR).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

PRODUCT HIGHLIGHTS

1. Easily Interfaced:
   Digital inputs are latched with a $\overline{WR}$ signal for microprocessor interfacing. A 5V regulated supply is internally generated permitting wider tolerances on the supplies without affecting the TTL digital input switching levels.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

$\overline{WR}$	ADG221 IN	ADG222 IN	SWITCH CONDITION
0	0	1	ON
0	1	0	OFF
1	X	X	Retains Previous Switch Condition

Table I. Truth Table

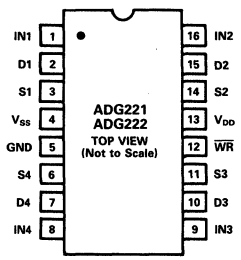
SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, unless otherwise noted)

Parameter	K Version 25°C	K Version −40°C to +85°C	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}	60		60		60		Ω typ	−10V≤V_S≤+10V
	90	145	90	145	90	145	Ω max	I_{DS} = 1.0mA
								Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S ∓14V; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)	0.5		0.5		0.5		nA typ	V_D = ±14V; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[1]	300		300		300		ns max	Test Circuit 4
t_{OFF}[1]	250		250		250		ns max	Test Circuit 4
t_W[1] Write Pulse Width		100		100	100	120	ns min	
t_S[1] Digital Input Setup Time		100		100	100	120	ns min	
t_H[1] Digital Input Hold Time		20		20	20	20	ns min	
OFF Isolation	80		80		80		dB typ	V_S = 10V (p-p); f = 100kHz
								R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_D, C_S (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V
								Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		1.5		1.5		1.5	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		25.5		25.5		25.5	mW max	

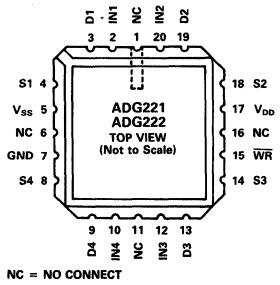
NOTE
[1]Sample tested at 25°C to ensure compliance.
t_{ON}, t_{OFF} are the same for both IN and $\overline{WR}$ digital input changes.
Specifications subject to change without notice.

PIN CONFIGURATIONS

DIP

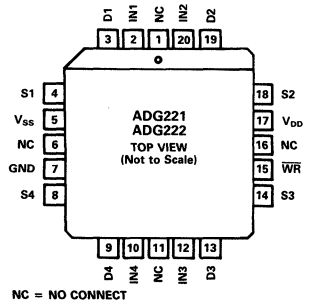


LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise stated)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
Voltage at S, D . . . . . V_{SS} −0.3V to V_{DD} +0.3V
Continuous Current, S or D 30mA
Pulsed Current S or D
1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[1]
Voltage at IN, $\overline{WR}$ . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First

Power Dissipation (Any Package)
Up to +75°C 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

NOTE
[1]Overvoltage at IN, $\overline{WR}$, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

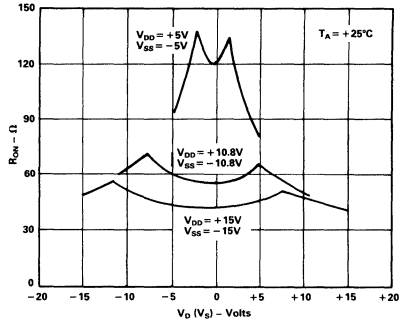
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

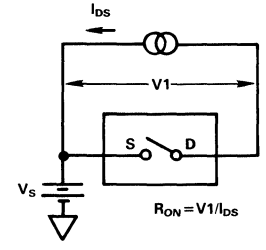
7

Typical Performance Characteristics and Test Circuits

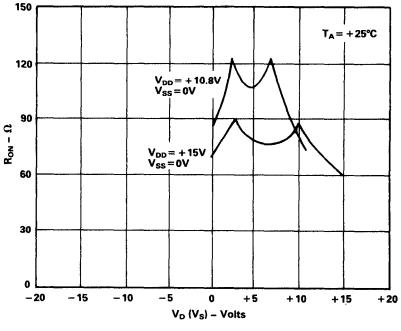
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



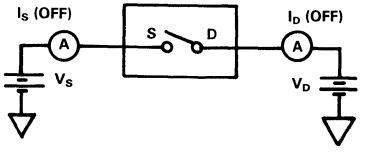
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



Test Circuit 1

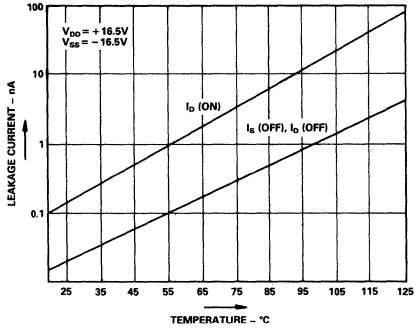


R_{ON} as a Function of V_D (V_S): Single Supply Voltage

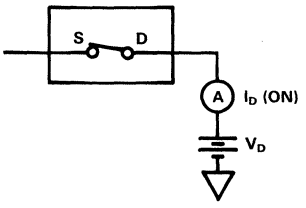


Test Circuit 2

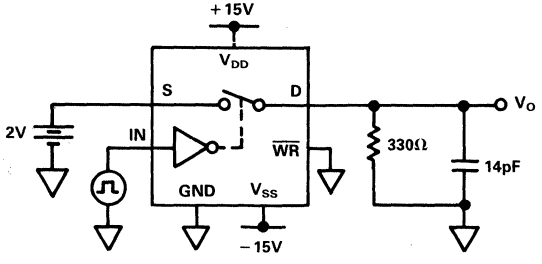
Typical Performance Characteristics and Test Circuits Cont'd

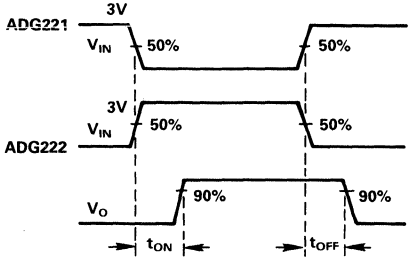


Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

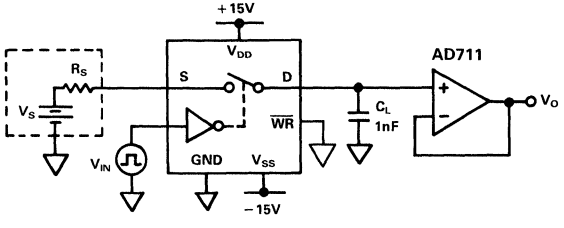


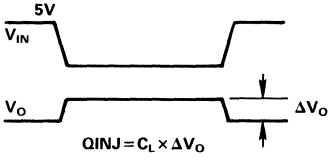
Test Circuit 3



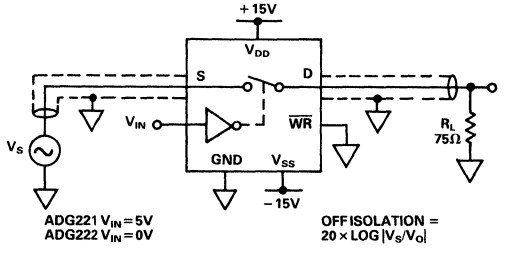


Test Circuit 4

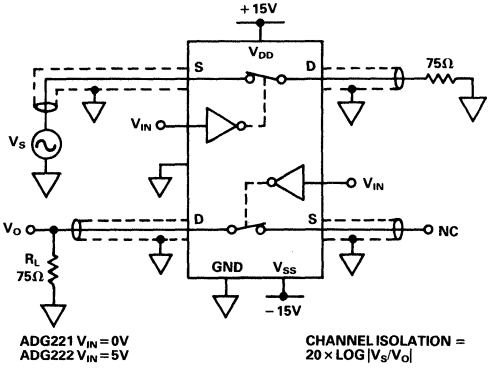




Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation



Test Circuit 7. Channel to Channel Isolation

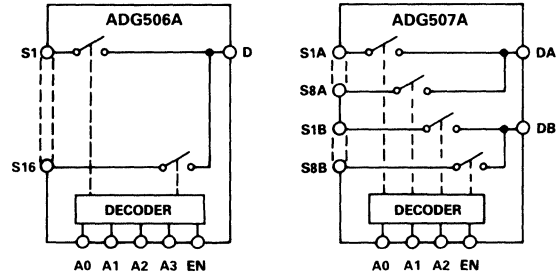
ANALOG DEVICES

CMOS 8/16 Channel Analog Multiplexers

ADG506A/ADG507A

FEATURES
44V Supply Maximum Rating
V_{SS} to V_{DD} Analog Signal Range
Single/Dual Supply Specifications
Wide Supply Ranges (10.8V to 16.5V)
Extended Plastic Temperature Range (−40°C to +85°C)
Low Power Dissipation (28mW max)
Low Leakage (20pA typ)
Superior Alternative to:
DG506A, HI-506
DG507A, HI-507

ADG506A/ADG507A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG506A and ADG507A are CMOS monolithic analog multiplexers with 16 channels and dual 8 channels respectively. The ADG506A switches one of 16 inputs to a common output depending on the state of four binary addresses and an enable input. The ADG507A switches one of 8 differential inputs to a common differential output depending on the state of three binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG506A and ADG507A are designed on an enhanced LC^2MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Extended Signal Range:
   The enhanced LC^2MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
3. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

ORDERING INFORMATION[1]

Temperature Range and Package Options[2]

−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP (N-28)	**Hermetic (Q-28)**	**Hermetic (Q-28)**
ADG506AKN	ADG506ABQ	ADG506ATQ
ADG507AKN	ADG507ABQ	ADG507ATQ
PLCC[3] (P-28A)		**LCCC[4] (E-28A)**
ADG506AKP		ADG506ATE
ADG507AKP		ADG507ATE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

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SPECIFICATIONS

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted)

	ADG506A ADG507A K Version		ADG506A ADG507A B Version		ADG506A ADG507A T Version			
Parameter	+25°C	−40°C to +85°C	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C	**Units**	**Comments**
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
R_{ON} Match	5		5		5		% typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 3
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A only)		25		25		25	nA max	V1 = ±10V, V2 = ∓10V; Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = =0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	V1 = ±10V, V2 = ∓10V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON}(EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
t_{OFF}(EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted)

Parameter	ADG506A ADG507A K Version +25°C	ADG506A ADG507A K Version −40°C to +85°C	ADG506A ADG507A B Version +25°C	ADG506A ADG507A B Version −40°C to +85°C	ADG506A ADG507A T Version +25°C	ADG506A ADG507A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	$0V \le V_S \le +10V$, $I_{DS} = 0.5mA$; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	$0V \le V_S \le +10V$, $I_{DS} = 0.5mA$
R_{ON} Match	5		5		5		% typ	$0V \le V_S \le +10V$, $I_{DS} = 0.5mA$
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG506A	1	200	1	200	1	200	nA max	Test Circuit 3
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG506A	1	200	1	200	1	200	nA max	Test Circuit 4
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A only)		25		25		25	nA max	V1 = +10V/0V, V2 = 0V/+10V; Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	300		300		300		ns typ	V1 = +10V/0V, V2 = 0V/+10V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
t_{OFF} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	$V_{IN} = V_{INL}$ or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

TRUTH TABLES

A3	A2	A1	A0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

X = Don't Care

ADG506A

A2	A1	A0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

ADG507A

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	40mA
Digital Inputs[1]	
Voltage at A, EN	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commercial (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTE
[1]Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

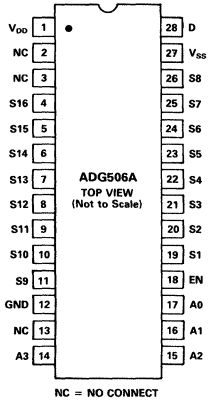
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

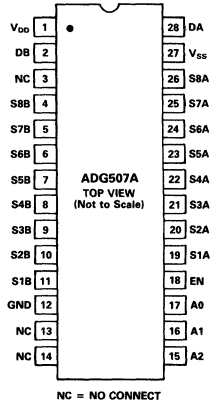
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

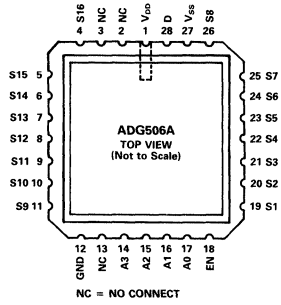
PIN CONFIGURATIONS

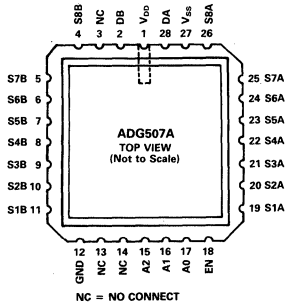
DIP



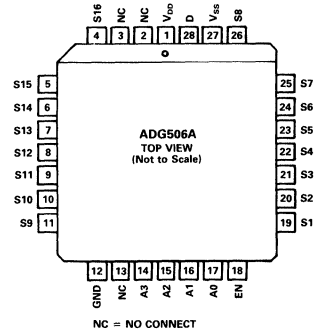


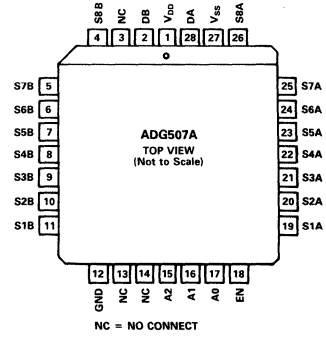
LCCC



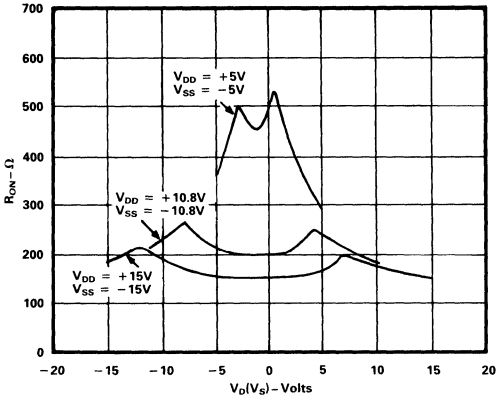


PLCC

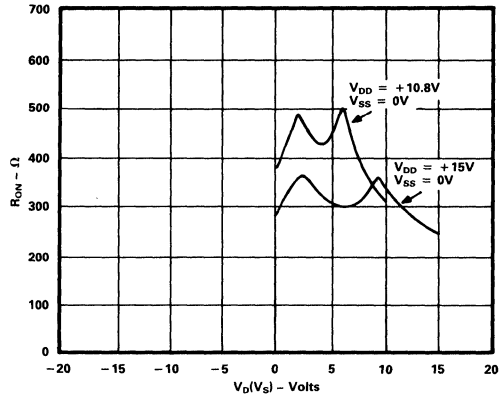




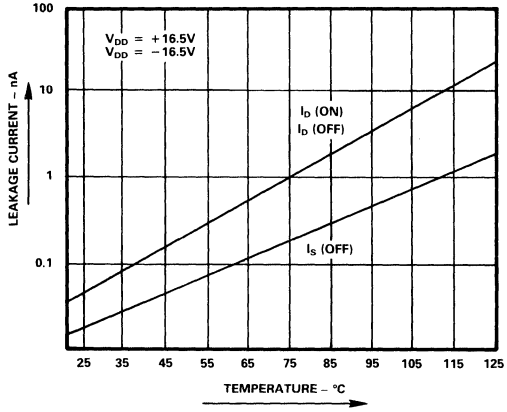
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



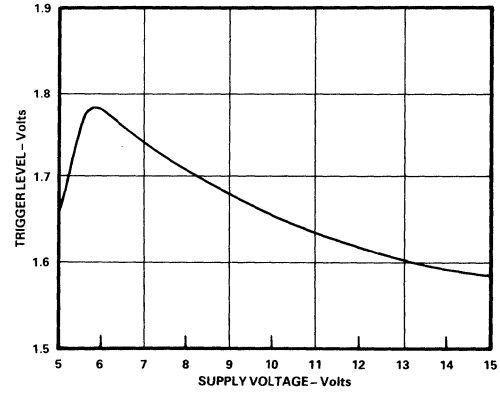
R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, T_A = +25°C



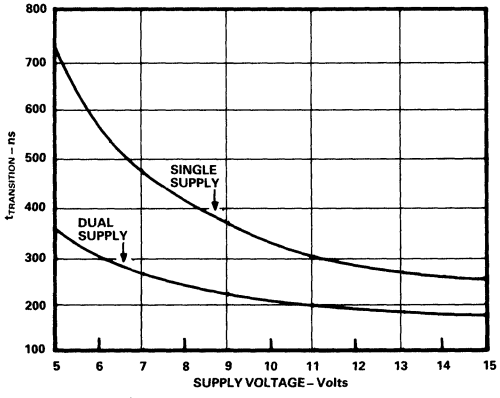
R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, T_A = +25°C



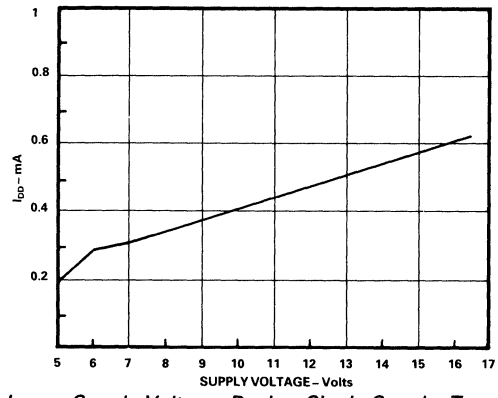
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C



$t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = +25°C (Note: For V_{DD} and $|V_{SS}| < 10V$; $V1 = V_{DD}/V_{SS}$, $V2 = V_{SS}/V_{DD}$. See Test Circuit 6)

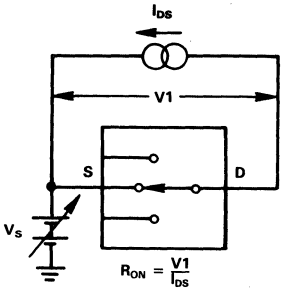


I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C

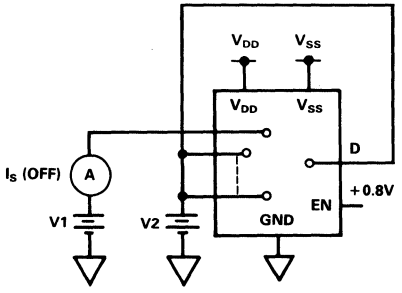
Test Circuits

Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

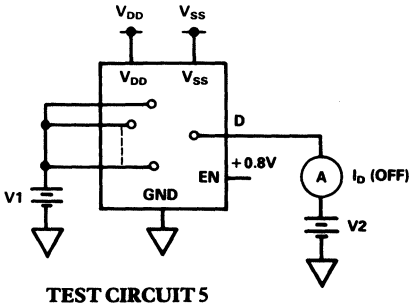
TEST CIRCUIT 1
R_{ON}



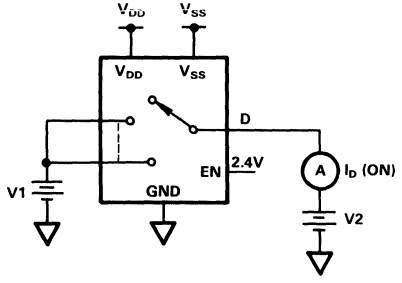
TEST CIRCUIT 2
I_S (OFF)



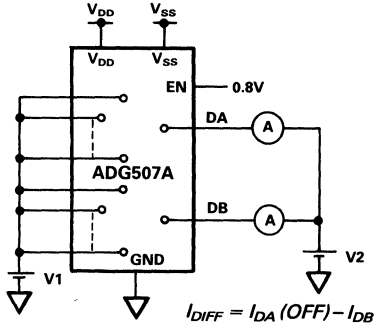
TEST CIRCUIT 3
I_D (OFF)



TEST CIRCUIT 4
I_D (ON)

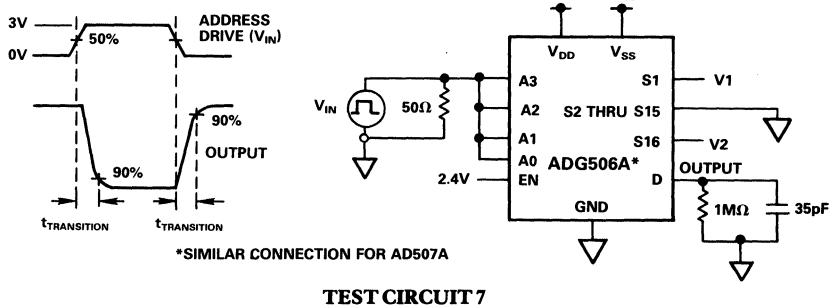


TEST CIRCUIT 5
I_{DIFF}



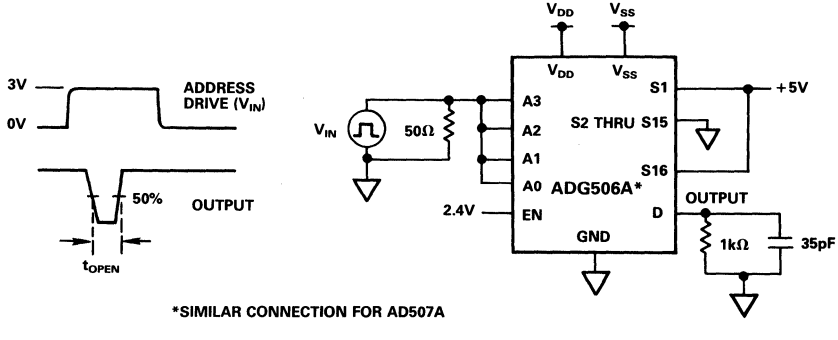
$I_{DIFF} = I_{DA}(OFF) - I_{DB}(OFF)$

TEST CIRCUIT 6
SWITCHING TIME OF MULTIPLEXER, $t_{TRANSITION}$



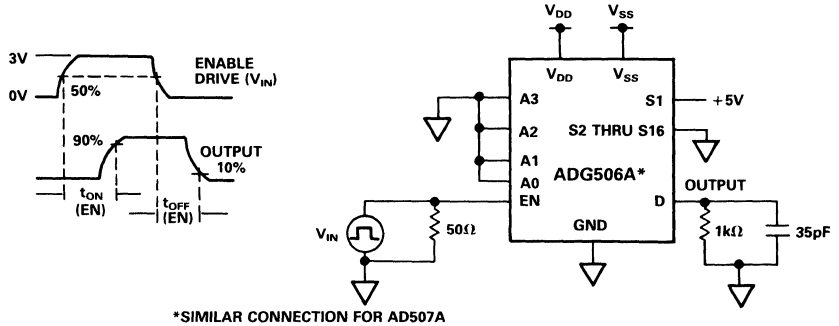
*SIMILAR CONNECTION FOR AD507A

TEST CIRCUIT 7
BREAK-BEFORE-MAKE DELAY, t_{OPEN}



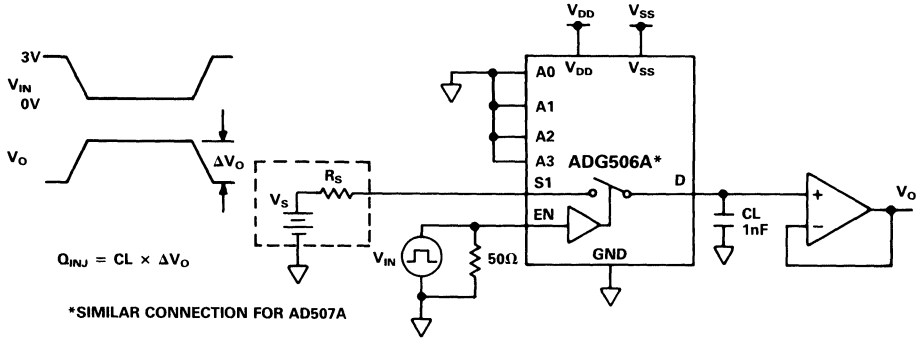
*SIMILAR CONNECTION FOR AD507A

TEST CIRCUIT 8
ENABLE DELAY, t_{ON} (EN), t_{OFF} (EN)



*SIMILAR CONNECTION FOR AD507A

TEST CIRCUIT 9
CHARGE INJECTION

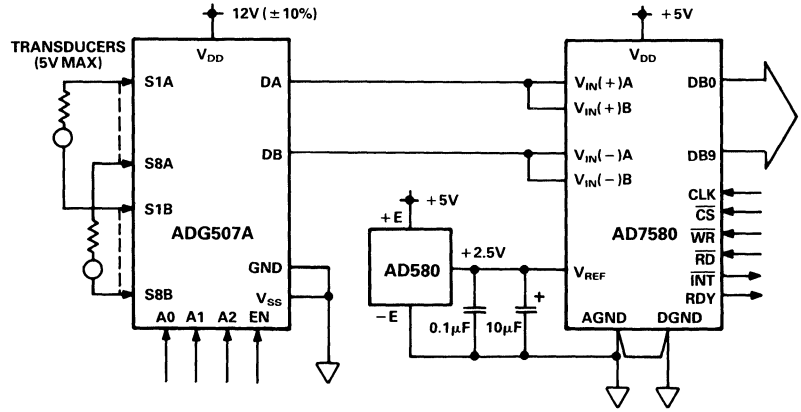


*SIMILAR CONNECTION FOR AD507A

SINGLE SUPPLY AUTOMOTIVE APPLICATION

The excellent performance of the multiplexers under single supply conditions makes the ADG506A/ADG507A suitable in applications, such as automotive and disc drives, where only positive power supply voltages are normally available. The following application circuit shows the ADG507A connected as an 8-channel differential multiplexer in an automotive, data acquisition application circuit.

The AD7580 is a 10-bit successive approximation ADC which has an on-chip sample-hold amplifier and provides a conversion result in 20μs. The ADC has a differential analog inputs and is configured in the application circuit for a span of 2.5V over a common-mode range 0 to +5V. Wider common-mode ranges can be accomodated. See the AD7579/AD7580 data sheet for more details. The complete system operates from +12V (±10%) and +5V supplies. The analog input signals to the ADG507A contain information such as temperature, pressure, speed etc.



ADG507A in a Single Supply Automotive Data Acquisition Application.

TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

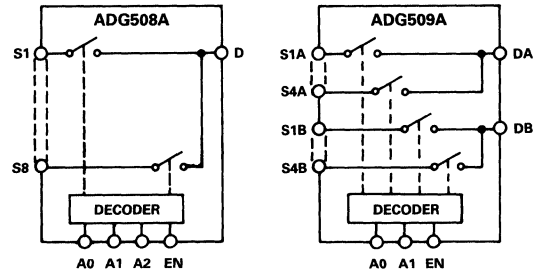
ANALOG DEVICES

CMOS 4/8 Channel Analog Multiplexers

ADG508A/ADG509A

FEATURES
- **44V Supply Maximum Rating**
- **V_{SS} to V_{DD} Analog Signal Range**
- **Single/Dual Supply Specifications**
- **Wide Supply Ranges (10.8V to 16.5V)**
- **Extended Plastic Temperature Range (−40°C to +85°C)**
- **Low Power Dissipation (28mW max)**
- **Low Leakage (20pA typ)**
- **Superior Alternative to:**
  - **DG508A, HI-508**
  - **DG509A, HI-509**

ADG508A/ADG509A FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG508A and ADG509A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. The ADG508A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG509A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG508A and ADG509A are designed on an enhanced LC^{2}MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Extended Signal Range:
   The enhanced LC^{2}MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
3. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

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ORDERING INFORMATION[1]

Temperature Range and Package Options[2,3]

−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP (N-16)	**Hermetic (Q-16)**	**Hermetic (Q-16)**
ADG508AKN	ADG508ABQ	ADG508ATQ
ADG509AKN	ADG509ABQ	ADG509ATQ
PLCC[4] (P-20A)		**LCCC[5] (E-20A)**
ADG508AKP		ADG508ATE
ADG509AKP		ADG509ATE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD), see DESC drawing #5962-77052.
[2]See Section 14 for package outline information.
[3]Also available in SOIC packages (ADG508AKR, ADG509AKR).
[4]PLCC: Plastic Leaded Chip Carrier.
[5]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted)

	ADG508A ADG509A K Version		ADG508A ADG509A B Version		ADG508A ADG509A T Version			
Parameter	+25°C	−40°C to +85°C	25°C	−40°C to +85°C	+25°C	−55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V min V max	
R_{ON}	280		280		280		Ω typ	−10V≤V_S≤+10V, I_{DS} = 1mA
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	V_S = 0, I_{DS} = 1mA
R_{ON} Match	5		5		5		% typ	−10V≤V_S≤+10V, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V_{S1} = ±10V, V_D = V_{S2} to V_{SN} = ∓10V
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V_{S1} to V_{SN} = ±10V, V_D = ∓10V
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V_{S2} to V_{SN} = ±10V, V_D = V_{S1} = ∓10V
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	$V_{S1A/B}$ to $V_{S4A/B}$ = ±10V, V_{DA} = V_{DB} = ∓10V
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	R_L = 1MΩ, C_L = 35pF
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	R_L = 1kΩ, C_L = 35pF
	25	10	25	10	25	10	ns min	
t_{ON}(EN)[1]	200		200		200		ns typ	R_L = 1kΩ, C_L = 35pF
	300	400	300	400	300	400	ns max	
t_{OFF}(EN)[1]	200		200		200		ns typ	R_L = 1kΩ, C_L = 35pF
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG508A	22		22		22		pF typ	V_{EN} = 0.8V
ADG509A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, C_L = 1000pF, V_S = 0V
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted)

Parameter	ADG508A ADG509A K Version +25°C	ADG508A ADG509A K Version −40°C to +85°C	ADG508A ADG509A B Version +25°C	ADG508A ADG509A B Version −40°C to +85°C	ADG508A ADG509A T Version +25°C	ADG508A ADG509A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	GND≤V_S≤+10V, I_{DS} = 0.5mA
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	V_S = 0, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	GND≤V_S≤+10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V_{S1} = +10V/GND, V_D = V_{S2} to V_{SN} = GND/+10V
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V_{S1} to V_{SN} = +10V/GND, V_D = GND/+10V
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V_{S2} to V_{SN} = +10V/GND, V_D = V_{S1} = GND/+10V
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	$V_{S1A/B}$ to $V_{S4A/B}$ = +10V/GND, V_{DA} = V_{DB} = GND/+10V
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	300		300		300		ns typ	R_L = 1MΩ, C_L = 35pF
	450	600	450	600	450	600	ns max	
t_{OPEN}[1]	50		50		50		ns typ	R_L = 1kΩ, C_L = 35pF
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	250		250		250		ns typ	R_L = 1kΩ, C_L = 35pF
	450	600	450	600	450	600	ns max	
t_{OFF} (EN)[1]	250		250		250		ns typ	R_L = 1kΩ, C_L = 35pF
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG508A	22		22		22		pF typ	V_{EN} = 0.8V
ADG509A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, C_L = 1000pF, V_S = 0V
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

TRUTH TABLES

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care *ADG508A*

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care *ADG509A*

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	40mA
Digital Inputs[1]	
Voltage at A, EN	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commercial (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 10sec)	+300°C

NOTE
[1]Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

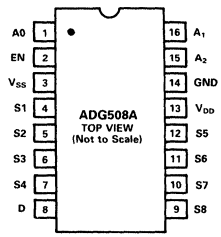
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

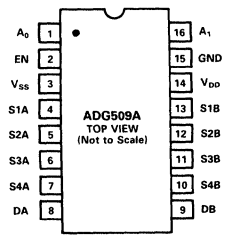
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

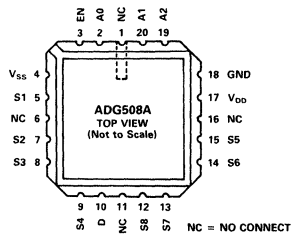
PIN CONFIGURATIONS

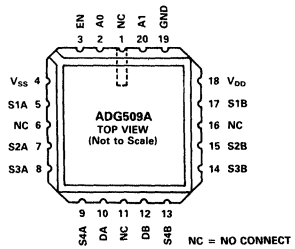
DIP



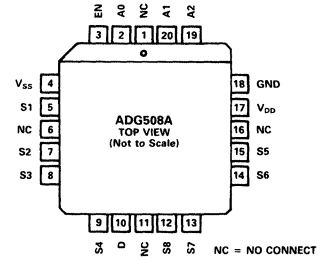


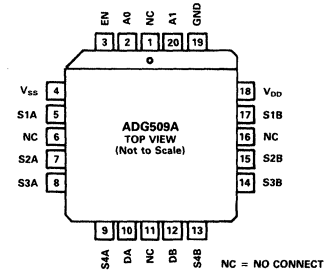
LCCC





PLCC





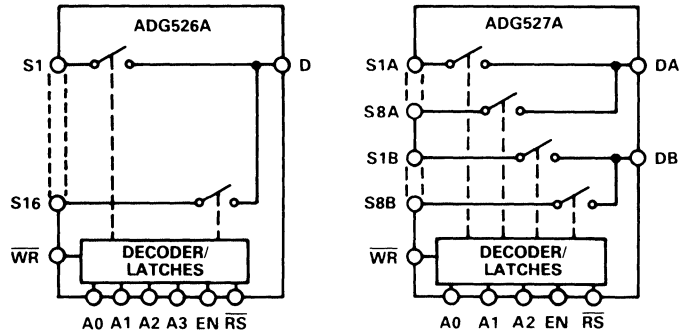
CMOS Latched 8/16 Channel Analog Multiplexers

ADG526A/ADG527A

FEATURES

- **44V Supply Maximum Rating**
- **V_{SS} to V_{DD} Analog Signal Range**
- **Single/Dual Supply Specifications**
- **Wide Supply Ranges (10.8V to 16.5V)**
- **Microprocessor Compatible (100ns $\overline{WR}$ Pulse)**
- **Extended Plastic Temperature Range (−40°C to +85°C)**
- **Low Leakage (20pA typ)**
- **Low Power Dissipation (28mW max)**
- **Superior Alternative to:**
  - **DG526**
  - **DG527**

ADG526A/ADG527A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG526A and ADG527A are CMOS monolithic analog multiplexers with 16 channels and dual 8 channels respectively. On-chip latches facilitate microprocessor interfacing. The ADG526A switches one of 16 inputs to a common output depending on the state of four binary addresses and an enable input. The ADG527A switches one of 8 differential inputs to a common differential output depending on the state of three binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG526A and ADG527A are designed on an enhanced LC²MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Easily Interfaced:
   The ADG526A and ADG527A can be easily interfaced with microprocessors. The $\overline{WR}$ signal latches the state of the Address control lines and the Enable line. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off). $\overline{RS}$ can be tied to the microprocessor reset pin.
3. Extended Signal Range:
   The enhanced LC²MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
4. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

ORDERING INFORMATION[1]

Temperature Range and Package Options[2]

−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP (N-28)	**Hermetic (Q-28)**	**Hermetic (Q-28)**
ADG526AKN	ADG526ABQ	ADG526ATQ
ADG527AKN	ADG527ABQ	ADG527ATQ
PLCC[3] (P-28A)		**LCCC[4] (E-28A)**
ADG526AKP		ADG526ATE
ADG527AKP		ADG527ATE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted)

	ADG526A ADG527A K Version		ADG526A ADG527A B Version		ADG526A ADG527A T Version			
Parameter	+25°C	−40°C to +85°C	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V min V max	
R_{ON}	280		280		280		Ω typ	−10V≤V_S≤+10V, I_{DS} = 1mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	−10V≤V_S≤+10V, I_{DS} = 1mA
R_{ON} Match	5		5		5		% typ	−10V≤V_S≤+10V, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 3
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 4
ADG526A	1	200	1	200	1	200	nA max	
ADG527A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG527A only)		25		25		25	nA max	V1 = ±10V, V2 = ∓10V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	200		200		200		ns typ	V1 = ±10V, V2 = ∓10V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	200		200		200		ns typ	Test Circuits 8 and 9
	300	400	300	400	300	400	ns max	
t_{OFF} (EN, $\overline{RS}$)	200		200		200		ns typ	Test Circuits 8 and 10
	300	400	300	400	300	400	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG526A	44		44		44		pF typ	V_{EN} = 0.8V
ADG527A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 11
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted)

Parameter	ADG526A ADG527A K Version +25°C	ADG526A ADG527A K Version −40°C to +85°C	ADG526A ADG527A B Version +25°C	ADG526A ADG527A B Version −40°C to +85°C	ADG526A ADG527A T Version +25°C	ADG526A ADG527A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V_{SS} V_{DD}	V min V max	
R_{ON}	500		500		500		Ω typ	0V≤V_S≤+10V, I_{DS} = 0.5mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	0V≤V_S≤+10V, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	0V≤V_S≤+10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG526A	1	200	1	200	1	200	nA max	Test Circuit 3
ADG527A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG526A	1	200	1	200	1	200	nA max	Test Circuit 4
ADG527A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG527A only)		25		25		25	nA max	V1 = +10V/0V, V2 = 0V/+10V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	300		300		300		ns typ	V1 = +10V/0V, V2 = 0V/+10V;
	450	600	450	600	450	600	ns max	Test Circuit 6
t_{OPEN}	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	250		250		250		ns typ	Test Circuits 8 and 9
	450	600	450	600	450	600	ns max	
t_{OFF} (EN, $\overline{RS}$)	250		250		250		ns typ	Test Circuits 8 and 10
	450	600	450	600	450	600	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG526A	44		44		44		pF typ	V_{EN} = 0.8V
ADG527A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 11
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	11		11		11		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

7

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
Voltage at S, D . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D 20mA
Pulsed Current S or D
1ms Duration, 10% Duty Cycle 40mA
Digital Inputs[1]
Voltage at A, EN, $\overline{WR}$, $\overline{RS}$ . . . . . V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)
Up to +75°C 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commerical (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

NOTE
[1]Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by diodes. Current should be limited to the maximum rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLES

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

X = Don't Care

ADG526A

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

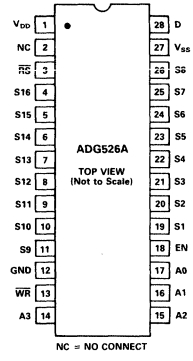
X = Don't Care

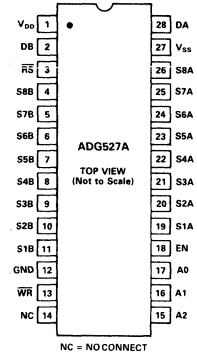
ADG527A

CAUTION
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

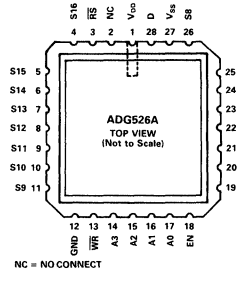
PIN CONFIGURATIONS

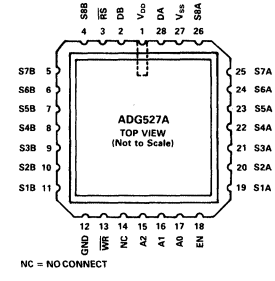
DIP



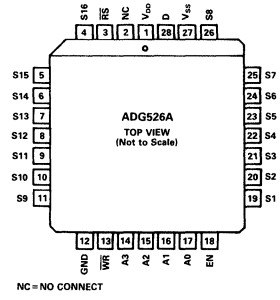


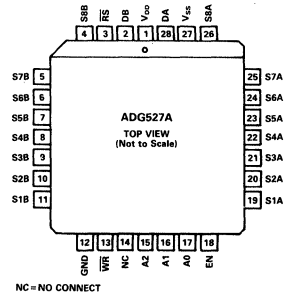
LCCC





PLCC





TIMING DIAGRAMS

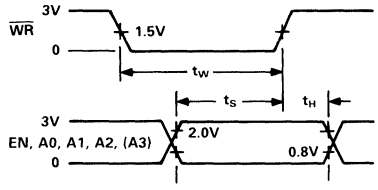


Figure 1

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

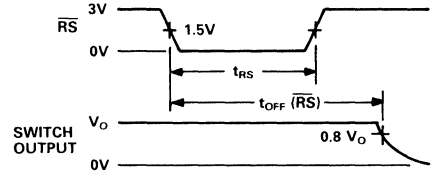


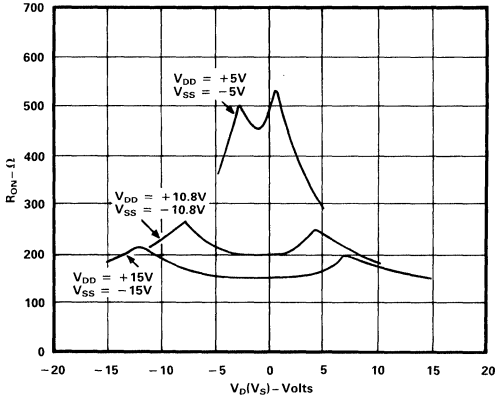
Figure 2

Figure 2 shows the Reset Pulse Width, t_{RS}, and Reset Turn-off Time, t_{OFF} ($\overline{RS}$).

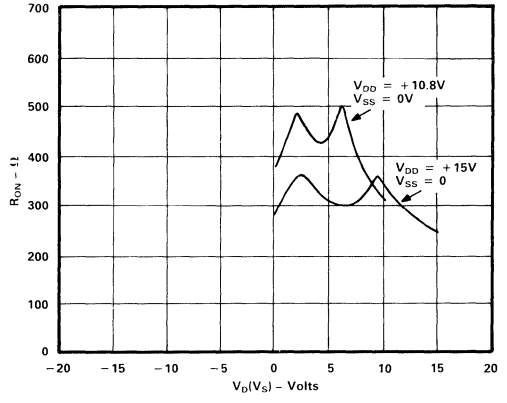
Note: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

Typical Performance Characteristics

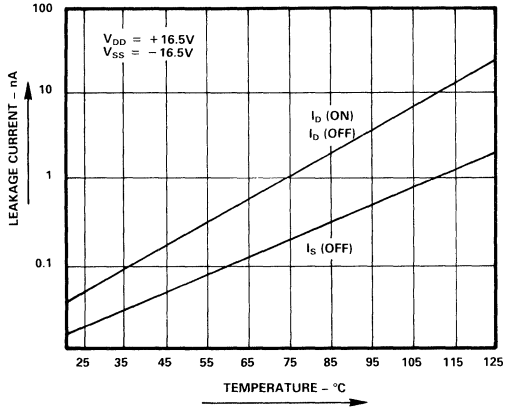
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



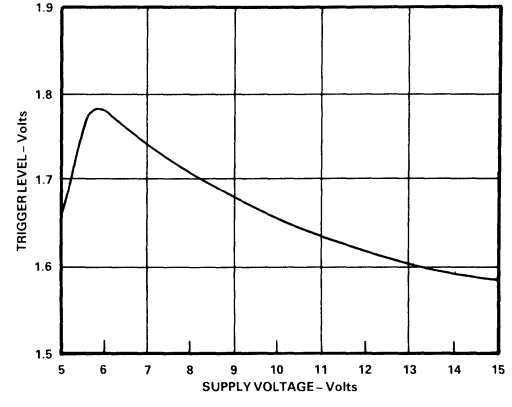
R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, T_A = +25°C



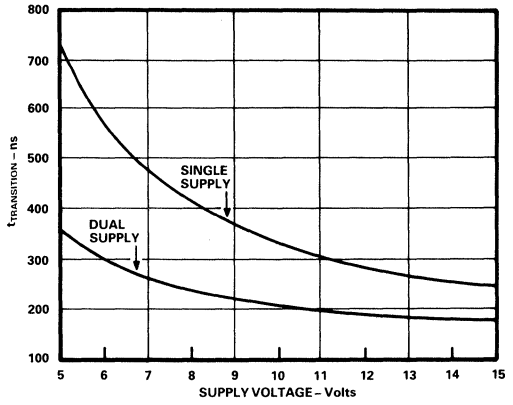
R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, T_A = +25°C



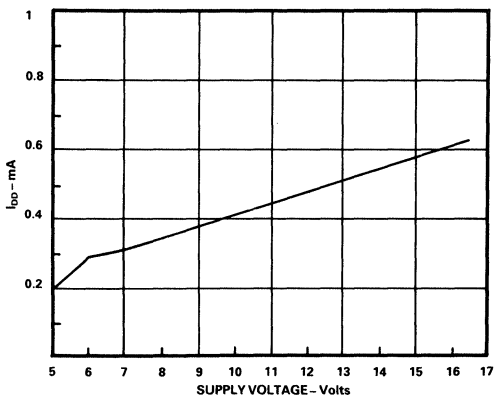
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C



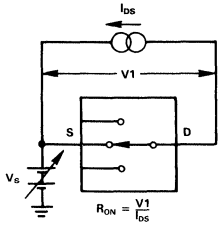
$t_{TRANSITION}$ vs Supply Voltage: Dual and Single Supplies, T_A = +25°C
(Note: For V_{DD} and $|V_{SS}| < 10V$; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}. See Test Circuit 6)



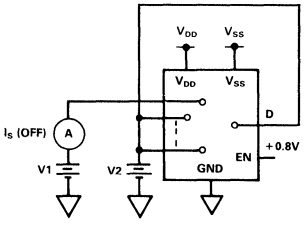
I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C

Test Circuits

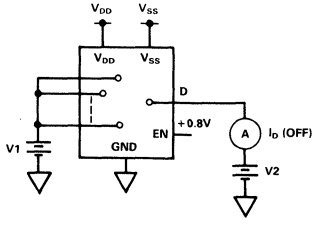
TEST CIRCUIT 1
R_{ON}



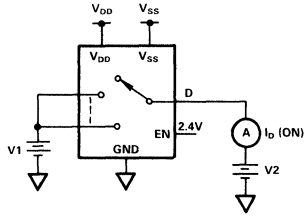
TEST CIRCUIT 2
I_S (OFF)



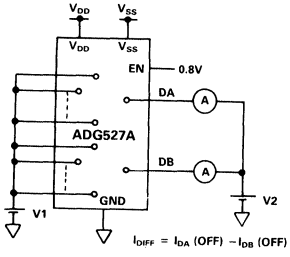
TEST CIRCUIT 3
I_D (OFF)



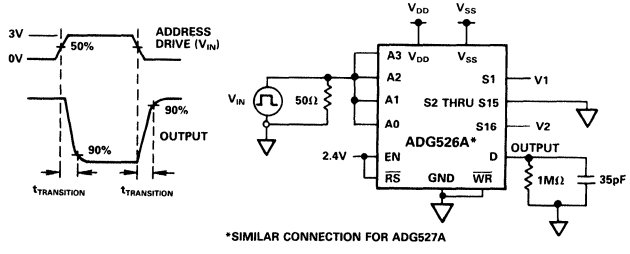
TEST CIRCUIT 4
I_D (ON)



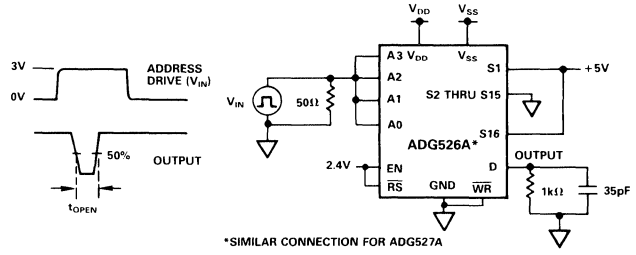
TEST CIRCUIT 5
I_{DIFF}



TEST CIRCUIT 6
SWITCHING TIME OF MULTIPLEXER, $t_{TRANSITION}$

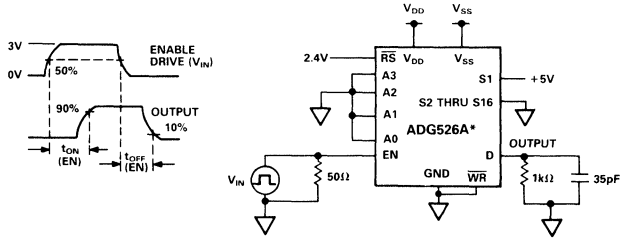


TEST CIRCUIT 7
BREAK-BEFORE-MAKE DELAY, t_{OPEN}



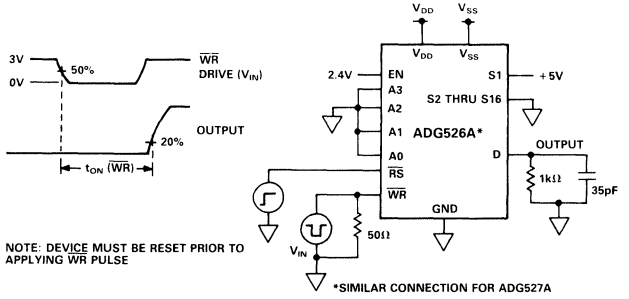
*SIMILAR CONNECTION FOR ADG527A

TEST CIRCUIT 8
ENABLE DELAY, t_{ON} (EN), t_{OFF} (EN)



*SIMILAR CONNECTION FOR ADG527A

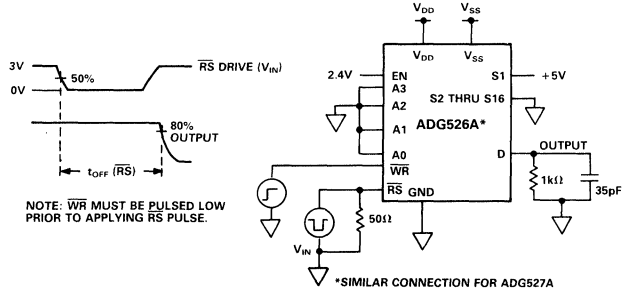
TEST CIRCUIT 9
WRITE TURN-ON TIME, t_{ON} ($\overline{WR}$)



NOTE: DEVICE MUST BE RESET PRIOR TO APPLYING WR PULSE

*SIMILAR CONNECTION FOR ADG527A

TEST CIRCUIT 10
RESET TURN-OFF TIME, t_{OFF} ($\overline{RS}$)

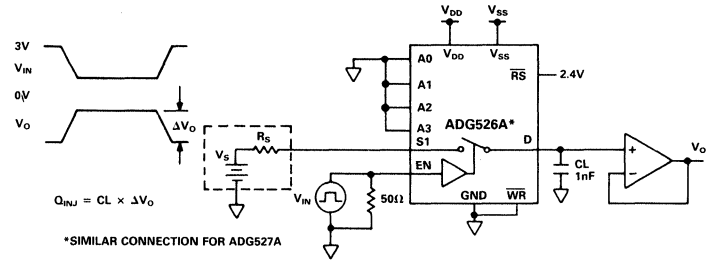


NOTE: WR MUST BE PULSED LOW PRIOR TO APPLYING RS PULSE.

*SIMILAR CONNECTION FOR ADG527A

7

TEST CIRCUIT 11
CHARGE INJECTION



TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

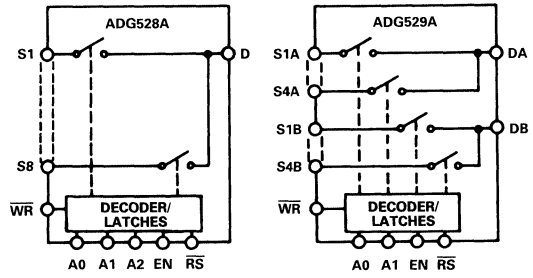
ANALOG DEVICES

CMOS Latched 4/8 Channel Analog Multiplexers

ADG528A/ADG529A

FEATURES
44V Supply Maximum Rating
V_{SS} to V_{DD} Analog Signal Range
Single/Dual Supply Specifications
Wide Supply Ranges (10.8V to 16.5V)
Microprocessor Compatible (100ns $\overline{WR}$ Pulse)
Extended Plastic Temperature Range
(−40°C to +85°C)
Low Leakage (20pA typ)
Low Power Dissipation (28mW max)
Superior Alternative to:
DG528
DG529

ADG528A/ADG529A FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG528A and ADG529A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. On-chip latches facilitate microprocessor interfacing. The ADG528A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG529A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG528A and ADG529A are designed on an enhanced LC^{2}MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

ORDERING INFORMATION[1]

Temperature Range and Package Options[2]

−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP (N-18)	**Hermetic (Q-18)**	**Hermetic (Q-18)**
ADG528AKN	ADG528ABQ	ADG528ATQ
ADG529AKN	ADG529ABQ	ADG529ATQ
PLCC[3] (P-20A)		**LCCC[4] (E-20A)**
ADG528AKP		ADG528ATE
ADG529AKP		ADG529ATE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Easily Interfaced:
   The ADG528A and ADG529A can be easily interfaced with microprocessors. The $\overline{WR}$ signal latches the state of the address control lines and the enable line. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off). $\overline{RS}$ can be tied to the microprocessor reset pin.
3. Extended Signal Range:
   The enhanced LC^{2}MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
4. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

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SPECIFICATIONS

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted)

Parameter	ADG528A ADG529A K Version +25°C	ADG528A ADG529A K Version −40°C to +85°C	ADG528A ADG529A B Version +25°C	ADG528A ADG529A B Version −40°C to +85°C	ADG528A ADG529A T Version +25°C	ADG528A ADG529A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	$-10V \le V_S \le +10V$, I_{DS} = 1mA
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	$-10V \le V_S \le +10V$, I_{DS} = 1mA
R_{ON} Match	5		5		5		% typ	$-10V \le V_S \le +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	$V_{S1} = \pm 10V$, $V_D = V_{S2}$ to $V_{SN} = \mp 10V$
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V_{S1} to $V_{SN} = \pm 10V$, $V_D = \mp 10V$
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V_{S2} to $V_{SN} = \pm 10V$, $V_D = V_{Si} = \mp 10V$
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	$V_{S1A/B}$ to $V_{S4A/B} = \pm 10V$, $V_{DA} = V_{DB} = \mp 10V$
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	200		200		200		ns typ	R_L = 1MΩ, C_L = 35pF
	300	400	300	400	300	400	ns max	
t_{OPEN}	50		50		50		ns typ	R_L = 1kΩ, C_L = 35pF
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	200		200		200		ns typ	R_L = 1kΩ, C_L = 35pF
	300	400	300	400	300	400	ns max	
t_{OFF} (EN, $\overline{RS}$)	200		200		200		ns typ	R_L = 1kΩ, C_L = 35pF
	300	400	300	400	300	400	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG528A	22		22		22		pF typ	V_{EN} = 0.8V
ADG529A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, C_L = 1000pF, V_S = 0V
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	$V_{IN} = V_{INL}$ or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted)

Parameter	ADG528A ADG529A K Version +25°C	K Version −40°C to +85°C	ADG528A ADG529A B Version +25°C	B Version −40°C to +85°C	ADG528A ADG529A T Version +25°C	T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	GND	GND	GND	GND	GND	GND	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	GND≤V_S≤+10V, I_{DS} = 0.5mA
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	GND≤V_S≤+10V, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	GND≤V_S≤+10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V_{S1} = +10V/GND, V_D = V_{S2} to V_{SN} = GND/+10V
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V_{S1} to V_{SN} = +10V/GND, V_D = GND/+10V
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V_{S2} to V_{SN} = +10V/GND, V_D = V_{S1} = GND/+10V
ADG528A	1	100	1	100	1	100	nA max	
ADG529A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	$V_{S1A/B}$ to $V_{S4A/B}$ = +10V/GND, V_{DA} = V_{DB} = GND/+10V
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS[1]								
$t_{TRANSITION}$	300		300		300		ns typ	R_L = 1mΩ, C_L = 35pF
	450	600	450	600	450	600	ns max	
t_{OPEN}	50		50		50		ns typ	R_L = 1kΩ, C_L = 35pF
	25	10	25	10	25	10	ns min	
t_{ON} (EN, $\overline{WR}$)	250		250		250		ns typ	R_L = 1kΩ, C_L = 35pF
	450	600	450	600	450	600	ns max	
t_{OFF} (EN, $\overline{RS}$)	250		250		250		ns typ	R_L = 1kΩ, C_L = 35pF
	450	600	450	600	450	600	ns max	
t_W Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
t_S Address, Enable Setup Time		100		100		100	ns min	See Figure 1
t_H Address, Enable Hold Time		10		10		10	ns min	See Figure 1
t_{RS} Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG528A	22		22		22		pF typ	V_{EN} = 0.8V
ADG529A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, C_L = 1000pF, V_S = 0V
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	11		11		11		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

TRUTH TABLES

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

ADG528A

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	↓	1	Retains Previous Switch Condition
X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

X = Don't Care

ADG529A

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
Voltage at S, D . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D 20mA
Pulsed Current S or D
1ms Duration, 10% Duty Cycle 40mA
Digital Inputs[1]
Voltage at A, EN, $\overline{WR}$, $\overline{RS}$ . . . . . V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)
Up to +75°C 470mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
Commerical (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

NOTE
[1]Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by diodes. Current should be limited to the maximum rating above.

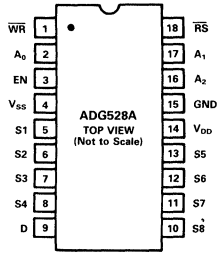
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

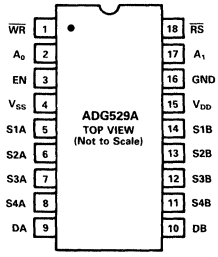
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

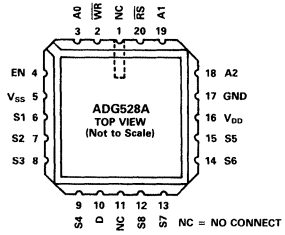
PIN CONFIGURATIONS

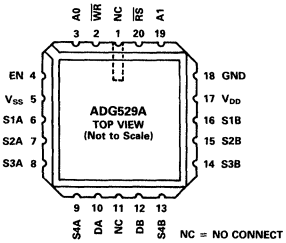
DIP



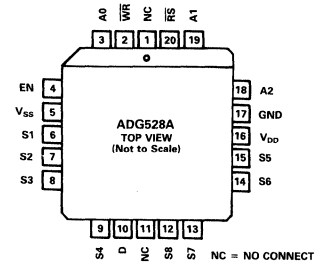


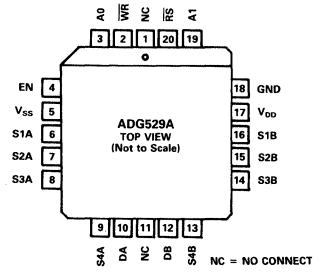
LCCC





PLCC





TIMING DIAGRAMS

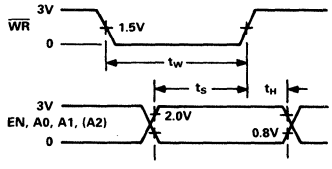


Figure 1

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

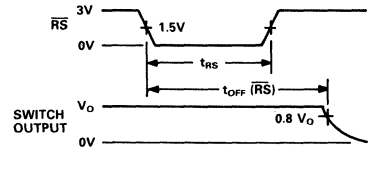


Figure 2

Figure 2 shows the Reset Pulse Width, t_{RS}, and Reset Turn-off Time, t_{OFF} ($\overline{RS}$).

Note: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

Voltage References
Contents

Selection Guide
Voltage References

Model	Ouput Voltage V	Initial Accuracy % F.S. max	Temp Stability ppm/°C max	Package Options[1]	Temp Range[2]	Page	Comments
AD589	**+1.235**	**1.2–2.8**	**10–100**	**H**	**C, M**	**8–51**	**Two Terminal, 1.2 V Reference**
AD580	**+2.5**	**0.4–3**	**10–85**	**H**	**C, M**	**8–5**	**Precision, Three Terminal, 2.5 V Reference**
AD1403	+2.5	0.4–1	25–40	N	C	8–63	Second Source, 2.5 V Reference
AD586	**+5**	**0.05–0.4**	**5–25**	**Q, R**	**C, M**	**8–23**	**Precision, Buried Zener 5 V Reference**
ADREF02	+5	0.3–0.5	8.5–25	Q	C, M	8–75	Second Source, 5 V Reference
AD689	**+8.129**	**0.05–0.2**	**5–25**	**Q**	**C, M**	**8–55**	**Precision, 8.192 Volt Reference**
AD2700	+10	0.025–0.05	3–10	D	C, M	8–67	Very High Precision 10 V Reference
AD581	+10	0.05–0.3	5–30	H	C, M	8–9	Three Terminal 10 V Bandgap Reference
AD587	**+10**	**0.05–0.1**	**5–20**	**Q, R**	**C, M**	**8–31**	**Precision Buried Zener 10 V Reference**
ADREF01	+10	0.3–0.5	8.5–25	Q	C, M	8–75	Second Source 10 V Reference
AD2710	**+10**	**0.01**	**1–5**	**N**	**C**	**8–71**	**Ultrahigh Precision 10 V Reference**
AD2712	**±10**	**0.01**	**1–5**	**N**	**C**	**8–71**	**Ultrahigh Precision ±10 V Reference**
AD2702	**±10**	**0.025–0.05**	**3–10**	**D**	**C, M**	**8–67**	**Very High Precision ±10 V Reference over Full Military Temp Range**
AD2701	**−10**	**0.025–0.05**	**3–10**	**D**	**C, M**	**8–67**	**Very High Precision −10 V Reference**
AD588	**Selectable**	**0.01–0.03**	**1.5–4**	**D**	**I, M**	**8–39**	**Ultrahigh Precision, Monolithic Programmable Reference**
AD584	**Selectable**	**0.05–0.3**	**5–30**	**E, H**	**C, M**	**8–15**	**Precision, Programmable Bandgap Reference**

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
Voltage References

A voltage reference is used to provide an accurately known voltage which can be utilized in a circuit or system. For example, measurement systems rely on precision references in order to establish a basis for absolute measurement accuracy. Any reference inaccuracy will undermine the accuracy of the overall system. Thus, ideal references are characterized by accurately set (and traceable to recognized fundamental standards) constant output voltage, independent of temperature, load changes, input voltage variation and time.

TYPES OF REFERENCES

Some of the available IC reference circuits use the bandgap principle: the V_{BE} of any silicon transistor has a negative tempco of about 2mV/°C, which can be extrapolated to approximately 1.2 volts at absolute zero (the *bandgap* voltage of silicon). Since identical transistors operating at constant current densities will have predictably different temperature coefficients of base-emitter voltage, it is possible to arrange circuit elements so as to null out the temperature coefficients associated with the two phenomena and produce a constant voltage (usually 1.2 volts). This temperature-invariant voltage can be amplified and buffered to produce a standard voltage value, such as 2.5V or 10.0V. The bandgap types cataloged here include the AD1403 and the AD580 (2.5V), the AD581 (10.0V) and the multi-output AD584 (2.5, 5.0, 7.5 and/or 10.0V).

Another popular form of reference circuit uses a selected low-drift Zener diode, followed by a buffer-amplifier-and-precision-gain stage to provide a standard output voltage.

A buried-Zener design provides lower noise and drift than bandgap references, with laser trimming of thin-film resistors for excellent accuracy and low drift versus temperature. This technique provides initial accuracy to ±1mV and temperature drifts as low as 1.5ppm in the AD588 (+10V, +5V, ±5V tracking, −5V and −10V outputs). Similar reference designs with single voltage outputs (AD586 and AD587, +5V and +10V respectively) have accuracies and temperature coefficients that are nearly as good as the AD588.

Several of the references allow the user to optionally connect a capacitor to a noise reduction pin on the IC and so further reduce the noise output of the reference. In the AD586, the wideband noise (to 1MHz) of 200μV peak-to-peak (p-p) is reduced to 160μV p-p by adding a 1μF capacitor to the noise reduction point.

Output current capability of the voltage reference must also be considered when selecting a reference. The amount of current that the reference must source, or sink, for the rest of the system affects which references are acceptable or may need additional buffering.

Kelvin connections provide output sense and force connections, so that the actual voltage at the load is sensed and any IR drops in the leads are compensated. The AD588 provides sense and force connections in its design.

DEFINITIONS OF SPECIFICATIONS

Line regulation. The change in output voltage due to a specified change in input voltage. It is usually expressed in percent per volt or microvolts per volt of input change.

Load regulation. The change in output voltage for a specified change in load current. It is generally expressed in microvolts per milliampere, or ohms of dc output resistance. This specification includes the effect of self-heating due to increased power dissipation at higher load currents.

Output voltage tolerance. The deviation from the nominal output voltage at 25°C and specified input voltage as measured by a device traceable to a recognized fundamental voltage standard.

Output voltage change with temperature. The change in output voltage from the value at 25°C ambient; it is independent of variations in the other operating conditions. Analog Devices specifies both an error band and an equivalent temperature coefficient (in ppm/°C) for most references. The error band (e.g., ±5mV, −55°C to +125°C) is defined graphically in terms of a box (voltage vertically, temperature horizontally) whose diagonals extend from 25°C to T_{max} and 25°C to T_{min}, with a slope equal to the stated temperature coefficient. Thus, the total absolute error for a particular reference over its specified temperature range is equal to the output voltage tolerance at 25°C plus the error band.

Turn-on settling time. The time, from a cold start, for the reference output to settle within a specified error band. This definition relates only to the electrical turn-on of the chip, and does not include thermal settling time which depends on the package, heat-sinking and load-current change.

Long-term stability. The change in output voltage versus time, specified in ppm/1000 hours.

Noise. The narrowband (0.1 to 10Hz) and wideband (to 1MHz) random noise on the reference output. It may be measured in μV p-p or in $nV/\sqrt{Hz}$.

ANALOG DEVICES

High Precision 2.5V IC Reference

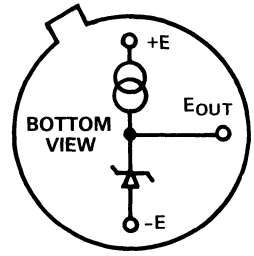
AD580*

FEATURES

Laser Trimmed to High Accuracy: 2.500V ±0.4%
3-Terminal Device: Voltage In/Voltage Out
Excellent Temperature Stability: 10ppm/°C (AD580M, U)
Excellent Long Term Stability: 250μV (25μV/Month)
Low Quiescent Current: 1.5mA max
Small, Hermetic IC Package: TO-52 Can

AD580 FUNCTIONAL BLOCK DIAGRAM

TO-52



PRODUCT DESCRIPTION

The AD580 is a three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output for inputs between 4.5V and 30V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provide the AD580 with an initial tolerance of ±0.4%, a temperature stability of better than 10ppm/°C and long-term stability of better than 250μV. In addition, the low quiescent current drain of 1.5mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580 allows operation with 5 volt logic supplies making the AD580 ideal for digital panel meter applications or whenever only a single logic power supply is available.

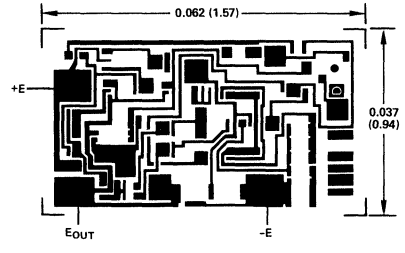
The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Laser-trimming of the thin-film resistors minimizes the AD580 output error. For example, the AD580L output tolerance is ±10mV.
2. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
3. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for systems that contain a single logic power supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities to 10ppm/°C and long term stability better than 250μV.
5. The low quiescent current drain of the AD580 makes it ideal for CMOS and other low power applications.

AD580 CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



The AD580 is also available in chip form. Consult the factory for specifications and applications information.

SPECIFICATIONS (@ E_{IN} = +15V and 25°C)

Model	AD580J			AD580K			AD580L			AD580M			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)			±75			±25			±10			±10	mV
OUTPUT VOLTAGE CHANGE													
T_{min} to T_{max}			15			7			4.3			1.75	mV
			85			40			25			10	ppm/°C
LINE REGULATION													
$7V \leq V_{IN} \leq 30V$		1.5	6		1.5	4			2			2	mV
$4.5V \leq V_{IN} \leq 7V$		0.3	3		0.3	2			1			1	mV
LOAD REGULATION													
ΔI = 10mA			10			10			10			10	mV
QUIESCENT CURRENT		1.0	1.5		1.0	1.5		1.0	1.5		1.0	1.5	mA
NOISE (0.1Hz to 10Hz)		60			60			60			60		μV (p-p)
STABILITY													
Long Term		250			250			250			250		μV
Per Month		25			25			25			25		μV
TEMPERATURE PERFORMANCE													
Specified	0		+70	0		+70	0		+70	0		+70	°C
Operating	−55		+125	−55		+125	−55		+125	−55		+125	°C
Storage	65		+175	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTION[1]													
TO-52 (H-03A)		*			*			*			*		

Model	AD580S			AD580T			AD580U			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)			±25			±10			±10	mV
OUTPUT VOLTAGE CHANGE										
T_{min} to T_{max}			25			11			4.5	mV
			55			25			10	ppm/°C
LINE REGULATION										
$7V \leq V_{IN} \leq 30V$		1.5	6			2			2	mV
$4.5V \leq V_{IN} \leq 7V$		0.3	3			1			1	mV
LOAD REGULATION										
ΔI = 10mA			10			10			10	mV
QUIESCENT CURRENT		1.0	1.5		1.0	1.5		1.0	1.5	mA
NOISE (0.1Hz to 10Hz)		60			60			60		μV (p-p)
STABILITY										
Long Term		250			250			250		μV
Per Month		25			25			25		μV
TEMPERATURE PERFORMANCE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−55		+150	−55		+150	−55		+150	°C
Storage	−65		+175	−65		+175	−65		+175	°C
ABSOLUTE MAXIMUM RATINGS										
Input Voltage	40V									
Power Dissipation @ +25°C										
Ambient Temperature	350mW									
Derate above +25°C	2.8mW/°C									
Lead Temperature (Soldering, 10 sec)	300°C									
Thermal Resistance										
Junction-to-Case	100°C/W									
Junction-to-Ambient	360°C/W									
PACKAGE OPTION[1]										
TO-52 (H-03A)		*			*			*		

NOTES

[1] See Section 14 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

THEORY OF OPERATION

Most precision IC references use complex multichip hybrid designs based on expensive temperature-compensated zener diodes. Others are monolithic with on-chip zener diodes; these often require more than one power supply and, with the zener breakdown occuring near 6.3 volts, will not operate from a low voltage logic supply.

The AD580 family (AD580, AD581, AD584, AD589) uses the "bandgap" concept to produce a stable, low-temperature-coefficient voltage reference suitable for high accuracy data-acquisition components and systems. The device makes use of the underlying physical nature of a silicon transistor base-emitter voltage in the forward-biased operating region. All such transistors have approximately a -2mV/°C temperature coefficient, unsuitable for use directly as a low TC reference; however, extrapolation of the temperature characteristic of any one of these devices to absolute zero (with emitter current proportional to absolute temperature) reveals that it will go to a V_{BE} of 1.205 volts at 0K, as shown in Figure 1. Thus, if a voltage could be developed with an opposing temperature coefficient to sum with V_{BE} to total 1.205 volts, a zero-TC reference would result and operation from a single, low-voltage supply would be possible. The AD580 circuit provides such a compensating voltage, V_1 in Figure 2, by driving two transistors at different current densities and amplifying the resulting V_{BE} difference (ΔV_{BE} – which now has a positive TC); the sum (V_Z) is then buffered and amplified up to 2.5 volts to provide a usable reference-voltage output. Figure 3 is the schematic diagram of the AD580.

The AD580 operates as a three-terminal reference, which means that no additional components are required for biasing or current setting. The connection diagram, Figure 4 is quite simple.

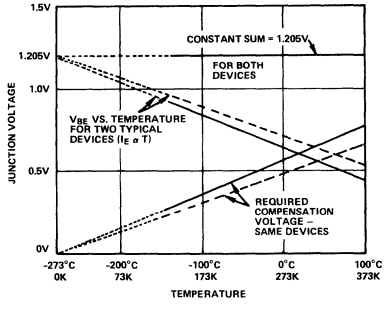


Figure 1. Extrapolated Variation of Base-Emitter Voltage with Temperature ($I_E \alpha T$), and Required Compensation, Shown for Two Different Devices

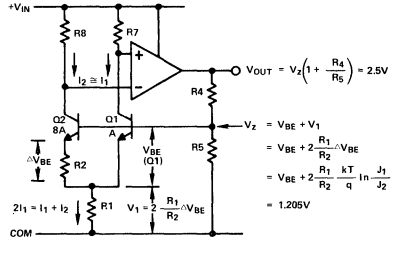


Figure 2. Basic Bandgap-Reference Regulator Circuit

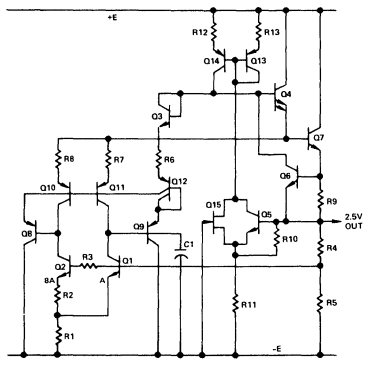


Figure 3. AD580 Schematic Diagram

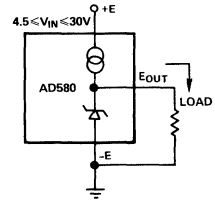


Figure 4. AD580 Connection Diagram

VOLTAGE VARIATION VS. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD580 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

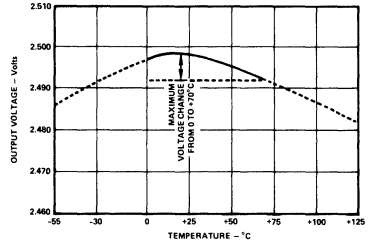


Figure 5. Typical AD580K Output Voltage vs. Temperature

The AD580M guarantees a maximum deviation of 1.75mV over the 0 to +70°C temperature range. This can be shown to be equivalent to 10ppm/°C average maximum; i.e. . .

$$\frac{1.75\text{mV max}}{70^\circ\text{C}} \times \frac{1}{2.5\text{V}} = 10\text{ppm}/^\circ\text{C max average}$$

The AD580 typically exhibits a variation of 1.5mV over the power supply range of 7 to 30 volts. Figure 6 is a plot of AD580 line rejection versus frequency.

NOISE PERFORMANCE

Figure 7 represents the peak-to-peak noise of the AD580 from 1Hz (3dB point) to a 3dB high end shown on the horizontal axis. Peak-to-peak noise from 1Hz to 1MHz is approximately 600μV.

THE AD580 AS A CURRENT LIMITER

The AD580 represents an excellent alternative to current limiter diodes which require factory-selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD580 approach is not limited to a specially selected factory set current limit; it can be programmed from 1 to 10mA with the insertion of a single external resistor. The approximate temperature coefficient of current limit for the AD580 used in this mode is 0.13%/°C for I_{LIM} = 1mA and 0.01%/°C for I_{LIM} = 13mA (see Figure 9). Figure 8 displays the high output impedance of the AD580 used as a current limiter for I_{LIM} = 1, 2, 3, 4, 5mA.

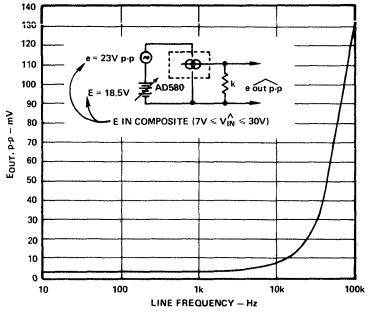


Figure 6. AD580 Line Rejection Plot

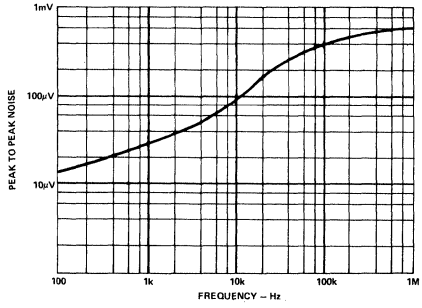


Figure 7. Peak-to-Peak Output Noise vs. Frequency

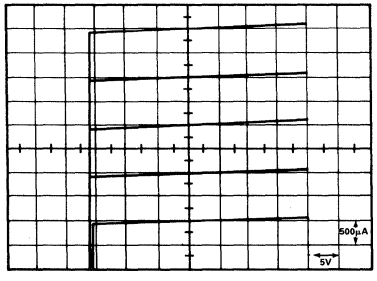


Figure 8. Input Current vs. Input Voltage (Integral Loads)

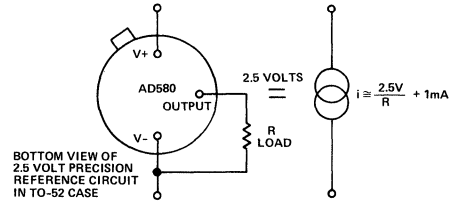


Figure 9. A Two-Component Precision Current Limiter

THE AD580 AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD580 has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

Figure 10 shows the AD580 used as a reference for the AD7542 12-bit CMOS DAC with complete microprocessor interface. The AD580 and the AD7542 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7542 includes three 4-bit data registers, a 12-bit DAC register, and address decoding logic; it may thus be interfaced directly to a 4-, 8- or 16-bit data bus. Only 8mA of quiescent current from the single +5 volt supply is required to operate the AD7542 which is packaged in a small 16-pin DIP. The AD544 output amplifier is also low power, requiring only 2.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7542KN without user trims and it typically settles to ±1/2 LSB in less than 3μs. It will provide the 0 to -2.5 volt output swing from ±5 volt supplies.

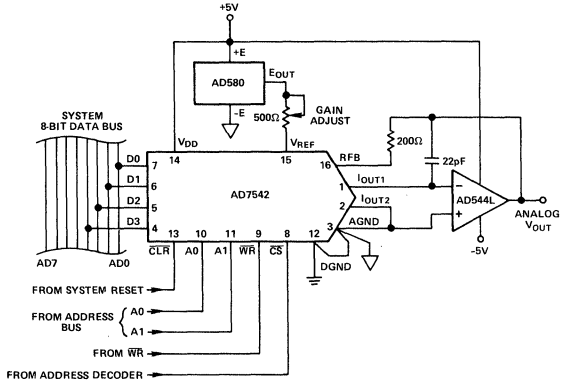


Figure 10. Low Power, Low Voltage Reference for the AD7542 Microprocessor-Compatible 12-Bit DAC

ANALOG DEVICES

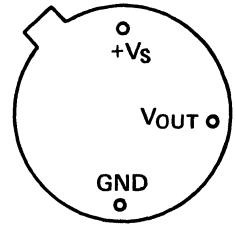
High Precision 10V IC Reference

AD581*

FEATURES

Laser-Trimmed to High Accuracy:
10.000 Volts ±5mV (L and U)
Trimmed Temperature Coefficient:
5ppm/°C max, 0 to +70°C (L)
10ppm/°C max, -55°C to +125°C (U)
Excellent Long-Term Stability:
25ppm/1000 hrs. (Noncumulative)
Negative 10 Volt Reference Capability
Low Quiescent Current: 1.0mA max
10mA Current Output Capability
3-Terminal TO-5 Package

AD581 FUNCTIONAL BLOCK DIAGRAM



TO-5
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical Zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected Zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the -55°C to +125°C range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

***Covered by Patent Nos. 3,887,863; RE 30,586**

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.

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SPECIFICATIONS (@ V_{IN} = +15V and 25°C)

Model	AD581J Min	AD581J Typ	AD581J Max	AD581K Min	AD581K Typ	AD581K Max	AD581L Min	AD581L Typ	AD581L Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			**±5**	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			**±13.5**			**±6.75**			**±2.25**	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			5	ppm/°C
LINE REGULATION										
15V≤V_{IN}≤30V			**3.0**			**3.0**			**3.0**	mV
			(0.002)			(0.002)			(0.002)	%/V
13V≤V_{IN}≤15V			**1.0**			**1.0**			**1.0**	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
0≤I_{OUT}≤5mA		200	**500**		200	**500**		200	**500**	µV/mA
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		µs
NOISE (0.1 to 10Hz)		50			50			50		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			µA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Specified	0		+70	0		+70	0		+70	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[2]										
TO-5 (H-03B)		AD581JH			AD581KH			AD581LH		

Model	AD581S Min	AD581S Typ	AD581S Max	AD581T Min	AD581T Typ	AD581T Max	AD581U Min	AD581U Typ	AD581U Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			**±5**	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			**±30**			**±15**			**±10**	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			10	ppm/°C
LINE REGULATION										
15V≤V_{IN}≤30V			**3.0**			**3.0**			**3.0**	mV
			(0.002)			(0.002)			(0.002)	%/V
13V≤V_{IN}≤15V			**1.0**			**1.0**			**1.0**	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
0≤I_{OUT}≤5mA		200	**500**		200	**500**		200	**500**	µV/mA
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		µs
NOISE (0.1 to 10Hz)		50			50			50		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	200			200			200			µA
Sink −55°C to +85°C	5			5			5			mA
TEMPERATURE RANGE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[2]										
TO-5 (H-03B)		AD581SH			AD581TH			AD581UH		

NOTES
[1]See Figure 7.
[2] See Section 14 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAX RATINGS

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . −55°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C
Thermal Resistance
Junction-to-Ambient . . . . . 150°C/W

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 30 volts.

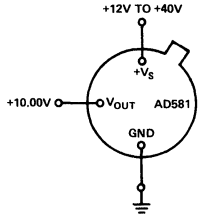
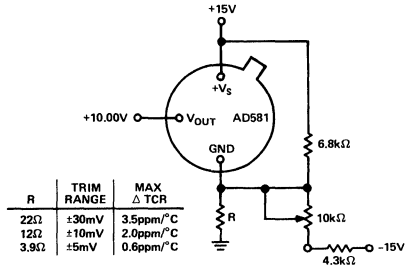


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ±30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.



R	TRIM RANGE	MAX Δ TCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration

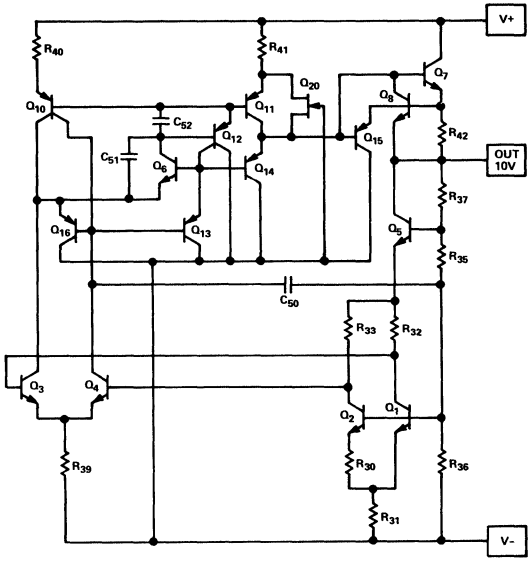


Figure 3. Simplified Schematic

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VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard Zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 4. Five-point measurement of each device guarantees the error band over the -55°C to +125°C range; three-point measurement guarantees the error band from 0 to +70°C.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).

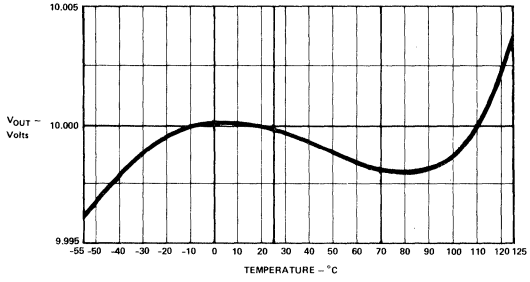


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

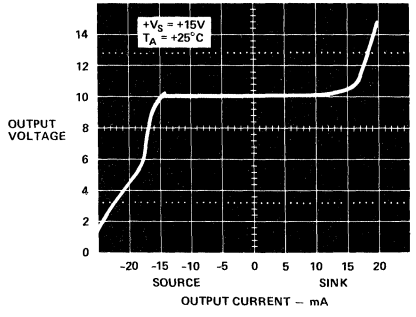


Figure 5. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

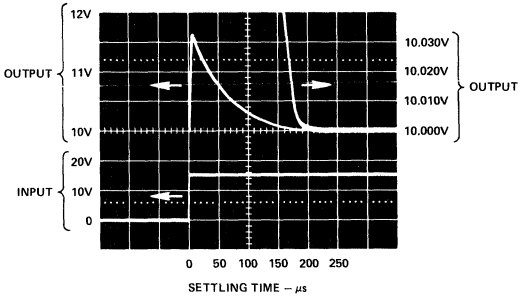


Figure 6. Output Settling Characteristic

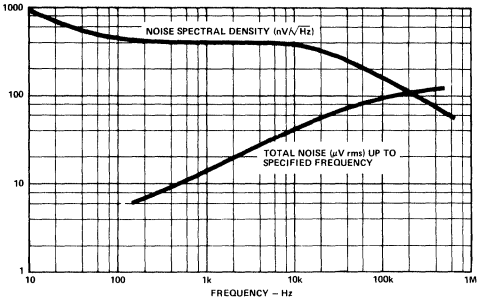


Figure 7. Spectral Noise Density and Total rms Noise vs. Frequency

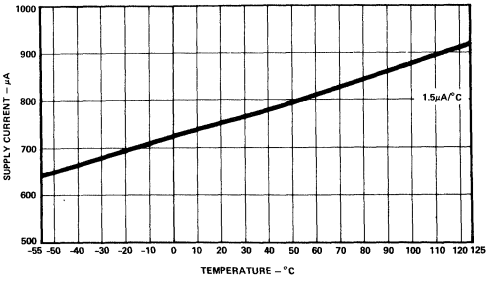


Figure 8. Quiescent Current vs. Temperature

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 9 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

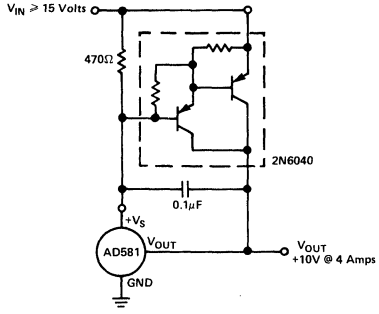


Figure 9. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 10. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that the other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

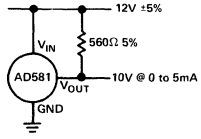


Figure 10. 12-Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

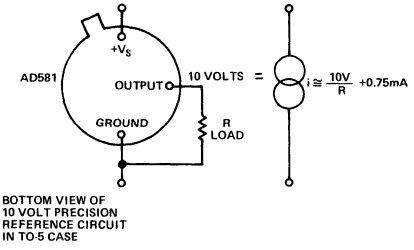


Figure 11. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "Zener" mode to provide a precision -10.00 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

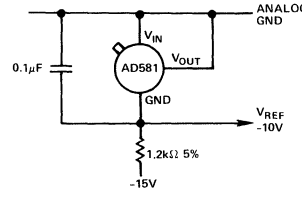


Figure 12. Two-Terminal −10 Volt Reference

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7533 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up, as shown in Figure 14, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to -10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its -10 volt "Zener" mode, as shown in Figure 12 (the $-10V_{REF}$ output is connected directly to the $V_{REF\ IN}$ of the CMOS DAC). The AD581 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 14. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

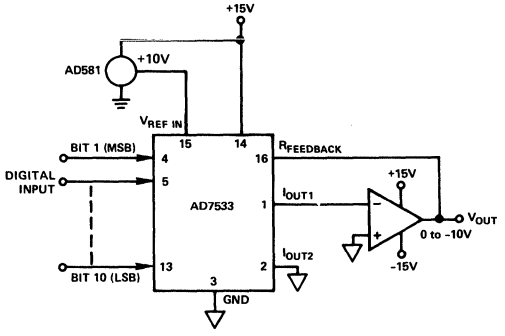


Figure 13. Low Power 10-Bit CMOS DAC Application

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

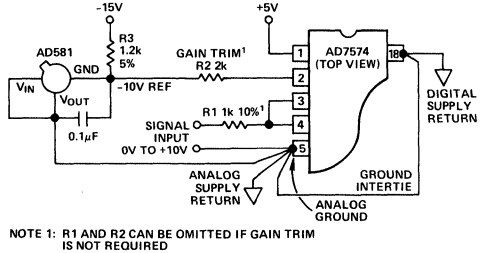


Figure 14. AD581 as Negative 10-Volt Reference for CMOS ADC

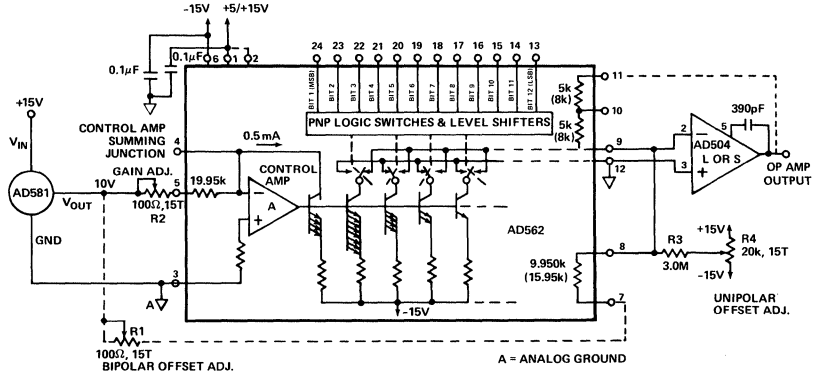


Figure 15. Precision 12-Bit D/A Converter

ANALOG DEVICES

Pin Programmable Precision Voltage Reference

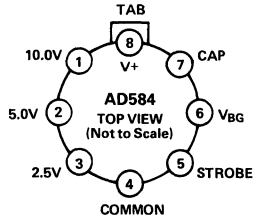
AD584*

FEATURES

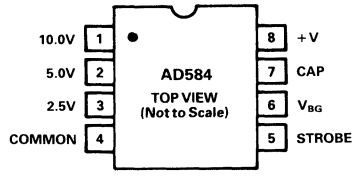
- **Four Programmable Output Voltages: 10.000V, 7.500V, 5.000V, 2.500V**
- **Laser-Trimmed to High Accuracies**
- **No External Components Required**
- **Trimmed Temperature Coefficient: 5ppm/°C max, 0 to +70°C (AD584L) 15ppm/°C max, −55°C to +125°C (AD584T)**
- **Zero Output Strobe Terminal Provided**
- **Two Terminal Negative Reference Capability (5V & Above)**
- **Output Sources or Sinks Current**
- **Low Quiescent Current: 1.0mA max**
- **10mA Current Output Capability**

AD584 PIN CONFIGURATIONS

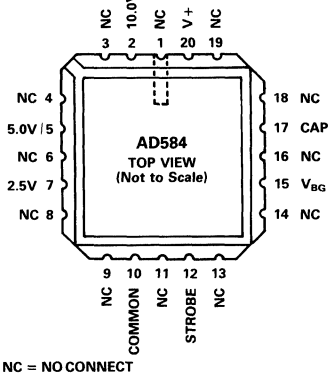
8-Pin TO-99



8-Pin DIP



20-Pin LCC



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K, and L are specified for operation from 0 to +70°C and packaged in 8-pin plastic package; the AD584S and T are specified for the -55°C to-+125°C range. All grades are packaged in a hermetically sealed eight-terminal TO-99 metal can and 20-pin LCC for surface mount applications.

***Covered by U.S. Patent No. 3,887,863; RE 30,586**

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).

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SPECIFICATIONS (@ V_{IN} = 15V and 25°C)

Model	AD584J			AD584K			AD584L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE										
Maximum Error[1] for Nominal										
Outputs of:										
10.000V			**±30**			**±10**			**±5**	mV
7.500V			**±20**			**±8**			**±4**	mV
5.000V			**±15**			**±6**			**±3**	mV
2.500V			**±7.5**			**±3.5**			**±2.5**	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C										
Value, T_{min} to T_{max}[2]										
10.000, 7.500, 5.000V Outputs			**30**			**15**			**5**	ppm/°C
2.500V Output			**30**			**15**			**10**	ppm/°C
Differential Temperature										
Coefficients Between Outputs		5			3			3		ppm/°C
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
Temperature Variation		1.5			1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200			200		µs
NOISE										
(0.1 to 10Hz)		50			50			50		µV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
LINE REGULATION (No Load)										
$15V \leq V_{IN} \leq 30V$			**0.002**			**0.002**			**0.002**	%/V
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$			**0.005**			**0.005**			**0.005**	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$, All Outputs		20	**50**		20	**50**		20	**50**	ppm/mA
OUTPUT CURRENT										
$V_{IN} \geq V_{OUT} + 2.5V$										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			mA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Operating	0		+70	0		+70	0		+70	°C
Storage	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTIONS[3]										
TO-99 (H-08A)		AD584JH			AD584KH			AD584LH		
Plastic (N-8)		AD584JN			AD584KN			AD584LN		
LCC (E-20A)		AD584JE			AD584KE			AD584LE		

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]See Section 14 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . −55°C to +125°C
Lead Temperature (Soldering 10sec) . . . . . +300°C
Thermal Resistance
Junction-to-Ambient (H-08A) . . . . . 150°C/W
(E-20A) . . . . . 120°C/W

Model	AD584S Min	AD584S Typ	AD584S Max	AD584T Min	AD584T Typ	AD584T Max	Units
OUTPUT VOLTAGE TOLERANCE							
Maximum Error[1] for Nominal							
Outputs of:							
10.000V			**±30**			**±10**	mV
7.500V			**±20**			**±8**	mV
5.000V			**±15**			**±6**	mV
2.500V			**±7.5**			**±3.5**	mV
OUTPUT VOLTAGE CHANGE							
Maximum Deviation from +25°C							
Value, T_{min} to T_{max}[2]							
10.000, 7.500, 5.000V Outputs			**30**			**15**	ppm/°C
2.500V Output			**30**			**20**	ppm/°C
Differential Temperature							
Coefficients Between Outputs		5			3		ppm/°C
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**	mA
Temperature Variation		1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200		µs
NOISE							
(0.1 to 10Hz)		50			50		µV p-p
LONG-TERM STABILITY		25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30		mA
LINE REGULATION (No Load)							
$15V \leq V_{IN} \leq 30V$			**0.002**			**0.002**	%/V
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$			**0.005**			**0.005**	%/V
LOAD REGULATION							
$0 \leq I_{OUT} \leq 5mA$, All Outputs		20	**50**		20	**50**	ppm/mA
OUTPUT CURRENT							
$V_{IN} \geq V_{OUT} + 2.5V$							
Source @ +25°C	10			10			mA
Source T_{min} to T_{max}	5			5			mA
Sink T_{min} to T_{max}	200			200			µA
Sink −55°C to +85°C	5			5			mA
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	°C
PACKAGE OPTIONS[3]							
TO-99 (H-08A)		AD584SH			AD584TH		
LCC (E-20A)		AD584SE			AD584TE		

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]See Section 14 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

8

Applying the AD584

APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

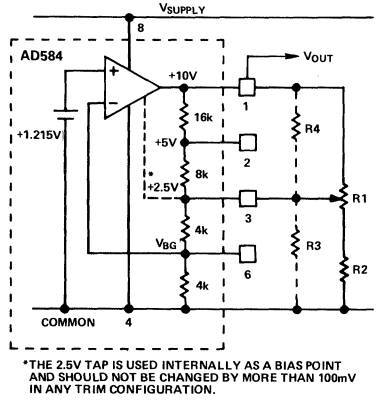


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 3 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

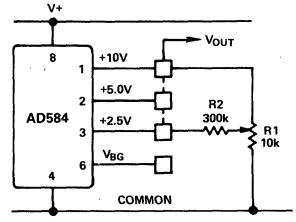


Figure 2. Output Trimming

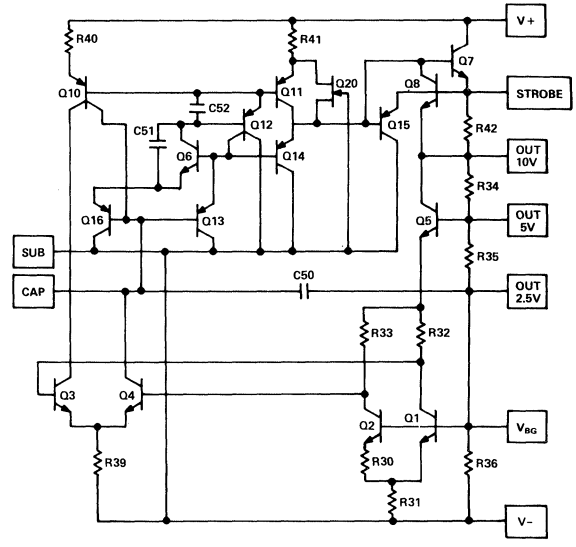


Figure 3. Schematic Diagram

PERFORMANCE OVER TEMPERATURE

Each AD584 is tested at five temperatures over the -55°C to +125°C range to ensure that each device falls within the Maximum Error Band (see Figure 4) specified for a particular grade (i.e., S and T grades); three-point measurement guarantees performance within the error band from 0 to +70°C (i.e., J, K, or L grades). The error band guaranteed for the AD584 is the maximum deviation from the initial value at +25°C. Thus, given the grade of the AD584, the designer can easily determine the maximum total error from initial tolerance plus temperature variation. For example, for the AD584T, the initial tolerance is ±10mV and the error band is ±15mV. Hence, the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C.

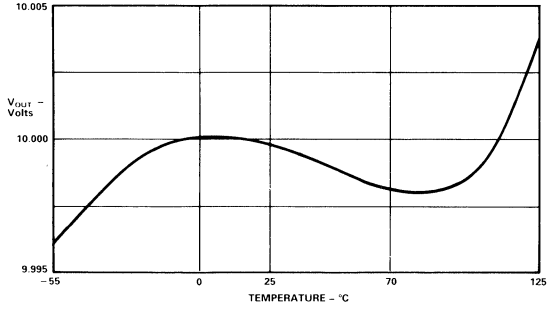


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD584 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device is shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

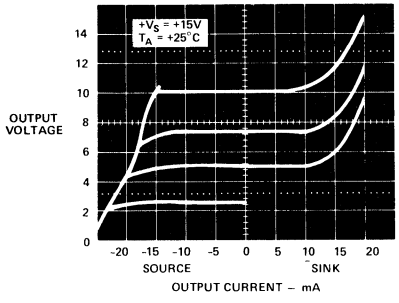


Figure 5. AD584 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD584. Figure 6a is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

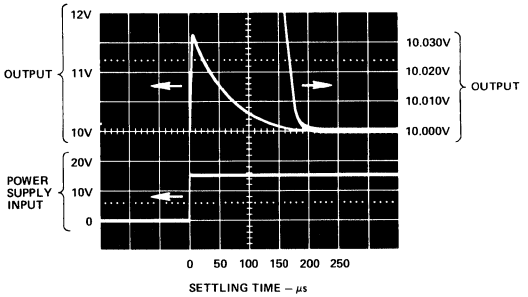


Figure 6. Output Settling Characteristic

NOISE FILTERING

The bandwidth of the output amplifier in the AD584 can be reduced to filter the output noise. A capacitor ranging between 0.01μF and 0.1μF connected between the Cap and V_{BG} terminals will further reduce the wideband and feedthrough noise in the output of the AD584, as shown in Figure 8. However, this will tend to increase the turn-on settling time of the device so ample warm-up time should be allowed.

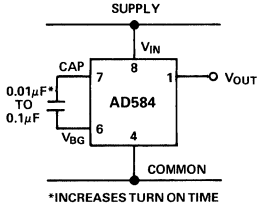


Figure 7. Additional Noise Filtering with an External Capacitor

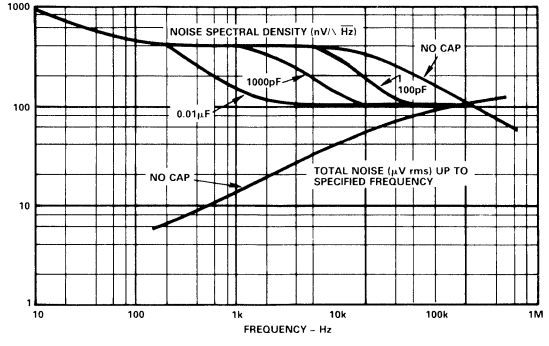


Figure 8. Spectral Noise Density and Total rms Noise vs. Frequency

Applications of the AD584

USING THE STROBE TERMINAL

The AD584 has a strobe input which can be used to zero the output. This unique feature permits a variety of new applications in signal and power conditioning circuits.

Figure 9 illustrates the strobe connection. A simple NPN switch can be used to translate a TTL logic signal into a strobe of the output. The AD584 operates normally when there is no current drawn from pin 5. Bringing this terminal low, to less than 200mV, will allow the output voltage to go to zero. In this mode the AD584 should not be required to source or sink current (unless a 0.7V residual output is permissible). If the AD584 is required to sink a transient current while strobed off, the strobe terminal input current should be limited by a 100Ω resistor as shown in Figure 9.

The strobe terminal will tolerate up to 5μA leakage and its driver should be capable of sinking 500μA continuous. A low leakage open collector gate can be used to drive the strobe terminal directly, provided the gate can withstand the AD584 output voltage plus one volt.

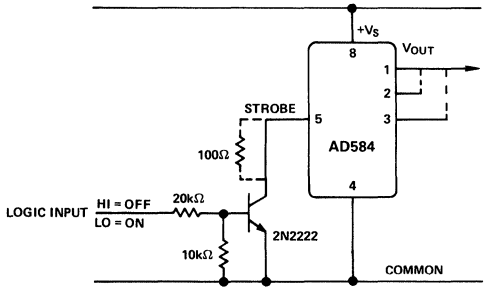


Figure 9. Use of the Strobe Terminal

PRECISION HIGH CURRENT SUPPLY

The AD584 can be easily connected to a power PNP or power Darlington PNP device to provide much greater output current capability. The circuit shown in Figure 10 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

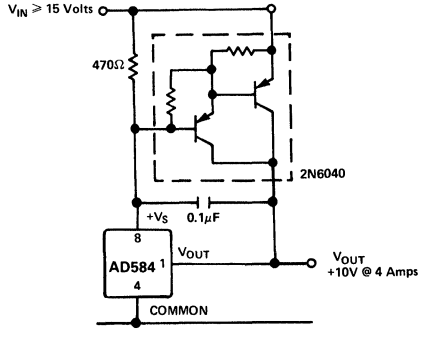


Figure 10. High Current Precision Supply

The AD584 can also use an NPN or Darlington NPN transistor to boost its output current. Simply connect the 10V output terminal of the AD584 to the base of the NPN booster and take the output from the booster emitter as shown in Figure 11. The 5.0V or 2.5V pin must connect to the actual output in this configuration. Variable or adjustable outputs (as shown in Figures 1 and 2) may be combined with +5.0V connection to obtain outputs above +5.0V.

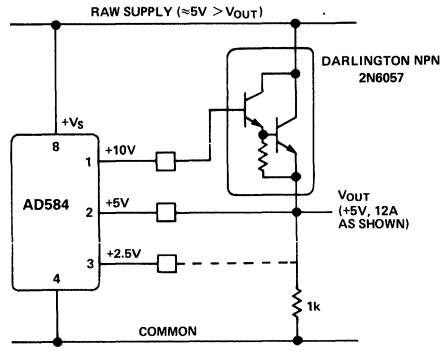


Figure 11. NPN Output Current Booster

THE AD584 AS A CURRENT LIMITER

The AD584 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. Use of current limiting diodes often results in temperature coefficients of 1%/°C. Use of the AD584 in this mode is not limited to a set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor (see Figure 12). Of course, the minimum voltage required to drive the connection is 5 volts.

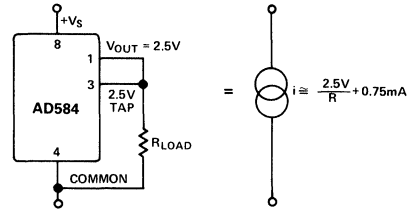


Figure 12. A Two-Component Precision Current Limiter

NEGATIVE REFERENCE VOLTAGES FROM AN AD584

The AD584 can also be used in a two-terminal "zener" mode to provide a precision -10, -7.5 or -5.0 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the positive supply (in this case, ground). The AD584 common pin is connected through a resistor to the negative supply. The output is now taken from the common pin instead of V_{OUT}. With 1mA flowing through the AD584 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2Ω. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD584 is always between 1 and 5mA. The temperature characteristics and long-term stability of the

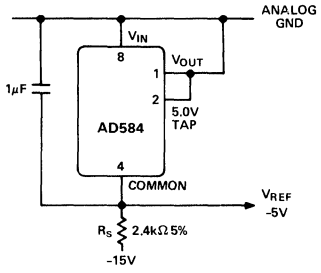


Figure 13. Two-Terminal -5 Volt Reference

device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD584 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 0.5 volts above the desired output voltage. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD584 always remains within its regulating range of 1 to 5mA.

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD584 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up as shown in Figure 14, the standard output voltages are inverted by the amplifier/DAC configuration to produce converted voltage ranges. For example, a +10V reference produces a 0 to -10V range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. The AD584 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

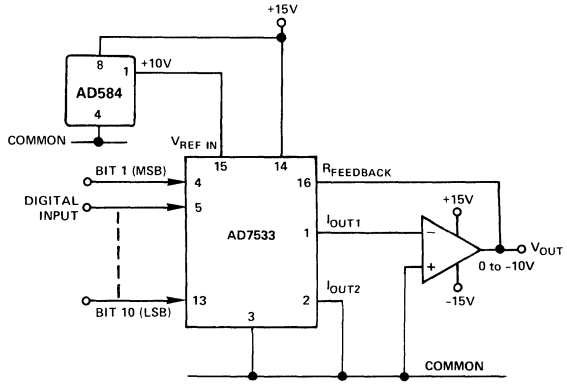


Figure 14. Low Power 10-Bit CMOS DAC Application

PRECISION D/A CONVERTER REFERENCE

The AD562, like many D/A converters, is designed to operate with a +10 volt reference element (Figure 15). In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k

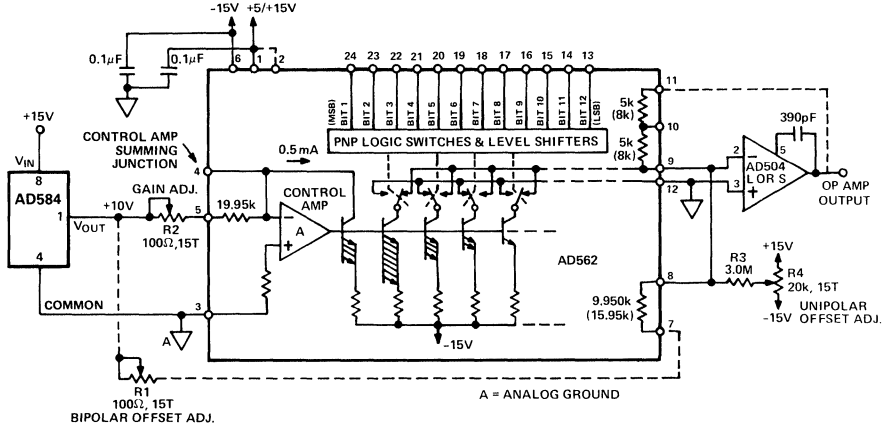


Figure 15. Precision 12-Bit D/A Converter

span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD584L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C. Figure 17 demonstrates the flexibility of the AD584 applied to another popular D/A configuration.

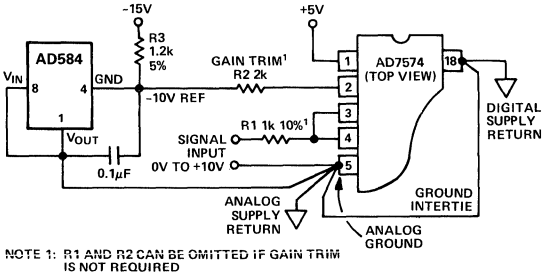


Figure 16. AD584 as Negative 10 Volt Reference for CMOS ADC

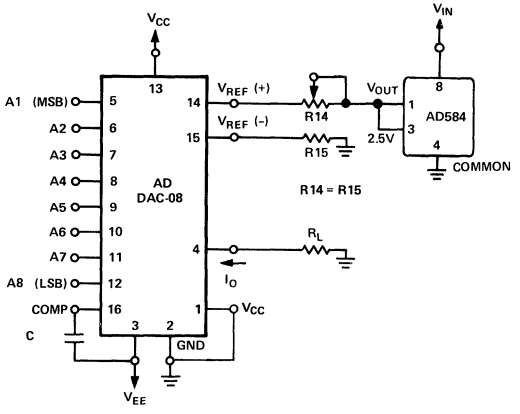
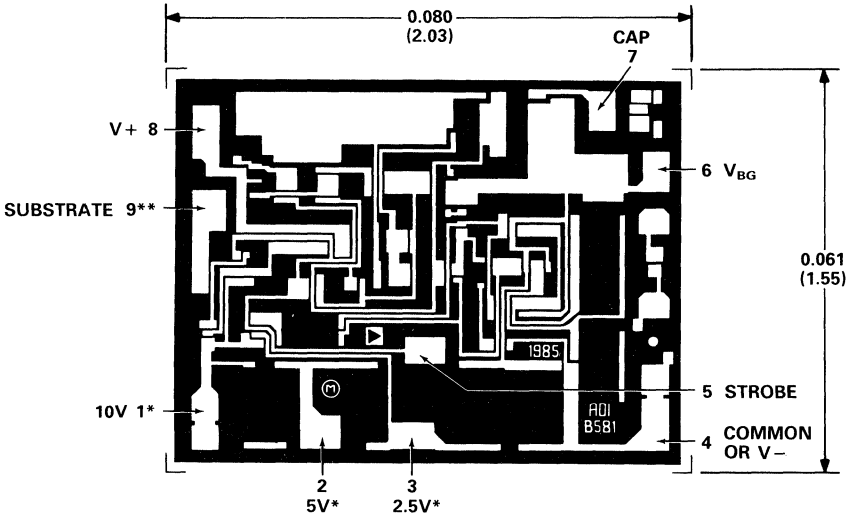


Figure 17. Current Output 8-Bit D/A

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99, 8-PIN METAL PACKAGE.
*INTERCONNECTIONS REQUIRED; SEE PIN DESIGNATIONS FOR INFORMATIONS.
**NOT BROUGHT OUT IN PACKAGED DEVICE.

ANALOG DEVICES

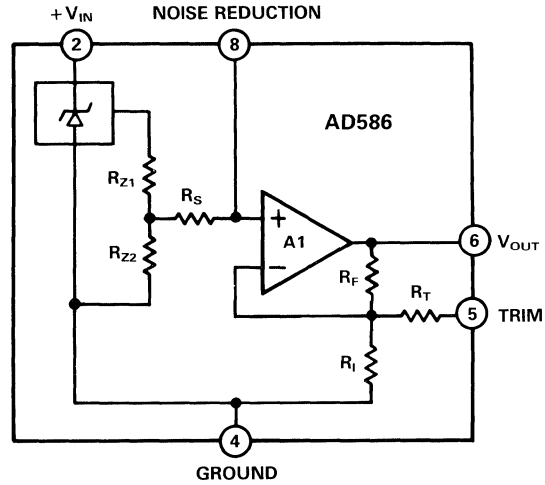
High-Precision 5V Reference

AD586

FEATURES

Laser Trimmed to High Accuracy:
5.000V ±2.5mV (L Grade)
Trimmed Temperature Coefficient:
5ppm/°C max, 0 to +70°C (L Grade)
10ppm/°C max, −55°C to +125°C (T Grade)
Noise Reduction Capability
Low Quiescent Current: 3mA max
Output Trim Capability

AD586 FUNCTIONAL BLOCK DIAGRAM



NOTE: PINS 1, 3 & 7 ARE INTERNAL TEST POINTS.
MAKE NO CONNECTIONS TO THESE POINTS.

8

PRODUCT DESCRIPTION

The AD586 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD586 provides outstanding performance at low cost.

The AD586 offers much higher performance than most other 5V references. Because the AD586 uses an industry standard pinout, many systems can be upgraded instantly with the AD586. The buried Zener approach to reference design provides lower noise and drift than bandgap voltage references. The AD586 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD586 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD586J, K and L are specified for operation from 0 to +70°C, and the AD586S and T are specified for −55°C to +125°C operation. All grades are packaged in an 8-pin cerdip package. The AD586J and the AD586K are also available in an 8-pin plastic surface mount small outline (SO) package.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD586L has a maximum deviation from 5.000V of ±3.625mV between 0 and +70°C, and the AD586T guarantees ±7.5mV maximum total error between −55°C and +125°C.
2. For applications requiring higher precision, an optional fine-trim connection is provided.
3. Any system using an industry standard pinout reference can be upgraded instantly with the AD586.
4. Output noise of the AD586 is very low, typically 4μV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.

SPECIFICATIONS (T_A = +25°C, V_{IN} = +15V unless otherwise specified)

Model	AD586J Min	AD586J Typ	AD586J Max	AD586K Min	AD586K Typ	AD586K Max	AD586L Min	AD586L Typ	AD586L Max	AD586S Min	AD586S Typ	AD586S Max	AD586T Min	AD586T Typ	AD586T Max	Units
Output Voltage	4.980		5.020	4.995		5.005	4.9975		5.0025	4.990		5.010	4.9975		5.0025	V
Output Voltage Drift[1]																
0 to +70°C			25			15			5							ppm/°C
−55°C to +125°C												20			10	
Gain Adjustment	+6			+6			+6			+6			+6			%
	−2			−2			−2			−2			−2			
Line Regulation[1]																
10.8V < +V_{IN} <36V																
T_{min} to T_{max}			100			100			100							±μV/V
11.4V < +V_{IN} <36V																
T_{min} to T_{max}												150			150	
Load Regulation[1]																
Sourcing 0 < I_{OUT} <10mA																
25°C			100			100			100			150			150	μV/mA
T_{min} to T_{max}			100			100			100			150			150	
Sinking −10 < I_{OUT} <0mA																
25°C			400			400			400			400			400	
Quiescent Current		2	3		2	3		2	3		2	3		2	3	mA
Power Consumption		30			30			30			30			30		mW
Output Noise																
0.1Hz to 10Hz		4			4			4			4			4		μV p-p
Spectral Density, 100Hz		100			100			100			100			100		nV/$\sqrt{Hz}$
Long-Term Stability		15			15			15			15			15		ppm/1000Hr
Short-Circuit Current-to-Ground		30	50		30	50		30	50		30	50		30	50	mA
Temperature Range																
Specified Performance	0		+70	0		+70	0		+70	−55		+125	−55		+125	°C
Operating Performance[2]	−40		+85	−40		+85	−40		+85	−55		+125	−55		+125	

NOTES

[1]Maximum output voltage drift is guaranteed for all packages and grades. Cerdip packaged parts are also 100% production tested.

[2]The operating temperature ranged is defined as the temperatures extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

Specifications subject to change without notice.

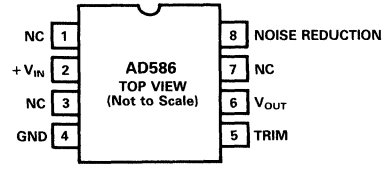
Specifications in boldface are tested on all production units at final electrical test. Result from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground 36V
Power Dissipation (25°C) 500mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temp (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
θ_{JC} . . . . . 22°C/W
θ_{JA} . . . . . 110°C/W
Output Protection: Output safe for indefinite short to ground or V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM

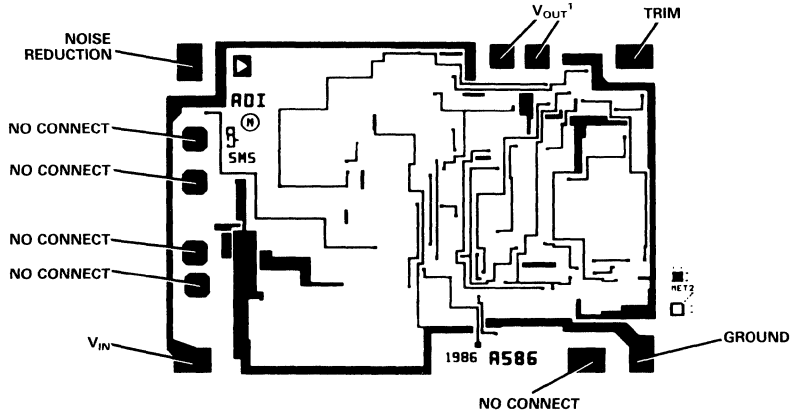


DIE SPECIFICATIONS

The following specifications are tested at the die level for AD586JCHIPS. These die are probed at 25°C only. (T_A = +25°C, V_{IN} = +15V unless otherwise specified)

Parameter	AD586JCHIPS Min	Typ	Max	Units
Output Voltage	4.980		5.020	V
Gain Adjustment	+6			%
	−2			%
Line Regulation				
10.8V < +V_{IN} <36V			100	±μV/V
Load Regulation				
Sourcing 0<I_{OUT} <10mA			100	μV/mA
Sinking −10<I_{OUT} <0mA			400	μV/mA
Quiescent Current			3	mA
Short-Circuit Current-to-Ground			50	mA

DIE LAYOUT



Die Size: 0.081 × 0.060 inches

NOTES

[1]Both V_{OUT} pads should be connected to the output.

Die Thickness: The standard thickness of Analog Devices Bipolar dice is 24 mils ± 2 mils.

Die Dimensions: The dimensions given have a tolerance of ± 2 mils.

Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.

Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die. In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.

Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.

Surface Metalization: The metalization to Analog Devices bipolar dice is aluminum. Minimum thickness is 10,000Å.

Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows have 3.5 mils by 3.5 mils minimum.

ORDERING GUIDE

Model	Initial Error mV	Temp. Coefficient ppm/°C	Temp. Range °C	Package Options*
AD586JQ	20	25.	0 to +70	Cerdip (Q-8)
AD586JR	20	25	0 to +70	SOIC (R-8)
AD586KQ	5	15	0 to +70	Cerdip (Q-8)
AD586KR	5	15	0 to +70	SOIC (R-8)
AD586LQ	2.5	5	0 to +70	Cerdip (Q-8)
AD586SQ	10	20	−55 to +125	Cerdip (Q-8)
AD586TQ	2.5	10	−55 to +125	Cerdip (Q-8)
AD586JCHIPS	20	25	0 to +70	–

*See Section 14 for package outline information.

THEORY OF OPERATION

The AD586 consists of a proprietary buried Zener diode reference, an amplifier to buffer the output and several high stability thin-film resistors as shown in the block diagram in Figure 1. This design results in a high precision monolithic 5V output reference with initial offset of 2.5mV or less. The temperature compensation circuitry provides the device with a temperature coefficient of under 5 ppm/°C.

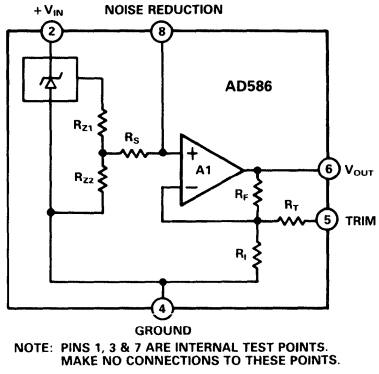


Figure 1. AD586 Functional Block Diagram

Using the bias compensation resistor between the Zener output and the noninverting input to the amplifier, a capacitor can be added at the NOISE REDUCTION pin (Pin 8) to form a low pass filter and reduce the noise contribution of the Zener to the circuit.

APPLYING THE AD586

The AD586 is simple to use in virtually all precision reference applications. When power is applied to Pin 2 and Pin 4 is grounded, Pin 6 provides a 5V output. No external components are required; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD586 requires less than 3mA quiescent current from an operating supply of +12V or +15V.

An external fine trim may be desired to set the output level to exactly 5.000V (calibrated to a main system reference). System calibration may also require a reference voltage that is slightly different from 5.000V, for example, 5.12V for binary applications. In either case, the optional trim circuit shown in Figure 2 can offset the output by as much as 300mV, if desired, with minimal effect on other device characteristics.

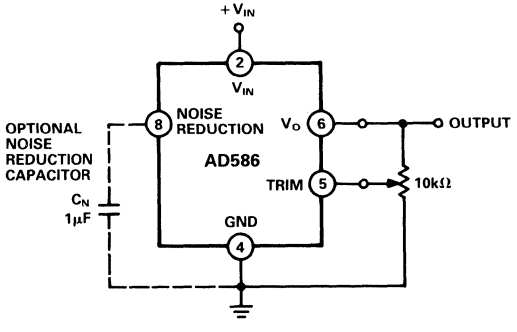


Figure 2. Optional Fine Trim Configuration

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD586 is typically less than 4μV p-p over the 0.1Hz to 10Hz band. Noise in a 1MHz bandwidth is approximately 200μV p-p. The dominant source of this noise is the buried Zener which contributes approximately $100nV/\sqrt{Hz}$. In comparison, the op amp's contribution is negligible. Figure 3 shows the 0.1Hz to 10Hz noise of a typical AD586. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.922Hz bandwidth.

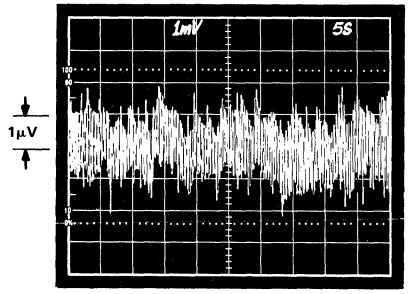


Figure 3. 0.1Hz to 10Hz Noise

If further noise reduction is desired, an external capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2. This capacitor, combined with the 4kΩ R_S and the Zener resistances form a low-pass filter on the output of the Zener cell. A 1μF capacitor will have a 3dB point at 12Hz, and it will reduce the high-frequency (to 1MHz) noise to about 160μV p-p. Figure 4 shows the 1MHz noise of a typical AD586 both with and without a 1μF capacitor.

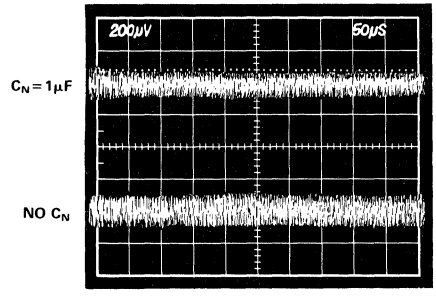
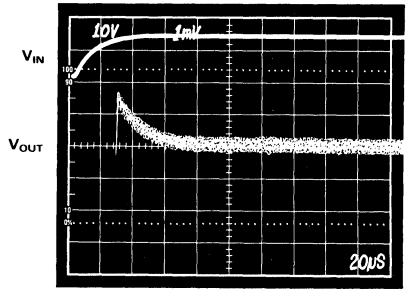


Figure 4. Effect of 1μF Noise Reduction Capacitor on Broadband Noise

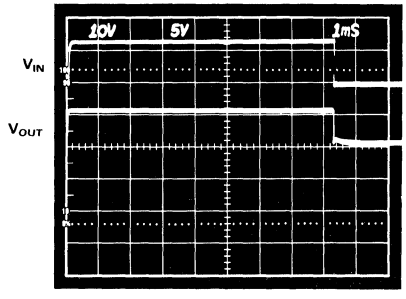
TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are: the time for the active circuits to settle, and the time for the thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD586. It shows the settling to be about 60μsec to 0.01%. Note the absence of any thermal tails when the horizontal scale is expanded to 1ms/cm in Figure 5b.

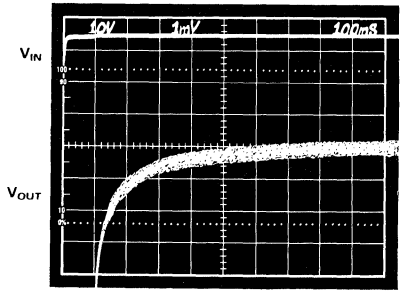
Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor acts as an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1μF capacitor, the initial turn-on time is approximately 400ms to 0.01% (see Figure 5c).



a. Electrical Turn-On



b. Extended Time Scale



c. Turn-on with 1μF C_N

Figure 5. Turn-on Characteristics

DYNAMIC PERFORMANCE

The output buffer amplifier is designed to provide the AD586 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 6 displays the characteristics of the AD586 output amplifier driving a 0 to 10mA load.

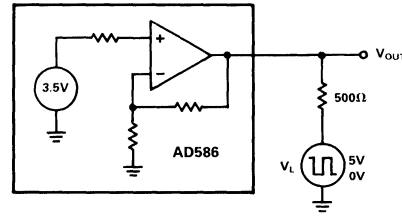


Figure 6a. Transient Load Test Circuit

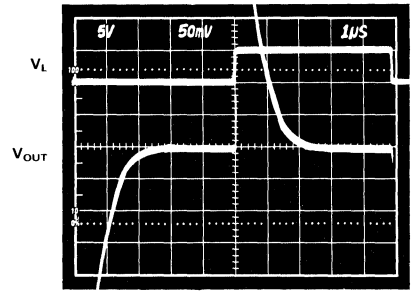


Figure 6b. Large-Scale Transient Response

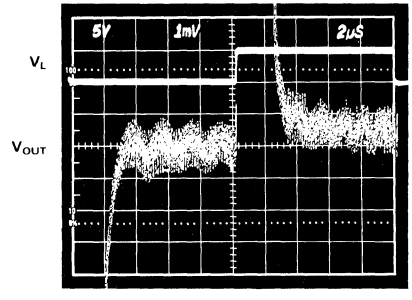


Figure 6c. Fine-Scale Settling for Transient Load

In some applications, a varying load may be both resistive and capacitive in nature, or the load may be connected to the AD586 by a long capacitive cable.

Figure 7 displays the output amplifier characteristics driving a 1000pF, 0 to 10mA load.

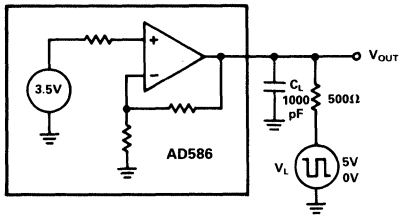


Figure 7a. Capacitive Load Transient Response Test Circuit

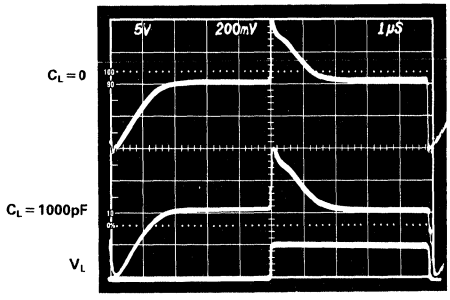


Figure 7b. Output Response with Capacitive Load

LOAD REGULATION

The AD586 has excellent load regulation characteristics. Figure 8 shows that varying the load several mA changes the output by a few μV. The AD586 has somewhat better load regulation performance sourcing current than sinking current.

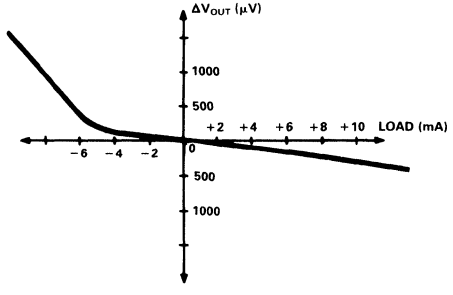


Figure 8. Typical Load Regulation Characteristics

TEMPERATURE PERFORMANCE

The AD586 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centrigrade; i.e., ppm/°C. However, because of nonlinearities in temperature characteristics which originated in standard Zener references (such as "S" type characteristics), most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves the measurement of the output at three or more different temperatures to specify an output voltage error band.

Figure 9 shows the typical output voltage drift for the AD586L and illustrates the test methodology. The box in Figure 9 is bounded on the sides by the operating temperature extremes, and on the top and the bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left to the upper right corner of the box determines the performance grade of the device.

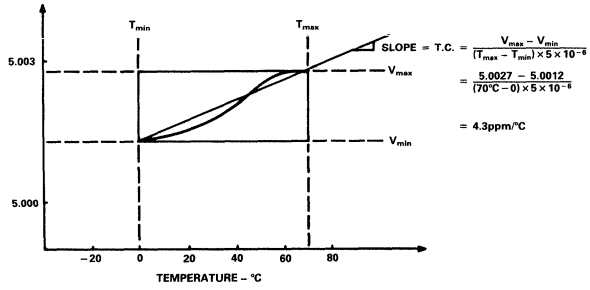


Figure 9. Typical AD586L Temperature Drift

Each AD586JQ, KQ and LQ grade unit is tested at 0, +25°C and +70°C. Each AD586SQ and TQ grade unit is tested at −55°C, +25°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. The maximum height of the box for the appropriate temperature range and device grade is shown in Figure 10. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD586 will produce a curve similar to that in Figure 9, but output readings may vary depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE (mV)	
	0 TO +70°C	−55°C TO +125°C
AD586J	8.75	
AD586K	5.25	
AD586L	1.75	
AD586S		18.00
AD586T		9.00

Figure 10. Maximum Output Change in mV

NEGATIVE REFERENCE VOLTAGE FROM AN AD586

The AD586 can be used to provide a precision −5.000V output as shown in Figure 11. The V_{IN} pin is tied to at least a +6V supply, the output pin is grounded, and the AD586 ground pin is connected through a resistor, R_S, to a −15V supply. The −5V output is now taken from the ground pin (Pin 4) instead of V_{OUT}. It is essential to arrange the output load and the supply resistor R_S so that the net current through the AD586 is between 2.5mA and 10.0mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard +5V output configuration.

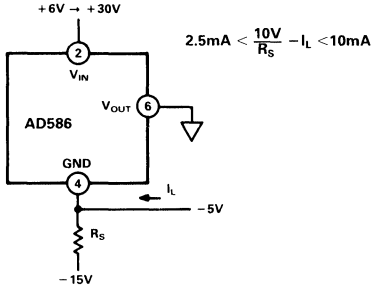


Figure 11. AD586 as a Negative 5V Reference

USING THE AD586 WITH CONVERTERS

The AD586 is an ideal reference for a wide variety of 8-, 12-, 14- and 16-bit A/D and D/A converters. Several representative examples follow.

5V REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD586 is ideal for applications with 10- and 12-bit multiplying CMOS D/A converters. In the standard hookup, as shown in Figure 12, the AD586 is paired with the AD7545 12-bit multiplying DAC and the AD711 high-speed BiFET Op Amp. The amplifier DAC configuration produces a unipolar 0 to −5V output range. Bipolar output applications and other operating details can be found on the individual product data sheets.

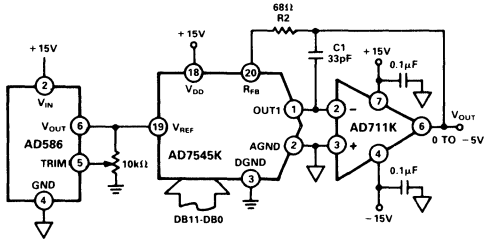


Figure 12. Low-Power 12-Bit CMOS DAC Application

The AD586 can also be used as a precision reference for multiple DACs. Figure 13 shows the AD586, the AD7628 dual DAC and the AD712 dual op amp hooked up for single supply operation to produce 0 to −5V outputs. Because both DACs are on the same die and share a common reference and output op amps, the DAC outputs will exhibit similar gain TCs.

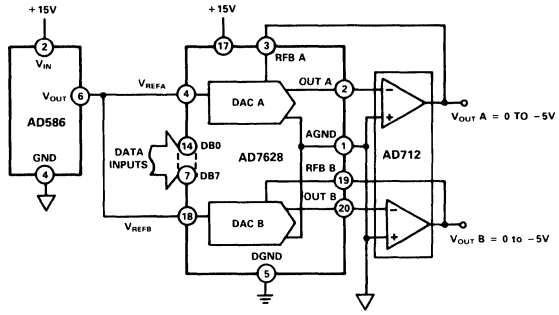


Figure 13. AD586 as a 5V Reference for a CMOS Dual DAC

STACKED PRECISION REFERENCES FOR MULTIPLE VOLTAGES

Often, a design requires several reference voltages. Three AD586s can be stacked, as shown in Figure 14, to produce +5.000V, +10.000V, and +15.000V outputs. This scheme can be extended to any number of AD586s as long as the maximum load current is not exceeded. This design provides the additional advantage of improved line regulation on the +5.0V output. Changes in V_{IN} of +18V to +50V produces an output change that is below the noise level of the references.

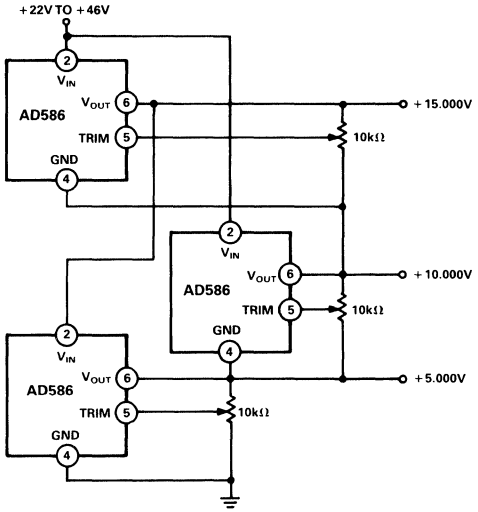


Figure 14. Multiple AD586s Stacked for Precision 5V, 10V and 15V Outputs

PRECISION CURRENT SOURCE

The design of the AD586 allows it to be easily configured as a current source. By choosing the control resistor R_C in Figure 15, you can vary the load current from the quiescent current (2mA typically) to approximately 10mA. The compliance voltage of this circuit varies from about +5V to +21V depending upon the value of V_{IN}.

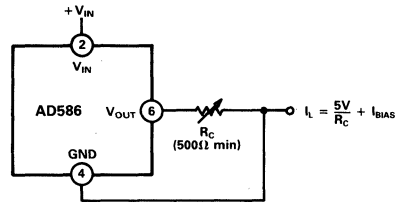


Figure 15. Precision Current Source

PRECISION HIGH CURRENT SUPPLY

For higher currents, the AD586 can easily be connected to a power PNP or power Darlington PNP device. The circuit in Figure 16 can deliver up to 4 amps to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high-frequency supply rejection results can be obtained by removing the capacitor.

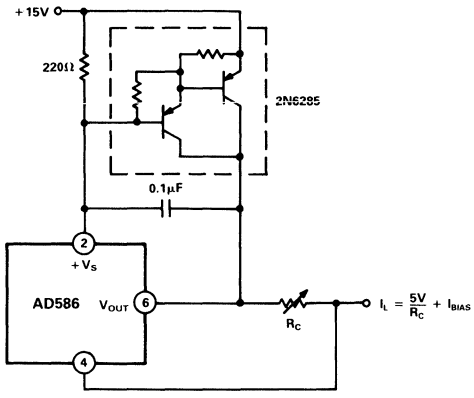


Figure 16a. Precision High-Current Current Source

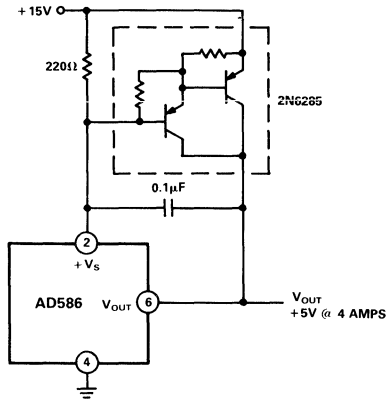


Figure 16b. Precision High-Current Voltage Source

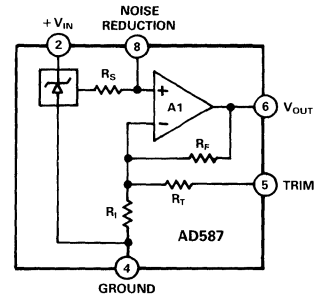
High Precision 10V Reference

AD587

FEATURES

Laser Trimmed to High Accuracy: 10.000V ±5mV (L and U Grades)
Trimmed Temperature Coefficient: 5ppm/°C max, (L and U Grades)
Noise Reduction Capability
Low Quiescent Current: 4mA max
Output Trim Capability

AD587 FUNCTIONAL BLOCK DIAGRAM



NOTE: MAKE NO CONNECTIONS TO PINS 1, 7 AND 8.

PRODUCT DESCRIPTION

The AD587 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD587 provides outstanding performance at low cost.

The AD587 offers much higher performance than most other 10V references. Because the AD587 uses an industry standard pinout, many systems can be upgraded instantly with the AD587. The buried Zener approach to reference design provides lower noise and drift than band-gap voltage references. The AD587 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD587 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD587J, K and L are specified for operation from 0 to +70°C, and the AD587S, T and U are specified for −55°C to +125°C operation. All grades are available in 8-pin cerdip. The J version is also available in an 8-pin Small Outline IC (SOIC) package for surface mount applications and the J and K grades also come in an 8-pin plastic package.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD587L has a maximum deviation from 10.000V of ±8.5mV between 0 and +70°C, and the AD587U guarantees ±14mV maximum total error between −55°C and +125°C.
2. For applications requiring higher precision, an optional fine-trim connection is provided.
3. Any system using an industry standard pinout 10 volt reference can be upgraded instantly with the AD587.
4. Output noise of the AD587 is very low, typically 4μV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.

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SPECIFICATIONS (T_A = +25°C, V_{IN} = +15V unless otherwise specified)

Model	AD587J/S Min	AD587J/S Typ	AD587J/S Max	AD587K/T Min	AD587K/T Typ	AD587K/T Max	AD587L/U Min	AD587L/U Typ	AD587L/U Max	Units
Output Voltage	**9.990**		**10.010**	**9.995**		**10.005**	**9.995**		**10.005**	V
Output Voltage Drift[1]										
0 to +70°C			20			10			5	ppm/°C
−55°C to +125°C			20			10			5	
Gain Adjustment	+3			+3			+3			%
	−1			−1			−1			
Line Regulation[1]										
13.5V ≤ +V_{IN} ≤36V										
T_{min} to T_{max}			**100**			**100**			**100**	±μV/V
Load Regulation[1]										
Sourcing 0 < I_{OUT} <10mA										
T_{min} to T_{max}			**100**			**100**			**100**	±μV/mA
Sinking −10 < I_{OUT} <0mA										
T_{min} to T_{max}			**100**			**100**			**100**	
Quiescent Current		2	**4**		2	**4**		2	**4**	mA
Power Dissipation		30			30			30		mW
Output Noise										
0.1Hz to 10Hz		4			4			4		μV p-p
Spectral Density, 100Hz		100			100			100		nV/√Hz
Long-Term Stability		15			15			15		±ppm/1000Hr
Short-Circuit Current-to-Ground		30	**50**		30	**50**		30	**50**	mA
Short-Circuit Current-to-V_{IN}		30	**50**		30	**50**		30	**50**	mA
Temperature Range										
Specified Performance (J, K, L)	0		+70	0		+70	0		+70	°C
Operating Performance (J, K, L)[2]	−40		+85	−40		+85	−40		+85	
Specified Performance (S, T, U)	−55		+125	−55		+125	−55		+125	
Operating Performance (S, T, U)[2]	−55		+125	−55		+125	−55		+125	

NOTES

[1]Spec is guaranteed for all packages and grades. Cerdip packaged parts are 100% production tested.

[2]The operating temperature ranged is defined as the temperatures extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Result from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Initial Error mV	Temp. Coefficient ppm/°C	Temp. Range °C	Package Options*
AD587JQ	10	20	0 to +70	Cerdip (Q-8)
AD587JR	10	20	0 to +70	SO (R-8)
AD587JN	10	20	0 to +70	Plastic (N-8)
AD587KQ	5	10	0 to +70	Cerdip (Q-8)
AD587KN	5	10	0 to +70	Plastic (N-8)
AD587LQ	5	5	0 to +70	Cerdip (Q-8)
AD587SQ	20	20	−55 to +125	Cerdip (Q-8)
AD587TQ	10	10	−55 to +125	Cerdip (Q-8)
AD587UQ	5	5	−55 to +125	Cerdip (Q-8)
AD587JCHIPS	10	20	0 to +70	–

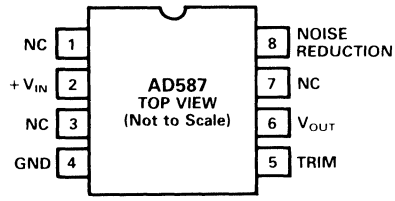
*See Section 14 for package outline information.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground 36V
Power Dissipation (25°C) 500mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temp (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
θ_{JC} . . . . . 22°C/W
θ_{JA} . . . . . 110°C/W
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM

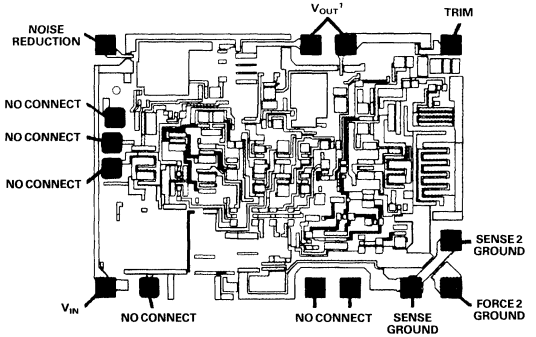


DIE SPECIFICATIONS

The following specifications are tested at the die level for AD587JCHIPS. These die are probed at 25°C only. (T_A = +25°, V_{IN} = +15V unless otherwise specified)

Parameter	AD587JCHIPS Min	Typ	Max	Units
Output Voltage	9.990		10.010	V
Gain Adjustment	−1		3	%
Line Regulation 13.5V < +V_{IN} <36V			100	±μV/V
Load Regulation Sourcing 0<I_{OUT} <10mA Sinking −10<I_{OUT} <0mA			100 100	μV/mA μV/mA
Quiescent Current		2	4	mA
Short-Circuit Current-to-Ground			50	mA
Short-Circuit Current-to-V_{OUT}			50	mA

DIE LAYOUT



Die Size: 0.052 × 0.039 inches

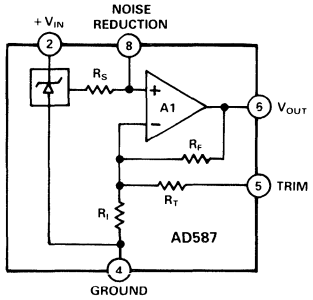
NOTES
[1]Both V_{OUT} pads should be connected to the output.
[2]Sense and force grounds must be tied together.

Die Thickness: The standard thickness of Analog Devices Bipolar dice is 24 mils ± 2 mils.
Die Dimensions: The dimensions given have a tolerance of ± 2 mils.
Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.
Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die. In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.
Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.
Surface Metalization: The metalization to Analog Devices bipolar dice is aluminum. Minimum thickness is 10,000Å.
Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows have 3.5 mils by 3.5 mils minimum.

8

THEORY OF OPERATION

The AD587 consists of a proprietary buried Zener diode reference, an amplifier to buffer the output and several high stability thin-film resistors as shown in the block diagram in Figure 1. This design results in a high precision monolithic 10V output reference with initial offset of 5mV or less. The temperature compensation circuitry provides the device with a temperature coefficient of under 5ppm/°C.



NOTE: MAKE NO CONNECTIONS TO PINS 1, 7 AND 8.

Figure 1. AD587 Functional Block Diagram

A capacitor can be added at the NOISE REDUCTION pin (Pin 8) to form a low pass filter with R_S to reduce the noise contribution of the Zener to the circuit.

APPLYING THE AD587

The AD587 is simple to use in virtually all precision reference applications. When power is applied to Pin 2, and Pin 4 is grounded, Pin 6 provides a 10V output. No external components are required; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD587 requires less than 4mA quiescent current from an operating supply of +15V.

Fine trimming may be desired to set the output level to exactly 10.000V (calibrated to a main system reference). System calibration may also require a reference voltage that is slightly different from 10.000V, for example, 10.24V for binary applications. In either case, the optional trim circuit shown in Figure 2 can offset the output by as much as 300mV, if desired, with minimal effect on other device characteristics.

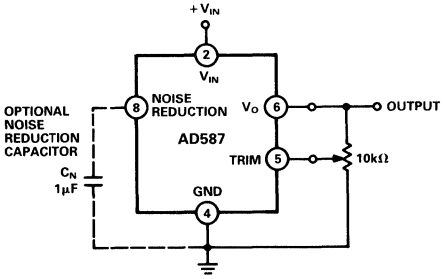


Figure 2. Optional Fine Trim Configuration

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD587 is typically less than 4μV p-p over the 0.1Hz to 10Hz band. Noise in a 1MHz bandwidth is approximately 200μV p-p. The dominant source of this noise is the buried Zener which contributes approximately 100nV/$\sqrt{\text{Hz}}$. In comparison, the op amp's contribution is negligible. Figure 3 shows the 0.1Hz to 10Hz noise of a typical AD587. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.922Hz bandwidth.

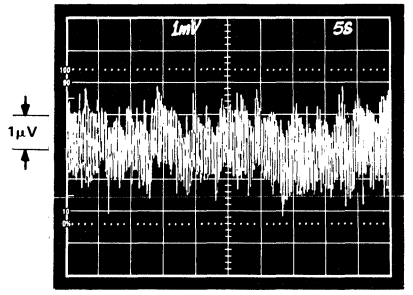


Figure 3. 0.1Hz to 10Hz Noise

If further noise reduction is desired, an external capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2. This capacitor, combined with the 4kΩ R_S and the Zener resistances, form a low-pass filter on the output of the Zener cell. A 1μF capacitor will have a 3dB point at 40Hz, and it will reduce the high-frequency (to 1MHz) noise to about 160μV p-p. Figure 4 shows the 1MHz noise of a typical AD587 both with and without a 1μF capacitor.

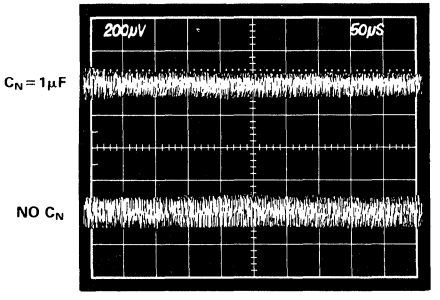
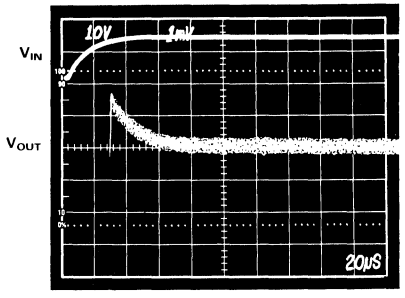


Figure 4. Effect of 1μF Noise Reduction Capacitor on Broadband Noise

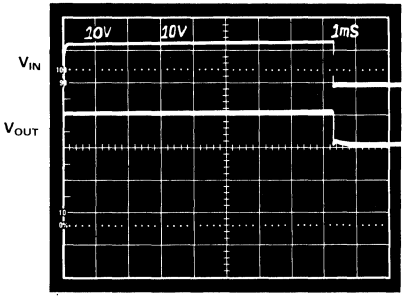
TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are: the time for the active circuits to settle, and the time for the thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD587. It shows the settling to be about 60μs to 0.01%. Note the absence of any thermal tails when the horizontal scale is expanded to 1ms/cm in Figure 5b.

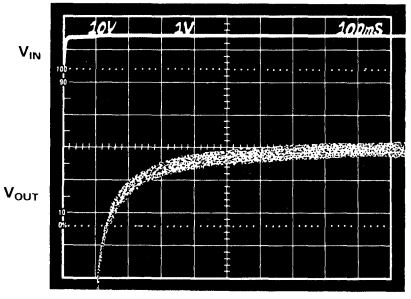
Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor acts as an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1μF capacitor, the initial turn-on time is approximately 400ms to 0.01% (see Figure 5c).



a. Electrical Turn-On



b. Extended Time Scale



c. Turn-on with 1μF C_N

Figure 5. Turn-on Characteristics

DYNAMIC PERFORMANCE

The output buffer amplifier is designed to provide the AD587 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 6 displays the characteristics of the AD587 output amplifier driving a 0 to 10mA load.

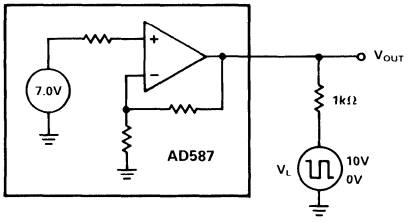


Figure 6a. Transient Load Test Circuit

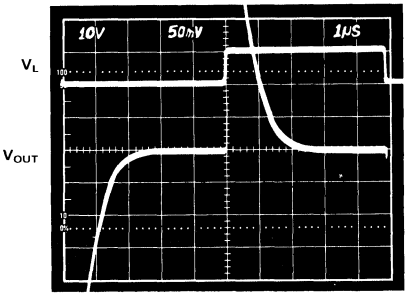


Figure 6b. Large-Scale Transient Response

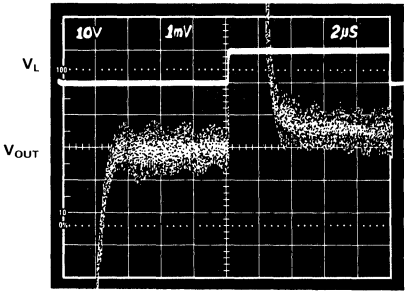


Figure 6c. Fine Scale Settling for Transient Load

8

In some applications, a varying load may be both resistive and capacitive in nature, or the load may be connected to the AD587 by a long capacitive cable.

Figure 7 displays the output amplifier characteristics driving a 1000pF, 0 to 10mA load.

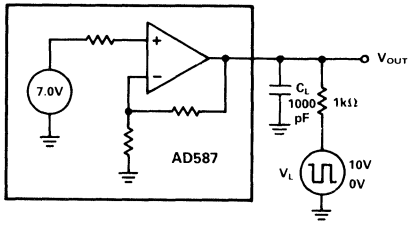


Figure 7a. Capacitive Load Transient Response Test Circuit

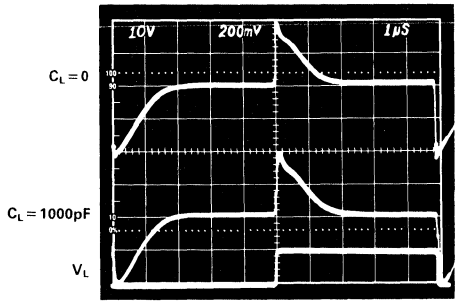


Figure 7b. Output Response with Capacitive Load

LOAD REGULATION

The AD587 has excellent load regulation characteristics. Figure 8 shows that varying the load several mA changes the output by only a few μV.

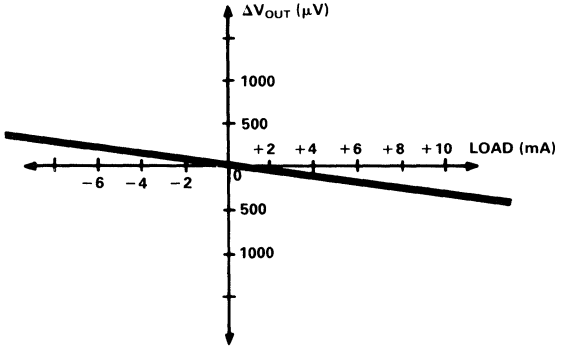


Figure 8. Typical Load Regulation Characteristics

TEMPERATURE PERFORMANCE

The AD587 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centrigrade; i.e., ppm/°C. However, because of nonlinearities in temperature characteristics which originated in standard Zener references (such as "S" type characteristics), most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves the measurement of the output at 3 or more different temperatures to specify an output voltage error band.

Figure 9 shows the typical output voltage drift for the AD587L and illustrates the test methodology. The box in Figure 9 is bounded on the sides by the operating temperature extremes, and on the top and the bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left to the upper right corner of the box determines the performance grade of the device.

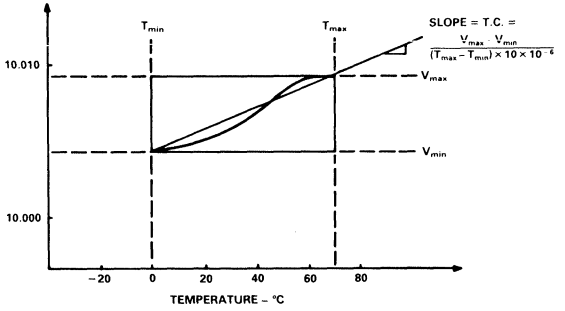


Figure 9. Typical AD587L Temperature Drift

Each AD587J, K, L grade unit is tested at 0, +25°C and +70°C. Each AD587S, T, and U grade unit is tested at −55°C, +25°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. The maximum height of the box for the appropriate temperature range and device grade is shown in Figure 10. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD587 will produce a curve similar to that in Figure 9, but output readings may vary depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE (mV)	
	0 TO +70°C	−55°C TO +125°C
AD587J	24	
AD587K	12	
AD587L	8.5	
AD587S		46
AD587T		23
AD587U		14

Figure 10. Maximum Output Change in mV

NEGATIVE REFERENCE VOLTAGE FROM AN AD587

The AD587 can be used to provide a precision −10.000V output as shown in Figure 11. The V_{IN} pin is tied to at least a +3.5V supply, the output pin is grounded, and the AD587 ground pin is connected through a resistor, R_S, to a −15V supply. The −10V output is now taken from the ground pin (Pin 4) instead of V_{OUT}. It is essential to arrange the output load and the supply resistor R_S so that the net current through the AD587 is between 2.5mA and 10.0mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard +10V output configuration.

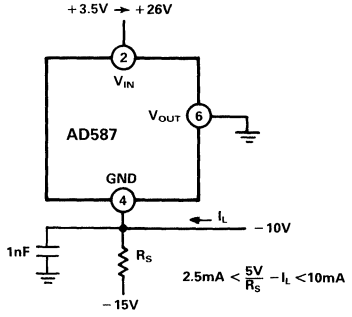


Figure 11. AD587 as a Negative 10V Reference

USING THE AD587 WITH CONVERTERS

The AD587 is an ideal reference for a wide variety of 8-, 12-, 14- and 16-bit A/D and D/A converters. Several representative examples follow.

10V REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD587 is ideal for applications with 10- and 12-bit multiplying CMOS D/A converters. In the standard hookup, as shown in Figure 12, the AD587 is paired with the AD7545 12-bit multiplying DAC and the AD711 high-speed BiFET Op Amp. The amplifier DAC configuration produces a unipolar 0 to −10V output range. Bipolar output applications and other operating details can be found on the individual product data sheets.

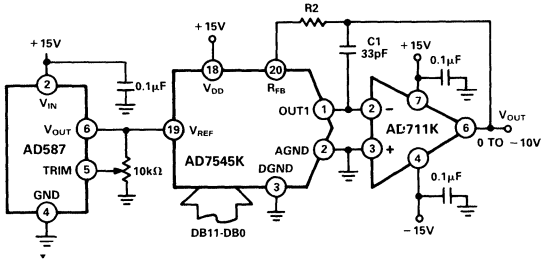


Figure 12. Low-Power 12-Bit CMOS DAC Application

The AD587 can also be used as a precision reference for multiple DACs. Figure 13 shows the AD587, the AD7628 dual DAC and the AD712 dual op amp hooked up for single supply operation to produce 0 to −10V outputs. Because both DACs are on the same die and share a common reference and output op amps; the DAC outputs will exhibit similar gain TCs.

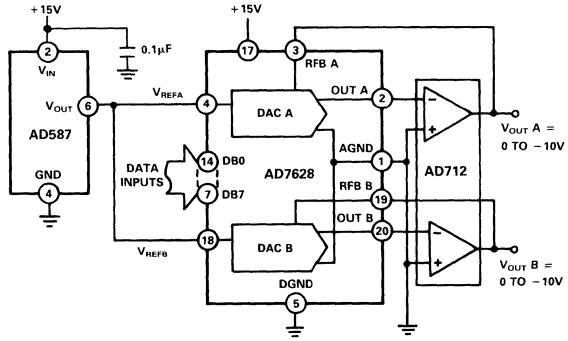


Figure 13. AD587 as a 10V Reference for a CMOS Dual DAC

PRECISION CURRENT SOURCE

The design of the AD587 allows it to be easily configured as a current source. By choosing the control resistor R_C in Figure 14, you can vary the load current from the quiescent current (2mA typically) to approximately 10mA.

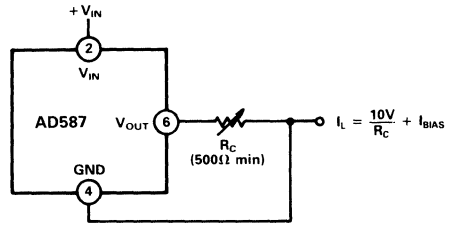


Figure 14. Precision Current Source

PRECISION HIGH CURRENT SUPPLY

For higher currents, the AD587 can easily be connected to a power PNP or power Darlington PNP device. The circuit in Figure 15 can deliver up to 4 amps to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high-frequency supply rejection results can be obtained by removing the capacitor.

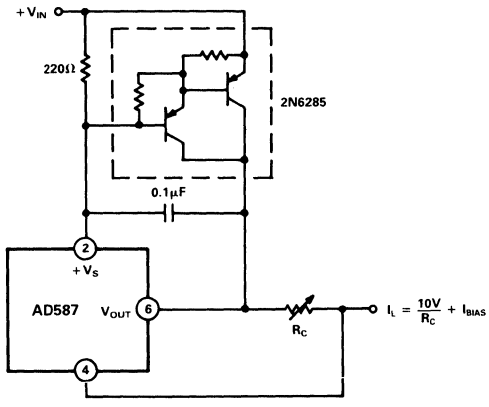


Figure 15a. Precision High-Current Current Source

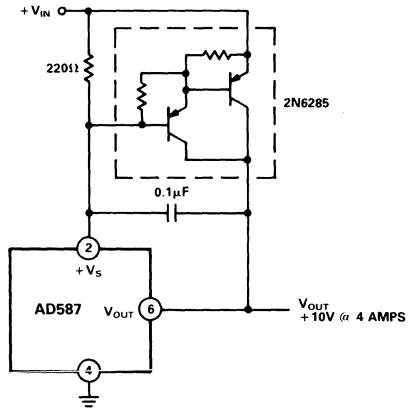


Figure 15b. Precision High-Current Voltage Source

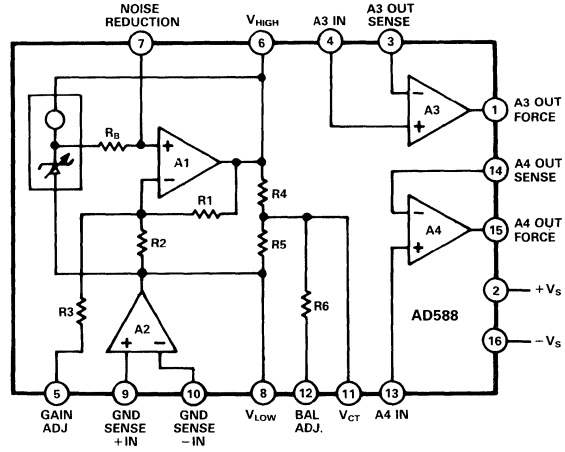
ANALOG DEVICES

High Precision Voltage Reference

AD588*

FEATURES
Low Drift – 1.5ppm/°C
Low Initial Error – 1mV
Pin-Programmable Output
+10V, +5V, ±5V Tracking, −5V, −10V
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine-Insertable DIP and Surface Mount Packaging

AD588 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser-trimmed for low offset and low drift to maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 in conjunction autocalibration software.

The AD588 is available in six versions. AD588AD and BD grades are packaged in a 16-pin side-brazed ceramic DIP and are specified for the −25°C to +85°C industrial temperature range. The ceramic AD588SD and TD grades are specified for the full military/aerospace temperature range. For surface mount applications, the AD588AE, SE and TE grades will also be available in 20-pin LCC packages.

***Covered by Patent Number 4,644,253**

PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the Zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Output noise of the AD588 is very low – typically 6μV p-p. A pin is provided for additional noise filtering using an external capacitor.
3. A precision ±5V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than one millivolt and a fine-trim is available for applications requiring exact symmetry between the +5V and −5V outputs.
4. Pin strapping capability allows configuration of a wide variety of outputs: ±5V, +5V & +10V, −5V & −10V dual outputs or +5V, −5V, +10V, −10V single outputs.
5. Extensive temperature testing at −55°C, −25°C, 0, +25°C, +50°C, +70°C, +85°C and +125°C ensures that the specified temperature coefficient is truly representative of device performance.

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SPECIFICATIONS (typical @ +25°C, +10V output, V_S = ±15V unless otherwise noted[1])

	AD588SD/SE			AD588AD/TD/AE/TE			AD588BD			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
OUTPUT VOLTAGE ERROR										
+10V, −10V Outputs	−5		+5	−3		+3	−1		+1	mV
+5V, −5V Outputs	−5		+5	−3		+3	−1		+1	mV
±5V TRACKING MODE										
Symmetry Error	−1.5		+1.5	−1.5		+1.5	−0.75		+0.75	mV
OUTPUT VOLTAGE DRIFT										
0 to +70°C (A, B, C)					±2		−1.5		+1.5	ppm/°C
−25°C to +85°C (A, B)				−3		+3	−3		+3	ppm/°C
−55°C to +125°C (S, T)	−6		+6	−4		+4				ppm/°C
GAIN ADJ AND BAL ADJ[2]										
Trim Range		±4			±4			±4		mV
Input Resistance		150			150			150		kΩ
LINE REGULATION										
T_{min} to T_{max}[3]			±200			±200			±200	μV/V
LOAD REGULATION										
T_{min} to T_{max}										
+10V Output, $0<I_{OUT}<10mA$			±50			±50			±50	μV/mA
−10V Output, $-10<I_{OUT}<0mA$			±50			±50			±50	μV/mA
SUPPLY CURRENT										
T_{min} to T_{max}		6	10		6	10		6	10	mA
Power Dissipation		180	300		180	300		180	300	mW
OUTPUT NOISE (Any Output)										
0.1 to 10Hz		6			6			6		μV p-p
Spectral Density, 100Hz		100			100			100		nV/√Hz
LONG-TERM STABILITY (@ +25°C)	15				15			15		ppm/1000hr
BUFFER AMPLIFIERS										
Offset Voltage		100			100			100		μV
Offset Voltage Drift		1			1			1		μV/°C
Bias Current		20			20			20		nA
Open Loop Gain		110			110			110		dB
Output Current A3, A4	−10		+10	−10		+10	−10		+10	mA
Common Mode Rejection (A3, A4)										
V_{CM} = 1V p-p		100			100			100		dB
Short-Circuit Current		50			50			50		mA
TEMPERATURE RANGE										
Specified Performance										
A, B Grades				−25		+85	−25		+85	°C
S, T Grades	−55		+125	−55		+125				°C

NOTES

[1]Output — Configuration

+10V — Figure 2a

−10V — Figure 2c

+5V, −5V, ±5V — Figure 2b

Specifications tested using +10V configuration unless otherwise indicated.

[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

[3]Test Conditions:

+10V Output $-V_S = -15V, 13.5V \leq +V_S \leq 18V$

−10V Output $-18V \leq -V_S \leq -13.5V, +V_S = 15V$

±5V Output $+V_S = +18V, -V_S = -18V$ to $+V_S = +10.8V, -V_S = -10.8V$

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Part Number	Initial Error	Temperature Coefficient	Temperature Range °C	Package Option[1]
AD588AD	3mV	3ppm/°C	−25 to +85	Ceramic (D-16)
AD588AE	3mV	3ppm/°C	−25 to +85	LCC (E-20A)
AD588BD	1mV	1.5ppm/°C	−25 to +85*	Ceramic (D-16)
AD588SD	5mV	6ppm/°C	−55 to +125	Ceramic (D-16)
AD588SE	5mV	6ppm/°C	−55 to +125	LCC (E-20A)
AD588TD	3mV	4ppm/°C	−55 to +125	Ceramic (D-16)
AD588TE	3mV	4ppm/°C	−55 to +125	LCC (E-20A)

*Temperature Coefficient specified from 0 to +70°C.

[1]See Section 14 for package outline information.

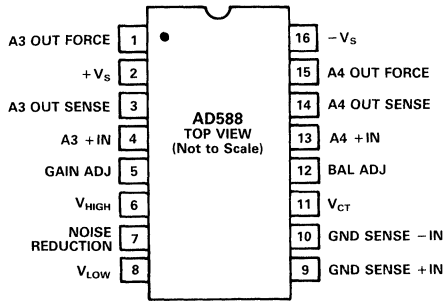
ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to $-V_S$ 36V
Power Dissipation (+25°C)
D Package 600mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
D (θ_{JA}/θ_{JC}) . . . . . 90/25°C/W
Output Protection: All outputs safe if shorted to ground

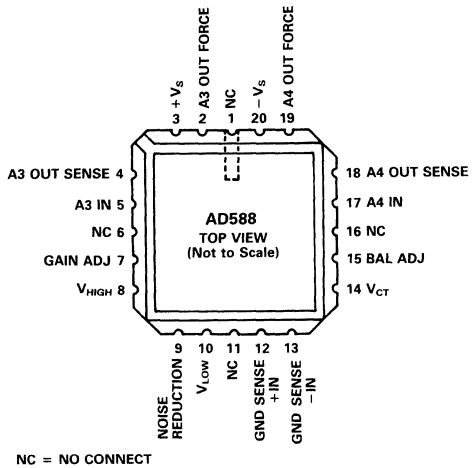
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

DIP



LCC



NC = NO CONNECT

THEORY OF OPERATION

The AD588 consists of a buried Zener diode reference, amplifiers used to provide pin programmable output ranges, and associated thin-film resistors as shown in the block diagram of Figure 1. The temperature compensation circuitry provides the device with a temperature coefficient of 1.5ppm/°C or less.

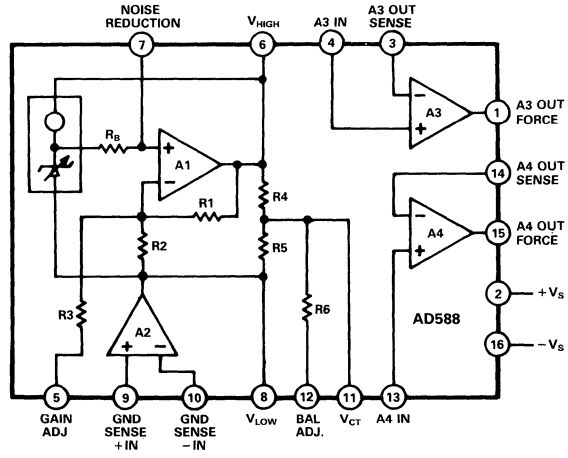


Figure 1. AD588 Functional Block Diagram

Amplifier A1 performs several functions. A1 primarily acts to amplify the Zener voltage from 6.5V to the required 10V output. In addition, A1 also provides for external adjustment of the 10V output through pin 5, the GAIN ADJUST. Using the bias compensation resistor between the Zener output and the non-inverting input to A1, a capacitor can be added at the NOISE REDUCTION pin (pin 7) to form a low pass filter and reduce the noise contribution of the Zener to the circuit. Two matched 10kΩ nominal thin film resistors (R4 & R5) divide the 10V output in half. Pin V_{CT} (pin 11) provides access to the center of the voltage span and pin 12 (BALANCE ADJUST) can be used for fine adjustment of this division.

Ground sensing for the circuit is provided by amplifier A2. The noninverting input (pin 9) senses the system ground which will be transferred to the point on the circuit where the inverting input (pin 10) is connected. This may be pin 6, 8 or 11. The output of A2 drives pin 8 to the appropriate voltage. Thus, if pin 10 is connected to pin 8, the V_{LOW} pin will be the same voltage as the system ground. Alternatively, if pin 10 is connected to the V_{CT} pin, it will be ground and pin 6 and pin 8 will be +5V and −5V respectively.

Amplifiers A3 and A4 are internally compensated and are used to buffer the voltages at pins 6, 8 and 11 as well as to provide a full Kelvin output. Thus, the AD588 has a full Kelvin capability by providing the means to sense a system ground and provide forced and sensed outputs referenced to that ground.

8

Applying the AD588

APPLYING THE AD588

The AD588 can be configured to provide +10V and −10V reference outputs as shown in Figures 2a and 2c respectively. It can also be used to provide +5V, −5V or a ±5V tracking reference as shown in Figure 2b. Table I details the appropriate pin connections for each output range. In each case, pin 9 is connected to system ground and power is applied to pins 2 and 16.

The architecture of the AD588 provides ground sense and uncommitted output buffer amplifiers which offer the user a great deal of functional flexibility. The AD588 is specified and tested in the configurations shown in Figure 2. The user may choose to take advantage of the many other configuration options available with the AD588. However, performance in these configurations is not guaranteed to meet the extremely stringent data sheet specifications.

As indicated in Table I, a +5V buffered output can be provided using amplifier A4 in the +10V configuration (Figure 2a). A −5V buffered output can be provided using amplifier A3 in the −10V configuration (Figure 2c). Specifications are not guaranteed for the +5V or −5V outputs in these configurations. Performance will be similar to that specified for the +10V or −10V outputs.

As indicated in Table I, unbuffered outputs are available at pins 6, 8 and 11. Loading of these unbuffered outputs will impair circuit performance.

Amplifiers A3 and A4 can be used interchangeably. However, the AD588 is tested (and the specifications are guaranteed) with the amplifiers connected as indicated in Figure 2 and Table I. When either A3 or A4 is unused, its output force and sense pins should be connected and the input tied to ground.

Two outputs of the same voltage may be obtained by connecting both A3 and A4 to the appropriate unbuffered output on pin 6, 8 or 11. Performance in these dual output configurations will typically meet data sheet specifications.

CALIBRATION

Generally, the AD588 will meet the requirements of a precision system without additional adjustment. Initial output voltage error of 1mV and output noise specs of 10μV p-p allow for accuracies of 12-16 bits. However, in applications where an even greater level of accuracy is required, additional calibration may be called for. Provision for trimming has been made through the use of the GAIN ADJUST and BALANCE ADJUST pins (pins 5 and 12 respectively).

The AD588 provides a precision 10V span with a center tap (V_{CT}) which is used with the buffer and ground sense amplifiers to achieve the voltage output configurations in Table I. GAIN ADJUST and BALANCE ADJUST can be used in any of these configurations to trim the magnitude of the span voltage and the position of the center tap within the span. The GAIN ADJUST should be performed first. Although the trims are not interactive within the device, the GAIN trim will move the BALANCE trim point as it changes the magnitude of the span.

Figure 2b. shows GAIN and BALANCE trims in a +5V and −5V tracking configuration. A 100kΩ 20-turn potentiometer is used for each trim. The potentiometer for GAIN trim is connected between pins 6 (V_{HIGH}) and 8 (V_{LOW}) with the wiper connected to pin 5 (GAIN ADJ). The potentiometer is adjusted to produce exactly 10V between pins 1 and 15, the amplifier outputs. The BALANCE potentiometer, also connected between pins 6 and 8 with the wiper to pin 12 (BAL ADJ), is then adjusted to center the span from +5V to −5V.

Trimming in other configurations works in exactly the same manner. When producing +10V and +5V, GAIN ADJ is used to trim +10V and BAL ADJ is used to trim +5V. In the −10V and −5V configuration, GAIN ADJ is again used to trim the magnitude of the span, −10V, while BAL ADJ is used to trim the center tap, −5V.

Range	Connect Pin 10 to Pin:	Unbuffered[1] Output on Pins −10V	−5V	0V	+5V	+10V	Buffered Output Connections	Buffered Output on Pins −10V	−5V	0V	+5V	+10V
+10V	8	–	–	8	11	6	11-13 & 14-15	–	–	–	15	–
							6-4 & 3-1	–	–	–	–	1
−5V or +5V	11	–	8	11	6	–	8-13 & 14-15	–	15	–	–	–
							6-4 & 3-1	–	–	–	1	–
−10V	6	8	11	6	–	–	8-13 & 14-15	15	–	–	–	–
							11-4 & 3-1	–	1	–	–	–
+5V	11	–	–	–	6	–	6-4 & 3-1	–	–	–	1	–
−5V		–	8	–	–	–	8-13 & 14-15	–	15	–	–	–

[1]"Unbuffered" outputs should not be loaded.

Table I. AD588 Connections

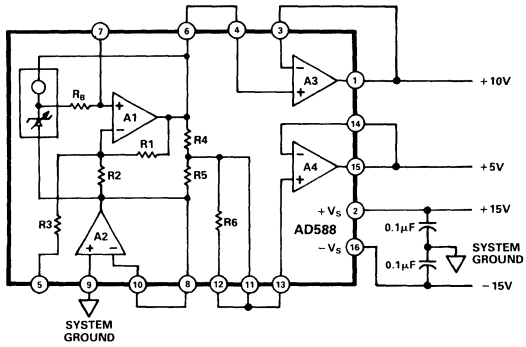


Figure 2a. +10V Output

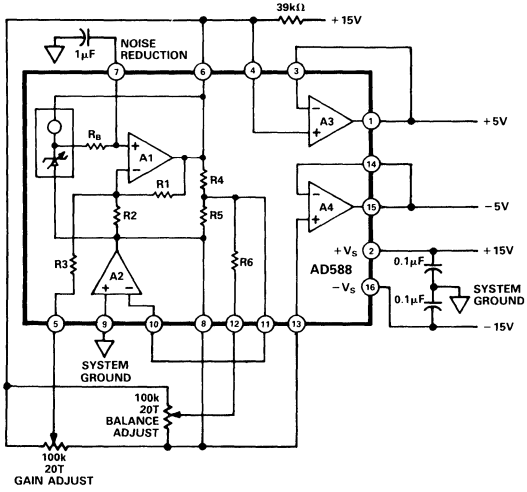


Figure 2b. +5V and −5V Outputs

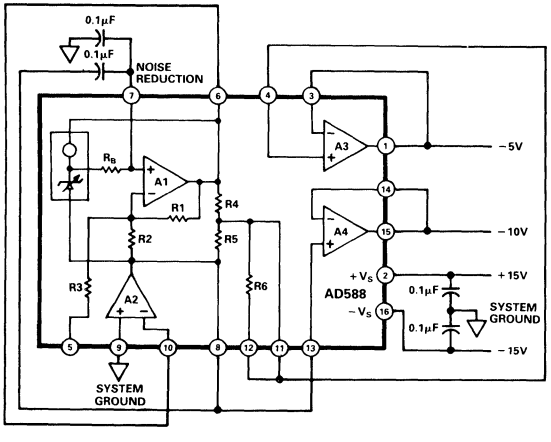


Figure 2c. −10V Output

In single output configurations, GAIN ADJ is used to trim outputs utilizing the full span (+10V or −10V) while BAL ADJ is used to trim outputs using half the span (+5V or −5V).

Input impedance on both the GAIN ADJUST and BALANCE ADJUST pins is approximately 150kΩ. The GAIN ADJUST trim network effectively attenuates the 10V across the trim potentiometer by a factor of about 1500 to provide a trim range of −3.5mV to +7.5mV with a resolution of approximately 550μV/turn (20 turn potentiometer). The BALANCE ADJUST trim network attenuates the trim voltage by a factor of about 1400, providing a trim range of ±4.5mV with resolution of 450μV/turn.

Trimming the AD588 introduces no additional errors over temperature so precision potentiometers are not required.

For single output voltage ranges, or in cases when BALANCE ADJUST is not required, pin 12 should be connected to pin 11. If GAIN ADJUST is not required, pin 5 should be left floating.

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD588 is typically less than 6μV p-p over the 0.1Hz to 10Hz band. Noise in a 1MHz bandwidth is approximately 600μV p-p. The dominant source of this noise is the buried Zener which contributes approximately 100nV/$\sqrt{\text{Hz}}$. In comparison, the op amp's contribution is negligible. Figure 3 shows the 0.1Hz to 10Hz noise of a typical AD588.

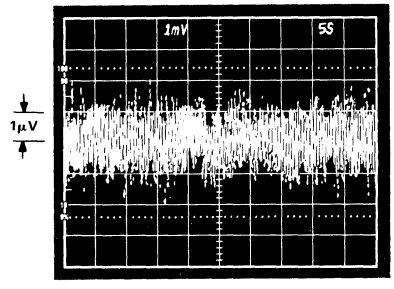


Figure 3. 0.1Hz to 10Hz Noise

If further noise reduction is desired, an optional capacitor may be added between the NOISE REDUCTION pin and ground as shown in Figure 2b. This will form a low pass filter with the 4kΩ R_B on the output of the Zener cell. A 1μF capacitor will have a 3dB point at 40Hz and will reduce the high frequency (to 1MHz) noise to about 200μV p-p. Figure 4 shows the 1MHz noise of a typical AD588 both with and without a 1μF capacitor.

Note that a second capacitor is needed in order to implement the NOISE REDUCTION feature when using the AD588 in the −10V mode (Figure 2c.). The NOISE REDUCTION capacitor is limited to 0.1μF maximum in this mode.

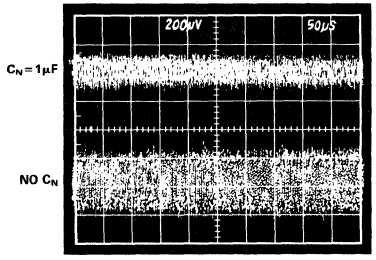
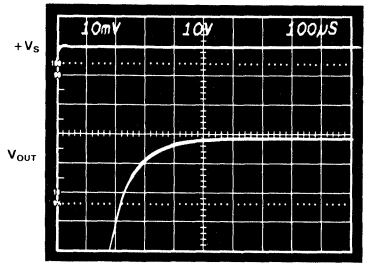


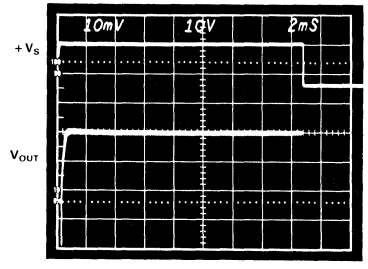
Figure 4. Effect of 1μF Noise Reduction Capacitor on Broadband Noise

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is the turn-on settling time. Two components normally associated with this are: time for active circuits to settle and time for thermal gradients on the chip to stabilize. Figure 5 shows the turn-on characteristics of the AD588. It shows the settling to be about 600μs. Note the absence of any thermal tails when the horizontal scale is expanded to 2ms/cm in Figure 5b.



a. Electrical Turn-On



b. Extended Time Scale

Figure 5. Turn-On Characteristics

Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor presents an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn-on time. In the case of a 1μF capacitor, the initial turn-on time is approximately 60ms (see Figure 6).

Note: If the NOISE REDUCTION feature is used in the ±5V configuration, a 39kΩ resistor between pins 6 and 2 is required for proper startup.

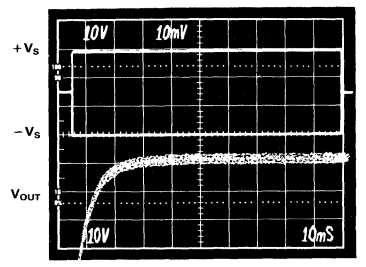


Figure 6. Turn-on with 1μF C_N

TEMPERATURE PERFORMANCE

The AD588 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Figure 7 shows typical output voltage drift for the AD588BD and illustrates the test methodology. The box in Figure 7 is bounded on the sides by the operating temperature extremes and on top and bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left corner of the box determines the performance grade of the device.

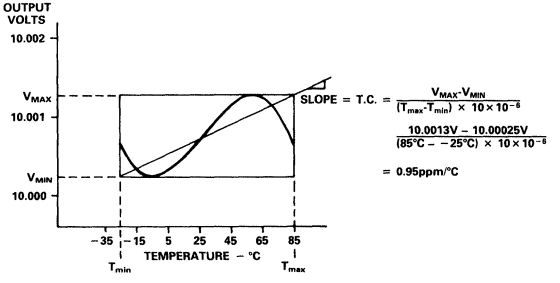


Figure 7. Typical AD588BD Temperature Drift

Each AD588A and B grade unit is tested at −25°C, 0°C, +25°C, +50°C, +70°C and +85°C. Each AD588S and T grade unit is tested at −55°C, −25°C, 0°C, +25°C, +50°C, +70°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. Maximum height of the box for the appropriate temperature range is shown in Figure 8. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD588 will produce a curve similar to that in Figure 7, but output readings may vary depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE mV		
	0 TO +70°C	−25°C TO +85°C	−55°C TO +125°C
AD588AD	1.40 (typ)	3.30	
AD588BD	1.05	3.30	
AD588SD			10.80
AD588TD			7.20

Figure 8. Maximum Output Change – mV

KELVIN CONNECTIONS

Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. As seen in Figure 9a, the load current and wire resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. The Kelvin connection of Figure 9b overcomes the problem by including the wire resistance within the forcing loop of the amplifier and sensing the load voltage. The amplifier corrects for any errors in the load voltage. In the circuit shown, the output of the amplifier would actually be at 10 volts + V_{ERROR} and the voltage at the load would be the desired 10 volts.

The AD588 has three amplifiers which can be used to implement Kelvin connections. Amplifier A2 is dedicated to the ground force-sense function while uncommitted amplifiers A3 and A4 are free for other force-sense chores.

In some single-output applications, one amplifier may be unused.

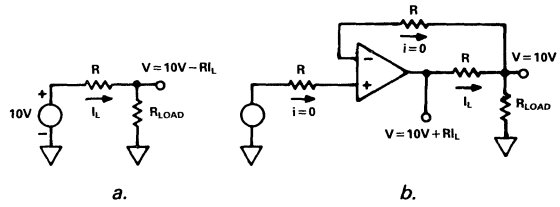
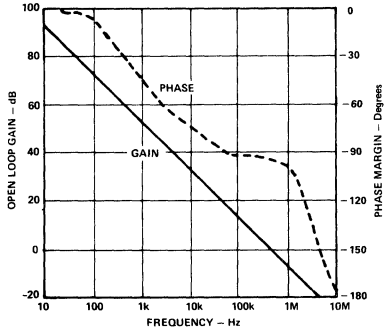


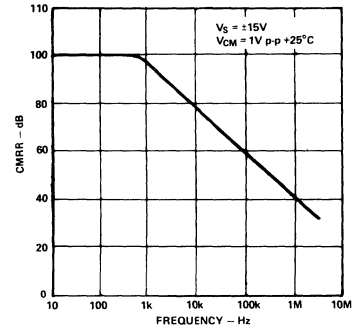
Figure 9. Advantage of Kelvin Connection

In such cases, the unused amplifier should be connected as a unity-gain follower (force + sense pin tied together) and the input should be connected to ground.

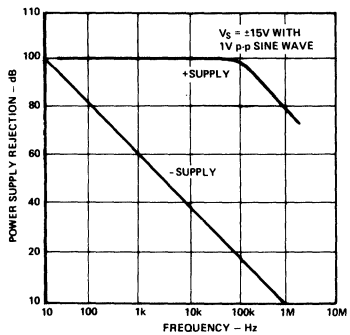
An unused amplifier section may be used for other circuit functions as well. The curves on this page show the typical performance of A3 and A4.



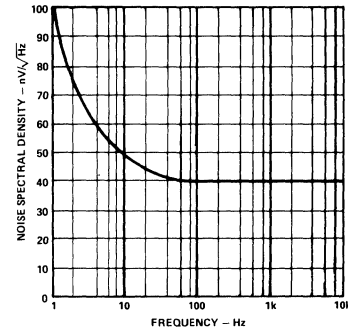
Open Loop Frequency Response (A3, A4)



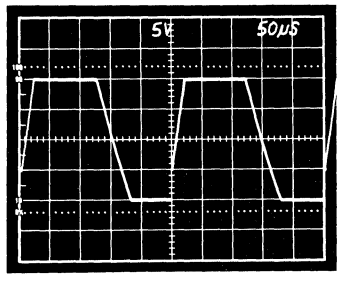
Common Mode Rejection vs. Frequency (A3, A4)



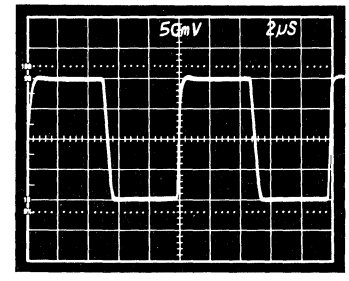
Power Supply Rejection vs. Frequency (A3, A4)



Input Noise Voltage Spectral Density



Unity Gain Follower Pulse Response (Large Signal)



Unity Gain Follower Pulse Response (Small Signal)

8

DYNAMIC PERFORMANCE

The output buffer amplifiers (A3 and A4) are designed to provide the AD588 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 10 displays the characteristics of the AD588 output amplifier driving a 0 to 10mA load.

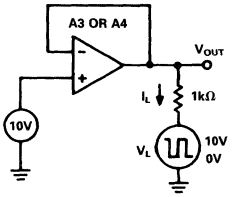


Figure 10a. Transient Load Test Circuit

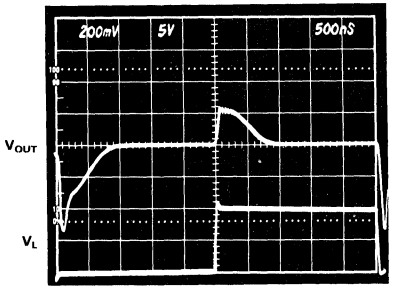


Figure 10b. Large-Scale Transient Response

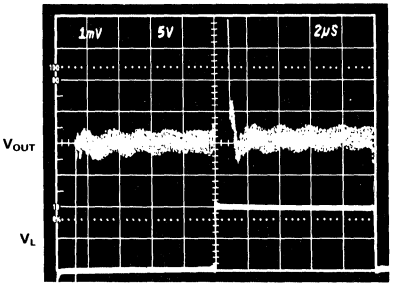


Figure 10c. Fine Scale Settling for Transient Load

Figure 11 displays the output amplifier characteristics driving a 5mA to 10mA load, a common situation found when the reference is shared among multiple converters or is used to provide a bipolar offset current.

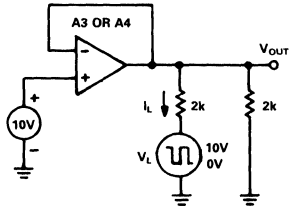


Figure 11a. Transient and Constant Load Test Circuit

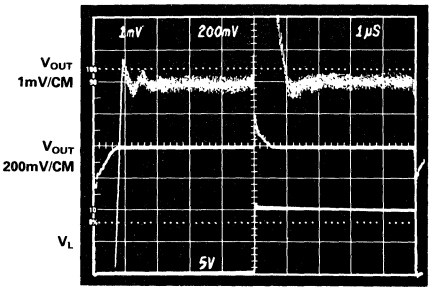


Figure 11b. Transient Response 5-10mA Load

In some applications, a varying load may be both resistive and capacitive in nature, or be connected to the AD588 by a long capacitive cable.

Figure 12 displays the output amplifier characteristics driving a 1,000pF, 0-to-10mA load.

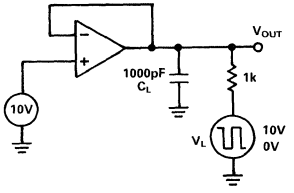


Figure 12a. Capacitive Load Transient Response Test Circuit

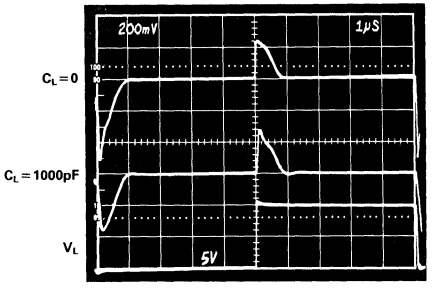


Figure 12b. Output Response with Capacitive Load

Figure 13 displays the crosstalk between output amplifiers. The top trace shows the output of A4, dc-coupled and offset by 10 volts, while the output of A3 is subjected to a 0-to-10mA load current step. The transient at A4 settles in about 1µs, and the load-induced offset is about 100µV.

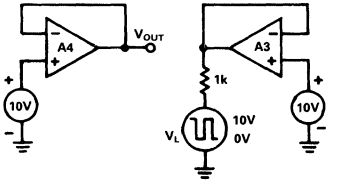


Figure 13a. Load Crosstalk Test Circuit

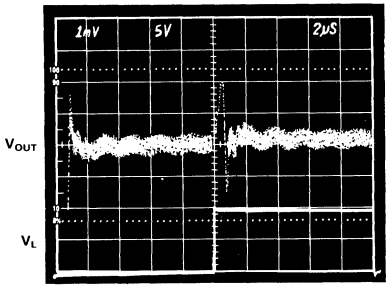


Figure 13b. Load Crosstalk

Attempts to drive a large capacitive load (in excess of 1,000pF) may result in ringing or oscillation, as shown in the step response photo (Figure 14a). This is due to the additional pole formed by the load capacitance and the output impedance of the amplifier, which consumes phase margin. The recommended method of driving capacitive loads of this magnitude is shown in Figure 14b. The 150Ω resistor isolates the capacitive load from the output stage, while the 1MΩ resistor provides a dc feedback path and preserves the output accuracy. The 150pF capacitor provides a high-frequency feedback loop. The performance of this circuit is shown in Figure 14c.

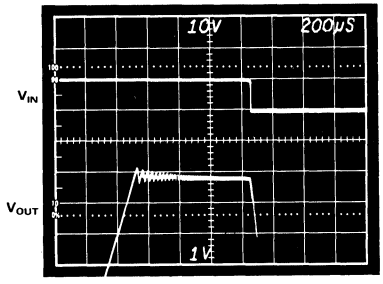


Figure 14a. Output Amplifier Step Response, $C_L = 1\mu F$

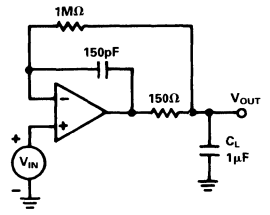


Figure 14b. Compensation for Capacitive Loads

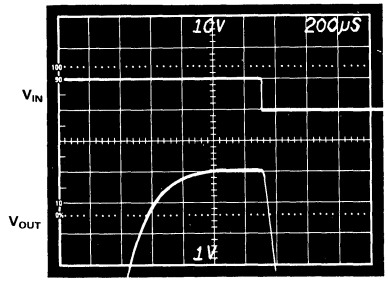


Figure 14c. Output Amplifier Step Response Using Figure 14b Compensation

USING THE AD588 WITH CONVERTERS

The AD588 is an ideal reference for a wide variety of A/D and D/A converters. Several representative examples follow.

14-Bit Digital-to-Analog Converter – AD7535

High resolution CMOS D/A converters require a reference voltage of high precision to maintain rated accuracy. The combination of the AD588 and AD7535 takes advantage of the initial accuracy, drift and full Kelvin output capability of the AD588 as well as the resolution, monotonicity and accuracy of the AD7535 to produce a subsystem with outstanding characteristics.

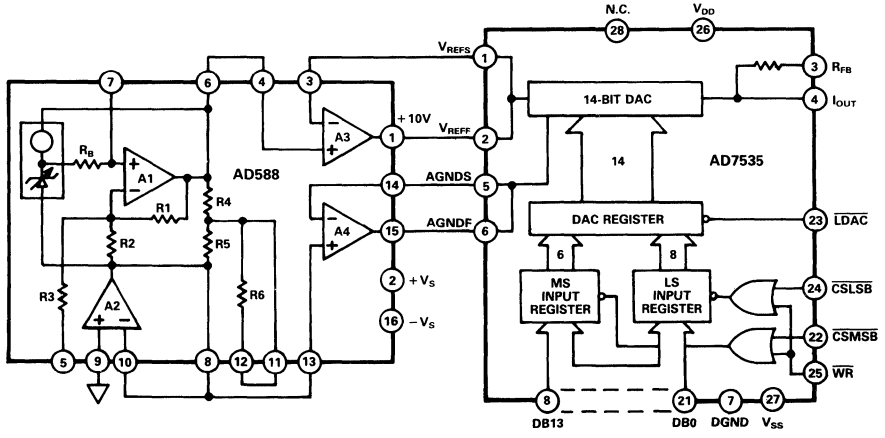


Figure 15. AD588/AD7535 Connections

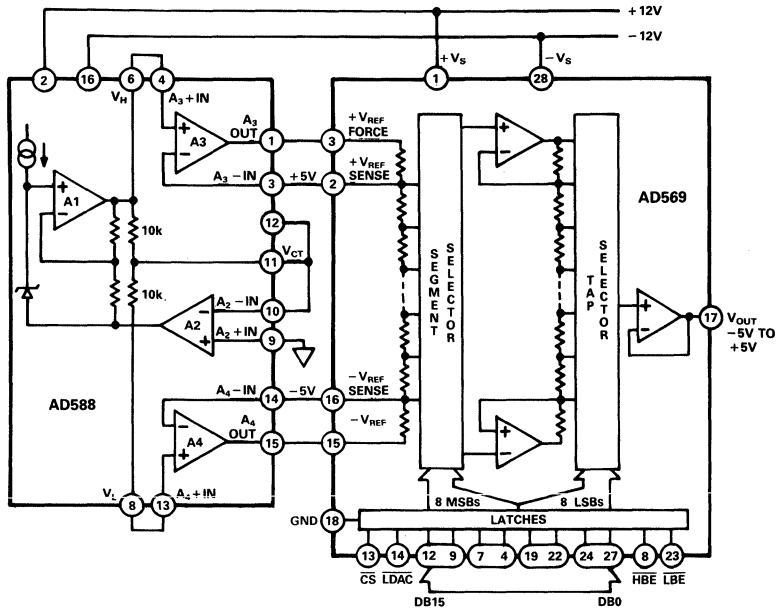


Figure 16. High-Accuracy ±5V Tracking Reference for AD569

16-Bit Digital-to-Analog Converter – AD569

Another application which fully utilizes the capabilities of the AD588 is supplying a reference for the AD569, as shown in Figure 16. Amplifier A2 senses system common and forces V_{CT} to assume this value, producing +5V and −5V at pins 6 and 8 respectively. Amplifiers A3 and A4 buffer these voltages out to the appropriate reference force-sense pins of the AD569. The full Kelvin scheme eliminates the effect of the circuit traces or wires and the wire bonds of the AD588 and AD569 themselves, which would otherwise degrade system performance.

SUBSTITUTING FOR INTERNAL REFERENCES

Many converters include built-in references. Unfortunately, such references are the major source of drift in these converters. By using a more stable external reference like the AD588, drift performance can be improved dramatically.

12-Bit Analog-to-Digital Conveter – AD574A

The AD574A is specified for gain drift from 10ppm/°C to 50ppm/°C, (depending on grade) using the on-chip reference. The reference contributes typically 75% of this drift. Therefore, the total drift using an AD588 to supply the reference can be improved by a factor of 3 to 4.

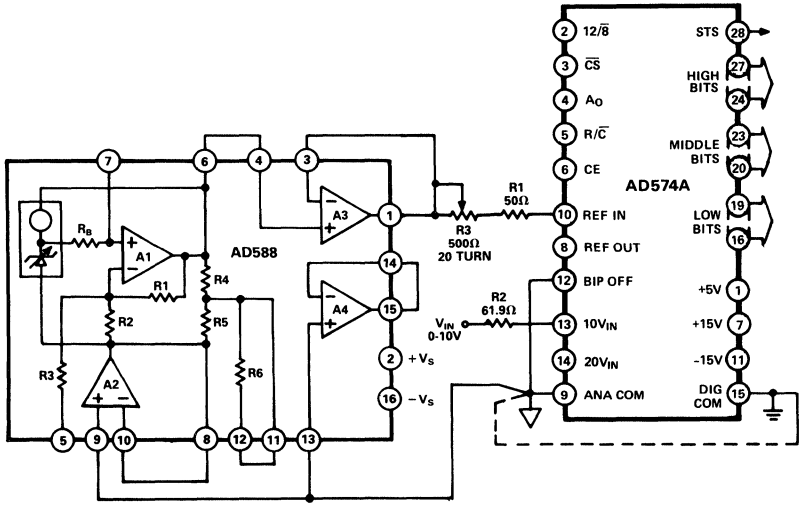


Figure 17. AD588/AD574A Connections

Using this combination may result in apparent increases in full-scale error due to the difference between the on-board reference by which the device is laser trimmed and the external reference with which the device is actually applied. The on-board reference is specified to be 10V ± 100mV while the external reference is specified to be 10V ± 1mV. This may result in up to 101mV of apparent full-scale error beyond the ± 25mV specified AD574 gain error. Resistors R2 and R3 allow this error to be nulled. Their contribution to full-scale drift is negligible.

The high output drive capability allows the AD588 to drive up to 6 converters in a multi-converter system. All converters will have gain errors that track to better than ± 5ppm/°C.

RTD EXCITATION

The Resistance Temperature Detector (RTD) is a circuit element whose resistance is characterized by a positive temperature coefficient. A measurement of resistance indicates the measured temperature. Unfortunately, the resistance of the wires leading to the RTD often adds error to this measurement. The 4-wire ohms measurement overcomes this problem. This method uses two wires to bring an excitation current to the RTD and two additional wires to tap off the resulting RTD voltage. If these additional two wires go to a high input impedance measurement circuit, the effect of their resistance is negligible. Therefore, they transmit the true RTD voltage.

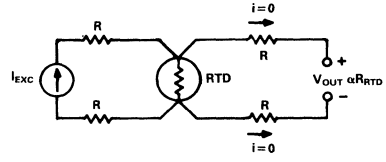


Figure 18. 4-Wire Ohms Measurement

A practical consideration when using the 4-wire ohms technique with an RTD is the self-heating effect that the excitation current has on the temperature of the RTD. The designer must choose the smallest practical excitation current that still gives the desired resolution. RTD manufactures usually specify the self-heating effect of each of their models or types of RTDs.

Figure 19 shows an AD588 providing the precision excitation current for a 100Ω RTD. The small excitation current of 1mA dissipates a mere 0.1mW of power in the RTD.

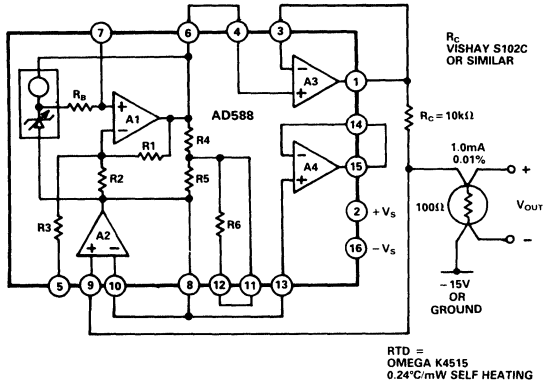


Figure 19. Precision Current Source for RTD

BOOSTED PRECISION CURRENT SOURCE

In the RTD current-source application the load current is limited to ± 10mA by the output drive capability of amplifier A3. In the event that more drive current is needed, a series pass transistor can be inserted inside the feedback loop to provide higher current. Accuracy and drift performance are unaffected by the pass transistor.

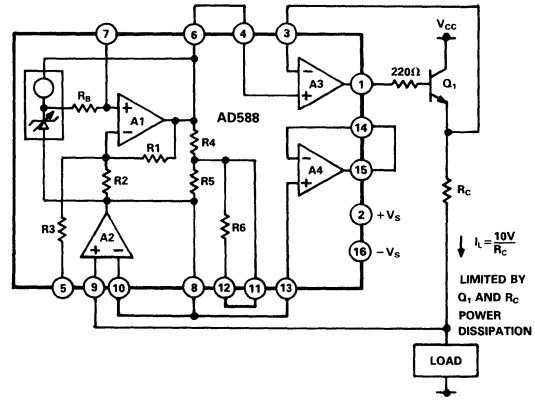
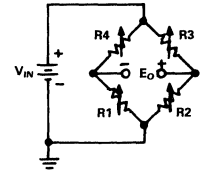


Figure 20. Boosted Precision Current Source

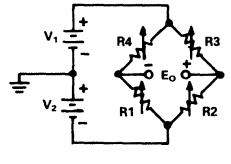
BRIDGE DRIVER CIRCUITS

The Wheatstone bridge is a common transducer. In its simplest form, a bridge consists of 4 two terminal elements connected to form a quadrilateral, a source of excitation connected along one of the diagonals and a detector comprising the other diagonal. Figure 21a shows a simple bridge driven from a unipolar excitation supply. E_O, a differential voltage, is proportional to the deviation of the element from the initial bridge values. Unfortunately, this bridge output voltage is riding on a common-mode voltage equal to approximately $V_{IN}/2$. Further processing of this signal may necessarily be limited to high common-mode rejection techniques such as instrumentation or isolation amplifiers.

Figure 21b shows the same bridge transducer, but this time it is driven from pair of bipolar supplies. This configuration ideally eliminates the common-mode voltage and relaxes the restrictions on any processing elements that follow.



a. Unipolar Drive



b. Bipolar Drive

Figure 21. Bridge Transducer Excitation

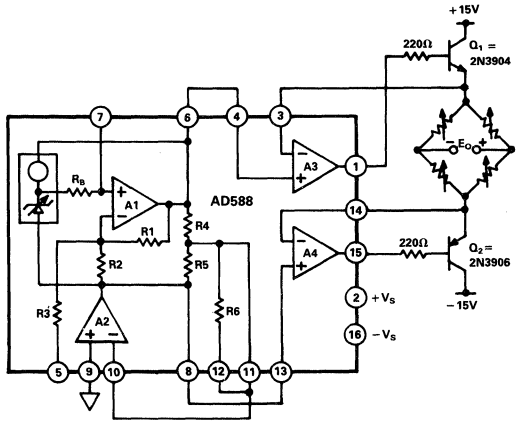


Figure 22. Bipolar Bridge Drive

As shown in Figure 22, the AD588 is an excellent choice for the control element in a bipolar bridge driver scheme. Transistors Q1 and Q2 serve as series pass elements to boost the current drive capability to the 28mA required by a typical 350Ω bridge. A differential gain stage may still be required if the bridge balance is not perfect. Such gain stages can be expensive.

Additional common-mode voltage reduction is realized by using the circuit illustrated in Figure 23. A1, the ground sense amplifier, servo's the supplies on the bridge to maintain a virtual ground at one center tap. The voltage which appears on the opposite center tap is now single-ended (referred to ground) and can be amplified by a less expensive circuit.

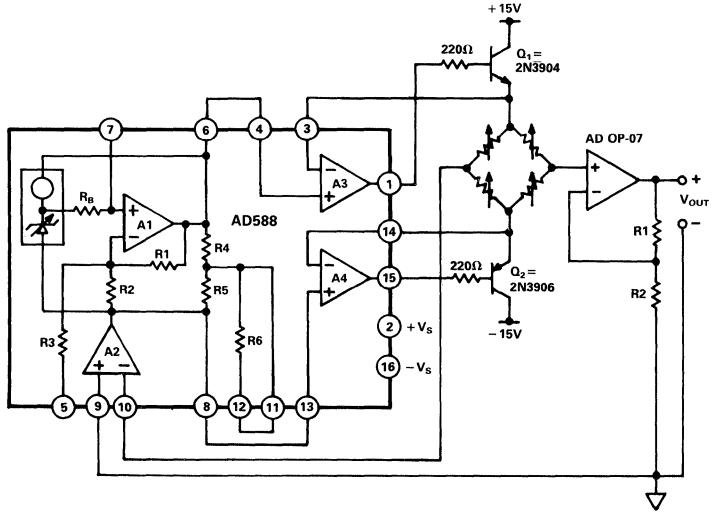


Figure 23. Floating Bipolar Bridge Drive with Minimum CMV

ANALOG DEVICES

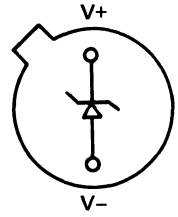
Two-Terminal IC 1.2V Reference

AD589

FEATURES

Superior Replacement for Other 1.2V References
Wide Operating Range: 50μA to 5mA
Low Power: 60μW Total P_D at 50μA
Low Temperature Coefficient:
10ppm/°C max, 0 to +70°C (AD589M)
25ppm/°C max, -55°C to +125°C (AD589U)
Two Terminal "Zener" Operation
Low Output Impedance: 0.6Ω
No Frequency Compensation Required
Low Cost

AD589 FUNCTIONAL BLOCK DIAGRAM



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589 is available in seven versions. The AD589J, K, L and M grades are specified for 0 to +70°C operation, while the S, T and U grades are rated for the full -55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD589 is a two-terminal device which delivers a a constant reference voltage for a wide range of input current.
2. Output impedance of 0.6Ω and temperature coefficients as low as 10ppm/°C insure stable output voltage over a wide range of operating conditions.
3. The AD589 can be operated as a positive or negative reference. "Floating" operation is also possible.
4. The AD589 will operate with total current as low as 50μA (60μW total power dissipation), ideal for battery powered instrument applications.
5. The AD589 is an exact replacement for other 1.2V references, offering superior temperature performance and reduced sensitivity to capacitive loading.

8

SPECIFICATIONS (typical @ I_{IN} = 500μA and T_A = +25°C unless otherwise noted)

Model	AD589JH			AD589KH			AD589LH			AD589MH			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE, T_A = +25°C	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	V
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA – 5mA)			5			5			5			5	mV
DYNAMIC OUTPUT IMPEDANCE		0.6	**2**		0.6	**2**		0.6	**2**		0.6	**2**	Ω
RMS NOISE VOLTAGE 10Hz<f<10kHz		5			5			5			5		μV
TEMPERATURE COEFFICIENT[1]			100			**50**			**25**			**10**	ppm/°C
TURN-ON SETTLING TIME TO 0.1%		25			25			25			25		μs
OPERATING CURRENT[2]	**0.05**		5	**0.05**		5	**0.05**		5	**0.05**		5	mA
OPERATING TEMPERATURE	0		+70	0		+70	0		+70	0		+70	°C
PACKAGE OPTION[3] Metal Can (H-02A)	AD589JH			AD589KH			AD589LH			AD589MH			

Model	AD589SH			AD589TH			AD589UH			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE, T_A = +25°C	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	V
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA – 5mA)			5			5			5	mV
DYNAMIC OUTPUT IMPEDANCE		0.6	**2**		0.6	**2**		0.6	**2**	Ω
RMS NOISE VOLTAGE 10Hz<f<10kHz		5			5			5		μV
TEMPERATURE COEFFICIENT[1]			**100**			**50**			**25**	ppm/°C
TURN-ON SETTLING TIME TO 0.1%		25			25			25		μs
OPERATING CURRENT[2]	**0.05**		5	**0.05**		5	**0.05**		5	mA
OPERATING TEMPERATURE	–55		+125	–55		+125	–55		+125	°C
PACKAGE OPTION[3] Metal Can (H-02A)	AD589SH			AD589TH			AD589UH			

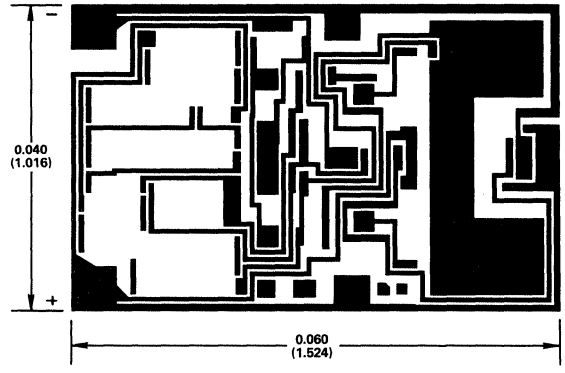
NOTES
[1]See following page for explanation of temperature coefficient measurement method.
[2]Optimum performance is obtained at currents below 500μA.
Stray shunt capacitances should be minimized. If strays cannot be avoided, a shunt capacitor of at least 1000pF is recommended.
[3]See Section 14 for package outline information.
Specifications shown in boldface are tested on all production units at final electrical test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Current 10mA
Reverse Current 10mA
Power Dissipation[1] 125mW
Storage Temperature Range . . . . . –65°C to +175°C
Operating Junction Temperature Range . –55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

NOTE
[1]Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and $\theta_{JA} = 400 = C/W$.

AD589 CHIP DIMENSIONS AND PAD LAYOUT



THE AD589 IS AVAILABLE IN CHIP FORM WITH FULLY TESTED AND GUARANTEED SPECIFICATIONS. CONSULT FACTORY FOR AVAILABLE GRADES AND PRICING.

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD589 consistently follows the curve shown in Figure 1. Three-point measurement guarantees the error band over the specified temperature range. The temperature coefficients specified on page 2 represent the slopes of the diagonals of the error band from +25°C to T_{min} and +25°C to T_{max}.

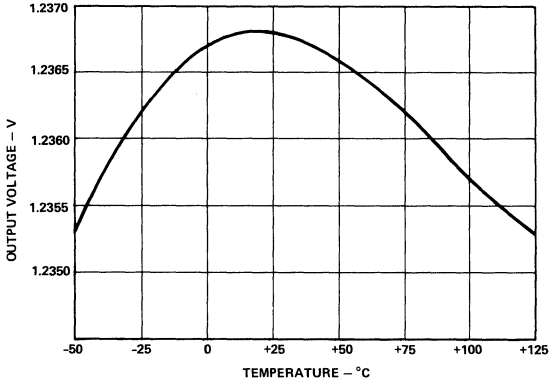


Figure 1. Typical AD589 Temperature Characteristics

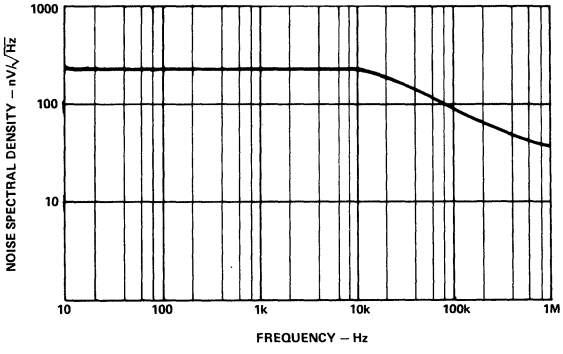


Figure 2. Noise Spectral Density

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 3 displays the turn-on characteristic of the AD589. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 25μs, and there is no long thermal tail appearing after that point.

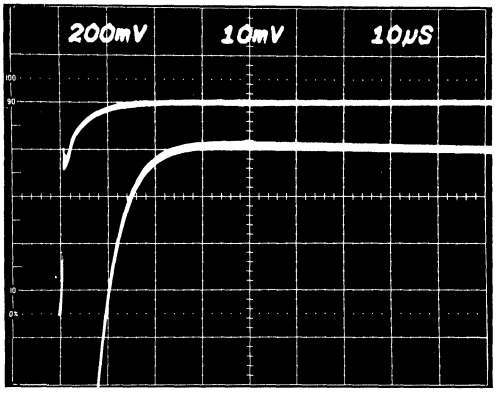


Figure 3. Output Settling Characteristics

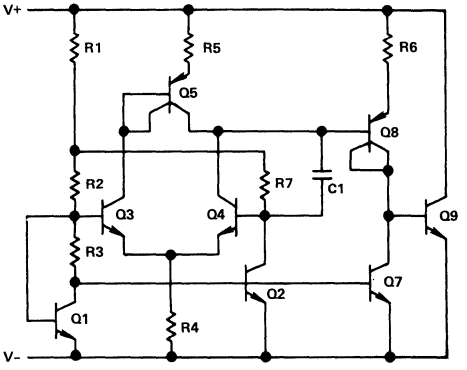


Figure 4. Schematic Diagram

APPLICATION INFORMATION

The AD589 functions as a two-terminal shunt-type regulator. It provides a constant 1.23V output for a wide range of input current from 50μA to 5mA. Figure 5 shows the simplest configuration for an output voltage of 1.2V or less. Note that no frequency compensation is required. If additional filtering is desired for ultra low noise applications, minimum recommended capacitance is 1000pF.

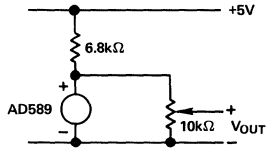


Figure 5. Basic Configuration for 1.2V or Less

The AD589 can also be used as a building block to generate other values of reference voltage. Figure 6 shows a circuit which produces a buffered 10V output. Total supply current for this circuit is approximately 2mA.

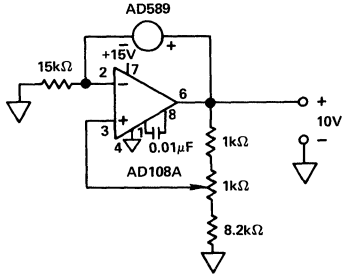
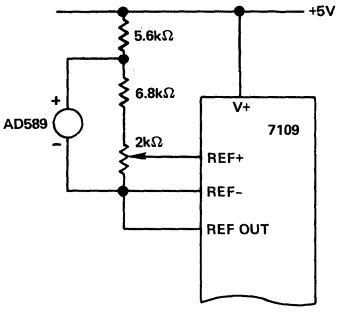
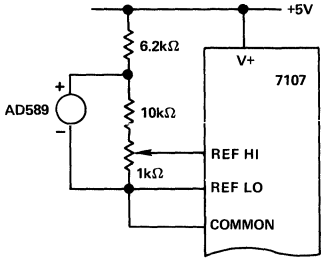


Figure 6. Single-Supply Buffered 10V Reference

The low power operation of the AD589 makes it ideal for use in battery operated portable equipment. It is especially useful as a reference for CMOS analog-to-digital converters. Figure 7 shows the AD589 used in conjunction with two popular integrating type CMOS A/D converters.



a. With 7109 12-Bit Binary A/D



b. With 7107 Panel Meter A/D

Figure 7. AD589 Used as Reference for CMOS A/D Converters

The AD589 also is useful as a reference for CMOS multiplying DACs such as the AD7533. These DACs require a negative reference voltage in order to provide a positive output range. Figure 8 shows the AD589 used to supply an equivalent -1.0V reference to an AD7533.

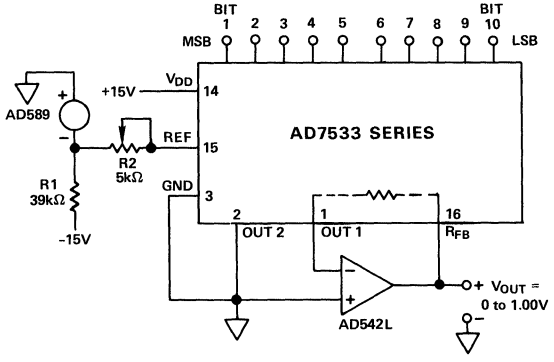


Figure 8. AD589 as Reference for 10-Bit CMOS DAC

ANALOG DEVICES

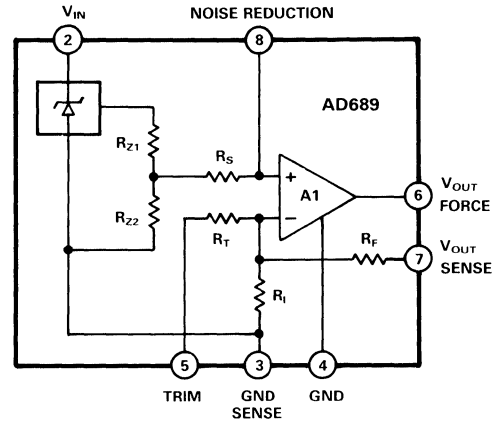
High Precision 8.192V Reference

AD689

FEATURES

Laser Trimmed to High Accuracy:
8.192V ±4mV (L, T Grades)
Input Voltage Range from 10.8V to 36V
Provides Convenient Scaling for Converters:
2mV/LSB for 12-Bit Converters
Trimmed Temperature Coefficients:
5ppm/°C max, 0 to +70°C (L Grade)
10ppm/°C max, −55 to +125°C (T Grade)
Noise Reduction Capability
Versatile Force and Sense Connections

AD689 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD689 is the industry's first precision reference to deliver a voltage between traditional 5V and 10V references. The AD689 will accurately deliver 8.192V while operating on supply voltages of ±12V, with ±10% tolerances. All 10V references require greater than 10.8V (12V-10%) to operate properly, forcing the use of 5V references in most 12V systems. An 8.192V reference provides a major increase in signal range. The AD689 also features excellent static and dynamic line and load regulation characteristics.

The AD689 uses a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors. Trimming is performed for initial accuracy and temperature coefficient, resulting in very low errors over temperature without the use of additional components.

The AD689 includes the reference cell and an amplifier which is laser trimmed for low drift. Force and sense connections can be made on both the amplifier output and ground to maintain the accuracy of the reference cell. This allows the AD689 to be used with boosters for driving long lines or high current loads while maintaining full accuracy at the load.

The AD689 is recommended for use in all data conversion applications where ±12V ±10% supplies preclude the use of both external and internal 10V references.

The AD689J, K and L are tested and specified for operation from 0 to +70°C, and the AD689S and T are tested and specified for −55°C to +125°C operation. All grades are packaged in an 8-pin cerdip.

PRODUCT HIGHLIGHTS

1. Laser trimming of both the initial accuracy and the temperature coefficient results in very low errors over temperature without the use of external components.
2. For applications requiring higher initial accuracy, an optional fine trim connection is provided. The trim range allows the output voltage to be accurately set down to 8.000V.
3. Output noise of the AD689 is very low, typically 2μV p-p. A noise reduction pin is provided for additional noise filtering with an external capacitor.
4. Force and sense connections allow remote sensing of load and ground variations to accurately supply 8.192V at the load.
5. The AD689 sources and sinks current with excellent regulation, allowing a variety of both positive and negative output voltage configurations.

SPECIFICATIONS (T_A = +25°C, V_{IN} = +12V, ±10% unless otherwise specified)

	AD689J			AD689K			AD689L			AD689S			AD689T			
Model	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	**8.176**		**8.208**	**8.184**		**8.200**	**8.188**		**8.196**	**8.176**		**8.208**	**8.188**		**8.196**	V
Output Voltage Drift[1]																
0 to +70°C			**25**			**15**			**5**							ppm/°C
−55°C to +125°C												**20**			**10**	
Gain Adjustment	**+8**			**+8**			**+8**			**+8**			**+8**			%
	−3			**−3**			**−3**			**−3**			**−3**			
Line Regulation																
10.8V < +V_{IN} <36V																
T_{min} to T_{max}			**200**			**200**			**200**			**250**			**250**	±μV/V
Load Regulation																
Sourcing 0 < I_{OUT} <8.192mA																
Sinking −8.192 < I_{OUT} <0mA																
T_{min} to T_{max}			**100**			**100**			**100**			**100**			**100**	μV/mA
Quiescent Current		2	5		2	5		2	5		2	5		2	5	mA
Power Consumption		24	66		24	66		24	66		24	66		24	66	mW
Output Noise																
0.1Hz to 10Hz		2			2			2			2			2		μV p-p
Spectral Density, 100Hz		100			100			100			100			100		nV/√Hz
Long-Term Stability		15			15			15			15			15		ppm/1000Hr
Short-Circuit Current-to-Ground or V_{IN}		30	**50**		30	**50**		30	**50**		30	**50**		30	**50**	mA
Temperature Range																
Specified Performance	0		+70	0		+70	0		+70	−55		+125	−55		+125	°C
Operating Performance[2]	−40		+85	−40		+85	−40		+85	−55		+125	−55		+125	

NOTES

[1]Maximum output voltage drift is guaranteed for all packages and grades. Cerdip packaged parts are also 100% production tested.

[2]The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

Specifications subject to change without notice.

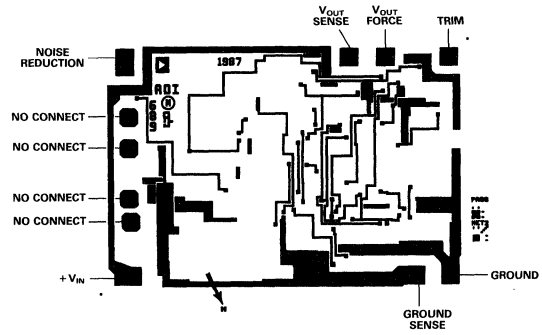
Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground . . . . . +36V
Power Dissipation (25°C) 500mW
GND to GNDS 200mV
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Package Thermal Resistance
θ_{JC} . . . . . 22°C/W
θ_{JA} . . . . . 110°C/W
Output Protection: Output safe for indefinite short to ground or V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BONDING DIAGRAM



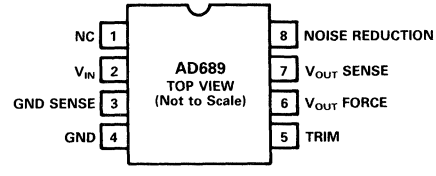
DIE SIZE: 0.081" × 0.060"

ORDERING GUIDE

Model	Initial Error mV	Temp. Coefficient ppm/°C	Temp. Range °C	Package Option*
AD689JQ	16	25	0 to +70	Cerdip (Q-8)
AD689KQ	8	15	0 to +70	Cerdip (Q-8)
AD689LQ	4	5	0 to +70	Cerdip (Q-8)
AD689SQ	16	20	−55 to +125	Cerdip (Q-8)
AD689TQ	4	10	−55 to +125	Cerdip (Q-8)
AD689JCHIPS	16	25	0 to +70	

*See Section 14 for package outline information.

CONNECTION DIAGRAM



THEORY OF OPERATION

The AD689 consists of a buried Zener diode reference, amplifier and several high stabilty thin-film resistors as shown in the block diagram in Figure 1. This design results in a high precision, monolithic 8.192V output reference with initial errors of less than 4mV. The temperature compensation circuitry provides the device with a temperature coefficient of less than 5ppm/°C.

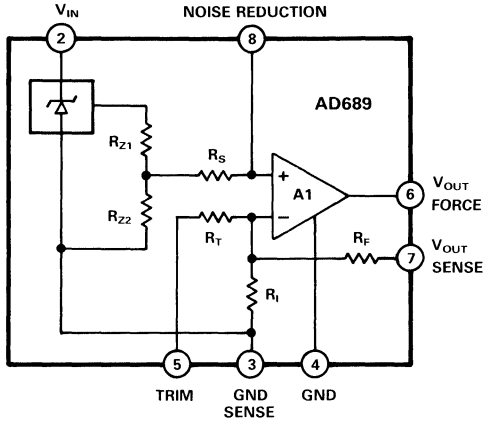


Figure 1. AD689 Functional Block Diagram

Amplifier A1 is configured to serve multiple functions. A1 primarily acts to amplify the Zener voltage from the buried Zener diode to the required 8.192V output. In addition, A1 is configured to allow force and sense connections from its output terminal to the feedback resistor (R_F) and from its ground reference to the buried Zener and input resistor (R_I) ground. A1 also provides adjustment of the 8.192V output through Pin 5, TRIM.

Separating A1 ground from the buried Zener diode ground provides many additional features. First it allows the AD689 to provide excellent load regulation when sourcing and sinking current. It reduces the total current that flows from the buried Zener diode ground to the sense node. This minimizes voltage drops due to parasitic impedances, hence allowing accurate sensing of voltage variations at the load ground. Finally, current variations due to temperature coefficients, which in turn cause voltage errors, are minimized by reducing the total current that would flow from a single ground point.

Using the bias compensation resistor (R_S) between the Zener output and the noninverting output of the amplifier, a capacitor can be added at the NOISE REDUCTION pin (Pin 8) to form a low pass filter and reduce the noise contribution of the Zener to the circuit.

APPLYING THE AD689

The 8.192V output of the AD689 allows convenient binarily scaled bit levels when used with data converters. With a 12-bit data converter the LSB would equal 8.192V/4096, or 2mV.

The AD689 is simple to use in virtually all precision reference applications. Pins 6 and 7 are connected together at the load; Pins 3 and 4 are grounded; and power is applied to Pin 2. No external components are required; the degree of desired absolute accuracy is achieved by simply selecting the required device grade. The AD689 requires less than 5mA quiescent current when operating from a supply of +10.8V to +36V.

An external fine trim may be added to null out initial voltage errors. The optional trim circuit shown in Figure 2 can adjust the 8.192V output from +8% (655mV) to −3% (−245mV) with minimal effect on other device characteristics.

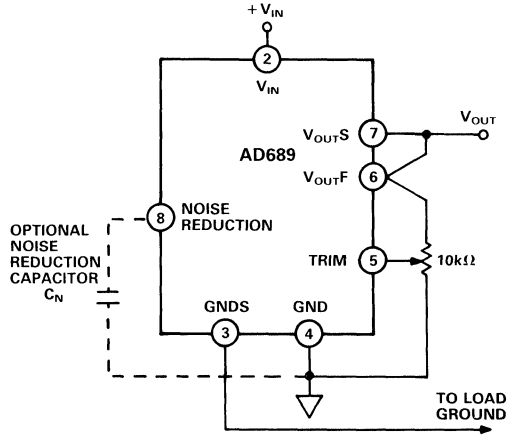


Figure 2. Optional Fine Trim Configuration

FORCE AND SENSE CONNECTIONS

Force and sense connections offer a convenient method of eliminating the effects of voltage drops in circuit wires. As seen in Figure 3a, the load current and wire resistance produce an error ($V_{ERROR} = R_W \times I_L$) at the load. The force and sense connection of Figure 3b overcomes the problem by including the wire resistance within the forcing loop of the amplifier and sensing the load voltage. The amplifier corrects for any errors in the load voltage. In the circuit shown, the output of the amplifier would actually be at 8.192V + V_{ERROR}, and the voltage at the load would be the desired 8.192V. If, for example, in Figure 3a the load resistor is sinking 8.192mA from the 8.192V reference and the load is 2 feet away using 28 gage wire (R = 0.066Ω/ft), the resulting V_{ERROR} would be $2 \times 0.066 \times 8.192\text{mA} = 1.08\text{mV}$. This represents greater than 0.5LSB of error in a 12-bit system.

Since amplifier A1 is not configured as a true buffer amplifier, the V_{OUT} SENSE pin (Pin 7) carries approximately 500μA of current. This level of current when used in the above example will result in 66μV of error, or 0.033LSB.

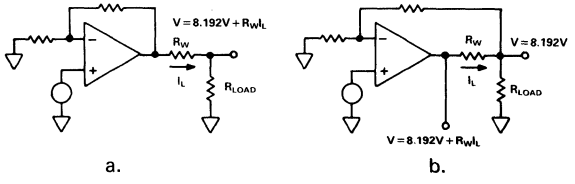


Figure 3. Advantage of Force and Sense Connections

GROUNDING CONSIDERATIONS

Analysis of the ground current magnitudes, ground current paths and ground impedances is crucial when high accuracy analog circuits are designed. The AD689 has two ground pins, GND (Pin 4) and GND SENSE (Pin 3). The GND pin is the ground reference for the internal operational amplifier. It will carry most of the quiescent current (I_Q = 5mA maximum) when the AD689 is sourcing current and up to an additional 8.192mA when the AD689 is sinking current. The GND SENSE pin is the reference for the buried Zener diode and gain setting resistors and carries approximately 1mA. Connecting GND SENSE to the load ground will allow the AD689 to accurately deliver 8.192V at the load, independent of variations of the "GND" voltage relative to the load ground.

The grounding method that is used depends on the accuracy requirements of the application. In general, GND SENSE should be connected to GND at the load ground, without connection to GND at the AD689.

Simple Ground Connection

Figure 4a shows a simple connection of the AD689 to a load resistor (R_L). GND and GND SENSE are connected at the load ground and the 8.192V is delivered across R_L.

High Accuracy Ground Connection and Analysis

Figure 4b shows the addition of Z_W, and Z_{G1} and Z_{GN}. They represent the sense wire, the AD689 ground wire and additional ground wire impedances. Also shown in Figure 4b is a power supply connected to the AD689 and to a block representing additional analog circuits. The total current that flows through Z_{G1} could be much greater than 1mA current from the GND SENSE pin, developing a potentially large voltage drop across Z_{G1}. If GND and GND SENSE are connected at the AD689, the AD689 would sense V_{ZG1} and deliver 8.192V + V_{ZG1} across R_L. To minimize the voltage error at the load, GND SENSE is connected instead at load ground. The voltage error now delivered at the load is reduced to V_{ZW}, where $V_{ZW} < V_{ZG1}$. For example, if Z_{G1} = Z_W and the total ground current flowing through Z_{G1} is 20mA, then V_{ZG1} = 20 (V_{ZW}) and the potential error at the load is reduced by a factor of 20.

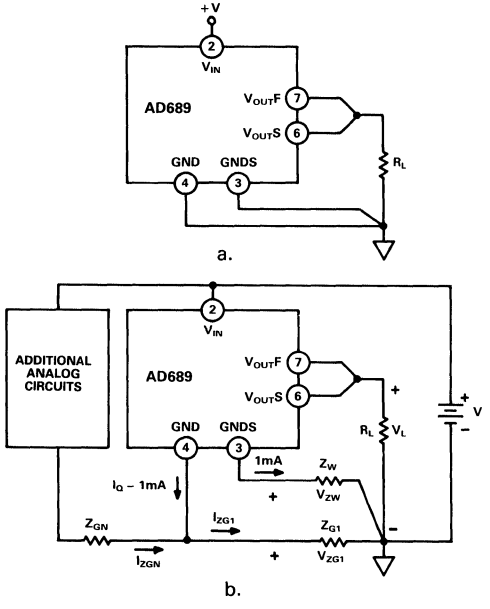


Figure 4. Grounding the AD689

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD689 is typically less than 2μV p-p over the 0.1Hz to 10Hz band. Noise in a 1MHz bandwidth is approximately 200μV p-p. The dominant source of this noise is the buried Zener which contributes approximately 100nV/$\sqrt{\text{Hz}}$. In comparison, the op amp's contribution is negligible. Figure 5 shows the 0.1Hz to 10Hz noise of a typical AD689. The noise measurement is made with a bandpass filter made of a 1-pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.922Hz bandwidth.

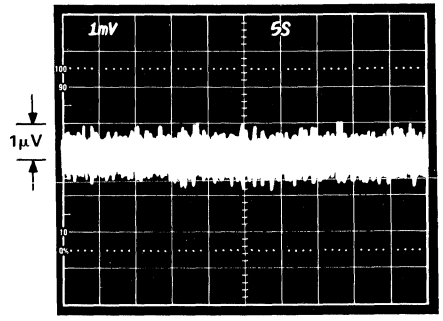


Figure 5. 0.1Hz to 10Hz Noise

If further noise reduction is desired, an external capacitor may be added between the NOISE REDUCTION pin and the GND pin as shown in Figure 2. This capacitor, combined with the 4kΩ R_S and the Zener resistances forms a low-pass filter on the output of the Zener cell. The addition of a 1μF capacitor forms a filter with a 3dB point at 12Hz, and it will reduce the high-frequency (to 1MHz) noise to about 200μV p-p. Figure 6 shows the 1MHz noise of a typical AD689 both with and without a 1μF capacitor.

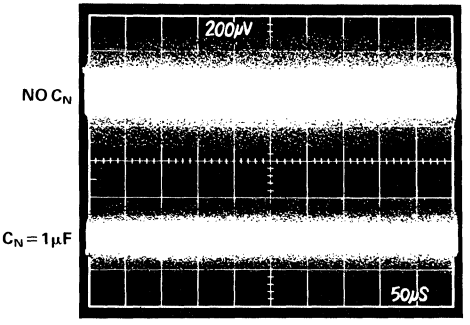


Figure 6. Effect of 1μF Noise Reduction Capacitor on Broadband Noise

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components normally associated with this are: the time for the active circuits to settle, and the time for the thermal gradients on the chip to

stabilize. Figure 7 shows the turn-on characteristics of the AD689. It shows the settling to be about 20μs to 0.01%. Note the absence of any thermal tails when the horizontal scale is expanded to 1ms/cm in Figure 7b.

Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor acts as an additional load to the internal Zener diode's current source resulting in a somewhat longer turn-on time. In the case of a 1μF capacitor, the initial turn-on time is approximately 100ms to 0.01%, as shown in Figure 7c.

DYNAMIC PERFORMANCE

The output amplifier is designed to provided the AD689 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 8 displays the characteristics of the AD689 output amplifier driving a 0 to +8.192mA load.

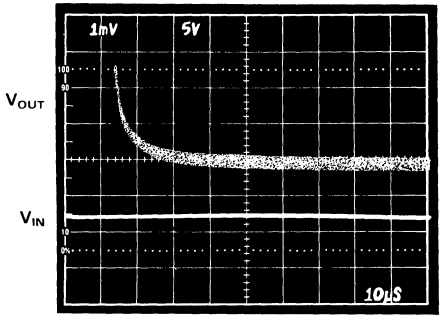


Figure 7a. Electrical Turn-On

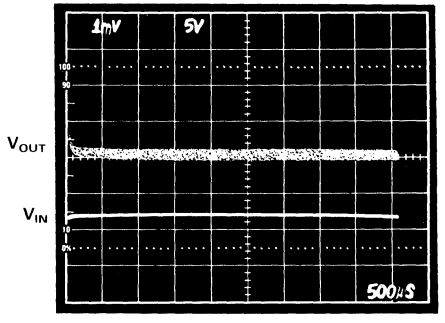


Figure 7b. Extended Time Scale

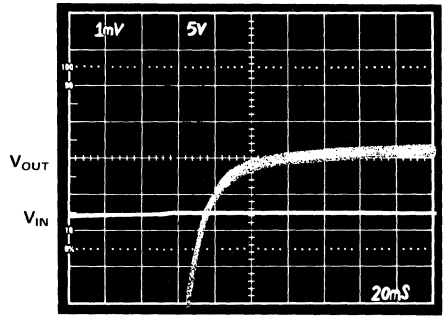


Figure 7c. Turn-On with 1μF C_N

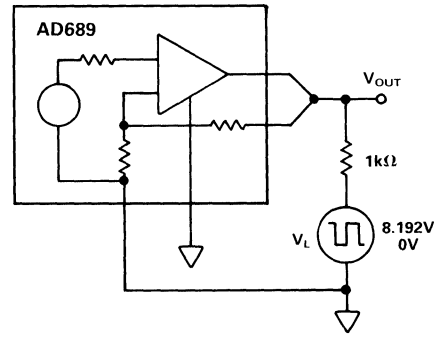


Figure 8a. Transient Load Test Circuit

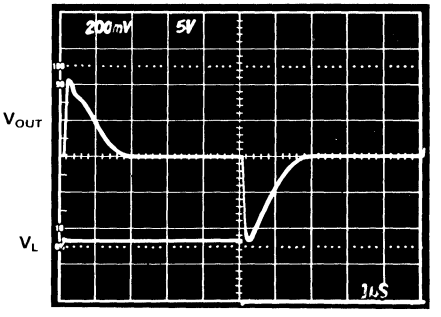


Figure 8b. Large-Scale Transient Response

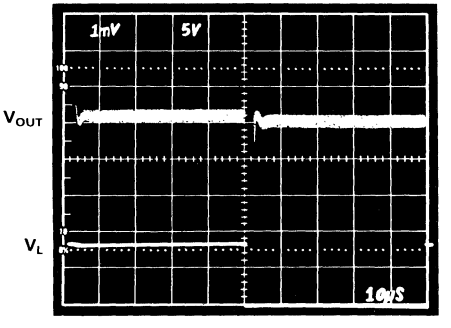


Figure 8c. Fine-Scale Settling for Transient Load

In some applications, a varying load may be both resistive and capacitive in nature, or the load may be connected to the AD689 by a long capacitive cable.

Figure 9 displays the output amplifier characteristics driving a 1000pF, 0 to +8.192mA load.

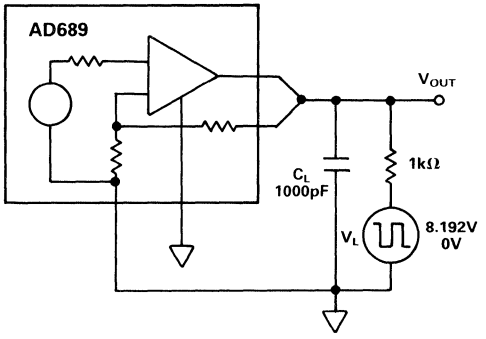


Figure 9a. Capacitive Load Transient Response Test Circuit

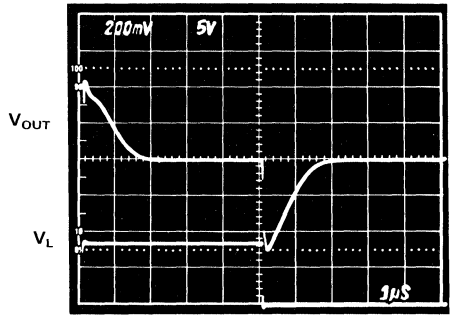


Figure 9b. Output Response with Capacitive Load

TRANSIENT SUPPRESSION IN NOISY ENVIRONMENTS

A precision reference must also exhibit excellent line regulation in noisy environments such as in switching power supply designs, and during electromechanical switching and inductive/capacitive load switching. These environments cause transients on the power supplies which must be internally rejected by the reference or bypassed with the use of external capacitors. Figure 10 shows PSRR versus frequency for the AD689. The voltage applied to V_{IN} is +12V dc plus a 2V p-p sine wave which is varied from 10Hz to 1MHz.

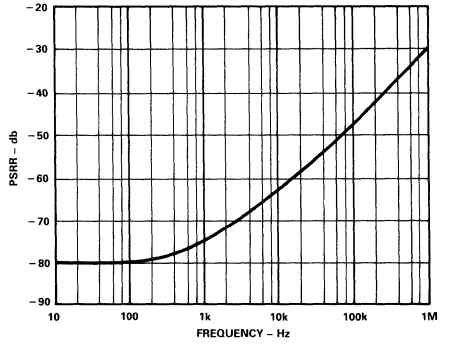


Figure 10. PSRR vs. Frequency

LOAD REGULATION

The AD689 has excellent load regulation characteristics. Figure 11 shows that varying the load a few mA changes the output by several μV. The AD689 exhibits linear load regulation both sourcing and sinking current. Separating the output amplifier ground from the buried Zener ground provides the excellent negative load regulation characteristic.

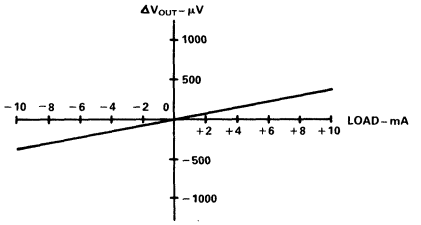


Figure 11. Typical Load Regulation Characteristics

TEMPERATURE PERFORMANCE

The AD689 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using maximum deviation per degree centigrade; i.e., ppm/°C. However, because of nonlinearities in temperature characteristics which originated in standard Zener references (such as "S" type characteristics), most manufacturers now use a maximum limit error band approach to specify devices. This technique involves the measuring of the output at three or more different temperatures to specify an output voltage error band.

Figure 12 shows the typical output voltage drift for the AD689L and illustrates the test methodology. The box in Figure 12 is bounded on the top and bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left to the upper right corner of the box determines the performance grade of the device.

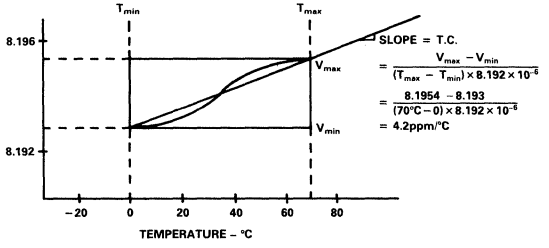


Figure 12. Typical AD689L Temperature Drift

Each AD689J, K, L grade unit is tested at 0, +25°C and +70°C. Each AD689S and T grade unit is tested at −55°C, +25°C and +125°C. This approach ensures that the variations in output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. The maximum height of the box for the appropriate temperature range and device grade is shown in Table I. Duplication of these results requires a combination of high accuracy and stable temperature control in

a test system. Evaluation of the AD689 will produce a curve similar to that in Figure 12, but output readings may vary depending on the test methods and equipment utilized.

Device Grade	Maximum Output Change – mV	
	0 to +70°C	−55°C to +125°C
AD689J	9.22	
AD689K	5.53	
AD689L	1.84	
AD689S		16.38
AD689T		8.19

Table I. Maximum Output Change in mV

USING THE AD689 FOR 12V, 12-BIT CONVERTERS

The AD689 is an ideal reference for use with data converters which require superior load regulation characteristics. The combination of excellent electrical specifications along with flexible force and sense connections allow the AD689 to be used in numerous applications. Several representative examples follow.

MONOLITHIC QUAD 12-BIT DAC – AD664

Four voltage output DACs in a monolithic package with flexible digital interface capabilites and 12-bit accuracies are just a few of the key features of the AD664. The AD689 can be utilized as the voltage reference input as shown in Figure 13 to provide convenient 2mV/LSB scaling. The AD689 is sensed at the AD664 to eliminate any voltage drops that might occur due to current flowing from the AD689 through wire resistances. In precision data conversion applications a voltage reference must maintain its output level during load variations. The AD689 maintains its 8.192V output with a maximum load regulation of 100μV/mA. The change of input resistance at the reference input of the AD664 is specified at 1.4kΩ. A load variation of 1.4kΩ at an input of 8.192V would result in a maximum of 0.3mV output change from the AD689; for the 12-bit AD664 this represents 0.15LSBs.

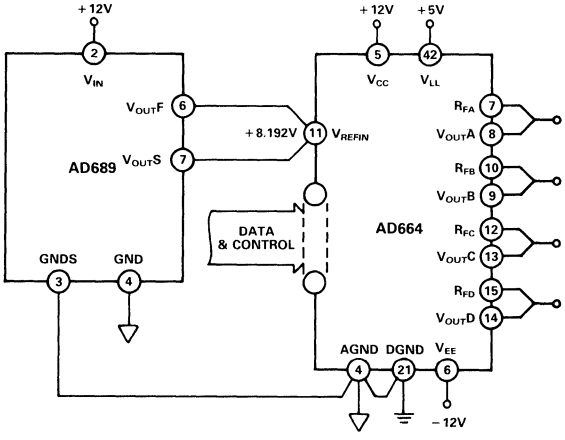


Figure 13. Quad 12-Bit DAC Application

±12V POWER SUPPLIES LIMIT REFERENCE SELECTION

In many systems with ±12V supplies, 5V references have to be substituted for 10V references due to headroom requirements from the supply input to the reference output. The AD689 is specified to operate with 12V ±10% supplies, increasing the voltage signal range by greater than 50% over systems using 5V references.

12-BIT DIGITAL-TO-ANALOG CONVERTER – AD767

The AD767 is specified to operate on supplies ranging from ±15V ±10% to ±12V ±5%. However, if ±12V ±10% supplies are used, then the supply voltage could drop to 10.8V. Because the internal 10V reference will not function properly at +10.8V, an external reference must be used. Figure 14 shows the AD689 connected through a trim resistor to REF IN (Pin 7) on the AD767. Additional trim range must be provided since the internal reference of the AD767 has a 1% tolerance (±100mV) and full-scale and bipolar offset are both trimmed with the internal reference. The connection of internal scaling resistors allows the AD767 to be configured in many voltage output ranges as shown in Table II. Tables III and IV show output voltage levels when the AD767 is configured in straight binary and offset binary modes.

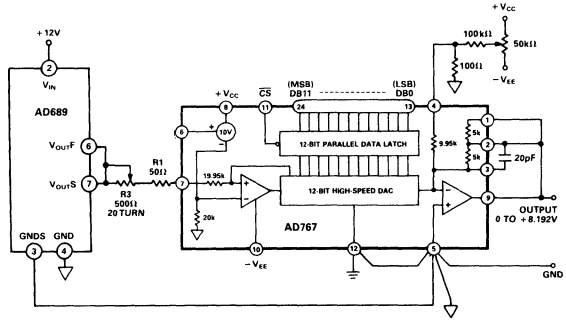


Figure 14. The AD689 as a Reference for the AD767

Output Range	Digital Input	LSB
±8.192V	Offset Binary	4mV
±4.096V	Offset Binary	2mV
±2.048V	Offset Binary	1mV
0 to +8.192V	Straight Binary	2mV
0 to +4.096V	Straight Binary	1mV

Table II. AD767 Output Voltage Ranges with AD689 Voltage Reference

Digital Input (Hex)	Analog Output
FFF	8.192V(4095/4096) = 8.190V
.	
.	
003	8.192V(0003/4096) = 0.006V
002	8.192V(0002/4096) = 0.004V
001	8.192V(0001/4096) = 0.002V
000	8.192V(0000/4096) = 0

Note: 1LSB = $8.192V/2^{12}$ = 2mV

Table III. Straight Binary Codes

Digital Input (Hex)	Analog Output
FFF	8.192V(2047/2048) = +8.188V
.	
801	8.192V(0001/2048) = +0.004V
800	8.192V(0000/2048) = 0
7FF	8.192V(0001/2048) = −0.004V
.	
001	8.192V(2047/2048) = −8.188V
000	8.192V(2048/2048) = −8.192V

Note: 1LSB = $8.192V/2^{11}$ = 4mV

Table IV. Bipolar (Offset Binary) Codes

12-BIT ANALOG-TO-DIGITAL CONVERTER – AD574A

The AD574A is a complete 12-bit A/D converter with reference and clock. It is specified to operate on ±15V ±10% supplies or ±12V ±5% supplies. The internal +10V reference does not function properly with the use of ±12V ±10% supplies; the AD689 is then the ideal choice for an external reference. The AD689 also provides excellent temperature coefficent characteristics, reducing the gain T. C. by as much as 75% (depending on grade) over use of the internal reference. Figure 15 shows the AD689 connected in the optional trim configuration mode. The additional trim range is required since the internal reference of the AD574A has a ±20mV tolerance, and full scale and offsets are both trimmed with the internal reference. The force and sense outputs are connected as closely as possible to the AD574A, and the ground sense pin is connected at the ANALOG COMMON pin (Pin 9) of the AD574A. This ensures that the AD689 will accurately deliver the 8.192V at the reference input.

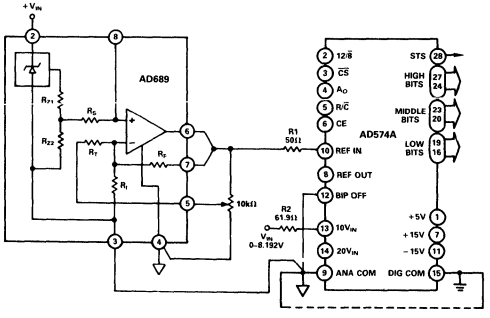


Figure 15. AD689/AD574A Connections

NEGATIVE REFERENCE VOLTAGE FROM AN AD689

The AD689 can be used to provide a precision −8.192V output as shown in Figure 16. The V_{IN} pin is tied to at least a +3V supply; the output pins are grounded; and the AD689 ground pins are connected through a resistor to a −12V supply. The equation provided in Figure 16 calculates the value of the resistor (R_S) such that when no load is connected the AD689 will sink the maximum current (8.192mA) plus the maximum quiescent current (5mA). When the load is connected, the AD689 will respond by reducing the current it sinks by the equivalent of the load current. The −8.192V output is produced at the ground pins (Pins 3 and 4) instead of the V_{OUT} pins. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard +8.192V configuration.

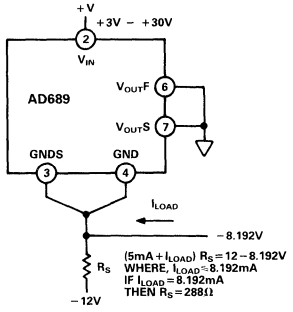


Figure 16. AD689 as a Negative 8.192V Reference

PRECISION CURRENT SOURCE

The design of the AD689 allows it to be easily configured as a precision current source. By choosing the control resistor R_C in Figure 17, you can vary the load current (I_L) from the quiescent current (2mA typically) to approximately 10mA. The compliance voltage (V_L) of this circuit varies depending upon the value of $+V_{IN}$ as shown in Figure 17.

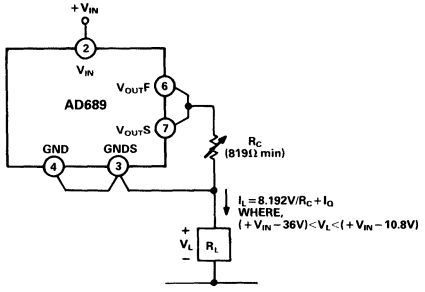


Figure 17. Precision Current Source

PRECISION HIGH CURRENT SUPPLY

For higher currents, the AD689 can easily be connected to a power NPN or power Darlington NPN device. The circuit in Figure 18 can deliver up to 4 amps to the load. Due to potential headroom limitations on the V_{OUT} FORCE (Pin 6) when the power supply drops to a minimum of 10.8V, a resistor (R) from the power supply to V_{OUT} FORCE (Pin 6) is added to provide the maximum base current required by the 2N6282. The AD689 will, therefore, only be required to sink current. This arrangement guarantees sufficient base drive for the Darlington if the power supply drops to 10.8V. The formula provided calculates the value of R based on the minimum power supply voltage expected, V_{BE} and I_B maximum.

$$R = \frac{V_{IN}\,(\min) - (8.192V + V_{BE} + I_B\,[\max] \times 20\Omega)}{I_B\,(\max)}$$

Where,

V_{IN} (min) ≥ 10.8V

I_B (max) ≤ 8.192mA

For example,

When, V_{IN} = 10.8V, I_C = 4A, I_B = 2mA (max),

V_{BE} = 1.2V

Then R = 684Ω

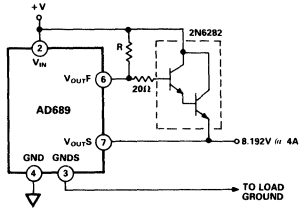


Figure 18a. Precision High-Current Voltage Source

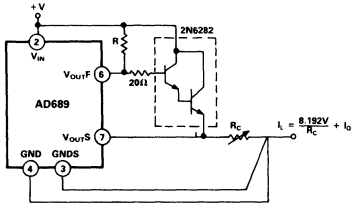


Figure 18b. Precision High-Current Current Source

ANALOG DEVICES

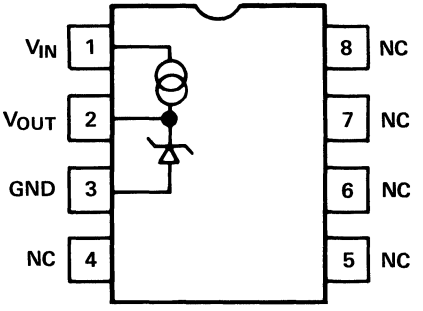
Low Cost, Precision 2.5V IC References

AD1403/AD1403A*

FEATURES

Improved, Lower Cost, Replacements for Standard 1403, 1403A
3-Terminal Device: Voltage In/Voltage Out
Laser Trimmed to High Accuracy: 2.500V ±10mV (AD1403A)
Excellent Temperature Stability: 25ppm/°C (AD1403A)
Low Quiescent Current: 1.5mA max
10mA Current Output Capability
Low Cost
Convenient Mini-DIP Package

AD1403/AD1403A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1403 and AD1403A are improved three-terminal, low cost, temperature compensated, bandgap voltage references that provide a fixed 2.5V output voltage for inputs between 4.5V and 40V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provides the AD1403/AD1403A with an initial tolerance of ±10mV and a temperature stability of better than 25ppm/°C. In addition, the low quiescent current drain of 1.5mA (max) offers a clear advantage over classical zener techniques.

The AD1403 or AD1403A is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD1403/AD1403A allows operation with 5 volt logic supplies, making these devices ideal for digital panel meter applications and when only a single logic supply is available.

The AD1403 and AD1403A are specified for operation over the 0 to +70°C temperature range. The AD580 series of 2.5 volt precision IC references is recommended for applications where operation over the −55°C to +125°C range is required.

*Covered by Patent Numbers: 3,887,863; RE30,586.

PRODUCT HIGHLIGHTS

1. The AD1403A offers improved initial tolerance over the industry-standard 1403A: ±10mV versus ±25mV at a lower cost.
2. The three-terminal voltage in/voltage out operation of the AD1403/AD1403A provides a regulated output voltage without any external components.
3. The AD1403/AD1403A provides a stable 2.5V output voltage for input voltages between 4.5V and 40V making these devices ideal for systems that contain a single logic supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD1403A with temperature stabilities of 25ppm/°C.
5. The low 1.5mA maximum quiescent current drain of the AD1403 and AD1403A makes them ideal for CMOS and other low power applications.

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SPECIFICATIONS (V_{IN} = 15V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0mA)	V_O				
AD1403		2.475	2.500	2.525	V
AD1403A		2.490	2.500	2.510	
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
AD1403		–	10	40	
AD1403A		–	10	25	
Output Voltage Change, 0 to +70°C	ΔV_O				mV
AD1403		–	–	7.0	
AD1403A		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15V≤V_{IN}≤40V)		–	1.2	4.5	
(4.5≤V_{IN}≤15V)		–	0.6	3.0	
Load Regulation (0mA<I_O<10mA)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0mA)	I_I	–	1.2	1.5	mA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	40	V
Storage Temperature	T_{STG}	-25 to 100	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

Specifications subject to change without notice.

ORDERING INFORMATION

Device	Initial Tolerance	Package Option[1]
AD1403	±25mV	N-8
AD1403A	±10mV	N-8

NOTE
[1] See Section 14 for package outline information.

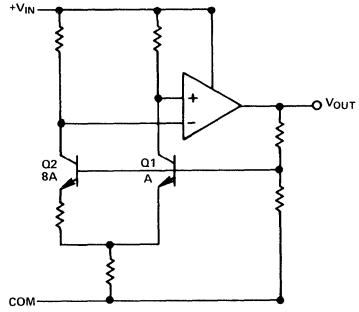


Figure 1. Simplified AD1403 Schematic

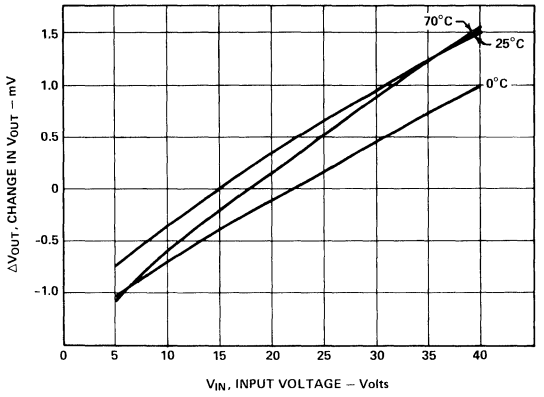


Figure 2. Typical Change in V_{OUT} vs. V_{IN} (Normalized to V_{OUT} @ V_{IN} = 15V @ T_C = 25°C)

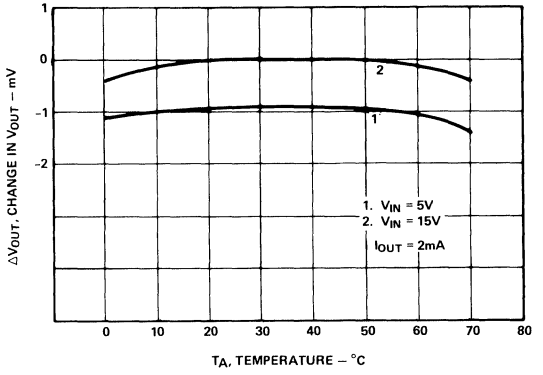


Figure 5. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V)

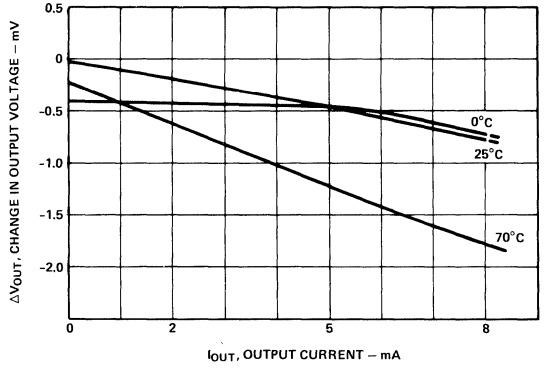


Figure 3. Change in Output Voltage vs. Load Current (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

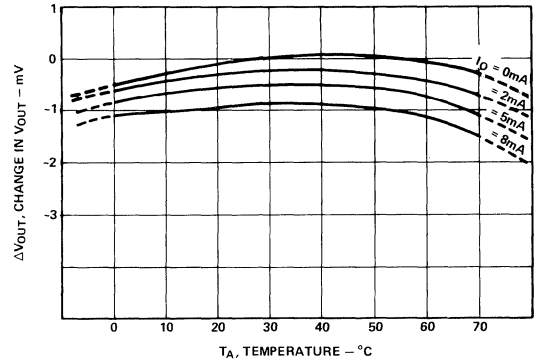


Figure 6. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

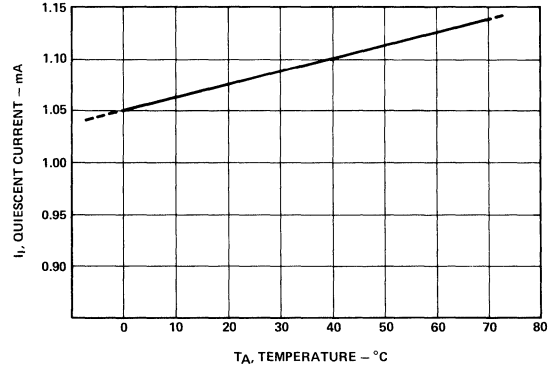


Figure 4. Quiescent Current vs. Temperature (V_{IN} = 15V, I_{OUT} = 0mA)

8

Applying the AD1403/AD1403A

VOLTAGE VARIATION VS. TEMPERATURE AND LINE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD1403 is shown in Figure 6. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

The AD1403 exhibits a worst-case shift of 7.5mV over the entire range of operating input voltage, 4.5 volts to 40 volts. Typically, the shift is less than 1mV as shown in Figure 3.

THE AD1403A AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD1403A has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1.5mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

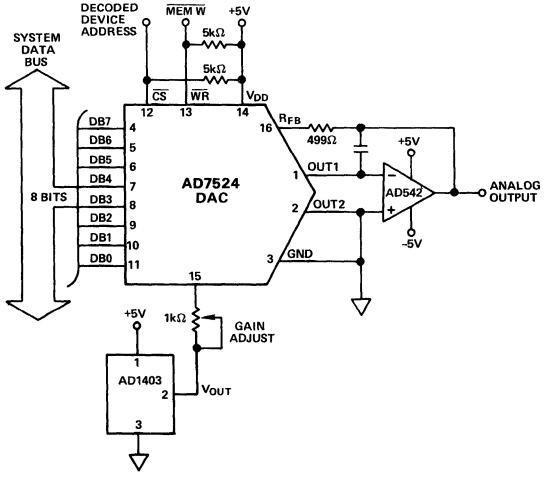


Figure 7. Low Power, Low Voltage Reference for the AD7524 Microprocessor-Compatible 8-Bit DAC

Figure 9 shows the AD1403A used as a reference for the AD7524 low-cost 8-bit CMOS DAC with complete microprocessor interface. The AD1403A and the AD7524 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7524 includes an 8-bit data register, and address decoding logic; it may thus be interfaced directly to an 8- or 16-bit data bus. Only 300μA of quiescent current from the single +5 volt supply is required to operate the AD7524 which is packaged in a small 16 pin DIP. The AD542 output amplifier is also low power, requiring only 1.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7524KN without user trims and it typically settles to ±1/2LSB in less than 5 microseconds. It will provide the 0 volt to -2.5 volt output swing from ±5 volt supplies.

THE AD1403 AS A PRECISION PROGRAMMABLE CURRENT SOURCE

The AD1403 is an excellent building block for precision current sources. Its wide range of operating voltages, 4.5V to 40V, along with excellent line regulation over that range (7.5mV) result in high insensitivity to varying load impedances. The low quiescent current (I_I) of 1.5mA (max) and the maximum specified maximum load current of 10mA allows the user to program current to any value between 1.5mA and 10mA.

Figure 10a shows the AD1403 connected as a current source. Total current is equal to the quiescent current plus the load current. Most of the temperature coefficient comes from the quiescent current term I_I, which has a typical TC of 0.13%/°C (1300ppm/°C). The load voltage (and hence current) TC is much lower at ±40ppm/°C max (AD1403). Therefore, the overall temperature coefficient decreases rapidly as the load current is increased. Figure 10b shows the typical temperature coefficient for currents between 1.5mA and 10mA. Use of an AD1403A will not improve the TC appreciably.

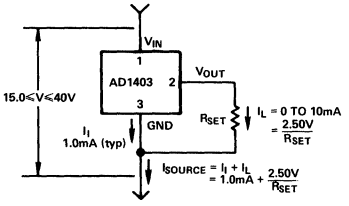


Figure 8a. The AD1403 as a Precision Programmable Current Source

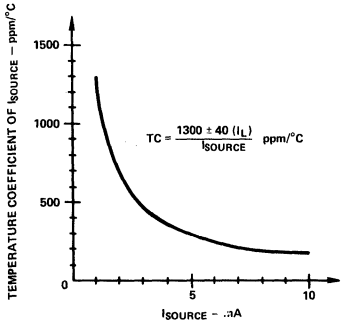


Figure 8b. Typical Temperature Coefficient of Current Source

ANALOG DEVICES

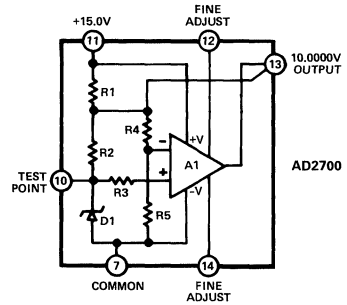
±10 Volt Precision Reference Series

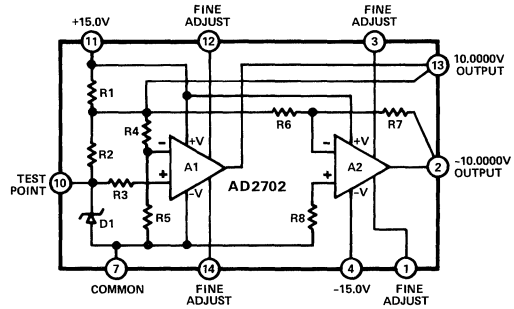
AD2700/AD2701/AD2702

FEATURES

Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed -55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected
Available as /883B

AD2700 SERIES FUNCTIONAL BLOCK DIAGRAMS





PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package. Both are often used with 52XX Series 12-bit A/D converters which require -10V external references for high accuracy over wide temperature ranges.

All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range. Screening to MIL-STD-883 is available for "S" and "U" grades of the AD2700 family.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature performance results in very high accuracy over the temperature range without external components. The AD2700/01/02 LD grades have a maximum output voltage error at 25°C of ±2.5mV with no external adjustments.
2. The performance of the AD2700 series is achieved by a well-characterized design and precise control over the manufacturing process.
3. The AD2700 series is well suited for a broad range of applications requiring an accurate, stable reference source such as high resolution data converters (12 or 14 bits), test and measurement systems and calibration standards.

Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

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SPECIFICATIONS (max or min @ E_{IN} ±15V @ +25°C, R_L = 2kΩ unless otherwise noted)

MODEL	JD	LD	SD	UD
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissipation @ +25°C – AD2700, 01	300mW	*	*	*
– AD2702	450mW	*	*	*
Operating Temperature Range	-25°C to +85°C	*	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE ERROR @ +25°C				
AD2700 10.000V	±0.005V	±0.0025V	*	**
AD2701 -10.000V	±0.005V	±0.0025V	*	**
AD2702 ±10.000V	±0.005V	±0.0025V	*	**
OUTPUT CURRENT[1] – @ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. temp. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE ERROR – AD2700,01	10ppm/°C	3ppm/°C	**	**
(T_{min} to T_{max})[2]	±11.0mV	±4.3mV	±8mV	±5.5mV
AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300μV/V	*	*	*
LOAD REGULATION				
0 to ±10mA	50μV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT – AD2700, 01	±14mA	*	*	*
– AD2702	+17mA, -4mA	*	*	*
NOISE				
(0.1 to 10Hz)	50μV p-p typ	*	*	*
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. (typ)	*	*	*
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4μV/°C per mV of Adjust (typ)	*	*	*
PACKAGE OPTION[3,4]	DH-14C	DH-14C	DH-14C	DH-14C

NOTES
*Same as "JD" grade performance.
**Same as "LD" grade performance.
***Same as "SD" grade performance.

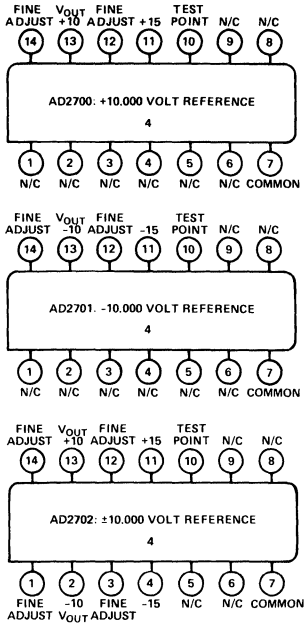
[1] Specified with resistive load to common. Device not intended for use in driving a dynamic load.

[2] Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C. The box limits are noted below the drift values used to calculate the box.

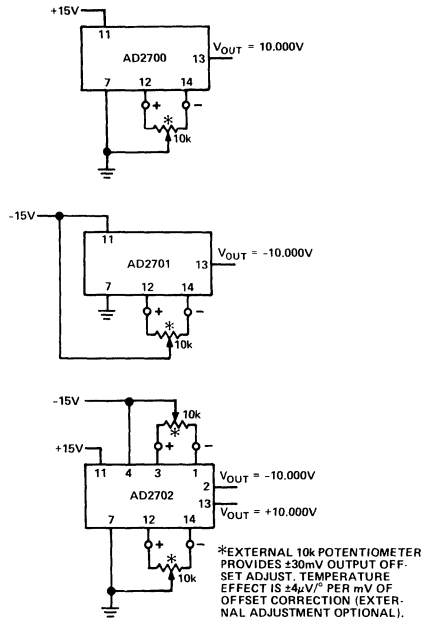
[3] Analog Devices reserves the right to ship metal packages (outline DH-14B) in lieu of the standard ceramic packages for J and L grade parts.

[4] See Section 14 for package outline information.

Specifications subject to change without notice.

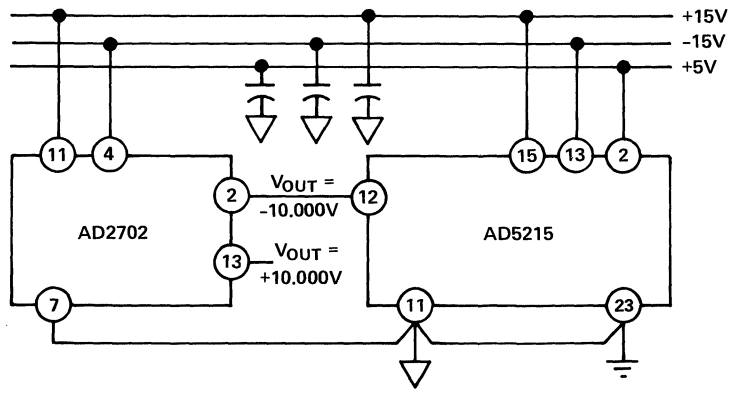


Pin Designations



Fine Trim Connections

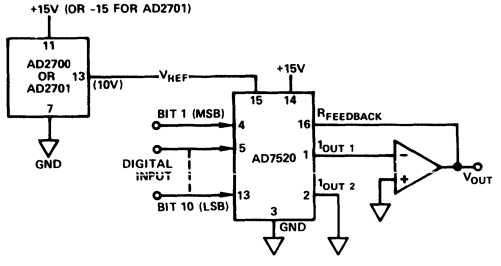
8



Using AD2702 Reference with the Fast, High Accuracy AD5215 – 12-Bit ADC

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to -10 volt output range. Alternatively, using the -10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of -10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 Data Sheet.

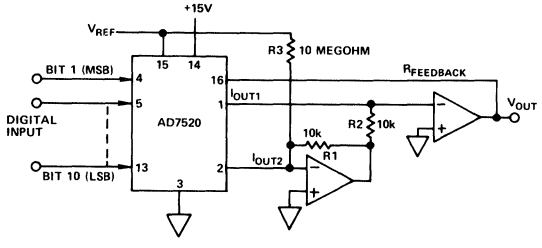


Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table I. Code Table — Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

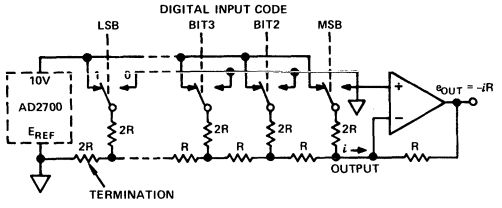
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

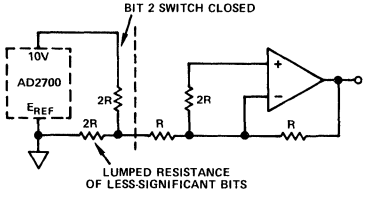
Table II. Code Table — Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

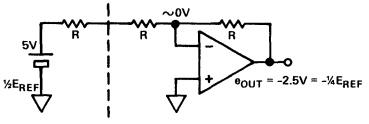
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = \frac{1}{4}E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence — because the amplifier summing point is at virtual ground — the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to 2^{-n} E_{REF}.



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b.)

ANALOG DEVICES

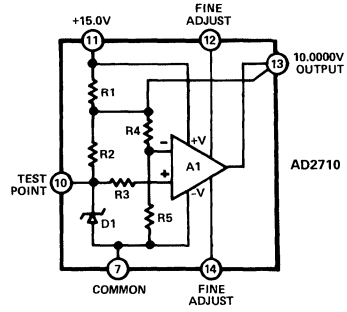
±10.000 Volt Ultrahigh Precision Reference Series

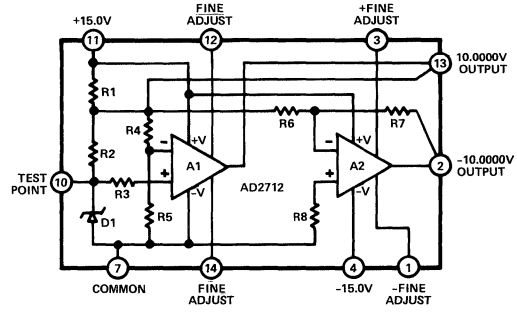
AD2710/AD2712

FEATURES

Laser Trimmed to High Accuracy: 10.000V ± 1.0mV
Low Temperature Coefficient: 1ppm/°C (L Grade)
Excellent Long Term Stability: 25ppm/1000hrs.
5mA Output Current Capability
Low Noise: 30μV p-p
Short Circuit Protected
No Heater Utilized
Small Size (Standard 14-Pin DIP Package)

AD2710/AD2712 FUNCTIONAL BLOCK DIAGRAMS





PRODUCT DESCRIPTION

The AD2710 and AD2712 are temperature-compensated, hybrid voltage references which provide precise 10.000V output from an unregulated input level from 13.5 to 16.5 volts. Active laser trimming is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in ultra high precision performance previously available only in oven-regulated modules. The 1.0mV maximum initial error and 1ppm/°C guaranteed maximum temperature coefficient of the AD2710L and AD2712L represent the best performance combination available without using ovens or heated substrates for temperature regulation.

The AD2710 series of precision 10.000 volt references offer the user unequalled accuracy and stability with performance guaranteed over the 0 to +70°C temperature range. The devices combine the recognized advantages of thin film technology and active laser trimming with a unique integrated ceramic package design to provide an excellent reference for use in applications requiring high accuracy and stability.

The AD2710 is recommended for use as a reference for 10-, 12- and 14-bit D/A converters which require an external reference. The device is also suitable for many types of high resolution A/D converters, either successive approximation or integrating designs. The 5mA output drive capability of the device also makes the AD2710 ideal for use as a master system reference.

For systems requiring a dual tracking reference, the AD2712 offers both positive and negative outputs in a single package. All units are packaged in an integrated ceramic 14-pin side-brazed package offering superior reliability over other package designs.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature coefficient results in very high accuracy over the temperature range without the use of external components. AD2710 has a maximum deviation from 10.000 volts of ±1.00mV at 25°C with no external adjustments.
2. The AD2710 and AD2712 are well suited for a broad range of applications requiring an accurate, stable reference source such as data converters, test and measurement systems and calibration standards.
3. The performance of the AD2710 series is achieved by a well-characterized design and close control over the manufacturing process. This eliminates the need for temperature-controlled ovens to provide stability.
4. The advanced multilayer integrated ceramic package results in superior electrical performance as well as inherent high reliability.

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SPECIFICATIONS (typical @ V_S ±15V after a 5 minute warm-up at +25°C, no load condition unless otherwise specified)

Model		AD2710KN	AD2710LN	AD2712KN	AD2712LN
ABSOLUTE MAXIMUM RATINGS					
Input Voltage (for applicable supply)		±18V	*	*	*
Power Dissipation @ +25°C		300mW	*	450mW	**
Operating Temperature Range		0 to +70°C	*	*	*
Storage Temperature Range		−55°C to +100°C	*	*	*
Lead Temperature (soldering, 20s)		+260°C	*	*	*
Short Circuit Protection (to GND)		Continuous	*	*	*
OUTPUT VOLTAGE ERROR[1]					
+25°C		±1.0mV max	*	*	*
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT[2]					
+10V Output	+25°C to +70°C	±2ppm/°C max	±1ppm/°C max	±2ppm/°C max	±1ppm/°C max
	0 to +25°C	±5ppm/°C max	*[3]	*	*[3]
−10V Output[4]	+25°C to +70°C	Not Applicable	Not Applicable	±3ppm/°C max	±2ppm/°C max
	0 to +25°C	Not Applicable	Not Applicable	±5ppm/°C max	**
LINE REGULATION					
V_S = ±13.5 to ±16.5[5]		125μV/V(200μV/V max)	*	*	*
OUTPUT CURRENT		10mA	*	*	*
LOAD REGULATION					
I_O = 0 to ±5mA		50μV/mA(100μV/mA max)	*	*	*
OUTPUT RESISTANCE		0.05Ω	*	*	*
INPUT VOLTAGE[5]					
Operating Range		±13V to ±18V	*	*	*
Specified Performance		±13.5V to ±16.5V	*	*	*
QUIESCENT SUPPLY CURRENT					
V_S+		9mA(14mA max)	*	12mA (16mA max)	**
V_S−[5]		Not Applicable	Not Applicable	2mA (4mA max)	**
NOISE					
0.1 to 10Hz		30μV p-p	*	*	*
LONG-TERM STABILITY					
T_A = +25°C		25ppm/1000 Hours	*	*	*
EXTERNAL TRIM RANGE[6]		±10mV	*	*	*
PACKAGE OPTION[7]		DH-14A	*	*	*

NOTES

*Same as AD2710KN. **Same as AD2712KN performance.

[1] Specifications apply to both outputs of the AD2712.

[2] Refer to next page for definition of temperature-related error specifications.

[3] The AD2710LN and AD2712LN outputs are guaranteed for a maximum ±2ppm/°C temperature coefficient over the +15°C to +25°C temperature range. Refer to Figure 1.

[4] The +10V and −10V outputs of the AD2712 typically track within ±1ppm/°C over the specified temperature range.

[5] Negative power supply not required for AD2710.

[6] Use of the output trim will change the temperature coefficient approximately 0.3ppm/°C for each millivolt of adjustment.

[7] See Section 14 for package outline information.

Specifications subject to change without notice.

UNDERSTANDING THE SPECIFICATIONS

The AD2710 and AD2712 precision references are designed for applications requiring both the lowest possible initial error at room temperature and the lowest possible temperature drift. The specification for initial error is relatively straight-forward, and is the absolute error from exactly 10.000V. The specification for temperature drift, however, must be explained.

Various methods have been used to specify the temperature drift of voltage references, including the "butterfly", "box", and "modified-box" (or total error) methods. The AD2710 and AD2712 are specified with the "butterfly" method.

Using three or more temperatures provides the user with a tighter drift specification, eliminating possible mid-range excursions. The AD2710 and AD2712 have been designed and characterized as having a smooth drift curve with a virtually straight segment from +25°C to +70°C. The typical curve as shown is concave downward and gradually increases slope near 0°C.

As can be seen from Figure 1, the AD2710L and AD2712L +10V outputs will exhibit a maximum temperature coefficient of ±1ppm/°C (±2ppm/°C for "K" grade) from +25°C to +70°C. Over the short range between +15°C and +25°C, the AD2710L and AD2712L +10V outputs have a maximum drift of only ±2ppm/°C and a maximum drift of ±5ppm/°C from 0 to +15°C. The negative output of the AD2712L has a similar temperature coefficient characteristic with a maximum slope of ±2ppm/°C from +25°C to +70°C. This limit continues from +25°C to +15°C and then increases to a ±5ppm/°C maximum slope from +15°C and 0°C. Every unit is 100 percent tested and guaranteed to meet these specifications over the full 0 to +70°C temperature range.

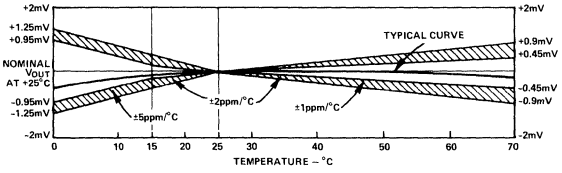


Figure 1. Maximum Change from +10V Output from +25°C Value vs. Temperature

All grades of the AD2710 and AD2712 are tested after a five minute warm-up period. This warm-up allows the entire circuit to attain thermal equilibrium. The warm-up drift is approximately 500 microvolts and is completely settled approximately three minutes after turn-on. Figure 2 shows the typical warm-up characteristics of the AD2710.

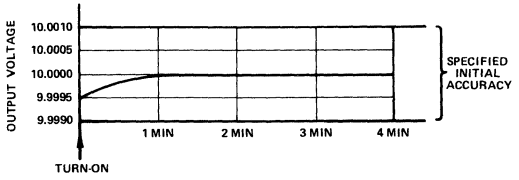


Figure 2. AD2710 Typical Warm-Up Drift

USING THE AD2710 AS A DAC REFERENCE

Digital-to-analog converters require a reference to establish the full scale output range. It is this reference which will ultimately determine the absolute accuracy of the converter. While many converters include internal reference sources, better overall performance can be obtained if a higher precision external reference is used.

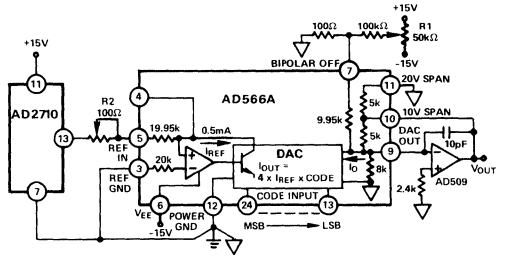


Figure 3. Low Drift 12-Bit D/A Converter

Figure 3 shows the AD2710 used with the AD566A high-speed 12-bit DAC. The AD566AKD is laser trimmed for ±1/4LSB maximum nonlinearity, and exhibits a gain temperature coefficient of 3ppm/°C. Use of the AD2710LN reference will result in a worst case total gain temperature coefficient of 4ppm/°C. After initial calibration of the DAC scale factor at room temperature, 12-bit absolute accuracy can be maintained over the +15°C to +70°C temperature range. The high output current capability of the AD2710 allows it to serve as a reference for up to 10 such converters in a system.

The resolution of the AD566A can be extended as shown in Figure 3 by summing the output of another DAC. In this example, an AD559 is used to provide 4 additional bits. Since the AD559 is driven from the same AD2710 reference as the AD566A which provides the higher-order bits, and uses a similar internal thin-film resistor ladder, it will exhibit first-order temperature tracking. While this circuit provides 16-bits of resolution, it is only as accurate as the AD566A used for the most significant bits. Use of an AD566AKD will typically achieve ±0.003% accuracy (±1/2LSB at 14 bits).

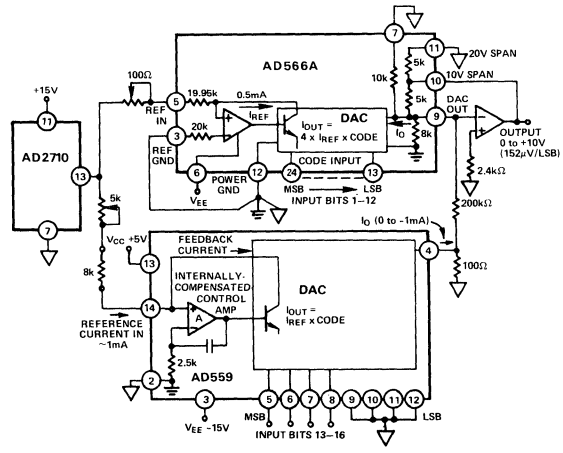


Figure 4. 16-Bit Binary DAC with AD2710 Reference

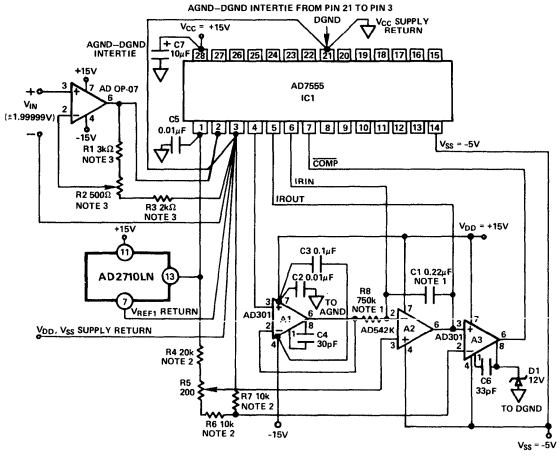
HIGH RESOLUTION ANALOG-TO-DIGITAL CONVERSION

The AD2710 is well-suited to both system and instrument-level analog-to-digital converter reference requirements. The excellent absolute accuracy and low temperature drift allow low-cost measurement systems to offer high levels of performance.

The AD7555 is a 4½/5½ digit ADC subsystem which uses the quad-slope conversion technique to achieve high accuracy at low cost. This patented conversion process performs automatic correction for offsets and other errors in the analog circuitry as a part of each conversion. Total scale factor drift 1.2ppm/°C is possible using the AD2710L reference and medium-precision external amplifiers. This represents a full scale drift of less than ±10 counts in ±200,000 from +15°C to +45°C. Less than 1 count of drift will occur in the 4 1/2 digit mode.

The AD7555 was designed for use with a 4.096V reference, which produces a ±2 volt input range. When the AD2710 is used, the input range is increased to ±4.88281V (24.4μV/count). The new scaling can be handled either by using a precision gain stage before the AD7555 analog input as shown or by using a microprocessor to digitally correct the scale. The actual input signal value can be computed by multiplying the count produced by the AD7555 by V_{REF1} (10 volts in this case), and dividing the result by 409600. Details of the digital circuitry of the AD7555 can be found on the AD7555 data sheet.

It should be noted that when the AD7555 is used with the AD2710 10 volt reference, it is necessary to use a V_{CC} greater than 10 volts. Thus the digital inputs and outputs of the ADC will be compatible with CMOS logic levels.



NOTES:
1. R8 C1 VALUES SHOWN ARE FOR 5 1/2 DIGIT MODE. FOR 4 1/2 DIGIT MODE R_8 = 360k, C_1 = 0.22μF. SUITABLE CAPACITORS AVAILABLE FROM COMPONENT RESEARCH CO. INC., 1655 26th STREET, SANTA MONICA, CA. 90404. (STOCK NUMBER FOR 0.22μF CAPACITOR IS D11B224KXW).
2. R4, R6, R7 1% TOLERANCE
3. R1, R3 SHOULD TRACK WITHIN 0.5ppm/°C. EITHER BULK METAL OR WIRE-WOUND RESISTORS (OR A THIN-FILM NETWORK) SHOULD BE USED. R2 SHOULD BE A LOW-TC TYPE POTENTIOMETER OR A SELECTED LOW DRIFT FIXED RESISTOR.

Figure 5. High Accuracy Low Drift A/D Converter

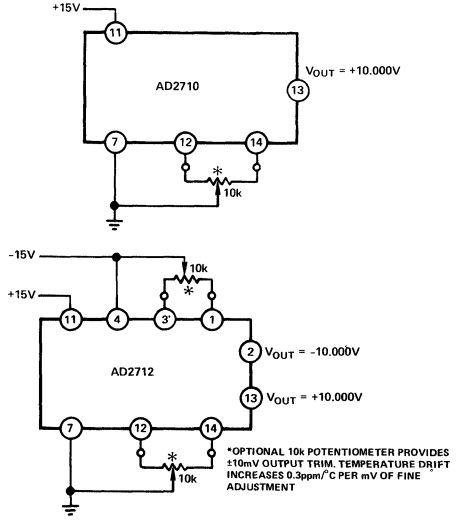


Figure 6. Optional Fine Trim Connections

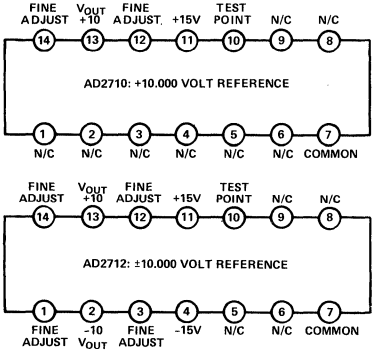


Figure 7. Pin Connections (Top View)

ANALOG DEVICES

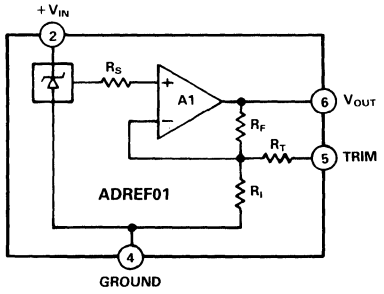
10V + 5V References

ADREF01/ADREF02

FEATURES

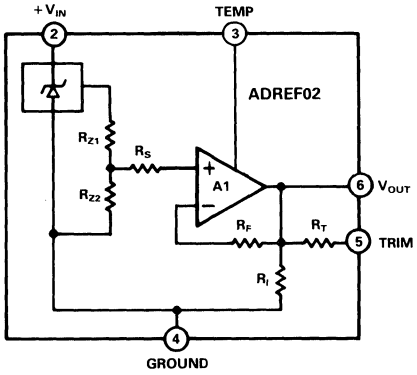
Replacement for Industry Standard REF01/REF02
Laser Trimmed to High Accuracy:
10.000V ±30mV (REF01)
5.000V ±15mV (REF02)
(A and E Grades)
Trimmed Temperature Coefficient: 8.5ppm/°C max
(A and E Grades)
Low Noise: 4μV p-p Typical
Output Trim Capability
Temperature Output Pin (REF02)
Machine Insertable Hermetic Cerdip Package

ADREF01 FUNCTIONAL BLOCK DIAGRAM



NOTE: MAKE NO CONNECTIONS TO PINS 1, 3, 7 AND 8.

ADREF02 FUNCTIONAL BLOCK DIAGRAM



NOTE: PINS 1, 7 & 8 ARE INTERNAL TEST POINTS. MAKE NO CONNECTIONS TO THESE POINTS.

PRODUCT DESCRIPTION

The ADREF01 and ADREF02 are a 10V and 5V reference, respectively, that utilize a buried Zener diode for minimal noise and drift over temperature. The Zener diode provides a precise 10.0V (5.0V for REF02) output from an unregulated input voltage of 13.5V (10.8V for REF02) to 36V. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient.

The +10V output can be adjusted over a +3%, −1% range with minimal effect on device characteristics. The +5V output can also be adjusted over a +6%, −2% range with minimal effect on device characteristics. The ADREF01 and ADREF02 offer good drift characteristics, low power consumption, and good accuracy for applications requiring a low-cost reference.

These devices are recommended as references for 8-, 10- and 12-bit D/A converters that require an external reference. They are also ideal for all types of A/D converters with up to 12-bit accuracy.

The ADREF01E/ADREF02E and ADREF01H/ADREF02H are specified for operation from 0 to +70°C, and the ADREF01/ADREF02 and ADREF01A/ADREF02A are specified for operation between −55°C and +125°C. All grades are packaged in a hermetic 8-pin cerdip package.

PRODUCT HIGHLIGHTS

1. The ADREF01 is a second source equivalent to the industry standard REF01.
2. The ADREF01 provides a stable 10.000V output for input voltages between 13.5V and 36V.
3. Laser Wafer Trimming reduces ADREF01 initial offset error to 30mV (A and E grades).
4. The ADREF02 is a second source equivalent to the industry standard REF02.
5. The ADREF02 provides a stable 5.000V output for input voltages between 10.8V and 36V.
6. Laser Wafer Trimming reduces ADREF02 initial offset error to 15mV (A and E grades).
7. Temperature out pin enables the ADREF02 to be configured as a temperature transducer.
8. The buried Zener diode reference on both devices reduces noise to 4μV p-p and improves temperature stability to 8.5ppm/°C max (A and E grades).
9. Cerdip packaging provides hermeticity and machine insertability at a low price for the devices.

8

SPECIFICATIONS (T_A = +25°C, V_{IN} = +15V unless otherwise specified)

Model	ADREF01H Min	ADREF01H Typ	ADREF01H Max	ADREF01E Min	ADREF01E Typ	ADREF01E Max	ADREF01 Min	ADREF01 Typ	ADREF01 Max	ADREF01A Min	ADREF01A Typ	ADREF01A Max	Units
Output Voltage	**9.950**		**10.050**	**9.970**		**10.030**	**9.950**		**10.050**	**9.970**		**10.030**	V
Output Voltage Drift													
0 to +70°C		10	25		3	8.5							± ppm/°C
−55°C to +125°C								10	25		3	8.5	
Gain Adjustment	−1			−1			−1			−1			%
	+3			+3			+3			+3			
Line Regulation (T_{min} to T_{max})													
13.5V ≤ +V_{IN} ≤ 36V			**100**			**100**			**100**			**100**	± µV/V
Load Regulation													
Sourcing 0 < I_{OUT} < 10mA													
T_{min} to T_{max}			**100**			**100**			**100**			**100**	± µV/mA
Sinking −10 < I_{OUT} < 0mA													
T_{min} to T_{max}			**100**			**100**			**100**			**100**	
Quiescent Current		2	**4**		2	**4**		2	**4**		2	**4**	mA
Power Dissipation		30			30			30			30		mW
Output Noise													
0.1Hz to 10Hz		4			4			4			4		µV p-p
Spectral Density, 100Hz		100			100			100			100		nV/√Hz
Long-Term Stability		15			15			15			15		ppm/1000Hr
Short-Circuit Current-to-Ground		30	**50**		30	**50**		30	**50**		30	**50**	mA
Short-Circuit Current-to-V_{IN}		30	50		30	50		30	50		30	50	mA
Turn-On Settling Time													
to 0.01% FS		60			60			60			60		µs
Temperature Range													
Specified Performance	0		+70	0		+70	−55		+125	−55		+125	°C

NOTE
Specifications subject to change without notice.

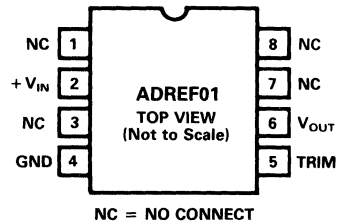
Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS* (ADREF01 and ADREF02)

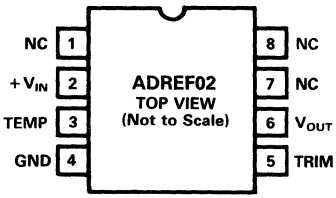
V_{IN} to Ground 36V
Power Dissipation (25°C) 500mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temp (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
θ_{JC} . . . . . 22°C/W
θ_{JA} . . . . . 110°C/W
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



NC = NO CONNECT



NC = NO CONNECT

SPECIFICATIONS (T_A = +25°C, V_{IN} = +15V unless otherwise specified)

Model	ADREF02H Min	ADREF02H Typ	ADREF02H Max	ADREF02E Min	ADREF02E Typ	ADREF02E Max	ADREF02 Min	ADREF02 Typ	ADREF02 Max	ADREF02A Min	ADREF02A Typ	ADREF02A Max	Units
Output Voltage	**4.975**		**5.025**	**4.985**		**5.015**	**4.975**		**5.025**	**4.985**		**5.015**	V
Output Voltage Drift													
0 to +70°C		10	**25**		3	**8.5**							ppm/°C
−55°C to +125°C								10	**25**		3	**8.5**	
Gain Adjustment	**−2**			**−2**			**−2**			**−2**			%
	+6			**+6**			**+6**			**+6**			%
Line Regulation (T_{min} to T_{max})													
10.8V < +V_{IN} <36V			**100**			**100**							±μV/V
11.4V < +V_{IN} <36V									**150**			**150**	
Load Regulation													
Sourcing 0 < I_{OUT} <10mA													
+25°C			**100**			**100**			**100**			**100**	μV/mA
T_{min} to T_{max}			**100**			**100**			**150**			**150**	
Sinking −10 < I_{OUT} <0mA													
+25°C			**400**			**400**			**400**			**400**	
Quiescent Current		2	**3**		2	**3**		2	**3**		2	**3**	mA
Power Dissipation		30			30			30			30		mW
Output Noise													
0.1Hz to 10Hz		4			4			4			4		μV p-p
Spectral Density, 100Hz		100			100			100			100		nV/√Hz
Long-Term Stability		15			15			15			15		ppm/1000Hr
Short-Circuit Current-to-Ground		30	**50**		30	**50**		30	**50**		30	**50**	mA
Turn-On Settling Time													
to 0.01% FS		60			60			60			60		μs
Temperature Voltage Output		630			630			630			630		mV
Temperature Voltage Output													
Temperature Coefficient		2.1			2.1			2.1			2.1		mV/°C
Temperature Range													
Specified Performance	0		+70	0		+70	−55		+125	−55		+125	°C

NOTE
Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

8

ORDERING GUIDE

Model	Initial Error mV	Temp. Coefficient ppm/°C	Temp. Range °C	Package Option*
ADREF01HQ/ADREF02HQ	50/25	25	0 to +70	Cerdip (Q-8)
ADREF01EQ/ADREF02EQ	30/15	8.5	0 to +70	Cerdip (Q-8)
ADREF01Q/ADREF02Q	50/25	25	−55 to +125	Cerdip (Q-8)
ADREF01AQ/ADREF02AQ	30/15	8.5	−55 to +125	Cerdip (Q-8)

*See Section 14 for package outline information.

THEORY OF OPERATION

The ADREF01 and ADREF02 consist of a proprietary buried Zener diode reference, an output buffer amplifier, and several high stability thin-film resistors. This design provides an accurate 10V reference with initial offset of 30mV or less, or an accurate 5V reference with initial offset of 15mV or less, and a temperature coefficient of 8.5ppm/°C (A and E grades).

LOAD REGULATION

The ADREF01 and ADREF02 have excellent load regulation characteristics. Figure 1 shows that varying the load several mA changes the output by only a few μV. The ADREF02 has somewhat better load regulation performance sourcing current than sinking current.

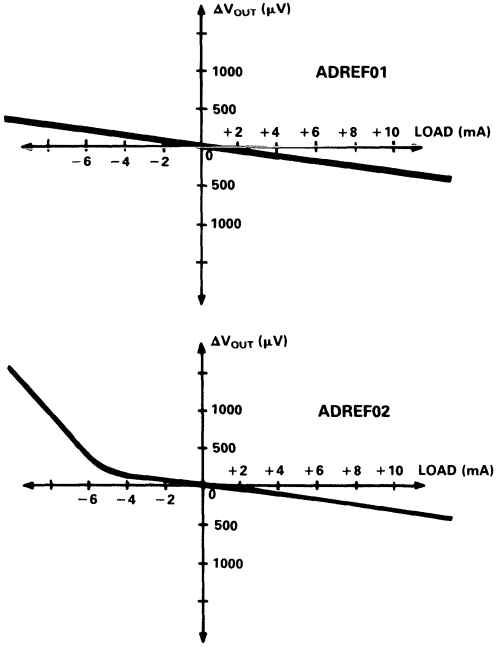


Figure 1. Typical Load Regulation Characteristics

TEMPERATURE PERFORMANCE

The ADREF01 and ADREF02 are designed for reference applications where good temperature performance is needed. Temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centrigrade; i.e., ppm/°C. However, because of nonlinearities in temperature characteristics which originated in standard Zener references (such as "S" type characteristics), most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves the measurement of the output at three or more different temperatures to specify an output voltage error band.

Figure 2 shows the typical output voltage drift for the ADREF01E and ADREF02E and illustrates the test methodology. The box in Figure 2 is bounded on the sides by the operating temperature extremes, and on the top and the bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left to the upper right corner of the box determines the performance grade of the device.

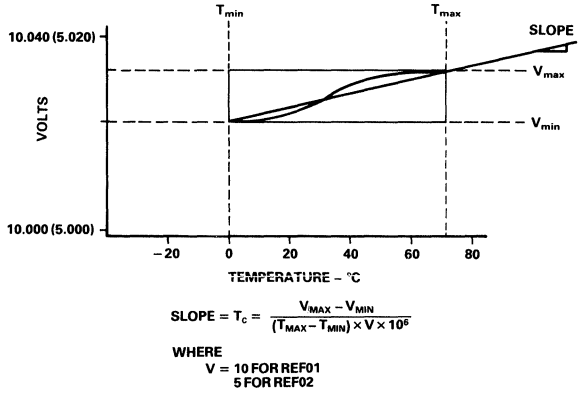


Figure 2. Typical ADREF01E/ADREF02E Temperature Drift

Each E and H grade unit is tested at 0, +25°C and +70°C. Each ADREF01/ADREF02 & A grade unit is tested at −55°C, +25°C and +125°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. The maximum height of the box for the appropriate temperature range and device grade is shown in Figure 3. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the ADREF01 or ADREF02 will produce a curve similar to that in Figure 3, but output readings may vary depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE (mV)	
	0 TO +70°C	−55°C TO +125°C
ADREF01H/02H	67.5/8.75	
ADREF01E/02E	36/2.98	
ADREF01/02		95/22.50
ADREF01A/02A		45.3/7.65

Figure 3. Maximum Output Change in mV

APPLYING THE ADREF01 AND ADREF02

The ADREF01 is simple to use in virtually all reference applications. When power is applied to Pin 2 and Pin 4 is grounded, Pin 6 provides a 10V output. No external components are required; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The ADREF01 requires less than 4mA quiescent current from an operating supply of +15V. The ADREF02 requires less than 3mA quiescent current from an operating supply of +12V or +15V.

An external fine trim may be desired to set the output level to exactly 10.000V or 5.000V when using ADREF02 (calibrated to a main system reference). System calibration may also require a reference voltage that is slightly different from 10.000V, for example, 10.24V for binary applications in the REF01 or 5.12V in the REF02. In either case, the optional trim circuit shown in Figure 4 can offset the output by as much as 300mV, if desired, with minimal effect on other device characteristics.

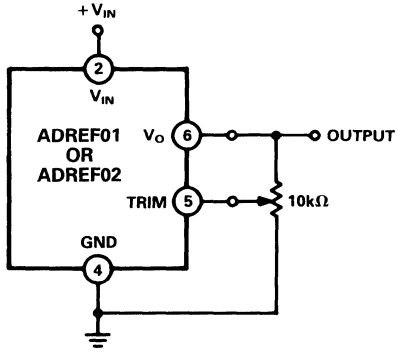


Figure 4. Optional Fine Trim Configuration

NEGATIVE REFERENCE VOLTAGE FROM AN ADREF01

The ADREF01 can be used to provide a −10.000V output as shown in Figure 5. The V_{IN} pin is tied to at least a +3.5V supply, the output pin is grounded, and the ADREF01 ground pin is connected through a resistor, R_S, to a −15V supply. The −10V output is now taken from the ground pin (Pin 4) instead of V_{OUT}. It is essential to arrange the output load and the supply resistor R_S so that the net current through the ADREF01 is between 2.5mA and 10mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard +10V output configuration.

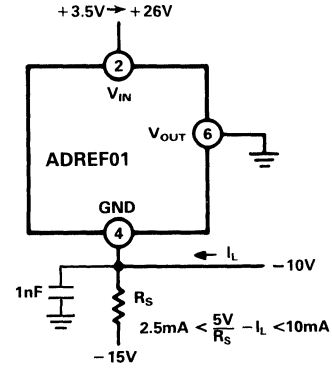


Figure 5. Negative 10V Reference

NEGATIVE REFERENCE VOLTAGE FROM AN ADREF02

The ADREF02 can be used to provide a −5.000V output as shown in Figure 6. The V_{IN} pin is tied to at least a +6V supply, the output pin is grounded, and the ADREF02 ground pin is connected through a 4kΩ resistor to a −15V supply. The −5V output is now taken from the ground pin (Pin 4) instead of V_{OUT}. It is essential to arrange the output load and the supply resistor R_S so that the net current through the ADREF02 is less than 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard +5V output configuration.

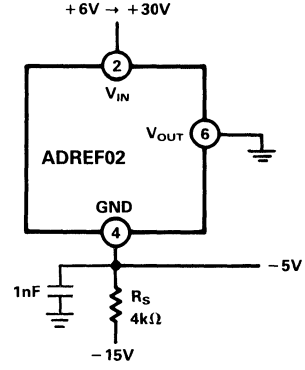


Figure 6. Negative 5V Reference

5V OR 10V REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The ADREF02 is ideal for applications with 10- and 12-bit multiplying CMOS D/A converters. In the standard hook-up, as shown in Figure 7, the ADREF02 is paired with the AD7533 10-bit multiplying DAC and the AD711 high-speed BiFET op amp. The amplifier/DAC configuration produces a unipolar 0 to −5V output range. Bipolar output applications and other operating details can be found on the AD7533 data sheet. The ADREF01 can also be used in this configuration to produce a unipolar 0 to −10V output range.

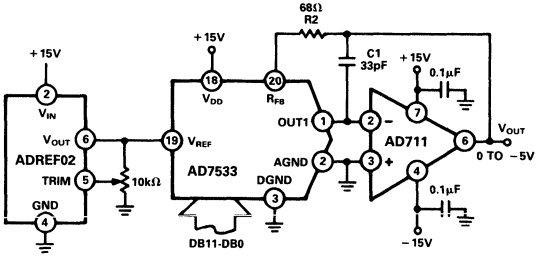


Figure 7. Low-Cost 10-Bit CMOS DAC Application

CURRENT SOURCE

The design of the ADREF01 allows it to be easily configured as a current source. The voltage drop from Pin 2 to Pin 4 in Figure 8 must remain between 13.5V and 36V. There will be a constant 10V drop across R_C. By choosing control resistor R_C you can vary the load current from the quiescent current (2mA typically) to approximately 10mA.

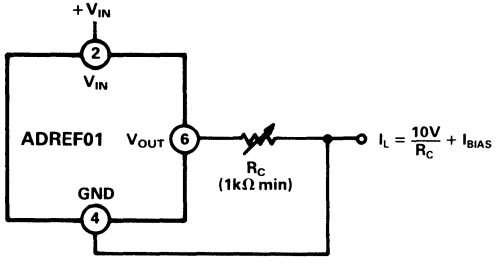


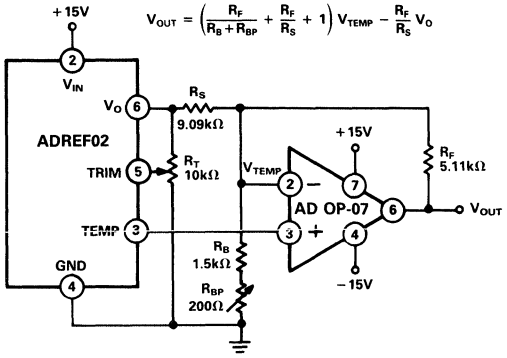
Figure 8. Current Source

In the case of the ADREF02, the voltage drop across Pin 2 to Pin 4 from Figure 8 must remain between 8V and 36V. There will be a constant 5V drop across R_C (500Ω minimum)

$$I_L = \frac{5V}{R_C} + I_Q.$$

TEMPERATURE TRANSDUCER

The temperature out pin of the ADREF02 allows it to be used as a temperature transducer. The output of Pin 3 (TEMP) is a voltage that varies linearly with temperature. V_{TEMP} at 25°C is 630mV, and the temperature coefficient is 2.1mV/°C. In the configuration shown in Figure 9, V_{OUT} from Pin 6 of the ADREF02 provides a stable reference voltage for the AD OP-07 op amp. The temperature dependent voltage from the TEMP pin of the ADREF02 is amplified by the AD OP-07 to provide a wider full-scale range and more current sourcing capability.



TEMPERATURE	V_{OUT}
−55°C	−0.55V
0°C	0V
+125°C	+1.25V

Figure 9. Temperature Transducer

The resistor values in Figure 9 produce an output (V_{OUT}) that varies 10mV/°C from −0.55V to +1.25V over the military temperature range. The potentiometer R_T controls the offset of the transfer function, and the potentiometer R_{BP} controls its slope. The equation in Figure 9 can be used to set resistor values for other output ranges.

Data Acquisition Subsystems
Contents

Selection Guide
Data Acquisition Subsystems

Model	Resolution Bits	Throughput Rate kHz	No. Channels	Bus Interface	Package Options[1]	Temp Range[2]	Page	Comments
AD1332	**12**	**125**	**1**	**12**	**D**	**I**	**9–31**	**Complete 12-Bit 125 kHz Sampling ADC**
***AD1330**	**12**	**100**	**1**	**12**	**D**	**C**	**9-29**	**18-Bit Floating Point DAS**
***AD1334**	**12**	**65**	**4**	**12**	**D**	**I**	**9–49**	**Four-Channel 12-Bit Sampling ADC**
AD368	**12**	**50**	**1**	**12**	**D**	**I, M**	**9–19**	**Complete 12-Bit ADC with Programmable Gains of 1, 8, 64, 512**
AD369	**12**	**50**	**1**	**12**	**M**	**I**	**9–19**	**Complete 12-Bit ADC with Programmable Gains of 1, 10, 100, 500**
AD364	12	50	16/8	12	D	C, M	9–5	High Speed 16-Channel 12-Bit DAS
AD363	12	40	16/8	12	D	C, M	9–5	16-Channel 12-Bit DAS
AD1362			**16/8**		**D**	**C, M**	**9–65**	**16-Channel Analog Front-End for 12-Bit ADC**
DAS1152	**14**	**25**	**1**	**14**	**D**	**I**	**9–73**	**14-Bit High Accuracy Sampling ADC**
DAS1157	**14**	**18**	**1**	**14**	**D**	**I**	**9–77**	**Low Power 14-Bit Sampling ADC**
DAS1153	**15**	**25**	**1**	**15**	**D**	**I**	**9–73**	**15-Bit High Accuracy Sampling ADC**
DAS1158	**15**	**18**	**1**	**15**	**D**	**I**	**9–77**	**Low-Power 16-Bit Sampling ADC**
AD367	15		1	Serial	M	C	9–13	Integrating ADC with Programmable Gain Amplifier
DAS1159	**16**	**18**	**1**	**16**	**D**	**I**	**9–77**	**Low Power 16-Bit Sampling ADC**

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; M–Metal Hermetic Dual-In-Line.
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

Orientation
Data Acquisition Subsystems

Data acquisition subsystems provide many of the functional elements of a complete data acquisition system, in various combinations. By doing this, these subsystems allow complete performance to be provided and specified more easily than with systems built from individual components.

Among the functional blocks that data acquisition subsystems provide are:

- multiple channel input multiplexer
- programmable gain amplifier
- sample-hold amplifier
- microprocessor interface
- analog-to-digital converter
- converter reference

The data acquisition subsystems detailed on the following pages provide a wide span of performance capabilities. Resolutions of 12, 14, 15 and 16 bits, gain ranges of 64:1 up to 512:1 and throughputs from 18 to 50kHz are available. These specifications must be compared along with input range, package size, power consumption and linearity to decide which data acquisition subsystem, if any, is best for the application.

Complete 16-Channel, 12-Bit Data Acquisition Systems

AD363/AD364

FEATURES

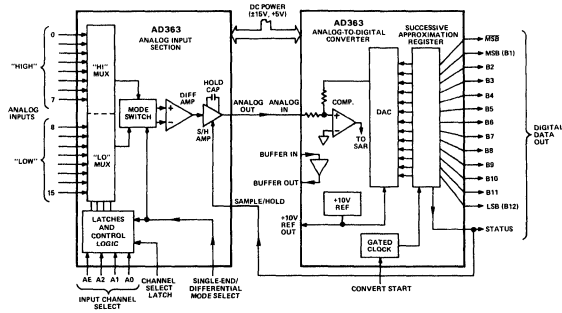
AD363

16-Channel Data Acquisition Input Stage with:
- **Digitally Controlled Channel Selection/Mode Control**
- **16 Single-Ended or 8 Differential Channels**
- **25kHz Throughput Rate**
- **Guaranteed No Missing Codes Over Temperature**

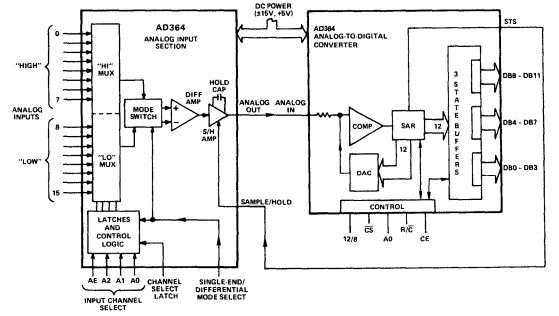
AD364

16-Channel Data Acquisition Input Stage with:
- **Digitally Controlled Channel Selection/Mode Control**
- **16 Single-Ended or 8 Differential Channels**
- **20kHz Throughput Rate**
- **Guaranteed No Missing Codes Over Temperature**
- **Three-State Buffered Digital Output**

AD363 FUNCTIONAL BLOCK DIAGRAM



AD364 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTIONS

The AD363/AD364 are 16-channel data acquisition systems which condition and subsequently convert a voltage signal into a 12-bit digital word. The system consists of two devices, the analog input stage (AIS) and the analog-to-digital converter (ADC). The AIS includes a 16-channel multiplexer, a differential amplifier and a sample-and-hold amplifier. The ADC is a 12-bit successive approximation type converter with an on-board voltage reference and a three-state digital output. The AIS is manufactured using reliable hybrid circuit technology and is packaged in a 32-pin DIP. The ADC is a monolithic IC and is packaged in a 18-pin DIP.

The AD364 is a sixteen channel data acquisition system which conditions and subsequently converts a voltage signal into a 12-bit digital word. The system consists of two devices, the analog input stage (AIS) and the analog-to-digital converter (ADC). The AIS includes a 16-channel multiplexer, a differential amplifier and a sample-and-hold amplifier. The ADC is a 12-bit successive approximation type converter with an on-board voltage reference and a three-state digital output. The AIS is manufactured using reliable hybrid circuit technology and is packaged in a 32-pin DIP. The ADC is a single-chip IC and is packaged in a 28-pin DIP.

Both products are specified for operation over both commercial (0 to +70°C) and military (−55°C to +125°C) temperature ranges. The AD363 and AD364 are available with screening in accordance with the B Program of ADI Microelectronics. Please contact the factory or nearest sales office for details.

ORDERING GUIDE

Model	Temperature Range
AD363RKD	0 to +70°C
AD363RSD	−55°C to +125°C
AD364RJD	0 to +70°C
AD364RKD	0 to +70°C
AD364RSD	−55°C to +125°C
AD364RTD	−55°C to +125°C

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

Parameter	AD363RK	AD363RS
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Ranges		
Bipolar	±2.5V, ±5.0V, ±10.0V	*
Unipolar	0 to +5V, 0 to +10V	*
Input (Bias) Current, Per Channel	±50nA max	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
RESOLUTION	12 BITS	*
ACCURACY		
Gain Error[1]	±0.05% FSR (Adj. to Zero)	*
Unipolar Offset Error	±10mV (Adj to Zero)	*
Bipolar Offset Error	±20mV (Adj to Zero)	*
Linearity Error	±½LSB max	*
Differential Linearity Error	±1LSB max (±½LSB typ)	*
Relative Accuracy	±0.025% FSR	*
Noise Error	1mV p-p, 0 to 1MHz	*
TEMPERATURE COEFFICIENTS		
Gain	±30ppm/°C max (±10ppm/°C typ)	±25ppm/°C max (±15ppm/°C typ)
Offset, ±10V Range	±10ppm/°C max (±5ppm/°C typ)	±8ppm/°C max (±5ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	*
SIGNAL DYNAMICS		
Conversion Time[2]	25μs max (22μs typ)	*
Throughput Rate, Full Rated Accuracy	25kHz min (30kHz typ)	*
Sample and Hold		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time		
To ±0.01% of Final Value for Full Scale Step	18μs max (10μs, typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[3]		
Convert Command (to ADC Section, Pin 21)	Positive Pulse, 200ns min Width. Leading Edge ("0" to "1") Resets Register, Trailing Edge ("1" to "0") Starts Conversion.	*
	1TTL Load	*
Input Channel Select (To Analog Input Section, Pins 28-31)	4 Bit Binary, Channel Address.	*
	1LS TTL Load	*
Channel Select Latch (To Analog Input Section, Pin 32)	"1" Latch Transparent	*
	"0" Latched	*
	4LS TTL Loads	*
Sample-Hold Command (To Analog Input Section Pin 13 Normally Connected To ADC "Status", Pin 20)	"0" Sample Mode	*
	"1" Hold Mode	*
	2LS TTL Loads	*
Short Cycle (To ADC Section Pin 14)	Connect to +5V for 12 Bits Resolution.	*
	Connect to Output Bit n + 1 For n Bits Resolution.	*
	1TTL Load	*
Single Ended/Differential Mode Select (To Analog Input Section, Pin 1)	"0": Single-Ended Mode	*
	"1": Differential Mode (+4.0V min)	*
	3TTL Loads	*

Parameter	AD363RK	AD363RS
DIGITAL OUTPUT SIGNALS[3]		
(All Codes Positive True)		
Parallel Data		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary/Two's Complement	*
Output Drive	2TTL Loads	*
Serial Data (NRZ Format)		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Output Drive	2TTL Loads	*
Status ($\overline{\text{Status}}$)	Logic "1" ("0") During Conversion	*
Output Drive	2TTL Loads	*
Internal Clock		
Output Drive	2TTL Loads	*
Frequency	500kHz	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV	*
Max External Current	±1mA	*
Voltage Temp. Coefficient	±20ppm/°C, max	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ +45mA max (+38mA typ)	*
	-15V, ±5% @ -45mA max (-38mA typ)	*
	+5V, ±5% @ +136mA max (+113mA typ)	*
Total Power Dissipation	2 watts max (1.7 watts typ)	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[4]	-55°C to +150°C
PACKAGE OPTIONS[5]		
Analog Input Section (DH-32E)	AD363RKD	AD363RSD
ADC Section (DH-32C)	AD363RKD	AD363RSD

NOTES:
[1] With 50Ω, 1% fixed resistor in place of Gain Adjust pot.
[2] Conversion time of ADC Section.
[3] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V.
One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.
[4] AD363K External Hold Capacitor is limited to +85°C; Analog Input Section and ADC Section may be stored at up to +150°C.
[5] See Section 14 for package outline information.
*Specifications same as AD363RK.
Specifications subject to change without notice.

9

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V	V_{IN}, Signal	±V, Analog Supply
+V, Analog Supply	+16V	V_{IN}, Digital	0 to +V, Digital Supply
-V, Analog Supply	-16V	A_{GND} to D_{GND}	±1V

AD363 PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION		ANALOG TO DIGITAL CONVERTER SECTION	
Pin Number	Function	Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode (+4.0V min)	1	Data Bit 12 (Least Significant Bit) Out
2	Digital Ground	2	Data Bit 11 Out
3	Positive Digital Power Supply, +5V	3	Data Bit 10 Out
4	"High" Analog Input, Channel 7	4	Data Bit 9 Out
5	"High" Analog Input, Channel 6	5	Data Bit 8 Out
6	"High" Analog Input, Channel 5	6	Data Bit 7 Out
7	"High" Analog Input, Channel 4	7	Data Bit 6 Out
8	"High" Analog Input, Channel 3	8	Data Bit 5 Out
9	"High" Analog Input, Channel 2	9	Data Bit 4 Out
10	"High" Analog Input, Channel 1	10	Data Bit 3 Out
11	"High" Analog Input, Channel 0	11	Data Bit 2 Out
12	No Connect	12	Data Bit 1 (Most Significant Bit) Out
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 20	13	$\overline{\text{Data Bit 1}}$ ($\overline{\text{MSB}}$) Out
		14	Short Cycle Control Connect to +5V for 12 Bits Connect to Bit (n+1) Out for n Bits
		15	Digital Ground
		16	Positive Digital Power Supply, +5V
14	Offset Adjust	17	$\overline{\text{Status}}$ Out "0": Conversion in Progress (Parallel Data Not Valid) "1": Conversion Complete (Parallel Data Valid)
15	Offset Adjust		
16	Analog Output Normally Connected to ADC "Analog In"		
17	Analog Ground	18	+10Volt Reference Out
18	"High" ("Low") Analog Input, Channel 15 (7)	19	Clock Out (Runs During Conversion)
19	"High" ("Low") Analog Input, Channel 14 (6)	20	Status Out "0": Conversion Complete (Parallel Data Valid) "1": Conversion in Progress (Parallel Data Not Valid)
20	Negative Analog Power Supply, -15V		
21	Positive Analog Power Supply, +15V		
22	"High" ("Low") Analog Input, Channel 13 (5)		
23	"High" ("Low") Analog Input, Channel 12 (4)		
24	"High" ("Low") Analog Input, Channel 11 (3)	21	Convert Start In Reset Logic : ↑ Start Convert : ↓
25	"High" ("Low") Analog Input, Channel 10 (2)		
26	"High" ("Low") Analog Input, Channel 9 (1)		
27	"High" ("Low") Analog Input, Channel 8 (0)	22	Comparator In
28	Input Channel Select, Address Bit AE	23	Bipolar Offset Open for Unipolar Inputs Connect to ADC Pin 22 for Bipolar Inputs
29	Input Channel Select, Address Bit A0		
30	Input Channel Select, Address Bit A1		
31	Input Channel Select, Address Bit A2		
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"	24	10V Span R In
		25	20V Span R In
		26	Analog Ground
		27	Gain Adjust
		28	Positive Analog Power Supply, +15V
		29	Buffer Out (For External Use)
		30	Buffer In (For External Use)
		31	Negative Analog Power Supply, -15V
		32	Serial Data Out Each Bit Valid On Trailing (↓) Edge Clock Out, ADC Pin 19

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

Parameter	AD364RJ	AD364RK	AD364RS	AD364RT	Units
ANALOG INPUTS					
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)				
Input Voltage Range					
T_{min} to T_{max}	±10	*	*	*	V
Input (Bias) Current per Channel	±50	*	*	*	nA
Input Impedance ON Channel	10^{10}/100	*	*	*	Ω/pF
OFF Channel	10^{10}/10	*	*	*	Ω/pF
Input Fault Current	20	*	*	*	mA max
(Power ON or OFF)					(Internally
Common Mode Rejection					Limited)
Differential Mode 1kHz 20Vp-p	70 min (80 typ)	*	*	*	dB
Mux Cross Talk (Any OFF Channel					
to Any ON Channel) 1kHz					
20V p-p	-80 max (-90 typ)	*	*	*	dB
Offset, Channel to Channel	±5	*	*	*	mV max
ACCURACY					
Gain Error[1]	0.3	*	*	*	% of FSR
Unipolar Offset Error[2]	±10	±8	*	**	mV
Bipolar Offset Error[2]	±50	±20	*	**	mV
Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Differential Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Noise Error	1mV p-p 0.1Hz to 1MHz	*	*	*	
TEMPERATURE COEFFICIENTS					
Gain	54	31	*	**	ppm/°C
Offset (±10V Range)	12	7	*	**	ppm/°C
Operating Temperature Range	0 to +70°C	*	-55°C to +125°C	***	ppm/°C
SIGNAL DYNAMICS					
Conversion Time	32 max (25 typ)	*	*	*	µs
Throughput Rate, Full Accuracy	20 min (25 typ)	*	*	*	kHz
Sample Hold					
Aperture Delay	100 max (50 typ)	*	*	*	ns
Aperture Uncertainty	500 max (100 typ)	*	*	*	ps
Acquisition Time					
To 0.01% of Final Value					
For Full Scale Step	18 max (10 typ)	*	*	*	µs
Feedthrough at 1kHz	-70 max (-80 typ)	*	*	*	dB
Droop Rate	2 max (1 typ)	*	*	*	mV/ms
DIGITAL INPUT SIGNALS					
Analog Input Section					
Input Channel Select	4 Bit Binary Address	*	*	*	
	1 LS TTL Load	*	*	*	
Channel Select Latch	"1" Latch Transparent	*	*	*	
	"0" Latched	*	*	*	
	4 LS TTL Loads	*	*	*	
Single Ended/Differential	"0" Single Ended	*	*	*	
Mode Select	"1" Differential (+4V min)	*	*	*	
	3TTL Loads	*	*	*	
Sample and Hold Command	"0" Sample Mode	*	*	*	
	"1" Hold Mode	*	*	*	
	1TTL Load	*	*	*	
ADC Section[3] $4.5 \leqslant V_L \leqslant 5.5$					
Logic Input Threshold					
T_{min} to T_{max}					
Logic "1"	2.0	*	*	*	V min
Logic "0"	0.8	*	*	*	V max
Logic Input Current					
T_{min} to T_{max}					
Logic "1"	10	*	*	*	µA max
Logic "0"	10	*	*	*	µA max
DIGITAL OUTPUT SIGNALS					
Logic Outputs T_{min} to T_{max}					
Sink Current V_{OUT} = 0.4V	1.6	*	*	*	mA min
Source Current V_{OUT} = 2.4V	0.5	*	*	*	mA min
Output Leakage When In					
Three State	±40	*	*	*	µA max
Output Coding					
Unipolar	Positive True Binary	*	*	*	
Bipolar	Positive True Offset				
	Binary	*	*	*	

Parameter	AD364RJ	AD364RK	AD364RS	AD364RT	Units
POWER REQUIREMENTS					
Supply Voltages/Currents	+15V, ±5% @ 36mA max	*	*	*	
	-15V, ±5% @ 65mA max	*	*	*	
	+5V, ±5% @ 75mA max	*	*	*	
PACKAGE OPTIONS[4]					
Analog Input Section (DH-32E)	AD364RJD	AD364RKD	AD364RSD	AD364RTD	
ADC Section (D-28)	AD364RJD	AD364RKD	AD364RSD	AD364RTD	

NOTES
[1] With 50Ω resistor from REF IN to REF OUT. Adjustable to zero.
[2] Adjustable to zero.
[3] 12/$\overline{8}$ line must be hard wired to V_{LOGIC} or digital common.
[4] See Section 14 for package outline information.
*Specifications same as AD364J.

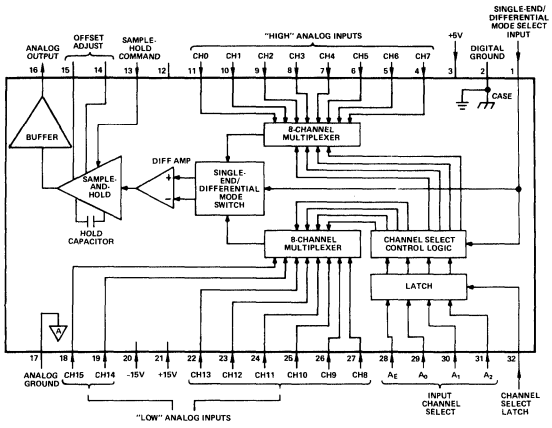
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V	V_{IN}, Signal	±V, Analog Supply
+V, Analog Supply	+16V	V_{IN}, Digital	0 to +V, Digital Supply
-V, Analog Supply	-16V	A_{GND} to D_{GND}	±1V

AD364 PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION		ANALOG TO DIGITAL CONVERTER SECTION	
Pin Number	Function	Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode	1	Logic Power Supply, +5V
2	Digital Common	2	Data Mode Select (12/$\overline{8}$) "0": 8 Upper Bits or 4 Lower Bits as Selected by Byte Select (A_0)
3	Positive Digital Power Supply, +5V		
4	"High" Analog Input, Channel 7	3	Chip Select ($\overline{CS}$) "0": Device Selected "1": Device Inhibited
5	"High" Analog Input, Channel 6		
6	"High" Analog Input, Channel 5		
7	"High" Analog Input, Channel 4	4	Byte Address/Short Cycle (A_0) "0": Upper 8 Bits Enabled (12/$\overline{8}$ "0")/ 12 Bit Cycle "1": Lower 4 Bits Enabled (12/$\overline{8}$ "1")/ 8 Bit Cycle
8	"High" Analog Input, Channel 3		
9	"High" Analog Input, Channel 2		
10	"High" Analog Input, Channel 1		
11	"High" Analog Input, Channel 0		
12	No Connect	5	Read Convert (R/$\overline{C}$) "0": Convert Start "1": Read Enable
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 28	6	Chip Enable (CE) ⎍: R/$\overline{C}$ "0", $\overline{CS}$ "0" Initiates Conversion ⎍: R/$\overline{C}$ "1", $\overline{CS}$ "0" Initiates Read "0": Device Disabled "1": Device Enabled
14	Offset Adjust		
15	Offset Adjust		
16	Analog Output Normally Connected to ADC "Analog In"	7	Analog Power Supply, +15V (V_{CC})
		8	Reference Out, +10V
17	Analog Common	9	Analog Common (AC)
18	"High" ("Low") Analog Input, Channel 15 (7)	10	Reference In
19	"High" ("Low") Analog Input, Channel 14 (6)	11	Analog Power Supply, -15V (V_{EE})
20	Negative Analog Power Supply, -15V	12	Bipolar Offset
21	Positive Analog Power Supply, +15V	13	10 Volt Span Input
22	"High" ("Low") Analog Input, Channel 13 (5)	14	20 Volt Span Input
23	"High" ("Low") Analog Input, Channel 12 (4)	15	Digital Common (DC)
24	"High" ("Low") Analog Input, Channel 11 (3)	16	Data Bit 0
25	"High" ("Low") Analog Input, Channel 10 (2)	17	Data Bit 1
26	"High" ("Low") Analog Input, Channel 9 (1)	18	Data Bit 2
27	"High" ("Low") Analog Input, Channel 8 (0)	19	Data Bit 3
28	Input Channel Select, Address Bit AE	20	Data Bit 4
29	Input Channel Select, Address Bit A0	21	Data Bit 5
30	Input Channel Select, Address Bit A1	22	Data Bit 6
31	Input Channel Select, Address Bit A2	23	Data Bit 7
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"	24	Data Bit 8
		25	Data Bit 9
		26	Data Bit 10
		27	Data Bit 11
		28	Status Out



AIS Functional Block Diagram

Concept

Figure 1 shows a general DAS application.

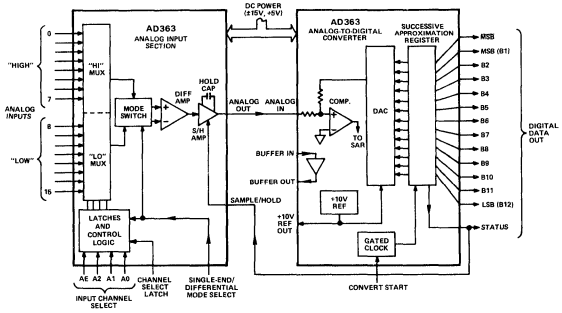


Figure 1. AD363

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

System Timing

Figure 2 is a timing diagram for the circuit shown in Figure 1 and operating at maximum conversion rate.

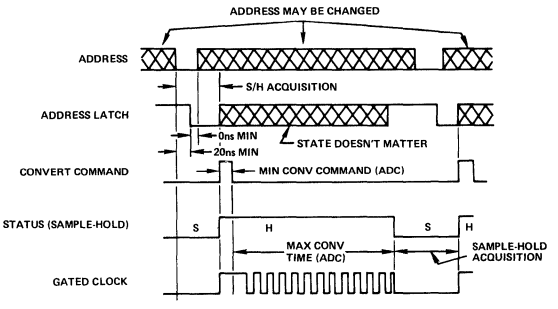


Figure 2. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

Single-Ended/Differential Mode Control

The AIS features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a non-TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels) (+4.0V min)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF

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Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table I. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "hold" mode).

Input Channel Address Latch

The AIS is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (pin 13) is normally connected to the Status output (pin 20) from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1", putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous sample mode.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AIS may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to the AIS voltage offset and if a gain stage was to be inserted between the AIS and the ADC. To adjust the offset of the AIS, the circuit shown in Figure 4 is recommended.

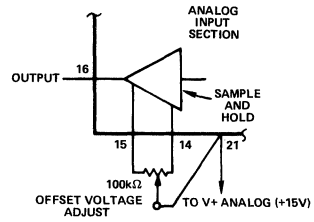


Figure 4. AIS Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (pin 17) and Digital Ground (pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AIS as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AIS they should be connected with back-to-back general purpose diodes as shown in Figure 5. This will protect the AIS from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200mV between grounds, however this difference will be reflected directly as an input offset voltage.

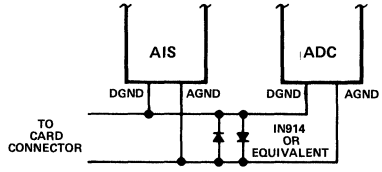


Figure 5. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

ANALOG DEVICES

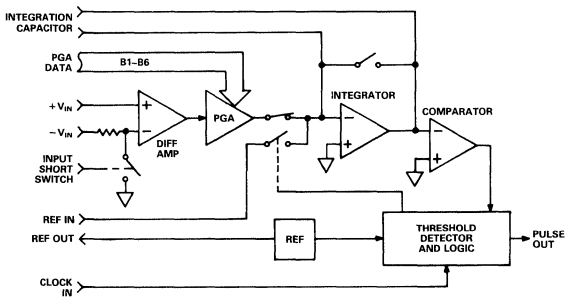
High Resolution Programmable Gain DAS

AD367

FEATURES
Differential Input – Programmable Gain Amplifier
6-Bit (1 of 64) Gain Control
Internal −10V Reference
15-Bit Integral Nonlinearity
±305μV Resolution
10ms Conversion Time
External Integration Capacitor
Programmable Conversion Time

APPLICATIONS
Medical Instruments
Blood Analyzers
Analytical Instrumentation
Data Acquisition Systems
Chromatography
Process Control

AD367 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD367 is a wide dynamic range integrated circuit which contains all the analog functions needed to construct a high resolution, high accuracy integrating Data Acquisition System. It utilizes hybrid technology to incorporate a programmable gain amplifier, integration amplifier, −10V reference, comparator, and control logic in a 24-pin hermetic dual-in-line package.

The programmable gain amplifier provides 6-bits (1 of 64) gain control which are digitally selectable with CMOS voltage levels. The dual slope converter uses time to quantitize the analog input signal. The differential front-end allows true differential inputs with high common mode rejection, or single-ended inputs with ground sense capability. This conversion technique has inherent high frequency noise immunity and excellent normal mode noise rejection at frequencies that are integal multiples of $1/T_1$ (T_1 = the signal integration period). The conversion accuracy is independent of both the integration capacitance and clock frequency, since they affect both the signal integration phase and reference integration phase in the same ratio. A microprocessor and software routine or any digitizing timer that accepts TTL inputs can be used to count clock pulses to digitize the AD367 output. The integration capacitor is external, therefore conversion time may be adjusted by the user. The nominal value is 0.012μF for an integration time of 4ms and total conversion time of 10ms. By choice of integration capacitor and clock frequency the integration time is programmed from a minimum of 2ms to a maximum of 20ms. The maximum conversion rate is 200 samples per second.

PRODUCT HIGHLIGHTS

1. The AD367KM provides true 15-bit (±0.00305% FSR maximum linearity error) performance with 305μV resolution.
2. The differential input programmable gain amplifier front end has 6-bit (1 of 64) gain control. This provides gains of 0.282V/V to 24V/V, or input full-scale ranges of 0.417V to 10.0V for maximum flexibility.
3. The integration capacitor is external. Integration time is user-programmable, from 2ms to 20ms. The maximum conversion rate is 200 conversions per second.
4. The dual slope integration conversion technique provides superior high frequency noise immunity, and excellent normal mode noise rejection of frequencies which are multiples of the inverse of the integration period.
5. An internal precision −10.0V reference is provided, but an external reference may be used for multi-channel applications where use of a system reference is required.
6. The pulse-width output is easily converted to digital binary format by the addition of external IC counter-timers. The counter clock rate is independent of the integrator clock rate.

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ORDERING GUIDE

Model	Linearity Error	Resolution	Temperature Range
AD367KM	±0.00305% FSR	±305μV	0 to +70°C

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, +5V, T1 = 4.000ms, C_{INT} = 0.012μF[1] unless otherwise noted)

Parameter	AD367KM Min	Typ	Max	Units
ACCURACY/RESOLUTION				
Integral Nonlinearity Error [2]			0.00305	% FSR
Resolution [3]	±305			μV
ANALOG INPUTS				
Range	0		10	V
Input Resistance	80			kΩ
Common Mode Rejection Ratio[4]	90	100		dB
V_{REF} Input Resistance	300			kΩ
Shorting Switch Isolation[5]	45	56		dB
DIGITAL INPUTS				
Clock				
V_{IH}	2.0			V
V_{IL}			0.7	V
Gain Bits[6]				
V_{IH}	14.5			V
V_{IL}			0.5	V
DIGITAL OUTPUT (LSTTL Compatible)				
V_{OH}	2.4			V
V_{OL}			0.4	V
I_{OH}	−370			μA
I_{OL}			6	mA
DYNAMIC PERFORMANCE				
Conversion Time			10	ms
Offset Pulse Width[7]	152	200	248	μs
Scale Factor	361	384	407	μs/V
Over Temperature		±10		ppm/°C
PSRR[8]				
+15V ± 3%		0.5		μs/V
−15V ± 3%		0.5		μs/V
+5V ± 3%		1		μs/V
PROGRAMMABLE GAIN AMPLIFIER[9]				
Maximum Gain		24		V/V
Minimum Gain		0.282		V/V
Resolution			6	Bits
Gain Error, Any Range			±2	%
Gain Linearity Error			±0.00305	% FSR
INTERNAL VOLTAGE REFERENCE				
V_{REF}	−9.95	−10	−10.05	V
vs. Temperature		10	15	ppm/°C
Maximum External Current without Degradation			500	μA
POWER REQUIREMENTS				
Positive Supply Range	14.55	15	15.45	V
Negative Supply Range	−14.55	−15	−15.45	V
Logic Supply Range	4.75	5	5.25	V
Supply Current				
+15V		18		mA
−15V		23		mA
+5V		27		mA
Power Dissipation		750	1100	mW
TEMPERATURE RANGE				
Specification	0		70	°C
Operating	−25		+85	°C
Storage	−55		+125	°C
PACKAGE OPTION[10] (DH-24D)	24-Pin DIP			

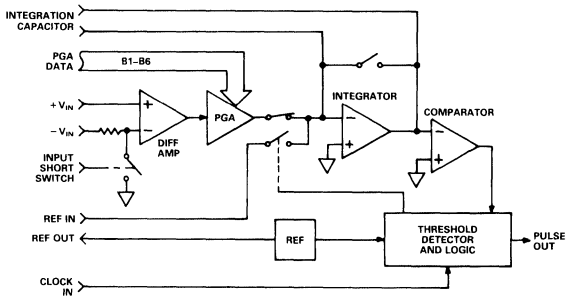
NOTES
[1]Polystyrene or Teflon.
[2]Referenced to the input.
[3]Referenced to the output of the programmable gain stage (Pin 4).
[4]Source impedance <1Ω 0 to 10V
[5]A_{INL} (Pin 2) at analog ground.
[6]Open collector TTL and 15V CMOS compatible.

[7]Offset Pulse width (V_{IN} = 0V) = $\frac{V_{OS} C R_{INT2}}{V_{REF}}$, R_{INT2} = 327kΩ nominal.

[8]V_{IN} = 10V, Gain = 1.03.

[9]Gain = $\frac{24 \times (128 \times B1 + 64 \times B2 + 32 \times B3 + 16 \times B4 + 8 \times B5 + 4 \times B6 + 3)}{255}$

[10]See Section 14 for package outline information.
Specifications subject to change without notice.



AD367 Functional Block Diagram

BASIC OPERATION

The AD367 is a high resolution dual slope integrating converter building block. Its output is a pulse width whose duration is proportional to the input voltage and the gain selected. The active-low output pulse is used to gate a separate counter which accumulates pulses from a high speed clock. This partition of the analog-to-digital conversion function into an analog processing section and digital counting greatly reduces the potential for crosstalk between the noisy digital function and the low-level signal processing performed by the analog front-end. This preserves the inherent rejection of high frequency normal mode noise that is a prime advantage of the dual slope conversion technique.

INPUT STAGE

The AD367 is internally partitioned into a differential-input amplifier, a single-ended user-programmable gain amplifier, and the actual dual-slope converter. The differential amplifier allows digitization of input signals with common mode voltages of up to ±10V. It has a nominal input impedance of 100kΩ and is configured for unity gain.

The programmable gain amplifier (PGA) is programmed via a 6-bit digital code. If "B_1", represents the logical value of the most significant gain-selected bit, "B_2" the next most significant bit, etc., then the gain of the PGA is:

$$G = \frac{(128B_1 + 64B_2 + 32B_3 + 16B_4 + 8B_5 + 4B_6 + 3) \times 24}{255}$$

The gain-select pins are internally pulled-up to the +15V supply. Gain programming can be accomplished using either an open collector TTL Driver such as the 7406 or with 4000-series CMOS (V_{DD} = 15V). For fixed gain applications the gain-select pins can be tied to analog ground or left open as required.

B_1	B_2	B_3	B_4	B_5	B_6	GAIN (V/V)
0	0	0	0	0	0	0.282
0	0	0	0	0	1	0.659
			.			.
			.			.
			.			.
1	0	0	0	0	0	12.33
			.			.
			.			.
			.			.
1	1	1	1	1	1	24.00

Table I. AD367 PGA Truth Table

INTEGRATOR STAGE

The AD367 integrator stage uses the dual slope conversion technique. A simplified dual slope converter is shown in Figure 1. While the input pulse is applied to clock in, the input signal is applied to the integrator. After a predetermined period the input pulse is removed, a reference signal of opposite polarity is applied to the integrator, and the output pulse is initiated. At the moment the integrator is switched to the reference (deintegration) phase the accumulated charge on the integrating capacitor is proportional to the average value of the input over the integration interval. The deintegration of the reference is an opposite going ramp with slope V_{REF}/RC. When the integrator output reaches zero, the comparator is tripped and the output pulse is terminated. This completes the conversion cycle. Since the charge gained in the integration phase is proportional to $V_{IN} \times T$ (see Figure 1) and the amount of charge lost is proportional to $V_{REF} \times t$ (and equal to the amount of charge gained) t is proportional to V_{IN}/V_{REF}. The converter output is thus a pulse whose width is proportional to the input voltage. A dual slope converter is therefore a Voltage-to-Time converter. If the output pulse is used to gate a binary counter, the output of the counter will be binary digital representation of the input voltage.

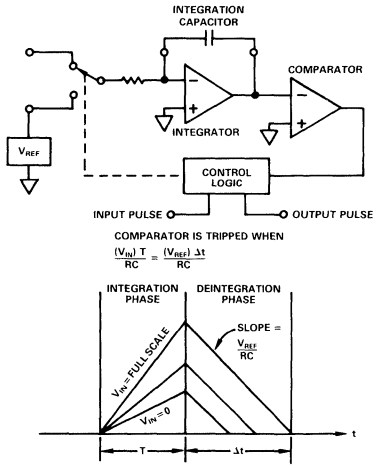


Figure 1. Simplified Basic Dual Slope Converter

ADVANTAGES OF DUAL-SLOPE INTEGRATION

Conversion accuracy is independent of the length of the clock period and the integrating capacitance. Theoretical accuracy depends only on the absolute value of the reference and the stability of the clock. Even changes in other components such as the comparator input offset voltage have no effect as long as they do not change during a conversion. Differential linearity is excellent since the technique is analog and inherently free from discontinuities.

AD367 DETAILED OPERATION

The input differential amplifier operates with input voltages within the common mode range of 0 to 10V. The input resistance is 100kΩ (80kΩ minimum) and there is a shorting switch on the noninverting input for user calibration in single-ended mode.

The input shorting switch shorts $+V_{IN}$ to ground through 20kΩ to limit the short circuit current of the driver. The AD367 inputs must be buffered. The AD OP-07 is well recommended for this purpose, due to its low noise. For source impedances of less than 5-10kΩ the AD OP-27 would be an even better choice. Note: The high 1/f noise of most FET and BiFET amplifiers make them unsuitable for this application.

The offset of the PGA section is not trimmable per se, however, the direct PGA output is available on Pin 4. Great care must be exercised to avoid introducing extraneous signals at this point. A more detailed procedure for offset trim and calibration of the AD367 is given below in the calibration section.

The dual slope converter section is configured for a nominal full-scale input voltage of 10V. In addition, the zero point of the converter is offset by 5% full scale. This guarantees that the converter linearity will not be degraded for inputs near zero. Maximum linearity is obtained when the gain is programmed so that the maximum full-scale input voltage produces an output pulse of maximum duration consistent with the desired conversion rate. Alternatively the gain can be set to provide a 10V signal to the integrator (or Pin 4, the output of the PGA) when a full-scale input is supplied.

The built-in offset is also used to protect against possible negative polarity inputs while taking very low level measurements (or "dark current" readings from optical sensors). The offset pulse is accomplished by using a portion of the internal reference as the threshold voltage to signal the end of conversion as shown in Figure 2. This voltage appears on Pin 7 and is factory set for

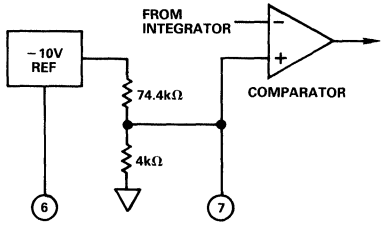


Figure 2.

−0.510V, which yields a nominal 200μs offset pulse with a 0.012μF integration capacitor. This offset pulse width may be adjusted by using a 100kΩ potentiometer as shown in Figure 3.

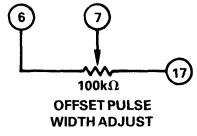


Figure 3.

The leading edge of an externally applied negative going clock pulse initiates a conversion. The AD367 will output a pulse whose width is proportional to the input signal. The output pulse is active low. Its leading (falling) edge is triggered by the rising edge of the external clock, and its trailing edge is dependent upon the input signal level. When using the internal reference or with an external −10V reference a clock pulse of 4ms provides an integrator full-scale range of 10V with a 0.012μF integration cap.

For other reference and integration capacitor values the signal integration period should be adjusted to prevent saturation of the integrator, i.e., the maximum integrator deflection should not exceed 10V.

The AD367 Transfer Function is:

$$\text{Pulse Width} = \frac{-V_{IN}}{V_{REF}} \times \frac{R_{INT2}}{R_{INT1}} T_1 + \frac{V_{OS}\, C\, R_{INT2}}{V_{REF}}$$

Where:

T_1 = The clock period
V_{OS} = Voltage Offset (−0.510V nominal)
C = Integration Capacitor
R_{INT1} = Signal Integration Resistor = 340kΩ
R_{INT2} = Reference Integration Resistor = 327kΩ
V_{REF} = −10V (if internal voltage reference is used)

Figure 4 shows the AD367 operation for a near full-scale input voltage. The input signal is integrated as the negative slope, and the reference voltage as the positive slope. The output pulse is low until the positive going edge (the reference integration phase) exceeds $-V_{OS}$ (+0.510V). The rising edge of the clock coincides with the knee of the integrator and the falling edge of the output.

Figure 5 shows a good view of the offset at work. A slight negative input voltage will not cause an absence of output pulse ($V_{IN} > -0.05V$).

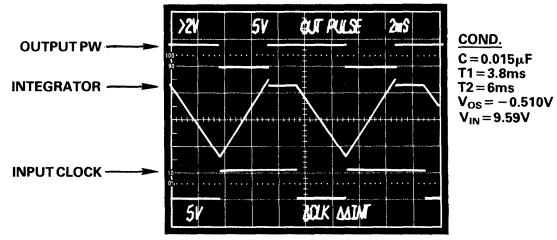


Figure 4.

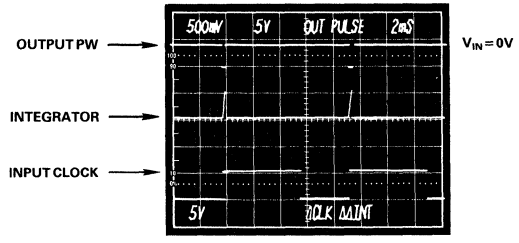


Figure 5.

To maximize the resolution and accuracy of the converter, the PGA gain should be set such that the maximum input signal voltage provides a 10V signal to the integrator (Pin 4). Then the clock pulse width and integration capacitor should be selected using the relation:

$$\frac{T_1}{C_{INT}} \cong R_{INT1} = 340k\Omega$$

This ensures that the maximum dynamic range of the integrator is used, and will result in the best linearity from the converter. Polystyrene or Teflon capacitors only are recommended. The AD367 Timing Diagram is shown in Figure 6.

PGA settling under worst-case conditions (Gain = 24, full-scale input voltage step) is typically 70μs, as shown in Figure 8. The PGA output must be allowed to settle before a conversion is initiated, or the first conversion result after an input voltage change ignored if the AD367 is operated in continuous conversion mode. Figure 9 shows the PGA settling after a change from minimum to maximum gain (0.282 to 24 V/V), which is also 70μs typically.

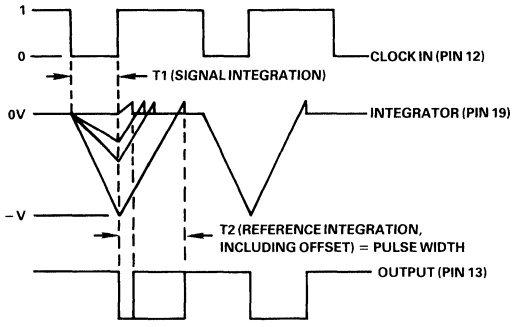


Figure 6. AD367 Timing Diagram

CALIBRATION

The AD367 should be endpoint calibrated for maximum system accuracy. Calibration is a straightforward procedure:

1. Choose a gain consistent with keeping the output of the programmable gain amplifier at or below 10V when a full-scale input voltage is applied.
2. Apply a zero input signal, V_Z. Use the shorting switch if the input is single-ended. The shorting switch will ensure a good ground potential at the input.
3. Measure the output offset pulse, PW_{OS}.
4. Apply a known full-scale voltage, V_{FS}, to the inputs.
5. Measure the output full-scale pulse, PW_{FS}.
6. Subsequent measurements will give, to within ±0.00305% FSR, the input voltage according to the following equation:

$$V_{IN} = (\text{Pulse Out} - PW_{OS}) \times \frac{(V_{FS} - V_Z)}{(PW_{FS} - PW_{OS})} + V_Z$$

INPUT, GROUNDING, AND DECOUPLING CONSIDERATIONS

For most applications, the AD367 will be used with single-ended inputs and the internal −10V reference. The connections for this mode of operation are shown in Figure 7, including input buffering, power supply decoupling, and input ground sense. As with many data acquisition components, the AD367 has separate analog and digital grounds. These pins (15 and 17) are not connected internally, but should be tied together at one point as close to the converter as possible. Ideally, a single solid ground plane under the converter is desirable. Current flows through the wires and etch stripes of circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground and the ground pins of the AD367. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize IR losses from current flow in the converter to system ground run. Care must be taken to prevent digital logic return currents from being summed into the same return path as analog signals to prevent measurement errors.

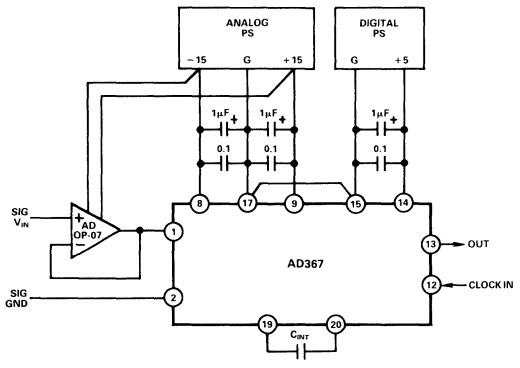


Figure 7. Input Connections for Single-Ended Operation

Each of the AD367's supply terminals should be capacitively decoupled as close to the AD367 as possible. A large value capacitor, such as 1μF, in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies should be decoupled to the analog ground pin, and the logic supply to the digital ground pin.

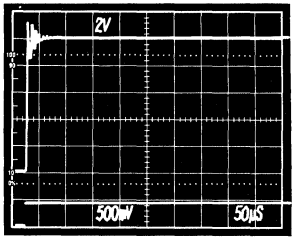


Figure 8. AD367 PGA Section Settling

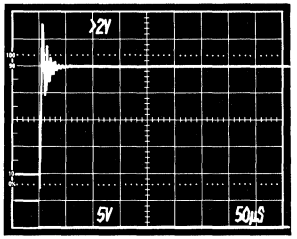


Figure 9. AD367 PGA Section Gain Settling

The metal case is at analog ground potential for shielding. Care should be exercised to prevent shorting to board circuitry beneath the part.

GENERAL INTERFACE CONSIDERATIONS

The control logic of the AD367 and the synchronous counter scheme shown in Figure 10 makes direct connection to most microprocessor buses possible. While it is impossible to describe the details of the interface connections for every microprocessor, a representative example is presented here.

Analog-to-digital converters, like any I/O device, may be interfaced to microprocessors by several methods. These include direct memory access (DMA), isolated or accumulator I/O, and memory-mapped I/O. DMA is the fastest, since conversions occur automatically and data updates into memory are transparent to the processor. DMA logic is very processor-dependent and requires specialized dedicated hardware.

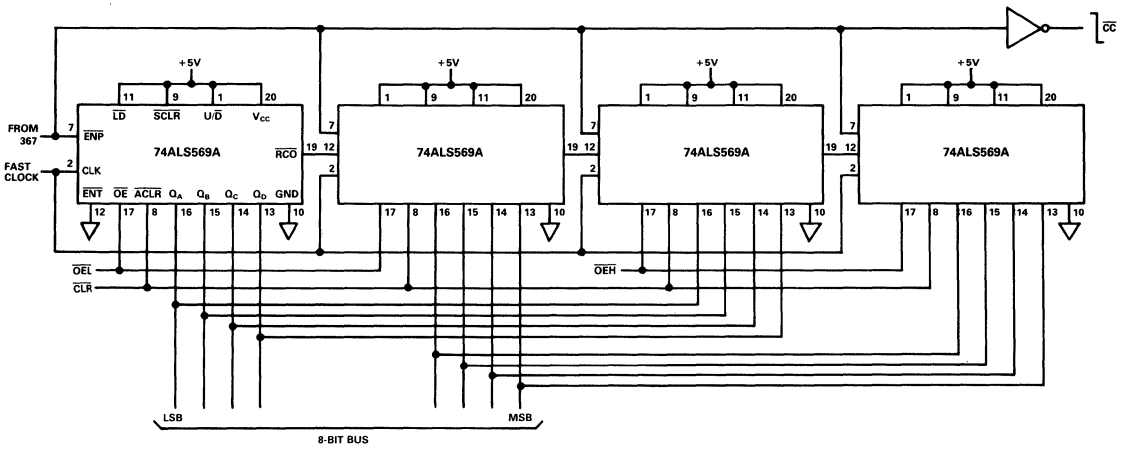


Figure 10. General Counter Scheme 8-Bit Bus

Memory-mapped and accumulator I/O are more often used and easier to implement. Accumulator I/O uses a distinct set of control signals which, combined with the address bus, define a totally separate I/O address space. The architecture is simple from a hardware standpoint, since address decoding requirements are not severe, and distinct I/O pulses are easily located for system debugging. However, processors using accumulator I/O can generally only send data to an output device from the accumulator. This can make for cumbersome software, since processor controlled transfers of I/O data to a memory location cannot be accomplished in a single instruction.

Memory-mapped I/O assigns the I/O device to one or more locations in the logical memory space of the microprocessor. This technique has the advantage that the full range of memory reference instructions may be used to operate on the data. The potential disadvantages include limiting the memory space available for program and data memory, somewhat more complex address decoding and more difficult isolation of device select pulses for system debugging. Nevertheless, many microprocessors offer only the memory-mapped I/O.

CONNECTING COUNTERS FOR DIGITAL OUTPUT

Figure 10 shows a simple circuit for converting the AD367 pulse width output to binary digital code using the 74LS569A synchronous counter. This scheme is compatible with μP systems using an 8-bit wide data bus structure, such as the 6809. It is easily upgraded to 16-bit structures by connecting OEH to OEL and connecting the 16 outputs directly to the bus instead of together.

Decode logic for the 6809μP is shown in Figure 11.

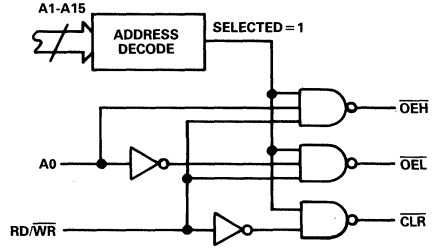
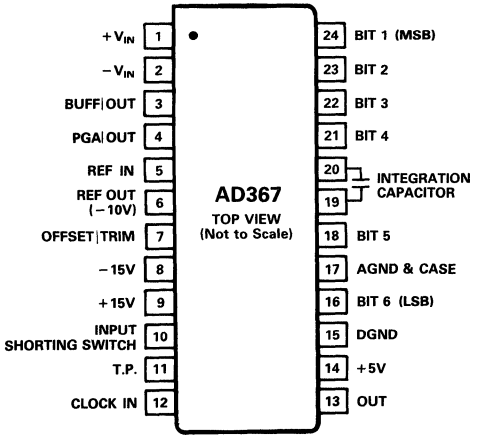


Figure 11. Decode Scheme for 6809

PIN CONFIGURATION



Complete 12-Bit A/D Converters with Programmable Gain

AD368/AD369

FEATURES

Low Cost Data Acquisition Systems Including:
- **Programmable Gain Instrumentation Amplifier**
- **Track-and-Hold Amplifier**
- **12-Bit A/D Converter**

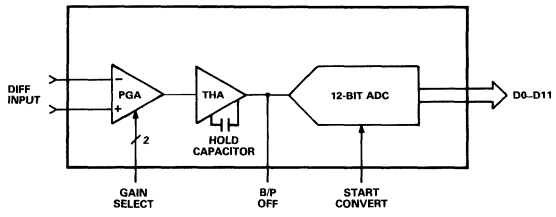
Digitally Controlled Gains:
- **AD368 Gains = 1, 8, 64, 512**
- **AD369 Gains = 1, 10, 100, 500**

50kHz Throughput Rate
Small Size: 28-Pin Hermetic Double DIP
Guaranteed No Missing Codes Over Specified Temperature
True 12-Bit Linear; Error ≤1/2LSB (B-Grade)
Unipolar or Bipolar Operation
MIL-STD-883B Screening Available

APPLICATIONS

Microprocessor Based Data Acquisition
Wide Dynamic Range Measurement Systems
Analytic and Medical Instruments
Multichannel Systems With High/Low Level Signals

AD368/AD369 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD368/AD369 are low cost, wide dynamic range data acquisition systems which condition and subsequently convert an analog signal into a 12-bit digital word. They include a programmable gain amplifier, a track-and-hold amplifier, and a 12-bit analog-to-digital converter – all in a 28-pin dual in-line package.

The digitally programmable-gain amplifier (PGA) of the AD368 enables the user to select binary-based gains of 1, 8, 64, and 512. These gain steps are especially useful in extending system dynamic range in DSP applications. The PGA of the AD369, with gains of 1, 10, 100, and 500, allows the user to choose full-scale input voltage ranges of 10V, 1V, 100mV, and 20mV, respectively. In addition, the precision differential input of the PGA provides the AD368/AD369 with excellent common-mode rejection.

The track-and-hold amplifier (T/H) features excellent linearity, low noise, and an internal hold capacitor.

The successive approximation analog-to-digital converter (ADC) features true 12-bit operation, with 0.012% max nonlinearity (B-grade). The user can select bipolar or unipolar operation to digitize both ac and dc input signals.

The AD368/AD369 provide a completely specified (industrial and military temperature ranges) and tested function in a space saving 28-pin hermetic package for system designers with cost, space, and time constraints.

9

ORDERING GUIDE

Model	Monotonic Temperature Range 10 Bits	Monotonic Temperature Range 12 Bits	Offset Temperature Drift	Units
AD368AD		−25°C to +85°C	25 + 0.2 × G	mV
AD368BD		−25°C to +85°C	10 + 0.1 × G	mV
AD368SD	−55°C to +125°C	−55°C to +85°C	25 + 0.2 × G	mV
AD369AD		−25°C to +85°C	25 + 0.2 × G	mV
AD369BD		−25°C to +85°C	10 + 0.1 × G	mV
AD369SD	−55°C to +125°C	−55°C to +125°C	25 + 0.2 × G	mV

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, +5V, R_{SPAN} = 63Ω and R(B/P) = 31Ω unless otherwise noted)

Parameter	AD368AD/SD AD369AD/SD Min	Typ	Max	AD368BD AD369BD Min	Typ	Max	Units
ANALOG INPUT							
Voltage Range, Unipolar (G = 1)	0		+10	*		*	V
Voltage Range, Bipolar (G = 1)	−5		+5	*		*	V
Common-Mode Voltage		$12-(V_{DIFF}\times G/2)$			*		V
Resistance		10^9			*		Ω
Capacitance		5			*		pF
Bias Current (I_B)		10	50		*	25	nA
I_B vs. Temperature		50			*		pA/°C
Input Offset Current (I_{OS})		2	20		*	10	nA
I_{OS} vs. Temperature		20			*		pA/°C
Noise Current (0.1 to 10Hz)		60			*		pA p-p
Output Offset Voltage (V_{OS})[1]		$5+0.02\times G$	$25+0.2\times G$		*	$10+0.1\times G$	mV
V_{OS} vs. Temperature		$70+0.2\times G$	$300+2.0\times G$		*	*	μV/°C
V_{OS} vs. Common-Mode Voltage[2]		$60+0.5\times G$	$320+3.2\times G$		*	$150+1.5\times G$	μV/V
V_{OS} vs. Supply Voltage[3]		$100+1.0\times G$	$2300+10\times G$		*	$1000+4\times G$	μV/V
Output Noise Voltage (rms)							
G = 1		250			*		μV
G = 8, 10		260			*		μV
G = 64, 100		340			*		μV
G = 512, 500		600			*		μV
DIGITAL INPUTS[4]							
V_{IH}	3.0		V_{CC}	*		*	V
V_{IL}	0.0		0.8	*		*	V
I_{IH}, I_{IL}		0.01	1.0		*	*	μA
C/S Pulse Width	50			*			ns
DIGITAL OUTPUTS, 12-BIT PARALLEL							
V_{OH} @ I_{OH} = −40μA	3.6	5.0		*	*		V
V_{OL} @ I_{OL} = 1.6mA		0.2	0.4		*	*	V
SIGNAL DYNAMICS							
Conversion Time (t_C)		12	15		*	*	μs
t_C vs. Temperature		−10			*		ns/°C
System Throughput Rate[5]							
G = 1, 8, 10			50			*	kHz
G = 64, 100			50			*	kHz
G = 512, 500			20			*	kHz
Gain Switching Time		1.5	2.0		*	*	μs
PGA Settling Time (to 1/2LSB)							
G = 1, 8, 10		8	10		*	*	μs
G = 64, 100		12	15		*	*	μs
G = 512, 500		40	50		*	*	μs
Amplifier −3dB Bandwidth							
G = 1		1000			*		kHz
G = 8, 10		400			*		kHz
G = 64, 100		150			*		kHz
G = 512, 500		40			*		kHz
T/$\overline{H}$ Acquisition Time (t_{ACQ} to 1/2LSB)			3			*	μs
T/$\overline{H}$ Aperture Delay Time (t_{AP})		140	250		*	*	ns
t_{AP} vs. Temperature		−0.3			*		ns/°C
Aperture Jitter		1			*		ns
ACCURACY							
Integral Nonlinearity		0.30	0.75		*	0.5	LSB
Differential Nonlinearity (DNL)[6]		0.30	0.90		*	0.5	LSB
Gain Error @ G = 1		0.05	0.5		*	0.2	%
@ Other Gains Referred to G = 1[7]		0.01	0.1		*	0.05	%
Gain vs. Temperature @ G = 1		3	30		*	*	ppm/°C
@ Other Gains Referred to G = 1		3	10		*	*	ppm/°C
Gain vs. Supply Voltage							
V_P ± 10%		10	30		*	*	ppm/%
V_N ± 10%		5	30		*	*	ppm/%
V_{CC} ± 10%		5	15		*	*	ppm/%

Parameter	AD368AD/SD AD369AD/SD Min	Typ	Max	AD368BD AD369BD Min	Typ	Max	Units
MONOTONIC TEMPERATURE RANGE							
12 Bits	−25		+85	−25		+85	°C
	−55 (S Grade)		+85 (S Grade)				°C
10 Bits	−55 (S Grade)		+125 (S Grade)				°C
REFERENCE							
Voltage (V_{REF})	6.28	6.30	6.32	*	*	*	V
V_{REF} vs. Temperature			20			*	ppm/°C
Internal Resistance		2			*		Ω
External Load			0.5			*	mA
POWER REQUIREMENTS							
Positive Supply Range	+13.5	15	16.5	*	*	*	V
Negative Supply Range	−13.5	−15	−16.5	*	*	*	V
Logic Supply Range	4.5	5.0	5.5	*	*	*	V
Supply Current, V_{IN} = 10V, f_C = 50kHz							
+15V		15	20		*	*	mA
−15V		30	40	*	*		mA
+5V		20	35		*	*	mA
Power Consumption		775			*		mW
THERMAL RESISTANCE (J-A)		25			*		°C/W
PACKAGE OPTION[8]							
DH-28A		AD368AD/SD AD369AD/SD			AD368BD AD369BD		

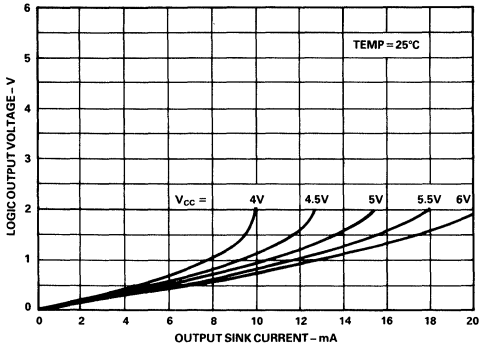
NOTES
*Same specifications as A Grade.
[1]Offset voltage applies to both bipolar and unipolar operating modes.
[2]V_{CM} = ±10V.
[3]V_S = ±10%.
[4]For digital inputs, pull-up resistors needed (typ 5kΩ) when interfacing with TTL/DTL logic.
[5]Assumes pipelining, i.e., signal is inputted to I.A. when T/H goes into hold mode, allowing voltage to settle concurrently with A/D conversion (see timing diagram).
[6]Includes T/H droop rate.
[7]This is gain error (% FS) after error at G = 1 is cancelled by adjustment. Without adjustment, total error becomes: E (Total) = E (G = 1) + E (G = 8/10, 64/100, or 512/500).
[8]See Section 14 for package outline information.
Specifications subject to change without notice.

9

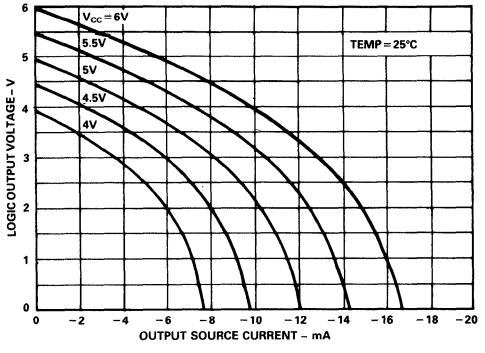
ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Positive Supply, V_P	−0.3	+17	V
Negative Supply, V_N	+0.3	−17	V
Digital-to-Analog Ground	−1	+1	V
Logic Supply	−0.3	+7	V
Analog Input (Either)	V_N	V_P	V
Analog Input Current	−10	+10	mA
Lead Soldering, 10 sec		+300	°C
Storage Temperature	−65	+150	°C

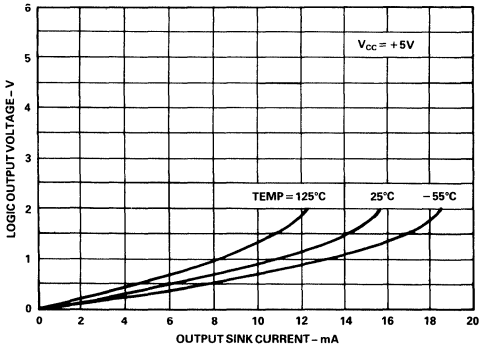
LOGIC OUTPUTS TYPICAL PERFORMANCE GRAPHS



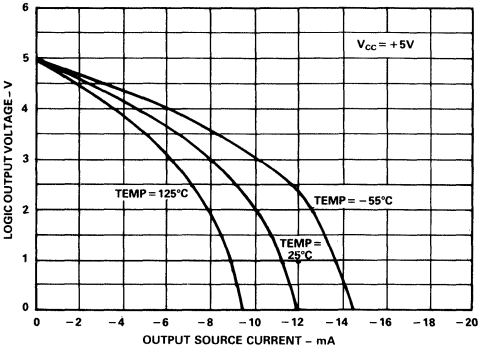
Logic Low Level Output Voltage vs. Sink Current



Logic High Level Output Voltage vs. Source Current

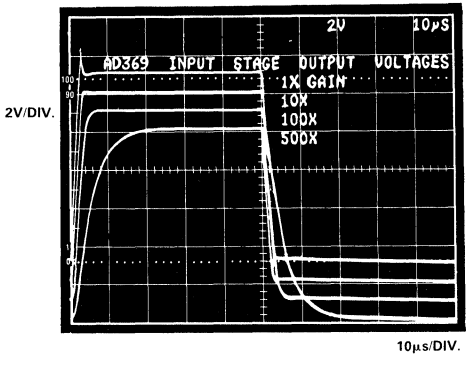


Logic Low Level Output Voltage vs. Sink Current

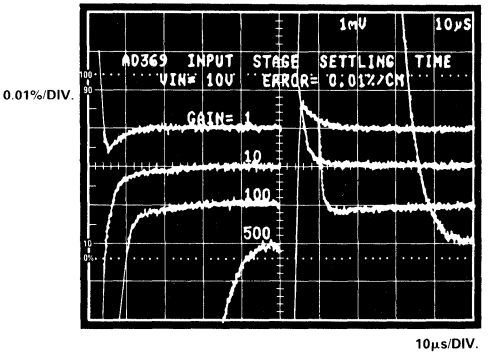


Logic High Level Output Voltage vs. Source Current

AMPLIFIER LARGE SIGNAL RESPONSE



AD369 Input Stage Output Voltage



AD369 Input Stage Settling Time

ANALOG INPUT

An analog multiplexer and resistor network form the gain switching circuit of the PGA. As shown in Table I, the user selects a gain according to the state of binary address inputs G0 and G1.

Also shown in the table is the input range data. The full-scale range of the DAS is 10V, and an LSB value is 4.8μV/4.9μV in the gain 512/500 mode; therefore, the dynamic range of the AD368/AD369 is 126dB.

The PGA uses a monolithic instrumentation amplifier, which is based on the classic three-op-amp approach. The differential analog input is amplified, according to gain selection, by two input op amps. The third amplifier, a unity gain subtractor, removes any common-mode signal and yields a single-ended output.

DATA CONVERSION

The track-and-hold amplifier is a monolithic device with an internal hold capacitor. It has an acquisition time of ≤3μs.

Input signals are digitized using a successive-approximation A/D converter. The rising (L to H) edge of the Convert Start pulse resets the internal flip-flops of the SAR. The falling (H to L) edge of the pulse initiates the conversion. After an aperture delay of 230ns, the track and hold amplifier goes into the hold mode, and the Status output goes High, indicating a conversion is in progress. Conversion time from the falling edge of the CS pulse is 15μs, maximum. A low output on the Status line indicates that the conversion is complete. The data at the output is valid at least 15ns before the Status goes low (see timing diagram). This gives sufficient setup time so that data may be latched to an external register on the falling edge of the Status pulse. The T/H amplifier returns to the tracking mode when the Status line goes low. Data is valid at the output until the next falling edge of a C/S pulse. After a maximum of 3μs acquisition time, a new C/S pulse may be issued to begin a new conversion. Timing diagrams are shown in Figure 1.

Figure 1a shows timing when a conversion sequence has first begun. All functions are being performed in series. This is the timing for the first data conversion, assuming a new gain must be selected.

The timing in Figure 1b assumes conversions are progressing continuously. After a conversion has been initiated by the falling edge of the C/S pulse, a new analog signal may be inputted to the DAS or a new gain may be selected. The figure shows that if a new gain is selected, no more than 2μs later, the new voltage begins settling at the PGA output. In the G = 512/500 mode, the determining factor for conversion speed is the amplifier settling time and, if necessary, the gain switching time. If the PGA gain is not switched, the conversion time for G = 512/500 becomes 50μs, maximum, and a minimum throughput rate of 20kHz can be achieved.

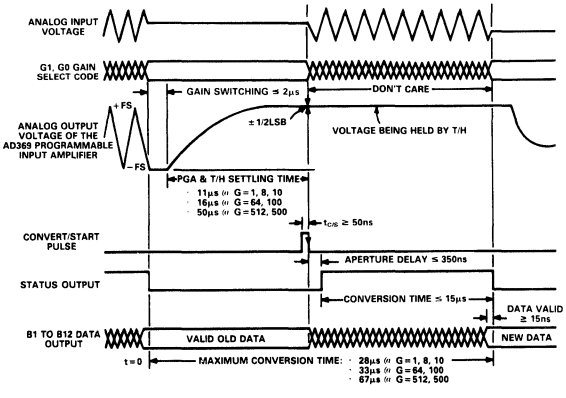


Figure 1a. AD368/AD369 Timing Diagram Without Pipelining

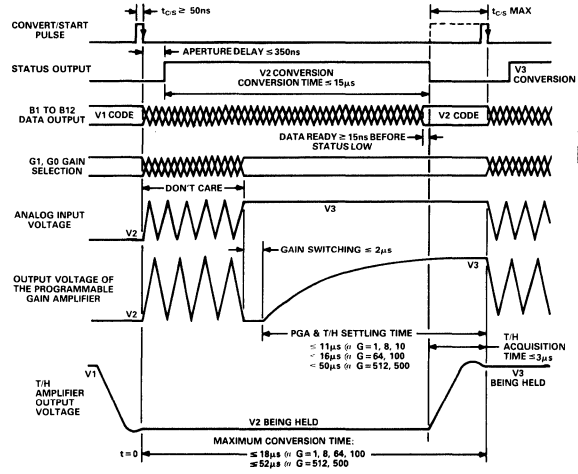


Figure 1b. AD368/AD369 Timing Diagram With Pipelining

Gain Code G1	G0	Programmable Gain Amplifier Gain	Analog Input Voltage Range Unipolar		Bipolar		One Least Significant Bit (LSB) Value
0	0	1	0	+10V	−5V	+5V	2.44mV
0	1	8, 10	0	+1.25V, +1V	−0.625V, −0.5V	+0.625V, +0.5V	0.31mV, 0.24mV
1	0	64, 100	0	+156mV, +100mV	−78mV, −50mV	+78mV, +50mV	38μV, 24μV
1	1	512, 500	0	+19.5mV, +20mV	−9.75mV, −10mV	+9.75mV, +10mV	4.8μV, 4.9μV

Table I. Input Voltage Range Selection

CALIBRATING THE AD368/AD369 WITH TRIMPOTS

This is a calibration procedure which is implemented with potentiometers, resistors, and LEDs. The hardware can be incorporated on the board which utilizes the AD368/AD369 for convenient field calibration.

The ideal transfer function of the AD368/AD369 in Figure 2 shows that the output code steps up from all ones to all zeros as the analog input voltage increases from the minus full scale limit to the plus full scale limit. The purpose of the calibration is to put the first and last bit transitions where they belong; 1LSB above −FS and 1LSB below +FS respectively.

The transfer function shows that for each output code there is an associated quantization uncertainty of 1LSB. For a given code, there is an LSB wide range of possible analog input voltages. Only at the transition point between two adjacent codes is there a precise correlation between input voltage and digital output. This circumstance must be utilized in the calibration or the accuracy may be off by ±1/2LSB.

In reality, due to noise on the analog input, the transitions do not occur as sharply as illustrated in the figure. When changing codes, the output will toggle constantly while moving from one value to the next. The desired transition point is obtained when 50% of the time the output is above this point and 50% of the time the output is below it. This transition point may be observed on an oscilloscope. Another way to measure this 50% duty cycle is by using a light emitting diode (LED) as shown in Figure 3. The duty cycle is approximately 50% when the LED is about halfway between minimum and maximum brightness.

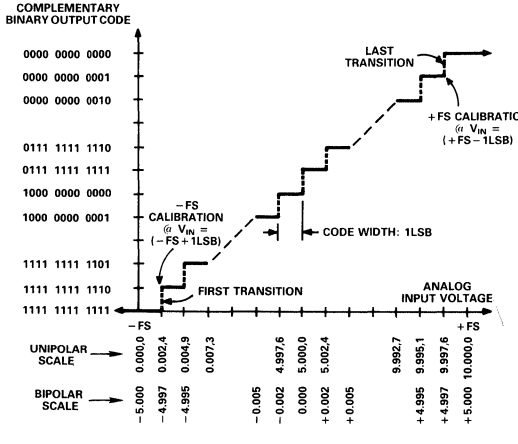


Figure 2. AD368/AD369 Transfer Function

UNIPOLAR MODE CALIBRATION

Figure 3 shows the AD368/AD369 in the unipolar mode of operation, with calibration hardware connected. The calibration begins with cancellation of the input stage offset by applying 0V to the input and manipulating R_{RTI} and R_{RTO} until the first transition occurs exactly at 0V, regardless of the amplifier gain. The next step in the calibration is to cancel the output stage offset by adjusting R_{RTO} to put the first transition at the proper input voltage of +1LSB. Finally, R_{SPAN} is adjusted and the last bit transition is put 1LSB below +FS.

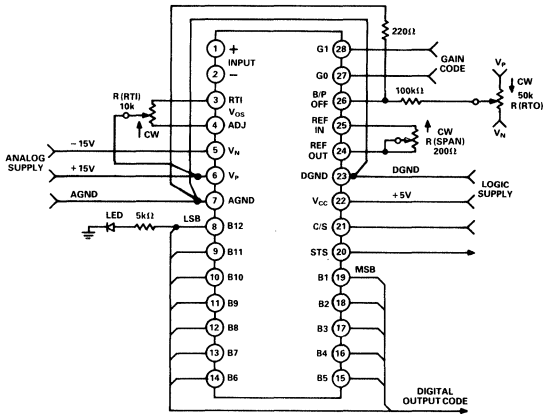


Figure 3. AD368/AD369 in the Unipolar Mode with RTI V_{OS}, RTO V_{OS} and Span Trimpots

Calibration steps for input stage offset voltage (V_{OS}) cancellation:

1. Connect the inputs to analog ground.
2. Set G=512/500 and turn R_{RTI} all the way clockwise (CW). This shifts the transfer function to the right, causing the output code to be all ones. The LED will light up.
3. Now turn R_{RTI} counterclockwise (CCW) until the LED dims to half brightness. The first transition is now positioned at the $V_{IN}=0$ line.
4. Switch to G=1 and turn R_{RTO} all the way CW. This will cause the output code to be all ones again.
5. Turn R_{RTO} CCW until the LED dims; the first transition is at 0V again.
6. Switch the gain to G=512/500, turn R_{RTI} CW just enough to assure an all ones code, then turn it CCW until the LED dims to half brightness.
7. Switch the gain back to one, turn R_{RTO} CW enough to assure an all ones code, then turn it CCW until the LED dims.
8. Repeat steps 5 and 6 until the LED brightness does not change when switching between G=1 and G=512/500. The input stage offset voltage is now zero.

Calibration steps for the output stage offset voltage (V_{OS}) cancellation:

1. Connect the inputs to a 2.44mV supply, as in Figure 4.
2. Set G=1, turn R_{RTO} all the way CW, assuring an all ones output and lighting the LED.
3. Turn R_{RTO} CCW until the LED dims to half brightness. The first transition is now 1LSB above 0V.

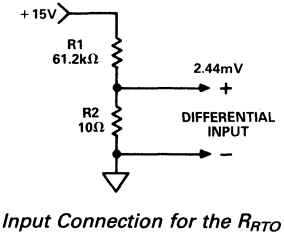


Figure 4. Input Connection for the R_{RTO} Calibration

Calibration steps for Gain Error (SPAN) cancellation:

1. Apply a precise 10V–2.44mV across the input of the AD368/AD369. A voltage divider as shown in Figure 5 can be employed; in conjunction with a precision voltmeter to verify an input of 9.997,56V.
2. Set G = 1, turn R_{SPAN} all the way CCW, assuring an output of all zeros.
3. Turn R_{SPAN} CW until the LED begins to light up (about half-brightness). At this point the last transition will be at +FS −1LSB.

The calibration in the unipolar mode is now complete.

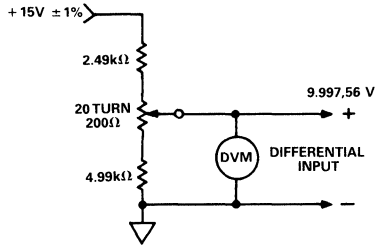


Figure 5. Input Connection for the R_{SPAN} Calibration

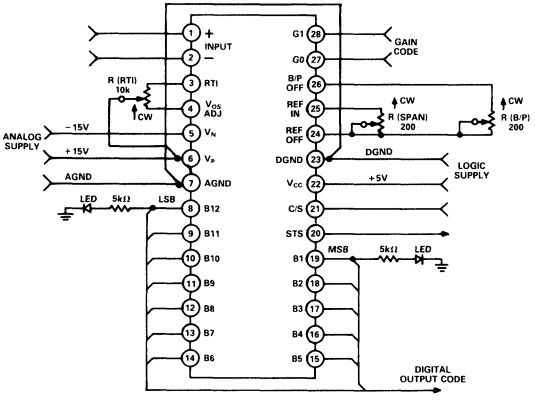


Figure 6. AD368/AD369 in the Bipolar Mode with Offset and Gain Trimpots

BIPOLAR MODE CALIBRATION

The AD368/AD369, with calibration hardware, are shown in Figure 6 for operation in the bipolar mode. The adjustments begin, as in the unipolar case, with the input stage V_{OS} cancellation. In this case however, the calibration is different because the 0V point is now at mid-scale; the MSB is used instead of the LSB. Next in the calibration is to adjust R_{RTO} and put the first LSB transition at an input voltage of −5V +1LSB. Last is the R_{SPAN} adjust to put the last bit transition 1LSB below +5V.

Input stage V_{OS} cancellation steps:

1. Connect the inputs to analog ground.
2. Select G = 512/500 and turn R_{RTI} until the MSB LED is at half-brightness.
3. Switch to G = 1 and adjust R_{RTO} until the LED is again at half-brightness.
4. Repeat steps 2. and 3. until the LED brightness does not change when gains are switched. This indicates that the input stage V_{OS} = 0V.

Output stage V_{OS} cancellation steps:

1. Set G = 1.
2. Connect the plus input to ground and the minus input to 4.997,56 volts using a voltage divider such as in Figure 7.
3. Turn R_{RTO} completely CW to assure an output code of all ones.
4. Now turn R_{RTO} CCW until the LSB LED dims to half-brightness. The first transition is now 1LSB above −FS.

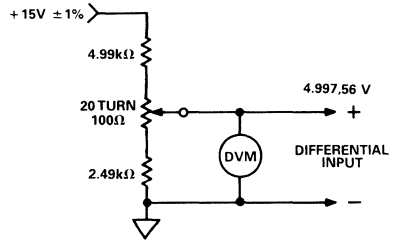


Figure 7. Voltage Divider to Derive RTO V_{OS} and Span Calibration Voltage

Gain Error cancellation steps:

1. Set G = 1.
2. Now connect the plus input to 4.997,56 Volts and the minus input to analog ground.
3. Turn R_{SPAN} completely CCW to assure an output code of all zeros.
4. Now turn R_{SPAN} CW until the LSB LED begins to light up. At this point the last bit transition will be at +FS −1LSB.

Calibration in the bipolar mode is now complete.

CALIBRATING THE AD368/AD369 WITHOUT TRIMPOTS

Figure 8 shows the AD368/AD369 in the unipolar mode with calibration hardware consisting of a Quad 8-Bit D/A Converter (AD7226) circuit instead of the previous trimpot configuration. The calibration procedure is basically the same as before except that instead of adjusting the potentiometers, three DACs are used to correct for offsets and gain error. Bipolar calibration may be accomplished by referring to Figure 6.

This calibration routine has some excellent benefits in addition to the elimination of potentiometers. Dipswitches may be used initially to set the 8-bit word values needed for each connection; however, after the word values are determined, this data may be stored into a memory (i.e., RAM) for auto-calibration in the field. The entire calibration may be accomplished under microprocessor control. Temperature offsets may be cancelled by using a temperature sensor in conjunction with a microprocessor.

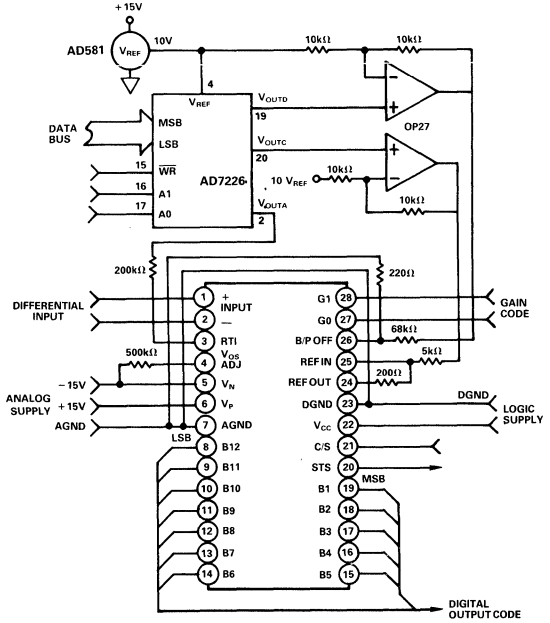


Figure 8. AD368/AD369 in the Unipolar Mode with D/A Circuit Replacing Trimpots

INPUT PROTECTION

There are two considerations when applying input protection for the PGA: 1) that maximum input current must be limited to less than 20mA and 2) that input voltages must not exceed the supplies. Outside the linear operating range, the input impedance of the AD368/AD369 becomes low and nonlinear due to the input transistors going into saturation. The graph in Figure 9 illustrates the input current vs. differential input voltage relationship without input protection.

Resistors of 1kΩ in series with each input would keep the currents within safe limits for input voltages in the range of $V_P = +15V$ to $V_N = -15V$. Figure 10 shows the external components necessary to protect the AD368/AD369 under all overload conditions at any gain. The diodes to the supplies are necessary if input voltages outside of the range of the supplies are encountered.

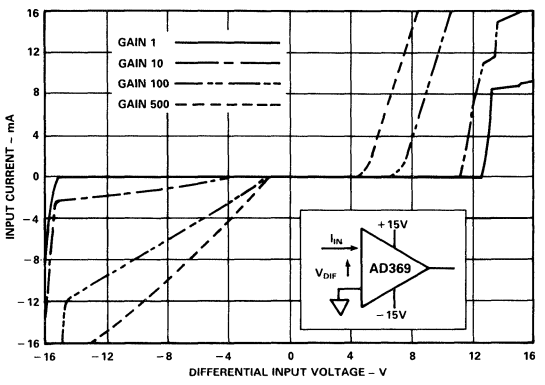


Figure 9. Input Current vs. Differential Input Voltage Without Input Protection

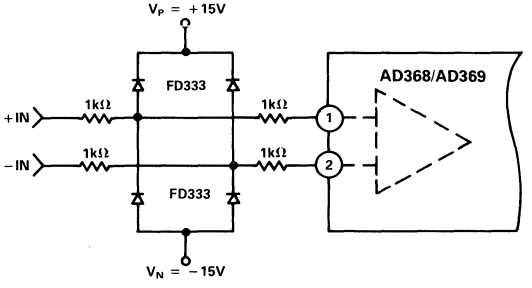


Figure 10. Input Protection Circuit for AD368/AD369

The equivalent noise resistance of the AD368/AD369 input stage is only 1kΩ. Input protection resistors, however, will quickly degrade this excellent noise performance. To reduce the noise encountered with added resistors, FETs may be used to limit the input current. FETs, such as the 2N4416, with low I_{DSS} and low on-resistance should be used. Figure 11 shows the protection circuit and Figure 12 shows the input current vs. the differential input voltage with the FET protection circuit. The 20kΩ resistor is put in series with the gate to limit the "reverse" I_{DSS} current and does not add to the noise.

The above input protection circuits also protect the AD368/AD369 in case there is a voltage applied to the input while the supplies are shut off.

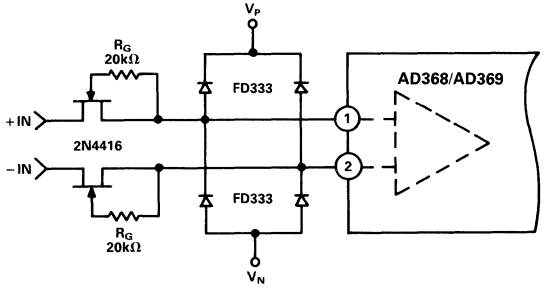


Figure 11. Low Noise Input Protection Circuit for AD368/AD369

If using multiplexers, proper device selection can provide AD368/AD369 input protection. Some MUXes limit the maximum current as well as the maximum output voltage to safe levels. Keep in mind that the on resistance of the MUX will add to the input stage noise.

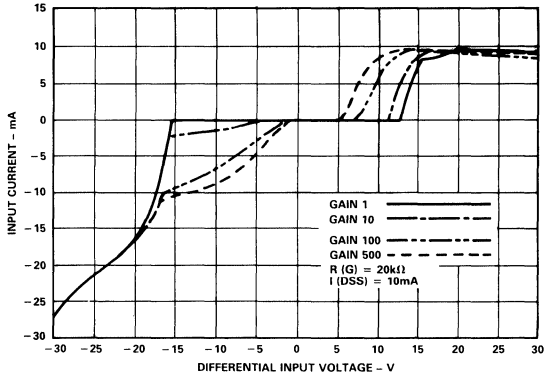


Figure 12. AD625 Input Protection with 2N4416 FETs and FD333 Clamping Diodes

GROUND RETURNS FOR INPUT BIAS CURRENTS

There must be a direct return path for the input bias currents of the PGA input transistors; otherwise, they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying floating input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 13.

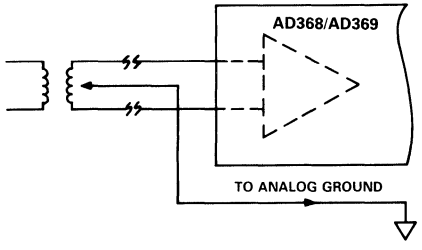


Figure 13a. Ground Returns for Bias Currents with Transformer Coupled Input

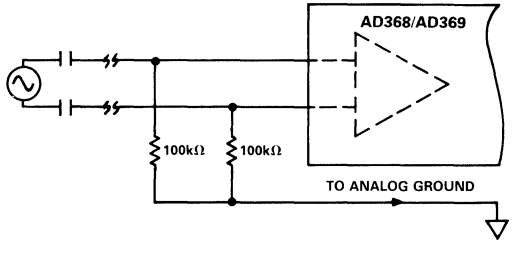


Figure 13b. Ground Returns for Bias Currents with ac Coupled Inputs

GROUND CONNECTIONS

The digital and analog ground pins of the AD368/AD369 should be tied together as close to the package as possible to avoid noise coupling from the digital ground to the analog circuit. When an application calls for separate grounding entirely, a 0.1μF capacitor should be connected between the AGND and DGND pins to filter out any noise.

POWER SUPPLY DECOUPLING

Each of the AD368/AD369 supply terminals should be capacitively decoupled as close to the IC as possible. A 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are decoupled to the analog ground pin and the Logic supply is decoupled to the digital ground pin.

TRACK-AND-HOLD ERRORS

The aperture delay time is the time required for the track-and-hold amplifier to switch from track to hold. Since this is effectively a constant, it may be tuned out by advancing the track-to-hold command with respect to the input signal.

Unlike the aperture delay time, aperture jitter is a true error source and must be considered. Aperture jitter is a result of noise within the switching network. It causes variations in the value of the analog input being held. The aperture error which results from this jitter is directly related to the dV/dT of the analog input and may limit the signal bandwidth. The aperture jitter of the T/H in the AD368/AD369, however, is small enough that the instrumentation amplifier will limit the signal frequency well below the frequency at which the jitter error would be of concern.

Droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major contributors are switch leakage current and bias current. This dV_{OUT}/dT is equal to the ratio of the total leakage current, I_l to the hold capacitance, C_H. The droop rate of the T/H in the AD368/AD369 is included in the differential nonlinearity specification.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change. Care should be taken to assure that both input lines are balanced with regard to parasitic capacitances and source resistances; otherwise, the excellent common-mode rejection of the AD368/AD369 will be degraded.

ERRORS DUE TO BANDWIDTH LIMITATIONS OF THE AD368/AD369

When using the AD368/AD369 to digitize sine-wave signals, it is important to know the frequency at which the system response roll-off will cause an error of 1/2LSB.

The ratio of output to input voltage for the instrumentation amplifier of the AD368/AD369 is:

$$| V_O/V_I | = G/ | (1+jf/f_a) | = G/[1+(f/f_a)^2]^{0.5}$$

where f_a equals the −3dB bandwidth and a single-pole roll-off is assumed.

It can be shown that the V_O/V_I ratio will have an error of 1/2LSB for a 12-bit A/D converter when:

$$f(1/2LSB) = f_a/\sqrt{2^{12}} = f_a/64.$$

The instrumentation amplifier will have reached the limit of 12-bit precision for signal frequencies of $f_a/64$. The frequency can be doubled at the expense of two bits of accuracy.

The frequency at which the amplitude of a 10V p-p sine wave is reduced by one half of an LSB is typically 10kHz, 3.5kHz, 1.7kHz, and 0.5kHz at gains of 1, 10, 100, and 500 respectively.

NOISE CONSIDERATIONS

Assuming normally distributed or white noise, the rms noise voltage E_n of a system is a function of its noise bandwidth BW_N. The correlation between −3dB bandwidth (BW) and BW_N is dependant upon the frequency response of the system under consideration.[1] For a 6dB/octave filter, the ratio is $\pi/2 = 1.57$. For a "brick wall" filter it is one. The noise correlation is simply: $E_N = e_N\sqrt{BW_N}$, where e_N is the noise density ($nV/\sqrt{Hz}$).

The noise of the input signal must also be added to the noise of the DAS. Again, in calculating the rms noise contribution of the signal, the BW_N of the source must be considered. If not filter limited before the AD368/AD369 input, the BW_N of the PGA, as stated above, must be used, which is about $\pi/2$ times its −3dB bandwidth.

Input protection resistors will also contribute to the total system noise. The rms noise voltage of a 1kΩ resistor over a noise bandwidth of 1Hz is 4nV. So, the noise voltage of a resistor, R(kΩ) and a noise bandwidth, BW_N(Hz) is: $E_N(R) = 4nV\sqrt{R \times BW_N}$.

The total system rms noise is given by the equation:

$$E_N(\text{system}) = \sqrt{E_N(AD369)^2 + [G \times E_N(R_{IN})]^2 + [G \times E_N(\text{sig})]^2}$$

Once the system rms noise value is known, the probability of the peak-to-peak value of the noise exceeding an LSB is given in Table II.

LSB/E_N	Probability of Noise Exceeding 1LSB
1.0	62.0%
2.0	32.0%
3.0	13.0%
4.0	4.6%
5.0	1.2%
5.15	1.0%
6.0	0.27%
6.6	0.10%

Table II.

[1]See "Low Noise Electronic Design," by C. D. Motchenbacher, F. C. Fitchen.

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a voltage known as the "Seebeck" or thermocouple emf is generated when the two junctions are at different temperatures. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV/°C). This means that care must be taken to insure that all connections in the input circuit of the AD368/AD369 remain isothermal. In addition, the user should also avoid air currents over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise.

The base emitter junction of an input transistor can rectify out-of-band signals (i.e., RF interference). These rectified voltages act as small dc offset errors. In the case of a resistive transducer, a small capacitor (e.g. 150pF) across the input working against the internal resistance of the transducer may suffice to provide an RC filter without affecting system bandwidth. Again, every effort should be made to match the capacitance at Pins 1 and 2, to preserve CMR.

ANALOG DEVICES

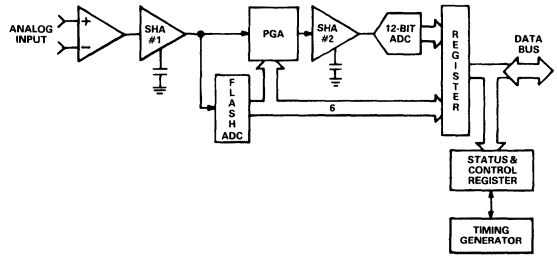
18-Bit Floating Point Data Acquisition System

AD1330

FEATURES
18-Bit Dynamic Range
12-Bit Significand
6-Bit Normalization
100 kHz Conversion Rate
Sample-and-Hold Included
Status Word

APPLICATIONS
Sonar Signal Processing
Vibration Analysis
PC Data Acquisition
Medical Instrumentation
General Purpose DSP

AD1330 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1330 is an 18-bit Floating Point Data Acquisition System. The device will digitize signals up to 50 kHz, at conversion rates up to 100 kHz. The output word format consists of an 18-bit word expressed as a 12-bit 2s complement significand and a 6-bit normalization term. The device offers 12-bits of resolution and 18-bits of dynamic range.

The AD1330 incorporates all of the necessary circuitry to acquire, hold and digitize the input signal, and output a digital representation. A complete AD1330 consists of two hybrids, one a 32-pin and the other a 48-pin. The 32-pin hybrid contains the "front end" or Analog Input Section (AIS), while the 48-pin package contains the "back-end" or Conversion & Control Section (CCS).

The analog input section consists of: differential amplifier, sample-and-hold and programmable gain amplifier. The differential amplifier and sample-and-hold have been optimized for low noise, low harmonic distortion and wide dynamic range. The differential amplifier provides optional ground sensing. Ground sensing is enabled by connecting the sense input to analog ground at the signal source. In addition, the user may select whether to bypass the differential amplifier since the input and output connections are made available at the package pins. Operation of the sample-and-hold is via the SHA1H-L and SHA1S-L signals which are internally generated by the control logic. The SHA is compensated for droop, distortion and feedthrough. The PGA incorporates an auto-zero loop to remove dc offsets. The auto-zero loop is enabled by connecting the auto-zero out to PGA in. All control signals to the PGA-AUTOZ-L, SHORT-L and GAIN-L through GAIN64-L are generated by the control logic.

The CCS contains a 7-bit flash ADC, a second SHA, 12-bit ADC, control logic and bus interface logic. The flash ADC generates the first conversion product (normalization constant) which in turn is used to set the gain of the PGA. The SHA is used to pipeline the analog input and to hold it for conversion by the successive approximation 12-bit ADC. The congrol logic generates all of the required timing and control signals to the AIS and CCS. The bus interface circuitry (BI) provides a high speed interface to a 16-bit data bus. The AD1330 generates an interrupt signal which may be used to initiate a read cycle. Reading of output data clears the interrupt; otherwise the interrupt is automatically cleared and output data is updated after 4.8 microseconds.

On each conversion cycle there are three output words available from the AD1330. The first two contain the ADC and normalization outputs; the third contains the status world. A complete result is obtained by multiplying (or scaling) the ADC result by the normalization constant.

The AD1330 has four operating modes: auto gain, fixed gain, forced gain and autocalibrate. In auto gain mode the PGA gain is set during each conversion cycle according to the result from the flash ADC. This process maximizes the amplitude of the signal presented to the 12-bit ADC thereby optimizing the resolution and accuracy of the conversion process. The fixed gain mode holds the last gain setting and inhibits any further updates to the PGA. The forced gain mode allows the user to set a specific gain via the data bus. In autocalibrate, the AD1330 corrects for any offset voltages in the second SHA and 12-bit ADC. Mode selection should be made immediately after reading the previous result. Changing modes before readback may overwrite the output data and is not recommended. Autocalibrate takes 10 microseconds, and one such cycle is initiated on powerup and at any time RST-L is asserted.

9

Complete 12-Bit Sampling A/D Converter for Digital Signal Processing

AD1332

FEATURES

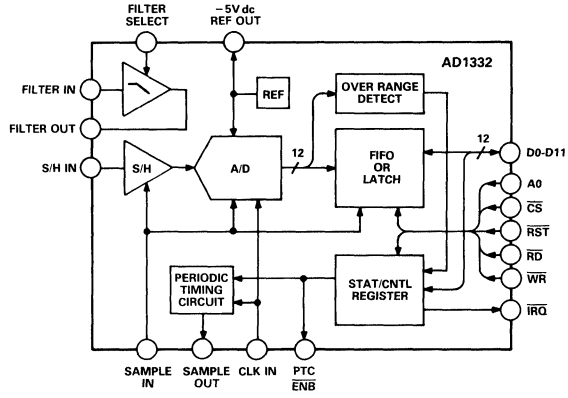
Complete A/D System for DSP Includes:
- **4th Order Antialiasing Filter**
- **12-Bit Sampling A/D Converter**
- **32-Word FIFO Memory**
- **Fully Asynchronous, High Speed Digital Interface**

Sample Rate up to 125kHz
Entire System is Dynamically Specified
15ns Data Access Time Allows "No Wait State" Interface to: ADSP-2100 (A), TMS320C25 DSP56000, NECμPD77230

APPLICATIONS

Sonar Signal Processing
Vibration Analysis
Ultrasound Imaging
PC Data Acquisition
High Speed Modems
Motion Control
Speech Processing

AD1332 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1332 is a complete, 12-bit A/D converter system optimized for use in high speed digital signal processing (DSP) applications. The device consists of a fourth order antialiasing filter, a 12-bit sampling A/D, a fully asynchronous high speed digital interface and a 32-word FIFO memory. The AD1332 is manufactured using highly reliable advanced hybrid circuit assembly techniques and is packaged in a 40-pin hermetic DIP.

The antialiasing filter is an active four-pole Butterworth. Cut-off frequencies (f_C) are user-selectable (capacitor programmable), and operation is specified for f_C up to 50kHz. The filter may be bypassed entirely if desired.

The 12-bit sampling A/D converter can convert ±5V full-scale signals at sample rates up to 125kHz. The rate is programmable by means of a single external clock. The entire converter system is specified and tested for signal-to-noise ratio and total harmonic distortion.

The digital interface provides a true asynchronous link between the A/D and a high speed microprocessor. Data transfer is controlled by generating an interrupt signal when data is available. Interrupts can be generated when the FIFO is full (32 words), half-full (16 words), or when a single word of data is ready (FIFO bypassed). In addition, the AD1332 can generate an interrupt signal when the A/D conversion results are overrange.

The AD1332 provides a completely specified and tested system that bridges the interface and specification gap between A/D converters and high speed DSP.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, V_{DD} = +5V, unless otherwise noted)

Parameter	AD1332BD Min	Typ	Max	Units
FILTER (C1–C4 = 500pF ±1%)				
Input Impedance	8	10		kΩ
Voltage Range	±10			V
Output Voltage Range $R_L \geq 4k$	±10			V
Corner Frequency, Accuracy		±2		%
Drift		±0.01		%/°C
Gain[1] @ dc	−0.05		+0.05	dB
$0.8f_C$	−1		+1	dB
f_C		−3		dB
$4f_C$		−48	−45	dB
$10f_C$		−76		dB
Settling Time to 0.01%, 10V Step		100	125	µs
Offset		±2	±5	mV
Drift		±20	±100	µV/°C
Noise		75		µV rms
SAMPLING A/D CONVERTER[2]				
Input Impedance	4	5		kΩ
Voltage Range		−5 to +5		V
Output Coding		Offset Binary		
CLK IN Frequency	0.5		2.5	MHz
High Time	200			ns
Low Time	200			ns
Sampling Rate (f_S)			125	kHz
S/H				
Acquisition Time			2.8	µs
Droop Rate		0.5	1.0	mV/ms
Over Temperature		Doubles Every 10°C		
Aperture Delay Time		35		ns
Static Characteristics				
Integral Nonlinearity		±1/2	±1	LSB
Over Temperature			±1	LSB
Resolution for No Missing Codes	12			Bits
Over Temperature	12			Bits
− Full-Scale Error		±1	±2	LSB
Over Temperature		±2	±8	LSB
+ Full-Scale Error		±1	±2	LSB
Over Temperature		±2	±8	LSB
PSRR, $\pm V_S$		±2	±6	LSB
Dynamic Characteristics[1,3]				
With Filter (f_C = 50kHz)				
Signal-to-Noise Ratio, f_{IN} = 38.7kHz	70	72		dB
Total Harmonic Distortion, f_{IN} = 38.7kHz		−82	−72	dB
Intermodulation Distortion, f_{IN1} = 32.8kHz & f_{IN2} = 34.3kHz		−82	−72	dB
Without Filter				
Signal-to-Noise Ratio, f_{IN} = 60.9kHz	70	72		dB
Total Harmonic Distortion, f_{IN} = 60.9kHz		−78	−68	dB
Intermodulation Distortion, f_{IN1} = 58.7kHz & f_{IN2} = 60.9kHz		−78	−68	dB
Reference Voltage	−5.05		−4.95	V
Output Current	±1	±2		mA
Drift		±5	±25	ppm/°C

Parameter	AD1332BD Min	Typ	Max	Units
DIGITAL INPUTS[1]				
$\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{RST}$, A0, D0–D11, PTC $\overline{ENB}$				
Input Voltage, Logic Low			+0.8	V
Input Voltage, Logic High	+2.0			V
Input Current			±200	μA
SAMPLE IN, CLK IN				
Input Voltage, Logic Low			+1.5	V
Input Voltage, Logic High	+3.5			V
Input Current			±10	μA
Input Capacitance		5		pF
$\overline{RST}$ LOW Pulse Width	10			ns
DIGITAL OUTPUTS[1]				
D0–D11, SAMPLE OUT				
Output Voltage, Logic Low, I_{OL} = 4mA			+0.4	V
Output Voltage, Logic High				
D0–D11, I_{OH} = −4mA	+2.4			V
SAMPLE OUT, I_{OH} = −0.4mA	+4.0			
High Impedance Leakage Current			±10	μA
$\overline{IRQ}$, PTC $\overline{ENB}$				
Output Voltage, Logic Low I_{OL} = 4mA			+0.4	V
Off-State Leakage			±10	μA
Output Capacitance		5		pF
$\overline{IRQ}$ LOW to D0–D11 Valid[4]			0	ns
POWER REQUIREMENTS				
Operating Range				
$\pm V_S$	±11.4		±15.75	V
V_{DD}	+4.75		+5.25	V
$+V_S$ Supply Current		47	66	mA
$-V_S$ Supply Current		46	65	mA
$+V_{DD}$ Supply Current		2	5	mA
Consumption				
$\pm V_S$ = ±12V		1.2	1.4	W
$\pm V_S$ = ±15V		1.5	1.75	W
TEMPERATURE RANGE				
Operating and Specified	−40		+85	°C
Storage	−65		+150	°C

NOTES
[1]Guaranteed over operating temperature range, tested at +25°C only.
[2]f_{CLK} = 2.5MHz, SAMPLE IN connected to SAMPLE OUT, PTC $\overline{ENB}$ = Low.
[3]THD of harmonics 2-7 of the fundamental. SNR of fundamental less harmonics 2-7.
[4]$\overline{RD}$, $\overline{CS}$, AO = "Low;" $\overline{WR}$, $\overline{RST}$ = "High."

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units.
All other specifications are guaranteed but not tested.

SWITCHING CHARACTERISTICS (over operating temperature and power supply voltage range, with C_{OUT} = 30pF or 100pF except where noted)

Parameter	Description	Conditions	Min	Max	Units
READ CYCLE					
t_{RC}	Read Cycle Time	C_{OUT} = 30pF	25		ns
		C_{OUT} = 100pF	35		ns
t_A	Data Access Time	C_{OUT} = 30pF		15	ns
		C_{OUT} = 100pF		25	ns
		C_{OUT} = 150pF		30	ns
t_{LZ}	Output Low Z Time		2		ns
t_{HZ}	Output High Z Time	C_{OUT} = 30pF		15	ns
		C_{OUT} = 100pF		25	ns
t_{OH}	Output Hold Time		2		ns
t_{AORD}	A0 Valid to $\overline{RD}$ LOW		3		ns
t_{RDAO}	$\overline{RD}$ HIGH to A0 Invalid		3		ns
t_{AOCS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSAO}	$\overline{CS}$ HIGH to A0 Invalid		3		ns
WRITE CYCLE					
t_{WC}	Write Cycle Time		15		ns
t_{WP}	Write Pulse Width		5		ns
t_{SU}	Data Setup Time		2		ns
t_{IH}	Input Hold Time		3		ns
t_{AOWR}	A0 Valid to $\overline{WR}$ LOW		3		ns
t_{WRAO}	$\overline{WR}$ HIGH to A0 Invalid		3		ns
t_{AOCS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSAO}	$\overline{CS}$ HIGH to A0 Invalid		3		ns

NOTE
Specifications subject to change without notice.
Specifications are guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +17V
$-V_S$ to APWR/ASIG GND . . . . . −17V
V_{DD} to DGND . . . . . +7V
APWR/ASIG GND to DGND . . . . . −0.3V to +0.3V
Analog Input to APWR/ASIG GND
S/H IN, FILTER IN, C1vg-C4vg . . . . . $-V_S$ to $+V_S$
Digital Input to APWR GND
SAMPLE IN, CLK IN . . . . . −0.3V to +7V
Digital Input to DGND
D0-D11, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, $\overline{RST}$,
PTC $\overline{ENB}$ . . . . . −0.3V to V_{DD} +0.3V
Output Short Circuit Duration
FILTER OUT, REF OUT or C1wv-C4wv . . . . Indefinite
Digital Output . . . . . 1 Output for 1sec
Lead Temperature Range,
Soldering for 10sec . . . . . +300°C

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

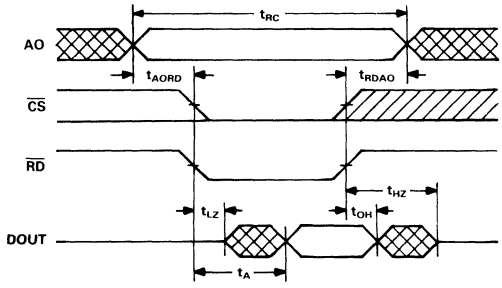
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

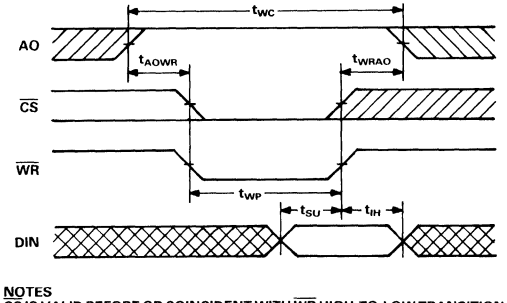
Model	Temperature Range	Package Option*
AD1332BD	−40°C to +85°C	DH-40A
AD1332TD/883B	−55°C to +125°C	DH-40A

*See Section 14 for package outline information.



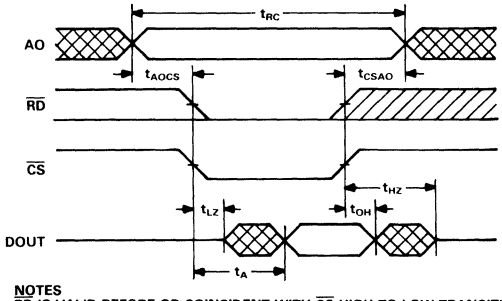
NOTES
CS IS VALID BEFORE OR COINCIDENT WITH RD HIGH-TO-LOW TRANSITION.
CS IS INVALID AFTER OR COINCIDENT WITH RD LOW-TO-HIGH TRANSITION.
WR IS NOT ACTIVE DURING READ CYCLE.

Figure 1a. Timing Waveform for Read Cycle No.1 (RD Controlled)



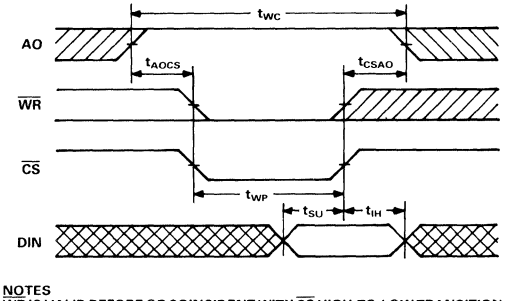
NOTES
CS IS VALID BEFORE OR COINCIDENT WITH WR HIGH-TO-LOW TRANSITION.
CS IS INVALID AFTER OR COINCIDENT WITH WR LOW-TO-HIGH TRANSITION.
RD IS NOT ACTIVE DURING WRITE CYCLE.

Figure 2a. Timing Waveform for Write Cycle No. 1 (WR Controlled)



NOTES
RD IS VALID BEFORE OR COINCIDENT WITH CS HIGH-TO-LOW TRANSITION.
RD IS INVALID AFTER OR COINCIDENT WITH CS LOW-TO-HIGH TRANSITION.
WR IS NOT ACTIVE DURING READ CYCLE.

Figure 1b. Timing Waveform for Read Cycle No. 2 (CS Controlled)



NOTES
WR IS VALID BEFORE OR COINCIDENT WITH CS HIGH-TO-LOW TRANSITION.
WR IS INVALID AFTER OR COINCIDENT WITH CS LOW-TO-HIGH TRANSITION.
RD IS NOT ACTIVE DURING WRITE CYCLE.

Figure 2b. Timing Waveform for Write Cycle No. 2 (CS Controlled)

9

AC TEST CONDITIONS

Input Pulse Levels	DGND to +3.0V
Input Rise/Fall Times	<5ns
Timing Reference Levels	
Inputs	1.5V
Outputs	
LOW	0.4V
HIGH	2.4V
Enabled to LOW	$V_T - 0.1V$
Enabled to HIGH	$V_T + 0.1V$
Disabled from LOW	$V_{OL} + 0.5V$
Disabled from HIGH	$V_{OH} - 0.5V$

$V_T = 1.5V$, the voltage to which 3-stated outputs are forced.

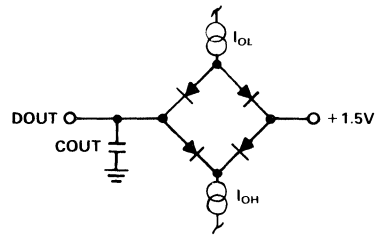


Figure 3. Output Load

Typical Characteristics

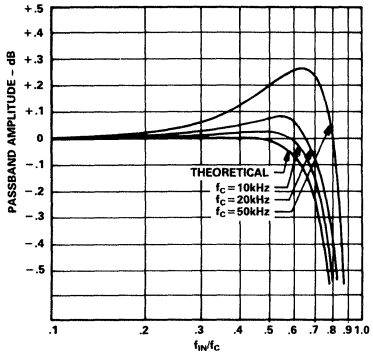


Figure 4. Filter Passband Response Normalized to the Cutoff Frequency

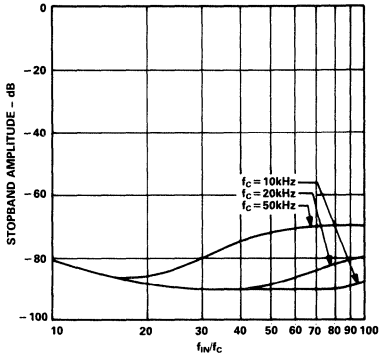


Figure 5. Filter Stopband Response Normalized to the Cutoff Frequency

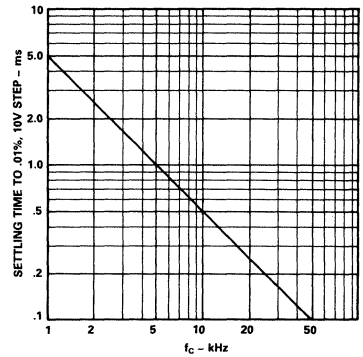


Figure 6. Filter Settling Time to 0.01% vs. Cutoff Frequency

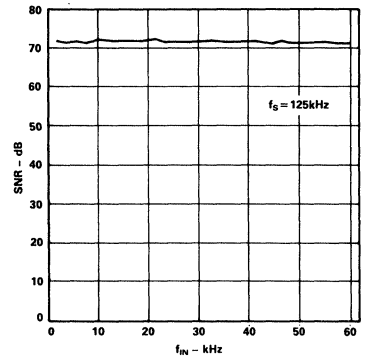


Figure 7. A/D SNR vs. Frequency

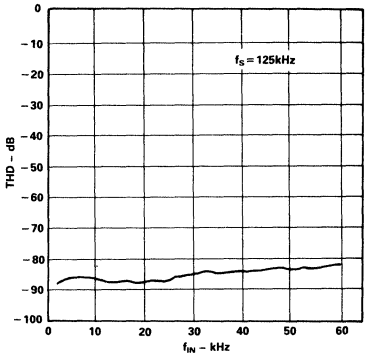


Figure 8. A/D THD vs. Frequency

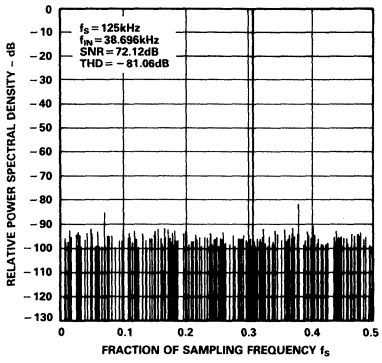


Figure 9. Filter & A/D Spectral Response

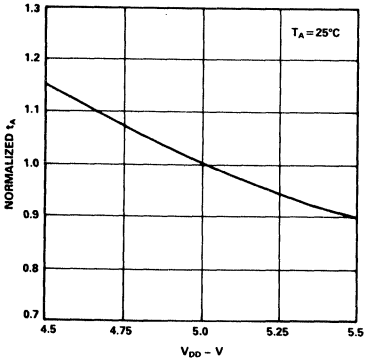


Figure 10. Normalized Data Access Time vs. V_{DD}

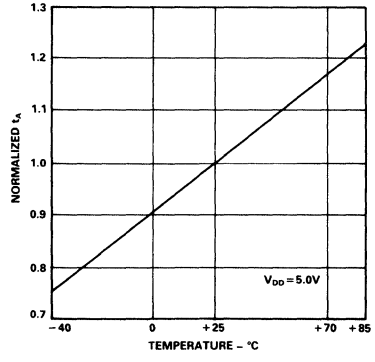


Figure 11. Normalized Data Access Time vs. Temperature

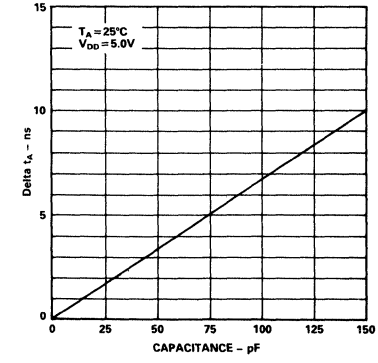
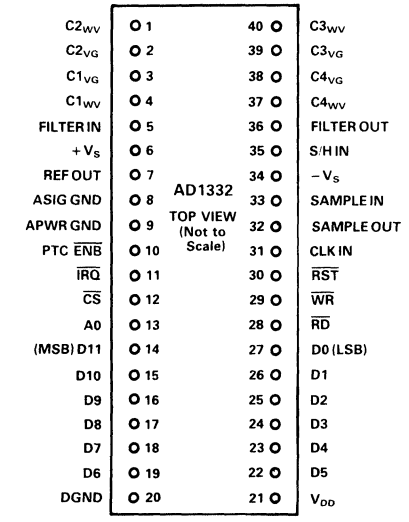


Figure 12. Change in Data Access Time vs. Loading

PIN CONFIGURATION



PIN DESCRIPTIONS

Pin	Mnemonic	Function
3, 4	C1vg, C1wv	Pins where 4 equal value capacitors are added to set filter corner.
2, 1	C2vg, C2wv	Frequency f_C according to:
39, 40	C3vg, C3wv	
38, 37	C4vg, C4wv	$f_C = 25\text{kHz} \div C$, C in nF
5	FILTER IN	Filter input.
36	FILTER OUT	Filter output.
35	S/H IN	Sample and hold analog input.
8	ASIG GND	Analog signal ground.
7	REF OUT	−5V reference output.
6, 34	$+V_S$, $-V_S$	Analog power supplies.
9	APWR GND	Analog power ground.
31	CLK IN	External clock input to the A/D converter and the Periodic Timing Circuit.
32	SAMPLE OUT	Periodic Timing Circuit output. Connection to SAMPLE IN sets sample rate at $f_{CLK} \div 20$.
33	SAMPLE IN	S/H and A/D converter control input.
10	PTC $\overline{\text{ENB}}$	Input and (open-drain) output used to enable periodic timing externally or through μP interface.
11	$\overline{\text{IRQ}}$	Open drain interrupt request. User programmable to become active on any of the following conditions: One A/D conversion result available; FIFO half full or full; A/D conversion results overrange.
12	$\overline{\text{CS}}$	Chip select input.
13	A0	Address bit zero. Selects data path from FIFO/latch (low) or from/to Status/Control register (high).
27-22	D0-D5	Bidirectional 3-state data lines. D11 is A/D converter MSB when D0–D11 are outputs.
19-14	D6-D11	D7 is Status/Control register MSB.
28	$\overline{\text{RD}}$	Read control input (D0–D11).
29	$\overline{\text{WR}}$	Write control input (D0–D7).
30	$\overline{\text{RST}}$	Reset. In reset state, FIFO is transparent & overrange detector is disabled.
20, 21	DGND, V_{DD}	Digital power supply.

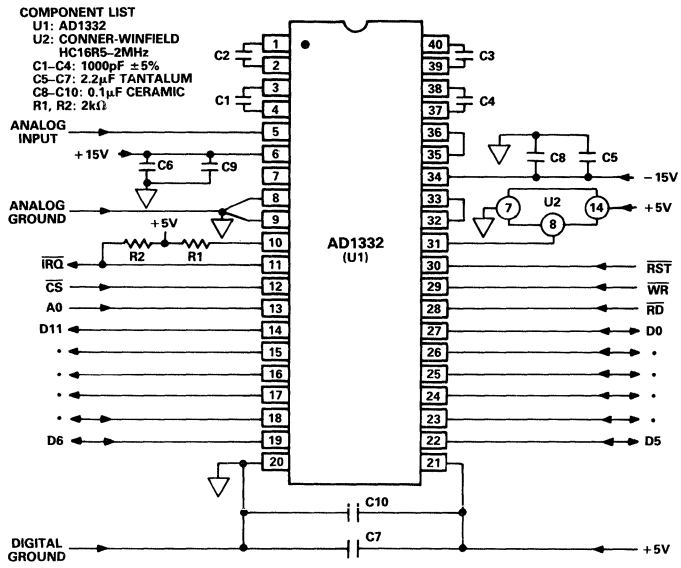


Figure 13. Typical Interface Circuit (f_C = 25kHz, f_S = 100kHz)

CONTROL AND STATUS REGISTER DESCRIPTIONS

Control

Bit→	7	6	5	4	3	2	1	0
	PTCEN	$\overline{L}$/F	$\overline{HF}$/F	ORNG	X	X	X	X

Bit	Mnemonic	Function
7	PTCEN	A "0" in this bit position will disable the periodic timing circuit. A "1" in this bit position will enable the periodic timing circuit.
6	$\overline{L}$/F	A "0" in this bit position will reset the FIFO and enable the transparent latch. $\overline{IRQ}$ will become active on the completion of an A/D conversion cycle. $\overline{IRQ}$ will become inactive on the start of the next A/D conversion cycle. A "1" in this bit position will enable the FIFO and activate $\overline{IRQ}$ when the FIFO is half full or full (depending on CBIT 5). $\overline{IRQ}$ will become inactive on the start of the next A/D conversion cycle or when the FIFO is read from.
5	$\overline{HF}$/F	A "0" in this bit position will cause $\overline{IRQ}$ to become active when the 16th word is shifted into the FIFO (if the FIFO is enabled). A "1" in this bit position will cause $\overline{IRQ}$ to become active when the 32nd word is shifted into the FIFO (if the FIFO is enabled).
4	ORNG	A "0" in this bit position will disable the overrange interrupt capability. A "1" in this bit position will activate $\overline{IRQ}$ if overranged (all "0"s or all "1"s) data is shifted into the FIFO. $\overline{IRQ}$ will become inactive when this bit is reset to "0."
3-0	X	Not defined.

Status

Bit→	7	6	5	4	3	2	1	0
	FLAG	DATA	ORUN	ORNG	X	X	X	X

Bit	Mnemonic	Function
7	FLAG	Logical OR of status Bits 4 & 6.
6	DATA	Set if $\overline{IRQ}$ becomes active because data is available. Reset when FIFO is read from if FIFO used. Reset when $\overline{IRQ}$ becomes inactive if latch is used.
5	ORUN	Set when FIFO has overrun. Reset by control Bit 6.
4	ORNG	Set if $\overline{IRQ}$ became active because of overrange condition. Reset by control Bit 4.
3-0	X	Not defined.

DISCUSSION

General

The AD1332 is a complete solution for sampling and quantifying signals in the audio bandwidth and provides a direct parallel interface to a high speed microprocessor for digital signal processing (DSP). A block diagram of the AD1332 is shown on page 1.

DSP is the mathematical manipulation of dynamic signals which have been represented in numerical form. To successfully process a signal, the signal must be sampled and quantified such that accuracy is preserved and aliasing is avoided. The AD1332 provides this capability by enabling the user to coordinate its antialiasing filter cutoff frequency with the converter sample rate, completely independent from the DSP processor speed.

Sampled Data Systems

The process of sampling a continuous-time signal x(t) at a sample rate f_S causes a periodic replication in the frequency domain of the continuous time Fourier transform (CTFT) x(f) of the original signal about integer multiples of f_S. If the sample rate is selected too low for the bandwidth of x(t), the replicated transforms will overlap with adjacent transforms as illustrated in Figure 14b. This overlap is known as frequency aliasing and will cause distortion if the samples are used in an attempt to reconstruct the original time signal.

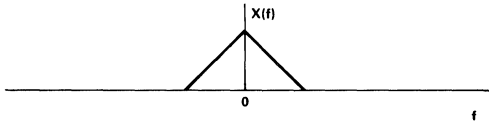


Figure 14a. Original Continuous-Time Fourier Transform (CTFT) or x(t)

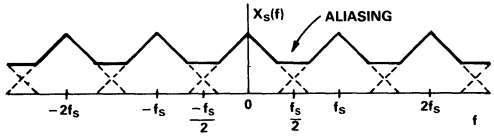


Figure 14b. Sampling Produces Aliased Replications of x(f)

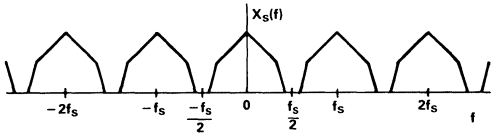


Figure 14c. Replications of x(f) when x(t) is Band Limited

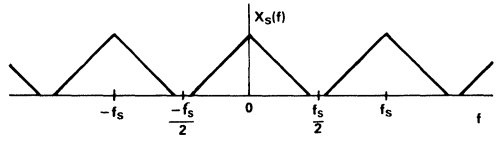


Figure 14d. Replications of x(f) when x(t) is Over Sampled

Aliasing can be avoided by limiting the bandwidth of x(t) to a maximum frequency F_O with an antialiasing filter and sampling at $f_S > 2F_O$, which is known as the Nyquist criteria. In practice, for a fixed sample rate, the amount of aliasing that occurs can be reduced by attenuating interferences outside of the frequency bandwidth of interest as illustrated in Figure 14c. Similarly, for a fixed amount of attenuation outside of the frequency bandwidth of interest, the amount of aliasing that occurs can be reduced by increasing the sampling rate as illustrated in Figure 14d.

The amount of aliasing that is acceptable in a given application should be less than the minimum detectable signal, which is set by the A/D converter signal-to-noise ratio. The amount of aliasing that will occur is a function of the

(1) frequency bandwidth of interest
(2) strength of interferences outside of (1)
(3) filter order and
(4) sample rate.

The user must select (3) and (4) given a converter with a particular SNR to correctly sample a signal in (1) given (2).

Quantization Effects

For an ideal A/D converter, the noise floor is determined by the quantization level used in the digitization process. The signal-to-noise ratio (SNR) for an A/D converter is the ratio of the rms magnitude of the fundamental frequency to the rms sum of all nonharmonically related signals up to half the sampling frequency. SNR is therefore a figure of merit associated with a converter that defines the minimum detectable signal. The theoretical limit on SNR due to quantization noise is

$$\text{SNR max (dB)} = 6.02N + 1.76$$

where N is the number of bits in the converter. For a 12-bit converter such as the AD1332, the maximum SNR is 74dB.

ANTIALIASING FILTER

Features Description

The antialiasing filter in the AD1332 is an active 4th order Butterworth approximation of a low pass filter. A key feature of the Butterworth approximation is a maximally flat magnitude response. For Butterworth filters, attenuation at the cutoff frequency f_C is 3dB and "rolloff" after f_C is 20dB per decade, per pole. Actual AD1332 filter frequency responses for 25kHz and 50kHz cutoff frequencies are shown in Figures 15a and 15b.

It can be shown that an LC ladder filter designed for maximum power transfer from the source exhibits extremely low sensitivity to component variations. This property of the LC filter is exploited

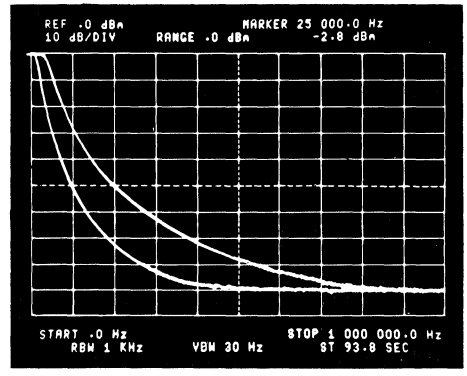


Figure 15a. Filter Response, f_C = 25kHz & 50kHz (C1–C4 = 1000pF & C1–C4 = 500pF)

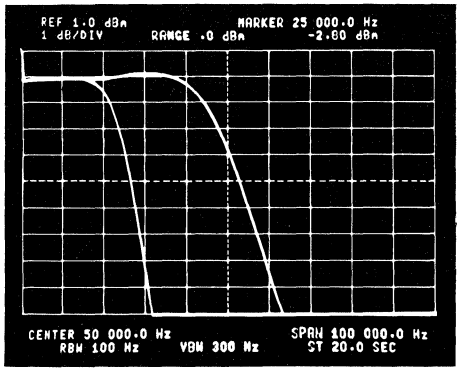


Figure 15b. Filter Passband Response, f_C = 25kHz & 50kHz (C1–C4 = 1000pF @ C1–C4 = 500pF)

in the design of the AD1332 antialiasing filter, which is an RC-active simulation of an LC "prototype." The active components consist of low noise, high-speed operational amplifiers which enable the AD1332 filter to maintain extremely low distortion and consistent response characteristics for cutoff frequencies up to 50kHz. The passive components are precisely trimmed thin-film resistors and external capacitors supplied by the user.

Since the circuit configuration is extremely insensitive to component variations, tight (1%–2%) tolerance capacitors are not required unless the cutoff frequency must be precisely controlled. For example, Figure 16 compares the passband response when capacitors C1–C4 are 1000pF 1% tolerance versus the response when one of the capacitors (C3) is 10% high (1100pF). Note that no additional passband "peaking" is observable, although the cutoff frequency has changed approximately 5% from Figure 15's 25kHz to 23.75kHz.

In contrast to switched capacitor filters, the AD1332 filter does not require a clock, prefiltering nor post-filtering since it is not a sampled data system.

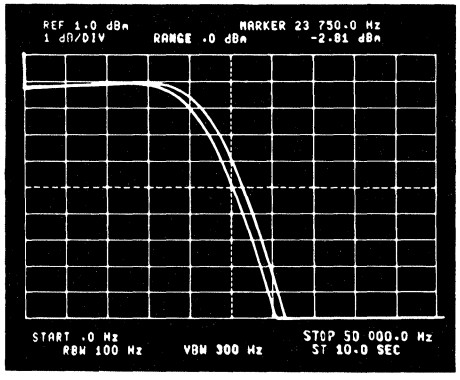


Figure 16. Filter Passband Response, f_C = 25kHz (C1–C4 = 1000pF & C1, C2, C4 = 1000pF, C3 = 1100pF)

Operational Description

Four equal value capacitors are used to select the cutoff frequency f_C according to the equation:

$$f_C = 25\text{kHz} \div C$$

where C is the capacitor value in nF. Good quality, low dissipation factor capacitors such as monolithic ceramic, metallized polycarbonate or polystyrene should be used. If polystyrene capacitors are used, the lead connected to the outer foil should be connected to the AD1332 Cwv (working voltage) pins. If the filter is not used; C1vg (Pin 3), C2vg (Pin 2), C3vg (Pin 39) and C4vg (Pin 38) should all be tied to ASIG GND (pin 8).

SAMPLING A/D CONVERTER

Features Description

The AD1332 provides a complete analog to digital converter function that allows the user to select a sample rate up to 125kHz while maintaining true 12-bit accuracy. As shown on page 1, the AD1332 includes an on-board sample and hold amplifier and low drift voltage reference. The analog input voltage range is from −5V to +5V and the digital output coding is Offset Binary (see Table I). Twos complement coding can be obtained by inverting the MSB (D11).

Output Code	Center of Code Voltage (V)
000 . . . 000	−5.000000
011 . . . 111	−0.002441
100 . . . 000	0.000000
111 . . . 111	+4.997559

Table I. A/D Conversion Relationship

Operational Description

Analog signal information is converted to a 12-bit digital word by means of sampling the waveform and digitizing the sample using the successive approximation conversion technique. Two timing modes are available for sampling and converting the analog input.

Periodic Timing Mode

The periodic timing mode samples the input signal at equally spaced time intervals at a rate that is proportional to the input clock frequency. The connections required for the periodic timing mode for sample rates between 25kHz and 125kHz are shown in Figure 17. In this mode, the clock input is divided down internally to generate the SAMPLE OUT signal which is connected to the SAMPLE IN pin. The periodic timing circuit allots 7 clock periods to sample and hold acquisition and 13 clock periods to A/D conversion. The sample rate is therefore:

$$f_S = f_{CLK} \div 20$$

which is 125kHz for a 2.5MHz clock. The timing diagram for this mode is shown in Figure 18.

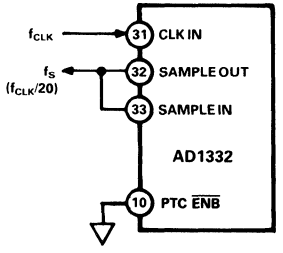


Figure 17. Periodic Timing Mode Connections

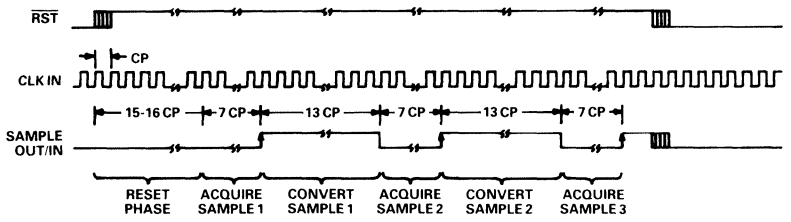


Figure 18a. Timing Diagram for Periodic Timing Mode (PTC $\overline{ENB}$ = 0)

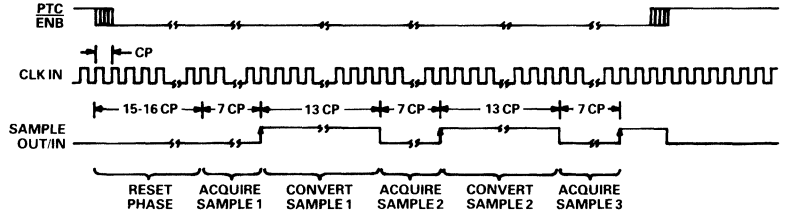


Figure 18b. Timing Diagram for Periodic Timing Mode ($\overline{RST}$ = 1)

PTC $\overline{ENB}$ functions as an "on/off" switch for the periodic timing circuit and is both an input and an open drain output. The periodic timing circuit can therefore be activated either through the microprocessor interface (via Control Register Bit 7) or externally by an open drain driver (such as the 74HC03). The circuit can also be permanently enabled by grounding PTC $\overline{ENB}$.

As shown in Figure 19, slowing the clock down below 1MHz will result in degraded performance at high temperatures when the sampled input "droops" during the A/D conversion. Figure 20 shows the modifications required to the circuit shown in Figure 17 to maintain 12-bit linearity over temperature. This circuit simply divides the SAMPLE OUT signal by an appropriate power of two to sample at the correct rate while maintaining a 500kHz to 2.5MHz A/D converter clock.

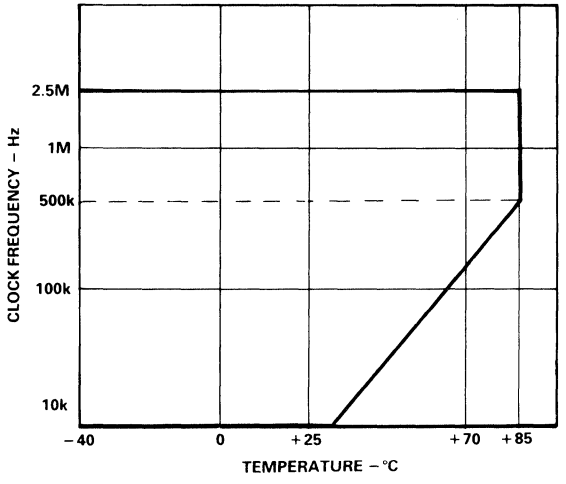
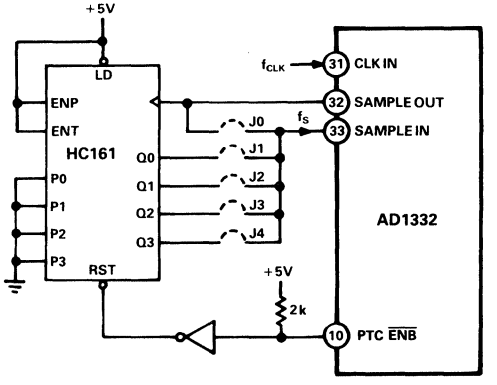


Figure 19. Range of Clock Frequencies vs. Temperature for 12-Bit Linearity



Jumper	f_{CLK}/f_S	f_S Range w/ 500kHz ≤ f_{CLK} ≤ 2.5MHz	
J0	20	25.00kHz –	125.00kHz
J1	40	12.50	62.500
J2	80	6.25	31.250
J3	160	3.125	15.625
J4	320	1.5625	7.8125

Figure 20. Periodic Timing Mode Connections when 500kHz≤f_{CLK}≤2.5MHz

It is important to note that since the clock is used to define the amount of time between samples that it should be crystal controlled since instability in the clock circuit will appear as additional timing uncertainty ("jitter") in the sample and hold, which will result in degraded SNR.

Externally Triggered Mode

If the periodic timing circuit is not used, conversions can be triggered externally by connecting the AD1332 as shown in Figure 21. The timing diagram for this mode is shown in Figure 22. The duty cycle for the CONVERT START command must allow a minimum of 2.8μs for sample and hold acquisition. Note that if the CONVERT START command is not synchronized to the clock input, up to 15 clock periods will be required to complete the conversion cycle so the maximum sampling rate in this mode will be 110kHz when a 2.5MHz clock is used.

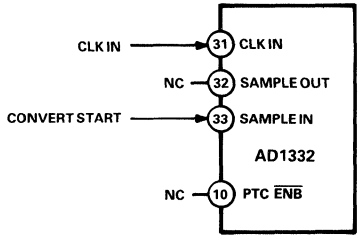


Figure 21. Externally Triggered Mode Connections

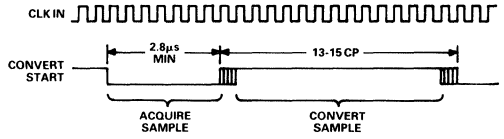


Figure 22. Timing Diagram for Externally Triggered Mode

Since the clock does not define the amount of time between samples, it need not be crystal controlled.

HIGH-SPEED DIGITAL INTERFACE

Features Description

The AD1332 completes the solution for A/D conversion in DSP applications by providing the systems designer a direct, high speed parallel digital interface. The prime feature of this interface architecture is that it operates completely asynchronously from the A/D converter and therefore allows the AD1332 to appear as "memory" to a microprocessor.

The combination of fully asynchronous operation with respect to the A/D conversion process and fast data access time allows the AD1332 user to upgrade to faster versions, or even different vendors, of DSP hardware without having to add synchronization or wait state logic. In addition, by virtue of hybrid circuit technology, the user is not required to add external circuitry to prevent digital feedthrough into the analog section.

The AD1332 data transfer is accomplished by employing an interrupt driven architecture. Interrupts can be programmed by the microprocessor to be generated when the FIFO is full (32 conversion results), half-full (16 conversion results) or after every conversion (FIFO is bypassed). The AD1332 digital interface also includes an overrange detect circuit, which can generate an interrupt if the sampled analog input signal exceeds positive or negative full scale, to alert the system that a conversion result has been generated that will result in a nonlinearity in the subsequent signal processing.

Operational Description

The AD1332 can interface directly to a microprocessor via standard data (D0-D11), address (A0) and control lines ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{IRQ}$ and $\overline{RST}$).

Data Transfer

The data lines D0-D11 are bidirectional I/O that are TTL compatible and have 4mA drive capability. The data lines are used to transfer control information into, and A/D conversion results with status information out of, the AD1332. Address line A0 is an input that is used to select as the data path either A/D conversion results (A0 = 0) or the Control/Status Registers (A0 = 1) and would typically be the least significant address bit in the system if the AD1332 is "mapped" to adjacent memory locations. Chip-Select ($\overline{CS}$) is used to define a unique location in memory for the AD1332 and should be formed by decoding the upper address bits. Read ($\overline{RD}$) and Write ($\overline{WR}$) define the type of data transfer.

Figures 26 – 31 illustrate how the AD1332 interfaces to a number of popular single-chip digital signal processors.

Interrupts

Interrupt Request ($\overline{IRQ}$) is an open drain output that can be used to interrupt the processor on any of the conditions programmed in the control register. The processor should be programmed to interrupt on the falling edge of its Interrupt Request input.

FIFO Half-Full Interrupt

The timing for interrupts that are generated when the FIFO is half full is shown in Figures 23a and 23b. In both figures, $\overline{IRQ}$ becomes active when the 16th A/D conversion result is shifted into the FIFO. In Figure 23a, the processor responds immediately and a read cycle takes place before the next conversion cycle begins. Here, the completion of the read cycle shifts the first conversion result (which was just read by the processor) out of the FIFO, replaces it with the second conversion result and causes $\overline{IRQ}$ to become inactive since there are now 15 conversion results in the FIFO.

In Figure 23b, the processor does not respond before the next conversion cycle begins and $\overline{IRQ}$ becomes inactive. The FIFO continues to accept conversion results and the processor can read from the FIFO at any time so long as the FIFO has not overrun.

This mode allows the AD1332 to have a low interrupting priority since the processor has 340 A/D converter clock periods (17 conversions × 20 clock periods per conversion) in the periodic timing mode before the FIFO overruns. Therefore, the processor will have up to 136μs to respond at the maximum sample rate of 125kHz (since f_{CLK} = 2.5MHz).

FIFO Full Interrupt

The timing for interrupts that are generated when the FIFO is full is shown in Figures 24a and 24b. In both figures, $\overline{IRQ}$ becomes active when the 32nd A/D conversion result is shifted into the FIFO. In Figure 24a, the processor responds immediately and a read cycle takes place before the next conversion cycle begins. Here, the completion of the read cycle shifts the first conversion result (which was just read by the processor) out of the FIFO, replaces it with the second conversion result and causes $\overline{IRQ}$ to become inactive because there are now 31 conversion results in the FIFO.

In Figure 24b, the processor does not respond before the next conversion cycle begins and $\overline{IRQ}$ becomes inactive. The processor must read from the FIFO before the completion of the current conversion cycle or the FIFO will overrun.

This mode maximizes the memory capability of the AD1332 but requires a fairly high interrupting priority in the processor since the processor has only 20 A/D converter clock periods (1 conversion

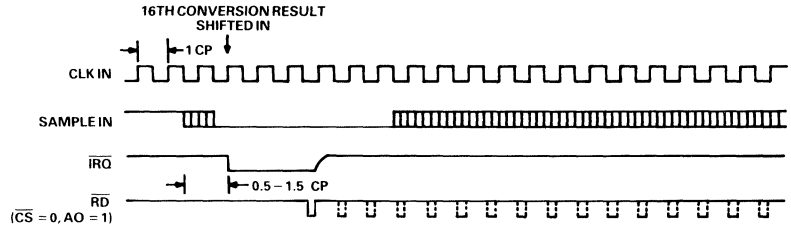


Figure 23a. Timing Diagram for Half-Full Interrupt (Read before 17th Conversion Started)

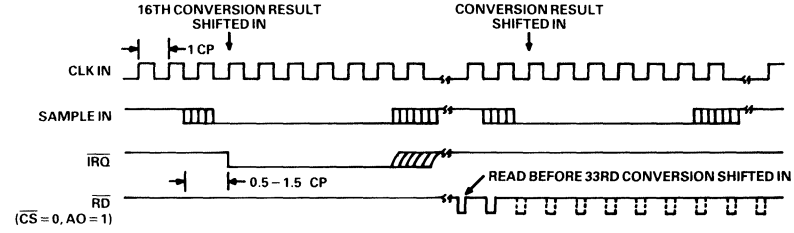


Figure 23b. Timing Diagram for Half-Full Interrupt (Read after 17th Conversion Started)

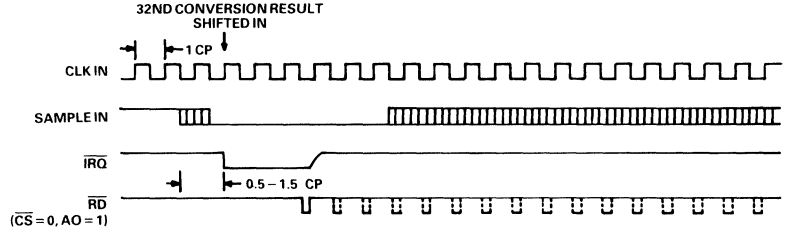


Figure 24a. Timing Diagram for Full Interrupt (Read before 33rd Conversion Started)

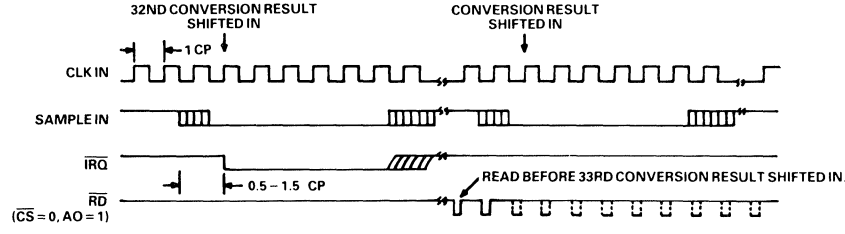


Figure 24b. Timing Diagram for Full Interrupt (Read after 33rd Conversion Started)

× 20 clock periods per conversion) in the periodic timing mode before the FIFO overruns. Therefore, the processor will have only 8μs to respond at the maximum sample rate of 125kHz (since f_{CLK} = 2.5MHz).

Conversion Results Overrange Interrupt

If the FIFO is used, the AD1332 can be programmed to generate interrupts when overranged conversion results are shifted into the FIFO. If $\overline{IRQ}$ became active as a result of an overrange condition, the only way it can become inactive is to clear Bit 4 of the control register. Typically, the user should clear the entire control register which will, in effect, remove the interrupt, reset the FIFO and reset the periodic timing circuit.

Should the overrange interrupt capability be used, Status Register Bits 4 and 6 can be used to identify whether the interrupt occurred as a result of an overrange condition or FIFO half full (or full).

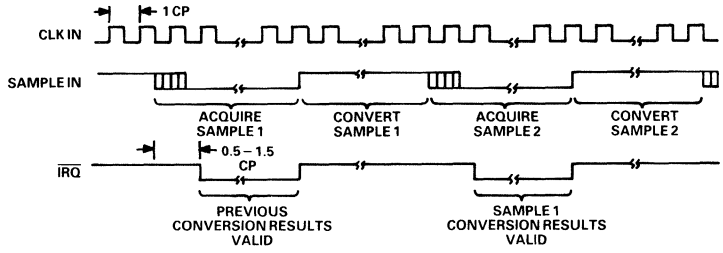


Figure 25. Timing Diagram for Single Conversion Interrupt

Single Conversion Interrupt (FIFO Bypassed)
The timing for interrupts that are generated when the FIFO is bypassed is shown in Figure 25. Here, $\overline{IRQ}$ becomes active at the completion of a single A/D conversion cycle, which may be up to two A/D converter clock periods after the sample and hold starts acquiring the next sample. $\overline{IRQ}$ remains active, independent of the read cycle, until the next conversion cycle begins. Data is valid so long as $\overline{IRQ}$ remains active.

This mode makes data available immediately after the conversion process has been completed, and is therefore very similar to the operation of a conventional A/D converter if $\overline{IRQ}$ is taken to mean conversion STATUS. This mode is most useful when a single conversion result is necessary to adjust a system parameter, such as the gain of a PGA that may be in front of an AD1332.

Since $\overline{IRQ}$ will only be valid for six A/D converter clock periods in periodic timing mode (2.4μs with a 2.5MHz clock), a high interrupting priority should be assigned by the processor. Should the single conversion result be necessary to adjust a system parameter as described above, it may be more efficient to "poll" the Status Register to determine when the conversion result is available.

Operation Other than with a Microprocessor
The AD1332 can be used in other microprocessor environments by grounding Pins 12, 13 and 28 ($\overline{CS}$, A0 and $\overline{RD}$), connecting Pin 29 ($\overline{WR}$) to V_{DD} and pulsing $\overline{RST}$ low. This will permanently enable the AD1332 3-state outputs and clear the control register, causing the FIFO to be bypassed.

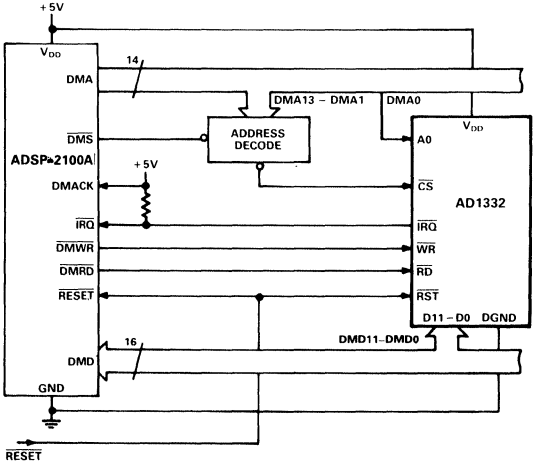


Figure 26. ADSP-2100A to AD1332 Interface

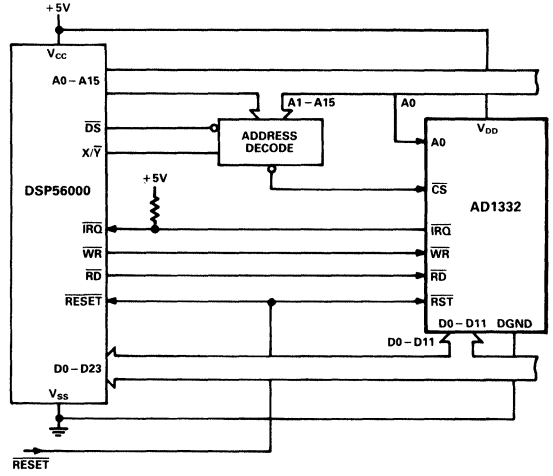


Figure 27. DSP56000 to AD1332 Interface

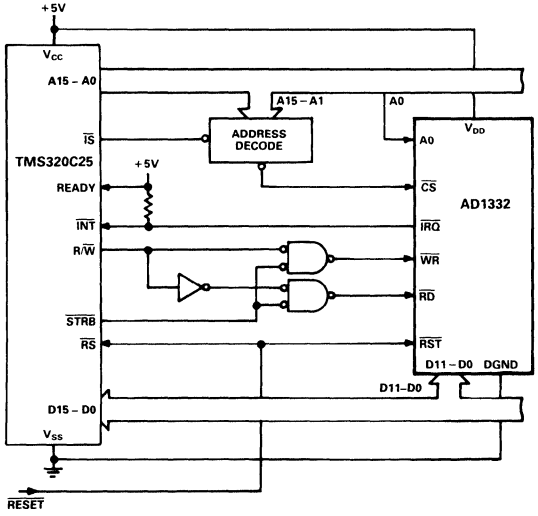


Figure 28. TMS320C25 to AD1332 Interface

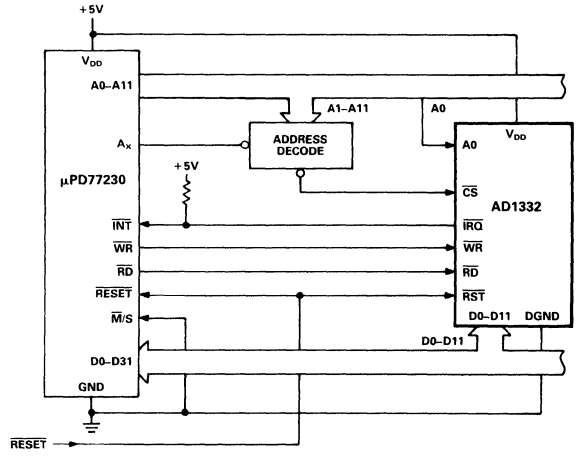


Figure 29. μPD77230 to AD1332 Interface

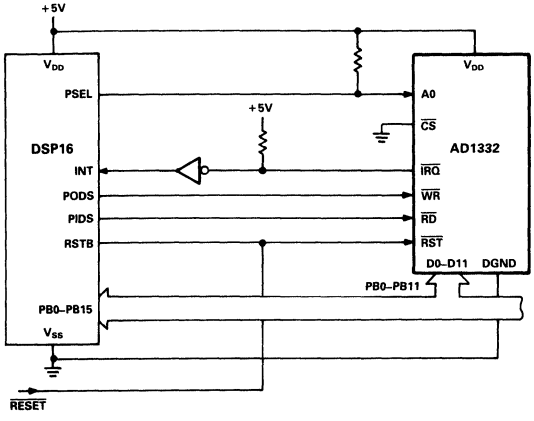


Figure 30. DSP16 to AD1332 Interface

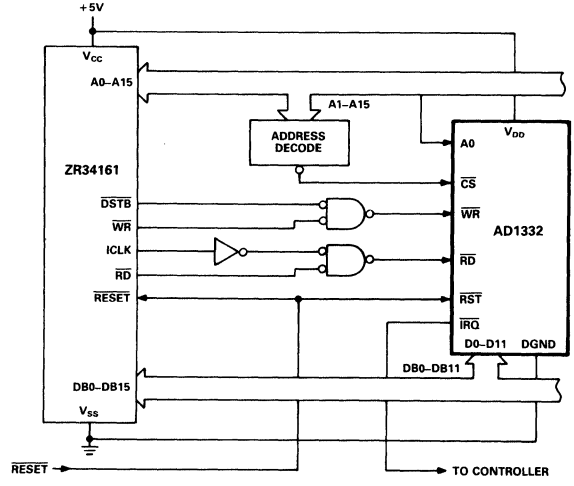


Figure 31. ZR34161 to AD1332 Interface

Multiple AD1332s

The architecture of the AD1332 allows multiple devices to be used in a microprocessor based system. Figure 32 illustrates how four AD1332s can be configured to simultaneously sample their analog inputs and reside in eight sequential locations in a microprocessor's memory address space. Since the AD1332s are sampling at the same rate, one AD1332 functions as the "master" and drives its own SAMPLE IN pin as well as those of the remaining devices ("slaves"). The Control Register of each device should be programmed to interrupt on the same condition so that the same number of conversion results are available from all devices.

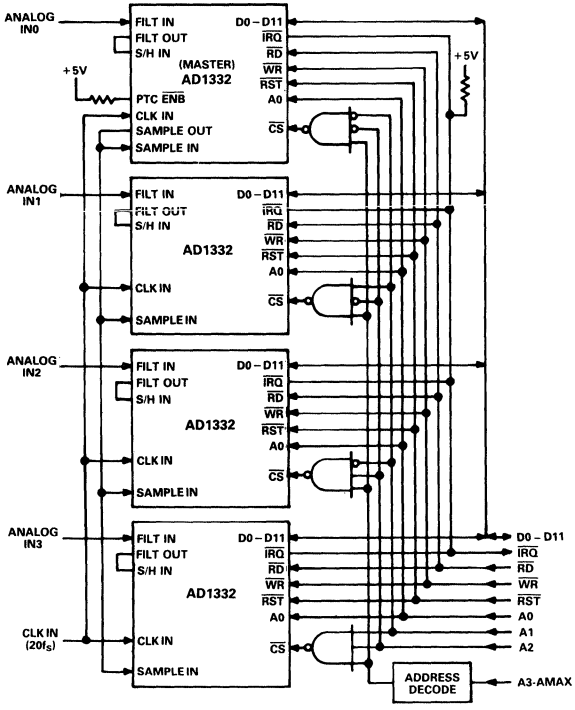


Figure 32. 4-Channel Simultaneous Sampling System

Sequential Sampling

Figure 33 illustrates how an AD1332 can be configured to sequentially sample sixteen channels of analog inputs. The circuit works as follows. The HC161 outputs Q0-Q3 form the address bits for the AD7506 muliplexer. Through the microprocessor interface, the periodic timing circuit is enabled and the HC161 is taken out of reset by setting Control Register Bit 7. Since the HC161 was reset, Channel 0 is initially selected. Following an AD1332 reset cycle (15-16 clock periods), 7 clock periods are used to acquire the Channel 0 input. Once acquired, the rising edge of SAMPLE OUT puts the AD1332 sample and hold into hold mode, starts the A/D conversion and advances the HC161 one count. Therefore, while Channel 0 is being converted, the multiplexer switches to Channel 1 and settles during the 13 clock periods required for A/D conversion.

The above continues until Channel 15 has been sampled, at which point the HC161 returns to an all zero count and commences another pass through the 16 channels. The process can be terminated by clearing Control Register Bit 7.

Since each channel is sampled on every 16th rising edge of the SAMPLE OUT signal, the effective sampling rate is:

$$f_S = (f_{CLK} \div 20) \div (\text{Number of Channels})$$

$$= f_{CLK} \div 320$$

Any number of channels can be sequentially sampled with slight modifications to the circuit shown in Figure 33.

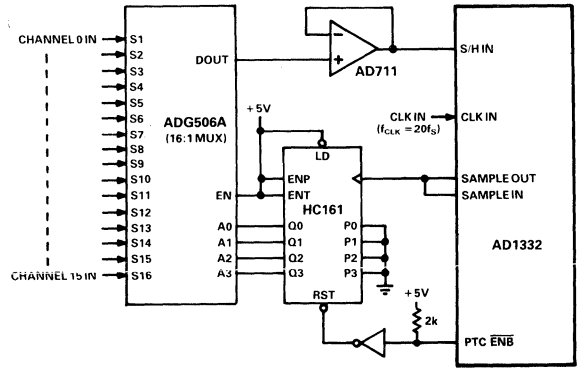


Figure 33. 16-Channel Sequential Sampling System

SUCCESSFULLY APPLYING THE AD1332

Grounding

In order to obtain the specified performance of the AD1332, proper grounding and power supply decoupling techniques must be observed. First, it is imperative that a ground plane be used. A ground plane provides a low resistance, low inductance path for currents to flow back to their source. Without a ground plane, currents will return to the source in such a way as to minimize the energy of the system and therefore parasitic inductances will exist in such undesirable locations as power supply lines and signal grounds.

Second, all three ground connections on the AD1332 must be tied together to the ground plane. The AD1332 APWR GND (Pin 9) carries the imbalance current from the analog power supplies ($\pm V_S$). APWR GND is also connected to the package seal ring/lid and therefore can cause coupling between the analog and digital sections if it is not tied directly to the ground plane.

ASIG GND (Pin 8) is the signal ground internal to the AD1332 and is "common" for the filter, −5V reference, sample and hold, and A/D converter. The current that flows through this pin from the A/D converter is a dynamic current that changes on every clock cycle. Inductance in this trace will therefore cause a reduction in performance in the entire analog section.

DGND (Pin 20) is a separate ground connection for the digital interface chip. It carries a dynamic current every time a digital output changes state, and inductance in the trace that connects to this pin will reduce the noise margin between the A/D converter and the digital interface chip.

Power Supply Decoupling

The power supply decoupling capacitors supply the instantaneous current to the AD1332 and also provide some high frequency filtering. The filtering aspect of the capacitors should not be counted on however, and the user should make every effort to

supply quiet, well regulated power supplies to the AD1332. Switching mode power supplies are not recommended for the analog power supplies $\pm V_S$.

Decoupling capacitors should be placed as close to the device as possible to minimize inductances in power supply traces. A 2.2μF (or greater) solid tantalum capacitor in parallel with a 0.1μF ceramic capacitor should be used for decoupling each $+V_S$ and $-V_S$. A 1.0μF (or greater) solid tantalum capacitor should be used for decoupling V_{DD}.

Transmission Line Effects

The digital interface has 10K ECL speed and with 15pF loading exhibits a typical edge rate of 1.4ns. High speed CMOS systems that incorporate the AD1332 must use careful PCB layout and impedance matching techniques to reduce crosstalk and voltage reflections.

Crosstalk

The fast edge rates with large voltage swings of CMOS systems can result in capacitive and inductive coupling (crosstalk) between adjacent PCB signal traces and may compromise signal integrity and reduce noise margins. The effect can be most severe on data lines that are near "clocked" control lines, such as Read, Write and Chip Select lines, when they actually change their logic state as a result of crosstalk.

To reduce crosstalk, the PCB layout should minimize long parallel traces. If this can not be avoided, clock lines should be shielded from data and address lines by running ground traces along side them.

Voltage Reflections

The gross impedance mismatch between high impedance CMOS inputs and low impedance CMOS outputs invites unwanted voltage reflections and "ringing" that can also compromise signal integrity and reduce noise margins. This level of mismatch causes a nearly equal and opposite negative pulse to be reflected back from the load to the source when the round trip delay of the line exceeds the rise or fall time of the driving signal. For a typical line delay of 0.055ns/cm with a 1.4ns edge rate, this translates to only 13cm (5 inches) for the AD1332. Provided the signal lines are over a ground plane, this may never be a problem since the added capacitance will reduce the edge rate.

The effect will be most severe on "clock" lines in synchronous systems such as Read, Write and Chip Select lines. For example, should the AD1332 Read control input ($\overline{RD}$) be double clocked as a result of a reflection while in a read cycle, in most cases the digital interface chip will be fast enough to respond. If the FIFO is being read from, a second shift out will occur and A/D conversion results will be lost.

Since CMOS output stages are not capable of delivering enough current to the load when a transmission line (PCB trace) is terminated in its characteristic impedance, a series damping is recommended when reflections must be reduced or eliminated. Here, a small resistor (typically 10Ω to 75Ω) is inserted in series with the transmission line as close to the source as possible. The goal is to match the series resistance plus driver output impedance to the transmission line impedance. This will keep the wave that is reflected back from the load to source from reflecting back to the load.

The primary disadvantage of series termination is that due to the voltage divider formed by the source resistance and line impedance, the voltage at the input to the line is midway between logic levels during the two way propagation delay time. This means that although any number of device inputs may be attached at the load end, other device inputs cannot be distributed along the transmission line.

REFERENCES

1. Oppenheim, Alan V. and Schafer, Ronald W., *Digital Signal Processing*, Prentice Hall, 1975.

2. Marple, S. Lawrence, *Digital Spectral Analysis with Applications*, Prentice, Hall 1987.

3. Cypress Semiconductor, *CMOS Data Book*, Cypress Semiconductor, 1987.

ANALOG DEVICES Four-Channel 12-Bit Sampling A/D Converter for Digital Signal Processing

AD1334

FEATURES

Four-Channel A/D Converter for DSP Includes:
- **Simultaneous or Independent Sampling Capability**
- **12-Bit Accurate A/D Converter**
- **2-Bit Channel ID Tags Each Conversion Result**
- **32-Word FIFO Memory**
- **Fully Asynchronous, High Speed Digital Interface**

Single-Channel Sample Rate Up to 67kHz
Four-Channel Simultaneous Sample Rate Up to 28kHz
Entire System Dynamically Characterized
Minimal Effective Aperture Delay Mismatch from Channel-to-Channel & Device-to-Device
15ns Data Access Time Allows "No Wait State" Interface to: ADSP-2100 (A), TMS320C25 DSP56000, NECμPD77230
Low Power, 250mW/Channel

APPLICATIONS

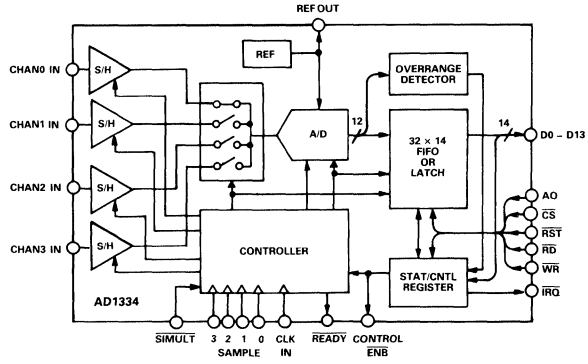
Sonar Signal Processing
Robotics/Machine Control
Disk-Drive Head Positioning
Vibration Analysis

PRODUCT DESCRIPTION

The AD1334 is a four-channel, 12-bit, sampling A/D converter system optimized for use in multichannel digital signal processing (DSP) applications. The device consists of four independent sample-and-hold amplifiers, a multiplexer, an A/D converter, a controller, a 32-word FIFO memory and a fully asynchronous high speed digital interface. The product is packaged in a 40-pin hermetic DIP.

The channel controller enables the AD1334 to appear as four independent channels of analog input by generating all of the timing necessary to ensure that the sampled channel is digitized to 12-bit accuracy. Upon receipt of a sample command, the controller will immediately place the sample-and-hold amplifier into hold mode and then prioritize and schedule the held value for A/D conversion. At the appropriate time, the sampled input is gated through the multiplexer and, after settling, is digitized by the A/D converter. The sample-and-hold amplifier is then returned to sample mode so that it can acquire the next sample.

AD1334 FUNCTIONAL BLOCK DIAGRAM



For effective use in simultaneous sampling applications, the sample-and-hold amplifiers are designed to provide a minimum amount of aperture delay time mismatch from channel-to-channel and device-to-device.

The 12-bit A/D converter can convert ± 5V full scale signals at sample rates up to 67kHz for single-channel operation. In the simultaneous mode, the AD1334 has a four-channel sample rate up to 28kHz. The entire converter system is specified and tested for signal-to-noise ratio, total harmonic distortion and channel-to-channel isolation.

The digital interface provides a true asynchronous link between the A/D and a high speed microprocessor. Data transfer is controlled by generating an interrupt signal when data is available. Interrupts can be generated when the FIFO is full (32 words), half-full (16 words), or when a single word of data is ready (FIFO bypassed). The AD1334 can also generate an interrupt when the A/D conversion results are overrange.

The AD1334 provides a completely specified and tested system that bridges the interface and specification gap between A/D converters and high speed DSP.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, V_{DD} = +5V and f_{CLK} = 2.5MHz unless noted)

Parameter	AD1334BD Min	Typ	Max	Units
S/H, Mux & A/D Converter[1]				
Input Impedance	2	2.5		kΩ
Voltage Range		−5 to +5		V
Output Coding		Offset Binary		
CLK IN Frequency, (f_{CLK})	1.0		**2.5**	MHz
High Time	200			ns
Low Time	200			ns
Sampling Rate Per Channel (f_S)				
Simultaneous Mode ($\overline{SIMULT}$ = LOW)				
1 Channel			67	kHz
2 Channels			46	kHz
3 Channels			35	kHz
4 Channels			**28**	kHz
Independent Mode ($\overline{SIMULT}$ = HIGH)				
1 Channel			67	kHz
2 Channels			67	kHz
3 Channels			44	kHz
4 Channels			33	kHz
S/H				
Acquisition Time to 0.01%		6.5	7.5	µs
Droop Rate		0.2	1.0	mV/ms
Over Temperature		Doubles Every 10°C		
−3dB Small Signal Bandwidth		200		kHz
Group Delay[2] (f_{IN}<10kHz)		785		ns
Aperture Delay[3]	0	10	15	ns
Effective Aperture Delay[4] (f_{IN}<10kHz)	−700	−775	−850	ns
Static Characteristics				
Integral Nonlinearity		±1/2	**±1**	LSB
Over Temperature			±1	LSB
Resolution for No Missing Codes	**12**			Bits
Over Temperature	12			Bits
−Full-Scale Error		±2	**±4**	LSB
Over Temperature		±4	±8	LSB
+Full-Scale Error		±2	**±4**	LSB
Over Temperature		±4	±8	LSB
PSRR, $\pm V_S$		±1/2		LSB/V
Dynamic Characteristics[5,6]				
Signal-to-Noise Ratio, f_{IN} = 13.6kHz	**70**	72		dB
Total Harmonic Distortion, f_{IN} = 13.6kHz		−86	**−76**	dB
Intermodulation Distortion, f_{IN1} = 13.1kHz & f_{IN2} = 13.6kHz		−86	**−76**	dB
Channel-to-Channel Isolation[7], f_{IN} = 8.009kHz				
$\overline{SIMULT}$ = LOW	**70**	78		dB
$\overline{SIMULT}$ = HIGH		74		dB
Reference Voltage	**−5.05**		**−4.95**	V
Output Current	**±1**	±2		mA
Drift		±5	±25	ppm/°C

Parameter	AD1334BD Min	Typ	Max	Units
DIGITAL INPUTS[6]				
Voltage Input, LOW			+0.8	V
HIGH	+2.0			V
Input Current			±250	μA
Input Capacitance		5		pF
$\overline{RST}$ LOW Pulse Width	10			ns
DIGITAL OUTPUTS[6]				
D0–D13, $\overline{READY}$				
Output Voltage, Logic LOW, I_{OL} = 4mA			+0.4	V
Output Voltage, Logic HIGH, I_{OH} = −4mA	+2.4			V
3-State Leakage Current			±10	μA
$\overline{IRQ}$, CONTROL $\overline{ENB}$				
Output Voltage, Logic LOW, I_{OL} = 4mA			+0.4	V
$\overline{IRQ}$ Off-State Leakage			±10	μA
Output Capacitance		5		pF
FIFO Fall-Thru Time		400	800	ns
$\overline{IRQ}$ LOW to D0–D13 Valid[8]			0	ns
POWER REQUIREMENTS				
Operating Range				
$\pm V_S$	±11.4		±15.75	V
V_{DD}	+4.75		+5.25	V
Supply Current				
$+V_S$		42	60	mA
$-V_S$		40	57	mA
$+V_{DD}$		2	5	mA
Consumption				
$\pm V_S$ = ±12V		1.0	1.2	W
$\pm V_S$ = ±15V		1.2	1.5	W
TEMPERATURE RANGE				
Operating and Specified	−40		+85	°C
Storage	−65		+150	°C

NOTES

[1]Specifications are per channel in 4 Channel Simultaneous Mode (SAMPLE 0-3 connected together and $\overline{SIMULT}$ & CONTROL $\overline{ENB}$ = LOW), at f_S = 28kHz, and with SAMPLE 0-3 having an 80% duty cycle unless noted.

[2]Group delay is the negative of the 1st derivative of phase with respect to frequency and is a measure of the analog time delay through the S/H.

[3]Aperture delay is the time delay from the SAMPLE input to S/H switch opening and is a measure of the digital time delay through the S/H.

[4]Effective aperture delay is the difference between analog and digital time delays described in (2) and (3).

[5]THD of harmonics 2-7 of the fundamental.
SNR of fundamental less harmonics 2-7.

[6]Guaranteed over operating temperature and power supply voltage range tested at +25°C only.

[7]Isolation of any one channel from remaining three channels which have near maximum amplitude ac signals at their inputs.

[8]$\overline{RD}$, $\overline{CS}$, AO = LOW; $\overline{WR}$, $\overline{RST}$ = HIGH.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units. All other specifications are guaranteed but not tested.

SWITCHING CHARACTERISTICS (over operating temperature and power supply voltage range, with C_{OUT} = 30pF or 100pF except where noted)

Parameter	Description	Conditions	Min	Max	Units
READ CYCLE					
t_{RC}	Read Cycle Time	C_{OUT} = 30pF	25		ns
		C_{OUT} = 100pF	35		ns
t_A	Data Access Time	C_{OUT} = 30pF		15	ns
		C_{OUT} = 100pF		25	ns
t_{LZ}	Output Low Z Time		2		ns
t_{HZ}	Output High Z Time	C_{OUT} = 30pF		15	ns
		C_{OUT} = 100pF		25	ns
t_{OH}	Output Hold Time		2		ns
t_{AORD}	A0 Valid to $\overline{RD}$ LOW		3		ns
t_{RDAO}	$\overline{RD}$ HIGH to A0 Invalid		3		ns
t_{AOCS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSAO}	$\overline{CS}$ HIGH to A0 Invalid		3		ns
WRITE CYCLE					
t_{WC}	Write Cycle Time		15		ns
t_{WP}	Write Pulse Width		5		ns
t_{SU}	Data Setup Time		2		ns
t_{IH}	Input Hold Time		3		ns
t_{AOWR}	A0 Valid to $\overline{WR}$ LOW		3		ns
t_{WRAO}	$\overline{WR}$ HIGH to A0 Invalid		3		ns
t_{AOCS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSAO}	$\overline{CS}$ HIGH to A0 Invalid		3		ns

Specifications subject to change without notice.
All specifications are guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +17V
$-V_S$ to APWR/ASIG GND . . . . . −17V
V_{DD} to DGND . . . . . +7V
APWR/ASIG GND to DGND . . . . . −0.3V to +0.3V
Analog Input to APWR/ASIG GND . . . . . $-V_S$ to $+V_S$
Digital Input to APWR GND
SAMPLE0-SAMPLE3, CLK IN, $\overline{SIMULT}$, CONTROL $\overline{ENB}$ . . . . . −0.3V to +7V
Digital Input to DGND
D0–D13, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, $\overline{RST}$ . . −0.3V to V_{DD} + 0.3V
Output Short Circuit Duration
REF OUT, TP . . . . . Indefinite
Digital Output . . . . . 1 Output for 1sec
Lead Temperature Range,
Soldering for 10sec . . . . . +300°C

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

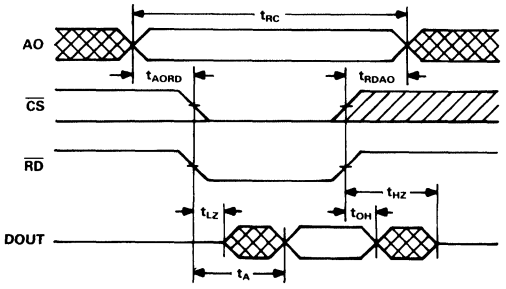
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

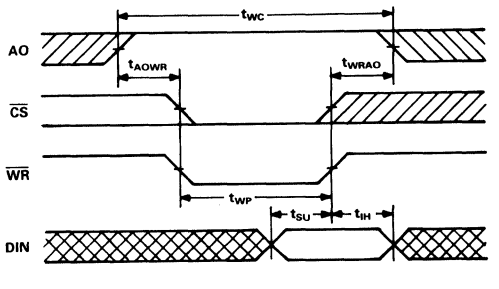
Model	Temperature Range	Package Options*
AD1334BD	−40°C to +85°C	DH-40A
AD1334TD883B	−55°C to +125°C	DH-40A

*See Section 14 for package outline information.



NOTES
CS IS VALID BEFORE OR COINCIDENT WITH RD HIGH-TO-LOW TRANSITION.
CS IS INVALID AFTER OR COINCIDENT WITH RD LOW-TO-HIGH TRANSITION.
WR IS NOT ACTIVE DURING READ CYCLE.

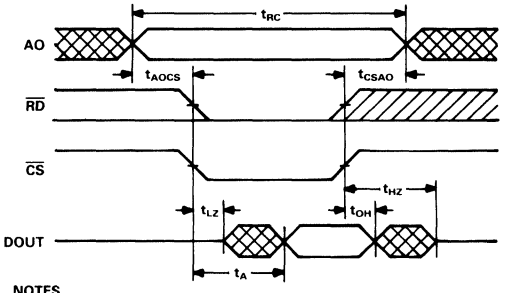
Timing Waveform for Read Cycle No. 1 (RD Controlled)



NOTES
CS IS VALID BEFORE OR COINCIDENT WITH WR HIGH-TO-LOW TRANSITION.
CS IS INVALID AFTER OR COINCIDENT WITH WR LOW-TO-HIGH TRANSITION.
RD IS NOT ACTIVE DURING WRITE CYCLE.

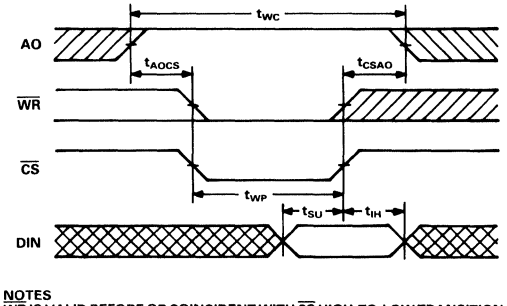
Timing Waveform for Write Cycle No. 1 (WR Controlled)

Figure 1.



NOTES
RD IS VALID BEFORE OR COINCIDENT WITH CS HIGH-TO-LOW TRANSITION.
RD IS INVALID AFTER OR COINCIDENT WITH CS LOW-TO-HIGH TRANSITION.
WR IS NOT ACTIVE DURING READ CYCLE.

Timing Waveform for Read Cycle No. 2 (CS Controlled)



NOTES
WR IS VALID BEFORE OR COINCIDENT WITH CS HIGH-TO-LOW TRANSITION.
WR IS INVALID AFTER OR COINCIDENT WITH CS LOW-TO-HIGH TRANSITION.
RD IS NOT ACTIVE DURING WRITE CYCLE.

Timing Waveform for Write Cycle No. 2 (CS Controlled)

Figure 2.

9

AC TEST CONDITIONS

Input Pulse Levels	DGND to +3.0V
Input Rise/Fall Times	<5ns
Timing Reference Levels	
Inputs	1.5V
Outputs	
LOW	0.4V
HIGH	2.4V
Enabled to LOW	$V_T - 0.1V$
Enabled to HIGH	$V_T + 0.1V$
Disabled from LOW	$V_{OL} + 0.5V$
Disabled from HIGH	$V_{OH} - 0.5V$

$V_T = 1.5V$, the voltage to which 3-stated outputs are forced.

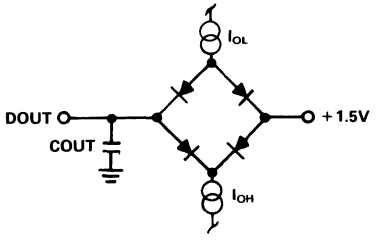


Figure 3. Output Load

Typical Characteristics

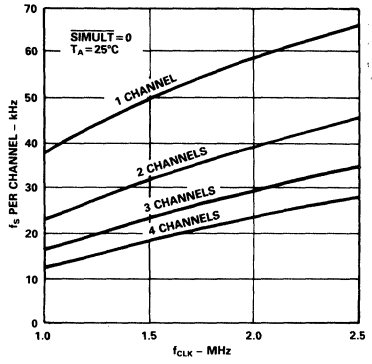


Figure 4. Maximum Sample Rate vs. Clock Frequency (Simultaneous Mode)

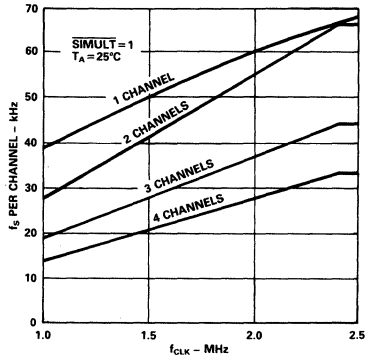


Figure 5. Maximum Sample Rate vs. Clock Frequency (Independent Mode)

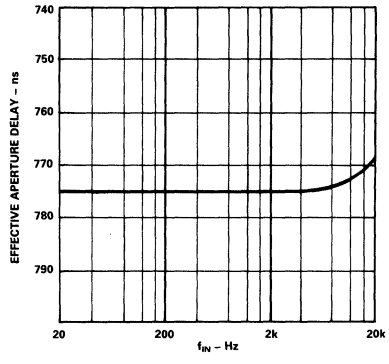


Figure 6. Effective Aperture Delay vs. Frequency

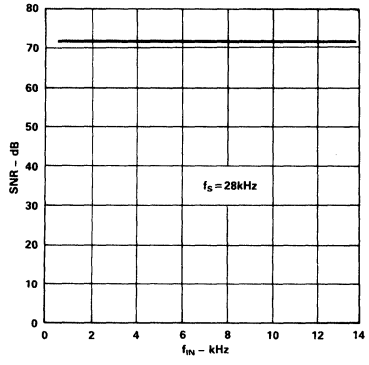


Figure 7. A/D SNR vs. Frequency (Average of Four Channels, Simultaneous Mode)

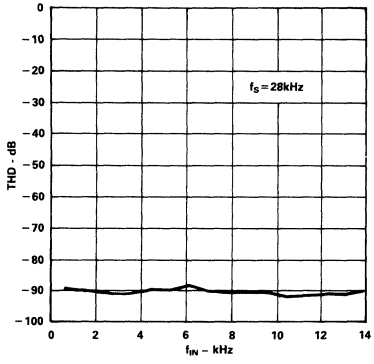


Figure 8. A/D THD vs. Frequency (Average of Four Channels, Simultaneous Mode)

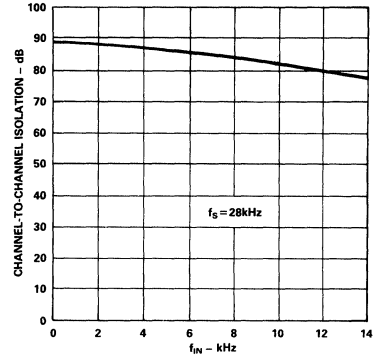


Figure 9. Channel-to-Channel Isolation vs. Frequency

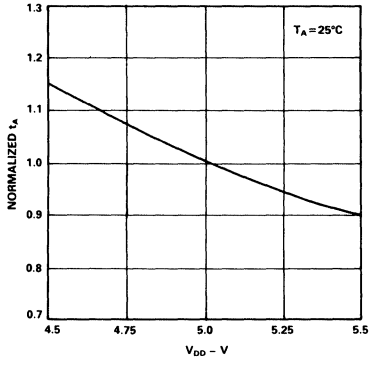


Figure 10. Normalized Data Access Time vs. V_{DD}

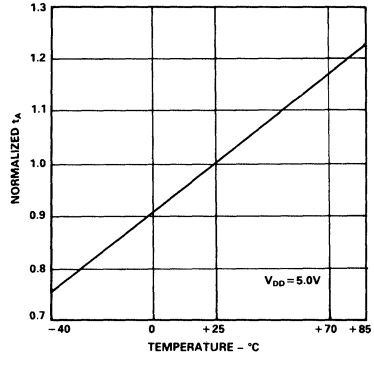


Figure 11. Normalized Data Access Time vs. Temperature

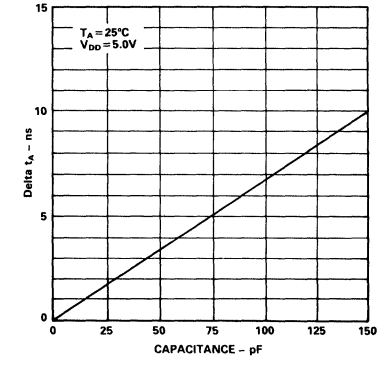
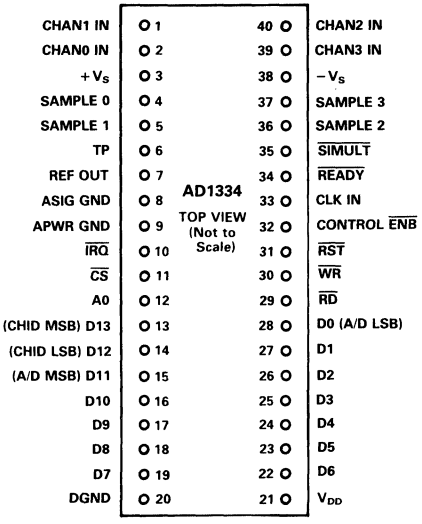


Figure 12. Change in Data Access Time vs. Loading

PIN CONFIGURATION



PIN DESCRIPTIONS

Pin	Mnemonic	Function
2	CHAN 0 IN	Channel 0 analog input.
1	CHAN 1 IN	Channel 1 analog input.
40	CHAN 2 IN	Channel 2 analog input.
39	CHAN 3 IN	Channel 3 analog input.
6	TP	Test Point (no connect).
32	CONTROL $\overline{ENB}$	Input and (open drain) output used to enable controller externally or through µP interface.
34	$\overline{READY}$	Output that, in simultaneous mode, indicates all channels have been successfully converted and device is ready to sample.
35	$\overline{SIMULT}$	Input that when LOW sets controller to simultaneous mode which keeps S/Hs in hold mode until all channels have been converted.
8	ASIG GND	Analog signal ground.
7	REF OUT	−5V reference output.
3, 38	$+V_S$, $-V_S$	Analog power supplies.
9	APWR GND	Analog power ground.
33	CLK IN	External clock input to the A/D converter and channel controller.
4	SAMPLE 0	Channel 0 S/H control input.
5	SAMPLE 1	Channel 1 S/H control input.
36	SAMPLE 2	Channel 2 S/H control input.
37	SAMPLE 3	Channel 3 S/H control input.
10	$\overline{IRQ}$	Open drain interrupt request. User programmable to become active on any of the following conditions: One A/D Conversion Result Available; FIFO Half Full or Full; A/D Conversion Results Over range.
11	$\overline{CS}$	Chip select input.
12	A0	Address bit zero. Selects data path from FIFO/latch (low) or from/to Status/Control register (high).
28–22	D0–D6	Bidirectional 3-state data lines. D11 is A/D converter MSB when D0–D13 are outputs. D7 is Status/
19–13	D7–D13	Control register MSB. D12 and D13 carry channel ID number.
29	$\overline{RD}$	Read control input (D0–D13).
30	$\overline{WR}$	Write control input (D0–D7).
31	$\overline{RST}$	Reset. In reset state, FIFO is transparent & overrange detector is disabled.
20, 21	DGND, V_{DD}	Digital power supply.

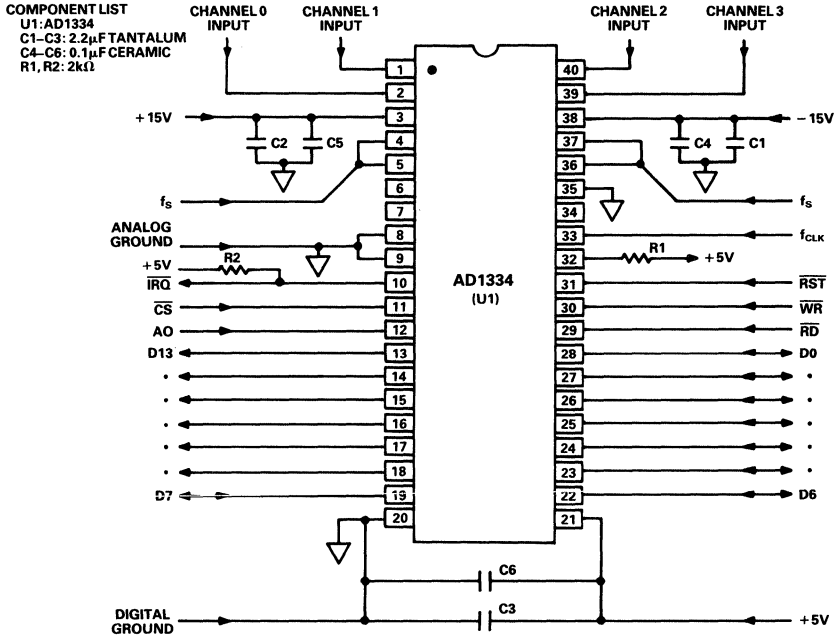


Figure 13. Typical Interface Circuit (Simultaneous Mode)

CONTROL AND STATUS REGISTER DESCRIPTIONS

Control

Bit→	7	6	5	4	3	2	1	0
	CTLEN	$\overline{L}$/F	$\overline{HF}$/F	ORNG	X	X	X	X

Bit	Mnemonic	Function
7	CTLEN	A "0" in this bit position will disable the controller. A "1" in this bit position will enable the controller.
6	$\overline{L}$/F	A "0" in this bit position will reset the FIFO and enable the transparent latch. $\overline{IRQ}$ will become active on the completion of an A/D conversion cycle. $\overline{IRQ}$ will become inactive on the start of the next A/D conversion cycle. A "1" in this bit position will enable the FIFO and activate $\overline{IRQ}$ when the FIFO is half full or full (depending on CBIT 5). $\overline{IRQ}$ will become inactive on the start of the next A/D conversion cycle or when the FIFO is read from.
5	$\overline{HF}$/F	A "0" in this bit position will cause $\overline{IRQ}$ to become active when the 16th word is shifted into the FIFO (if the FIFO is enabled). A "1" in this bit position will cause $\overline{IRQ}$ to become active when the 32nd word is shifted into the FIFO (if the FIFO is enabled).
4	ORNG	A "0" in this bit position will disable the overrange interrupt capability. A "1" in this bit position will activate $\overline{IRQ}$ if overranged (all "0"s or all "1"s) data is shifted into the FIFO. $\overline{IRQ}$ will become inactive when this bit is reset to "0."
3–0	X	Not defined.

Status

Bit→	7	6	5	4	3	2	1	0
	FLAG	DATA	ORUN	ORNG	X	X	X	X

Bit	Mnemonic	Function
7	FLAG	Logical OR of status Bits 4 & 6.
6	DATA	Set if $\overline{IRQ}$ becomes active because data is available. Reset when FIFO is read from if FIFO used. Reset when $\overline{IRQ}$ becomes inactive if latch is used.
5	ORUN	Set when FIFO has overrun. Reset by control Bit 6.
4	ORNG	Set if $\overline{IRQ}$ becomes active because of overrange condition. Reset by control Bit 4.
3–0	X	Not defined.

SAMPLE-AND-HOLD AMPLIFIERS

The four sample and hold amplifiers internal to the AD1334 combine precision high speed amplifiers and switches together with laser trimmed thin-film resistors to offer a performance and power efficient front end for multichannel applications. Each sample-and-hold amplifier is designed to minimize the effects of dc and ac error sources in simultaneous as well as independent sampling applications.

Operational Description

The sample and hold amplifier architecture is based on an integrator which results in a relatively low input impedance (2.5kΩ) and an acquisition time of 7.5μs (maximum). DC error sources are specified and controlled through the use of precision amplifiers, low leakage switches and package-level laser trimming of thin-film resistors.

Group delay is specified and controlled through the use of trimmed thin-film resistors, tight-tolerance hold capacitors and high speed amplifiers. Aperture delay is specified and controlled through the use of high speed CMOS logic and DMOS switches. The effective aperture delay, which is the delay seen by the user, is therefore controlled from channel to channel and from device to device. The effective aperture delay is negative because the held value corresponds to a value of input voltage that occurred before the amplifier was put into hold mode.

In applications where endpoint (+FS and −FS) accuracy is critical, the source impedance should be minimized because each ohm will typically change the gain of the sample and hold amplifier by 0.04%. This should not be a problem in most cases because the low impedance output of either a programmable gain amplifier or antialiasing filter will be connected to each of the AD1334's analog inputs.

CHANNEL CONTROLLER

The AD1334 Channel Controller enables the AD1334 to appear as four independent channels of analog input by generating all of the timing necessary to ensure that the sampled channel is digitized to 12-bit accuracy. Upon receipt of a sample command, the controller will immediately place the sample-and-hold amplifier into hold mode and then prioritize and schedule the held value for A/D conversion. At the appropriate time, the sampled input is gated through the multiplexer and, after settling, is digitized by the A/D converter. The sample-and-hold amplifier is then returned to sample mode so that it can acquire the next sample.

Operational Description

Timing is initiated on the rising edge of SAMPLE 0–3 control inputs. To minimize the effects of digital feedthrough from the control inputs, it is recommended that the falling edge occur before sample-and-hold acquisition (sample-and-holds have a maximum 7.5μs acquisition time) and after the A/D conversion is complete.

CONTROL $\overline{\text{ENB}}$ functions as an "on/off" switch for the controller and is both an input and an open drain output. The controller can therefore be activated either through the microprocessor interface (via control register Bit 7) or externally by an open drain driver (such as the 74HC03). The controller can also be permanently enabled by grounding CONTROL $\overline{\text{ENB}}$. The timing for enabling and disabling the controller as described above is shown in Figure 14.

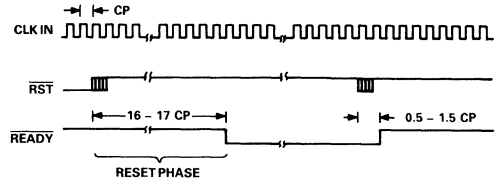


Figure 14a. Timing Diagram for Resetting Controller (CONTROL $\overline{ENB} = 0$)

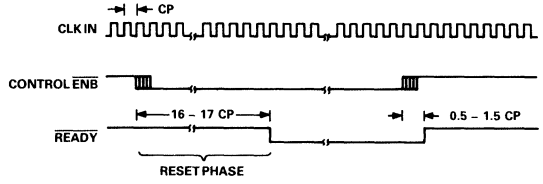


Figure 14b. Timing Diagram for Enabling Controller ($\overline{RST} = 1$)

The channel controller also adds 2 bits (D12 and D13) of data to each A/D conversion result for channel identification. Table I summarizes this relationship.

D13	D12	A/D Conversion Results From
0	0	Channel 0
0	1	1
1	0	2
1	1	3

Table I.

Two timing modes are available for sampling and converting each or all of the analog inputs. (Note – The timing diagrams shown refer to Channels "A,B,C,D" rather than "0,1,2,3." This was done because each channel is completely independent of the other three channels and, in fact, Channel A can be any of Channels 0, 1, 2 or 3, Channel B can be any of Channels 0, 1, 2 or 3, etc.)

Simultaneous Mode

Simultaneous mode is selected by connecting the $\overline{\text{SIMULT}}$ pin to logic low. This mode should be used when any 2, 3 or all 4 channels are to be sampled simultaneously (i.e., at the same instant in time). This mode keeps the sample-and-hold amplifiers on the sampled channels in hold mode until the sampled inputs have been digitized and will normally result in better channel-to-channel isolation relative to independent mode. The timing diagram for this mode is shown in Figure 15. Note that $\overline{\text{IRQ}}$ becomes active on the completion of every A/D conversion since the FIFO is not being used.

Prioritizing logic internal to the channel controller can be used to ensure that the channels are converted in a predetermined sequence. Synchronizing the sample control signal (rising edge of SAMPLE 0–3) to either the rising or falling edge of the clock will result in Channel 0 being converted before Channel 1, Channel 1 before Channel 2, and Channel 2 before Channel 3. An obvious advantage to this is that the user can choose to ignore data Bits 12 and 13 (D12 and D13) which carry the channel identification.

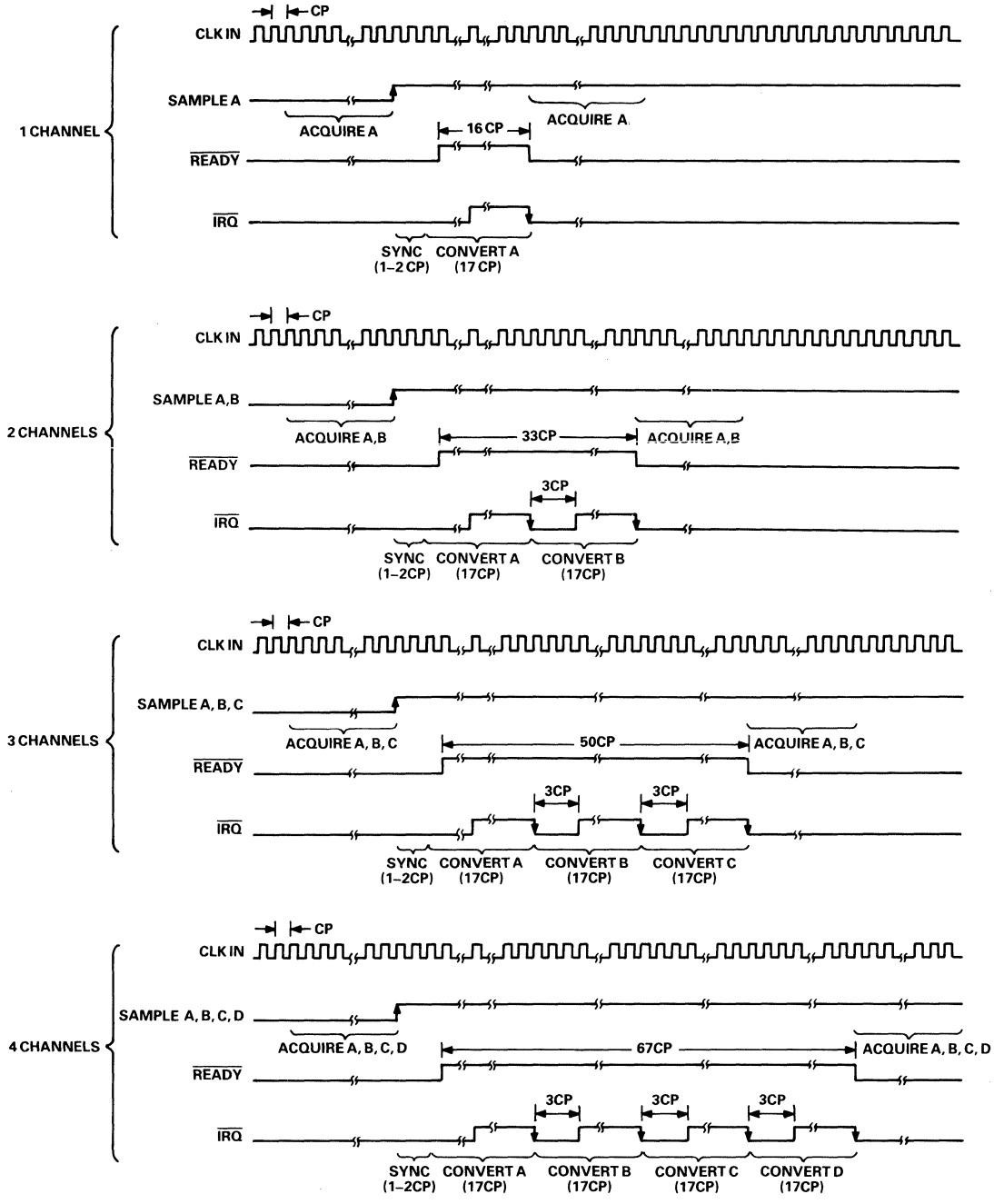


Figure 15. Timing for Simultaneous Sampling ($\overline{SIMULT}$ = Low, FIFO Not Used)

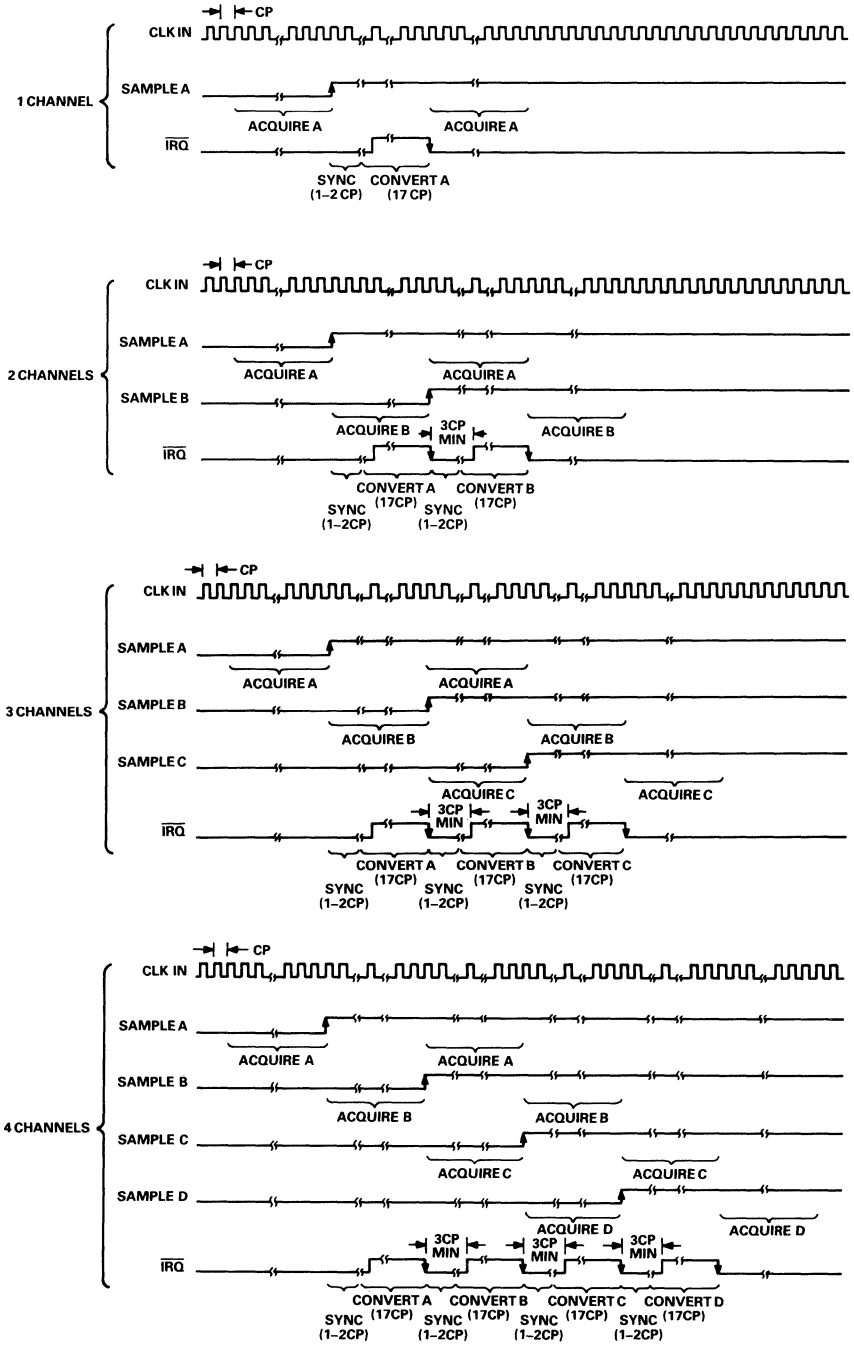


Figure 16. Timing for Independent Sampling ($\overline{SIMULT}$ = High, FIFO Not Used) w/Worst Case Skew of SAMPLE Control Inputs

If the FIFO is used, the falling edge of the $\overline{\text{READY}}$ signal, can be used as an interrupt signal to notify a processor that the 1, 2, 3 or 4 channels have been successfully converted and have been shifted into the FIFO. All conversion results can be read from the FIFO with the exception of the last one, which must fall through to the output (fall-through time is typically 400ns). $\overline{\text{READY}}$ can also be used as a signal to the device generating the sample command that the previous group of samples have been converted and that the next group of samples are being acquired.

Independent Mode

Independent mode is selected by connecting the $\overline{\text{SIMULT}}$ pin to logic high. This mode should be used when any number of channels are sampled independently. In contrast to simultaneous mode, this mode returns the sample-and-hold amplifier on the sampled channel to sample mode when the channel input has been digitized. This mode allows the AD1334 to emulate up to four independent sampling A/D converters, each of which can accommodate different sample rates and hence different signal bandwidths. The timing diagram for this mode is shown in Figure 16. Note that $\overline{\text{IRQ}}$ becomes active on the completion of every A/D conversion since the FIFO is not being used.

The $\overline{\text{READY}}$ signal has no implicit definition in this mode, other than the falling edge indicating that the controller has no conversions pending.

A/D CONVERTER

The analog input voltage range goes from −5V to +5V and the digital output coding is Offset Binary (see Table II). Twos complement coding can be obtained by inverting the MSB (D11).

Center of Code Voltage (V)	Output Code
−5.000000	000 . . . 000
−0.002441	011 . . . 111
0.000000	100 . . . 000
+4.997559	111 . . . 111

Table II. A/D Conversion Relationship

Operational Description

Analog signal information is converted to a 12-bit digital word by sampling the waveform and digitizing it using the successive-approximation conversion technique. Since the clock does not define the amount of time between samples, it need not be crystal controlled. Best performance will be obtained by operating the clock at the maximum 2.5MHz clock frequency.

HIGH SPEED DIGITAL INTERFACE

The AD1334 completes the solution for A/D conversion in DSP applications by providing the system's designer a direct, high speed parallel digital interface. The prime feature of this interface architecture is that it operates completely asynchronously from the A/D converter and therefore allows the AD1334 to appear as "memory" to a microprocessor.

The combination of fully asynchronous operation with respect to the A/D conversion process and fast data access time allows the AD1334 user to upgrade to faster versions, or even different vendors, of DSP hardware without having to add synchronization or wait state logic. In addition, by virtue of hybrid circuit technology, the user is not required to add external circuitry to prevent digital feedthrough into the analog section.

The AD1334 data transfer is accomplished by employing an interrupt driven architecture. Interrupts can be programmed by the microprocessor to be generated when the FIFO is full (32 conversion results), half-full (16 conversion results) or after every conversion (FIFO is bypassed). The AD1334 digital interface also includes an overrange detect circuit, which can generate an interrupt if the sampled analog input signal exceeds positive or negative full scale, to alert the system that a conversion result has been generated that will result in a nonlinearity in the subsequent signal processing.

Operational Description

The AD1334 can interface directly to a microprocessor via standard data (D0 – D13), address (A0) and control lines read ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$, $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$).

Data Transfer

The data lines D0 – D13 are bidirectional I/O that are TTL compatible and have 4mA drive capability. The data lines are used to transfer control information into, and A/D conversion results with status information and channel identification out of the AD1334. Address line A0 is an input that is used to select as the data path either A/D conversion results with channel ID (A0 = 0) or the Control/Status Registers (A0 = 1) and would typically be the least significant address bit in the system if the AD1334 is "mapped" to adjacent memory locations. Chip Select ($\overline{\text{CS}}$) is used to define a unique location in memory for the AD1334 and should be formed by decoding the upper address bits. Read ($\overline{\text{RD}}$) and Write ($\overline{\text{WR}}$) define the type of data transfer.

Figures 17–22 illustrate how the AD1334 interfaces to a number of popular single chip digital signal processors.

Interrupts

Interrupt Request ($\overline{\text{IRQ}}$) is an open drain output that can be used to interrupt the processor on any of the conditions programmed in the control register. $\overline{\text{READY}}$ can be used in simultaneous applications as an alternative processor interrupt signal as described above. In either case, the processor should be programmed to interrupt on the falling edge of its Interrupt Request input.

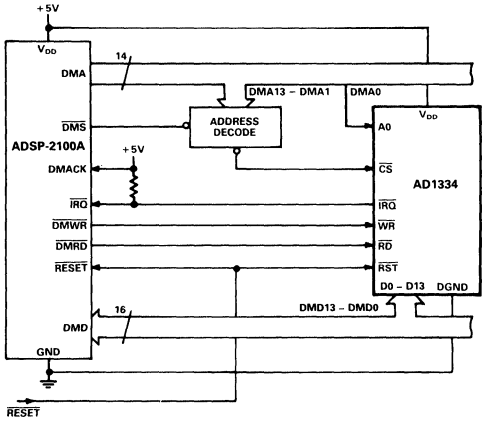


Figure 17. ADSP-2100A to AD1334 Interface

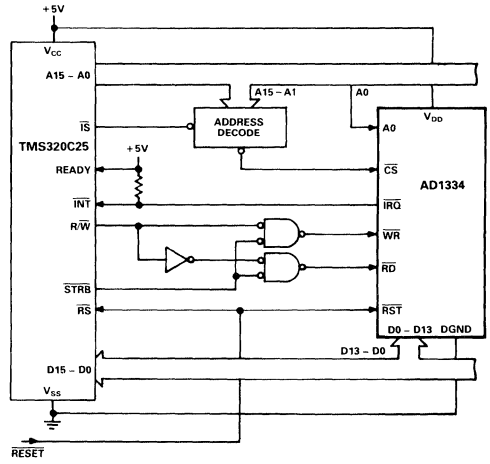


Figure 18. TMS320C25 to AD1334 Interface

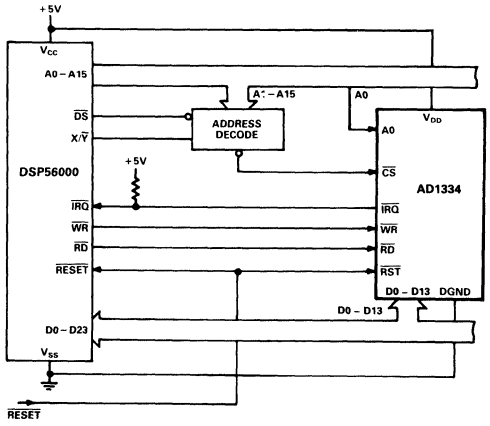


Figure 19. DSP56000 to AD1334 Interface

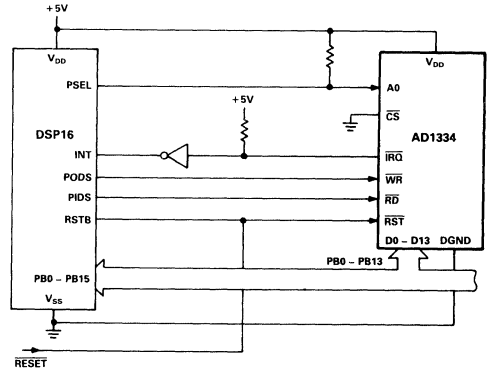


Figure 20. DSP16 to AD1334 Interface

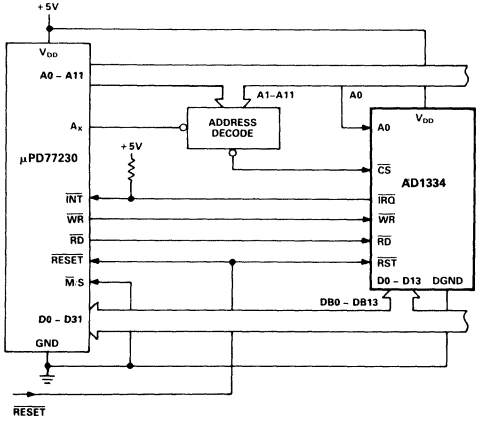


Figure 21. μPD77230 to AD1334 Interface

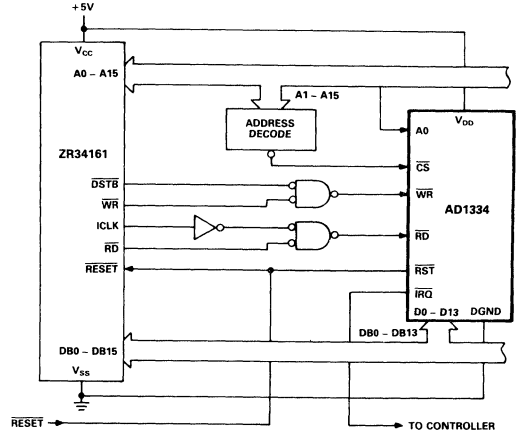


Figure 22. ZR34161 to AD1334 Interface

FIFO Half-Full Interrupt

The timing for interrupts that are generated when the FIFO is half-full is shown in Figures 23a and 23b. In both figures, $\overline{IRQ}$ becomes active when the 16th A/D conversion result is shifted into the FIFO. In Figure 23a, the processor responds immediately and a read cycle takes place before the next conversion cycle begins. Here, the completion of the read cycle shifts the 1st conversion result (which was just read by the processor) out of the FIFO, replaces it with the second conversion result and causes $\overline{IRQ}$ to become inactive since there are now 15 conversion results in the FIFO.

In Figure 23b, the processor does not respond before the next conversion cycle begins and $\overline{IRQ}$ becomes inactive. The FIFO continues to accept conversion results and the processor can read from the FIFO at any time so long as the FIFO has not overrun.

This mode allows the AD1334 to have a low interrupting priority since the processor has up to 17 additional A/D conversions before the FIFO overruns. Therefore, the processor will have up to 260μs to respond at the maximum sample rate of 65kHz.

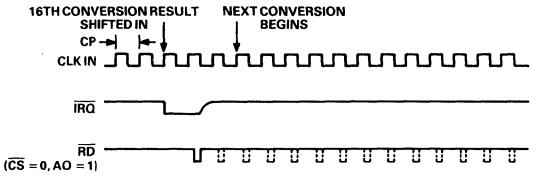


Figure 23a. Timing Diagram for Half-Full Interrupt (Read Before 17th Conversion Started)

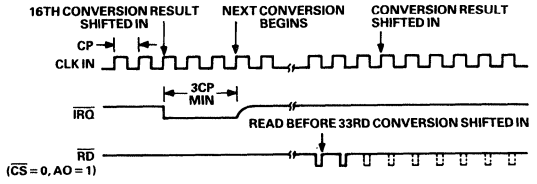


Figure 23b. Timing Diagram for Half-Full Interrupt (Read After 17th Conversion Started)

FIFO Full Interrupt

The timing for interrupts that are generated when the FIFO is full is shown in Figures 24a and 24b. In both figures, $\overline{IRQ}$ becomes active when the 32nd A/D conversion result is shifted into the FIFO. In Figure 24a, the processor responds immediately and a read cycle takes place before the next conversion cycle begins. Here, the completion of the read cycle shifts the first conversion result (which was just read by the processor) out of the FIFO, replaces it with the second conversion result and causes $\overline{IRQ}$ to become inactive because there are now 31 conversion results in the FIFO.

In Figure 24b, the processor does not respond before the next conversion cycle begins and $\overline{IRQ}$ becomes inactive. The processor must read from the FIFO before the completion of the current conversion cycle or the FIFO will overrun. This mode maximizes the memory capability of the AD1334 but requires a fairly high interrupting priority in the processor since the processor has only one A/D conversion before the FIFO overruns. Therefore, the processor will have only 15μs to respond at the maximum sample rate of 65kHz.

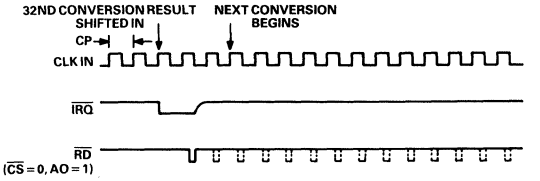


Figure 24a. Timing Diagram for Full Interrupt (Read Before 33rd Conversion Started)

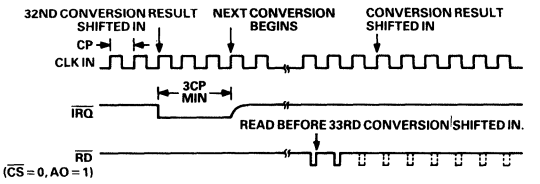


Figure 24b.Timing Diagram for Full Interrupt (Read After 33rd Conversion Started)

Conversion Results Overrange Interrupt

If the FIFO is used, the AD1334 can be programmed to generate interrupts when overranged conversion results are shifted into the FIFO. If $\overline{IRQ}$ became active as a result of an overrange condition, the only way it can become inactive is to clear Bit 4 of the control register. Typically, the user should clear the entire control register which will, in effect, remove the interrupt, reset the FIFO and disable the controller.

Should the overrange interrupt capability be used, Status Register Bits 4 and 6 can be used to identify whether the interrupt occurred as a result of an overrange condition or FIFO half-full (or full).

Single Conversion Interrupt (FIFO Bypassed)

The timing for interrupts that are generated when the FIFO is bypassed is shown in Figures 15 and 16. Here, $\overline{IRQ}$ becomes active at the completion of each A/D conversion cycle. $\overline{IRQ}$ remains active, independent of the read cycle, until the next conversion cycle begins, which is a minimum of three clock periods (1.2μs with 2.5MHz clock). Data is valid so long as $\overline{IRQ}$ remains active.

This mode makes data available immediately after the conversion process has been completed and is therefore very similar to the operation of a conventional A/D converter if $\overline{IRQ}$ is taken to mean conversion STATUS. This mode is most useful when a single conversion result is necessary to adjust a system parameter, such as the gain of a PGA that may be in front of an AD1334.

Since $\overline{IRQ}$ will only be valid for only three A/D clock periods (1.2μs with a 2.5MHz clock), a high interrupting priority should be assigned by the processor. Should the single conversion result be necessary to adjust a system parameter as described above, it may be more efficient to "poll" the Status Register to determine when the conversion result is available.

Operation Other Than with a Microprocessor

The AD1334 can be used in other than microprocessor environments by grounding pins 11, 12 and 29 ($\overline{CS}$, A0 and $\overline{RD}$), connecting Pin 30 ($\overline{WR}$) to V_{DD} and pulsing $\overline{RST}$ low. This will permanently enable the AD1334 three-state outputs and clear the control register, causing the FIFO to be bypassed.

Multiple AD1334s

The architecture of the AD1334 allows multiple devices to be used in a microprocessor based system. Figure 25 illustrates how four AD1334s can be configured to simultaneously sample their analog inputs and reside in eight sequential locations in a microprocessor's memory address space. The control register of each device should be programmed to interrupt on the same condition so that the same number of conversion results are available from all devices.

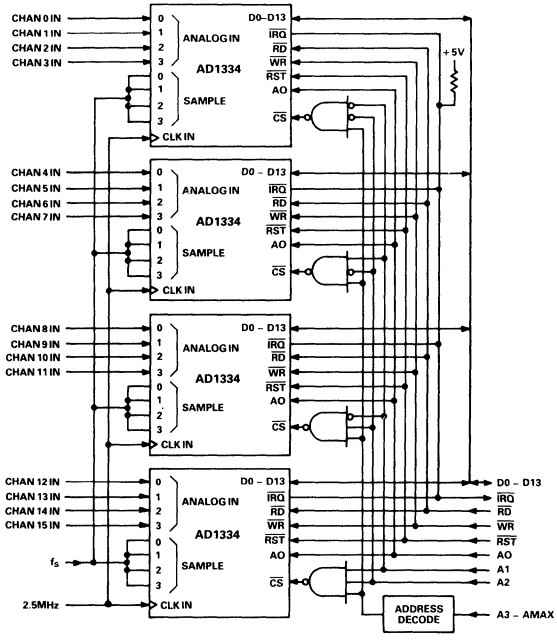


Figure 25. Sixteen-Channel Simultaneous Sampling System

Floating Point Converter

Figure 26 illustrates how to boost the dynamic range of the AD1334 by including it in a floating point A/D converter architecture. The AD526 is a single-ended programmable gain amplifier with gains of 1,2,4,8 and 16. Here, four AD526s are "hardwired" into gains of 1,2,4 and 8 to extend the dynamic range of the AD1334 to 15 bits. Fully differential inputs with gains up to 500 can be obtained by substituting the AD365 for the AD526.

The AD1334 is operated in simultaneous mode, with one AD526 per channel. Upon receipt of a sample command, the four channels are sampled and converted. Table III summarizes the input voltage range for each channel.

Channel	Input Voltage Range
0	−5V to +5V
1	−2.5V to +2.5V
2	−1.25V to +1.25V
3	−625mV to +625mV

Table III.

For each group of four samples, a processor can be used to discard the three A/D conversion results that were not converted on the optimum range. The system shown can provide results at sample rates up to 28kHz.

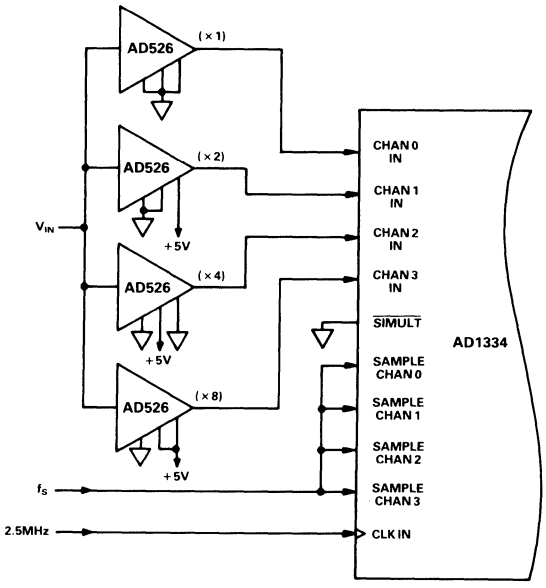


Figure 26. Fifteen-Bit Floating Point A/D Converter

SUCCESSFULLY APPLYING THE AD1334

Grounding

In order to obtain the specified performance of the AD1334, proper grounding and power supply decoupling techniques must be observed. First, it is imperative that a ground plane be used. A ground plane provides a low resistance, low inductance path for currents to flow back to their source. Without a ground plane, currents will return to the source in such a way as to minimize the energy of the system and therefore parasitic inductances will exist in such undesirable locations as power supply lines and signal grounds.

Second, all three ground connections on the AD1334 must be tied together to the ground plane. The AD1334 APWR GND (Pin 9) carries the imbalance current from the analog power supplies ($\pm V_S$). APWR GND is also connected to the package seal ring/lid and therefore can cause coupling between the analog and digital sections if it is not tied directly to the ground plane.

ASIG GND (Pin 8) is the signal ground internal to the AD1334 and is "common" for the −5V reference, sample-and-hold amplifiers, multiplexer and A/D converter. The current that flows through this pin from the A/D converter is a dynamic current that changes on every clock cycle. Inductance in this trace will therefore cause a reduction in performance in the entire analog section.

DGND (Pin 20) is a separate ground connection for the digital interface chip. It carries a dynamic current every time a digital output changes state, and inductance in the trace that connects to this pin will reduce the noise margin between the A/D converter and the digital interface chip.

Power Supply Decoupling

The power supply decoupling capacitors supply the instantaneous current to the AD1334 and also provide some high frequency filtering. The filtering aspect of the capacitors should not be counted on however, and the user should make every effort to supply quiet, well regulated power supplies to the AD1334. Switching mode power supplies are not recommended for the analog power supplies $\pm V_S$.

Decoupling capacitors should be placed as close to the device as possible to minimize inductances in power supply traces. A 2.2μF (or greater) solid tantalum capacitor in parallel with a 0.1μF ceramic capacitor should be used for decoupling each $+V_S$ and $-V_S$. A 1.0μF (or greater) solid tantalum capacitor should be used for decoupling V_{DD}.

Transmission Line Effects

The digital interface has 10K ECL speed and with 15pF loading exhibits a typical edge rate of 1.4ns. High speed CMOS systems that incorporate the AD1334 must use careful PCB layout and impedance matching techniques to reduce crosstalk and voltage reflections.

Crosstalk

The fast edge rates with large voltage swings of CMOS systems can result in capacitive and inductive coupling (crosstalk) between adjacent PCB signal traces and may compromise signal integrity and reduce noise margins. The effect can be most severe on data lines that are near "clocked" control lines, such as Read, Write and Chip Select lines, when they actually change their logic state as a result of crosstalk.

To reduce crosstalk, the PCB layout should minimize long parallel traces. If this can not be avoided, clock lines should be shielded from data and address lines by running ground traces along side them.

Voltage Reflections

The gross impedance mismatch between high impedance CMOS inputs and low impedance CMOS outputs invites unwanted voltage reflections and "ringing" that can also compromise signal integrity and reduce noise margins. This level of mismatch causes a nearly equal and opposite negative pulse to be reflected back from the load to the source when the round trip delay of the line exceeds the rise or fall time of the driving signal. For a typical line delay of 0.055ns/cm with a 1.4ns edge rate, this translates to only 13cm (5 inches) for the AD1334. Provided the signal lines are over a ground plane, this may never be a problem since the added capacitance will reduce the edge rate.

The effect will be most severe on "clock" lines in synchronous systems such as Read, Write and Chip Select lines. For example, should the AD1334 Read control input ($\overline{RD}$) be double clocked as a result of a reflection while in a read cycle, in most cases the digital interface chip will be fast enough to respond. If the FIFO is being read from, a second shift out will occur and A/D conversion results will be lost.

Since CMOS output stages are not capable of delivering enough current to the load when a transmission line (PCB trace) is terminated in its characteristic impedance, series damping is recommended when reflections must be reduced or eliminated. Here, a small resistor (typically 10Ω to 75Ω) is inserted in series with the transmission line as close to the source as possible. The goal is to match the series resistance plus driver output impedance to the transmission line impedance. This will keep the wave that is reflected back from the load to source from reflecting back to the load.

The primary disadvantage of series termination is that due to the voltage divider formed by the source resistance and line impedance, the voltage at the input to the line is midway between logic levels during the two-way propagation delay time. This means that although any number of device inputs may be attached at the load end, other device inputs cannot be distributed along the transmission line.

REFERENCES

Cypress Semiconductor, CMOS Data Book, Cypress Semiconductor, 1987.

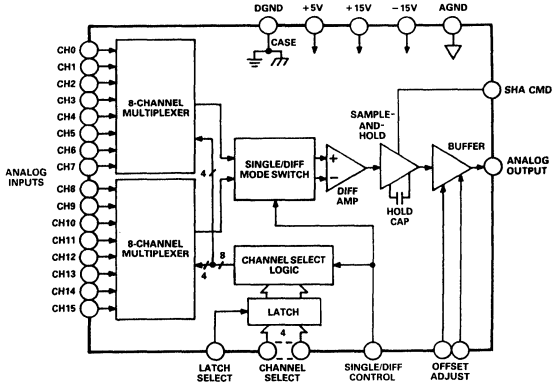
16-Channel, 12-Bit Data Acquisition System

AD1362

FEATURES

- **Pin and Functional Replacement for AD362:**
  - **Lower Power Dissipation**
  - **Lower Noise**
  - **Internal Hold Capacitor**
- **16 Single-Ended or 8 Differential Channels with Switchable Mode Control**
- **True 12-Bit Precision: Nonlinearity ≤0.005%**
- **High Speed: 10μs Acquisition Time to 0.01%**
- **Complete and Calibrated: No Additional Parts Required**
- **Versatile: Simple Interface to Popular Analog-to-Digital Converters**
- **High Differential Input Impedance ($10^{10}\Omega$) and Common Mode Rejection (80dB)**
- **Fully Protected Multiplexer Inputs**

AD1362 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1362 is a complete, precision16-channel data acquisition system. The device contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD1362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

The sample-and-hold mode control is designed to connect directly to the "Status" output of an analog-to-digital converter so that a convert command to the ADC will automatically put the sample-and-hold into the "Hold" mode. An internal precision hold capacitor is included with each AD1362. The AD1362 output amplifier is capable of driving the unbuffered analog input of most high speed, 12-bit successive-approximation ADCs. The interface is thereby reduced to two simple connections with no additional components required.

The AD1362KD is specified for operation over a 0 to +70°C temperature range while the AD1362SD operates to specification from −55°C to +125°C. Processing to MIL-STD-883, Class B is available for the AD1362SD. Both grades are packaged in a hermetic 32-pin ceramic dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD1362, when used with a precision analog to digital converter, forms a complete, accurate, high-speed data acquisition system.
2. The 16-input channels may be configured in single-ended, differential or a mixture of both modes. Mode switching is provided by a user controllable internal analog switch.
3. Multiplexers, differential amplifier, sample-and-hold and high-speed output buffer provide complete analog interfacing capabilities.
4. Internal channel address latches are provided to facilitate interfacing the AD1362 to data, address or control buses.
5. The AD1362 is specified over the entire military temperature range, −55°C to +125°C. Processing to MIL-STD-883, Class B is available.

9

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

Parameter	Test Condition	AD1362KD Min	AD1362KD Typ	AD1362KD Max	AD1362SD Min	AD1362SD Typ	AD1362SD Max	Units
ANALOG INPUTS								
Input Voltage Range	T_{min} to T_{max}	−10		+10	*		*	V
Input Bias Current	Per Channel			±50			*	nA
Input Impedance	On Channel		10			*		GΩ
			100			*		pF
	Off Channel		10			*		GΩ
			10			*		pF
Input Fault Current	Power Off or On			20			*	mA
Common Mode Rejection	Diff Mode, 1kHz, 20V p-p	70	80		*	*		dB
Mux Crosstalk, Any Off Ch to Any On Ch	1kHz, 20V p-p	−80	−90		*	*		dB
Ch to Ch Offset				±2.5			*	mV
ACCURACY								
Gain Error	T_{min} to T_{max}			±0.02			*	% FSR
Offset Error	T_{min} to T_{max}			±4			*	mV
Linearity Error	@ 25°C			±0.005			*	%
	T_{min} to T_{max}			±0.01			*	%
Noise Error	25°C, 0.1 to 1MHz			0.5			*	mV p-p
	T_{min} to T_{max}, 0.1 to 1MHz			1.0			*	mV p-p
TEMPERATURE COEFFICIENTS								
Gain	T_{min} to T_{max}			±4			±2	ppm/°C
Offset	±10V Range, T_{min} to T_{max}			±2			±1.5	ppm/°C
SAMPLE AND HOLD DYNAMICS								
Aperture Delay			150	200		*	*	ns
Aperture Uncertainty			100	500		*	*	ps
Acquisition Time	20V Step to ±0.01%		10	18		*	*	µs
Feedthrough	1kHz		−80	−70		*	*	dB
Droop Rate			1	2		*	*	mV/ms
Pedestal Voltage		−15	11	+15	*	*	*	mV
POWER SUPPLY REQUIREMENTS								
+V, Analog Voltage		+14.25		+15.75	*		*	V
−V, Analog Voltage		−14.25		−14.75	*		*	V
+V, Digital Voltage		+4.75		+5.25	*		*	V
+V, Analog Current				30			*	mA
−V, Analog Current				30			*	mA
+V, Digital Current				40			*	mA
Total Power Dissipation			0.5	1.1			*	W
TEMPERATURE RANGE								
Specification		0		+70	−55		+125	°C
Storage		−55		+85	−55		+150	°C

DIGITAL INPUT SIGNALS

Signal	Pins	TTL[1] Loads	Logic High	Logic Low
Input Channel Select	28-31	1LS	(4-Bit Binary Address)	
Channel Select Latch	32	8LS	Transparent	Latched
Single Ended/Diff Mode Select	1	3LS	Differential	Single Ended
Sample-and-Hold Command	13	2LS	Hold	Sample

NOTE

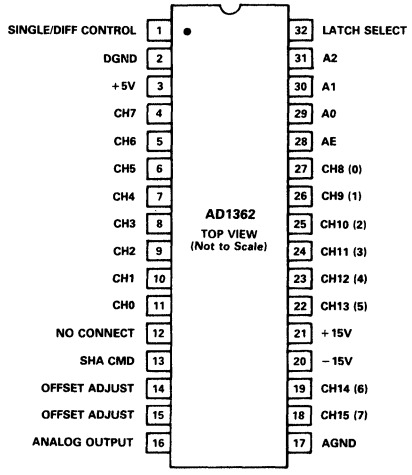
[1]One TTL Load is defined as I_{IL}=−1.6mA max @ V_{IL}=0.4V, I_{IH}=40µA max @ V_{IH}=2.4V. One LSTTL Load is defined as I_{IL}=−0.36mA @ V_{IL}=0.4V, I_{IH}=20µA max @ V_{IH}=2.7V.

*Specifications same as AD1362KD.

ABSOLUTE MAXIMUM RATINGS

+V, Digital Supply . . . . . +5.5V
+V, Analog Supply . . . . . +17V
−V, Analog Supply . . . . . −17V
V_{IN}, Signal . . . . . ±V Analog Supply
V_{IN}, Digital . . . . . 0 to +V, Digital Supply
AGND to DGND . . . . . ±1V

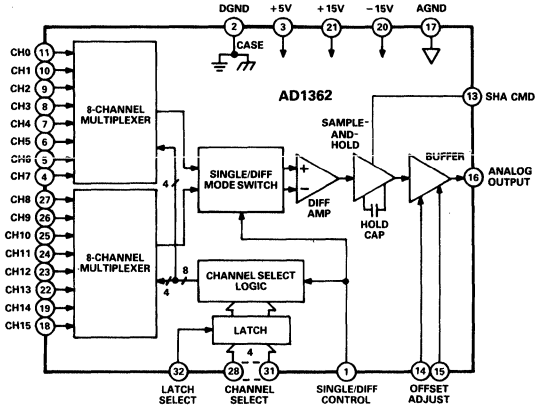
AD1362 PIN ASSIGNMENT



Function	Number	Description
Single/Diff Control	1	Mode Select, Differential or Single Ended
DGND	2	Digital Ground
+5V	3	Digital Power Supply, +5V dc
Ch 7	4	"High" Analog Input Channel 7
Ch 6	5	"High" Analog Input Channel 6
Ch 5	6	"High" Analog Input Channel 5
Ch 4	7	"High" Analog Input Channel 4
Ch 3	8	"High" Analog Input Channel 3
Ch 2	9	"High" Analog Input Channel 2
Ch 1	10	"High" Analog Input Channel 1
Ch 0	11	"High" Analog Input Channel 0
NC	12	No Connect
SHA Cmd	13	Sample/Hold Control Input to SHA
Offset Adjust	14	Offset Adjustment Input #1
Offset Adjust	15	Offset Adjustment Input #2
Analog Output	16	Analog Output to ADC
AGND	17	Analog Ground
Ch 15	18	"High" ("Low") Analog Input Channel 15 (7)
Ch 14	19	"High" ("Low") Analog Input Channel 14 (6)
−15V	20	Negative Analog Power Supply −15V dc
+15V	21	Positive Analog Power Supply +15V dc
Ch 13	22	"High" ("Low") Analog Input Channel 15 (5)
Ch 12	23	"High" ("Low") Analog Input Channel 14 (4)
Ch 11	24	"High" ("Low") Analog Input Channel 13 (3)
Ch 10	25	"High" ("Low") Analog Input Channel 12 (2)
Ch 9	26	"High" ("Low") Analog Input Channel 11 (1)
Ch 8	27	"High" ("Low") Analog Input Channel 10 (0)
AE	28	Input Channel Address MSB
A0	29	Input Channel Address Bit 0
A1	30	Input Channel Address Bit 1
A2	31	Input Channel Address Bit 2
Latch Select	32	Channel Select Latch Control Input

FUNCTIONAL DESCRIPTION

The AD1362 consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high speed output buffer, channel address latches and control logic as shown in the block diagram. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD1362 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single AD1362 to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD1362 by dynamically switching the input mode control.



AD1362 Block Diagram

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Latch Select input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Latch Select input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes.

The sample-and-hold is a high speed device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

The output buffer is a high speed amplifier whose output impedance remains low and constant at high frequencies. Therefore, the AD1362 may drive a fast, unbuffered, precision ADC without loss of accuracy.

THEORY OF OPERATION

Concept

The AD1362 is intended to be used in conjunction with a high speed, precision analog-to-digital converter to form a complete data acquisition system (DAS). Figure 1 shows a general AD1362 with ADC DAS application.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

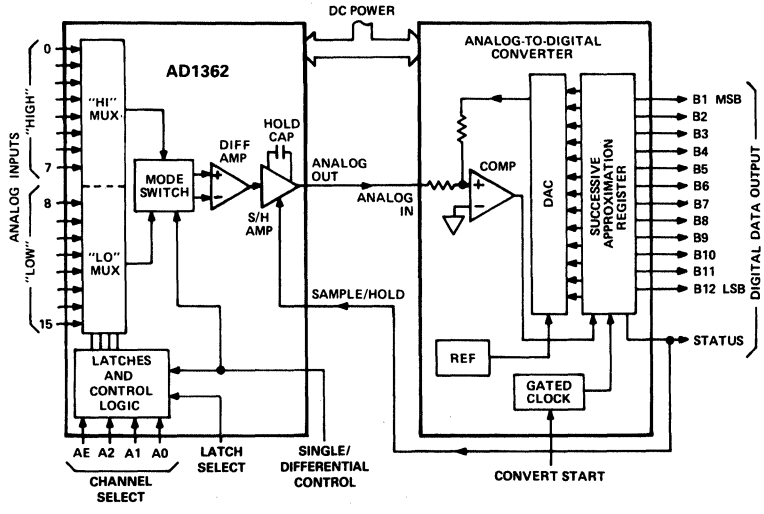


Figure 1. AD1362 with ADC as a Complete Data Acquisition System

System Timing

Figure 2 is a timing diagram for the AD1362 connected as shown in Figure 1 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12-bit type such as the AD573 or AD ADC80.

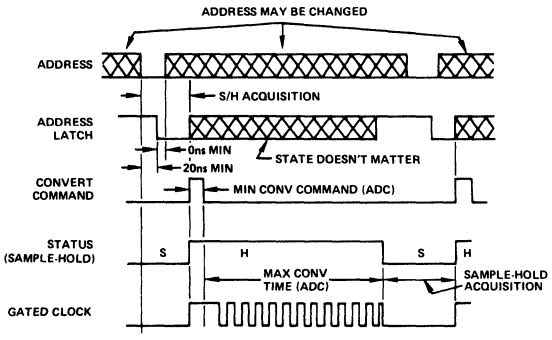


Figure 2. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status Line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy," the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0." The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full scale (different channels may have widely-varying data), the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

NOTE

Valid Output Data

Not all ADCs have all data bits available when Status indicates that the conversion is complete. Some successive approximation ADCs must have a Status delay built in or the final data bit will lag Status. This will result in two problems:

1. The sample-and-hold will return to Sample, disturbing the analog input to the ADC as it is attempting to convert the least significant bit. This may result in an error.
2. If the falling edge of Status is being used to load the data into a register, the least significant bit will not be valid when loaded.

An external delay or use of an ADC with a valid Status output is necessary to prevent this problem.

Single-Ended/Differential Mode Control

The AD1362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to Pin 1:

"0": Single-Ended (16 channels)
"1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Channel Select address bits, AE, A0, A1, A2 (Pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1, and A2; AE must be enabled with a Logic "1." Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0	None	
0	0	0	1	1	None	
0	0	1	0	2	None	
0	0	1	1	3	None	
0	1	0	0	4	None	
0	1	0	1	5	None	
0	1	1	0	6	None	
0	1	1	1	7	None	
1	0	0	0	8	0	0
1	0	0	1	9	1	1
1	0	1	0	10	2	2
1	0	1	1	11	3	3
1	1	0	0	12	4	5
1	1	0	1	13	5	5
1	1	1	0	14	6	6
1	1	1	1	15	7	7

Table I. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the AD1362 to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

Input Channel Address Latch

The AD1362 is equipped with a latch for the input Channel Select address bits. If the Latch Select pin is at Logic "1," input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input is normally connected to the Status output from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1" putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this applicataion, it also allows the user to change channels and/or SE/DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous Sample mode.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AD1362 may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Data Acquisition System. An example of such a case would be if the input signals were small (<10mV) relative to AD1362 offset and gain errors. To adjust the offset of the AD1362, the circuit shown in Figure 3 is recommended.

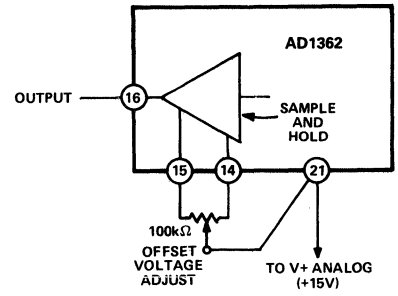


Figure 3. AD1362 Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground and Digital Ground are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD1362 as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AD1362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 4. This will protect the AD1362 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200mV between grounds; however, this difference will be reflected directly as an input offset voltage.

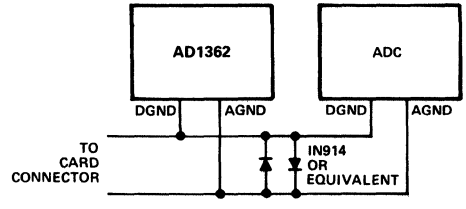


Figure 4. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. One microfarad tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disk capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Interfacing to Popular Analog to Digital Converters

The AD1362 has been designed to interface directly to most analog to digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made.
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

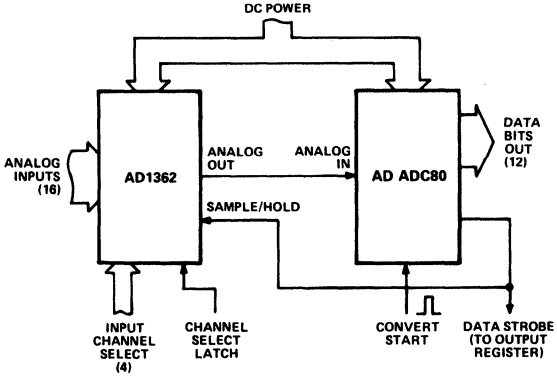
Complete system throughput performance is determined by combining the worst-case specifications of the AD1362 and the ADC. If guaranteed system performance is required, the AD363 and AD364 are recommended. The AD363 includes an AD1362 and an AD572 12-bit, 25-microsecond precision ADC. The AD364 consists of an AD1362 and an AD574 12-bit, microprocessor compatible, low cost ADC. Each is specified as a complete, two-package system.

Figure 5a shows the AD1362 driving an AD ADC80. The AD ADC80 is a 12-bit, 25-microsecond, low cost ADC that meets all of the requirements listed above. Throughput rate is typically 30kHz with no missing codes over the operating temperature range.

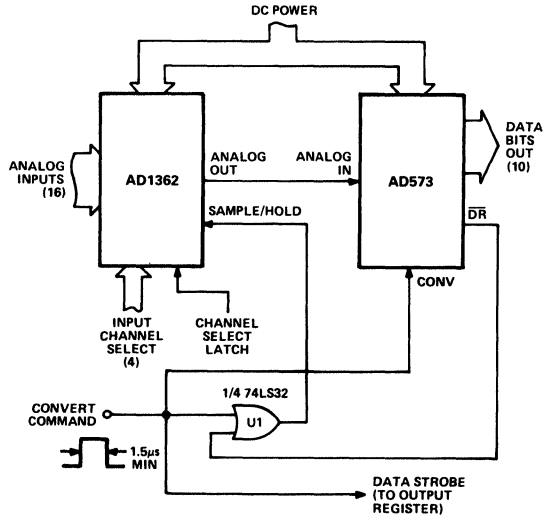
Figure 5b shows a 10-bit application based on the AD1362 and the AD573, a complete low cost 10-bit, 25-microsecond ADC. In this case, one of the above requirements is not met:

1. $\overline{DR}$ ($\overline{DATA\ READY}$), as Status, is positive-true, but . . .
2. $\overline{DR}$ does not indicate that a conversion is in progress until 1.5μs after conversion starts.

The gating provided by U1 allows the applied convert command (CC) to initiate input hold at the AD1362. CC must last for more than 1.5μs so that $\overline{DR}$ may then assume control of Hold.



a. 12-Bit DAS Using AD1362 and AD ADC80



b. 10-Bit Using AD1362 and AD573

Figure 5. Data Acquisition Systsems Based on the AD1362 and Popular ADCs

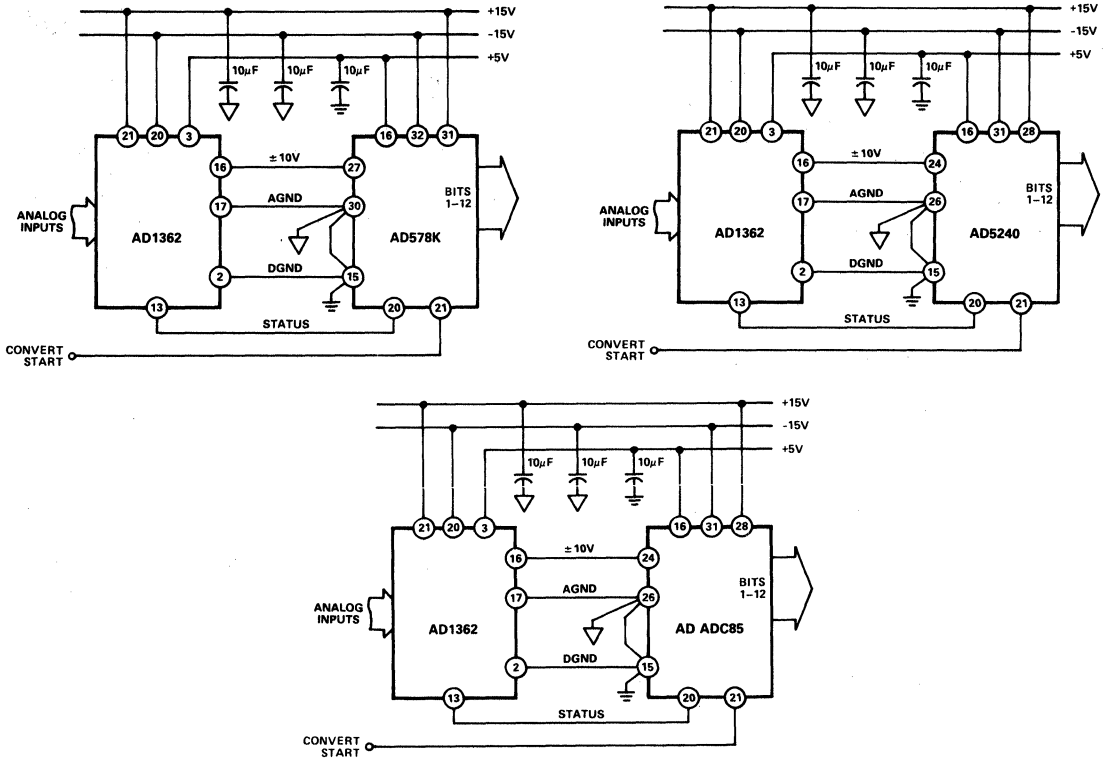


Figure 6. High Speed Data Acquisition Systems Based on AD1362 and Fast ADCs.

AD1362 ORDERING GUIDE

Model	Specification Temperature Range	Max Gain TC	Package Options*
AD1362KD	0 to +70°C	±4ppm/°C	DH–32E
AD1362SD	−55°C to +125°C	±2ppm/°C	DH–32E
AD1362SD/883B	−55°C to +125°C	±2ppm/°C	DH–32E

*See Section 14 for package outline information.

14-Bit & 15-Bit Sampling Analog-to-Digital Converters

DAS1152/DAS1153

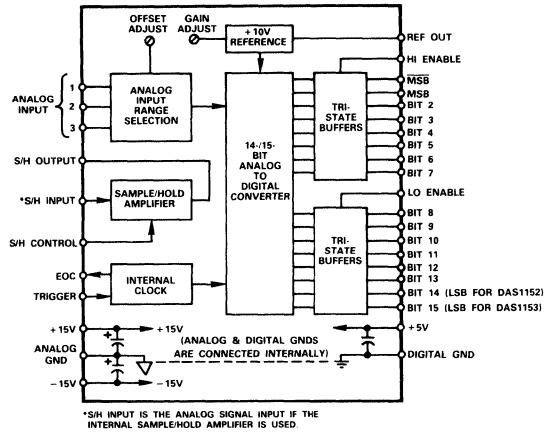
FEATURES

- **Complete with High Accuracy Sample/Hold and A/D Converter**
- **Differential Nonlinearity: ±0.002% FSR max (DAS1153)**
- **Nonlinearity: DAS1152: ±0.005% FSR max**
  DAS1153: ±0.003% FSR max
- **Low Differential Nonlinearity T.C.: ±2ppm/°C max**
- **High Throughput Rate: 25kHz min (DAS1152)**
- **High Feedthrough Rejection: −96dB**
- **Byte-Selectable Tri-State Buffered Outputs**
- **Internal Gain & Offset Potentiometers**
- **Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules**

APPLICATIONS

- **Process Control Data Acquisition**
- **Automated Test Equipment**
- **Seismic Data Acquisition**
- **Nuclear Instrumentation**
- **Medical Instrumentation**
- **Robotics**

DAS1152/DAS1153 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAS1152/DAS1153 are 14-/15-bit sampling analog-to-digital converters having a maximum throughput rate of 25kHz/20kHz. They provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1152)/±0.003% FSR (DAS1153) and differential nonlinearity of ±0.003% FSR (DAS1152)/±0.002% FSR (DAS1153) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C (DAS1153) maximum, zero T.C. of ±80μV/°C maximum, gain T. C. of ±8ppm/°C maximum and power supply sensitivity of ±0.001% FSR/% V_S are also provided by the DAS1152/DAS1153.

The DAS1152/DAS1153 make extensive use of both integrated circuit and thin film components to obtain their excellent performance, small size, and low cost. The devices contain a precision sample/hold amplifier, high accuracy 14-/15-bit analog-to-digital converter, tri-state output buffers, internal gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

Four analog input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V, and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement. Tri-state buffers provide easy interface to bus structured applications.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

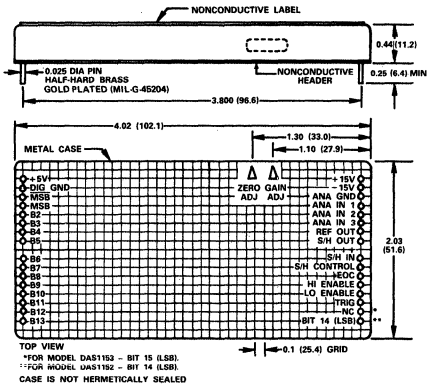
MODEL	DAS1152	DAS1153
RESOLUTION	14 Bits	15 Bits
DYNAMIC PERFORMANCE		
Throughput Rate	25kHz min	20kHz min
Conversion Time	35μs max	44μs max
S/H Acquisition Time	4μs max	5μs max
S/H Aperture Delay	50ns	*
S/H Aperture Uncertainty	1ns	*
Feedthrough Rejection[1]	−96dB	*
Droop Rate	0.05μV/μs (0.1μV/μs max)	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*
ACCURACY		
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max
Differential Nonlinearity	±0.003% FSR[3] max	±0.002% FSR[3] max
No Missing Codes	Guaranteed	*
±3σ Noise (S/H plus A/D)	75μV rms	*
±3σ Noise (A/D)	50μV rms	*
STABILITY		
Differential Nonlinearity T.C.	±2ppm/°C max	*
Gain T.C.	±8ppm/°C max	*
Zero T.C.	±30μV/°C typ, ±80μV/°C max	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_s	*
ANALOG INPUT		
Voltage Range		
Bipolar	±5V, ±10V	*
Unipolar	0 to +5V, 0 to +10V	*
ADC Input Impedance 0 to +5V	2.5kΩ	*
0 to +10V, ±5V	5kΩ	*
±10V	10.0kΩ	*
S/H Input Impedance	100MΩ|5pF	*
DIGITAL INPUTS		
Convert Command[4]	1TTL Load, Positive Pulse	*
	Negative Edge Triggered	*
S/H Control	HOLD = Logic 0	*
	SAMPLE = Logic 1	*
Low Enable, High Enable	ENABLE = Logic 0	*
DIGITAL OUTPUTS		
Parallel Data Outputs		
Unipolar	Binary	*
Bipolar	Offset Binary, 2's Complement	*
Output Drive	2TTL Loads	*
Status	Logic "1" During Conversion	*
Output Drive	2TTL Loads	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*
External Load Current (Rated Performance)	2mA max	*
Temperature Stability	±5ppm/°C max	*
POWER REQUIREMENTS		
Rated Voltages	±15V (±3%), +5V (±5%)	*
Operating Voltages[5]	±12V to +17V, +4.75V to +5.25V	*
Supply Current Drain ±15V	±37mA	*
+5V	80mA	*
TEMPERATURE RANGE		
Specified	0 to +70°C	*
Operating	−25°C to +85°C	*
Storage	−25°C to +85°C	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*
Shielding	Electrostatic (RFI) 6 Sides,	*
	Electromagnetic (EMI) 5 Sides	*
SIZE	2" × 4" × 0.44" Metal Package	*

NOTES
*Specifications same as DAS1152
[1]Measured in hold mode, input 20V pk-pk @ 10kHz.
[2]Worst-case summation of S/H and A/D nonlinearity errors.
[3]FSR means Full Scale Range.
[4]When connecting the Convert Command and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4μs (max, DAS1152)/5μs (max, DAS1153). If the A/D converter is only used, the Convert Command pulse width should be 100ns min (see Figure 2).
[5]If only the ADC portion is used, the operating power supply voltage can be maintained at ±12V to ±17V. But if the S/H section is required, the operating voltage must be maintained at ±15V (±3%) or the S/H input voltage must be limited to −7V to +10V for a ±12V supply voltage.
[6]Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



OPERATION

The DAS1152/DAS1153 are functionally complete data acquisition subsystems being fully characterized as such. All the necessary data acquisition and microprocessor interface elements are provided internal to these devices. Accuracy and performance criteria are tested and specified for the entire system. Thus, design time and associated high accuracy problems are minimized because layout and component optimization have already been performed.

For operation, the only connections necessary to the DAS1152/DAS1153 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table I. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Table I. Analog Input Pin Programming

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

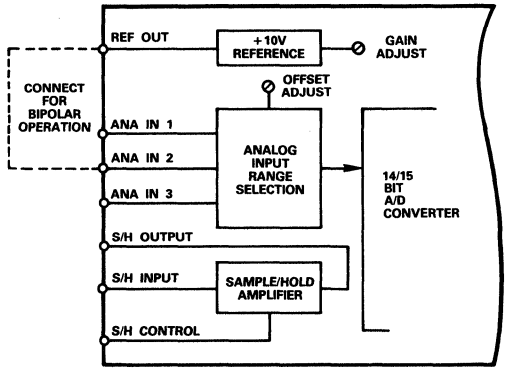


Figure 2. Analog Input Block Diagram

TIMING DIAGRAM

The timing diagram for the DAS1152/DAS1153 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 4μs (DAS1152)/5μs (DAS1153) to insure accuracy is attained. If the sample/hold amplifier is not used, the trigger pulse needs to be only 100ns (min) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking 35μs/44μs maximum for the DAS1152/DAS1153 respectively. At this time, the STATUS line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

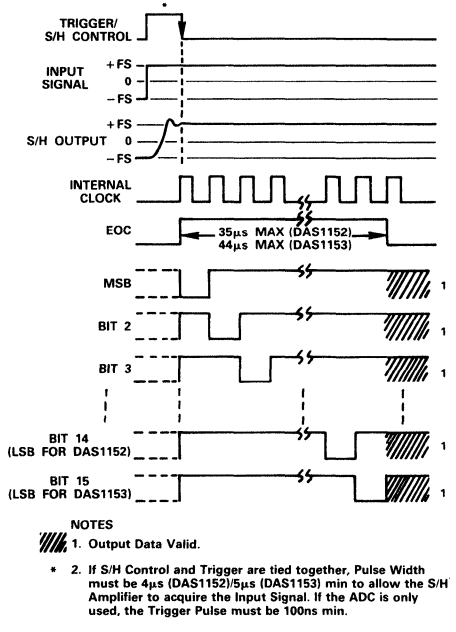


Figure 3. DAS1152/DAS1153 Timing Diagram

GAIN AND OFFSET ADJUSTMENT

The DAS1152/DAS1153 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ± 1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a 0 to +5V unipolar range set the input to +153μV for the DAS1152 and +76μV for the DAS1153. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001.

For the ±5V bipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a ±10V bipolar range set the input voltage precisely to +610μV for the DAS1152 and +305μV for the DAS1153. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1152)/ +9.99954V (DAS1153) for the 0 to +10V units, +4.99954V (DAS1152)/+4.99977V (DAS1153) for 0 to +5V units, +9.99817V (DAS1152)/+9.99909V (DAS1153) for ±10V units, or +4.99909V (DAS1152)/+4.99954V (DAS1153) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1152/DAS1153 INPUT/OUTPUT RELATIONSHIPS

The DAS1152/DAS1153 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ($\overline{\text{MSB}}$) is used to obtain two's complement coding. Table II shows the DAS1152/DAS1153 unipolar analog input/digital output relationships. Tables III and IV show the DAS1152/DAS1153 bipolar analog input/digital output relationships.

NOMINAL BIPOLAR INPUT-OUTPUT RELATIONSHIPS

ANALOG INPUT			
0 to +5V Range		0 to +10V Range	
DAS1152	DAS1153	DAS1152	DAS1153
+4.99969V	+4.99984V	+9.99939V	+9.99969V
+2.50000V	+2.50000V	+5.0000V	+5.00000V
+0.62500V	+0.62500V	+1.25000V	+1.25000V
+0.0003V	+0.00015V	+0.0006V	+0.0003V
+0.0000V	+0.0000V	+0.0000V	+0.0000V

DIGITAL OUTPUT	
Binary Code	
DAS1152	DAS1153
11 111 111 111 111	111 111 111 111 111
10 000 000 000 000	100 000 000 000 000
00 100 000 000 000	001 000 000 000 000
00 000 000 000 001	000 000 000 000 001
00 000 000 000 000	000 000 000 000 000

Table II. Unipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99939V	+9.99878V	11 111 111 111 111	01 111 111 111 111
+2.50000V	+5.0000V	11 000 000 000 000	01 000 000 000 000
+0.00061V	+0.00122V	10 000 000 000 001	00 000 000 000 001
+0.00000V	+0.00000V	10 000 000 000 000	00 000 000 000 000
−5.00000V	−10.00000V	00 000 000 000 000	10 000 000 000 000

Table III. DAS1152 Bipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99969V	+9.99939V	111 111 111 111 111	011 111 111 111 111
+2.50000V	+5.0000V	110 000 000 000 000	010 000 000 000 000
+0.0003V	+0.00061V	100 000 000 000 001	000 000 000 000 001
+0.00000V	+0.00000V	100 000 000 000 000	000 000 000 000 000
−5.00000V	−10.00000V	000 000 000 000 000	100 000 000 000 000

Table IV. DAS1153 Bipolar Input/Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1152/DAS1153, care must still be taken to provide proper grounding due to the high accuracy nature of these devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1152/DAS1153 terminals.

No power supply decoupling is required since, the DAS1152/ DAS1153, contain high quality tantalum capacitors on each of the power supply inputs to ground.

Low Power 14-Bit, 15-Bit & 16-Bit Sampling Analog-to-Digital Converters

DAS1157/DAS1158/DAS1159

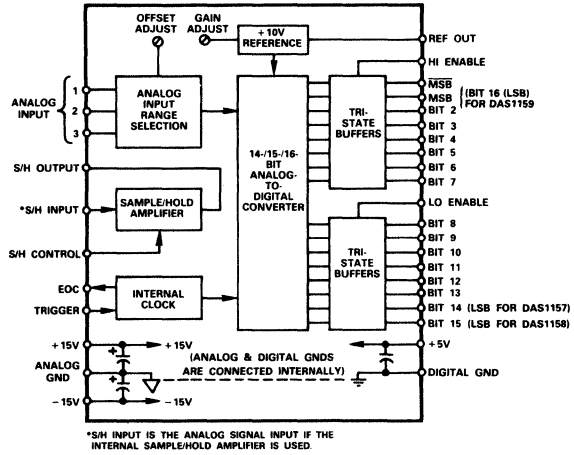
FEATURES

- **Complete with High Accuracy Sample/Hold and A/D Converter**
- **Low Power Consumption: 650mW max, $V_S = \pm 15V$**
- **Rated Performance: −25°C to +85°C**
- **Low Nonlinearity (DAS1158 and DAS1159)**
  - **Differential: ±0.0015% FSR max**
  - **Integral: ±0.003% FSR max**
  - **Differential T.C.: ±1ppm/°C max**
- **High Throughput Rate: 18kHz min**
- **Byte-Selectable Tri-State Buffered Outputs**
- **Internal Gain & Offset Potentiometers**
- **Improved Second Source to A/D/A/M-834 and A/D/A/M-835 Modules**

APPLICATIONS

- **Seismic Data Acquisition**
- **Portable Field Instrumentation**
- **Automated Test Equipment**
- **Process Control Data Acquisition**
- **Medical Instrumentation**

DAS1157/DAS1158/DAS1159
FUNCTIONAL BLOCK DIAGRAM



*S/H INPUT IS THE ANALOG SIGNAL INPUT IF THE INTERNAL SAMPLE/HOLD AMPLIFIER IS USED.

GENERAL DESCRIPTION

The DAS1157/DAS1158/DAS1159 are 14-/15-/16-bit sampling analog-to-digital converters. They are ideally suited for use in portable and remote data acquisition equipment where low power consumption (650mW maximum) and wide temperature range (−25°C to +85°C rated performance) are required.

DAS1157/DAS1158/DAS1159 provide guaranteed high accuracy and high stability system performance essential to medical, analytical and process control equipment: differential nonlinearity of ±0.0015% max and integral nonlinearity of ±0.003% max (DAS1158 and DAS1159); no missing codes guaranteed; gain T.C. of ±8ppm/°C max, zero T.C. of ±80μV/°C max and differential nonlinearity T.C. of ±1ppm/°C max.

The wide dynamic range will enhance the performance of critical measurements in gas and liquid chromatography, blood analyzers, distributed data acquisition in factory automation and power generating equipment, and in automatic test equipment.

The DAS1157/DAS1158/DAS1159 make use of Analog Devices' proprietary CMOS technology to achieve low power operation, while utilizing the latest integrated circuit and thin-film components to achieve the highest level of performance and reliability.

As shown in Figure 1, each device contains a precision sample/hold amplifier, high accuracy 14-/15-/16-bit analog-to-digital converter, precision reference, CMOS tri-state output buffers (for direct 8-bit or 16-bit bus interface), user accessible gain and offset adjust potentiometers, and power supply bypass capacitors, all in a compact low profile 2″ × 4″ × 0.375″ metal case package. No additional components are required for operation.

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SPECIFICATIONS (typical @ +25°C, V_S = ±15V, V_D = +5V unless otherwise specified)

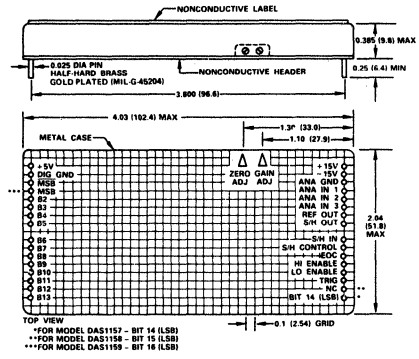
MODEL	DAS1157	DAS1158	DAS1159
RESOLUTION	14 Bits	15 Bits	16 Bits
DYNAMIC PERFORMANCE			
Throughput Rate	18kHz min	*	*
Conversion Time	50µs max	*	*
S/H Acquisition Time	5µs max	*	*
S/H Aperture Delay	250ns	*	*
S/H Aperture Uncertainty	1ns	*	*
Feedthrough Rejection[1]	−90dB min	*	*
Droop Rate	0.05µV/µs, 0.1µV/µs max	*	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*	*
ACCURACY			
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max	**
Differential Nonlinearity[4]	±0.003% FSR[3] max	±0.0015% FSR[3] max	**
No Missing Codes	Guaranteed	*	*
±3σ Noise (S/H plus A/D)	0.0022% p-p (75µV rms)	*	*
±3σ Noise (A/D)	0.0015% p-p (50µV rms)	*	*
STABILITY			
Differential Nonlinearity T.C.	±2ppm/°C max	±1ppm/°C max	**
Gain T.C.	±8ppm/°C max	*	*
Zero T.C.	±30µV/°C typ, ±80µV/°C max	*	*
Conversion Time T.C.	±0.05%/°C	*	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_S	*	*
Warm-Up Time	Less than 1 Minute	*	*
ANALOG INPUT			
Voltage Range			
Bipolar	±5V, ±10V	*	*
Unipolar[4]	0 to +5V, 0 to +10V	*	*
ADC Input Impedance 0 to +5V	2.5kΩ	*	*
0 to +10V, ±5V	5kΩ	*	*
±10V	10kΩ	*	*
S/H Input Impedance	100MΩ‖5pF	*	*
DIGITAL INPUTS			
A/D Trigger[5]	Positive Pulse, Neg. Edge Triggered	*	*
Logic Levels	5V CMOS Compatible	*	*
S/H Control	SAMPLE = Logic 1, TTL Compatible	*	*
Low Enable, High Enable[6]	ENABLE = Logic 0, CMOS/TTL Compatible	*	*
DIGITAL OUTPUTS			
Parallel Data Outputs			
Unipolar	Binary	*	See Note 7
Bipolar	Offset Binary, 2's Complement	*	See Note 7
Output Drive	2TTL Loads	*	*
End of Conversion	Logic "1" During Conversion	*	*
Output Drive	2TTL Loads	*	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*	*
External Load Current (Rated Performance)	2mA max	*	*
POWER REQUIREMENTS			
Rated Voltages	±15V (±3%), +5V (±5%)	*	*
Operating Voltages[8,9]	±12V to ±17V, +4.75V to +5.25V	*	*
Supply Current Drain ±15V	±15mA	*	*
+5V	10mA	*	*
Total Power Consumption, V_S = ±15V	500mW typ, 650mW max	*	*
TEMPERATURE RANGE			
Rated Performance	−25°C to +85°C	*	*
Operating	−25°C to +85°C	*	*
Storage	−40°C to +100°C	*	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*	*
Shielding	Electrostatic (RFI) 6 Sides	*	*
	Electromagnetic (EMI) 5 Sides	*	*
SIZE	2" × 4" × 0.375" Metal Package	*	*

NOTES
*Specifications same as DAS1157
**Specifications same as DAS1158
[1]Measured in hold mode, input 20V pk-pk @ 10kHz.
[2]Worst-case summation of S/H and A/D nonlinearity errors.
[3]FSR means Full Scale Range.
[4]Differential Nonlinearity in the 0 to +5V input range is specified as ±0.003% typical for the DAS1157, DAS1158 and DAS1159.
[5]When connecting the Trigger and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy (5µs min). If the A/D converter only is used, the Trigger pulse width should be 1µs min (see Figure 3).
[6]Low Byte Enable pin connections are Bits 8 through 15; High Byte Enable pin connections are $\overline{MSB}$, MSB or Bit 16 and Bits 2 through 7.
[7]DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only. The MSB must be inverted for binary and offset binary codes.
[8]When the S/H section is required, $-V_S$ must be at least 5 volts more negative than the most negative analog input voltage (example: V_S = ±12V dc, therefore, maximum analog input is +10 and −7V).
[9]Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

OPERATION

For operation, the only connections necessary to the DAS1157/DAS1158/DAS1159 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

Input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement (DAS1157 and DAS1158). DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table I. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Table I. Analog Input Pin Programming

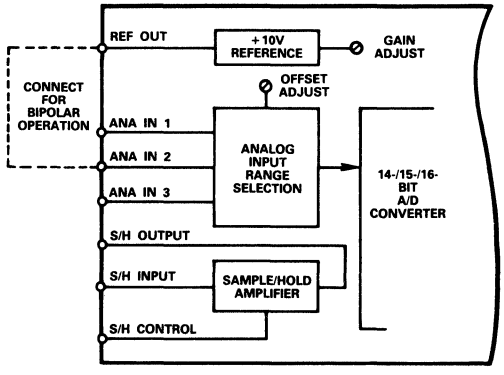


Figure 2. Analog Input Block Diagram

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

TIMING DIAGRAM

The timing diagram for the DAS1157/DAS1158/DAS1159 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 5μs to insure accuracy. If the sample/hold amplifier is not used, the trigger pulse needs to be 1μs (minimum) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, all internal logic is reset and the A/D conversion begins. The conversion process can be retriggered at any time, including during conversion.

With this negative edge of the trigger pulse, the MSB is set high with the remaining digital outputs set to logic low state, and the end of conversion is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched high at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-/16-bit conversion taking 50μs maximum. At this time, the end of conversion line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

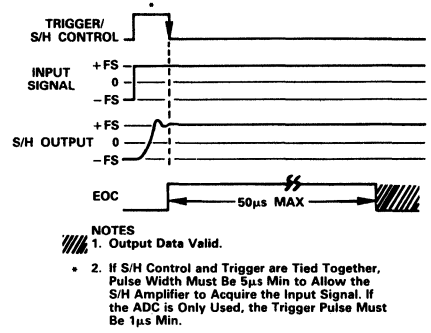


Figure 3. DAS1157/DAS1158/DAS1159 Timing Diagram

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GAIN AND OFFSET ADJUSTMENT

The DAS1157/DAS1158/DAS1159 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Offset calibration is not affected by changes in gain calibration, and should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range, set the input voltage precisely to +305μV for the DAS1157, +153μV for the DAS1158 and +76μV for the DAS1159. For a 0 to +5V unipolar range, set the input to +153μV for the DAS1157, +76μV for the DAS1158 and +38μV for the DAS1159. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001 (DAS1157/DAS1158) or from 100.....000 to 100.....001 (DAS1159).

For the ±5V bipolar range, set the input voltage precisely to +305μV for the DAS1157, +153μV for the DAS1158 and +76μV for the DAS1159. For a ±10V bipolar range, set the input voltage precisely to +610μV for the DAS1157, +305μV for the DAS1158 and +153μV for the DAS1159. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1157)/ +9.99954V (DAS1158)/+9.99977V (DAS1159) for the 0 to +10V units, +4.99954V (DAS1157)/+4.99977V (DAS1158)/ +4.99989V (DAS1159) for 0 to +5V units, +9.99817V (DAS1157)/+9.99909V (DAS1158)/+9.99954V (DAS1159) for ±10V units, or +4.99909V (DAS1157)/+4.99954V (DAS1158)/ +4.99977V (DAS1159) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 or modified binary and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1157/DAS1158/DAS1159 INPUT/OUTPUT RELATIONSHIPS

The DAS1157/DAS1158 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ($\overline{\text{MSB}}$) is used to obtain two's complement coding. The DAS1159 produces a modified binary coded output when configured as a unipolar device. Configured as a bipolar device it can only produce two's complement output codes. The DAS1159 uses $\overline{\text{MSB}}$ to obtain the modified binary and two's complement output codes; the DAS1159 does not have an MSB output. Table II shows the DAS1157/ DAS1158/DAS1159 unipolar analog input/digital output relationships. Table III shows the DAS1157/DAS1158/DAS1159 bipolar analog input/digital output relationships.

Input Voltage–Output Code Relationships

Unipolar Input Voltages

Analog Input		Digital Output
0 to +5V Range	**0 to +10V Range**	
DAS1157		Binary Code
+4.99969V	+9.99939V	11 1111 1111 1111
+0.00000V	+0.00000V	00 0000 0000 0000
DAS1158		Binary Code
+4.99985V	+9.99969V	111 1111 1111 1111
+0.00000V	+0.00000V	000 0000 0000 0000
DAS1159		Modified Binary Code
+4.99992V	+9.99985V	0111 1111 1111 1111
+0.00000V	+0.00000V	1000 0000 0000 0000

Table II. Unipolar Input-Output Relationships

Bipolar Input Voltages

Analog Input		Digital Output	
±5V Range	**±10V Range**	**Offset Binary Code**	**Two's Complement Code**
DAS1157			
+4.99939V	+9.99878V	11 1111 1111 1111	01 1111 1111 1111
+0.00000V	+0.00000V	10 0000 0000 0000	00 0000 0000 0000
−5.00000V	−10.00000V	00 0000 0000 0000	10 0000 0000 0000
DAS1158			
+4.99969V	+9.99939V	111 1111 1111 1111	011 1111 1111 1111
+0.00000V	+0.00000V	100 0000 0000 0000	000 0000 0000 0000
−5.00000V	−10.00000V	000 0000 0000 0000	100 0000 0000 0000
DAS1159			
+4.99985V	+9.99969V		0111 1111 1111 1111
+0.00000V	+0.00000V		0000 0000 0000 0000
−5.00000V	−10.00000V		1000 0000 0000 0000

Table III. Bipolar Input-Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

No power supply decoupling is required since the DAS1157/ DAS1158/DAS1159 contain high quality tantalum capacitors on each of the power supply inputs to ground.

The analog and digital grounds are internally connected in the DAS1157/DAS1158/DAS1159. But in many applications, an external connection between the digital ground pin and analog ground pin is advisable for optimum performance.

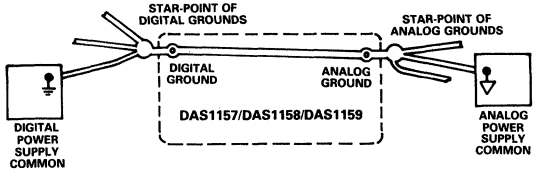


Figure 4. Typical Ground Layout for DAS1157/DAS1158/ DAS1159

Microcomputer I/O Boards

The RTI® Series consists of analog and digital input/output boards that are compatible with all of the popular microcomputer bus standards including:

- IBM PC/XT/AT*
- IBM PS/2*, Micro Channel* Architecture
- STD Bus
- VMEbus
- MULTIBUS*

All boards are 100% bus compatible and are optimized for peak performance on each bus. Different analog/digital conversion speeds, resolution and choice of analog output and channel expansion capability are available allowing customization of the bus based solutions. They are cost effective and provide a convenient means to interface a computer to the real world.

SIGNAL CONDITIONERS

For data acquisition applications requiring signal conditioning and transducer interface with high-voltage isolation, the 3B and 5B Series of signal conditioners or one of the analog signal conditioning panels can be connected directly to the RTI Series boards.

Both the 3B and 5B Series are unmatched in terms of isolation, reliability and ease of use. The 3B Series interfaces to the widest range of signals and is user configurable. The 5B Series consists of functionally complete, high performance, low cost signal conditioners. A family of multiplexed analog signal conditioning panels offers an alternative for systems with high point counts where single channel modularity is not required.

Via a variety of optional backplanes and convenient ribbon cabling to the RTI Series I/O Boards, signal conditioners bring real-world signals into the computer, including millivoltage, voltage, current, thermocouple, RTD, strain gage, LVDT and frequency. For further information on signal conditioners, see Linear Products Databook.

SOFTWARE

Many RTI Series boards are supported by MS-DOS* I/O driver software that provides easy to use, high level calls and commands for user written software programs for languages like Microsoft* BASIC (Interpreted and Compiled), QuickBASIC, C, Pascal, TURBO Pascal*, FORTRAN and MACRO Assembler.

Popular menu-driven data acquisition application software supports many of the RTI Series boards, including ASYST*, LABTECH* NOTEBOOK, LABTECH CONTROL, UnkelScope*, SNAPSHOT STORAGE SCOPE*, Control EG* and THE FIX*. These software packages make it easy to configure a complete solution using Analog Devices I/O and your choice of computer.

Selection Guide
Microcomputer I/O Boards

IBM PC/XT/AT COMPATIBLE BOARDS

Model	Function	Analog Input Channels	Resolution	Throughput XT	Throughput AT	Other Analog Input Features	Analog Output Channels	Resolution	Digital I/O	Other Features	Compatible
RTI-800	Analog Input and Digital I/O	32SE/16D1	12 Bits	31kHz 58kHz 91kHz	27kHz 58kHz 58kHz	Direct Connection to 3B/5B Signal Conditioning	N/A	—	8 Digital Inputs 8 Digital Outputs	3 Counter/Timers	PC/XT/AT
RTI-802	Analog Output	N/A	–	–	–	–	4 (-4 Version) 8 (-8 Version)	12 Bits	N/A	Remote Sensing	PC/XT/AT
RTI-815	Multifunction Analog and Digital I/O	32SE/16D1	12 Bits	31kHz 58kHz 91kHz	27kHz 58kHz 58kHz	Direct Connection to 3B/5B Signal Conditioning	2	12 Bits	8 Digital Inputs 8 Digital Outputs	3 Counter/Timers	PC/XT/AT
RTI-817	Digital I/O	N/A	–	—	—	N/A	N/A	—	Three 8-Bit Ports Each Port Configurable as Input or Output	Interrupt on Change of State. Compatible to Solid-State Relay Modules	PC/XT/AT
RTI-820	Modular Analog and Digital I/O	Up to 64 Inputs	12 Bits	19kHz	19kHz	Supports Direct Connection Up to 4 Signal Conditioning Panels STB-HL02, STB-TC, STB-HLI, STB-TCI, 5B02	Up to 16 Outputs	12 Bits	Three 8-Bit Ports Each Port Configurable as Input or Output		PC/XT/AT
RTI-850	High-Resolution Analog Input	8D	16 Bits 15 Bits 14 Bits	N/A	50kHz 52kHz 55kHz	Extensive Triggering	N/A	—	N/A	256K On-Board Sample Memory	AT
RTI-860	High Speed Simultaneous Analog Input	16SE	12 Bits 8 Bits	N/A	250kHz 330kHz	Extensive Triggering Simultaneous S/H	N/A	—	N/A	256K On-Board Sample Memory	AT

STD BUS COMPATIBLE I/O BOARDS

		STD BUS (NMOS)								STD BUS (CMOS)			
	Analog Devices Part Number	**RTI-1226**	**RTI-1225**	**RTI-1260**	**RTI-1262**	**RTI-1265**	**RTI-1266**	**RTI-1267**	**RTI-1270**	**RTI-1280**	**RTI-1281**	**RTI-1282**	**RTI-1287**
Board Type	Input	●		●		●			●	●			
	Input/Output		●				●	●			●		●
	Output				●							●	
Channel Capacity	Input (Single Ended/ Differential)	16/8	16/8	32/16		64	64	24 Digital I/O	16/16	16/8	16/8		24 Digital I/O
	Output		2		4		16				2	4 or 8	
Input Resolution	10 Bits	●	●										
	12 Bits			●		●	●		●	●	●		
Output Resolution	8 Bits		●										
	12 Bits				●		●				●	●	
Additional Features													
Programmable Gain Amplification				●						●	●		
Single +5V Operation		●	●	●	●	●	●	●	●	●	●	●	●
4–20mA Output					●							●	
Direct Sensor Interface Thermocouples, RTDs						●	●		●				
IBM PC Software Compatible						●	●	●					

IBM PS/2 MICROCHANNEL COMPATIBLE HARDWARE

	RTI-204	**RTI-205**	**RTI-217**
Channel Capacity			
Analog Input	8SE	8SE	
Analog Output		2	
Digital I/O	8	8	32
A/D Resolution (Bits)	12	12	
D/A Resolution (Bits)		12	
Acquisition Thruput	19kHz	19kHz	

Selection Guide
Microcomputer I/O Boards

VMEbus COMPATIBLE I/O BOARDS

	Analog Devices Part Number	VMEbus RTI-600	VMEbus RTI-602
Board Type	Input	•	
	Input/Output		
	Output		•
Channel Capacity	Input (Single Ended/ Differential)	32/16	
	Output		4
Input Resolution	10 Bits		
	12 Bits	•	
Output Resolution	8 Bits		
	12 Bits		•
Additional Features			
Programmable Gain Amplification		•	
Single +5V Operation		•	•
4–20mA Output			•
Direct Sensor Interface Thermocouples, RTDs			

MULTIBUS COMPATIBLE I/O BOARDS

	Analog Devices Part Number	MULTIBUS RTI-711	MULTIBUS RTI-724	MULTIBUS RTI-732
Board Type	Input	•		
	Input/Output			•
	Output		•	
Channel Capacity	Input (Single Ended/ Differential)	32/16		32/16
	Output		4	2
Input Resolution	10 Bits			
	12 Bits	•		•
Output Resolution	8 Bits			
	12 Bits		•	•
Additional Features				
Programmable Gain Amplification		•		•
Single +5V Operation		•	•	•
4–20mA Output				•
Direct Sensor Interface Thermocouples, RTDs				

Application Specific Integrated Circuits

Analog Devices offers a full spectrum of capabilities in application specific integrated circuits (ASICs). These chip-level systems can implement designs with 12-bit accuracy and 16-bit resolution that formerly required board-level solutions.

Analog Devices can incorporate most of the functions of its standard monolithic parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a predefined system-on-a-chip known as a Linear System Macro to your application.

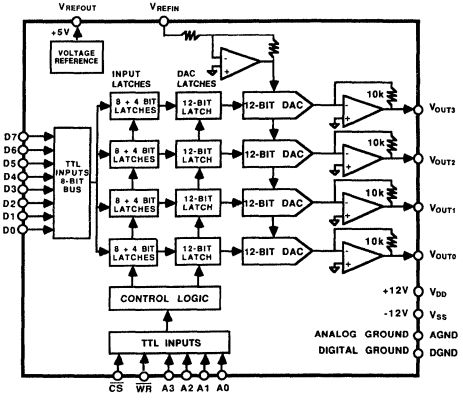
Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, California and England.

Multiple locations for fabrication, assembly and testing ensure a ready supply of production parts. Products can be processed in full MIL-38510 certified facilities.

DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASIC parts. Described here are two Linear System Macros, a custom chipset and a semicustom chip.

AD75004 QUAD DAC



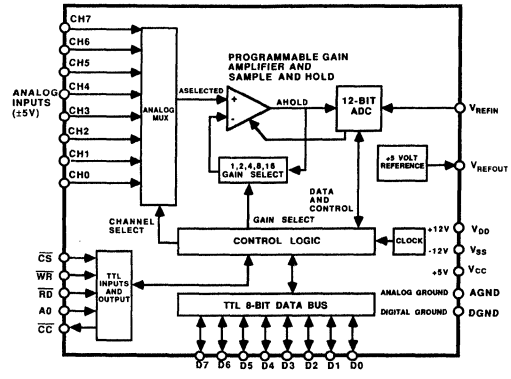
AD75004 Quad DAC

This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously.

AD75003 Data Acquisition System

This DAS converts analog signals on 8 input channels to 12-bit values and interfaces via an 8-bit parallel bus. The chip integrates an 8-channel multiplexer, programmable-gain amplifier, sample-and-hold and 12-bit A/D converter with internal voltage reference.

AD75003 DATA ACQUISITION SYSTEM



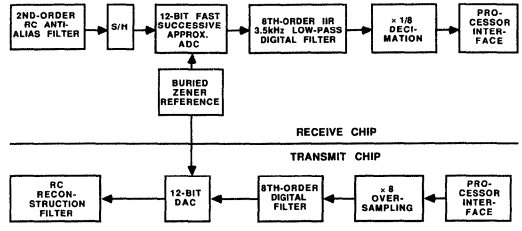
Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. One such device is a semicustom, serial-interface DAS. The AD75003 design was altered to have programmable gains of 1 to 20 instead of 1 to 16, and a serial UART instead of an 8-bit parallel interface. In addition to the AD75003 functions, this part contains a precision instrumentation amplifier, a programmable line-frequency notch filter, a 7-bit trim DAC and a temperature sensor.

Modem Chipset

Library cells can be combined to form macro building blocks for high speed modems. This two-chip design concept filters and converts data to interface a digital signal processor with the analog circuitry of a 9600-baud modem. On one chip, the received signal passes through an antialiasing filter, sample-and-hold, 12-bit A/D converter, 8th-order digital filter and decimation. On the other chip, transmit data is 8× oversampled, then goes to an 8th-order filter, a 12-bit DAC and an active reconstruction filter.

HIGH SPEED MODEM CHIPSET



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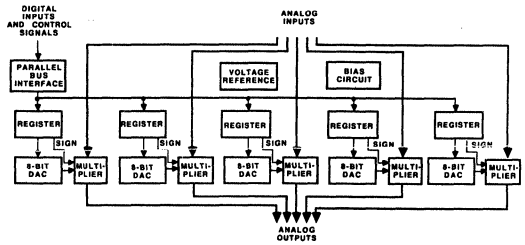
Transversal Filter Element
This circuit implements five taps of a finite-impulse response filter. Each tap comprises an 8-bit DAC and a multiplier, which handle signals up to 40 MHz. A parallel interface sets the tap weights.

TRANSVERSAL FILTER ELEMENT



HIGH PERFORMANCE PROCESSES

Analog Devices' semicustom and custom circuits are fabricated using the same high performance processes as our standard ICs. These technologies include two mixed bipolar-CMOS processes, a high voltage CMOS process and high speed and low power bipolar processes. These processes can include thin-film resistors which may be laser trimmed for precise matching and stable performance over a wide temperature range.

The BiMOS II and Linear Compatible CMOS (LC^2MOS) processes combine bipolar and CMOS devices on one chip. Functional density is an order of magnitude greater than previous mixed-signal processes; over 20,000 devices can be placed on a single chip. Bipolar transistors provide low noise, low offset input stages and high power output stages. The CMOS devices offer high input impedance, and make dense logic and good switches for data converters, multiplexers and switched-capacitor filters. LC^2MOS also provides a JFET for very low input noise.

The bipolar-CMOS processes operate on supply voltages ranging from single +5 volts to split ±15 V, with signal levels ranging from single-ended +3 V to ±10 V. These processes are ideally suited for applications in data acquisition, instrumentation, industrial automation and telecommunications.

The High Voltage Switch (HVS) process provides quality analog switches that can operate with supply voltages up to ±22 volts. It can combine switches and multiplexers with CMOS logic.

The Flash bipolar process makes high speed linear signal processing, data conversion and ECL logic functions on one chip. Signal levels are ±4 volts with ±5 V supplies or up to +10 V with a +12 V supply. Applications include disk-drive read/write circuitry and high speed telecommunications equipment.

The Complementary Bipolar (CB) process features high speed PNP and NPN devices for precision, low power linear applications. It also offers low noise buried Zener references and dual-gate JFETs. CB runs on +5 V to ±15 V supplies.

The table below summarizes the processes available for designing ASICs. Other processes in development will offer even higher speed, denser logic and higher integration of analog and digital functions.

ANALOG DEVICES HIGH-PERFORMANCE PROCESSES FOR ASICs

Process	Power	Signal	Features
BiMOS II	±12 V	±8 V	Wide Variety of Precision Linear and Digital Functions
LC^2MOS	+5 V to ±15 V	+3 V to ±10 V	Wide Variety of Precision Linear and Digital Functions
HVS	+5 V to ±22 V	+2 V to ±18 V	High Voltage Switches, Muxes and Logic Functions
Flash	±5 V or +12 V	±4 V or +10 V	High Speed Linear and Digital Functions
CB	+5 V to ±15 V	+2 V to ±10 V	High Speed, Low Power Linear Functions

CELL LIBRARIES

Cell libraries for the bipolar CMOS processes are described below. These libraries are growing with the development of new processes, macrocells and cells. Many new catalog parts will also be available as cells. Your local sales office can give you current information on the cell libraries and available Linear System Macros.

Operational amplifiers are available in bipolar, JFET and CMOS configurations. Representative bipolar op amp cells have performance characteristics similar to an AD OP-27 and a slew-enhanced AD741. The LC^{2}MOS process offers JFET op amps, including an AD544 equivalent.

Instrumentation amplifiers with performance comparable to the AD521 and AD524 are available. Comparators suitable for 12-bit-accurate applications are available. Linear comparators have response times down to 100 nanoseconds and strobed comparators have setup/access times down to 50 nanoseconds.

Digital-to-analog converters range in resolution from 8 to 14 bits, and include cells similar to the AD667 and AD1856. Analog-to-digital converters vary from 8 to 12 bits in resolution, and include cells equivalent to the AD7572 and AD674. One half-flash ADC cell converts to 8-bit accuracy in 500 nanoseconds, and one successive approximation cell converts to 12 bits in 5 microseconds.

Support cells include sample-and-hold amplifiers with performance comparable to the AD585, low-voltage bandgap references comparable to the AD584 and low noise buried Zener references.

RC active filters and programmable switched-capacitor filters are available with specifications in these ranges:

Topology: all classical filter types
Frequency Range: 200Hz to 20kHz (switched-cap) or 100Hz to1MHz (RC)
Number of Sections: up to 10th-order (switched-cap) or 4th-order (RC)
Signal/Noise and THD: >72dB, compatible with 12-bit data acquisition.

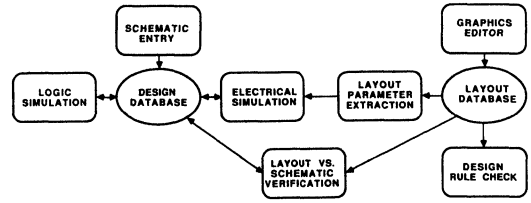
Logic cells include gates, counters, registers, PLA, RAM and ROM. Interface cells include 8-bit and 16-bit parallel I/O ports and UARTs.

DESIGN AND LAYOUT

Analog Devices engineers will design your integrated circuit, drawing on their years of experience and using powerful computer-aided design (CAD) tools. These comprehensive CAD tools help design, simulate and lay out the circuit and aid in generating test programs.

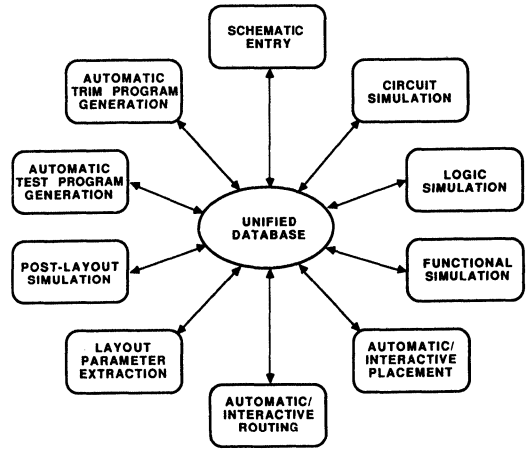
The following figure shows the standard design cycle which begins with schematic entry. After logic and initial electrical simulation, the designer uses the graphics editor to lay out the circuit. Parasitics and other data are extracted from the layout and circuit operation is simulated again. Finally, the system checks that the layout follows process design rules and matches the schematic.

IC DESIGN WITH
COMMERCIAL CAD SYSTEM



In addition to using these commercial CAD tools, Analog Devices has developed a proprietary compiler for mixed-signal IC design, called JANUS. By integrating all design functions into one environment with a common database, JANUS reduces design time by an order of magnitude.

IC DESIGN WITH JANUS
PROPRIETARY CAD SYSTEM



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To speed schematic entry, the designer selects devices, cells and macrocells from comprehensive menus. Device generators allow the designer to specify devices for maximum performance and minimum size. Analog, logic and functional simulators verify the performance of individual cells and the overall chip design. Placement and routing algorithms complete circuit layouts automatically, yet allow interaction with the designer to handle special cases. When placing devices and cells, JANUS considers thermal and electrical matching as well as die area. An expert system optimizes routing to minimize interconnect length and number of vias. Post-layout simulation comprehends the parasitics of the final routing and is more accurate than the initial simulation.

Future goals for JANUS include automatically generating programs for production trim and test of analog/digital ICs.

TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, Teradyne and LTX test equipment. The design, wafer probe and test areas share data on the network for statistical analysis and device modelling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

PACKAGING

Analog Devices ICs are available in most modern package types, including high pin-count and surface mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below. This list is constantly expanded and other packages may be used if they are suitable for high performance applications.

Available Packages

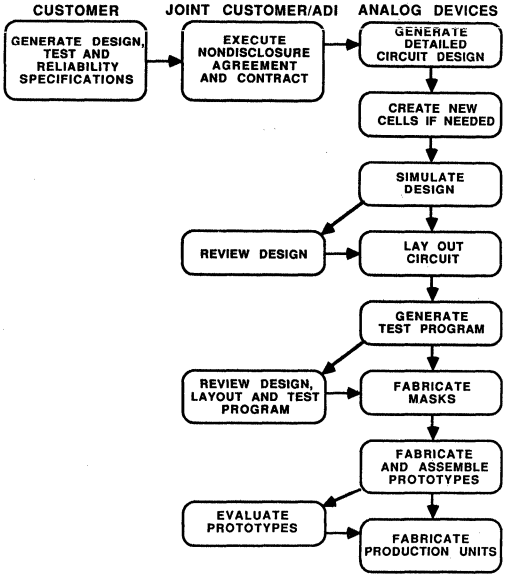
Pin-grid array (PGA): 68 to 144 pins
Leaded ceramic chip carrier (LDCC): 44 pins
Leadless ceramic chip carrier (LCC): 20 to 68 I/Os
Plastic quad flat pack (PQFP): 100 pins
Plastic leaded chip carrier (PLCC): 20 to 52 pins
Plastic dual in-line package (DIP): 14 to 64 pins
Side-brazed DIP: 14 to 64 pins
Frit-seal DIP (Cerdip): 14 to 28 pins
Small outline (SO): 14 and 16 pins

PROGRAM RESPONSIBILITIES AND INTERFACES

The following chart shows the major phases in developing an ASIC and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices Sales Engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.

PROGRAM RESPONSIBILITIES AND INTERFACES



Power Supplies
Modular AC/DC Power Supplies

GENERAL DESCRIPTION
Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low-cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 25 mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES
- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5 V), Dual (±12 V, ±15 V), and Triple (±15 V/+5 V, ±15 V/+1 V to +15 V) Output Supplies
- Current Outputs:
  25 mA to 1000 mA for Dual and Triple Output Supplies
  250 mA to 5000 mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

GENERAL SPECIFICATIONS

Power Requirements	
Input Voltage Range:	105 V ac to 125 V ac
Frequency:	50 Hz to 250 Hz
Electrical Specifications	
Temperature Coefficient:	0.02%/°C
Output Voltage Accuracy:	±2%, max See Specifications Table
Breakdown Voltage:	500 V rms, min
Isolation Resistance:	50 MΩ
Short Circuit Protection:	All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.
Environmental Requirements	
Operating Temperature Range:	−25°C to +71°C
Storage Temperature Range:	−25°C to +85°C

SPECIFICATIONS – Typical @ +25°C and 115 V ac 60 Hz unless otherwise noted*

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. max %	Load Reg. max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	904	±15	±50	0.02	0.02	±200 mV −0 mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
	Single Output	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
		928	5	3000	0.05	0.10	±2%	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	−1%	0.5	
		927	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2%	1.0 (typ)	
		2B35J	±15	±65	0.08	0.1	(−0, +300 mV)	0.5	3.5×2.5×1.25
			+1 to +15**	125	0.08	0.1		0.25	
		2B35K	±15	±65	0.01	0.02	(−0, +300 mV)	0.5	3.5×2.5×1.25
			+1 to +15**	125	0.01	0.02		0.25	
Chassis Mounted	Dual Output	952	±15	±100	0.05	0.05	±2%	1	4.4×2.7×1.45
		970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.45
		973	±15	±350	0.05	0.05	±2%	1	4.4×2.7×2.00
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.45
		976	5	3000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
		977	5	5000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
	Triple Output	972	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	300	0.02	0.10	±2%	1.0 (typ)	
		974	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2%	1.0 (typ)	

*Consult Analog Devices Power Supplies Catalog for additional information.
**Resistor programmable.
Specifications subject to change without notice.

Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offers system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Fourteen models are offered in five power levels of 1 watt, 1.8 watts, 4.5 watts, 6 watts and 12 watts. Input voltage versions include 5 volt, 12 volt, 24 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±60 mA to 1000 mA output current capability.

Most models are high efficiency (typicaly over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20 kHz) Converter Switching Frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (Either Output to Common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free Air Convection Cooling
  No external heat sink or specification derating is required over the operating temperature range.

GENERAL SPECIFICATIONS FOR 1 W AND 1.8 W MODELS

Line Regulation – Full Range: ±0.3% (±1% max, 949)
Load Regulation – No Load to Full Load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20 mV p-p (with 15 μF tantalum capacitor across each output) 2 mV rms max, 949)
Breakdown Voltage: 300 V dc min (500 V dc min, 949)
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5 W, 6 W AND 12 W MODELS

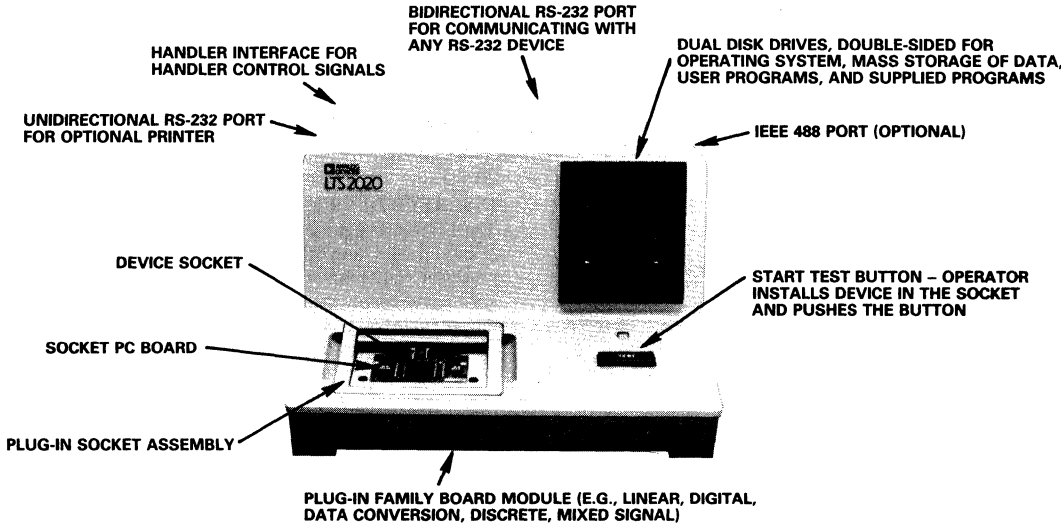
Line Regulation – Full Range: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Load Regulation – No Load to Full Load: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Output Noise and Ripple: 1 mV rms max
Breakdown Voltage: 500 V dc min
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

SPECIFICATIONS – Typical @ +25°C at nominal input voltage unless otherwise noted*

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	2.0×2.0×0.38
958	5	100	5	4.5/5.5	200 mA	±5%	−0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17A	±1%	±0.01%	58%	2.0×2.0×0.38
960	±12	±40	5	4.5/5.5	384 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
964	±15	±33	12	10.8/13.2	165 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
965	±15	±190	5	4.65/5.5	1.7 A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
966	±15	±190	12	11.2/13.2	710 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
967	±15	±190	24	22.3/26.4	350 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6 A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35 A	±1%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6 A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250 mA	±0.5%	±0.01%	61%	2.0×2.0×0.38
951	±15	±410	5	4.65/5.5	3.7 A	±0.5%	±0.01%	62%	3.5×2.5×0.88

NOTES
[1]Models 940 and 941 will deliver up to 120 mA output current (and Model 943 will deliver up to 600 mA) over an input voltage range of 4.65 V dc and 5.5 V dc.
*Consult Analog Devices Power Suppies Catalog for additional information.
**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120 mA.
Specifications subject to change without notice.

LTS-2020 Component Test Systems



THE LTS CONCEPT

The LTS-2020 is a versatile component test system which tests a multitude of components to the manufacturer's specifications (linear, digital, data conversion, and discrete devices). The system offers such features as RS-232 ports for networking, IEEE for compatibility with handlers and probers, dual disk drives for mass storage of data, automatic self-calibration, and a full statistical analysis software package.

The LTS-2020 provides several data output formats – datalog, yield analysis, and statistical analysis. The console provides the primary measurement and control functions to test a specific class of devices. The socket assembly is the mechanical and electronic interface for the family board and the DUT board. The DUT board plugs directly into the socket assembly and contains the circuitry and socket, specific to the actual device under test.

Analog Devices' component test systems are the first benchtop testers that are programmable in BASIC and fill-in-the-blanks CREATE. CREATE is menu-driven software which prompts the user for data sheet limits and conditions, then builds a completed test program for the specified device. Turnkey program libraries are available for each of the device families.

Far more than just comprehensive production testers, these test systems can handle complex engineering analysis and incoming inspection. They are the first systems that can provide all the capabilities of today's large centralized test systems at a price that is approximately one-third the cost. The LTS-2020 not only provides the flexibility of distributed or decentralized testing, it allows for cost effective multiple system purchases. They increase overall test reliability since the threat of a single big failure is eliminated in a distributed testing environment.

LTS-2020 Test Capabilities

MIXED SIGNAL TEST CAPABILITY

The LTS-2800 Mixed Signal Family Board and LTS-0680 Test Head perform a wide variety of ac and dc parametric tests on devices such as complex hybrids, octal DACs, ASICs, converters, and pulse width modulators. The family board supplies the dc pin drivers, the dc force and measure system, a V_{CC} buffer, an rms-to-dc conversion circuit, voltage and current sources, and a 24 × 5 switching matrix. With its 24 programmable pin drivers, the system can provide high and low digital voltages, a three-state (high impedance) output mode, and accurate voltages and currents (V/I source).

The family board incorporates a series of 12-bit calibrated sources, used for programming V_{IL} and V_{IH} voltage levels at the digital inputs of the device under test. A threshold source for programming voltage levels on a comparator is used to detect digital output voltage levels accurately. For forcing and measuring currents, a V/I source provides and measures 10 μA to 400 mA and voltages to ±20 V.

A switching matrix provides system flexibility by allowing any one of several capabilities to be switched to any of the pin drivers. These include the measure system, V/I source, V_{IH} and V_{IL} sources, the rms-to-dc circuit, and BNC input and output connectors for interconnection with external instruments using the IEEE-488 bus.

The LTS-0680 Mixed Signal Test Head contains a precise and versatile time measure unit which provides accurate ac measurement of propagation delays, slew rates, pulse widths, and rise and fall times. It also incorporates a 16-bit user data bus, 16-bit relay driver bus, four 12-bit programmable sources, and a user's expansion board. A square wave source to the DUT provides up to ±10 volt signals, from 1.22 kHz to 2.5 MHz.

LTS-2020 Test Capabilities (Continued)

LINEAR DEVICE TEST CAPABILITY

The LTS-2101 Operational Amplifier Family Board tests today's very demanding high precision op amps, comparators, and regulators. This board houses the test loop used in testing op amps and comparators and the pulse load circuitry used in developing the high currents needed for voltage regulator testing.

For testing devices under 100 μV, the LTS-2101 offers a tight offset spec of ±(0.25% + 5 μV). Use of low thermal Emf relays and a test loop gain of 10,045 ensures superior low level V_{OS} measurement performance for optimum repeatability of low level signals.

Testing of low current devices is achieved with the LTS-0614 Socket Assembly which is designed to test bias and offset currents with an accuracy of ±(5% + 25 fA) for any FET amplifier, including quad devices. Program libraries containing prewritten test programs for many standard op amps, comparators and regulators are available on disk.

ANALOG-TO-DIGITAL TEST CAPABILITY

The LTS-2200 ADC Family Board provides the test circuitry required for testing monolithic, hybrid, or modular ADCs. An on-board 16-bit microprocessor with 8K bytes of memory acts as a slave for the system console and executes preprogrammed test routines such as linearity, all codes existence, transition noise measurements, and conversion time measurements at high speed. Absolute accuracy can be measured within 200 μV. Linearity, differential nonlinearity, offset, gain, and PSSR are tested to ±0.05 DUT LSB +200 μV. Turnkey test packages are available for many of the standard ADCs currently in use.

DIGITAL-TO-ANALOG TEST CAPABILITY

The LTS-2302 DAC Family Board utilizes advanced state-of-the-art test techniques to provide comprehensive test capabilities for a wide variety of D/A converters. It will test both voltage and current output DACs, DACs with and without buffer registers, and serial or parallel input DACs to 16-bit accuracy.

High repeatability on low level signals is achieved because of the grounding scheme on the LTS-2302. The incorporation of high level components in the V/I circuits ensures true accuracy. In addition, the methodology for measuring low bit currents allows appropriate testing of this parameter on CMOS DACs.

Output leakage current on the LTS-2302 is measured with the bit drivers to the DAC set to logic 0. Current is measured using the I to V converter. A 1 MΩ resistor within the I to V circuitry ensures sensitivity, thereby measuring current down to ±1 μA full scale.

DIGITAL DEVICE TEST CAPABILITY

The LTS-2510 Digital Device Family Board provides 24-pin driver/detectors and a precision, four quadrant V/I source for testing SSI/MSI TTL and CMOS digital devices. This board contains four programmable device supplies and switching circuitry necessary for performing accurate parametric measurements on all device pins.

Together with the LTS-0655 remote ac test fixture, dynamic parametric testing of 24-pin SSI/MSI TTL digital devices can be achieved. Accuracies are achieved down to ±4% + 1.5 ns at a resolution of 500 ps. Dynamic parameters tested are propagation delay, setup, and hold times.

DISCRETE DEVICE TEST CAPABILITY

The LTS-2600 Transistor Family Board tests bipolar transistors, JFETs, diodes, and optocouplers. An on-board 16-bit microprocessor with 4K bytes of memory acts as a slave for the LTS system and coordinates the timing and pulse width control of the stimulus and measurement signals. In addition, the microprocessor monitors the interlock circuitry to insure safe handling of high power test signals.

MOSFET software packages support the testing of N and P channel enhancement mode and N channel depletion mode devices. Tests which may be performed on MOSFET devices include Idss, Igss, Igssf, Igssr, Id (off), Id (on), B Vdss, B Vgss, B Vgssf, B Vgssr, Vds (on), Vgs (th), Vgsoff, Vsd, Rds (on), and Gsf.

The Smartpower Test Fixture will support fast, accurate testing of devices such as Darlington Arrays, Differential Line Drivers/Receivers, and Transceivers/Repeaters. It contains a matrix board which facilitates the muxing of High Voltage/High Current V/Is, a nonometer, diffamp, 16-bit measure system, and mecca ground reference to any one of eight matrix points at the DUT site and eight dc pin drivers programmable to any one of four modes – V/I, V_{IH}, V_{IL} or Tristate. This configuration allows true digital dc parametric testing of the front end of smartpower devices while providing the high voltage and high current capability to test the discrete output stage.

ANALOG SWITCH TEST CAPABILITY

The LTS-2700 Analog Switch Family Board adds switch and multiplexer testing capability to the LTS-2020. This test capability, with CREATE software, allows datalogged device testing at the incoming inspection and semiconductor manufacturing levels and includes software power for use in component evaluation applications.

The LTS-2700 tests on and off drain to source leakage currents with an accuracy of 250 pA while forcing differential voltages up to 50 V (± 25 V from GND). Other tests performed are drain to source on resistance, greatest change in drain-source on resistance between channels, digital input current and supply current.

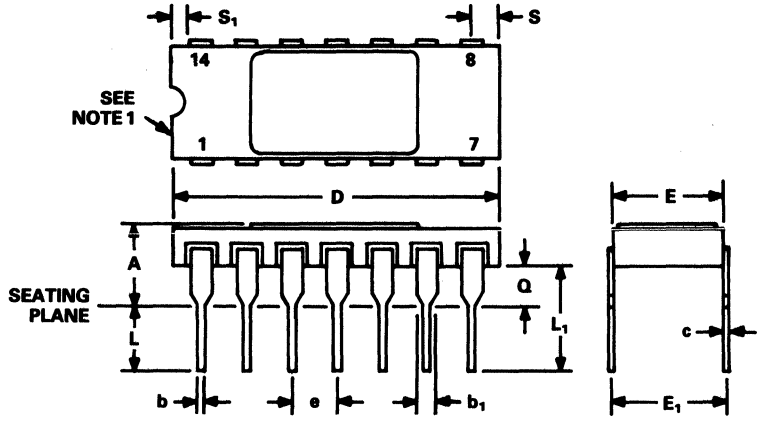
Twenty high integrity analog lines are provided – four to be used as drain connections and sixteen for source connections. Also provided are eight programmable digital drivers, four digital control bits, six variable power supplies, and one fixed +5 V supply. These combinations of sources provide testing of devices such as 4-channel switches, 16 to 1 multiplexers, and other combinations of switches and multiplexers.

Package Information
Contents

Package Outline Dimensions

D-14

14-Lead Side Brazed Ceramic DIP

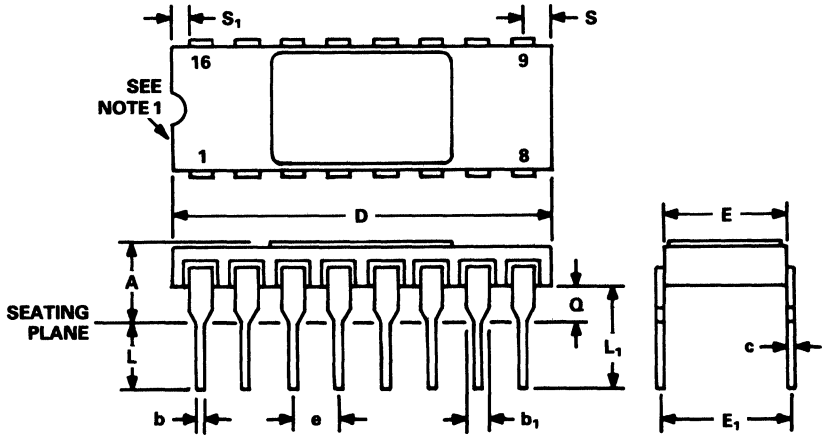


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twelve spaces.

D-16
16-Lead Side Brazed Ceramic DIP

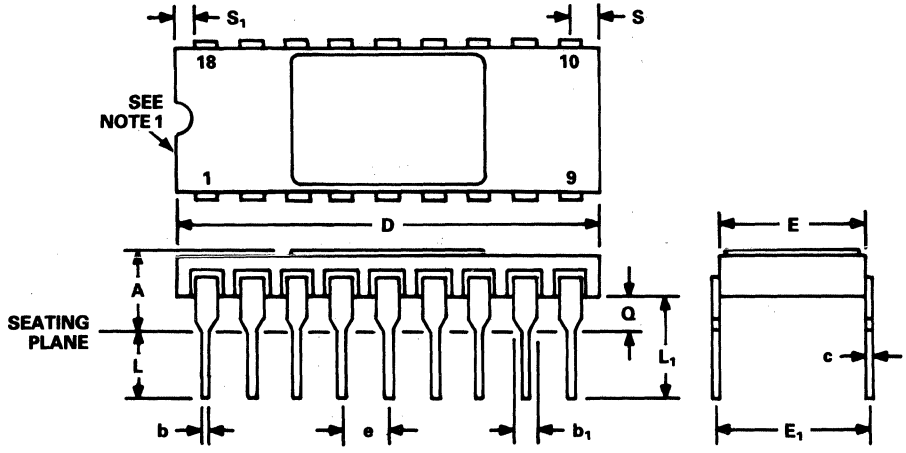


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Fourteen spaces.

D-18

18-Lead Side Brazed Ceramic DIP

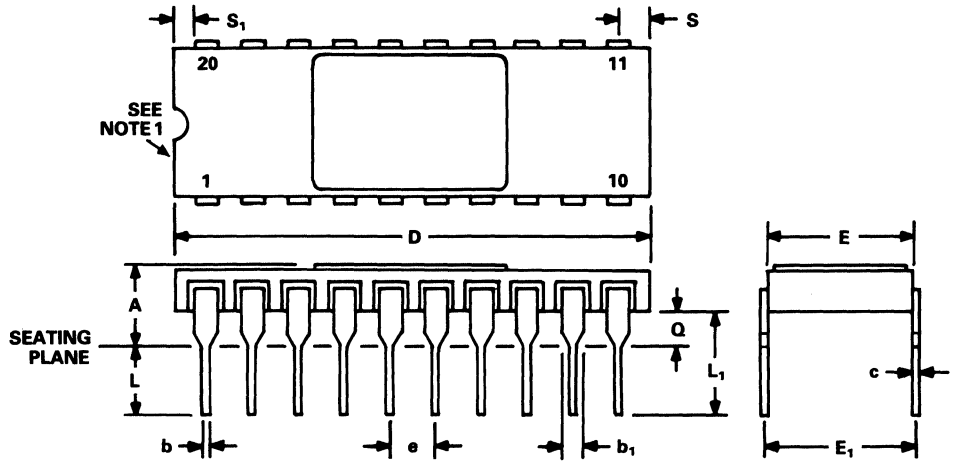


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Sixteen spaces.

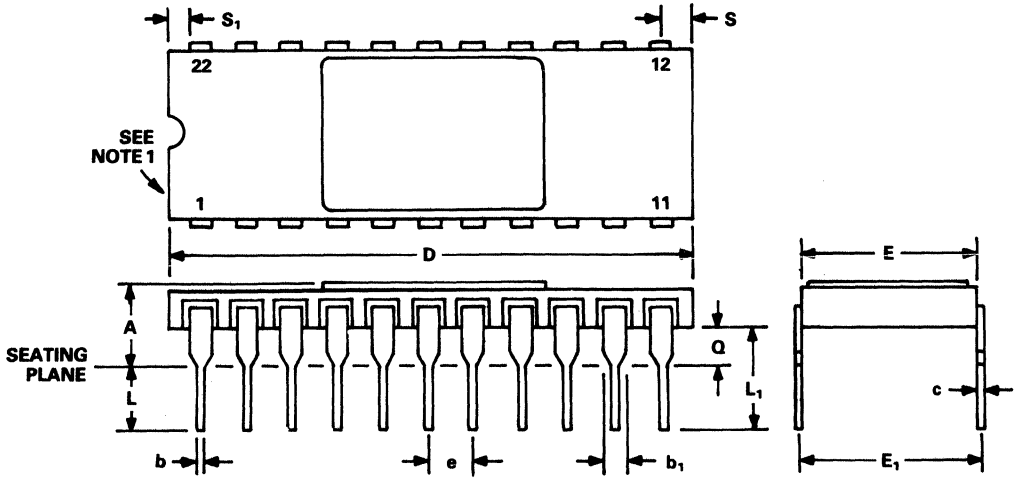
D-20
20-Lead Side Brazed Ceramic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Eighteen spaces.

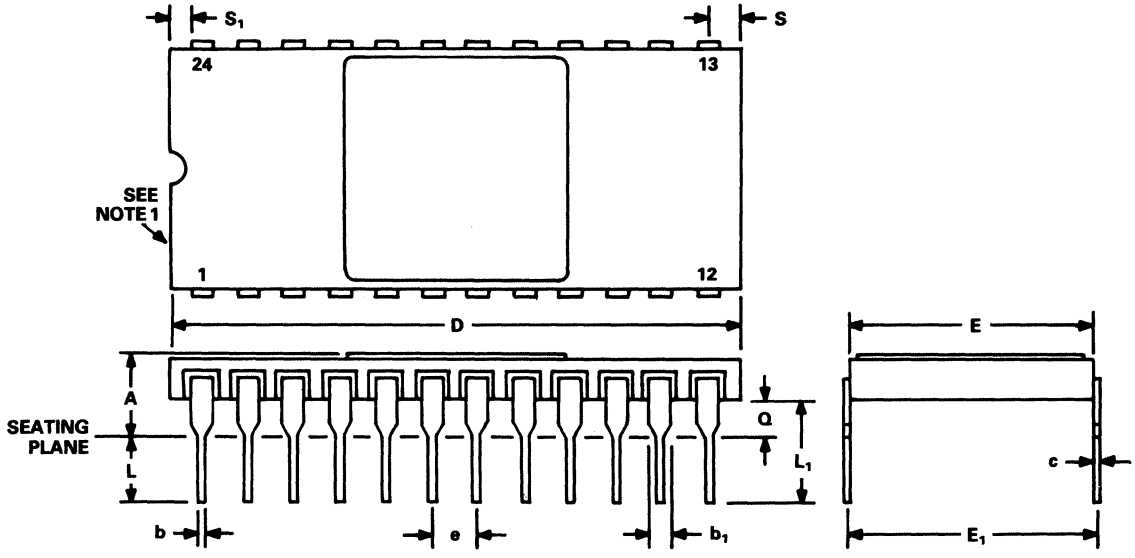
D-22
22-Lead Side Brazed Ceramic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.111		28.22	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty spaces.

D-24
24-Lead Side Brazed Ceramic DIP

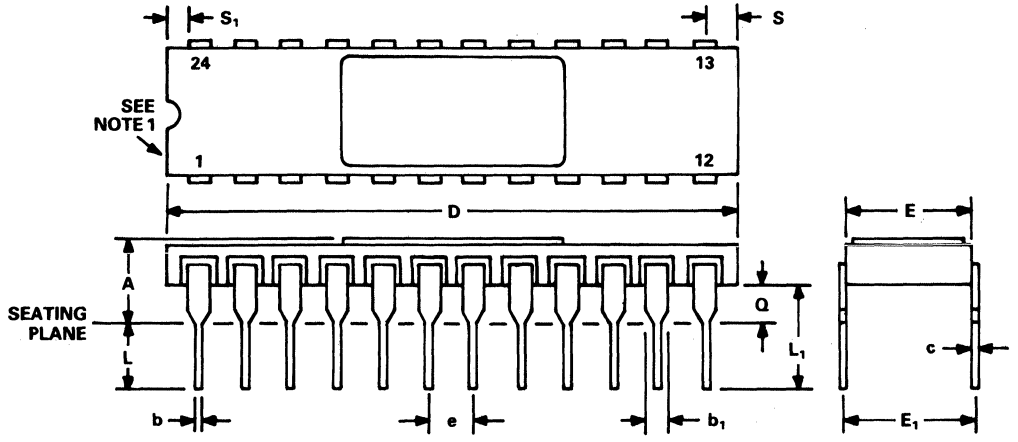


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		1.290		32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.090	0.110	2.29	2.79	7
L	0.120	0.200	3.05	5.08	
L_1	0.150		3.81		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-two spaces.

D-24A

24-Lead Side Brazed Ceramic DIP (Single Width)

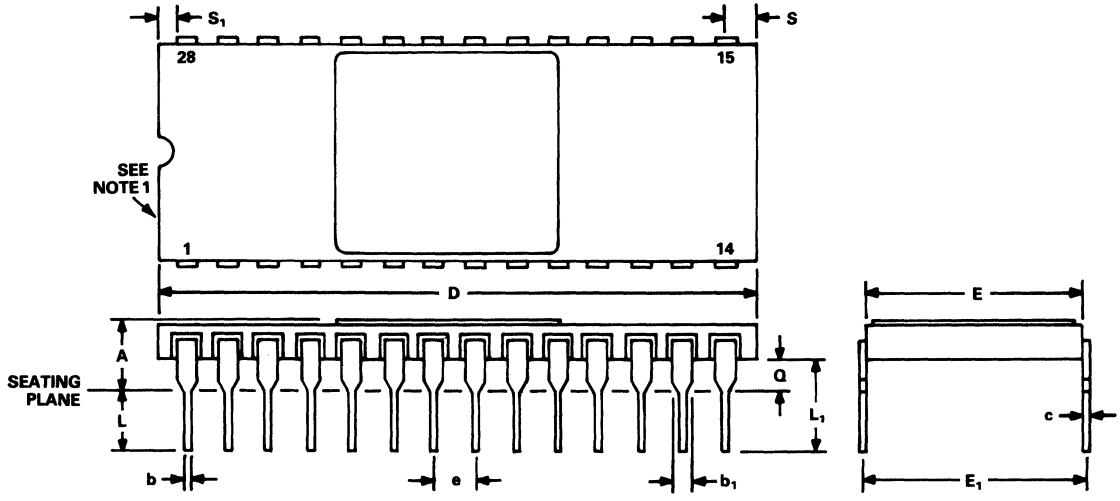


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-two spaces.

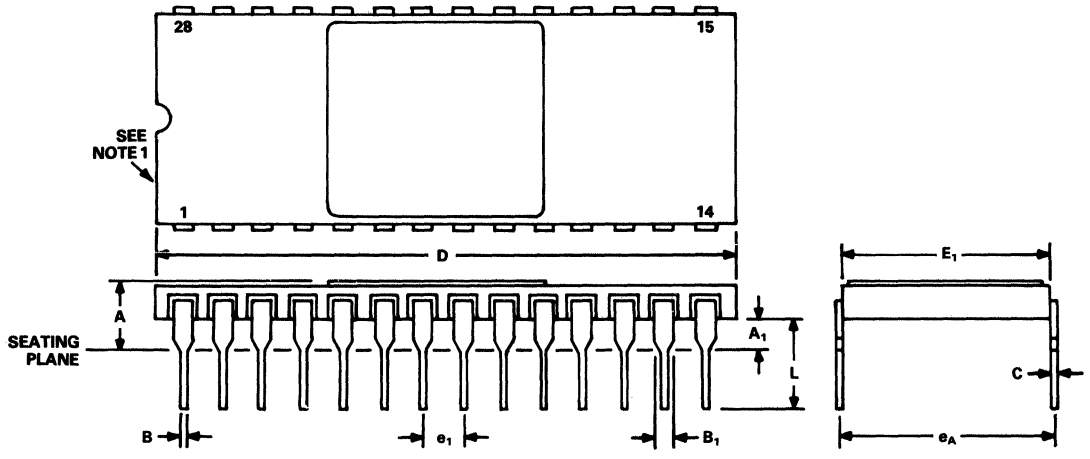
D-28
28-Lead Side Brazed Ceramic DIP



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.018	0.20	0.46	6
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.100		2.54	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-six spaces.

D-28A
28-Pin Side Brazed

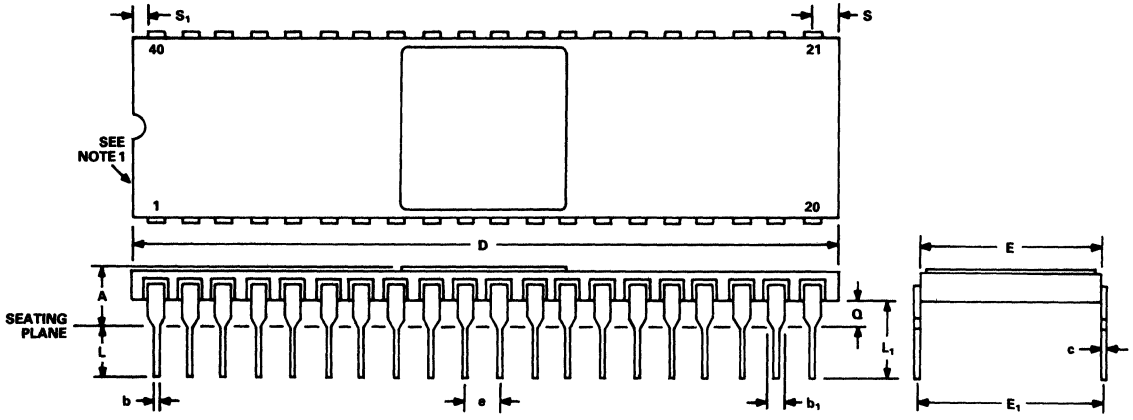


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.175		4.45	
A_1	0.040		1.02		3
B	0.015	0.020	0.38	0.51	5
B_1	0.045	0.055	1.14	1.40	2,5
C	0.008	0.012	0.20	0.30	5
D		1.420		36.07	4
E_1	0.580	0.605	14.73	15.37	4
e_A	0.600 TYP		15.24 TYP		
e_1	0.095	0.105	2.41	2.67	6
L	0.200		5.08		

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension B_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
6. Twenty-six spaces.

D-40
40-Lead Side Brazed Ceramic DIP

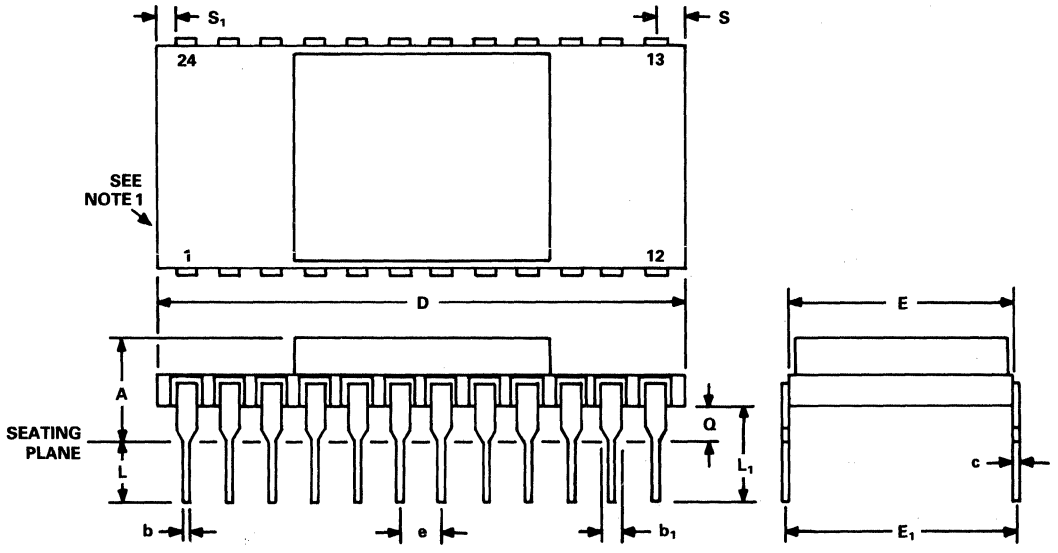


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		2.096		53.24	4
E	0.590	0.620	12.95	15.75	4
E_1	0.520	0.630	13.21	16.00	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Thirty-eight spaces.

DH-24A

24-Lead Size Brazed Ceramic DIP for Hybrid



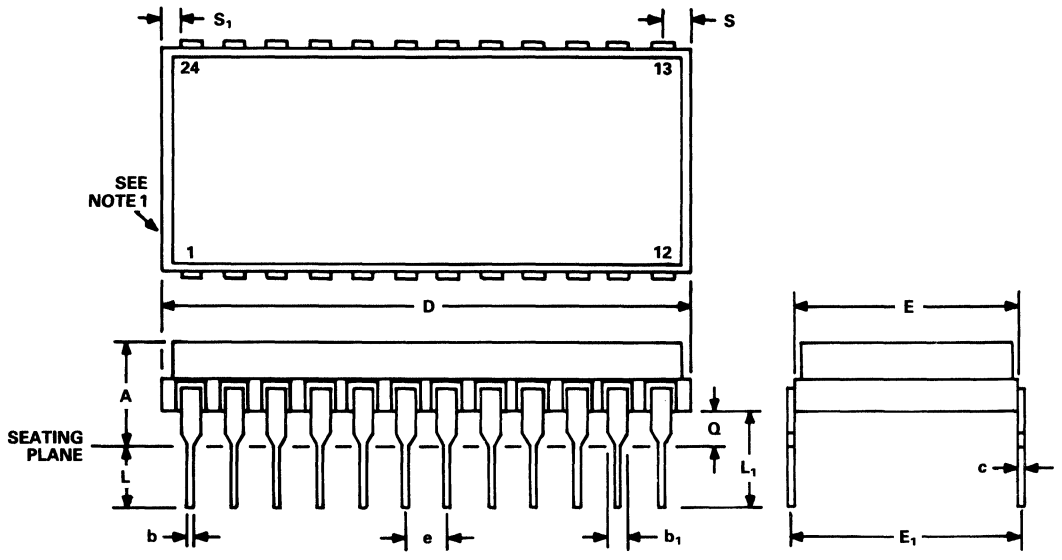
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.212		29.69	
E	0.580	0.600	14.21	14.70	
E_1	0.590	0.620	14.99	15.75	6
e	0.100 BSC		2.54 BSC		4,7
L	0.120	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twenty-two spaces.

DH-24C

24-Lead Side Brazed Ceramic DIP for Hybrid (Large Cavity)



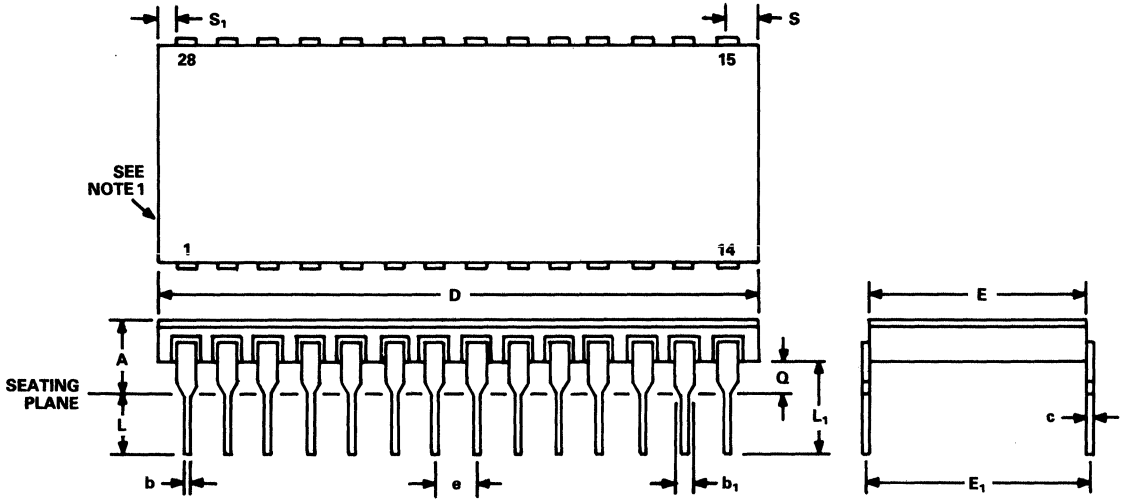
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.245		6.22	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.270		31.11	
E	0.585	0.610	14.33	15.49	
E_1	0.590	0.620	14.99	15.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.120	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twenty-two spaces.

DH-28

28-Lead Side Brazed Ceramic DIP for Hybrid (Large Cavity)



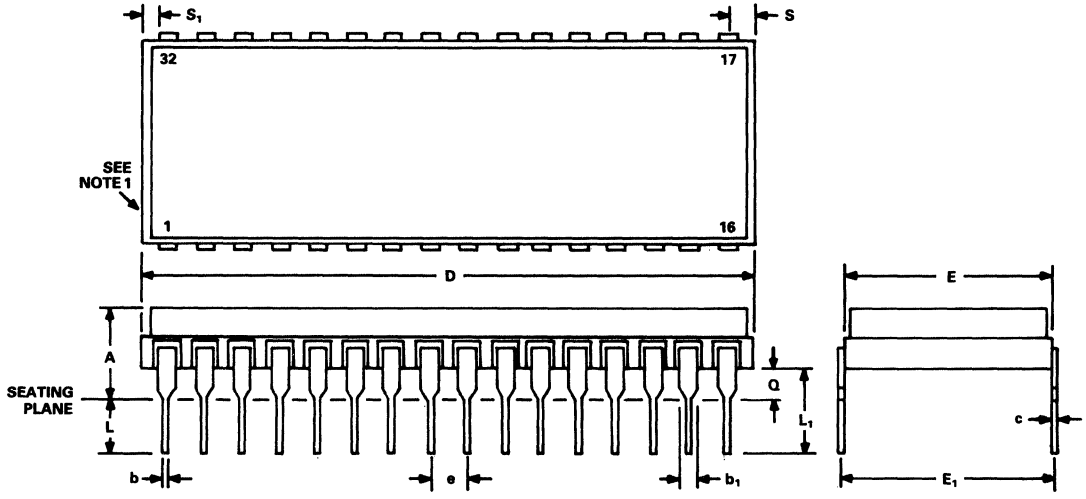
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.414		34.64	
E	0.580	0.610	14.73	15.49	
E_1	0.590	0.620	14.99	15.75	6
e	0.100 BSC		2.54 BSC		4,7
L	0.120	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twenty-six spaces.

DH-32B

32-Lead Side Brazed Ceramic DIP for Hybrid ("Skinny")



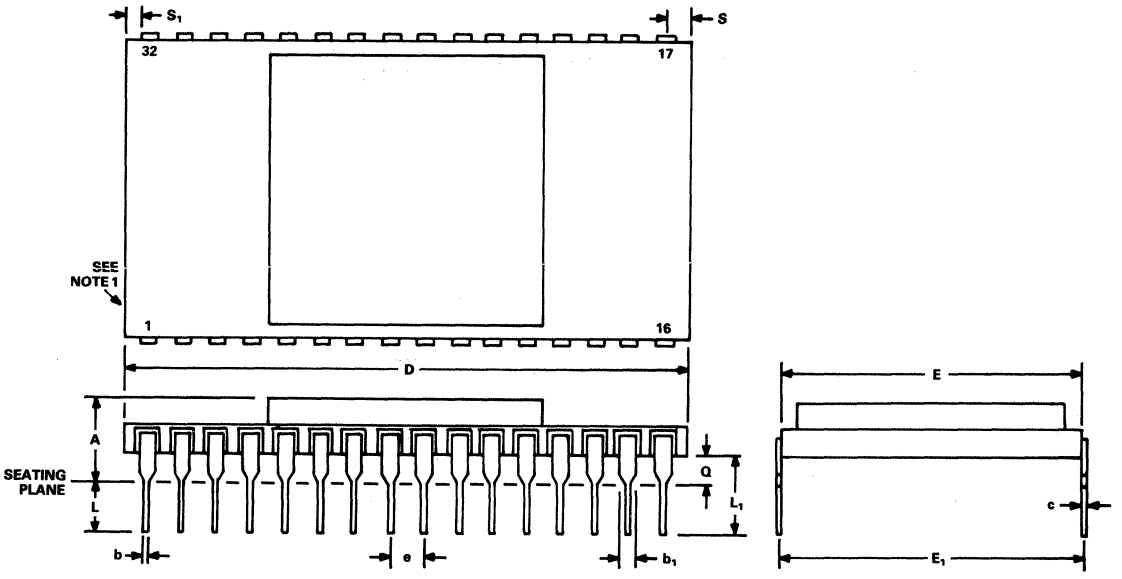
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.280		7.11	
b	0.016	0.020	0.41	0.51	
b_1	0.035	0.045	0.89	1.14	2
c	0.009	0.012	0.23	0.31	
D	1.584	1.640	40.64	41.66	
E	0.580	0.605	14.73	15.24	
E_1	0.590	0.610	14.99	15.49	6
e	0.100 BSC		2.54 BSC		4,7
L	0.125	0.200	3.18	5.08	
L_1	0.180		4.57		
Q	0.015	0.060	1.02	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.**
3. **Dimension Q shall be measured from the seating plane to the base plane.**
4. **The basic pin spacing is 0.100" (2.54mm) between centerlines.**
5. **Applies to all four corners.**
6. **E_1 shall be measured at the centerline of the leads.**
7. **Thirty spaces.**

DH-32C

32-Lead Side Brazed Ceramic DIP for Hybrid (Small Cavity)



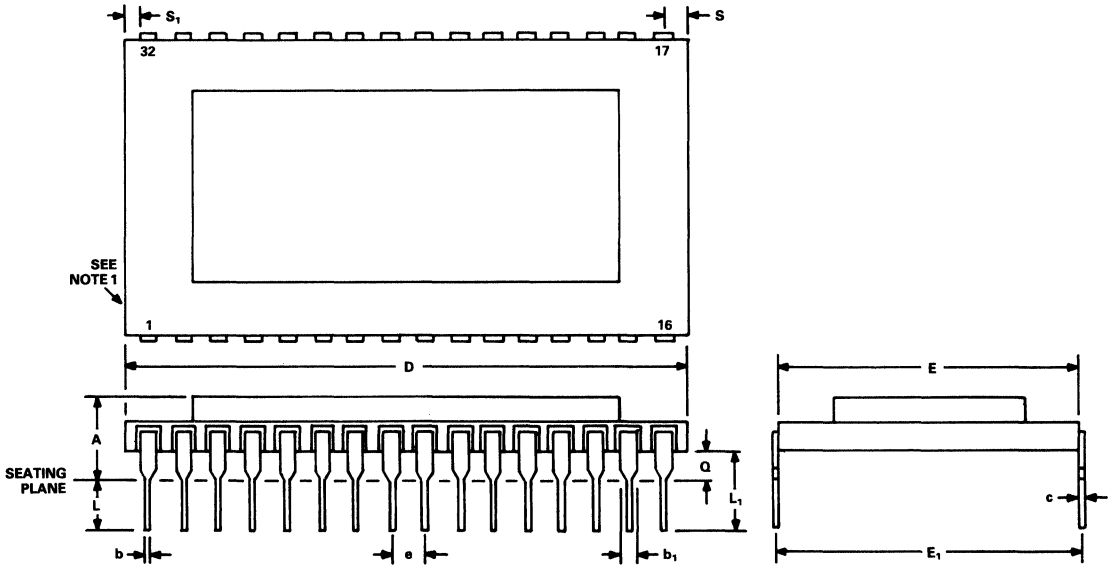
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.280		7.11	
b	0.016	0.020	0.41	0.51	
b_1	0.035	0.055	0.89	1.40	2
c	0.009	0.012	0.23	0.31	
D		1.620		41.14	
E	0.870	0.910	22.10	23.11	
E_1	0.890	0.930	22.61	23.62	6
e	0.100 BSC		2.54 BSC		4,7
L	0.150	0.180	3.81	4.57	
L_1	0.190	0.230	4.83	5.84	
Q	0.015	0.060	1.02	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

DH-32D

32-Lead Side Brazed Ceramic DIP for Hybrid (Medium Cavity)



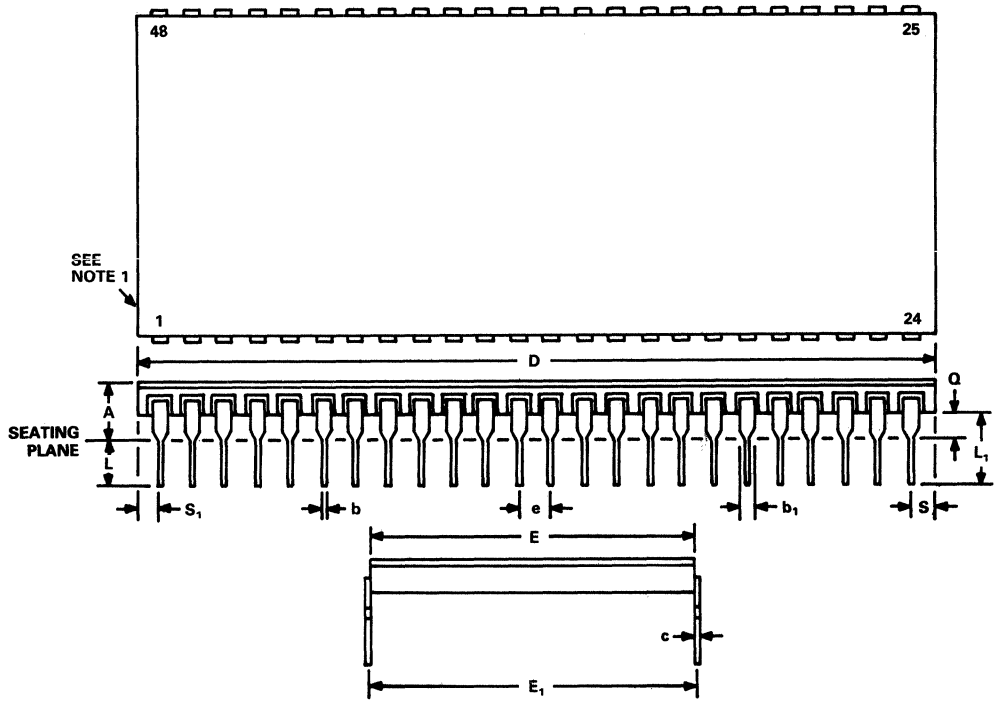
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.280		7.11	
b	0.016	0.020	0.41	0.51	
b_1	0.035	0.055	0.89	1.40	2
c	0.009	0.012	0.23	0.31	
D		1.616		39.59	
E	0.870	0.910	22.10	23.11	
E_1	0.890	0.930	22.61	23.62	6
e	0.100 BSC		2.54 BSC		4,7
L	0.125	0.200	3.18	5.08	
L_1	0.180		4.57		
Q	0.015	0.060	1.02	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

DH-48

48-Lead Side Brazed Ceramic DIP for Hybrid

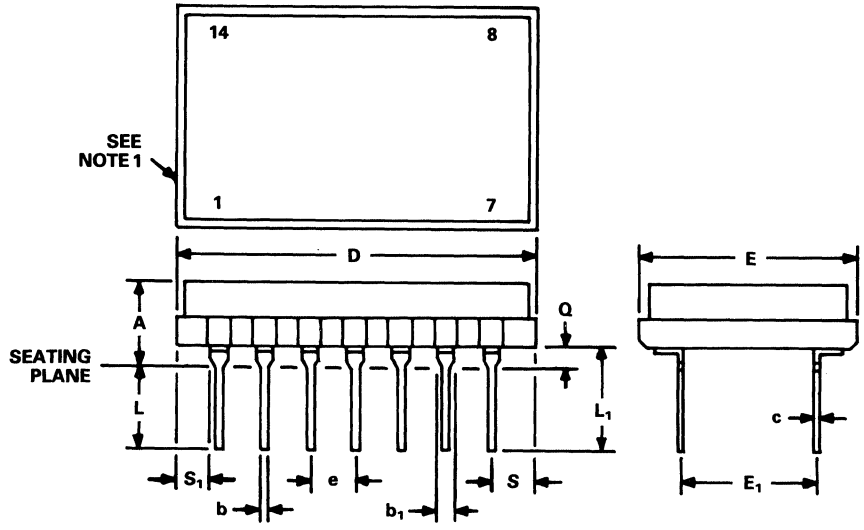


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.240		6.10	
b	0.016	0.020	0.41	0.51	
b_1	0.045	0.055	1.14	1.39	2
c	0.008	0.012	0.20	0.31	
D	2.450	2.500	62.23	63.50	
E	0.985	1.005	25.02	25.53	
E_1	0.990	1.010	25.15	25.65	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.140	0.175	3.56	4.44	
L_1	0.180		4.57		
Q	0.040	0.060	1.02	1.52	3
S		0.104		2.03	5
S_1	0.049		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Forty-six spaces.

DH-14A
14-Lead Bottom Brazed Ceramic DIP

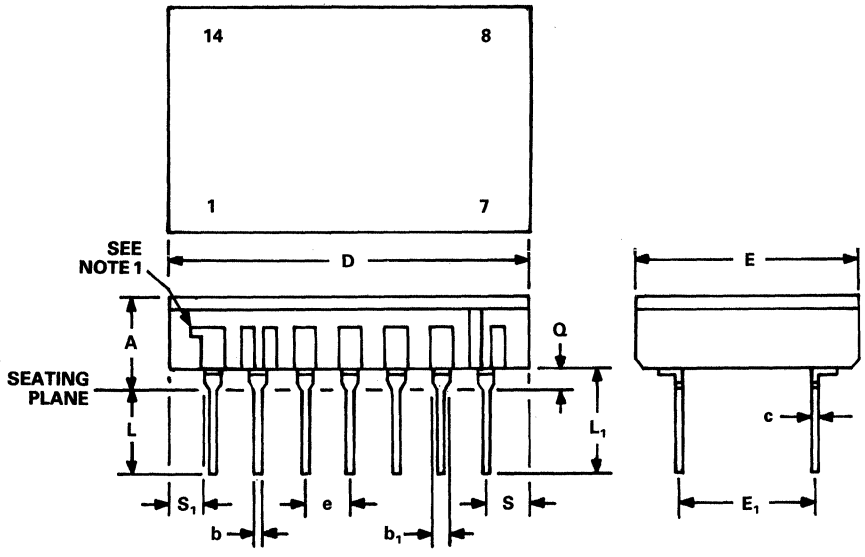


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.220		5.59	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		0.805		20.45	
E	0.480	0.505	12.19	12.83	
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		4,7
L	0.125	0.200	3.18	5.08	
L_1	0.180		4.57		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twelve spaces.

DH-14C

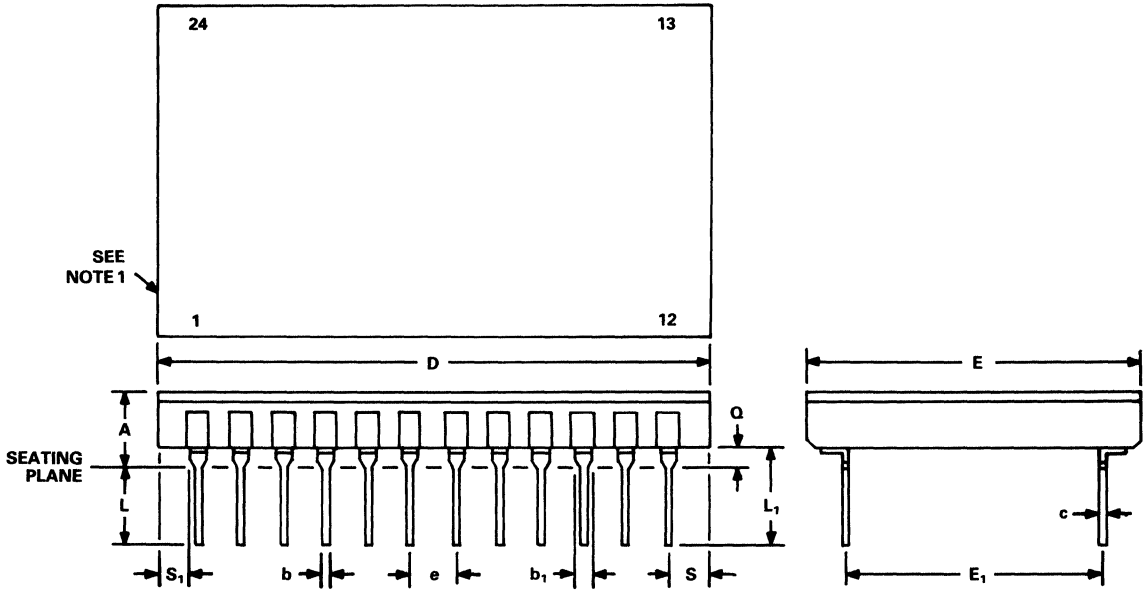
14-Lead Bottom Brazed Ceramic DIP



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.140	0.200	3.56	5.08	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D	0.770	0.810	19.56	20.57	
E	0.480	0.510	12.19	12.95	
E_1	0.295	0.305	7.49	7.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.150	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.035	0.38	1.91	3
S		0.137		3.48	5
S_1	0.060		0.52		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twelve spaces.

DH-24B
24-Lead Bottom Brazed Ceramic DIP

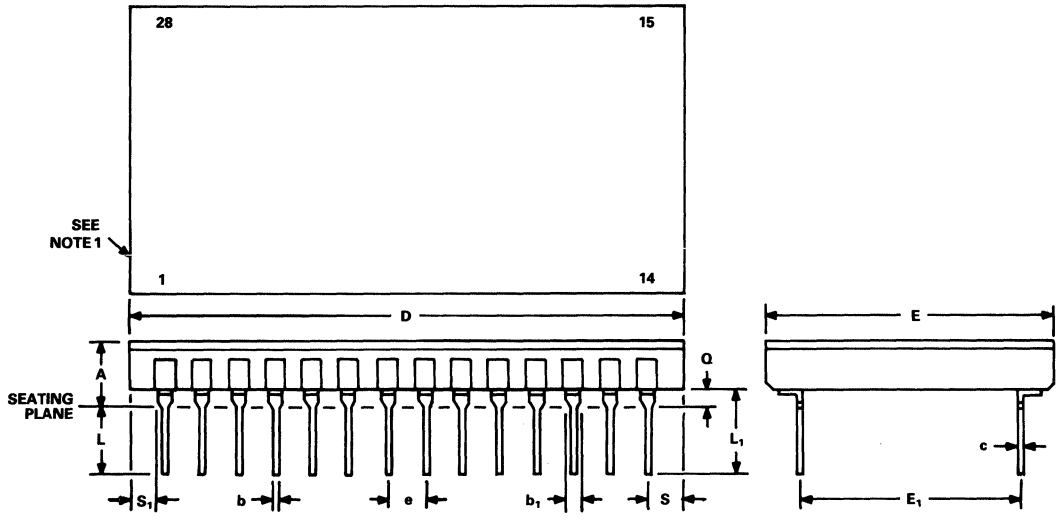


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.320		33.53	
E	0.770	0.810	19.56	20.57	
E_1	0.550	0.620	14.99	15.75	6
e	0.100 BSC		2.54 BSC		4,7
L	0.120	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twenty-two spaces.

14

DH-28A
28-Lead Bottom Brazed Ceramic DIP

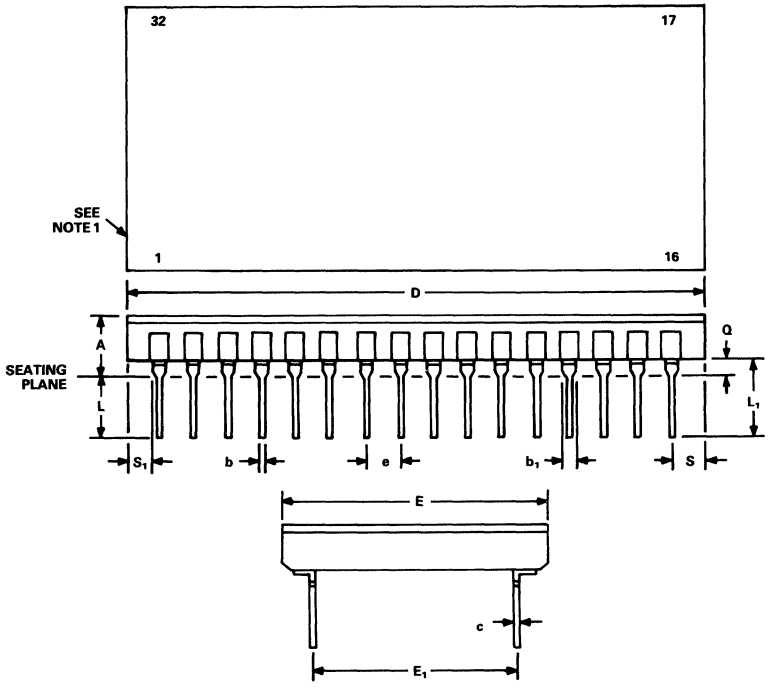


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.575		40.00	
E	0.770	0.810	19.56	20.57	
E_1	0.550	0.620	14.99	15.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.120	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.075	0.38	1.91	3
S		0.137		3.48	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The base pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of all the leads.
7. Twenty-six spaces.

DH-32E

32-Lead Bottom Brazed Ceramic DIP



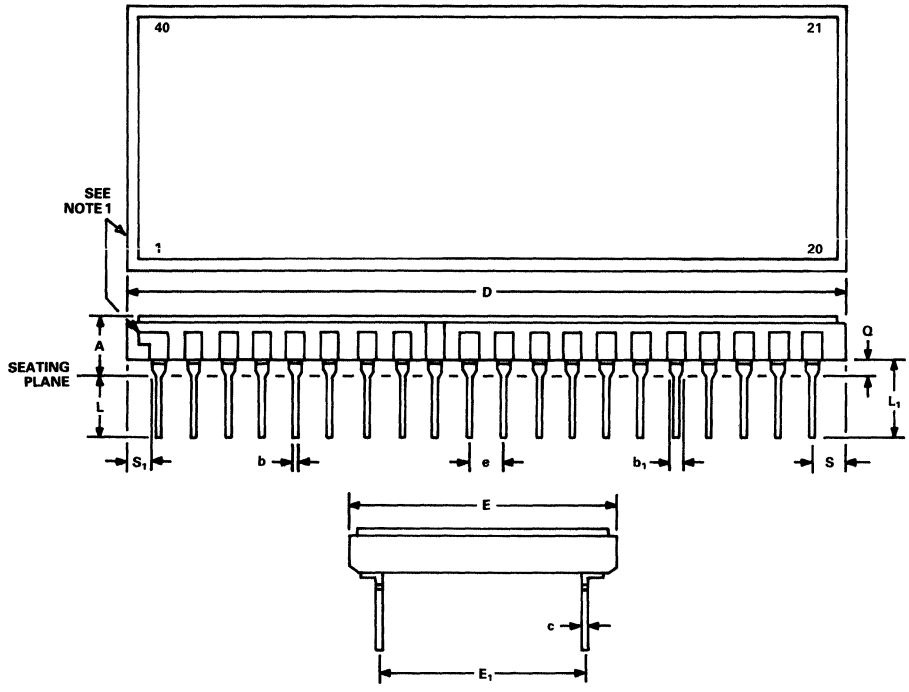
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.750		44.31	
E	1.075	1.105	27.31	28.07	
E_1	0.850	0.920	21.59	23.37	6
e	0.100 BSC		2.54 BSC		4,7
L	0.120	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.075	0.38	1.91	3
S		0.120		3.05	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

DH-40A

40-Lead Bottom Brazed Ceramic DIP

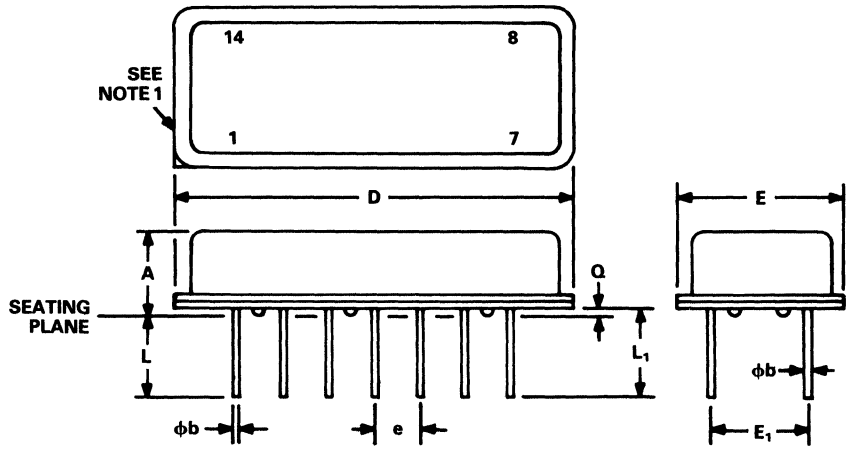


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.060	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		2.120		53.85	
E	0.770	0.810	19.56	20.57	
E_1	0.580	0.620	14.73	15.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.120	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty-eight spaces.

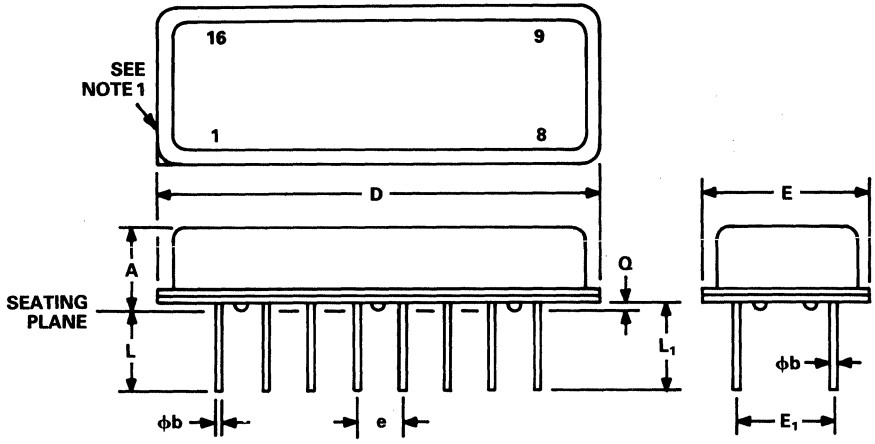
DH-14B
14-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
ϕb	0.014	0.023	0.36	0.58	2
D		0.885		22.48	
E	0.490	0.520	12.45	13.21	
E_1	0.295	0.305	7.49	7.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.140	0.200	3.56	5.08	
L_1	0.160		4.57		
Q	0.015	0.075	0.38	1.91	3

NOTES
1. Index area; a square corner or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twelve spaces.

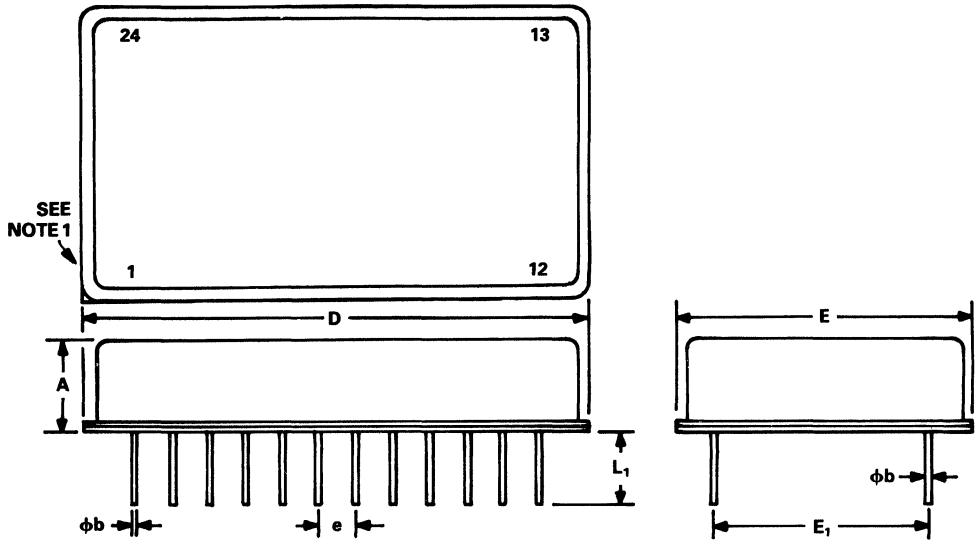
DH-16B
16-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.175	0.215	4.45	5.46	
ϕb	0.016	0.020	0.41	0.51	
D	0.960	0.985	24.40	25.00	
E	0.490	0.520	12.45	13.21	
E_1	0.295	0.305	7.49	7.75	4
e	0.095	0.105	2.41	2.67	5
L_1	0.160	0.255	4.06	6.48	

NOTES
1. Index area; a square corner or a lead one identification mark is located adjacent to lead one.
2. Pin 6 is electrically connected to the case.
3. Case has metal bottom surface.
4. E_1 shall be measured at the centerline of the leads.
5. Fourteen spaces.

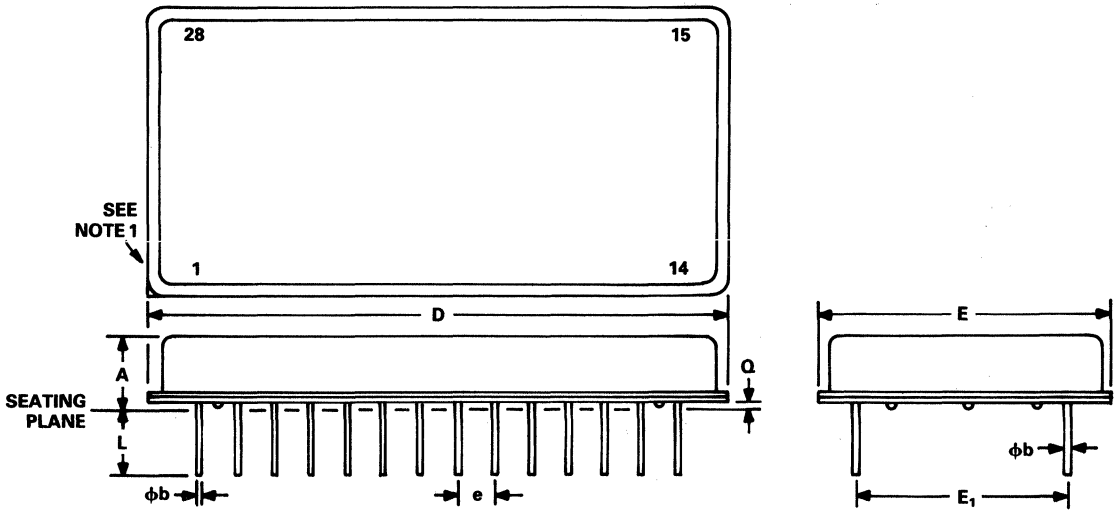
DH-24D
24-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.250		6.35	
ϕb	0.016	0.020	0.41	0.51	
D		1.385		35.18	
E		0.810		20.57	
E_1	0.590	0.610	15.00	15.50	3
e	0.100 BSC		2.54 BSC		2
L_1	0.140	0.210	3.56	5.33	

NOTES
1. Index area; a colored bead or identification mark is located at lead one.
2. The basic pin spacing is 0.100″ (2.54mm) between centerlines.
3. E_1 shall be measured at the centerline of the leads.

DH-28B
28-Lead Metal Platform DIP

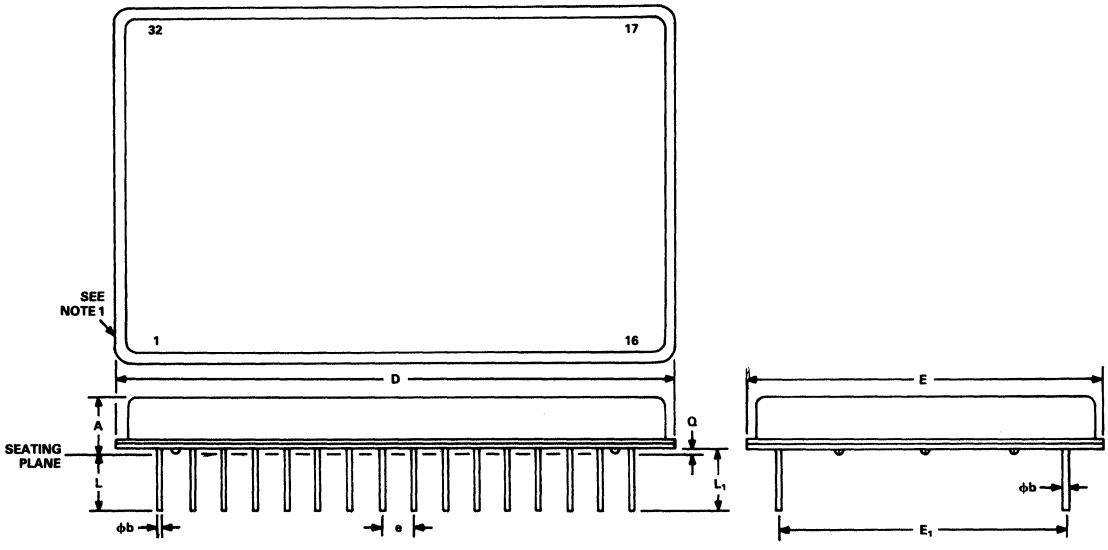


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.205	4.70	5.21	
ϕb	0.016	0.020	0.41	0.51	
D	1.555	1.585	39.50	40.26	
E	0.785	0.805	19.93	20.48	
E_1	0.590	0.610	15.00	15.50	4
e	0.100 BSC		2.54 BSC		3
L	0.140	0.210	3.56	5.33	
Q	0.020	0.030	0.51	0.76	2

NOTES
1. Index area; a colored bead or identification mark is located at lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic spacing is 0.100" (2.54mm) between centerlines.
4. E_1 shall be measured at the centerline of the leads.

DH-32A

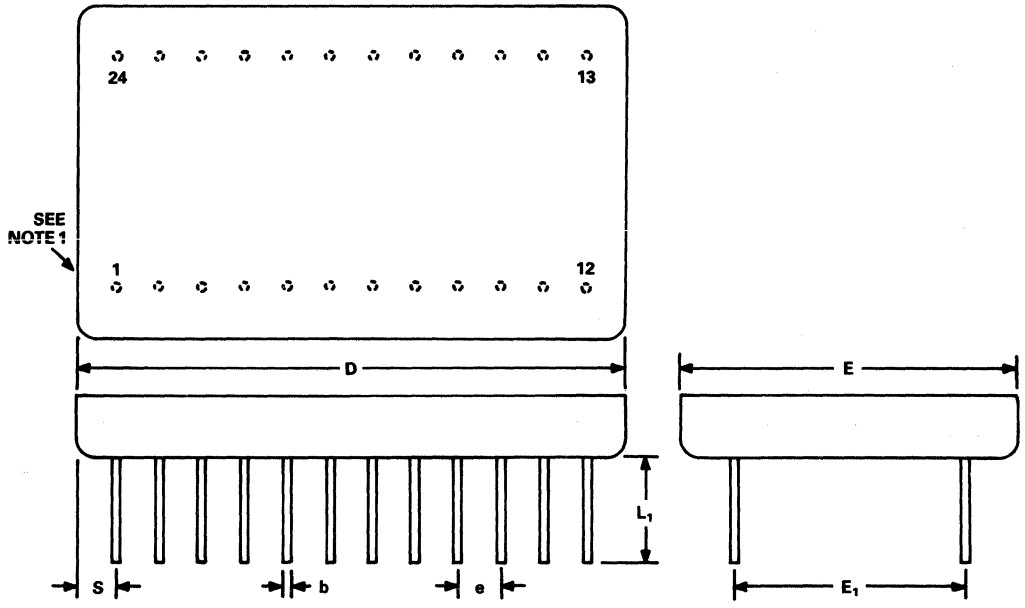
32-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.280		7.11	
ϕb	0.016	0.020	0.41	0.51	2
D		1.755		44.58	
E	1.125	1.155	28.58	29.34	
E_1	0.890	0.910	22.61	23.11	6
e	0.100 BSC		2.54 BSC		4,7
L	0.140	0.210	3.56	5.33	
L_1	0.160		3.81		
Q	0.020	0.030	0.52	0.75	3

NOTES
1. Index area; a colored bead or identification mark is located at lead one.
2. The minimum limit for dimension ϕb may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

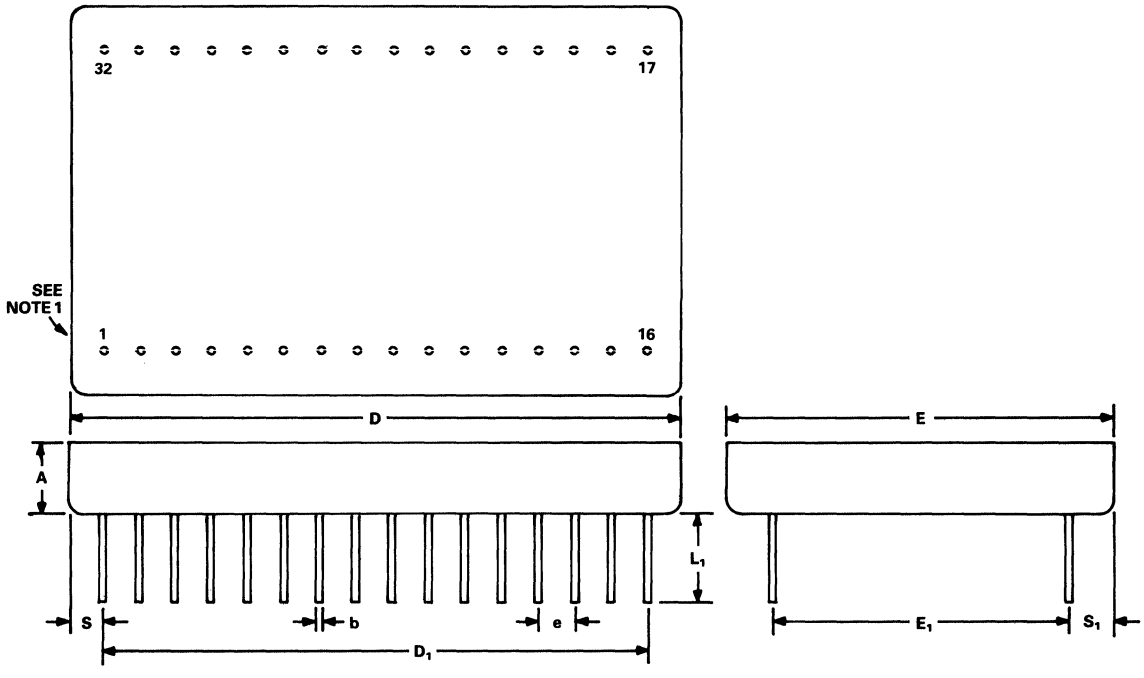
M-24A
24-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
b	0.014	0.023	0.36	0.58	
D	1.265	1.280	32.131	32.51	
E	0.765	0.780	19.431	19.80	
E_1	0.590	0.620	12.95	15.75	3
e	0.090	0.110	2.29	2.79	4
L_1	0.230	0.270	5.84	6.85	
S		0.090		2.29	2

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E_1 shall be measured at the centerline of the leads.
7. Twenty-two spaces.

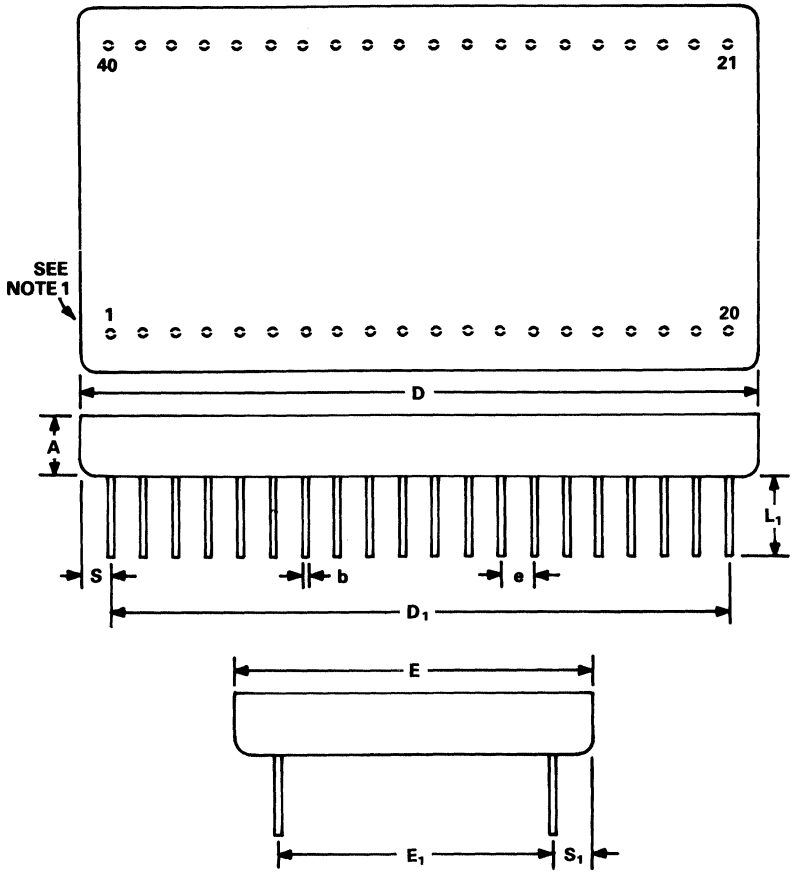
M-32
32-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b		0.020		0.51	
D		1.745		44.323	
D_1	1.494	1.506	37.948	38.252	
E		1.145		29.083	
E_1	0.880	0.920	22.352	23.368	3
e	0.098	0.102	2.49	2.59	4
L_1	0.240		6.09		
S	0.115	0.135	2.92	3.43	2
S_1	0.115	0.135	2.92	3.43	2

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E_1 shall be measured at the centerline of the leads.
4. Thirty spaces.

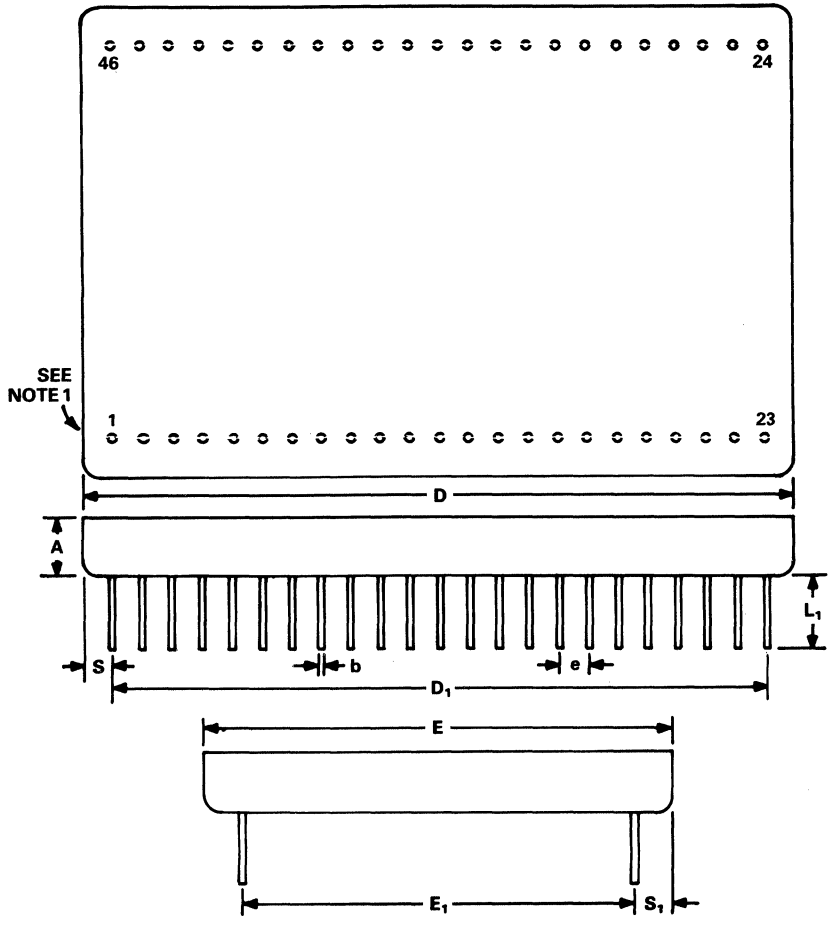
M-40
40-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.19		4.83	
D		2.145		54.483	
D_1	1.894	1.906	48.108	48.412	
E		1.145		29.083	
E_1	0.880	0.920	22.352	23.368	3
e	0.098	0.102	2.49	2.59	4
L_1	0.240		6.09		
S	0.115	0.135	2.92	3.43	2
S_1	0.115	0.135	2.92	3.43	2

NOTES
1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **Applies to all four corners.**
3. **E_1 shall be measured at the centerline of the leads.**
4. **Thirty-Eight spaces.**

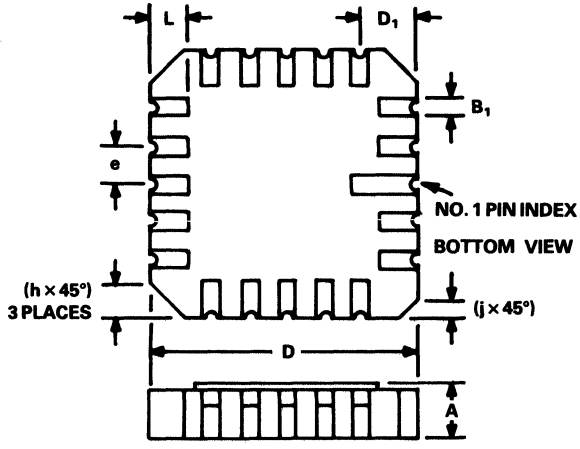
M-46
46-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.231		5.86	
b	0.016	0.020	0.410	0.510	
D		2.380		60.452	
D_1	2.194	2.206	55.728	56.032	
E		1.580		40.132	
E_1	1.280	1.320	32.512	33.528	3
e	0.098	0.102	2.49	2.59	4
L_1		0.210		5.334	
S	0.080	0.100	2.032	2.54	2
S_1	0.130	0.150	3.302	3.81	2

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E_1 shall be measured at the centerline of the leads.
4. Forty-four spaces.

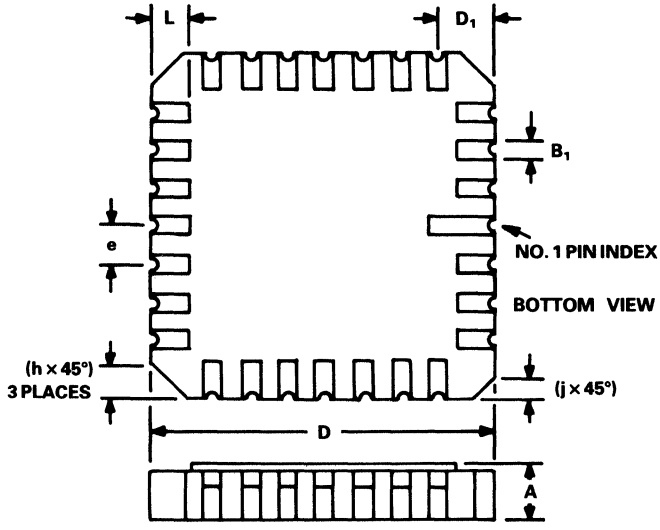
E-20A
20-Terminal Leadless Ceramic Chip Carrier



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.342	0.358	8.69	9.09	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. **Dimension A controls the overall package thickness.**
2. **Applies to all 4 sides.**
3. **All terminals are gold plated.**

E-28A
28-Terminal Leadless Ceramic Chip Carrier



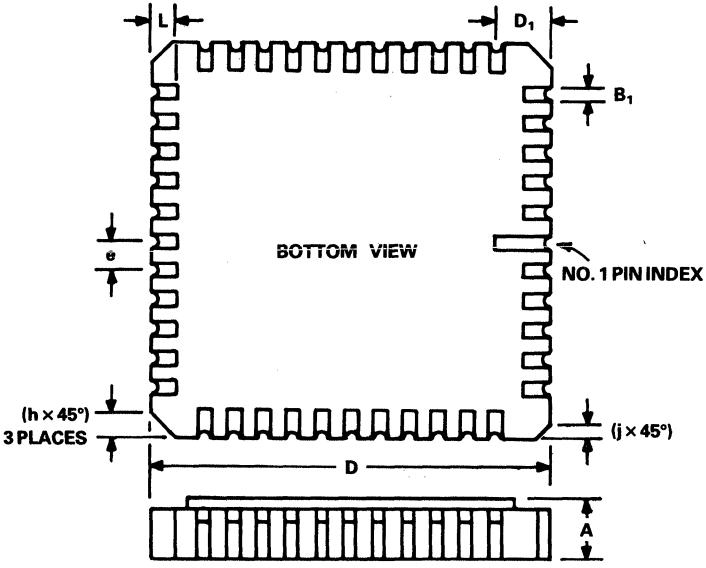
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.442	0.458	11.23	11.63	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. **Dimension A controls the overall package thickness.**
2. **Applies to all 4 sides.**
3. **All terminals are gold plated.**

14

E-44A

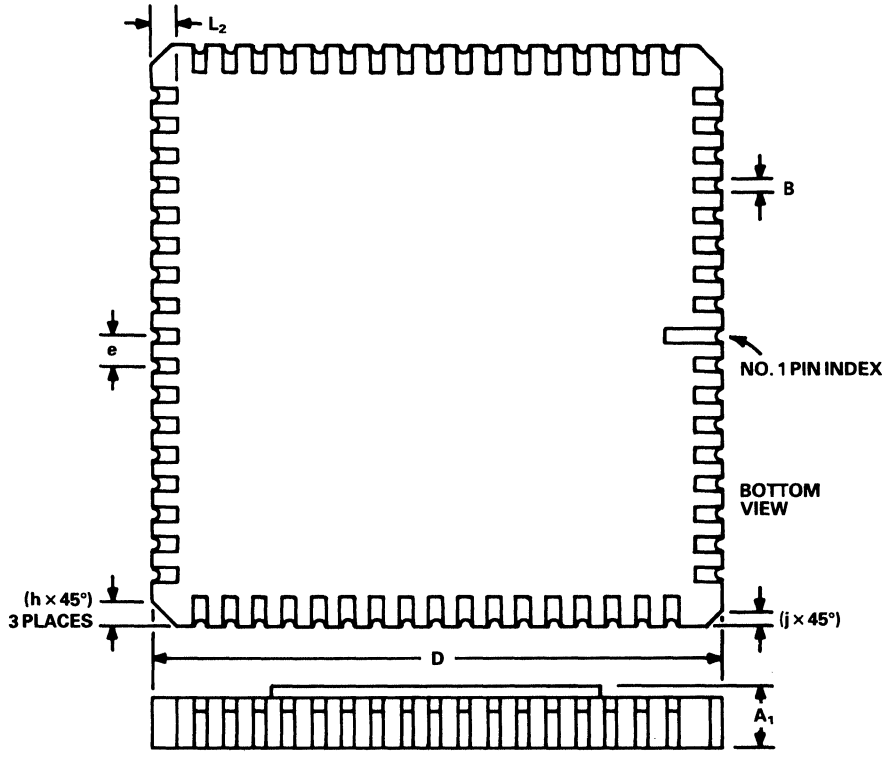
44-Terminal Leadless Ceramic Chip Carrier



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.640	0.662	16.27	16.82	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

E-68A
68-Terminal Leadless Chip Carrier



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A_1	0.065	0.103	1.65	2.62	1
B	0.020	0.030	0.51	0.76	
D	0.940	0.965	23.88	24.51	2
e	0.045	0.055	1.14	1.40	
h	0.040 TYP		1.02 TYP		
j	0.020 TYP		0.51 TYP		
L_2	0.045	0.055	1.14	1.40	

NOTES
1. Dimension controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

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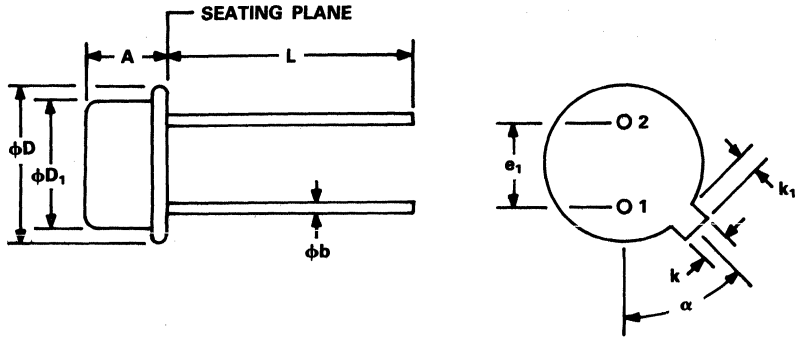
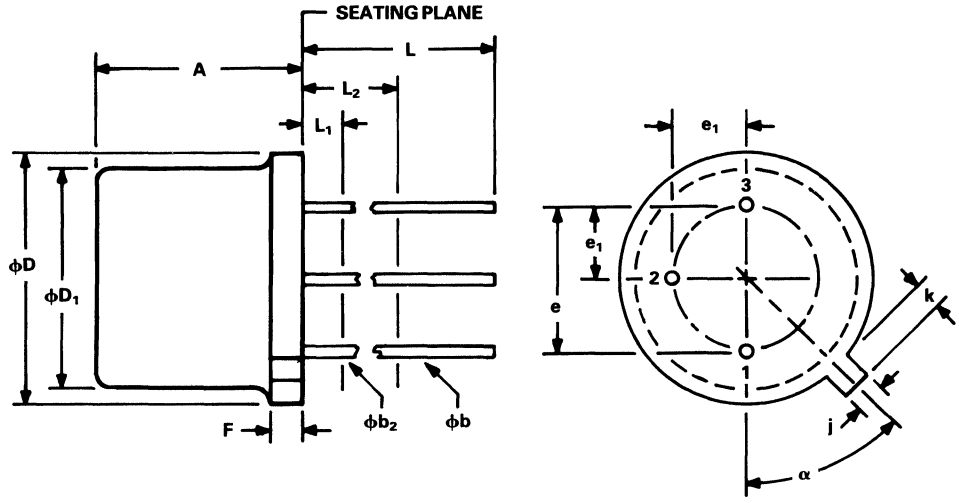
H-02A
2-Lead Metal Can



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.125	0.150	3.17	3.81	
ϕb	0.015	0.019	0.38	0.48	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e_1	0.100 BSC		2.54 BSC		1
k	0.036	0.045	0.91	1.17	
k_1	0.028	0.048	0.71	1.22	
L	0.500	0.750	12.70	19.05	
α	45° BSC		45° BSC		1

NOTES
1. Leads having maximum diameter 0.019″ (0.48mm) measured in gauging plane 0.54″ (1.37mm) + 0.001″ (0.03mm) – 0.000″ (0.00mm) below the seating plane of the device are within 0.007″ (0.18mm) of their true positions relative to the maximum-width tab.
2. All leads – increase maximum limit by 0.003″ (0.08mm) when hot solder dip finish is applied.

H-03A
3-Lead Metal Can (TO-52)

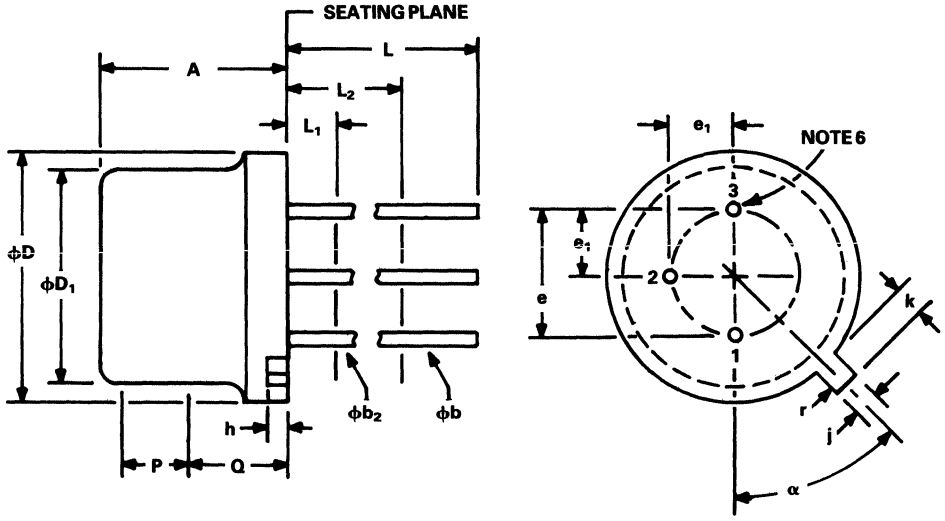


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.115	0.150	2.92	3.81	
ϕb		0.021		0.53	1,4
ϕb_2	0.016	0.019	0.41	0.48	1,4
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		2
e_1	0.050 T.P.		1.27 T.P.		2
F		0.030		0.76	
j	0.036	0.046	0.91	1.17	
k	0.028	0.048	0.71	1.22	3
L	0.500		12.70		1
L_1		0.050		1.27	1
L_2	0.250		6.35		
α	45° T. P.				

NOTES
1. (Three Leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.5" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.054" (1.4mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

H-03B

3-Lead Metal Can (TO-5 Style)

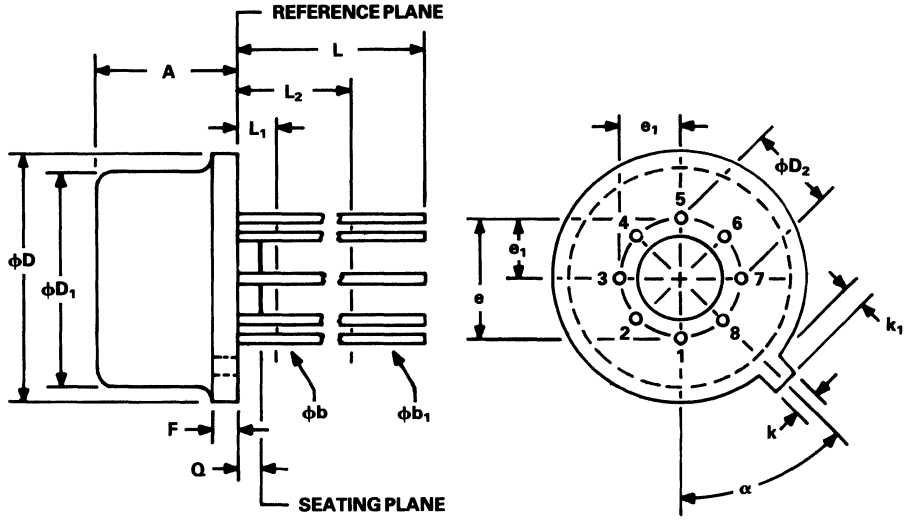


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.021	0.41	0.53	2, 7
ϕb_2	0.016	0.019	0.41	0.48	2, 7
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
e	0.200 T.P.		5.08 T.P.		4
e_1	0.100 T.P.		2.54 T.P.		
h	0.015	0.035	0.38	0.89	
j	0.028	0.034	0.71	0.86	
k	0.029	0.045	0.74	1.14	3
L	0.500		12.70		2
L_1		0.050		1.27	2
L_2	0.250		6.35		2
P	0.100		2.54		1
Q					5
r		0.007		0.18	
α	45° T.P.				

NOTES

1. This zone is controlled for automatic handling. The variation in actual diameter within the zone shall not exceed 0.010″ (0.25mm).
2. (Three leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.500″ (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500″ (12.70mm) from seating plane.
3. Measured from maximum diameter of the actual device.
4. Leads having maximum diameter 0.019″ (0.48mm) measured in gauging plane 0.54″ (1.37mm) + 0.001″ (0.03mm) – 0.000″ (0.00mm) below the seating plane of the device are within 0.007″ (0.18mm) of their true positions relative to the maximum-width tab.
5. Details of outline in this zone optional.
6. Lead #3 connected to case.
7. All leads – increase maximum limit by 0.003″ (0.08mm) when hot solder dip finish is applied.

H-08A
8-Lead Metal Can (TO-99)

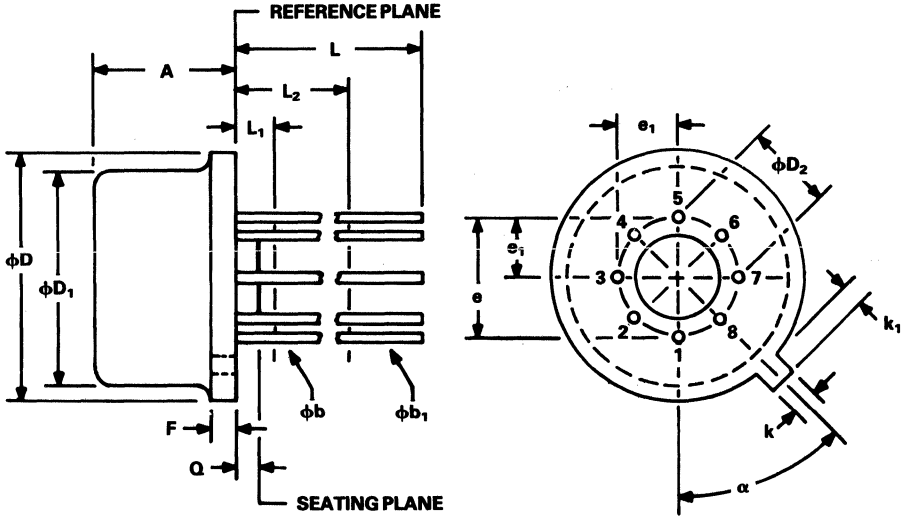


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	
L	0.500	0.750	12.70	19.05	
L_1		0.050		1.27	
L_2	0.250		6.35		
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES
1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500" (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product are within 0.007" (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003" (0.08mm) when hot solder dip finish is applied.

H-08B

8-Lead Metal Can (TO-99 Style)

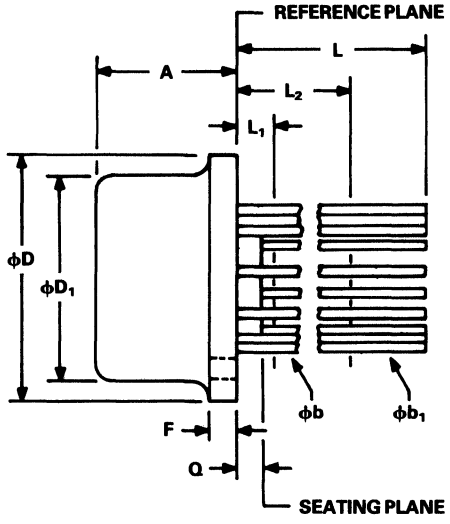


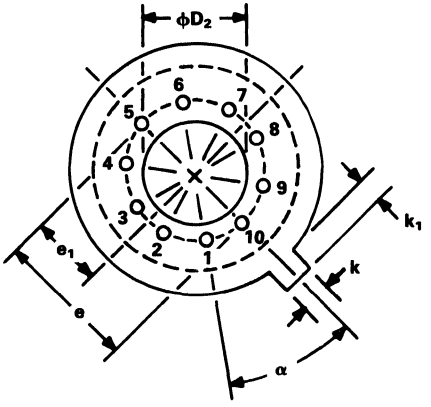
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500″ (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500″ (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019″ (0.48mm) measued in gauging plane 0.054″ (1.37mm) + 0.001″ (0.03mm) – 0.000″ (0.00mm) below the base plane of the product are within 0.007″ (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003″ (0.08mm) when hot solder dip finish is applied.

H-10A
10-Lead Metal Can (TO-100)

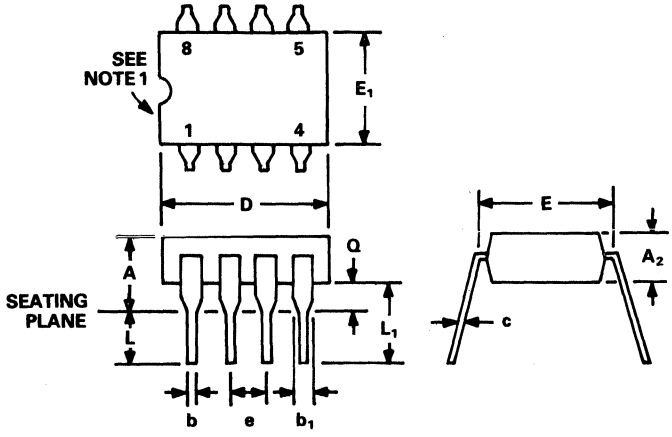




SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	36° BSC		36° BSC		3

NOTES
1. (Three Leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.5″ (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5″ (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019″ (0.48mm) measured in gauging plane 0.054″ (1.4mm) + 0.001″ (0.03mm) – 0.000″ (0.00mm) below the seating plane of the device are within 0.007″ (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003″ (0.08mm) when hot solder dip finish is applied.

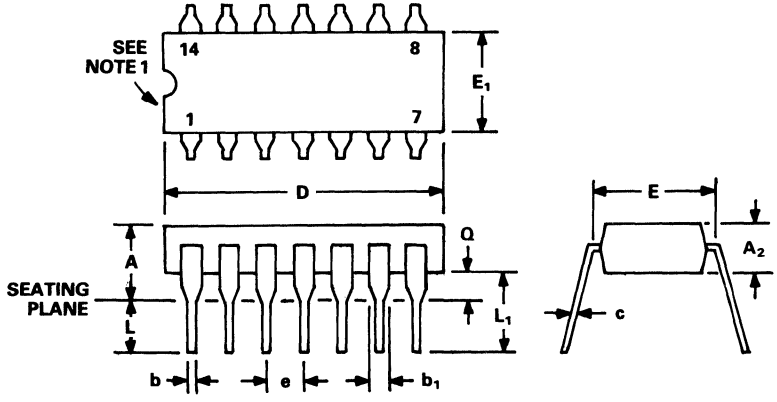
N-8
8-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

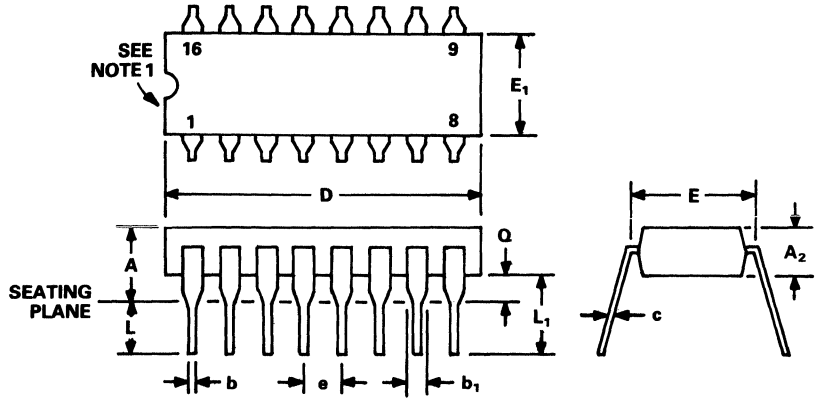
N-14
14-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

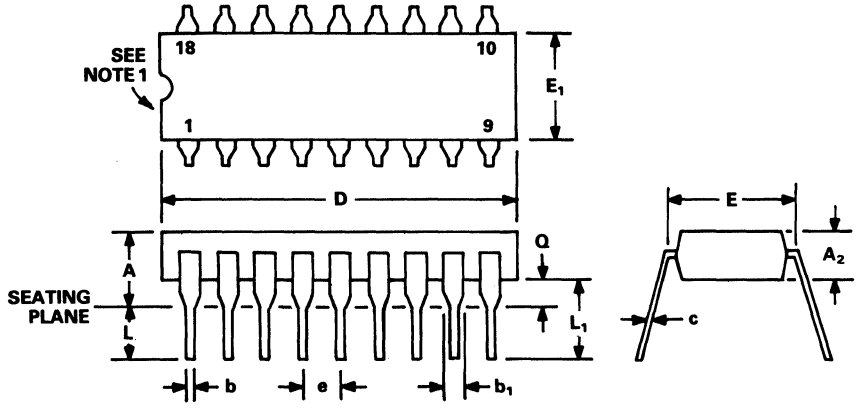
N-16
16-Lead Plastic DIP



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-18
18-Lead Plastic DIP

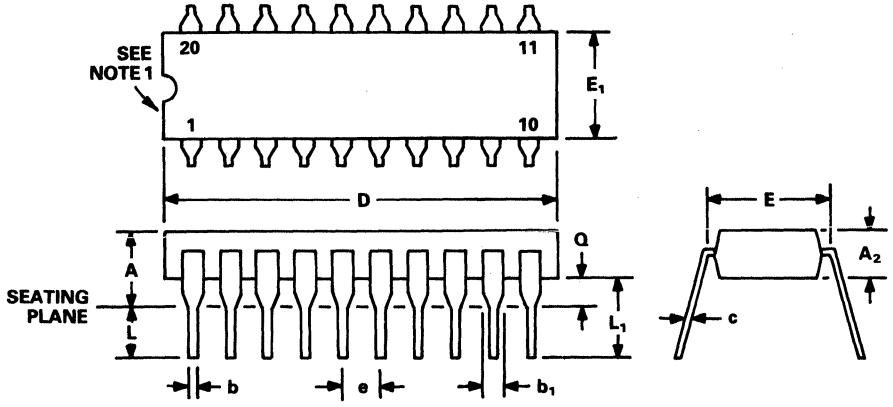


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.845	0.925	21.47	23.49	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

14

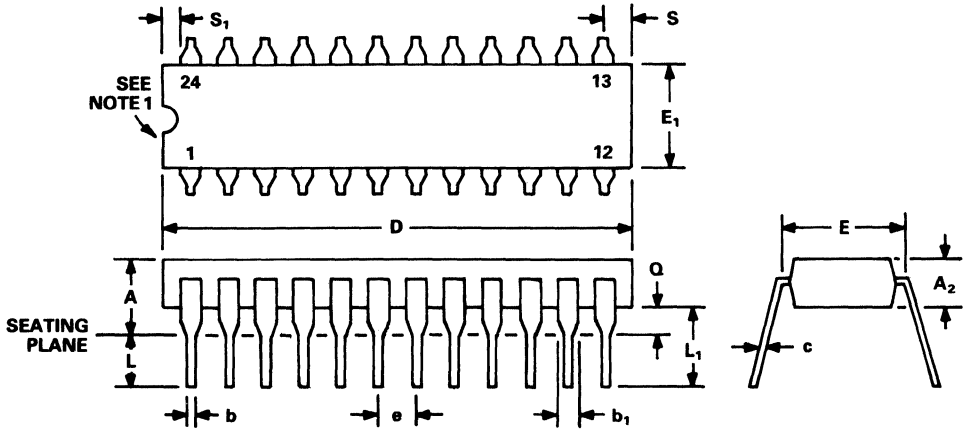
N-20
20-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.50	26.90	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-24
24-Lead Plastic DIP

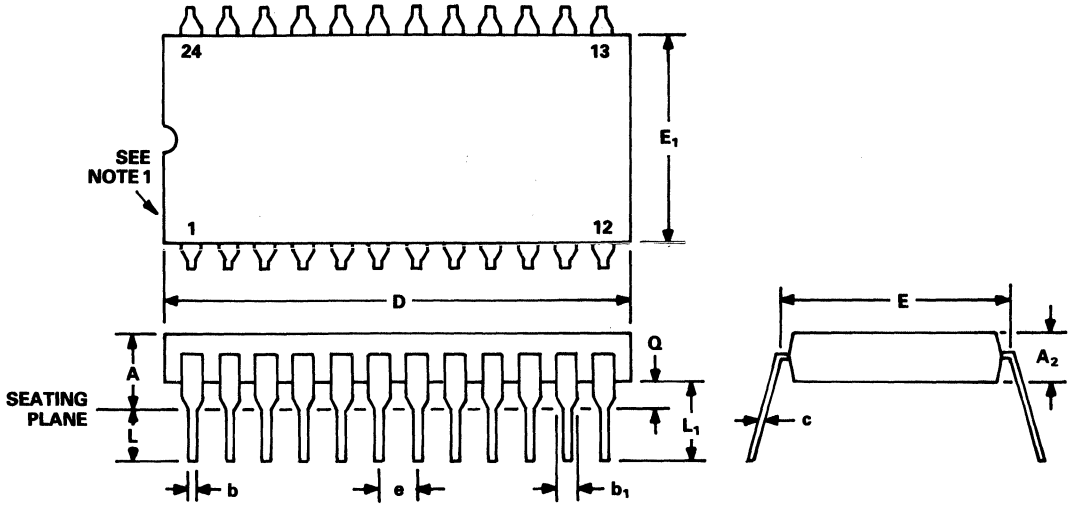


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.60	32.30	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

14

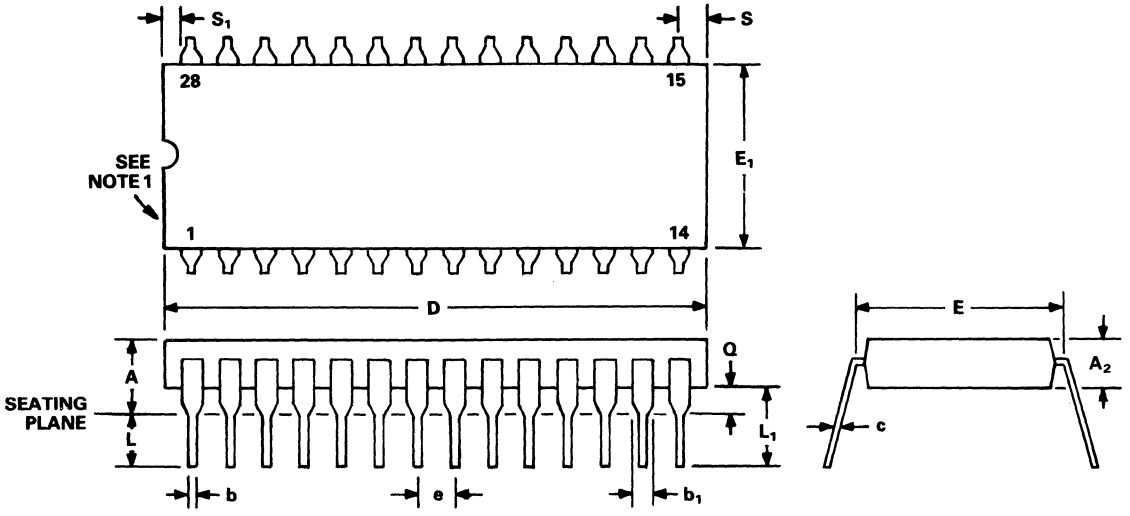
N-24A
24-Lead Plastic DIP (Double Width)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.250		6.35	
A_2	0.125	0.195	3.18	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.030	0.070	0.77	1.77	
c	0.008	0.015	0.204	0.381	
D	1.150	1.290	29.30	32.70	2
E	0.600	0.625	15.24	15.87	
E_1	0.485	0.580	12.32	14.73	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

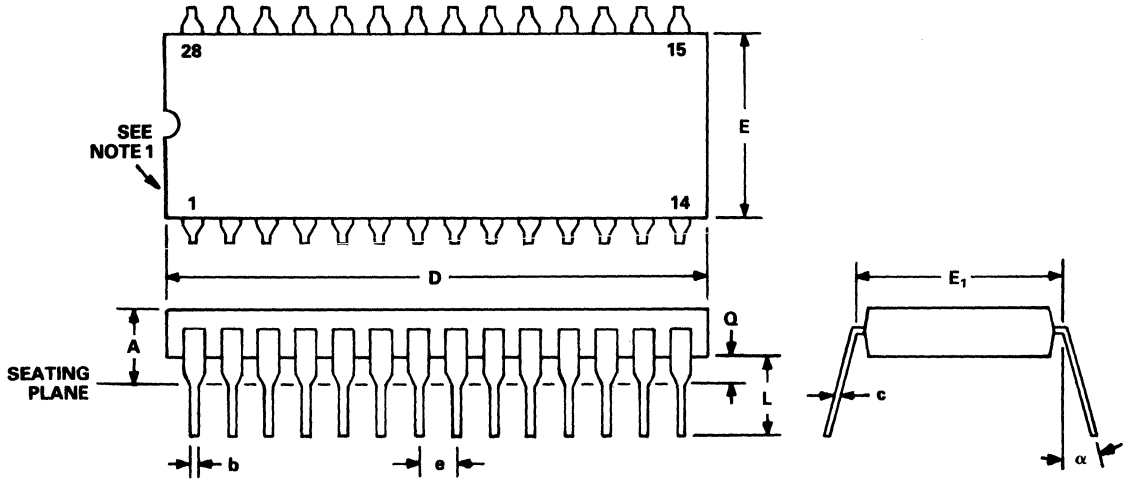
N-28
28-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.250		6.35	
A_2	0.125	0.195	3.18	4.95	
b	0.014	0.022	0.356	0.558	
b_1		0.070		1.77	
c	0.008	0.015	0.204	0.381	
D	1.380	1.565	35.10	39.70	2
E	0.600	0.625	15.24	15.87	
E_1	0.485	0.580	12.32	14.73	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

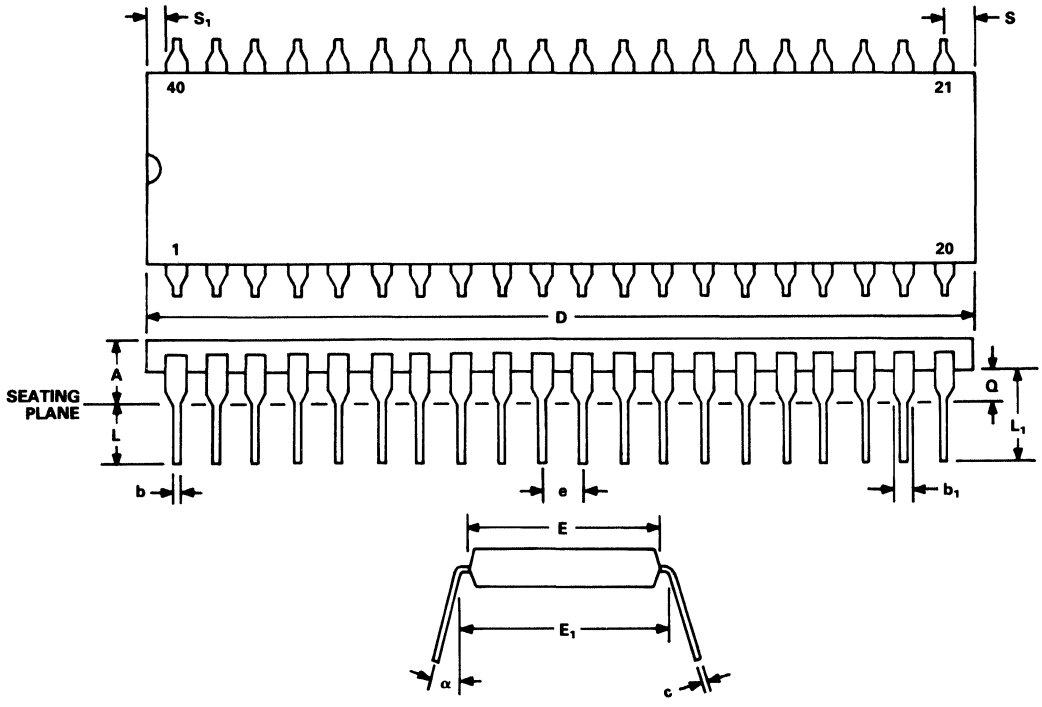
N-28A
28-Pin Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.080	
b	0.015	0.020	0.381	0.508	3
c	0.008	0.012	0.203	0.305	3
D	1.440	1.450	35.580	36.830	
E	0.530	0.550	13.470	13.970	
E_1	0.594	0.606	15.090	15.400	2
e	0.096	0.105	2.420	2.670	4
L	0.120	0.175	3.050	4.450	
Q	0.020	0.060	0.560	1.580	
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
3. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
4. Twenty-six spaces.

N-40A
40-Pin Plastic DIP

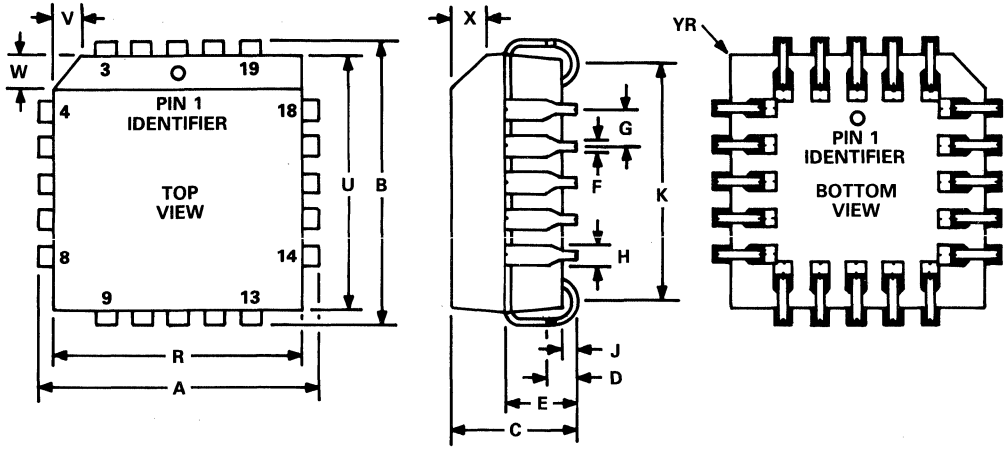


NOTE:
LEADS ARE SOLDER-PLATED KOVAR OR ALLOY 42

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
b	0.015	0.025	0.38	0.64
b_1	0.040	0.060	1.02	1.52
c	0.008	0.015	0.20	0.38
D	–	2.08	–	52.83
E	0.550	0.550	13.46	13.97
E_1	0.580	0.620	14.73	15.75
e	0.100 BSC		2.54 BSC	
L	0.120	0.175	3.05	4.45
L_1	0.140	–	3.56	–
Q	0.015	0.060	0.38	1.52
S	–	0.110	–	2.79
S_1	0.005	–	0.13	–
α	0°	15°	0°	15°

P-20A

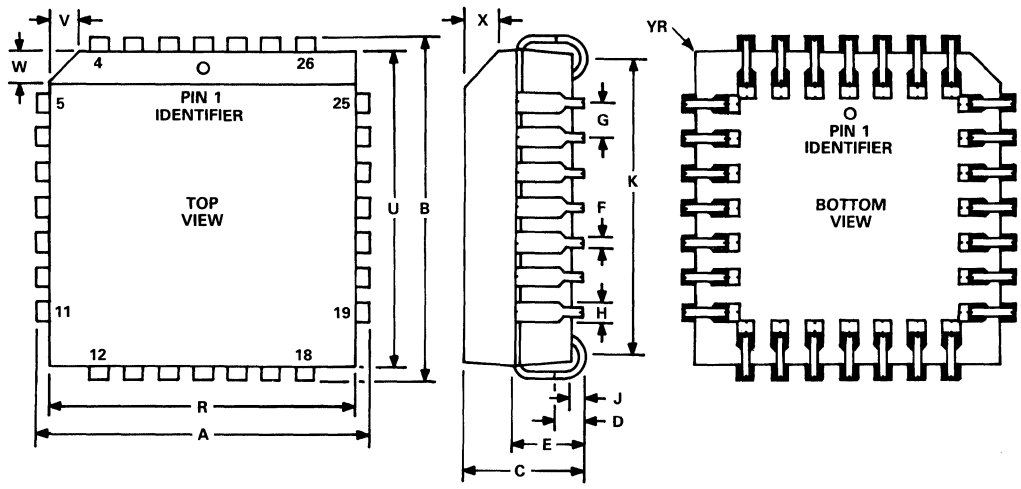
20-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.02
B	0.385	0.395	9.78	10.02
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.290	0.330	7.37	8.38
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-28A

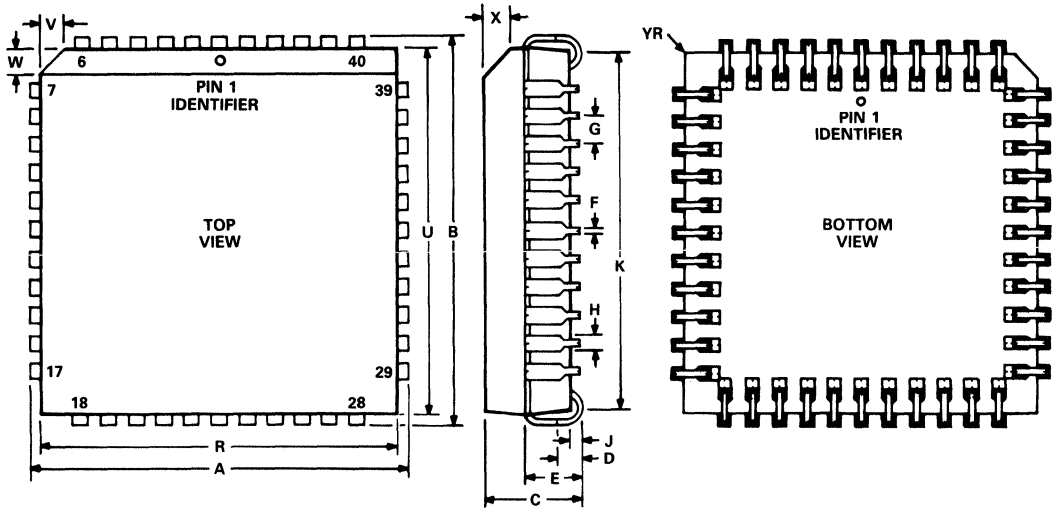
28-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.390	0.430	9.91	10.92
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

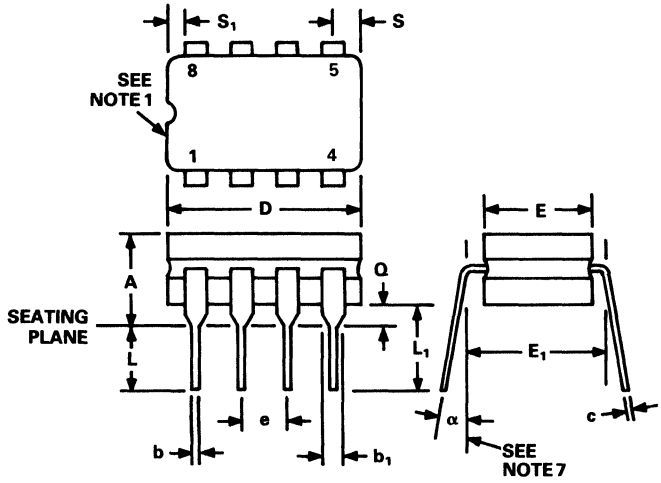
P-44A

44-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.650	0.656	16.51	16.66
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

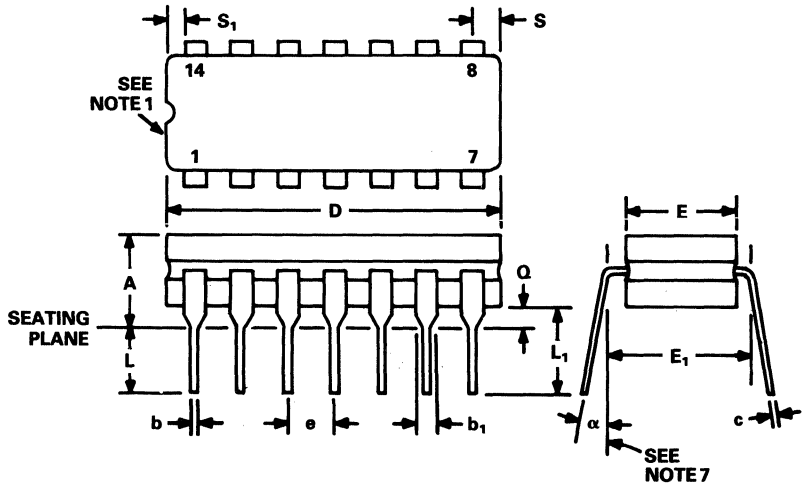
Q-8
8-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.35	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

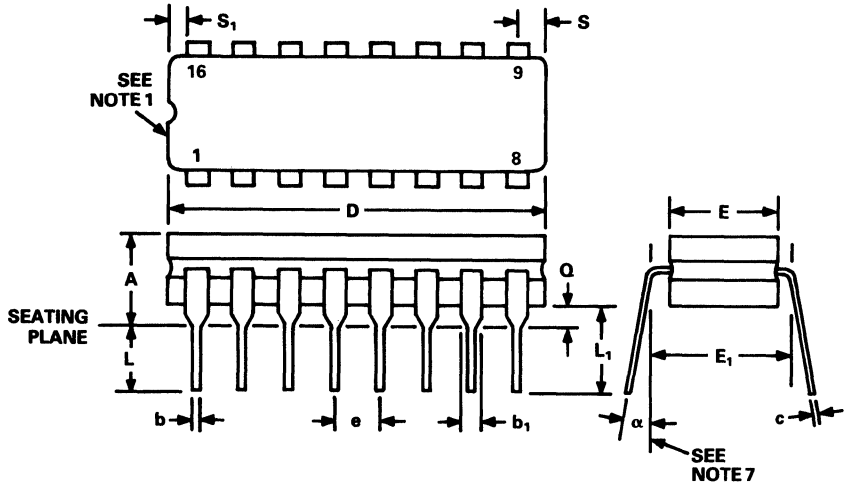
Q-14
14-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twelve spaces.

Q-16
16-Lead Cerdip

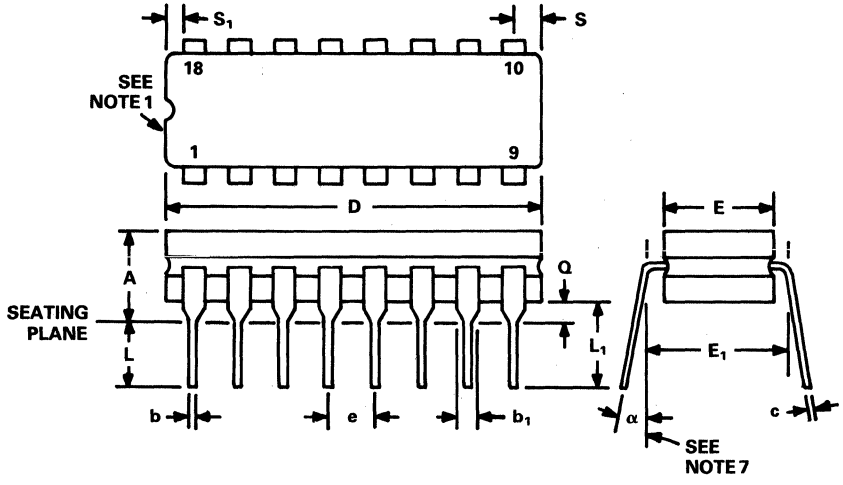


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Fourteen spaces.

14

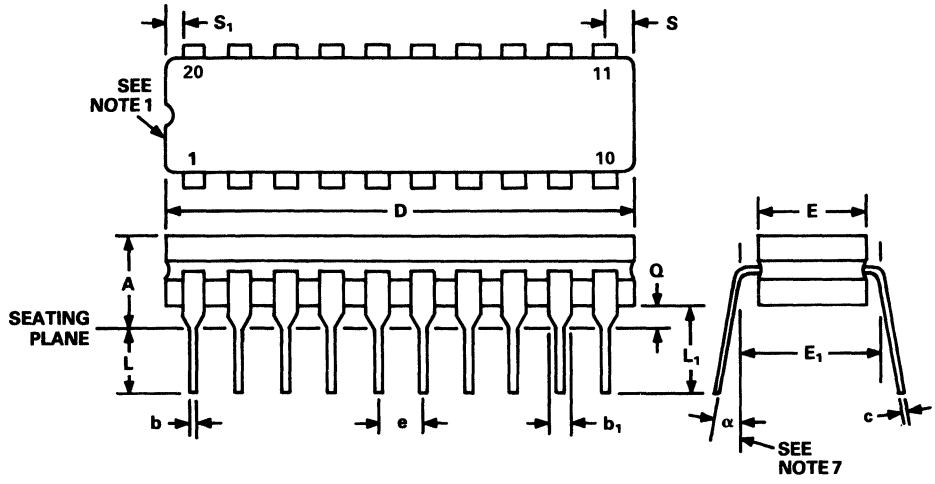
Q-18
18-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Sixteen spaces.

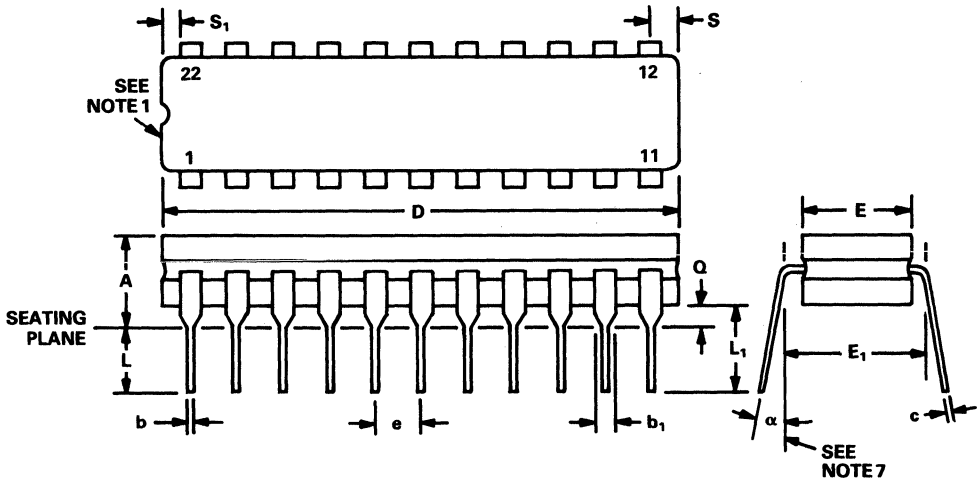
Q-20
20-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Eighteen spaces.

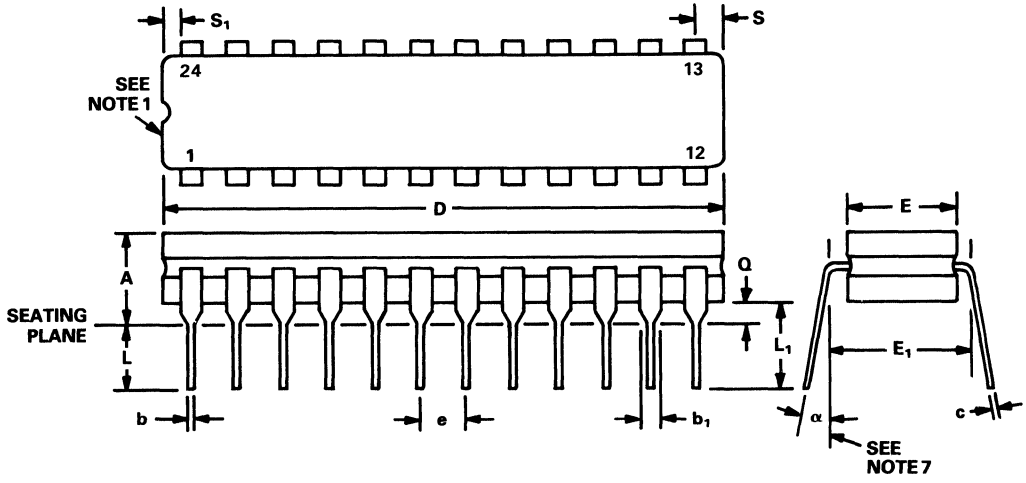
Q-22
22-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		1.175		29.85	4
E	0.320	0.410	8.13	10.41	4
E_1	0.390	0.420	9.09	10.67	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1		0.150		3.81	
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty spaces.

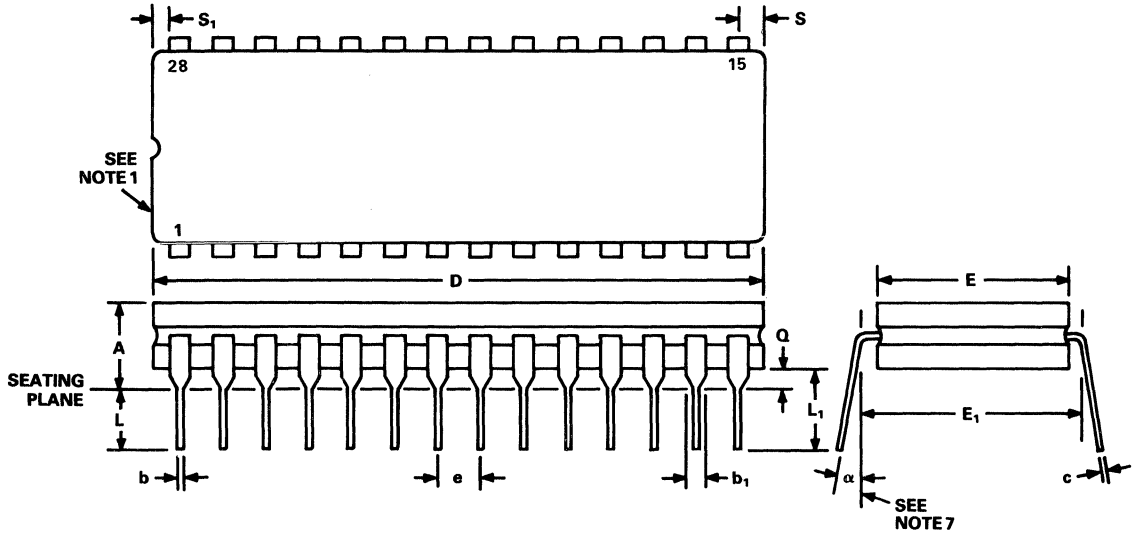
Q-24
24-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-two spaces.

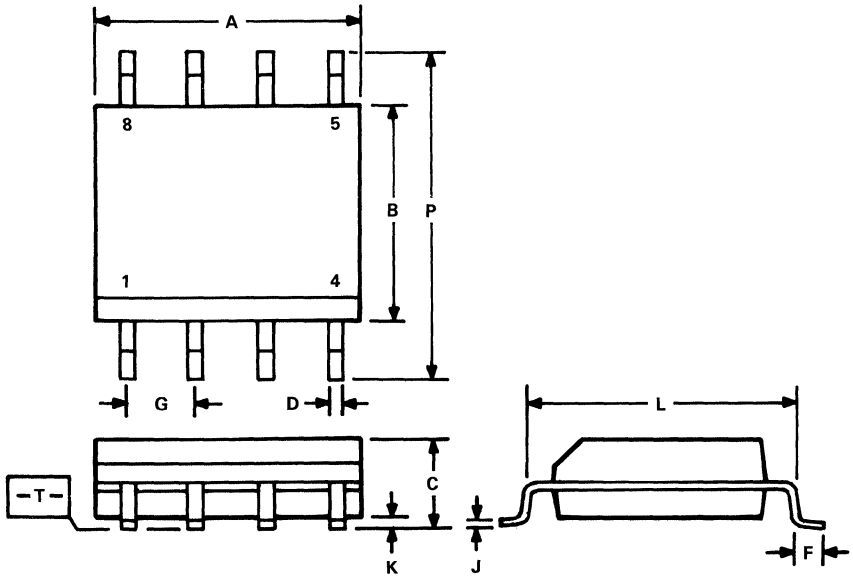
Q-28
28-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.018	0.20	0.46	7
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015		0.38		3
S		0.100		2.54	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

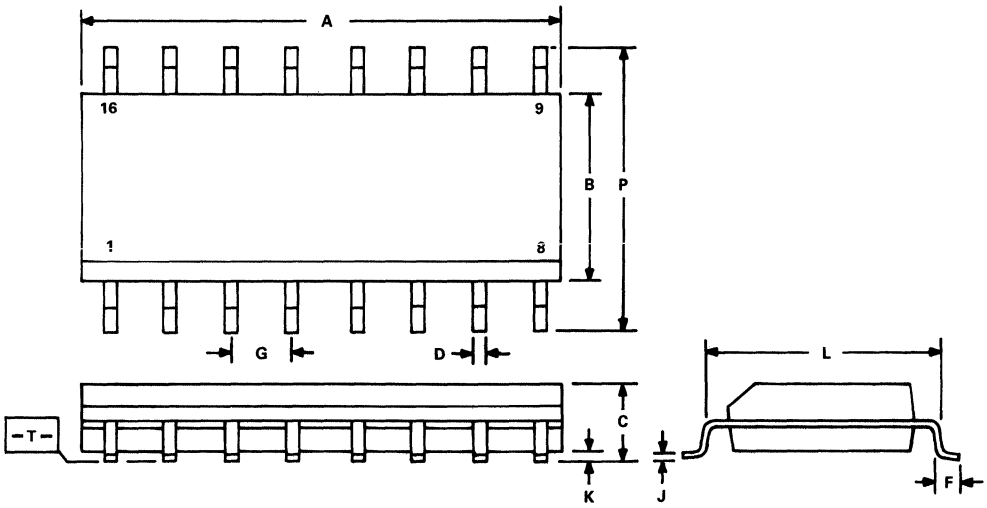
NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-six spaces.

R-8
8-Lead Small Outline (SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.188	0.198	4.77	5.03
B	0.150	0.158	3.81	4.01
C	0.089	0.107	2.26	2.72
D	0.014	0.022	0.36	0.56
F	0.018	0.034	0.46	0.86
G	0.050 BSC		1.27 BSC	
J	0.007	0.015	0.18	0.38
K	0.005	0.011	0.125	0.275
L	0.195	0.205	4.95	5.21
P	0.224	0.248	5.69	6.29

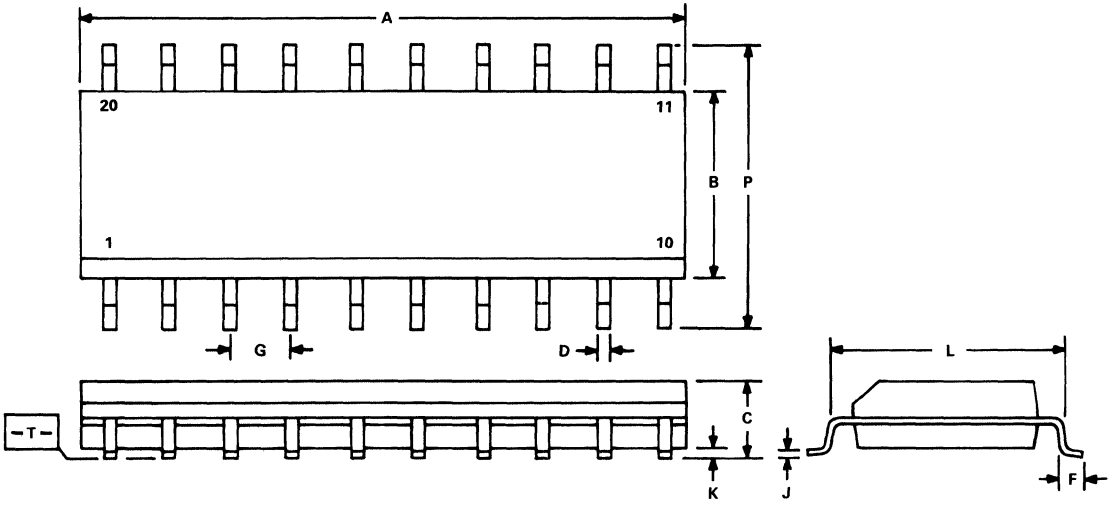
R-16
16-Lead Small Outline (SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.398	0.413	10.10	10.50
B	0.291	0.299	7.40	7.60
C	0.089	0.107	2.26	2.72
D	0.014	0.022	0.36	0.56
F	0.018	0.034	0.46	0.86
G	0.050 BSC		1.27 BSC	
J	0.007	0.015	0.18	0.38
K	0.005	0.011	0.125	0.275
L	0.195	0.205	4.95	5.21
P	0.404	0.419	10.26	10.65

R-20

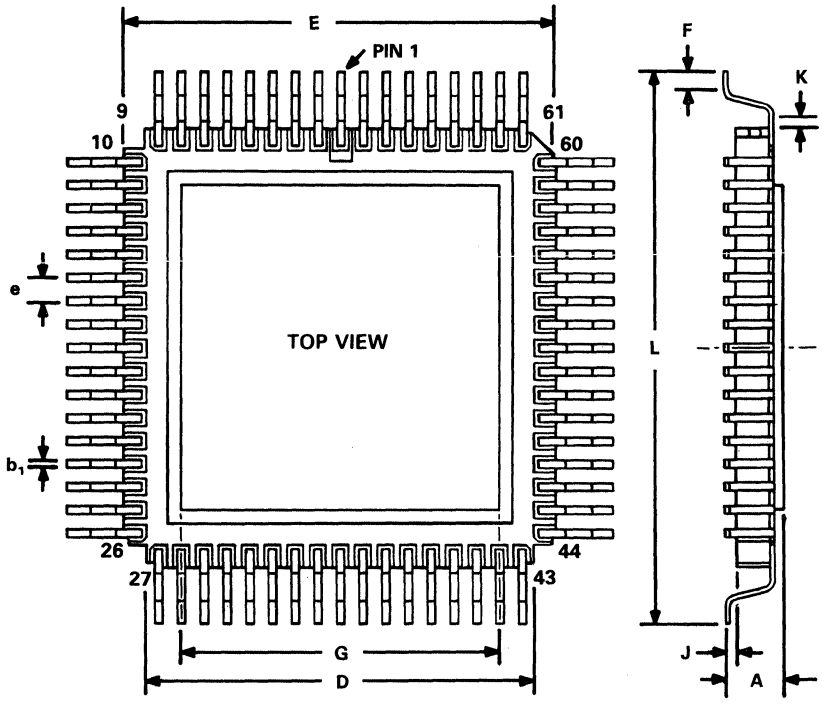
20-Lead Small Outline (SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.496	0.512	12.60	13.00
B	0.291	0.299	7.40	7.60
C	0.089	0.107	2.26	2.72
D	0.014	0.022	0.36	0.56
F	0.018	0.034	0.46	0.86
G	0.050 BSC		1.27 BSC	
J	0.007	0.015	0.18	0.38
K	0.005	0.011	0.125	0.275
L	0.195	0.205	4.95	5.21
P	0.404	0.419	10.00	10.65

Z-68

68-Lead Leaded Chip Carrier (Ceramic)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.092	0.118	2.337	2.997
b_1	0.016	0.020	0.452	0.462
D	0.841	0.859	21.361	21.819
e	0.050 BSC		1.27 BSC	
E	0.940	0.960	23.876	24.384
F	0.040		1.016	
G	0.695	0.705	17.653	17.907
K	0.025		0.625	
L	1.200	1.220	30.476	30.984

Appendix Contents

Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

Many of the data sheets in the Databook for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. I.C. and hybrid part numbers are created using one of these two systems:

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit model number*, an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows the somewhat different numbering scheme used by our Computer Labs Division for some hybrid circuits. The number starts with a three-character alphabetic prefix, followed by a hyphen, a three- or four-digit number, and alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

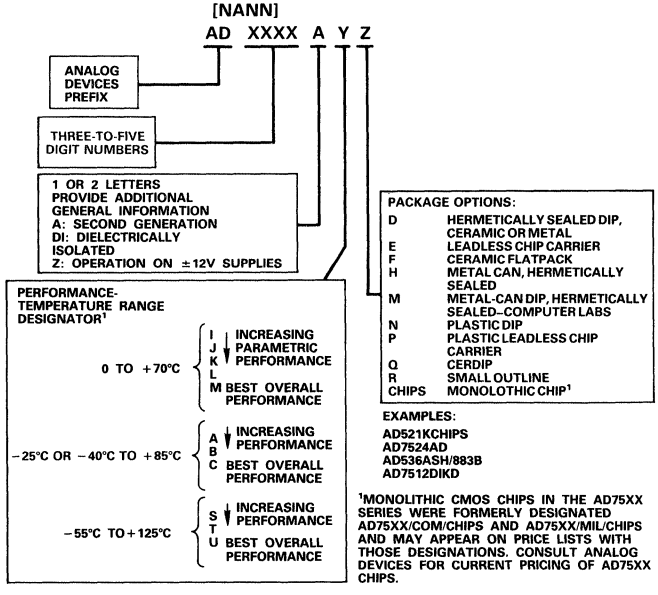


Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades have the Added Suffix, /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

***For some models, the combination [digit][letter][two or three digits] is used instead of ADXXXX, e.g., 2S80.**

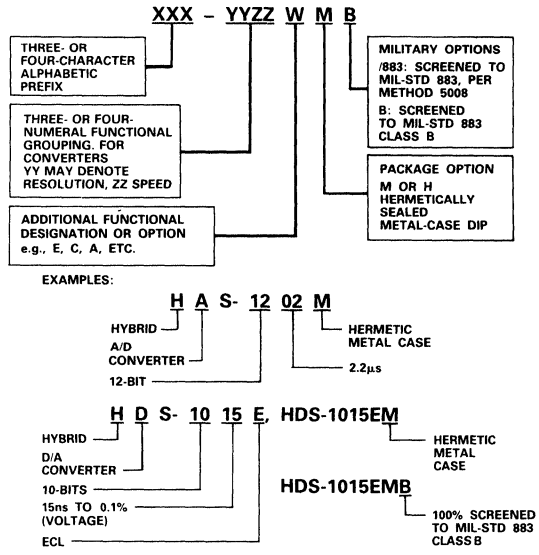


Figure 2. Computer Labs Video Hybrid Product Designations

SECOND SOURCE

In addition to our many proprietary products, we also manufacture devices that are fit-, form-, and function-compatible (and often superior in performance and reliability) to popular products that originated elsewhere. For such products, we usually add the prefix "AD" to the familiar model number (example: ADDAC85C-CBI-V).

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via TWX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. On all orders under fifty dollars ($50.00), a five-dollar ($5.00) processing charge is required.

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and µMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Not Included in the Databook (But Still Available)

The information published in this Databook is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs or in designs for which they are uniquely suitable. Data sheets on these products are available upon request.

Model	Model	Model	Model	Model
AD101	AD7522	DAS1128	SDC1702/RDC1702	234
AD108/208/308	AD7523	DAS1150	SDC1704/RDC1704	235
AD108A/208A/308A	AD7525	DAS1151	SDC1711/RDC1711	260
AD111/211/311	AD7530	DAS1155	SDC1721	261
AD293	AD7531	DAS1156	SDC1725/RDC1725	272
AD294	AD7541	DRC1765/66	SDC1726/RDC1726	273
AD351	AD7546	DSC1705/06	SDC1768/RDC1768	275
AD370/371	AD7550	DTM1716/17	SHA-2A	276
AD503	AD7552	HAS-0802	SHA-5	277
AD506	AD7571	HAS-1002	SHA-1114	285
AD510	AD7574	HDD-1409	SHA-1134	288
AD515	AD ADC-816	HDH-0802	SHA-1144	310
AD518	ADC-10Z	HDH-1003	SSCT1621	426
AD528	ADC-12QZ	HDH-1205	STM Series	428
AD530	ADC-14I/17I	HDL-3806	TSL1612	429
AD531	ADC1100	HDS-0810E	2B24	432
AD533	ADC1105	HDS-0820	2B34	433
AD535	ADC1111	HDS-1015E	2B52	434
AD545	ADC1143	HDS-1025	2B53	435
AD567	ADC-QM	HDS-1240E	2B56	436
AD611	AD DAC-08	IPA1751	2B57A-1	440
AD651	ADG201	IRDC1730	2B58A	442
AD801	ADSHC-85	IRDC1731	2B59A	450
AD2004	API1620/1718	IRDC1732	2S20	452
AD2006	BDM 1615/16	IRDC1733	40	458
AD2008	BDM 1617	MATV-0811	44	460
AD2009	CAV-0920	MATV-0816	45	606
AD2016	CAV-1210	MATV-0820	46	610
AD2020	DAC-M	MCI1794	48	756
AD2033	DAC-QS	MOD-1005	50	903
AD2036	DAC-QZ	MOD-1020	51	906
AD2037	DAC-10Z	OSC1754	52	915
AD2038	DAC1009	RDC1721	118	926
AD2040	DAC1108	RTM Series	171	947
AD3554	DAC1132	SAC1763	233	959
AD3860	DAC1146	SBCD1752/53		968
AD6012	DAC1420	SBCD1756/57		
AD7110	DAC1422	SCDX1623		
AD7118	DAC1423	SCM1677		
AD7506		SDC1604		
AD7507		SDC1700/RDC1700		
AD7520				
AD7521				

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but – as a rule – they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
AD362	AD1362	ADM501	ADM501/506	SERDEX	μMAC-5000	424	435/AD534
AD376	AD1376	ADP501	ADP511	SHA-1A	None	427	None
AD501	AD711	ADSHM-5	HTC-0300	SHA-3	None	454	AD537
AD502	AD711	CAV-1020	MOD-1020	SHA-4	None	456	AD537
AD505	AD509	CAV-1202	None	SHA-6	SHA1144	602J10	AD524
AD508	AD517	DAC-100F	None	THC-0300	HTC-0300	602J100	AD524
AD511	AD711	DAC-10H	DAC-10Z	THC-0750	None	602K100	AD524
AD512	AD711	DAC1106	None	THC-1500	None	603	AD524
AD513	AD711	DAC1112	DAC12QS	THS-0025	HTC-0300	605	AD524
AD514	AD711	DAC1118	None	THS-0060	HTC-0300	752	759
AD516	AD711	DAC1122	AD7541	THS-0225	None	901	904
AD520	AD524	DAC1125	AD7533	TSDC1608-1611	TSL1612	907	921
AD523	AD549	HDL-3805	HDL-3806	2N3954	None	908	921
AD546	AD711	HTC-0500	HTC-0300	2N5900	None	909	921
AD555	AD7519	IDC1703	IRDC1730/1731	41	AD515	931	None
AD559	None	MAH-0801	HAS-0802	43	AD549	932	None
AD612	AD524	MAH-1001	HAS-1002	47	48	933	None
AD614	AD524	MAS-0801	HAS-0802	101 (Module)	45	935	None
AD810-813	None	MAS-1001	HAS-1002	102	48	942	None
AD814-816	None	MAS-1202	HAS-1202	106	118	944	None
AD818	None	MDA-LB	None	107	118	946	None
AD820-822	None	MDA-LD	None	108	52	948	947
AD830-833	None	MDA-UB	None	110	48	956	None
AD835-839	None	MDA-UD	None	111	AD308	971	921
AD1408	None	MDA-8H	None	114	None		
AD1508	None	MDA-10H	None	115	None		
AD2003	AD2021	MDA-10Z	None	120	50		
AD2022	None	MDA-11MF	AD7521	141	40		
AD2023	None	MDH-0870	None	142	48		
AD2024	None	MDH-1001	None	143	52		
AD2025	None	MDH-1202	None	146	AD382		
AD2027	None	MDMS-0801	AD9768	149	50		
AD2028	None	MDMS-1001	HDM-1210	153	AD517		
AD5010/6020	AD9000	MDMS-1101	HDM-1210	161	None		
AD7115	None	MDS-0815	None	163	None		
AD7513	None	MDS-0815E	None	165	None		
AD7516	AD7510DI	MDS-0830	HDS-0820	170	171		
AD7519	None	MDS-0850	HDS-0820	180	AD OP-07		
AD7527	None	MDS-1020	None	183	184		
AD7544	None	MDS-1020E	None	220	234		
AD7555	None	MDS-1040	HDS-1025	230	235		
AD7560	None	MDS-1080	HDS-1025	231	233		
AD7570	None	MDS-1240	None	232	235		
AD7583	None	MDSL-0802	HDS-0820	274J	284J		
ADC-8S	None	MDSL-0825	None	279	286J		
ADC1102	None	MDSL-1002	HDS-1025	280	281		
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ADC1109	None	MDSL-1201	HDS-1250	283J	292A		
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AD DAC100	None	RTI-1201	RTI-711 Series	311	None		
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Technical Publications

TECHNICAL PUBLICATIONS

Analog Devices provides a wide array of FREE technical publications. These include Data Sheets for all products, Catalogs, Application Notes and Guides and four serial publications. *Analog Productlog*, a digest of new-production information; *DSPatch™*, a newsletter about digital signal-processing (applications); *Analog Briefings*, current information about products for military/avionics and the status of reliability at ADI; and *Analog Dialogue*, our technical magazine, with in-depth discussions of products, technologies and applications.

In addition to the free publications, five technical reference books are available at reasonable cost. Subsystem products are supported with hardware, software, and user documentation, at prices related to content.

Brief descriptions of typical publications appear below. For copies of any items, to subscribe to any of our free serials or to request any other publications, please get in touch with Analog Devices or the nearest sales office.

CATALOGS

Data Acquisition Products Databooks. Contain selection guides, data sheets and other useful information about all Analog Devices ICs, hybrids, modules and subsystem components recommended for new designs. The 1989/90 series consists of:

DATA CONVERSION PRODUCTS DATABOOK—1989/90. Data Sheets and Selection Guides on D/A, A/D, V/F, and F/V Converters, Sample-Track/Hold Amplifiers, Voltage References, Multiplexers & Switches, Synchro-Resolver Converters, Data Acquisition Subsystems, Application-Specific ICs. (Available FREE.)

DSP PRODUCTS DATABOOK—1989. Data Sheets, Selection Guides and Application Notes on DSP Microprocessor, Microcoded Support Components, Floating-Point Components and Fixed-Point Components. (Available FREE.)

LINEAR PRODUCTS DATABOOK—1989/90. Data Sheets and Selection Guides on Op Amps, Instrumentation Amplifiers, Isolators, RMS-to-DC Converters, Multipliers/Dividers, Log/Antilog Amplifiers, RMS-to-DC Converters, Comparators, Temperature-Measuring Components and Transducers, Special Function Components, Digital Panel Instruments, Signal-Conditioning Components and Subsystems. (Available FREE.)

MILITARY PRODUCTS DATABOOK. Information and data on products processed in accordance with MIL-STD-883 Class B.

PERSONAL-COMPUTER BASED MEASUREMENT & CONTROL SOLUTIONS—Hardware and Software. Data acquisition for various buses, including PC/XT/AT* and PS/2* Micro Channel*, Modular Signal Conditioners, Signal-Conditioning Panels, Application Software, and Driver Software. Includes Do-It-Yourself Ordering Guides and Hot Line (1-800-4-ANALOG).

POWER SUPPLIES–Linear Supplies•DC-DC Converters. 12-page short-form catalog listing ac/dc power supplies, modular dc/dc converters, power-supply test procedures, transients, thermal derating, mechanical outlines of packages and sockets.

APPLICATION NOTES AND GUIDES

All are available upon request.

Application Notes.

A/D Converters:
- "Exploring the AD667 12-Bit Analog Output Port."
- "Interacing the AD7572 to High-Speed DSP Processors."
- "The AD7574 Analog-to-Microprocessor Interface."

Amplifiers:
- "An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change."
- "Applications of High-Performance BiFET Op Amps."
- "A User's Guide to IC Instrumentation Amplifiers."
- "How to Select Operational Amplifiers."
- "How to Test Basic Operational Amplifier Parameters."
- "Low-Cost Two-Chip Voltage-Controlled Amplifier and Video Switch."
- "Using the AD9610 Transimpedance Amplifier."

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- "Bipolar Operation with the AD7572."
- "Circuit Applications of the AD7226 Quad CMOS DAC."
- "CMOS D/A Converter Circuits for +5-Volt Supplies."
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- "How to Obtain the Best Performance from the AD7572."
- "Interfacing the AD7549 Dual 12-Bit DAC to the MCS-48 and MCS-51 Microcomputer Families."
- "Simple DAC-Based Circuit Implements Constant Linear Velocity (CLV) Motor Speed Control."
- "Simple Interface Between D/A Converter and Microcomputer Leads to Programmable Sine-Wave Oscillator."
- "The AD7224 DAC Provides Programmable Voltages Over Varying Ranges."
- "Three-Phase Sine Wave Generation Using the AD7226 Quad DAC."

Digital Signal-Processing (Note: Four additional DSP Application Notes will be found in the *1989 DSP Products Databook*):
- "Considerations for Selecting a DSP Processor." (ADSP-2100A vs. TMS320C25)
- "Implement a Cache Memory in Your Word-Slice® System."
- "Implement a Writeable Control Store in Your Word-Slice® System."
- "Loading an ADSP-2101 Program via the Serial Port."
- "Sharing the Output Bus of the ADSP-1401 Microprogram Sequencer."

"Variable-Width Bit Reversing with the ADSP-1410 Address Generator."

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"Use of the AD590 Temperature Transducer in a Remote Sensing Application."

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"Operation and Applications of the AD654 IC V-to-F Converter."

Video Applications:

"Changing Your VGA Design from a 171/176 to an ADV471."

"Improved PCB Layouts for Video RAM-DACs Can Use Either PLCC or DIP Package Types."

"The AD9502 Video Signal Digitizer and Its Application."

"Video Formats & Required Load Terminations."

Application Guides.

Analog CMOS Switches and Multiplexers. A 16-page short-form guide to high-speed CMOS switches, CMOS switches with dielectric isolation and CMOS multiplexers. Also included are reliability data and information on single-supply operation.

Applications Guide for Isolation Amplifiers and Signal Conditioners. A 20-page guide to specifications and applications of galvanically isolated amplifiers and signal conditioners for industrial, instrumentation and medical applications.

CMOS DAC Application Guide 3rd Edition by Phil Burton (1989—64 pages). Introduction to CMOS DACs, Inside CMOS DACs, Basic Application Circuits in Current-Steering Mode, Single-Supply Operation Using Voltage-Switching Mode, The Logic Interface, Applications.

ESD Prevention Manual – Protecting ICs from electrostatic discharges. Thirty pages of information that will assist the reader in implementing an appropriate and effective program to assure protection against electrostatic discharge (ESD) failures.

High-Speed Data Conversion – A 24-page short-form guide to video and other high-speed A/D and D/A converters and accessories, in forms ranging from monolithic ICs to card-level products.

RMS-to-DC Conversion Application Guide 2nd Edition by C. Kitchin and L. Counts (1986—61 pages). RMS-DC Conversion: Theory, Basic Design Considerations; RMS Application Circuits; Testing Critical Parameters; Input Buffer Amplifier Requirements; Programs for Computing Errors, Ripple and Settling Time.

Surface Mount IC—A 28 page guide to ICs in SO and PLCC packages. Products include op amps, rms-to-dc converters, DACs, ADCs, VFCs, sample-holds and CMOS switches.

DSP MANUALS

Available at no charge for single copies; write on letterhead.

ADSP-2100 Family Support Publications—for the ADSP-2100 and ADSP-2101 single-chip signal processors.

ADSP-2100 USER'S MANUAL. Introduction, Computational Units, Data Moves, Program Control, System Interface, Instruction Set Overview, Appendixes. 162 pages.

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ADSP-2100 EVALUATION BOARD MANUAL. Overview; Installation; Configuration; Operation; Analog Interface; Prototyping Connector; Demonstration Programs; Appendixes: Specification, Replacing Hardware, Terminal Emulation, Memory Expansion, Demo Disk, Schematics/Data Sheets. 156 pages.

ADSP-2101 USER'S MANUAL—Architecture. Introduction, Computational Units, Data Moves, Program Control, Timer, Serial Ports, System Interface, Memory Interface, Instruction Set Overview, Appendixes. 184 pages.

ADSP-2100 FAMILY APPLICATIONS HANDBOOK, Volume 1. Introduction, Fixed-Point Arithmetic, Floating-Point Arithmetic, Fixed-Coefficient Digital Filters, FFTs, Adaptive Filters, Image Processing, Linear Predictive Speech Coding, High-Speed Modem Algorithms, Bibliography. 178 pages.

ADSP-2100 FAMILY APPLICATIONS HANDBOOK, Volume 2. Overview, Graphics, Multirate Filters, PCM, ADPCM, Dual-Tone Multi-Frequency (DTMF). 248 pages.

ADSP-2100 FAMILY APPLICATIONS HANDBOOK, Volume 3. Introduction, Fast Fourier Transforms, Memory Interface, Multiprocessing, Host Interface, Sonar Beamforming. 168 pages.

Word-Slice User's Manual (ADSP-1401/ ADSP-1402 Program Sequencers and ADSP-1410 Address Generator). Introduction; Program Sequencers: Internal Architecture, Jumps, Interrupt Processing, System Interface, Instruction Set; ADSP-1410: Internal Architecture, Addressing Operations, Precision Modes, System Interface, Instruction Set. 218 pages.

Technical Publications

TECHNICAL REFERENCE BOOKS—Can be purchased from Analog Devices, Inc.; send check for indicated amount to One Technology Way, P.O. Box 796, Norwood, MA 02062. If more than one book is ordered, deduct a discount of $1 from the price of each book. VISA accepted; phone (617) 461-3392.

ANALOG-DIGITAL CONVERSION HANDBOOK: Third Edition, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice-Hall (1986). A comprehensive guide to A/D and D/A converters and their applications. This third edition of our classic is in hard-cover and has more than 700 pages, an Index, a Bibliography, and much new material, including: video-speed, synchro-resolver, V/F, high-resolution, and logarithmic converters, ICs for DSP, and a "Guide for the Troubled." Seven of its 22 chapters are totally new. $32.95

NEW–DIGITAL SIGNAL PROCESSING IN VLSI, by Richard J. Higgins. Englewood Cliffs NJ: Prentice-Hall (1990). An introductory 614-page guide for the engineer and scientist who needs to understand and use DSP algorithms and special-purpose DSP hardware ICs—and the software tools developed to carry them out efficiently. Real-World Signal Processing; Sampled Signals and Systems; The DFT and the FFT Algorithm; Digital Filters; The Bridge to VLSI; Real DSP Hardware; Software Development for the DSP System; DSP Applications; plus Bibliography and Index. $38.00

NONLINEAR CIRCUITS HANDBOOK: Designing with Analog Function Modules and ICs, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1974). A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction devices. Principles, circuitry, performance, specifications, testing, and application of these devices–Contains 325 illustrations. $5.95

SYNCHRO & RESOLVER CONVERSION, edited by Geoff Boyes. Norwood, MA; Analog Devices, Inc. (1980). Principles and practice of interfacing synchros, resolvers, and Inductosyns* to digital and analog circuitry. $11.50

TRANSDUCER INTERFACING HANDBOOK: A Guide to Analog Signal Conditioning, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1980). A book for the electronic engineer who must interface transducers for temperature, pressure, force, level, or flow to electronics, these 260 pages tell how transducers work—as circuit elements—and how to connect them to electronic circuits for effective processing of their signals. $14.50

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G1182a–175–7/89