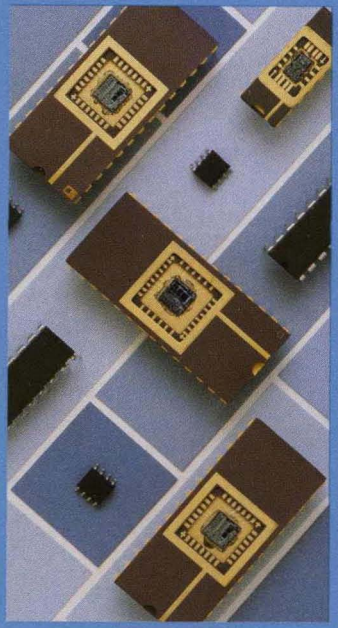
ANALOG DEVICES

1990/91



LINEAR PRODUCTS DATABOOK

OPERATIONAL AMPLIFIERS
COMPARATORS
INSTRUMENTATION AMPLIFIERS
ISOLATION AMPLIFIERS
ANALOG MULTIPLIERS/DIVIDERS
LOG/ANTILOG AMPLIFIERS
RMS-TO-DC CONVERTERS
MASS STORAGE COMPONENTS
ATE COMPONENTS
TEMPERATURE TRANSDUCERS
SIGNAL CONDITIONING COMPONENTS & SUBSYSTEMS
AUTOMOTIVE COMPONENTS
APPLICATION SPECIFIC ICS
DIGITAL PANEL INSTRUMENTS/POWER SUPPLIES
COMPONENT TEST SYSTEMS

LINEAR PRODUCTS DATABOOK 1990/91

ANALOG DEVICES

How to Find Product Data in This Databook

THIS VOLUME

Contains Data Sheets, Selection Guides and a wealth of background information on op amps and a wide variety of components for analog signal processing.

It is one member of a three-volume, 3,300-page set of Databooks describing and specifying Linear, Conversion and DSP products from Analog Devices, Inc., in IC, hybrid and assembled form for measurement, control and real-world signal processing.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Volume-Section-Page location of data sheets catalogued in any of the 3 volumes.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), add our "AD" prefix and look it up in the index.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your function in the list on the opposite page or in the Table of Contents on pages 1–5 through 1–10. Turn directly to the appropriate Section. You will find a functional Selection Guide at the beginning of the Section. The Selection Guides (and the "Orientation" that usually accompanies them) will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria.

IF YOU CAN'T FIND IT HERE . . . ASK!

If it's not a "linear" signal-conditioning product, it's probably in one of the two sister volumes, the *Data Conversion Products Databook* or the *DSP Products Databook*. If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or phoning (617)-329-4700, Extension 3392.

See Worldwide Service Directory on pages 21-10 and 21-11 at the back of this volume for our sales office phone numbers.

Contents of Other Databooks

DATA CONVERSION PRODUCTS DATABOOK

D/A Converters
A/D Converters
V/F & F/V Converters
Synchro & Resolver Converters
Sample/Track–Hold Amplifiers
CMOS Switches & Multiplexers
Voltage References
Data Acquisition Subsystems
Microcomputer I/O Boards
Application Specific ICs
Power Supplies
Component Test Systems

DSP PRODUCTS DATABOOK

DSP Processors
Microcoded Support Components
Floating-Point Components
Fixed-Point Components

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ANALOG DEVICES

LINEAR PRODUCTS DATABOOK
1990

Products in this book may be covered by one or more of the following patents. Additional patents are pending.

U.S.:
RE29,619, RE29,992, RE30,586, RE31,850, DES. 233,909, 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,268,759, 4,270,118, 4,286,225, 4,309,693, 4,313,083, 4,323,795, 4,338,591, 4,349,811, 4,363,024, 4,374,314, 4,383,222, 4,395,647, 4,399,345, 4,400,689, 4,400,690, 4,427,973, 4,439,724, 4,460,891, 4,475,103, 4,475,169, 4,476,538, 4,481,708, 4,484,149, 4,485,372, 4,491,825, 4,511,413, 4,521,764, 4,543,560, 4,543,561, 4,547,766, 4,547,961, 4,556,870, 4,558,242, 4,562,400, 4,565,000, 4,586,019, 4,586,155, 4,590,456, 4,596,976, 4,601,760, 4,604,532, 4,608,541, 4,622,512, 4,626,769, 4,639,683, 4,644,253, 4,646,056, 4,646,238, 4,678,936, 4,684,922, 4,685,200, 4,694,276, 4,697,151, 4,703,283, 4,707,682, 4,709,167, 4,717,883, 4,722,910, 4,742,331, 4,751,455, 4,752,900, 4,761,636, 4,769,564, 4,771,011, 4,774,685, 4,791,318, 4,791,551, 4,800,524, 4,804,960, 4,808,908, 4,811,296, 4,814,767, 4,833,345, 4,839,653, 4,855,585, 4,855,618, 4,855,684, 4,857,862, 4,859,944, 4,862,073, 4,864,454, 4,866,505, 4,878,770, 4,879,505, 4,884,075, 4,885,585, 4,891,533, 4,891,645, 4,899,152, 4,902,959, 4,904,921, 4,924,227, 4,926,178, 4,928,103, 4,929,909,

France:
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Japan:
1,092,928, 1,242,936, 1,242,965, 1,306,235, 1,337,318, 1,401,661, 1,412,991, 1,432,164

West Germany:
2,014 034, 25 40 451.7, 26 11 858.1

U.K.:
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Sweden:
7603320-8

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Introduction

Analog Devices designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SOIC, LCC, PLCC), and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. A quarter-century of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high performance mixed-signal ASICs.

MAJOR PROGRESS

Since publication of the selection guides in the *1988 Databook Series,* more than 120 significant new products have been introduced by Analog Devices; they run the gamut from brand new product categories and technologies to new standard products (with improvements in price, performance or design) to augmented second-source products. They are all classified and summarized in these volumes, along with existing products that are desirable for use in new designs.

Examples of outstanding new products to be found in this book include:

- the AD840–849 series of monolithic operational amplifiers combining high speed and precision—fabricated in Analog Devices' complementary bipolar process—and the wideband, low-distortion AD9617/9618 current-feedback op amps
- the AD546 low cost plastic-packaged electrometer op amp
- the AD705 op amp with minimal voltage and current drifts
- the AD640 monolithic high-accuracy wideband logarithmic-amplifier strip
- the AD598 monolithic error-insensitive LVDT signal conditioner
- the high speed, monolithic AD9696/9697 single and dual comparators—and the fast, high-precision AD790 comparator
- the monolithic AD1322 200 MHz pin drivers and AD1315 active load for ATE applications
- the monolithic AD9901 dead-zone-free precision phase discriminator
- the 6B Series of configurable, digitizing, "sensor-to-serial" isolated signal-conditioning modules.

Many more could have been included in this list.

THE 1990 LINEAR PRODUCTS DATABOOK

This volume provides complete technical data on Analog Devices "linear" products—designed to process, condition and otherwise operate on *analog signals* with *analog results* . One of a set of three volumes, it is accompanied by the *DSP Products Databook*, dedicated to products for high-performance digital signal-processing (i.e., *digital-to-digital*), and the *Conversion Products Databook*, which covers products involved in spanning the interface *between analog and digital.*

The product data in this book are intended primarily for the majority of users who are concerned with new designs. For this reason, those existing and available products that offer little if any unique advantage over newer products in future designs are included in the Index and data sheets are available from us separately—but they are not published in this book.

This book includes:

- comprehensive data sheets on more than 160 significant product families
- orientation material and selection guides for rapid product finding
- a representative list of available Analog Devices technical publications on real-world analog and digital signal-processing
- our Worldwide Sales Directory and
- the Product Index to all three volumes.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for precision measurement and control. Besides tutorial material and comprehensive data sheets, including a large number in our Databooks, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several free serial publications; for example, *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch*™ is a quarterly newsletter that brings its reader up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to Databook catalogs—and general short-form selection guides—we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 21-7 to 21-9 at the back of the book.

DSPatch is a trademark of Analog Devices, Inc.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Sales Directory, as of the publication date, appears on pages 21-10 and 21-11 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is the companywide Quality Improvement Process (QIP). In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 for ICs in the U.S. and Ireland and MIL-STD-1772 for hybrids. More than 14 of our products—both proprietary and second-source—have qualified for JAN part numbers; others are in the process. A larger number of products—including many of the newer ones just starting the JAN qualification process—are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts (the 1990 issue contains data on nearly 223 available product families). A newsletter, *Analog Briefings*®, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, these devices are suffixed "/+" and are available from stock.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in the Index, turn to page 21-4 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 21-5 you will find a guide to substitutions (where possible) for products no longer available.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

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Selection Guide
Operational Amplifiers

High Speed Amplifiers

Model	GBW MHz typ	SR V/μs typ	Settling Time ns to % typ	A_{CL} min V/V	V_{OS} mV typ	I_{OUT} mA min	Supply Current mA typ	Package Options[1]	Temp Range[2]	Page	Comments
AD5539	1400	600	12–1	+5, −4	2	11	25	N, Q	C, M	2-335	Improved Replacement for SE/NE5539
AD829	750	230	65–0.1	1	0.2	32 typ	5	N, Q, R	C, I, M	2-247	High Speed, Low Noise, Video Amp
AD844	900	2000	100–0.1	1	0.05	80	6.5	N, Q, R	I, M	2-287	Constant 10 ns Rise Time for Any Pulse Input, Current Feedback
AD849	725	300	80–0.1	25	0.3	32 typ	5.1	N, Q, R	C, I, M	2-327	High Speed, Low Power Preamp, Drives Capacitive Loads
AD846	450	450	110–0.01	1	0.025	65 typ	5	N, Q	I, M	2-307	High Speed, Precision, Current Feedback
AD840	400	400	100–0.01	10	0.1	50	10.5	N, Q	C, M	2-251	Wide Bandwidth Precision, Fast Settling, $A_{VCL} \geq 10$
AD9617	180	1600	10–0.1	3	0.4	60	34	N, Q, R	C, I, M	2-359	Low Distortion, Wide Bandwidth, IMD≤ −70 dBc at 20 MHz
AD848	175	300	100–0.1	5	0.2	32 typ	5.1	N, Q, R	C, I, M	2-327	High Speed, Low Power, Drives Capacitive Loads
AD9618	160	1800	10–0.1	+5, −1	0.2	60	31	N, Q, R	C, I, M	2-367	Low Distortion, Wideband, IMD ≤ −70 dBc at 20 MHz
AD9610	100	3500	18–0.1	1	0.3	50	21	H	I, M	2-351	Wide Bandwidth, Fast Settling
AD842	80	375	100–0.01	2	0.5	50	13	H, N, Q	C, M	2-267	Fast Settling, High Current Output, Cable Driver, $A_{VCL} \geq 2$
AD827	50	300	120–0.1	1	0.5	32 typ	10	N, Q, R	C, I, M	2-239	Dual AD847
AD847	50	300	120–0.1	1	0.5	32 typ	5.1	N, Q, R	C, I, M	2-319	High Speed, Low Power, Drives Capacitive Loads
AD841	40	300	110–0.01	1	0.5	50	11	E, H, N, Q	C, M	2-259	High Speed, Precision, Drives Capacitive Loads
AD843	34	250	135–0.01	1	0.5	50	12	N, Q, H	C, I, M	2-275	FET Input, Fast Settling, High Speed
AD845	16	100	350–0.01	1	0.7	50 typ	10	N, Q	C, I, M	2-299	FET Input, Fast Settling, High Speed
AD744	13	75	500–0.01	+2, −1	0.3	25	3.5	H, N, Q, R	C, I, M	2-219	FET Input, Fast Settling, High Speed, Custom Compensation
AD746	13	75	500–0.01	+2, −1	0.3	25	3.5	H, N, Q, R	C, I, M	2-231	Dual AD744
AD713	4	20	1000–0.01	1	0.3	25 typ	10	H, N, Q	C, I, M	2-191	Quad AD711
AD711	3	16	1000–0.01	1	0.3	25 typ	2.5	H, N, Q, R	C, I, M	2-167	Precision BiFET
AD712	3	16	1000–0.01	1	0.3	25 typ	5	H, N, Q, R	C, I, M	2-179	Dual AD711

[1]Package Options: E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Selection Guide
Operational Amplifiers

Precision Amplifiers

Model	V_{OS} μV max	V_{OS} TC μV/°C max	Noise μV p-p 0.1–10 Hz typ	GBW MHz typ	Slew Rate V/μs typ	I_B nA max	CMRR dB f = 1 kHz typ	Package Options[1]	Temp Range[2]	Page	Comments
AD707	**5–100**	**0.03–0.3**	**0.23**	**0.9**	**0.3**	**0.5–2.5**	**140**	**H, N, Q, R**	**C, I, M**	**2–151**	**Highest DC Precision**
AD708	**5–90**	**0.03–0.3**	**0.23**	**0.9**	**0.3**	**0.5–2.5**	**140**	**H, N, Q, R**	**C, I, M**	**2–159**	**Dual AD707**
AD844	**50–300**	**1–5**	**—**	**60**	**2000**	**450**	**—**	**N, Q**	**I, M**	**2–287**	**Precision, High Speed**
AD846	**25–200**	**0.8–5.5**	**—**	**75**	**450**	**450**	**—**	**N, Q**	**I, M**	**2–307**	**High Precision, High Speed**
AD OP-07	**25–100**	**0.6–2.5**	**0.35**	**0.6**	**0.17**	**2–12**	**95**	**H, N, Q, R**	**C, M**	**2–383**	**Improved Industry Standard**
AD OP-27	**25–100**	**0.6–1.8**	**0.08**	**8**	**2.8**	**40–80**	**123**	**H, N, Q**	**I, M**	**2–389**	**Ultralow Noise**
AD OP-37	**25–100**	**0.6–1.8**	**0.08**	**63 (GBP)**	**17**	**40–80**	**123**	**H, N, Q**	**I, M**	**2–397**	**Combines Precision and Speed**
AD705	**25–90**	**0.6–2.0**	**0.5**	**0.8**	**0.15**	**0.1–0.15**	**110**	**N, Q, R**	**C, I, M**	**2–135**	**Low I_B Precision Bipolar**
AD704	**50–100**	**0.6–1.5**	**0.5**	**0.8**	**0.15**	**0.15–0.25**	**110**	**N, Q, R**	**C, I, M**	**2–131**	**Quad AD705**
AD706	**50–100**	**1.0–1.5**	**0.5**	**0.8**	**0.15**	**0.15–0.25**	**110**	**N, Q, R**	**C, I, M**	**2–143**	**Dual AD705**
AD517	50–100	1.3–3	2	0.25	0.1	0.25–2	94	H	C, M	2–45	
AD547	250–1000	1–5	2	1	3	0.025–0.05	60	H	C, M	2–51	Low Drift BiFET
AD647	250–1000	2.5–10	4	1	3	0.035	76	E, H	C, M	2–115	Dual AD547
AD548	**250–2000**	**2–20**	**2**	**1**	**1.8**	**0.03–0.015**	**83**	**H, N, Q, R**	**C, I, M**	**2–75**	**Low Power BiFET**
AD648	**100–2000**	**3–20**	**2**	**1**	**1.8**	**0.03–0.015**	**83**	**H, N, Q, R**	**C, I, M**	**2–121**	**Dual AD548**

Low Noise Amplifiers

Model	Voltage Noise en typ 10 kHz nV√Hz	Voltage Noise en typ 1 kHz nV√Hz	Current Noise In ± In− typ 1 kHz pA√Hz	I_B typ nA	V_{OS} mV typ	GBW MHz typ	SR V/μs typ	Settling Time ns to % typ	A_{CL} min V/V	Package Options[1]	Temp Range[2]	Page	Comments
AD9617	**1.3**	**2.0**	**45/45**	**12000**	**0.5**	**190**	**1600**	**10–0.1**	**±1**	**N, Q, R**	**C, I, M**	**2–359**	**Low Distortion, Wide Bandwidth**
AD9618	**1.3**	**2.0**	**45/45**	**10000**	**0.5**	**160**	**1800**	**9–0.1**	**+5, −1**	**N, Q, R**	**C, I, M**	**2–367**	**Low Distortion, Wide Bandwidth**
AD844	**—**	**2**	**12/10**	**200**	**0.05**	**900**	**2000**	**100–0.1**	**1**	**N, Q**	**I, M**	**2–287**	**Current Feedback Amplifier**
AD846	**—**	**2**	**6/20**	**100**	**0.025**	**450**	**450**	**110–0.01**	**1**	**N, Q**	**I, M**	**2–307**	**Current Feedback, Precision**
AD849	**—**	**3**	**—**	**3300**	**0.3**	**725**	**300**	**80–0.1**	**25**	**N, Q, R**	**C, I, M**	**2–327**	**High Speed, Low Power**
AD OP-27	**0.35**	**3**	**0.4/0.4**	**10**	**0.025**	**8**	**1.7**	**—**	**1**	**H, N, Q**	**I, M**	**2–389**	**Low Noise, Precision**
AD OP-37	**0.08**	**3**	**0.4/0.4**	**10**	**0.025**	**63**	**17**	**—**	**5**	**H, N, Q**	**I, M**	**2–397**	**Low Noise, Precision**
AD743	**2.9**	**3.2**	**0.007**	**0.15**	**0.1**	**4.5**	**2.8**	**—**	**1**	**N, Q, R**	**C, I, M**	**2–207**	**Ultralow Noise FET Input**
AD829	**—**	**2**	**1.5**	**3300**	**0.2**	**750**	**230**	**65–0.1**	**1**	**N, Q, R**	**C, I, M**	**2–247**	**High Speed, Low Noise, Video Amp**
AD5539	**—**	**4**	**—**	**6000**	**2**	**1400**	**600**	**12–1**	**+5,−4**	**N, Q**	**C, M**	**2–335**	**Improved Replacement for NE5539**
AD840	**—**	**4**	**—**	**3500**	**0.1**	**400**	**400**	**100–0.01**	**10**	**N, Q**	**C, M**	**2–251**	**Wide Bandwidth, Precision**
AD848	**—**	**5**	**—**	**3300**	**0.2**	**175**	**300**	**100–0.1**	**5**	**N, Q, R**	**C, I, M**	**2–327**	**High Speed, Low Power**
AD645	**8**	**9**	**0.6/0.6**	**0.0007**	**0.1**	**2**	**2**	**—**	**1**	**H, N**	**C, I, M**	**2–107**	**FET Input, Low I_B**
AD9611	1.1	1.6	38/38	1000	0.5	280	1900	13–0.01	1	H	I, M	21–4	Ultrafast Settling, Wide Bandwidth
AD9610	**0.7**	**1.6**	**32/32**	**5000**	**0.3**	**100**	**3500**	**18—0.1**	**1**	**H**	**I, M**	**2–351**	**Wide Bandwidth, Fast Settling**

Low Cost, General Purpose Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[3]	SR V/µs typ	Settling Time µs 0.01% typ	Noise µV p–p 0.1–10 Hz typ	Package Options[1]	Temp Range[2]	Page	Comments
AD707	**0.015–0.09**	**0.1–1**	**1–2.5**	**0.9**	**0.15**	**—**	**0.23**	**H, N, Q, R**	**C, I, M**	**2–151**	**Very High DC Precision**
AD705	**0.025–0.09**	**0.6–2.0**	**0.1–0.15**	**0.8**	**0.15**	**—**	**0.5**	**N, Q, R**	**C, I, M**	**2–135**	**Low I_B Precision Bipolar**
AD704	**0.05–0.10**	**0.6–1.5**	**0.15–0.25**	**0.8**	**0.15**	**8**	**0.5**	**N, Q, R**	**C, I, M**	**2–131**	**Quad AD705**
AD706	**0.05–0.10**	**1.0–1.5**	**0.15–0.25**	**0.8**	**0.15**	**8**	**0.5**	**N, Q, R**	**C, I, M**	**2–143**	**Dual AD705**
AD OP–07	**0.025–0.15**	**0.6–2.5**	**3–12**	**0.6**	**0.17**	**—**	**0.35–0.38**	**H, N, Q, R**	**C, M**	**2–383**	**Improved Industry Standard**
AD711	**0.025–2**	**3–20**	**0.025–0.05**	**4**	**20**	**1**	**2**	**H, N, Q, R**	**C, I, M**	**2–167**	**Excellent Combination of AC and DC Performance at Very Competitive Prices**
AD548	**0.25–2**	**2–20**	**0.01–0.02**	**1**	**1.8**	**8**	**2**	**H, N, Q, R**	**C, I, M**	**2–75**	**Low Power, High Performance**
AD542	0.5–2	5–20	0.025–0.05	1	3	—	2	H	C, M	2–51	High Performance BiFET
AD544	0.5–2	5–20	0.025–0.05	2	13	—	2	H	C, M	2–51	High Performance BiFET
AD741	3–6	20	200–500	1	0.5	—	—	H, N	C, I, M	2–203	Improved Second Source

Low Input Current Amplifiers

Model	I_B pA max	Input Impedance Differential Ω‖pF typ	Input Impedance Common Mode Ω‖pF typ	CMRR dB f=1 kHz typ	V_{OS} mV max	V_{OS} TC µV/°C max	BW MHz typ[3]	Package Options[1]	Temp Range[2]	Page	Comments
AD549	**0.06–0.25**	**10^{13}‖1**	**10^{15}‖0.8**	**62**	**0.25–1**	**5–20**	**1**	**H**	**C, M**	**2–83**	**Monolithic, Lowest I_B**
AD515A	0.075–0.3	10^{13}‖1.6	10^{15}‖0.8	62	1–3	15–50	1	H	C	2–39	Lower Cost AD515 Replacement
AD546	**0.5–1**	**10^{13}‖1**	**10^{15}‖0.8**	**62**	**1–2**	**20**	**1**	**N**	**C**	**2–63**	**Precision Low Cost Electrometer**
AD645	**1.5–3**	**10^{13}‖1**	**10^{14}‖3**	**94**	**0.25–0.5**	**5–10**	**2**	**H, N**	**C, I, M**	**2–107**	**Low Noise, Precision BIFET**
AD545A	1–2	10^{13}‖1.6	10^{15}‖0.8	62	0.25–1	3–25	1	H	C	2–59	Lower Cost AD545 Replacement
AD548	**10–20**	**10^{12}‖3**	**3×10^{12}‖3**	**84**	**0.25–2**	**2–20**	**1**	**H, N, Q, R**	**C, I, M**	**2–75**	**Low Power, Low Cost**
AD547	25–50	10^{12}‖6	10^{12}‖13	60	0.25–1	1–5	1	H	C, M	2–51	Low Drift
AD711	**25–50**	**3×10^{12}‖5.5**	**3×10^{12}‖5.5**	**62**	**0.25–2**	**3–20**	**4**	**H, N, Q, R**	**C, I, M**	**2–167**	**Low Cost BiFET, Excellent AC and DC Performance**

[1]Package Options: E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
[3]Unity gain small signal bandwidth.
Boldface Type: Product recommended for new design.

Selection Guide
Operational Amplifiers

Dual Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time to 0.01% µs typ	Package Options[2]	Temp Range[3]	Page	Comments
AD708	**0.03–0.1**	**0.3–1.0**	**1–2.5**	**0.9**	**0.3**		**H, N, Q**	**C, I, M**	**2–159**	**Highest DC Precision; Excellent Matching Between Amps, Dual AD707**
AD706	**0.05–0.10**	**1.0–1.5**	**0.15–0.25**	**0.8**	**0.15**	**—**	**N, Q, R**	**C, I, M**	**2–143**	**Dual AD705, Low I_B Precision Bipolar**
AD712	**0.3–3**	**5–20**	**0.05–0.075**	**4**	**20**	**1**	**H, N, Q, R**	**C, I, M**	**2–179**	**Excellent AC and DC Performance, Dual AD711**
AD746	**0.25–1**	**3–20**	**0.15**	**13**	**75**	**0.5**	**H, N, Q**	**C, I, M**	**2–231**	**Precision, Fast Settling, Dual AD744**
AD647	0.25–1	2.5–10	0.035–0.075	1	3		E, H	C, M	2–115	Dual AD547
AD648	**0.3–2**	**3–20**	**0.01–0.02**	**1**	**1.8**	**8**	**H, N, Q**	**C, I, M**	**2–121**	**Low Power, BiFET, Dual AD548**
AD642	0.5–2		0.035–0.075	1	3		H	C, M	2–95	Dual AD542
AD644	0.5–2		0.035–0.075	2	13		H	C, M	2–101	Dual AD544
AD827	**2.0–4.0**	**15**	**—**	**50**	**300**	**0.065–0.1**	**N, Q, R**	**C, I, M**	**2–239**	**Dual AD847, High Speed, Low Power**

Quad Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B pA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time to 0.01% µs typ	Package Options[2]	Temp Ranges[3]	Page	Comments
AD704	**0.05–0.10**	**0.6–1.5**	**150–250**	**0.8**	**0.15**	**—**	**N, Q, R**	**C, I, M**	**2–131**	**Quad AD705, Low I_B Precision Bipolar**
AD713	**0.5–1.5**	**20**	**75–150**	**4**	**20**	**1**	**N, Q**	**C, I, M**	**2–191**	**Superior AC and DC Performance, Quad AD711**

Unity Gain Buffers

Model	−3 dB BW MHz typ	SR V/µS min	I_{OUT} mA min	V_{OS} mV typ	I_{SS} mA max	Package Options[2]	Temp Range[3]	Page	Comments
AD9630	**700**	**1800**	**50**	**2**	**22**	**N, R, Q, Z**	**I, M**	**2–377**	**High Performance, Wide-Band Buffer**
AD9620	**600**	**2300**	**50**	**2**	**40**	**D**	**I, M**	**2–375**	**High Performance, Low Harmonic Distortion Buffer**

[1]Unity gain small signal bandwidth.
[2]Package Options: D–Side-Brazed Dual-In Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; Q–Cerdip; R–Small Outline Plastic (SOIC); Z–Leaded Chip Carrier (Gull Wing).
[3]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
Operational Amplifiers

The amplifiers listed in this volume are intended to provide cost-effective solutions to the bulk of op amp requirements in precision measurement and control, as well as to more general requirements in electronic circuits. The technical data included here* cover the properties of more than 40 op amp families, comprising about 100 distinct types. Some are general purpose; others provide near optimum performance for specific classes of application.

They differ in a variety of ways, for example, circuit technology, circuit architecture, package type and contents, input properties, output properties, operating temperature range and in terms of the many performance specifications. Most are monolithic ICs, including precision and high-speed dual devices; some are hybrid ICs.

The IC and hybrid amplifiers catalogued in this volume are available in a broad choice of packaging styles, temperature ranges, and performance grades. If your application calls for versions of these products that have been processed in accordance with MIL-STD-883, a wealth of relevant information can be found in the latest edition of the *Military Products Databook*, available free upon request from Analog Devices.

BACKGROUND

The operational amplifier is today the most widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control) and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 2-17 a bibliography that should make available up to 99% of information needed now and then, with "fanout" to the vast body of literature that – with some redundancy – will provide the remainder. Analog Devices' op amp data sheets are an excellent source of pertinent information.

SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To make a proper choice of an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.*
   Signal levels, closed-loop gain, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.
2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.*
   Two manufacturers may have comparable published specifications, but they may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured and then must be able to translate these published specifications in terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishing the circuit architecture, (2) defining the performance levels and (3) choosing the amplifier(s).

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks" and linear circuit books as well as in application notes and data sheets.
2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps and establish acceptable ranges of parameters and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high frequency performance and transient behavior of the op amp block (and its effect on the closed-loop circuit) for large and small signals. It will be helpful to develop an application checklist which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy – static and dynamic – and the environmental conditions.
3. The designer must then relate acceptable performance of the op amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows this discussion.

***In addition to the products listed here, which are recommended for new designs, a number of older products are still available (see page 21-4); data sheets are available upon request.**

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier. For example, an adjustable-gain wideband application may call for a *transimpedance* op amp to keep bandwidth independent of gain setting.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, dc offset and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical and environmenal requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the dc discussion below. The reader is then returned to an expanded discussion of gain bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

1. If dc information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and/or output and all of the "drift" specifications may usually be ignored, and
2. Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where dc information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain bandwidth of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open-loop gain over closed-loop gain, and is responsible for the diminishing error due to fluctuations in the open-loop gain due to time, temperature, etc. For example, if the closed-loop gain is 1,000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

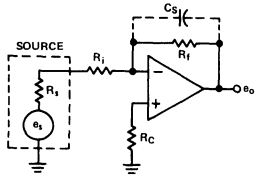
Most operational amplifiers are voltage-to-voltage amplifiers. However, for wide bandwidth applications, it is often useful to consider applying a class of current-to-voltage amplifiers called *current feedback (transimpedance) amplifiers*. They are characterized by *transresistance* ($\Delta V_o/\Delta I_i$) instead of gain ($\Delta V_o/\Delta V_i$). Unlike voltage amplifiers, with their high input impedance, current feedback amplifiers have *low* (ideally zero) input impedance in order to minimize the gain-error voltage developed by their input current. Such amplifiers tend to be characterized by high slewing rates and high closed-loop bandwidth. In contrast to the *constant gain* × *bandwidth* of most voltage amplifiers, the closed-loop bandwidth of a current feedback amplifier is essentially independent of closed-loop gain – as long as the feedback resistance is kept constant when the gain is adjusted.

Offset and Drift Considerations

In the majority of op amp applications, final selection is determined by the dc offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_s, and the amount of loading error which is acceptable. Most amplifier circuits are designed around the inverting and noninverting circuits of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i, and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback), and in this case input impedance is approximately equal to the common-mode impedance of the amplifier R_{CM}.
2. *How much drift error can be tolerated?* The question is related to the input signal level, e_s, and the required accuracy. For example, to amplify or otherwise manipulate a dc input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

   When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b) and difference current can be calculated by the equations of Figure 1.



$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i\right]$$

Signal Input Drift Error = V_d

For $R_C = 0$ and $R_s \ll R_i$

$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\frac{R_f + R_i}{R_f} + i_d R_i\right]$$

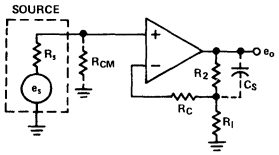
Signal Input Drift Error = V_d

For $R_C = R_i R_f/(R_i + R_f)$ and $R_s \ll R_i$

Input Impedance $R_{IN} \approx R_i$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1a. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_b R_s\right] \text{ for } R_C = 0$$

Signal Drift Error = V_d

$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_d R_s\right] \text{ for } R_C = R_s - \frac{R_i R_2}{R_i + R_2}$$

Signal Drift Error = V_d

Input Impedance $R_{IN} \approx R_{CM}$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1b. Noninverting Configuration

For example, in the case of the inverting circuit, an offset error voltage, i_bR_i, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.

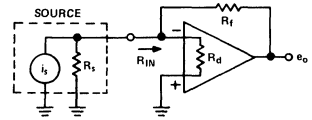
Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input impedance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications where common-mode errors may rule out this circuit configuration. Transimpedance amplifiers in the noninverting configuration have high dynamic input impedance, but they must be driven from a source that can furnish the input current. This rules out the possibility of unloading some high impedance sources but still permits a single amplifier to be used for noninverting gains (as always, it is helpful to consult the data sheet).

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from $+25°C$ need be considered. For example, over the range of $-25°C$ to $+85°C$, the maximum temperature excursion (ΔT) from $+25°C$ would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2a. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2b.



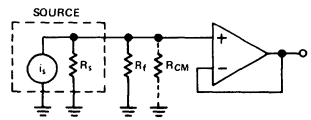
$$e_o = -R_f\left[i_s + e_{os}\left(\frac{R_f + R_s}{R_s R_f}\right) + i_b\right]$$

Signal Drift error = $I\epsilon$

$$\text{Input Impedance } R_{IN} = \left(\frac{R_f R_d}{R_f + R_d}\right)\left(\frac{1}{1 + A\beta}\right)$$

$$\text{where } 1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s \quad R_d} \qquad \% \text{ Drift Error} = \frac{100\, I\epsilon}{i_s}$$

Figure 2a. Current Amplifier



$$e_o = R_f i_s + e_{os} + i_b R_f \text{ for } R_s > R_f$$

Signal Drift Error = V_d

Input Impedance $R_{IN} \approx R_f$

$$\% \text{ Drift Error} = \frac{100V_o}{R_f i_s}$$

Figure 2b. Voltage Amplifier with Sampling Resistor

This approach has several disadvantages as compared to the circuit of Figure 2a. First, the noninverting amplifier introduces common-mode errors which do not occur for Figure 2a. Second, an ideal current meter would have zero impedance whereas R_f in Figure 2b may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm}, for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

The current amplifier of Figure 2a circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open-loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_ϵ referred to the input, use the following expression.

$$\Delta I_\epsilon = \left[\frac{\Delta e_{os}}{\Delta T}\left(\frac{R_f + R_s}{R_f R_s}\right) + \frac{\Delta i_B}{\Delta T}\right]\Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_ϵ, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for dc and audio-frequency-range applications. However, amplifiers having unity-gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μs, in general, require special design techniques. Amplifiers with wideband, fast response characteristics have been listed in the Wide Bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1a, if R_f were one megohm, and stray capacitance, C_S, were one picofarad, then the closed-loop bandwidth would be limited to 160kHz ($1/(2\pi R_F C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged, which in turn is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_iC_S$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1b) is that input impedance, being determined by potentiometric feedback, is independent of the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_S will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common-mode rejection error (with frequency) introduced by the noninverter.

For greater emphasis, wideband applications can be separated into categories – steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

STEADY STATE APPLICATIONS

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is dc coupling required?* If dc information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output dc offset. Your only concern here is that dc offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for ac signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at dc as shown in Figure 3. The gain of this kind of circuit can be small at dc but large at high frequencies.

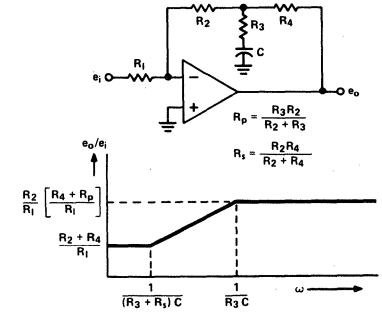


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. *What closed-loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. For V/V amplifiers, to a first approximation the intersection of the open- and closed-loop gain curves in Figure 4 gives the closed loop bandwidth, f_{c1} (−3dB). For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade each at lower gain. For transimpedance amplifiers, f_{c1} changes little over a wide range of gain as set by the choice of R_1.
3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed-loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open- to closed-loop gain ($A\beta = A/G$). You will find in most of the equations defining the closed-loop characteristic of a feedback (V/V) amplifier that the loop gain ($A\beta$) is the

determining factor in performance. Some of the more notable examples of this point are as follows:

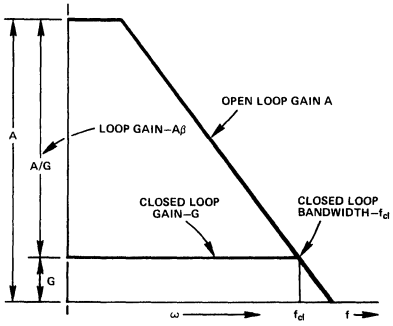


Figure 4. Closed-Loop Bandwidth and Loop Gain

a. Closed-loop gain stability $= \Delta G/G$
$\Delta G/G = (\Delta A/A)\ [1/(1+A\beta)]$ where $\Delta A/A$ is the open-loop gain stability, usually about 1%/°C.

b. Closed-loop output impedance $= Z_{ocl} = Z_o/(1+A\beta)$, where Z_o is the open-loop output impedance, usually 200 to 5,000 ohms.

c. Closed-loop nonlinearity $= L_{cl} = L_{ol}/(1+A\beta)$, where L_{ol} is the open-loop linearity error, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications, and this is readily achievable at dc and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?*
You should examine your expected output waveform and select an amplifier whose slewing rate, with the expected capacitive output load, exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions, you will get distortion and unexpected dc offsets at the output of the amplifier.

For some monolithic amplifier designs intended for high-gain and wide-bandwidth applications, their frequency response is not a simple 6dB roll-off; the response may be shaped with external RC components for improved performance at lower closed-loop gains. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated V/V op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

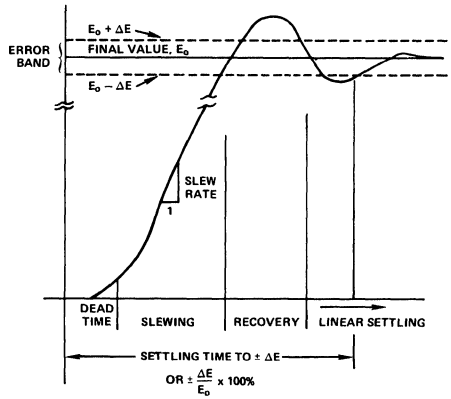


Figure 5. Typical Settling Time Characteristics

TRANSIENT APPLICATIONS

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

The time and frequency response of a linear, bilateral network or amplifier are related by well know mathematics. For example, the step response for a well behaved, ideally linear, 6dB/octave amplifier with a closed-loop bandwidth of ω_{cl} is shown in Figure 6.

However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed-loop parameter, it cannot be readily predicted from the open-loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels and no capacitive loading (unless otherwise indicated). A full-scale step input is used to determine settling time and the step is generally unipolar – i.e., from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full-scale step transition.

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

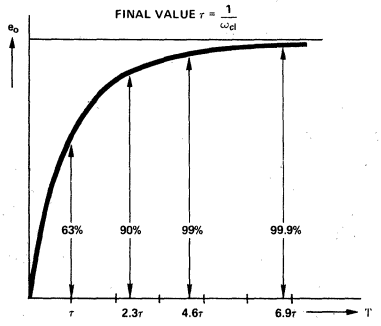


Figure 6. Step Response for Linear 6dB/Octave Amplifier

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF and digital noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will greatly reduce noise pickup.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise," is generated in the resistive component of any impedance and has a value:

$$e_n = \sqrt{4kTBR}$$

where e_n = the rms value of the noise voltage
k = Boltzman's Constant (1.38×10^{23} joules/K)
T = absolute temperature of the resistance, K
B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the thermal noise equation may appear unwieldy, for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

1. Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n\ (\text{rms}) = (40\text{nV}/\sqrt{\text{Hz}}) \left(\sqrt{\frac{R}{100\text{k}\Omega}\ (\text{BW})} \right)$$

2. To convert the rms noise to a p-p value, a conversion factor of 6.6μV p-p/μV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.
3. The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

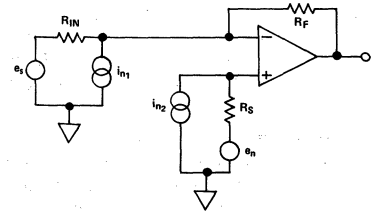
$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots e_n^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be less than 5%.

4. Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 7a illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a rms fashion.

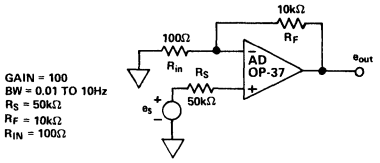


COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4kTBR_{IN}}\ (R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4kTBR_S}\ (R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4kTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\ (R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\ (R_F/R_{IN}+1)$

TOTAL NOISE = $\sqrt{(e_{R_{IN}} G)^2 + [e_{R_S}(G+1)]^2 + e^2_{R_F} + [(i_{n_1} R_F)^2] + [(i_{n_2} R_S)(G+1)]^2 + [e_n (G+1)]^2}$

Figure 7a. Noise Components

Figure 7b illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, a low noise type amplifier (AD OP-37) is being used with a 50kΩ source impedance. The two major noise sources, in addition to the AD OP-37's input voltage noise of 0.18μV p-p, are the Johnson noise (59μV p-p) and current noise (83pA p-p).



1) RESISTOR NOISE: $R_F \rightarrow 13nV/\sqrt{Hz}$
$R_{IN} \rightarrow (1.3nV/\sqrt{Hz}$
$R_S \rightarrow (28nV/\sqrt{Hz})\ 101 = 2.8\mu V/\sqrt{Hz}$
TOTAL RESISTOR NOISE IN 10Hz BW =
$(2.8\mu V/\sqrt{Hz})\ (\sqrt{10Hz})\ 6.6\mu V$ p-p/μV rms = $59\mu V$ p-p

2) AMPLIFIER CURRENT NOISE: (83pA p-p)(50k)(101) = $422\mu V$ (R_S)
(83pA p-p)(10k) = $0.8\mu V$ (R_F)

3) AMPLIFIER VOLTAGE NOISE: (0.18V p-p)(101) = $18.2\mu V$ p-p

TOTAL OUTPUT NOISE = $\sqrt{(422)^2 + (59)^2 + (18.2)^2 + (0.18)^2}$ = $426\mu V$ p-p

Figure 7b. Design Example

HOW THE OPERATIONAL AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the many types available from Analog Devices, we have provided a Selection Guide in which amplifiers are grouped in terms of common properties which have been optimized in order to satisfy the needs of specific classes of applications. Once the choice has been narrowed to the manageable number of types in any group, distinctions can be drawn in terms of other requirements or considerations.

Temperature Range and Nomenclature: Analog Devices operational-amplifier nomenclature uses suffixes to permit ready identification of the temperature range for which device operation to meet critical specifications has been designed or selected. The most popular range comprises the "commercial" temperatures from 0 to 70°C; it is designated by suffixes such as J, K, L, M, in order of increasingly tighter specs (e.g., AD549L). Also popular is the "extended" range, −55°C to +125°C, designated by S, T, U, (e.g., AD510S); not all families have types with specified performance in this range. There are a few types designed for operation in the "industrial" range, −25°C to +85°C, designated by A, B. Wide-range types will generally meet the same or better specs in a narrower temperature range. A few types are second-sources for products originally introduced by other manufacturers. In those instances, the generic nomenclature is used (AD741C) or enlarged upon, if superior selections are offered (e.g., AD741L).

SELECTION GUIDES

Seven Selection Guides classify operational amplifiers within these categories:

High Speed Amplifiers
Unity Gain Buffers
Precision Amplifiers (low V_{OS}, low drift, high dc gain)
Low Input-Current Amplifiers
Low Noise Amplifiers
Low Cost, General Purpose Op Amps
Dual Op Amps
Quad Op Amps

The choice of category depends on which class of specifications is most critical. Within these categories, the selection guides provide comparisons of salient specifications.

These selection areas are pretty broad; they include various criteria, not all of which are central to the application. For example, if one is seeking a high-input-impedance amplifier for an ac application, voltage offset and drift may be far less critical than bias current, and both of these may be unimportant compared to bandwidth.

With the hope that it will be found useful, the following interpretive list identifies the best device choices in a variety of categories:

(At the extremes of performance are the *fastest* op amps and the *highest-precision* op amps.)

The *fastest* op amps include those having

- the highest *slewing rates*, – the hybrid AD9610 (3,500V/μs), and the monolithic AD844 (2,000V/μs) and AD9618 (1,800V/μs)
- the lowest *settling time* – the monolithic CB (complementary bipolar) AD840/841/842/846 (110ns to ±0.01%), the hybrid AD9610 (20ns to 0.1%) and the AD9618 (9ns to 0.1%)
- the highest *gain-bandwidth* – the AD5539 (1,400MHz) and the CB AD844 (900MHz), AD849 (725MHz) and AD840 (400MHz)

High-speed op amps are characterized by high slewing rates, fast settling time and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data in buffers, D/A converters, and multiplexer circuits; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimum distortion since the large-signal bandwidth is closely related to the slewing rate.

ICs using the proprietary Analog Devices CB (complementary bipolar) process contain wideband PNP and NPN transistors that have similar characteristics – without the use of dielectric isolation. Since poor frequency response of lateral PNPs is the source of the bandwidth limitation in conventional linear bipolar processes, CB devices can have much faster response.

The *highest-precision* monolithic op amp families include those having

- the grades with the lowest *untrimmed offset voltage*– the AD707 (15μV) and AD OP-07/27/37 (25μV)
- the lowest *bias current* – the revolutionary *electrometer* op amp using top-gate-FET inputs, the AD549 (60 femtoamperes)
- the *lowest drift* – the AD707 (100nV/°C)
- the *highest open-loop gain* (hence highest accuracy as an integrator and high-gain amplifier) – again the AD707! (13×10^6V/V)
- the highest *common-mode rejection* – once again the AD707 (130dB), followed by the AD OP-27/37 (114dB) and the AD OP-07 (110dB)

Precision op amps (in this list) include those emphasizing

- *Low bias current and high input impedance.* These types use the inherently high input impedance and low leakage current of junction field-effect transistors (FETs) to deal with configurations that measure low currents or involve high resistance values. Applications range from general purpose high-impedance circuitry to integrators, current-to-voltage converters, and log-function generation, to

measurements with high-impedance transducers such as photomultipliers, flame detectors, pH cells and radiation detectors.

- *High accuracy* through low offset and drift voltage, low voltage noise, high open-loop gain, and high common-mode rejection (CMR). Such types are used for high-accuracy instrumentation, low-level transducer circuitry, precision voltage comparison, and impedance buffering.

  All FET-input op amps from Analog Devices are conservatively manufactured to meet their published bias-current specifications *after full warmup* (some manufacturers specify *initial* current, which is lower than warmed-up bias current). Our published max bias-current specification applies to *either* input (some manufacturers call "bias current" the *average* of the two input currents).

For applications needing high, but not extreme, performance or *where high speed and high precision must be combined*, there are a number of device families to be considered. For example,

- the complementary-bipolar AD844 family *combines low offset voltage* (200μV) *with high slewing rate* (2000V/μs)
- the AD744 BiFET family *combines low input bias current* (50pA) *with low settling time* (500ns to 0.01%)
- the AD OP-37 family *combines low drift* (600nV/°C) *with wide gain bandwidth* (63MHz)
- the hybrid AD381/382 combine 50pA bias current with 0.75μs settling time (to 0.1%) and 50mA output-current range

Fast amplifiers, which often boast output current ranges of 50mA or 100mA, include families with

- *high slewing rate* – the CB monolithic AD846 (400V/μs) and AD840/841/842 (400/300/375V/μs), and the hybrid, AD380 (330V/μs), and AD9617/9618 (1,400V/μs)
- *low settling time* – the monolithic AD847/848/849 (65ns to 0.1%) and hybrid HOS-050 (80ns to 0.1%, 200ns to 0.01%), the AD845 and AD744 families (300ns and 500ns to 0.01%), and the AD9617 (10ns to 0.1%) and AD9618 (9ns to 0.1%)
- *wide gain-bandwidth* – the monolithic AD848 (250MHz) and the hybrid AD9611 (280MHz) and HOS-050/060 (100MHz)

High-precision monolithic amplifier families start with lower grades of the highest-precision families; beyond this, they include the

- *low-drift* AD OP-07/27/37 families (600nV/°C)
- *high-gain* AD OP-07 (3×10^6) and AD OP-27/37 (1×10^6)
- *high-CMR* AD821 (90dB); low-V_{os} AD846 (200μV) and a
- wide selection of low bias-current FET-input op amps – the AD645 (2pA) and AD548 (10pA), and the AD711 (25pA)

Many of these devices are duplicated in a single package; for example,

- the AD712 is a dual AD711
- the AD746 is a dual AD744
- the AD648 is a dual AD548
- the AD708 is a dual AD707
- the AD713 is a *quad* version of the AD711

Also included in this section are *buffers*, wideband amplifiers having slightly less than unity gain, low output impedance and high output-current availability (50mA). Although they can stand alone, a more frequent use is inside-the-loop as a "booster" amplifier to magnify the output power capability of any op amp or reduce the dynamic output impedance without losing precision. A typical example is the AD9630, which can follow slewing rates of up to 1,800V/μs with a full-power frequency of 125MHz and deliver voltages up to ±3V and currents up to ±50mA.

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage

Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, under overload conditions or between applications, such as voltage comparators, the voltage between the inputs can be large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection

An ideal operational amplifier responds only to the difference voltage between inputs ($e^+ - e^-$) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is usually expressed logarithmically: CMR (in dB) = $20 \log_{10}$ (CMRR).

The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified but decrease and become less in the neighborhood of large CMV. Published CMR specifications for op amps pertain to low-frequency voltages, unless specified otherwise: CMR decreases with frequency.

Common-Mode Voltage, Maximum

For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connections.

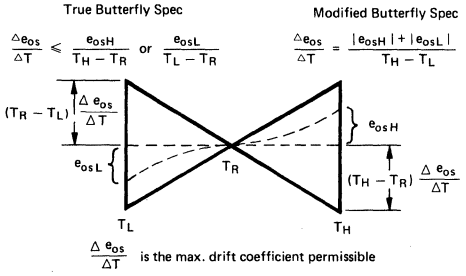
Drift vs. Supply

Offset voltage, bias current and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature

Offset voltage, bias current and difference current all change, or "drift," from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature range); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drift in the two ranges must be less than the specified drift rate (μV/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").



The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time

Offset voltage, bias current and difference current change with time as components age. It is important to realize that drift with time is random and rarely – if ever – accumulates linearly for healthy devices. For example, voltage drift might be quoted at 15μV/month, whereas cumulative drift might not exceed 50μV in a year. A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response

The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a predetermined distortion level. There is no industrywide accepted value for the distortion level which determines the full-linear-response limitation, but unless otherwise noted, we use 3% as a a maximum acceptable limit.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more serious effect (often overlooked) is an effect equivalent to dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often of interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current

Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average*.

Analog Devices specifies initial bias current, I_b, as the bias current at either input, specified at +25°C ambient with the input junctions *at normal operating temperature*. (Some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" specs used by some manufacturers may be met only during a brief interval after the power is burned on, and I_b may be quadrupled under ordinary operation conditions.)

Initial Difference Current

Difference current is defined as the difference between the bias currents at the two inputs. Uncompensated input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated internally at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal impedance loads at both inputs.

Input Impedance

Differential input impedance of voltage-input op amps is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry).

However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the noninverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage
Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise
Input voltage- and current-noise characteristics can be specified and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. When evaluating noise performance, bandwidth or period must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise," resistor noise or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some amplifiers types, spectral-density plots or "spot noise," at specific frequencies, in $\mu V/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain
Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response*.

For *transimpedance amplifiers*, since the input is a current and the output is a voltage, the "gain" is expressed in ohms ($R = V/I$). Because small changes in current cause large voltage changes, the transimpedance can be quite large – e.g., 100MΩ for the AD846. As long as the amplifier's internal input impedance is very low, errors in closed-loop circuitry depend principally on the ratio, R_F/R_T, relative to unity – where R_F is the feedback resistance and R_T is the transimpedance. It will be recalled that, in V/V op amps, the increase in error depends mainly on $R_F/(AR_I)$, where A is the open-loop gain and R_I is the resistance of the external input resistor. The significant difference is that, as gain or transresistance decreases with increasing frequency, the error in transimpedance-amplifier circuits is independent of R_I; hence closed-loop gain can be increased by reducing R_I without substantially affecting bandwidth.

Overload Recovery
Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output
Rated output *voltage* is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time
Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate limited overload (if it occurs) and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate
The slewing rate of an amplifier, usually in volts per microsecond (V/μs), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response
Unity-gain small-signal response is the frequency at which the open-loop gain (or its projection on a Bodé plot) falls to 1V/V, or 0dB under a specified compensation condition. For amplifiers having 6 dB-per-octave rolloff, this frequency is also called

unity-gain bandwidth; for such amplifiers, the *gain-bandwidth product* is essentially constant. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification.

For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and noninverting configurations. However, if feed-forward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

For amplifiers having 6 dB-per-octave rolloff, this frequency is also called *unity-gain bandwidth;* for such amplifiers, the *gain-bandwidth product* is essentially constant.

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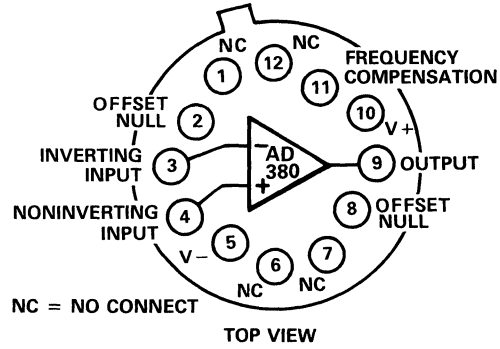
ANALOG DEVICES

Wideband, Fast-Settling FET-Input Op Amp

AD380

FEATURES
High Output Current: 50mA @ ±10V
Fast Settling to 0.1%: 130ns
High Slew Rate: 330V/μs
High Gain-Bandwidth Product: 300MHz
High Unity Gain Bandwidth: 40MHz
Low Offset Voltage (1mV for AD380K, L, S)

AD380 FUNCTIONAL BLOCK DIAGRAM



TOP VIEW

PRODUCT DESCRIPTION

The AD380 is a hybrid operational amplifier that combines the low input bias current advantages of a FET input stage with the high slew rate and line driving capability of a fast, high power output amplifier.

The AD380 has a slew rate of 330V/μs and will output ±10V at ±50mA. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate, or settling time for the given application.

A true differential input ensures equally superior performance in all system designs whether they are inverting, noninverting, or differential.

The AD380 is especially designed for use in applications, such as fast A/D, D/A and sampling circuits, that require fast and smooth settling and FET input parameters.

The AD380 is offered in three commercial versions, J, K and L specified from 0 to +70°C and one extended temperature version, the S, specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-8 style cans.

PRODUCT HIGHLIGHTS

1. The AD380's high output current (50mA @ ±10V) makes it suitable for driving terminated 200Ω twisted pairs.
2. The fast settling output (250ns to 0.01%) makes the AD380 an ideal choice for video A/D and D/A converters and sample and hold applications.
3. The settling wave forms are not only fast but are also very smooth. The absence of large overshoot and oscillations makes the AD380 a very predictable and dependable system element.
4. The high gain-bandwidth product (300MHz) ensures low distortion in high frequency applications.
5. Quick, symmetrical overdrive recovery time (250ns) is assured by an internal antisaturation diode. This is useful in applications where large transient signals may occur.
6. The precision input (1mV offset, max), along with fast settling and high current output make the AD380 an excellent choice for:
   - ATE pin drivers
   - precision coax buffers
   - signal conditioning on pulse waveforms
   - high resolution graphics displays.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD380JH	AD380KH	AD380LH	AD380SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, no load	40,000 min	*	*	*
V_{OUT} = ±10V, $R_L \geq 200\Omega$	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 200Ω, T_A = min to max	±12V (±10V min)	*	*	*
Output Impedance (Open Loop)	100Ω	*	*	*
Short Circuit Current	100mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	40MHz	*	*	*
Gain-Bandwidth Product, f = 100kHz, C_C = 1pF	300MHz (200MHz min)	*	*	*
Full Power Response	6MHz	*	*	*
Slew Rate, C_C = 1pF, 20V Swing	330V/μs (200V/μs min)	*	*	*
Settling Time: 10V Step to 1%	90ns	*	*	*
10V Step to 0.1%	130ns	*	*	*
10V Step to 0.01%	250ns	250ns (400ns max)	**	**
INPUT OFFSET VOLTAGE	2.0mV max	1.0mV max	**	**
vs. Temperature[1], T_A = min to max	50μV/°C max	20μV/°C max	10μV/°C max	50μV/°C max
vs. Supply	1mV/V max	*	*	*
INPUT BIAS CURRENT				
Either Input, Initial[2]	10pA (100pA max)	*	*	*
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{11}\Omega \| 6pF$	*	*	*
Common Mode	$10^{11}\Omega \| 6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[3]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	60dB min	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(6 to 20)V	*	*	*
Quiescent Current	12mA (15mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz to 100Hz	3.3μV p-p (0.5μV rms)	*	*	*
100Hz to 10kHz	6.6μV p-p (1μV rms)	*	*	*
10kHz to 1MHz	40μV p-p (6μV rms)	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance θ_{JA}	100°C/W	*	*	*
θ_{JC}	70°C/W	*	*	*
PACKAGE OPTION[4]				
TO-8 Style	H-12A	*	*	*

NOTES

[1]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of offset nulled.

[2]Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures see Figure 16.

[3]Defined as the maximum safe voltage between inputs such that neither exceeds ±10V from ground.

[4]See Section 20 for package outline information.

*Specifications same as AD380JH.

**Specifications same as AD380KH.

Specifications subject to change without notice.

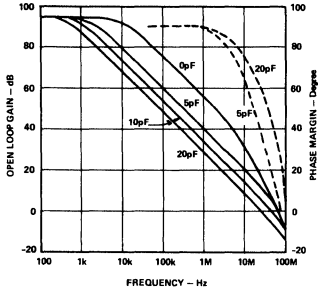


Figure 1. Open Loop Frequency Response

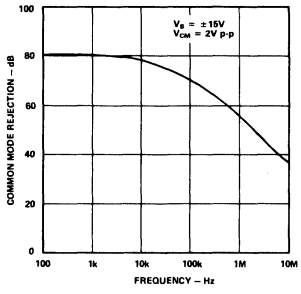


Figure 2. CMRR vs. Frequency

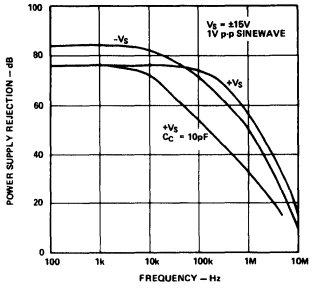


Figure 3. PSRR vs. Frequency

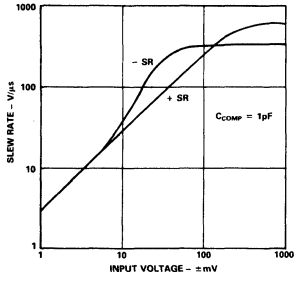


Figure 4. Slew Rate vs. Differential Input Voltage

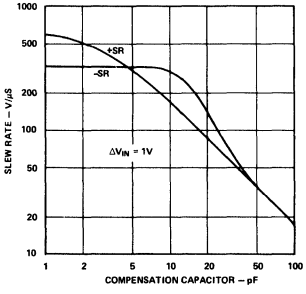


Figure 5. Slew Rate vs. Compensation Capacitor

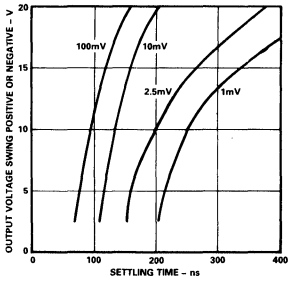


Figure 6. Output Settling Time vs. Output Voltage Swing and Error

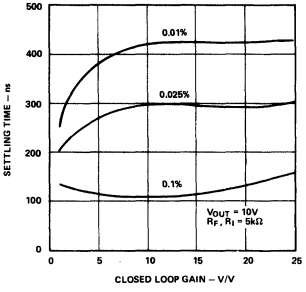


Figure 7. Settling Time vs. Closed Loop Gain

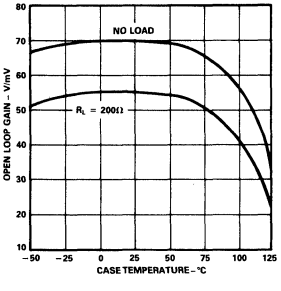


Figure 8. Gain vs. Temperature

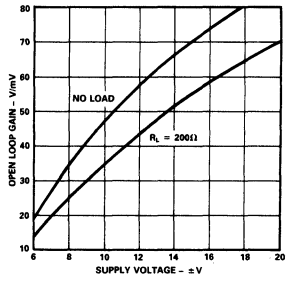


Figure 9. Gain vs. Supply Voltage

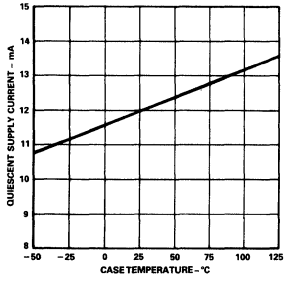


Figure 10. Supply Current vs. Temperature

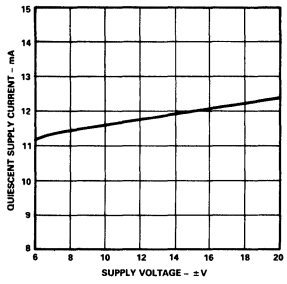


Figure 11. Supply Current vs. Supply Voltage

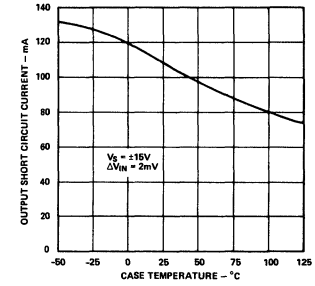


Figure 12. I_{SC} vs. Temperature

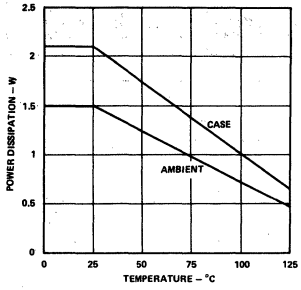


Figure 13. Power Dissipation vs. Temperature

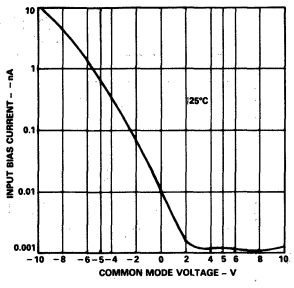


Figure 14. Input Bias Current vs. Common Mode Voltage

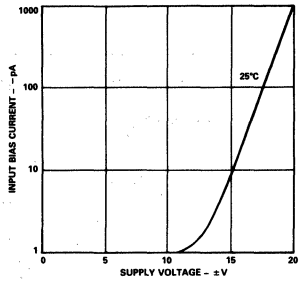


Figure 15. Input Bias Current vs. Supply Voltage

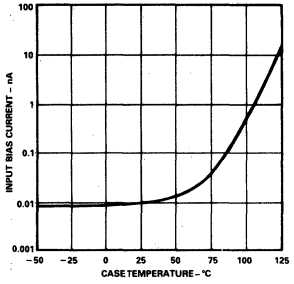


Figure 16. Input Bias Current vs. Temperature

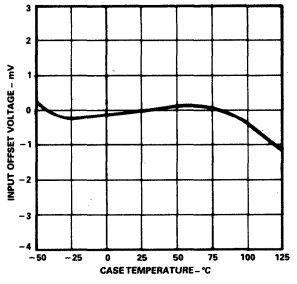


Figure 17. Offset Voltage vs. Temperature

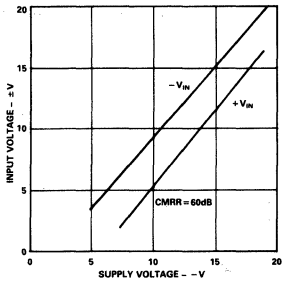


Figure 18. Input Voltage Range vs. Supply Voltage

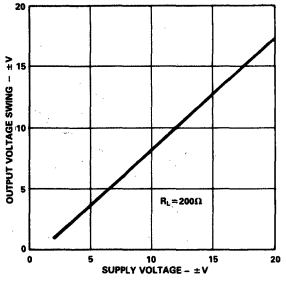


Figure 19. Output Voltage Swing vs. Supply Voltage

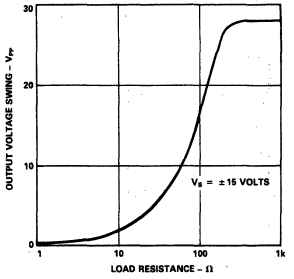


Figure 20. Output Voltage Swing vs. Load Resistance

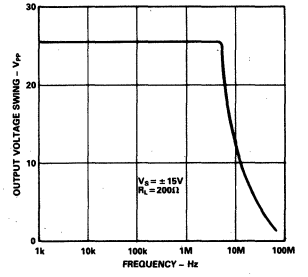


Figure 21. Large Signal Frequency Response

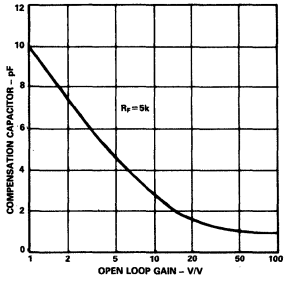


Figure 22. Recommended Compensation Capacitor vs. Closed Loop Gain

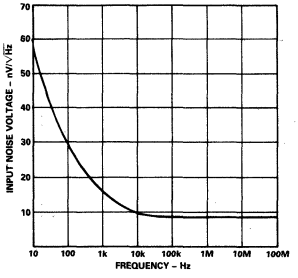


Figure 23. Input Noise Voltage Spectral Density

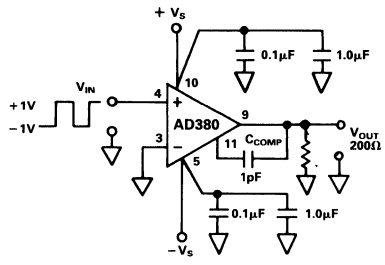


Figure 24a. Overdrive Recovery Test Circuit

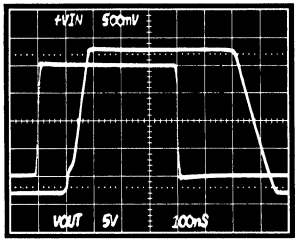


Figure 24b. Overdrive Recovery Response (Symmetrial 20ns Version Available)

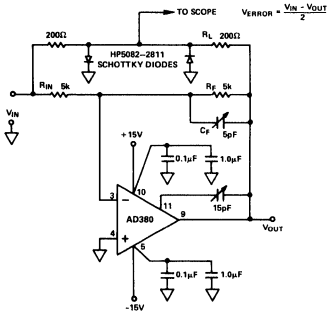


Figure 25a. Unity Gain Inverter Settling Time Test Circuit

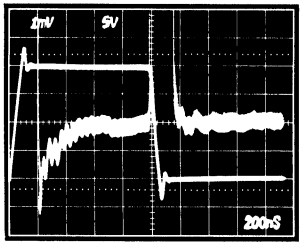


Figure 25b. Unity Gain Inverter Large Signal Response

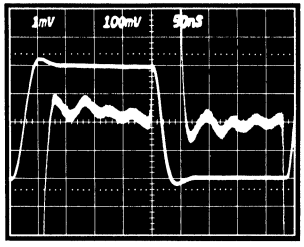


Figure 25c. Unity Gain Inverter Small Signal Response

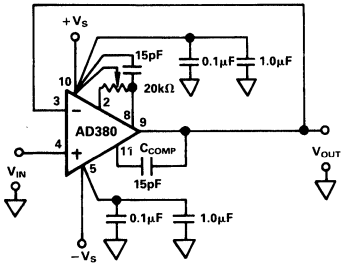


Figure 26a. Unity Gain Buffer Circuit

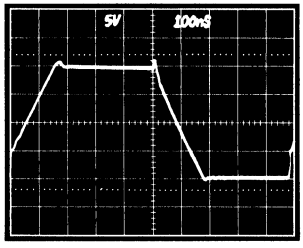


Figure 26b. Unity Gain Buffer Large Signal Response

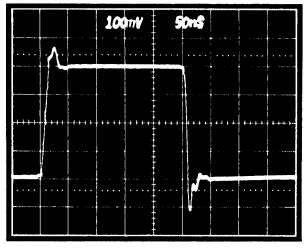


Figure 26c. Unity Gain Small Signal Response

APPLICATIONS INFORMATION

Compensation Capacitor

For low gain applications a 5pF to 27pF capacitor between the frequency compensation input (pin 11) and the output (pin 9) will reduce the risk of oscillation by adding phase margin. A compensation capacitor is especially needed when driving capacitive loads. For gains greater than 30 a 1pF compensation capacitor is recommended; see Figure 22.

For unity gain buffer applications it may be necessary to add a small (10pF to 20pF) capacitor between pins 8 and 10 for improved phase margin; see Figure 26a.

Offset Null

If the initial offset voltage is not low enough for the user's application offset nulling is required. To null the offset tie a 20kΩ potentiometer between the offset null pins (pins 2 and 8). The wiper of the potentiometer is tied to the positive supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

To minimize the effects of offset voltage drift as a function of temperature, null the offset at the midpoint of the operating temperature range. For example, if the operating environment is 0°C to 70°C do the offset nulling at 35°C. This will insure a maximum offset voltage drift of 35 times the V_{OS} drift specification at either temperature extreme.

Typical Circuits

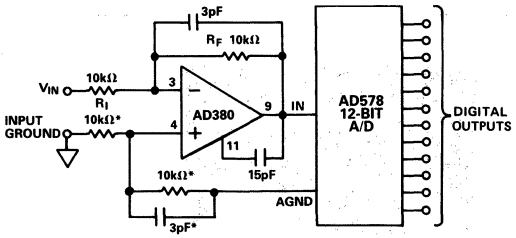


Figure 27. Fast-Settling Buffer

Its quick recovery from load variations makes the AD380 an excellent buffer for fast successive approximation A/D converters; see Figure 27.

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

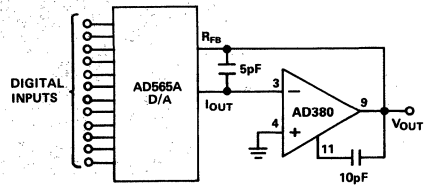


Figure 28. 12-Bit Voltage Output DAC Circuit Settles to 1/2LSB in 300ns

The AD565A 12-bit digital to analog converter with an AD380 output amplifier will give a voltage output that typically settles to within 1/2LSB in less than 300ns. Total settling time is the root mean square of the DAC current output settling time and the output amplifier settling time.

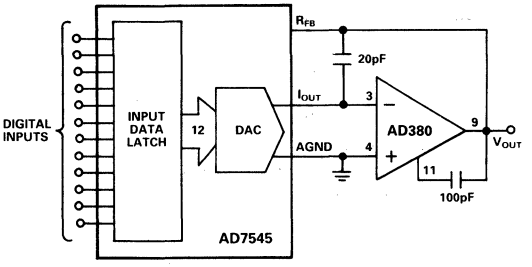


Figure 29. CMOS DAC Output Amplifier

CMOS DAC output amplifiers require low offset voltage op amps. The output impedance of CMOS DACs varies with input code. This can cause a code dependent error term at the output that approaches the op amps' offset voltage. If the DAC has a differential nonlinearity of 1/2LSB, it will require an output amplifier with less than 1/2LSB offset error to remain monotonic. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus, the AD380KH, with only 1mV offset maximum, will contribute less than 1/2LSB to differential linearity error.

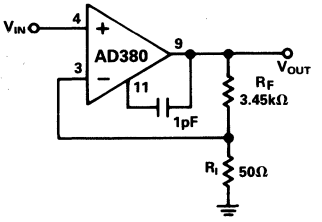


Figure 30. Video Amplifier

The high output current capability of the AD380 makes it suitable for video speed driver applications. In the circuit above the closed loop gain of 70 (37dB) is available over a bandwidth of 5MHz. Note that a 1pF compensation capacitor is required in this high gain application.

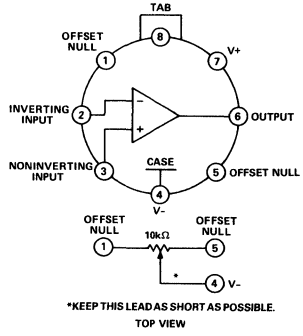
ANALOG DEVICES

High Speed, Low Drift FET Operational Amplifiers

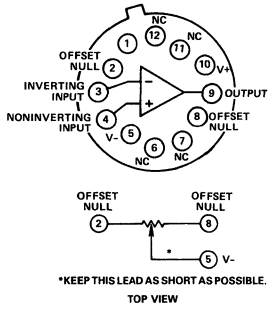
AD381/AD382

FEATURES
High Slew Rate 30V/μs
Fast Settling to 0.1%: 700ns
High Output Current: 50mA for AD382 (10mA for AD381)
Low Drift (5μV/°C–L Grades)
Low Offset Voltage (250μV–L Grades)
Low Input Bias Currents
Low Noise (2μV p-p)

AD381 PIN CONFIGURATION



AD382 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD381/AD382 are hybrid operational amplifiers combining the very low input bias current advantages of a FET input stage with high slew rate and line driving capability of a high power output stage.

The offset voltage (0.25mV maximum for the L grades) and offset voltage drift (5μV/°C maximum for the L grades) are exceptionally low for high speed operational amplifiers.

In addition to superior low drift performance, the AD381 and AD382 offer the lowest guaranteed input bias currents of any wideband FET amplifier with 100pA max for the J grades of each and 50pA max for the AD382 K, L and S grades. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our FET amplifiers are specified under actual operating conditions.

The AD381 and AD382 are especially designed for use in applications, such as precision high speed data acquisition systems and signal conditioning circuits, that require excellent input parameters and a fast, high power output.

The AD381 and AD382 are offered in three commercial versions, J, K and L specified from 0 to +70°C, and one extended temperature version, the S specified from −55°C to +125°C. All grades are packaged in hermetically sealed metal cans.

PRODUCT HIGHLIGHTS

1. Laser trimming techniques reduce offset voltage drift to 5μV/°C max and reduce offset voltage to only 250μV max on the L grade versions.
2. Analog Devices FET processing provides 100pA max (20pA typical) bias currents specified after 5 minutes of warm-up.
3. Internal frequency compensation, low offset voltage, and full device protection eliminate the need for external components and adjustments. This reduces circuit size and complexity and increases reliability.
4. The fast settling output (700ns to 0.1%) makes the AD381 and AD382 ideal for D/A and A/D converter amplifier applications.
5. The AD382's high output current (50mA minimum at ±10 volts) makes it suitable for driving terminated (200Ω) twisted pair cables over the commercial temperature ranges.
6. The high slew rate (30V/μs) and high gain bandwidth product (5MHz) make the AD381 and AD382 an ideal choice for sample and holds and for high speed integrator circuits.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD381JH AD382JH	AD381KH AD382KH	AD381LH AD382LH	AD381SH AD382SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$ (AD381)	60,000 min	100,000 min	**	**
V_{OUT} = ±10V, R_L = 200Ω (AD382)	25,000 min	35,000 min	**	**
R_L = 10kΩ (AD382)	100,000 min	150,000 min	**	**
OUTPUT CHARACTERISTICS (AD382)				
Voltage @ R_L = 200Ω	±12V (±10V min)	*	*	Note 1
Voltage @ R_L = 10kΩ	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	80mA	*	*	*
OUTPUT CHARACTERISTICS (AD381)				
Voltage @ R_L = 1kΩ, T_A = min to max	±12V (±10V min)	*	*	Note 2
Voltage @ R_L = 2kΩ, T_A = min to max	±12V (±10V min)	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	20mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	5MHz	*	*	*
Full Power Response	500kHz	*	*	*
Slew Rate, Unity Gain	30V/μs (20V/μs min)	*	*	*
Settling Time: 10V Step to 0.1%	700ns	*	*	*
10V Step to 0.01%	1.2μs	1.2μs (2.0μs max)	**	**
INPUT OFFSET VOLTAGE	1.0mV max	0.5mV max	0.25mV max	*
vs. Temperature, T_A = min to max[3]	15μV/°C max	10μV/°C max	5μV/°C max	10μV/°C max
vs. Supply	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT[4]				
Either Input (AD381)	20pA (100pA max)	*	*	*
Either Input (AD382)	20pA (100pA max)	10pA (50pA max)	**	**
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 7pF$	*	*	*
Common Mode	$10^{12}\Omega \| 7pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common-Mode Rejection, V_{IN} = ±10V	76dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	
Quiescent Current AD382	3.4mA (6mA max)	*	*	*
AD381	3.2mA (5mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz–10Hz	2μV p-p	*	*	*
10Hz	$35nV/\sqrt{Hz}$	*	*	*
100Hz	$22nV/\sqrt{Hz}$	*	*	*
1kHz	$18nV/\sqrt{Hz}$	*	*	*
10kHz	$16nV/\sqrt{Hz}$	*	*	*
TEMPERATURE RANGE[6]				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance – θ_{JA} (AD382)	100°C/W	*	*	*
Thermal Resistance – θ_{JC} (AD382)	70°C/W	*	*	*

NOTES

[1]The AD382SH has an output voltage of ±12V (±10V min) for a 200Ω load from T_{min} to +100°C. To +125°C the output current is 35mA.

[2]The AD381SH has an output voltage of ±12V (±10V min) for a 1kΩ load from T_{min} to +70°C. From +70°C to +125°C the output current is 7mA.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C for every mV of offset nulled.

[4]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[6]The S-grade is available in full compliance with MIL-STD-883 Rev C. Ask for the MIL-data sheet.

*Specifications same as J grade.

**Specifications same as K grade.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Initial Offset	Offset T.C.	Output	Package Options*
AD381JH	1mV	15μV/°C	10mA	H-08B
AD381KH	0.5mV	10μV/°C	10mA	H-08B
AD381LH	0.25mV	5μV/°C	10mA	H-08B
AD381SH	1mV	10μV/°C	10mA	H-08B
AD382JH	1mV	15μV/°C	50mA	H-12A
AD382KH	0.5mV	10μV/°C	50mA	H-12A
AD382LH	0.25mV	5μV/°C	50mA	H-12A
AD382SH	1mV	10μV/°C	50mA	H-12A

*See Section 20 for package outline information.

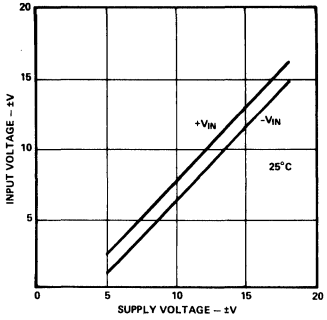


Figure 1. Input Voltage Range vs. Supply Voltage

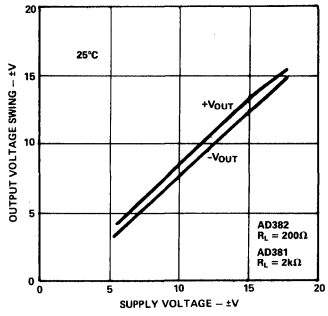


Figure 2. Output Voltage Swing vs. Supply Voltage

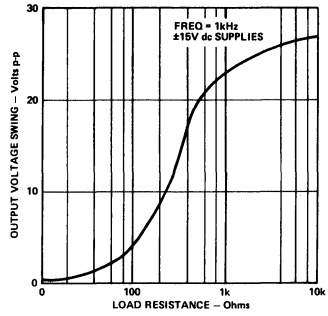


Figure 3a. Output Voltage Swing vs. Load Resistor for AD381

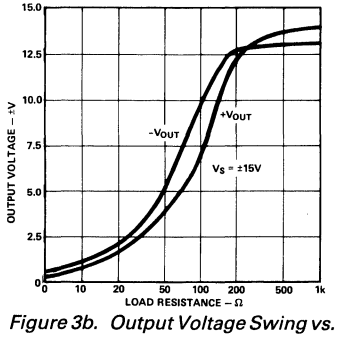


Figure 3b. Output Voltage Swing vs. Load Resistor for AD382

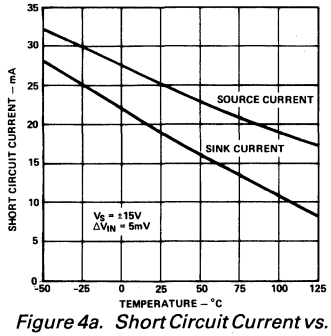


Figure 4a. Short Circuit Current vs. Temperature for AD381

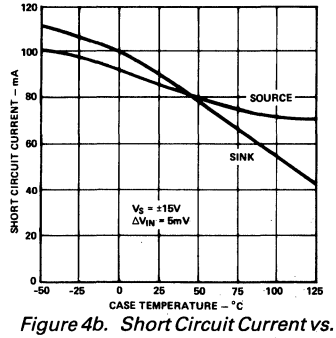


Figure 4b. Short Circuit Current vs. Temperature for AD382

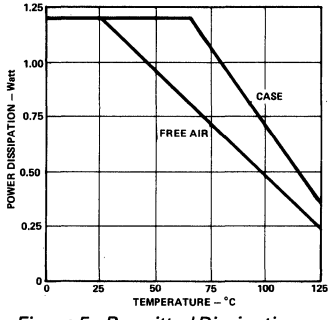


Figure 5. Permitted Dissipation vs. Temperature for AD382

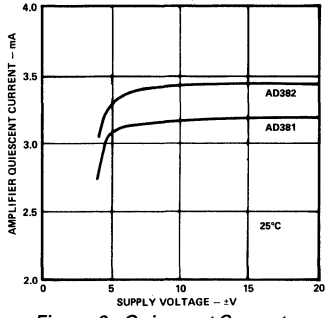


Figure 6. Quiescent Current vs. Supply Voltage

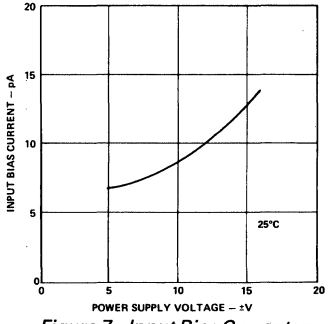


Figure 7. Input Bias Current vs. Supply Voltage

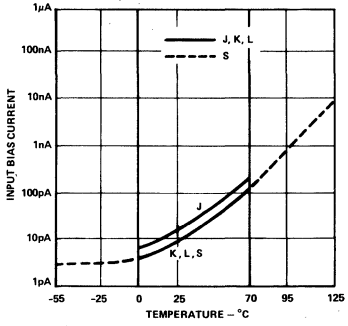


Figure 8. Input Bias Current vs. Temperature

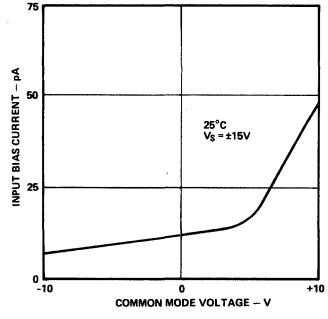


Figure 9. Input Bias Current vs. CMV

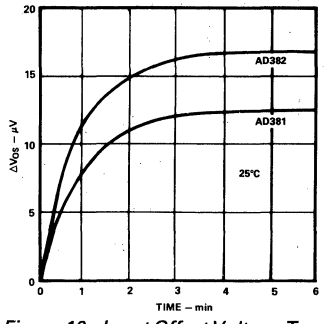


Figure 10. Input Offset Voltage Turn On Drift vs. Time

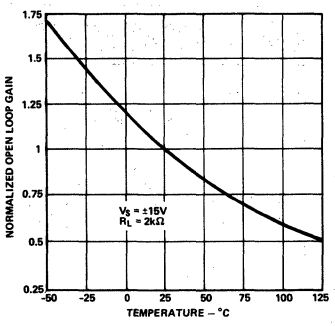


Figure 11a. Open Loop Gain vs. Temperature for AD381

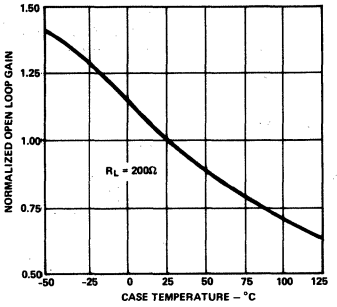


Figure 11b. Open Loop Gain vs. Temperature for AD382

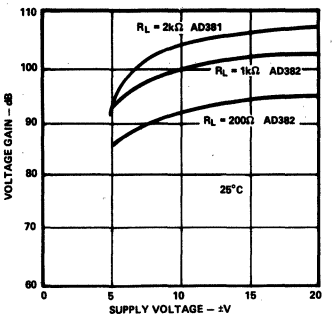


Figure 12. Open Loop Voltage Gain vs. Supply Voltage

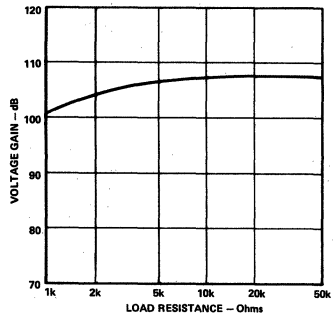


Figure 13a. Voltage Gain vs. Load Resistance for AD381

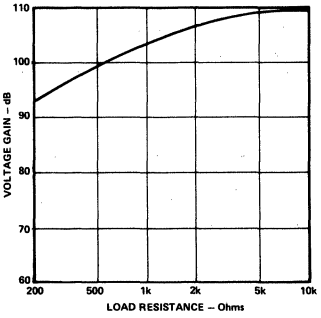


Figure 13b. Voltage Gain vs. Load Resistance for AD382

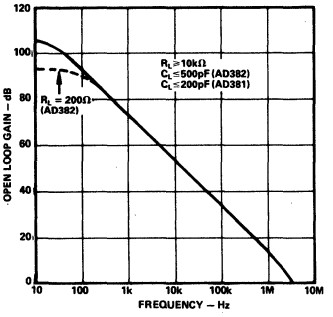


Figure 14. Open Loop Gain vs. Frequency

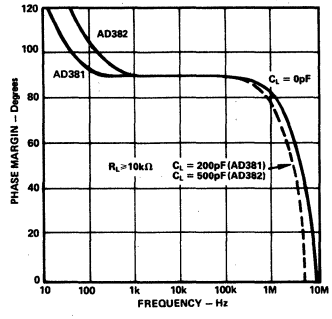


Figure 15. Phase Margin vs. Frequency

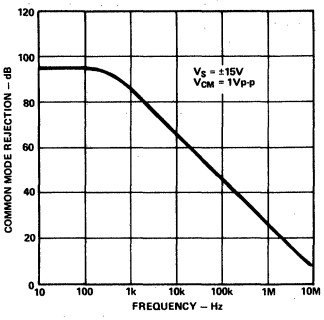


Figure 16. Common-Mode Rejection vs. Frequency

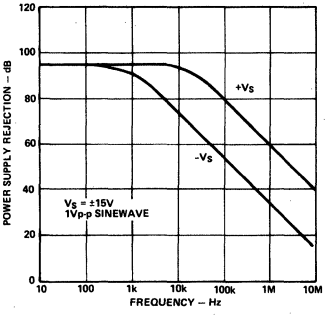


Figure 17. Power Supply Rejection vs. Frequency

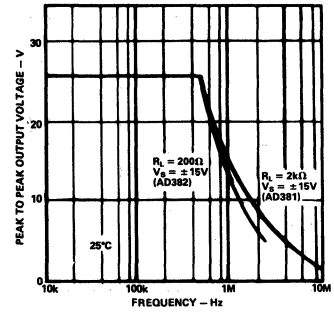


Figure 18. Large Signal Frequency Response

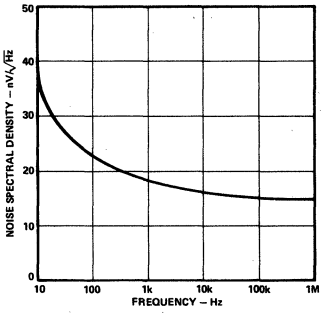


Figure 19. Noise vs. Frequency

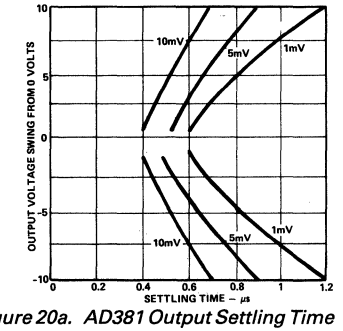


Figure 20a. AD381 Output Settling Time vs. Output Voltage Swing and Error (Circuit of Figure 22a)

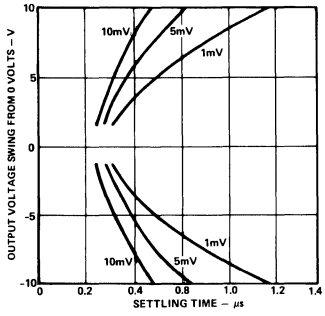


Figure 20b. AD382 Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

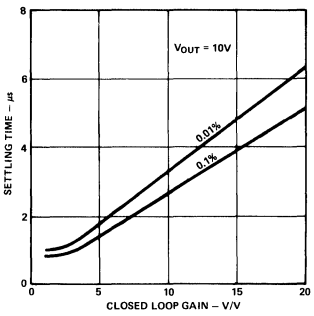


Figure 21. Settling Time vs. Closed Loop Gain (Circuits of Figures 22a & 23a)

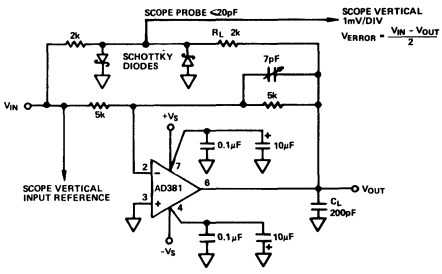


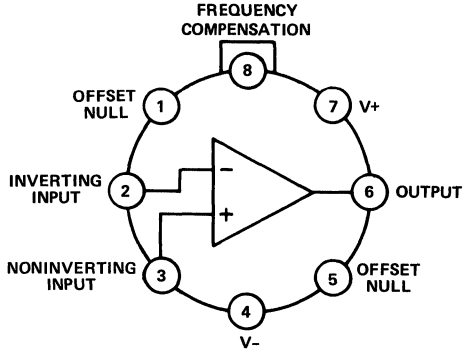
Figure 22. AD381 Unity Gain Inverter Settling Time Test Circuit

IC, Wideband, Fast Slewing General Purpose Operational Amplifier

AD507

FEATURES
Gain Bandwidth: 100MHz
Slew Rate: 20V/μs min
I_B: 15nA max (AD507K)
V_{os}: 3mV max (AD507K)
V_{os} Drift: 15μV/°C max (AD507K)
High Capacitive Drive

AD507 PIN CONFIGURATION



PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the extended temperature range, -55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.
5. To take full advantage of the inherent high reliability of IC's, every AD507S receives a 24 hour stabilization bake at +150°C.

MIL-STANDARD-883

The AD507S/883 has the same electrical specifications as the AD507S, but is subjected to the 100% screening requirements specified in MIL-STD-883, Method 5004, Class B.

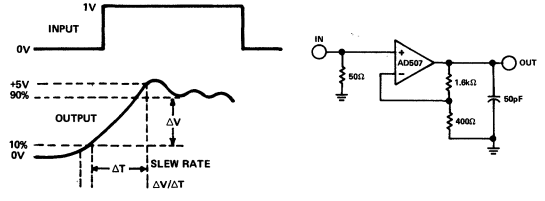
This procedure includes:

1. Pre-Cap Visual Inspection: Method 2010, Condition B.
2. Stabilization Bake: Method 1008, Condition C, 24 hours @ +150°C.
3. Temperature Cycle: Method 1010, Condition C, -65°C to +150°C, 10 cycles.
4. Centrifuge: Method 2001, Condition E, 30,000 g, Y_1 orientation.
5. Hermeticity, Gross Leak: Method 1014, Condition C, steps 1 and 2.
6. Hermeticity, Fine Leak: Method 1014, Condition A, 5×10^{-8} atm/cc/sec.
7. Burn-In: Method 1015, 160 hours @ +125°C.
8. Final Electrical Test.
9. External Visual: Method 2009.

SPECIFICATIONS (typical at +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD507J	AD507K	AD507S(AD507S/883)**
OPEN LOOP GAIN			
R_L = 2kΩ, C_L = 50pF	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T_{min} to T_{max}	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, C_L = 50pF, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ V_o = ±10V	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	1MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (±35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (500MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	12nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Operating	-25°C to +85°C	*	-65°C to +150°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTION[1]			
H-08A	AD507JH	AD507KH	AD507SH

NOTES
[1] See Section 20 for package outline information.
*Specifications same as AD507J.
**AD507S/883 minimum order 10 pieces.
Specifications subject to change without notice.



Slew Rate Definition and Test Circuit

APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

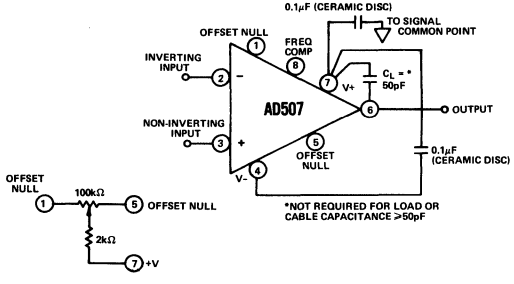


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

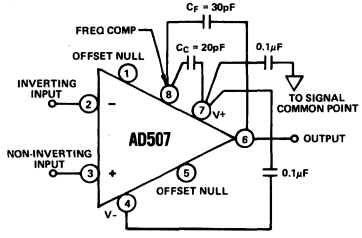


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.

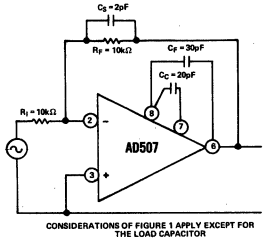
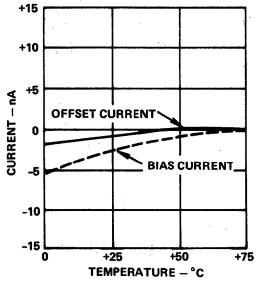
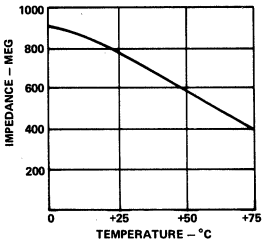


Figure 3. Fast Settling Time Configuration

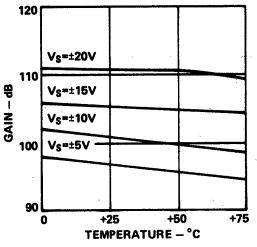
TYPICAL PERFORMANCE CURVES



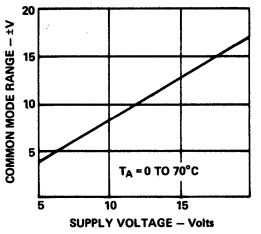
Input Bias Current and Offset Current vs Temperature



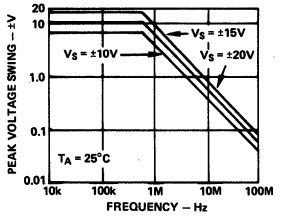
Input Impedance vs Temperature



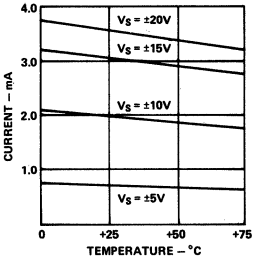
Open Loop Voltage Gain vs Temperature



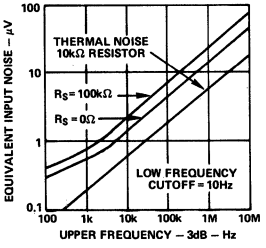
Common Mode Voltage Range vs Supply Voltage



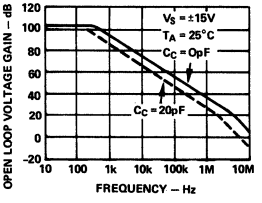
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency

ANALOG DEVICES

High Speed, Fast Settling IC Op Amp

AD509

FEATURES

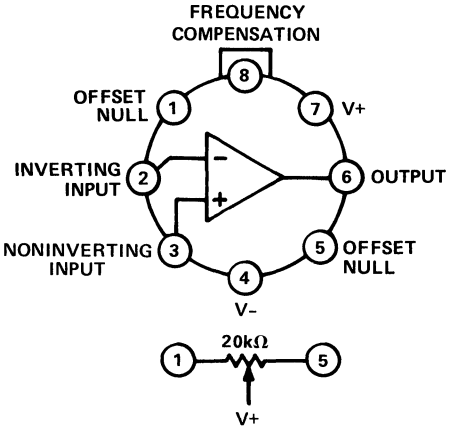
- Fast Settling Time
  - 0.1% in 500ns max
  - 0.01% in 2.5μs max
- High Slew Rate: 100V/μs min
- Low I_{OS}: 25nA max
- Guaranteed V_{OS} Drift: 30μV/°C max
- High CMRR: 80dB min
- Drives 500pF
- Low Price

APPLICATIONS

- D/A and A/D Conversion
- Wideband Amplifiers
- Multiplexers
- Pulse Amplifiers

AD509 PIN CONFIGURATIONS

TO-99



TOP VIEW

PRODUCT DESCRIPTION

The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. Other comparable dynamic parameters include a small signal bandwidth of 20MHz, slew rate of 100V/μs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to 30μV/°C max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to +70°C temperature range; the AD509S for operation from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains thus eliminating the elaborate stabilizing techniques required by other high speed IC op amps.
2. The AD509 will drive capacitive loads of 500pF without deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
3. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.
4. The AD509K and AD509S are 100% tested for minimum slew rate and guaranteed to settle to 0.01% of its final value in less than 2.5μs.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD509J Min	AD509J Typ	AD509J Max	AD509K Min	AD509K Typ	AD509K Max	AD509S Min	AD509S Typ	AD509S Max	Units
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**7,500**	15,000		**10,000**	15,000		**10,000**	15,000		V/V
T_{min} to T_{max}, R_L = 2kΩ	5,000			7,500			**7,500**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		V
FREQUENCY RESPONSE										
Unity Gain Small Signal		20			20			20		MHz
Full Power Response	1.2	1.6		1.5	2.0		1.5	2.0		MHz
Slew Rate, Unity Gain	80	120		80	120		100	120		V/μs
Settling Time										
to 0.1%		200			200			200	500	ms
to 0.01%		1.0			1.0			1.0	2.5	μs
INPUT OFFSET VOLTAGE										
Initial Offset		5	**10**		4	**8**		4	**8**	mV
Input Offset Voltage T_{min} to T_{max}			14			11			**11**	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**	μV/V
INPUT BIAS CURRENT										
Initial		125	**250**		100	**200**		100	**200**	nA
T_{min} to T_{max}			500			400			**400**	nA
INPUT OFFSET CURRENT										
Initial		20	50		10	25		10	25	nA
T_A = min to max			100			50			50	nA
INPUT IMPEDANCE										
Differential	40	100		50	100		50	100		MΩ
INPUT VOLTAGE RANGE										
Differential		±15			±15			±15		V
Common Mode		±10			±10			±10		V
Common Mode Rejection	**74**	90		**80**	90		**80**	90		dB
INPUT NOISE VOLTAGE										
f = 10Hz		100			100			100		nV/√Hz
f = 100Hz		30			30			30		nV/√Hz
f = 100kHz		19			19			19		nV/√Hz
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±20	±5		±20	±5		±20	V
Quiescent Current		4	**6**		4	**6**		4	**6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	−55		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[1]										
TO-99 Style (H-08A)		AD509JH			AD509KH			AD509SH		

NOTES
[1]See Section 20 for package outline information.
Specifications subject to change without notice.
All min and max specifications are guaranteed.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

APPLYING THE AD509

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting settling time. In most high speed amplifiers, after the amplifier has slewed to the vicinity of the final output voltage, it must recover from internal saturation and then allow any overshoot and ringing to damp out. These definitions are illustrated in Figure 1.

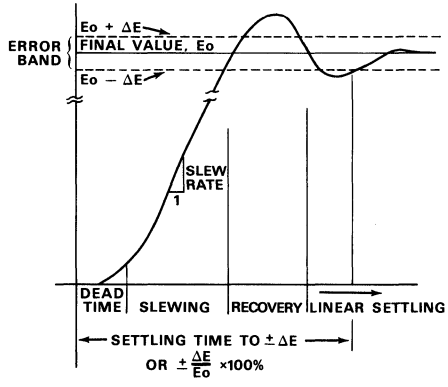


Figure 1. Settling Time

The AD509K and AD509S are guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5μs when tested as shown in Figure 2. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope

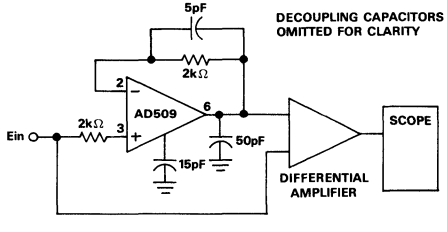


Figure 2. AD509 Settling Time Test Circuit

display. The resultant waveform of (E_O − E_{IN}) of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5μs. The top trace represents the output signal; the bottom trace represents the error signal.

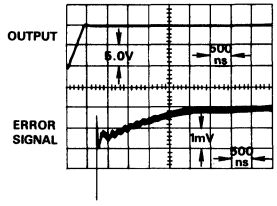


Figure 3. Settling Time of AD509

SETTLING TIME VS. R_f AND R_i. Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g., 5kΩ; in order to insure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance.

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509, compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under 2.0μs.

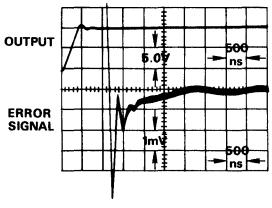


Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5μs. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are.....

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).

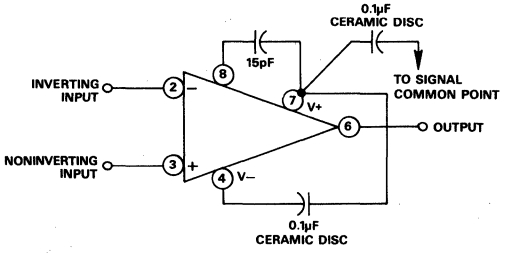


Figure 5. Configuration for Unity Gain Applications

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier. Minimize noise pickup.

DYNAMIC RESPONSE OF AD509

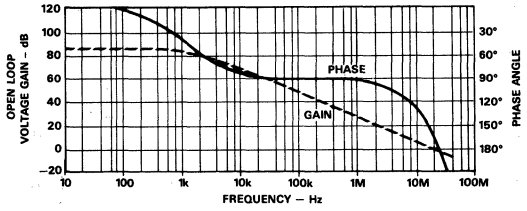


Figure 6. Open Loop Frequency and Phase Response

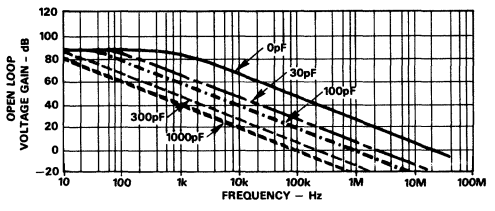


Figure 7. Open Loop Frequency Response for Various C_C's

THE AD509 AS AN OUTPUT AMPLIFIER FOR FAST CURRENT-OUTPUT D-TO-A CONVERTERS

Most fast integrated circuit digital to analog converters have current outputs. That is, the digital input code is translated to an output current proportional to the digital code. In many applications, that output current is converted to a voltage by connecting an operational amplifier in the current-to-voltage conversion mode.

The settling time of the combination depends on the settling time of the DAC and the output amplifier. A good approximation is:

$$t_s \text{ TOTAL} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

Some IC DACs settle to final output value in 100-500 nanoseconds. Since most IC op amps require a longer time to settle to ±0.1% or ±0.01% of final value, amplifier settling time can dominate total settling time. And for a 12-bit DAC, one least significant bit is only 0.024% of full-scale, so low drift and high linearity and precision are also required of the output amplifier.

Figure 8 shows the AD509K connected as an output amplifier with the AD565K, high speed 12-bit IC digital-to-analog converter. The 10 picofarad capacitor, C1, compensates for the 25pF AD565 output capacitance. The voltage output of the AD565K/AD509K combination settles to ±0.01% in one microsecond. The low input voltage drift and high open loop gain of the AD509K assures 12-bit accuracy over the operating temperature range.

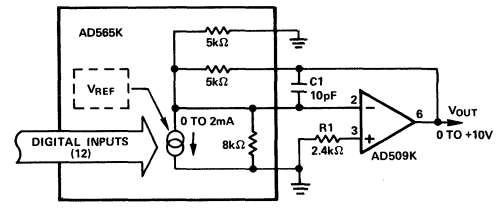


Figure 8. AD509 as an Output Amplifier for a Fast Current-Output D-to-A Converter

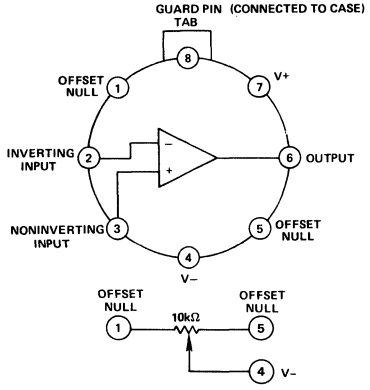
Monolithic Precision, Low Power FET-Input Electrometer Op Amp

AD515A*

FEATURES

Ultralow Bias Current: 75fA max (AD515AL)
150fA max (AD515AK)
300fA max (AD515AJ)
Low Power: 1.5mA max Quiescent Current (0.6mA typ)
Low Offset Voltage: 1.0mV max (AD515AK & L)
Low Drift: 15μV/°C max (AD515AK)
Low Noise: 4μV p-p, 0.1Hz to 10Hz

AD515A PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD515A is a monolithic FET-input operational amplifier with a guaranteed maximum input bias current of 75fA (AD515AL). The AD515A is a monolithic successor to the industry standard AD515 electrometer, and will replace the AD515 in most aplications. The AD515A also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultralow bias current circuits. All devices are internally compensated, protected against latch-up and are short circuit protected.

The AD515A's combination of low input bias current, low offset voltage and low drift optimizes it for a wide variety of electrometer and very high impedance buffer applications including photo-current detection, vacuum ion-gage measurement, long-term precision integration and low drift sample/hold applications. This amplifier is also an excellent choice for all forms of biomedical instrumentation such as pH/pIon sensitive electrodes, very low current oxygen sensors, and high impedance biological microprobes. In addition, the low cost and pin compatibility of the AD515A with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The $10^{15}\Omega$ common-mode input impedance ensures that the input bias current is essentially independent of common-mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (Pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients.

The AD515A is available in three versions of bias current and offset voltage, the "J", "K" and "L"; all are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed TO-99 package. The industry standard hybrid version, AD515, will also be available.

***Covered by Patent No. 4,639,683.**

PRODUCT HIGHLIGHTS

1. The AD515A provides subpicoampere bias currents in an integrated circuit amplifier.
   - The ultralow input bias currents are specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient with no heat sink. This parameter is 100% tested.
   - By using ±5V supplies, input bias current can typically be brought below 50fA.
2. The input offset voltage on all grades is laser trimmed, typically less than 500μV.
   - The offset voltage drift is 15μV/°C maximum on the K grade.
   - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3μV/°C per mV).
3. The low quiescent current drain of 0.6mA typical and 1.5mA maximum, keeps self-heating effects to a minimum and renders the AD515A suitable for a wide range of remote probe applications.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from 1MΩ to $10^{11}\Omega$, the Johnson noise of the source will easily dominate the noise characteristic.
5. Every AD515A receives a 24-hour stabilization bake at +150°C, to ensure reliability and long-term stability.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

Model	AD515AJ	AD515AK	AD515AL
OPEN-LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	**20,000V/V min**	**40,000V/V min**	**25,000V/V min**
$R_L \geq 10k\Omega$	**40,000V/V min**	**100,000V/V min**	**50,000V/V min**
T_A = min to max $R_L \geq 2k\Omega$	**15,000V/V min**	**40,000V/V min**	**25,000V/V min**
OUTPUT CHARACTERISTICS			
Voltage@R_L = 2kΩ, T_A = min to max	**±10V min (±12V typ)**	*	*
@R_L = 10kΩ, T_A = min to max	**±12V min (±13V typ)**	*	*
Load Capacitance[2]	1000pF		
Short-Circuit Current	**10mA min (20mA typ)**		
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1MHz	*	*
Full Power Response	5kHz min (50kHz typ)	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (3.0V/μs typ)	*	*
Overload Recovery Inverting Unity Gain	100μs max (2μs typ)	*	*
INPUT OFFSET VOLTAGE[3]	**3.0mV max (0.4mV typ)**	**1.0mV max (0.4mV typ)**	**1.0mV max (0.4mV typ)**
vs. Temperature, T_A = min to max	**50μV/°C max**	**15μV/°C max**	**25μV/°C max**
vs. Supply, T_A = min to max	**400μV/V max (50μV/V typ)**	**100μV/V max**	**200μV/V max**
INPUT BIAS CURRENT			
Either Input[4]	**300fA max**	**150fA max**	**75fA max**
INPUT IMPEDANCE			
Differential V_{DIFF} = ±1V	1.6pF‖$10^{13}\Omega$	*	*
Common Mode	0.8pF‖$10^{15}\Omega$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	4.0μV (p-p)	*	*
f = 10Hz	75nV/$\sqrt{Hz}$	*	*
f = 100Hz	55nV/$\sqrt{Hz}$	*	*
f = 1kHz	50nV/$\sqrt{Hz}$	*	*
Current, 0.1Hz to 10Hz	0.007pA (p-p)	*	*
10Hz to 10kHz	0.01pA rms	*	*
INPUT VOLTAGE RANGE			
Differential	**±20V min**	*	*
Common Mode, T_A = min to max	**±10V min (+12V, −11 typ)**	*	*
Common-Mode Rejection, V_{IN} = ±10V	**66dB min (94dB typ)**	**80dB min**	**70dB min**
Maximum Safe Input Voltage[5]	±V_S	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	**±5V min (±18V max)**	*	*
Quiescent Current	**1.5mA max (0.6mA typ)**	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	*
Storage	−65°C to +150°C	*	*
PACKAGE OPTION[6]			
TO-99 (H-08A)	AD515AJH	AD515AKH	AD515ALH

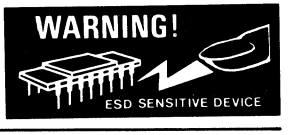
NOTES
*Specifications same as AD515AJ.
[1]Open Loop Gain is specified with or without nulling of V_{OS}.
[2]A conservative design would not exceed 750pF of load capacitance.
[3]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4]Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.
[5]If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.1mA. The input devices can handle overload currents of 0.1mA indefinitely without damage. See next page.
[6]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final test.

ESD PRECAUTIONS

Charges as high as 4000V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.



LAYOUT AND CONNECTIONS CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515A, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515A can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultralow input currents of the AD515A. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation and, hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515A is brought out separately to Pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry and reduces common-mode input capacitance to about 0.8pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and noninverting applications. If Pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

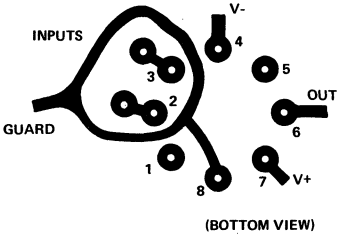


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515A can deliver. The best performance will be realized by using a teflon IC socket for the AD515A; but at least a teflon stand-off should be used for the high impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.
4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

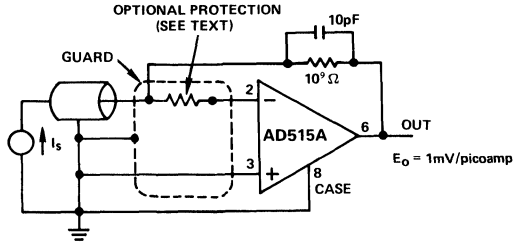


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

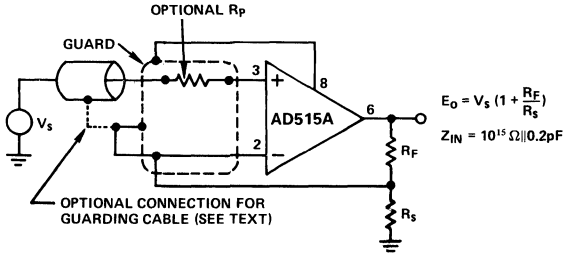


Figure 3. Very High Impedance Noninverting Amplifier

INPUT PROTECTION

The AD515A is guaranteed for a maximum safe input potential equal to the power supply potential.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate Zener protection schemes which often compromise overall performance. The AD515A requires input protection only if the source is not current limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.1mA (for example, 1MΩ for a 100V overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

COAXIAL CABLE AND CAPACITANCE EFFECTS

If it is not possible to attach the AD515A virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant such as Amphenol 21-537 will reduce the noise, but short, rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other objects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from: $\Delta V = Q/\Delta C$. Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is usually about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515A. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will destabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Noninverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to a guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may be destabilized and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at Pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

Typical Performance Curves

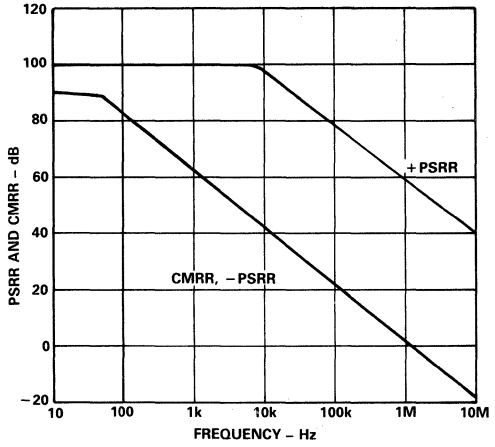


Figure 4. PSRR and CMRR vs. Frequency

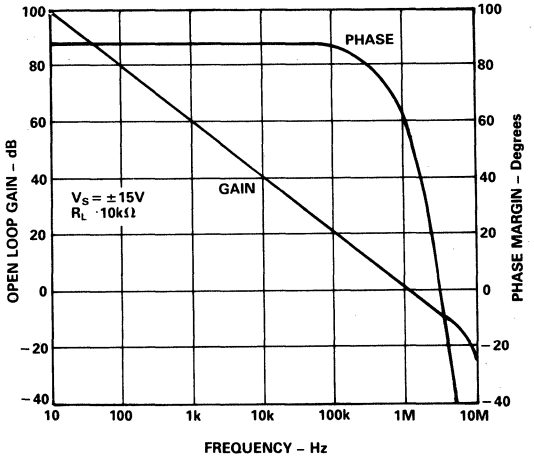


Figure 5. Open Loop Frequency Response

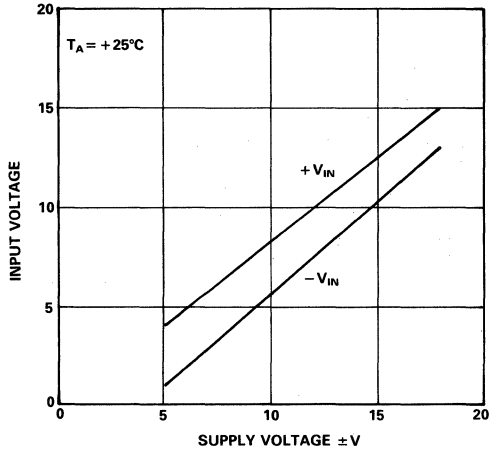


Figure 6. Input Common-Mode Range vs. Supply Voltage

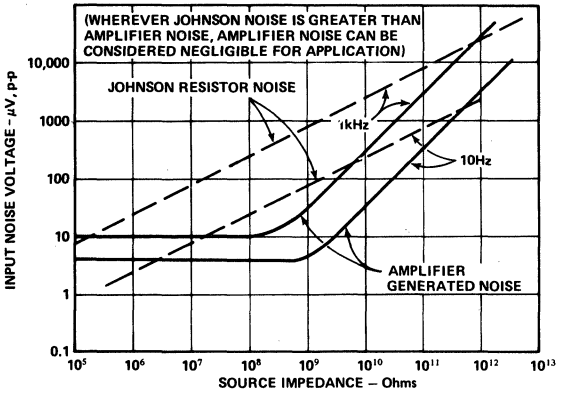


Figure 7. Peak-to-Peak Input Noise Voltage vs. Source Impedance and Bandwidth

ELECTROMETER APPLICATION NOTES

The AD515A offers subpicoampere input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515A and perhaps extending its performance limits.

1. As with all junction FET input devices, the temperature of the FETs themselves is all important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515A has been reduced to less than 1mA. Figure 8 shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10V at the output will cause at least an additional 25mW dissipation in the output stage (and some in other stages) over the typical 24mW, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many dc performance parameters are specified driving a 2kΩ load, to reduce this additional dissipation, we recommend restricting the load resistance to be at least 10kΩ.
4. Figure 10 shows the AD515A's input current versus differential input voltage. Input current at either terminal stays below a few hundred fA until one input terminal is forced higher than 1 to 1.5V above the other terminal. Input current limits at 30μA under these conditions.

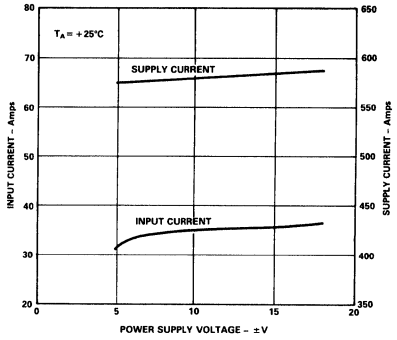


Figure 8. Input Bias Current and Supply Current vs. Supply Voltage

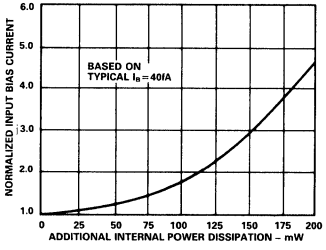


Figure 9. Input Bias Current vs. Additional Power Dissipation

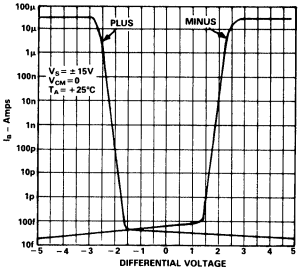


Figure 10. Input Bias Current vs. Differential Input Voltage

AD515A CIRCUIT APPLICATION NOTES

The AD515A is quite simple to apply to a wide variety of applications because of the pretrimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High MΩ resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high MΩ resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long-term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515A is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515A are significant only above $10^{11}\Omega$.

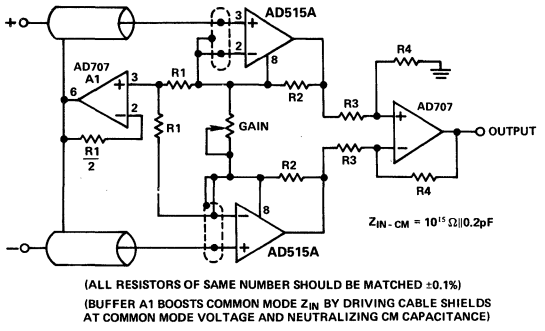


Figure 11. Very High Impedance Instrumentation Amplifier

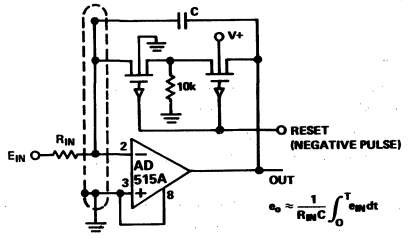


Figure 12. Low Drift Integrator and Low-Leakage Guarded Reset

LOW-LEVEL CURRENT-TO-VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above $10^9\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515A makes the tradeoff easier.

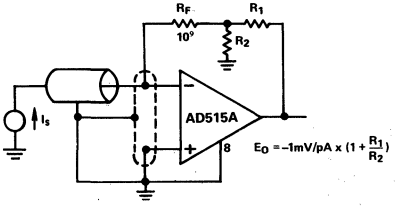


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the noninverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD524 instrumentation amplifier converts the floating differential signal to a single-ended output.

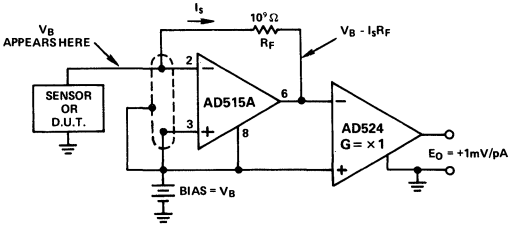


Figure 14. Current-to-Voltage Converters with Grounded Bias and Sensor

ANALOG DEVICES

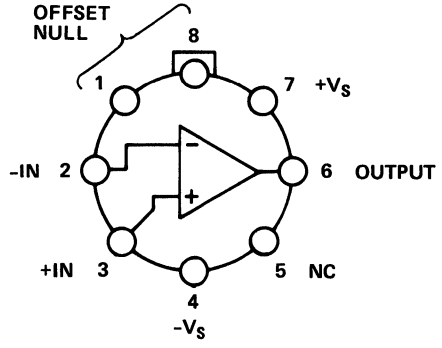
Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES

- **Low Input Bias Current: 1nA max (AD517L)**
- **Low Input Offset Current: 0.25nA max (AD517L)**
- **Low V_{OS}: 50μV max (AD517L), 150μV max (AD517J)**
- **Low V_{OS} Drift: 1.3μV/°C (AD517L)**
- **Internal Compensation**
- **MIL-Standard Parts Available**
- **8-Pin TO-99 Hermetic Metal Can**
- **Available in Chip Form**

AD517 PIN CONFIGURATION



TOP VIEW

PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 50μV and offset voltage drifts less than 1.3μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to $\pm V_S$), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.
7. Chips are available.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

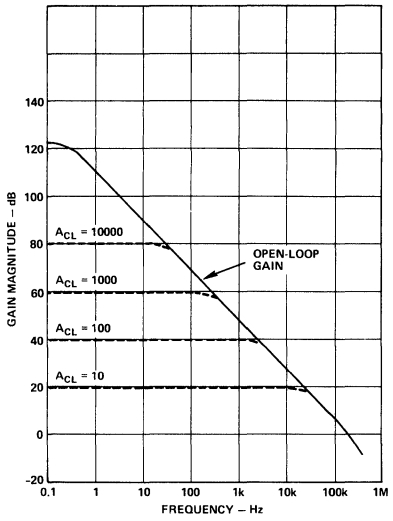
Model	AD517J Min	AD517J Typ	AD517J Max	AD517K Min	AD517K Typ	AD517K Max	AD517L Min	AD517L Typ	AD517L Max	AD517S Min	AD517S Typ	AD517S Max	Units
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**10^6**			**10^6**			**10^6**			**10^6**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	500,000			500,000			500,000			**250,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**			**±10**			**±10**			**±10**			V
Load Capacitance		1000			1000			1000			1000		pF
Output Current	10			10			10			10			mA
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		250			250			250			250		kHz
Full Power Response		1.5			1.5			1.5			1.5		kHz
Slew Rate, Unity Gain		0.10			0.10			0.10			0.10		V/µs
INPUT OFFSET VOLTAGE													
Initial Offset			**150**			**75**			**50**			**75**	µV
Input Offset vs. Temp.			3.0			**1.8**			**1.3**			**1.8**	µV/°C
Input Offset vs. Supply			**25**			**10**			**10**			**10**	µV/V
T_{min} to T_{max}			40			15			15			**20**	µV/V
INPUT BIAS CURRENT													
Initial			5			**2**			**1.0**			**2.0**	nA
T_{min} to T_{max}			8			3.5			1.5			**10**	nA
vs. Temp, T_{min} to T_{max}			±20			±10			±4			±10	pA/°C
INPUT OFFSET CURRENT													
Initial			**1.0**			**0.75**			**0.25**			**2.0**	nA
T_{min} to T_{max}			1.5			1.25			0.4			**10**	nA
INPUT IMPEDANCE													
Differential		15‖1.5			20‖1.5			20‖1.5			20‖1.5		MΩ‖pF
Common Mode		2.0×10^{9}			2.0×10^{9}			2.0×10^{9}			2.0×10^{9}		Ω
INPUT VOLTAGE RANGE													
Differential		±V_S			±V_S			±V_S			±V_S		V
Common Mode Rejection	**94**			**110**			**110**			**110**			dB
Common Mode Rejection T_{min} to T_{max}	94			110			100			**100**			dB
INPUT NOISE													
Voltage, 0.1Hz to 10Hz		2			2			2			2		µV p-p
f = 10Hz		35			35			35			35		nV/√Hz
f = 100Hz		25			25			25			25		nV/√Hz
f = 1kHz		20			20			20			20		nV/√Hz
Current, f = 10kHz		0.05			0.05			0.05			0.05		pA/√Hz
f = 100Hz		0.03			0.03			0.03			0.03		pA/√Hz
f = 1kHz		0.03			0.03			0.03			0.03		pA/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**4**			**3**			**3**			**3**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[1]													
TO-99 Style (H-08B)		AD517JH			AD517KH			AD517LH			AD517SH		
J and S Grade Chips Also Available													

NOTES

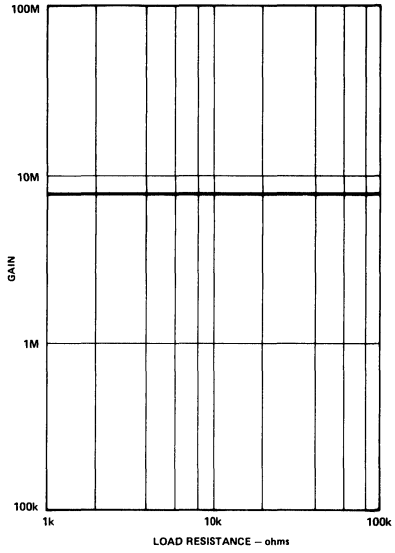
[1]See Section 20 for package outline information.

Specifications subject to change without notice.

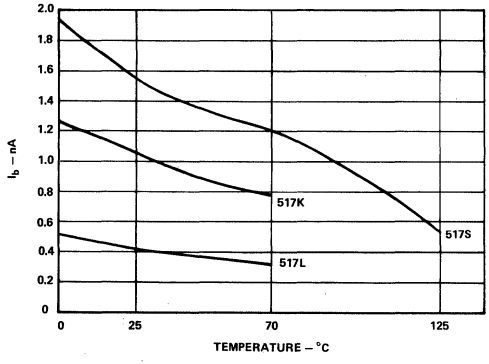
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



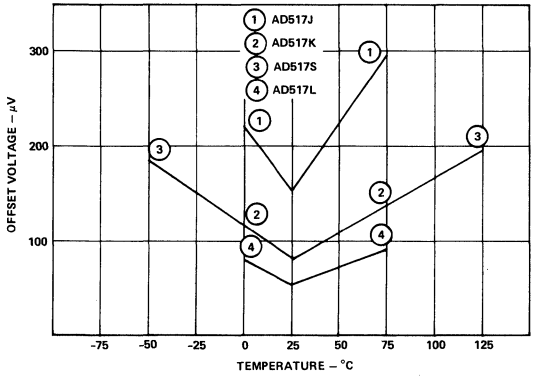
Small-Signal Gain vs. Frequency



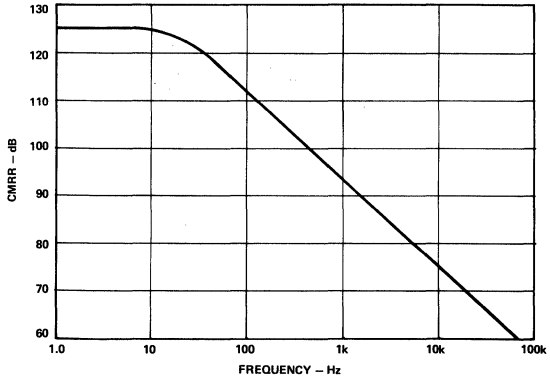
Open-Loop Gain vs. Load Resistance



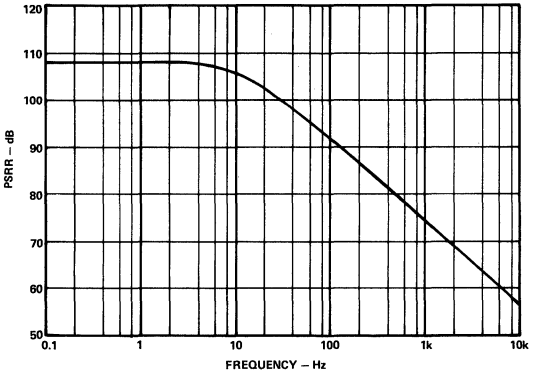
Input Bias Current vs. Temperature



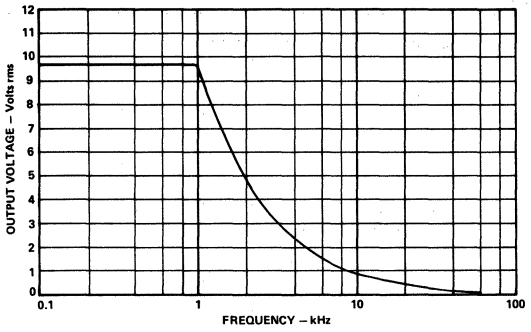
Untrimmed Offset Voltage vs. Temperature



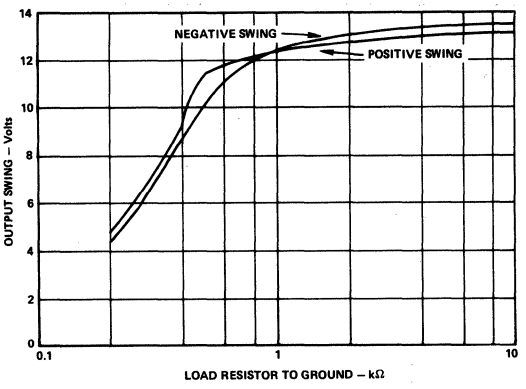
CMRR vs. Frequency



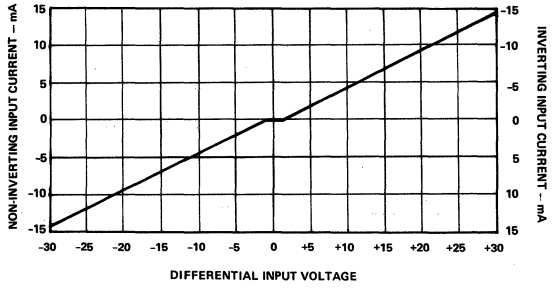
PSRR vs. Frequency



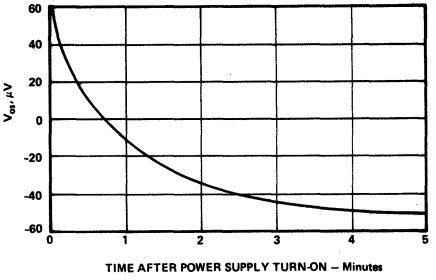
Maximum Undistorted Output vs. Frequency (Distortion ⩽ 1%)



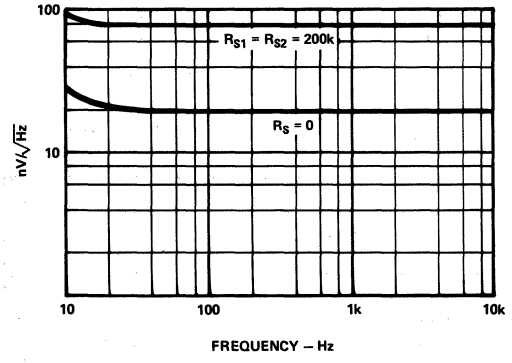
Output Voltage vs. Load Resistance



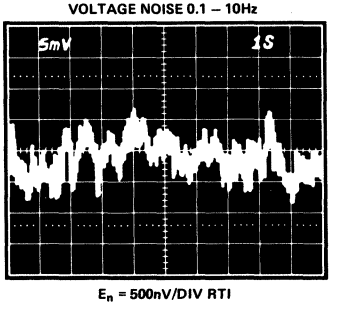
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

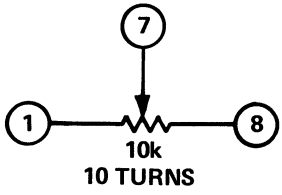
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

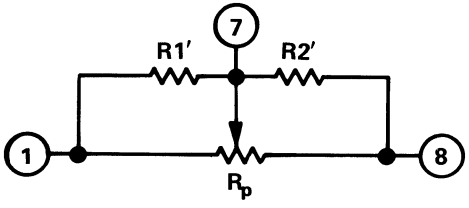
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1} \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

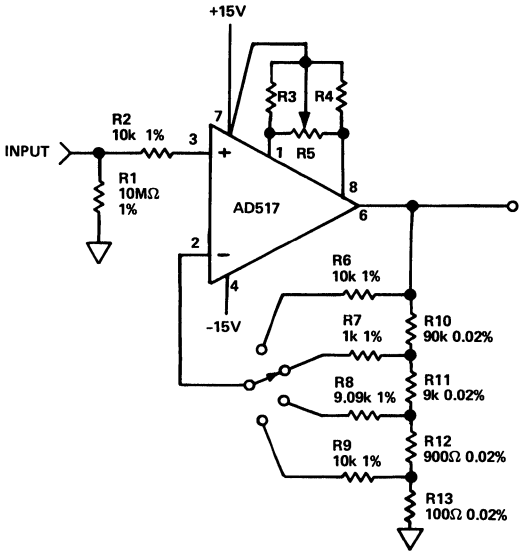


Figure 2. Stable Instrument Input Amplifier

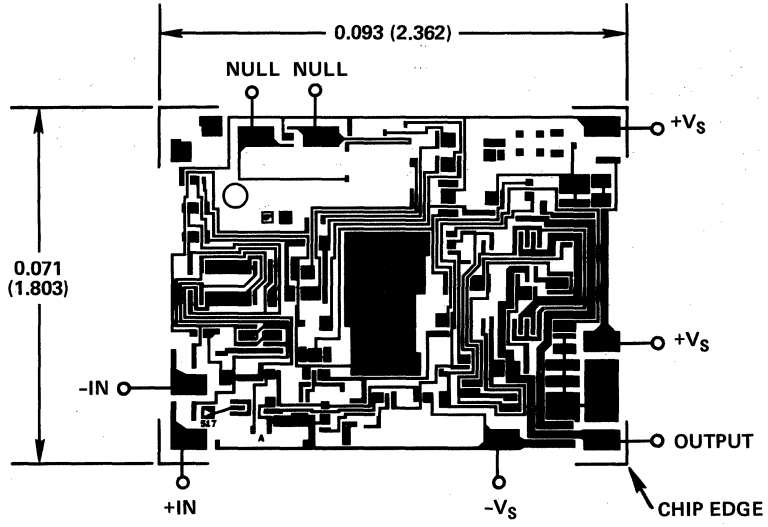
Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6, R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



THE AD517 IS AVAILABLE IN
LASER-TRIMMED CHIP FORM.

ANALOG DEVICES

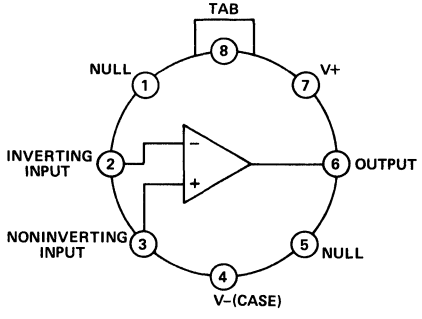
High Performance, BiFET Operational Amplifiers

AD542/AD544/AD547

FEATURES

Ultralow Drift: 1μV/°C – AD547L
Low Offset Voltage: 0.25mV – AD547L
Low Input Bias Currents: 25pA max, Warmed-Up
Low Quiescent Current: 1.5mA
Low Noise: 2μV p-p
High Open Loop Gain: 110dB
High Slew Rate: 13V/μs
Fast Settling to ±0.01%: 3μs
Low Total Harmonic Distortion: 0.0025%
Available in Hermetic Metal Can Packages and Chip Form
MIL-STD-883B Processing Available
Dual Versions Available: AD642, AD644, AD647

AD542/AD544/AD547 FUNCTIONAL BLOCK DIAGRAM



TOP VIEW

PRODUCT DESCRIPTION

The BiFET series are precision monolithic FET-input operational amplifiers fabricated with the most advanced BiFET and laser trimming technologies. The series offers bias currents significantly lower than currently available BiFET devices, 25pA max, warmed-up.

In addition, the offset voltage is laser trimmed to less than 0.25mV on the AD547L which is achieved by utilizing Analog's exclusive laser-wafer trimming (LWT) process. When combined with the AD547's low offset voltage drift (1μV/°C), these features offer the user IC performance truly superior to existing BiFET op amps–and at low, BiFET pricing.

The AD542 or AD547 is recommended for any operational amplifier application requiring excellent dc performance at low to moderate costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and high open-loop gain–even under heavy loading–ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is recommended for any operational amplifier application requiring excellent ac and dc performance at low cost. The 2MHz bandwidth and low offset of the AD544 make it the first choice as an output amplifier for current output D/A converters such as the AD7541, 12-bit CMOS DAC.

Devices in this series are available in four versions: the "J," "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the −55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing results in the lowest bias current available in a monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the device will meet its published specifications in actual use.
3. Advanced laser wafer trimming techniques reduce offset voltage drift to 1μV/°C max and offset voltage to only 0.25mV max on the AD547L.
4. Low voltage noise (2μV, p-p), and low offset voltage drift enhance performance as a precision op amp.
5. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
6. Low harmonic distortion (0.0025%) make the AD544 an ideal choice for audio applications.
7. Unmounted chips available for hybrid circuit applications.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD542 Min	AD542 Typ	AD542 Max	AD544 Min	AD544 Typ	AD544 Max	AD547 Min	AD547 Typ	AD547 Max	Units
OPEN LOOP GAIN[1]										
$V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$										
J	**100,000**			**30,000**			**100,000**			V/V
K, L, S	**250,000**			**50,000**			**250,000**			V/V
$T_A = T_{min}$ to T_{max}										
J	100,000			20,000			100,000			V/V
S	**100,000**			**20,000**			**100,000**			V/V
K, L	**250,000**			**40,000**			**250,000**			V/V
OUTPUT CHARACTERISTICS										
$V_{OUT} = R_L = 2k\Omega$										
$T_A = T_{min}$ to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		Volts
$V_{OUT} = R_L = 10k\Omega$										
$T_A = T_{min}$ to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		Volts
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1.0			2.0			1.0		MHz
Full Power Response		50			200			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**8.0**	13.0		**2.0**	3.0		V/μs
Total Harmonic Distortion					0.0025					%
INPUT OFFSET VOLTAGE[2]										
J			**2.0**			**2.0**			**1.0**	mV
K			**1.0**			**1.0**			**0.5**	mV
L			**0.5**			**0.5**			**0.25**	mV
S			**1.0**			**1.0**			**0.5**	mV
vs. Temperature[3]										
J			20			20			5	μV/°C
K			**10**			**10**			**2**	μV/°C
L			5			5			1	μV/°C
S			15			15			5	μV/°C
vs. Supply, $T_A = T_{min}$ to T_{max}										
J			200			200			**200**	μV/V
K, L, S			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[4]										
Either Input										
J			**50**			**50**			**50**	pA
K, L, S		10	**25**		10	**25**		10	**25**	pA
Input Offset Current										
J		5	**15**		5	**15**		5	**15**	pA
K, L, S		2	**15**		2	**15**		2	**15**	pA
INPUT IMPEDANCE										
Differential		$10^{12}\Omega \| 6pF$			$10^{12}\Omega \| 6pF$			$10^{12}\Omega \| 6pF$		
Common Mode		$10^{12}\Omega \| 3pF$			$10^{12}\Omega \| 3pF$			$10^{12}\Omega \| 3pF$		
INPUT VOLTAGE[5]										
Differential		±20			±20			±20		Volts
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		Volts
Common-Mode Rejection										
$V_{IN} = \pm 10V$										
J	**76**			**76**			**76**			dB
K, L, S	**80**			**80**			**80**			dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		Volts
Operating	±5		**±18**	±5		**±18**	±5		**±18**	Volts
Quiescent Current		1.1	**1.5**		1.8	**2.5**		1.1	**1.5**	mA
VOLTAGE NOISE										
0.1–10Hz										
J		2.0			2.0			2.0		μV p-p
K, L, S		2.0			2.0				**4.0**	μV p-p
10Hz		70			35			70		$nV/\sqrt{Hz}$
100Hz		45			22			45		$nV/\sqrt{Hz}$
1kHz		30			18			30		$nV/\sqrt{Hz}$
10kHz		25			16			25		$nV/\sqrt{Hz}$
TEMPERATURE RANGE										
Operating, Rated Performance										
J, K, L		0 to +70			0 to +70			0 to +70		°C
S		−55 to +125			−55 to +125			−55 to +125		°C
Storage		−65 to +150			−65 to +165			−65 to +165		°C
TRANSISTOR COUNT	29			29			29			
PACKAGE OPTIONS[6]										
TO-99 (H-08A)	AD542JH, AD542KH AD542LH, AD542SH			AD544JH, AD544KH AD544LH, AD544SH			AD547JH, AD547KH AD547LH, AD547SH			

NOTES
[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of nulled offset.
[4]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.
[6]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

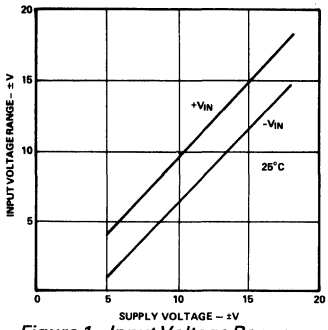


Figure 1. Input Voltage Range vs. Supply Voltage

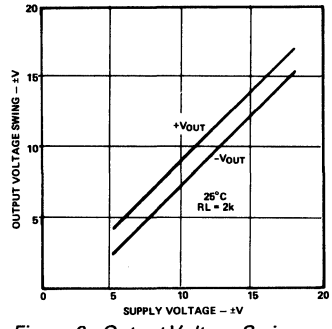


Figure 2. Output Voltage Swing vs. Supply Voltage

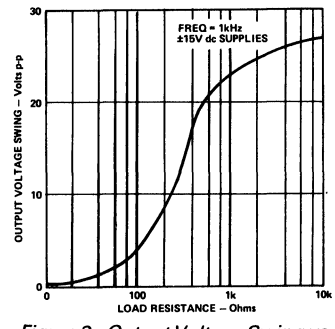


Figure 3. Output Voltage Swing vs. Load Resistance

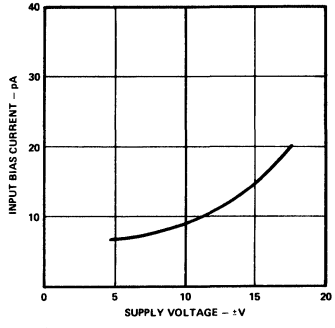


Figure 4. Input Bias Current vs. Supply Voltage

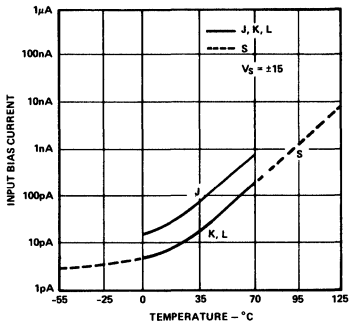


Figure 5. Input Bias Current vs. Temperature

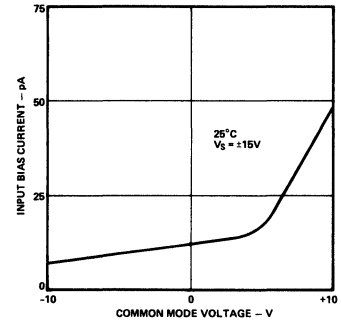


Figure 6. Input Bias Current vs. CMV

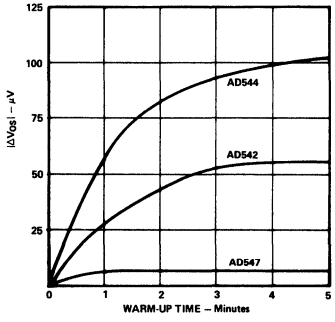


Figure 7. Change in Offset Voltage vs. Warm-Up Time

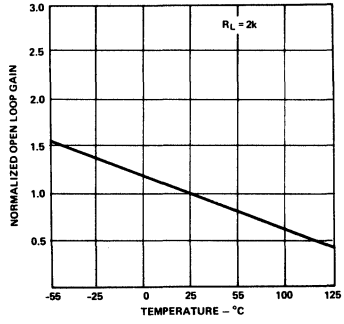


Figure 8. Open Loop Gain vs. Temperature

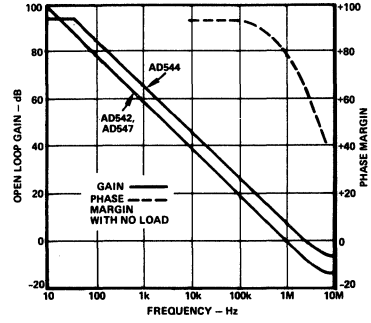


Figure 9. Open Loop Frequency Response

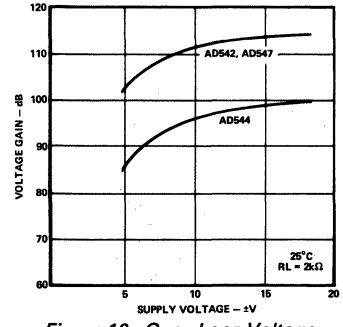


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

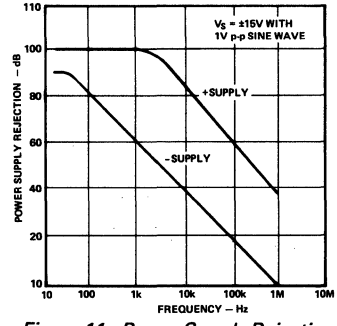


Figure 11. Power Supply Rejection vs. Frequency

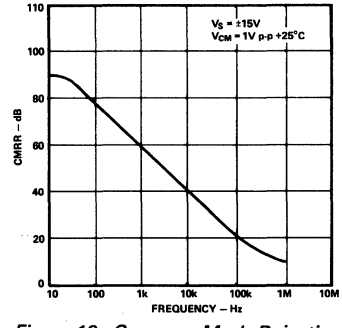


Figure 12. Common Mode Rejection Ratio vs. Frequency

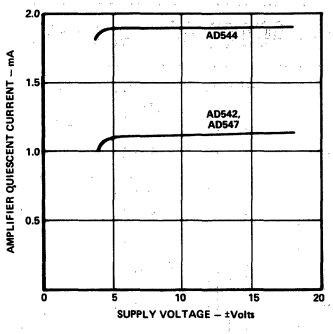


Figure 13. Quiescent Current vs. Supply Voltage

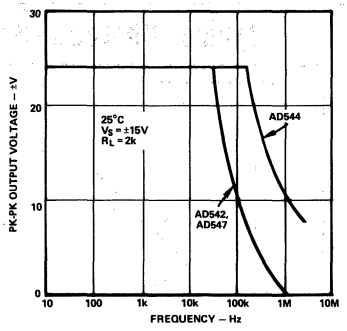


Figure 14. Large Signal Frequency Response

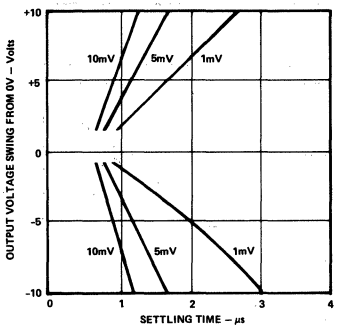


Figure 15. AD544 Output Swing and Error vs. Settling Time

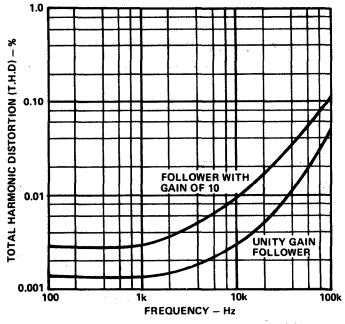


Figure 16. AD544 Total Harmonic Distortion vs. Frequency

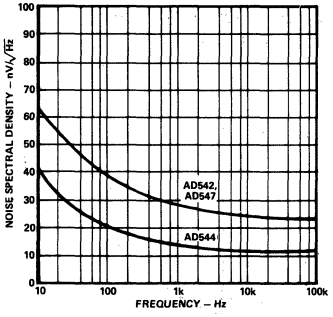


Figure 17. Input Noise Voltage Spectral Density

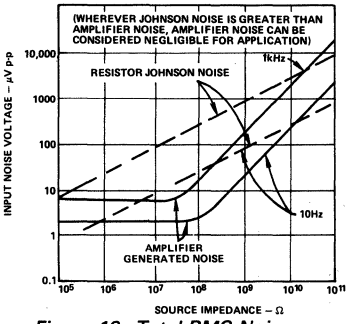
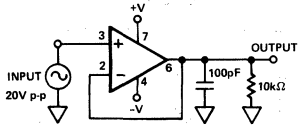
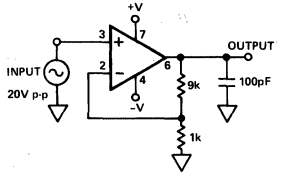


Figure 18. Total RMS Noise vs. Source Impedance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

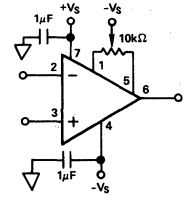


Figure 20. Standard Null Circuit

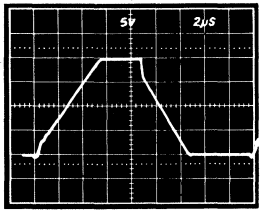


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

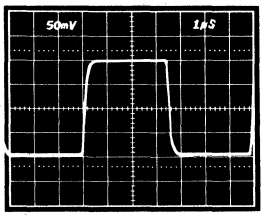


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

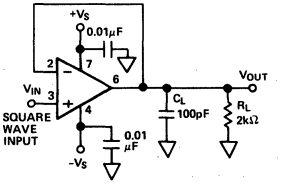


Figure 21c. Unity Gain Follower– AD542/AD547

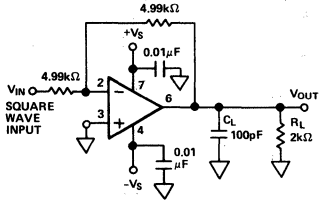


Figure 22a. Unity Gain Inverter– AD542/AD547

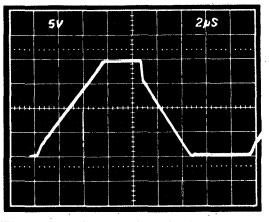


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

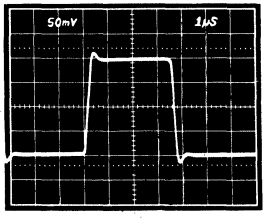


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

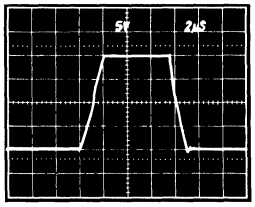


Figure 23a. Unity Gain Follower Pulse Response (Large Signal)

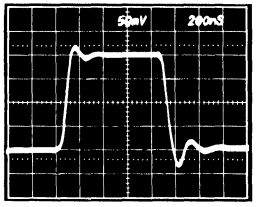


Figure 23b. Unity Gain Follower Pulse Response (Small Signal)

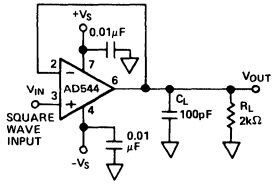


Figure 23c. Unity Gain Follower

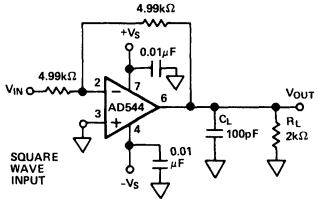


Figure 24a. Unity Gain Inverter

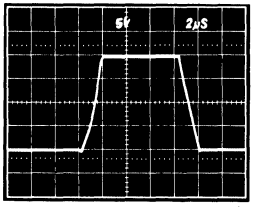


Figure 24b. Unity Gain Inverter Pulse Response (Large Signal)

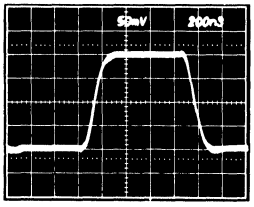


Figure 24c. Unity Gain Inverter Pulse Response (Small Signal)

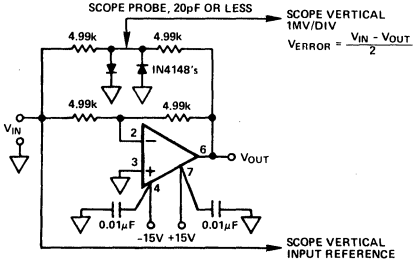


Figure 25. Settling Time Test Circuit

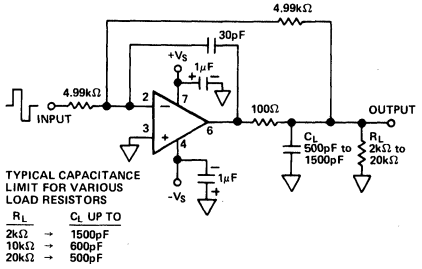


Figure 27. Circuit for Driving a Large Capacitance Load

The upper trace of the oscilloscope photograph of Figure 26 shows the settling characteristic of the AD544. The lower trace represents the input to Figure 27. The AD544 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

The circuit in Figure 27 employs a 100Ω isolation resistor which enables the amplifier to drive capacitance loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

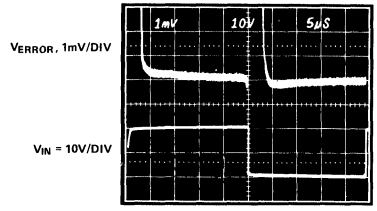


Figure 26. Settling Characteristic Detail – AD544

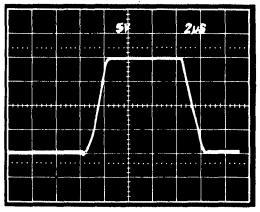


Figure 28. Transient Response $R_L = 2k\Omega$ $C_L = 500pF$–AD544

ORDERING GUIDE

Model	Initial Offset Voltage	Offset Voltage Drift	Settling Time to ±0.012% for 10V Step
AD542JH	2.0mV	20μV/°C	5μs
AD542KH	1.0mV	10μV/°C	5μs
AD542LH	0.5mV	5μV/°C	5μs
AD542SH	1.0mV	15μV/°C	5μs
AD547JH	1.0mV	5μV/°C	5μs
AD547KH	0.5mV	2μV/°C	5μs
AD547LH	0.25mV	1μV/°C	5μs
AD547SH	0.5mV	5μV/°C	5μs
AD544JH	2.0mV	20μV/°C	3μs
AD544KH	1.0mV	10μV/°C	3μs
AD544LH	0.5mV	5μV/°C	3μs
AD544SH	1.0mV	15μV/°C	3μs

BiFET Application Hints

APPLICATION NOTES

The BiFET series was designed for high performance op-amp applications that require true dc precision. To capitalize on all of the performance available from the BiFETs there are some practical error sources that should be considered.

The bias currents of JFET input amplifiers double with every 10°C increase in chip temperature. Therefore, minimizing the junction temperature of the chip will result in extending the performance limits of the device.

1. Heat dissipation due to power consumption is the main contributor to self-heating and can be minimized by reducing the power supplies to the lowest level allowed by the application.
2. The effects of output loading should be carefully considered. Greater power dissipation increases bias currents and decreases open loop gain.

GUARDING

The low input bias current (25pA) and low noise characteristics of the high performance BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance available from these amplifiers. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit.

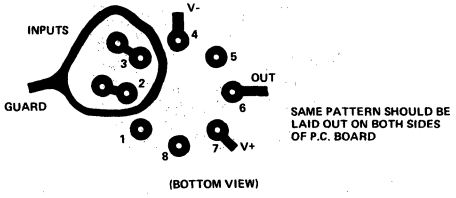


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The BiFET series is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±1 volt while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the BiFET series suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The BiFET series requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.

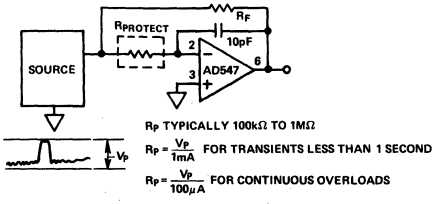


Figure 30. Input Protection

D/A CONVERTER APPLICATIONS

The BiFET series of operational amplifiers can be used with CMOS DACs to perform both 2-quadrant and 4-quadrant operation. The output impedance of a CMOS DAC varies with the digital word, thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The BiFET series with trimmed offset will minimize this effect. Additionally, the Schottky protection diodes recommended for use with many older CMOS DACs are not required when using one of the BiFET series amplifiers.

Figure 31a shows the AD547 and AD7541 configured for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at pin 17, the circuit operates as a unipolar converter. With an ac reference voltage or current, the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

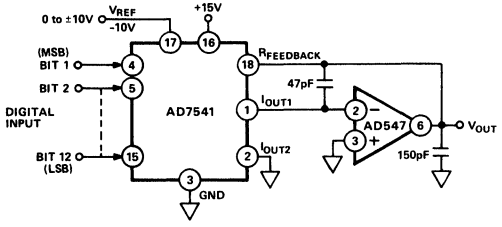


Figure 31a. AD547 Used as DAC Output Amplifier

The oscilloscope photo of Figure 31b shows the output of the circuit of Figure 31a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC (Gain $1-2^{-n}$). The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

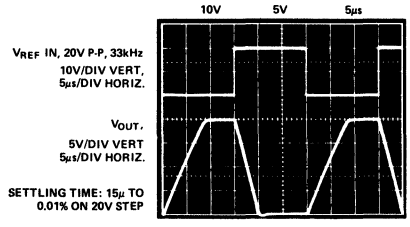


Figure 31b. Voltage Output DAC Settling Characteristic

Figure 32a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function.

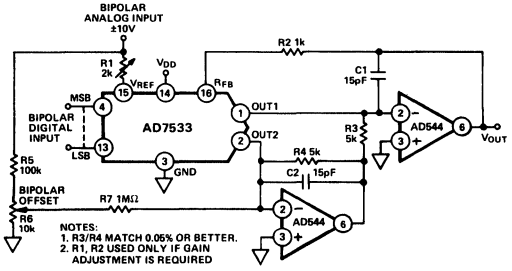


Figure 32a. AD544 Used as DAC Output Amplifiers

The photos exhibit the response to a step input at V_{REF}. Figure 32b is the large signal response and Figure 32c is the small signal response. C1 phase compensation (15pF) is required for stability when using high speed amplifiers. C1 is used to cancel the pole formed by the DAC internal feedback resistance and the output capacitance of the DAC.

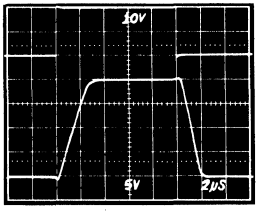


Figure 32b. Large Signal Response

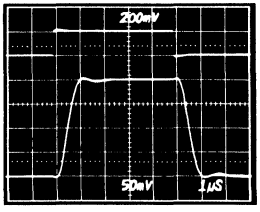


Figure 32c. Small Signal Response

USING THE AD547 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbence as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD547 make it suitable for wide dynamic range log amplifiers. Figure 33 is a schematic of a log ratio circuit employing the AD547 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100µA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

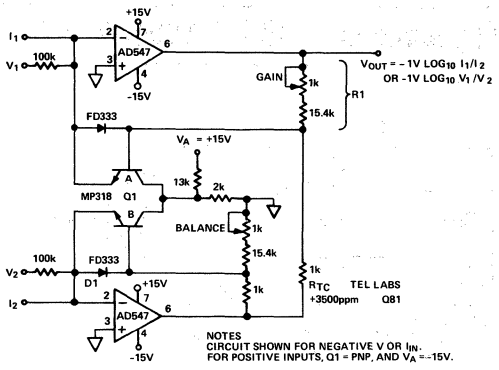


Figure 33. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{Kkt}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\ kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The −3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = −10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = −10.00V, V2 = −1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

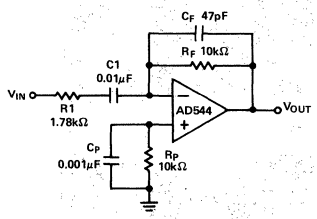


Figure 34. Differentiator

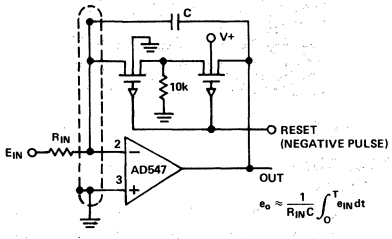


Figure 35. Low Drift Integrator and Low-Leakage Guarded Reset

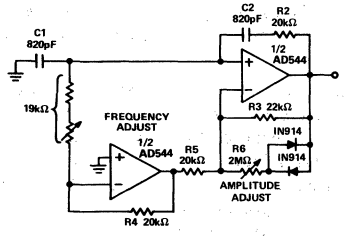


Figure 36. Wien-Bridge Oscillator – f_o = 10kHz

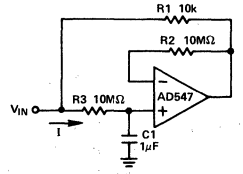


Figure 37. Capacitance Multiplier

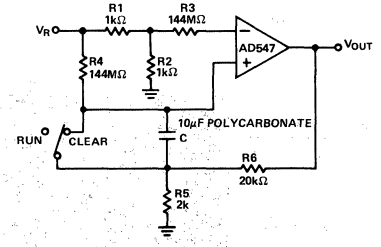


Figure 38. Long Interval Timer – 1,000 Seconds

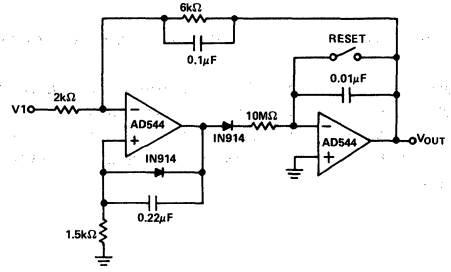


Figure 39. Positive Peak Detector

ANALOG DEVICES

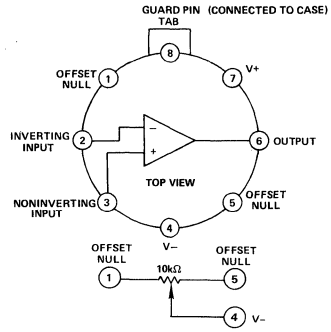
Monolithic Precision, Low Drift FET-Input Op Amp

AD545A*

FEATURES

Low Offset Voltage: 0.5mV max (AD545AL)
0.25mV max (AD545AM)
Low Offset Voltage Drift: 5μV/°C max (AD545AL),
3μV/°C max (AD545AM)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545AK, L, M)
Low Noise: 3μV p-p, 0.1Hz to 10Hz

AD545A PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD545A is a monolithic precision FET-input operational amplifier. It is a successor to the AD545 and will replace the AD545 in most applications. Bias current is specified as 2pA max for the AD545AJ and 1pA max for the AD545AK, L and M. Offset voltage is laser trimmed to 0.5mV max for the AD545AL, 0.25mV max for the AD545AM. All devices also feature low voltage noise and power consumption. The AD545A is internally compensated, short circuit protected and free of latch-up.

The AD545A series offers a broad combination of performance features. For precision applications the AD545AM specifies a 0.25mV max offset voltage, 3μV/°C max drift and 1pA max bias current. The AD545AJ, with a 1mV max offset voltage, 25μV/°C max drift and 2pA max bias current, is the best price performance choice.

These devices are recommended for a variety of general purpose and precision applications requiring low bias currents and high input impedance such as pH/pIon sensitive electrodes, photocurrent detectors, biological microprobes, long-term precision integrators and vacuum ion gage measurements. The versatility of the AD545A is further enhanced by its excellent low frequency noise (3μV p-p, 0.1Hz to 10Hz) and low power consumption (1.5mA max) for portable applications.

As with previous electrometer amplifier designs from Analog Devices, the case is guarded thus minimizing stray leakage. This feature will also shield the input circuitry from external noise and supply transients.

The AD545A is available in four versions of bias current and offset voltage, the "J", "K", "L", and "M." All are specified from 0 to +70°C and supplied in a hermetically sealed TO-99 package. The hybrid version, AD545, will also be available.

***Covered by U.S. Patent No. 4,639,683.**

PRODUCT HIGHLIGHTS

1. The offset voltage on the AD545A is laser trimmed to a level typically less than 250μV. Offset voltage drift is only 3μV/°C max for the AD545AM. If additional external nulling is desired, the effect on drift is minimal (approximately 2.5μV/°C mV, nulled).
2. Bias current is specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient.
3. The low quiescent current drain of 0.6mA typical, and 1.5mA max keeps self-heating to a minimum.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one MΩ up to $10^{11}\Omega$, the Johnson noise of the source will easily dominate the noise characteristics.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

Model	AD545AJ	AD545AK	AD545AL	AD545AM
OPEN LOOP GAIN[1]				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	**20,000V/V min**	**40,000V/V min**	**40,000V/V min**	**40,000V/V min**
$R_L \geq 10k\Omega$	**40,000V/V min**	**50,000V/V min**	**50,000V/V min**	**50,000V/V min**
T_A = min to max $R_L \geq 2k\Omega$	**15,000V/V min**	**25,000V/V min**	**40,000V/V min**	**40,000V/V min**
OUTPUT CHARACTERISTICS				
Voltage@R_L = 2kΩ, T_A = min to max	**±10V min (±12V typ)**	*	*	*
@R_L = 10kΩ, T_A = min to max	**±12V min (±13V typ)**	*	*	*
Load Capacitance[2]	500pF	*	*	*
Short Circuit Current	**10mA min (20mA typ)**	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1MHz	*	*	*
Full Power Response	5kHz min (30kHz typ)	*	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (2.0V/μs typ)	*	*	*
Overload Recovery Inverting Unity Gain	100μs max (2μs typ)	*	*	*
INPUT OFFSET VOLTAGE[3]	**1.0mV max**	**1.0mV max**	**0.5mV max**	**0.25mV max**
vs. Temperature, T_A = min to max	**25μV/°C max**	**15μV/°C max**	**5μV/°C max**	**3μV/°C max**
vs. Supply, T_A = min to max	**400μV/V max (50μV/V typ)**	**200μV/V max**	**200μV/V max**	**200μV/V max**
INPUT BIAS CURRENT				
Either Input[4]	**2pA max**	**1pA max**	**1pA max**	**1pA max**
INPUT IMPEDANCE				
Differential V_{IN} = ±1V	1.6pF‖$10^{13}\Omega$	*	*	*
Common Mode	0.8pF‖$10^{15}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	3.0μV (p-p)	*	*	**5μV (p-p) max**
f = 10Hz	55nV/$\sqrt{Hz}$	*	*	*
f = 100Hz	45nV/$\sqrt{Hz}$	*	*	*
f = 1kHz	35nV/$\sqrt{Hz}$	*	*	*
Current, 0.1Hz to 10Hz	0.03pA (p-p)	*	*	*
10Hz to 10kHz	0.05pA rms	*	*	*
INPUT VOLTAGE RANGE				
Differential	±20V min	*	*	*
Common Mode, T_A = min to max	±10V min	*	*	*
Common-Mode Rejection, V_{IN} = ±10V	**66dB min (80dB typ)**	**70dB min**	**76dB min**	**76dB min**
Maximum Safe Input Voltages[5]	±V_S	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	**±5V min (±18V max)**	*	*	*
Quiescent Current	**1.5mA max (0.6mA typ)**	*	*	*
TEMPERATURE				
Operating, Rated Performance	0 to +70°C	*	*	*
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTION[6]	H-08A	*	*	*

NOTES

*Specifications same as AD545AJ.

[1]Open Loop Gain is specified with or without nulling of V_{OS}.

[2]A conservative design would not exceed 500pF of load capacitance.

[3]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4]Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.

[5]If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.1mA. The input devices can handle overload currents of 0.1mA indefinitely without damage.

[6]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final test.

LAYOUT AND CONNECTIONS CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading.
2. The use of guarding techniques is essential to realizing the capability of the low input currents of the AD545A. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves an additional function of reducing the effective capacitance to the input line. The case of the AD545A is brought out separately to Pin 8 so that it can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.8pF. Figure 10 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and noninverting applications. If Pin 8 is not used for guarding, it should be connected to ground or one of the amplifier's power supplies to reduce noise.
3. Printed circuit board layout and construction is critical for achieving low leakage performance. The best performance will be realized by using a teflon IC socket for the AD545A but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 10 will minimize leakage as much as possible and should be applied to both sides of the board.

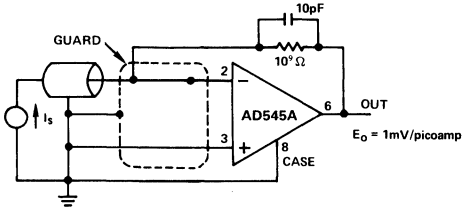


Figure 1. Picoampere Current-to-Voltage Converter Inverting Configuration

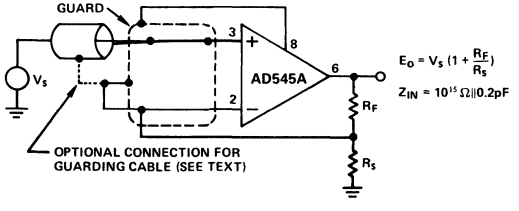


Figure 2. Very High Impedance Noninverting Amplifier

The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

APPLICATION NOTES

The AD545A offers one of the lowest input bias currents available in an integrated circuit package. Performing accurate measurements with this device requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD545A and extending its performance limits.

1. As with all junction FET input devices, the temperature of the FETs themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if possible, reduce the required voltage power supplies, since internal power consumption contributes the largest component of self-heating. The effects of this are shown in Figure 7, which shows typical input bias current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10V at the output will cause at least an additional 25mW dissipation in the output stage (and some in other stages) over the typical 24mW, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated (it doubles every 10°C); we recommend restricting the load impedance to be at least 10kΩ.
4. Figure 8 shows the AD545A's input currents versus differential input voltage. Input current at either terminal stays below a few hundred fA until one input terminal is forced higher than 1V to 1.5V above the other terminal. Input current limits at 30μA under these conditions.

Typical Performance Curves

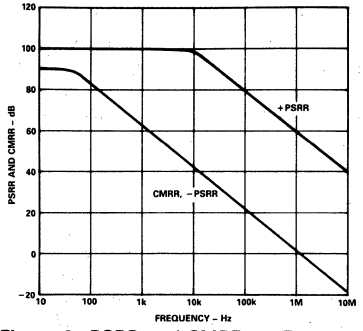


Figure 3. PSRR and CMRR vs. Frequency

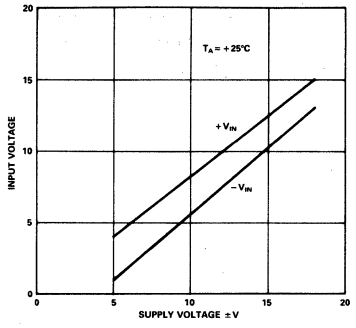


Figure 4. Input Common-Mode Range vs. Supply Voltage

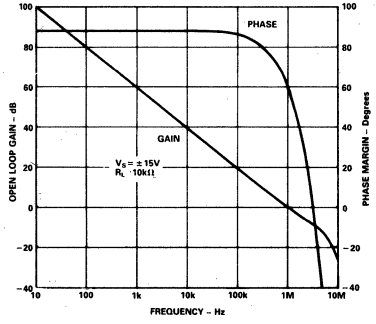


Figure 5. Open Loop Frequency Response

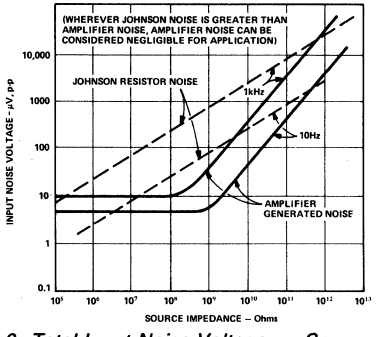


Figure 6. Total Input Noise Voltage vs. Source Impedance and Bandwidth

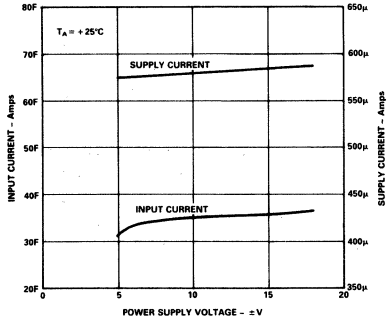


Figure 7. Input Bias Current and Supply Current vs. Supply Voltage

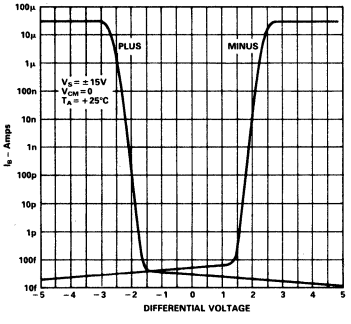


Figure 8. Input Bias Current vs. Differential Input Voltage

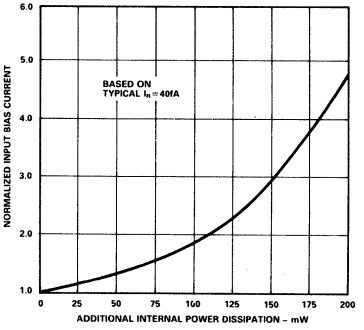


Figure 9. Input Bias Current vs. Additional Power Dissipation

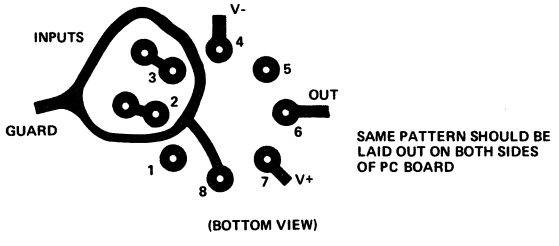


Figure 10. Board Layout for Guarding Inputs with Guarded TO-99 Package

1 pA Monolithic Electrometer Operational Amplifier

AD546*

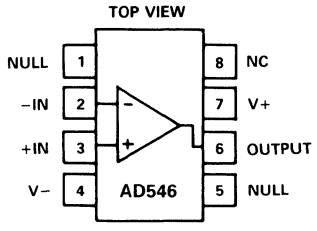
FEATURES
DC PERFORMANCE
1 mV max Input Offset Voltage
Low Offset Drift: 20 μV/°C
1 pA max Input Bias Current
Input Bias Current Guaranteed Over Full Common Mode Voltage Range

AC PERFORMANCE
3 V/μs Slew Rate
1 MHz Unity Gain Bandwidth
Low Input Voltage Noise: 4 μV p–p, 0.1 Hz to 10 Hz
Available in a Low Cost, 8-Pin Plastic Mini-DIP
Standard Op Amp Pinout

APPLICATIONS
Electrometer Amplifiers
Photodiode Preamps
pH Electrode Buffers
Log Ratio Amplifiers

AD546 CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD546 is a monolithic electrometer combining the virtues of low (1 pA) input bias current with the cost effectiveness of a plastic mini-DIP package. Both input offset voltage and input offset voltage drift are laser trimmed, providing very high performance for such a low cost amplifier.

Input bias currents are reduced significantly by using "topgate" JFET technology. The 10^{15} Ω common mode impedance, resulting from a bootstrapped input stage, insures that input bias current is essentially independent of common mode voltage variations.

The AD546 is suitable for applications requiring both minimal levels of input bias current and low input offset voltage. Applications for the AD546 include use as a buffer amplifier for current output transducers such as photodiodes and pH probes. It may also be used as a precision integrator or as a low droop rate sample and hold amplifier. The AD546 is pin compatible with standard op amps; its plastic mini-DIP package is ideal for use with automatic insertion equipment.

The AD546 is available in two performance grades, all rated over the 0 to +70°C commercial temperature range, and packaged in an 8-pin plastic mini-DIP.

PRODUCT HIGHLIGHTS

1. The input bias current of the AD546 is specified, 100% tested and guaranteed with the device in the fully warmed-up condition.
2. The input offset voltage of the AD546 is laser trimmed to less than 1 mV (AD546K).
3. The AD546 is packaged in a standard, low cost, 8-pin mini-DIP.
4. A low quiescent supply current of 700 μA minimizes any thermal effects which might degrade input bias current and input offset voltage specifications.

*Covered by Patent No. 4,639,683

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD546J Min	AD546J Typ	AD546J Max	AD546K Min	AD546K Typ	AD546K Max	Units
INPUT BIAS CURRENT[1]								
Either Input	V_{CM} = 0 V		0.2	**1**		0.2	**0.5**	pA
Either Input	V_{CM} = ±10 V		0.2	1		0.2	0.5	pA
Either Input @ T_{max}	V_{CM} = 0 V		40			20		pA
Either Input	V_{CM} = ±10 V		40			20		pA
Offset Current	V_{CM} = 0 V		0.17			0.09		pA
Offset Current @ T_{max}	V_{CM} = 0 V		13			7		pA
INPUT OFFSET VOLTAGE[2]								
Initial Offset				**2**			**1**	mV
Offset @ T_{max}				3			2	mV
vs. Temp.			20			20		μV/°C
vs. Supply				**100**			**100**	μV/V
vs. Supply	T_{min}–T_{max}			100			100	μV/V
Long Term Stability			20			20		μV/month
INPUT VOLTAGE NOISE								
	f = 0.1 Hz to 10 Hz		4			4		μV p-p
	f = 10 Hz		90			90		nV/√Hz
	f = 100 Hz		60			60		nV/√Hz
	f = 1 kHz		35			35		nV/√Hz
	f = 10 kHz		35			35		nV/√Hz
INPUT CURRENT NOISE								
	f = 0.1 Hz to 10 Hz		1.3			1.3		fA rms
	f = 1 kHz		0.4			0.4		fA/√Hz
INPUT IMPEDANCE								
Differential	V_{DIFF} = ±1 V		10^{13}‖1			10^{13}‖1		Ω‖pF
Common Mode	V_{CM} = ±10 V		10^{15}‖0.8			10^{15}‖0.8		Ω‖pF
OPEN LOOP GAIN	V_O = ±10 V, R_{LOAD} = 10 kΩ	**300**	1000		**300**	1000		V/mV
T_{min}–T_{max}	V_O = ±10 V, R_{LOAD} = 10 kΩ	300	800		300	800		V/mV
	V_O = ±10 V, R_{LOAD} = 2 kΩ	**100**	250		**100**	250		V/mV
T_{min}–T_{max}	V_O = ±10 V, R_{LOAD} = 2 kΩ	80	200		80	200		V/mV
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common Mode Voltage		**−10**		**+10**	**−10**		**+10**	V
Common Mode Rejection Ratio	V_{CM} = ±10 V	**80**	90		**84**	100		dB
	T_{min} to T_{max}	76	80		76	80		dB
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD} = 10 kΩ	**−12**		**+12**	**−12**		**+12**	V
	R_{LOAD} = 2 kΩ	**−10**		**+10**	**−10**		**+10**	V
Current	Short Circuit	**15**	20	35	**15**	20	35	mA
Load Capacitance Stability	Gain = +1		4000			4000		pF

Model	Conditions	AD546J Min	AD546J Typ	AD546J Max	AD546K Min	AD546K Typ	AD546K Max	Units
FREQUENCY RESPONSE								
Gain BW, Small Signal	G = −1	0.7	1.0		0.7	1.0		MHz
Full Power Response	V_O = 20 V p-p		50			50		kHz
Slew Rate, Unity Gain	G = −1	2	3		2	3		V/μs
Settling Time	to 0.1%		4.5			4.5		μs
	to 0.01%		5			5		μs
Overload Recovery	50% Overdrive Gain = −1		2			2		μs
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±5		±18	±5		±18	V
Quiescent Current			0.60	0.7		0.60	0.7	mA
Transistor Count	# of Transistors		50			50		
PACKAGE OPTIONS[4]								
Plastic Mini-DIP (N-8)		AD546JN			AD546KN			

NOTES
[1]Bias current specifications are guaranteed maximum, at either input, after 5 minutes of operation at T_A = +25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.
[2]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[3]Defined as max continuous voltage between inputs, such that neither exceeds ±10 V from ground.
[4]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 500 mW
Input Voltage[2] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range . . . . . −65°C to +125°C
Operating Temperature Range . . . . . 0 to +70°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ESD PRECAUTIONS

Charges as high as 4000 V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

Typical Characteristics (V_S = ±15 V, unless otherwise specified)

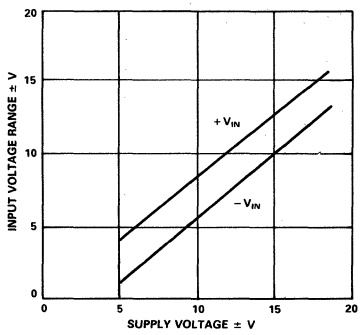


Figure 1. Input Voltage Range vs. Supply Voltage

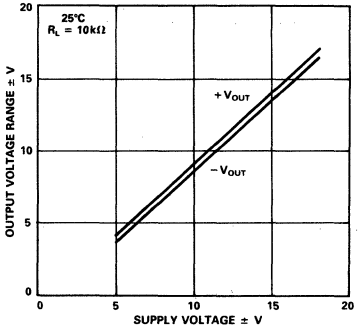


Figure 2. Output Voltage Range vs. Supply Voltage

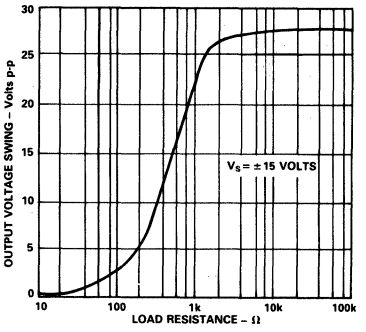


Figure 3. Output Voltage Swing vs. Load Resistance

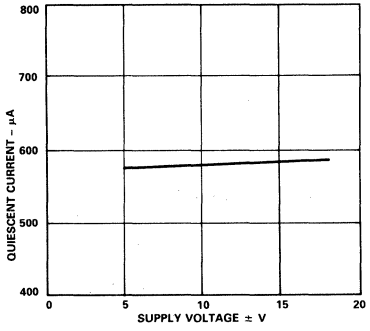


Figure 4. Quiescent Current vs. Supply Voltage

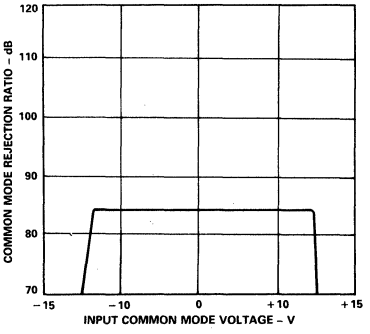


Figure 5. CMRR vs. Input Common Mode Voltage

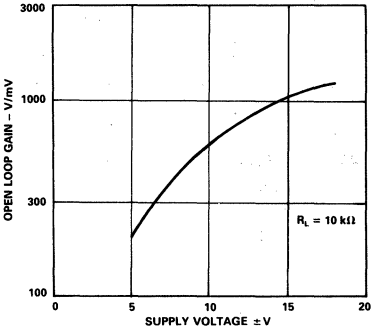


Figure 6. Open Loop Gain vs. Supply Voltage

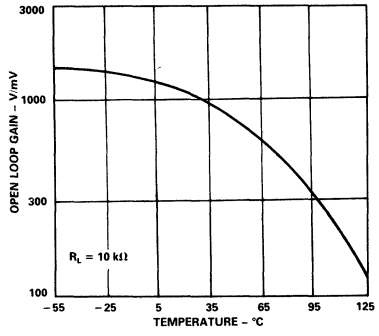


Figure 7. Open Loop Gain vs. Temperature

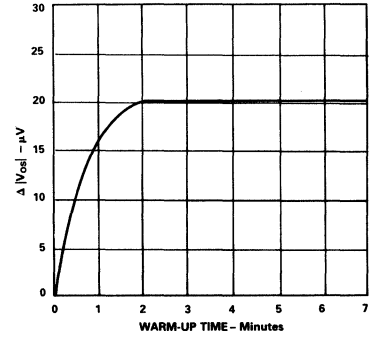


Figure 8. Change in Offset Voltage vs. Warm-Up Time

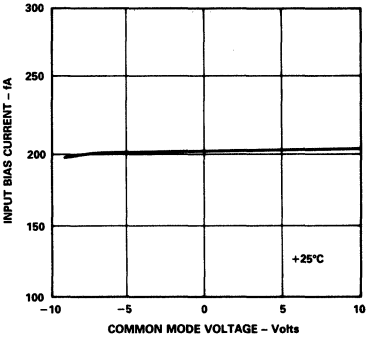


Figure 9. Input Bias Current vs. Common Mode Voltage

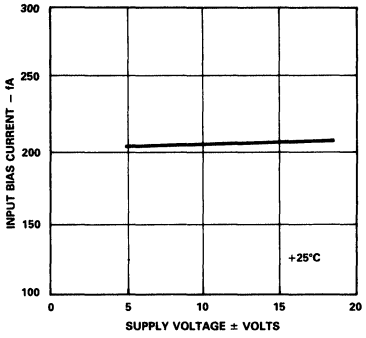


Figure 10. Input Bias Current vs. Supply Voltage

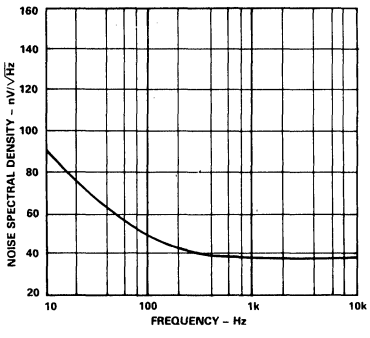


Figure 11. Input Voltage Noise Spectral Density vs. Frequency

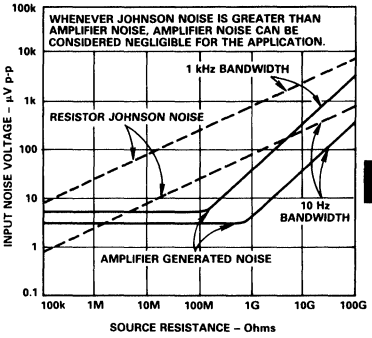


Figure 12. Noise vs. Source Resistance

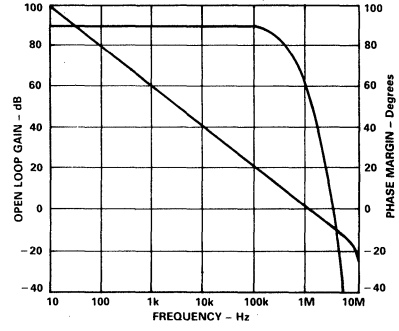


Figure 13. Open Loop Frequency Response

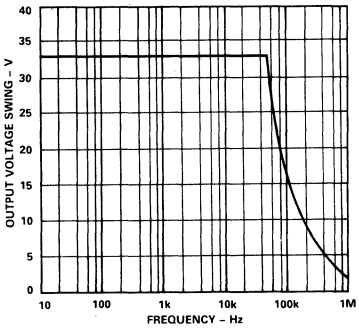


Figure 14. Large Signal Frequency Response

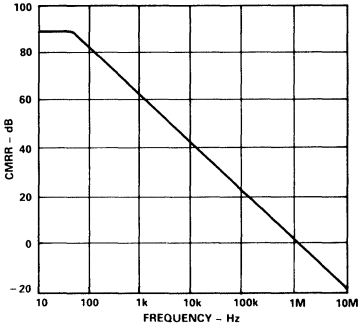


Figure 15. CMRR vs. Frequency

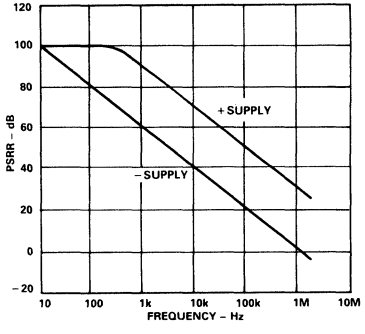


Figure 16. PSRR vs. Frequency

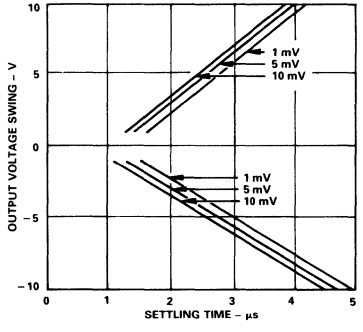


Figure 17. Output Swing and Error Voltage vs. Output Settling Time

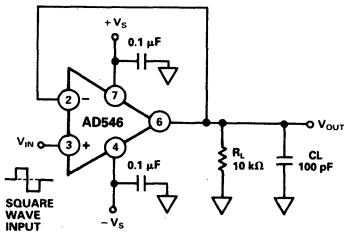


Figure 18. Unity Gain Follower

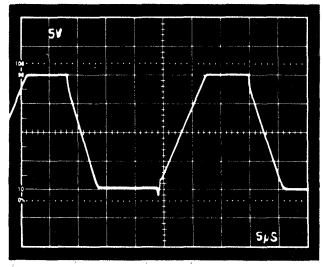


Figure 19. Unity Gain Follower Large Signal Pulse Response

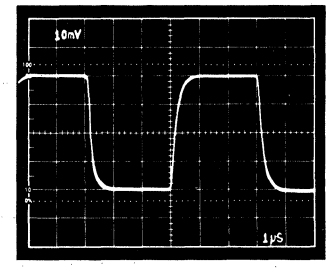


Figure 20. Unity Gain Follower Small Signal Pulse Response

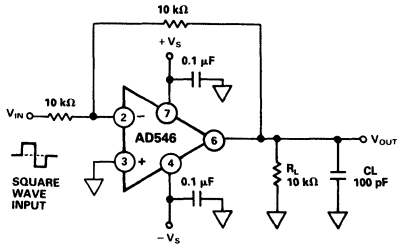


Figure 21. Unity Gain Inverter

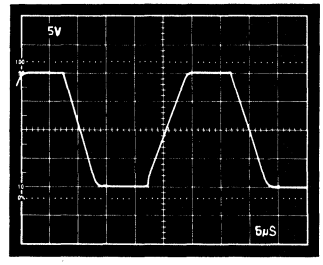


Figure 22. Unity Gain Inverter Large Signal Pulse Response

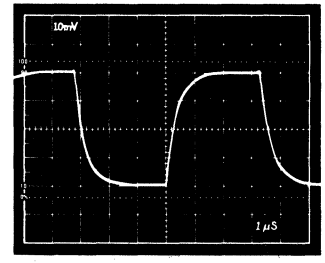


Figure 23. Unity Gain Inverter Small Signal Pulse Response

MINIMIZING INPUT CURRENT

The AD546 is guaranteed to have less than 1 pA max input bias current at room temperature. Careful attention to how the amplifier is used will reduce input currents in actual applications.

The amplifier operating temperature should be kept as low as possible to minimize input current. Like other JFET input amplifiers, the AD546's input current is sensitive to chip temperature, rising by a factor of 2.3 for every 10°C rise. This is illustrated in Figure 24, a plot of AD546 input current versus ambient temperature.

On-chip power dissipation will raise chip operating temperature causing an increase in input bias current. Due to the AD546's low quiescent supply current, chip temperature when the (unloaded) amplifier is operated with 15 V supplies, is less than 3°C higher than ambient. The difference in input current is negligible.

However, heavy output loads can cause a significant increase in chip temperature and a corresponding increase in input current. Maintaining a minimum load resistance of 10kΩ is recommended. Input current versus additional power dissipation due to output drive current is plotted in Figure 25.

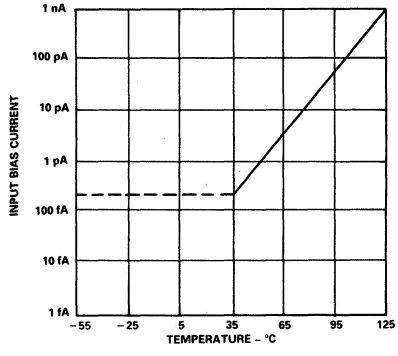


Figure 24. AD546 Input Bias Current vs. Ambient Temperature

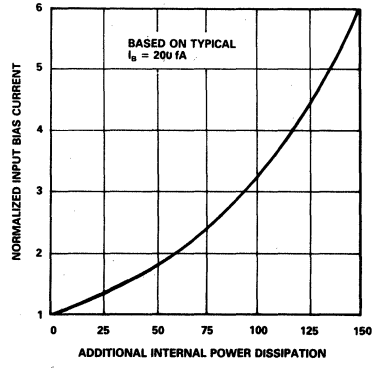


Figure 25. AD546 Input Bias Current vs. Additional Power Dissipation

Circuit Board Notes

The AD546 is designed for through hole mount into PC boards. Maintaining picoampere level resolution in that environment requires a lot of care. Since both the printed circuit board and the amplifier's package have a finite resistance, the voltage difference between the amplifier's input pin and other pins (or traces on the PC board) will cause parasitic currents to flow into (or out of) the signal path (see Figure 26). These currents can easily exceed the 1 pA input current level of the AD546 unless special precautions are taken. Two successful methods for minimizing leakage are guarding the AD546's input lines and maintaining adequate insulation resistance.

The AD546's positive input (Pin 3) is located next to the negative supply voltage pin (Pin 4). The negative input (Pin 2) is next to the balance adjust pin (Pin 1) which is biased at a potential close to the negative supply voltage. The layouts shown in Figures 27a and 27b for the inverter and follower connections will guard against the effects of low surface resistance of the board. Note that the guard traces should be placed on *both* sides of the board. In addition the input trace should be guarded on both of its edges along its entire length.

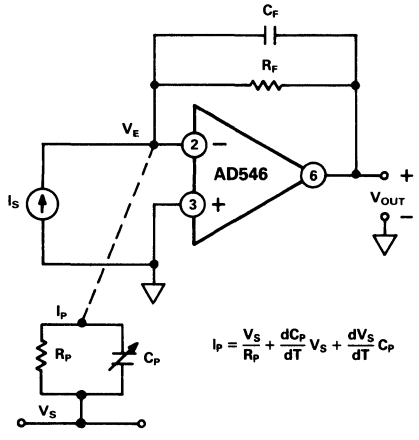
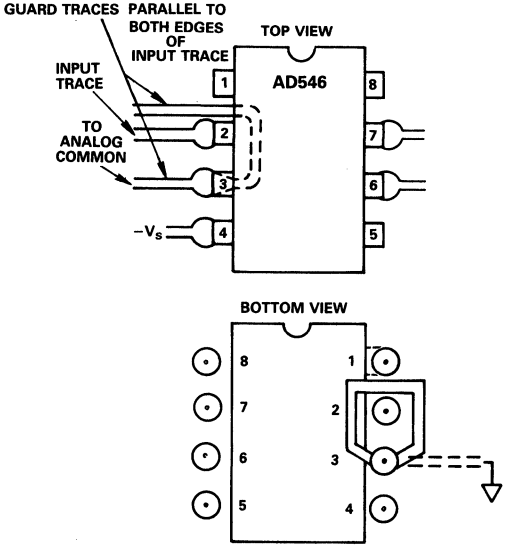


Figure 26. Sources of Parasitic Leakage Currents



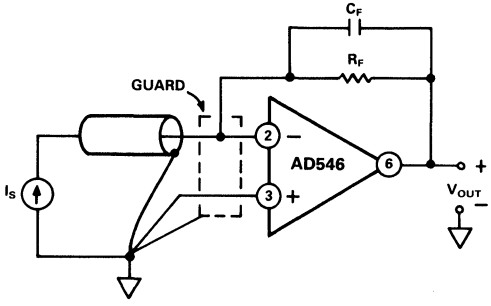


Figure 27a. Guarding Scheme—Inverter

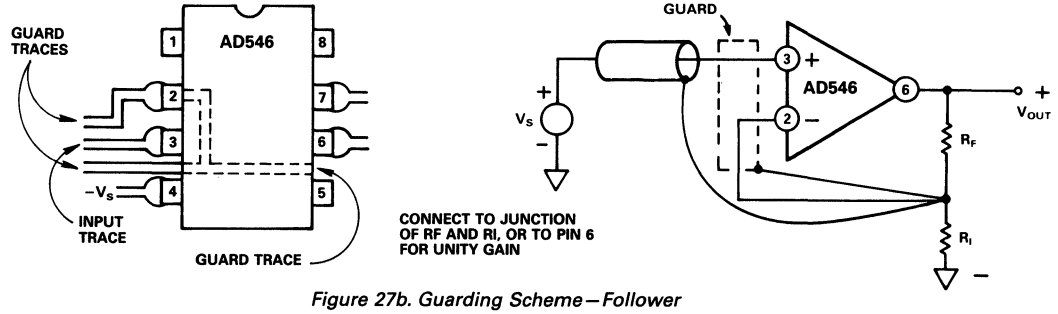


Figure 27b. Guarding Scheme—Follower

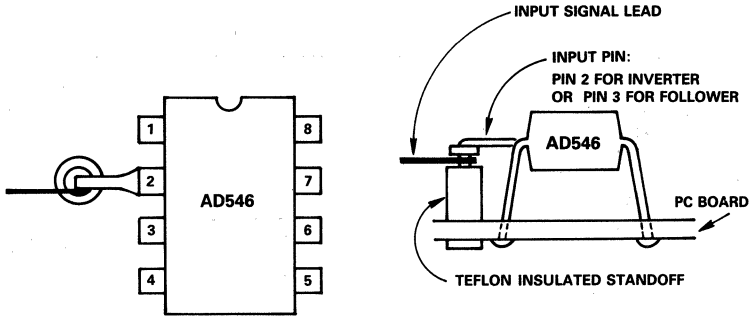


Figure 28. Input Pin to Insulating Standoff

Leakage through the bulk of the circuit board will still occur with the guarding schemes shown in Figures 27a and 27b. Standard "G10" type printed circuit board material may not have high enough volume resistivity to hold leakages at the sub-picoampere level particularly under high humidity conditions. One option that eliminates all effects of board resistance is shown in Figure 28. The AD546's sensitive input pin (either Pin 2 when connected as an inverter, or Pin 3 when connected as a follower) is bent up and soldered directly to a Teflon* insulated standoff. Both the signal input and feedback component leads must also be insulated from the circuit board by Teflon standoffs or low-leakage shielded cable.

Contaminants such as solder flux on the board's surface and on the amplifier's package can greatly reduce the insulation resistance between the input pin and those traces with supply or signal voltages. Both the package and the board must be kept clean and dry. An effective cleaning procedure is to first swab the surface with high grade isopropyl alcohol, then rinse it with deionized water and, finally, bake it at 80°C for 1 hour. Note that if either polystyrene or polypropylene capacitors are used on the printed circuit board, a baking temperature of 70°C is safer, since both of these plastic compounds begin to melt at approximately +85°C.

Other guidelines include making the circuit layout as compact as possible and reducing the length of input lines. Keeping circuit board components rigid and minimizing vibration will reduce triboelectric and piezoelectric effects. All precision high impedance circuitry requires shielding from electrical noise and interference. For example, a ground plane should be used under all high value (i.e., greater than 1 MΩ) feedback resistors. In some cases, a shield placed over the resistors, or even the entire amplifier, may be needed to minimize electrical interference originating from other circuits. Referring to the equation in Figure 26, this coupling can take place in either, or both, of two different forms—coupling via time varying fields:

$$\frac{dV}{dT} C_P$$

or by injection of parasitic currents by changes in capacitance due to mechanical vibration:

$$\frac{dCp}{dt} V$$

Both proper shielding and rigid mechanical mounting of components help minimize error currents from both of these sources. Table I lists various insulators and their properties.

Material[1]	Volume Resistivity (Ω–CM)	Minimal Triboelectric Effects	Minimal Piezoelectric Effects	Resistance to Water Absorption
Teflon*	10^{17}–10^{18}	W	W	G
Kel-F**	10^{17}–10^{18}	W	M	G
Sapphire	10^{16}–10^{18}	M	G	G
Polyethylene	10^{14}–10^{18}	M	G	M
Polystyrene	10^{12}–10^{18}	W	M	M
Ceramic	10^{12}–10^{14}	W	M	W
Glass Epoxy	10^{10}–10^{17}	W	M	W
PVC	10^{10}–10^{15}	G	M	G
Phenolic	10^{5} –10^{12}	W	G	W

G–Good with Regard to Property
M–Moderate with Regard to Property
W–Weak with Regard to Property

[1]*Electronic Measurements*, pp.15–17, Keithley Instruments, Inc., Cleveland, Ohio, 1977.
*Teflon is a registered trademark of E.I. du Pont Co.
**Kel-F is a registered trademark of 3-M Company.

Table I. Insulating Materials and Characteristics

OFFSET NULLING

The AD546's input offset voltage can be nulled by using balance Pins 1 and 5, as shown in Figure 29. Nulling the input offset voltage in this fashion will introduce an added input offset voltage drift component of 2.4 μV/°C per millivolt of nulled offset.

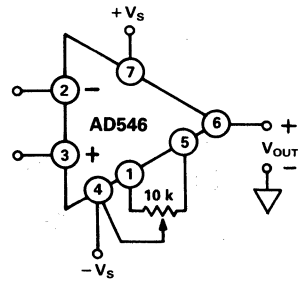


Figure 29. Standard Offset Null Circuit

The circuit in Figure 30 can be used when the amplifier is used as an inverter. This method introduces a small voltage in series with the amplifier's positive input terminal. The amplifier's input offset voltage drift with temperature is not affected. However, variation of the power supply voltages will cause offset shifts.

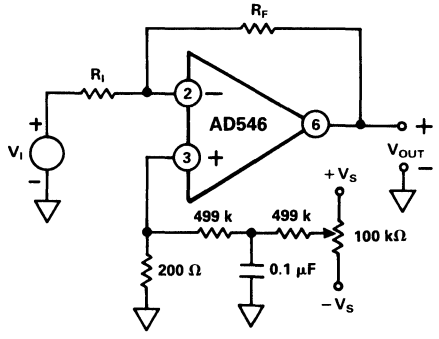


Figure 30. Alternate Offset Null Circuit for Inverter

AC RESPONSE WITH HIGH VALUE SOURCE AND FEEDBACK RESISTANCE

Source and feedback resistances greater than 100 kΩ will magnify the effect of input capacitances (stray and inherent to the AD546) on the ac behavior of the circuit. The effects of common mode and differential input capacitances should be taken into account since the circuit's bandwidth and stability can be adversely affected.

In a follower, the source resistance, R_S, and input common mode capacitance, C_S (including capacitance due to board and capacitance inherent to the AD546), form a pole that limits circuit bandwidth to $1/2\pi\ R_SC_S$. Figure 31 shows the follower pulse response from a 1 MΩ source resistance with the amplifier's input pin isolated from the board, only the effect of the AD546's input common mode capacitance is seen.

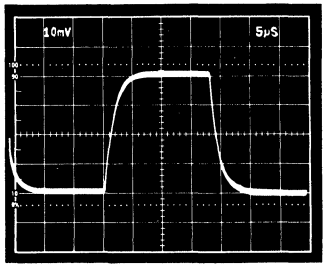


Figure 31. Follower Pulse Response from 1 MΩ Source Resistance

In an inverting configuration, the differential input capacitance forms a pole in the circuit's loop transmission. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1 MΩ, and the input pin isolated from the board appears in Figure 32. Figure 33 shows the response of the same circuit with a 1 pF feedback capacitance. Typical differential input capacitance for the AD546 is 1 pF.

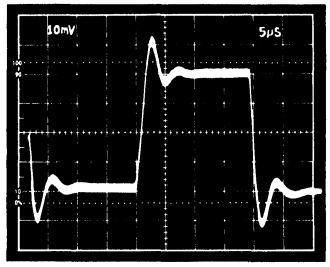


Figure 32. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

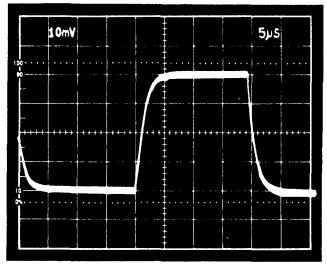


Figure 33. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1 pF Feedback Capacitance

COMMON MODE INPUT VOLTAGE OVERLOAD

The rated common-mode input voltage range of the AD546 is from 3 V less than the positive supply voltage to 5 V greater than the negative supply voltage. Exceeding this range will degrade the amplifier's CMRR. Driving the common mode voltage above the positive supply will cause the amplifier's output to saturate at the upper limit of output voltage. Recovery time is typically 2 μs after the input has been returned to within the normal operating range. Driving the input common mode voltage within 1 V of the negative supply causes phase reversal of the output signal. In this case, normal operation is typically resumed within 0.5 ms of the input voltage returning within range.

DIFFERENTIAL INPUT VOLTAGE OVERLOAD

A plot of the AD546's input current versus differential input voltage (defined as $V_{IN}+ - V_{IN}-$) appears in Figure 34. The

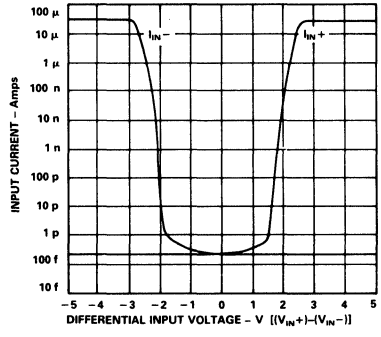


Figure 34. Input Current vs. Differential Input Voltage

input current at either terminal stays below a few hundred femtoamps until one input terminal is forced higher than 1 to 1.5 V above the other terminal. Under these conditions, the input current limits at 30 μA.

INPUT PROTECTION

The AD546 safely handles any input voltage within the supply voltage range. Subjecting the input terminals to voltages beyond the power supply can destroy the device or cause shifts in input current or offset voltage if the amplifier is not protected.

A protection scheme for the amplifier as an inverter is shown in Figure 35. The protection resistor, R_P, is chosen to limit the current through the inverting input to 1 mA for expected transient (less than 1 second) overvoltage conditions, or to 100 μA for a continuous overload. Since R_P is inside the feedback loop, and is much lower in value than the amplifier's input resistance, it does not affect the inverter's dc gain. However, the Johnson noise of the resistor will add root sum of squares to the amplifier's input noise.

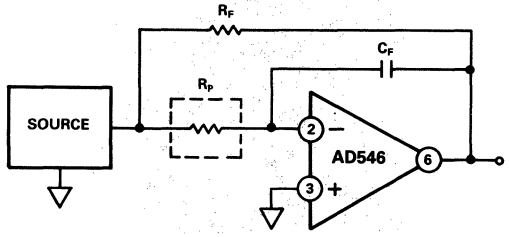


Figure 35. Inverter with Input Current Limit

In the corresponding version of this scheme for a follower, shown in Figure 36, R_P and the capacitance at the positive input terminal will produce a pole in the signal frequency response at a $f=1/2\pi RC$. Again, the Johnson noise of R_P will add to the amplifier's input voltage noise.

Figure 37 is a schematic of the AD546 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Low leakage diodes

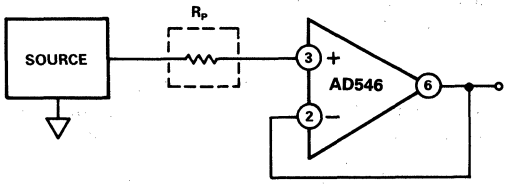


Figure 36. Follower with Input Current Limit

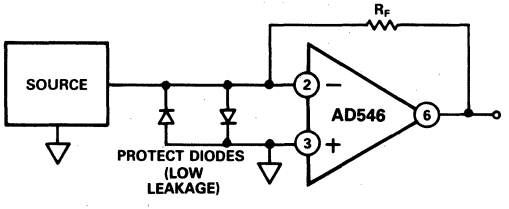


Figure 37. Input Voltage Clamp with Diodes

(less than 1 pA), such as the FD333's should be used, and should be shielded from light to keep photocurrents from being generated. Even with these precautions, the diodes will measurably increase the input current and capacitance.

In order to achieve the low input bias currents of the AD546, it is not possible to use the same on-chip protection as used in other Analog Devices op amps. This makes the AD546 sensitive to handling and precautions should be taken to minimize ESD exposure whenever possible.

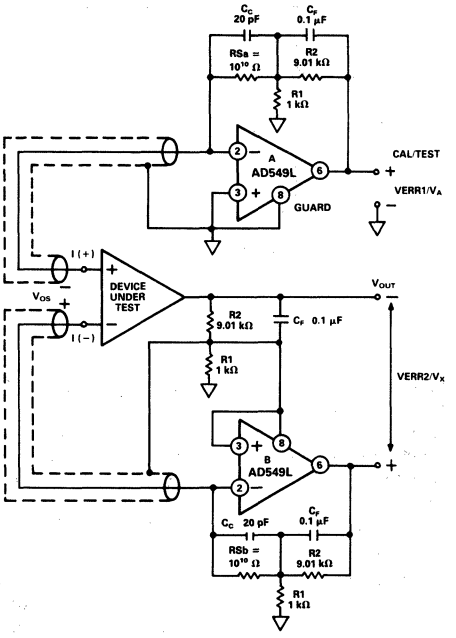


Figure 38. Sample and Difference Circuit for Measuring Electrometer Leakage Currents

MEASURING ELECTROMETER LEAKAGE CURRENTS

There are a number of methods used to test electrometer leakage currents, including current integration and direct current to voltage conversion. Regardless of the method used, board and interconnect cleanliness, proper choice of insulating materials (such as Teflon or Kel-F), correct guarding and shielding techniques and care in physical layout are essential for making accurate leakage measurements.

Figure 38 is a schematic of the sample and difference circuit which is useful for measuring the leakage currents of the AD546 and other electrometer amplifiers. The circuit uses two AD549 electrometer amplifiers (A and B) as current to voltage converters with high value (10^{10} Ω) sense resistors (RSa and RSb). R1 and R2 provide for an overall circuit sensitivity of 10 fA/mV (10 pA full scale). C_C and C_F provide noise suppression and loop compensation. C_C should be a low leakage polystyrene capacitor. An ultralow-leakage Kel-F test socket is used for contacting the device under test. Rigid Teflon coaxial cable is used to make connections to all high impedance nodes. The use of rigid coax affords immunity to error induced by mechanical vibration and provides an outer conductor for shielding. The entire circuit is enclosed in a grounded metal box.

The test apparatus is calibrated without a device under test present. A five minute stabilization period after the power is turned on is required. First, V_{ERR1} and V_{ERR2} are measured. These voltages are the errors caused by offset voltages and leakage currents of the current to voltage converters.

$$V_{ERR1} = 10\,(V_{OS}A - I_BA \times RSa)$$
$$V_{ERR2} = 10\,(V_{OS}B - I_BB \times RSb)$$

Once measured, these errors are subtracted from the readings taken with a device under test present. Amplifier B closes the feedback loop to the device under test, in addition to providing current to voltage conversion. The offset error of the device under test appears as a common mode signal and does not affect the test measurement. As a result, only the leakage current of the device under test is measured.

$$V_A - V_{ERR1} = 10[RSa \times I_B(+)]$$
$$V_X - V_{ERR2} = 10[RSb \times I_B(-)]$$

Although a series of devices can be tested after only one calibration measurement, calibration should be updated periodically to compensate for any thermal drift of the current-to-voltage converters or changes in the ambient environment. Laboratory results have shown that repeatable measurements within 10 fA can be realized when this apparatus is properly implemented. These results are achieved in part by the design of the circuit, which eliminates relays and other parasitic leakage paths in the high impedance signal lines, and in part by the inherent cancellation of errors through the calibration and measurement procedure.

PHOTODIODE INTERFACE

The AD546's 1 pA current and low input offset voltage make it a good choice for very sensitive photodiode preamps (Figure 39). The photodiode develops a signal current, I_S, equal to:

$$I_S = R \times P$$

where P is light power incident on the diode's surface in watts and R is the photodiode responsivity in amps/watt. R_F converts the signal current to an output voltage:

$$V_{OUT} = R_F \times I_S$$

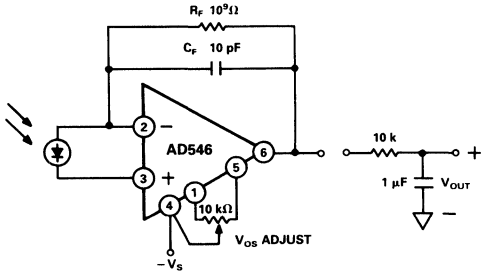


Figure 39. Photodiode Preamp

DC error sources and an equivalent circuit for a small area (0.2 mm square) photodiode are indicated in Figure 40.

Input current, I_B, will contribute an output voltage error, V_{E1}, proportional to the feedback resistance:

$$V_{E1} = I_B \times R_F$$

The op amp's input voltage offset will cause an error current through the photodiode's shunt resistance, R_S:

$$I = V_{OS}/R_S$$

The error current will result in an error voltage (V_{E2}) at the amplifier's output equal to:

$$V_{E2} = (1+R_F/R_S)\,V_{OS}$$

Given typical values of photodiode shunt resistance (on the order of $10^9\ \Omega$), R_F/R_S can be greater than one, especially if a large feedback resistance is used. Also, R_F/R_S will increase with temperature, as photodiode shunt resistance typically drops by a factor of two for every 10°C rise in temperature. An op amp with low offset voltage and low drift helps maintain accuracy.

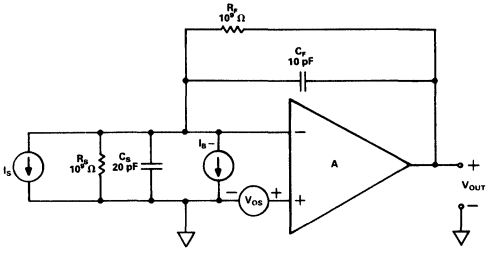


Figure 40. Photodiode Preamp DC Error Sources

Photodiode Preamp Noise

Noise limits the signal resolution obtainable with the preamp. The output voltage noise divided by the feedback resistance is the minimum current signal that can be detected. This minimum detectable current divided by the responsivity of the photodiode represents the lowest light power that can be detected by the preamp.

Noise sources associated with the photodiode, amplifier, and feedback resistance are shown in Figure 41; Figure 42 is the voltage spectral density versus frequency plot of each of the noise source's contribution to the output voltage noise (circuit parameters in Figure 40 are assumed). Each noise source's rms contribution to the total output voltage noise is obtained by integrating the square of its spectral density function over frequency. The rms value of the output voltage noise is the square root of the sum of all contributions. Minimizing the total area under these curves will optimize the preamplifier's resolution for a given bandwidth.

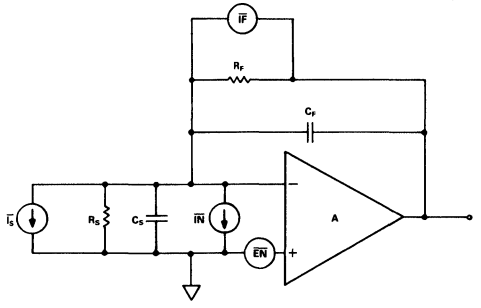


Figure 41. Photodiode Preamp Noise Sources

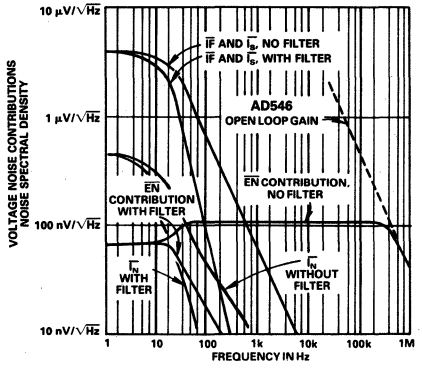


Figure 42. Photodiode Preamp Noise Sources' Spectral Density vs. Frequency

The photodiode preamp in Figure 39 can detect a signal current of 26 fA rms at a bandwidth of 16 Hz, which assuming a photodiode responsivity of 0.5 A/W, translates to a 52 fW rms minimum detectable power. The photodiode used has a high source resistance and low junction capacitance. C_F sets the signal bandwidth with R_F and also limits the "peak" in the noise gain that multiplies the op amp's input voltage noise contribution. A single pole filter at the amplifier's output limits the op amp's output voltage noise bandwidth to 26 Hz, a frequency comparable to the signal bandwidth. This greatly improves the preamplifier's signal to noise ratio (in this case, by a factor of three).

Photodiode Array Processor

The AD546 is a cost effective preamp for multichannel applications, such as amplifying signals from photo diode arrays, as illustrated in Figure 43. An AD546 preamp converts each of the diodes' output currents to a voltage. An 8 to 1 multiplexer switches a particular preamp output to the input of an AD1380 16-bit sampling ADC. The output of the ADC can be displayed or put onto a databus. Additional preamps and muxes can be added to handle larger arrays. Layout of multichannel circuits is critical. Refer to "PC board notes" for guidance.

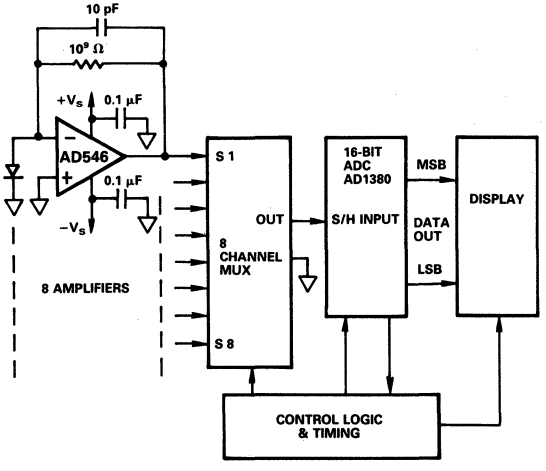


Figure 43. Photodiode Array Processor

pH PROBE AMPLIFIER

A pH probe can be modeled as a mV-level voltage source with a series source resistance dependent upon the electrode's composition and configuration. The glass bulb resistance of a typical pH electrode pair falls between 10^6 and 10^9 Ω. It is therefore important to select an amplifier with low enough input currents such that the voltage drop produced by the amplifier's input bias current and the electrode resistance does not become an appreciable percentage of a pH unit.

The circuit in Figure 44 illustrates the use of the AD546 as a pH probe amplifier. As with other electrometer applications, the use of guarding, shielding, Teflon standoffs, etc., is a must in order to capitalize on the AD546's low input current. If an AD546J (1 pA max input current) is used, the error contributed by input current will be held below 10 mV for pH electrode source impedances up to 10^9 Ω. Input offset voltage (which can be trimmed) will be below 2 mV. Refer to AD549 data sheet for temperature compensated pH probe amplifier circuit.

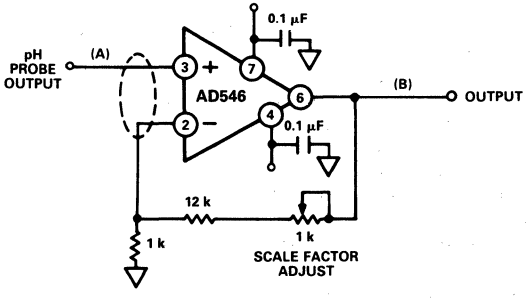


Figure 44. pH Probe Amplifier

ANALOG DEVICES

Precision, Low Power BiFET Op Amp

AD548

FEATURES

Enhanced Replacement for LF441 and TL061
DC Performance:
- **200μA max Quiescent Current**
- **10pA max Bias Current, Warmed Up (AD548C)**
- **250μV max Offset Voltage (AD548C)**
- **2μV/°C max Drift (AD548C)**
- **2μV p-p Noise, 0.1 to 10Hz**

AC Performance:
- **1.8V/μs Slew Rate**
- **1MHz Unity Gain Bandwidth**

Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages
MIL-STD-883B Parts Available
Dual Version Available: AD648
Surface Mount (SOIC) Package Available

PRODUCT DESCRIPTION

The AD548 is a low power, precision monolithic operational amplifier. It offers both low bias current (10pA max, warmed up) and low quiescent current (200μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD548's entire common-mode voltage range.

The economical J grade has a maximum guaranteed input offset voltage of less than 2mV and an input offset voltage drift of less than 20μV/°C. The C grade reduces input offset voltage to less than 0.25mV and offset voltage drift to less than 2μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

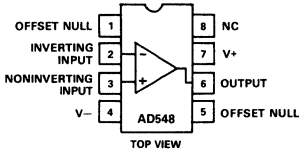
The AD548 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD548's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD548 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0 to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of −40°C to +85°C. The

AD548S and AD548T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

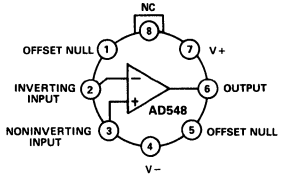
AD548 CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package, Cerdip (Q) Package and SOIC (R) Package

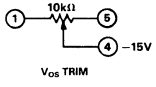


TOP VIEW

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE



V_{OS} TRIM

TOP VIEW

Extended reliability PLUS screening is available for parts specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD548 is available in an 8-pin plastic mini-DIP, cerdip, TO-99 metal can, surface mount (SOIC), or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high-performance, low-power applications.
2. The AD548 is pin compatible with industry standard op amps such as the LF441, TL061, and AD542, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2mV max) and drift (20μV/°C max) for the AD548J are achieved utilizing Analog Devices' laser drift trimming technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. A dual version, the AD648 is also available.
6. The AD548 is available in chip form.
7. Enhanced replacement for LF441 and TL061.

SPECIFICATIONS (@ + 25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD548J/A/S			AD548K/B/T			AD548C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	**2.0**		0.3	**0.5**		0.10	**0.25**	mV
T_{min} to T_{max}			3.0/3.0/**3.0**			**0.7/0.8/1.0**			**0.4**	mV
vs. Temp.			20			5			**2.0**	µV/°C
vs. Supply	**80**			**86**			**86**			dB
vs. Supply, T_{min} to T_{max}	76/76/**76**			**80**			**80**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input[2], V_{CM} = 0		5	**20**		3	**10**		3	**10**	pA
Either Input[2] at T_{max}, V_{CM} = 0			0.45/1.3/20			0.25/0.65/10			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			**30**			**15**			**15**	pA
Offset Current, V_{CM} = 0		5	**10**		2	5		2	5	pA
Offset Current at T_{max}			0.25/0.65/10			0.15/0.35/5			0.35	nA
INPUT IMPEDANCE										
Differential		$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$		Ω|pF
Common Mode		$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$		Ω|pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common Mode	**±11**	±12		**±11**	±12		**±11**	±12		V
Common-Mode Rejection										
V_{CM} = ±10V	**76**	90		**82**	92		**86**	98		dB
T_{min} to T_{max}	76/76/**76**	90		**82**	92		**86**	98		dB
V_{CM} = ±11V	**70**	84		**76**	86		**76**	90		dB
T_{min} to T_{max}	70/70/**70**	84		**76**	86		**76**	90		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4.0**	µV p-p
f = 10Hz		80			80			80		nV/√Hz
f = 100Hz		40			40			40		nV/√Hz
f = 1kHz		30			30			30		nV/√Hz
f = 10kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		1.8			1.8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	**1.0**	1.8		**1.0**	1.8		**1.0**	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 10k\Omega$	**300**	1000		**300**	1000		**300**	1000		V/mV
T_{min} to T_{max}, $R_L \geq 10k\Omega$	300/300/**300**	700		**300**	700		**300**	700		V/mV
V_O = ±10V, $R_L \geq 5k\Omega$	**150**	500		**150**	500		**150**	500		V/mV
T_{min} to T_{max}, $R_L \geq 5k\Omega$	150/150/**150**	300		**150**	300		**150**	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 10k\Omega$,	**±12**	±13		**±12**	±13		**±12**	±13		V
T_{min} to T_{max}	±12/±12/**±12**			**±12**			**±12**			
Voltage @ $R_L \geq 5k\Omega$,	**±11**	±12.3		**±11**	±12.3		**±11**	±12.3		V
T_{min} to T_{max}	±11/±11/**±11**			**±11**			**±11**			
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		170	**200**		170	**200**		170	**200**	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD548J			AD548K					
Industrial (−40°C to +85°C)		AD548A			AD548B			AD548C		
Military (−55°C to +125°C)		AD548S			AD548T					
PACKAGE OPTIONS[4]										
Plastic (N-8)	AD548JN			AD548KN						
Cerdip (Q-8)	AD548AQ, AD548SQ			AD548BQ, AD548TQ			AD548CQ			
Metal Can (H-08A)	AD548AH, AD548SH			AD548BH, AD548TH			AD548CH			
SOIC (R-8)	AD548AR, AD548JR			AD548BR						
Tape and Reel	AD548AR-REEL, AD548JR-REEL			AD548BR-REEL						
J and S Chips Also Available	AD548J CHIPS, AD548S CHIPS									

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications aré guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Defined as voltages between inputs, such that neither exceeds ±10V from ground.

[4]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
N	−65°C to +125°C
Operating Temperature Range	
AD548J/K	0 to +70°C
AD548A/B/C	−40°C to +85°C
AD548S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics

8-Pin Plastic Package: $\theta_{JA} = 90°C/W$

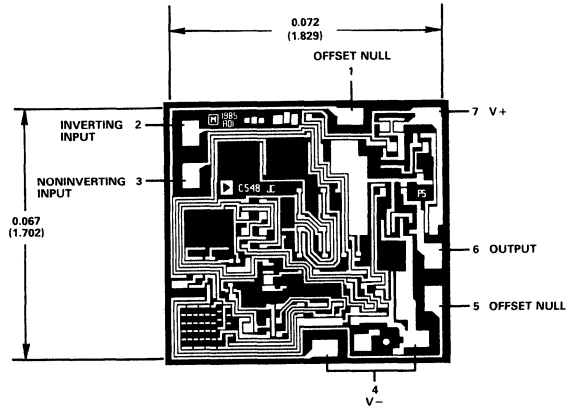
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W$, $\theta_{JA} = 110°C/W$

8-Pin Metal Can Package: $\theta_{JC} = 65°C/W$, $\theta_{JA} = 150°C/W$

[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



2

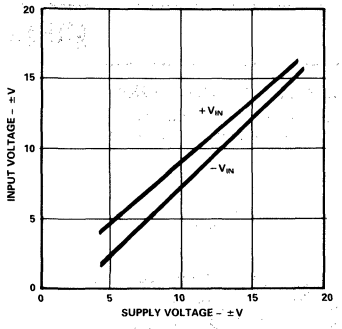


Figure 1. Input Voltage Range vs. Supply Voltage

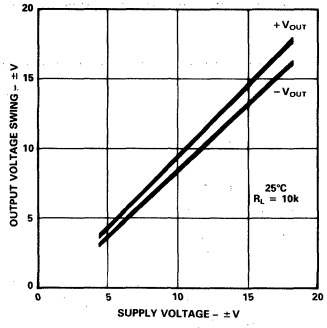


Figure 2. Output Voltage Swing vs. Supply Voltage

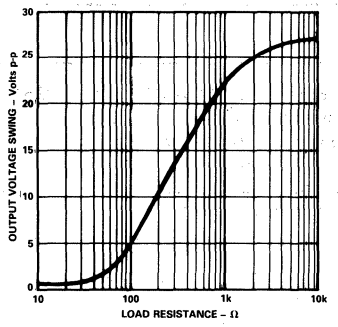


Figure 3. Output Voltage Swing vs. Load Resistance

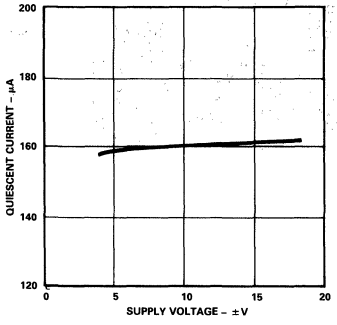


Figure 4. Quiescent Current vs. Supply Voltage

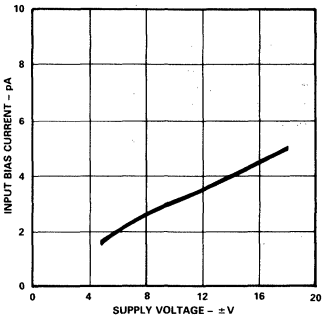


Figure 5. Input Bias Current vs. Supply Voltage

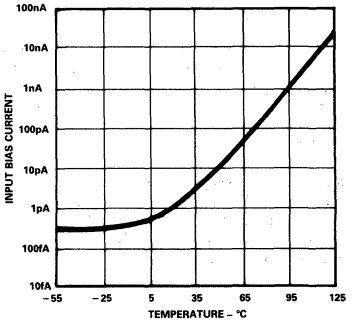


Figure 6. Input Bias Current vs. Temperature

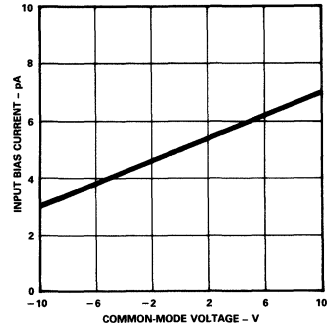


Figure 7. Input Bias Current vs. Common-Mode Voltage

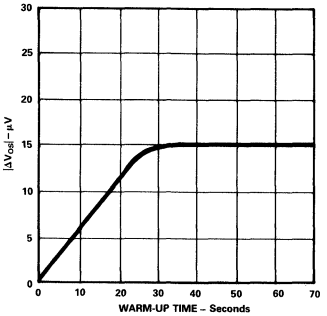


Figure 8. Change in Offset Voltage vs. Warm-Up Time

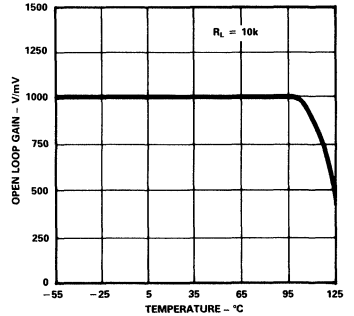


Figure 9. Open Loop Gain vs. Temperature

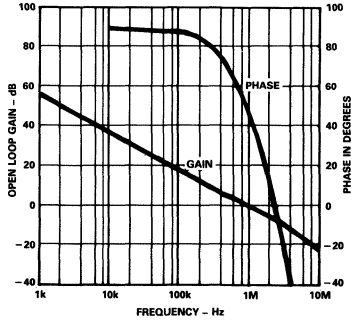


Figure 10. Open Loop Frequency Response

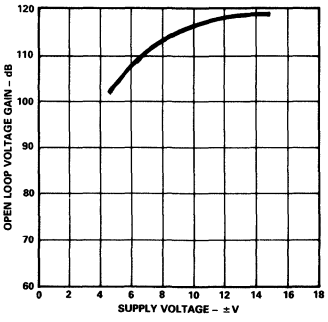


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

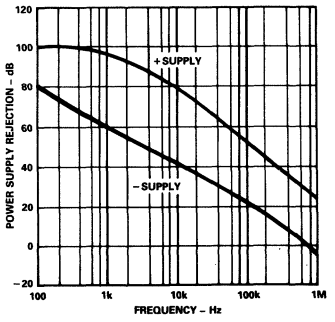


Figure 12. PSRR vs. Frequency

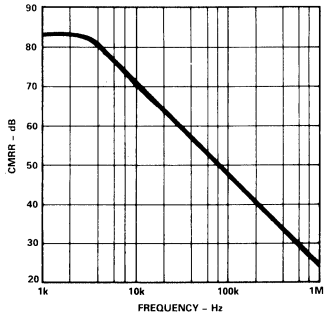


Figure 13. CMRR vs. Frequency

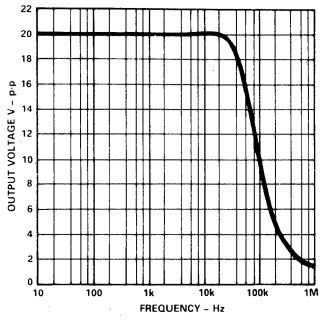


Figure 14. Large Signal Frequency Response

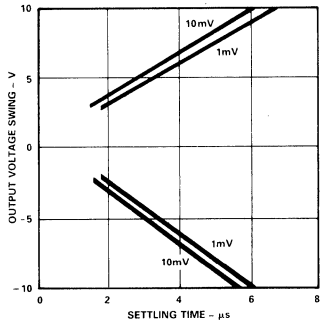


Figure 15. Output Swing and Error Voltage vs. Output Settling Time

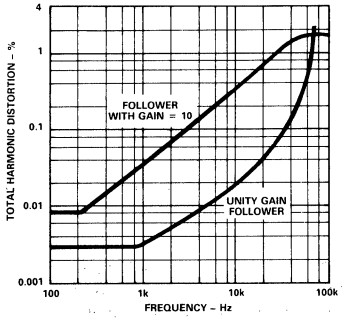


Figure 16. Total Harmonic Distortion vs. Frequency

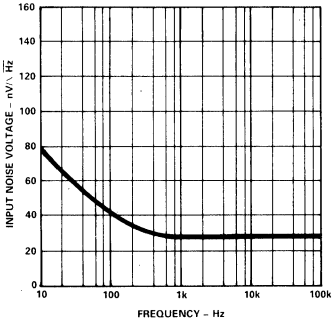


Figure 17. Input Noise Voltage Spectral Density

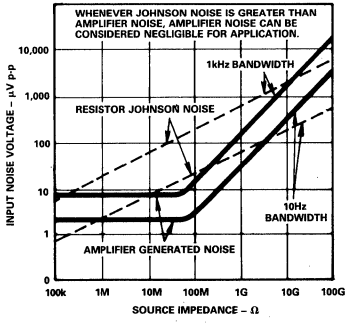


Figure 18. Total Noise vs. Source Impedance

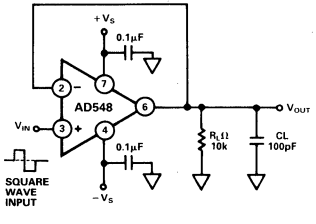


Figure 19a. Unity Gain Follower

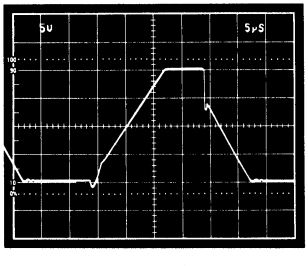


Figure 19b. Unity Gain Follower Pulse Response (Large Signal)

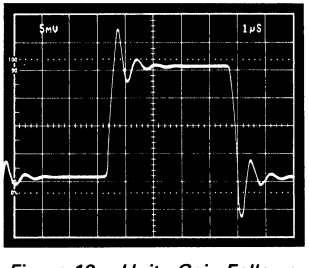


Figure 19c. Unity Gain Follower Pulse Response (Small Signal)

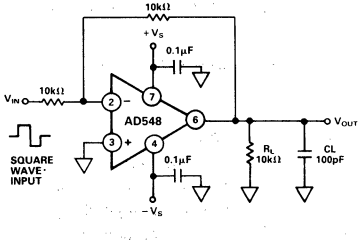


Figure 20a. Unity Gain Inverter

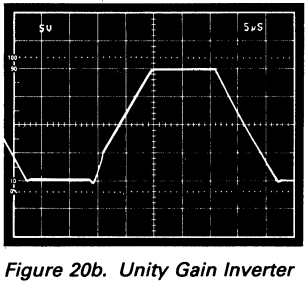


Figure 20b. Unity Gain Inverter Pulse Response (Large Signal)

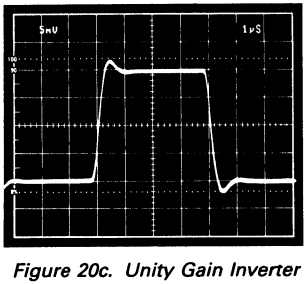


Figure 20c. Unity Gain Inverter Pulse Response (Small Signal)

Applying the AD548

APPLICATION NOTES

The AD548 is a JFET-input op amp with a guaranteed maximum I_B of less than 10pA, and offset and drift laser-trimmed to 0.25mV and 2μV/°C respectively (AD548C). AC specs include 1MHz bandwidth, 1.8V/μs typical slew rate and 8μs settling time for a 20V step to ±0.01% – all at a supply current less than 200μA. To capitalize on the device's performance, a number of error sources should be considered.

The minimal power drain and low offset drift of the AD548 reduce self-heating or "warm-up" effects on input offset voltage, making the AD548 ideal for on/off battery powered applications. The power dissipation due to the AD548's 200μA supply current has a negligible effect on input current, but heavy output loading will raise the chip temperature. Since a JFET's input current doubles for every 10°C rise in chip temperature, this can be a noticeable effect.

The amplifier is designed to be functional with power supply voltages as low as ±4.5V. It will exhibit a higher input offset voltage than at the rated supply voltage of ±15V, due to power supply rejection effects. The common-mode range of the AD548 extends from 3V more positive than the negative supply to 1V more negative than the positive supply. Designed to cleanly drive up to 10kΩ and 100pF loads, the AD548 will drive a 2kΩ load with reduced open loop gain.

OFFSET NULLING

Unlike bipolar input amplifiers, zeroing the input offset voltage of a BiFET op amp will not minimize offset drift. Using balance Pins 1 and 5 to adjust the input offset voltage as shown in Figure 21 will induce an added drift of 0.24μV/°C per 100μV of nulled offset. The low initial offset (0.25mV) of the AD548C results in only 0.6μV/°C of additional drift.

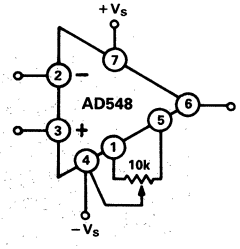


Figure 21. Offset Null Configuration

LAYOUT

To take full advantage of the AD548's 10pA max input current, parasitic leakages must be kept below an acceptable level. The practical limit of the resistance of epoxy or phenolic circuit board material is between $1 \times 10^{12}\Omega$ and $3 \times 10^{12}\Omega$. This can result in an additional leakage of 5pA between an input of 0V and a −15V supply line. Teflon or a similar low leakage material (with a resistance exceeding $10^{17}\Omega$) should be used to isolate high impedance input lines from adjacent lines carrying high voltages. The insulator should be kept clean, since contaminants will degrade the surface resistance.

A metal guard completely surrounding the high impedance nodes and driven by a voltage near the common-mode input potential can also be used to reduce some parasitic leakages. The guarding pattern in Figure 22 will reduce parasitic leakage due to finite board surface resistance; but it will not compensate for a low volume resistivity board.

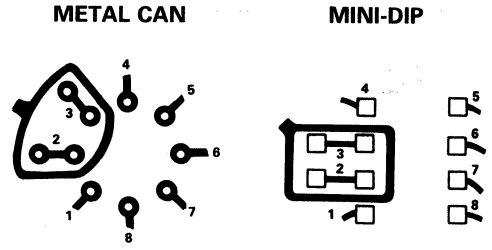


Figure 22. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD548 is guaranteed to withstand input voltages equal to the power supply potential. Exceeding the negative supply voltage on either input will forward bias the substrate junction of the chip. The induced current may destroy the amplifier due to excess heat.

Input protection is required in applications such as a flame detector in a gas chromatograph, where a very high potential may be applied to the input terminals during a sensor fault condition. Figure 23 shows a simple current limiting scheme that can be used. $R_{PROTECT}$ should be chosen such that the maximum overload current is 1.0mA (100kΩ for a 100V overload, for example).

Exceeding the negative common-mode range on either input terminal causes a phase reversal at the output, forcing the amplifier output to the corresponding high or low state. Exceeding the negative common-mode on both inputs simultaneously forces the output high. Exceeding the positive common-mode range on a single input doesn't cause a phase reversal, but if both inputs exceed the limit the output will be forced high. In all cases, normal amplifier operation is resumed when input voltages are brought back within the common-mode range.

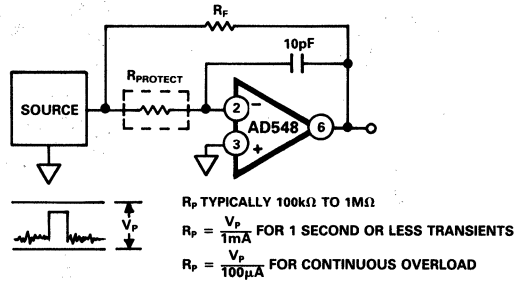


Figure 23. Input Protection of IV Converter

D/A CONVERTER OUTPUT BUFFER

The circuit in Figure 24 shows the AD548 and AD7545 12-bit CMOS D/A converter in a unipolar binary configuration. V_{OUT} will be equal to V_{REF} attenuated by a factor depending on the digital word. V_{REF} sets the full scale. Overall gain is trimmed by adjusting R_{IN}. The AD548's low input offset voltage, low drift and clean dynamics make it an attractive low power output buffer.

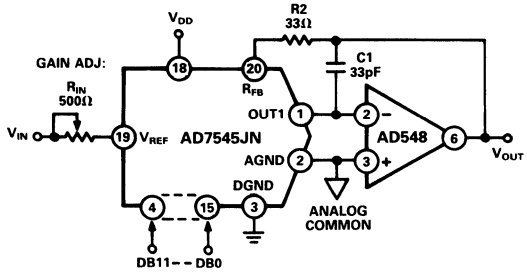


Figure 24. AD548 Used as DAC Output Amplifier

The input offset voltage of the AD548 output amplifier results in an output error voltage. This error voltage equals the input offset voltage of the op amp times the noise gain of the amplifier. That is:

$$V_{OS}\ \text{Output} = V_{OS}\ \text{Input}\left(1+\frac{R_{FB}}{R_O}\right)$$

R_{FB} is the feedback resistor for the op amp, which is internal to the DAC. R_O is the DAC's R-2R ladder output resistance. The value of R_O is code dependent. This has the effect of changing the offset error voltage at the amplifier's output. An output amplifier with a sub millivolt input offset voltage is needed to preserve the linearity of the DAC's transfer function.

The AD548 in this configuration provides a 700kHz small signal bandwidth and 1.8V/μs typical slew rate. The 33pF capacitor across the feedback resistor optimizes the circuit's response. The oscilloscope photos in Figures 25 and 26 show small and large signal outputs of the circuit in Figure 24. Upper traces show the input signal V_{IN}. Lower traces are the resulting output voltage with the DAC's digital input set to all 1s. The AD548 settles to ±0.01% for a 20V input step in 14μs.

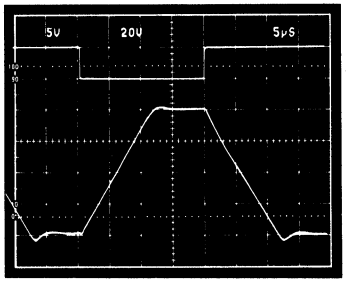


Figure 25. Response to ±20V p-p Reference Square Wave

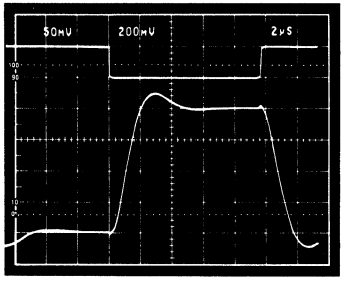


Figure 26. Response to ±100mV p-p Reference Square Wave

PHOTODIODE PREAMP

The performance of the photodiode preamp shown in Figure 27 is enhanced by the AD548's low input current, input voltage offset and offset voltage drift. The photodiode sources a current proportional to the incident light power on its surface. R_F converts the photodiode current to an output voltage equal to $R_F \times I_S$.

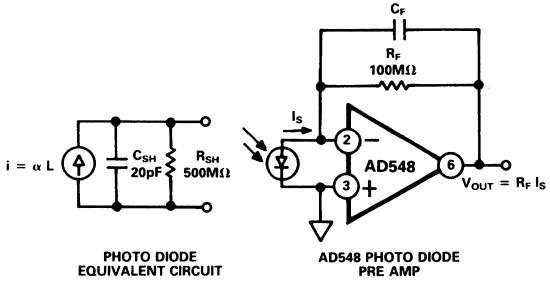


Figure 27.

An error budget illustrating the importance of low amplifier input current, voltage offset and offset voltage drift to minimize output voltage errors can be developed by considering the equivalent circuit for the small (0.2mm² area) photodiode shown in Figure 27. The input current results in an error proportional to the feedback resistance used. The amplifier's offset will produce an error proportional to the preamp's noise gain $(1+R_F/R_{SH})$, where R_{SH} is the photodiode shunt resistance. The amplifier's input current will double with every 10°C rise in temperature, and the photodiode's shunt resistance halves with every 10°C rise. The error budget in Figure 28 assumes a room temperature photodiode R_{SH} of 500MΩ, and the maximum input current and input offset voltage specs of an AD548C.

TEMP °C	R_{SH} (MΩ)	V_{OS} (μV)	$(1+R_F/R_{SH})V_{OS}$	I_B (pA)	$I_B R_F$	TOTAL
−25	15,970	150	151μV	0.30	30μV	181μV
0	2,830	200	207μV	2.26	262μV	469μV
+25	500	250	300μV	10.00	1.0mV	1.30mV
+50	88.5	300	640μV	56.6	5.6mV	6.24mV
+75	15.6	350	2.6mV	320	32mV	34.6mV
+85	7.8	370	5.1mV	640	64mV	69.1mV

Figure 28. Photo Diode Pre-Amp Errors Over Temperature

The capacitance at the amplifier's negative input (the sum of the photodiode's shunt capacitance, the op amp's differential input capacitance, stray capacitance due to wiring, etc.) will cause a rise in the preamp's noise gain over frequency. This can result in excess noise over the bandwidth of interest. C_F reduces the noise gain "peaking" at the expense of bandwidth.

INSTRUMENTATION AMPLIFIER

The AD548C's maximum input current of 10pA makes it an excellent building block for the high input impedance instrumentation amplifier shown in Figure 29. Total current drain for this circuit is under 600μA. This configuration is optimal for conditioning differential voltages from high impedance sources.

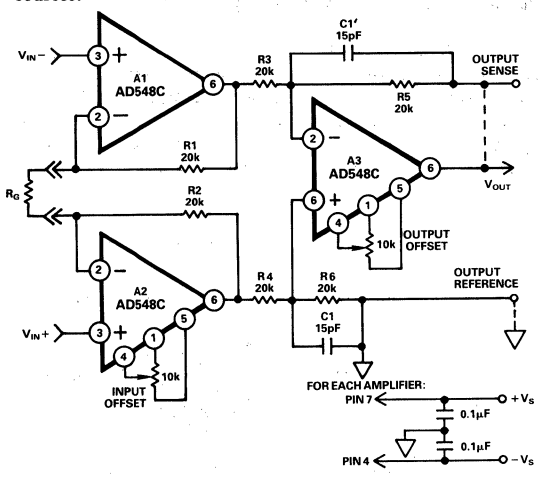


Figure 29. Low Power Instrumentation Amplifier

The overall gain of the circuit is controlled by R_G, resulting in the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{(R_1 + R_2)}{R_G}$$

Gains of 1 to 100 can be accommodated with gain nonlinearities of less than 0.01%. Referred to input errors, which contribute an output error proportional to in amp gain, include a maximum untrimmed input offset voltage of 0.5mV and an input offset voltage drift over temperature of 4μV/°C. Output errors, which are independent of gain, will contribute an additional 0.5mV offset and 4μV/°C drift. The maximum input current is 15pA over the common-mode range, with a common-mode impedance of over $1 \times 10^{12}\Omega$. Resistor pairs R3/R5 and R4/R6 should be ratio matched to 0.01% to take full advantage of the AD548's high common mode rejection. Capacitors C1 and C1′ compensate for peaking in the gain over frequency caused by input capacitance when gains of 1 to 3 are used.

The −3dB small signal bandwidth for this low power instrumentation amplifier is 700kHz for a gain of 1 and 10kHz for a gain of 100. The typical output slew rate is 1.8V/μs.

LOG RATIO AMPLIFIER

Log ratio amplifiers are useful for a variety of signal conditioning applications, such as linearizing exponential transducer outputs and compressing analog signals having a wide dynamic range. The AD548's picoamp level input current and low input offset voltage make it a good choice for the front-end amplifier of the log ratio circuit shown in Figure 30. This circuit produces an output voltage equal to the log base 10 of the ratio of the input currents I_1 and I_2. Resistive inputs R1 and R2 are provided for voltage inputs.

Input currents I_1 and I_2 set the collector currents of Q1 and Q2, a matched pair of logging transistors. Voltages at points A and B are developed according to the following familiar diode equation:

$$V_{BE} = (kT/q) \ln (I_C/I_{ES})$$

In this equation, k is Boltzmann's constant, T is absolute temperature, q is an electron charge, and I_{ES} is the reverse saturation current of the logging transistors. The difference of these two voltages is taken by the subtractor section and scaled by a factor of approximately 16 by resistors R9, R10, and R8. Temperature compensation is provided by resistors R8 and R15, which have a positive 3500 ppm/°C temperature coefficient. The transfer function for the output voltage is:

$$V_{OUT} = 1V \log_{10} (I_2/I_1)$$

Frequency compensation is provided by R11, R12, C1, and C2. Small signal bandwidth is approximately 300kHz at input currents above 100μA and will proportionally decrease with lower signal levels. D1, D2, R13, and R14 compensate for the effects of the two logging transistors' ohmic emitter resistance.

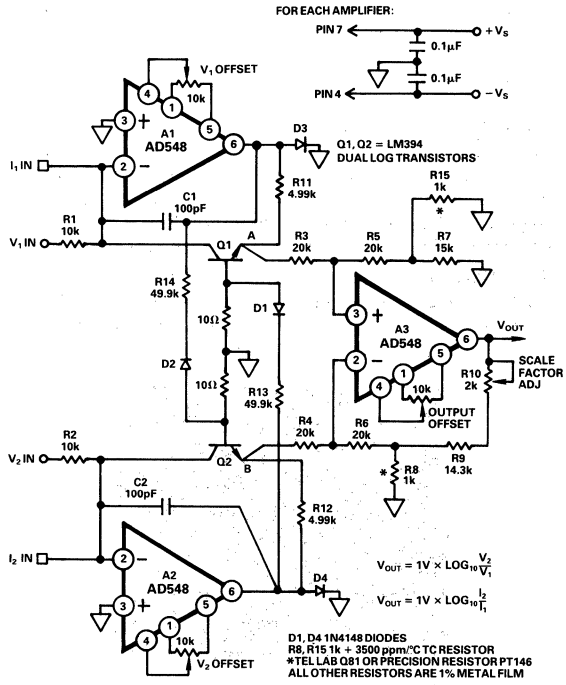


Figure 30. Log Ratio Amplifier

To trim this circuit, set the two input currents to 10μA and adjust V_{OUT} to zero by adjusting the potentiometer on A3. Then set I_2 to 1μA and adjust the scale factor such that the output voltage is 1V by trimming potentiometer R10. Offset adjustment for A1 and A2 is provided to increase the accuracy of the voltage inputs.

This circuit ensures a 1% log conformance error over an input current range of 300pA to 1mA, with low level accuracy limited by the AD548's input current. The low level input voltage accuracy of this circuit is limited by the input offset voltage and drift of the AD548.

Ultralow Input Bias Current Operational Amplifier

AD549*

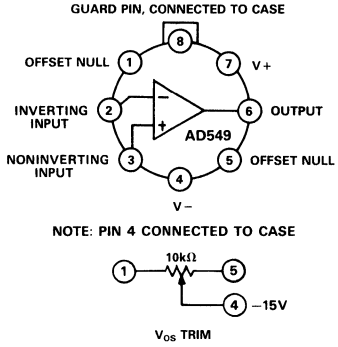
FEATURES

Ultralow Bias Current: 60 fA max (AD549L)
250 fA max (AD549J)
Input Bias Current Guaranteed Over Common-Mode Voltage Range
Low Offset Voltage: 0.25 mV max (AD549K)
1.00 mV max (AD549J)
Low Offset Drift: 5 μV/°C max (AD549K)
20 μV/°C max (AD549J)
Low Power: 700 μA max Supply Current
Low Input Voltage Noise: 4 μV p–p 0.1 to 10 Hz
MIL-STD-883B Parts Available

APPLICATIONS

Electrometer Amplifiers
Photodiode Preamp
pH Electrode Buffer
Vacuum Ion Gage Measurement

AD549 CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The AD549 is a monolithic electrometer operational amplifier with very low input bias current. Input offset voltage and input offset voltage drift are laser trimmed for precision performance. The AD549's ultralow input current is achieved with "Topgate" JFET technology, a process development exclusive to Analog Devices. This technology allows the fabrication of extremely low input current JFETs compatible with a standard junction-isolated bipolar process. The 10^{15} Ω common-mode impedance, a result of the bootstrapped input stage, insures that the input current is essentially independent of common-mode voltage.

The AD549 is suited for applications requiring very low input current and low input offset voltage. It excels as a preamp for a wide variety of current output transducers such as photodiodes, photomultiplier tubes, or oxygen sensors. The AD549 can also be used as a precision integrator or low droop sample and hold. The AD549 is pin compatible with standard FET and electrometer op amps, allowing designers to upgrade the performance of present systems at little additional cost.

The AD549 is available in a TO-99 hermetic package. The case is connected to Pin 8 so that the metal case can be independently connected to a point at the same potential as the input terminals, minimizing stray leakage to the case.

The AD549 is available in four performance grades. The J, K, and L versions are rated over the commercial temperature range 0 to 170°C. The S grade is specified over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C. Extended reliability PLUS screening is also available. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests derived from MIL-STD-883B, Rev C.

PRODUCT HIGHLIGHTS

1. The AD549's input currents are specified, 100% tested and guaranteed after the device is warmed up. Input current is guaranteed over the entire common-mode input voltage range.
2. The AD549's input offset voltage and drift are laser trimmed to 0.25 mV and 5 μV/°C (AD549K), 1 mV and 20 μV/°C (AD549J).
3. A maximum quiescent supply current of 700 μA minimizes heating effects on input current and offset voltage.
4. AC specifications include 1 MHz unity gain bandwidth and 3 V/μs slew rate. Settling time for a 10 V input step is 5 μs to 0.01%.
5. The AD549 is an improved replacement for the AD515, OPA104, and 3528.

***Covered by Patent No. 4,639,683.**

SPECIFICATIONS (@ +25°C and V_S = +15 V dc, unless otherwise noted)

Model	AD549J Min	AD549J Typ	AD549J Max	AD549K Min	AD549K Typ	AD549K Max	AD549L Min	AD549L Typ	AD549L Max	AD549S Min	AD549S Typ	AD549S Max	Units
INPUT BIAS CURRENT[1]													
Either Input, V_{CM} = 0 V		150	**250**		75	**100**		40	**60**		75	**100**	fA
Either Input, V_{CM} = ±10 V		150	250		75	100		40	60		75	100	fA
Either Input at T_{max}, V_{CM} = 0 V		11			4.2			2.8			420		pA
Offset Current		50			30			20			30		fA
Offset Current at T_{max}		2.2			1.3			0.85			125		pA
INPUT OFFSET VOLTAGE[2]													
Initial Offset		0.5	**1.0**		0.15	**0.25**		0.3	**0.5**		0.3	**0.5**	mV
Offset at T_{max}			**1.9**			**0.4**			**0.9**			**2.0**	mV
vs. Temperature		10	**20**		2	**5**		5	**10**		10	**15**	µV/°C
vs. Supply		32	**100**		10	**32**		10	**32**		10	**32**	µV/V
vs. Supply, T_{min} to T_{max}		32	**100**		10	**32**		10	**32**		32	**50**	µV/V
Long-Term Offset Stability		15			15			15			15		µV/Month
INPUT VOLTAGE NOISE													
f = 0.1 Hz to 10 Hz		4			4	**6**		4			4		µV p-p
f = 10 Hz		90			90			90			90		nV/√Hz
f = 100 Hz		60			60			60			60		nV/√Hz
f = 1 kHz		35			35			35			35		nV/√Hz
f = 10 kHz		35			35			35			35		nV/√Hz
INPUT CURRENT NOISE													
f=0.1 Hz to 10 Hz		0.7			0.5			0.36			0.5		fA rms
f=1 kHz		0.22			0.16			0.11			0.16		fA/√Hz
INPUT IMPEDANCE													
Differential V_{DIFF} = ±1		10^{13}‖1			10^{13}‖1			10^{13}‖1			10^{13}‖1		Ω‖pF
Common Mode V_{CM} = ±10		10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8		Ω‖pF
OPEN-LOOP GAIN													
V_O @ ±10 V, R_L = 10 k	**300**	1000		**300**	1000		**300**	1000		**300**	1000		V/mV
V_O @ ±10 V, R_L = 10 k, T_{min} to T_{max}	**300**	800		**300**	800		**300**	800		**300**	800		V/mV
V_O = ±10 V, R_L = 2 k	**100**	250		**100**	250		**100**	250		**100**	250		V/mV
V_O = ±10 V, R_L = 2 k, T_{min} to T_{max}	**80**	200		**80**	200		**80**	200		**25**	150		V/mV
INPUT VOLTAGE RANGE													
Differential[3]			±20			±20			±20			±20	V
Common-Mode Voltage	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	V
Common-Mode Rejection Ratio													
V=+10 V, −10 V	**80**	90		**90**	100		**90**	100		**90**	100		dB
T_{min} to T_{max}	**76**	80		**80**	90		**80**	90		**80**	90		dB
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 10 k, T_{min} to T_{max}	**−12**		**+12**	**−12**		**+12**	**−12**		**+12**	**−12**		**+12**	V
Voltage @ R_L = 2 k, T_{min} to T_{max}	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	V
Short Circuit Current	15	20	**35**	15	20	**35**	15	20	**35**	15	20	**35**	mA
T_{min} to T_{max}	**9**			**9**			**9**			**6**			mA
Load Capacitance Stability G = +1		4000			4000			4000			4000		pF
FREQUENCY RESPONSE													
Unity Gain, Small Signal	0.7	1.0		0.7	1.0		0.7	1.0		0.7	1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate	2	3		2	3		2	3		2	3		V/µs
Settling Time, 0.1%		4.5			4.5			4.5			4.5		µs
0.01%		5			5			5			5		µs
Overload Recovery, 50% Overdrive, G = −1		2			2			2			2		µs
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**	mA

Model	AD549J Min	AD549J Typ	AD549J Max	AD549K Min	AD549K Typ	AD549K Max	AD549L Min	AD549L Typ	AD549L Max	AD549S Min	AD549S Typ	AD549S Max	Units
TEMPERATURE RANGE													
Operating, Rated Performance	0		70	0		70	0		70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[4]													
TO-99 (H-08A)	AD549JH			AD549KH			AD549LH			AD549SH			

NOTES
[1]Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.
[2]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[3]Defined as max continuous voltage between the inputs such that neither input exceeds ±10 V from ground.
[4]See Section 20 for package outline information.

Specifications subject to change without notice.

All min and max specifications are guaranteed.Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

2

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 500 mW
Input Voltage . . . . . ±18 V[2]
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range H . . . . . −65°C to +150°C
Operating Temperature Range
AD549J, K, L . . . . . 0 to +70°C
AD549S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

CAUTION:

ESD (electrostatic discharge) sensitive device. Charges as high as 4000 V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

Typical Characateristics

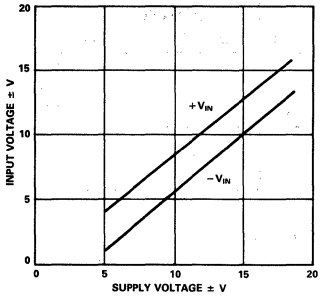


Figure 1. Input Voltage Range vs. Supply Voltage

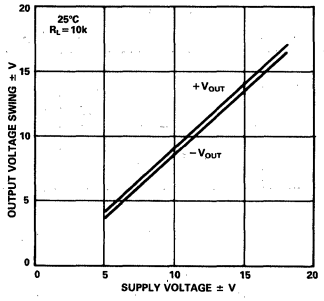


Figure 2. Output Voltage Swing vs. Supply Voltage

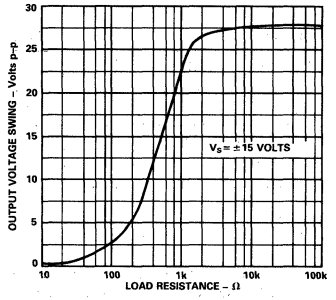


Figure 3. Output Voltage Swing vs. Load Resistance

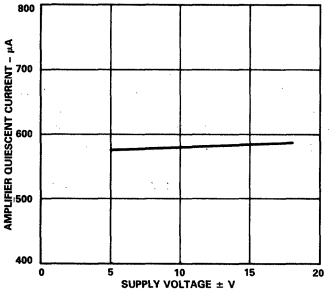


Figure 4. Quiescent Current vs. Supply Voltage

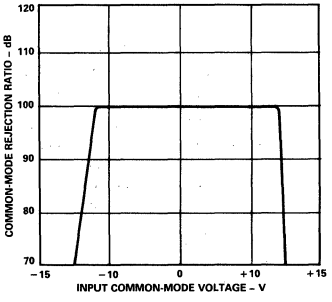


Figure 5. CMRR vs. Input Common-Mode Voltage

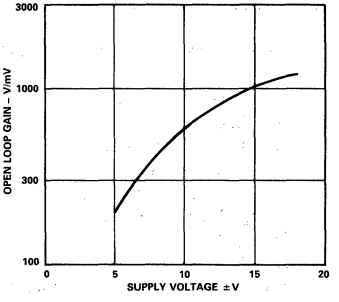


Figure 6. Open-Loop Gain vs. Supply Voltage

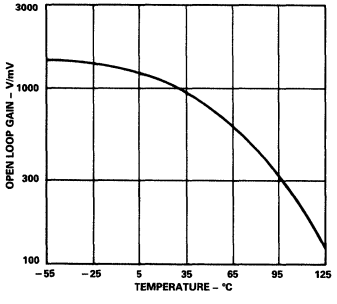


Figure 7. Open-Loop Gain vs. Temperature

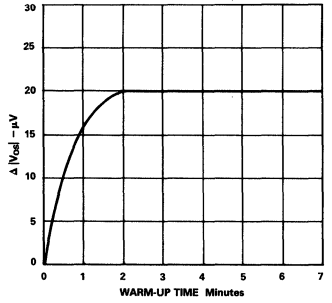


Figure 8. Change in Offset Voltage vs. Warm-Up Time

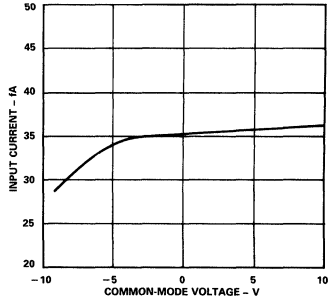


Figure 9. Input Bias Current vs. Common-Mode Voltage

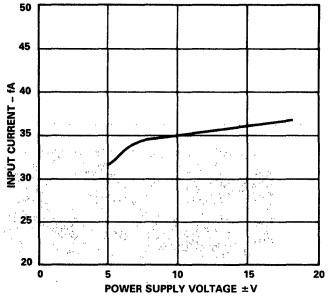


Figure 10. Input Bias Current vs. Supply Voltage

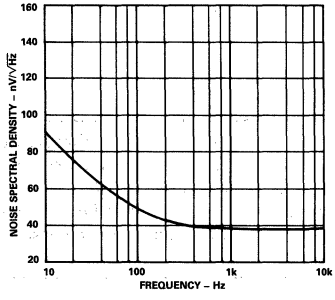


Figure 11. Input Voltage Noise Spectral Density

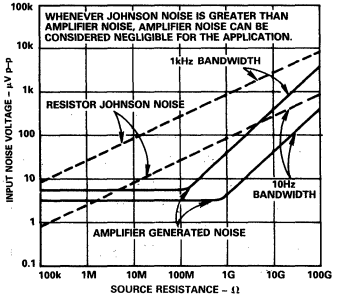


Figure 12. Noise vs. Source Resistance

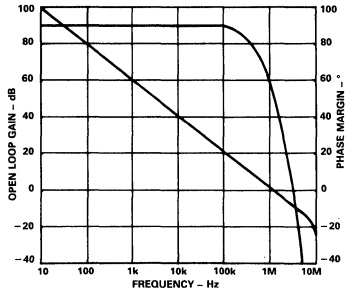


Figure 13. Open-Loop Frequency Response

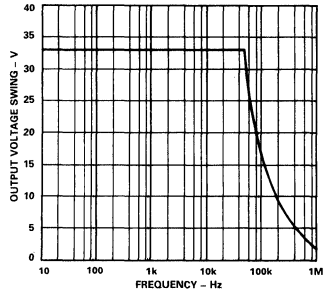


Figure 14. Large Signal Frequency Response

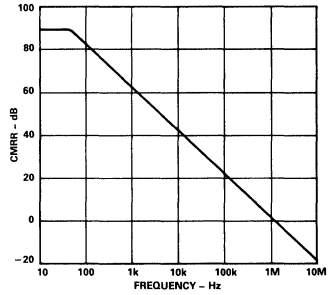


Figure 15. CMRR vs. Frequency

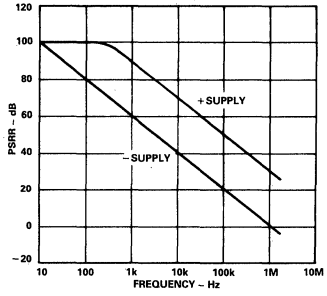


Figure 16. PSRR vs. Frequency

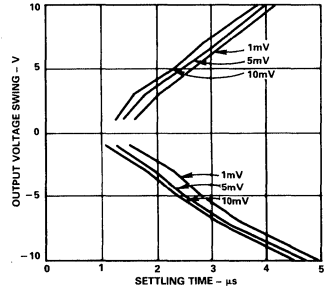


Figure 17. Output Voltage Swing and Error vs. Settling Time

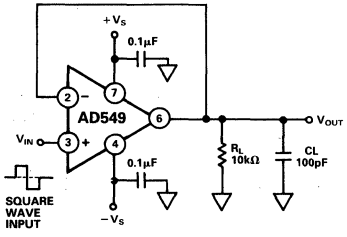


Figure 18. Unity Gain Follower

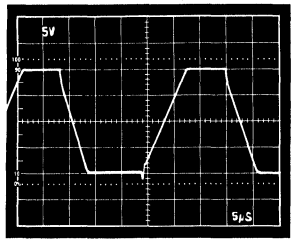


Figure 19. Unity Gain Follower Large Signal Pulse Response

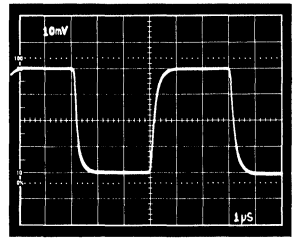


Figure 20. Unity Gain Follower Small Signal Pulse Response

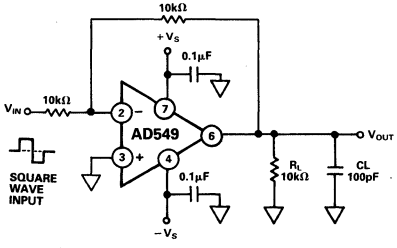


Figure 21. Unity Gain Inverter

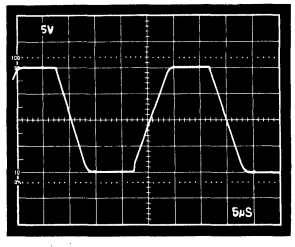


Figure 22. Unity Gain Inverter Large Signal Pulse Response

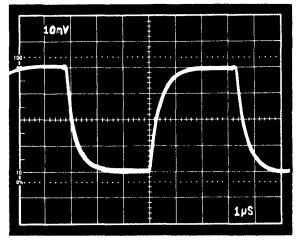


Figure 23. Unity Gain Inverter Small Signal Pulse Response

MINIMIZING INPUT CURRENT

The AD549 has been optimized for low input current and offset voltage. Careful attention to how the amplifier is used will reduce input currents in actual applications.

The amplifier operating temperature should be kept as low as possible to minimize input current. Like other JFET input amplifiers, the AD549's input current is sensitive to chip temperature, rising by a factor of 2.3 for every 10°C rise. This is illustrated in Figure 24, a plot of AD549 input current versus ambient temperature.

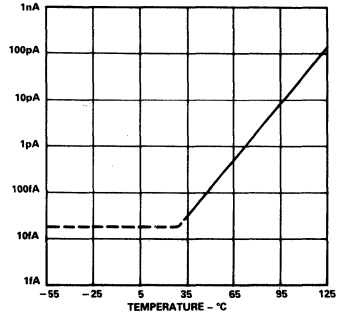


Figure 24. AD549 Input Bias Current vs. Ambient Temperature

On-chip power dissipation will raise chip operating temperature causing an increase in input bias current. Due to the AD549's low quiescent supply current, chip temperature when the (unloaded) amplifier is operated with 15 V supplies, is less than 3°C higher than ambient. The difference in input current is negligible.

However, heavy output loads can cause a significant increase in chip temperature and a corresponding increase in input current. Maintaining a minimum load resistance of 10 Ω is recommended. Input current versus additional power dissipation due to output drive current is plotted in Figure 25.

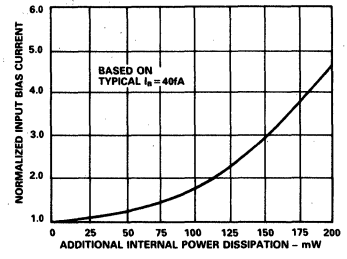


Figure 25. AD549 Input Bias Current vs. Additional Power Dissipation

CIRCUIT BOARD NOTES

There are a number of physical phenomena that generate spurious currents that degrade the accuracy of low current measurements. Figure 26 is a schematic of an I-to-V converter with these parasitic currents modeled.

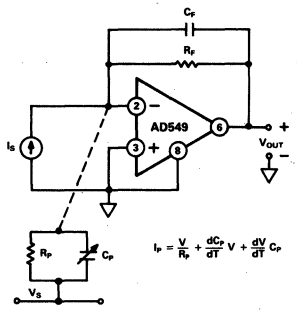


Figure 26. Sources of Parasitic Leakage Currents

Finite resistance from input lines to voltages on the board, modeled by resistor R_P, results in parasitic leakage. Insulation resistance of over 10^{15} Ω must be maintained between the amplifier's signal and supply lines in order to capitalize on the AD549's low input currents. Standard PC board material does not have high enough insulation resistance. Therefore, the AD549's input leads should be connected to standoffs made of insulating material with adequate volume resistivity (e.g., Teflon*). The surface of the insulator's surface must be kept clean in order to preserve surface resistivity. For Teflon, an effective cleaning procedure consists of swabbing the surface with high-grade isopropyl alcohol, rinsing with deionized water, and baking the board at 80°C for 10 minutes.

In addition to high volume and surface resistivity, other properties are desirable in the insulating material chosen. Resistance to water absorption is important since surface water films drastically reduce surface resistivity. The insulator chosen should also exhibit minimal piezoelectric effects (charge emission due to mechanical stress) and triboelectric effects (charge generated by friction). Charge imbalances generated by these mechanisms can appear as parasitic leakage currents. These effects are modeled by variable capacitor C_P in Figure 26. The table in Figure 27 lists various insulators and their properties.[1]

Material	Volume Resistivity (Ω–CM)	Minimal Triboelectric Effects	Minimal Piezoelectric Effects	Resistance to Water Absorption
Teflon	10^{17}–10^{18}	W	W	G
Kel-F**	10^{17}–10^{18}	W	M	G
Sapphire	10^{16}–10^{18}	M	G	G
Polyethylene	10^{14}–10^{18}	M	G	M
Polystyrene	10^{12}–10^{18}	W	M	M
Ceramic	10^{12}–10^{14}	W	M	W
Glass Epoxy	10^{10}–10^{17}	W	M	W
PVC	10^{10}–10^{15}	G	M	G
Phenolic	10^{5} –10^{12}	W	G	W

G–Good with Regard to Property
M–Moderate with Regard to Property
W–Weak with Regard to Property

Figure 27. Insulating Materials and Characteristics

[1]Electronic Measurements, pp.15–17, Keithley Instruments, Inc., Cleveland, Ohio, 1977.

*Teflon is a registered trademark of E.I. DuPont Co.
**Kel-F is a registered trademark of 3-M Company.

Guarding the input lines by completely surrounding them with a metal conductor biased near the input lines' potential has two major benefits. First, parasitic leakage from the signal line is reduced since the voltage between the input line and the guard is very low. Second, stray capacitance at the input node is minimized. Input capacitance can substantially degrade signal bandwidth and the stability of the I-to-V converter. The case of the AD549 is connected to Pin 8 so that it can be bootstrapped near the input potential. This minimizes pin leakage and input common-mode capacitance due to the case. Guard schemes for inverting and noninverting amplifier topologies are illustrated in Figures 28 and 29.

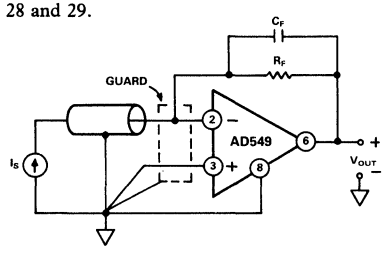


Figure 28. Inverting Amplifier with Guard

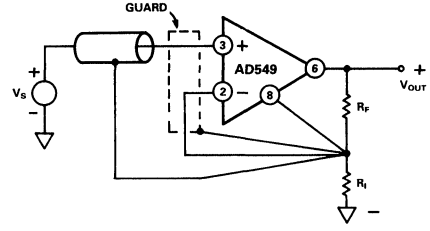


Figure 29. Noninverting Amplifier with Guard

Other guidelines include keeping the circuit layout as compact as possible and input lines short. Keeping the assembly rigid and minimizing sources of vibration will reduce triboelectric and piezoelectric effects. All precision high impedance circuitry requires shielding against interference noise. Low noise coax or triax cables should be used for remote connections to the input signal lines.

OFFSET NULLING

The AD549's input offset voltage can be nulled by using balance Pins 1 and 5, as shown in Figure 30. Nulling the input offset voltage in this fashion will introduce an added input offset voltage drift component of 2.4 μV/°C per millivolt of nulled offset (a maximum additional drift of 0.6 μV/°C for the AD549K, 1.2 μV/°C for the AD549L, 2.4 μV/°C for the AD549J).

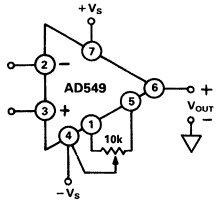


Figure 30. Standard Offset Null Circuit

The approach in Figure 31 can be used when the amplifier is used as an inverter. This method introduces a small voltage referenced to the power supplies in series with the amplifier's positive input terminal. The amplifier's input offset voltage drift with temperature is not affected. However, variation of the power supply voltages will cause offset shifts.

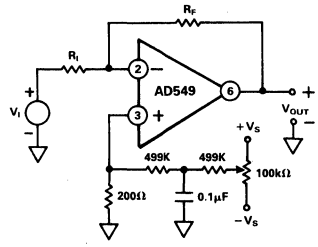


Figure 31. Alternate Offset Null Circuit for Inverter

AC RESPONSE WITH HIGH VALUE SOURCE AND FEEDBACK RESISTANCE

Source and feedback resistances greater than 100 kΩ will magnify the effect of input capacitances (stray and inherent to the AD549) on the ac behavior of the circuit. The effects of common-mode and differential input capacitances should be taken into account since the circuit's bandwidth and stability can be adversely affected.

In a follower, the source resistance and input common-mode capacitance form a pole that limits the bandwidth to $1/2\pi\ R_S C_S$. Bootstrapping the metal case by connecting Pin 8 to the output minimizes capacitance due to the package. Figures 32 and 33 show the follower pulse response from a 1 MΩ source resistance with and without the package connected to the output. Typical common-mode input capacitance for the AD549 is 0.8 pF.

In an inverting configuration, the differential input capacitance forms a pole in the circuit's loop transmission. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1 MΩ appears in Figure 34. Figure 35 shows the response of the same circuit with a 1 pF feedback capacitance. Typical differential input capacitance for the AD549 is 1 pF.

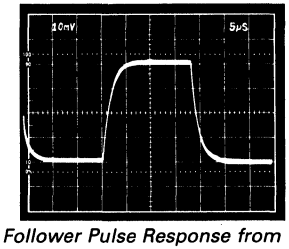


Figure 32. Follower Pulse Response from 1 MΩ Source Resistance, Case Not Bootstrapped

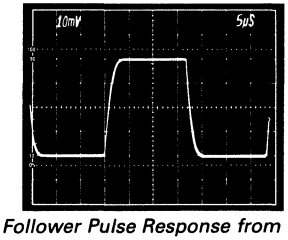


Figure 33. Follower Pulse Response from 1 MΩ Source Resistance, Case Bootstrapped

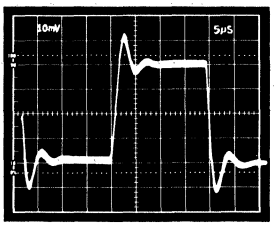


Figure 34. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

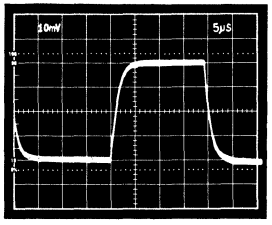


Figure 35. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1pF Feedback Capacitance

COMMON-MODE INPUT VOLTAGE OVERLOAD

The rated common-mode input voltage range of the AD549 is from 3 V less than the positive supply voltage to 5 V greater than the negative supply voltage. Exceeding this range will degrade the amplifier's CMRR. Driving the common-mode voltage above the positive supply will cause the amplifier's output to saturate at the upper limit of output voltage. Recovery time is typically 2 µs after the input has been returned to within the normal operating range. Driving the input common-mode voltage within 1 V of the negative supply causes phase reversal of the output signal. In this case, normal operation is typically resumed within 0.5 µs of the input voltage returning within range.

DIFFERENTIAL INPUT VOLTAGE OVERLOAD

A plot of the AD549's input currents versus differential input voltage (defined as $V_{IN}+ - V_{IN}-$) appears in Figure 36. The input current at either terminal stays below a few hundred femtoamps until one input terminal is forced higher than 1 to 1.5 V above the other terminal. Under these conditions, the input current limits at 30 µA.

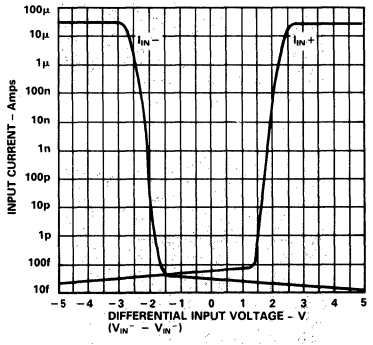


Figure 36. Input Current vs. Differential Input Voltage

INPUT PROTECTION

The AD549 safely handles any input voltage within the supply voltage range. Subjecting the input terminals to voltages beyond the power supply can destroy the device or cause shifts in input current or offset voltage if the amplifier is not protected.

A protection scheme for the amplifier as an inverter is shown in Figure 37. R_P is chosen to limit the current through the inverting input to 1 mA for expected transient (less than 1 second) overvoltage conditions, or to 100 µA for a continuous overload. Since R_P is inside the feedback loop, and is much lower in value than the amplifier's input resistance, it does not affect the inverter's dc gain. However, the Johnson noise of the resistor will add root sum of squares to the amplifier's input noise.

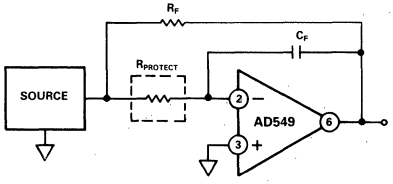


Figure 37. Inverter with Input Current Limit

In the corresponding version of this scheme for a follower, shown in Figure 38, R_P and the capacitance at the positive input terminal will produce a pole in the signal frequency response at a $f = 1/2\pi RC$. Again, the Johnson noise R_P will add to the amplifier's input voltage noise.

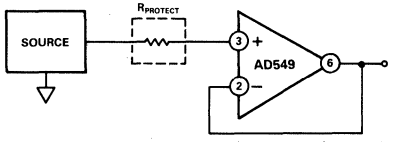


Figure 38. Follower with Input Current Limit

Figure 39 is a schematic of the AD549 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Low leakage diodes, such as the FD333's should be used, and should be shielded from light to keep photocurrents from being generated. Even with these precautions, the diodes will measurably increase the input current and capacitance.

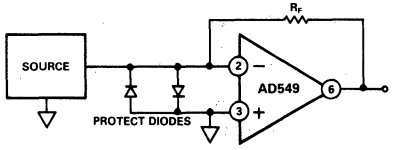


Figure 39. Input Voltage Clamp with Diodes

SAMPLE AND DIFFERENCE CIRCUIT TO MEASURE ELECTROMETER LEAKAGE CURRENTS

There are a number of methods used to test electrometer leakage currents, including current integration and direct current to voltage conversion. Regardless of the method used, board and interconnect cleanliness, proper choice of insulating materials (such as Teflon or Kel-F), correct guarding and shielding techniques and care in physical layout are essential to making accurate leakage measurements.

Figure 40 is a schematic of the sample and difference circuit. It uses two AD549 electrometer amplifiers (A and B) as current-to-voltage converters with high value (10^{10} Ω) sense resistors (RSa and RSb). R1 and R2 provide for an overall circuit sensitivity of 10 fA/mV (10 pA full scale). C_C and C_F provide noise suppression and loop compensation. C_C should be a low leakage polystyrene capacitor. An ultralow leakage Kel-F test socket is used for contacting the device under test. Rigid Teflon coaxial cable is used to make connections to all high impedance nodes. The use of rigid coax affords immunity to error induced by mechanical vibration and provides an outer conductor for shielding. The entire circuit is enclosed in a grounded metal box.

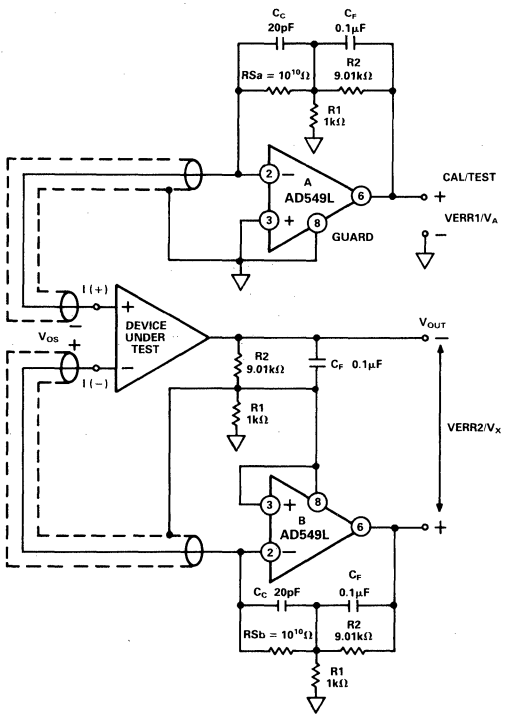


Figure 40. Sample and Difference Circuit for Measuring Electrometer Leakage Currents

The test apparatus is calibrated without a device under test present. A five minute stabilization period after the power is turned on is required. First, V_{ERR1} and V_{ERR2} are measured. These voltages are the errors caused by offset voltages and leakage currents of the current to voltage converters.

$$V_{ERR1} = 10\ (V_{OS}A - I_BA \times RSa)$$
$$V_{ERR2} = 10\ (V_{OS}B - I_BB \times RSb)$$

Once measured, these errors are subtracted from the readings taken with a device under test present. Amplifier B closes the feedback loop to the device under test, in addition to providing current to voltage conversion. The offset error of the device under test appears as a common-mode signal and does not affect the test measurement. As a result, only the leakage current of the device under test is measured.

$$V_A - V_{ERR1} = 10[RSa \times I_B(+)]$$
$$V_X - V_{ERR2} = 10[RSb \times I_B(-)]$$

Although a series of devices can be tested after only one calibration measurement, calibration should be updated periodically to compensate for any thermal drift of the current to voltage converters or changes in the ambient environment. Laboratory results have shown that repeatable measurements within 10 fA can be realized when this apparatus is properly implemented. These results are achieved in part by the design of the circuit, which eliminates relays and other parasitic leakage paths in the high impedance signal lines, and in part by the inherent cancellation of errors through the calibration and measurement procedure.

PHOTODIODE INTERFACE

The AD549's low input current and low input offset voltage make it an excellent choice for very sensitive photodiode preamps (Figure 41). The photodiode develops a signal current, I_S equal to:

$$I_S = R \times P$$

where P is light power incident on the diode's surface in Watts and R is the photodiode responsivity in Amps/Watt. R_F converts the signal current to an output voltage:

$$V_{OUT} = R_F \times I_S$$

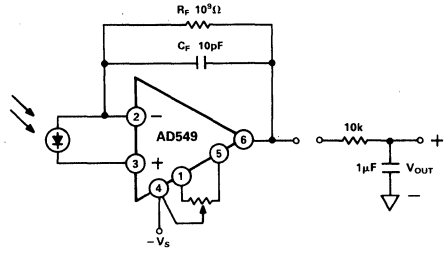


Figure 41. Photodiode Preamp

DC error sources and an equivalent circuit for a small area (0.2 mm square) photodiode are indicated in Figure 42.

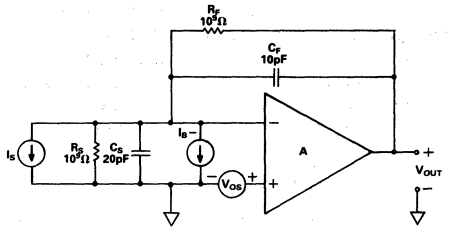


Figure 42. Photodiode Preamp DC Error Sources

Input current, I_B, will contribute an output voltage error, V_{E1}, proportional to the feedback resistance:

$$V_{E1} = I_B \times R_F$$

The op amp's input voltage offset will cause an error current through the photodiode's shunt resistance, R_S:

$$I = V_{OS}/R_S$$

The error current will result in an error voltage (V_{E2}) at the amplifier's output equal to:

$$V_{E2} = (1+R_F/R_S)\, V_{OS}$$

Given typical values of photodiode shunt resistance (on the order of 10^9 Ω), R_F/R_S can easily be greater than one, especially if a large feedback resistance is used. Also, R_F/R_S will increase with temperature, as photodiode shunt resistance typically drops by a factor of two for every 10°C rise in temperature. An op amp with low offset voltage and low drift must be used in order to maintain accuracy. The AD549K offers guaranteed maximum 0.25 mV offset voltage, and 5 mV/°C drift for very sensitive applications.

Photodiode Preamp Noise

Noise limits the signal resolution obtainable with the preamp. The output voltage noise divided by the feedback resistance is the minimum current signal that can be detected. This minimum detectable current divided by the responsivity of the photodiode represents the lowest light power that can be detected by the preamp.

Noise sources associated with the photodiode, amplifier, and feedback resistance are shown in Figure 43; Figure 44 is the spectral density versus frequency plot of each of the noise source's contribution to the output voltage noise (circuit parameters in Figure 42 are assumed). Each noise source's rms contribution to the total output voltage noise is obtained by integrating the square of its spectral density function over frequency. The rms value of the output voltage noise is the square root of the sum of all contributions. Minimizing the total area under these curves will optimize the preamplifier's resolution for a given bandwidth.

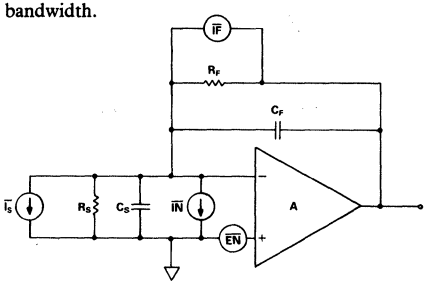


Figure 43. Photodiode Preamp Noise Sources

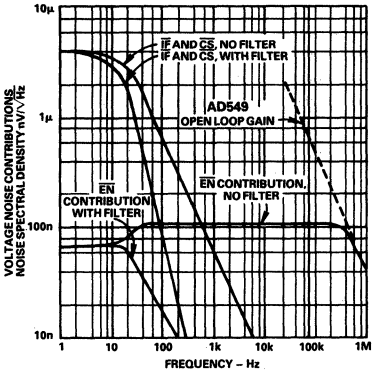


Figure 44. Photodiode Preamp Noise Sources' Spectral Density vs. Frequency

The photodiode preamp in Figure 41 can detect a signal current of 26 fA rms at a bandwidth of 16 Hz, which assuming a photodiode responsivity of 0.5 A/W, translates to a 52 fW rms minimum detectable power. The photodiode used has a high source resistance and low junction capacitance. C_F sets the signal bandwidth with R_F and also limits the "peak" in the noise gain that multiplies the op amp's input voltage noise contribution. A single pole filter at the amplifier's output limits the op amp's output voltage noise bandwidth to 26 Hz, a frequency comparable to the signal bandwidth. This greatly improves the preamplifier's signal to noise ratio (in this case, by a factor of three).

Log Ratio Amplifier

Logarithmic ratio circuits are useful for processing signals with wide dynamic range. The AD549L's 60 fA maximum input current makes it possible to build a log ratio amplifier with 1% log conformance for input current ranging from 10 pA to 1 mA, a dynamic range of 160 dB.

The log ratio amplifier in Figure 45 provides an output voltage proportional to the log base 10 of the ratio of the input currents I1 and I2. Resistors R1 and R2 are provided for voltage inputs. Since NPN devices are used in the feedback loop of the front-end amplifiers that provide the log transfer function, the output is valid only for positive input voltages and input currents. The input currents set the collector currents IC1 and IC2 of a matched pair of log transistors Q1 and Q2 to develop voltages VA and VB:

$$VA, B = -(kT/q) \ln IC/IES$$

where IES is the transistors' saturation current.

The difference of VA and VB is taken by the subtractor section to obtain:

$$VC = (kT/q) \ln (IC2/IC1)$$

VC is scaled up by the ratio of (R9+R10)/R8, which is equal to approximately 16 at room temperature, resulting in the output voltage:

$$V_{OUT} = 1 \times \log (IC2/IC1)\ V.$$

R8 is a resistor with a positive 3500 ppm/°C temperature coefficient to provide the necessary temperature compensation. The parallel combination of R15 and R7 is provided to keep the subtractor section's gain for positive and negative inputs matched over temperature.

Frequency compensation is provided by R11, R12, and C1 and C2. The bandwidth of the circuit is 300 kHz at input signals greater than 50 μA, and decreases smoothly with decreasing signal levels.

To trim the circuit, set the input currents to 10 μA and trim A3's offset using the amplifier's trim potentiometer so the output equals 0. Then set I1 to 1 μA and adjust the output to equal 1 V by trimming R10. Additional offset trims on the amplifiers A1 and A2 can be used to increase the voltage input accuracy and dynamic range.

The very low input current of the AD549 makes this circuit useful over a very wide range of signal currents. The total input current (which determines the low level accuracy of the circuit) is the sum of the amplifier input current, the leakage across the compensating capacitor (negligible if polystyrene or Teflon capacitor is used), and the collector to collector, and collector to base leakages of one side of the dual log transistors. The magnitude of these last two leakages depend on the amplifier's input offset voltage and are typically less than 10 fA with 1 mV offsets. The low level accuracy is limited primarily by the amplifier's input current, only 60 fA maximum when the AD549L is used.

The effects of the emitter resistance of Q1 and Q2 can degrade the circuit's accuracy at input currents above 100 μA. The networks composed of R13, D1, R16, and R14, D2, R17 compensate for these errors, so that this circuit has less than 1% log conformance error at 1 mA input currents. The correct value for R13 and R14 depends on the type of log transistors used. 49.9 kΩ resistors were chosen for use with LM394 transistors. Smaller resistance values will be needed for smaller log transistors.

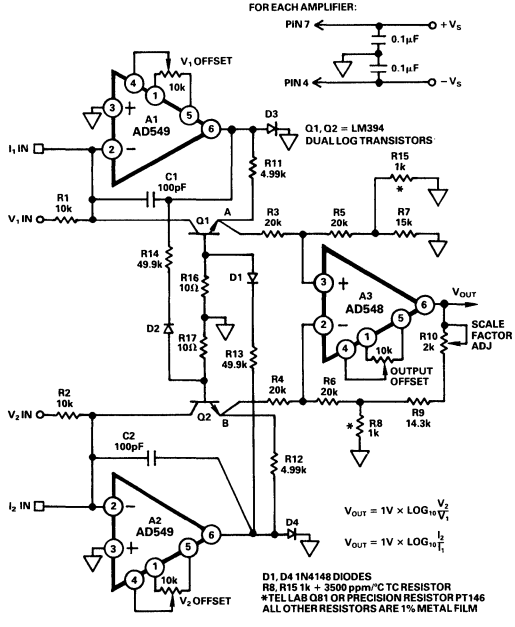


Figure 45. Log Ratio Amplifier

TEMPERATURE COMPENSATED pH PROBE AMPLIFIER

A pH probe can be modeled as a mV-level voltage source with a series source resistance dependent upon the electrode's composition and configuration. The glass bulb resistance of a typical pH electrode pair falls between 10^6 and 10^9 Ω. It is therefore important to select an amplifier with low enough input currents such that the voltage drop produced by the amplifier's input bias current and the electrode resistance does not become an appreciable percentage of a pH unit.

The circuit in Figure 46 illustrates the use of the AD549 as a pH probe amplifier. As with other electrometer applications, the use of guarding, shielding, Teflon standoffs, etc., is a must in order to capitalize on the AD549's low input current. If an AD549L (60 fA max input current) is used, the error contributed by input current will be held below 60 μV for pH electrode source impedances up to 10^9 Ω. Input offset voltage (which can be trimmed) will be below 0.5 mV.

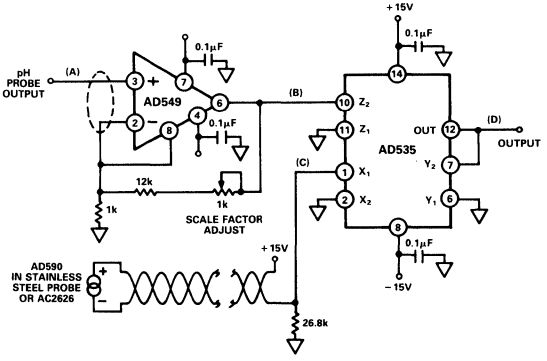


Figure 46. Temperature Compensated pH Probe Amplifier

The pH probe output is ideally zero volts at a pH of 7 independent of temperature. The slope of the probe's transfer function, though predictable, is temperature dependent (−54.2 mV/pH at 0 and −74.04 mV/pH at 100°C). By using an AD590 temperature sensor and an AD535 analog divider, an accurate temperature compensation network can be added to the basic pH probe amplifier. The table in Figure 47 shows voltages at various points and illustrates the compensation. The AD549 is set for a noninverting gain of 13.51. The output of the AD590 circuitry (point C) will be equal to 10 V at 100°C and decrease by 26.8 mV/°C. The output of the AD535 analog divider (point D) will be a temperature compensated output voltage centered at zero volts for a pH of 7, and having a transfer function of −1.00V/pH unit. The output range spans from −7.00 V (pH=14) to +7.00 V (pH=0).

PROBE TEMP	A (PROBE OUTPUT)	B (A×13.51)	C (590 OUTPUT)	D (10 B/C)
0	54.20 mV	0.732 V	7.32 V	1.00 V
25°C	59.16 mV	0.799 V	7.99 V	1.00 V
37°C	61.54 mV	0.831 V	8.31 V	1.00 V
60°C	66.10 mV	0.893 V	8.93 V	1.00 V
100°C	74.04 mV	1.000 V	10.00 V	1.00 V

Figure 47. Table Illustrating Temperature Compensation

ANALOG DEVICES

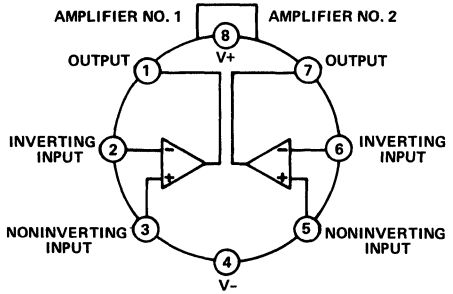
Precision, Low Cost Dual BiFET Op Amp

AD642

FEATURES

Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Current
Crosstalk-124dB at 1kHz
Low Bias Current: 35pA max Warmed Up
Low Offset Voltage: 500μV max
Low Input Voltage Noise: 2μV p-p
High Open Loop Gain
Low Quiescent Current: 2.8mA max
Low Total Harmonic Distortion
Standard Dual Amplifier Pin Out
Available in Hermetic Metal Can Package and Chip Form
MIL-STD-883B Processing Available
Single Version Available: AD542

AD642 PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TOP VIEW

PRODUCT DESCRIPTION

The AD642 is a pair of matched high speed monolithic BiFET operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max matched to 25pA for the AD642K and L; 75pA max, matched to 35pA for the AD642J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV and matched to 0.25mV for the AD642L, 1.0mV and matched to 0.5mV for the AD642K, utilizing Analog's laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This optimizes the process to product matched bias currents which have lower initial bias currents than other popular BiFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and combined with superior IC processing guarantees offset voltage tracking over the temperature range.

The AD642 is recommended for applications in which excellent ac and dc performance is required. The matched amplifiers provide a low-cost solution for true instrumentation amplifiers, log ratio amplifiers, and output amplifiers for four quadrant multiplying D/A converters such as the AD7541.

The AD642 is available in four versions: the "J", "K" and "L," all specified over the 0 to +70°C temperature range and one version, "S," over the -55°C to +125°C extended operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can or available in chip form.

PRODUCT HIGHLIGHTS

1. The AD642 has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD642 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max and matched side to side to 0.25mV (AD642L), thus eliminating the need for external nulling.
4. Low voltage noise (2μV, p-p), and high open loop gain enhance the AD642's performance as a precision op amp.
5. The standard dual amplifier pin out allows the AD642 to replace lower performance duals without redesign.
6. The AD642 is available in chip form.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD642J Min	AD642J Typ	AD642J Max	AD642K Min	AD642K Typ	AD642K Max	AD642L Min	AD642L Typ	AD642L Max	AD642S Min	AD642S Typ	AD642S Max	Units
OPEN LOOP GAIN													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			**250,000**			**250,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		V/μs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			3.5	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			200			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			3.5	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±15	±5		±15	±5		±15	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
TRANSISTOR COUNT		58			58			58			58		
PACKAGE OPTION[5]													
TO-99 Style (H-08B)		AD642JH			AD642KH			AD642LH			AD642SH		

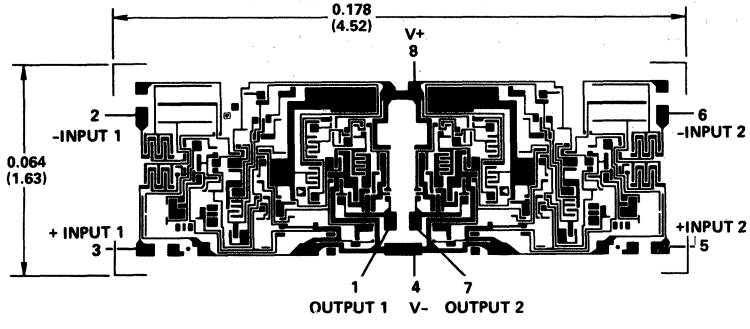
NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.
[5]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm)



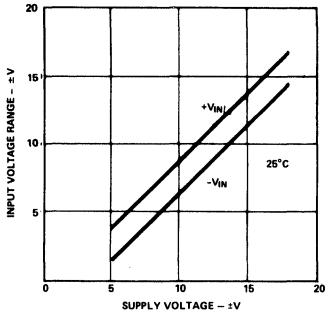


Figure 1. Input Voltage Range vs. Supply Voltage

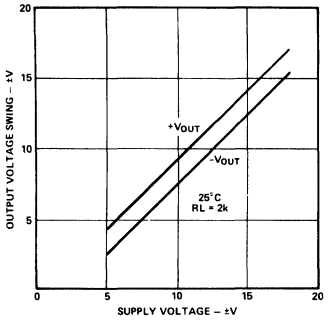


Figure 2. Output Voltage Swing vs. Supply Voltage

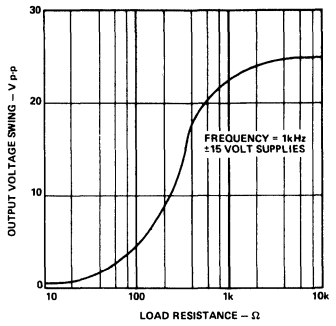


Figure 3. Output Voltage Swing vs. Load Resistance

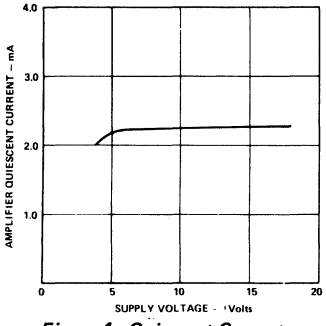


Figure 4. Quiescent Current vs. Supply Voltage

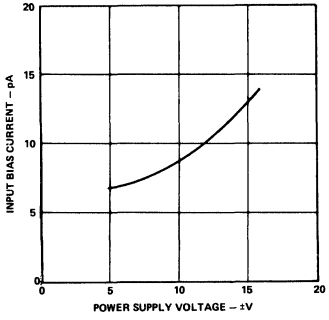


Figure 5. Input Bias Current vs. Power Supply Voltage

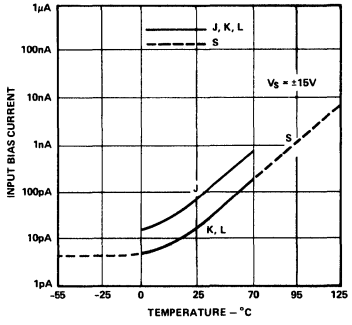


Figure 6. Input Bias Current vs. Temperature

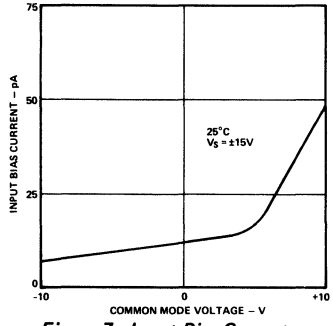


Figure 7. Input Bias Current vs. CMV

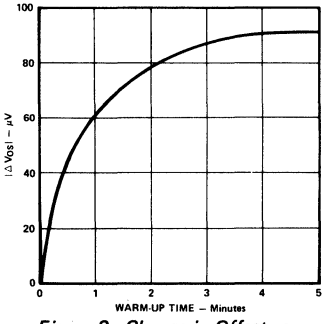


Figure 8. Change in Offset vs. Warm-Up Time

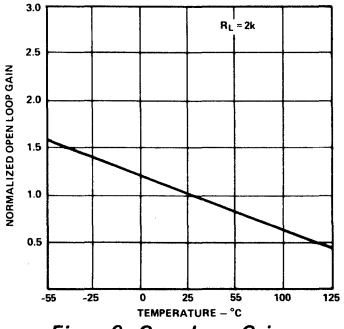


Figure 9. Open Loop Gain vs. Temperature

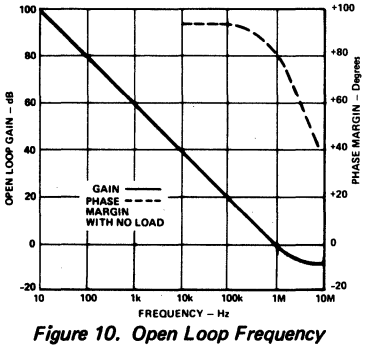


Figure 10. Open Loop Frequency Response

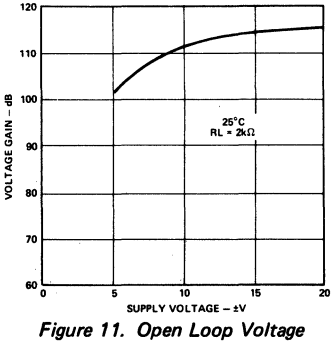


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

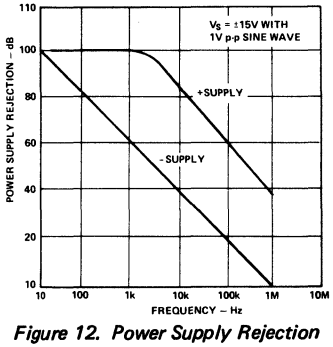


Figure 12. Power Supply Rejection vs. Frequency

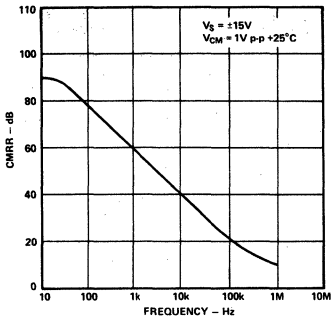


Figure 13. Common Mode Rejection Ratio vs. Frequency

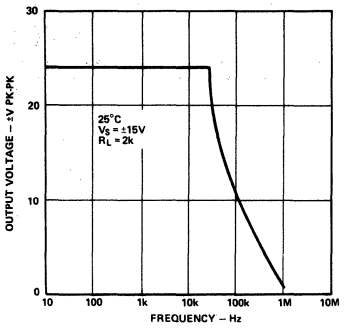


Figure 14. Large Signal Frequency Response

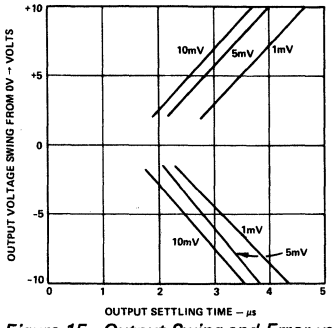


Figure 15. Output Swing and Error vs. Output Settling Time (Circuit of Figure 23)

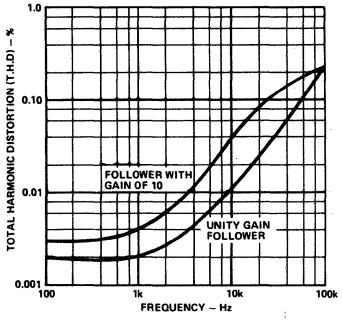


Figure 16. Total Harmonic Distortion vs. Frequency

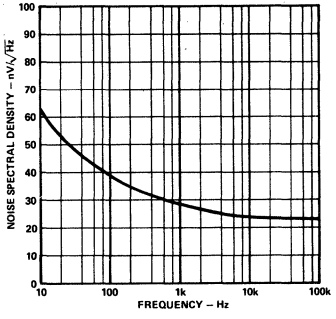


Figure 17. Input Noise Voltage Spectral Density

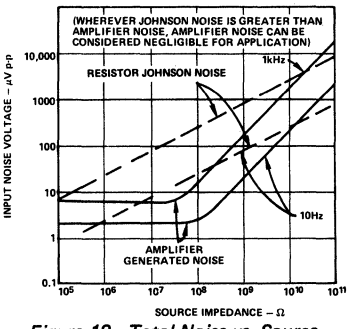
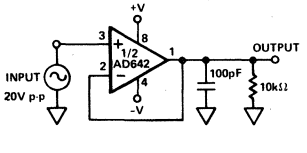
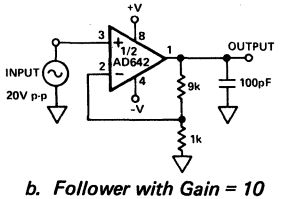


Figure 18. Total Noise vs. Source Impedance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

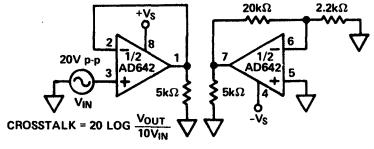


Figure 20. Crosstalk Test Circuit

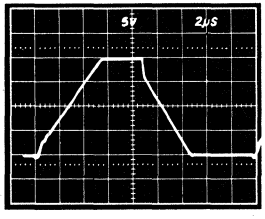


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

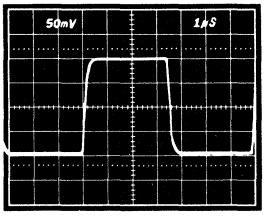


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

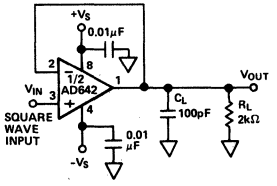


Figure 21c. Unity Gain Follower

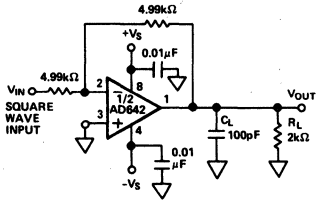


Figure 22a. Unity Gain Inverter

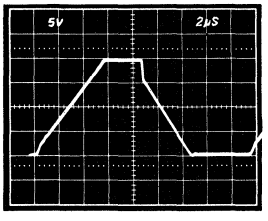


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

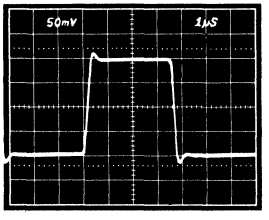


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

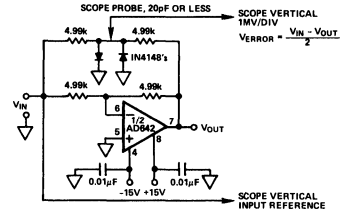


Figure 23. Settling Time Test Circuit

Fast settling time (8μs to 0.01% for 20V p-p step), low power and low offset voltage make the AD642 an excellent choice for use as an output amplifier for current output D/A converters such as the AD7541.

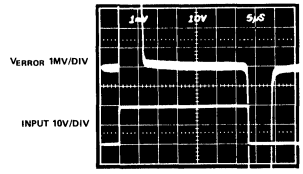
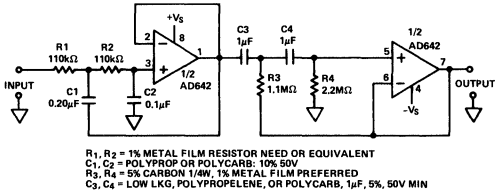


Figure 24. Settling Characteristic Detail

The upper trace of the oscilloscope photograph of Figure 24 shows the settling characteristic of the AD642. The lower trace represents the input to Figure 23. The AD642 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain optimum settling time.



R1, R2 = 1% METAL FILM RESISTOR NEED OR EQUIVALENT
C1, C2 = POLYPROP OR POLYCARB: 10% 50V
R3, R4 = 5% CARBON 1/4W, 1% METAL FILM PREFERRED
C3, C4 = LOW LKG, POLYPROPELENE, OR POLYCARB, 1μF, 5%, 50V MIN

Figure 25. 0.1Hz to 10Hz 2nd Order Bandpass Filter, Maximally Flat

The low frequency (1/f) noise has a power spectrum that is inversely proportional to frequency. Typically this noise is not important above 10Hz, but it can be important for low frequency-high gain applications.

The low noise characteristics of the AD642 make it ideal for 1/f noise testing circuits. The circuit of Figure 25 is a 0.1Hz to 10Hz bandpass filter with second order filter characteristics.

The circuit illustrated in Figure 26 uses two AD642s to construct an instrumentation amplifier with low input current (35pA max), high linearity and low offset voltage and offset voltage drift. The AD644 may be substituted for increased speed, but the higher open-loop gain of the AD642 maintains better linearity over the gain range of 1 to 1000. Amplifier A1 is an AD642L for low input offset voltage (250μV max) and low input offset voltage drift at high gains because matching and tracking are very important for the balanced input stage. Amplifier A2 serves two nonrelated functions, output amplifier and active data-guard drive, and does not require close matching between sections; thus it may be an AD642J.

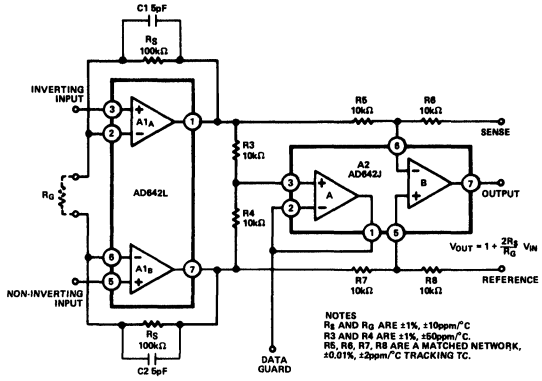
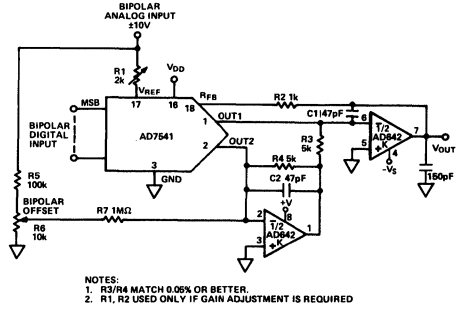


Figure 26. Precision FET Input Instrumentation Amplifier

The output impedance of a CMOS DAC varies with the digital word thus changing the noise of the amplifier circuit. This effect will cause a nonlinearity whose magnitude is dependent on the offset voltage of the amplifier. The AD642K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD642.



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED

Figure 27a. AD642 Used as DAC Output Amplifier

Figure 27a illustrates the AD7541 12-bit digital-to-analog converter, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplication.

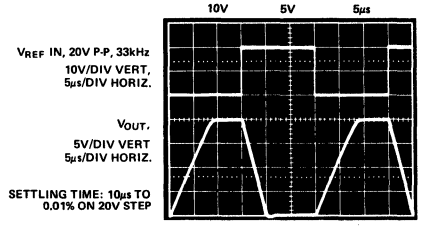


Figure 27b. Voltage Output DAC Settling Characteristic

The photo above shows the output of the circuit of Figure 27a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC. The 47pF capacitor across the feedback

resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

Log amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD642 make it suitable for wide dynamic range log amplifiers. Figure 28 is a schematic of a log ratio circuit employing the AD642 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100μA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

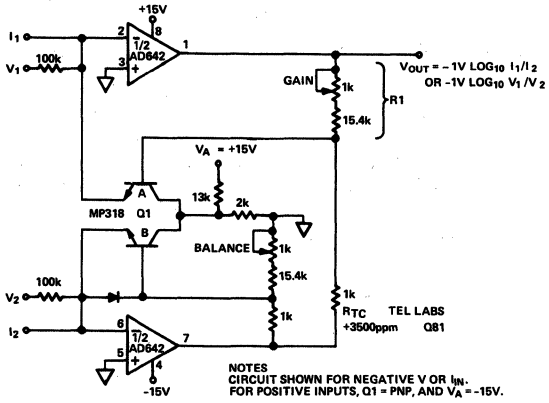


Figure 28. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

The low input bias current (35pA) and low noise characteristics of the AD642 make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD642 can deliver. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid shielded cables.

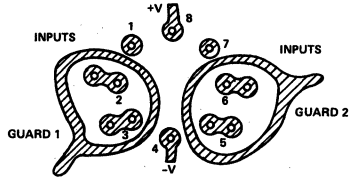


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD642 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±0.5 volts while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the AD642 suitable for low speed voltage comparators directly connected to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD642 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.

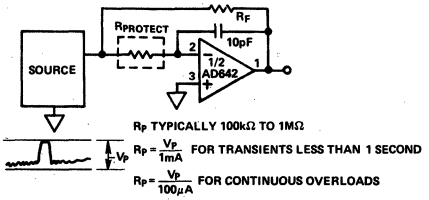


Figure 30. AD642 Input Protection

ANALOG DEVICES

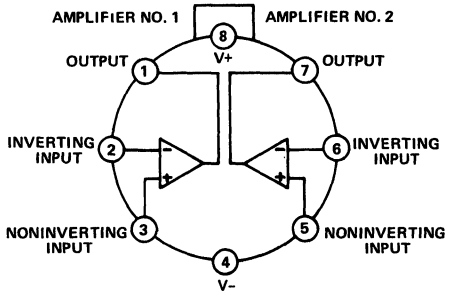
Dual High Speed, Implanted BiFET Op Amp

AD644

FEATURES

Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Currents
Crosstalk -124dB at 1kHz
Low Bias Current: 35pA max Warmed Up
Low Offset Voltage: 500μV max
Low Input Voltage Noise: 2μV p-p
High Slew Rate: 13V/μs
Low Quiescent Current: 4.5mA max
Fast Settling to ±0.01%: 3μs
Low Total Harmonic Distortion: 0.0015% at 1kHz
Standard Dual Amplifier Pin Out
Available in Hermetic Metal Can Package and Chip Form
MIL-STD-883B Processing Available
Single Version Available: AD544

AD644 PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TOP VIEW

PRODUCT DESCRIPTION

The AD644 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser-trimming technologies. The AD644 offers matched bias currents that are significantly lower than currently available monolithic dual BiFET operational amplifiers: 35pA max, matched to 25pA for the AD644K and L, 75pA max matched to 35pA for the AD644J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV, and matched to 0.25mV for the AD644L, 1.0mV and matched to 0.5mV for the AD644K, utilizing Analog Devices' laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This process optimizes the ability to produce matched amplifiers which have lower initial bias currents than other popular BiFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and superior IC processing guarantees offset voltage tracking over the temperature range.

The AD644 is recommended for applications in which both excellent ac and dc performance is required. The matched amplifiers provide a low cost solution to true wideband instrumentation amplifiers, low dc drift active filters and output amplifiers for four quadrant multiplying D/A converters such as the AD7541, 12-bit CMOS DAC.

The AD644 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically sealed, TO-99 metal can or available in chip form.

PRODUCT HIGHLIGHTS

1. The AD644 has tight side to side matching specifications to ensure high performance without matching individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD644 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max matched side to side to 0.25mV (AD644L), thus eliminating the need for external nulling.
4. Improved bipolar and JFET processing on the AD644 result in the lowest matched bias current available in a high speed monolithic FET op amp.
5. Low voltage noise (2μV p-p) and high open loop gain enhance the AD644's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD644 ideal for D/A, A/D, sample-hold circuits and dual high speed integrators.
7. Low harmonic distortion (0.0015%) and low crosstalk (-124dB) make the AD644 an ideal choice for stereo audio applications.
8. The standard dual amplifier pin out allows the AD644 to replace lower performance duals without redesign.
9. The AD644 is available in chip form.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD644J Min	AD644J Typ	AD644J Max	AD644K Min	AD644K Typ	AD644K Max	AD644L Min	AD644L Typ	AD644L Max	AD644S Min	AD644S Typ	AD644S Max	Units
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**30,000**			**50,000**			**50,000**			**50,000**			V/V
T_{min} to T_{max}, R_L = 2kΩ	20,000			**40,000**			**40,000**			**20,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ R_L = 10kΩ, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		2.0			2.0			2.0			2.0		MHz
Full Power Response		200			200			200			200		kHz
Slew Rate, Unity Gain	**8.0**	13.0		**8.0**	13.0		**8.0**	13.0		**8.0**	13.0		V/μs
Total Harmonic Distortion		0.0015			0.0015			0.0015			0.0015		%
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			3.5	mV
Input Offset Voltage vs. Suppl;, T_{min} to T_{max}			200			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		10			5			5			5		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			3.5	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		10^{12}‖6			10^{12}‖6			10^{12}‖6			10^{12}‖6		MΩ‖pF
Common Mode		10^{12}‖3			10^{12}‖3			10^{12}‖3			10^{12}‖3		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		35			35			35			35		nV/√Hz
f = 100Hz		22			22			22			22		nV/√Hz
f = 1kHz		18			18			18			18		nV/√Hz
f = 10kHz		16			16			16			16		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		3.5	**4.5**		3.5	**4.5**		3.5	**4.5**		3.5	**4.5**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[5]													
TO-99 Style (H-08B)		AD644JH			AD644KH			AD644LH			AD644SH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

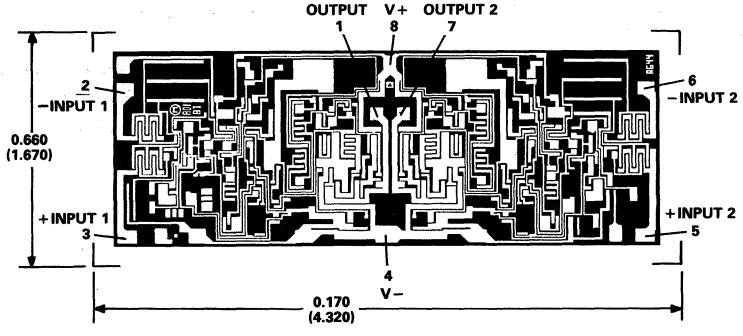
[5]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



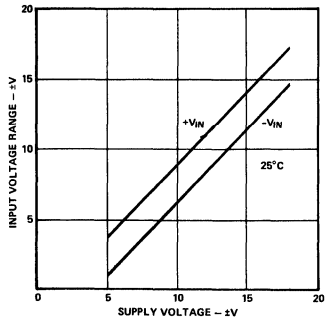


Figure 1. Input Voltage Range vs. Supply Voltage

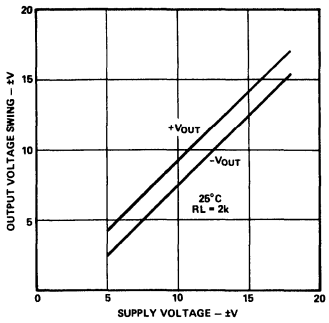


Figure 2. Output Voltage Swing vs. Supply Voltage

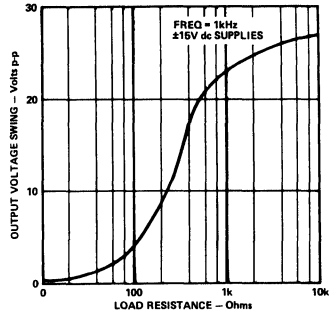


Figure 3. Output Voltage Swing vs. Load Resistance

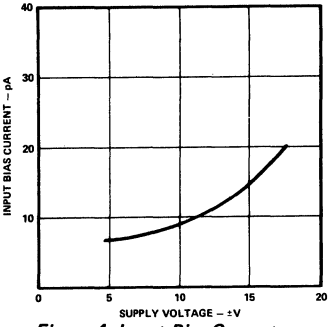


Figure 4. Input Bias Current vs. Supply Voltage

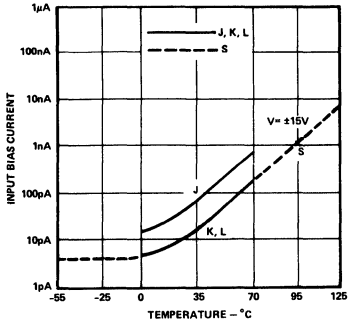


Figure 5. Input Bias Current vs. Temperature

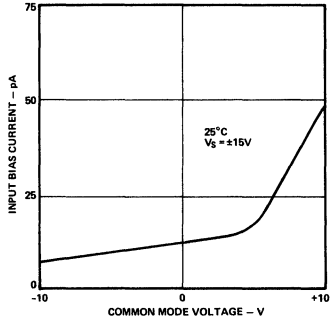


Figure 6. Input Bias Current vs. CMV

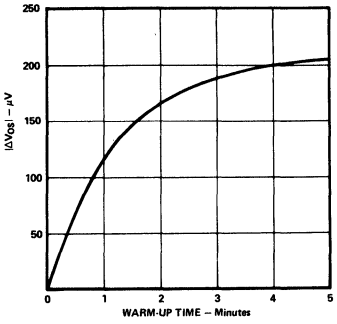


Figure 7. Change in Offset Voltage vs. Warm-Up Time

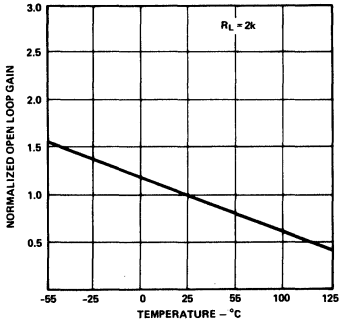


Figure 8. Open Loop Gain vs. Temperature

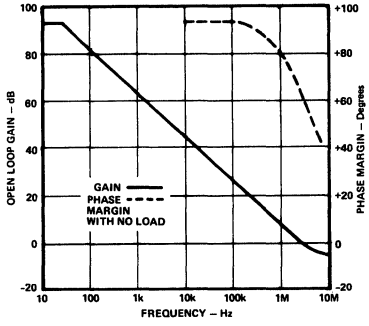


Figure 9. Open Loop Frequency Response

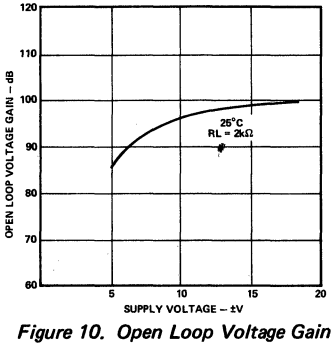


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

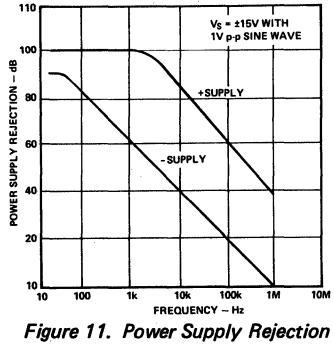


Figure 11. Power Supply Rejection vs. Frequency

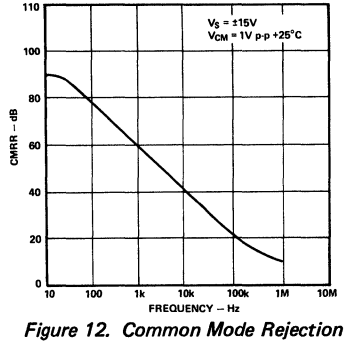


Figure 12. Common Mode Rejection Ratio vs. Frequency

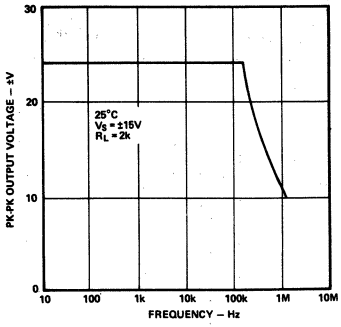


Figure 13. Large Signal Frequency Response

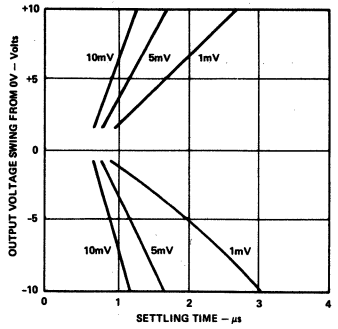


Figure 14. Output Swing and Error vs. Settling Time (Circuit of Figure 23a)

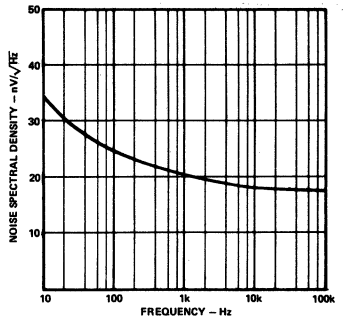


Figure 15. Noise Spectral Density

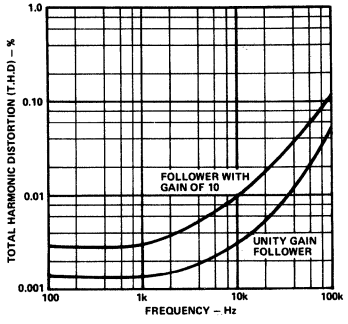


Figure 16. Total Harmonic Distortion vs. Frequency

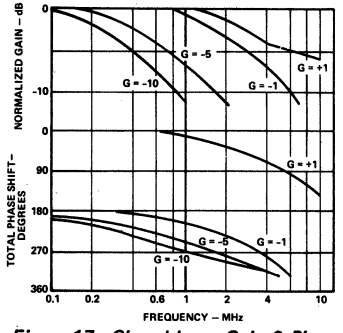


Figure 17. Closed Loop Gain & Phase vs. Frequency

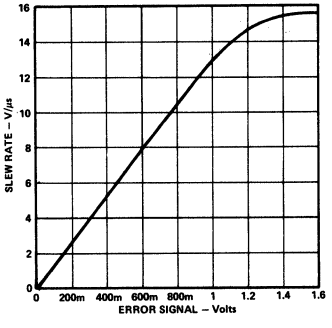
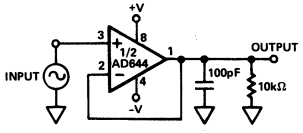
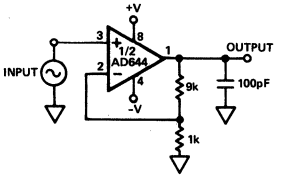


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

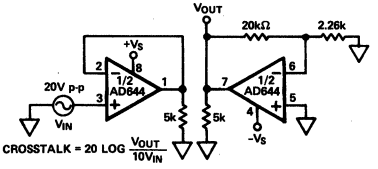


Figure 20. Crosstalk Test Circuit

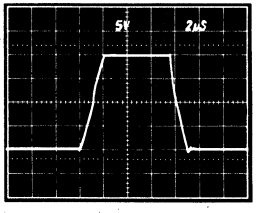


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

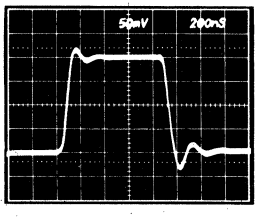


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

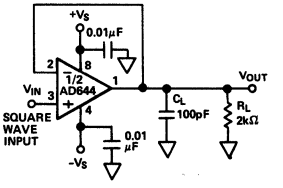


Figure 21c. Unity Gain Follower

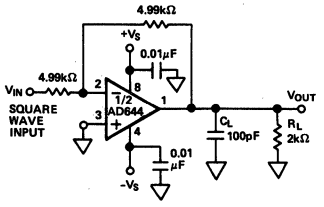


Figure 22a. Unity Gain Inverter

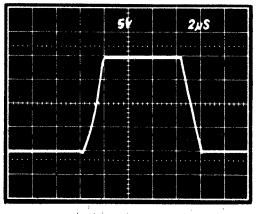


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

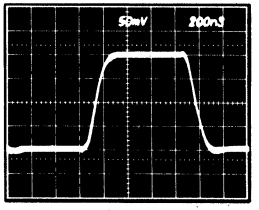


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

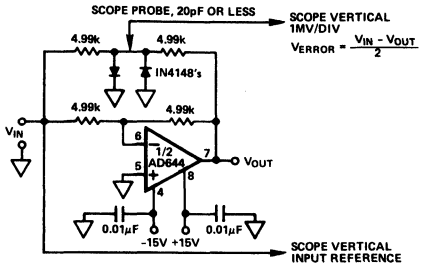


Figure 23a. Settling Time Test Circuit

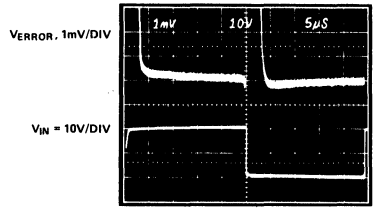


Figure 23b. Settling Characteristic Detail

The fast settling time (3.0μs to 0.01% for 20V p-p step) and low offset voltage make the AD644 an excellent choice as an output amplifier for current output D/A converters such as the AD7541. The upper trace of the oscilloscope photograph of Figure 23b shows the settling characteristics of the AD644. The lower trace represents the input to Figure 23a. The AD644 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

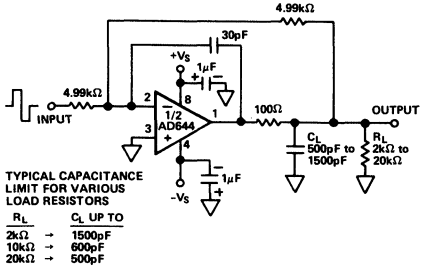
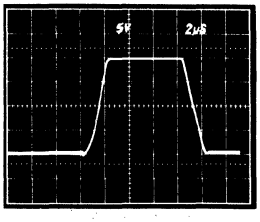


Figure 24. Circuit for Driving a Large Capacitive Load



Transient Response $R_L = 2k\Omega$ $C_L = 500pF$

The circuit in Figure 24 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

The low input bias current (35pA), low noise, high slew rate and high bandwidth characteristics of the AD644 make it suitable for electrometer applications such as photodiode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD644 can deliver. The input guarding scheme shown in Figure 25 will minimize leakage as much as possible. The same layout should be used on both sides of a double side board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, such conductors should be replaced by rigid shielded cables.

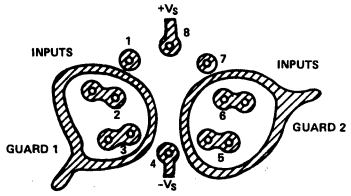


Figure 25. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD644 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±1 volt while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the AD644 suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD644 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 26 shows proper connections.

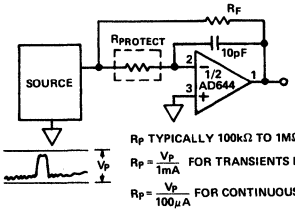


Figure 26. AD644 Input Protection

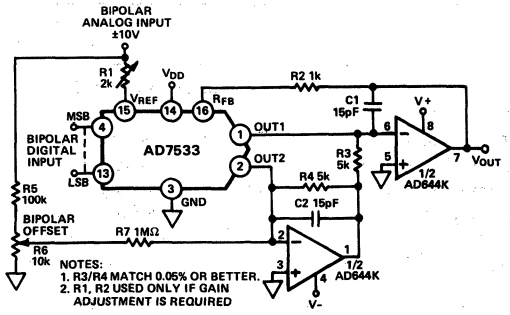


Figure 27a. AD644 Used as DAC Output Amplifiers

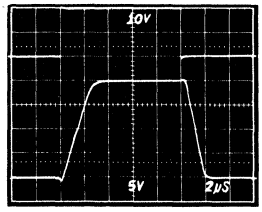


Figure 27b. Large Signal Response

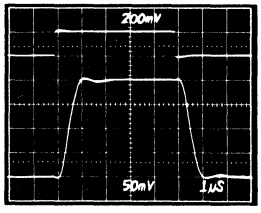


Figure 27c. Small Signal Response

Figure 27a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. The photos exhibit the response to a step input at V_{REF}. Figure 27b is the large signal response and Figure 27c is the small signal response.

The output impedance of a CMOS DAC varies with the digital word thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The AD644K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD644.

ACTIVE FILTERS

Literature on active filter techniques and characteristics based on operational amplifiers is readily available. The successful application of an active filter however, depends on the component selection to achieve the desired performance. The AD644 is recommended for filters in medical, instrumentation, data acquisition and audio applications, because of its high gain bandwidth figure, symmetrical slewing, low noise, and low offset voltage.

The state variable filter (Figure 28) is stable, easily tuned and is independent of circuit Q and gain. The use of the AD644 with its low input bias current simplifies the resistor (R3, R4) selection for the passband center frequency, circuit Q and voltage gain.

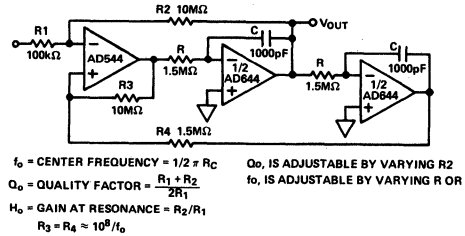


Figure 28. Band Pass State Variable Filter

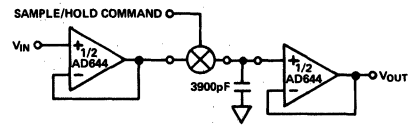


Figure 29. Sample and Hold Circuit

The sample and hold circuit, shown in Figure 29 is suitable for use with 8-bit A/D converters. The acquisition time using a 3900pF capacitor and fast CMOS SPST (ADG200) switch is 15μs.

The droop rate is very low 25×10^{-9} V/μs due to the low input bias currents of the AD644. Care should be taken to minimize leakage paths. Leakages around the hold capacitor will increase the droop rate and degrade performance.

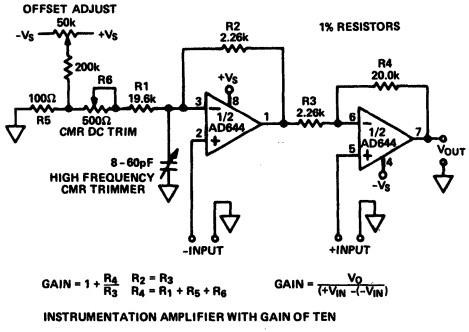


Figure 30. Wide Bandwidth Instrumentation Amplifier

The AD644 in the circuit of Figure 30 provides highly accurate signal conditioning with high frequency input signals. It provides an offset voltage drift of 10μV/°C, CMRR of 80dB over the range of dc to 10kHz and a bandwidth of 200kHz (-3dB) at 1V p-p output. The circuit of Figure 30 can be configured for a gain range of 2 to 1000 with a typical nonlinearity of 0.01% at a gain of 10.

ANALOG DEVICES

Low Noise, Precision, FET Op Amp

AD645

FEATURES

Improved Replacement for Burr-Brown OPA-111 and OPA-121 Op Amp

LOW NOISE

2.5 μV p–p max, 0.1 Hz to 10 Hz
20 nV/√Hz max at 100 Hz
11 fA p–p Current Noise 0.1 Hz to 10 Hz

HIGH DC ACCURACY

250 μV max Offset Voltage
5 μV/°C max Drift
1.5 pA max Input Bias Current
114 dB min Open-Loop Gain

AC PERFORMANCE

2 V/μs Slew Rate
2 MHz Unity-Gain Bandwidth
Available in Plastic Mini-DIP or 8-Pin Header Packages.
Both MIL-STD-883B and Plus Processing Are Available.

APPLICATIONS

Low Noise Photodiode Preamps
CT Scanners

PRODUCT DESCRIPTION

The AD645 is a low noise, precision, FET input, monolithic operational amplifier. It offers both the low voltage noise of a bipolar input op amp and the very low bias current of a FET-input device. The 10^{14} Ω common-mode impedance insures that input bias current is essentially independent of common-mode voltage variations.

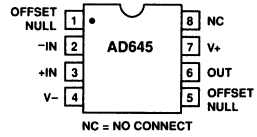
The AD645 has both excellent dc performance and a guaranteed and tested maximum input voltage noise. It features 1.5 pA maximum input bias current and 250 μV maximum offset voltage.

The AD645 is useful for many high input impedance, low noise applications. It is available in five performance grades. The AD645J and AD645K are rated over the commercial temperature range of 0 to +70°C. The AD645A and AD645B are rated over the industrial temperature of −40°C to +85°C. The AD645S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B.

The AD645 is available in 8-pin plastic mini-DIP, 8-pin header, or in chip form.

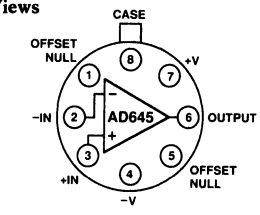
AD645 CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package



TO-99 (H) Package

Top Views



NOTE: CASE IS CONNECTED TO PIN #8

PRODUCT HIGHLIGHTS

1. The guaranteed and tested low frequency noise level makes the AD645 suitable for many low noise applications where a FET input op amp is needed.
2. The low input bias current of 1.5 pA allows the AD645 to be used for amplifying the output of high impedance sources.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD645J/A Min	AD645J/A Typ	AD645J/A Max	AD645K/B Min	AD645K/B Typ	AD645K/B Max	AD645S Min	AD645S Typ	AD645S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			100	500		50	250		100	500	μV
Offset	T_{min} to T_{max}		300	1000		100	400		500	1500	μV
vs. Temperature			3	12		2	5		4	10	μV/°C
vs. Supply (PSRR)		90	110		94	110		90	110		dB
vs. Supply	T_{min} to T_{max}		100		90	100		86	95		dB
INPUT BIAS CURRENT[2]											
Either Input	V_{CM} = 0 V		0.7/1.8	3/5		0.7/1.8	1.5/3		1.8	5	pA
Either Input @T_{max}	V_{CM} = 0 V		16/115			16/115			1800		pA
Either Input	V_{CM} = +10 V		0.8/1.9			0.8/1.9			1.9		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5		0.1	1.0	pA
Offset Current @T_{max}	V_{CM} = 0 V		2/6			2/6			100		pA
FREQUENCY RESPONSE											
Unity-Gain BW, Small Signal	G = −1		2			2			2		MHz
Full Power Response	V_O = 20 V p–p, R_{LOAD} = 2 kΩ	16	32		16	32		16	32		kHz
Slew Rate, Unity Gain	V_{OUT} = 20 V p–p, R_{LOAD} = 2 kΩ	1	2		1	2		1	2		V/μs
SETTLING TIME[3]											
To 0.1%			6			6			6		μs
To 0.01%			8			8			8		μs
Overload Recovery[4]	50% Overdrive		5			5			5		μs
Total Harmonic Distortion	f = 1 kHz, R_{LOAD} ≥ 2 kΩ, V_O = 3 V rms		0.0006			0.0006			0.0006		%
INPUT IMPEDANCE											
Differential	V_{DIFF} = ±1 V		10^{12}‖1			10^{12}‖1			10^{12}‖1		Ω‖pF
Common-Mode			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage		±10	+11, −10.4		±10	+11, −10.4		±10	+11, −10.4		V
Over Max Oper. Range		±10			±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		90	110		dB
	T_{min} to T_{max}		100		90	100		86	100		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		1.0	3.3		1.0	**2.5**		1.0	3.3	μV p–p
	f = 10 Hz		20	50		20	40		20	50	nV/√Hz
	f = 100 Hz		10	**30**		10	**20**		10	**30**	nV/√Hz
	f = 1 kHz		9	15		9	12		9	15	nV/√Hz
	f = 10 kHz		8	10		8	10		8	10	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 to 10 Hz		11	20		11	15		11	20	fA p–p
	f = 0.1 to 20 kHz		0.6	1.1		0.6	0.8		0.6	1.1	fA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V, R_{LOAD} ≥ 2 kΩ	114	130		120	130		114	130		dB
	T_{min} to T_{max}				114			110			dB
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 2 kΩ	±10	±11		±10	±11		±10	±11		V
	T_{min} to T_{max}	±10			±10			±10			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		±5	±10		mA
	Short Circuit		±15			±15			±15		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			3.0	3.5		3.0	3.5		3.0	3.5	mA
TRANSISTOR COUNT	# of Transistors		62			62			62		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Gain = −1, R_{LOAD} = 2 kΩ

[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.

[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test, all others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] (@ T_A = +25°C)
8-Pin Header Package . . . . . 500 mW
8-Pin Mini-DIP Package . . . . . 750 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (H) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Operating Temperature Range
AD645J/K . . . . . 0 to +70°C
AD645A/B . . . . . −40°C to +85°C
AD645S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . 300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics:
8-Pin Plastic Mini-DIP Package: θ_{JA} = 100°C/Watt
8-Pin Header Package: θ_{JA} = 200°C/Watt

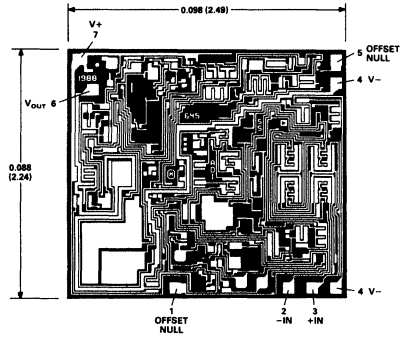
ORDERING GUIDE*

Temperature Range	Mini-DIP (N-8)	Header (H-08A)
Commercial 0 to +70°C	AD645JN AD645KN	
Industrial −40°C to +85°C		AD645AH AD645BH
Military −55°C to +125°C		AD645SH AD645SH/883B

"J" and "S" Grade Chips are also available.
*See Section 20 for package outline information.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



Typical Characteristics (@ +25°C, ±15 V unless otherwise stated)

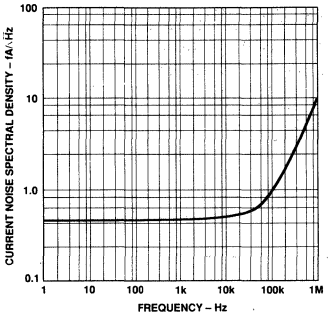


Figure 1. Current Noise Spectral Density

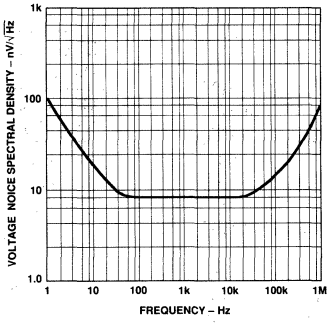


Figure 2. Voltage Noise Spectral Density

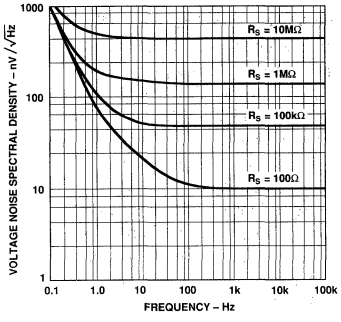


Figure 3. Voltage Noise Spectral Density vs. Frequency for Various Load Resistances

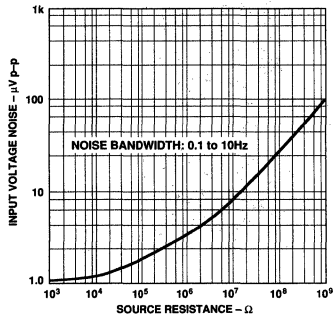


Figure 4. Input Voltage Noise vs. Source Resistance

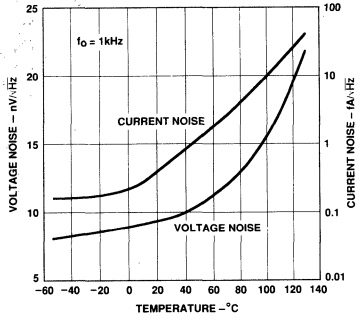


Figure 5. Voltage and Current Noise Spectral Density vs. Temperature

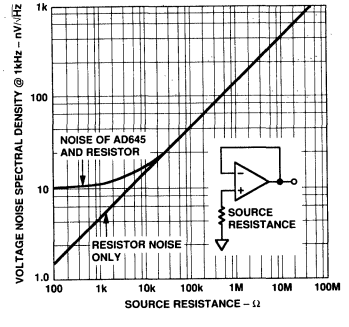


Figure 6. Voltage Noise Spectral Density @ 1 kHz vs. Source Resistance

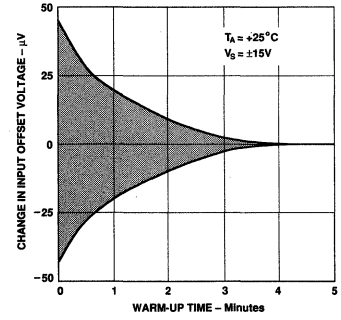


Figure 7. Change in Input Offset Voltage vs. Warmup Time

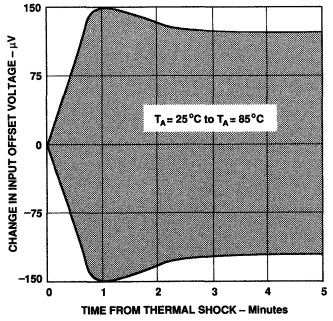


Figure 8. Change in Input Offset Voltage vs. Time from Thermal Shock

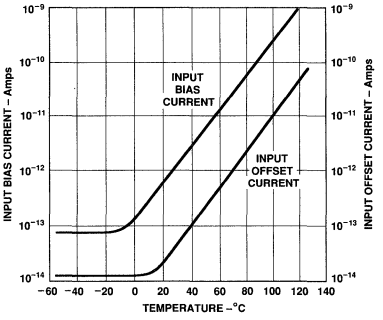


Figure 9. Input Bias and Offset Currents vs. Temperature

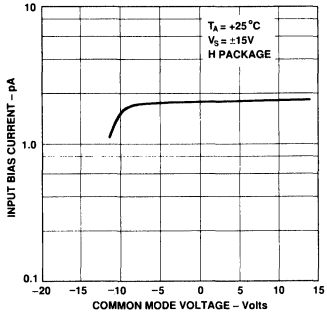


Figure 10. Input Bias Current vs. Common-Mode Voltage

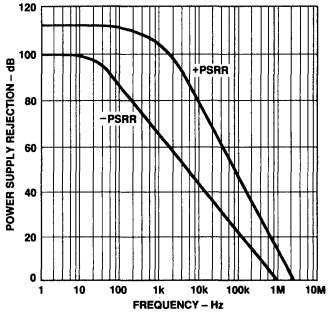


Figure 11. Power Supply Rejection vs. Frequency

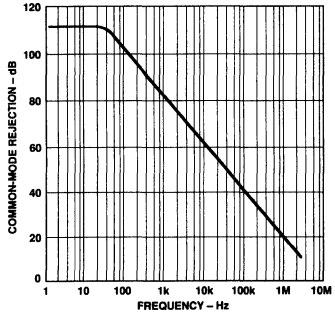


Figure 12. Common-Mode Rejection vs. Frequency

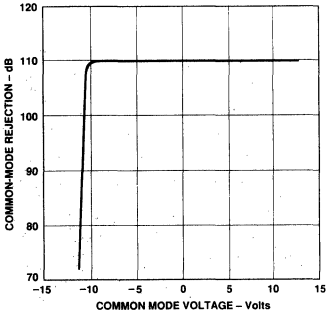


Figure 13. Common-Mode Rejection vs. Input Common-Mode Voltage

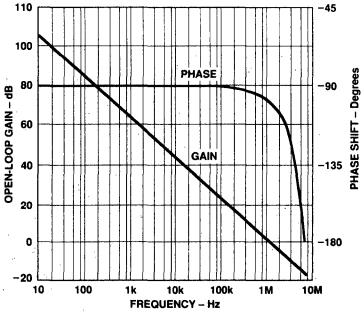


Figure 14. Open-Loop Gain and Phase Shift vs. Frequency

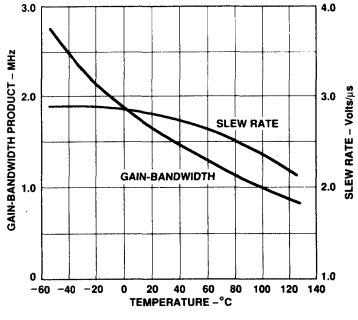


Figure 15. Gain-Bandwidth Product and Slew Rate vs. Temperature

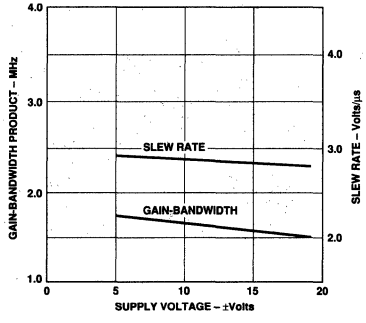


Figure 16. Gain-Bandwidth and Slew Rate vs. Supply Voltage

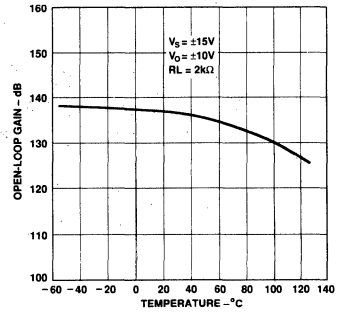


Figure 17. Open-Loop Gain vs. Temperature

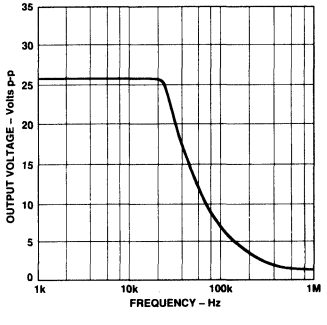


Figure 18. Large Signal Frequency Response

Typical Characteristics

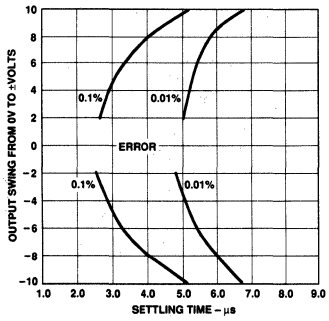


Figure 19. Output Swing and Error vs. Settling Time

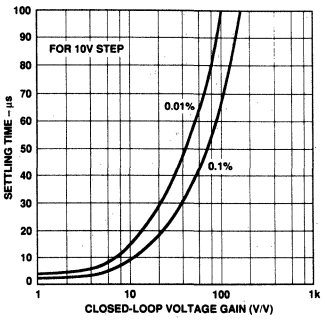


Figure 20. Settling Time vs. Closed-Loop Voltage Gain

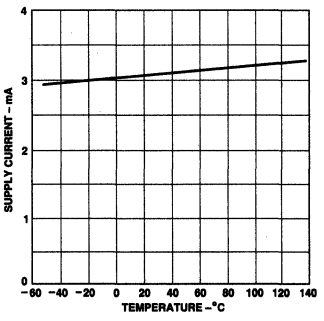


Figure 21. Supply Current vs. Temperature

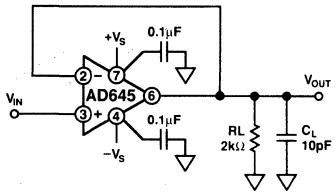


Figure 22a. Unity-Gain Follower

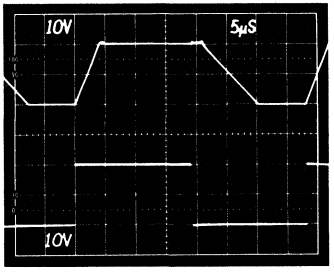


Figure 22b. Unity-Gain Follower Large Signal Pulse Response

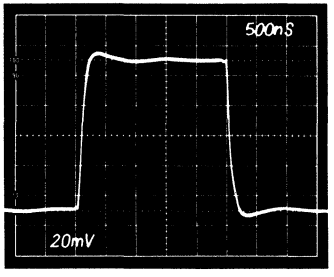


Figure 22c. Unity-Gain Follower Small Signal Pulse Response

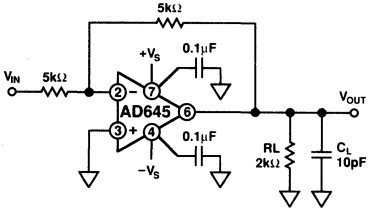


Figure 23a. Unity-Gain Inverter

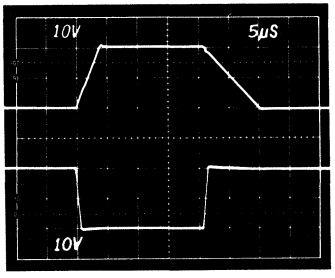


Figure 23b. Unity-Gain Inverter Large Signal Pulse Response

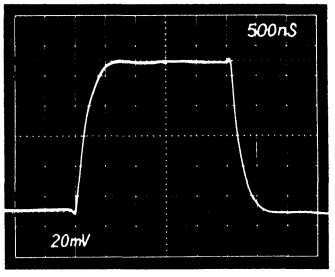


Figure 23c. Unity-Gain Inverter Small Signal Pulse Response

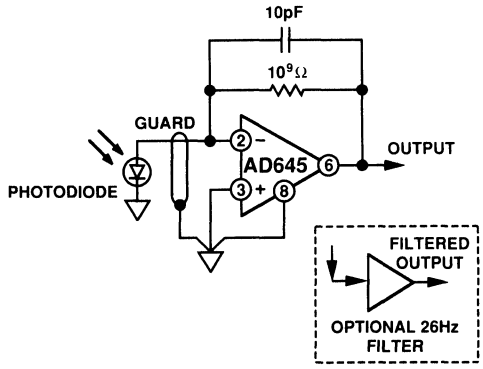


Figure 24. The AD645 Used as a Sensitive Preamplifier

Preamplifier Applications

The low input current and offset voltage levels of the AD645 together with its low voltage noise make this amplifier an excellent choice for preamplifiers used in sensitive photodiode applications. In a typical preamp circuit, shown in Figure 24, the output of the amplifier is equal to:

$$V_{OUT} = I_D\,(Rf) = Rp\,(P)\,Rf$$

where:

I_D = photodiode signal current (Amps)

Rp = photodiode sensitivity (Amp/Watt)

Rf = the value of the feedback resistor, in ohms.

P = light power incident to photodiode surface, in watts.

An equivalent model for a photodiode and its dc error sources is shown in Figure 25. The amplifier's input current, I_B, will contribute an output voltage error which will be proportional to the value of the feedback resistor. The offset voltage error, V_{OS}, will cause a "dark" current error due to the photodiode's finite shunt resistance, Rd. The resulting output voltage error, V_E, is equal to:

$$V_E = (1 + Rf/Rd)\,V_{OS} + Rf\,I_B$$

A shunt resistance on the order of 10^9 ohms is typical for a small photodiode. Resistance Rd is a junction resistance which will typically drop by a factor of two for every 10°C rise in temperature. In the AD645, both the offset voltage and drift are low, this helps minimize these errors.

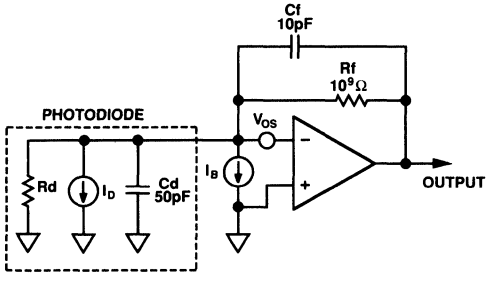


Figure 25. A Photodiode Model Showing DC Error Sources

Minimizing Noise Contributions

The noise level limits the resolution obtainable from any preamplifier. The total output voltage noise divided by the feedback resistance of the op amp defines the minimum detectable signal current. The minimum detectable current divided by the photodiode sensitivity is the minimum detectable light power.

Sources of noise in a typical preamp are shown in Figure 26. The total noise contribution is defined as:

$$\overline{V_{OUT}} = \sqrt{(\overline{i_n}^2 + \overline{i_f}^2 + \overline{i_s}^2)\left(\frac{Rf}{1 + s\,|Cf|\,Rf}\right)^2 + |\overline{en}^2|\left(1 + \frac{Rf}{Rd}\left(\frac{1 + s\,|Cd|\,Rd}{1 + s\,|Cf|\,Rf}\right)\right)^2}$$

Figure 27, a spectral density versus frequency plot of each source's noise contribution, shows that the bandwidth of the amplifier's input voltage noise contribution is much greater than its signal bandwidth. In addition, capacitance at the summing junction results in a "peaking" of noise gain in this configuration. This effect can be substantial when large photodiodes with large shunt capacitances are used. Capacitor Cf sets the signal bandwidth and also limits the peak in the noise gain. Each source's rms or root-sum-square contribution to noise is obtained by integrating the sum of the squares of all the noise sources and then by obtaining the square root of this sum. Minimizing the total area under these curves will optimize the preamplifier's overall noise performance.

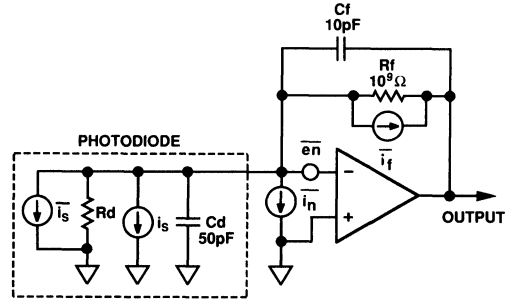


Figure 26. Noise Contributions of Various Sources

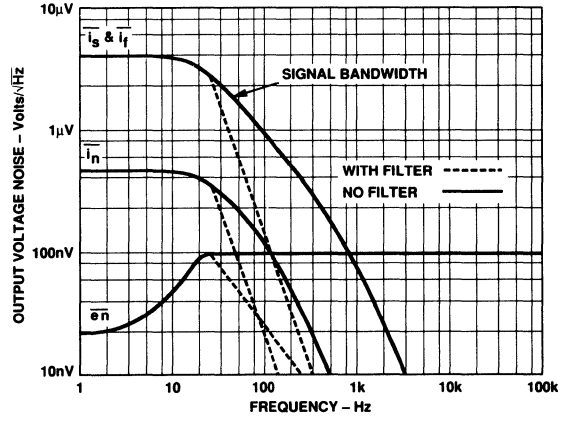


Figure 27. Voltage Noise Spectral Density of the Circuit of Figure 26 with and without an Output Filter

An output filter with a passband close to that of the signal can greatly improve the preamplifier's signal to noise ratio. The photodiode preamplifier shown in Figure 26—without a bandpass filter—has a total output noise of 50 μV rms. Using a 26 Hz single pole output filter, the total output noise drops to 23 μV rms, a factor of 2 improvement with no loss in signal bandwidth.

Using a "T" Network

A "T" network, shown in Figure 28, can be used to boost the effective transimpedance of an I to V converter, for a given feedback resistor value. Unfortunately, amplifier noise and offset voltage contributions are also amplified by the "T" network gain. A low noise, low offset voltage amplifier, such as the AD645, is needed for this type of application.

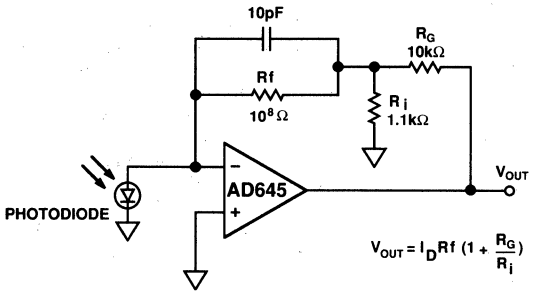


Figure 28. A Photodiode Preamp Employing a "T" Network for Added Gain

A pH Probe Buffer Amplifier

A typical pH probe requires a buffer amplifier to isolate its 10^6 to 10^9 Ω source resistance from external circuitry. Just such an amplifier is shown in Figure 29. The low input current of the AD645 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50 mV per pH unit at room temperature, has a +3300 ppm/°C temperature coefficient. The buffer of Figure 29 provides an output voltage equal to 1 volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor, part number Q81, 1 kΩ , 1%, +3500 ppm/°C, available from Tel Labs Inc.

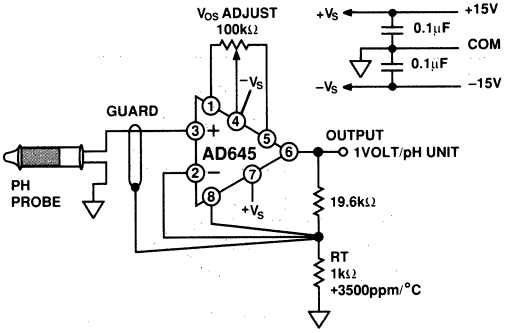


Figure 29. A pH Probe Amplifier

Circuit Board Notes

The AD645 is designed for through hole mount into PC boards. Maintaining picoampere level resolution in that environment requires a lot of care. Since both the printed circuit board and the amplifier's package have a finite resistance, the voltage difference between the amplifier's input pin and other pins (or traces on the PC board) will cause parasitic currents to flow into (or out of) the signal path. These currents can easily exceed the 1.5 pA input current level of the AD645 unless special precautions are taken. Two successful methods for minimizing leakage are: guarding the AD645's input lines and maintaining adequate insulation resistance.

Guarding the input lines by completely surrounding them with a metal conductor biased near the input lines' potential has two major benefits. First, parasitic leakage from the signal line is reduced, since the voltage between the input line and the guard is very low. Second, stray capacitance at the input terminal is minimized which in turn increases signal bandwidth. In the header or can package, the case of the AD645 is connected to Pin 8 so that it may be tied to the input potential (when operating as a follower) or tied to ground (when operating as an inverter). The AD645's positive input (Pin 3) is located next to the negative supply voltage pin (Pin 4). The negative input (Pin 2) is next to the balance adjust pin (Pin 1) which is biased at a potential close to that of the negative supply voltage. Note that any guard traces should be placed on *both* sides of the board. In addition, the input trace should be guarded along both of its edges, along its entire length.

Contaminants such as solder flux, on the board's surface and on the amplifier's package, can greatly reduce the insulation resistance and also increase the sensitivity to atmospheric humidity. Both the package and the board must be kept clean and dry. An effective cleaning procedure is to: first, swab the surface with high grade isopropyl alcohol, then rinse it with deionized water, and finally, bake it at 80°C for 1 hour. Note that if either polystyrene or polypropylene capacitors are used on the printed circuit board that a baking temperature of 70°C is safer, since both of these plastic compounds begin to melt at approximately +85°C.

ANALOG DEVICES

Ultralow Drift, Dual BiFET Op Amp

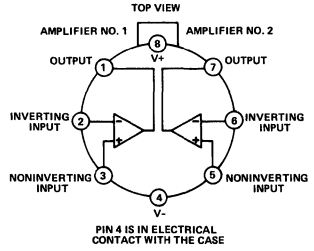
AD647

FEATURES

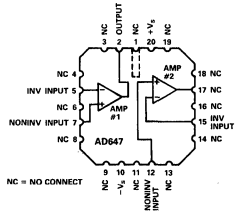
- **Low Offset Voltage Drift**
- **Matched Offset Voltage**
- **Matched Offset Voltage Over Temperature**
- **Matched Bias Current**
- **Crosstalk: −124dB at 1kHz**
- **Low Bias Current: 35pA max Warmed Up**
- **Low Offset Voltage: 250μV max**
- **Low Input Voltage: 2μV p–p**
- **High Open Loop Gain: 108dB**
- **Low Quiescent Current: 2.8mA max**
- **Low Total Harmonic Distortion**
- **Standard Dual Amplifier Pinout**
- **Available in Hermetic Metal Can Package, Hermetic Surface Mount (20-Pin LCC) and Chip Form**
- **MIL-STD-883B Processing Also Available**
- **Single Version Available: AD547**

AD647 PIN CONFIGURATIONS

TO-99 (H) Package



LCC (E) Package



PRODUCT DESCRIPTION

The AD647 is an ultralow drift, dual JFET amplifier that combines high performance and convenience in a single package.

The AD647 uses the most advanced ion-implantation and laser wafer drift trimming technologies to achieve the highest performance currently available in a dual JFET. Ion-implantation permits the fabrication of matched JFETs on a monolithic bipolar chip. Laser wafer drift trimming trims both the initial offset voltage and its drift with temperature to provide offsets as low as 100μV (250μV max) and drifts of 2.5μV/°C max.

In addition to outstanding individual amplifier performance, the AD647 offers guaranteed and tested matching performance on critical parameters such as offset voltage, offset voltage drift and bias currents.

The high level of performance makes the AD647 especially well suited for high precision instrumentation amplifier applications that previously would have required the costly selection and matching of space wasting single amplifiers.

The AD647 is offered in four performance grades, three commercial (the J, K and L) and one extended (the S). All are supplied in hermetically sealed 8-pin TO-99 packages and are available processed to MIL-STD-883B. The LCC version is also available processed to MIL-STD-883B.

PRODUCT HIGHLIGHTS

1. The AD647 is guaranteed and tested to tight matching specifications to ensure high performance and to eliminate the selection and matching of single devices.
2. Laser wafer drift trimming reduces offset voltage and offset voltage drifts to 250μV and 2.5μV/°C max.
3. Voltage noise is guraanteed at 4μV p–p max (0.1 to 10Hz) on K, L and S grades.
4. Bias current (35pA K, L, S; 75pA J) is specified after five minutes of operation.
5. Total supply current is a low 2.8mA max.
6. High open loop gain ensures high linearity in precision instrumentation amplifier applications.
7. The standard dual amplifier pinout permits the direct substitution of the AD647 for lower performance devices.
8. The AD647 is available in chip form.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD647J Min	AD647J Typ	AD647J Max	AD647K Min	AD647K Typ	AD647K Max	AD647L Min	AD647L Typ	AD647L Max	AD647S Min	AD647S Typ	AD647S Max	Units
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, R_L = 2kΩ	100,000			**250,000**			**250,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ R_L = 10kΩ, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		V/μs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage vs. Temp.			**10**			5			2.5			**5.0**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			200			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			**10**			5			2.5			**10.0**	μV/°C
Input Bias Current			**35**			25			25			25	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		10^{12}‖6			10^{12}‖6			10^{12}‖6			10^{12}‖6		MΩ‖pF
Common Mode		10^{12}‖6			10^{12}‖6			10^{12}‖6			10^{12}‖6		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common-Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2				**4**			**4**			**4**	μV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[5]													
TO-99 Style (H-08B)		AD647JH			AD647KH			AD647LH			AD647SH		
LCC (E-20A)											AD647SE		
											AD647SE/883B		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

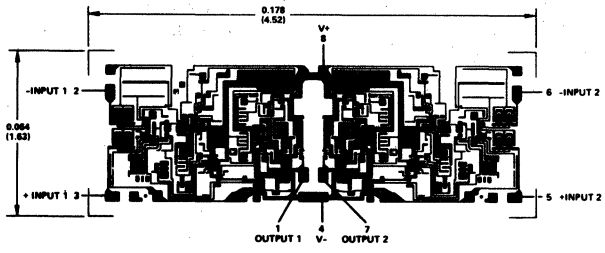
[5]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



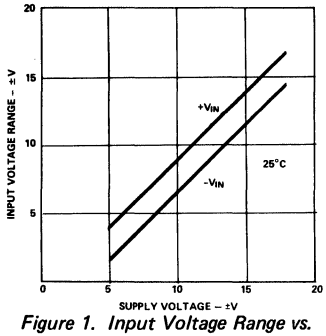


Figure 1. Input Voltage Range vs. Supply Voltage

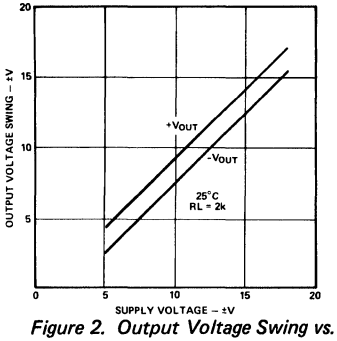


Figure 2. Output Voltage Swing vs. Supply Voltage

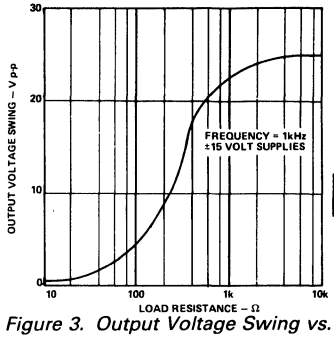


Figure 3. Output Voltage Swing vs. Load Resistance

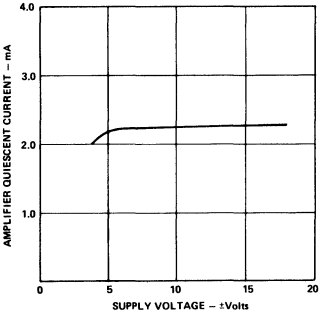


Figure 4. Quiescent Current vs. Supply Voltage

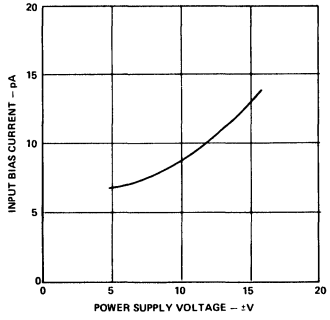


Figure 5. Input Bias Current vs. Power Supply Voltage

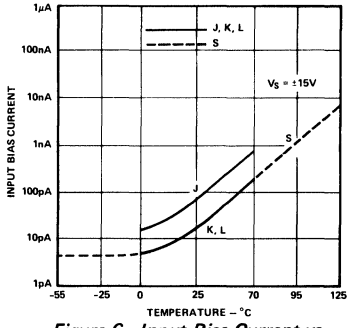


Figure 6. Input Bias Current vs. Temperature

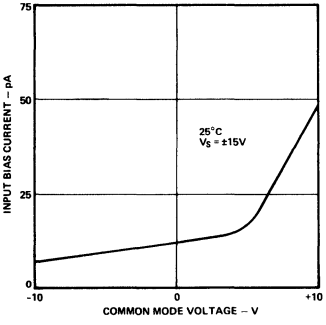


Figure 7. Input Bias Current vs. CMV

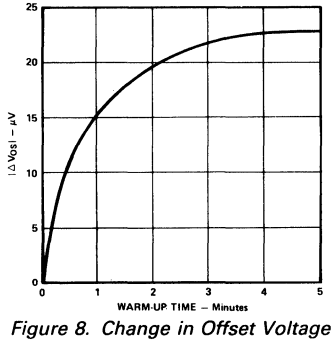


Figure 8. Change in Offset Voltage vs. Warm-Up Time

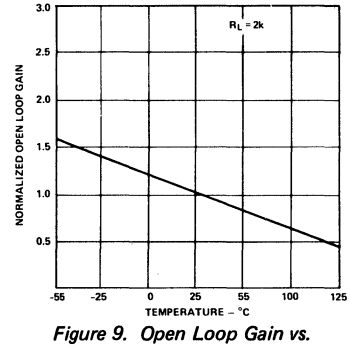


Figure 9. Open Loop Gain vs. Temperature

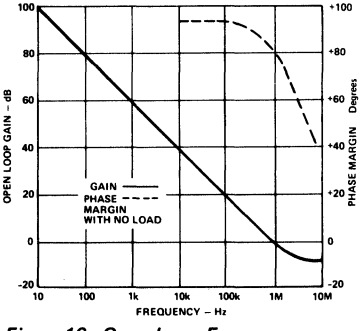


Figure 10. Open Loop Frequency Response

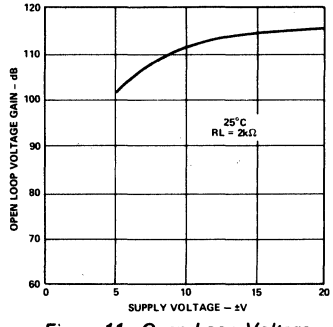


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

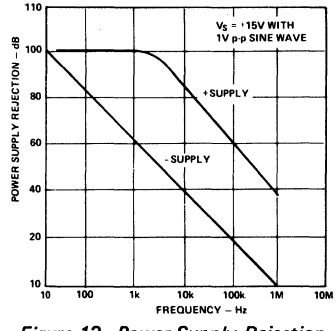


Figure 12. Power Supply Rejection vs. Frequency

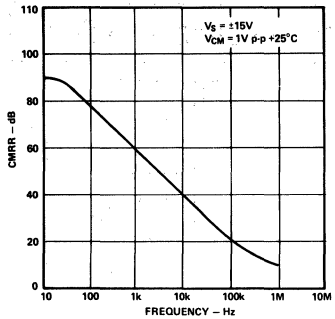


Figure 13. Common-Mode Rejection Ratio vs. Frequency

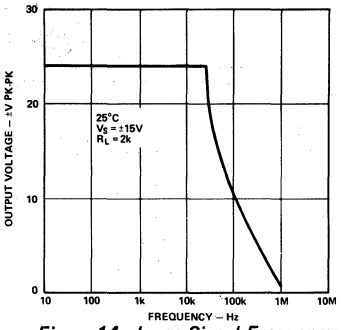


Figure 14. Large Signal Frequency Response

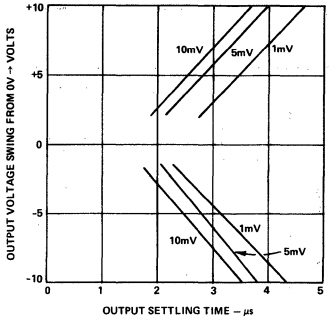


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

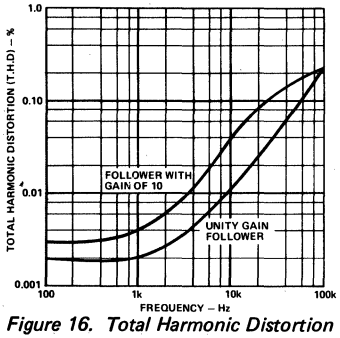


Figure 16. Total Harmonic Distortion vs. Frequency

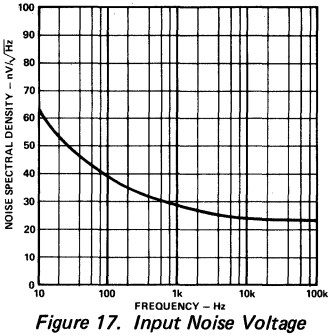


Figure 17. Input Noise Voltage Spectral Density

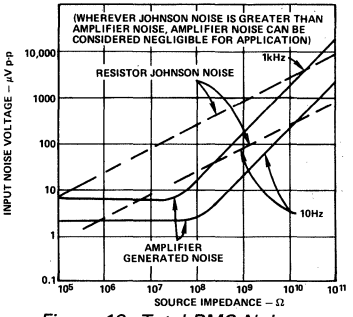
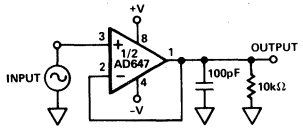
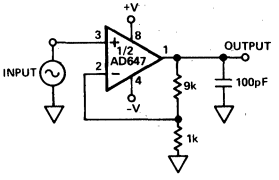


Figure 18. Total RMS Noise vs. Source Impedance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

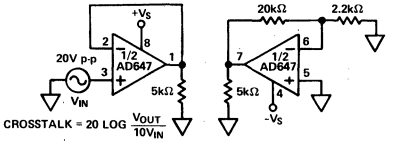


Figure 20. Crosstalk Test Circuit

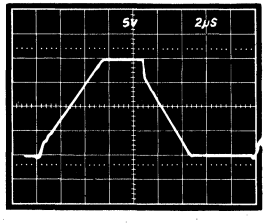


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

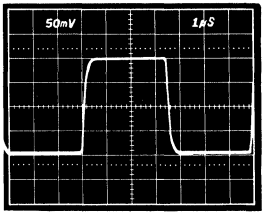


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

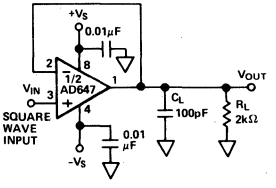


Figure 21c. Unity Gain Follower

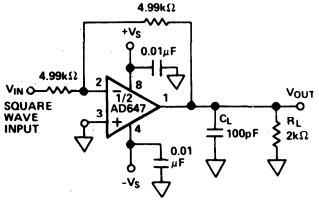


Figure 22a. Unity Gain Inverter

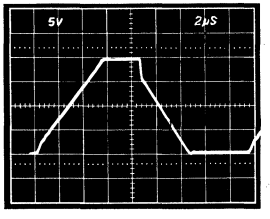


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

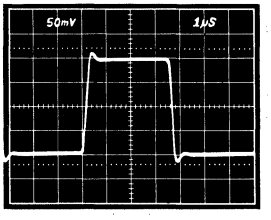


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

APPLICATION NOTES

The AD647 is fully specified under actual operating conditions to insure high performance in any application, but there are some steps that will improve on even this high level of performance.

The bias current of a JFET amplifier doubles with every 10°C increase in junction temperature. Any heat source that can be eliminated or minimized will significantly improve bias current performance. To account for normal power dissipation, the largest contributor to chip self-heating, the bias currents of the AD647 are guaranteed fully warmed up with ±15V supplies. A decrease in supply voltage will decrease power consumption, resulting in a corresponding drop in bias currents.

Open loop gain and bias currents, to some extent, are affected by output loading. In applications where high linearity is essential, load impedance should be kept as high as possible to minimize degradation of open loop gain.

The outstanding ac and dc performance of the AD647 make it an ideal choice for critical instrumentation applications. In such applications, leakage paths, line losses and external noise sources should be considered in the layout of printed circuit boards. A guard ring surrounding the inputs and connected to a low impedance potential (at the same level as the inputs) should be placed on both sides of the circuit board. This will eliminate leakage paths that could degrade bias current performance. All signal paths should be shielded to minimize noise pick-up.

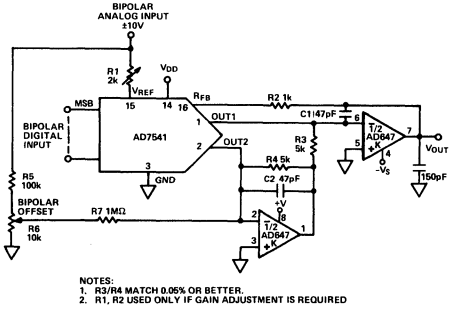


Figure 23. AD647 Used as DAC Output Amplifier

A CMOS DAC AMPLIFIER

The output impedance of a CMOS DAC, such as the AD7541, varies with digital input code. This causes a corresponding variation in the noise gain of the DAC-amplifier combination. This noise gain modulation introduces a nonlinearity whose magnitude is dependent on the amount of offset voltage present.

Laser wafer drift trimming lowers the initial offset voltage and the offset voltage drift of the AD647, therefore minimizing the effect of this nonlinearity and its drift with temperature. This, in conjunction with the low bias current and high open loop gain, makes the AD647 ideal for DAC output amplifier applications.

THE AD647 USED WITH THE AD7546

Figure 24 shows the AD647 used with the AD7546 16-bit segment DAC. In this application, amplifier performance is critical to the overall performance of the AD7546. A1 is used as a dual precision buffer. Here the offset voltage match, low offset voltage and high open loop gain of the AD647 ensure monotonicity and high linearity over the entire operating temperature range. A2 serves a dual function: amplifier A is a Track and Hold circuit that deglitches the DAC output and amplifier B acts as an output amplifier. The performance of the amplifiers of A2 is crucial to the accuracy of the system. The errors of these amplifiers are added to the errors due strictly to DAC imperfections. For this reason great care should be used in the selection of these amplifiers. The matching characteristics, low bias current and low temperature coefficients of the AD647 make it ideal for this application.

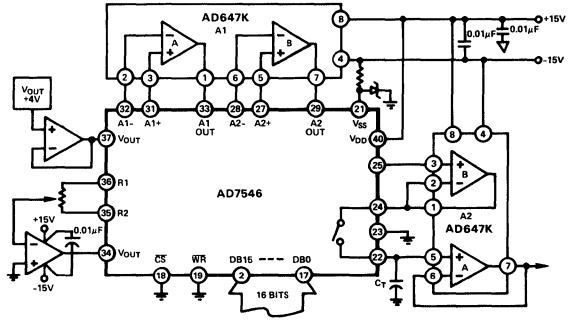


Figure 24. AD647 Used with AD7546 16-Bit DAC

USING THE AD647 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in a wide range of analog computational applications, ranging from the simple linearization of exponential transducer outputs to the use of logarithms in computations involving multi-term products or arbitrary exponents. Log amps also facilitate the compression of wide ranging analog input signals into a range that can be easily handled using standard circuit techniques.

The picoamp level input current and low offset voltage of the AD647 make it suitable for wide dynamic range log amplifiers. Figure 27 is a schematic of a log ratio circuit employing the AD647 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100μA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

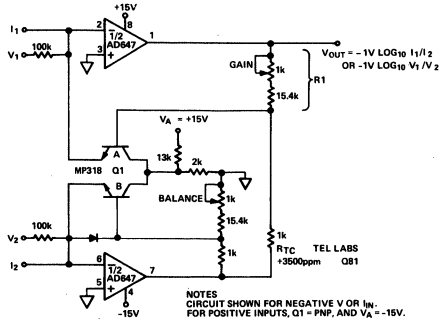


Figure 25. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base-emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce a 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, which may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

ACTIVE FILTERS

In active low pass filtering applications the dc accuracy of the amplifiers used is critical to the performance of the filter circuits. DC error sources such as offset voltage and bias currents represent the largest individual contributors to output error. Offset voltages will be passed by the filtering network and may, depending on the design of the filter circuit, be amplified and generate unacceptable output offset voltages. In filter circuits for low frequency ranges large value resistors are used to generate the low pass filter function. Input bias currents passing through these resistors will generate an additional offset voltage that will also be passed to the output of the filter.

The use of the AD647 will minimize these error sources and, therefore, maximize filter accuracy. The wide variety of performance levels of the AD647 allows for just the amount of accuracy required for any given application.

AD647 AS AN INSTRUMENTATION AMPLIFIER

The circuit shown in Figure 26 uses the AD647 to construct an ultra high precision instrumentation amplifier. In this type of application the matching characteristics of a monolithic dual amplifier are crucial to ensure high performance.

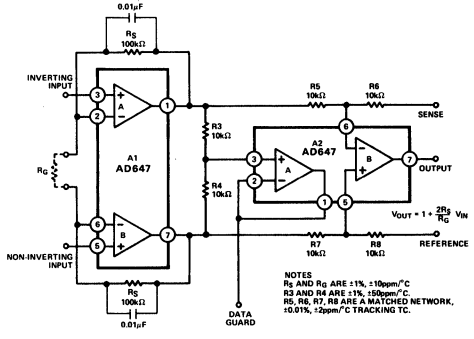


Figure 26. Precision FET Input Instrumentation Amplifier

The use of an AD647L as the input amplifier A1, guarantees maximum offset voltage of 250μV, drift of 2.5μV/°C and bias currents of 35pA. A2 serves two less critical functions in the amplifier and, therefore can be an AD647J. Amplifier A is an active data guard which increases ac CMRR and minimizes extraneous signal pickup and leakage. Amplifier B is the output amplifier of the instrumentation amplifier. To attain the precision available from this configuration, a great deal of care should be taken when selecting the external components. CMRR will depend on the matching of resistors R1, R2, R3, and R4. The gain drift performance of this circuit will be affected by the matching TC of the resistors used.

ANALOG DEVICES

Dual Precision, Low Power BiFET Op Amp

AD648

FEATURES

DC Performance
- **400 μA max Quiescent Current**
- **10 pA max Bias Current, Warmed Up (AD648C)**
- **300 μV max Offset Voltage (AD648C)**
- **3 μV/°C max Drift (AD648C)**
- **2 μV p–p Noise, 0.1 Hz to 10 Hz**

AC Performance
- **1.8 V/μs Slew Rate**
- **1 MHz Unity Gain Bandwidth**

Available in Plastic Mini-DIP, Cerdip, Plastic SOIC and Hermetic Metal Can Packages

MIL-STD-883B Parts Available

Surface Mount (SOIC) Package Available in Tape and Reel

Single Version: AD548

PRODUCT DESCRIPTION

The AD648 is a matched pair of low power, precision monolithic operational amplifiers. It offers both low bias current (10 pA max, warmed up) and low quiescent current (400 μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD648's entire common-mode voltage range.

The economical J grade has a maximum guaranteed offset voltage of less than 2 mV and an offset voltage drift of less than 20 μV/°C. The C grade reduces offset voltage to less than 0.30 mV and offset voltage drift to less than 3 μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

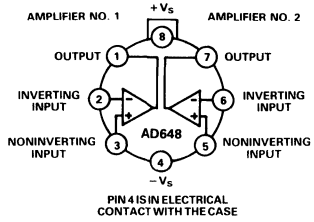
The AD648 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD648's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86 dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD648 is pinned out in a standard dual op amp configuration and is available in seven performance grades. The AD648J and AD648K are rated over the commercial temperature range of 0 to +70°C. The AD648A, AD648B and AD648C are rated over the industrial temperature range of −40°C to +85°C. The AD648S and AD648T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

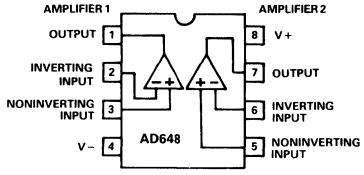
Extended reliability PLUS screening is available for parts specified over the commercial and industrial temperature ranges.

AD648 CONNECTION DIAGRAMS

TO-99
(H) Package



Plastic Mini-DIP (N) Package,
Plastic SOIC (R) Package
and
Cerdip (Q) Package



PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD648 is available in an 8-pin plastic mini-DIP, cerdip, SOIC, TO-99 metal can, or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD648 the ideal op amp for high performance, low power applications.
2. The AD648 is pin compatible with industry standard dual op amps such as the LF442, TL062, and AD642, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2 mV max) and drift (20 μV/°C max) for the AD648J are achieved utilizing Analog Devices' laser drift trimming technology.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. Matching characteristics are excellent for all grades. The input offset voltage matching between amplifiers in the AD648J is within 2 mV, for the C grade matching is within 0.4 mV.
6. Crosstalk between amplifiers is less than −120 dB at 1 kHz.
7. The AD648 is available in chip form.

SPECIFICATIONS (@ +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	AD648J/A/S			AD648K/B/T			AD648C			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	**2.0**		0.3	**1.0**		0.10	**0.3**	mV
T_{min} to T_{max}			3.0/3.0/**3.0**			1.5/1.5/2.0			0.5	mV
vs. Temp.			20			**10**			3.0	µV/°C
vs. Supply	**80**			**86**			86			dB
vs. Supply, T_{min} to T_{max}	76/76/**76**			**80**			**80**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input,[2] V_{CM} = 0		5	**20**		3	**10**		3	**10**	pA
Either Input[2] at T_{max}, V_{CM} = 0			0.45/1.3/20			0.25/0.65/10			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			**30**			15			15	pA
Offset Current, V_{CM} = 0		5	**10**		2	5		2	5	pA
Offset Current at T_{max}			0.25/0.7/10			0.15/0.35/5			0.35	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage		1.0	**2.0**		0.5	**1.0**		0.2	**0.4**	mV
Input Offset Voltage T_{min} to T_{max}			3.0/3.0/**3.0**			**1.5/1.5/2.0**			**0.5**	mV
Input Offset Voltage vs. Temp		8			5			2.5		µV/°C
Input Bias Current			**10**			5			5	pA
Crosstalk		−120			−120			−120		dB
INPUT IMPEDANCE										
Differential		$1\times10^{12}\|3$			$1\times10^{12}\|3$			$1\times10^{12}\|3$		Ω|pF
Common Mode		$3\times10^{12}\|3$			$3\times10^{12}\|3$			$3\times10^{12}\|3$		Ω|pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common Mode	**±11**	±12		**±11**	±12		**±11**	±12		V
Common-Mode Rejection										
V_{CM} = ±10 V	**76**			**82**			**86**			dB
T_{min} to T_{max}	76/76/**76**			**82**			**86**			dB
V_{CM} = ±11 V	**70**			**76**			**76**			dB
T_{min} to T_{max}	70/70/**70**			**76**			**76**			dB
INPUT VOLTAGE NOISE										
Voltage 0.1 Hz to 10 Hz		2			2			2	**4.0**	µV p-p
f = 10 Hz		80			80			80		nV/√Hz
f = 100 Hz		40			40			40		nV/√Hz
f = 1 kHz		30			30			30		nV/√Hz
f = 10 kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1 kHz		1.8			1.8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	**1.0**	1.8		**1.0**	1.8		**1.0**	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN-LOOP GAIN										
V_O = ±10 V, $R_L \geq$ 10 kΩ	**300**	1000		**300**	1000		**300**	1000		V/mV
T_{min} to T_{max}, $R_L \geq$ 10 kΩ	300/300/**300**	700		**300**	700		**300**	700		V/mV
V_O = ±10 V, $R_L \geq$ 5 kΩ	**150**	500		**150**	500		**150**	500		V/mV
T_{min} to T_{max}, $R_L \geq$ 5 kΩ	150/150/**150**	300		**150**	300		**150**	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq$ 10 kΩ, T_{min} to T_{max}	±12/±12/**±12**	±13		**±12**	±13		**±12**	±13		V
Voltage @ $R_L \geq$ 5 kΩ, T_{min} to T_{max}	±11/±11/**±11**	±12		**±11**	±12		**±11**	±12		V
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		**±18**	±4.5		**±18**	±4.5		**±18**	V
Quiescent Current (Both Amplifiers)		340	**400**		340	**400**		340	**400**	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD648J			AD648K					
Industrial (−40°C to +85°C)		AD648A			AD648B			AD648C		
Military (−55°C to +125°C)		AD648S			AD648T					
PACKAGE OPTIONS[5]										
SOIC (R-8)		AD648JR			AD648KR					
Plastic (N-8)		AD648JN			AD648KN					
Cerdip (Q-8)		AD648AQ, AD648SQ			AD648BQ, AD648TQ			AD648CQ		
Metal Can (H-08A)		AD648AH, AD648SH			AD648BH, AD648TH			AD648CH		
Tape and Reel		AD648JR-REEL			AD648KR-REEL					
J and S Grade Chips Available										

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Defined as voltages between inputs, such that neither exceeds ±10 V from ground.
[5]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

2

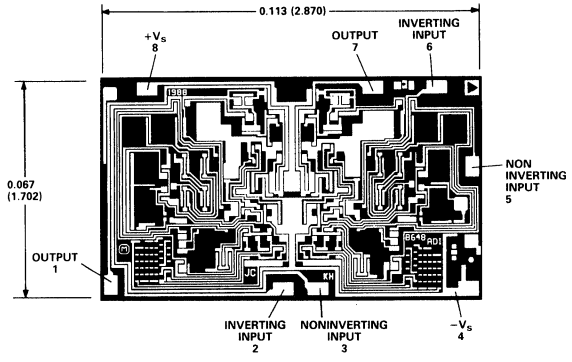
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltage[3] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range Q, H . . . . . −65°C to +150°C
N . . . . . −65°C to +125°C
Operating Temperature Range
AD648J/K . . . . . 0 to +70°C
AD648A/B/C . . . . . −40°C to +85°C
AD648S/T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics
8-Pin Plastic DIP Package: θ_{JA} = 165°C/Watt
8-Pin Cerdip Package: θ_{JC} = 22°C/Watt, θ_{JA} = 110°C/Watt
8-Pin Metal Can Package: θ_{JC} = 65°C/Watt, θ_{JA} = 150°C/Watt
[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics

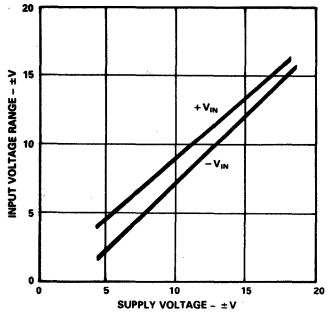


Figure 1. Input Voltage Range vs. Supply Voltage

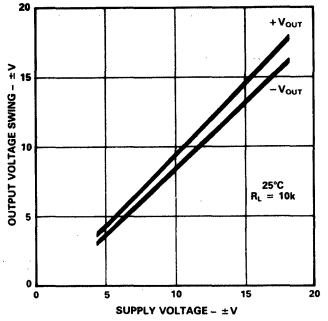


Figure 2. Output Voltage Swing vs. Supply Voltage

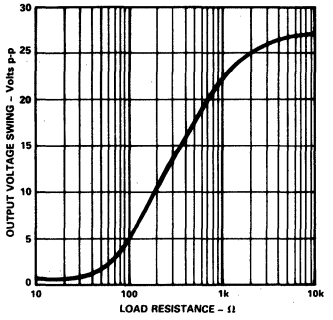


Figure 3. Output Voltage Swing vs. Load Resistance

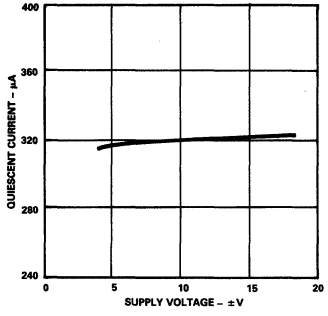


Figure 4. Quiescent Current vs. Supply Voltage

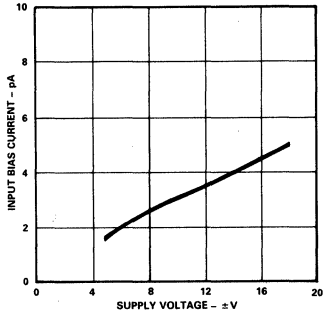


Figure 5. Input Bias Current vs. Supply Voltage

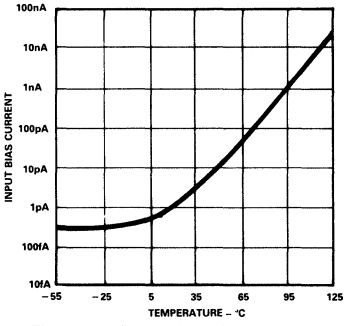


Figure 6. Input Bias Current vs. Temperature

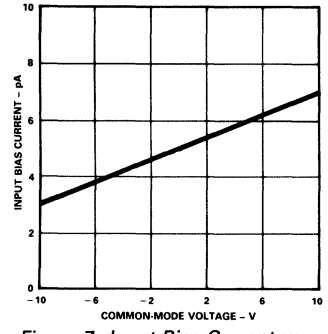


Figure 7. Input Bias Current vs. Common-Mode Voltage

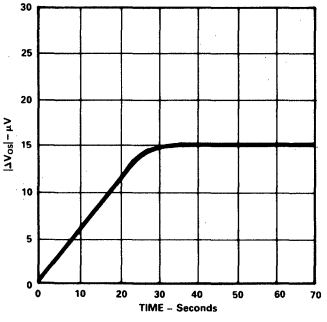


Figure 8. Change in Offset Voltage vs. Warm-Up Time

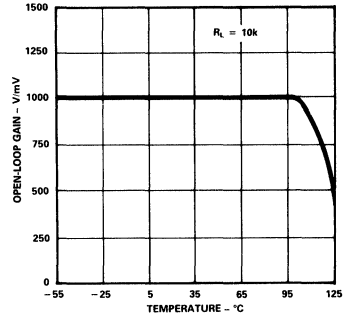


Figure 9. Open-Loop Gain vs. Temperature

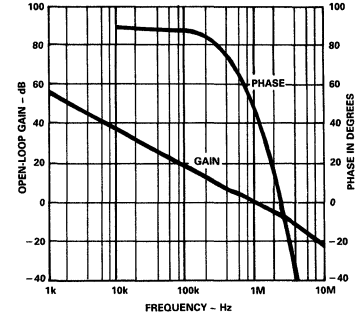


Figure 10. Open-Loop Frequency Response

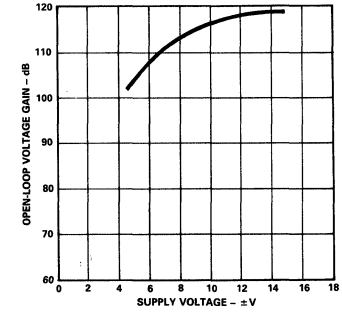


Figure 11. Open-Loop Voltage Gain vs. Supply Voltage

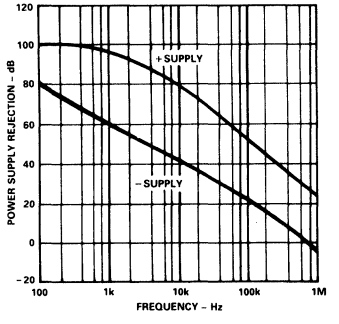


Figure 12. PSRR vs. Frequency

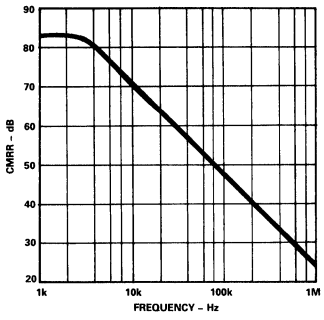


Figure 13. CMRR vs. Frequency

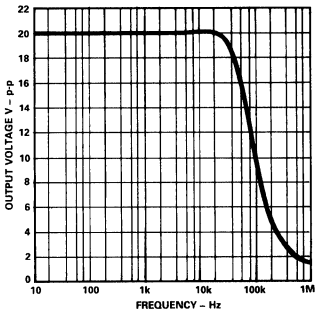


Figure 14. Large Signal Frequency Response

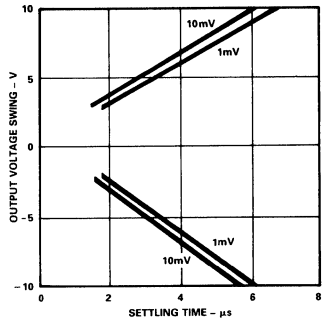


Figure 15. Output Swing and Error Voltage vs. Output Settling Time

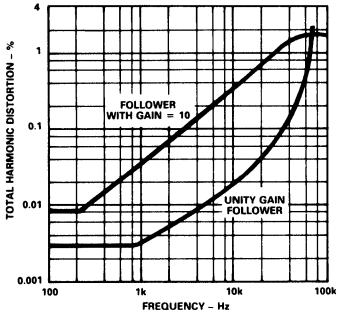


Figure 16. Total Harmonic Distortion vs. Frequency

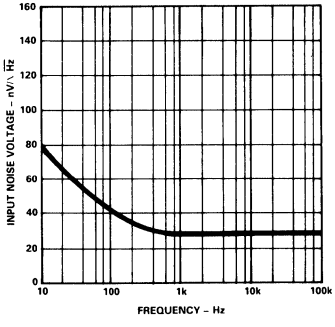


Figure 17. Input Noise Voltage Spectral Density

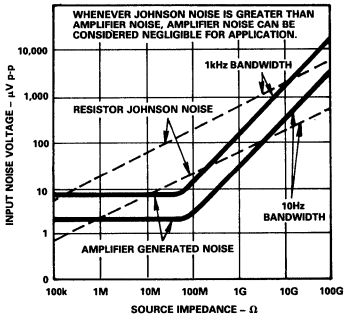


Figure 18. Total Noise vs. Source Impedance

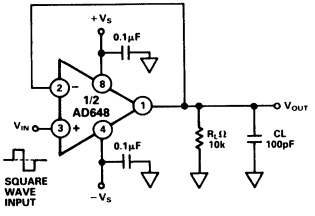


Figure 19a. Unity Gain Follower

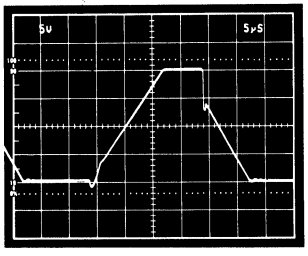


Figure 19b. Unity Gain Follower Pulse Response (Large Signal)

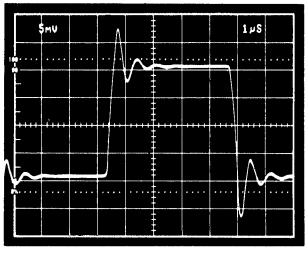


Figure 19c. Unity Gain Follower Pulse Response (Small Signal)

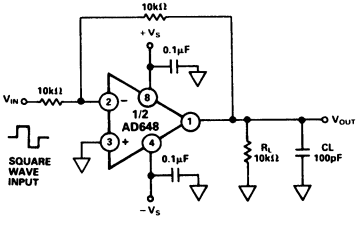


Figure 20a. Unity Gain Inverter

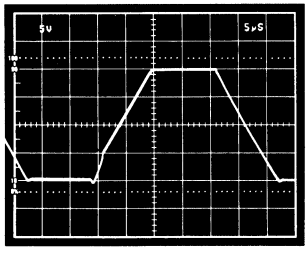


Figure 20b. Unity Gain Inverter Pulse Response (Large Signal)

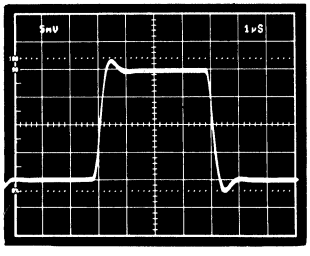


Figure 20c. Unity Gain Inverter Pulse Response (Small Signal)

Applying the AD648

APPLICATION NOTES

The AD648 is a pair of JFET-input op amps with a guaranteed maximum I_B of less than 10 pA, and offset and drift laser-trimmed to 0.3 mV and 3 μV/°C, respectively (AD648C). AC specs include 1 MHz bandwidth, 1.8 V/μs typical slew rate and 8 μs settling time for a 20 V step to ±0.01%—all at a supply current less than 400 μA. To capitalize on the device's performance, a number of error sources should be considered.

The minimal power drain and low offset drift of the AD648 reduce self-heating or "warm-up" effects on input offset voltage, making the AD648 ideal for on/off battery powered applications. The power dissipation due to the AD648's 400 μA supply current has a negligible effect on input current, but heavy output loading will raise the chip temperature. Since a JFET's input current doubles for every 10°C rise in chip temperature, this can be a noticeable effect.

The amplifier is designed to be functional with power supply voltages as low as ±4.5 V. It will exhibit a higher input offset voltage than at the rated supply voltage of ±15 V, due to power supply rejection effects. Common-mode range extends from 3 V more positive than the negative supply to 1 V more negative than the positive supply. Designed to cleanly drive up to 10 kΩ and 100 pF loads, the AD648 will drive a 2 kΩ load with reduced open-loop gain.

Figure 21 shows the recommended crosstalk test circuit. A typical value for crosstalk is −120 dB at 1 kHz.

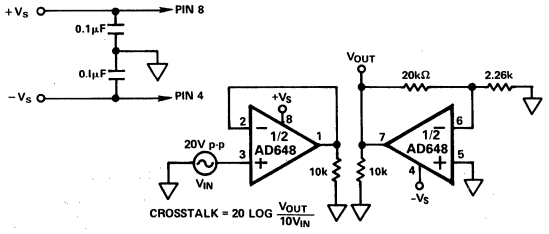


Figure 21. Crosstalk Test Circuit

LAYOUT

To take full advantage of the AD648's 10 pA max input current, parasitic leakages must be kept below an acceptable level. The practical limit of the resistance of epoxy or phenolic circuit board material is between 1×10^{12} Ω and 3×10^{12} Ω. This can result in an additional leakage of 5 pA between an input of 0 V and a −15 V supply line. Teflon or a similar low leakage material (with a resistance exceeding 10^{17} Ω) should be used to isolate high impedance input lines from adjacent lines carrying high voltages. The insulator should be kept clean, since contaminants will degrade the surface resistance.

A metal guard completely surrounding the high impedance nodes and driven by a voltage near the common-mode input potential can also be used to reduce some parasitic leakages. The guarding pattern in Figure 22 will reduce parasitic leakage due to finite board surface resistance; but it will not compensate for a low volume resistivity board.

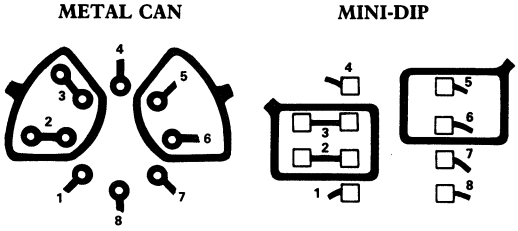


Figure 22. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD648 is guaranteed to withstand input voltages equal to the power supply potential. Exceeding the negative supply voltage on either input will forward bias the substrate junction of the chip. The induced current may destroy the amplifier due to excess heat.

Input protection is required in applications such as a flame detector in a gas chromatograph, where a very high potential may be applied to the input terminals during a sensor fault condition. Figures 23a and 23b show simple current limiting schemes that can be used. $R_{PROTECT}$ should be chosen such that the maximum overload current is 1.0 mA (for example 100 kΩ for a 100 V overload).

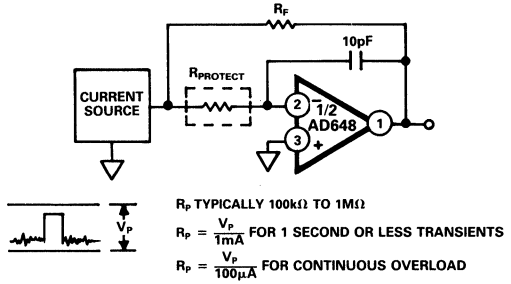


Figure 23a. Input Protection of I-to-V Converter

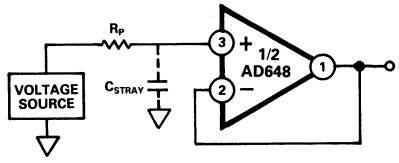


Figure 23b. Voltage Follower Input Protection Method

Figure 23b shows the recommended method for protecting a voltage follower from excessive currents due to high voltage breakdown. The protection resistor, R_p, limits the input current. A nominal value of 100 kΩ will limit the input current to less than 1 mA with a 100 volt input voltage applied.

The stray capacitance between the summing junction and ground will produce a high frequency roll-off with a corner frequency equal to:

$$f_{corner} = \frac{1}{2\pi R_p C_{stray}}$$

Accordingly, a 100 kΩ value for R_p with a 3 pF C_{stray} will cause a 3dB corner frequency to occur at 531 kHz.

Figure 23c shows a diode clamp protection scheme for an I-to-V converter using low leakage diodes. Because the diodes are connected to the op amp's summing junction, which is a virtual ground, their leakage contribution is minimal.

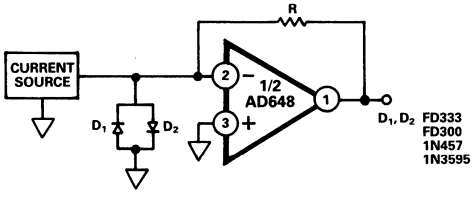


Figure 23c. I-to-V Converter with Diode Input Protection

Exceeding the negative common-mode range on either input terminal causes a phase reversal at the output, forcing the amplifier output to the corresponding high or low state. Exceeding the negative common-mode on both inputs simultaneously forces the output high. Exceeding the positive common-mode range on a single input doesn't cause a phase reversal; but if both inputs exceed the limit, the output will be forced high. In all cases, normal amplifier operation is resumed when input voltages are brought back within the common-mode range.

2

D/A CONVERTER BIPOLAR OUTPUT BUFFER

The circuit in Figure 24 provides 4 quadrant multiplication with a resolution of 12 bits. The AD648 is used to convert the AD7545 CMOS DAC's output current to a voltage and provides the necessary level shifting to achieve a bipolar voltage output. The circuit operates with a 12-bit plus sign input code. The transfer function is shown in Figure 25.

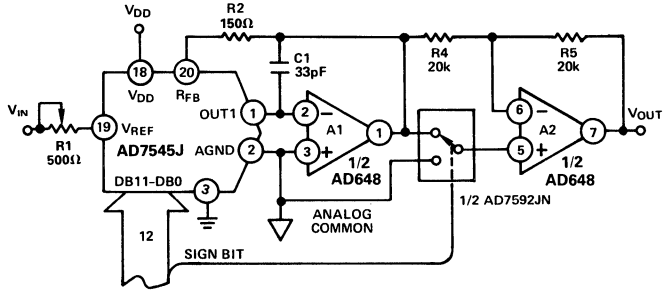


Figure 24. 12-Bit Plus Sign Magnitude D/A Converter

SIGN BIT	BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT
0	1111 1111 1111	$+V_{IN} \times (4095/4096)$
0	0000 0000 0000	0 VOLTS
1	0000 0000 0000	0 VOLTS
1	1111 1111 1111	$-V_{IN} \times (4095/4096)$

NOTE: SIGN BIT AT "0" CONNECTS THE NONINVERTING INPUT OF A2 TO ANALOG COMMON

Figure 25. Sign Magnitude Code Table

The AD7592 is a fully protected dual CMOS SPDT switch with data latches. R4 and R5 should match to within 0.01% to maintain the accuracy of the converter. A mismatch between R4 and R5 introduces a gain error. Overall gain is trimmed by adjusting R_{IN}. The AD648's low input offset voltage, low drift over temperature, and excellent dynamics make it an attractive low power output buffer.

The input offset voltage of the AD648 output amplifier results in an output error voltage. This error voltage equals the input offset voltage of the op amp times the noise gain of the amplifier.

That is:

$$V_{OS}\ Output = V_{OS}\ Input \left(1 + \frac{R_{FB}}{R_O}\right)$$

R_{FB} is the feedback resistor for the op amp, which is internal to the DAC. R_O is the DAC's R-2R ladder output resistance. The value of R_O is code dependent. This has the effect of changing the offset error voltage at the amplifier's output. An output amplifier with a sub millivolt input offset voltage is needed to preserve the linearity of the DAC's transfer function.

The AD648 in this configuration provides a 700 kHz small signal bandwidth and 1.8 V/μs typical slew rate. The 33 pF capacitor across the feedback resistor optimizes the circuit's response. The oscilloscope photos in Figures 26a and 26b show small and large signal outputs of the circuit in Figure 24. Upper traces show the input signal V_{IN}. Lower traces are the resulting output voltage with the DAC's digital input set to all 1s. The circuit settles to ±0.01% for a 20 V input step in 14 μs.

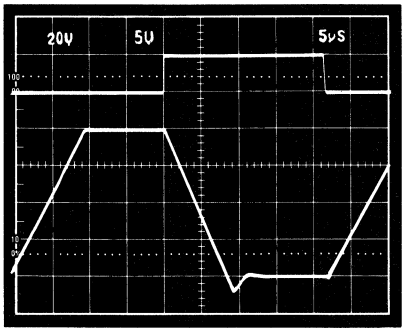


Figure 26a. Response to ±20 V p–p Reference Square Wave

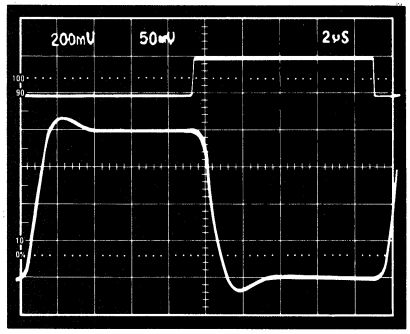


Figure 26b. Response to ±100 mV p–p Reference Square Wave

DUAL PHOTODIODE PREAMP

The performance of the dual photodiode preamp shown in Figure 27 is enhanced by the AD648's low input current, input voltage offset, and offset voltage drift. Each photodiode sources a current proportional to the incident light power on its surface. R_F converts the photodiode current to an output voltage equal to $R_F \times I_S$.

An error budget illustrating the importance of low amplifier input current, voltage offset, and offset voltage drift to minimize output voltage errors can be developed by considering the equivalent circuit for the small (0.2 mm^2 area) photodiode shown in Figure 27. The input current results in an error proportional to the feedback resistance used. The amplifier's offset will produce an error proportional to the preamp's noise gain $(1+R_F/R_{SH})$, where R_{SH} is the photodiode shunt resistance. The amplifier's input current will double with every 10°C rise in temperature, and the photodiode's shunt resistance halves with every 10°C rise. The error budget in Figure 28 assumes a room temperature photodiode R_{SH} of 500 MΩ, and the maximum input current and input offset voltage specs of an AD648C.

The capacitance at the amplifier's negative input (the sum of the photodiode's shunt capacitance, the op amp's differential input capacitance, stray capacitance due to wiring, etc.) will cause a rise in the preamp's noise gain over frequency. This can result in excess noise over the bandwidth of interest. C_F reduces the noise gain "peaking" at the expense of signal bandwidth.

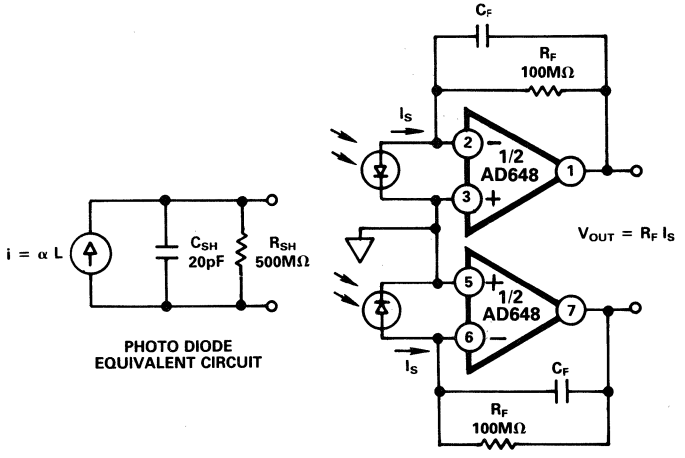


Figure 27. A Dual Photodiode Pre-Amp

TEMP °C	R_{SH} (MΩ)	V_{OS} (μV)	(1 + R_F/R_{SH}) V_{OS}	I_B (pA)	I_BR_F	TOTAL
−25	15,970	150	151 μV	0.30	30 μV	181 μV
0	2,830	225	233 μV	2.26	262 μV	495 μV
+25	500	300	360 μV	10.00	1.0 mV	1.36 mV
+50	88.5	375	800 μV	56.6	5.6 mV	6.40 mV
+75	15.6	450	3.33 mV	320	32 mV	35.3 mV
+85	7.8	480	6.63 mV	640	64 mV	70.6 mV

Figure 28. Photodiode Pre-Amp Errors over Temperature

INSTRUMENTATION AMPLIFIER

The AD648J's maximum input current of 20 pA per amplifier makes it an excellent building block for the high input impedance instrumentation amplifier shown in Figure 29. Total current drain for this circuit is under 600 μA. This configuration is optimal for conditioning differential voltages from high impedance sources.

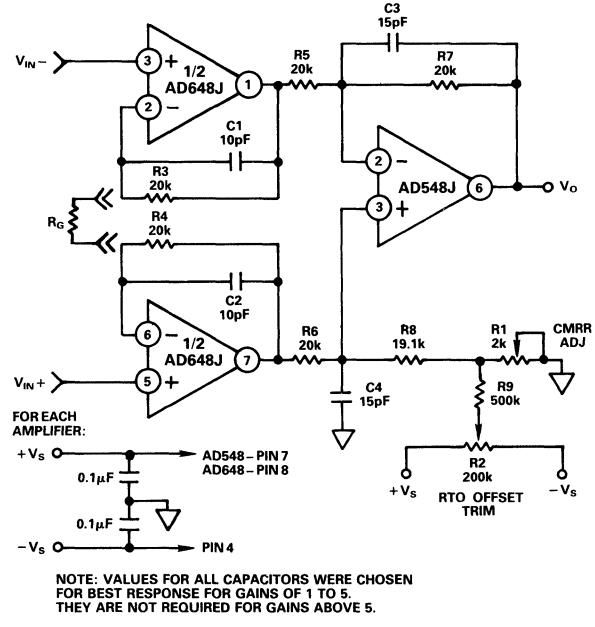
The overall gain of the circuit is controlled by R_G, resulting in the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{(R_3 + R_4)}{R_G}$$

Gains of 1 to 100 can be accommodated with gain nonlinearities of less than 0.01%. The maximum input current is 30 pA over the common-mode range, with a common-mode impedance of over $1 \times 10^{12}\Omega$. The capacitors C1, C2, C3 and C4 compensate for peaking in the gain over frequency which is caused by input capacitance.

To calibrate this circuit, first adjust trimmer R1 for common-mode rejection with +10 volts dc applied to the input pins. Next, adjust R2 for zero offset at V_{OUT} with both inputs grounded. Trim the circuit a second time for optimal performance.

The −3dB small signal bandwidth for this low power instrumentation amplifier is 700 kHz for a gain of 1 and 10 kHz for a gain of 100. The typical output slew rate is 1.8 V/μs.



NOTE: VALUES FOR ALL CAPACITORS WERE CHOSEN FOR BEST RESPONSE FOR GAINS OF 1 TO 5. THEY ARE NOT REQUIRED FOR GAINS ABOVE 5.

Figure 29. Low Power Instrumentation Amplifier

LOG RATIO AMPLIFIER

Log ratio amplifiers are useful for a variety of signal conditioning applications, such as linearizing exponential transducer outputs and compressing analog signals having a wide dynamic range. The AD648's picoamp level input current and low input offset voltage make it a good choice for the front-end amplifier of the log ratio circuit shown in Figure 30. This circuit produces an output voltage equal to the log base 10 of the ratio of the input currents I_1 and I_2. Resistive inputs R1 and R2 are provided for voltage inputs.

Input currents I_1 and I_2 set the collector currents of Q1 and Q2, a matched pair of logging transistors. Voltages at points A and B are developed according to the following familiar diode equation:

$$V_{BE} = (kT/q)\ ln\ (I_C/I_{ES})$$

In this equation, k is Boltzmann's constant, T is absolute temperature, q is an electron charge, and I_{ES} is the reverse saturation current of the logging transistors. The difference of these two voltages is taken by the subtractor section and scaled by a factor of approximately 16 by resistors R9, R10 and R8. Temperature compensation is provided by resistors R8 and R15, which have a positive 3500 ppm/°C temperature coefficient. The transfer function for the output voltage is:

$$V_{OUT} = 1V log_{10}\ (I_2/I_1)$$

Frequency compensation is provided by R11, R12, C1, and C2. Small signal bandwidth is approximately 300 kHz at input currents above 100 μA and will proportionally decrease with lower signal levels. D1, D2, R13, and R14 compensate for the effects of the two logging transistors' ohmic emitter resistance.

To trim this circuit, set the two input currents to 10 μA and adjust V_{OUT} to zero by adjusting the potentiometer on A3. Then set I_2 to 1 μA and adjust the scale factor such that the output voltage is 1V by trimming potentiometer R10. Offset adjustment for A1 and A2 is provided to increase the accuracy of the voltage inputs.

This circuit ensures a 1% log conformance error over an input current range of 300 pA to 1 mA, with low level accuracy limited by the AD648's input current. The low level input voltage accuracy of this circuit is limited by the input offset voltage and drift of the AD648.

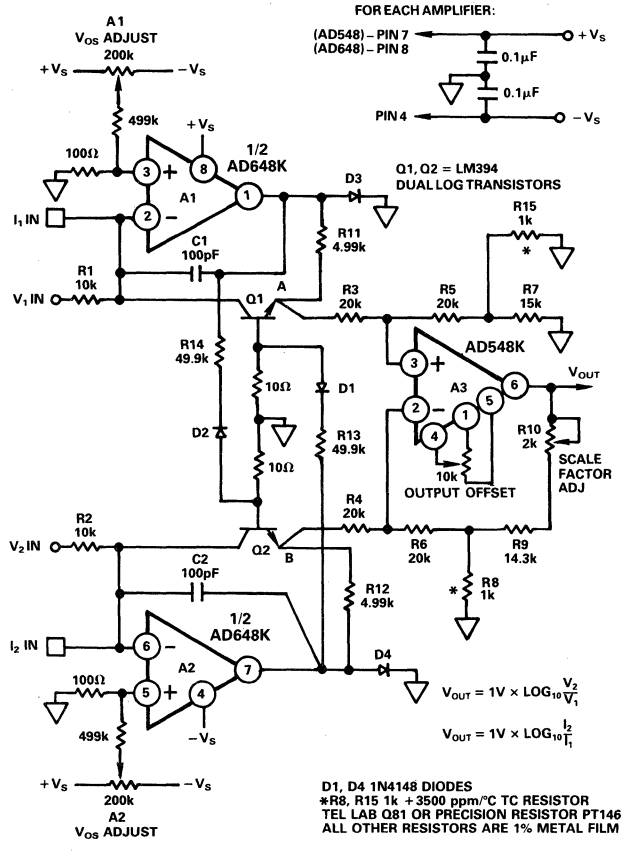


Figure 30. Precision Log Ratio Amplifier

ANALOG DEVICES

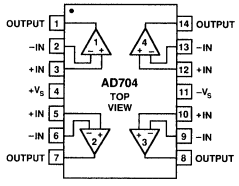
Quad Picoampere Input Current Bipolar Op Amp

AD704

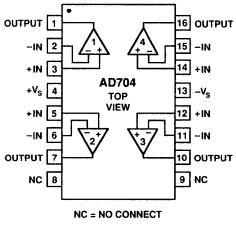
FEATURES
Enhanced Replacement for OP400 and LM324
HIGH DC PRECISION
40 μV max Offset Voltage
1 μV/°C max Offset Drift
100 pA max Input Bias Current
2.5 pA/°C max I_B Drift
LOW NOISE
0.5 μV p–p typ Noise, 0.1 Hz to 10 Hz
LOW POWER
600 μA max Supply Current per Amplifier
MIL-STD-883B Processing Available
Single Version: AD705
Dual Version: AD706
PRIMARY APPLICATIONS
Low Frequency Active Filters
Precision Instrumentation
Precision Integrators

AD704 CONNECTION DIAGRAMS

14-Pin Plastic (N) and 14-Pin Cerdip (Q) Packages



16-Pin SOIC (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD704 is a quad, low power bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower I_B drift over temperature. It utilizes Superbeta bipolar input transistors to achieve picoampere input bias current levels like FET input amplifiers at room temperature. However, its I_B only increases by 5× at 125°C unlike a BiFET amp, for which I_B doubles every 10°C resulting in a 1000× increase at +125°C. The AD704 achieves the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

Since it has only 1/20 the input bias current of an OP-07, the AD704 does not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the OP-07 which makes this amplifier usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the OP-07, the AD704 is better suited for today's higher density circuit boards.

The AD704 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation, and as a high quality integrator.

The AD704 is internally compensated for unity gain and is available in five performance grades. The AD704J and AD704K are rated over the commercial temperature range of 0 to +70°C. The AD704A and AD704B are rated over the industrial temperature of −40°C to +85°C. The AD704T is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD704 is offered in three package types: 14-pin plastic DIP, 14-pin cerdip and 16-pin wide-body SOIC packages. Chips are also available.

PRODUCT HIGHLIGHTS

1. The AD704 is a quad, low drift op amp that offers BiFET level input bias currents (at room temperature) yet has the low I_B drift of a bipolar amplifier. It may be used to upgrade circuits using quad op amps such as the OP400, LM324.
2. The AD704 can be used in applications where a chopper amplifier would normally be required but without the chopper's inherent noise and other problems.

SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, and ±15 V dc, unless otherwise noted)

Model	Conditions	AD704J/A Min	AD704J/A Typ	AD704J/A Max	AD704K/B Min	AD704K/B Typ	AD704K/B Max	AD704T Min	AD704T Typ	AD704T Max	Units
INPUT OFFSET VOLTAGE											
Initial Offset			30	100		10	40		10	50	μV
Offset	T_{min} – T_{max}		40	150		25	70		25	150	μV
vs. Temp. Average TC			0.2	1.5		0.2	1.0			1.0	μV/°C
vs. Supply (PSRR)	V_S = ±2 to ±18 V	110	132		110	132		114	132		dB
T_{min} – T_{max}	V_S = ±2.5 to ±18 V	108	126		108	126		108	126		dB
Long Term Stability			0.3			0.3			0.3		μV/month
INPUT BIAS CURRENT[1]	V_{CM} = 0 V		30	200		30	100		30	100	pA
	V_{CM} = ±13.5 V			250			150			150	pA
vs. Temp, Average TC			0.3			0.2			0.2		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V			300			200			600	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V			400			300			700	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		30	150		30	100		30	100	pA
	V_{CM} = ±13.5 V			200			150			150	pA
vs. Temp, Average TC			0.6			0.4			0.4		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V		80	250		80	200		80	300	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V		80	350		80	300		80	400	pA
MATCHING CHARACTERISTICS											
Offset Voltage				200			80			100	μV
	T_{min} – T_{max}			300			140			300	μV
Input Bias Current				400			200			200	pA
	T_{min} – T_{max}			600			400			400	pA
Common-Mode Rejection		104			110			110			dB
	T_{min} – T_{max}	102			104			104			dB
Power Supply Rejection		104			110			110			dB
	T_{min} – T_{max}	102			104			104			dB
Crosstalk	f = 10 Hz										
	R_L = 2 kΩ		135			135			135		dB
FREQUENCY RESPONSE											
UNITY GAIN											
Crossover Frequency		0.4	0.8		0.4	0.8		0.4	0.8		MHz
Slew Rate, Unity Gain	G = – 1	0.1	0.15		0.1	0.15		0.1	0.15		V/μs
Slew Rate	T_{min} – T_{max}	0.05	0.15		0.05	0.15		0.05	0.15		V/μs
INPUT IMPEDANCE											
Differential			40//2			40//2			40//2		MΩ//pF
Common Mode			300//2			300//2			300//2		GΩ//pF
INPUT VOLTAGE RANGE											
Common Mode Voltage		±13.5	±14		±13.5	±14		±13.5	±14		V
Common Mode Rejection											
Ratio	V_{CM} = ±13.5 V	110	132		114	132		114	132		dB
	T_{min} to T_{max}	108	128		108	128		108	128		dB
INPUT CURRENT NOISE	0.1 to 10 Hz		3			3	12		3	12	pA p–p
	f = 10 Hz		50			50			50		fA/$\sqrt{Hz}$
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.5			0.5			0.5	1.0	μV p–p
	f = 10 Hz		17			17			17		nV/$\sqrt{Hz}$
	f = 1 kHz		15	22		15	22		15	22	nV/$\sqrt{Hz}$
OPEN-LOOP GAIN	V_O = ±12 V										
	R_{LOAD} = 10 kΩ	200	2000		400	2000		400	2000		V/mV
	T_{min} to T_{max}	150	1500		300	1500		300	1500		V/mV
	V_O = ±10 V										
	R_{LOAD} = 2 kΩ	200	1000		300	1000		300	1000		V/mV
	T_{min} – T_{max}	150	1000		200	1000		200	1000		V/mV
OUTPUT CHARACTERISTICS											
Voltage Swing	R_{LOAD} = 10 kΩ										
	T_{min} – T_{max}	±13	±14		±13	±14		±13	±14		V
Current	Short Circuit		±15			±15			±15		mA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Model	Conditions	AD704J/A Min	AD704J/A Typ	AD704J/A Max	AD704K/B Min	AD704K/B Typ	AD704K/B Max	AD704T Min	AD704T Typ	AD704T Max	Units
CAPACITIVE LOAD											
Drive Capability	Gain = +1		10,000			10,000			10,000		pF
Output Resistance	Open-Loop		200			200			200		Ω
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±2.0		±18	±2.0		±18	±2.0		±18	V
Quiescent Current			1520	2400		1520	2400		1520	2400	μA
	T_{min} – T_{max}		1600	2600		1600	2600		1600	2600	μA
TRANSISTOR COUNT	No. of Transistors		180			180			180		

NOTES
[1]Bias Current Specifications are guaranteed maximum at either input.
Specifications subject to change without notice.
All min and max specifications are guaranteed.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±0.7 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
Q . . . . . −65°C to +150°C
N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD704J/K . . . . . 0 to +70°C
AD704A/B . . . . . −40°C to +85°C
AD704T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
14-Pin Plastic Package: θ_{JA} = 85°C/Watt
14-Pin Cerdip Package: θ_{JA} = 110°C/Watt
16-Pin Wide-Body Small Outline Package: θ_{JA} = 100°C/Watt
[3]The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.

ORDERING GUIDE*

Temperature Range	14-Pin Plastic Mini-DIP (N-14)	14-Pin Cerdip (Q-14)	16-Pin SOIC (R-16)
0 to +70°C	AD704JN AD704KN		AD704JR
−40°C to +85°C		AD704AQ AD704BQ	
−55°C to +125°C		AD704TQ	

*See Section 20 for package outine information.

Picoampere Input-Current Bipolar Op Amp

AD705

FEATURES

DC PERFORMANCE
- 25 μV max Offset Voltage (AD705T)
- 0.6 μV/°C max Drift (AD705K/T)
- 100 pA max Input Bias Current (AD705K)
- 250 pA max I_B Over MIL Temperature Range (AD705T)
- 114 dB min CMRR (AD705K/T)
- 114 dB min PSRR (AD705T)
- 200 V/mV min Open Loop Gain
- 0.5 μV p–p typ Noise, 0.1 Hz to 10 Hz
- 600 μA max Supply Current

AC PERFORMANCE
- 0.15 V/μs Slew Rate
- 800 kHz Unity Gain Crossover Frequency
- 10,000 pF Capacitive Load Drive Capability
- Low Cost
- Available in 8 Pin Plastic Mini-DIP, Hermetic Cerdip, Surface Mount (SOIC) Packages and Chip Form
- MIL-STD-883B Processing Available
- Dual Version Available: 706

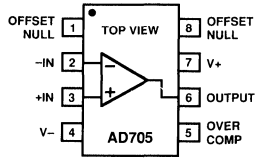
APPLICATIONS
- Low Frequency Active Filters
- Precision Instrumentation
- Precision Integrators

PRODUCT DESCRIPTION

The AD705 is a low power bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower I_B drift over temperature. The AD705 offers many of the advantages of BiFET and bipolar op amps without their inherent disadvantages. It utilizes superbeta bipolar input transistors to achieve the picoampere input bias current levels of FET input amplifiers (at room temperature), while its I_B typically only increases 5 times vs. BiFET amplifiers which exhibit a 1000X increase over temperature. This means that, at room temperature, while a typical BiFET may have less I_B than the AD705, the BiFET's input current will increase to a level of several nA at +125°C. Superbeta bipolar technology also permits the AD705 to achieve the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

The AD705 is a high quality replacement for the industry-standard OP-07 amplifier while drawing only one sixth of its power supply current. Since it has only 1/20th the input bias current of an OP-07, the AD705 can be used with much higher source impedances, while providing the same level of dc precision. In addition, since the input bias currents are at picoAmp levels, the commonly used "balancing" resistor (connected between the noninverting input of a bipolar op amp and ground) is not required.

AD705 CONNECTION DIAGRAM



8 PIN PLASTIC MINIDIP (N), CERDIP (Q) AND SOIC (R) PACKAGES

The AD705 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation and as a high quality integrator.

The AD705 is internally compensated for unity gain and is available in five performance grades. The AD705J and AD705K are rated over the commercial temperature range of 0 to +70°C. The AD705A and AD705B are rated over the industrial temperature range of −40°C to +85°C. The AD705T is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD705 is offered in three varieties of 8-pin package: plastic DIP, hermetic cerdip and surface mount (SOIC). "J" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD705 is a low drift op amp that offers BiFET level input bias currents, yet has the low I_B drift of a Bipolar amplifier. It upgrades the performance of circuits using op amps such as the OP-07, OP-97 and LT1012.
2. The combination of Analog Devices' advanced Superbeta processing technology and factory trimming provides both low drift and high dc precision.
3. The AD705 can be used in applications where a chopper amplifier would normally be required but without the chopper's inherent noise and other problems.

SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, and V_S = ±15 V dc, unless otherwise noted)

Parameter	Conditions	AD705J/A Min	AD705J/A Typ	AD705J/A Max	AD705K/B Min	AD705K/B Typ	AD705K/B Max	AD705T Min	AD705T Typ	AD705T Max	Units
INPUT OFFSET VOLTAGE											
Initial Offset			30	**90**		10	**35**		10	**25**	μV
Offset	T_{min} to T_{max}		45	150		25	**60**		25	**60**	μV
vs. Temp, Average TC			0.2	1.2		0.2	0.6		0.2	**0.6**	μV/°C
vs. Supply (PSRR)	V_S = ±2 V to ±18 V	**110**	129		**110**	129		**114**	129		dB
T_{min} to T_{max}	V_S = ±2.5 V to ±18 V	108	126		108	126		**108**	126		dB
Long Term Stability			0.3			0.3			0.3		μV/month
INPUT BIAS CURRENT[1]											
	V_{CM} = 0 V		60	**150**		30	**100**		30	**100**	pA
	V_{CM} = ±13.5 V		80	200		50	**150**		50	**150**	pA
vs. Temp, Average TC			0.3			0.3			0.6		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V		80	250		50	150		90	**250**	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V		100	450		70	350		120	**450**	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	**150**		30	**100**		30	**100**	pA
	V_{CM} = ±13.5 V		40	200		30	**150**		30	**150**	pA
vs. Temp, Average TC			0.3			0.3			0.4		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V		80	250		50	150		80	**250**	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V		80	450		50	350		80	**450**	pA
FREQUENCY RESPONSE											
Unity Gain											
Crossover Frequency		0.4	0.8		0.4	0.8		0.4	0.8		MHz
Slew Rate, Unity Gain	G = −1	0.1	0.15		0.1	0.15		0.1	0.15		V/μs
Slew Rate	T_{min} to T_{max}	0.05	0.15		0.05	0.15		0.05	0.15		V/μs
INPUT IMPEDANCE											
Differential			40//2			40//2			40//2		MΩ//pF
Common Mode			300//2			300//2			300//2		GΩ//pF
INPUT VOLTAGE RANGE											
Common Mode Voltage		±13.5	±14		±13.5	±14		±13.5	±14		V
COMMON MODE											
REJECTION RATIO	V_{CM} = ±13.5 V	**110**	132		**114**	132		**114**	132		dB
	T_{min} to T_{max}	108	128		108	128		**108**	128		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.5			0.5	1.0		0.5	1.0	μV p-p
	f = 10 Hz		17			17			17		nV/$\sqrt{Hz}$
	f = 1 kHz		15	22		15	22		15	22	nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f = 10 Hz		50			50			50		fA/$\sqrt{Hz}$
OPEN LOOP GAIN	V_O = ±12 V										
	R_{LOAD} = 10 kΩ	**300**	2000		**400**	2000		**400**	2000		V/mV
	T_{min} to T_{max}	200	1500		300	1500		300	1500		V/mV
	V_O = ±10 V										
	R_{LOAD} = 2 kΩ	**200**	1000		**300**	1000		**300**	1000		V/mV
	T_{min} to T_{max}	150	1000		200	1000		**200**	1000		V/mV
OUTPUT CHARACTERISTICS											
Voltage Swing	R_{LOAD} = 10 kΩ	±13	±14		±13	±14		±13	±14		V
	T_{min} to T_{max}	**±13**	±14		**±13**	±14		**±13**	±14		V
Current	Short Circuit		±15			±15			±15		mA
Capacitive Load											
Drive Capability	Gain = +1		10,000			10,000			10,000		pF
Output Resistance	Open Loop		200			200			200		Ω
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±2.0**		**±18**	**±2.0**		**±18**	**±2.0**		**±18**	V
Quiescent Current			380	**600**		380	**600**		380	**600**	μA
	T_{min} to T_{max}		400	800		400	800		400	**800**	μA
TEMPERATURE RANGE FOR RATED PERFORMANCE											
Commercial (0 to +70°C)			AD705J			AD705K					
Industrial (−40°C to +85°C)			AD705A			AD705B					
Military (−55°C to +125°C)									AD705T		

PACKAGE OPTIONS[2] 8-Pin Cerdip (Q-8) 8-Pin Plastic Mini-DIP (N-8) 8-Pin SOIC (R-8)		AD705AQ AD705JN AD705JR	AD705BQ AD705KN	AD705TQ
TRANSISTOR COUNT	# of Transistors	45	45	45

NOTES
[1]Bias Current Specifications are guaranteed maximum at either input.
[2]See Section 20 for package outline information.
All min and max specifications are guaranteed.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
Specifications subject to change without notice.

2

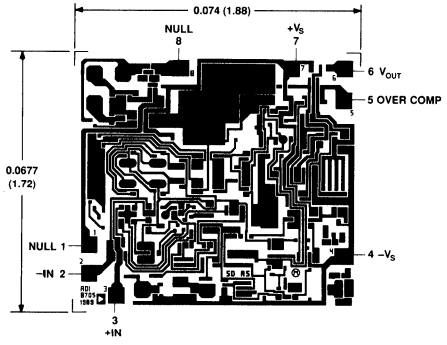
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±0.7 Volts
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD705J/K . . . . . 0 to +70°C
AD705A/B . . . . . −40°C to +85°C
AD705T . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt
[3]The Input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



Typical Characteristics (@ +25°C, V_S = ±15 V, unless otherwise noted)

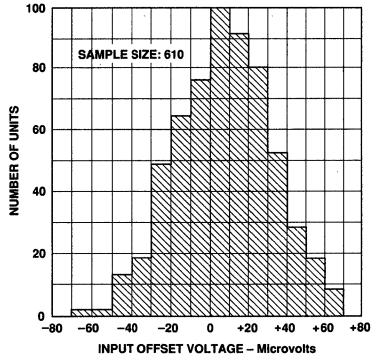


Figure 1. Typical Distribution of Input Offset Voltage

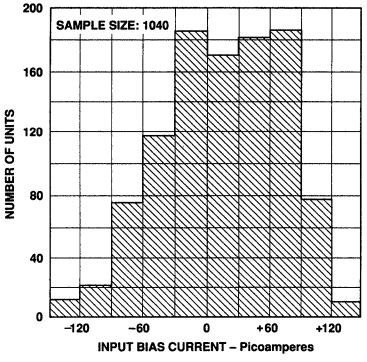


Figure 2. Typical Distribution of Input Bias Current

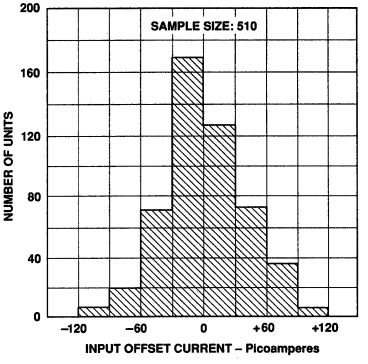


Figure 3. Typical Distribution of Input Offset Current

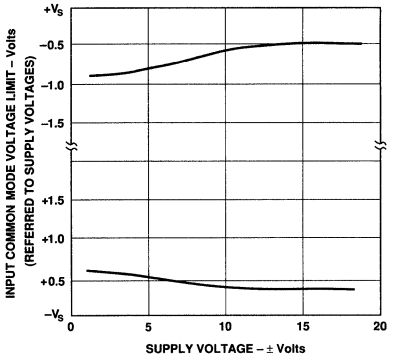


Figure 4. Input Common Mode Voltage Range vs. Supply Voltage

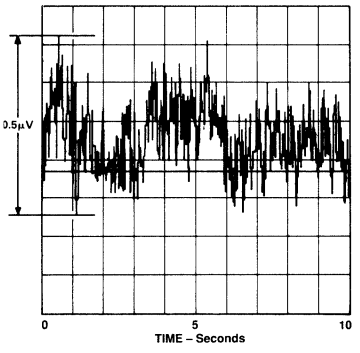


Figure 5. 0.1 Hz to 10 Hz Noise Voltage

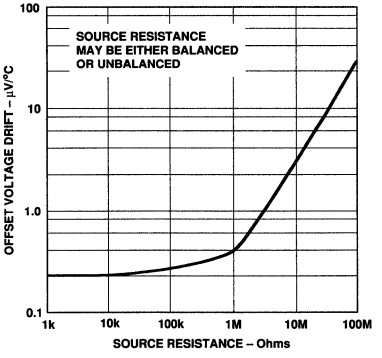


Figure 6. Offset Voltage Drift vs. Source Resistance

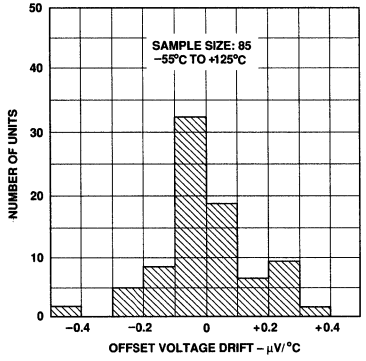


Figure 7. Typical Distribution of Offset Voltage Drift

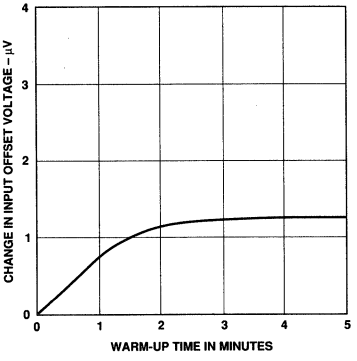


Figure 8. Change in Input Offset Voltage vs. Warm-Up Time

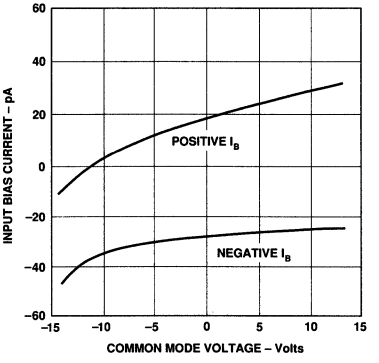


Figure 9. Input Bias Current vs. Common Mode Voltage

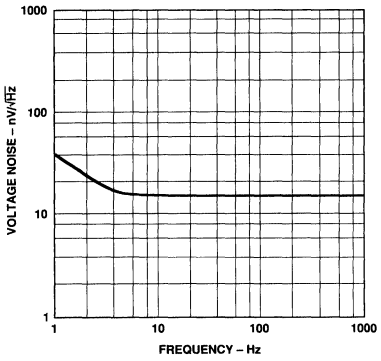


Figure 10. Input Noise Voltage Spectral Density

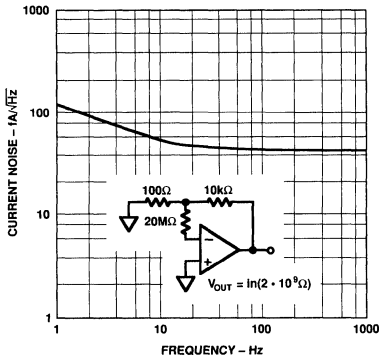


Figure 11. Input Noise Current Spectral Density

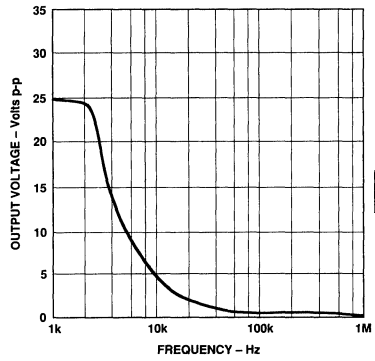


Figure 12. Large Signal Frequency Response

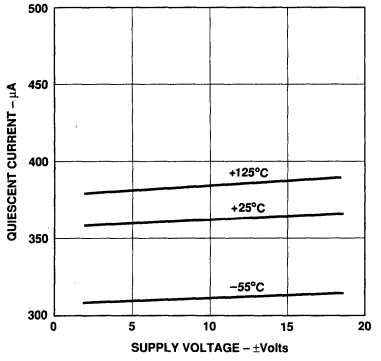


Figure 13. Quiescent Supply Current vs. Supply Voltage

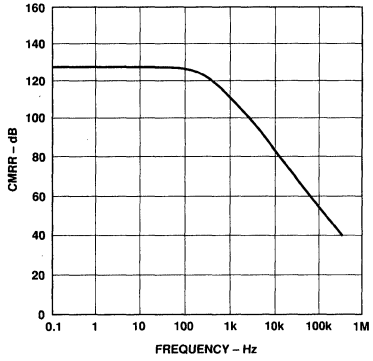


Figure 14. Common Mode Rejection vs. Frequency

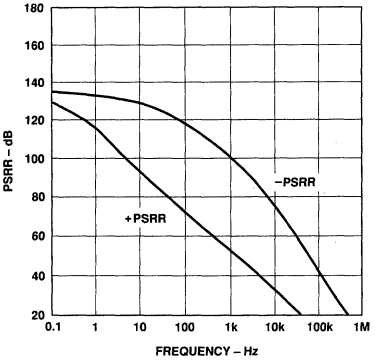


Figure 15. Power Supply Rejection vs. Frequency

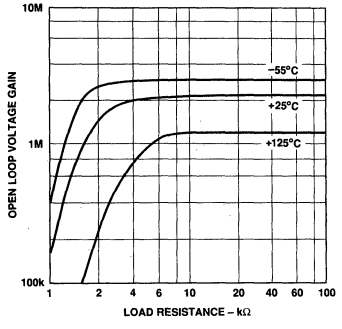


Figure 16. Open Loop Gain vs. Load Resistance over Temperature

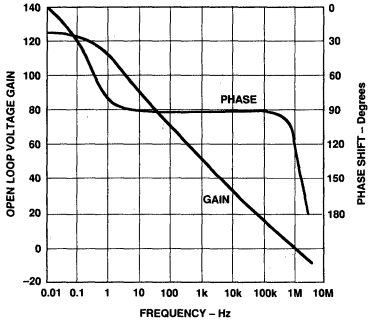


Figure 17. Open Loop Gain and Phase Shift vs. Frequency

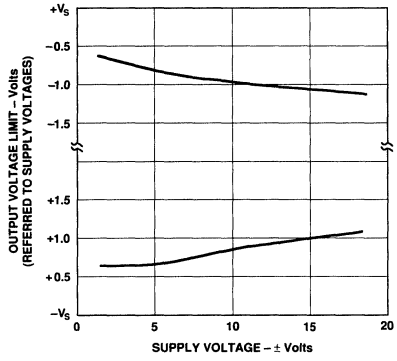


Figure 18. Output Voltage Limit vs. Supply Voltage

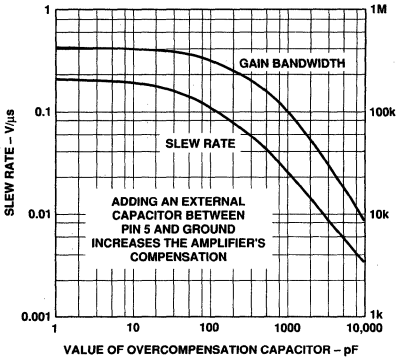


Figure 19. Slew Rate & Gain Bandwidth Product vs. Value of Overcompensation Capacitor

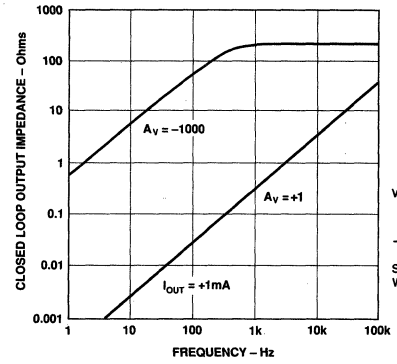


Figure 20. Magnitude of Closed Loop Output Impedance vs. Frequency

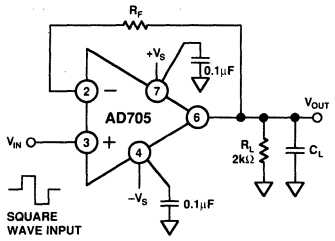


Figure 21a. Unity Gain Follower (For Large Signal Applications, Resistor R_F Limits the Current Through the Input Protection Diodes)

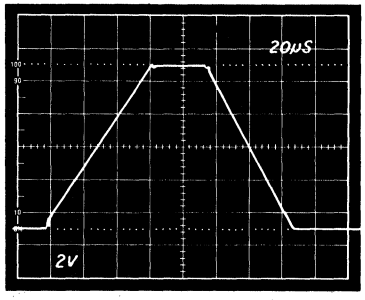


Figure 21b. Unity Gain Follower Large Signal Pulse Response R_F = 10 kΩ, C_L = 50 pF

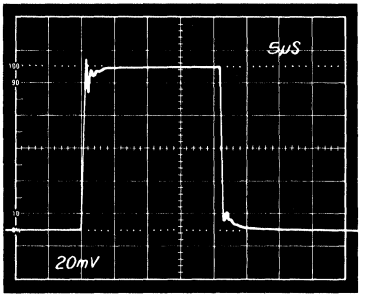


Figure 21c. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 100 pF

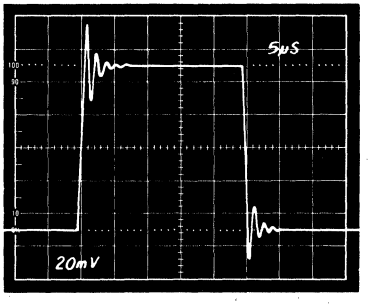


Figure 21d. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 1000 pF

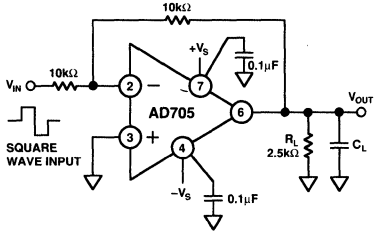


Figure 22a. Unity Gain Inverter

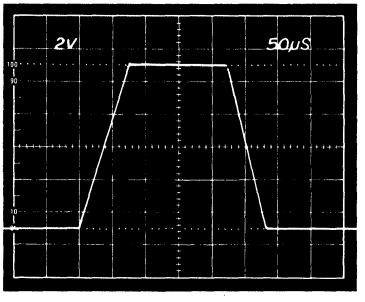


Figure 22b. Unity Gain Inverter Large Signal Pulse Response C_L = 50 pF

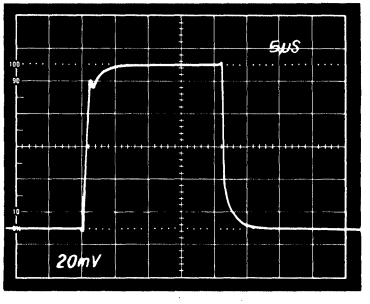


Figure 22c. Unity Gain Inverter Small Signal Pulse Response C_L = 100 pF

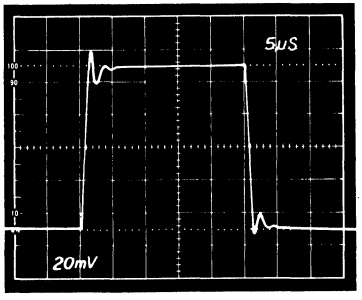


Figure 22d. Unity Gain Inverter Small Signal Pulse Response C_L = 1000 pF

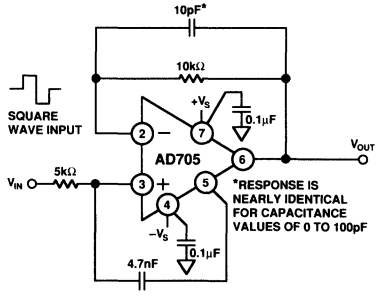


Figure 23a. Follower Connected in Feed-Forward Mode

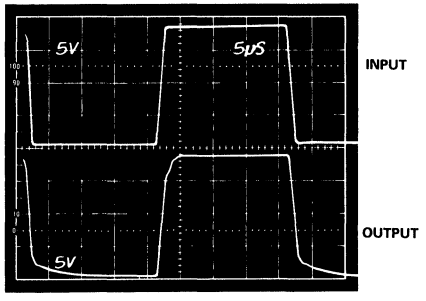


Figure 23b. Follower Feed-Forward Pulse Response

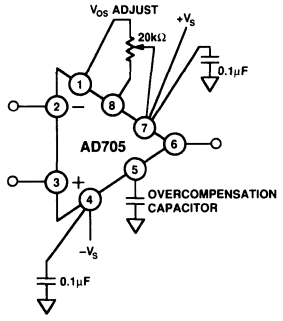


Figure 24. Offset Null and Overcompensation Connections

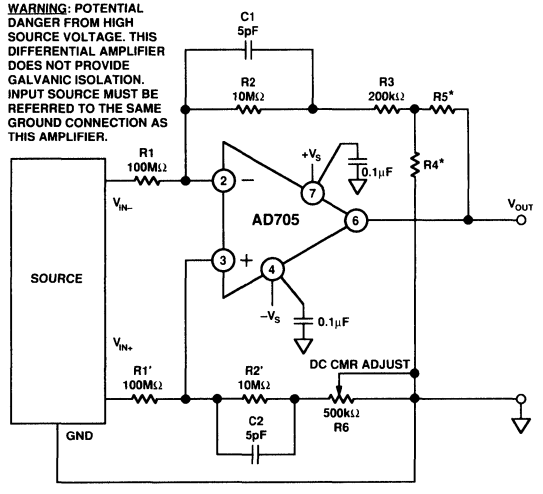


Figure 25. A High Performance Differential Amplifier Circuit

A High Performance Differential Amplifier Circuit

Figure 25 shows a high input impedance, differential amplifier circuit that features a high common mode voltage, and which operates at low power. Table I details its performance with changes in gain. To optimize the common mode rejection of this circuit at low frequencies and dc, apply a 1 volt, 1 Hz sine wave to both inputs. Measuring the output with an oscilloscope, adjust trimming potentiometer R6 for minimum output. For the best CMR at higher frequencies, capacitor C2 should be replaced with a 1.5 pF to 20 pF trimmer capacitor.

Both the IC socket and any standoffs at the op amp's input terminals should be made of Teflon* to maintain low input current drift over temperature.

*Teflon is a registered trademark of E.I. DuPont, Co.

Circuit Gain	R4 (Ω)	R5 (Ω)	Trimmed DC CMR (dB)	RTI Average Drift TC (μV/°C)	Circuit Bandwidth −3 dB
1	1.13 kΩ	10 kΩ	≥85	30	4.4 kHz
10	100 Ω	9.76 kΩ	≥85	30	2.8 kHz
100	10.2 Ω	10 kΩ	≥85	30	930 Hz

Table I. Typical Performance of Differential Amplifier Circuit Operating at Various Gains

A 1 Hz, 2-Pole, Active Filter

Table II gives recommended component values for the 1 Hz filter of Figure 26. An unusual characteristic of the AD705 is that both the input bias current and the input offset current and their drift remain low over most of the op amps rated temperature range. Therefore, for most applications, there is no need to use the normal balancing resistor tied between the noninverting terminal of the op amp and ground. Eliminating the standard balancing resistor reduces board space and lowers circuit noise. However, this resistor is needed at temperatures above 110°C, because input bias current starts to change rapidly, as shown by Figure 27.

Desired Low Pass Response	Pole Frequency (Hz)	Pole Q	C1 Value (μF)	C2 Value (μF)
Bessel Response	1.27	0.58	0.14	0.11
Butterworth Response	1.00	0.707	0.23	0.11
0.1 dB Chebychev	0.93	0.77	0.26	0.11
0.2 dB Chebychev	0.90	0.80	0.28	0.11
0.5 dB Chebychev	0.85	0.86	0.32	0.11
1.0 dB Chebychev	0.80	0.96	0.38	0.10

Specified Values are for a −3 dB point of 1.0 Hz.

For other frequencies, simply scale capacitors C1 and C2 directly; i.e., for 3 Hz Bessel response, C1 = 0.046 μF, C2 = 0.037 μF.

Table II. Recommended Component Values for the 1 Hz Low Pass Filter

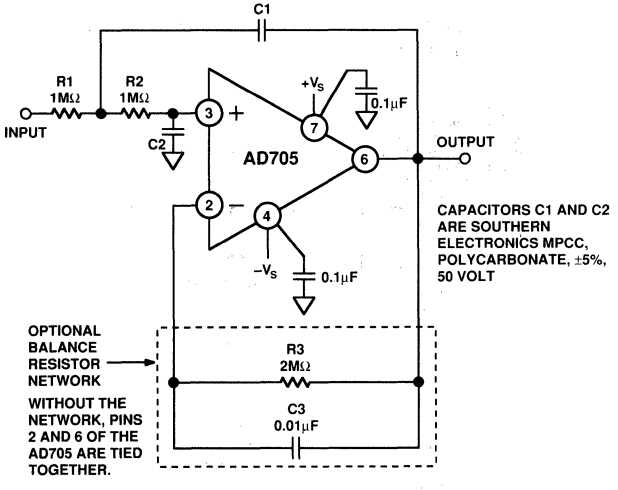


Figure 26. A 1 Hz, 2-Pole Active Filter

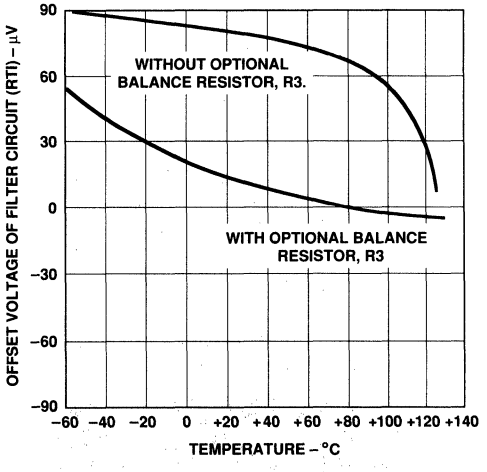


Figure 27. V_{OS} vs. Temperature of 1 Hz Filter

ANALOG DEVICES

Dual Picoampere Input Current Bipolar Op Amp

AD706

FEATURES
HIGH DC PRECISION
50 μV max Offset Voltage
0.6 μV/°C max Offset Drift
110 pA max Input Bias Current

LOW NOISE
0.5 μV p–p Voltage Noise, 0.1 Hz to 10 Hz

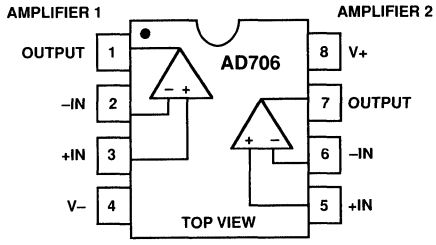
LOW POWER
750 μA Supply Current

Available in 8-Pin Plastic Mini-DIP, Hermetic Cerdip and Surface Mount (SOIC) Packages
MIL-STD-883B Processing Available
Single Version: AD705, Quad Version (AD704)

PRIMARY APPLICATIONS
Low Frequency Active Filters
Precision Instrumentation
Precision Integrators

AD706 CONNECTION DIAGRAM

Plastic Mini-DIP (N)
Cerdip (Q) and
Plastic SOIC (R) Packages



PRODUCT DESCRIPTION

The AD706 is a dual, low power, bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower I_B drift over temperature. It utilizes super-beta bipolar input transistors to achieve picoampere input bias current levels (similar to FET input amplifiers at room temperature), while its I_B typically only increases by 5× at 125°C (unlike a BiFET amp, for which I_B doubles every 10°C for a 1000× increase at 125°C). The AD706 also achieves the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

Since it has only 1/20 the input bias current of an OP-07, the AD706 does not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the OP-07 which makes this amplifier usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the OP-07, the AD706 is better suited for today's higher density boards.

The AD706 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation, and as a high quality integrator. The AD706 is internally compensated for unity gain and is available in five performance grades. The AD706J and AD706K are rated over the commercial temperature range of 0 to +70°C. The AD706A and AD706B are rated over the industrial temperature range of −40°C to +85°C. The AD706T is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD706 is offered in three varieties of an 8-pin package: plastic mini-DIP, hermetic cerdip and surface mount (SOIC). "J" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD706 is a dual low drift op amp that offers BiFET level input bias currents, yet has the low I_B drift of a bipolar amplifier. It may be used in circuits using dual op amps such as the OP-200, and LT1024.
2. The AD706 provides both low drift and high dc precision.
3. The AD706 can be used in applications where a chopper amplifier would normally be required but without the chopper's inherent noise.

SPECIFICATIONS (@ T_A = +25° C, V_{CM} = 0 V, and ±15 V dc, unless otherwise noted)

Parameter	Conditions	AD706J/A Min	AD706J/A Typ	AD706J/A Max	AD706K/B Min	AD706K/B Typ	AD706K/B Max	AD706T Min	AD706T Typ	AD706T Max	Units
INPUT OFFSET VOLTAGE											
Initial Offset			30	100		10	50		10	50	µV
Offset	T_{min} to T_{max}		40	150		25	100		25	100	µV
vs. Temp, Average TC			0.2	1.5		0.2	0.6		0.2	0.6	µV/°C
vs. Supply (PSRR)	V_S = ±2 V to ±18 V	110	132		112	132		112	132		dB
T_{min} to T_{max}	V_S = ±2.5 V to ±18 V	106	126		108	126		108	126		dB
Long Term Stability			0.3			0.3			0.3		µV/month
INPUT BIAS CURRENT[1]											
	V_{CM} = 0 V		50	200		30	110		30	120	pA
	V_{CM} = ±13.5 V			250			160			170	pA
vs. Temp, Average TC			0.3			0.2			0.2		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V			300			200			400	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V			400			300			600	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		30	150		30	100		30	100	pA
	V_{CM} = ±13.5 V			250			200			200	pA
vs. Temp, Average TC			0.6			0.4			0.4		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V		80	250		80	200		80	300	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V		80	350		80	300		80	450	pA
MATCHING CHARACTERISTICS											
Offset Voltage				150			75			75	µV
	T_{min} to T_{max}			250			150			200	µV
Input Bias Current[2]				300			150			200	pA
	T_{min} to T_{max}			500			250			400	pA
Common-Mode Rejection		106			110			110			dB
	T_{min} to T_{max}	106			108			108			dB
Power Supply Rejection		106			110			110			dB
	T_{min} to T_{max}	104			106			106			dB
Crosstalk	@ f = 10 Hz										
(Figure 19a)	R_L = 2 kΩ		150			150			150		dB
FREQUENCY RESPONSE											
Unity Gain Crossover Frequency			0.8			0.8			0.8		MHz
Slew Rate	G = −1		0.15			0.15			0.15		V/µs
	T_{min} to T_{max}		0.15			0.15			0.15		V/µs
INPUT IMPEDANCE											
Differential			40//2			40//2			40//2		MΩ//pF
Common Mode			300//2			300//2			300//2		GΩ//pF
INPUT VOLTAGE RANGE											
Common-Mode Voltage		±13.5	±14		±13.5	±14		±13.5	±14		V
Common-Mode Rejection Ratio	V_{CM} = ±13.5 V	110	132		114	132		114	132		dB
	T_{min} to T_{max}	108	128		108	128		108	128		dB
INPUT CURRENT NOISE	0.1 Hz to 10 Hz		3			3			3		pA p-p
	f = 10 Hz		50			50			50		fA/√Hz
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.5			0.5	1.0		0.5	1.0	µV p-p
	f = 10 Hz		17			17			17		nV/√Hz
	f = 1 kHz		15	22		15	22		15	22	nV/√Hz
OPEN-LOOP GAIN	V_O = ±12 V										
	R_{LOAD} = 10 kΩ	200	2000		400	2000		400	2000		V/mV
	T_{min} to T_{max}	150	1500		300	1500		300	1500		V/mV
	V_O = ±10 V										
	R_{LOAD} = 2 kΩ	200	1000		300	1000		200	1000		V/mV
	T_{min} to T_{max}	150	1000		200	1000		100	1000		V/mV
OUTPUT CHARACTERISTICS											
Voltage Swing	R_{LOAD} = 10 kΩ	±13	±14		±13	±14		±13	±14		V
	T_{min} to T_{max}	±13	±14		±13	±14		±13	±14		V
Current	Short Circuit		±15			±15			±15		mA
Capacitive Load Drive Capability	Gain = +1		10,000			10,000			10,000		pF

Parameter	Conditions	AD706J/A Min	AD706J/A Typ	AD706J/A Max	AD706K/B Min	AD706K/B Typ	AD706K/B Max	AD706T Min	AD706T Typ	AD706T Max	Units
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±2.0		±18	±2.0		±18	±2.0		±18	V
Quiescent Current, Total			0.75	1.2		0.75	1.2		0.75	1.2	mA
	T_{min} to T_{max}		0.8	1.4		0.8	1.4		0.8	1.6	mA
TRANSISTOR COUNT	# of Transistors		90			90			90		

NOTES
[1]Bias current specifications are guaranteed maximum at either input.
[2]Input bias current match is the difference between corresponding inputs (I_B of −IN of Amplifier #1 minus I_B of −IN of Amplifier #2).
Specifications subject to change without notice.

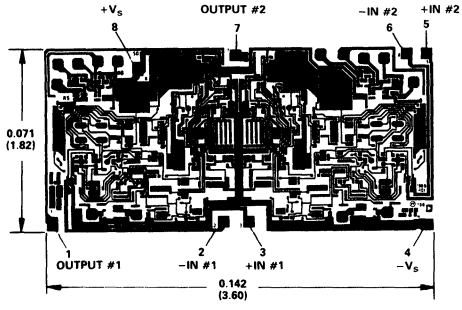
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation
(Total: Both Amplifiers)[2] . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±0.7 Volts
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD706J/K . . . . . 0 to +70°C
AD706A/B . . . . . −40°C to +85°C
AD706T . . . . . −55°C to +125°C
Lead Temperature (Soldering 10 secs) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 100°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt
[3]The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



ORDERING GUIDE*

Temperature Range	8-Pin Plastic Mini-DIP (N-8)	8-Pin Cerdip (Q-8)	8-Pin SOIC (R-8)
0 to +70°C	AD706JN AD706KN		AD706JR
−40°C to +85°C		AD706AQ AD706BQ	
−55°C to +125°C		AD706TQ	

*See Section 20 for package outline information.

Typical Characteristics (@ +25°C, V_S = ±15 V, unless otherwise noted)

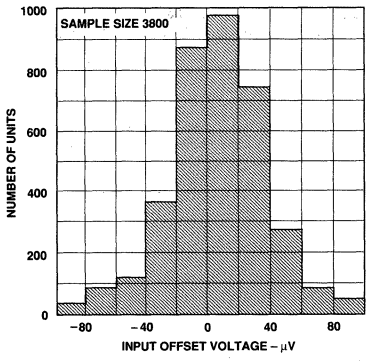


Figure 1. Typical Distribution of Input Offset Voltage

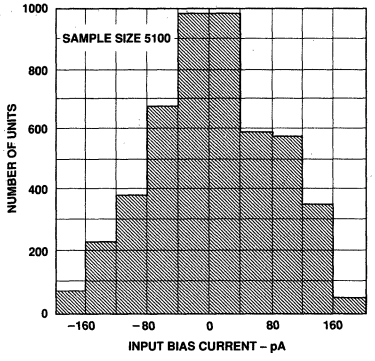


Figure 2. Typical Distribution of Input Bias Current

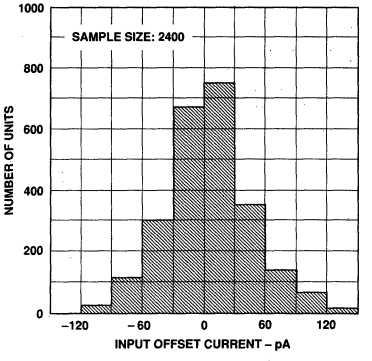


Figure 3. Typical Distribution of Input Offset Current

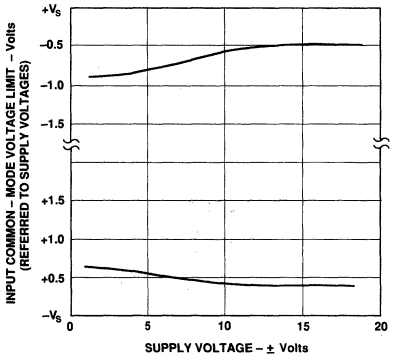


Figure 4. Input Common-Mode Voltage Range vs. Supply Voltage

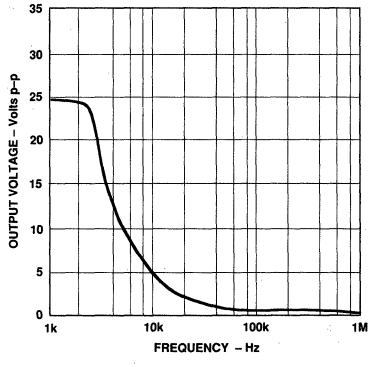


Figure 5. Large Signal Frequency Response

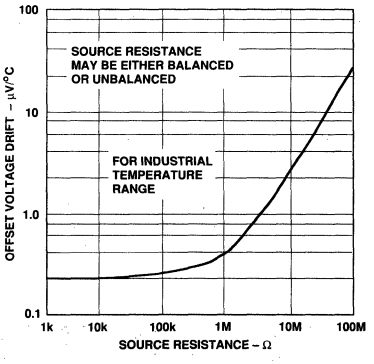


Figure 6. Offset Voltage Drift vs. Source Resistance

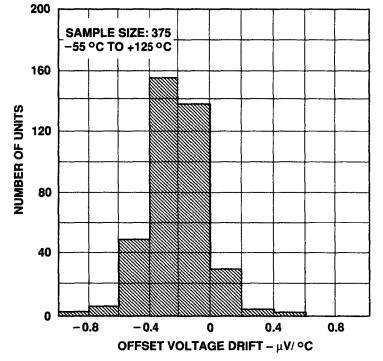


Figure 7. Typical Distribution of Offset Voltage Drift

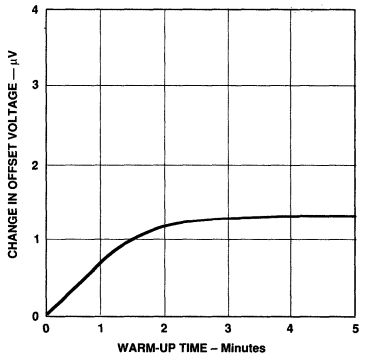


Figure 8. Change in Input Offset Voltage vs. Warm-up Time

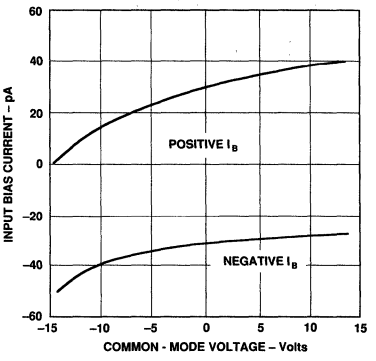


Figure 9. Input Bias Current vs. Common-Mode Voltage

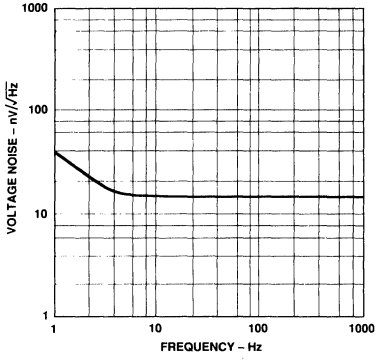


Figure 10. Input Noise Voltage Spectral Density

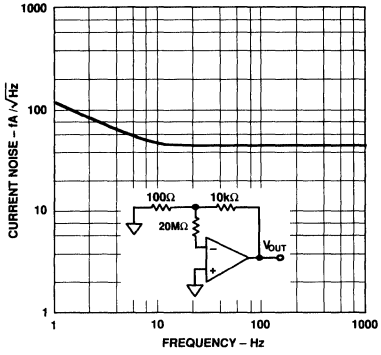


Figure 11. Input Noise Current Spectral Density

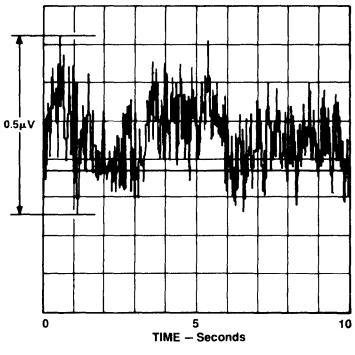


Figure 12. 0.1 Hz to 10 Hz Noise Voltage

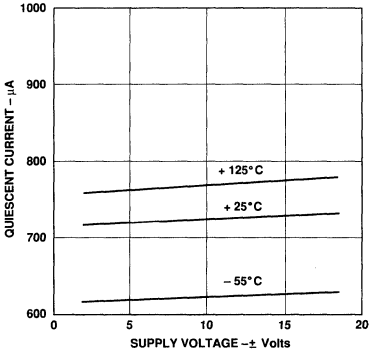


Figure 13. Quiescent Supply Current vs. Supply Voltage

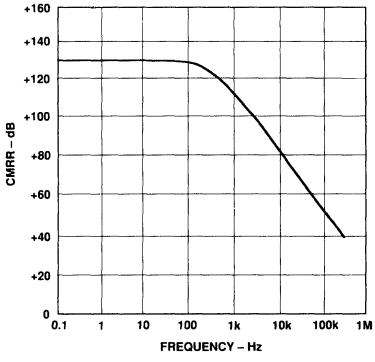


Figure 14. Common-Mode Rejection Ratio vs. Frequency

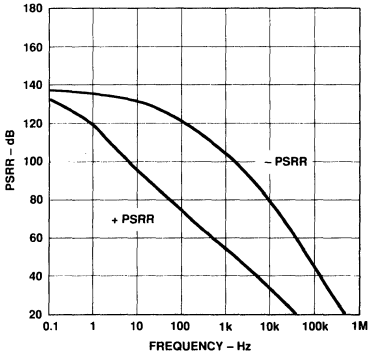
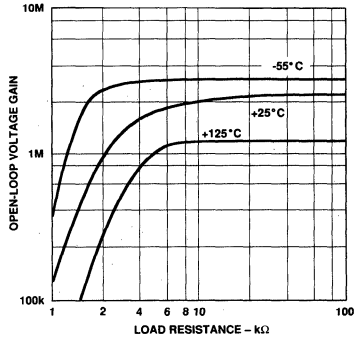
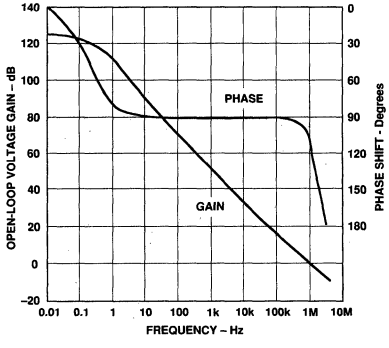


Figure 15. Power Supply Rejection Ratio vs. Frequency





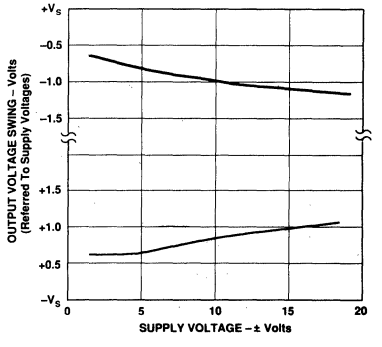


Figure 16. Open-Loop Gain vs. Load Resistance vs. Temperature

Figure 17. Open-Loop Gain and Phase Shift vs. Frequency

Figure 18. Output Voltage Swing vs. Supply Voltage

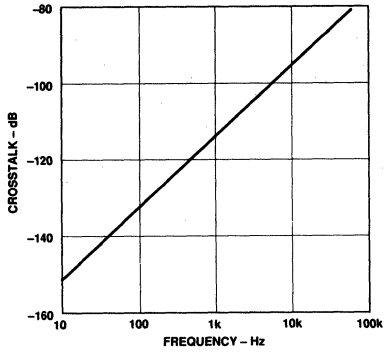


Figure 19a. Crosstalk vs. Frequency

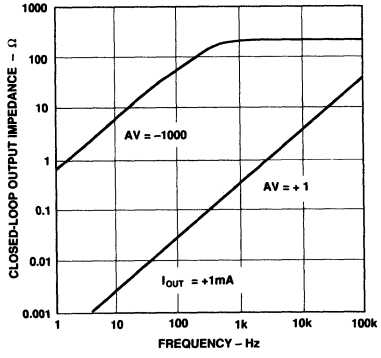


Figure 20. Magnitude of Closed-Loop Output Impedance vs. Frequency

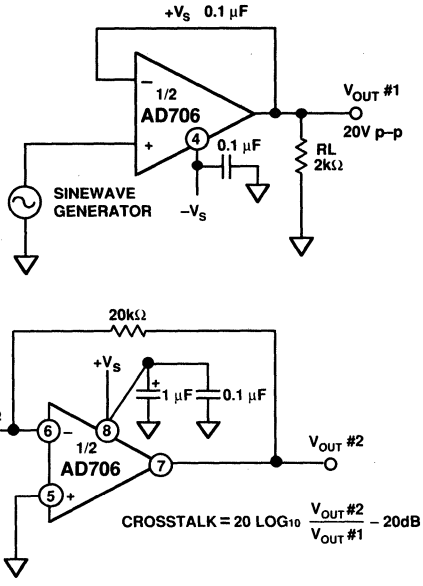


Figure 19b. Crosstalk Test Circuit

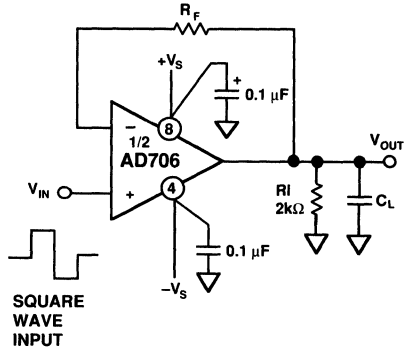


Figure 21a. Unity Gain Follower (For Large Signal Applications, Resistor R_F Limits the Current Through the Input Protection Diodes.)

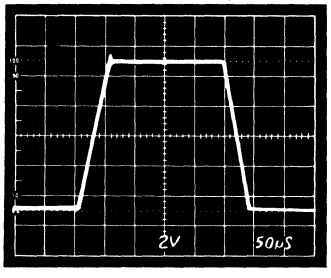


Figure 21b. Unity Gain Follower Large Signal Pulse Response R_F = 10 kΩ, C_L = 1,000 pF

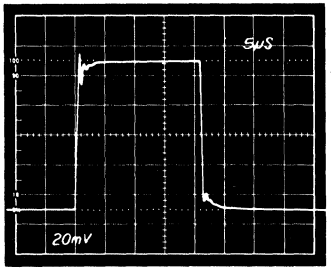


Figure 21c. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 100 pF

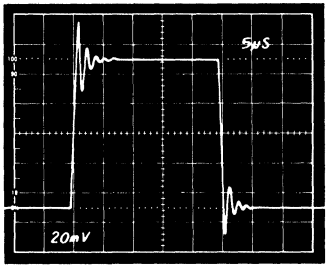


Figure 21d. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 1000 pF

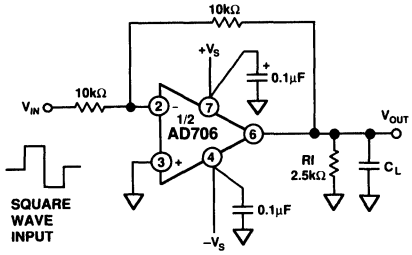


Figure 22a. Unity Gain Inverter Connection

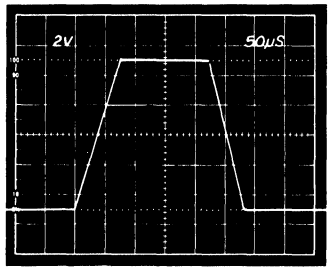


Figure 22b. Unity Gain Inverter Large Signal Pulse Response C_L = 1,000 pF

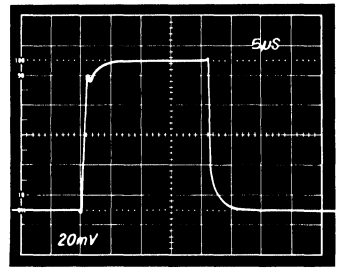


Figure 22c. Unity Gain Inverter Small Signal Pulse Response C_L = 100 pF

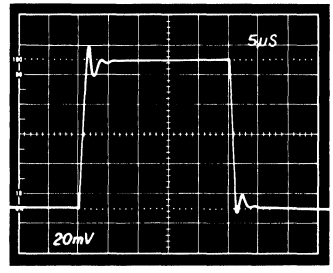


Figure 22d. Unity Gain Inverter Small Signal Pulse Response C_L = 1000 pF

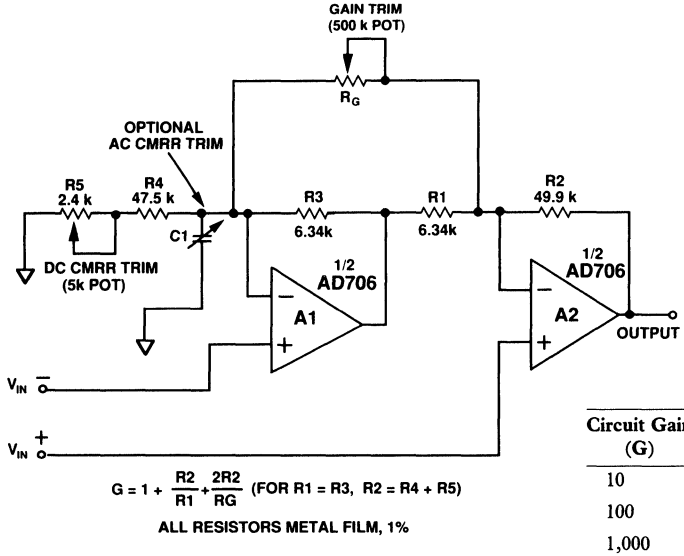


Figure 23. An Instrumentation Amplifier with a Gain of 10

Circuit Gain (G)	R1 & R3	R_G (Max Value of Potentiometer)	Bandwidth (−3 dB), Hz
10	6.34 kΩ	166 kΩ	50 k
100	526 Ω	16.6 kΩ	5 k
1,000	56.2 Ω	1.66 kΩ	0.5 k

Table I. Resistance Values for Various Gains

The instrumentation amplifier circuit of Figure 23 offers many performance benefits including BiFET-level input bias currents and low input offset voltage drift. It consumes only 1.0 mA quiescent current. Table I provides resistance values for 3 common circuit gains. For other gains, use the following equations:

$$R2 = R4 + R5 = 49.9\ k\Omega$$

$$R1 = R3 = \frac{49.9\ k\Omega}{0.9\ G - 1}$$

$$Max\ Value\ of\ R_G = \frac{99.8\ k}{0.06\ G}$$

$$C1 \approx \frac{1}{2\pi\ (R3)\ 5 \times 10^5}$$

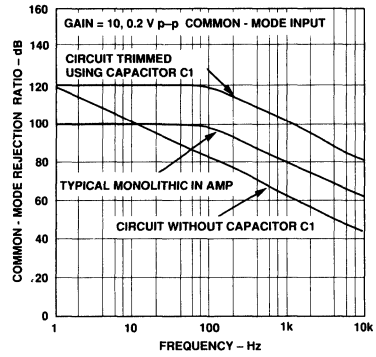


Figure 24. Common-Mode Rejection Ratio vs. Frequency vs. Value of Capacitor C1

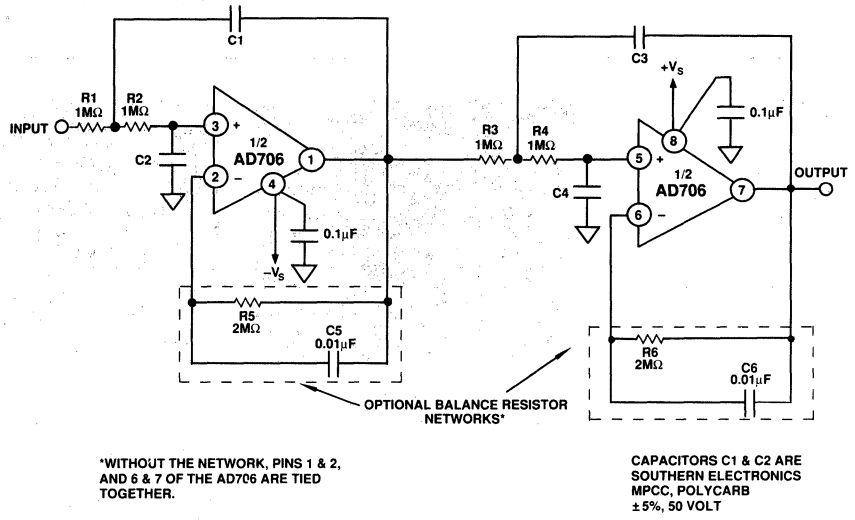


Figure 25. A 1 Hz, 4-Pole Active Filter

A 1 Hz, 4-Pole, Active Filter

An important characteristic of the AD706 is that both the input bias current, input offset current and their drift remain low over most of the op amp's rated temperature range. Therefore, for most applications, there is no need to use the normal balancing resistor. Adding the balancing resistor enhances performance at high temperatures, as shown by Figure 26.

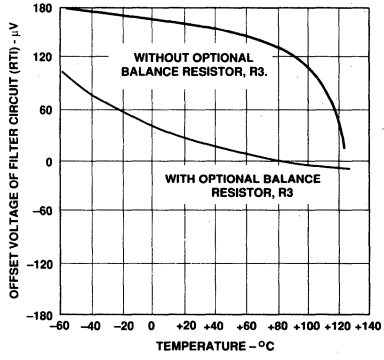


Figure 26. V_{OS} vs. Temperature Performance of the 1 Hz Filter

Desired Low Pass Response	Section 1 Frequency (Hz)	Q	Section 2 Frequency (Hz)	Q	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

NOTE
Specified Values are for a −3 dB point of 1.0 Hz. For other frequencies simply scale capacitors C1 through C4 directly; i.e.: for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357μF, C3 = 0.0533 μF, C4 = 0.0205 μF.

Table II. 1 Hz, 4-Pole, Low Pass Filter Recommended Component Values

ANALOG DEVICES

Ultralow Drift Op Amp

AD707

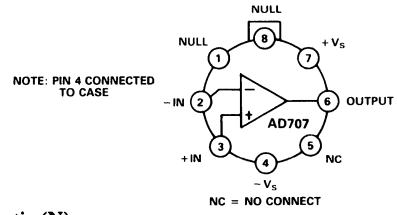
FEATURES

Very High DC Precision
15 μV max Offset Voltage
0.1 μV/°C max Offset Voltage Drift
0.35 μV p–p max Voltage Noise (0.1 Hz to 10 Hz)
8 V/μV min Open-Loop Gain
130 dB min CMRR
120 dB min PSRR
1 nA max Input Bias Current

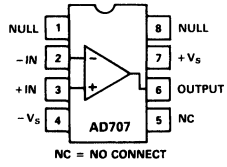
AC Performance
0.3 V/μs Slew Rate
0.9 MHz Closed-Loop Bandwidth
Dual Version: AD708

AD707 CONNECTION DIAGRAM

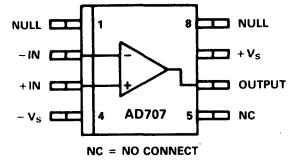
TO-99 (H) Package



Plastic (N) and Cerdip (Q) Packages



SOIC (R) Package



PRODUCT DESCRIPTION

The AD707 is a low cost, high precision op amp with state-of-the-art performance that makes it ideal for a wide range of precision applications. The offset voltage spec of less than 15 μV is the best available in a bipolar op amp, and maximum input offset current is 1.0 nA. The top grade is the first bipolar monolithic op amp to offer a maximum offset voltage drift of 0.1 μV/°C, and offset current drift and input bias current drift are both specified at 25 pA/°C maximum.

The AD707's open-loop gain is 8 V/μV minimum over the full ±10 V output range when driving a 1 kΩ load. Maximum input voltage noise is 350 nV p–p (0.1 Hz to 10 Hz). CMRR and PSRR are 130 dB and 120 dB minimum, respectively.

The AD707 is available in versions specified over commercial, industrial and military temperature ranges. It is offered in 8-pin plastic mini-DIP, small outline (SOIC), hermetic cerdip and hermetic TO-99 metal can packages. Chips, MIL-STD-883B, Rev. C, and tape & reel parts are also available.

APPLICATION HIGHLIGHTS

1. The AD707's 13 V/μV typical open-loop gain and 140 dB typical common-mode rejection ratio make it ideal for precision instrumentation applications.
2. The precision of the AD707 makes tighter error budgets possible at a lower cost.
3. The low offset voltage drift and low noise of the AD707 allow the designer to amplify very small signals without sacrificing overall system performance.
4. The AD707 can be used where chopper amplifiers are required, but without the inherent noise and application problems.
5. The AD707 is an improved pin-for-pin replacement for the OP-07, OP-77, OP-177 and the LT1001.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

	Conditions	AD707J/A Min	AD707J/A Typ	AD707J/A Max	AD707K/B/S Min	AD707K/B/S Typ	AD707K/B/S Max	AD707C/T Min	AD707C/T Typ	AD707C/T Max	Units
INPUT OFFSET VOLTAGE											
Initial			30	**90**		10	**25**		5	**15**	μV
vs. Temperature			0.3	1.0		0.1	**0.3**		0.03	**0.1**	μ V/°C
	T_{min} to T_{max}		50	100		15	**45**		7/8/8	**25**	μV
Long-Term Stability			0.3			0.3			0.2		μV/month
Adjustment Range	R2 =20 kΩ (Figure 19)		±4			±4			±4		mV
INPUT BIAS CURRENT			1.0	**2.5**		0.5	**1.5**		0.5	**1.0**	nA
	T_{min} to T_{max}		2.0	4.0		1.5	**3.0**		1.0	**2.0**	nA
Average Drift			15	40		15	25/25/35		10	25	pA/°C
OFFSET CURRENT	V_{CM}=0 V		0.5	**2.0**		0.3	**1.5**		0.1	**1.0**	nA
	T_{min} to T_{max}		2.0	4.0		1.0	**2.0**		0.2	**1.5**	nA
Average Drift			2	40		1	25/25/35		1	25	pA/°C
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.23	0.6		0.23	0.6		0.23	**0.35**	μV p-p
	f = 10 Hz		10.3	15		10.3	14		10.3	13	nV/√Hz
	f = 100 Hz		10.0	13.0		10.0	12		10.0	11.0	nV/√Hz
	f = 1 kHz		9.6	11.0		9.6	11.0		9.6	11.0	nV/√Hz
INPUT CURRENT NOISE	0.1 Hz to 10 Hz		14	35		14	30		14	**30**	pA p-p
	f = 10 Hz		0.32	0.9		0.32	0.8		0.32	0.8	pA/√Hz
	f = 100 Hz		0.14	0.27		0.14	0.23		0.14	0.23	pA/√Hz
	f = 1 kHz		0.12	0.18		0.12	0.17		0.12	0.17	pA/√Hz
COMMON-MODE REJECTION RATIO	V_{CM} = ±13 V	**120**	140		**130**	140		**130**	140		dB
	T_{min} to T_{max}	120	140		**130**	140		**130**	140		dB
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	**3**	13		5	13		**8**	13		V/μV
	T_{min} to T_{max}	3	13		5	13		**8**	13		V/μV
	R_{LOAD}≥1kΩ	**3**	13		5	13		**8**	13		V/μV
POWER SUPPLY REJECTION RATIO	V_S = ±3 V to ±18 V	**110**	130		**115**	130		**120**	130		dB
	T_{min} to T_{max}	110	130		**115**	130		**120**	130		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth			0.5	0.9		0.5	0.9		0.5	0.9	MHz
Slew Rate			0.15	0.3		0.15	0.3		0.15	0.3	V/μs
INPUT RESISTANCE											
Differential			24	100		45	200		60	200	MΩ
Common Mode				200			300			400	GΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥10 kΩ	**13.5**	14		**13.5**	14		**13.5**	14		±V
	R_{LOAD}≥2 kΩ	**12.5**	13.0		**12.5**	13.0		**12.5**	13.0		±V
	R_{LOAD}≥1 kΩ	**12.0**	12.5		**12.0**	12.5		**12.0**	12.5		±V
	R_{LOAD}≥2 kΩ T_{min} to T_{max}	12.0	13.0		**12.0**	13.0		**12.0**	13.0		±V
OPEN-LOOP OUTPUT RESISTANCE			60			60			60		Ω
POWER SUPPLY											
Current, Quiescent			2.5	**3**		2.5	**3**		2.5	**3**	mA
Power Consumption, No Load	V_S = ±15 V		75	**90**		75	**90**		75	**90**	mW
	V_S =±3 V		7.5	**9.0**		7.5	**9.0**		7.5	**9.0**	mW
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial	0 to +70°C	AD707JN, AD707JR			AD707KN, AD707KR[1]						
Industrial	−40°C to +85°C	AD707AQ, AD707AH AD707AR			AD707BQ, AD707BH			AD707CQ, AD707CH			
Military	−55°C to +125°C				AD707SQ, AD707SH			AD707TQ, AD707TH			
PACKAGE OPTIONS[2]											
Plastic (N-8)		AD707JN			AD707KN						
Cerdip (Q-8)		AD707AQ			AD707BQ/SQ			AD707CQ/TQ			
TO-99 (H-08A)		AD707AH			AD707BH/SH			AD707CH/TH			
SOIC (R-8)		AD707JR, AD707AR			AD707KR						
Tape and Reel		AD707JR-Reel			AD707KR-Reel						
Chips		AD707J-Chips			AD707S-Chips						

NOTES
[1]AD707KR parts are production tested at +25°C only. All T_{min} to T_{max} specifications are guaranteed but not 100% tested for this grade.
[2]See Section 20 for package outline information.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications are subject to change without notice.

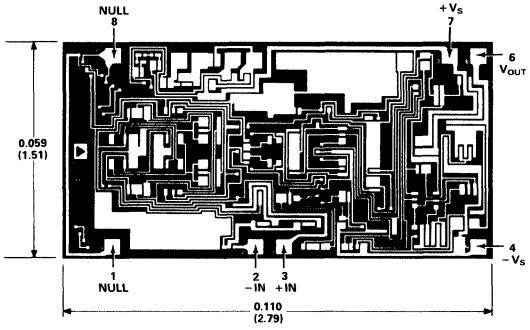
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range Q, H . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-pin plastic package: θ_{JA} = 165°C/watt; 8-pin cerdip package: θ_{JA} = 110°C/watt; 8-pin small outline package: θ_{JA} = 155°C/watt; 8-pin header package: 200°C/watt.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm)
Contact factory for latest dimensions.



Typical Characteristics

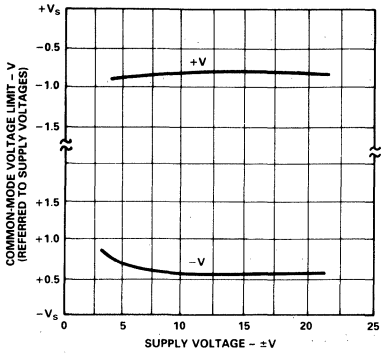


Figure 1. Input Common-Mode Range vs. Supply Voltage

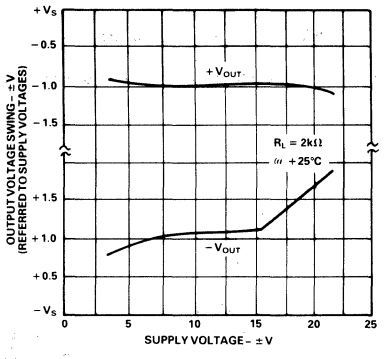


Figure 2. Output Voltage Swing vs. Supply Voltage

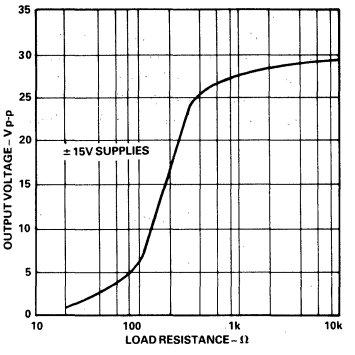


Figure 3. Output Voltage Swing vs. Load Resistance

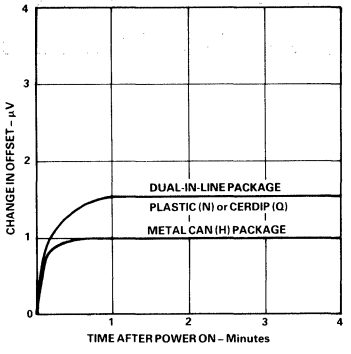


Figure 4. Offset Voltage Warm-Up Drift

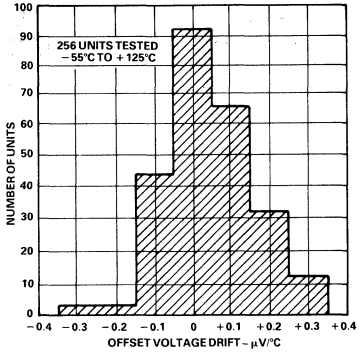


Figure 5. Typical Distribution of Offset Voltage Drift

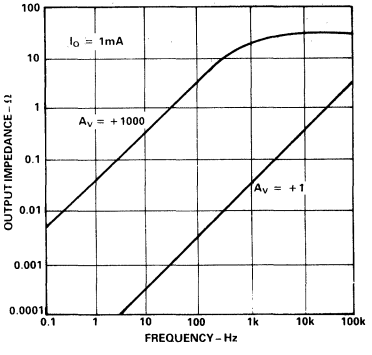


Figure 6. Output Impedance vs. Frequency

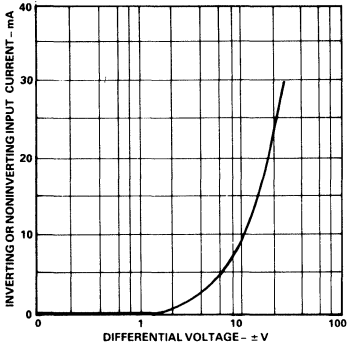


Figure 7. Input Current vs. Differential Input Voltage

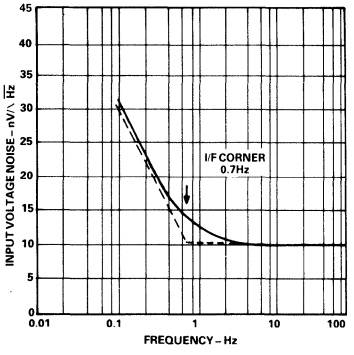


Figure 8. Input Noise Spectral Density

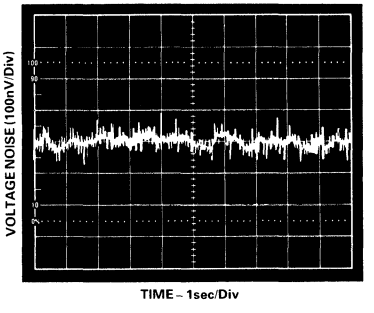


Figure 9. 0.1 Hz to 10 Hz Voltage Noise

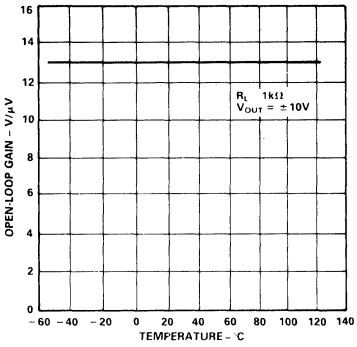


Figure 10. Open-Loop Gain vs. Temperature

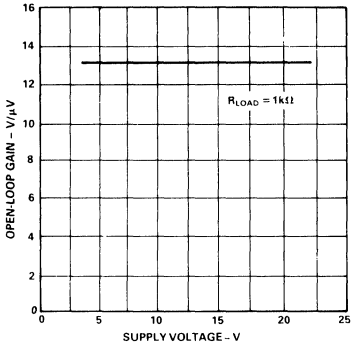


Figure 11. Open-Loop Gain vs. Supply Voltage

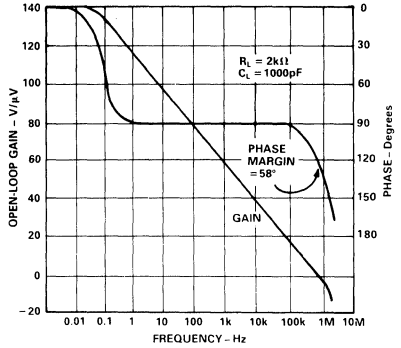


Figure 12. Open-Loop Gain and Phase vs. Frequency

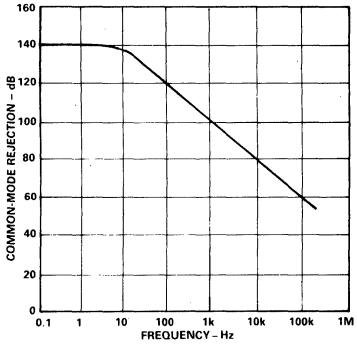


Figure 13. Common-Mode Rejection vs. Frequency

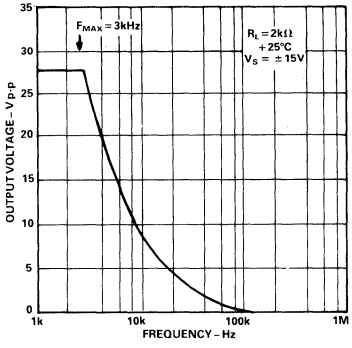


Figure 14. Large Signal Frequency Response

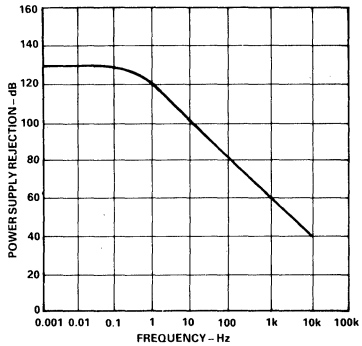


Figure 15. Power Supply Rejection vs. Frequency

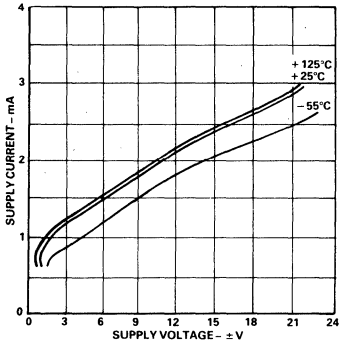


Figure 16. Supply Current vs. Supply Voltage

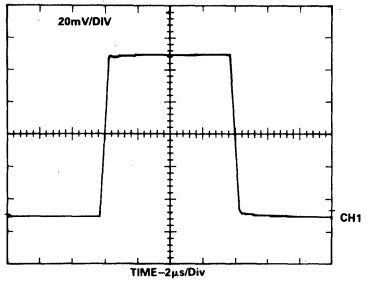


Figure 17. Small Signal Transient Response;
$A_V = +1$, $R_L = 2\ k\Omega$, $C_L = 50\ pF$

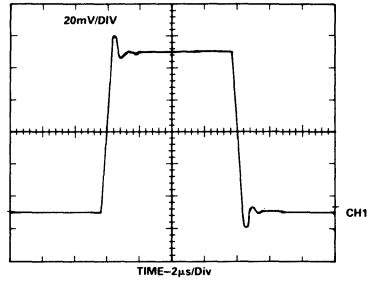


Figure 18. Small Signal Transient Response;
$A_V = +1$, $R_L = 2\ k\Omega$, $C_L = 1000\ pF$

OFFSET NULLING

The input offset voltage of the AD707 is the lowest available in a bipolar op amp, but if additional nulling is required, the circuit shown in Figure 19 offers a null range of 200 μV. For wider null capability, omit R1 and substitute a 20 kΩ potentiometer for R2.

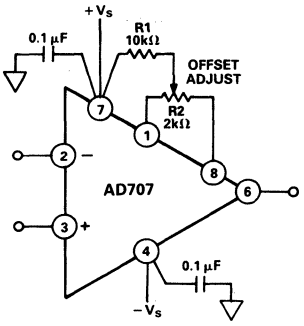


Figure 19. External Offset Nulling and Power Supply Bypassing

GAIN LINEARITY INTO A 1 kΩ LOAD

The gain and gain linearity of the AD707 are the highest available among monolithic bipolar amplifiers. Unlike other dc precision amplifiers, the AD707 shows no degradation in gain or gain linearity when driving loads in excess of 1 kΩ over a ±10 V output swing. This means high gain accuracy is assured over the output range. Figure 20 shows the gain of the AD707, AD OP-07, and the OP-77 amplifiers when driving a 1 kΩ load.

The AD707 will drive 10 mA of output current with no significant effect on its gain or linearity.

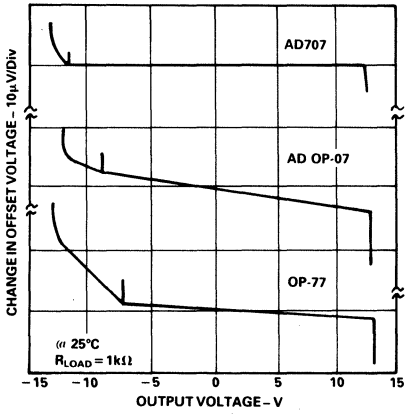


Figure 20. Gain Linearity of the AD707 vs. Other DC Precision Op Amps

OPERATION WITH A GAIN OF 100

Demonstrating the outstanding dc precision of the AD707 in practical applications, Table I shows an error budget calculation for the gain of −100 configuration shown in Figure 21.

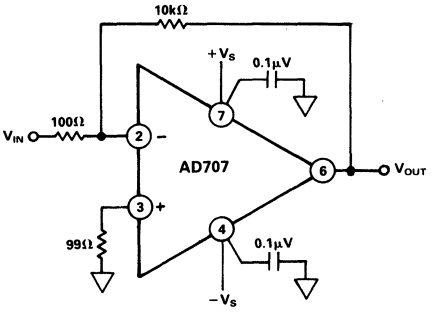


Figure 21. Gain of −100 Configuration

Error Source	Maximum Error Contribution A_V = 100 (C Grade) (Full Scale: V_{OUT} = 10 V, V_{IN} = 100 mV)	
V_{OS}	15 μV/100 mV	= 150 ppm
I_{OS}	(100 Ω)(1 nA)/100 mV	= 1 ppm
Gain (2 kΩ Load)	(100 V/8 × 10^6)100 mV	= 13 ppm
Noise	0.35 μV/100 mV	= 4 ppm
V_{OS} Drift	(0.1 V/°C)/100 mV	= 1 ppm/°C
		= 168 ppm
		+1 ppm/°C

Total Unadjusted Error
- @ +25°C = 168 ppm>12 Bits
- @ −55°C to +125°C = 268 ppm>11 Bits

With Offset Calibrated Out
- @ +25°C = 17 ppm>15 Bits
- @ −55°C to +125°C = 117 ppm>13 Bits

Table I. Error Budget

Although the initial offset voltage of the AD707 is very low, it is nonetheless the major contributor to system error. In cases requiring additional accuracy, the circuit shown in Figure 19 can be used to null out the initial offset voltage. This method will also cancel the effects of input offset current error. With the offsets nulled, the AD707C will add less than 17 ppm of error.

This error budget assumes no error in the resistor ratio and no errors from power supply variation (the 120 dB minimum PSRR of the AD707C makes this a good assumption). The external resistors can cause gain error from mismatch and drift over temperature.

18-BIT SETTLING TIME

Figure 22 shows the AD707 settling to within 80 μV of its final value for a 20 V output step in less than 100 μs (in the test configuration shown in Figure 23). To achieve settling to 18 bits, any amplifier specified to have a gain of 4 V/μV would appear to be good enough, however, this is not the case. In order to truly achieve 18-bit accuracy, the gain linearity must be better than 4 ppm.

The gain nonlinearity of the AD707 does not contribute to the error, and the gain itself only contributes 0.1 ppm. The gain error, along with the V_{OS} and V_{OS} drift errors do not comprise 1 LSB of error in a 18-bit system over the military temperature range. If calibration is used to null offset errors, the AD707 resolves up to 20 bits at +25°C.

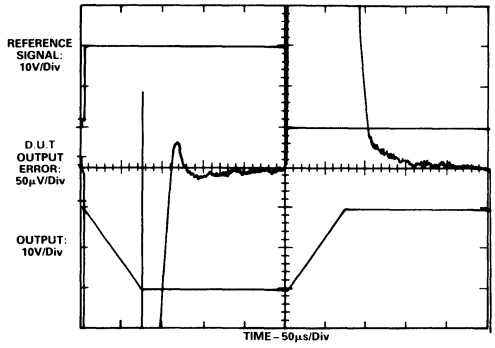


Figure 22. 18-Bit Settling

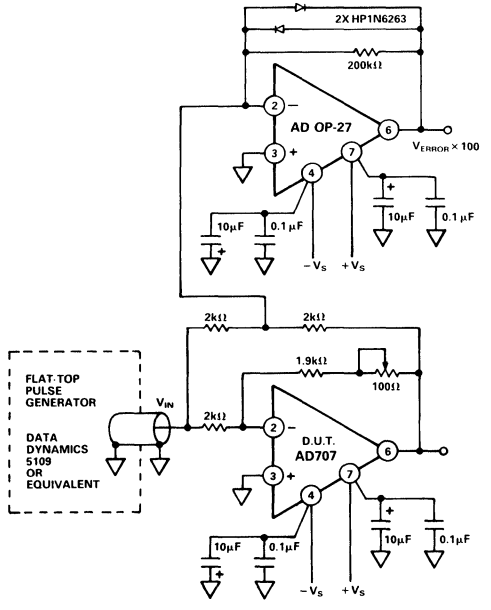


Figure 23. Op Amp Settling Time Test Circuit

140 dB CMRR INSTRUMENTATION AMPLIFIER

The extremely tight dc specifications of the AD707 enable the designer to build very high performance, high gain instrumentation amplifiers without having to select matched op amps for the crucial first stage. For the second stage, the lowest grade AD707 is ideally suited. The CMRR is typically the same as the high grade parts, but does not exact a premium for drift performance (which is less critical in the second stage). Figure 24 shows an example of the classic instrumentation amp. Figure 25 shows that the circuit has at least 140 dB of common-mode rejection for a ±10 V common-mode input at a gain of 1001 (R_G = 20 Ω).

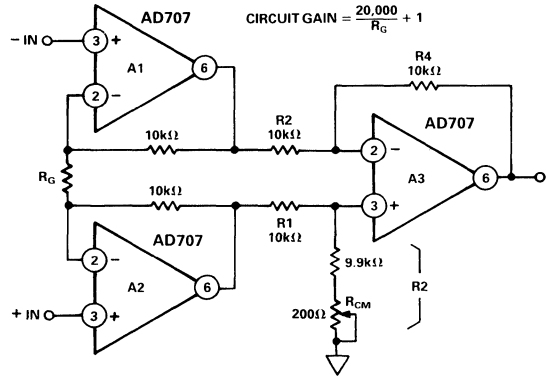


Figure 24. A 3 Op Amp Instrumentation Amplifier

High CMRR is obtained by first adjusting R_{CM} until the output does not change as the input is swept through the full common-mode range. The value of R_G should then be selected to achieve the desired gain. Matched resistors should be used for the output stage so that R_{CM} is as small as possible. The smaller the value of R_{CM}, the lower the noise introduced by potentiometer wiper vibrations. To maintain the CMRR at 140 dB over a 20°C range, the resistor ratios in the output stage, R1/R2 and R3/R4, must track each other better than 10 ppm/°C.

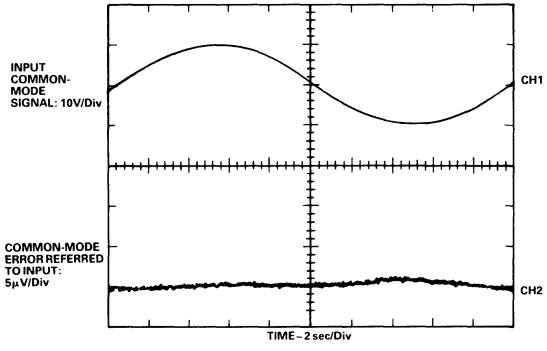


Figure 25. Instrumentation Amplifier Common-Mode Rejection

PRECISION CURRENT TRANSMITTER

The AD707's excellent dc performance, especially the low offset voltage, low offset voltage drift and high CMRR, makes it possible to make a high precision voltage-controlled current transmitter using a variation of the Howland Current Source circuit (Figure 26). This circuit provides a bidirectional load current which is derived from a differential input voltage.

The performance and accuracy of this circuit will depend almost entirely on the tolerance and selection of the resistors. The scale resistor (R_{SCALE}) and the four feedback resistors directly affect the accuracy of the load current and should be chosen carefully or trimmed.

As an example of the accuracy achievable, assume I_L must be 10 mA, and the available V_{IN} is only 10 mV.

R_{SCALE} = 10 mV/10 mA = 1 Ω

I_{ERROR} due to the AD707C:

Maximum I_{ERROR} = $2(V_{OS})/R_{SCALE}$ + $2(V_{OS}$ Drift$)/R_{SCALE}$ + I_{OS} (100 k/R_{SCALE})

= 2 (15 μV)/1 Ω + 2 (0.1 μV/°C)/1 Ω + 1 nA (100 k)/1 Ω (1.5 nA @ 125°C)

= 30 μA + 0.2 μA/°C + 100 μA (150 μA @ 125°C)

= 130 μA/10 mA = 1.3% @ 25°C

= 120 μA/10 mA = 2.00.25% @ 125°C

Low drift, high accuracy resistors are required to achieve high precision.

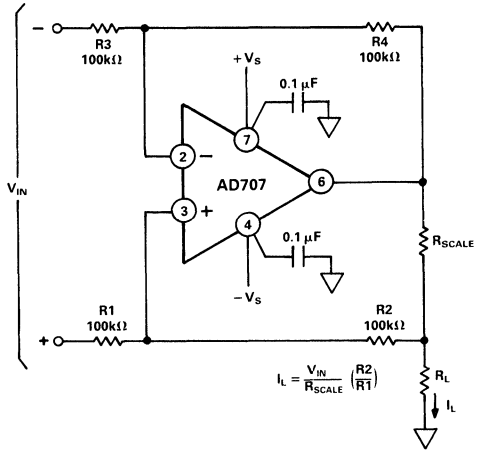


Figure 26. Precision Current Source/Sink

Ultralow Offset Voltage Dual Op Amp

AD708

FEATURES

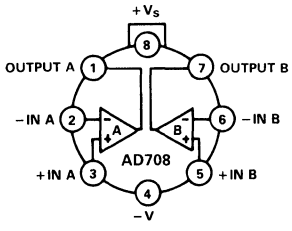
Very High dc Precision
- **30μV max Offset Voltage**
- **0.3μV/°C max Offset Voltage Drift**
- **0.35μV p-p max Voltage Noise (0.1 to 10Hz)**
- **5 Million V/V min Open Loop Gain**
- **130dB min CMRR**
- **120dB min PSRR**

Matching Characteristics
- **30μV max Offset Voltage Match**
- **0.3μV/°C max Offset Voltage Drift Match**
- **130dB min CMRR Match**

Single: AD707

Available in 8-Pin Plastic Mini-DIP, Hermetic Cerdip and TO-99 Metal Can Packages. Chips and /883B Parts Available.

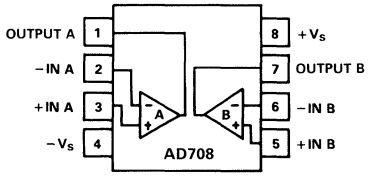
AD708 CONNECTION DIAGRAMS



TO-99 (H) Package

TOP VIEW

NOTE: PIN 4 CONNECTED TO CASE



Plastic (N), and Cerdip (Q) Packages

TOP VIEW

PRODUCT DESCRIPTION

The AD708 is a very high precision, dual monolithic operational amplifier. Each amplifier individually offers excellent dc precision with the best available max offset voltage and offset voltage drift of any dual bipolar op amp. In addition, the matching specifications are the best available in any dual op amp.

The AD708 sets a new standard for dual precision op amps by providing 5V/μV min open loop gain and guaranteed max input voltage noise of 350nV p-p (0.1 to 10Hz). All dc specifications show excellent stability over temperature, with offset voltage drift typically 0.1μV/°C and input bias current drift of 25pA/°C max. Both CMRR (130dB min) and PSRR (120dB min) are an order of magnitude improved over any available single monolithic op amp except the AD707.

The AD708 is available in four performance grades. The AD708J is rated over the commercial temperature range of 0 to +70°C and is available in a plastic mini-DIP package. The AD708A and AD708B are rated over the industrial temperature range of −40°C to +85°C and are available in a cerdip and TO-99 package. The AD708S is rated over the military temperature range of −55°C to +125°C and is available in cerdip and TO-99 packages. Military versions are available processed to MIL-STD-883B, Rev. C.

APPLICATION HIGHLIGHTS

1. The combination of outstanding matching and individual specifications makes the AD708 ideal for constructing high gain, precision instrumentation amplifiers.
2. The low offset voltage drift and noise of the AD708 allows the designer to amplify very small signals without sacrificing overall system performance.
3. The AD708's 10V/μV typical open loop gain and 140dB common-mode rejection make it ideal for precision applications.
4. Unmounted dice are available for hybrid circuit applications.
5. The AD708 is an improved replacement for the OP-207, OP-200 and the LT1002.

SPECIFICATIONS (@+25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD708J/A Min	AD708J/A Typ	AD708J/A Max	AD708B Min	AD708B Typ	AD708B Max	AD708S Min	AD708S Typ	AD708S Max	Units
INPUT OFFSET VOLTAGE[1]			30	**100**		5	**50**		5	**30**	μV
	T_{min}–T_{max}		50	150		15	65		15	**50**	μV
Drift			0.3	1.0		0.1	0.4		0.1	**0.3**	μV/°C
Long Term Stability			0.3			0.3			0.3		μV/month
INPUT BIAS CURRENT			1.0	**2.5**		0.5	**1.0**		0.5	**1**	nA
	T_{min}–T_{max}		2.0	4.0		1.0	2.0		1.0	**4**	nA
Average Drift			15	40		10	25		10	30	pA/°C
OFFSET CURRENT	V_{CM}=0V		0.5	**2.0**		0.1	**1.0**		0.1	**1**	nA
	T_{min}–T_{max}		2.0	4.0		0.2	1.5		0.2	**1.5**	nA
Average Drift			2	60		1	25		1	25	pA/°C
MATCHING CHARACTERISTICS[2]											
Offset Voltage				**80**			**50**			**30**	μV
	T_{min}–T_{max}			150			75			**50**	μV
Offset Voltage Drift				1.0			0.4			**0.3**	μV/°C
Input Bias Current				**4.0**			**1.0**			**1.0**	nA
	T_{min}–T_{max}			5.0			2.0			**2.0**	nA
Common-Mode Rejection		**120**	140		**130**	140		**130**	140		dB
	T_{min}–T_{max}	110			130			**130**			dB
Power Supply Rejection		**110**			**120**			**120**			dB
	T_{min}–T_{max}	110			120			**120**			dB
Channel Separation		135			140			140			dB
INPUT VOLTAGE NOISE	0.1Hz to 10Hz		0.23	0.6		0.23	0.6		0.23	**0.35**	μV p-p
	f=10Hz		10.3	18		10.3	12		10.3	12	nV/$\sqrt{Hz}$
	f=100Hz		10.0	13.0		10.0	11.0		10.0	11	nV/$\sqrt{Hz}$
	f=1kHz		9.6	11.0		9.6	11.0		9.6	11	nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	0.1Hz to 10Hz		14	35		14	35		14	35	pA p-p
	f=10Hz		0.32	0.9		0.32	0.8		0.32	0.8	pA/$\sqrt{Hz}$
	f=100Hz		0.14	0.27		0.14	0.23		0.14	0.23	pA/$\sqrt{Hz}$
	f=1kHz		0.12	0.18		0.12	0.17		0.12	0.17	pA/$\sqrt{Hz}$
COMMON-MODE REJECTION RATIO	V_{CM}=±13V	**120**	140		**130**	140		**130**	140		dB
	T_{min}–T_{max}	120	140		130	140		**130**	140		dB
OPEN LOOP GAIN	V_O=±10V										
	R_{LOAD}≥2kΩ	**3**	10		5	10		5	10		V/μV
	T_{min}–T_{max}	3	10		5	10		**4**	7		V/μV
POWER SUPPLY REJECTION RATIO	V_S=±3V to ±18V	**110**	130		**120**	130		**120**	130		dB
	T_{min}–T_{max}	110	130		120	130		**120**	130		dB
FREQUENCY RESPONSE											
Closed Loop Bandwidth		0.5	0.9		0.5	0.9		0.5	0.9		MHz
Slew Rate		0.15	0.3		0.15	0.3		0.15	0.3		V/μs
INPUT RESISTANCE											
Differential			60			200			200		MΩ
Common Mode			200			400			400		GΩ
OUTPUT VOLTAGE	R_{LOAD}≥10kΩ	**13.5**	14		**13.5**	14		**13.5**	14		±V
	R_{LOAD}≥2kΩ	**12.5**	13.0		**12.5**	13.0		**12.5**	13		±V
	R_{LOAD}≥1kΩ	**12.0**	12.5		**12.0**	12.5		**12.0**	12.5		±V
	R_{LOAD}≥2kΩ T_{min}–T_{max}	12.0	13.0		12.0	13.0		**12.0**	13		±V
OPEN LOOP OUTPUT RESISTANCE			60			60			60		Ω

Model	Conditions	AD708J/A Min	AD708J/A Typ	AD708J/A Max	AD708B Min	AD708B Typ	AD708B Max	AD708S Min	AD708S Typ	AD708S Max	Units
POWER SUPPLY											
Current, Quiescent			4.5	**5.5**		4.5	5.5		4.5	5.5	mA
Power Consumption	V_S=±15V										
	No Load		135	**165**		135	**165**		135	**165**	mW
	V_S=±3V		12	**18**		12	**18**		12	**18**	mW
Operating Range		±3		±18	±3		±18	±3		±18	V
PACKAGE OPTIONS[3]											
Plastic (N-8)			AD708JN								
Cerdip (Q-8)			AD708AQ			AD708BQ			AD708SQ		
TO-99 (H-08A)			AD708AH			AD708BH			AD708SH		
J Grade Chips Available			AD708J Chips								

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A=25°C
[2]Matching is defined as the difference between parameters of the two amplifiers.
[3]See Section 20 for package outline information.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

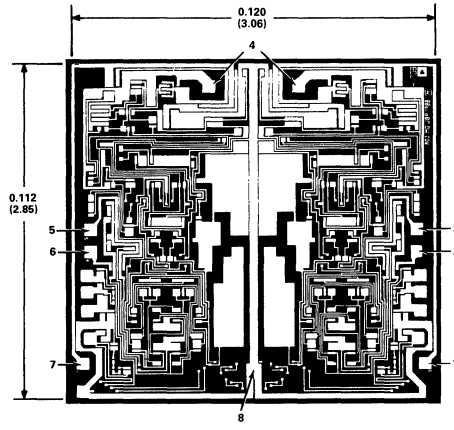
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22V
Internal Power Dissipation[2] 500mW
Input Voltage[3] . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range Q, H . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics
8-Pin Plastic Package: θ_{JA} = 165°C/Watt
8-Pin Cerdip Package: θ_{JC} = 22°C/Watt, θ_{JA} = 110°C/Watt
8-Pin Metal Can Package: θ_{JC} = 65°C/Watt, θ_{JA} = 150°C/Watt
[3]For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



Typical Characteristics ($V_S = \pm 15V$ and $T_A = +25°C$ unless otherwise noted)

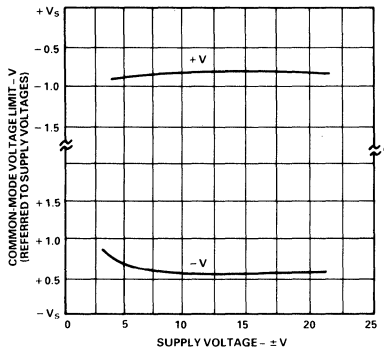


Figure 1. Input Common-Mode Range vs. Supply Voltage

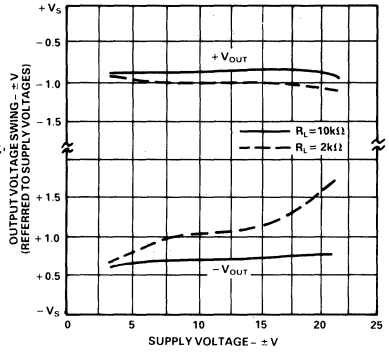


Figure 2. Output Voltage Swing vs. Supply Voltage

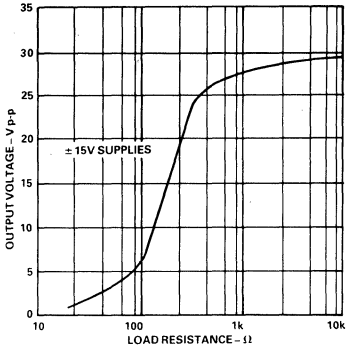


Figure 3. Output Voltage Swing vs. Load Resistance

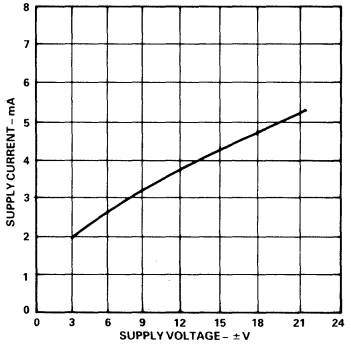


Figure 4. Supply Current vs. Supply Voltage

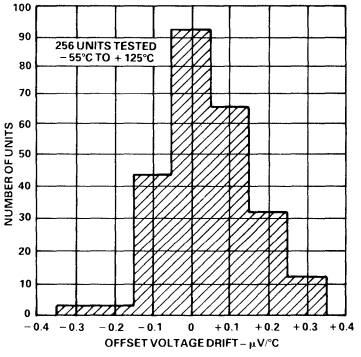


Figure 5. Typical Distribution of Offset Voltage Drift

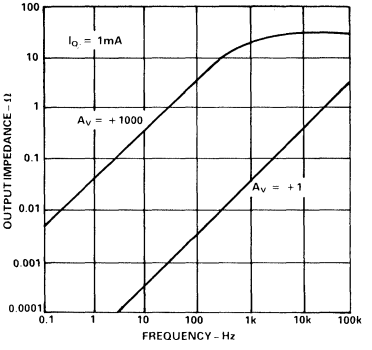


Figure 6. Output Impedance vs. Frequency

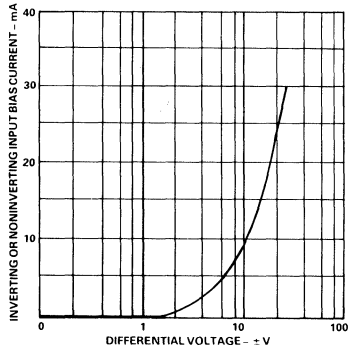


Figure 7. Input Bias Current vs. Differential Input Voltage

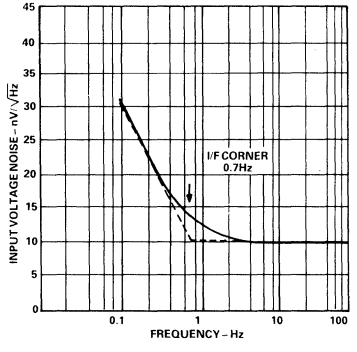


Figure 8. Input Noise Spectral Density

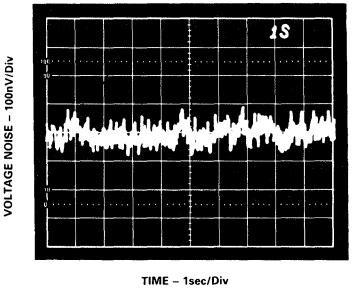


Figure 9. 0.1Hz to 10Hz Voltage Noise

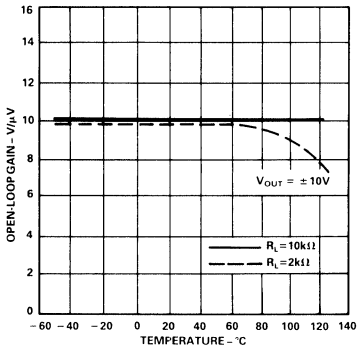


Figure 10. Open-Loop Gain vs. Temperature

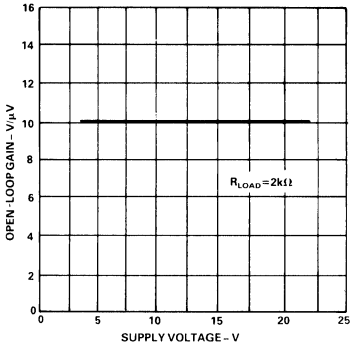


Figure 11. Open-Loop Gain vs. Supply Voltage

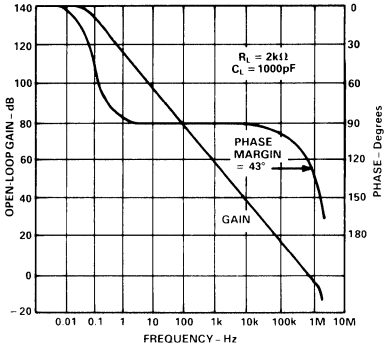


Figure 12. Open-Loop Gain and Phase vs. Frequency

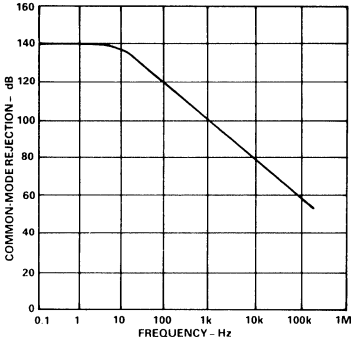


Figure 13. Common-Mode Rejection vs. Frequency

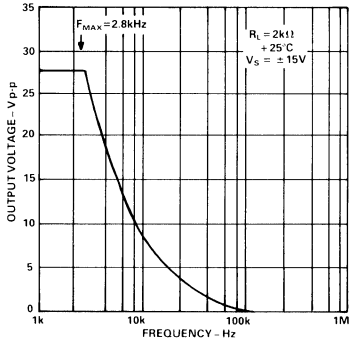


Figure 14. Large Signal Frequency Response

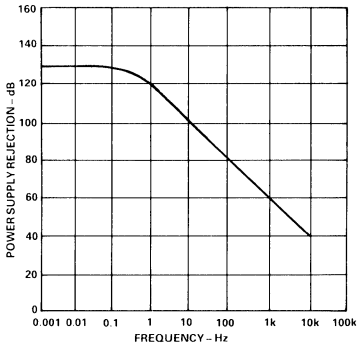


Figure 15. Power Supply Rejection vs. Frequency

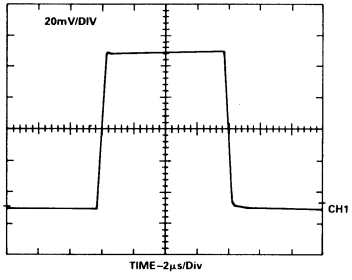


Figure 16. Small Signal Transient Response;
A_V = +1, R_L = 2kΩ, C_L = 50pF

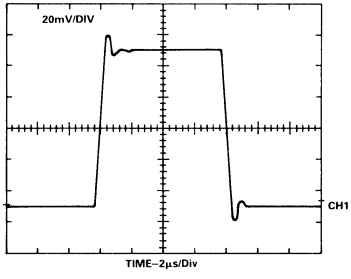


Figure 17. Small Signal Transient Response;
A_V = +1, R_L = 2kΩ, C_L = 1000pF

Matching Characteristics

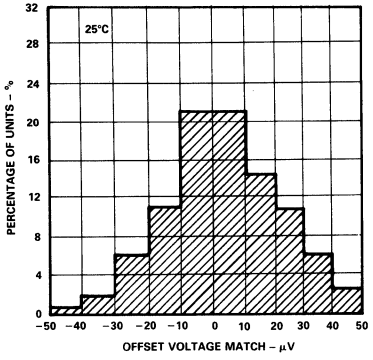


Figure 18. Typical Distribution of Offset Voltage Match

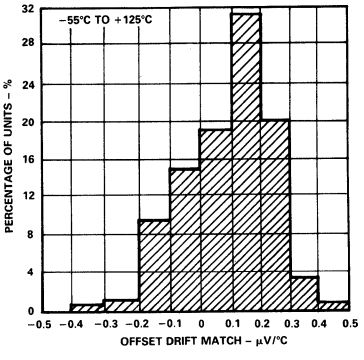


Figure 19. Typical Distribution of Offset Voltage Drift Match

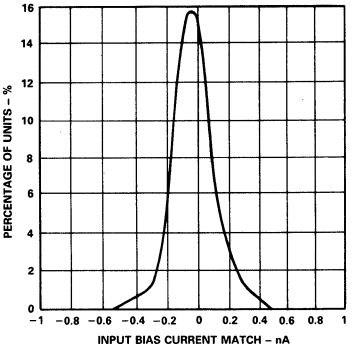


Figure 20. Typical Distribution of Input Bias Current Match

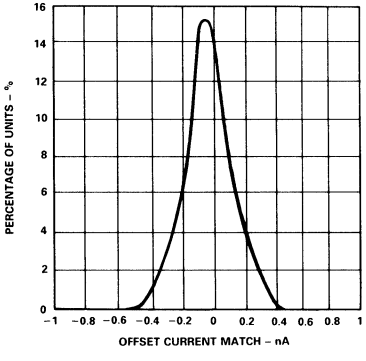


Figure 21. Typical Distribution of Input Offset Current Match

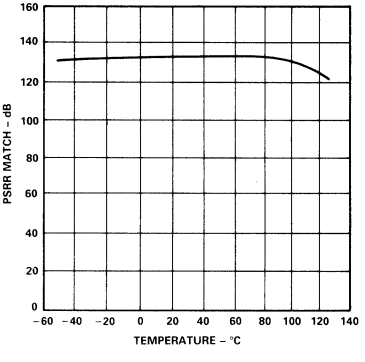


Figure 22. PSRR Match vs. Temperature

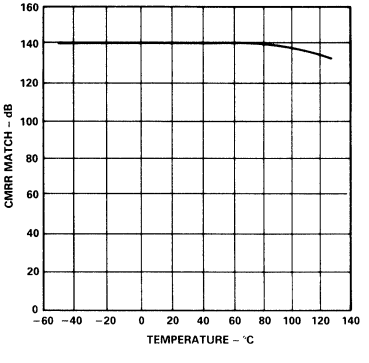


Figure 23. CMRR Match vs. Temperature

Crosstalk from Thermal Effects of Power Dissipation

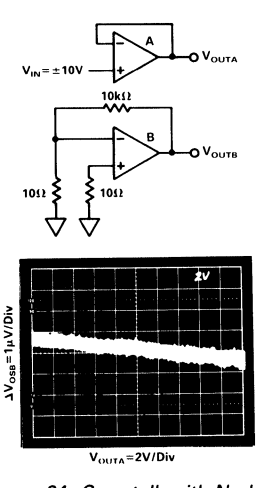


Figure 24. Crosstalk with No Load

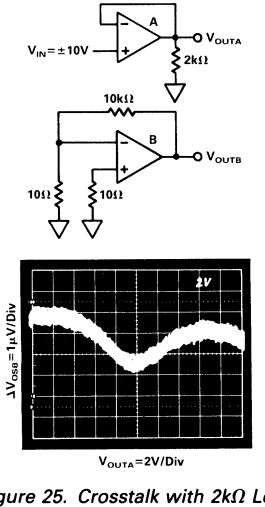


Figure 25. Crosstalk with 2kΩ Load

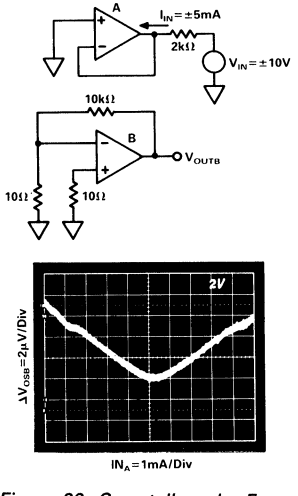


Figure 26. Crosstalk under Forced Source and Sink Conditions

CROSSTALK PERFORMANCE OF THE AD708

The AD708 exhibits very low crosstalk as shown in Figures 24, 25 and 26. Figure 24 shows the offset voltage induced in side B of the AD708 when side A's output is moving slowly (0.2Hz) from −10V to +10V under no load. This is the least stressful situation to the part since the overall power in the chip does not change; only the location of the power in the output devices changes. Figure 25 shows side B's input offset voltage change when side A is driving a 2kΩ load. Here the power is being changed in the chip with the maximum power change occurring at ±7.5V. Figure 26 shows crosstalk under the most severe conditions. Side A is connected as a follower with 0V input, and is now forced to sink and source ±5mA of output current (Power = (30V)(5mA) = 150mW). Even this large change in power causes only an 8μV (linear) change in side B's input offset voltage.

OPERATION WITH A GAIN OF −100

To show the outstanding dc precision of the AD708 in real application, Table I shows an error budget calculation for a gain of −100 configuration shown in Figure 27.

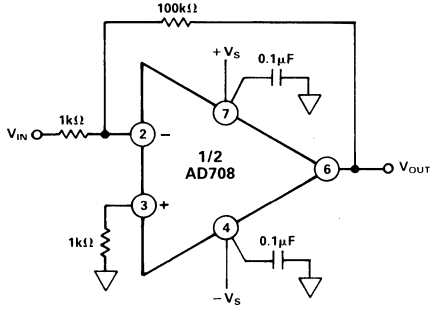


Figure 27. Gain of −100 Configuration

Error Sources	Maximum Error Contribution $A_V = 100$ (S Grade) (Full Scale: $V_{OUT} = 10V$, $V_{IN} = 100mV$)	
V_{OS}	30μV/100mV	= 300ppm
I_{OS}	(100kΩ)(1nA)/10V	= 10ppm
Gain (2kΩ load)	(10V/(5*10⁶))/100mV	= 20ppm
Noise	0.35μV/100mV	= 4ppm
V_{OS} Drift	(0.3μV/°C)/100mV	= 3ppm/°C
		= 334ppm
		+ 3ppm/°C
Total Unadjusted Error	@ 25°C	= 334ppm>11 Bits
	−55°C to +125°C	= 634ppm>10 Bits
With Offset Calibrated Out	@ 25°C	= 34ppm>14 Bits
	−55°C to +125°C	= 334ppm>11 Bits

Table I

This error budget assumes no error in the resistor ratio and no error from power supply variation (the 120dB minimum PSRR of the AD708S makes this a good assumption). The external resistors can cause gain error from mismatch and drift over temperature.

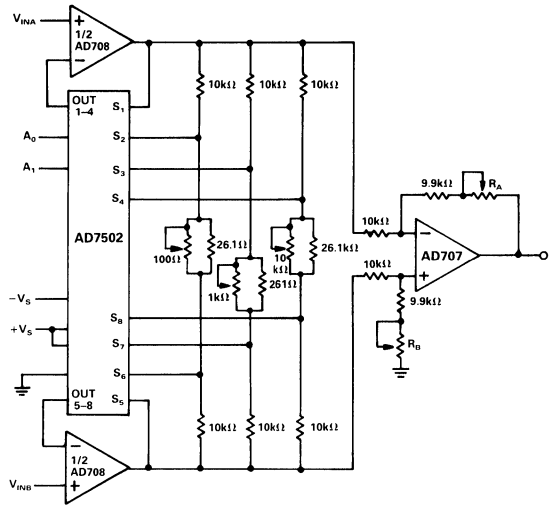


Figure 28. Precision PGA

High Precision Programmable Gain Amplifier

The three op amp programmable gain amplifier shown in Figure 28 takes advantage of the outstanding matching characteristics of the AD708 to achieve high dc precision. The gains of the circuit are controlled by the select lines, A0 and A1 of the AD7502 multiplexer, and are 1, 10, 100 and 1000 in this design.

The input stage attains very high dc precision due to the 30μV maximum offset voltage match of the AD708S and the 1nA maximum input bias current match. The accuracy is maintained over temperature because of the ultralow drift performance of the AD708. The output stage uses an AD707J and well matched resistors configured as a precision subtracter.

To achieve 0.1% gain accuracy, along with high common-mode rejection, the circuit should be trimmed as follows:

To maximize common-mode rejection:

1. Set the select lines for Gain = 1 and ground V_{INB}.
2. Apply a precision dc voltage to V_{INA} and trim R_A until $V_O = -V_{INA}$ to the required precision.
3. Next connect V_{INB} to V_{INA} and apply an input voltage equal to the full-scale common-mode expected.
4. Trim R_B until $V_O = 0V$.

To minimize gain errors:

1. Select Gain = 10 with the control lines and apply a differential input voltage.
2. Adjust the 100Ω potentiometer such that $V_O = 10V_{IN}$ (adjust V_{IN} magnitude as necessary).
3. Repeat for Gain = 100 and Gain = 1000, adjusting 1kΩ and 10kΩ potentiometers, respectively.

The design shown should allow for 0.1% gain accuracy and 0.1μV/V common-mode rejection when ±1% resistors and ±5% potentiometers are used.

BRIDGE SIGNAL CONDITIONER

The AD708 can be used in the circuit in Figure 29 to produce an accurate and inexpensive dynamic bridge conditioner. The low offset voltage match and low offset voltage drift match of the AD708 combine to achieve circuit performance better than all but the best instrumentation amplifiers. The AD708's outstanding specs: open loop gain, input offset currents and low input bias currents, do not limit circuit accuracy.

As configured, the circuit only requires a gain resistor, R_G, of suitable accuracy and a stable, accurate voltage reference. The transfer function is:

$$V_O = V_{REF}\,[\Delta R/(R+\Delta R)][R_G/R]$$

and the only significant errors due to the AD708S are:

$$V_{OS}\text{out} = (V_{OS}\text{match})(2R_G/R) = 25\text{mV}$$

$$V_{OS}\text{out}(T) = (V_{OS}\text{drift})(2R_G/R) = 0.3\text{mV/°C}$$

To achieve high accuracy, the resistor R_G should be 0.1% or better and have a low drift coefficient.

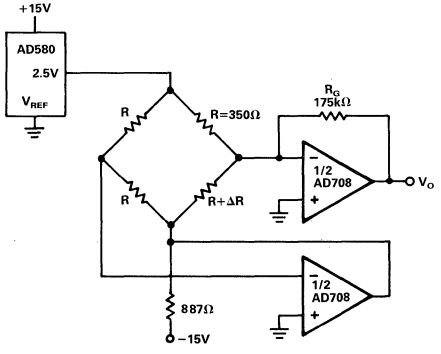


Figure 29. Bridge Signal Conditioning Circuit

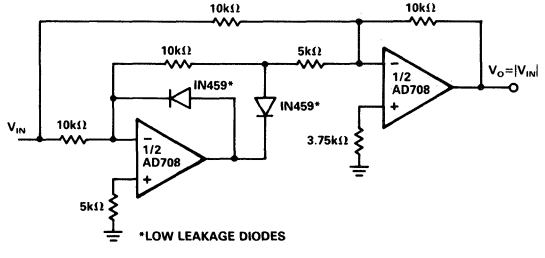


Figure 30. Precision Absolute Value Circuit

PRECISION ABSOLUTE VALUE CIRCUIT

The AD708 is ideally suited to the precision absolute value circuit shown in Figure 30. The low offset voltage match of the AD708 enables this circuit to accurately resolve the input signal. In addition, the tight offset voltage drift match maintains the resolution of the circuit over the full military temperature range. The AD708's high dc open loop gain and exceptional gain linearity allows the circuit to perform well at both large and small signal levels.

In this circuit, the only significant dc errors are due to the offset voltage of the two amplifiers, the input offset current match of the amplifiers, and the mismatch of the resistors. Errors associated with the AD708S contribute less than 0.001% error over −55°C to +125°C.

Maximum error at 25°C

$$\frac{30\mu V + (10k\Omega)(1nA)}{10V} = 40\mu V/10V = 4ppm \text{ Maximum}$$

error at +125°C or −55°C

$$\frac{50\mu V + (2nA)(10k\Omega)}{10V} = 7ppm\ @\ +125°C$$

Figure 31 shows V_{OUT} vs. V_{IN} for this circuit with a ±3mV input signal at 0.05Hz. Note that the circuit exhibits very low offset at the zero crossing. This circuit can also produce $V_{OUT} = -|V_{IN}|$ by reversing the polarity of the two diodes.

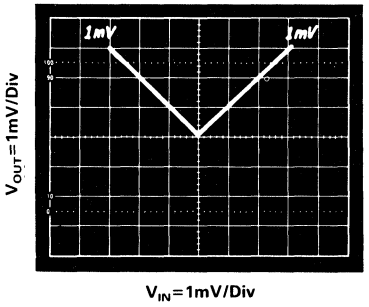


Figure 31. Absolute Value Circuit Performance (Input signal = 0.05Hz)

SELECTION OF PASSIVE COMPONENTS

To take full advantage of the high precision and low drift characteristics of the AD708, high quality passive components must be used. Discrete resistors and resistor networks with temperature coefficients of less than 10ppm/°C are available from Vishay, Caddock, PRP and others.

ANALOG DEVICES

Precision, Low Cost, High Speed BiFET Op Amp

AD711

FEATURES

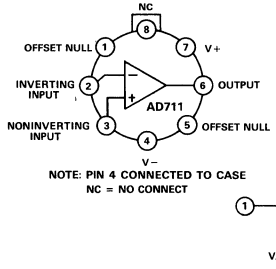
Enhanced Replacement for LF411 and TL081
AC PERFORMANCE:
- **Settles to ±0.01% in 1μs**
- **16V/μs min Slew Rate (AD711J)**
- **3MHz min Unity Gain Bandwidth (AD711J)**

DC PERFORMANCE:
- **0.25mV max Offset Voltage: (AD711C)**
- **3μV/°C max Drift: (AD711C)**
- **200V/mV min Open-Loop Gain (AD711K)**
- **4μV p–p max Noise, 0.1Hz to 10Hz (AD711C)**

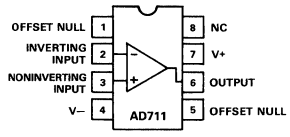
Available in Plastic Mini-DIP, Plastic SO, Hermetic Cerdip, and Hermetic Metal Can Packages
MIL-STD-883B Parts Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Surface Mount (SOIC)
Dual Version: AD712
Quad Version: AD713

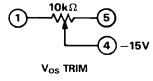
AD711 CONNECTION DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N) Plastic Small Outline (R) and Cerdip (Q) Packages





PRODUCT DESCRIPTION

The AD711 is a high speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD711 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD711 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD711 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD711J and AD711K are rated over the commercial temperature range of 0 to +70°C. The AD711A, AD711B and AD711C are rated over the industrial temperature range of −40°C to +85°C. The AD711S and AD711T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD711 is available in an 8-pin plastic mini-DIP, 8-pin small outline, cerdip, TO-99 metal can or chip form.

PRODUCT HIGHLIGHTS

1. The AD711 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.25mV max, C grade, 2mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 3μV/°C max on the AD711C.
3. Along with precision dc performance, the AD711 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD711 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1 to 10Hz (AD711C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 25pA max (AD711C) and an input offset current of 10pA max (AD711C). Both input bias current and input offset current are guaranteed in the warmed-up condition.

SPECIFICATIONS (@ + 25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD711J/A/S			AD711K/B/T			AD711C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	2/1/1		0.2	0.5		0.1	0.25	mV
T_{min} to T_{max}			3/2/2			1.0			0.45	mV
vs. Temp.		7	20/20/20		5	10		2	3	µV/°C
vs. Supply	76	95		80	100		86	110		dB
vs. Supply, T_{min} to T_{max}	76/76/76			80			86			dB
Long Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		15	50		15	50		15	25	pA
Either Input at T_{max}, V_{CM} = 0 (70°C/85°C/125°C)			1.1/3.2/51			1.1/3.2/51			1.6	nA
Either Input, V_{CM} = +10V		20	100		20	100		20	50	pA
Offset Current, V_{CM} = 0		10	25		5	25		5	10	pA
Offset Current at T_{max} (70°C/85°C/125°C)			0.57/1.6/26			0.57/1.6/26			0.65	nA
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	16	20		18	20		18	20		V/µs
Settling Time to 0.01%[3]		1	1.2		1	1.2		1	1.2	µs
Total Harmonic Distortion f = 1kHz $R_L \geq 2k\Omega$, V_O = 3V RMS		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common-Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common-Mode Voltage		+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		
Over Max Operating Range[5]	$-V_S+4V$		$+V_S-2V$	$-V_S+4V$		$+V_S-2V$	$-V_S+4V$		$+V_S-2V$	V
Common-Mode Rejection Ratio										
V_{CM} = ±10V	76	88		80	88		86	94		dB
T_{min} to T_{max}	76/76/76	84		80	84		86	90		dB
V_{CM} = ±11V	70	84		76	84		76	90		dB
T_{min} to T_{max}	70/70/70	80		74	80		74	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	4.0	µV p-p
f = 10Hz		45			45			45		nV/√Hz
f = 100Hz		22			22			22		nV/√Hz
f = 1kHz		18			18			18		nV/√Hz
f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN[6]										
V_O = ±10V, $R_L \geq 2k\Omega$	150	400		200	400		200	400		V/mV
V_O = ±10V, $R_L \geq 2k\Omega$, T_{min} to T_{max}	100/100/100			100			100			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	+13, −12.5	+13.9, −13.3		+13, −12.5	+13.9, −13.3		+13, −12.5	+13.9, −13.3		V
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	±12/±12/±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Short-Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		2.5	3.4		2.5	3.0		2.5	2.8	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD711J			AD711K					
Industrial (−40°C to +85°C)		AD711A			AD711B			AD711C		
Military (−55°C to +125°C)		AD711S			AD711T					
PACKAGE OPTIONS[7]										
Plastic (N-8)		AD711JN			AD711KN					
SOIC (R-8)		AD711JR			AD711KR					
Cerdip (Q-8)		AD711AQ, AD711SQ			AD711BQ, AD711TQ			AD711CQ		
TO-99 (H-08A)		AD711AH, AD711SH			AD711BH, AD711TH			AD711CH		
Tape and Reel		AD711JR-REEL			AD711KR-REEL					
TRANSISTOR COUNT		30			30			30		

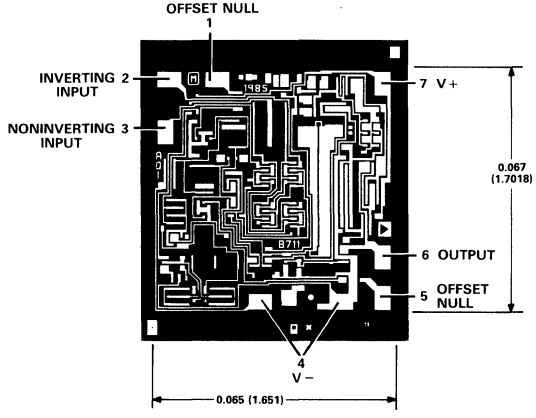
NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Refer to Figure 29.
[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[5]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.
[6]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.
[7]See Section 20 for package outline information.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

METALLIZATION PHOTOGRAPHY

Dimensions in inches and (mm).
Contact factory for latest dimensions.



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2] 500mW
Input Voltage[3] . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range Q, H . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Operating Temperature Range
AD711J/K . . . . . 0 to +70°C
AD711A/B/C . . . . . −40°C to +85°C
AD711S/T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics
8-Pin Plastic Package: θ_{JA} = 90°C/W
8-Pin Cerdip Package: θ_{JC} = 22°C/W, θ_{JA} = 110°C/W
8-Pin Metal Can Package: θ_{JC} = 65°C/W, θ_{JA} = 150°C/W
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

Typical Characteristics

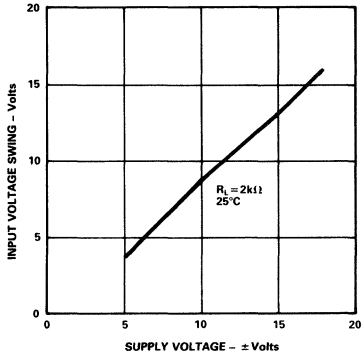


Figure 1. Input Voltage Swing vs. Supply Voltage

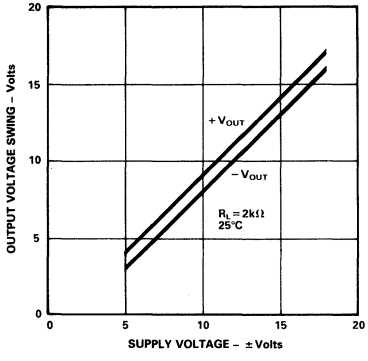


Figure 2. Output Voltage Swing vs. Supply Voltage

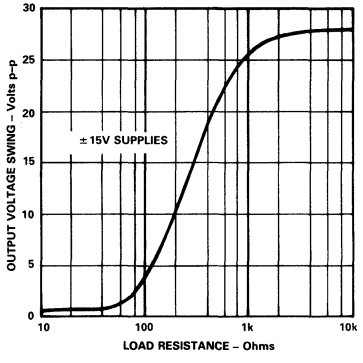


Figure 3. Output Voltage Swing vs. Load Resistance

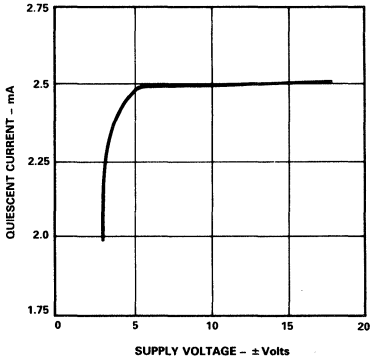


Figure 4. Quiescent Current vs. Supply Voltage

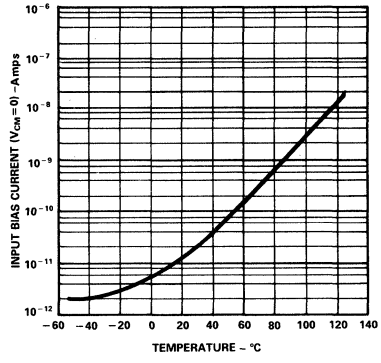


Figure 5. Input Bias Current vs. Temperature

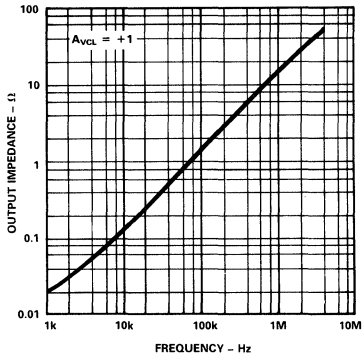


Figure 6. Output Impedance vs. Frequency

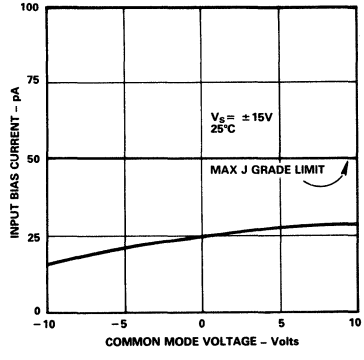


Figure 7. Input Bias Current vs. Common Mode Voltage

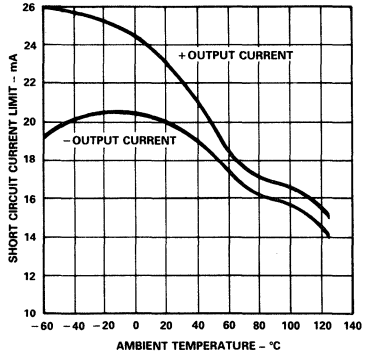


Figure 8. Short Circuit Current Limit vs. Temperature

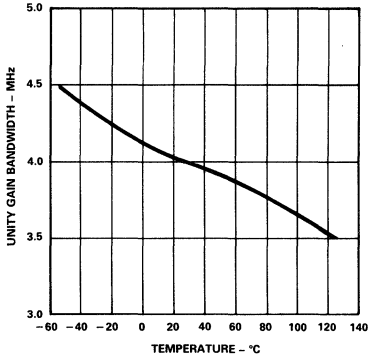


Figure 9. Unity Gain Bandwidth vs. Temperature

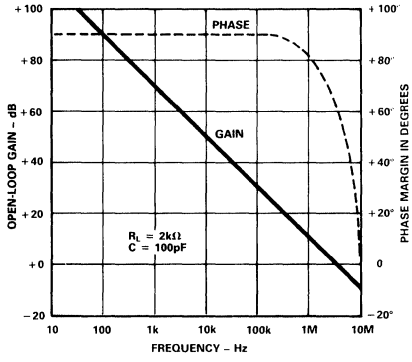


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

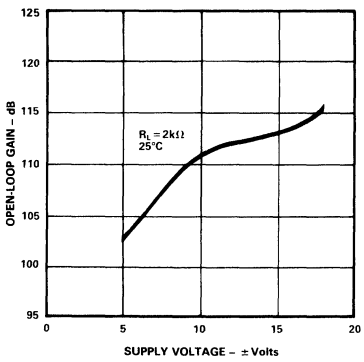


Figure 11. Open-Loop Gain vs. Supply Voltage

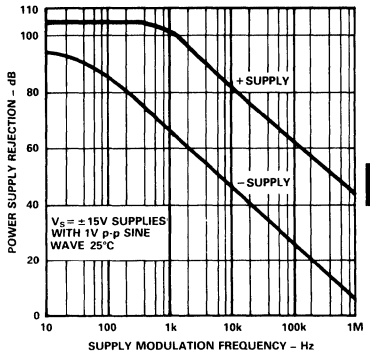


Figure 12. Power Supply Rejection vs. Frequency

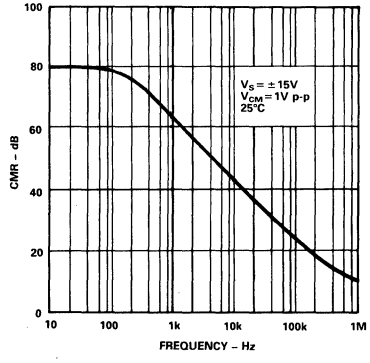


Figure 13. Common Mode Rejection vs. Frequency

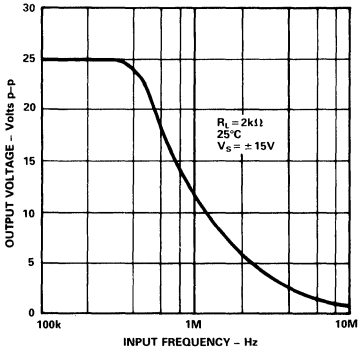


Figure 14. Large Signal Frequency Response

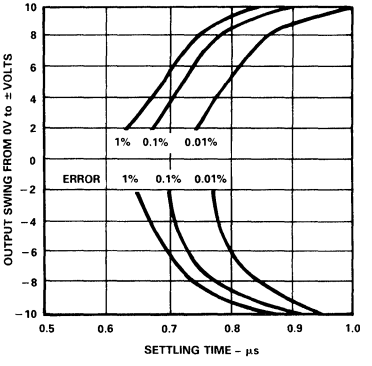


Figure 15. Output Swing and Error vs. Settling Time

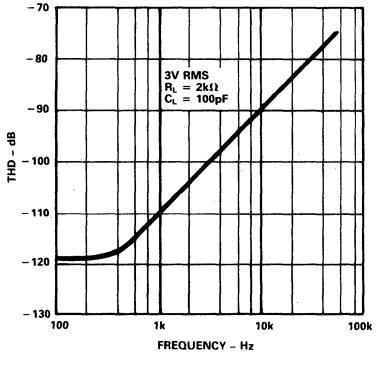


Figure 16. Total Harmonic Distortion vs. Frequency

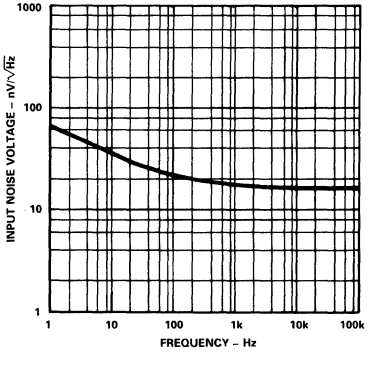


Figure 17. Input Noise Voltage Spectral Density

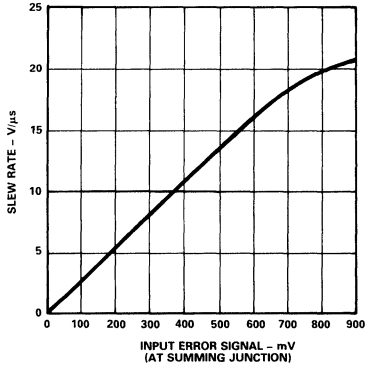


Figure 18. Slew Rate vs. Input Error Signal

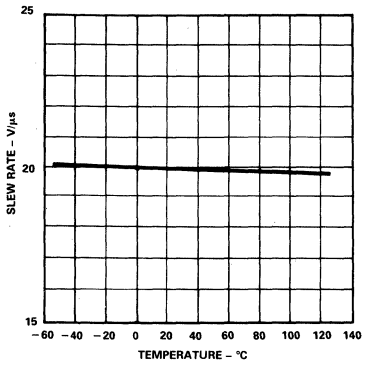


Figure 19. Slew Rate vs. Temperature

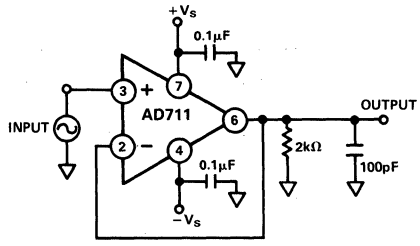


Figure 20. T.H.D. Test Circuit

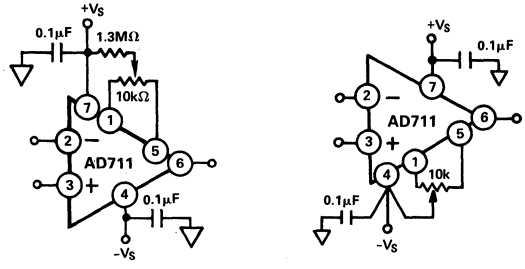


Figure 21. Offset Null Configurations

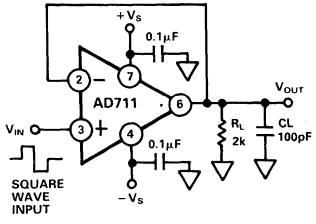


Figure 22a. Unity Gain Follower

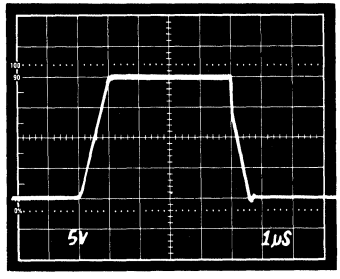


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

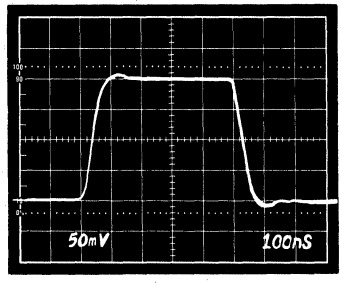


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

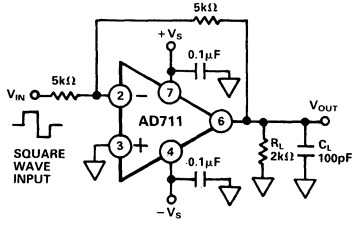


Figure 23a. Unity Gain Inverter

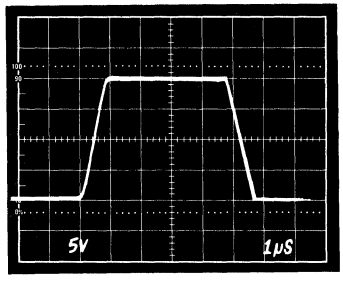


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

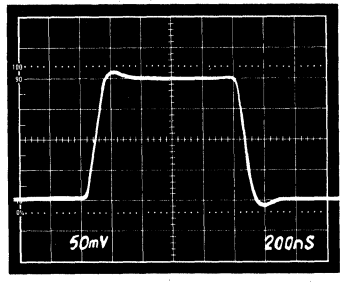


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

OPTIMIZING SETTLING TIME

Most bipolar high-speed D/A converters have curent outputs; therefore, for most applications, an external op amp is required for current-to-voltage conversion. The settling time of the converter/op amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1μs (to ±0.01% of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD711 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD711 – both photos show the worst case situation: a full-scale input transition. The DAC's 4kΩ [10kΩ‖8kΩ = 4.4kΩ] output impedance together with a 10kΩ feedback resistor produce an op amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op amp output (0 to −10V Figure 25a, −10V to 0V Figure 25b.)

Therefore, with an ideal op amp, settling to ±1/2LSB (±0.01%) requires that 375μV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD711 summing junction) must be less than 375μV. As shown in Figure 25, the total settling time for the AD711/AD565 combination is 1.2 microseconds.

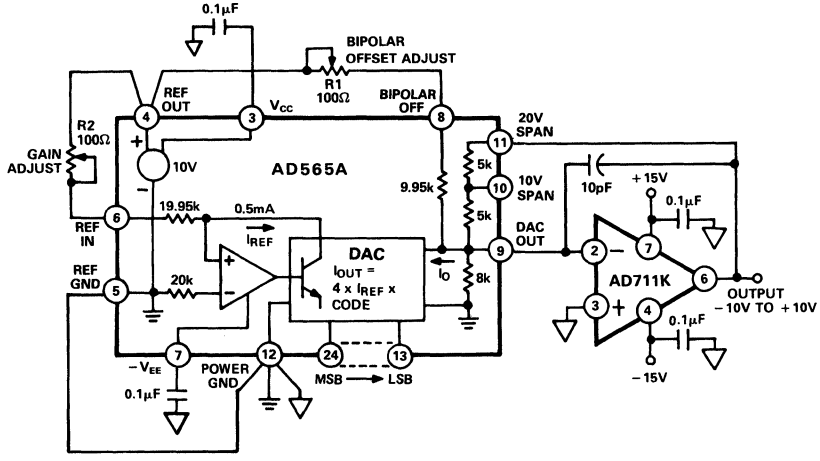
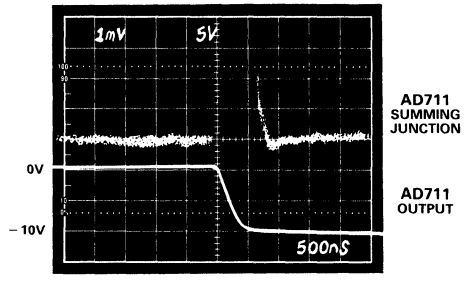
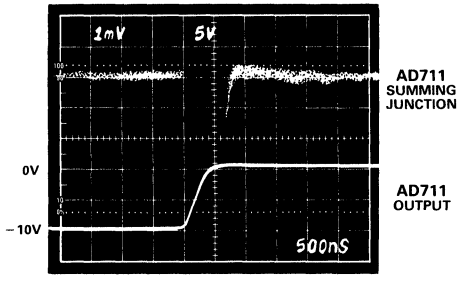


Figure 24. ±10V Voltage Output Bipolar DAC



a. (Full-Scale Negative Transition)



b. (Full-Scale Positive Transition)

Figure 25. Settling Characteristics for AD711 with AD565A

OP AMP SETTLING TIME – A MATHEMATICAL MODEL

The design of the AD711 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD711 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 250pF load capacitance when operating as a unity gain follower.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency of $\omega_O/2\pi$, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where $\frac{\omega_o}{2\pi}$ = op amp's unity gain frequency

G_N = "noise" gain of circuit $\left(1 + \frac{R}{R_O}\right)$

This equation may then be solved for C_f:

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1-G_N)}}{R\omega_o}$$

In these equations, capacitor C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op amp (since the two are in parallel).

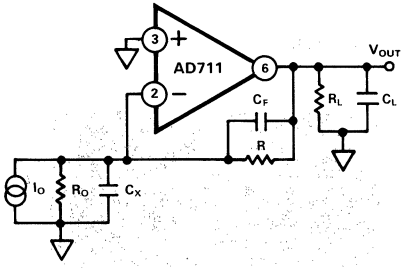


Figure 26a. Simplified Model of the AD711 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance C_X is EITHER the input capacitance of the op amp if a simple inverting op amp is being simulated OR it is the combined capacitance of the DAC output and the op amp input if the DAC buffer is being modeled.

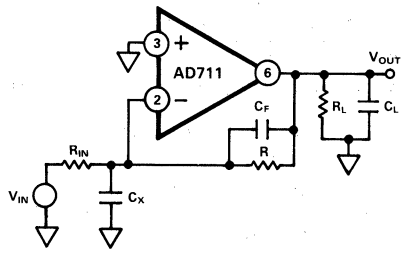


Figure 26b. Simplified Model of the AD711 Used as an Inverter

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp output. Since the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor, C_F, to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD711 with R = 4kΩ.

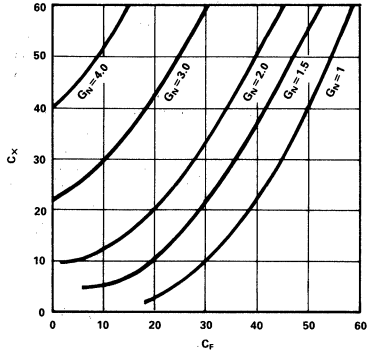


Figure 27. Value of Capacitor C_F vs. Value of C_X

The photos of Figures 28a and 28b show the dynamic response of the AD711 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high speed FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

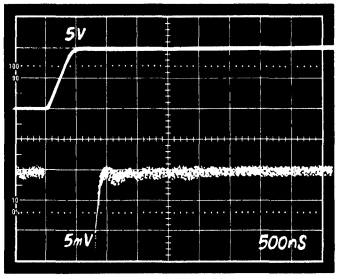


Figure 28a. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD711 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

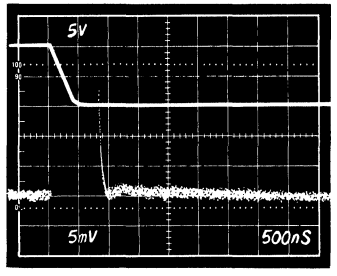


Figure 28b. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD711 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

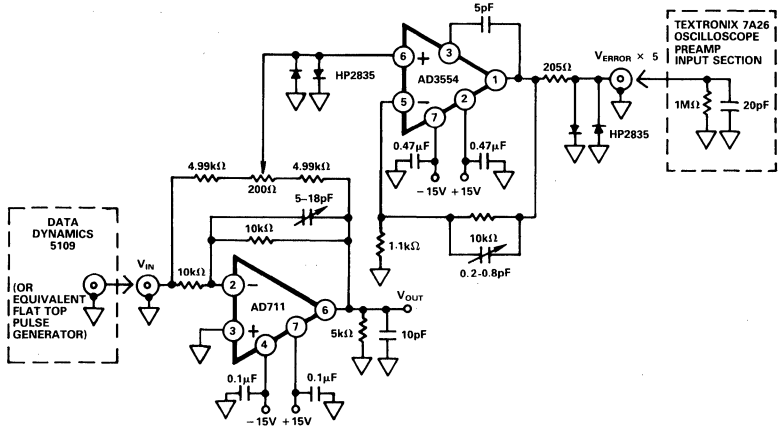
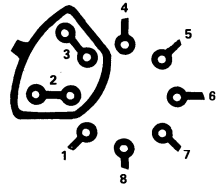


Figure 29. Settling Time Test Circuit

GUARDING

The low input bias current (15pA) and low noise characteristics of the AD711 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

TO-99 (H) Package



Plastic DIP (N) Package and Cerdip (Q) Package

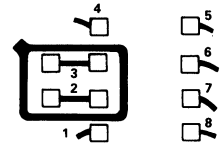


Figure 30. Board Layout for Guarding Inputs

D/A CONVERTER APPLICATIONS

The AD711 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD711K with guaranteed 500μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD711 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

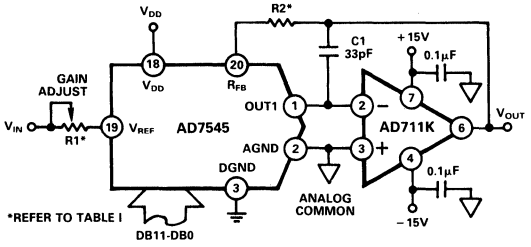


Figure 31. Unipolar Binary Operation

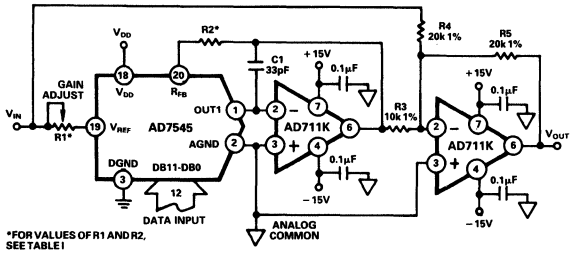


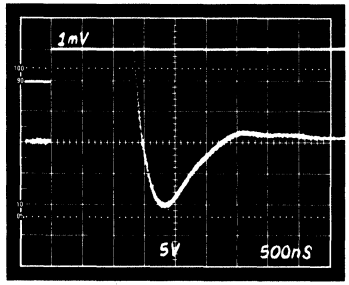
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

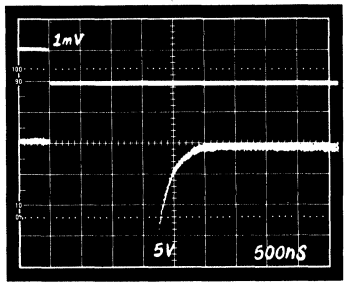
TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades of the AD7545 for V_{DD} = +5V

Figures 33a and 33b show the settling time characteristics of the AD711 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition



b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD711 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the 1/f region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD711C grade is specified at a maximum level of 4.0μV p-p, in a 0.1 to 10Hz bandwidth. Each AD711C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of 4.0μV are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD711 are sample-tested on an AQL basis to a limit of 6μV p-p, 0.1 to 10Hz.

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD711 is ideally suited to drive high speed A/D converters since it offers both wide bandwidth and high open-loop gain.

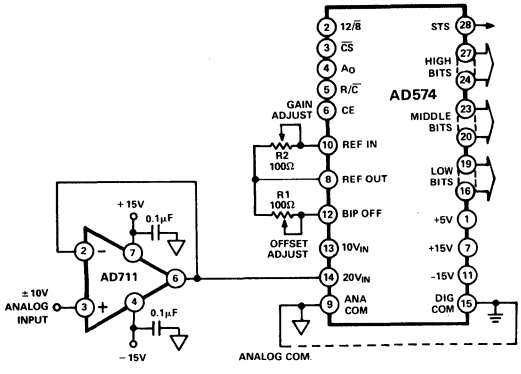
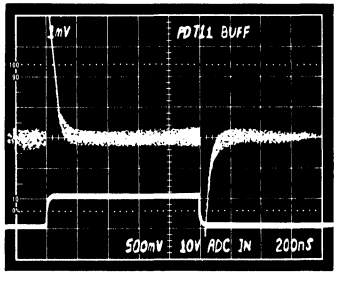
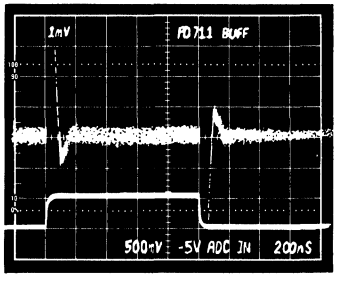


Figure 34. AD711 as ADC Unity Gain Buffer



a. Source Current = 2mA



b. Sink Current = 1mA

Figure 35. ADC Input Unity Gain Buffer Recovery Times

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L. Figure 37 shows a typical transient response for this connection.

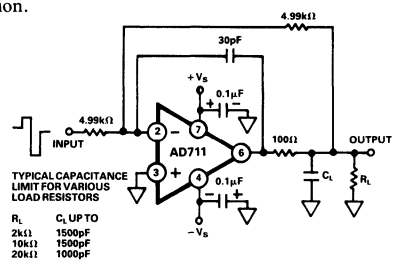


Figure 36. Circuit for Driving a Large Capacitive Load

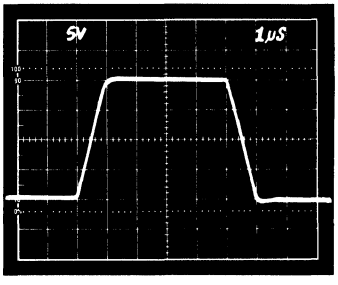


Figure 37. Transient Response R_L = 2kΩ, C_L =500pF

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the filter.

The use of a high performance amplifier such as the AD711 will minimize both dc and ac errors in all active filter applications.

SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD711 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD711 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

$R1 = R2 =$ user selected (typical values: 10kΩ – 100kΩ)

$$C1 = \frac{1.414}{(2\pi)\,(f_{cutoff})\,(R1)}, \quad C2 = \frac{0.707}{(2\pi)\,(f_{cutoff})\,(R1)}$$

Where C1 and C2 are in farads.

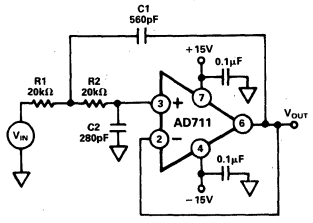


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD711 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low cost BiFET op amp showing 17dB more feedthrough at 5MHz.

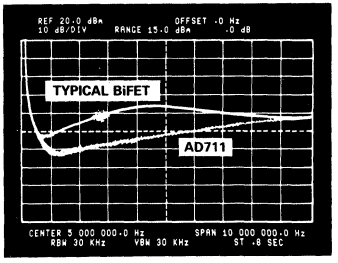


Figure 39.

9 POLE CHEBYCHEV FILTER

Figure 40 shows the AD711 and its dual counterpart, the AD712, as a 9 pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an anti-aliasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a 0.001μF capacitor and a 124kΩ resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001μF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

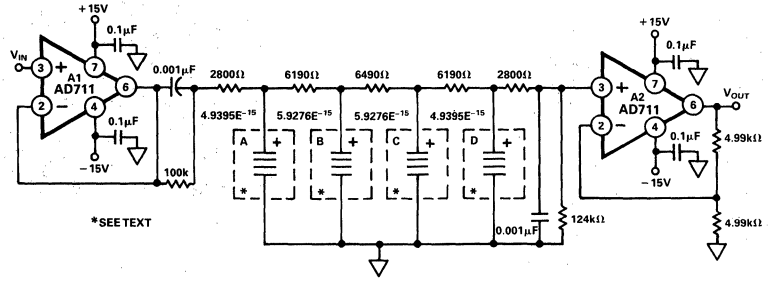


Figure 40. 9 Pole Chebychev Filter

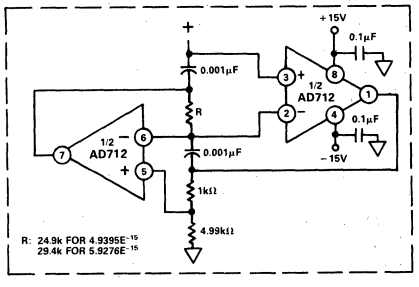


Figure 41. FDNR for 9 Pole Chebychev Filter

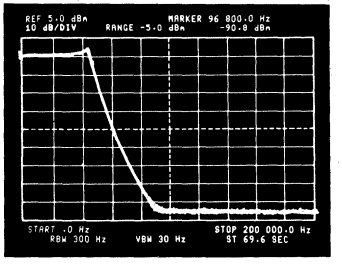


Figure 42. High Frequency Response for 9 Pole Chebychev Filter

ANALOG DEVICES

Dual Precision, Low Cost, High Speed, BiFET Op Amp

AD712

FEATURES

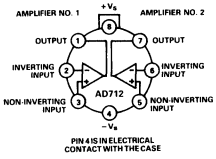
Enhanced Replacement for LF412 and TL082
AC PERFORMANCE:
- **Settles to ±0.01% in 1μs**
- **16V/μs min Slew Rate (AD712J)**
- **3MHz min Unity Gain Bandwidth (AD712J)**

DC PERFORMANCE:
- **0.30mV max Offset Voltage: (AD712C)**
- **5μV/°C max Drift: (AD712C)**
- **200V/mV min Open Loop Gain (AD712K)**
- **4μV p–p max Noise, 0.1Hz to 10Hz (AD712C)**

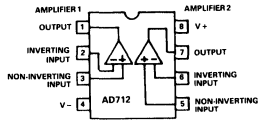
Surface Mount Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Parts Available
Single Version Available: AD711
Quad Version: AD713
Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form

AD712 FUNCTIONAL BLOCK DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N) Package, Cerdip (Q) Package and SOIC (R) Package



PRODUCT DESCRIPTION

The AD712 is a high speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD712 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD712 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD712 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD712J and AD712K are rated over the commercial temperature range of 0 to +70°C. The AD712A, AD712B and AD712C are rated over the industrial temperature range of −40°C to +85°C. The AD712S and AD712T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD712 is available in an 8-pin plastic mini-DIP, cerdip, TO-99 metal can, or chip form.

PRODUCT HIGHLIGHTS

1. The AD712 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.3mV max, C grade, 3mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 5μV/°C max on the AD712C.
3. Along with precision dc performance, the AD712 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD712 has a guaranteed and tested maximum voltage noise of 4μV p–p, 0.1 to 10Hz (AD712C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 50pA max (AD712C) and an input offset current of 10pA max (AD712C). Both input bias current and input offset current are guaranteed in the warmed-up condition.

SPECIFICATIONS (@ + 25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD712J/A/S Min	AD712J/A/S Typ	AD712J/A/S Max	AD712K/B/T Min	AD712K/B/T Typ	AD712K/B/T Max	AD712C Min	AD712C Typ	AD712C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	**3/1/1**		0.2	**1/0.7/0.7**		0.1	**0.30**	mV
T_{min} to T_{max}			4/2/2			**2/1.5/1.5**			**0.60**	mV
vs. Temp.		7	20/20/**20**		7	**10**		3	5	µV/°C
vs. Supply	**76**	95		**80**	100		**86**	110		dB
vs. Supply, T_{min} to T_{max}	76/76/**76**			**80**			**86**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		25	**75**		20	**75**		20	**50**	pA
Either Input at T_{max},										
V_{CM} = 0 (70°C/85°C/125°C)		0.6/1.6/26	1.7/4.8/**77**		0.5/1.3/20	1.7/4.8/**77**		1.3	3.2	nA
Either Input, V_{CM} = +10V			**100**			**100**			**75**	pA
Offset Current, V_{CM} = 0		10	**25**		5	**25**		5	**10**	pA
Offset Current at T_{max}										
(70°C/85°C/125°C)		0.3/0.7/11	0.6/1.6/**26**		0.1/0.3/5	0.6/1.6/**26**		0.3	0.7	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage			**3/1/1**			**1/0.7/0.7**			**0.3**	mV
Input Offset Voltage T_{min} to T_{max}			4/2/2			**2/1.5/1.5**			**0.6**	mV
Input Offset Voltage vs. Temp			20/20/**20**			**10**			5	µV/°C
Input Bias Current			**25**			**25**			**10**	pA
Crosstalk[4] @ 1kHz		120			120			120		dB
@ 100kHz		90			90			90		dB
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%[5]		1	1.2		1	1.2		1	1.2	µs
Total Harmonic Distortion										
f = 1kHz, $R_L \geq 2k\Omega$, V_O = 3V rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[6]		±20			±20			±20		V
Common-Mode Voltage										
Over Max Operating Range[7]	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	V
Common-Mode Rejection Ratio										
V_{CM} = ±10V	**76**	88		**80**	88		**86**	94		dB
T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
V_{CM} = ±11V	**70**	84		**76**	84		**76**	90		dB
T_{min} to T_{max}	70/70/**70**	80		**74**	80		**74**	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4**	µV p-p
f = 10Hz		45			45			45		nV/$\sqrt{Hz}$
f = 100Hz		22			22			22		nV/$\sqrt{Hz}$
f = 1kHz		18			18			18		nV/$\sqrt{Hz}$
f = 10kHz		16			16			16		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE										
f = 1kHz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**150**	400		**200**	400		**200**	400		V/mV
T_{min} to T_{max}, $R_L \geq 2k\Omega$	100/100/**100**			**100**			**100**			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
T_{min} to T_{max}	±12, ±12, **±12**	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Short Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current,										
Both Amplifiers		5	**6.8**		5	**6.0**		5	**5.6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD712J			AD712K					
Industrial (−40°C to +85°C)		AD712A			AD712B			AD712C		
Military (−55°C to +125°C)		AD712S			AD712T					
PACKAGE OPTIONS[8]										
SOIC (R-8)		AD712JR								
Plastic (N-8)		AD712JN			AD712KN					
Cerdip (Q-8)		AD712AQ, AD712SQ			AD712BQ, AD712TQ			AD712CQ		
TO-99 (H-08A)		AD712AH, AD712SH			AD712BH, AD712TH			AD712CH		
A, J and S Grade Chips Available										

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Refer to Figure 21.

[5]Refer to Figure 29.

[6]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[7]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.

[8]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
Storage Temperature Range N	−65°C to +125°C
Operating Temperature Range	
AD712J/K	0 to +70°C
AD712A/B/C	−40°C to +85°C
AD712S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 seconds)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics:

8-Pin Plastic Package: θ_{JA} = 165°C/W.

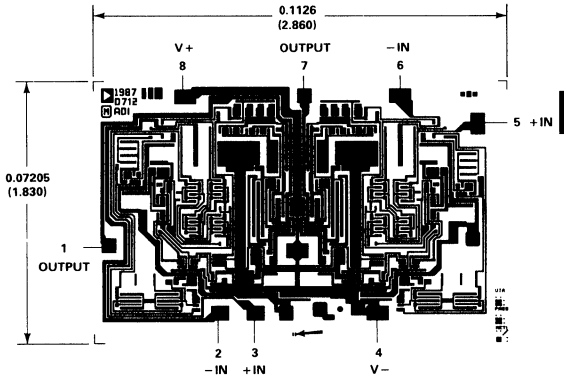
8-Pin Cerdip Package: θ_{JC} = 22°C/W, θ_{JA} = 110°C/W.

8-Pin Metal Can Package: θ_{JC} = 65°C/W, θ_{JA} = 150°C/W.

[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics

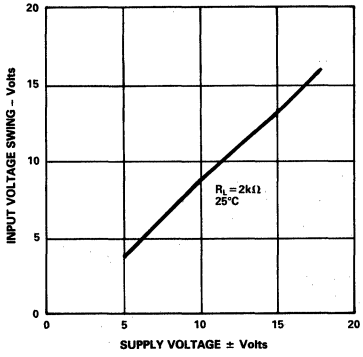


Figure 1. Input Voltage Swing vs. Supply Voltage

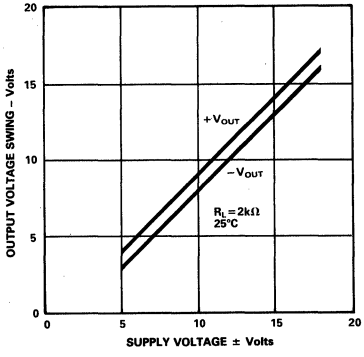


Figure 2. Output Voltage Swing vs. Supply Voltage

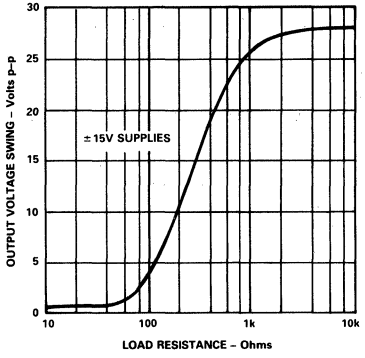


Figure 3. Output Voltage Swing vs. Load Resistance

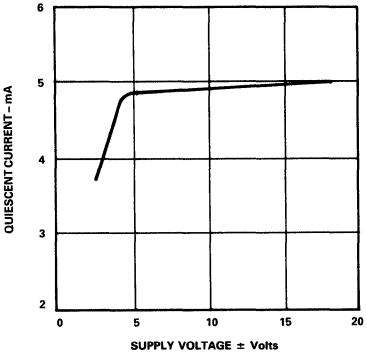


Figure 4. Quiescent Current vs. Supply Voltage

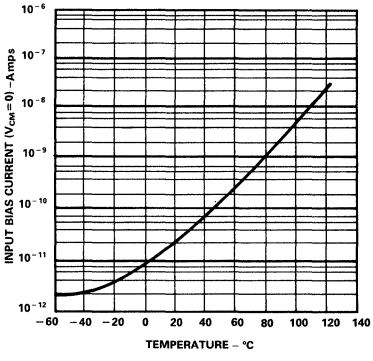


Figure 5. Input Bias Current vs. Temperature

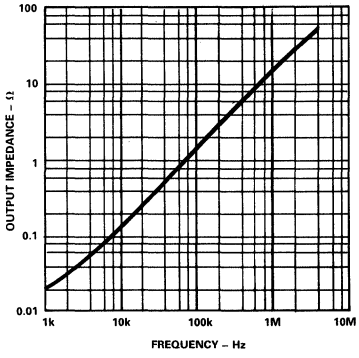


Figure 6. Output Impedance vs. Frequency

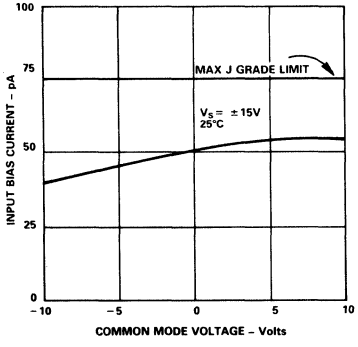


Figure 7. Input Bias Current vs. Common Mode Voltage

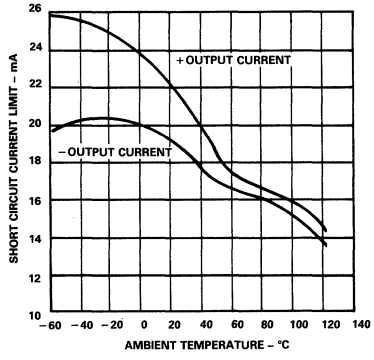


Figure 8. Short Circuit Current Limit vs. Temperature

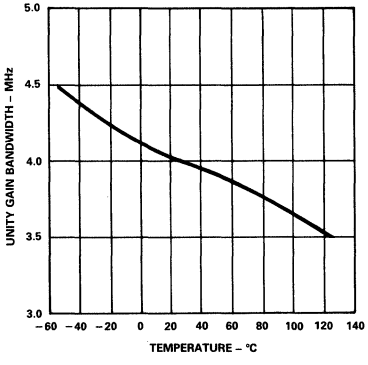


Figure 9. Unity Gain Bandwidth vs. Temperature

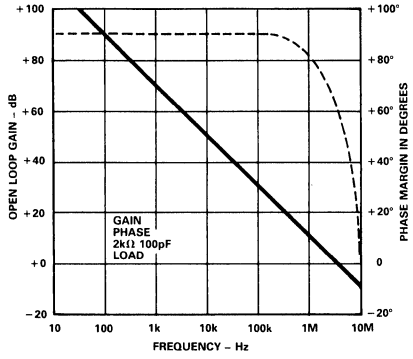


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

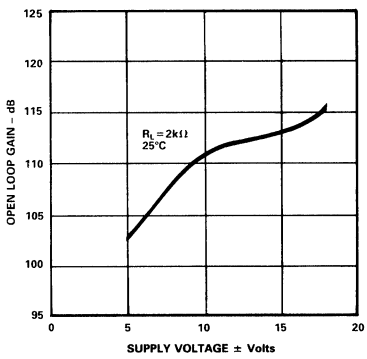


Figure 11. Open Loop Gain vs. Supply Voltage

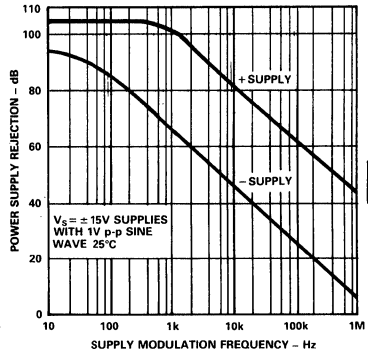


Figure 12. Power Supply Rejection vs. Frequency

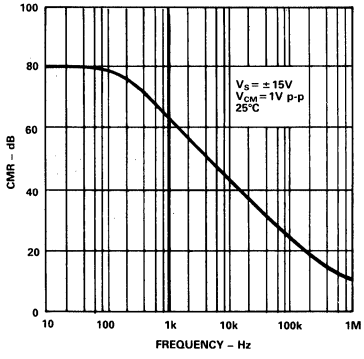


Figure 13. Common Mode Rejection vs. Frequency

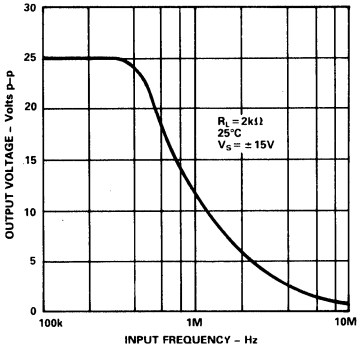


Figure 14. Large Signal Frequency Response

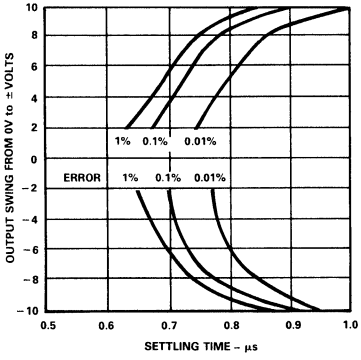


Figure 15. Output Swing and Error vs. Settling Time

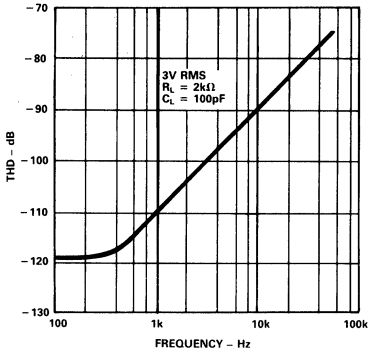


Figure 16. Total Harmonic Distortion vs. Frequency

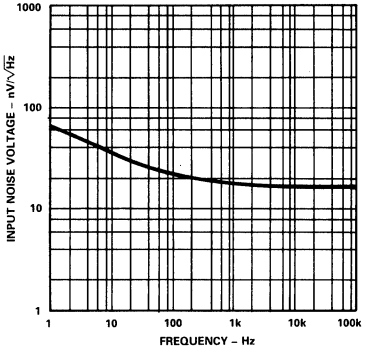


Figure 17. Input Noise Voltage Spectral Density

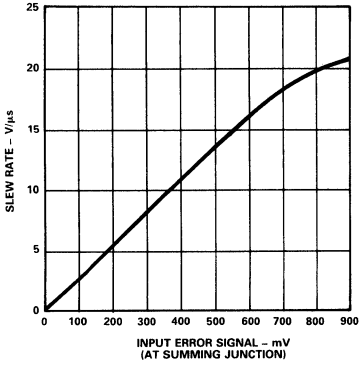


Figure 18. Slew Rate vs. Input Error Signal

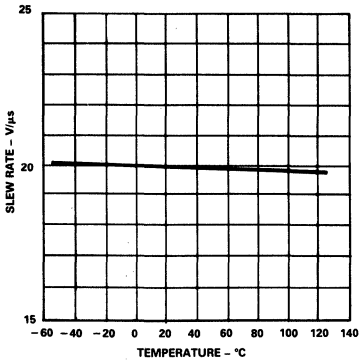


Figure 19. Slew Rate vs. Temperature

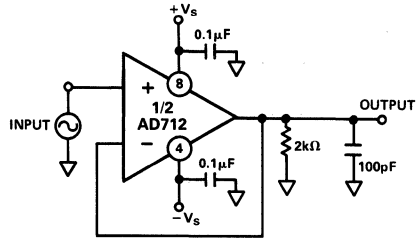


Figure 20. T.H.D. Test Circuit

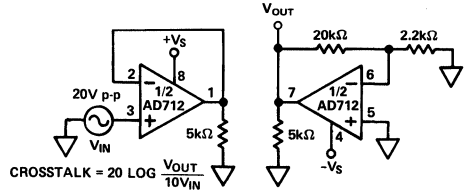


Figure 21. Crosstalk Test Circuit

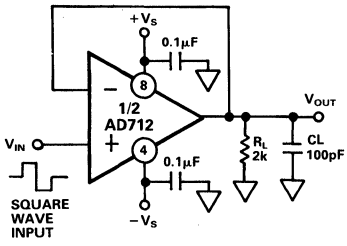


Figure 22a. Unity Gain Follower

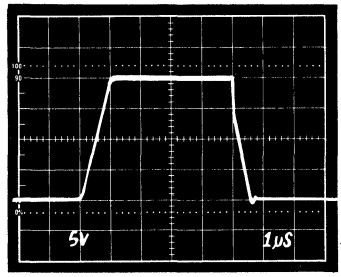


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

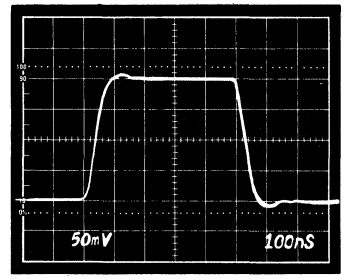


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

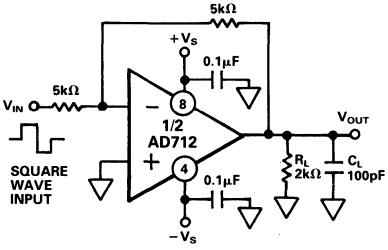


Figure 23a. Unity Gain Inverter

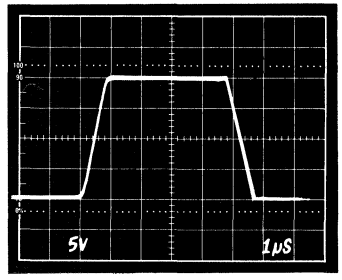


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

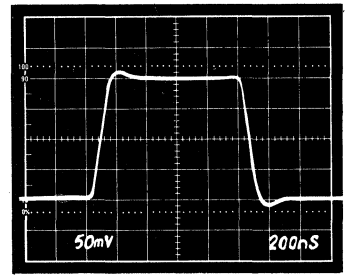


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

OPTIMIZING SETTLING TIME

Most bipolar high-speed D/A converters have curent outputs; therefore, for most applications, an external op-amp is required for current-to-voltage conversion. The settling time of the converter/op-amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op-amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1μs (to ±0.01% of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711/AD712 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD712 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD712 – both photos show the worst case situation: a full-scale input transition. The DAC's 4kΩ [10kΩ‖8kΩ = 4.4kΩ] output impedance together with a 10kΩ feedback resistor produce an op-amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op-amp output (0 to −10V Figure 25a, −10V to 0V Figure 25b.)

Therefore, with an ideal op-amp, settling to ±1/2LSB (±0.01%) requires that 375μV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD712 summing junction) must be less than 375μV. As shown in Figure 25, the total settling time for the AD712/AD565 combination is 1.2 microseconds.

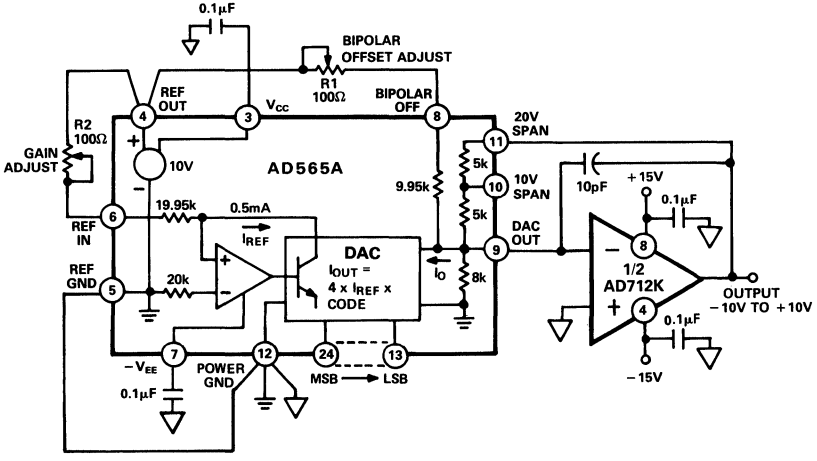
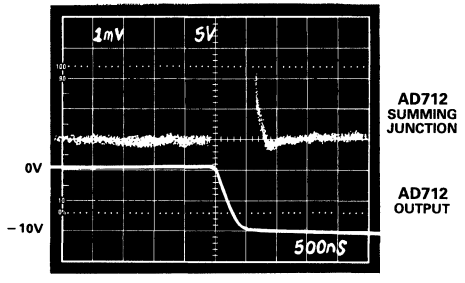
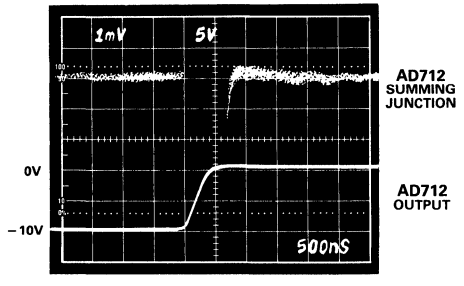


Figure 24. ±10V Voltage Output Bipolar DAC



a. (Full-Scale Negative Transition)



b. (Full-Scale Positive Transition)

Figure 25. Settling Characteristics for AD712 with AD565A

OP-AMP SETTLING TIME – A MATHEMATICAL MODEL

The design of the AD712 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD712 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 250pF load capacitance when operating as a unity gain follower.

If an op-amp is modeled as an ideal integrator with a unity gain crossover frequency of $\omega_O/2\pi$, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op-amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op-amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where $\frac{\omega_o}{2\pi}$ = op amp's unity gain frequency

G_N = "noise" gain of circuit $\left(1 + \frac{R}{R_O}\right)$

This equation may then be solved for C_f:

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1 - G_N)}}{R\omega_o}$$

In these equations, capacitor C_X is the total capacitance appearing at the inverting terminal of the op-amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op-amp (since the two are in parallel).

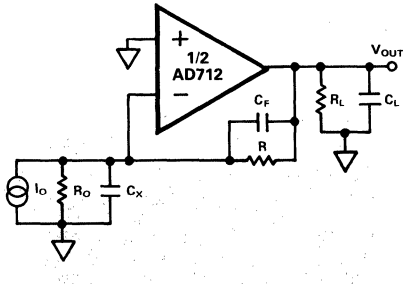


Figure 26a. Simplified Model of the AD712 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance C_X is EITHER the input capacitance of the op-amp if a simple inverting op-amp is being simulated OR it is the combined capacitance of the DAC output and the op-amp input if the DAC buffer is being modeled.

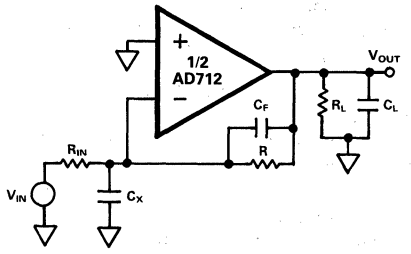


Figure 26b. Simplified Model of the AD712 Used as an Inverter

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op-amp output. Since the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor, C_F, to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD712 with R = 4kΩ.

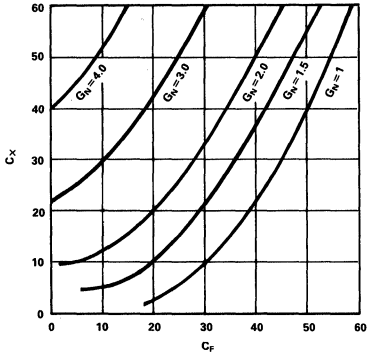


Figure 27. Value of Capacitor C_F vs. Value of C_X

The photos of Figures 28a and 28b show the dynamic response of the AD712 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high-speed, FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

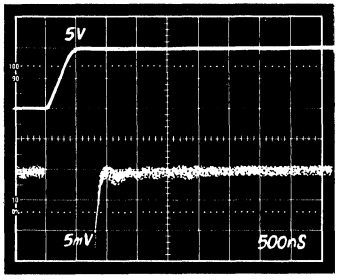


Figure 28a. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD712 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

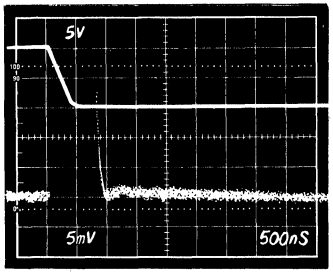


Figure 28b. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD712 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

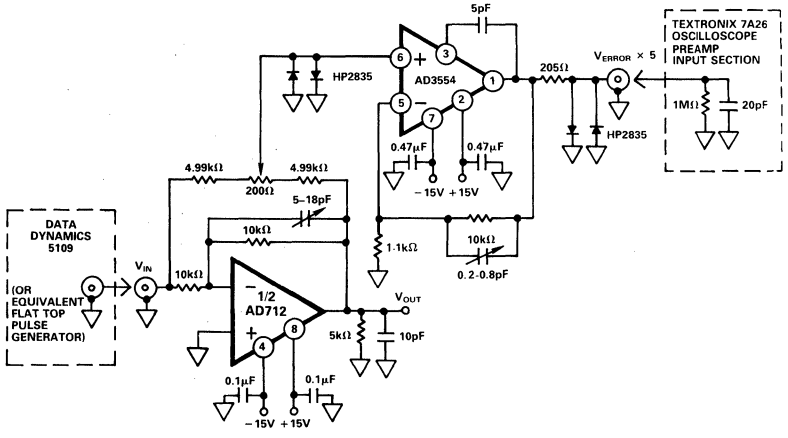


Figure 29. Settling Time Test Circuit

GUARDING

The low input bias current (15pA) and low noise characteristics of the AD712 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

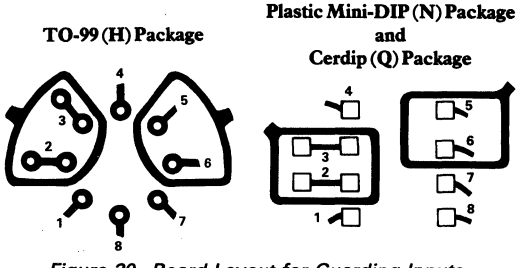


Figure 30. Board Layout for Guarding Inputs

D/A CONVERTER APPLICATIONS

The AD712 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD712K with guaranteed 700μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD712 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2 quadrant multiplication) or bipolar (4 quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

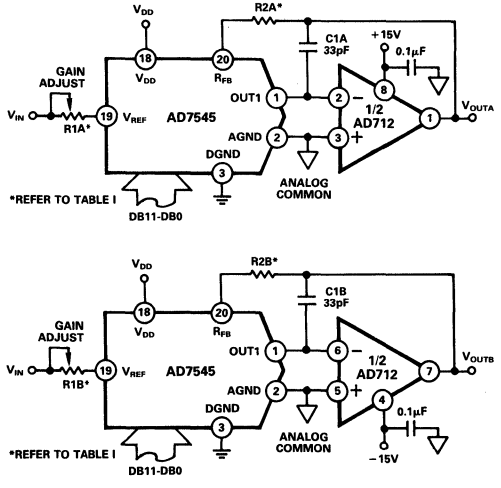


Figure 31. Unipolar Binary Operation

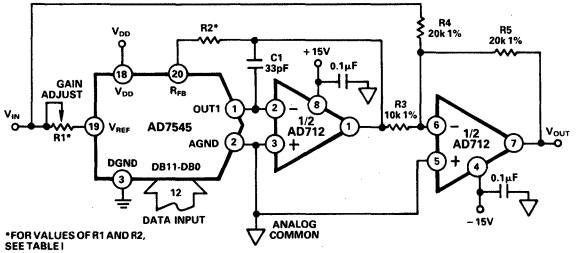


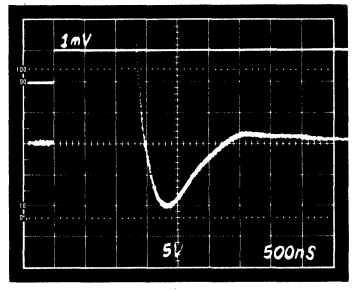
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

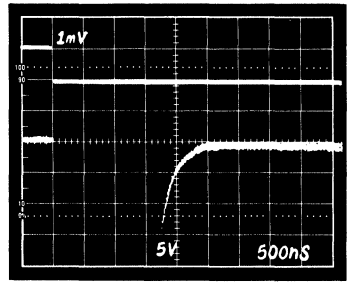
TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades of the AD7545 for V_{DD} = +5V

Figures 33a and 33b show the settling time characteristics of the AD712 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition



b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD712 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the 1/f region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD712C grade is specified at a maximum level of 4.0μV p-p, in a 0.1 to 10Hz bandwidth. Each AD712C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of 4.0μV are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD712 are sample-tested on an AQL basis to a limit of 6μV p-p, 0.1 to 10Hz.

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically-changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD712 is ideally suited to drive high-speed A/D converters since it offers both wide bandwidth and high open-loop gain.

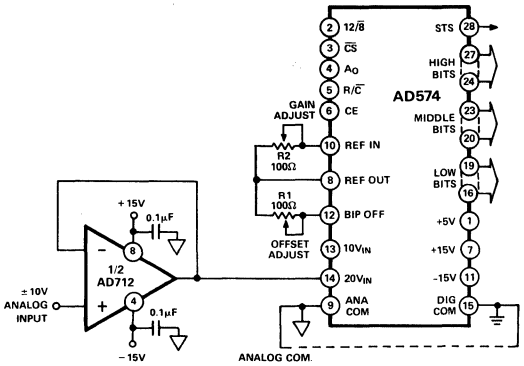
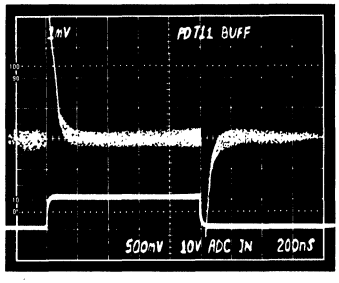
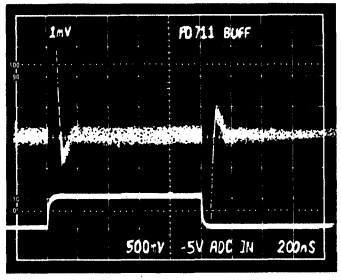


Figure 34. AD712 as ADC Unity Gain Buffer



a. Source Current = 2mA



b. Sink Current = 1mA

Figure 35. ADC Input Unity Gain Buffer Recovery Times

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L. Figure 37 shows a typical transient response for this connection.

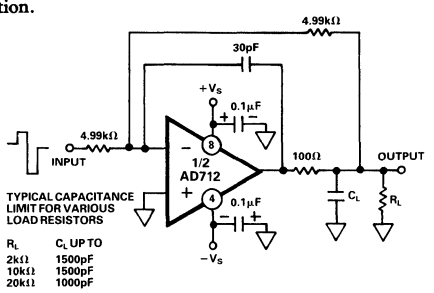


Figure 36. Circuit for Driving a Large Capacitive Load

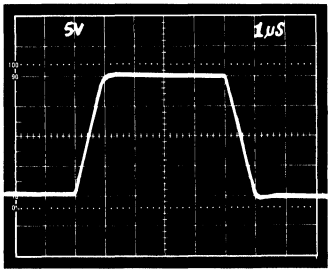


Figure 37. Transient Response R_L = 2kΩ, C_L =500pF

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the d.c. accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op-amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op-amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the filter.

The use of a high performance amplifier such as the AD712 will minimize both dc and ac errors in all active filter applications.

SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD712 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD712 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

R1 = R2 = user selected (typical values: 10kΩ – 100kΩ)

$$C1 \text{ (in farads)} = \frac{1.414}{(2\pi)\,(f_{cutoff})\,(R1)} \qquad C2 = \frac{0.707}{(2\pi)\,(f_{cutoff})\,(R1)}$$

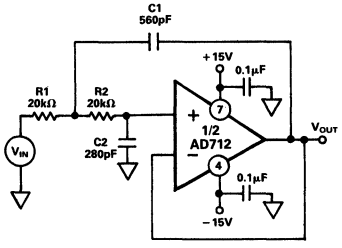


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD712 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low-cost BiFET op amp showing 17dB more feedthrough at 5MHz.

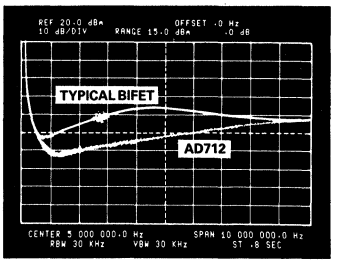


Figure 39.

9-POLE CHEBYCHEV FILTER

Figure 40 shows the AD712 and its single counterpart, the AD711, as a 9-pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an antialiasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a 0.001μF capacitor and a 124kΩ resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001μF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

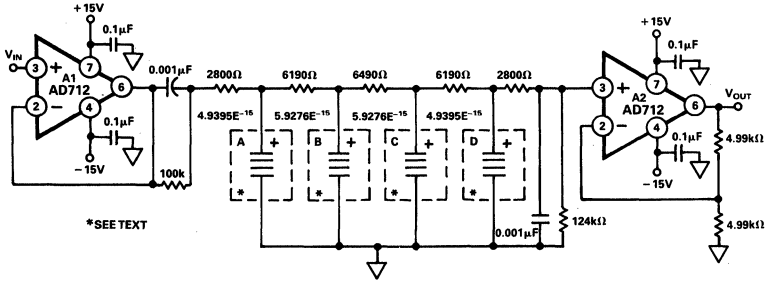


Figure 40. 9-Pole Chebychev Filter

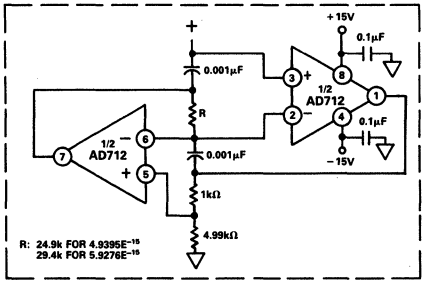


Figure 41. FDNR for 9-Pole Chebychev Filter

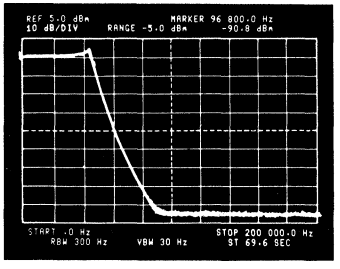


Figure 42. High Frequency Response for 9-Pole Chebychev Filter

Quad Precision, Low Cost, High Speed BiFET Op Amp

AD713

FEATURES
Enhanced Replacement for LF347 and TL084

AC PERFORMANCE
- **1μs Settling to 0.01% for 10V Step**
- **20V/μs Slew Rate**
- **0.0003% Total Harmonic Distortion (THD)**
- **4MHz Unity Gain Bandwidth**

DC PERFORMANCE
- **0.5mV max Offset Voltage (AD713K)**
- **20μV/°C max Drift (AD713K)**
- **200V/mV min Open Loop Gain (AD713K)**
- **2μV p–p typ Noise, 0.1Hz to 10Hz**

True 14-Bit Accuracy
Single Version: AD711, Dual Version: AD712
Available in 14-Pin Plastic DIP and Hermetic Cerdip Packages and Chip Form
MIL-STD-883B Processing Available

APPLICATIONS
Active Filters
Quad Output Buffers for 12- and 14-Bit DACs
Input Buffers for Precision ADCs
Photo Diode Preamplifier Applications

PRODUCT DESCRIPTION

The AD713 is a quad operational amplifier, consisting of four AD711 BiFET op amps. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates, and ample bandwidths. In addition, the AD713 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

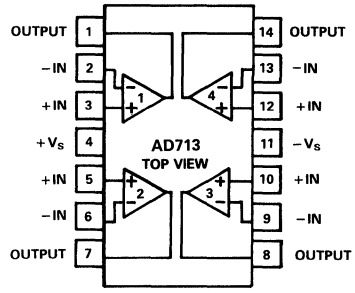
The single-pole response of the AD713 provides fast settling: 1μs to 0.01%. This feature combined with its high dc precision makes it suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. It is also an excellent choice for use in active filters in 12-, 14- and 16-bit data acquisition systems. Furthermore, the AD713's low total harmonic distortion (THD) level of 0.0003% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

The AD713 is internally compensated for stable operation at unity gain and is available in seven performance grades. The AD713J and AD713K are rated over the commercial temperature range of 0 to +70°C. The AD713A and AD713B are rated over the industrial temperature of −40°C to +85°C. The AD713S and AD713T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

The AD713 is offered in a 14-pin plastic DIP package, a hermetic cerdip package, or chip form.

AD713 FUNCTIONAL BLOCK DIAGRAM

Plastic DIP (N) Package
and
Cerdip (Q) Package



PRODUCT HIGHLIGHTS

1. The AD713 is a high speed BiFET op amp that offers excellent performance at competitive prices. It upgrades the performance of circuits using op amps such as the TL074/TL084, LT1058, LF347 and OPA404.
2. Slew rate is 100% tested for a guaranteed minimum of 16V/μs (J, A and S Grades).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provides outstanding dc precision. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
4. Very close matching of ac characteristics between the four amplifiers makes the AD713 ideal for high quality active filter applications.

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model		AD713J/A/S			AD713K/B/T			
	Conditions	Min	Typ	Max	Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[1]								
Initial Offset			0.3	**1.5**		0.2	**0.5**	mV
Offset	T_{min} to T_{max}		0.5	2/2/**2**		0.4	**0.7/0.7/1.0**	mV
vs. Temp.			5			5	**20/20/15**	μV/°C
vs. Supply		**78**	95		**84**	100		dB
vs. Supply	T_{min} to T_{max}	76/76/**76**	95		**84**	100		dB
Long-Term Stability			15			15		μV/month
INPUT BIAS CURRENT[2]								
Either Input	V_{CM}=0V		40	**150**		40	**75**	pA
Either Input @ T_{max} = 70°C/85°C/125°C	V_{CM}=0V			3.4/9.6/154			1.7/4.8/77	nA
Either Input	V_{CM}=+10V		55	200		55	**120**	pA
Offset Current	V_{CM}=0V		10	**75**		10	**35**	pA
Offset Current @ T_{max} = 70°C/85°C/125°C	V_{CM}=0V			1.7/4.8/77			0.8/2.2/36	nA
MATCHING CHARACTERISTICS								
Input Offset Voltage			0.5	**1.8**		0.4	**0.8**	mV
Input Offset Voltage	T_{min} to T_{max}		0.7	2.3/2.3/**2.3**		0.6	**1.0/1.0/1.3**	mV
Input Offset Voltage Drift			8			6	25	μV/°C
Input Bias Current			10	**100**		10	**35**	pA
Crosstalk (See Figure 20)	@ 1kHz			−130			−130	dB
	@ 100kHz			−95			−95	dB
FREQUENCY RESPONSE								
Gain BW, Small Signal	G=−1	3	4		3.4	4		MHz
Full Power Response	V_O=20V p-p		200			200		kHz
Slew Rate, Unity Gain	G=−1	**16**	20		**18**	20		V/μs
Settling Time to 0.01%	G=−1 (Fig. 23)		1	1.2		1	1.2	μs
Total Harmonic Distortion (See Figures 16 and 30)	f=1kHz RL≥2kΩ V_O=3V rms		0.0003			0.0003		%
INPUT IMPEDANCE								
Differential			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω||pF
Common Mode			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω||pF
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common Mode Voltage[4]			+14.5,−11.5			+14.5,−11.5		V
T_{min} to T_{max}		−11		+13	**−11**		+13	V
Common-Mode Rejection Ratio	V_{CM}=±10V	**78**	88		**84**	94		dB
	T_{min} to T_{max}	76/76/**76**	84		**82**	90		dB
	V_{CM}=±11V	**72**	84		**78**	90		dB
	T_{min} to T_{max}	70/70/**70**	80		**74**	84		dB
INPUT VOLTAGE NOISE	Noise 0.1 to 10Hz		2			2		μV p-p
	f=10Hz		45			45		nV/$\sqrt{Hz}$
	f=100Hz		22			22		nV/$\sqrt{Hz}$
	f=1kHz		18			18		nV/$\sqrt{Hz}$
	f=10kHz		16			16		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f=1kHz		0.01			0.01		pA/$\sqrt{Hz}$
OPEN LOOP GAIN	V_O=±10V							
	R_{LOAD}≥2kΩ	**150**	400		**200**	400		V/mV
	T_{min} to T_{max}	100/100/**100**			**100**			V/mV
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD}≥2kΩ	**+13,−12.5**	+13.9,−13.3		**+13,−12.5**	+13.9,−13.3		V
	T_{min} to T_{max}	±12/±12/**±12**	+13.8,−13.1		**±12**	+13.8,−13.1		V
Current	Short Circuit		25			25		mA

Model	Conditions	AD713J/A/S Min	AD713J/A/S Typ	AD713J/A/S Max	AD713K/B/T Min	AD713K/B/T Typ	AD713K/B/T Max	Units
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±4.5		±18	±4.5		±18	V
Quiescent Current			10.0	13.5		10.0	12.0	mA
PACKAGE OPTIONS[5]								
Plastic (N-14)		AD713JN			AD713KN			
Cerdip (Q-14)		AD713AQ, AD713SQ			AD713BQ, AD713TQ			
J and S Grade Chips Also Available								
TRANSISTOR COUNT	# of Transistors		120			120		

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[4]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.
[5]See Section 20 for package outline information.

Specifications subject to change without notice.
All min and max specifications are guaranteed.
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

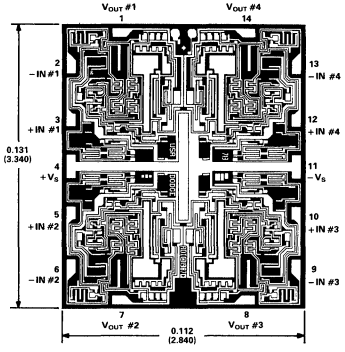
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2] 650mW
Input Voltage[3] . . . . . ±18V
Output Short Circuit Duration
(For One Amplifier) . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Operating Temperature Range
AD713J/K . . . . . 0 to +70°C
AD713A/B . . . . . −40°C to +85°C
AD713S/T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal characteristics: θ_{JC} = 30°C/Watt; θ_{JA} = 110°C/Watt.
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

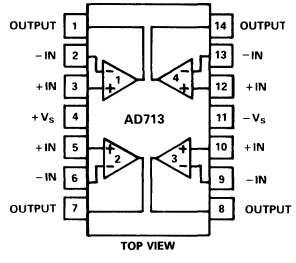
METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



CONNECTION DIAGRAM

Plastic (N) and Cerdip (Q) Packages



Typical Characteristics

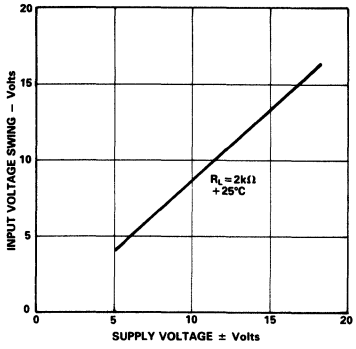


Figure 1. Input Voltage Swing vs. Supply Voltage

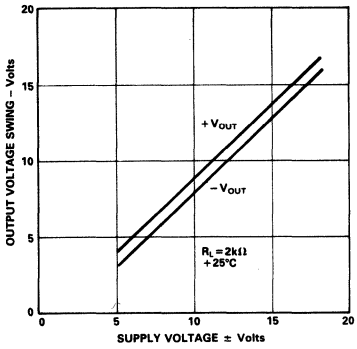


Figure 2. Output Voltage Swing vs. Supply Voltage

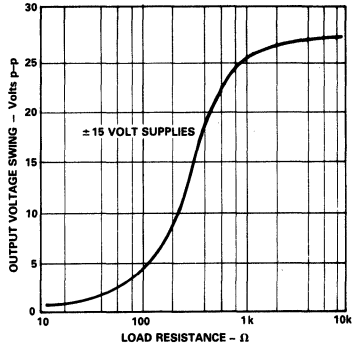


Figure 3. Output Voltage Swing vs. Load Resistance

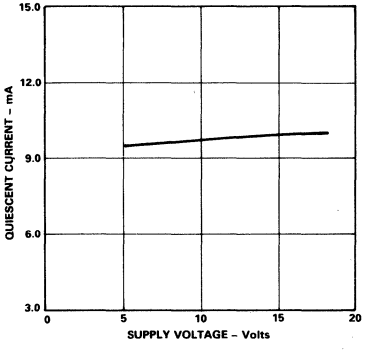


Figure 4. Quiescent Current vs. Supply Voltage

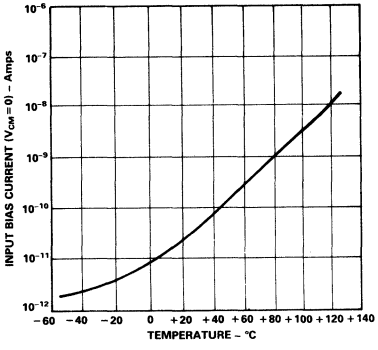


Figure 5. Input Bias Current vs. Temperature

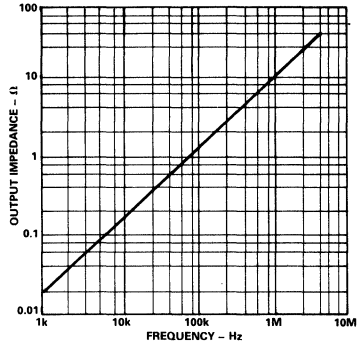


Figure 6. Output Impedance vs. Frequency, G = 1

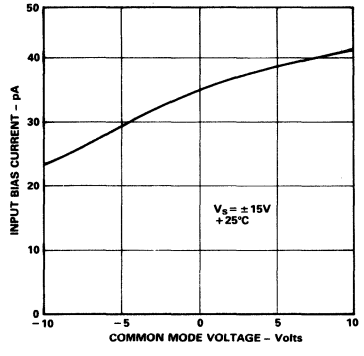


Figure 7. Input Bias Current vs. Common Mode Voltage

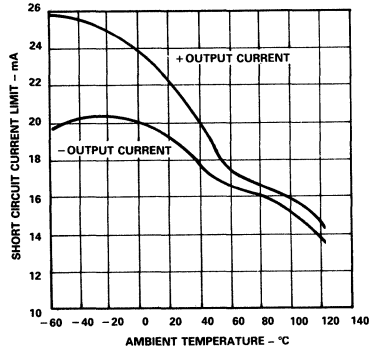


Figure 8. Short Circuit Current Limit vs. Temperature

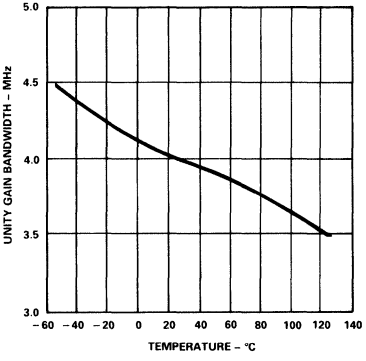


Figure 9. Gain Bandwidth Product vs. Temperature

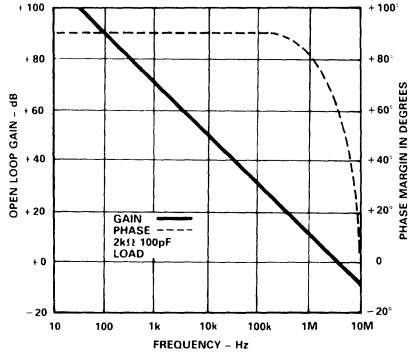


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

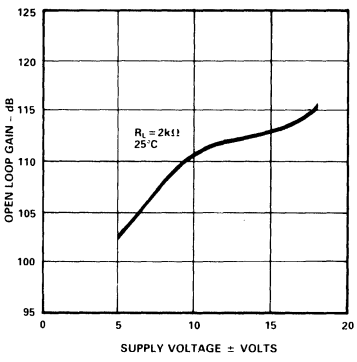


Figure 11. Open Loop Gain vs. Supply Voltage

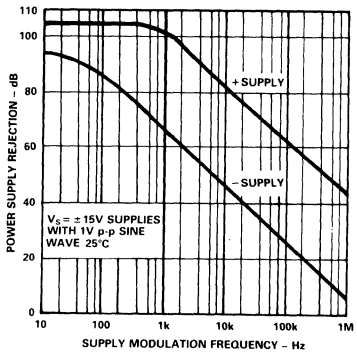


Figure 12. Power Supply Rejection vs. Frequency

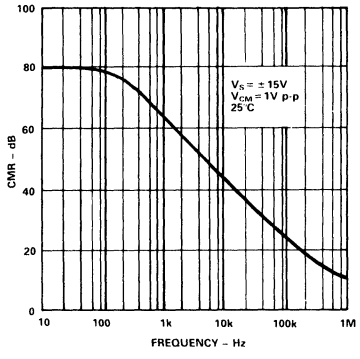


Figure 13. Common Mode Rejection vs. Frequency

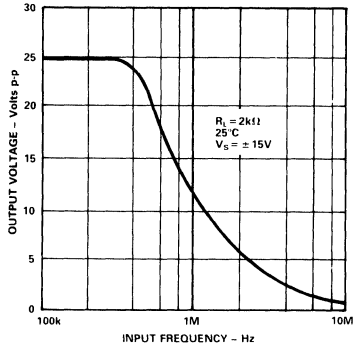


Figure 14. Large Signal Frequency Response

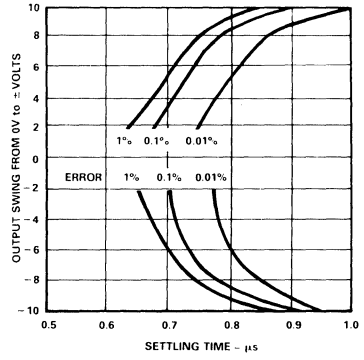


Figure 15. Output Swing and Error vs. Settling Time

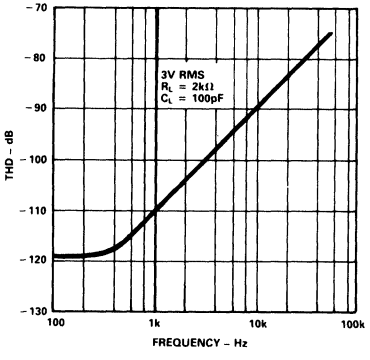


Figure 16. Total Harmonic Distortion vs. Frequency

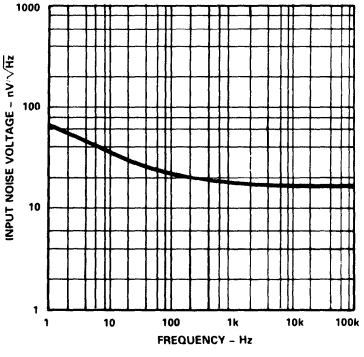


Figure 17. Input Noise Voltage Spectral Density

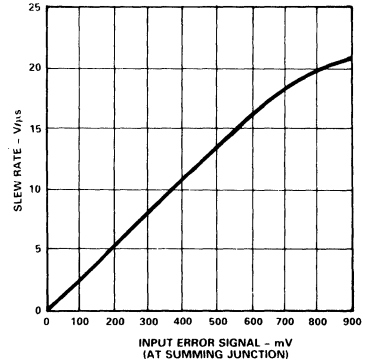
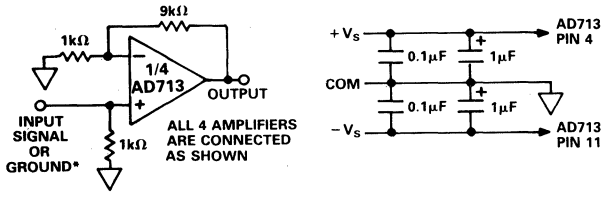


Figure 18. Slew Rate vs. Input Error Signal

Applying the AD713



*THE SIGNAL INPUT (1kHz SINEWAVE, 2V p-p) IS APPLIED TO ONE AMPLIFIER AT A TIME. THE OUTPUTS OF THE OTHER THREE AMPLIFIERS ARE THEN MEASURED FOR CROSSTALK.

Figure 19. Crosstalk Test Circuit

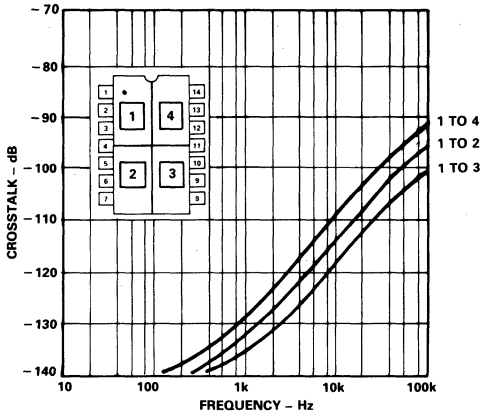


Figure 20. Crosstalk vs. Frequency

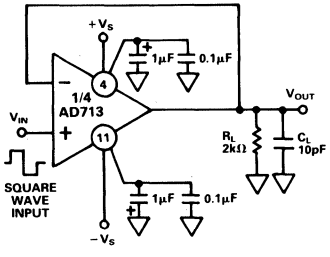


Figure 21a. Unity Gain Follower

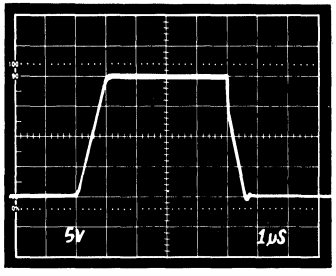


Figure 21b. Unity Gain Follower Large Signal Pulse Response

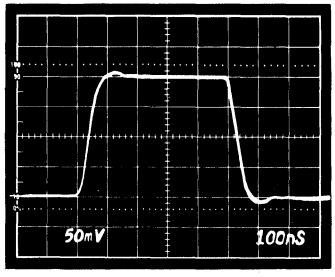


Figure 21c. Unity Gain Follower Small Signal Pulse Response

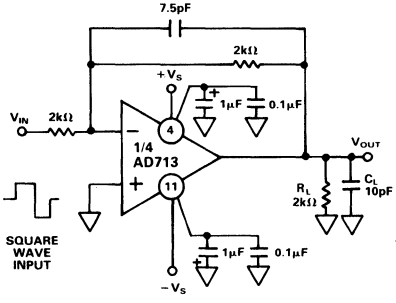


Figure 22a. Unity Gain Inverter

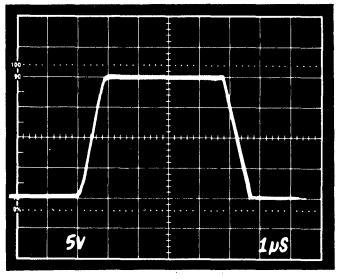


Figure 22b. Unity Gain Inverter Large Signal Pulse Response

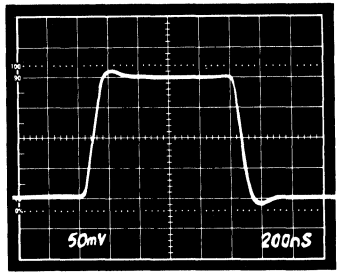


Figure 22c. Unity Gain Inverter Small Signal Pulse Response

MEASURING AD713 SETTLING TIME

The photos of Figures 24 and 25 show the dynamic response of the AD713 while operating in the settling time test circuit of Figure 23. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD713 under test, is clamped, amplified by op amp A2 and then clamped again.

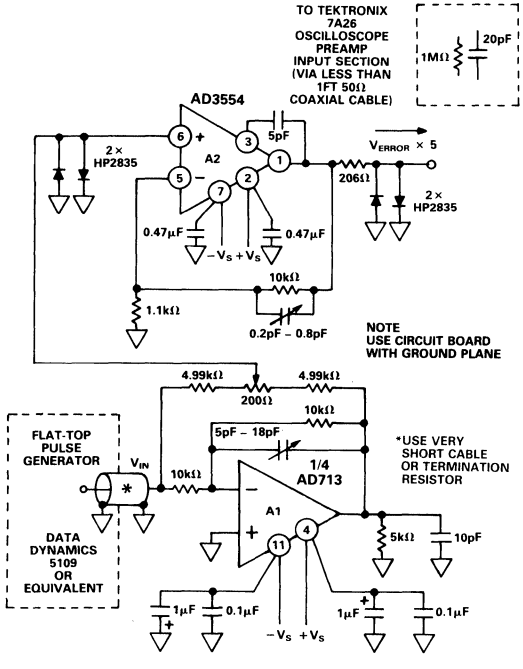


Figure 23. Settling Time Test Circuit

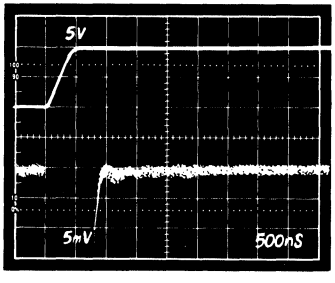


Figure 24. Settling Characteristics 0 to +10V Step. Upper Trace: Output of AD713 Under Test (5V/div). Lower Trace: Amplified Error Voltage (0.01%/div)

The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was carefully chosen because it recovers from the approximately 0.4 volt overload quickly enough to allow accurate measurement of the AD713's 1μs settling time. Amplifier A2 is a very high speed FET input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD713 under test (providing an overall gain of 5).

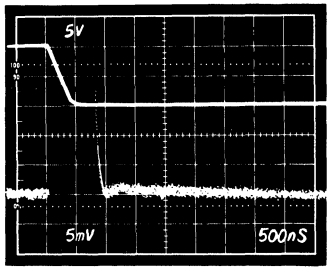


Figure 25. Settling Characteristics to −10V Step. Upper Trace: Output of AD713 Under Test (5V/div). Lower Trace: Amplified Error Voltage (0.01%/div)

POWER SUPPLY BYPASSING

The power supply connections to the AD713 must maintain a low impedance to ground over a bandwidth of 4MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1μF ceramic and a 1μF electrolytic capacitor as shown in Figure 26 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing in most applications. A minimum bypass capacitance of 0.1μF should be used for any application.

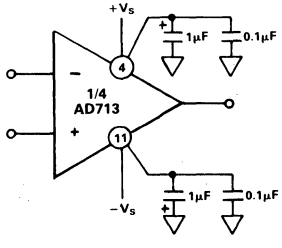


Figure 26. Recommended Power Supply Bypassing

A HIGH SPEED INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 27 can provide a range of gains from unity up to 1000 and higher using only a single AD713. The circuit bandwidth is 1.2MHz at a gain of 1 and 250kHz at a gain of 10; settling time for the entire circuit is less than 5μs to within 0.01% for a 10 volt step, (G = 10). Other uses for amplifier A4 include an active data guard and an active sense input.

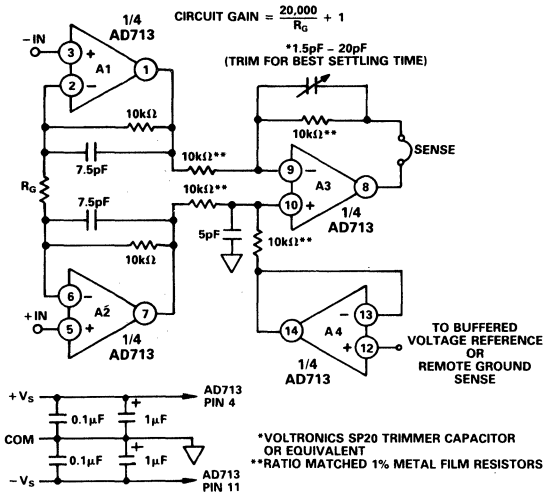


Figure 27. A High Speed Instrumentation Amplifier Circuit

Table I provides a performance summary for this circuit. The photo of Figure 28 shows the pulse response of this circuit for a gain of 10.

Gain	R_G	Bandwidth	T Settle (0.01%)
1	NC	1.2MHz	2μs
2	20kΩ	1.0MHz	2μs
10	4.04kΩ	0.25MHz	5μs

Table I. Performance Summary for the High Speed Instrumentation Amplifier Circuit

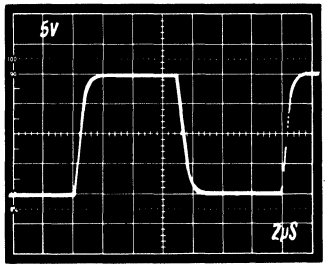


Figure 28. The Pulse Response of the High Speed Instrumentation Amplifier. Gain = 10

A HIGH SPEED FOUR OP AMP CASCADED AMPLIFIER CIRCUIT

Figure 29 shows how the four amplifiers of the AD713 may be connected in cascade to form a high gain, high bandwidth amplifier. This gain of 100 amplifier has a −3dB bandwidth greater than 600kHz.

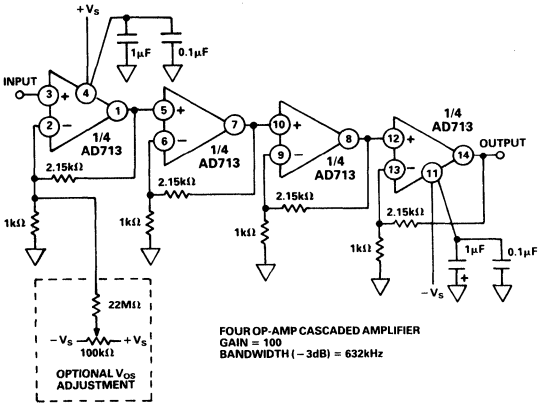


Figure 29. A High Speed Four Op Amp Cascaded Amplifier Circuit

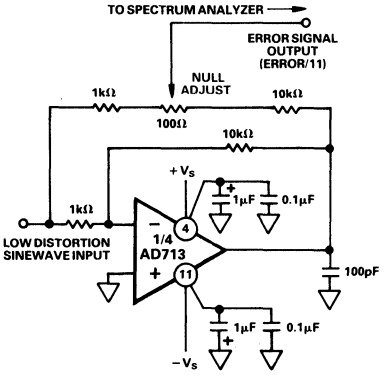


Figure 30. THD Test Circuit

HIGH SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

The wide input dynamic range of JFET amplifiers makes them ideal for use in both waveform reconstruction and digital-audio-DAC applications. The AD713, in conjunction with the AD1860 DAC, can achieve 0.0016% THD (here at a 4fs or a 176.4kHz update rate) without requiring the use of a deglitcher. Just such a circuit is shown in Figure 31. The 470pF feedback capacitor used with IC2a, along with op amp IC2b and its associated components, together form a 3-pole low-pass filter. Each or all of these poles can be tailored for the desired attenuation and phase characteristics required for a particular application. In this application, one half of an AD713 serves each channel in a two-channel stereo system.

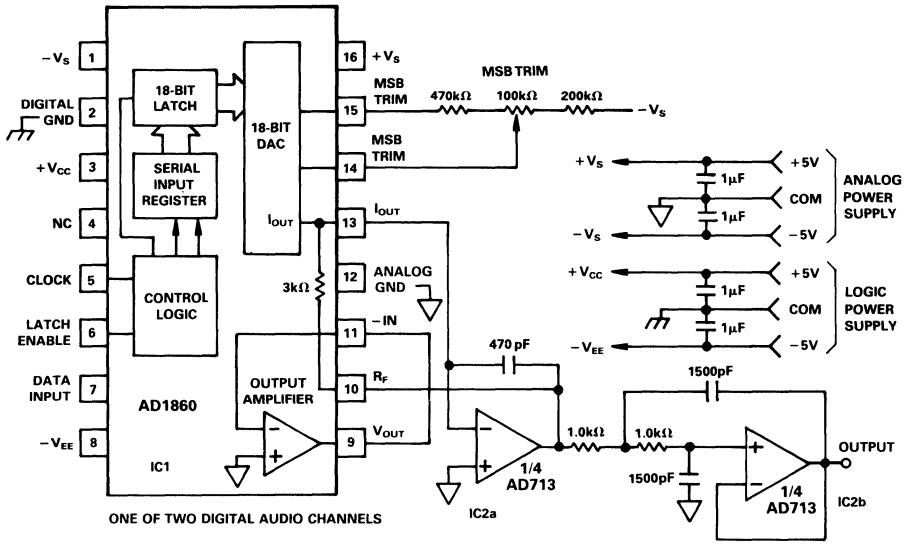


Figure 31. A D/A Converter Circuit for Digital Audio

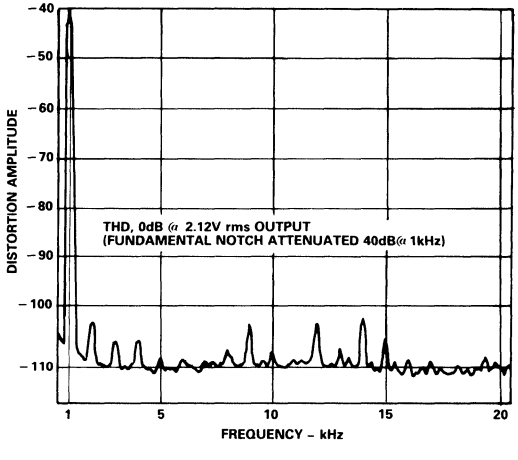


Figure 32. Harmonic Distortion vs. Frequency for the Digital Audio Circuit of Figure 31

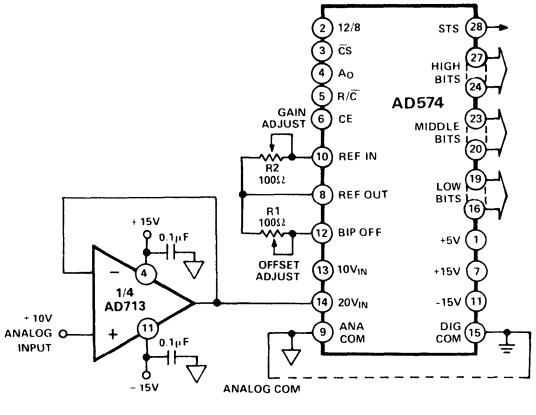


Figure 33. The AD713 as an ADC Buffer

Driving the Analog Input of an A/D Converter

An op amp driving the analog input of an A/D converter, such as that shown in Figure 33, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may vary by several hundred millivolts, resulting in high frequency modulation of the A/D input current. The output impedance of a feedback amplifier is made artificially low by its loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value.

Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω, due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidths, yielding slow recovery from output transients. The AD713 is ideally suited as a driver for A/D converters since it offers both a wide bandwidth and a high open loop gain.

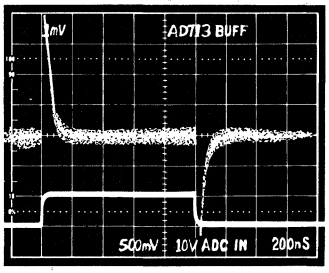


Figure 34. Buffer Recovery Time Source Current = 2mA

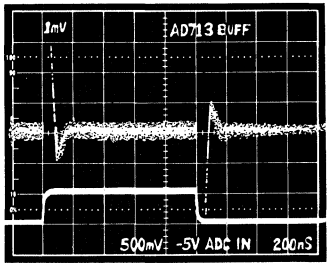


Figure 35. Buffer Recovery Time Sink Current = 1mA

Driving A Large Capacitive Load

The circuit of Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, Cl. Figure 37 shows a typical transient response for this connection.

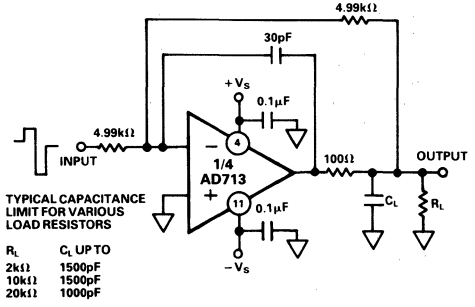


Figure 36. Circuit for Driving a Large Capacitance Load

Trim Resistor	JN/AQ/ SD	KN/BQ/ TD	LN/CQ/ UD	GLN/GCQ/ GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table II. Recommended Trim Resistor Values vs. Grades for AD7545 for V_D = +5V

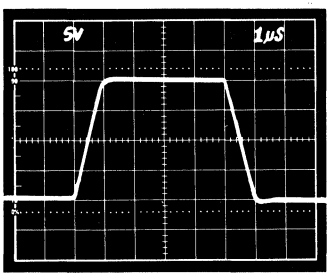


Figure 37. Transient Response, R_L = 2kΩ, C_L = 500pF

CMOS DAC APPLICATIONS

The AD713 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many "1"s, 3R for codes containing a single "1" and infinity for codes containing all zeros.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ , the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance. The AD713, with its guaranteed 1.5mV input offset voltage, minimizes this effect achieving 12-bit performance.

Figures 38 and 39 show the AD713 and a 12-bit CMOS DAC, the AD7545, configured for either a unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation which reduces overshoot and ringing.

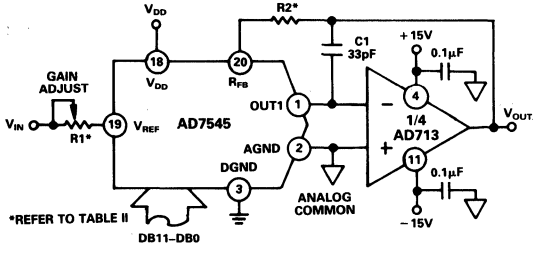


Figure 38. Unipolar Binary Operation

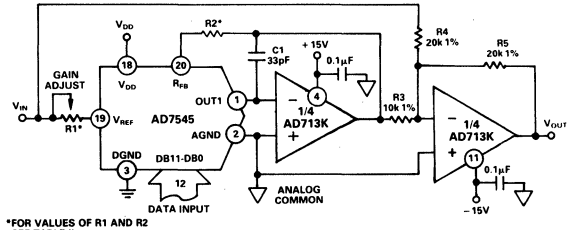
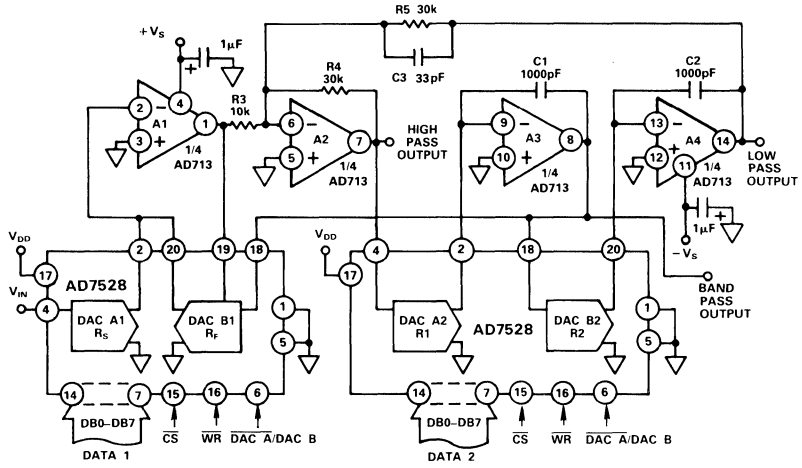


Figure 39. Bipolar Operation



CIRCUIT EQUATIONS

$C_1 = C_2$, $R_1 = R_2$, $R_4 = R_5$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

Note:
DAC equivalent resistance equals $\frac{256 \times (\text{DAC Ladder resistance})}{\text{DAC Digital Code}}$

Figure 40. A Programmable State Variable Filter Circuit

FILTER APPLICATIONS

A Programmable State Variable Filter

For the state variable or universal filter configuration of Figure 40 to function properly, DACs A1 and B1 need to control the gain and Q of the filter characteristic, while DACs A2 and B2 must accurately track for the simple expression of f_C to be true. This is readily accomplished using two AD7528 DACs and one AD713 quad op amp. Capacitor C3 compensates for the effects of op amp gain-bandwidth limitations.

This filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required. The programmable range for component values shown is f_C = 0 to 15kHz and Q = 0.3 to 4.5.

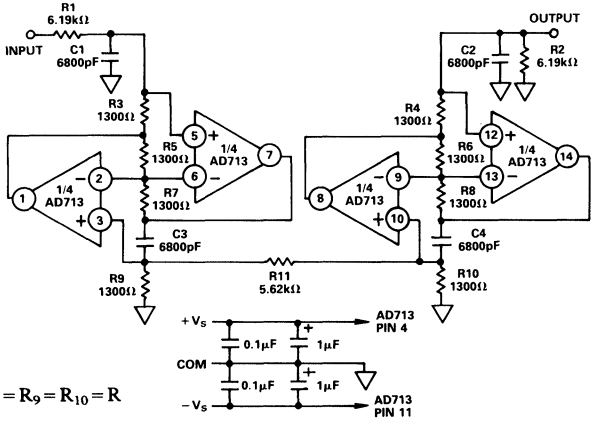
GIC and FDNR FILTER APPLICATIONS

The closely matched and uniform ac characteristics of the AD713 make it ideal for use in GIC (gyrator) and FDNR (frequency dependent negative resistor) filter applications. Figures 41 and 43 show the AD713 used in two typical active filters. The first shows a single AD713 simulating two coupled inductors configured as a one-third octave bandpass filter. A single section of this filter meets ANSI class II specifications and handles a 7.07V rms signal with <0.002% THD (20Hz-20kHz).

Figure 43 shows a 7-pole antialiasing filter for a 2× oversampling (88.2kHz) digital audio application. This filter has <0.05 dB pass band ripple and 19.8 ±0.3µs delay, dc-20kHz and will handle a 5V rms signal (V_S = ±15V) with no overload at any internal nodes.

The filter of Figure 41 can be scaled for any center frequency by using the formula:

$$f_C = \frac{1.11}{2\pi RC}$$



$$f_c = \frac{1.11}{2\pi RC}$$

$C_1 = C_2 = C_3 = C_4 = C$

$R_1 = R_2 = 4.76R$

$R_{11} = 4.32R$

$R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = R_9 = R_{10} = R$

Figure 41. A 1/3 Octave Filter Circuit

where all resistors and capacitors scale equally. Resistors R3—R8 should not be greater than 2kΩ in value, to prevent parasitic oscillations caused by the amplifier's input capacitance. If this is not practical, small lead capacitances (10-20pF) should be added across R5 and R6. Figures 42 and 44 show the output amplitude vs. frequency of these filters.

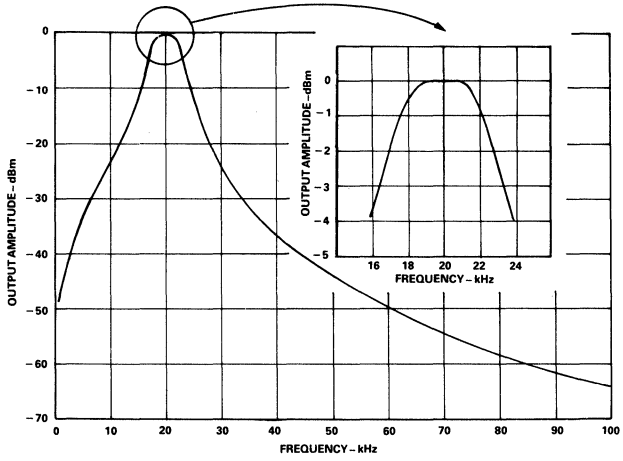


Figure 42. Output Amplitude vs. Frequency of 1/3 Octave Filter

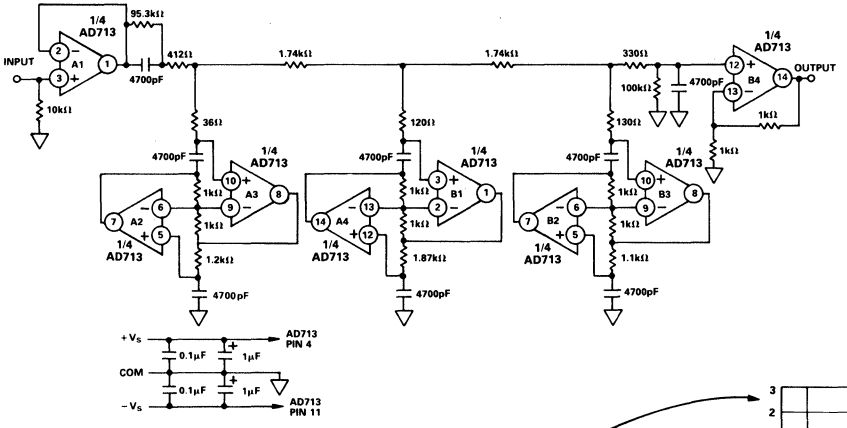


Figure 43. An Antialiasing Filter

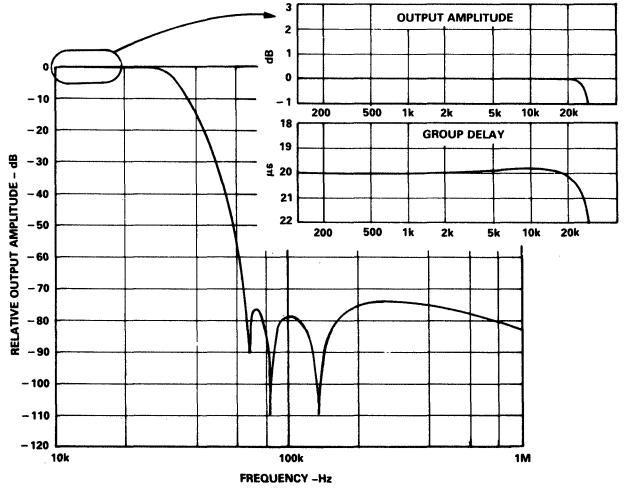


Figure 44. Relative Output Amplitude vs. Frequency of Antialiasing Filter

ANALOG DEVICES

Low Cost, High Accuracy IC Op Amps

AD741 Series

FEATURES

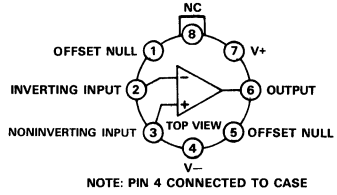
Precision Input Characteristics
- **Low V_{OS}: 0.5 mV max (L)**
- **Low V_{OS} Drift: 5 μV/°C max (L)**
- **Low I_b: 50 nA max (L)**
- **Low I_{OS}: 5 nA max (L)**
- **High CMRR: 90 dB min (K, L)**

High Output Capability
- **A_{OL} = 25,000 min, 1 kΩ Load (J, S)**
  T_{min} to T_{max}
- **V_O = ±10 V min, 1 kΩ Load (J, S)**

Chips and MIL-STD-883B Parts Available

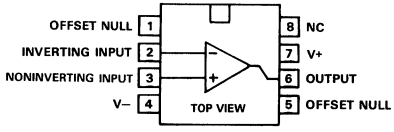
AD741 SERIES FUNCTIONAL BLOCK DIAGRAMS

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE

Mini-DIP (N) Package



GENERAL DESCRIPTION

The Analog Devices AD741 Series are high performance monolithic operational amplifiers. All the devices feature full short circuit protection and internal compensation.

The Analog Devices AD741J, AD741K, AD741L, and AD741S are specially tested and selected versions of the standard AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very-low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common-mode rejection. For example, the AD741L features maximum offset voltage drift of 5 μV/°C, offset voltage of 0.5 mV max, offset current of 5 nA max, bias current of 50 nA max, and a CMRR of 90 dB min. The AD741S offers guaranteed performance over the extended temperature range of −55°C to +125°C, with max offset voltage drift of 15 μV/°C, max offset voltage of 4 mV, max offset current of 25 nA, and a minimum CMRR of 80 dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000 swinging ±10 V into a 1 kΩ load from 0 to +70°C. The AD741S guarantees a minimum gain of 25,000 swinging ±10 V into a 1 kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common-mode range, and internal compensation. The AD741J, K and L are specified for operation from 0 to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

SPECIFICATIONS (typical @ +25°C and ±15 V dc, unless otherwise specified)

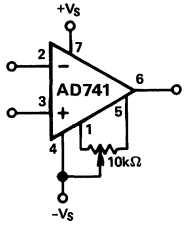
Model	AD741C Min	AD741C Typ	AD741C Max	AD741 Min	AD741 Typ	AD741 Max	AD741J Min	AD741J Typ	AD741J Max	Units
OPEN-LOOP GAIN										
R_L = 1 kΩ, V_O = ±10 V							**50,000**	200,000		V/V
R_L = 2 kΩ, V_O = ±10 V	**20,000**	200,000		**50,000**	200,000					V/V
T_A = min to max R_L = 2 kΩ	**15,000**			**25,000**			**25,000**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1 kΩ, T_A = min to max							**±10**	±13		V
Voltage @ R_L = 2 kΩ, T_A = min to max	**±10**	±13		**±10**	±13					V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Response (Unity Gain)										
Rise Time $C_L \leq$ 10 V p-p		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq$ 10 kΩ, Adjust to Zero		1.0	**6.0**		1.0	**5.0**		1.0	**3.0**	mV
T_A = min to max		1.0	**7.5**		1.0	**6.0**			**4.0**	mV
Average vs. Temperature (Untrimmed)									20	μV/°C
vs. Supply, T_A = min to max								30	100	μV/V
INPUT OFFSET CURRENT										
Initial		20	**200**		20	**200**		5	**50**	nA
T_A = min to max		40	**300**		85	500			**100**	nA
Average vs. Temperature								0.1		nA/°C
INPUT BIAS CURRENT										
Initial		80	**500**		80	**500**		40	**200**	nA
T_A = min to max		120	**800**		300	1,500			**400**	nA
Average vs. Temperature								0.6		nA/°C
INPUT IMPEDANCE DIFFERENTIAL	0.3	2.0		0.3	2.0			1.0		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe									±30	V
Common-Mode, max Safe	±12	±13		±12	±13			±15		V
Common-Mode Rejection,										
$R_S = \leq$ 10 kΩ, T_A = min to max,										
V_{IN} = ±12 V	**70**	90		**70**	90		**80**	90		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating							±5		±18	V
Power Supply Rejection Ratio		30	**150**		30	**150**				μV/V
Quiescent Current		1.7	**2.8**		1.7	**2.8**		2.2	**3.3**	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min					60	100				mW
T_A = max					45	75				mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	−55		+125	0		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C

NOTES

[1]For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice.

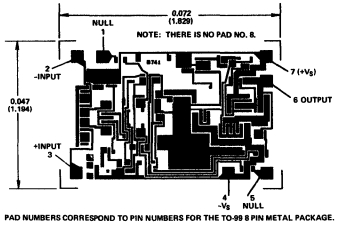
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.



Standard Nulling Offset Circuit

METALIZATION PHOTOGRAPHY

All versions of the AD741 are available in chip form. Contact factory for latest dimensions. Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

Model	AD741K Min	AD741K Typ	AD741K Max	AD741L Min	AD741L Typ	AD741L Max	AD741S Min	AD741S Typ	AD741S Max	Units
OPEN-LOOP GAIN										
R_L = 1 kΩ, V_O = ±10 V							50,000	200,000		V/V
R_L = 2 kΩ, V_O = ±10 V	50,000	200,000		50,000	200,000					V/V
T_A = min to max R_L = 2 kΩ	25,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1 kΩ, T_A = min to max										
Voltage @ R_L = 2 kΩ, T_A = min to max	±10	±13		±10	±13		±10	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Response (Unity Gain)										
Rise Time		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq 10$ kΩ, Adjust to Zero		0.5	2.0		0.2	0.5		1.0	2	mV
T_A = min to max			3.0			1.0			4	mV
Average vs. Temperature (Untrimmed)		6.0	15.0		2.0	5.0		6.0	15.0	μV/°C
vs. Supply, T_A = min to max		5	15.0		5	15.0		30	100	μV/V
INPUT OFFSET CURRENT										
Initial		2	10		2	5		2	10	nA
T_A = min to max			15			10			25	nA
Average vs. Temperature		0.02	0.02		0.02	0.1		0.1	0.25	nA/°C
INPUT BIAS CURRENT										
Initial		30	75		30	50		30	75	nA
T_A = min to max			120			100			250	nA
Average vs. Temperature		0.6	1.5		0.6	1.0		0.6	2.0	nA/°C
INPUT IMPEDANCE DIFFERENTIAL		2			2			2		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe		±30			±30			±30		V
Common-Mode, max Safe		±15			±15			±15		V
Common-Mode Rejection,										
$R_S = \leq 10$ kΩ, T_A = min to max,										
V_{IN} = ±12 V	90	100		90	100		90	100		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±22	±5		±22	±5		±22	V
Power Supply Rejection Ratio		20			20			20		μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.0	2.8	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min								60	100	mW
T_A = max								75	115	mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	AD741, J, K, L, S	AD741C
Supply Voltage	±22 V	±18 V
Internal Power Dissipation	500 mW[1]	500 mW
Differential Input Voltage	±30 V	±30 V
Input Voltage	±15 V	± 15 V
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature		
(Soldering, 60 sec)	+300°C	+300°C
Output Short Circuit Duration	Indefinite[2]	Indefinite

NOTES
[1]Rating applies for case temperature to +125°C. Derate TO-99 linearity at 6.5 mW/°C for ambient temperatures above +70°C.
[2]Rating applies for shorts to ground or either supply at case temperatures to +125°C or ambient temperatures to +75°C.

ORDERING GUIDE[1]

Model	Temperature Range	Package Options[2]	Initial Off Set Voltage
AD741CN	0 to +70°C	Mini-DIP (N-8)	6.0 mV
AD741CH	0 to +70°C	TO-99 (H-08A)	6.0 mV
AD741JN	0 to +70°C	Mini-DIP (N-8)	3.0 mV
AD741JH	0 to +70°C	TO-99 (H-08A)	3.0 mV
AD741KN	0 to +70°C	Mini-DIP (N-8)	2.0 mV
AD741KH	0 to +70°C	TO-99 (H-08A)	2.0 mV
AD741LN	0 to +70°C	Mini-DIP (N-8)	0.5 mV
AD741LH	0 to +70°C	TO-99 (H-08A)	0.5 mV
AD741H	−55°C to +125°C	TO-99 (H-08A)	5.0 mV
AD741SH	−55°C to +125°C	TO-99 (H-08A)	2.0 mV

NOTES
[1]J, K and S grade chips also available.
[2]See Section 20 for package outline information.

Typical Performance Curves

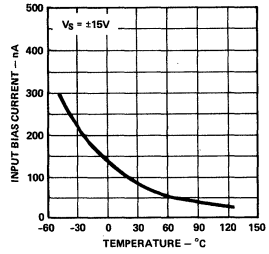


Figure 1. Input Bias Current vs. Temperature

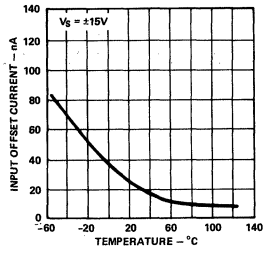


Figure 2. Input Offset Current vs. Temperature

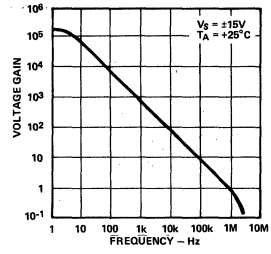


Figure 3. Open-Loop Gain vs. Frequency

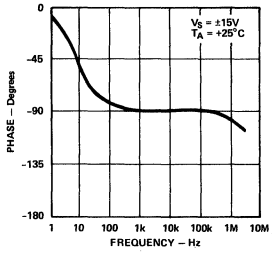


Figure 4. Open-Loop Phase Response vs. Frequency

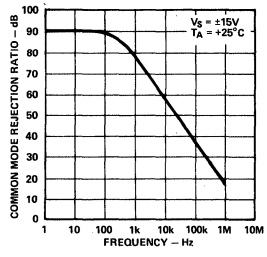


Figure 5. Common-Mode Rejection vs. Frequency

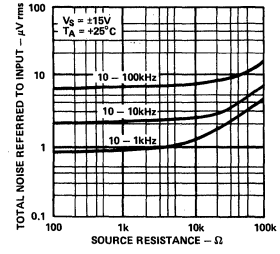


Figure 6. Broad Band Noise vs. Source Resistance

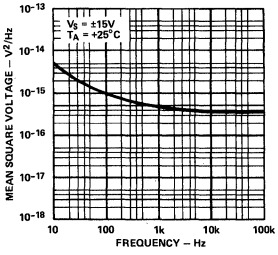


Figure 7. Input Noise Voltage vs. Frequency

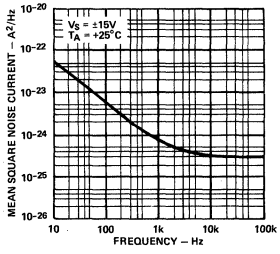


Figure 8. Input Noise Current vs. Frequency

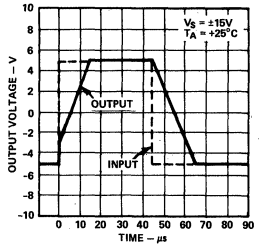


Figure 9. Voltage Follower Large Signal Pulse Response

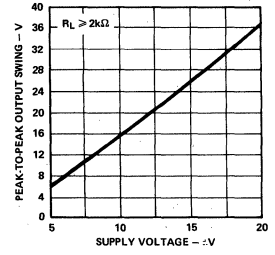


Figure 10. Output Voltage Swing vs. Supply Voltage

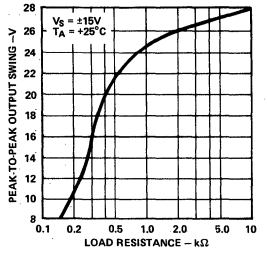


Figure 11. Output Voltage Swing vs. Load Resistance

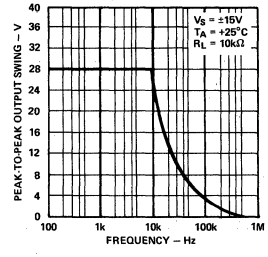


Figure 12. Output Voltage Swing vs. Frequency

ANALOG DEVICES

Ultralow Noise BiFET Op Amp

AD743

FEATURES

ULTRALOW NOISE PERFORMANCE
2.9 nV/√Hz at 10 kHz
0.38 μV p–p, 0.1 to 10 Hz
6.9 fA/√Hz Current Noise at 1 kHz

EXCELLENT DC PERFORMANCE
0.5 mV max Offset Voltage (AD743K)
250 pA max Input Bias Current (AD743K)
1000 V/mV min Open-Loop Gain

AC PERFORMANCE
2.8 V/μs Slew Rate
4.5 MHz Unity-Gain Bandwidth
THD = 0.0003% @ 1 kHz

APPLICATIONS
Sonar Preamplifiers
High Dynamic Range Filters (>140 dB)
Photodiode and IR Detector Amplifiers

PRODUCT DESCRIPTION

The AD743 is an ultralow noise precision, FET input, monolithic operational amplifier. It offers a combination of the ultralow voltage noise generally associated with bipolar input op amps and the very low input current of a FET-input device.

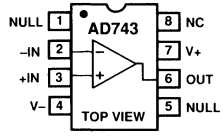
The AD743's guaranteed, maximum input voltage noise of 3.5 nV/√Hz at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is the maximum 1.0 μV p–p, 0.1 to 10 Hz noise. The AD743 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The AD743 is specifically designed for use as a preamp in capacitive sensors, such as ceramic hydrophones. It is available in six performance grades. The AD743J and AD743K are rated over the commercial temperature range of 0 to +70°C. The AD743A and AD743B are rated over the industrial temperature range of −40°C to +85°C. The AD743S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

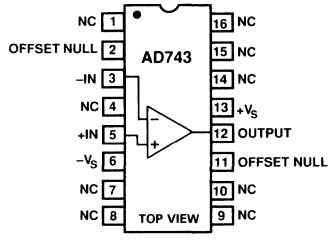
The AD743 is available in 8-pin plastic mini-DIP, 8-pin cerdip, 16-pin SOIC, or in chip form.

AD743 CONNECTION DIAGRAMS

8-Pin Plastic (N) and Cerdip (Q) Packages



16-Pin SOIC (R) Package



PRODUCT HIGHLIGHTS

1. The low offset voltage and low input offset voltage drift of the AD743 coupled with its ultralow noise performance mean that the AD743 can be used for upgrading many applications now using bipolar amplifiers.
2. The combination of low voltage and low current noise make the AD743 ideal for charge sensitive applications such as accelerometers and hydrophones.
3. The low input offset voltage and low noise level of the AD743 provide >140 dB dynamic range.
4. The typical 10 kHz noise level of 2.9 nV/√Hz permits a three op amp instrumentation amplifier, using three AD743s, to be built which exhibits less than 4.2 nV/√Hz noise at 10 kHz and which has low input bias currents.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD743J/A Min	AD743J/A Typ	AD743J/A Max	AD743K/B Min	AD743K/B Typ	AD743K/B Max	AD743S Min	AD743S Typ	AD743S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.25	1.0		0.1	0.5/0.25		0.25	1.0	mV
Initial Offset	T_{min} to T_{max}			2.0			1.0/0.50			2.0	mV
vs. Temp.	T_{min} to T_{max}		2			1			2		μV/°C
vs. Supply (PSRR)	±12 V to ±18 V	90	96		100	106		90	96		dB
vs. Supply (PSRR)	T_{min} to T_{max}	88			98	100		88			dB
INPUT BIAS CURRENT[2]											
Either Input	V_{CM} = 0 V		150	400		150	250		150	400	pA
Either Input @ T_{max}	V_{CM} = 0 V			8.8/25.6			5.5/16			413	nA
Either Input	V_{CM} = +10 V		250	600		250	400		300	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30			30			30		pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		20	100		25	50		20	100	pA
Offset Current @ T_{max}	V_{CM} = 0 V			2.2/6.4			1.1/3.2			102	nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = −1		4.5			4.5			4.5		MHz
Full Power Response	V_O = 20 V p-p		25			25			25		kHz
Slew Rate, Unity Gain	G = −1		2.8			2.8			2.8		V/μs
Settling Time to 0.01%			6			6			6		μs
Total Harmonic Distortion[3] (Fig. 16)	f = 1 kHz G = −1		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			$1 \times 10^{10} \| 20$			$1 \times 10^{10} \| 20$			$1 \times 10^{10} \| 20$		Ω||pF
Common Mode			$3 \times 10^{11} \| 18$			$3 \times 10^{11} \| 18$			$3 \times 10^{11} \| 18$		Ω||pF
INPUT VOLTAGE RANGE											
Differential[4]			±20			±20			±20		V
Common-Mode Voltage			+13.3, −10.7			+13.3, −10.7			+13.3, −10.7		V
Over Max Operating Range		−10		+12	−10		+12	−10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		90	102		80	95		dB
	T_{min} to T_{max}	78			88			78			dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.38			0.38	1.0		0.38		μV p-p
	f = 10 Hz		5.5			5.5			5.5		$nV/\sqrt{Hz}$
	f = 100 Hz		3.6			3.6			3.6		$nV/\sqrt{Hz}$
	f = 1 kHz		3.2			3.2			3.2		$nV/\sqrt{Hz}$
	f = 10 kHz		2.9			2.9	3.5		2.9		$nV/\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz		6.9			6.9			6.9		$fA/\sqrt{Hz}$
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 2 kΩ	1000	4000		2000	4000		1000	4000		V/mV
	T_{min} to T_{max}	800			800			800			V/mV
	R_{LOAD} = 600 Ω		1200			1200			1200		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 600 Ω	+13, −12			+13, −12			+13, −12			V
	R_{LOAD} ≥ 600 Ω T_{min} to T_{max}		+13.6, −12.6			+13.6, −12.6			+13.6, −12.6		V
	R_{LOAD} ≥ 2 kΩ	±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Current	Short Circuit	20	40		20	40		20	40		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.8		±18	±4.8		±18	±4.8		±18	V
Quiescent Current			8.1	10.0		8.1	10.0		8.1	10.0	mA
TRANSISTOR COUNT	# of Transistors		50			50			50		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Gain = −1, R_L = 2 kΩ, C_L = 10 pF.
[4]Defined as voltage between inputs, such that neither exceeds ±10 V from common.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test; all others are guaranteed but not necessarily tested. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD743J/K . . . . . 0 to +70°C
AD743A/B . . . . . −40°C to +85°C
AD743S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . . 300°C

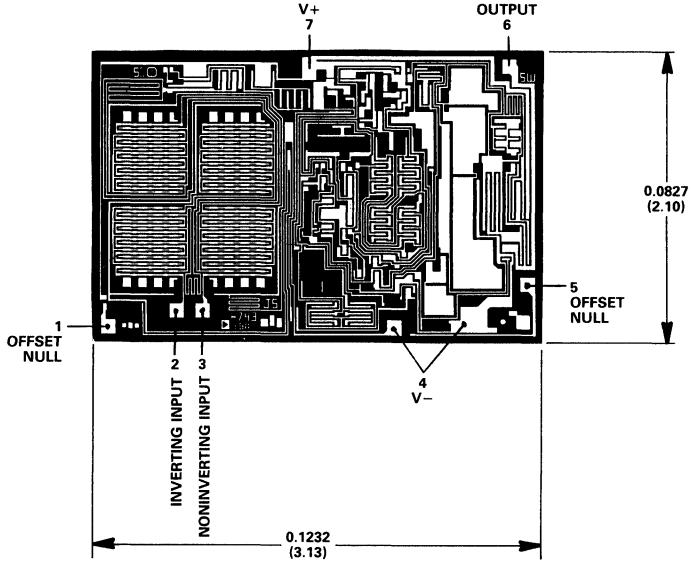
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-pin plastic package: θ_{JA} = 100°C/Watt
8-pin cerdip package: θ_{JA} = 110°C/Watt
16-pin plastic SOIC package: θ_{JA} = 90°C/Watt

ESD SUSCEPTIBILITY

All pins are rated for a minimum of 4000 V protection. ESD testing conforms to human body model.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics (@ +25°C, V_S = ±15 V)

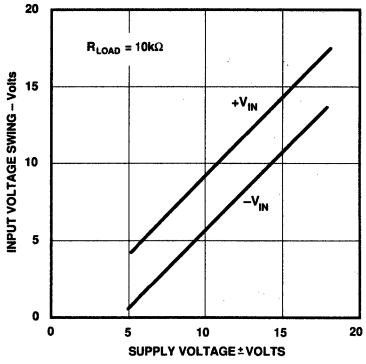


Figure 1. Input Voltage Swing vs. Supply Voltage

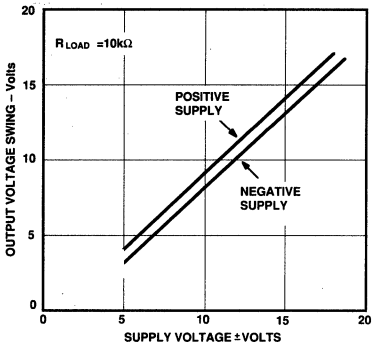


Figure 2. Output Voltage Swing vs. Supply Voltage

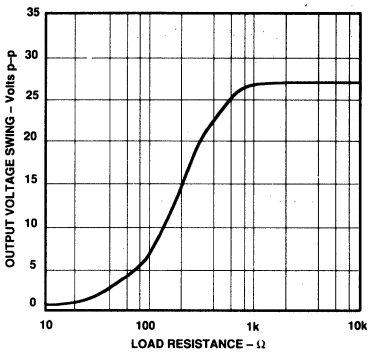


Figure 3. Output Voltage Swing vs. Load Resistance

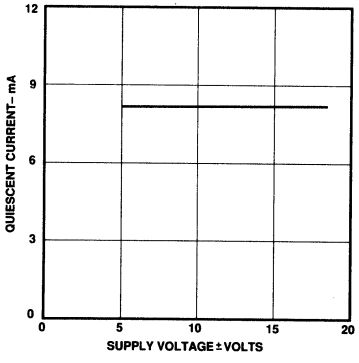


Figure 4. Quiescent Current vs. Supply Voltage

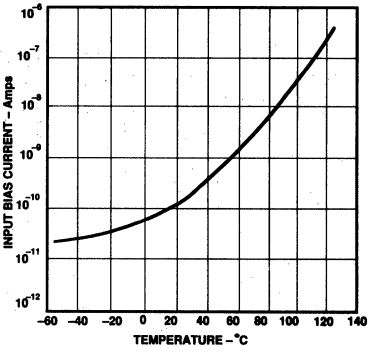


Figure 5. Input Bias Current vs. Temperature

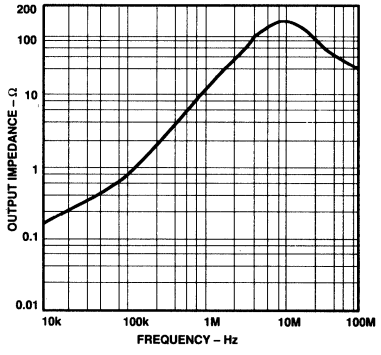


Figure 6. Output Impedance vs. Frequency (Closed Loop Gain = −1)

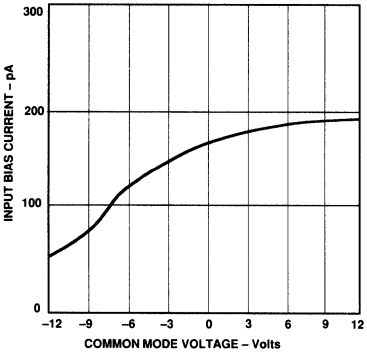


Figure 7. Input Bias Current vs. Common-Mode Voltage

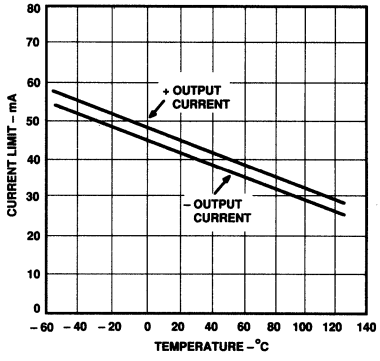


Figure 8. Short Circuit Current Limit vs. Temperature

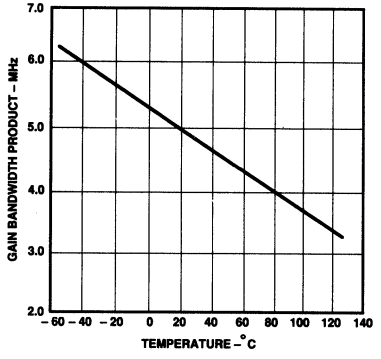


Figure 9. Gain Bandwidth Product vs. Temperature

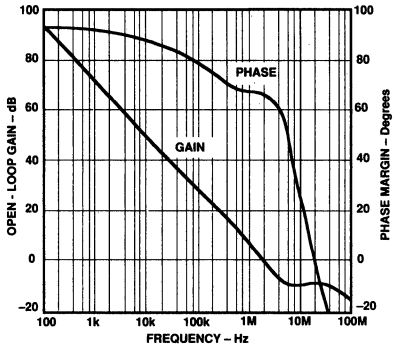


Figure 10. Open-Loop Gain and Phase vs. Frequency

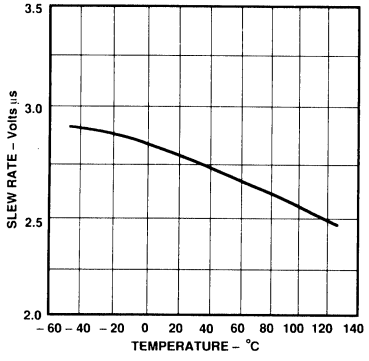


Figure 11. Slew Rate vs. Temperature (Gain = −1)

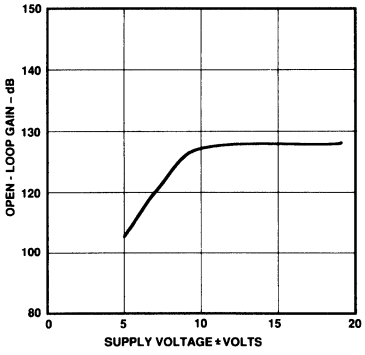


Figure 12. Open-Loop Gain vs. Supply Voltage, R_{LOAD} = 2K

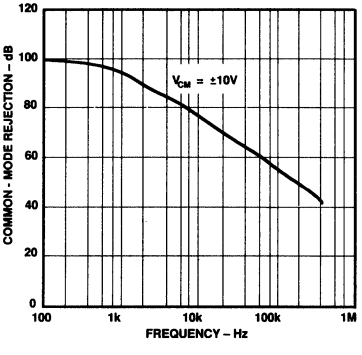


Figure 13. Common-Mode Rejection vs. Frequency

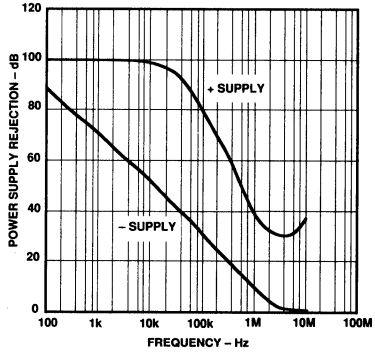


Figure 14. Power Supply Rejection vs. Frequency

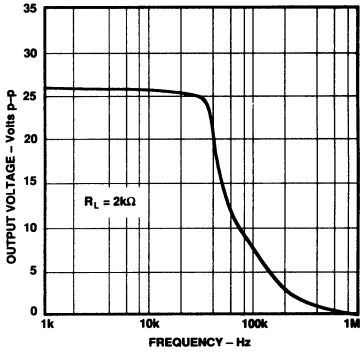


Figure 15. Large Signal Frequency Response

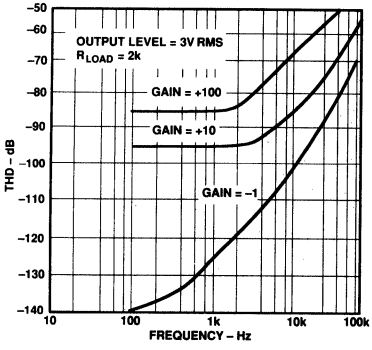


Figure 16. Total Harmonic Distortion vs. Frequency

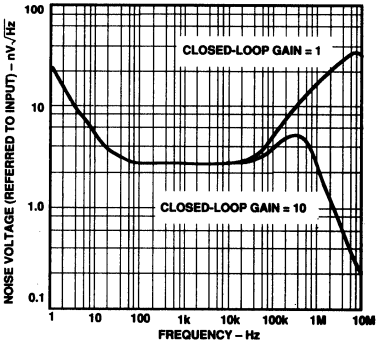


Figure 17. Input Noise Voltage Spectral Density

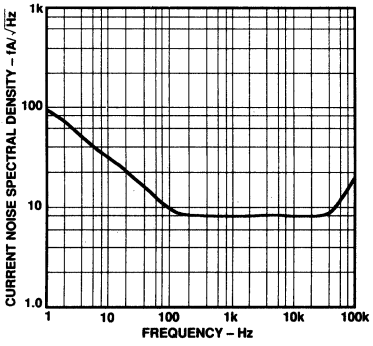


Figure 18. Input Noise Current Spectral Density

Typical Characteristics

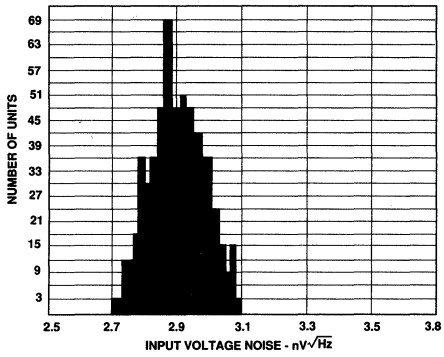


Figure 19. Typical Noise Distribution @ 10 kHz (602 Units)

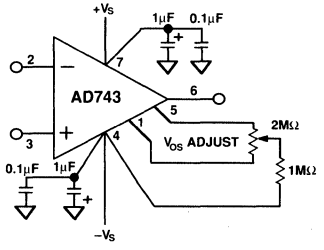


Figure 20. Offset Null Configuration

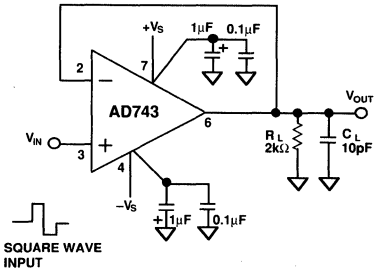


Figure 21. Unity-Gain Follower

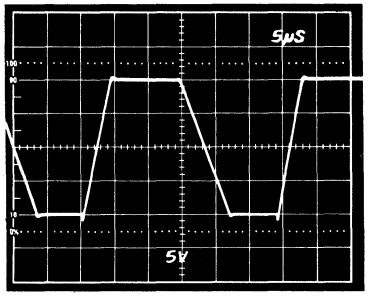


Figure 22a. Unity-Gain Follower Large Signal Pulse Response

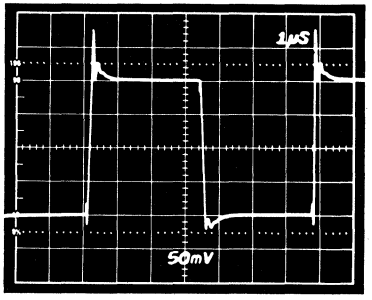


Figure 22b. Unity-Gain Follower Small Signal Pulse Response

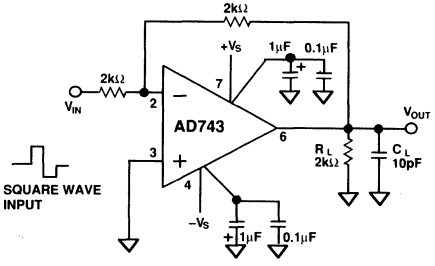


Figure 23a. Unity-Gain Inverter

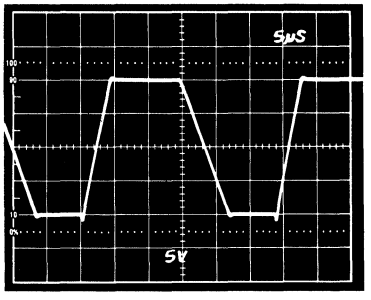


Figure 23b. Unity-Gain Inverter Large Signal Pulse Response

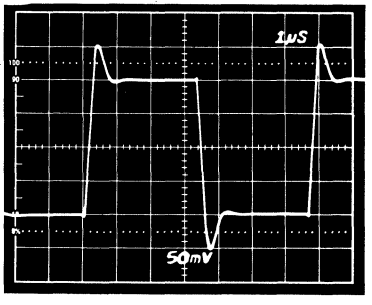


Figure 23c. Unity-Gain Inverter Small Signal Pulse Response

OP AMP PERFORMANCE: JFET VS. BIPOLAR

The AD743 is the first monolithic JFET op amp to offer the low input voltage noise of an industry-standard bipolar op amp without its inherent input current errors. This is demonstrated in Figure 24, which compares input voltage noise vs. input source resistance of the OP-27 and the AD743 op amps. From this figure, it is clear that at high source impedance the low current noise of the AD743 also provides lower total noise. It is also important to note that with the AD743 this noise reduction extends all the way down to low source impedances. The lower dc current errors of the AD743 also reduce errors due to offset and drift at high source impedances (Figure 25).

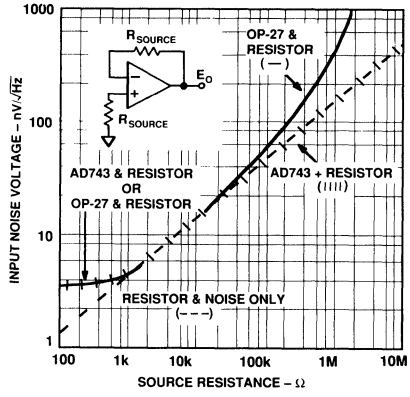


Figure 24. Total Input Noise Spectral Density @ 1 kHz vs. Source Resistance

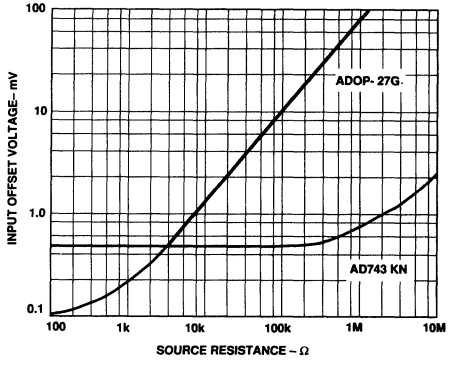


Figure 25. Input Offset Voltage vs. Source Resistance

DESIGNING CIRCUITS FOR LOW NOISE

An op amp's input voltage noise performance is typically divided into two regions: flatband and low frequency noise. The AD743 offers excellent performance with respect to both. The figure of 2.9 nV/$\sqrt{\text{Hz}}$ @ 10 kHz is excellent for a JFET input amplifier. The 0.1 to 10 Hz noise is typically 0.38 μV p-p. The user should pay careful attention to several design details in order to optimize low frequency noise performance. Random air currents can generate varying thermocouple voltages that appear as low frequency noise: therefore sensitive circuitry should be well shielded from air flow. Keeping absolute chip temperature low also reduces low frequency noise in two ways: first, the low frequency noise is strongly dependent on the ambient temperature and increases above +25°C. Secondly, since the gradient of temperature from the IC package to ambient is greater, the noise generated by random air currents, as previously mentioned, will be larger in magnitude. Chip temperature can be reduced both by operation at reduced supply voltages and by the use of a suitable clip-on heat sink, if possible.

Low frequency current noise can be computed from the magnitude of the dc bias current ($\tilde{I}_n = \sqrt{2qI_B\Delta f}$) and increases below approximately 100 Hz with a 1/f power spectral density. For the AD743 the typical value of current noise is 6.9 fA/$\sqrt{\text{Hz}}$ at 1 kHz. Using the formula, $\tilde{I}_n = \sqrt{4kT/R\Delta f}$, to compute the Johnson noise of a resistor, expressed as a current, one can see that the current noise of the AD743 is equivalent to that of a 3.45×10^8 Ω source resistance.

At high frequencies, the current noise of a FET increases proportionately to frequency. This noise is due to the "real" part of the gate input impedance, which decreases with frequency. This noise component usually is not important, since the voltage noise of the amplifier impressed upon its input capacitance is an apparent current noise of approximately the same magnitude.

In any FET input amplifier, the current noise of the internal bias circuitry can be coupled externally via the gate-to-source capacitances and appears as input current noise. This noise is totally correlated at the inputs, so source impedance matching will tend to cancel out its effect. Both input resistance and input capacitance should be balanced whenever dealing with source capacitances of less than 300 pF in value.

LOW NOISE CHARGE AMPLIFIERS

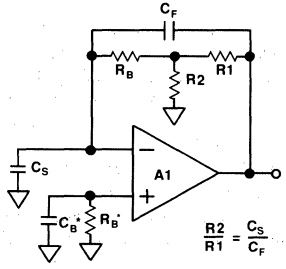
As stated, the AD743 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones. When dealing with a high source capacitance, it is useful to consider the total input charge uncertainty as a measure of system noise.

Charge (Q) is related to voltage and current by the simply stated fundamental relationships:

$$Q = CV \text{ and } I = \frac{dQ}{dt}$$

As shown, voltage, current and charge noise can all be directly related. The change in open circuit voltage (ΔV) on a capacitor will equal the combination of the change in charge (ΔQ/C) and the change in capacitance with a built in charge (Q/ΔC).

Figures 26 and 27 show two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier which has a very high input impedance, such as the AD743. Figure 26 shows a model of a charge amplifier circuit. Here, amplification depends on the principal of conservation of charge at the input of amplifier A1, which requires that the charge on capacitor C_S be transferred to capacitor C_F, thus yielding an output voltage of $\Delta Q/C_F$. The amplifiers input voltage noise will appear at the output amplified by the noise gain $(1 + (C_S/C_F))$ of the circuit.



*OPTIONAL, SEE TEXT

Figure 26. A Charge Amplifier Circuit

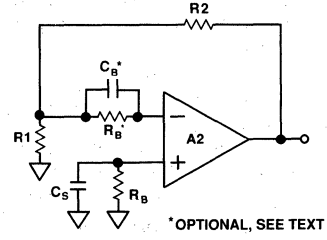


Figure 27. Model for a High Z Follower with Gain

The second circuit, Figure 27, is simply a high impedance follower with gain. Here the noise gain $(1 + (R1/R2))$ is the same as the gain to the voltage out of the transducer. Resistor R_B, in both circuits, is required as a dc bias current return.

There are three important sources of noise in these circuits. Amplifiers A1 and A2 contribute both voltage and current noise, while resistor R_B contributes a current noise of:

$$\widetilde{N} = \sqrt{4\,k\,\frac{T}{R_B}}\,\Delta f$$

where:

k = Boltzman's Constant = 1.381×10^{-23} Joules/Kelvin

T = Absolute Temperature, Kelvin (0°C = +273.2 Kelvin)

Δf = Bandwidth – in Hz (Assuming an Ideal "Brick Wall" Filter)

This must root-sum-square with the amplifier's own current noise.

Figure 28 shows that these two circuits have an identical frequency response and the same noise performance (provided that C_S/C_F = R1/R2). One feature of the first circuit is that a "T" network is used to increase the effective resistance of R_B and improve the low frequency cutoff point by the same factor.

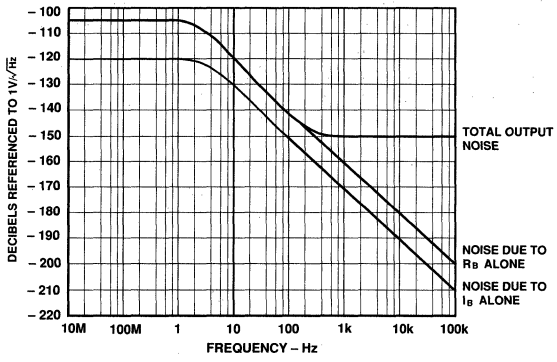


Figure 28. Noise at the Outputs of the Circuits of Figures 26 and 27. Gain = 10, C = 3000 pF, R_B = 22 MΩ

However, this does not change the noise contribution of R_B which, in this example, dominates at low frequencies. The graph of Figure 29 shows how to select an R_B large enough to minimize this resistor's contribution to overall circuit noise. When the equivalent current noise of R_B $((\sqrt{4kT})/R)$ equals the noise of I_B $(\sqrt{2qI_B})$, there is diminishing return in making R_B larger.

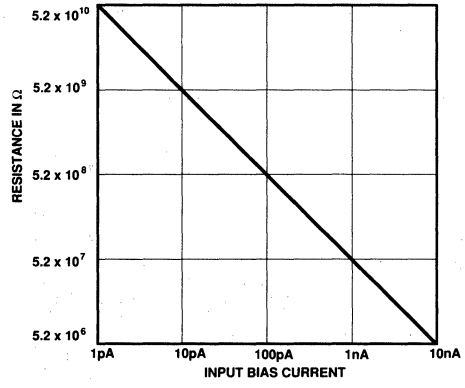


Figure 29. Graph of Resistance vs. Input Bias Current where the Equivalent Noise $\sqrt{4kT/R}$, Equals the Noise of the Bias Current $\sqrt{2qI_B}$

To maximize dc performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the optional resistor R_B in Figures 26 and 27. As previously mentioned, for best noise performance care should be taken to also balance the source capacitance designated by C_B. The value for C_B in Figure 26 would be equal to $C_F \parallel C_S$, in Figure 27). At values of C_B over 300 pF, there is a diminishing impact on noise; capacitor C_B can then be simply a large bypass of 0.01 μF or greater.

HOW CHIP PACKAGE TYPE AND POWER DISSIPATION AFFECT INPUT BIAS CURRENT

As with all JFET input amplifiers, the input bias current of the AD743 is a direct function of device junction temperature, I_B approximately doubling every 10°C. Figure 30 shows the relationship between bias current and junction temperature for the AD743. This graph shows that lowering the junction temperature will dramatically improve I_B.

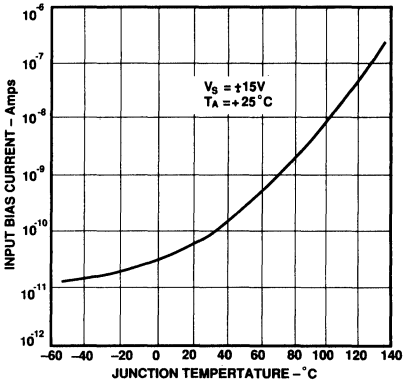
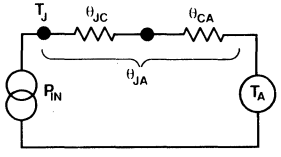


Figure 30. Input Bias Current vs. Junction Temperature

The dc thermal properties of an IC can be closely approximated by using the simple model of Figure 31 where current represents power dissipation, voltage represents temperature, and resistors represent thermal resistance (θ in °C/watt).



WHERE:
P_{IN} = DEVICE DISSIPATION
T_A = AMBIENT TEMPERATURE
T_J = JUNCTION TEMPERATURE
θ_{JC} = THERMAL RESISTANCE – JUNCTION TO CASE
θ_{CA} = THERMAL RESISTANCE – CASE TO AMBIENT

Figure 31. A Device Thermal Model

From this model $T_J = T_A + \theta_{JA}$ Pin. Therefore, I_B can be determined in a particular application by using Figure 30 together with the published data for θ_{JA} and power dissipation. The user can modify θ_{JA} by use of an appropriate clip-on heat sink such as the Aavid #5801. θ_{JA} is also a variable when using the AD743 in chip form. Figure 32 shows bias current vs. supply voltage with θ_{JA} as the third variable. This graph can be used to predict bias current after θ_{JA} has been computed. Again bias current will double for every 10°C. The designer using the AD743 in chip form (Figure 33) must also be concerned with both θ_{JC} and θ_{CA}, since θ_{JC} can be affected by the type of die mount technology used.

Typically, θ_{JC}'s will be in the 3°C to 5°C/watt range; therefore, for normal packages, this small power dissipation level may be ignored. But, with a large hybrid substrate, θ_{JC} will dominate proportionately more of the total θ_{JA}.

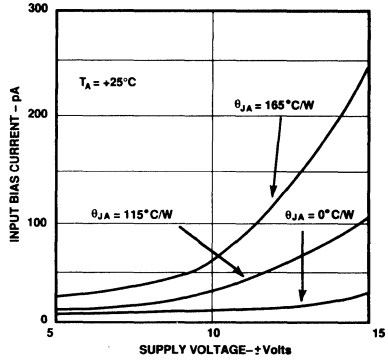


Figure 32. Input Bias Current vs. Supply Voltage for Various Values of θ_{JA}

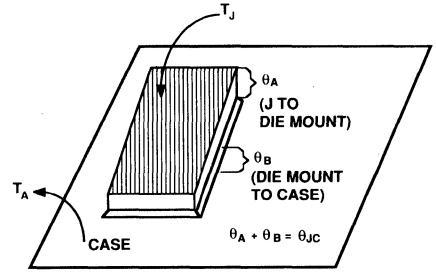
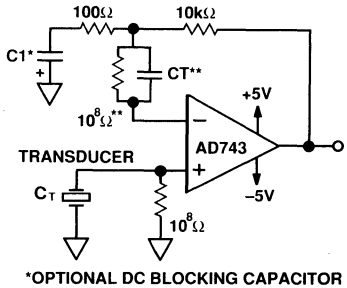


Figure 33. A Breakdown of Various Package Thermal Resistances

REDUCED POWER SUPPLY OPERATION FOR LOWER I_B

Reduced power supply operation lowers I_B in two ways: first, by lowering both the total power dissipation and second, by reducing the basic gate-to-junction leakage (Figure 32). Figure 34 shows a 40 dB gain piezoelectric transducer amplifier, which operates without an ac coupling capacitor, over the −40°C to +85°C temperature range. If the optional coupling capacitor is used, this circuit will operate over the entire −55°C to +125°C military temperature range.



*OPTIONAL DC BLOCKING CAPACITOR
**OPTIONAL, SEE TEXT

Figure 34. A Piezoelectric Transducer

AN INPUT-IMPEDANCE-COMPENSATED, SALLEN-KEY FILTER

The simple high pass filter of Figure 35 has an important source of error which is often overlooked. Even 5 pF of input capacitance in amplifier "A" will contribute an additional 1% of passband amplitude error, as well as distortion, proportional to the C/V characteristics of the input junction capacitance. The addition of the network designated "Z" will balance the source impedance—as seen by "A"—and thus eliminate these errors.

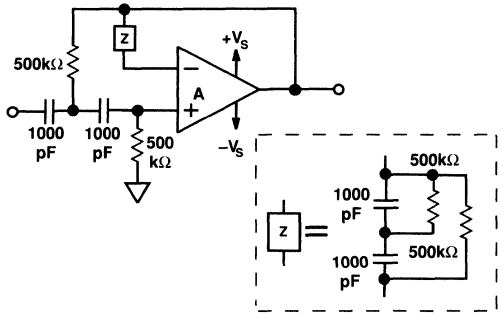


Figure 35. An Input Impedance Compensated Sallen-Key Filter

TWO HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

Two of the most popular charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output (pC/g).* Figures 36a and 36b show two ways in which to configure the AD743 as a low noise charge amplifier for use with a wide variety of piezoelectric accelerometers. The input sensitivity of these circuits will be determined by the value of capacitor C1 and is equal to:

$$\Delta V_{OUT} = \frac{\Delta Q_{OUT}}{C1}$$

The ratio of capacitor C1 to the internal capacitance (C_T) of the transducer determines the noise gain of this circuit ($1 + C_T/C1$). The amplifiers voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor R1. If a "T" network is used, the effective value is: R1 (1 + R2/R3).

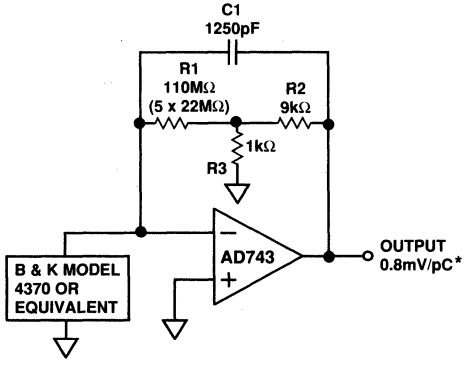


Figure 36a. A Basic Accelerometer Circuit

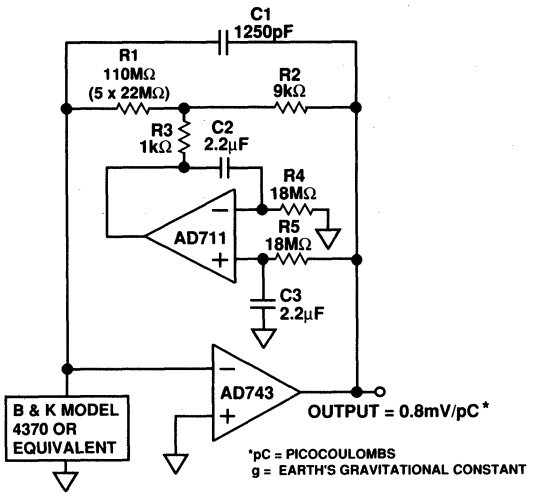


Figure 36b. An Accelerometer Circuit Employing a DC Servo Amplifier

A dc servo-loop (Figure 36b) can be used to assure a ≤10 mV dc output, without the need for a large compensating resistor when dealing with bias currents as large as 100 nA. For optimal low frequency performance, the time constant of the servo loop (R4C2 = R5C3) should be:

$$\text{Time Constant} \geq 10\, R1 \left(1 + \frac{R2}{R3}\right) C1$$

A LOW NOISE HYDROPHONE AMPLIFIER

Hyrophones are usually calibrated into the voltage-out mode. The circuits of Figures 37a and 37b can be used to amplify the output of a typical hydrophone. Figure 37a shows a typical dc coupled circuit. The optional resistor and capacitor serve to counteract the dc offset caused by bias currents flowing through resistor R1. Figure 37b, a variation of the original circuit, has a low frequency cutoff determined by an RC time constant equal to:

$$\text{Time Constant} = \frac{1}{2\pi \times C_C \times 100\ \Omega}$$

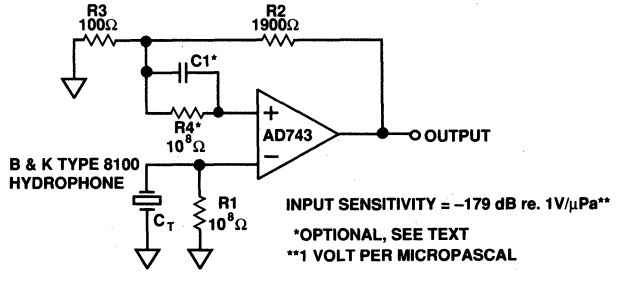


Figure 37a. A Basic Hydrophone Amplifier

*pC = Picocoulombs
g = Earth's Gravitational Constant

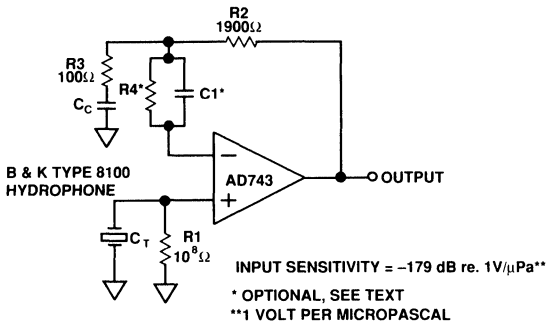


Figure 37b. An AC-Coupled, Low Noise Hydrophone Amplifier

Where the dc gain is 1 and the gain above the low frequency cutoff ($1/(2\pi C_C(100\ \Omega))$) is the same as the circuit of Figure 37a. The circuit of Figure 37c uses a dc servo loop to keep the dc output at 0 V and to maintain full dynamic range for I_B's up to 100 nA. The time constant of R7 and C2 should be larger than that of R1 and C_T for a smooth low frequency response.

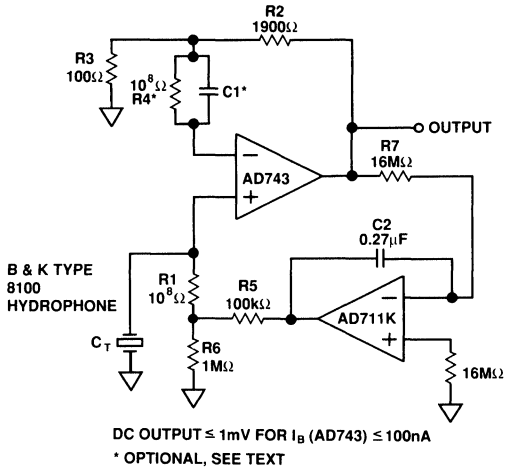


Figure 37c. A Hydrophone Amplifier Incorporating a DC Servo Loop

The transducer shown has a source capacitance of 7500 pF. For smaller transducer capacitances (≤300 pF), lowest noise can be achieved by adding a parallel RC network (R4 = R1, C1 = C_T) in series with the inverting input of the AD743.

Precision, 500ns Settling BiFET Op Amp

AD744

FEATURES

AC PERFORMANCE

- 500ns Settling to 0.01% for 10V Step
- 1.5μs Settling to 0.0025% for 10V Step
- 75V/μs Slew Rate
- 0.0003% Total Harmonic Distortion (THD)
- 13MHz Gain Bandwidth – Internal Compensation
- >200MHz Gain Bandwidth (G=1000) External Decompensation
- >1000pF Capacitive Load Drive Capability with 10V/μs Slew Rate – External Compensation

DC PERFORMANCE

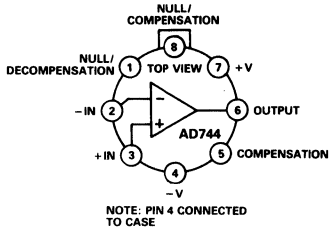
- 0.25mV max Offset Voltage (AD744C)
- 3μV/°C max Drift (AD744C)
- 250V/mV min Open-Loop Gain (AD744B)
- 4μV p-p max Noise, 0.1Hz to 10Hz (AD744C)
- Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form
- MIL-STD-883B Processing Available
- Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA–481A Standard

APPLICATIONS

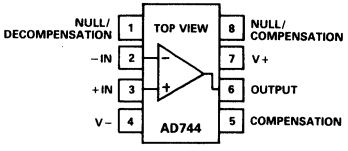
- Output Buffers for 12-Bit, 14-Bit and 16-Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters

AD744 CONNECTION DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N), Small Outline (R) and Cerdip (Q) Packages



PRODUCT DESCRIPTION

The AD744 is a fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD744 also offers the option of using custom compensation to achieve exceptional capacitive load drive capability.

The single-pole response of the AD744 provides fast settling: 500ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD744's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

The AD744 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater. External compensation may be applied to the AD744 for stable operation as a unity gain follower. External compensation also allows the AD744 to drive 1000pF capacitive loads, slewing at 10V/μs with full stability. Alternatively, external decompensation may be used to increase the gain bandwidth of the AD744 to over 200MHz at high gains. This makes the AD744 ideal for use as ac preamps in digital signal processing (DSP) front ends.

The AD744 is available in seven performance grades. The AD744J and AD744K are rated over the commercial temperature range of 0 to +70°C. The AD744A, AD744B and AD744C are rated over the industrial temperature range of −40°C to +85°C. The AD744S and AD744T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes a 168-hour burn-in, as well as other environmental and physical tests.

The AD744 is available in an 8-pin plastic mini-DIP, 8-pin small outline, 8-pin cerdip or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD744 is a high-speed BiFET op amp that offers excellent performance at competitive prices. It outperforms the OP42/44, OPA602/606, LF356 and LF400.
2. The AD744 offers exceptional dynamic response. It settles to 0.01% in 500ns and has a 100% tested minimum slew rate of 50V/μs (AD744B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.
4. The AD744 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1Hz to 10Hz (AD744C).

SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD744J/A/S Min	AD744J/A/S Typ	AD744J/A/S Max	AD744K/B/T Min	AD744K/B/T Typ	AD744K/B/T Max	AD744C Min	AD744C Typ	AD744C Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.3	**1.0**		0.25	**0.5**		0.10	**0.25**	mV
Offset	$T_{min}-T_{max}$			2/2/2			**1.0**			**0.45**	mV
vs. Temp			5	20/20/20		5	**10**		2	**3**	μV/°C
vs. Supply[2]		**82**	95		**88**	100		**92**	110		dB
vs. Supply	$T_{min}-T_{max}$	82/82/82			**88**			**92**			dB
Long-Term Stability			15			15			15		μV/month
INPUT BIAS CURRENT[3]											
Either Input	$V_{CM}=0V$		30	**100**		30	**100**		30	**50**	pA
Either Input @T_{max} =	$V_{CM}=0V$										
J, K	70°C		0.7	2.3		0.7	2.3				nA
A, B, C	85°C		1.9	6.4		1.9	6.4		1.9	3.2	nA
S, T	125°C		31	102		31	102				nA
Either Input	$V_{CM}=+10V$		40	150		40	**150**		40	**100**	pA
Offset Current	$V_{CM}=0V$		20	**50**		10	**50**		10	**20**	pA
Offset Current @T_{max} =	$V_{CM}=0V$										
J, K	70°C		0.4	1.1		0.2	1.1				nA
A, B, C	85°C		1.3	3.2		0.6	3.2		0.6	1.3	nA
S, T	125°C		20	52		10	52				nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	$G=-1$	8	13		9	13		9	13		MHz
Full Power Response	$V_O=20V$ p-p		1.2			1.2			1.2		MHz
Slew Rate, Unity Gain	$G=-1$	**45**	75		**50**	75		**50**	75		V/μs
Settling Time to 0.01%[4]	$G=-1$		0.5	0.75		0.5	0.75		0.5	0.75	μs
Total Harmonic	$f=1kHz$										
Distortion	$R1\geq 2k\Omega$										
	$V_O=3V$ rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω‖pF
Common Mode			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		V
Over Max Operating Range[6]		**−11**		**+13**	**−11**		**+13**	**−11**		**+13**	V
Common-Mode Rejection Ratio	$V_{CM}=\pm10V$	**78**	88		**82**	88		**86**	94		dB
	T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
	$V_{CM}=\pm11V$	**72**	84		**78**	84		**80**	90		dB
	T_{min} to T_{max}	70/70/**70**	80		**74**	80		**76**	84		dB
INPUT VOLTAGE NOISE	0.1 to 10Hz		2			2			2	**4**	μV p-p
	$f=10Hz$		45			45			45		nV/√Hz
	$f=100Hz$		22			22			22		nV/√Hz
	$f=1kHz$		18			18			18		nV/√Hz
	$f=10kHz$		16			16			16		nV/√Hz
INPUT CURRENT NOISE	$f=1kHz$		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN[7]	$V_O=\pm10V$										
	$R_{LOAD}\geq 2k\Omega$	**200**	400		**250**	400		**250**	400		V/mV
	T_{min} to T_{max}	100/100/**100**			**100**			**150**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq 2k\Omega$	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
	T_{min} to T_{max}	±12/±12/**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Current	Short-Circuit		25			25			25		mA
Capacitive Load[8]	Gain = −1			**1000**			**1000**			**1000**	pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			3.5	**5.0**		3.5	**4.0**		3.5	**4.0**	mA
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD744J			AD744K					
Industrial (−40°C to +85°C)			AD744A			AD744B			AD744C		
Military (−55°C to +125°C)			AD744S			AD744T					
PACKAGE OPTIONS[9]											
8-Pin Plastic Mini-DIP (N-8) and SOIC (R-8)			AD744JN, AD744JR			AD744KN, AD744KR					
8-Pin Cerdip (Q-8)			AD744AQ, AD744SQ			AD744BQ, AD744TQ			AD744CQ		
TO-99 Metal Can (H-08A)			AD744AH, AD744SH			AD744BH, AD744TH			AD744CH		
Tape and Reel			AD744JR-REEL			AD744KR-REEL					
J and S Grade Chips Also Available											

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A=+25°C$.

[2]PSRR test conditions: $+V_S=15V$, $-V_S=12V$ to 18V and $+V_S=12V$ to 18V, $-V_S=-15V$.

[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A=+25°C$. For higher temperature, the current doubles every 10°C.

[4]Gain = −1, $R_L=2k$, $C_L=10pF$, refer to Figure 25.

[5]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[6]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.

[7]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[8]Capacitive load drive specified for $C_{COMP}=20pF$ with the device connected as shown in Figure 32. Under these conditions, slew rate = 14V/μs and 0.01% settling time = 1.5μs typical. Refer to Table II for optimum compensation while driving a capacitive load.

[9]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q, H	−65°C to +150°C
Storage Temperature Range N, R	−65°C to +125°C
Operating Temperature Range	
AD744J/K	0 to +70°C
AD744A/B/C	−40°C to +85°C
AD744S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indited in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics

8-Pin Plastic Package: $\theta_{JA} = 90°C/W$

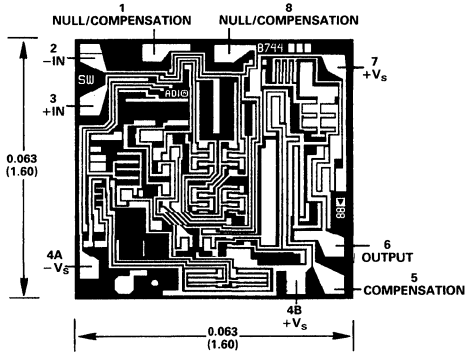
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W, \theta_{JA} = 110°C/W$

8-Pin Metal Can Package: $\theta_{JC} = 65°C/W, \theta_{JA} = 150°C/W$

[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics

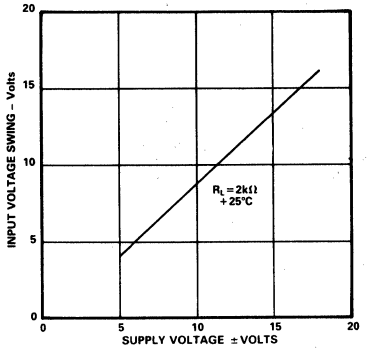


Figure 1. Input Voltage Swing vs. Supply Voltage

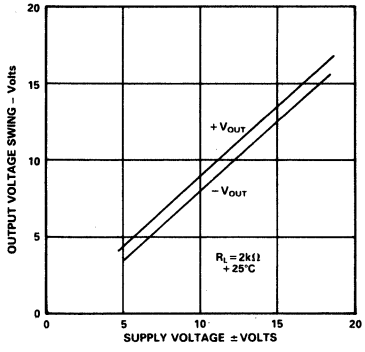


Figure 2. Output Voltage Swing vs. Supply Voltage

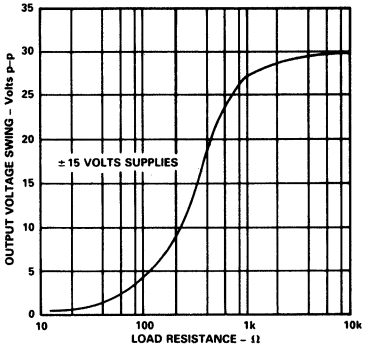


Figure 3. Output Voltage Swing vs. Load Resistance

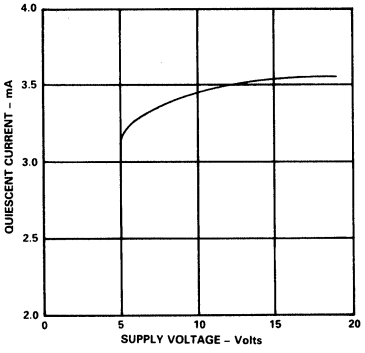


Figure 4. Quiescent Current vs. Supply Voltage

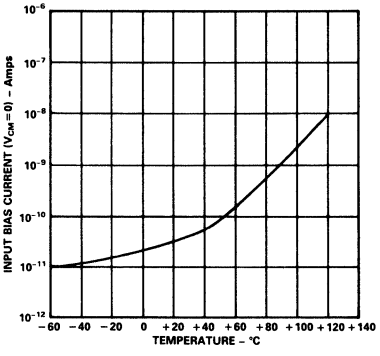


Figure 5. Input Bias Current vs. Temperature

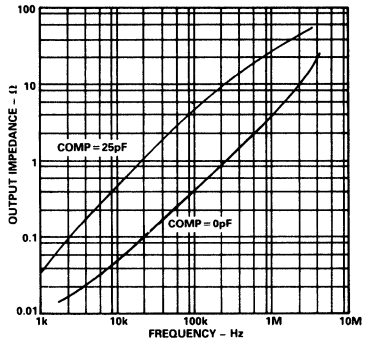


Figure 6. Output Impedance vs. Frequency

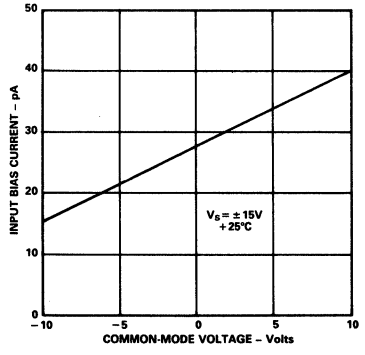


Figure 7. Input Bias Current vs. Common-Mode Voltage

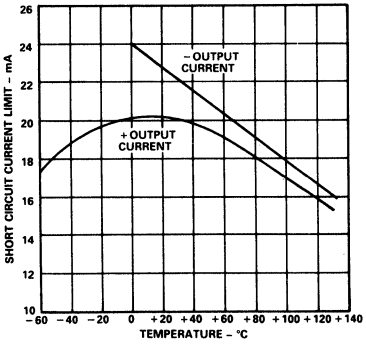


Figure 8. Short Circuit Current Limit vs. Temperature

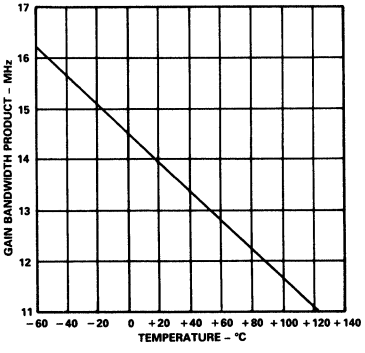


Figure 9. Gain Bandwidth Product vs. Temperature

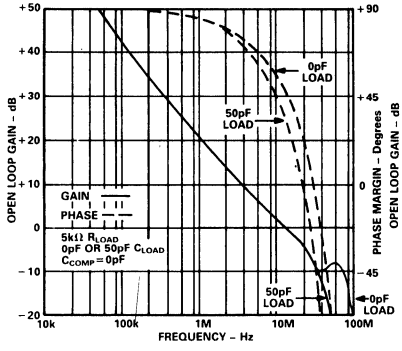


Figure 10. Open Loop Gain and Phase Margin vs. Frequency C_{COMP} = 0pF

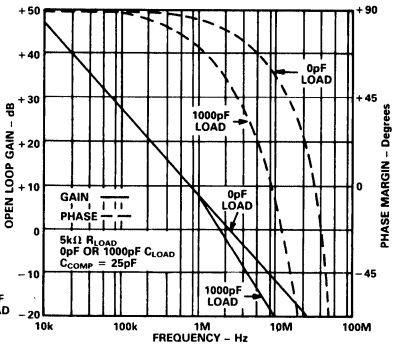


Figure 11. Open Loop Gain and Phase Margin vs. Frequency C_{COMP} = 25pF

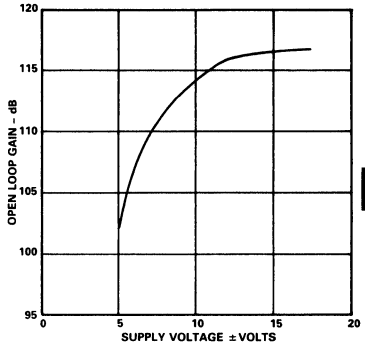


Figure 12. Open Loop Gain vs. Supply Voltage

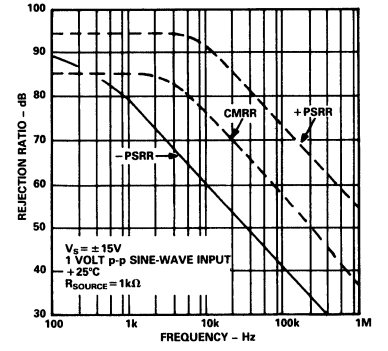


Figure 13. Common-Mode and Power Supply Rejection vs. Frequency

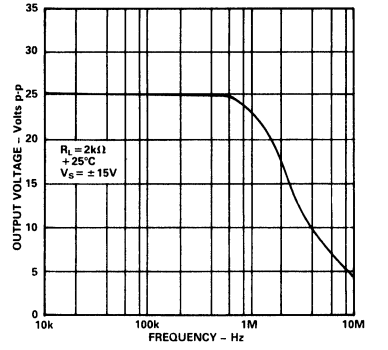


Figure 14. Large Signal Frequency Response

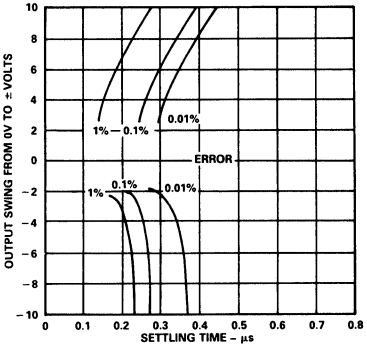


Figure 15. Output Swing and Error vs. Settling Time

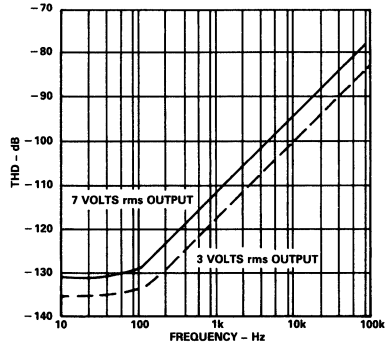


Figure 16. Total Harmonic Distortion vs. Frequency, Circuit of Figure 20 (G = 10)

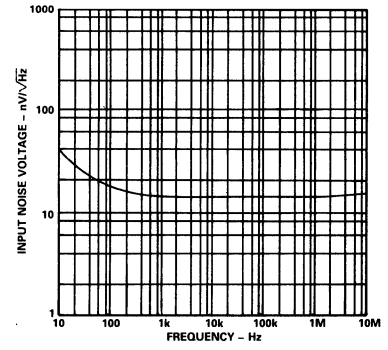


Figure 17. Input Noise Voltage Spectral Density

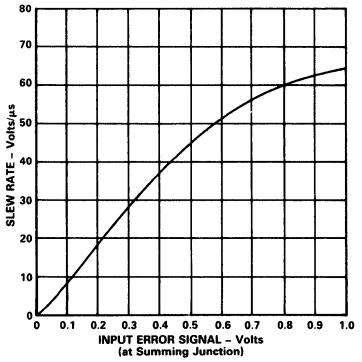


Figure 18. Slew Rate vs. Input Error Signal

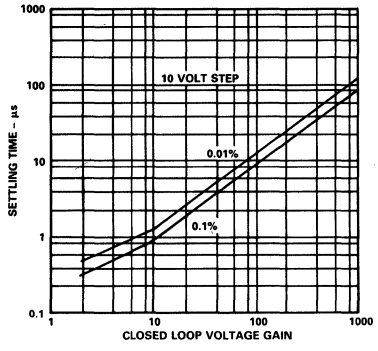


Figure 19. Settling Time vs. Closed Loop Voltage Gain

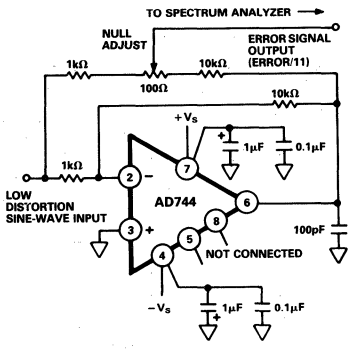


Figure 20. THD Test Circuit

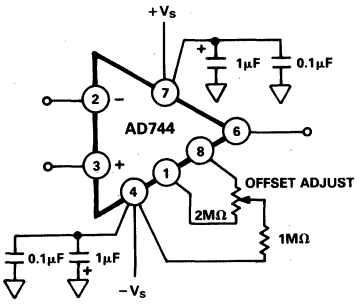


Figure 21. Offset Null Configuration

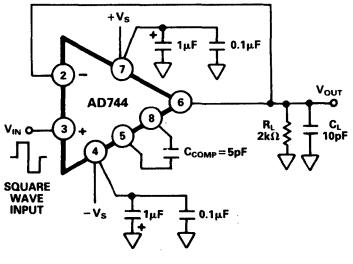


Figure 22a. Unity Gain Follower

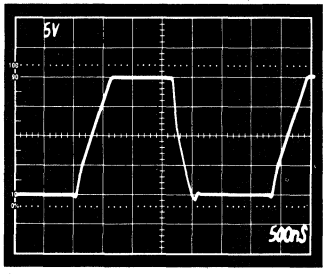


Figure 22b. Unity Gain Follower Large Signal Pulse Response, C_{COMP} = 5pF

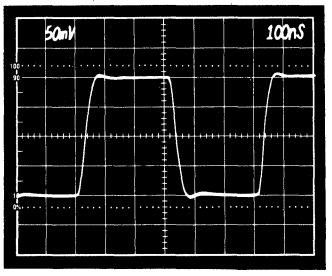


Figure 22c. Unity Gain Follower Small Signal Pulse Response, C_{COMP} = 5pF

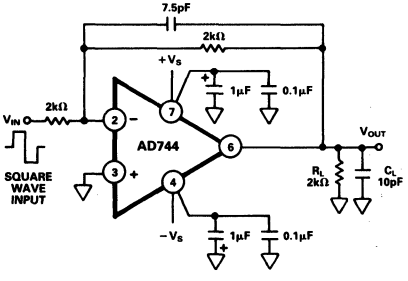


Figure 23a. Unity Gain Inverter

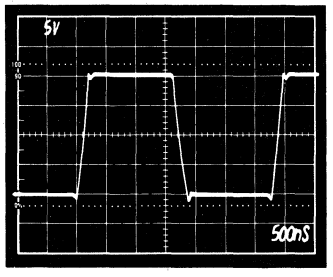


Figure 23b. Unity Gain Inverter Large Signal Pulse Response, C_{COMP} = 0pF

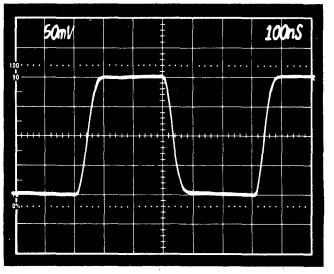


Figure 23c. Unity Gain Inverter Small Signal Pulse Response, C_{COMP} = 0pF

POWER SUPPLY BYPASSING

The power supply connections to the AD744 must maintain a low impedance to ground over a bandwidth of 10MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1μF ceramic and a 1μF electrolytic capacitor as shown in Figure 24 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1μF should be used for any application.

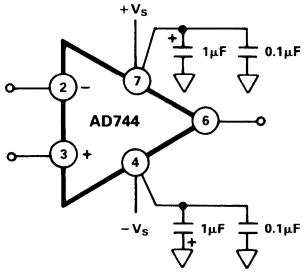


Figure 24. Recommended Power Supply Bypassing

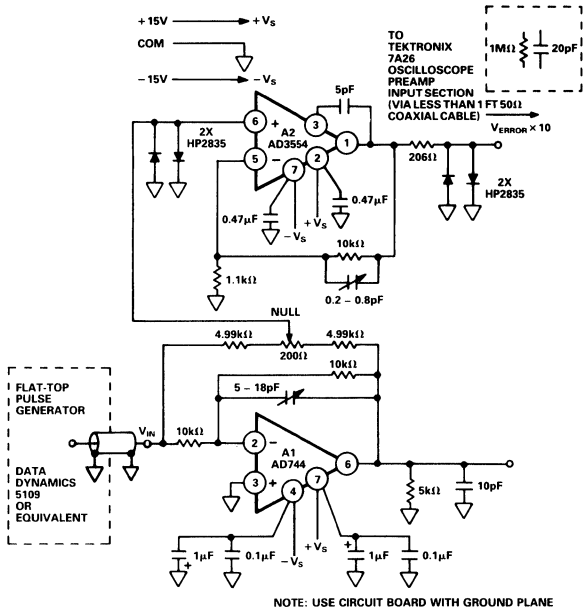


Figure 25. Settling Time Test Circuit

MEASURING AD744 SETTLING TIME

The photos of Figures 26 and 27 show the dynamic response of the AD744 while operating in the settling time test circuit of Figure 25. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD744 under test, is clamped, amplified by op amp A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was carefully chosen because it recovers from the approximately 0.4V overload quickly enough to allow accurate measurement of the AD744's 500ns settling time. Amplifier A2 is a very high-speed FET-input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD744 under test.

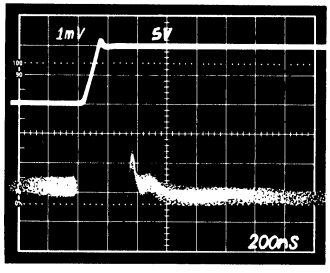


Figure 26. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD744 Under Test (5V/div.)
Lower Trace: Amplified Error Voltage (0.01%/div.)

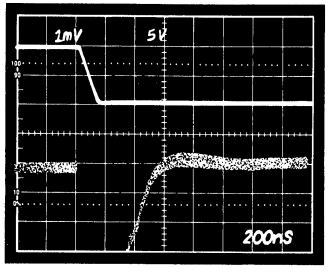


Figure 27. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD744 Under Test (5V/div.)
Lower Trace: Amplified Error Voltage (0.01%/div.)

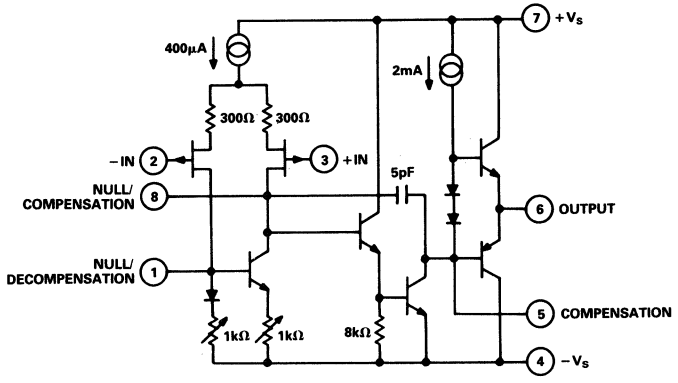


Figure 28. AD744 Simplified Schematic

EXTERNAL FREQUENCY COMPENSATION

Even though the AD744 is useable without compensation in most applications, it may be externally compensated for even more flexibility. This is accomplished by connecting a capacitor between Pins 5 and 8. Figure 28, a simplified schematic of the AD744, shows where this capacitor is connected. This feature is useful because it allows the AD744 to be used as a unity gain voltage follower. It also enables the amplifier to drive capacitive loads up to 2000pF and greater.

The slew rate and gain bandwidth product of the AD744 are inversely proportional to the value of the compensation capacitor, C_{COMP}. Therefore, when trying to maximize the speed of the amplifier, the value of C_{COMP} should be minimized. C_{COMP} can also be used to slow the amplifier to a point where the slew rate is perfectly symmetrical and well controlled. Figure 29 summarizes the effect of external compensation on slew rate and bandwidth.

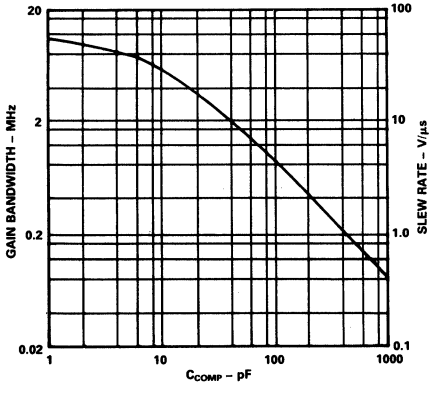


Figure 29. Gain Bandwidth and Slew Rate vs. C_{COMP}

The following section provides tables to show what C_{COMP} values will provide the necessary compensation for given circuit configurations and capacitive loads. In each case, the recommended C_{COMP} is a minimum value. A larger C_{COMP} can always be used, but slew rate and bandwidth performance will be degraded.

Figure 30 shows the AD744 configured as a unity gain voltage follower. In this case, a minimum compensation capacitor of 5pF is necessary for stable operation. Larger compensation capacitors can be used for driving larger capacitive loads. Table I outlines recommended minimum values for C_{COMP} based on the desired capacitive load. It also gives the slew rate and bandwidth that will be achieved for each case.

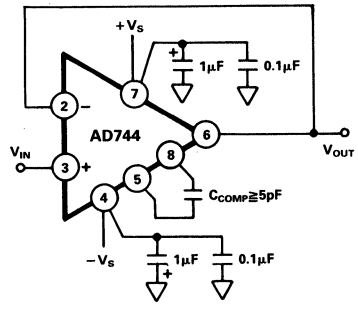


Figure 30. AD744 Connected as a Unity Gain Voltage Follower

Gain	Max C_{LOAD} (pF)	C_{COMP} (pF)	Slew Rate (V/μs)	−3dB Bandwidth (MHz)
1	50	5	37	6.5
1	150	10	25	4.3
1	2000	25	12.5	2.0

Table I. Recommended Values of C_{COMP} vs. Various Capacitive Loads

Figures 31 and 32 show the AD744 as a voltage follower with gain and as an inverting amplifier. In these cases, external compensation is not necessary for stable operation. However, compensation may be applied to drive capacitive loads above 50pF. Table II gives recommended C_{COMP} values, along with expected slew rates and bandwidths for a variety of load conditions and gains for the circuits in Figures 31 and 32.

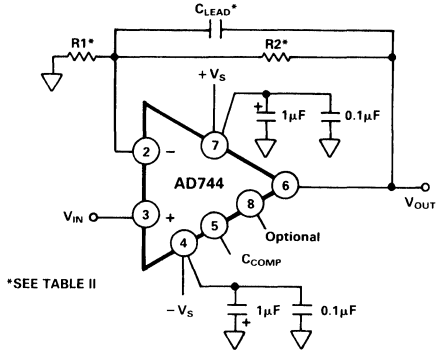


Figure 31. AD744 Connected as a Voltage Follower Operating at Gains of 2 or Greater

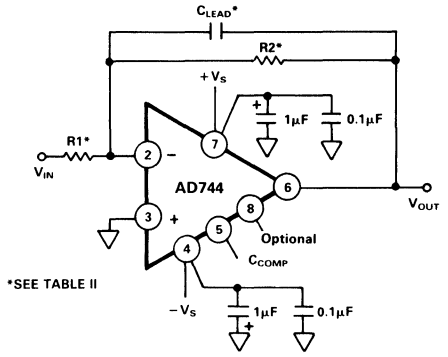


Figure 32. AD744 Connected as an Inverting Amplifier Operating at Gains of 1 or Greater

R1 (Ω)	R2 (Ω)	Gain Follower	Gain Inverter	Max C_{LOAD} (pF)	C_{COMP} (pF)	C_{LEAD} (pF)	Slew Rate (V/μs)	−3dB Bandwidth (MHz)
4.99k	4.99k	2	1	50	0	7	75	2.5**
4.99k	4.99k	2	1	150	5	7	37	2.3**
4.99k	4.99k	2	1	1000	20	–	14	1.2
4.99k	4.99k	2	1	>2000	25	–	12.5*	1.0
499Ω	4.99k	11	10	270	0	–	75	1.2
499Ω	4.99k	11	10	390	2	–	50	0.85
499Ω	4.99k	11	10	1000	5	–	37*	0.60

*Into large capacitive loads the AD744's 25mA output current limit sets the slew rate of the amplifier, in V/μs, equal to 0.025 amps divided by the value of C_{LOAD} in μF. Slew rate is specified into rated max C_{LOAD} except for cases marked *, which are specified with a 50pF load.
**Bandwidth with C_{LEAD} adjusted for minimum settling time.

Table II. Recommended Values of C_{COMP} vs. Various Load Conditions for the Circuits of Figures 31 and 32.

Using Decompensation to Extend the Gain Bandwidth Product

When the AD744 is used in applications where the closed-loop gain is greater than 10, gain bandwidth product may be enhanced by connecting a small capacitor between Pins 1 and 5 (Figure 33). At low frequencies, this capacitor cancels the effects of the chip's internal compensation capacitor, C_{COMP}, effectively decompensating the amplifier.

Due to manufacturing variations in the value of the internal C_{COMP}, it is recommended that the amplifier's response be optimized for the desired gain by using a 2 to 10pF trimmer capacitor rather than using a fixed value.

R1 (Ω)	R2 (Ω)	Gain Follower	Gain Inverter	−3dB Bandwidth	Gain/BW Product
1k	10k	11	10	2.5MHz	25MHz
100	10k	101	100	760kHz	76MHz
100	100k	1001	1000	225kHz	225MHz

Table III. Performance Summary for the Circuit of Figure 33

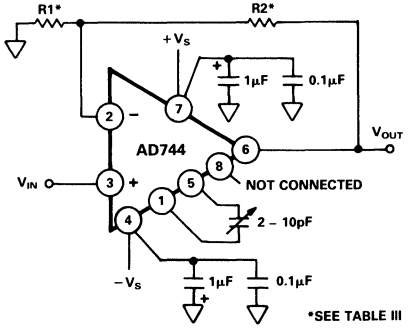


Figure 33. Using the Decompensation Connection to Extend Gain Bandwidth

HIGH-SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

Digital-to-analog converters which use bipolar transistors to switch currents into (or out of) their outputs can achieve very fast settling times. The AD565A, for example, is specified to settle to 12 bits in less than 250ns, with a current output. However, in many applications, a voltage output is desirable, and it would be useful – perhaps essential – that this I-to-V conversion be accomplished without increasing the settling time or without degrading the accuracy of the DAC.

Figure 34 is a schematic of an AD565A DAC using an AD744 output buffer. The 10pF C_{LEAD} capacitor compensates for the DAC's output capacitance, plus the 5.5pF amplifier input capacitance.

Figure 35 is an oscilloscope photo of the AD744's output voltage with a +10V to 0V step applied; this corresponds to an all "1s" to all "0s" code change on the DAC. Since the DAC is connected in the 20V span mode, 1LSB is equal to 4.88mV. Output settling time for the AD565/AD744 combination is less than 500ns to within a 2.44mV, 1/2LSB error band.

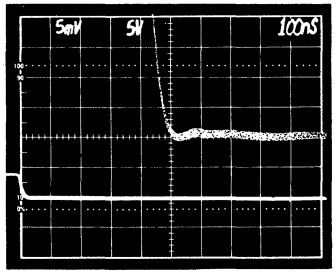


Figure 35. Upper Trace: AD744 Output Voltage for a +10V to 0V Step, Scale: 5mV/div.
Lower Trace: Logic Input Signal, Scale: 5V/div.

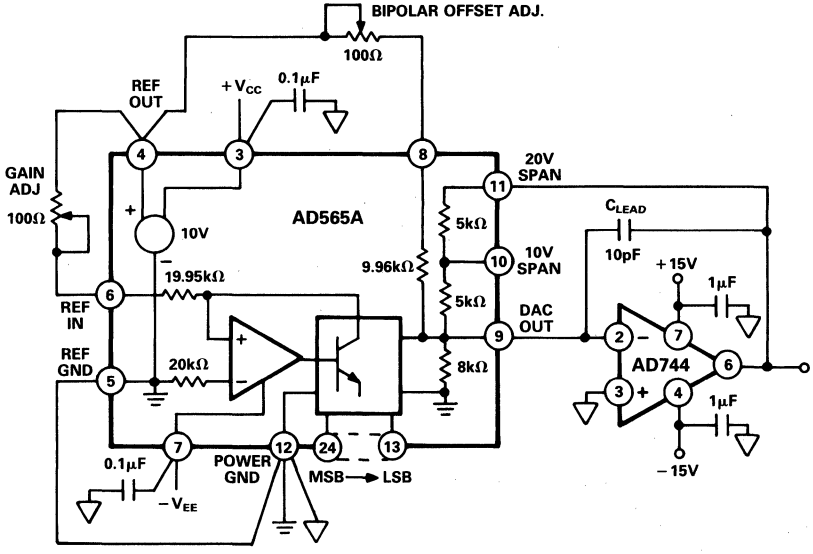


Figure 34. ±10V Voltage Output Bipolar DAC Using the AD744 as an Output Buffer

A HIGH-SPEED, 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 36 can provide a range of gains from unity up to 1000 and higher. The circuit bandwidth is 4MHz at a gain of 1 and 750kHz at a gain of 10; settling time for the entire circuit is less than 2μs to within 0.01% for a 10V step, (G = 10).

While the AD744 is not stable with 100% negative feedback (as when connected as a standard voltage follower), phase margin and therefore stability at unity gain may be increased to an acceptable level by placing the parallel combination of a resistor and a small lead capacitor between each amplifier's output and its inverting input terminal.

The only penalty associated with this method is a small bandwidth reduction at low gains. The optimum value for C_{LEAD} may be determined from the graph of Figure 41. This technique can be used in the circuit of Figure 36 to achieve stable operation at gains from unity to over 1000.

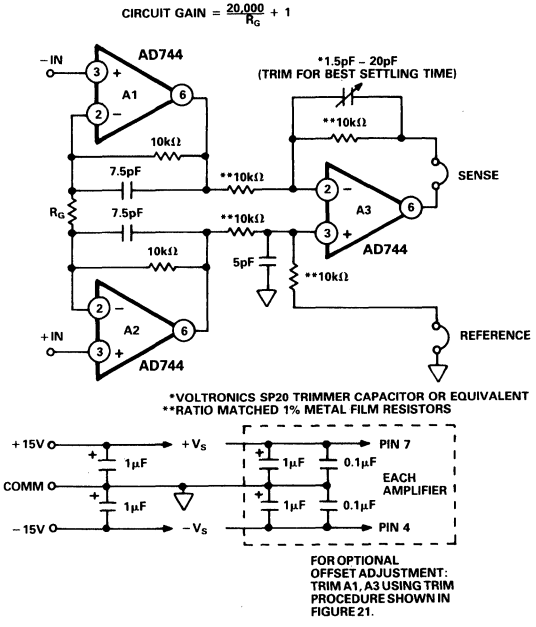


Figure 36. A High Performance, 3 Op Amp Instrumentation Amplifier Circuit

Gain	R_G	Bandwidth	T Settle (0.01%)
1	NC	3.5MHz	1.5μs
2	20kΩ	2.5MHz	1.0μs
10	2.22kΩ	1MHz	2μs
100	202Ω	290kHz	5μs

Table IV. Performance Summary for the 3 Op Amp Instrumentation Amplifier Circuit

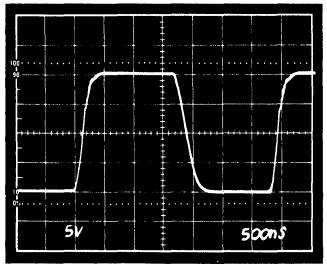


Figure 37. The Pulse Response of the 3 Op Amp Instrumentation Amplifier. Gain = 1, Horizontal Scale: 0.5μV/div., Vertical Scale: 5V/div. (Gain = 10)

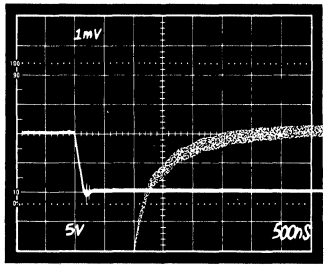


Figure 38. Settling Time of the 3 Op Amp Instrumentation Amplifier. Horizontal Scale: 500ns/div., Vertical Scale, Pulse Input: 5V/div., Output Settling: 1mV/div.

Minimizing Settling Time in Real-World Applications

An amplifier with a "single pole" or "ideal" integrator open-loop frequency response will achieve the minimum possible settling time for any given unity-gain bandwidth. However, when this "ideal" amplifier is used in a practical circuit, the actual settling time is increased above the minimum value because of added time constants which are introduced due to additional capacitance on the amplifier's summing junction. The following discussion will explain how to minimize this increase in settling time by the selection of the proper value for feedback capacitor, C_L.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency, f_O, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 39. This circuit models an op amp connected as an I-to-V converter.

Equation 1 would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects. Even considering these effects, the fine scale settling to <0.1% will be determined by the op amp's small signal behavior.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R\,(C_L+C_X)}{2\pi F_O}\,s^2 + \left(\frac{G_N}{2\pi F_O} + R\,C_L\right)s + 1}$$

Where F_O = the op amp's unity gain crossover frequency

G_N = the "noise" gain of the circuit $\left(1+\frac{R}{R_O}\right)$

This Equation May Then Be Solved for C_L:

Equation 2.

$$C_L = \frac{2 - G_N}{R\,2\pi F_O} + \frac{2\sqrt{RC_X\,2\pi F_O + (1-G_N)}}{R\,2\pi F_O}$$

In these equations, capacitance C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling an I-to-V converter application, the Norton equivalent circuit of Figure 39 can be used directly. Capacitance C_X is the total capacitance of the output of the current source plus the input capacitance of the op amp, which includes any stray capacitance at the op amp's input.

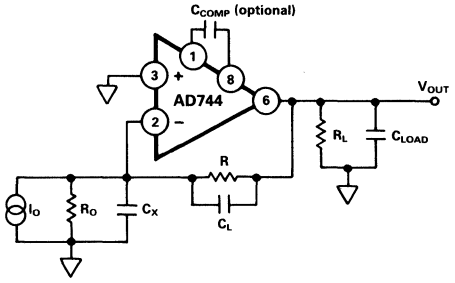


Figure 39. A Simplified Model of the AD744 Used as a Current-to-Voltage Converter

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier model of Figure 40 is created. Here capacitor C_X represents the input capacitance of the AD744 (5.5pF) plus any stray capacitance due to wiring and the type of IC package employed.

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp's output. If the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose the correct value for a small capacitor, C_L, which will optimize amplifier response. If the value of C_X is not known, C_L should be a variable capacitor.

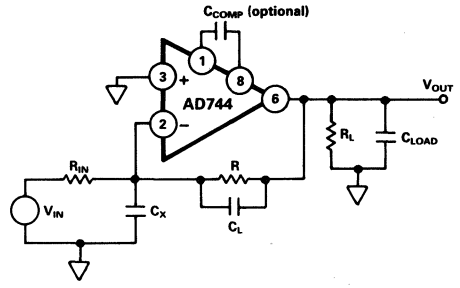


Figure 40. A Simplified Model of the AD744 Used as an Inverting Amplifier

As an aid to the designer, the optimum value of C_L for one specific amplifier connection can be determined from the graph of Figure 41. This graph has been produced for the case where the AD744 is connected as in Figures 39 and 40 with a practical minimum value for C_{STRAY} of 2pF and a total C_X value of 7.5pF.

The approximate value of C_L can be determined for almost any application by solving Equation 2. For example, the AD565/AD744 circuit of Figure 34 constrains all the variables of Equation 2 ($G_N = 3.25$, $R = 10k\Omega$, $F_O = 13MHz$, and $C_X = 32.5pF$). Therefore, under these conditions, $C_L = 10.5pF$.

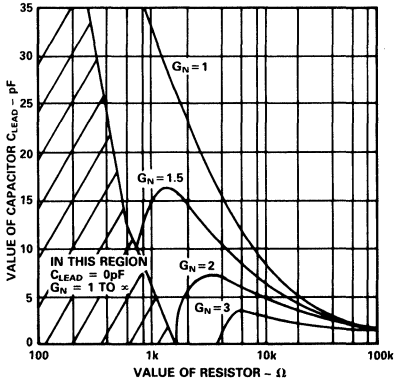


Figure 41. Practical Values of C_L vs. Resistance of R for Various Amplifier Noise Gains

Dual Precision, 500 ns Settling, BiFET Op Amp

AD746

FEATURES

AC PERFORMANCE
- 500 ns Settling to 0.01% for 10 V Step
- 75 V/μs Slew Rate
- 0.0001% Total Harmonic Distortion (THD)
- 13 MHz Gain Bandwidth
- Internal Compensation for Gains of +2 or Greater

DC PERFORMANCE
- 0.5 mV max Offset Voltage (AD746B)
- 10 μV/°C max Drift (AD746B)
- 175 V/mV min Open Loop Gain (AD746B)
- 2 μV p–p Noise, 0.1 Hz to 10 Hz
- Available in Plastic Mini-DIP, Cerdip and Surface Mount Packages
- MIL-STD-883B Processing Available
- Single Version Available: AD744

APPLICATIONS
- Dual Output Buffers for 12- and 14-Bit DACs
- Input Buffers for Precision ADCs, Wideband Preamplifiers and Low Distortion Audio Circuitry

PRODUCT DESCRIPTION

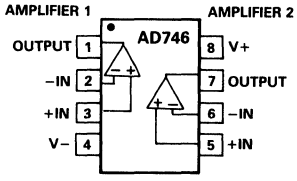
The AD746 is a dual operational amplifier, consisting of two AD744 BiFET op amps on a single chip. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates and ample bandwidths. In addition, the AD746 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

The single pole response of the AD746 provides fast settling: 500 ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. Furthermore, the AD746's low total harmonic distortion (THD) level of 0.0001% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

The AD746 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of 2 or greater. It is available in four performance grades. The AD746J is rated over the commercial temperature range of 0 to +70°C. The AD746A and AD746B are rated over the industrial temperature range of −40°C to +85°C. The AD746S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

AD746 CONNECTION DIAGRAM

Plastic Mini-DIP (N)
Cerdip (Q) and
Plastic SOIC (R) Packages



The AD746 is available in three 8-pin packages: plastic mini-DIP, hermetic cerdip and surface mount (SO).

PRODUCT HIGHLIGHTS

1. The AD746 offers exceptional dynamic response for high speed data acquisition systems. It settles to 0.01% in 500 ns and has a 100% tested minimum slew rate of 50 V/μs (AD746B).
2. Outstanding dc precision is provided by a combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
3. Differential and multichannel systems will benefit from the AD746's very close matching of ac characteristics. Input offset voltage specs are fully tested and guaranteed to a maximum of 0.5 mV (AD746B).
4. The AD746 has very close, guaranteed matching of input bias current between its two amplifiers.
5. Unity gain stable version AD712 also available.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD746J/A Min	AD746J/A Typ	AD746J/A Max	AD746B Min	AD746B Typ	AD746B Max	AD746S Min	AD746S Typ	AD746S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.3	**1.5**		0.25	**0.5**		0.3	**1.0**	mV
Offset	T_{min} to T_{max}			2.0			**0.7**			**1.5**	mV
vs. Temperature			12	20		5	**10**		12	**20**	μV/°C
vs. Supply[2] (PSRR)		**80**	95		**84**	100		**80**	95		dB
vs. Supply (PSRR)	T_{min} to T_{max}	80			**84**			**80**			dB
Long Term Stability			15			15			15		μV/month
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		110	**250**		110	**150**		110	**250**	pA
Either Input @ T_{max}	V_{CM} = 0 V		2.5/7	5.7/16		7	9.6		113	256	nA
Either Input	V_{CM} = +10 V		145	350		145	**200**		145	**350**	pA
Offset Current	V_{CM} = 0 V		45	**125**		45	**75**		45	**125**	pA
Offset Current @ T_{max}	V_{CM} = 0 V		1.0/3	2.8/8		3	4.8		45	128	nA
MATCHING CHARACTERISTICS											
Input Offset Voltage			0.6	**1.5**		0.3	**0.5**		0.6	**1.0**	mV
Input Offset Voltage	T_{min} to T_{max}			2.0			**0.7**			**1.5**	mV
Input Offset Voltage Drift				20			20			20	μV/°C
Input Bias Current				**125**			**75**			**125**	pA
Crosstalk	@ 1 kHz		120			120			120		dB
	@ 100 kHz		90			90			90		dB
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = −1	8	13		9	13		8	13		MHz
Slew Rate, Unity Gain	G = −1	**45**	75		**50**	75		**45**	75		V/μs
Full Power Response	V_O = 20 V p-p		600			600			600		kHz
Settling Time to 0.01%[4]	G = 1		0.5	0.75		0.5	0.75		0.5	0.75	μs
Total Harmonic Distortion	f = 1 kHz, Rl≥2 kΩ, V_O = 3 V rms		0.0001			0.0001			0.0001		%
INPUT IMPEDANCE											
Differential			$2.5\times10^{11}\|\|5.5$			$2.5\times10^{11}\|\|5.5$			$2.5\times10^{11}\|\|5.5$		Ω||pF
Common Mode			$2.5\times10^{11}\|\|5.5$			$2.5\times10^{11}\|\|5.5$			$2.5\times10^{11}\|\|5.5$		Ω||pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common Mode Voltage			+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		V
Over Max Operating Range[6]		**−11**		**+13**	**−11**		**+13**	**−11**		**+13**	V
Common Mode Rejection Ratio	V_{CM}=±10 V	**78**	88		**82**	88		**78**	88		dB
	T_{min} to T_{max}	76	84		**80**	84		**76**	84		dB
	V_{CM}=±11 V	**72**	84		**78**	84		**72**	84		dB
	T_{min} to T_{max}	70	80		**74**	80		**70**	80		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		2			2			2		μV p-p
	f = 10 Hz		45			45			45		nV/√Hz
	f = 100 Hz		22			22			22		nV/√Hz
	f = 1 kHz		18			18			18		nV/√Hz
	f = 10 kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	**150**	300		**175**	300		**150**	300		V/mV
	T_{min} to T_{max}	75	200		**75**	200		**65**	175		V/mV
OUTPUT CHARACTERSTICS											
Voltage	R_{LOAD}≥2 kΩ	**+13,−12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13,−12.5**	+13.9, −13.3		V
	T_{min} to T_{max}	±12	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Current	Short Circuit		25			25			25		mA
Max Capacitive Load	Gain = −1		50			50			50		pF
Driving Capability	Gain= −10		500			500			500		pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			7	**10**		7	**8.0**		7	**10**	mA
TEMPERATURE RANGE											
Rated Performance			0 to +70/−40 to +85			−40 to +85			−55 to +125		°C
PACKAGE OPTIONS[7]											
8-Pin Plastic Mini-DIP (N-8)			AD746JN								
8-Pin Cerdip (Q-8)			AD746AQ			AD746BQ			AD746SQ		
8-Pin Surface Mount (R-8)			AD746JR								
TRANSISTOR COUNT			54			54			54		

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]PSRR test conditions: $+V_S$ = 15 V, $-V_S$ = −12 V to −18 V and $+V_S$ = 12 V to 18 V, $-V_S$ = −15 V.
[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[4]Gain = −1, Rl = 2 k, Cl = 10 pF .
[5]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.
[6]Typically exceeding −14.1 V negative common mode voltage on either input results in an output phase reversal.
[7]See Section 20 for package outline information.

Specifications subject to change without notice.
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

2

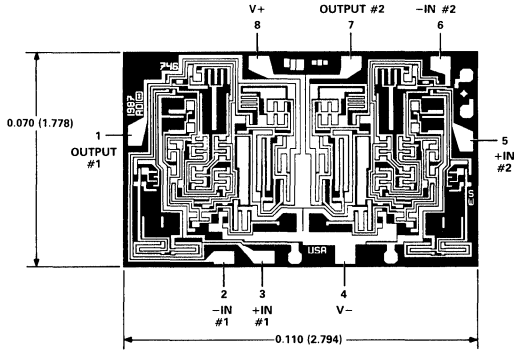
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltage . . . . . ±V_S
Output Short Circuit Duration
(For One Amplifier) . . . . . Indefinite
Differential Input Voltage . . . . . +V_S and −V_S
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD746J . . . . . 0 to +70°C
AD746A/B . . . . . −40°C to +85°C
AD746S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/Watt
8-Pin Cerdip Package: θ_{JC} = 22°C/Watt, θ_{JA} = 110°C/Watt
Small Outline Package: θ_{JA} = 155°C/Watt

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics

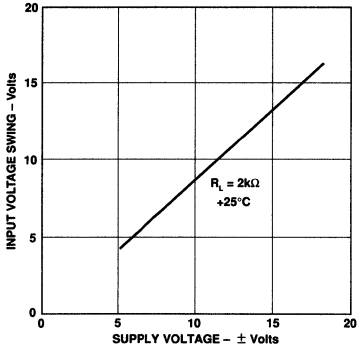


Figure 1. Input Voltage Swing vs. Supply Voltage

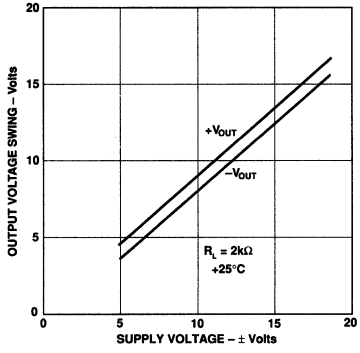


Figure 2. Output Voltage Swing vs. Supply Voltage

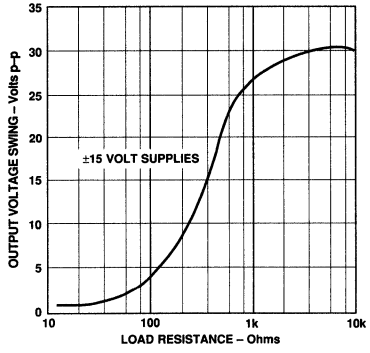


Figure 3. Output Voltage Swing vs. Load Resistance

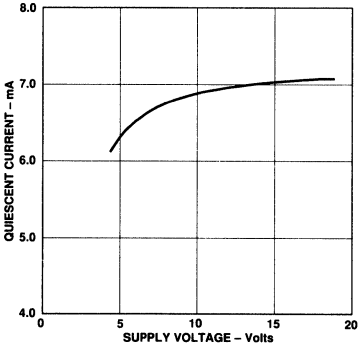


Figure 4. Quiescent Current vs. Supply Voltage

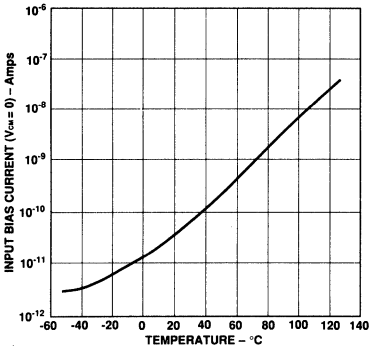


Figure 5. Input Bias Current vs. Temperature

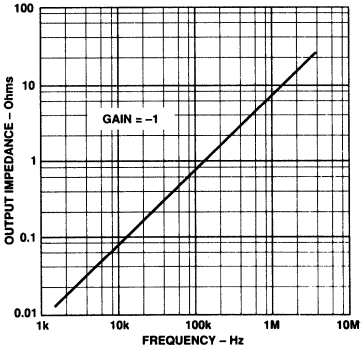


Figure 6. Output Impedance vs. Frequency

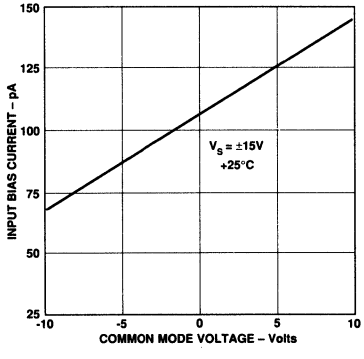


Figure 7. Input Bias Current vs. Common Mode Voltage

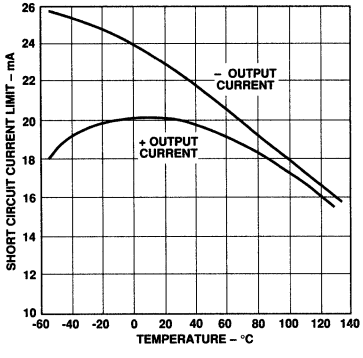


Figure 8. Short Circuit Current Limit vs. Temperature

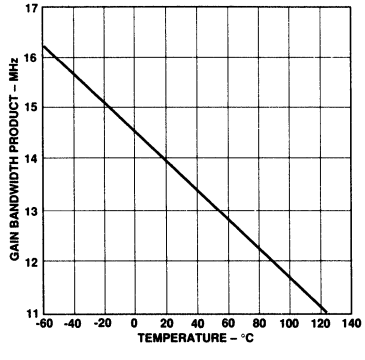


Figure 9. Gain Bandwidth Product vs. Temperature

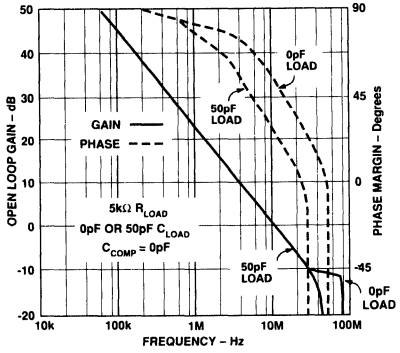


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

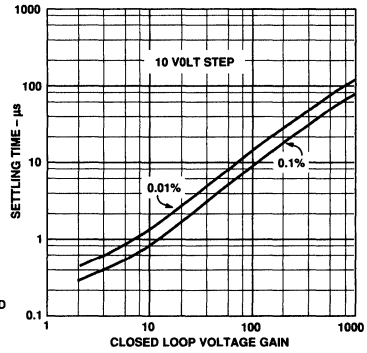


Figure 11. Settling Time vs. Closed Loop Voltage Gain

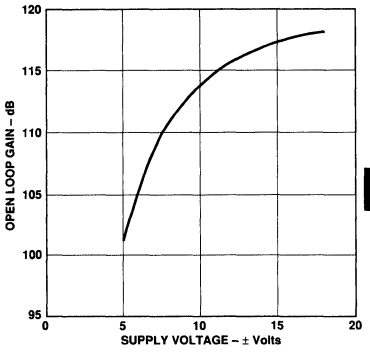


Figure 12. Open Loop Gain vs. Supply Voltage

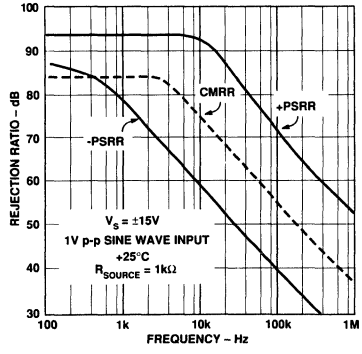


Figure 13. Common Mode and Power Supply Rejection vs. Frequency

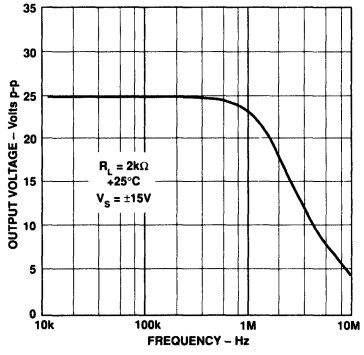


Figure 14. Large Signal Frequency Response

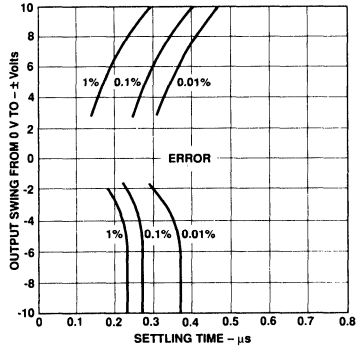


Figure 15. Output Swing and Error vs. Settling Time

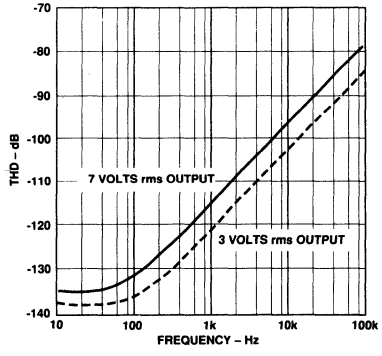


Figure 16. Total Harmonic Distortion vs. Frequency Using Circuit of Figure 19

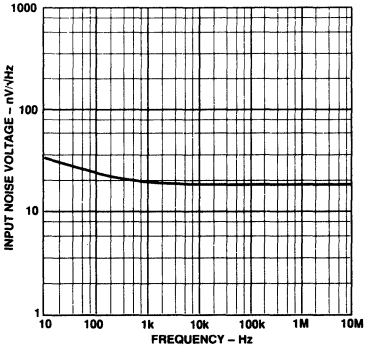


Figure 17. Input Noise Voltage Spectral Density

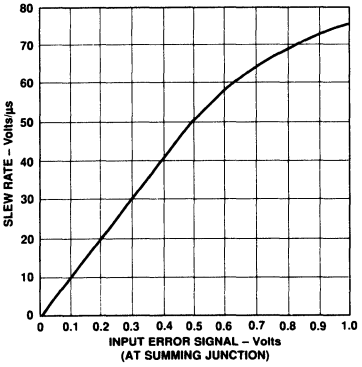


Figure 18. Slew Rate vs. Input Error Signal

Power Supply Bypassing

The power supply connections to the AD746 must maintain a low impedance to ground over a bandwidth of 13 MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1 μF ceramic and a 1 μF tantalum capacitor as shown in Figure 20 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1 μF should be used for any application.

If only one of the two amplifiers inside the AD746 is to be utilized, the unused amplifier should be connected as shown in Figure 21a. Note that the noninverting input should be grounded and that R_L and C_L are not required.

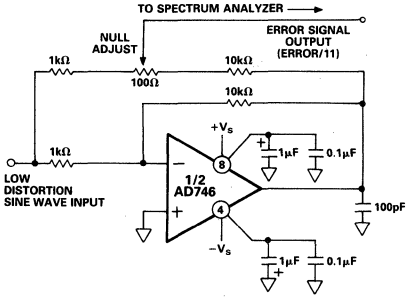


Figure 19. THD Test Circuit

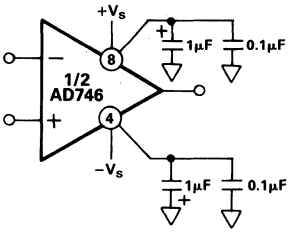


Figure 20. Power Supply Bypassing

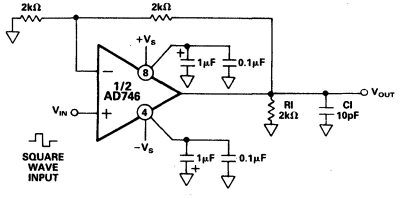


Figure 21a. Gain of 2 Follower

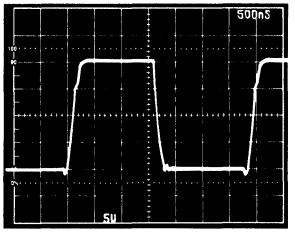


Figure 21b. Gain of 2 Follower Large Signal Pulse Response

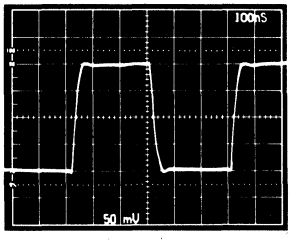


Figure 21c. Gain of 2 Follower Small Signal Pulse Response

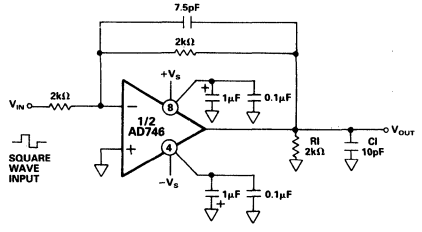


Figure 22a. Unity Gain Inverter

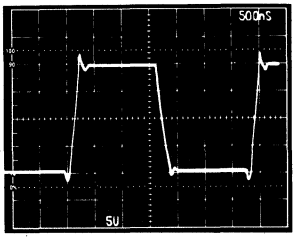


Figure 22b. Unity Gain Inverter Large Signal Pulse Response

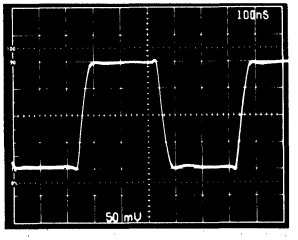


Figure 22c. Unity Gain Inverter Small Signal Pulse Response

A HIGH SPEED 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 23 can provide a range of gains from 2 up to 1000 and higher. The circuit bandwidth is 2.5 MHz at a gain of 2 and 750 kHz at a gain of 10; settling time for the entire circuit is less than 2 μs to within 0.01% for a 10 volt step, (G = 10).

Gain	R_G	Bandwidth	T_{SETTLE} (0.01%)
2	20 kΩ	2.5 MHz	1.0 μs
10	4.04 kΩ	1 MHz	2.0 μs
100	404 Ω	290 kHz	5.0 μs

Table I. Performance Summary for the 3 Op Amp Instrumentation Amplifier Circuit

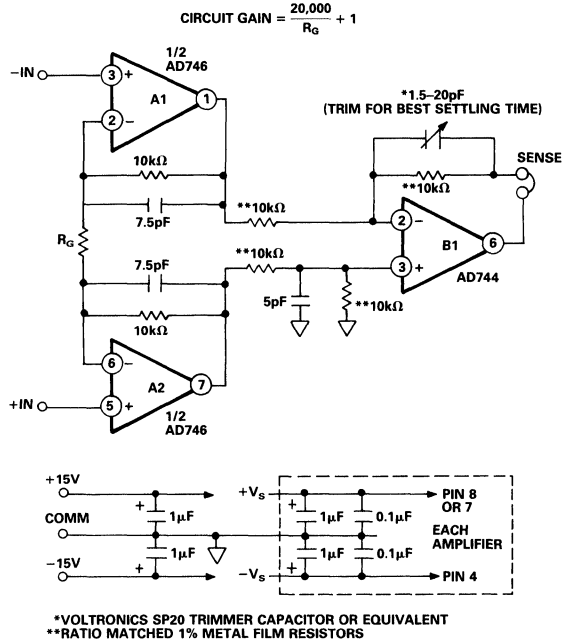


Figure 23. A High Performance, 3 Op Amp, Instrumentation Amplifier Circuit

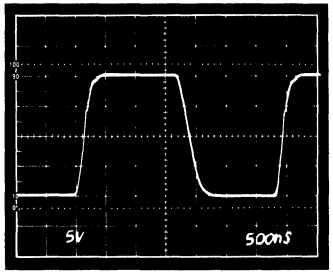


Figure 24. Pulse Response of the 3 Op Amp Instrumentation Amplifier. Gain = 10, Horizontal Scale: 0.5 μs/Div, Vertical Scale: 5 V/Div.

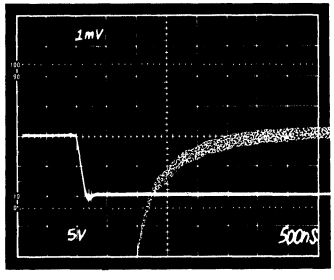


Figure 25. Settling Time of the 3 Op Amp Instrumentation Amplifier. Gain = 10, Horizontal Scale: 0.5 μs/Div, Vertical Scale: 5 V/Div. Error Signal Scale: 0.01%/Div.

THD Performance Considerations

The AD746 was carefully optimized to offer excellent performance in terms of total harmonic distortion (THD) in signal processing applications. The THD level when operating the AD746 in inverting gain applications will show a gradual rise from the distortion floor of 20 dB/decade (see Figure 28). In noninverting applications, care should be taken to balance the source impedances at both the inverting and noninverting inputs, to avoid distortion caused by the modulation of input capacitance inherent in all BiFET op amps.

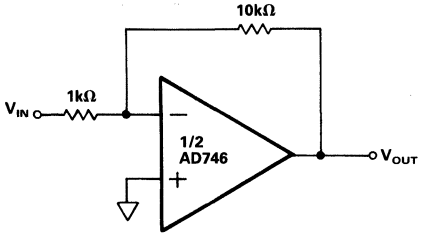


Figure 26. THD Measurement, Inverter Circuit

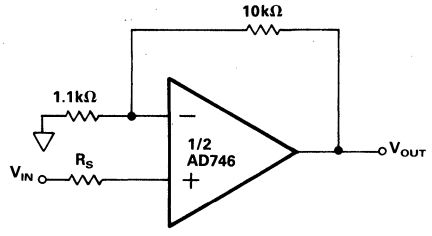


Figure 27. THD Measurement, Follower Circuit

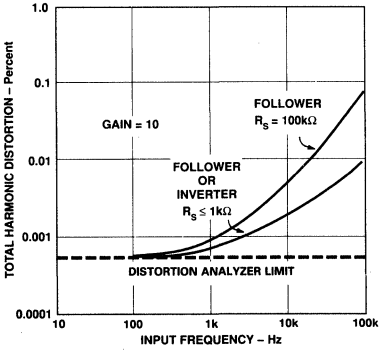


Figure 28. THD vs. Frequency Using Standard Distortion Analyzer

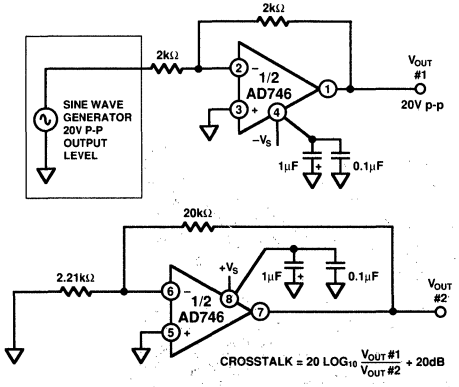


Figure 29. Crosstalk Test Circuit

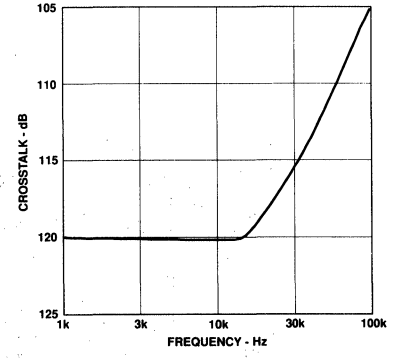


Figure 30. Crosstalk vs. Frequency

ANALOG DEVICES

High Speed, Low Power Dual Op Amp

AD827

FEATURES

HIGH SPEED
50 MHz Unity Gain Stable Operation
300 V/μs Slew Rate
120 ns Settling Time
Drives Unlimited Capacitive Loads

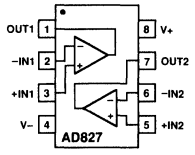
EXCELLENT VIDEO PERFORMANCE
0.04% Differential Gain @ 4.4 MHz
0.19° Differential Phase @ 4.4 MHz

GOOD DC PERFORMANCE
2 mV max Input Offset Voltage
15 μV/°C Input Offset Voltage Drift

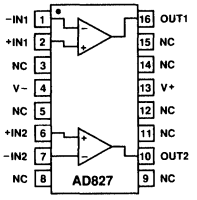
LOW POWER
Only 10 mA Total Supply Current for Both Amplifiers
±5 V to ±15 V Supplies

AD827 CONNECTION DIAGRAMS

8-Pin Plastic (N) and Cerdip (Q) Packages



16-Pin Small Outline (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD827 is a dual version of Analog Devices' industry-standard AD847 op amp. Like the AD847, it provides high speed, low power performance at low cost. The AD827 achieves a 300 V/μs slew rate and 50 MHz unity-gain bandwidth while consuming only 100 mW when operating from ±5 volt power supplies. Performance is specified for operation using ±5 V to ±15 V power supplies.

The AD827 offers an open-loop gain of 3,500 V/V into 500 Ω loads. It also features a low input voltage noise of 15 nV/$\sqrt{\text{Hz}}$, and a low input offset voltage of 2 mV maximum. Common-mode rejection ratio is a minimum of 80 dB. Power supply rejection ratio is maintained at better than 20 dB with input frequencies as high as 1 MHz, thus minimizing noise feedthrough from switching power supplies.

The AD827 is also ideal for use in demanding video applications, driving coaxial cables with less than 0.04% differential gain and 0.19° differential phase errors for 643 mV p–p into a 75 Ω reverse terminated cable.

The AD827 is also useful in multichannel, high speed data conversion systems where its fast (120 ns to 0.1%) settling time is of importance. In such applications, the AD827 serves as an input buffer for 8-bit to 10-bit A/D converters and as an output amplifier for high speed D/A converters.

APPLICATION HIGHLIGHTS

1. Performance is fully specified for operation using ±5 V to ±15 V supplies.
2. A 0.04% differential gain and 0.19° differential phase error at the 4.4 MHz color subcarrier frequency, together with its low cost, make it ideal for many video applications.
3. The AD827 can drive unlimited capacitive loads, while its 30 mA output current allows 50 Ω and 75 Ω reverse-terminated loads to be driven.
4. The AD827's 50 MHz unity-gain bandwidth makes it an ideal candidate for multistage active filters.
5. The AD827 is available in 8-pin plastic mini-DIP, cerdip, and 16-pin SOIC packages. Chips and MIL-STD-883B processing are also available.

SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Units
DC PERFORMANCE									
Input Offset Voltage[1]		±5 V		0.5	2		0.3	2	mV
	T_{min} to T_{max}				3.5			4	mV
		±15 V			4			4	mV
	T_{min} to T_{max}				6			6	mV
Offset Voltage Drift		±5 V to ±15 V		15			15		µV/°C
Input Bias Current		±5 V to ±15 V		3.3	7		3.3	7	µA
	T_{min} to T_{max}				8.2			9.5	µA
Input Offset Current		±5 V to ±15 V		50	300		50	300	nA
	T_{min} to T_{max}				400			400	nA
Offset Current Drift		±5 V to ±15 V		0.5			0.5		nA/°C
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	±5 V	78	95		80	95		dB
	V_{CM} = ±12 V	±15 V	78	95		80	95		dB
	T_{min} to T_{max}	±5 V to ±15 V	75			75			dB
Power Supply Rejection Ratio		±5 V to ±15 V	75	86		75	86		dB
	T_{min} to T_{max}		72			72			dB
Open-Loop Gain									
	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		2	3.5		2	3.5		V/mV
	T_{min} to T_{max}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{min} to T_{max}		1.5			1.5			V/mV
MATCHING CHARACTERISTICS									
Input Offset Voltage		±5 V		0.4			0.2		mV
Crosstalk	f = 5 MHz	±5 V		85			85		dB
DYNAMIC PERFORMANCE									
Unity-Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_O = 5 V p–p,								
	R_{LOAD} = 500 Ω	±5 V		12.7			12.7		MHz
	V_O = 20 V p–p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 500 Ω	±5 V		200			200		V/µs
	R_{LOAD} = 1 kΩ	±15 V		300			300		V/µs
Settling Time to 0.1%	A_V = −1								
	−2.5 V to +2.5 V	±5 V		65			65		ns
	−5 V to +5 V	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degrees
Differential Gain Error	f = 4.4 MHz	±15 V		0.04			0.04		%
Differential Phase Error	f = 4.4 MHz	±15 V		0.19			0.19		Degrees
Input Voltage Noise	f = 10 kHz	±15 V		15			15		nV/√Hz
Input Current Noise	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
Input Common-Mode Voltage Range		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short-Circuit Current Limit		±5 V to ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance				300			300		kΩ
Input Capacitance				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		10	13		10	13	mA
	T_{min} to T_{max}				16			16.5/17.5	mA
		±15 V		10.5	13.5		10.5	13.5	mA
	T_{min} to T_{max}				16.5			17/18	mA
TRANSISTOR COUNT				92			92		

NOTES
[1]Offset voltage for the AD827 is guaranteed after power is applied and the device is fully warmed up. All other specifications are measured using high speed test equipment, approximately 1 second after power is applied.
[2]Full Power Bandwidth = Slew Rate/2π V_{PEAK}.
[3]Gain = +1, rising edge.
All min and max specifications are guaranteed.
Specifications subject to change without notice.

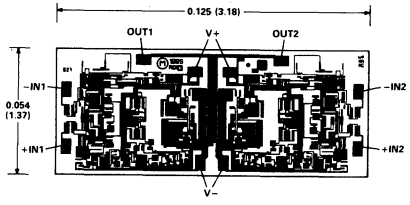
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) Package (Derate at 10 mW/°C) . . . . . 1.5 W
Cerdip (Q) Package (Derate at 8.7 mW/°C) . . . . . 1.3 W
Small Outline (R) Package (Derate at 10 mW/°C) . . . . 1.5 W
Input Common Mode Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 6 V
Output Short Circuit Duration[3] . . . . . Indefinite
Storage Temperature Range N, R . . . . . −65°C to +125°C
Storage Temperature Range Q . . . . . −65°C to +150°C
Operating Temperature Range
AD827J . . . . . 0 to +70°C
AD827A . . . . . −40°C to +85°C
AD827S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering to 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C. Thermal Characteristics:
Mini-DIP: θ_{JA} = 100°C/Watt, θ_{JC} = 33°C/Watt
Cerdip: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
16-Pin Small Outline Package: θ_{JA} = 100°C/Watt
[3]Indefinite short circuit duration is only permissible as long as the absolute maximum power rating is not exceeded.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Substrate is connected to V+.



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD827JN	0 to +70°C	8-Pin Plastic DIP (N-8)
AD827JR	0 to +70°C	16-Pin Plastic SO (R-16)
AD827AQ	−40°C to +85°C	8-Pin Cerdip (Q-8)
AD827SQ	−55°C to +125°C	8-Pin Cerdip (Q-8)
AD827SQ/883B	−55°C to +125°C	8-Pin Cerdip (Q-8)

NOTE
*See Section 20 for package outline information.

Typical Characteristics (@ +25°C & ±15 V, unless otherwise noted)

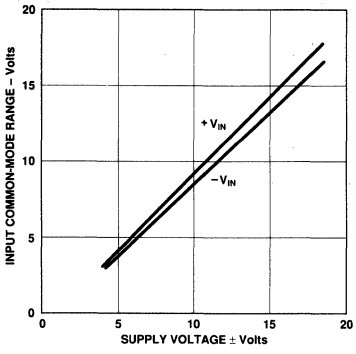


Figure 1. Input Common-Mode Range vs. Supply Voltage

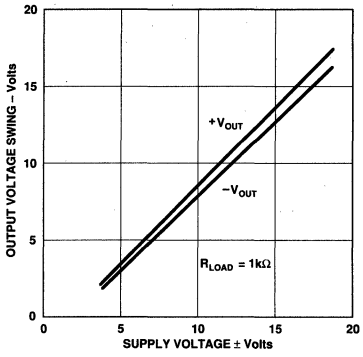


Figure 2. Output Voltage Swing vs. Supply Voltage

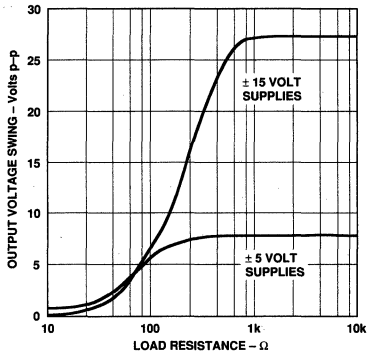


Figure 3. Output Voltage Swing vs. Load Resistance

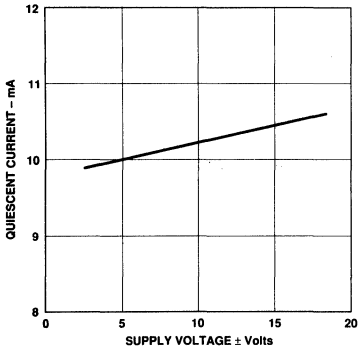


Figure 4. Quiescent Current vs. Supply Voltage

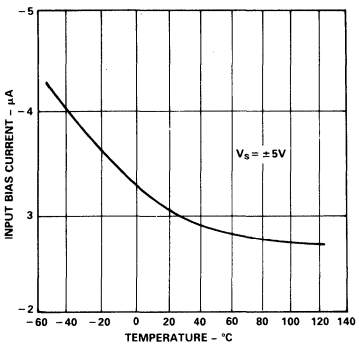


Figure 5. Input Bias Current vs. Temperature

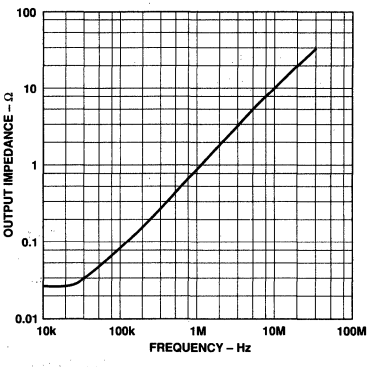


Figure 6. Closed-Loop Output Impedance vs. Frequency, Gain = +1

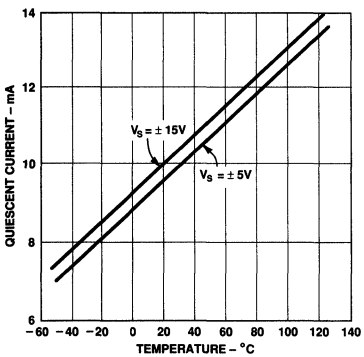


Figure 7. Quiescent Current vs. Temperature

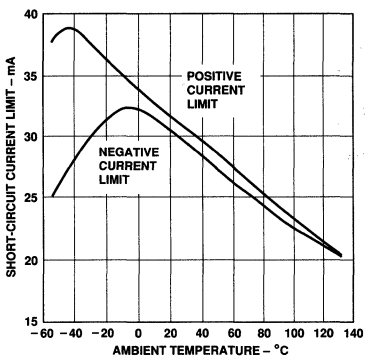


Figure 8. Short-Circuit Current Limit vs. Temperature

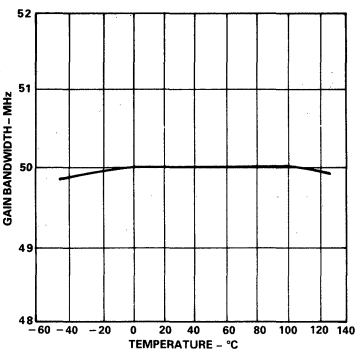


Figure 9. Gain Bandwidth vs. Temperature

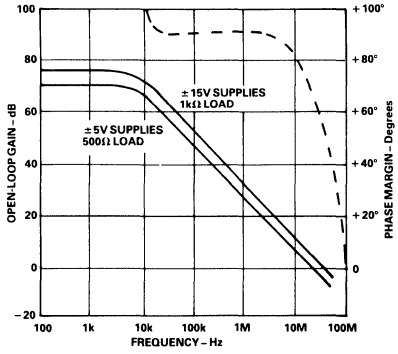


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

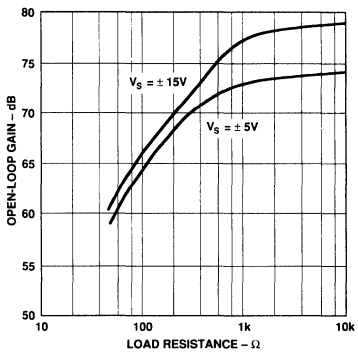


Figure 11. Open-Loop Gain vs. Load Resistance

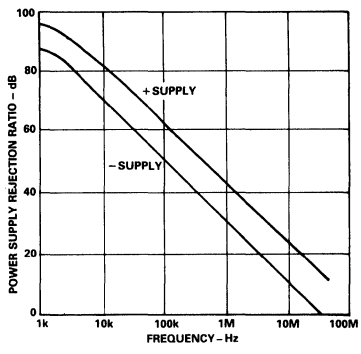


Figure 12. Power Supply Rejection Ratio vs. Frequency

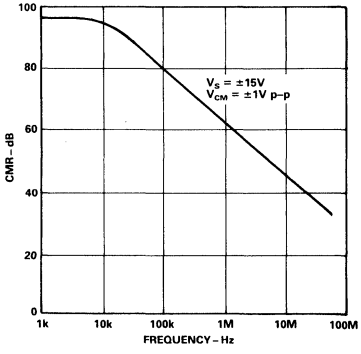


Figure 13. Common-Mode Rejection Ratio vs. Frequency

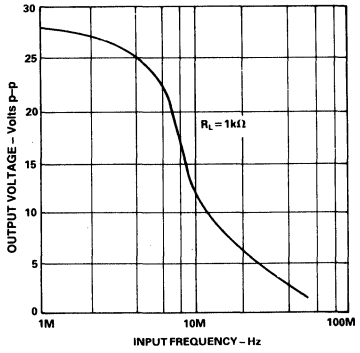


Figure 14. Large Signal Frequency Response

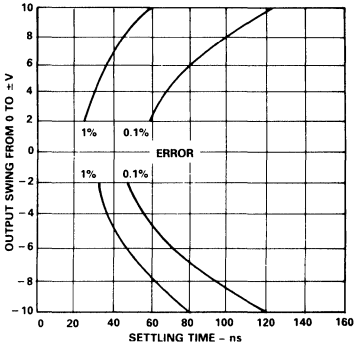


Figure 15. Output Swing and Error vs. Settling Time

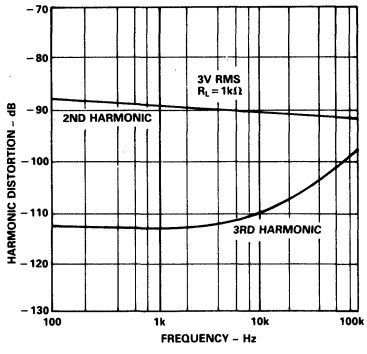


Figure 16. Harmonic Distortion vs. Frequency

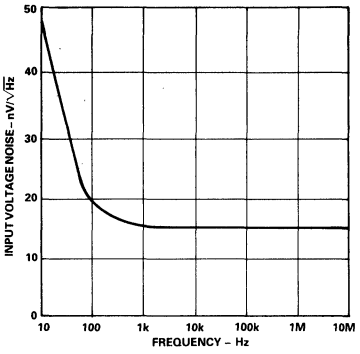


Figure 17. Input Voltage Noise Spectral Density

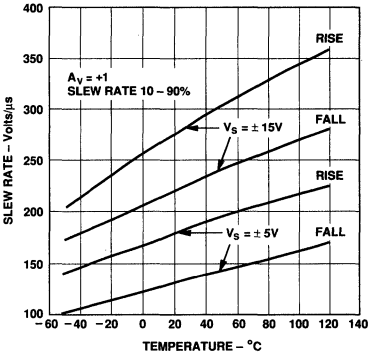


Figure 18. Slew Rate vs. Temperature

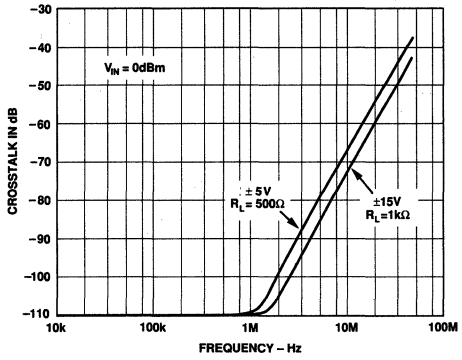


Figure 19. Crosstalk vs. Frequency

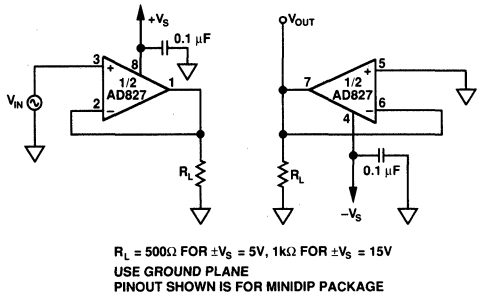


Figure 20. Crosstalk Test Circuit

INPUT PROTECTION PRECAUTIONS

An input resistor (resistor R_{IN} of Figure 21a) is recommended in circuits where the input common-mode voltage to the AD827 may exceed (on a transient basis) the positive supply voltage. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into their bases.

For high performance circuits, it is recommended that a second resistor (R_B in Figures 21a and 22a) be used to reduce bias-current errors by matching the impedance at each input. This resistor reduces the error caused by offset voltages by more than an order of magnitude.

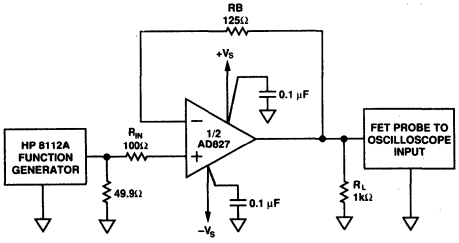


Figure 21a. Follower Connection

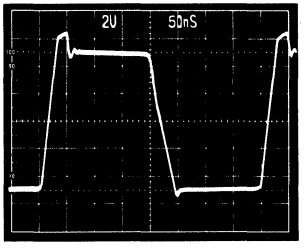


Figure 21b. Follower Large Signal Pulse Response

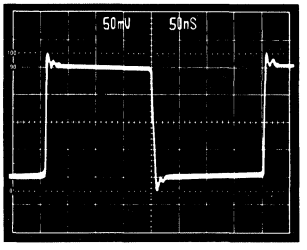


Figure 21c. Follower Small Signal Pulse Response

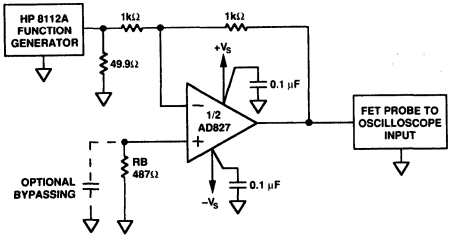


Figure 22a. Inverter Connection

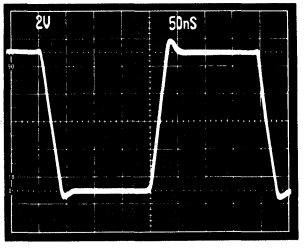


Figure 22b. Inverter Large Signal Pulse Response

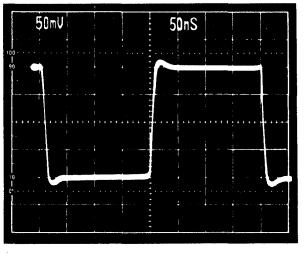


Figure 22c. Inverter Small Signal Pulse Response

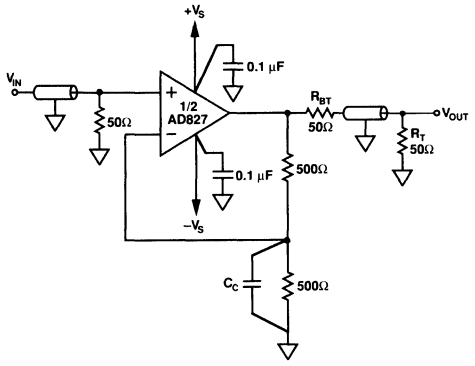


Figure 23. A Video Line Driver

VIDEO LINE DRIVER

The AD827 functions very well as a low cost, high speed line driver for either terminated or unterminated cables. Figure 23 shows the AD827 driving a doubly terminated cable in a follower configuration.

The termination resistor, R_T, (when equal to the cable's characteristic impedance) minimizes reflections from the far end of the cable. While operating from ±5 V supplies, the AD827 maintains a typical slew rate of 200 V/µs, which means it can drive a ±1 V, 30 MHz signal into a terminated cable.

Video Line Driver Performance Summary

V_{IN}*	V_{SUPPLY}	C_C	−3 dB B_W	Overshoot
0 dB or ±500 mV Step	±15	20 pF	23 MHz	4%
0 dB or ±500 mV Step	±15	15 pF	21 MHz	0%
0 dB or ±500 mV Step	±15	0 pF	13 MHz	0%
0 dB or ±500 mV Step	±5	20 pF	18 MHz	2%
0 dB or ±500 mV Step	±5	15 pF	16 MHz	0%
0 dB or ±500 mV Step	±5	0 pF	11 MHz	0%

NOTE
*−3 dB bandwidth numbers are for the 0 dBm signal input. Overshoot numbers are the percent overshoot of the 1 Volt step input.

Table I. Video Line Driver Performance Chart

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD827 output and the cable input, in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a flatter frequency response, although this requires that the op amp supply ±2 V to the output in order to achieve a ±1 V swing at resistor R_T.

A HIGH SPEED 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 24 can provide a range of gains. The chart of Table II details performance.

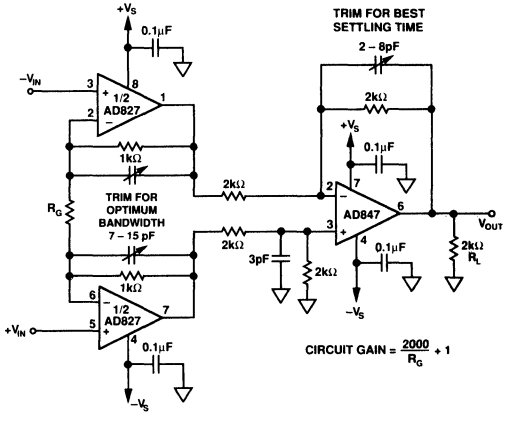


Figure 24. A High Bandwidth Three Op Amp Instrumentation Amplifier

Gain	R_G	Small Signal Bandwidth @ 1 V p–p Output
1	Open	16.1 MHz
2	2 k	14.7 MHz
10	226 Ω	4.9 MHz
100	20 Ω	660 kHz

Table II. Performance Specifications for the Three Op Amp Instrumentation Amplifier

A TWO-CHIP VOLTAGE-CONTROLLED AMPLIFIER (VCA) WITH EXPONENTIAL RESPONSE

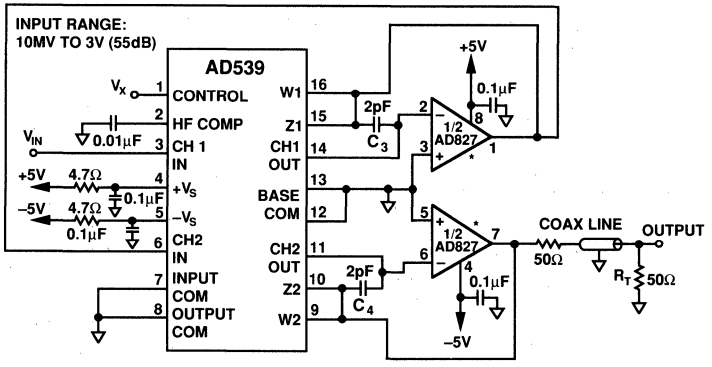
Voltage-controlled amplifiers are often used as building blocks in automatic gain control systems. Figure 25 shows a two-chip VCA built using the AD827 and the AD539, a dual, current-output multiplier. As configured, the circuit has its two multipliers connected in series. They could also be placed in parallel with an increase in bandwidth and a reduction in gain. The gain of the circuit is controlled by V_X, which can range from 0 to 3 V dc. Measurements show that this circuit easily supplies 2 V p–p into a 100 Ω load while operating from ±5 V supplies. The overall bandwidth of the circuit is approximately 7 MHz with 0.5 dB of peaking.

Each half of the AD827 serves as an I/V converter and converts the output current of one of the two multipliers in the AD539 into an output voltage. Each of the AD539's two multipliers contains two internal 6 kΩ feedback resistors; one is connected between the CH1 output and Z1, the other between the CH1 output and W1. Likewise, in the CH2 multiplier, one of the feedback resistors is connected between CH2 and Z2 and the other is connected between CH2 and Z2. In Figure 25, Z1 and W1 are tied together, as are Z2 and W2, providing a 3 kΩ feedback resistor for the op amp. The 2 pF capacitors connected between the AD539's W1 and CH1 and W2 and CH2 pins are in parallel with the feedback resistors and thus reduce peaking in the VCA's frequency response. Increasing the values of C3 and C4 can further reduce the peaking at the expense of reduced bandwidth. The 1.25 mA full-scale output current of the AD539 and the 3 kΩ feedback resistor set the full-scale output voltage of each multiplier at 3.25 V p–p.

Current limiting in the AD827 (typically 30 mA) limits the output voltage in this application to about 3 V p–p across a 100 Ω load. Driving a 50 Ω reverse-terminated load divides this value by two, limiting the maximum signal delivered to a 50 Ω load to about 1.5 V p–p, which suffices for video signal levels. The dynamic range of this circuit is approximately 55 dB and is primarily limited by feedthrough at low input levels and by the maximum output voltage at high levels.

Guidelines for Grounding and Bypassing

When designing practical high frequency circuits using the AD827, some special precautions are in order. Both short interconnection leads and a large ground plane are needed whenever possible to provide low resistance, low inductance circuit paths. One should remember to minimize the effects of capacitive coupling between circuits. Furthermore, IC sockets should be avoided. Feedback resistors should be of a low enough value that the time constant formed with stray circuit capacitances at the amplifier summing junction will not limit circuit performance. As a rule of thumb, use feedback resistor values that are less than 5 kΩ. If a larger resistor value is necessary, a small (<10 pF) feedback capacitor in parallel with the feedback resistor may be used. The use of 0.1 μF ceramic disc capacitors is recommended for bypassing the op amp's power supply leads.



*PINOUT SHOWN IS FOR MINI-DIP PACKAGE

$$V_{OUT} \text{ AT TERMINATION RESISTOR, } R_T = \frac{V_X^2 V_{IN}}{8V_2}$$

$$V_{OUT} \text{ AT PIN 8 OF AD827} = \frac{V_X^2 V_{IN}}{4V^2}$$

Figure 25. A Wide Range Voltage-Controlled Amplifier Circuit

ANALOG DEVICES

High Speed, Low Noise Video Op Amp

AD829

FEATURES

High Speed
- 120 MHz Bandwidth, Gain = −1
- 230 V/μs Slew Rate
- 90 ns Settling Time to 0.1%

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase

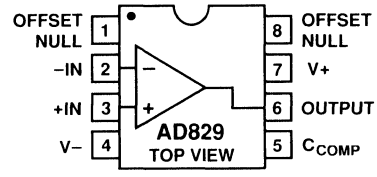
Low Noise
- 2 nV/$\sqrt{\text{Hz}}$ Input Voltage Noise
- 1.5 pA/$\sqrt{\text{Hz}}$ Input Current Noise

Excellent DC Precision
- 1 mV max Input Offset Voltage (Over Temp)
- 0.3 μV/°C Input Offset Drift

Flexible Operation
- Specified for ±5 V to ±15 V Operation
- ±3 V Output Swing into a 150 Ω Load
- External Compensation for Gains 1 to 20
- 5 mA Supply Current

AD829 CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N),
Cerdip (Q) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD829 is a low noise (2 nV/$\sqrt{\text{Hz}}$), high speed op amp with custom compensation that provides the user with gains from ±1 to ±20 while maintaining a bandwidth greater than 50 MHz. The AD829's 0.04° differential phase and 0.02% differential gain performance at 3.58 MHz and 4.43 MHz, driving reverse-terminated 50 Ω or 75 Ω cables, makes it ideally suited for professional video applications. The AD829 achieves its 230 V/μs uncompensated slew rate and 750 MHz gain bandwidth product while requiring only 5 mA of current from the power supplies.

The AD829's external compensation pin gives it exceptional versatility. For example, compensation can be selected to optimize the bandwidth for a given load and power supply voltage. As a gain-of-two line driver, the −3 dB bandwidth can be increased to 95 MHz at the expense of 1 dB of peaking. In addition, the AD829's output can also be clamped at its external compensation pin.

The AD829 has excellent dc performance. It offers a minimum open-loop gain of 30 V/mV into loads as low as 500 Ω, low input voltage noise of 2 nV/$\sqrt{\text{Hz}}$, and a low input offset voltage of 1 mV maximum. Common-mode rejection and power supply rejection ratios are both 120 dB.

The AD829 is also useful in multichannel, high speed data conversion where its fast (90 ns to 0.1%) settling time is of importance. In such applications, the AD829 serves as an input buffer for 8-to-10-bit A/D converters and as an output I/V converter for high speed D/A converters.

The AD829 provides many of the same advantages that a transimpedance amplifier offers, while operating as a traditional voltage feedback amplifier. A bandwidth greater than 50 MHz can be maintained for a range of gains by changing the external compensation capacitor. The AD829 and the transimpedance amplifier are both unity gain stable and provide similar voltage noise performance (2 nV/$\sqrt{\text{Hz}}$). However, the current noise of the AD829 (1.5 pA/$\sqrt{\text{Hz}}$) is less than 10% of the noise of transimpedance amps. Furthermore, the inputs of the AD829 are symmetrical.

PRODUCT HIGHLIGHTS

1. Input voltage noise of 2 nV/$\sqrt{\text{Hz}}$, current noise of 1.5 pA/$\sqrt{\text{Hz}}$ and 50 MHz bandwidth, for gains of 1 to 20, make the AD829 an ideal preamp.
2. Differential phase error of 0.04° and a 0.02% differential gain error, at the 3.58 MHz NTSC and 4.43 MHz PAL and SECAM color subcarrier frequencies, make it an outstanding video performer for driving reverse-terminated 50 Ω and 75 Ω cables to ±1 V (at their terminated end).
3. The AD829 can drive heavy capacitive loads.
4. Performance is fully specified for operation from ±5 V to ±15 V supplies.
5. Available in plastic, cerdip, and small outline packages. Chips and MIL-STD-883B parts are also available.

SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.2	1		0.1	0.5	mV
	T_{min} to T_{max}				1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7	µA
	T_{min} to T_{max}				8.2			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500	nA
	T_{min} to T_{max}				500			500	nA
Offset Current Drift		±5 V, ±15 V		0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		30	65		30	65		V/mV
	T_{min} to T_{max}		20			20			V/mV
	R_{LOAD} = 150 Ω			40			40		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		50	100		50	100		V/mV
	T_{min} to T_{max}		20			20			V/mV
	R_{LOAD} = 500 Ω			85			85		V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth Product		±5 V		600			600		MHz
		±15 V		750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p–p								
	R_{LOAD} = 500 Ω	±5 V		25			25		MHz
	V_O = 20 V p–p								
	R_{LOAD} = 1 kΩ	±15 V		3.6			3.6		MHz
Slew Rate[2]	R_{LOAD} = 500 Ω	±5 V		150			150		V/µs
	R_{LOAD} = 1 kΩ	±15 V		230			230		V/µs
Settling Time to 0.1%	A_V = −19								
	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step	±15 V		90			90		ns
Phase Margin[2]	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		dB
	T_{min} to T_{max}		96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		dB
	T_{min} to T_{max}		94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		2			2		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5		pA/$\sqrt{Hz}$
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.8			−3.8		V
		±15 V		+14.3			+14.3		V
				−13.8			−13.8		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 50 Ω	±5 V		1.4			1.4		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short Circuit Current		±5 V, ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance (Differential)				13			13		kΩ
Input Capacitance (Differential)[4]				5			5		pF
Input Capacitance (Common Mode)				1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2		MΩ

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18		±4.5	±18	V
Quiescent Current		±5 V		5	6.5		5	6.5	mA
	T_{min} to T_{max}				8.0			8.2/8.7	mA
		±15 V		5.3	6.8		5.3	6.8	mA
	T_{min} to T_{max}				8.3			8.5/9.0	mA
TRANSISTOR COUNT	Number of Transistors			46			46		

NOTES
[1]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[2]Tested at Gain = +20, C_{COMP} = 0 pF.
[3]3.58 MHz (NTSC) and 4.43 MHz (PAL & SECAM).
[4]Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.
Specifications subject to change without notice.

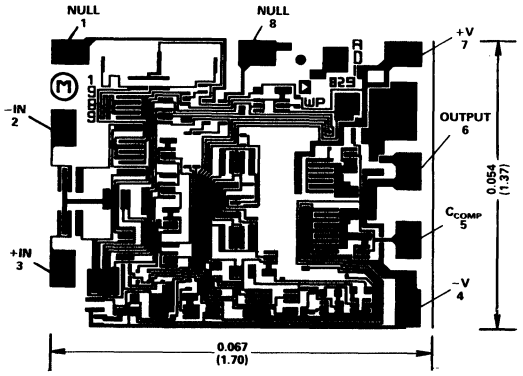
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.3 Watts
Small Outline (R) . . . . . 0.9 Watts
Cerdip (Q) . . . . . 1.3 Watts
Input Voltage . . . . . ±Vs
Differential Input Voltage[3] . . . . . ±6 Volts
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD829J . . . . . 0 to +70°C
AD829A . . . . . −40°C to +85°C
AD829S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.
Thermal characteristics:
8-pin plastic package: θ_{JA} = 100°C/watt (derate at 8.7 mW/°C)
8-pin cerdip package: θ_{JA} = 110°C/watt (derate at 8.7 mW/°C)
8-pin small outline package: θ_{JA} = 155°C/watt (derate at 6 mW/°C).
[3]If the differential voltage exceeds 6 volts, external series protection resistors should be added to limit the input current.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD829JN	0 to +70°C	8-Pin Plastic Mini-DIP	(N-8)
AD829JR	0 to +70°C	8-Pin Plastic SOIC	(R-8)
AD829AQ	−40°C to +85°C	8-Pin Cerdip	(Q-8)
AD829SQ	−55°C to +125°C	8-Pin Cerdip	(Q-8)
AD829SQ/883B	−55°C to +125°C	8-Pin Cerdip	(Q-8)

*See Section 20 for package outline information.

Typical Performance Characteristics

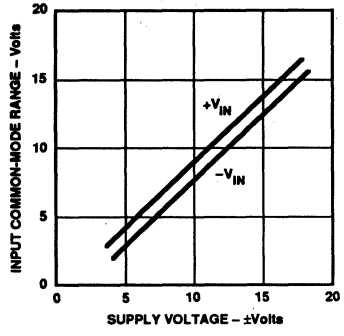


Figure 1. Input Common-Mode Range vs. Supply Voltage

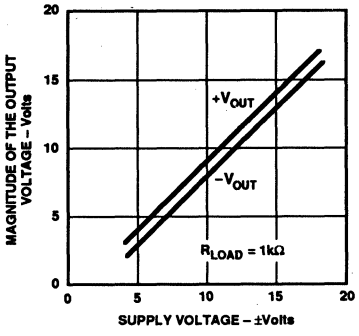


Figure 2. Output Voltage Swing vs. Supply Voltage

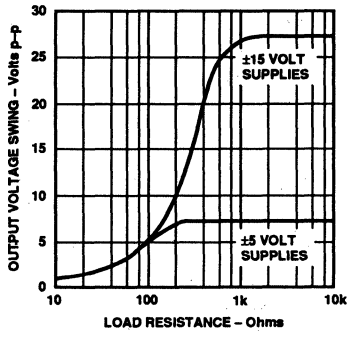


Figure 3. Output Voltage Swing vs. Resistive Load

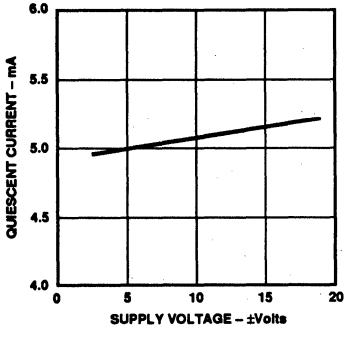


Figure 4. Quiescent Current vs. Supply Voltage

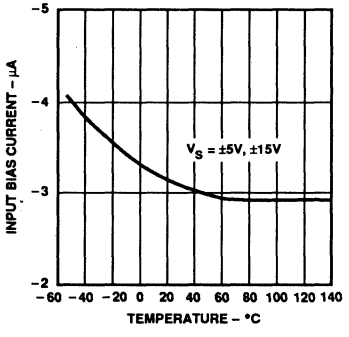


Figure 5. Input Bias Current vs. Temperature

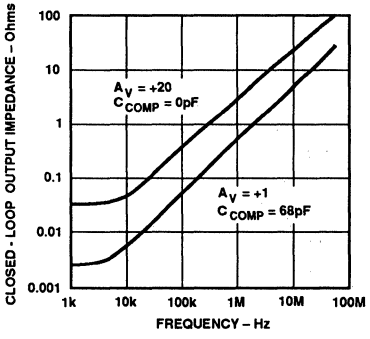


Figure 6. Closed-Loop Output Impedance vs. Frequency

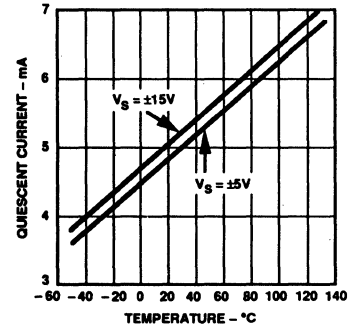


Figure 7. Quiescent Current vs. Temperature

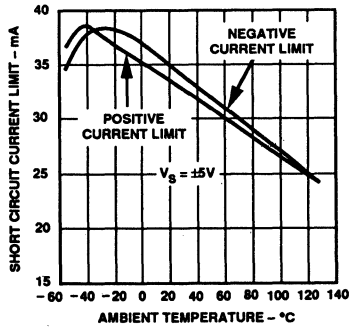


Figure 8. Short Circuit Current Limit vs. Temperature

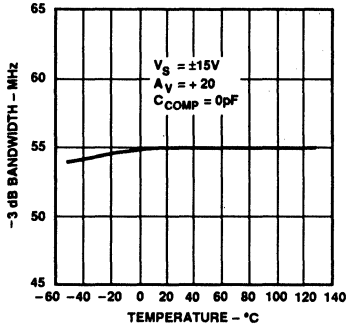


Figure 9. –3 dB Bandwidth vs. Temperature

ANALOG DEVICES

Wideband, Fast Settling Op Amp

AD840

FEATURES

Wideband AC Performance
- Gain Bandwidth Product: 400 MHz (Gain ≥ 10)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 400 V/μs
- Stable at Gains of 10 or Greater
- Full Power Bandwidth: 6.4 MHz for 20 V p–p into a 500 Ω Load

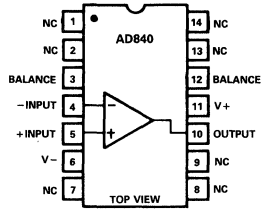
Precision DC Performance
- Input Offset Voltage: 0.3 mV max
- Input Offset Drift: 3 μV/°C typ
- Input Voltage Noise: 4 nV/$\sqrt{Hz}$
- Open-Loop Gain: 130 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

APPLICATIONS

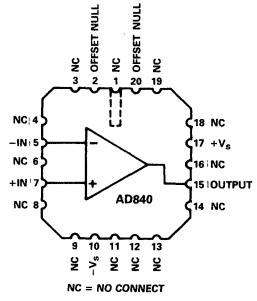
- Video and Pulse Amplifiers
- DAC and ADC Buffers
- Line Drivers
- Available in 14-Pin Plastic DIP, Hermetic Cerdip Packages and Chip Form
- MIL-STD-883B Processing Available

AD840 CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



LCC (E) Package



PRODUCT DESCRIPTION

The AD840 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD841, which is unity-gain stable, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 400 MHz gain bandwidth product, the AD840 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 100 ns for a 10 volt step.

The AD840 remains stable over its full operating temperature range at closed-loop gains of 10 or greater. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capability of 50 mA, a low input voltage noise of 4 nV/$\sqrt{Hz}$ and a low input offset voltage of 0.3 mV maximum (AD840K).

The 400 V/μs slew rate of the AD840, along with its 400 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD840 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD840 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD840 make it ideal for DAC and ADC buffers, line drivers and all types of video instrumentation circuitry.
2. The AD840 is truly a precision amplifier. It offers 12-bit accuracy to 0.01% or better and wide bandwidth, performance previously available only in hybrids.
3. The AD840's thermally balanced layout and the high speed of the CB process allow the AD840 to settle to 0.01% in 100 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 0.3 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where circuit gain will be 10 or greater.
6. The AD840 is an enhanced replacement for the HA2540.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD840J Min	AD840J Typ	AD840J Max	AD840K Min	AD840K Typ	AD840K Max	AD840S Min	AD840S Typ	AD840S Max	Units
INPUT OFFSET VOLTAGE[1]			0.2	**1**		0.1	**0.3**		0.2	**1**	mV
	$T_{min} - T_{max}$			1.5			**0.7**			2	mV
Offset Drift			5			3			5		µV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	µA
	$T_{min} - T_{max}$			10			**6**			12	µA
INPUT OFFSET CURRENT			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	µA
	$T_{min} - T_{max}$			0.5			**0.3**			0.6	µA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			30			30			30		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	12		**±10**	12		±10	12		V
Common-Mode Rejection	$V_{CM} = \pm 10$ V	**90**	110		**106**	115		**90**	110		dB
	$T_{min} - T_{max}$	85			**90**			85			dB
INPUT VOLTAGE NOISE	f = 1 kHz		4			4			4		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		10			10			10		µV rms
OPEN LOOP GAIN	$V_O = \pm 10$ V										
	R_{LOAD} = 1 kΩ	**100**	130		**100**	130		**100**	130		V/mV
	$T_{min} - T_{max}$	50	80		75	100		**50**	80		V/mV
	R_{LOAD} = 500 Ω	**75**			**100**			75			V/mV
	$T_{min} - T_{max}$	50			75			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD} \geq 500$ Ω										
	$T_{min} - T_{max}$	**±10**			**±10**			**±10**			V
Current	$V_{OUT} = \pm 10$ V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		15			15			15		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV p–p										
	$A_V = -10$		400			400			400		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	$R_{LOAD} \geq 500$ Ω	5.5	6.4		5.5	6.4		5.5	6.4		MHz
Rise Time	$A_V = -10$		10			10			10		ns
Overshoot[3]	$A_V = -10$		20			20			20		%
Slew Rate[3]	$A_V = -10$	350	400		350	400		350	400		V/µs
Settling Time[3] −10 V Step	$A_V = -10$										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
OVERDRIVE RECOVERY	−Overdrive		190			190			190		ns
	+Overdrive		350			350			350		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.025			0.025			0.025		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.04			0.04			0.04		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			10.5	**12**		10.5	**12**		10.5	**12**	mA
	$T_{min} - T_{max}$			14			**14**			**16**	mA
Power Supply Rejection Ratio	$V_S = \pm 5$ V to ±18 V	**90**	100		**94**	100		**90**	100		dB
	$T_{min} - T_{max}$	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		**0**		**+75**	0		**+75**	−55		**+125**	°C
PACKAGE OPTIONS[5]											
Cerdip (Q-14)			AD840JQ			AD840KQ			AD840SQ		
Plastic (N-14)			AD840JN			AD840KN					
LCC (E-20A)[6]									AD840SE		
J and S Grade Chips Also Available											

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = slew rate/2π V_{PEAK}.
[3]Refer to Figures 22 and 23.
[4]"S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
[5]See Section 20 for package outline information.
[6]Contact factory for availability.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	
Plastic (N)	1.5W
Cerdip (Q)	1.3W
Input Voltage	$\pm V_S$
Differential Input Voltage	±6V
Storage Temperature Range	
Q	−65°C to +150°C
N	−65°C to +125°C
Junction Temperature (T_J)	+175°C
Lead Temperature Range (Soldering 60sec)	+300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

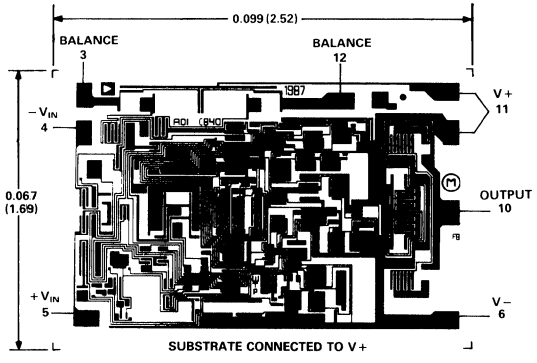
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}	
Cerdip Package	35°C/W	110°C/W	38°C/W	Recommended Heat Sink:
Plastic Package	30°C/W	95°C/W		Aavid Engineering ©#602B

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics (at +25°C and V_S % ±15 V, unless otherwise noted)

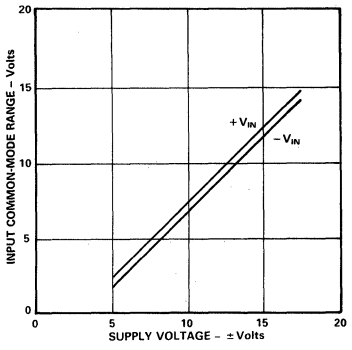


Figure 1. Input Common-Mode Range vs. Supply Voltage

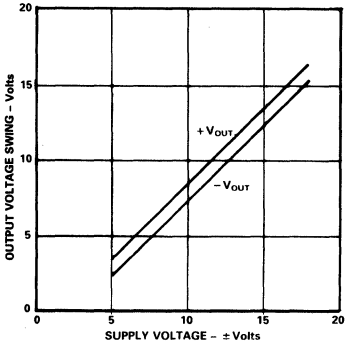


Figure 2. Output Voltage Swing vs. Supply Voltage

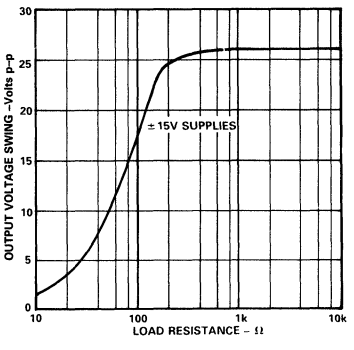


Figure 3. Output Voltage Swing vs. Load Resistance

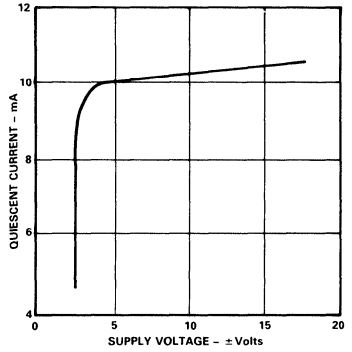


Figure 4. Quiescent Current vs. Supply Voltage

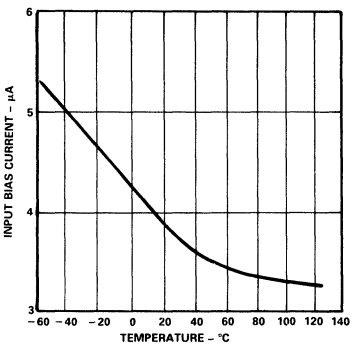


Figure 5. Input Bias Current vs. Temperature

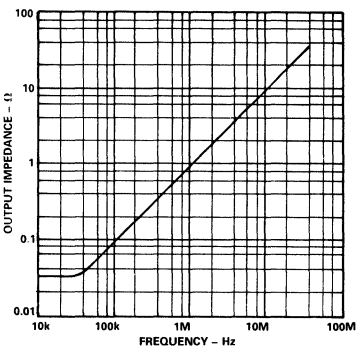


Figure 6. Output Impedance vs. Frequency

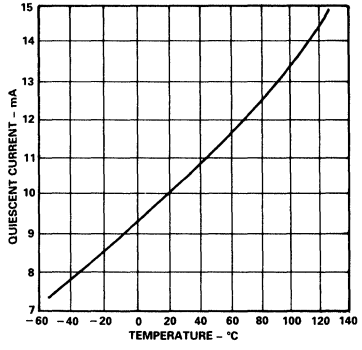


Figure 7. Quiescent Current vs. Temperature

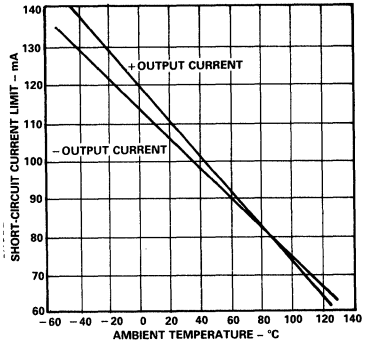


Figure 8. Short-Circuit Current Limit vs. Temperature

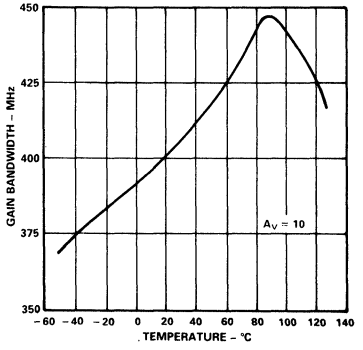


Figure 9. Gain Bandwidth Product vs. Temperature

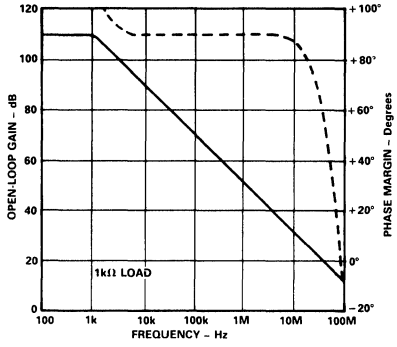


Figure 10. Open-Loop Gain and Phase Margin Phase vs. Frequency

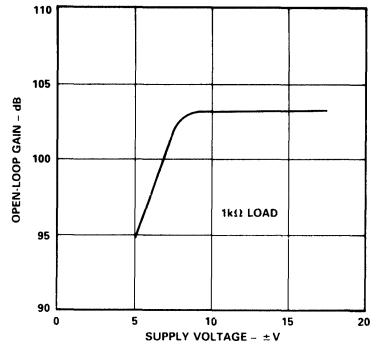


Figure 11. Open-Loop Gain vs. Supply Voltage

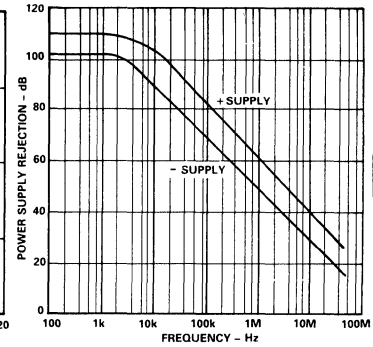


Figure 12. Power Supply Rejection vs. Frequency

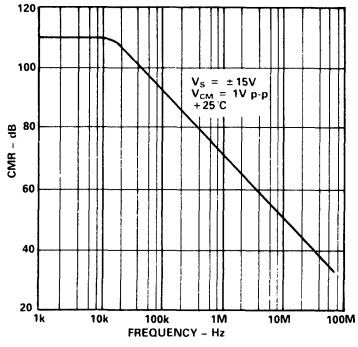


Figure 13. Common-Mode Rejection vs. Frequency

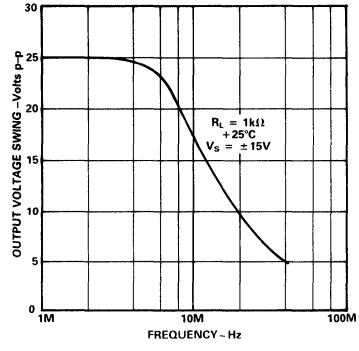


Figure 14. Large Signal Frequency Response

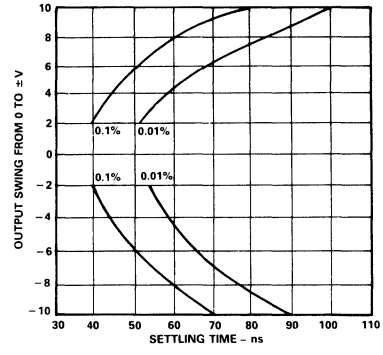


Figure 15. Output Swing and Error vs. Settling Time

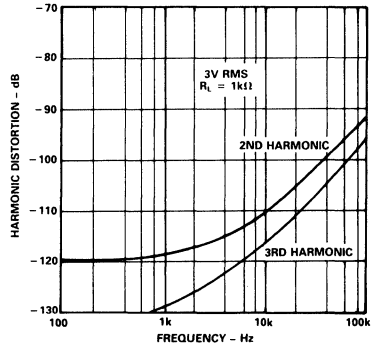


Figure 16. Harmonic Distortion vs. Frequency

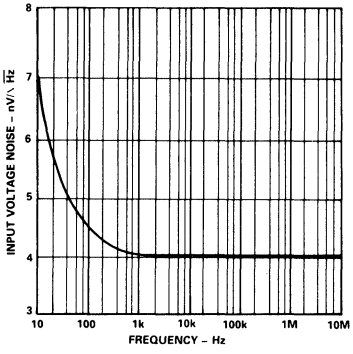


Figure 17. Input Voltage Noise Spectral Density

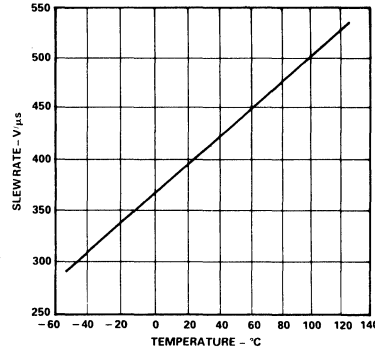


Figure 18. Slew Rate vs. Temperature

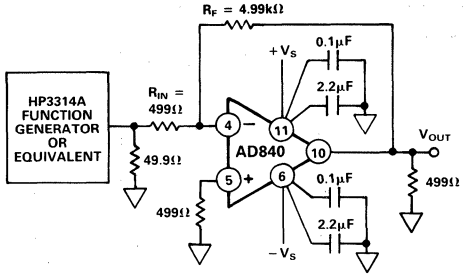


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

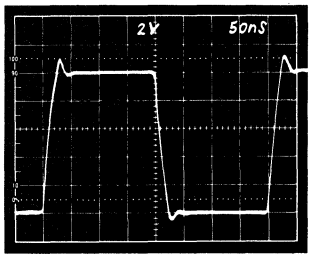


Figure 19b. Inverter Large Signal Pulse Response

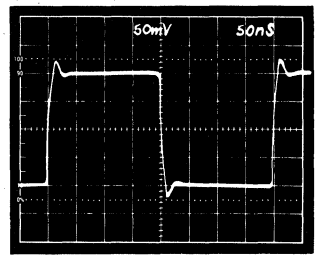


Figure 19c. Inverter Small Signal Pulse Response

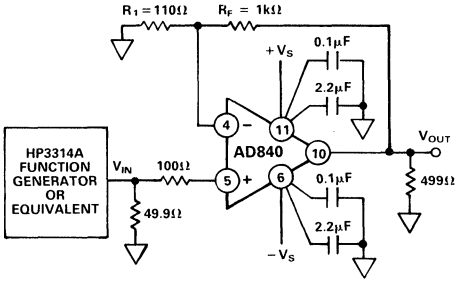


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

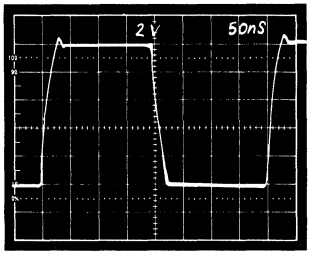


Figure 20b. Noninverting Large Signal Pulse Response

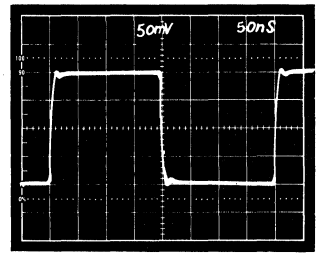


Figure 20c. Noninverting Small Signal Pulse Response

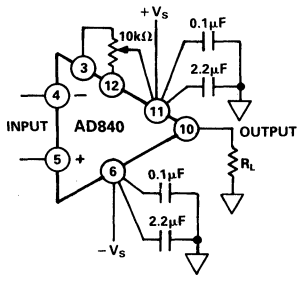


Figure 21. Offset Nulling (DIP Pinout)

OFFSET NULLING

The input offset voltage of the AD840 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

AD840 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD840 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

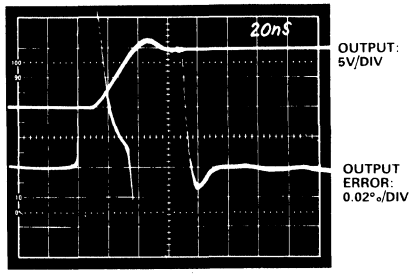


Figure 22. AD840 0.01% Settling Time

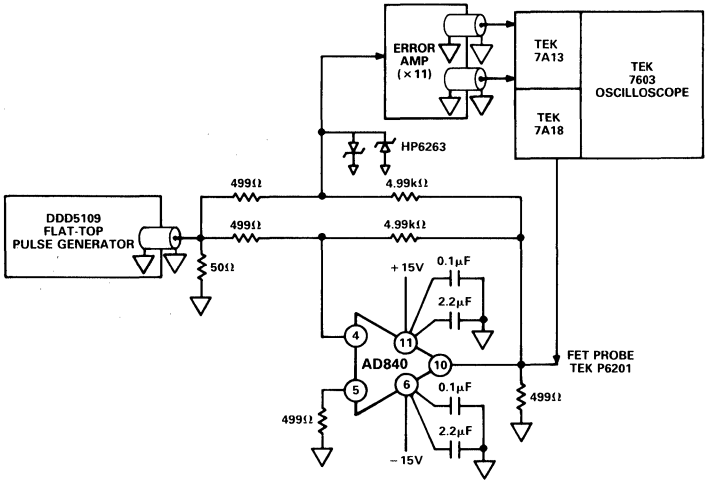


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD840's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 420 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp amplifies the error from the false summing junction by 11, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long-term" stability of the settling characteristics of the AD840 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

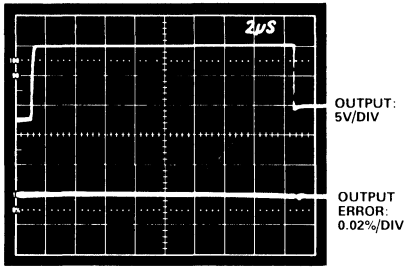


Figure 24. AD840 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD840, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided, because the increased inter-lead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (±10 pF) feedback capacitor in connected parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD840 is sensitive to capacitive loading. The AD840 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF. A resistor in series with the output can be used to decouple larger capacitive loads.

USING A HEAT SINK

The AD840 draws less quiescent power than most high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

HIGH SPEED DAC BUFFER CIRCUIT

The AD840's 100 ns settling time to 0.01% for a 10 V step makes it well suited as an output buffer for high speed D/A converters. Figure 25 shows the connections for producing a 0 to +10.24 V output swing from the AD568 35 ns DAC. With the AD568 in unbuffered voltage output mode, the AD840 is placed in noninverting configuration. As a result of the 1 kΩ span resistor provided internally in the AD568, the noise gain of this topology is 10. Only 5 pF is required across the feedback (span) resistor to optimize settling.

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD840. Typical recovery time is 190 ns from negative overdrive and 350 ns from positive overdrive.

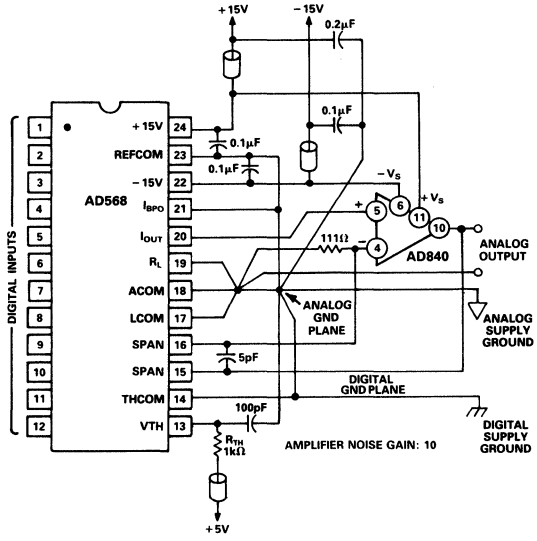


Figure 25. 0 to +10.24 V DAC Output Buffer

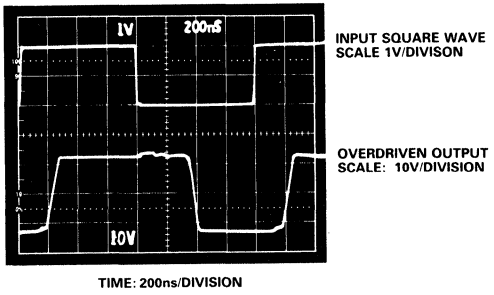


Figure 26. Overdrive Recovery

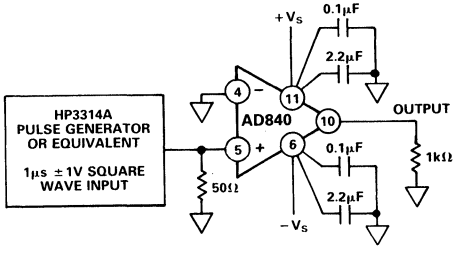


Figure 27. Overdrive Recovery Test Circuit

Wideband, Unity-Gain Stable, Fast Settling Op Amp

AD841

FEATURES

AC PERFORMANCE

Unity-Gain Bandwidth: 40 MHz

Fast Settling: 110 ns to 0.01%

Slew Rate: 300 V/μs

Full Power Bandwidth: 4.7 MHz for 20 V p–p into a 500 Ω Load

DC PERFORMANCE

Input Offset Voltage: 1 mV max

Input Voltage Noise: 13 nV/$\sqrt{Hz}$ typ

Open-Loop Gain: 45V/mV into a 1 kΩ Load

Output Current: 50 mA min

Supply Current: 12 mA max

APPLICATIONS

High Speed Signal Conditioning

Video and Pulse Amplifiers

Data Acquisition Systems

Line Drivers

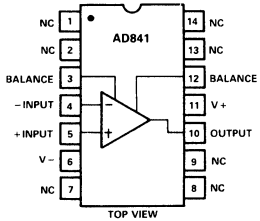
Active Filters

Available in 14-Pin Plastic DIP, Plastic SOIC, Hermetic Cerdip and TO-8 Metal Can Packages and Chip Form

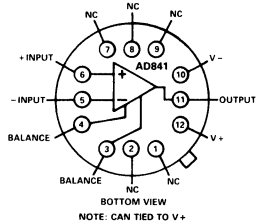
Chips and MIL-STD-883B Parts Available

AD841 CONNECTION DIAGRAMS

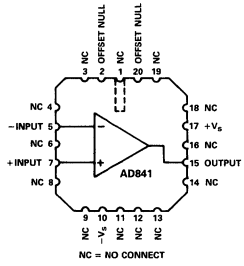
Plastic DIP (N) Package and Cerdip (Q) Package



TO-8 (H) Package



LCC (E) Package



PRODUCT DESCRIPTION

The AD841 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD840, which is stable at a gain of 10 or greater, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 40 MHz unity-gain bandwidth product, the AD841 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 110 ns for a 10 volt step.

Unlike many high frequency amplifiers, the AD841 requires no external compensation. It remains stable over its full operating temperature range. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capablity of 50 mA, a low input voltage noise of 13 nV/$\sqrt{Hz}$ and low input offset voltage of 1 mV maximum.

The 300 V/μs slew rate of the AD841, along with its 40 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is well suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD841 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD841 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD841 make it ideal for DAC and ADC buffers, and all types of video instrumentation circuitry.
2. The AD841 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth performance previously available only in hybrids.
3. The AD841's thermally balanced layout and the speed of the CB process allow the AD841 to settle to 0.01% in 110 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 1 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. The AD841 is an enhanced replacement for the HA2541.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD841J Min	AD841J Typ	AD841J Max	AD841K Min	AD841K Typ	AD841K Max	AD841S Min	AD841S Typ	AD841S Max	Units
INPUT OFFSET VOLTAGE[1]			0.8	**2.0**		0.5	**1.0**		0.5	**2.0**	mV
	T_{min}–T_{max}			5.0			**3.3**			5.5	mV
Offset Drift			35			35			35		µV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	µA
	T_{min}–T_{max}			10			**6**			**12**	µA
Input Offset Current			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	µA
	T_{min}–T_{max}			0.5			**0.3**			**0.6**	µA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			200			200			200		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**± 10**	12		**±10**	12		**±10**	12		V
Common Mode Rejection	V_{CM} = ±10 V	**86**	100		**103**	109		**86**	100		dB
	T_{min}–T_{max}	80			**100**			80			dB
INPUT VOLTAGE NOISE	f = 1 kHz		15			15			15		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		47			47			47		µV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**25**	45		**25**	45		**25**	45		V/mV
	T_{min}–T_{max}	12			**20**			**12**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω										
	T_{min}–T_{max}	±10			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
OUTPUT RESISTANCE	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p–p		40			40			40		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	R_{LOAD}≥500 Ω	3.1	4.7		3.1	4.7		3.1	4.7		MHz
Rise Time[3]	A_V = −1		10			10			10		ns
Overshoot[3]	A_V = −1		10			10			10		%
Slew Rate[3]	A_V = −1	200	300		200	300		200	300		V/µs
Settling Time – 10 V Step	A_V = −1										
	to 0.1%		90			90			90		ns
	to 0.01%		110			110			110		ns
OVERDRIVE RECOVERY	−Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.03			0.03			0.03		%
Differential Phase	f = 4.4 MHz		0.022			0.022			0.022		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			11	**12**		11	**12**		11	**12**	mA
	T_{min}–T_{max}			14			**14**			**16**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	**86**	100		**90**	100		**86**	100		dB
	T_{min}–T_{max}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[5]											
LCC (E-20A)[6]									AD841SE		
Cerdip (Q-14)			AD841JQ			AD841KQ			AD841SQ		
Plastic (N-14)			AD841JN			AD841KN					
TO-8 (H-12)			AD841JH			AD841KH			AD841SH		
J and S Grade Chips Also Available			AD841J CHIP						AD841S CHIP		

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = Slew Rate/2π V_{PEAK}.

[3]Refer to Figure 19.

[4]"S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

[5]See Section 20 for package outline information.

[6]Contact factory for availability.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
TO-8 (H) . . . . . 1.4 W
Plastic (N) . . . . . 1.5 W
Cerdip (Q) . . . . . 1.3 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Q, H . . . . . −65°C to +150°C
N . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

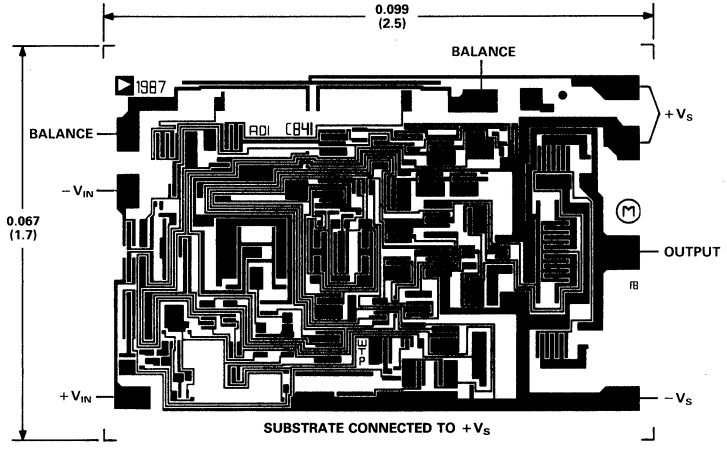
Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}	
Cerdip Package	35°C/W	110°C/W	38°C/W	Recommended Heat Sink:
TO-8 Package	30°C/W	100°C/W	37°C/W	Aavid Engineering ©#602B
Plastic Package	30°C/W	95°C/W		

2

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics (at +25°C and $V_S = \pm 15$ V, unless otherwise noted.

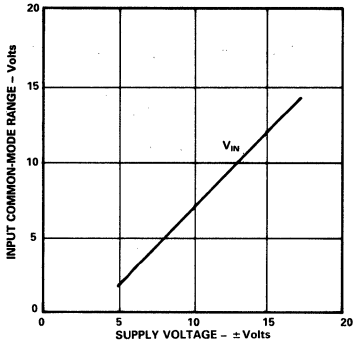


Figure 1. Input Common-Mode Range vs. Supply Voltage

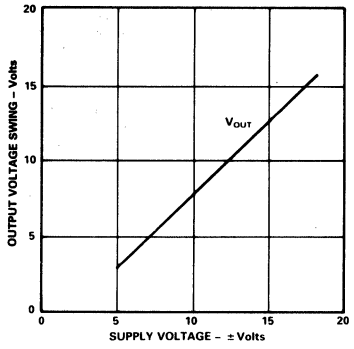


Figure 2. Output Voltage Swing vs. Supply Voltage

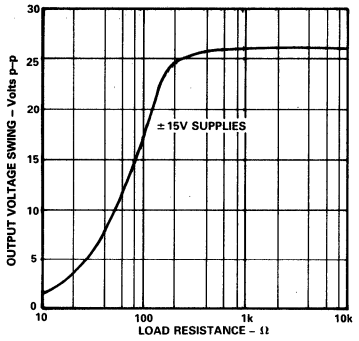


Figure 3. Output Voltage Swing vs. Load Resistance

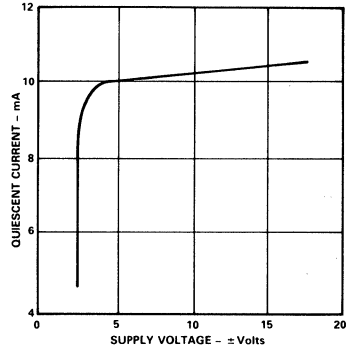


Figure 4. Quiescent Current vs. Supply Voltage

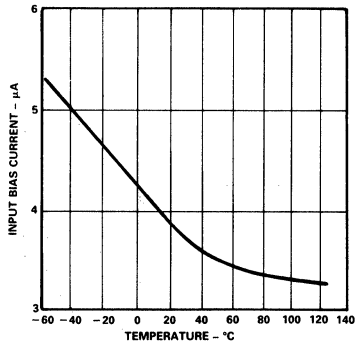


Figure 5. Input Bias Current vs. Temperature

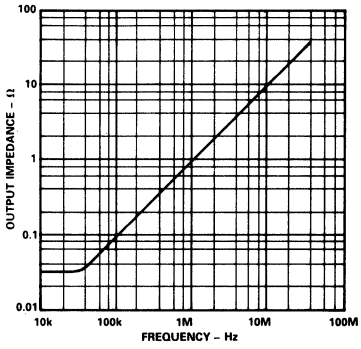


Figure 6. Output Impedance vs. Frequency

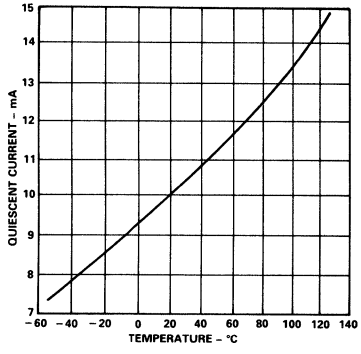


Figure 7. Quiescent Current vs. Temperature

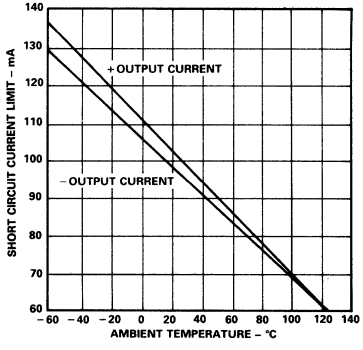


Figure 8. Short-Circuit Current Limit vs. Temperature

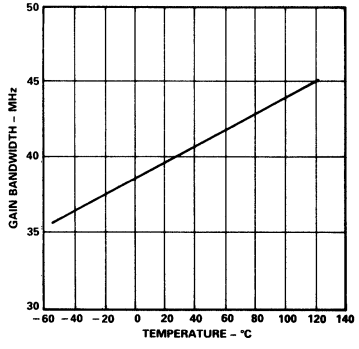


Figure 9. Gain Bandwidth Product vs. Temperature

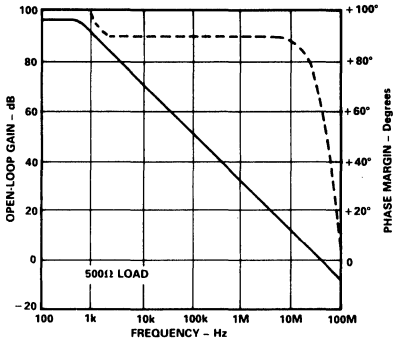


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

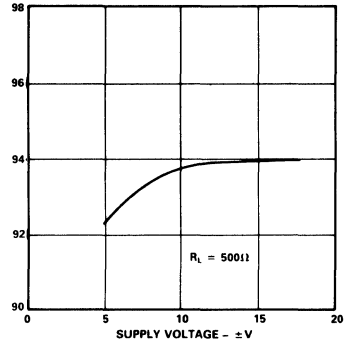


Figure 11. Open-Loop Gain vs. Supply Voltage

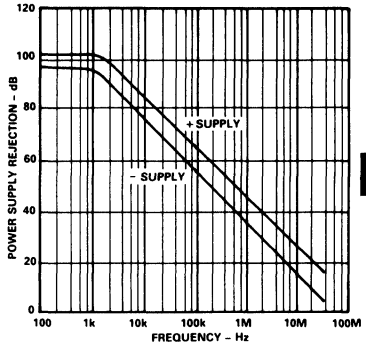


Figure 12. Power Supply Rejection vs. Frequency

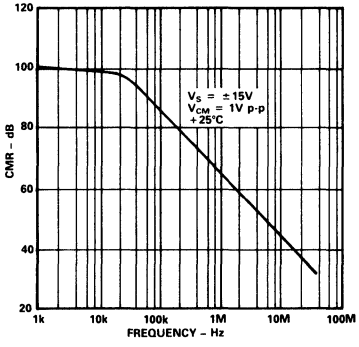


Figure 13. Common-Mode Rejection vs. Frequency

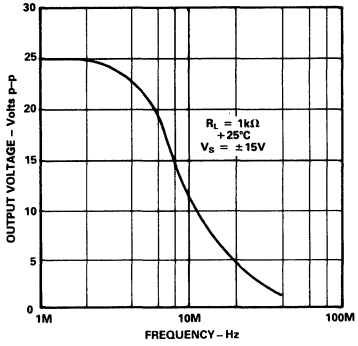


Figure 14. Large Signal Frequency Response

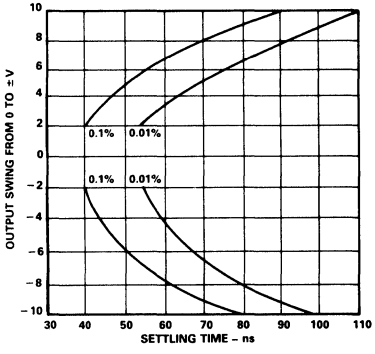


Figure 15. Output Swing and Error vs. Settling Time

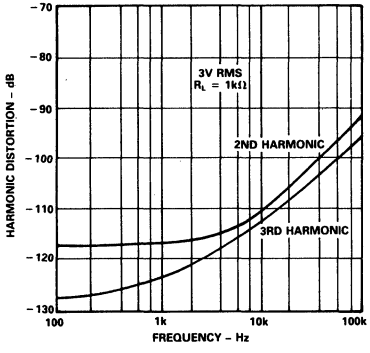


Figure 16. Harmonic Distortion vs. Frequency

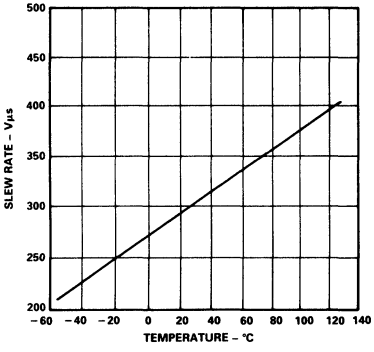


Figure 17. Slew Rate vs. Temperature

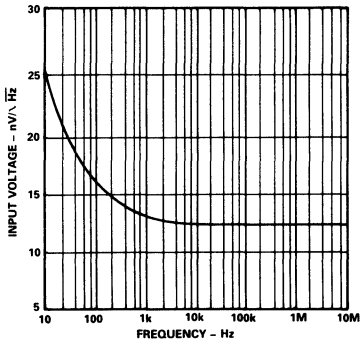


Figure 18. Input Noise Voltage Spectral Density

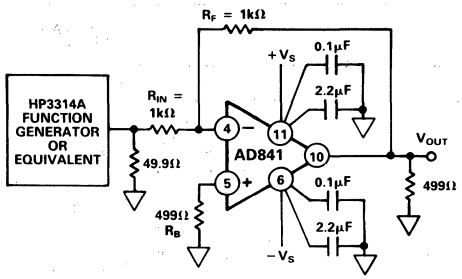


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

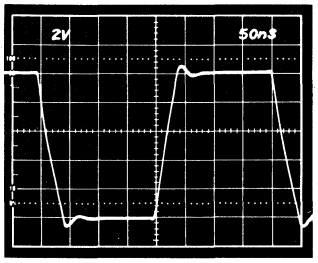


Figure 19b. Inverter Large Signal Pulse Response

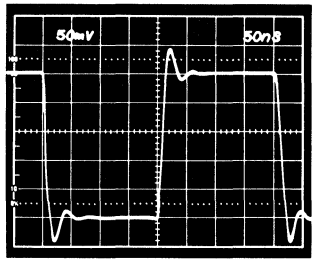


Figure 19c. Inverter Small Signal Pulse Response

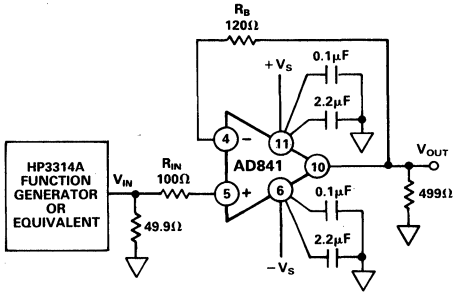


Figure 20a. Unity-Gain Buffer Amplifier Configuration (DIP Pinout)

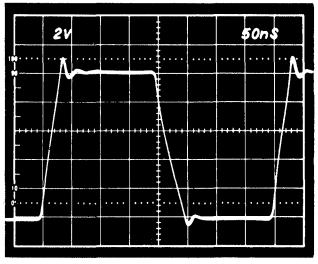


Figure 20b. Buffer Large Signal Pulse Response

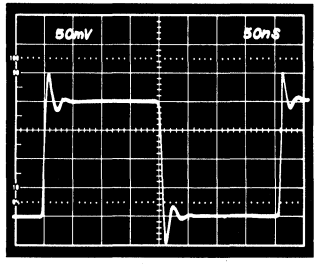


Figure 20c. Buffer Small Signal Pulse Response

OFFSET NULLING

The input offset voltage of the AD841 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

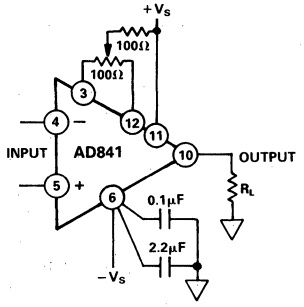


Figure 21. Offset Nulling (DIP Pinout)

INPUT CONSIDERATIONS

An input resistor (R_{IN} in Figure 20) is recommended in circuits where the input to the AD841 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into the input.

For high performance circuits it is recommended that a resistor (R_B in Figures 19 and 20) be used to reduce bias current errors by matching the impedance at each input. The output voltage error caused by the offset current is more than an order of magnitude less than the error present if the bias current error is not removed.

AD841 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD841 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing and (4) linear settling to within the specified error band.

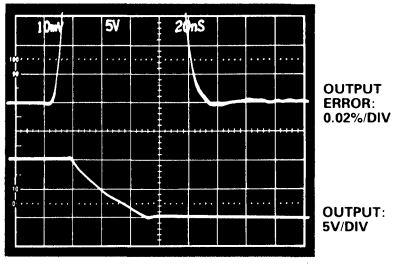


Figure 22. AD841 0.01% Settling Time

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

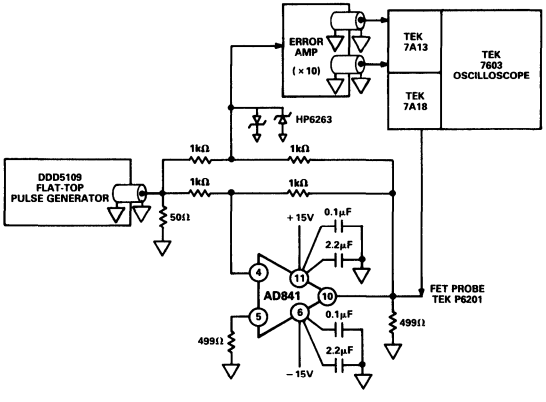


Figure 23. Settling Time Test Circuit

Measurement of the AD841's 0.01% settling in 110 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 500 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 10, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long term" stability of the settling characteristics of the AD841 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

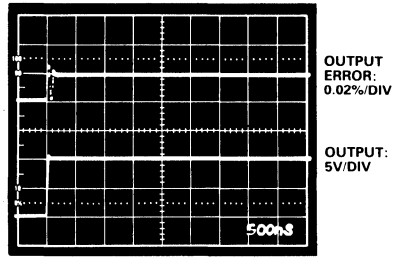


Figure 24. AD841 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD841, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD841 is sensitive to capacitive loading. The AD841 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF (for a unity-gain follower). A resistor in series with the output can be used to decouple larger capacitive loads.

Figure 25 shows a typical configuration for driving a large capacitive load. The 51 Ω output resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 51 Ω resistor and the load capacitance, C_L.

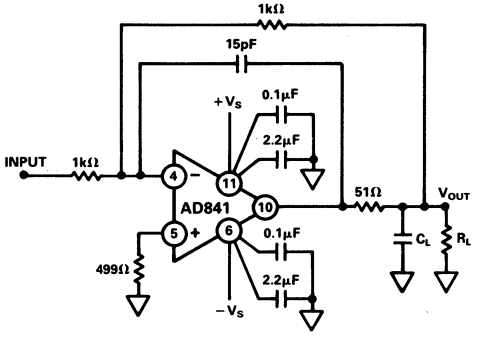


Figure 25. Circuit for Driving a Large Capacitive Load

USING A HEAT SINK

The AD841 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

TERMINATED LINE DRIVER

The AD841 functions very well as a high speed line driver of either terminated or unterminated cables. Figure 26 shows the AD841 driving a doubly terminated cable in a follower configuration. The AD841 maintains a typical slew rate of 300 V/μs, which means it can drive a ±10 V, 4.7 MHz signal or a ±3 V, 15.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD841 output and the cable in order to damp any stray signals caused by a mismatch between R_T and the cable's characteristic impedance.This will result in a "cleaner" signal, but since 1/2 the output voltage will be dropped across R_{BT}, the op amp must supply double the output signal required if there is no back termination. Therefore the full power bandwidth is cut in half.

If termination is not used, cables appear as capacitive loads. If this capacitive load is large, it should be decoupled from the AD841 by a resistor in series with the output (see above: Driving a Capacitive Load).

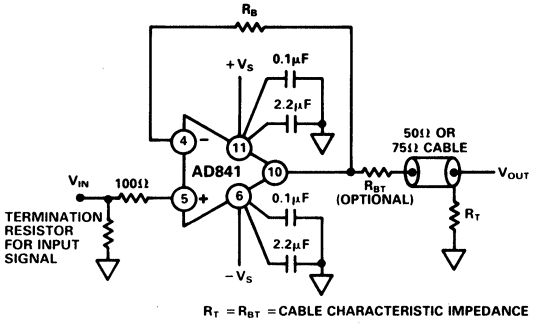


Figure 26. Line Driver Configuration

OVERDRIVE RECOVERY

Figure 27 shows the overdrive recovery capability of the AD841. Typical recovery time is 200 ns from negative overdrive and 700 ns from positive overdrive.

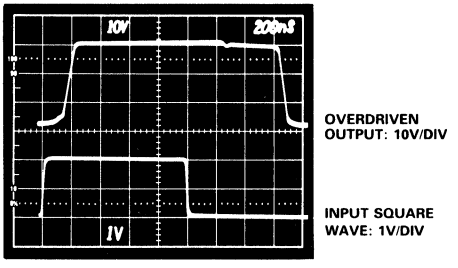


Figure 27. Overdrive Recovery

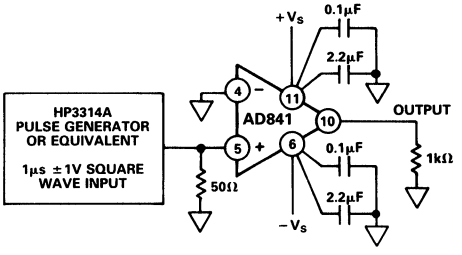


Figure 28. Overdrive Recovery Test Circuit

Wideband, High Output Current, Fast Settling Op Amp

AD842

FEATURES

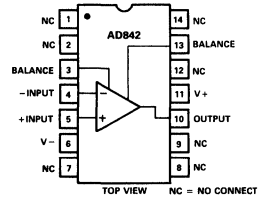
AC PERFORMANCE
- Gain Bandwidth Product: 80 MHz (Gain = 2)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 375 V/μs
- Stable at Gains of 2 or Greater
- Full Power Bandwidth: 6.0 MHz for 20 V p–p

DC PERFORMANCE
- Input Offset Voltage: 1 mV max
- Input Offset Drift: 14 μV/°C
- Input Voltage Noise: 9 nV/$\sqrt{Hz}$ typ
- Open-Loop Gain: 90 V/mV into a 500 Ω Load
- Output Current: 100 mA min
- Quiescent Supply Current: 14 mA max

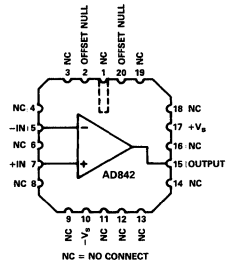
APPLICATIONS
- Line Drivers
- DAC and ADC Buffers
- Video and Pulse Amplifiers
- Available in Plastic DIP and Hermetic Metal Can, Hermetic Cerdip Packages and in Chip Form
- MIL-STD-883B Parts Available

AD842 CONNECTION DIAGRAMS

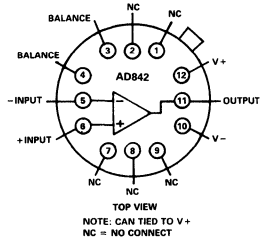
Plastic DIP (N) Package and Cerdip (Q) Package



TO-8 (H) Package



LCC (E) Package



PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80 MHz gain bandwidth, the AD842 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 100 ns for a 10 volt step.

The AD842 also offers a low quiescent current of 13 mA, a high output current drive capability (100 mA minimum), a low input voltage noise of 9 nV$\sqrt{Hz}$ and a low input offset voltage (1 mV maximum).

The 375 V/μs slew rate of the AD842, along with its 80 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffers amplifiers, lines drivers and all types of video instrumentation circuitry.
2. The AD842 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser-wafer trimming reduces the input offset voltage of 1 mV max, thus eliminating the need for external offset nulling in many applications.
4. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD842J Min	AD842J Typ	AD842J Max	AD842K Min	AD842K Typ	AD842K Max	AD842S Min	AD842S Typ	AD842S Max	Units
INPUT OFFSET VOLTAGE[1]			0.5	1.5		0.3	**1.0**		0.5	1.5	mV
	T_{min}–T_{max}			2.5			**1.5**			3.5	mV
Offset Drift			14			14			14		µV/°C
INPUT BIAS CURRENT			4.2	**8**		3.5	**5**		4.2	**8**	µA
	T_{min}–T_{max}			10			**6**			**12**	µA
Input Offset Current			0.1	**0.4**		0.05	**0.2**		0.1	**0.4**	µA
	T_{min}–T_{max}			0.5			**0.3**			**0.6**	µA
INPUT CHARACTERISTICS											
Input Resistance	Differential Mode		100			100			100		kΩ
Input Capacitance			2.0			2.0			2.0		pF
INPUT VOLTAGE RANGE											
Common Mode		**± 10**			**±10**			**±10**			V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	115		**90**	115		**86**	115		dB
	T_{min}–T_{max}	80			**86**			**80**			dB
INPUT VOLTAGE NOISE	f = 1 kHz		9			9			9		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		28			28			28		µV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**40**	90		**50**	90		**40**	90		V/mV
	T_{min}–T_{max}	20			**25**			**20**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**± 10**			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**100**			**100**			**100**			mA
	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV		80			80			80		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	R_{LOAD}≥500 Ω	4.7	6		4.7	6		4.7	6		MHz
Rise Time[3]	A_{VCL} = −2		10			10			10		ns
Overshoot[3]	A_{VCL} = −2		20			20			20		%
Slew Rate[3]	A_{VCL} = −2	300	375		300	375		300	375		V/µs
Settling Time[3]	10 V Step										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
Differential Gain	f = 4.4 MHz		0.015			0.015			0.015		%
Differential Phase	f = 4.4 MHz		0.035			0.035			0.035		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			13	**14**		13	**14**		13	**14**	mA
	T_{min}–T_{max}			16			**16**			**19**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V	**86**	100		**90**	105		**86**	100		dB
	T_{min}–T_{max}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[5]											
Plastic (N-14)			AD842JN			AD842KN					
Cerdip (Q-14)			AD842JQ			AD842KQ			AD842SQ		
TO-8 (H-12A)			AD842JH			AD842KH			AD842SH		
LCC[6] (E-20A)									AD842SE		
J and S Grade Chips Also Available											

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]FPBW Slew Rate/2π V_{PEAK}.

[3]Refer to Figures 22 and 23.

[4]"S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

[5]See Section 20 for package outline information.

[6]Contact factory for availability.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic (N) . . . . . 1.5 W
  Cerdip (Q) . . . . . 1.1 W
  TO-8 . . . . . 1.3 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
  Q, H . . . . . −65°C to +150°C
  N . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +150°C at an ambient temperature of +25°C.

Thermal Characteristics:

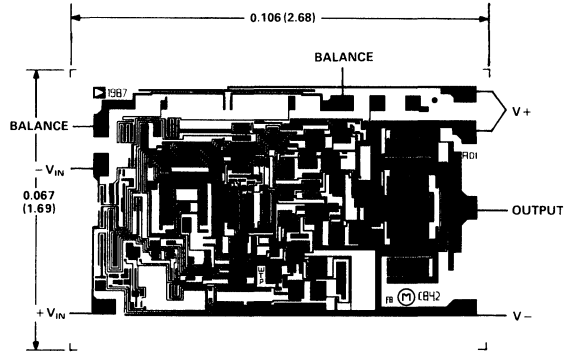
	θ_{JC}	θ_{JA}	θ_{SA}
Plastic Package	33°C/W	85°C/W	
Cerdip Package	35°C/W	110°C/W	38°C/W
TO-8 Package	30°C/W	100°C/W	27°C/W

Recommended heat sink: Aavid Engineering© #602B

2

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted.)

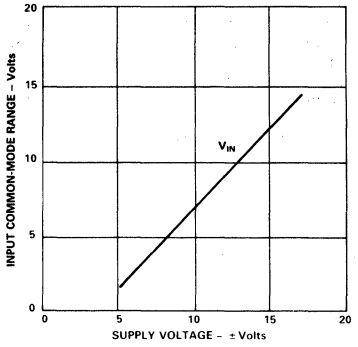


Figure 1. Input Common-Mode Range vs. Supply Voltage

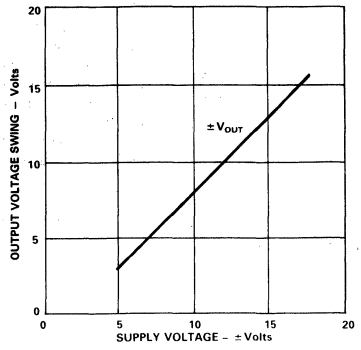


Figure 2. Output Voltage Swing vs. Supply Voltage

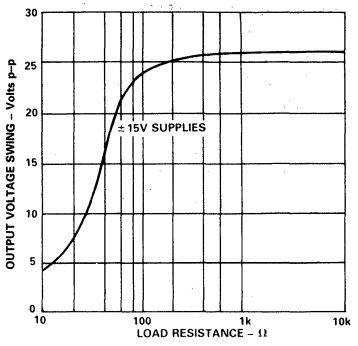


Figure 3. Output Voltage Swing vs. Load Resistance

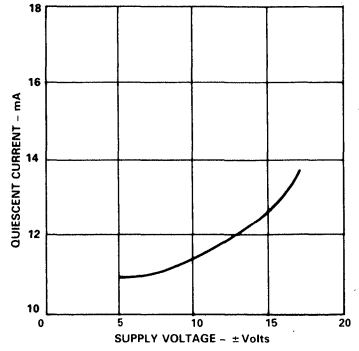


Figure 4. Quiescent Current vs. Supply Voltage

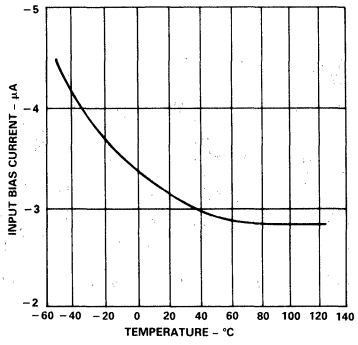


Figure 5. Input Bias Current vs. Temperature

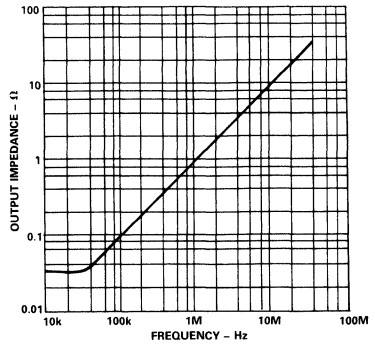


Figure 6. Output Impedance vs. Frequency

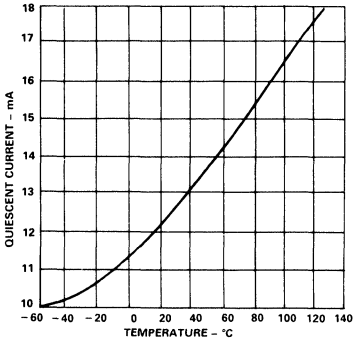


Figure 7. Quiescent Current vs. Temperature

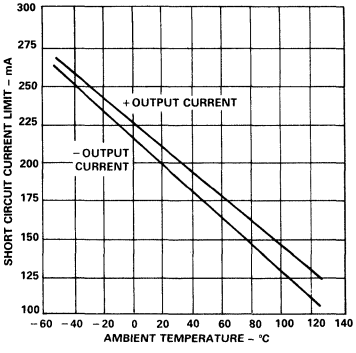


Figure 8. Short-Circuit Current Limit vs. Temperature

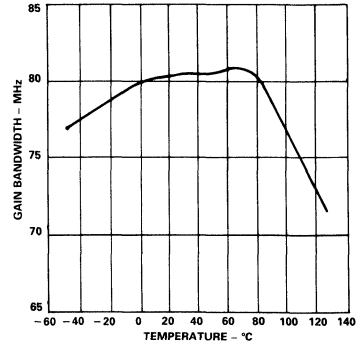


Figure 9. Gain Bandwidth Product vs. Temperature

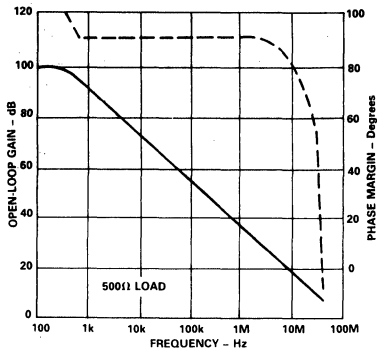


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

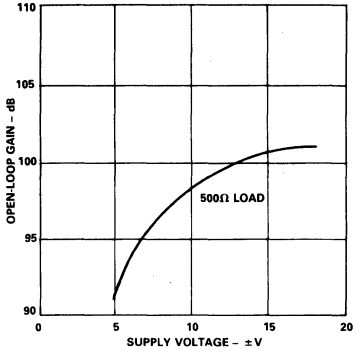


Figure 11. Open-Loop Gain vs. Supply Voltage

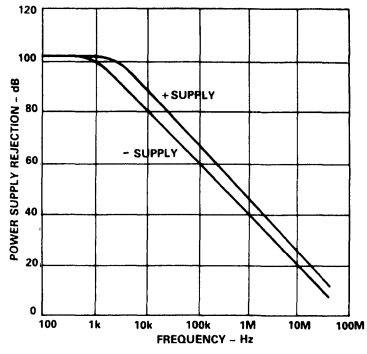


Figure 12. Power Supply Rejection vs. Frequency

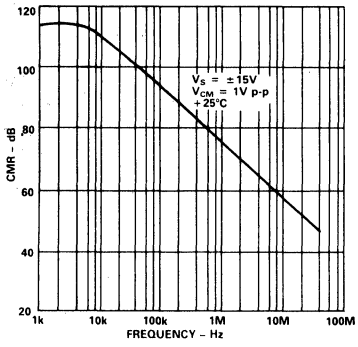


Figure 13. Common-Mode Rejection vs. Frequency

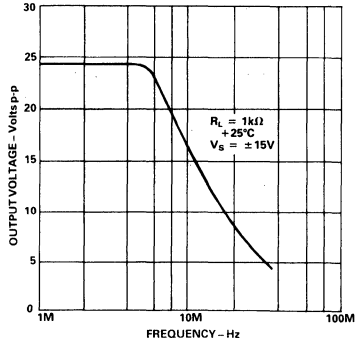


Figure 14. Large Signal Frequency Response

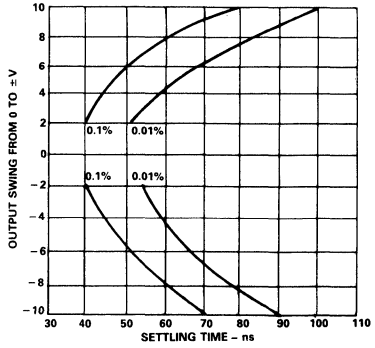


Figure 15. Output Swing and Error vs. Settling Time

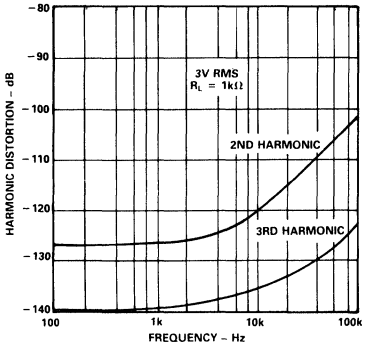


Figure 16. Harmonic Distortion vs. Frequency

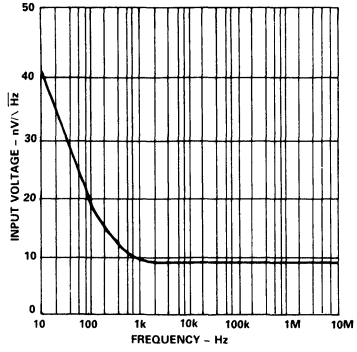


Figure 17. Input Voltage vs. Frequency

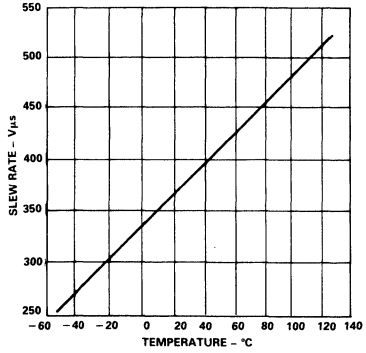


Figure 18. Slew Rate vs. Temperature

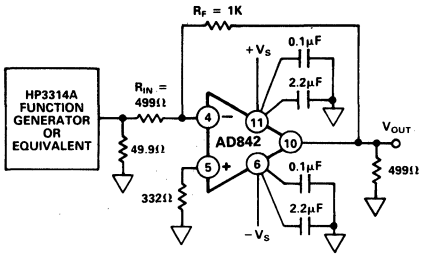


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

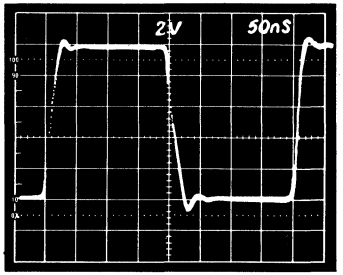


Figure 19b. Inverter Large Signal Pulse Response

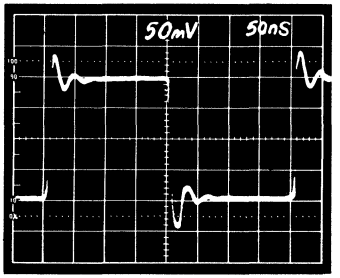


Figure 19c. Inverter Small Signal Pulse Response

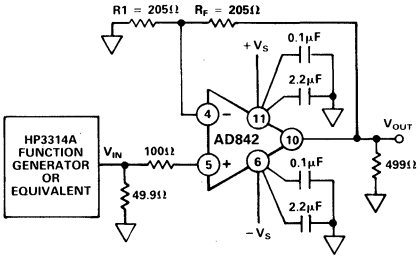


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

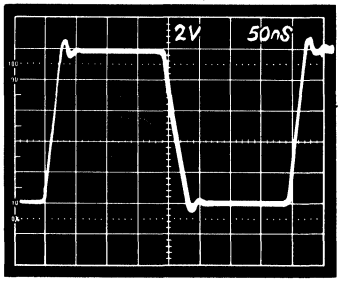


Figure 20b. Noninverting Large Signal Pulse Response

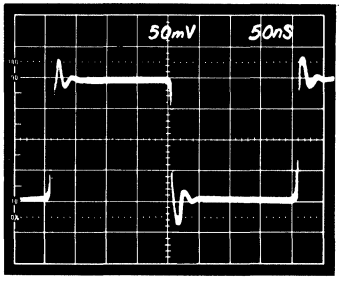


Figure 20c. Noninverting Small Signal Pulse Response

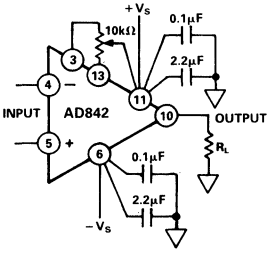


Figure 21. Offset Nulling (DIP Pinout)

OFFSET NULLING

The input offset voltage of the AD842 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

AD842 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD842 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include: (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

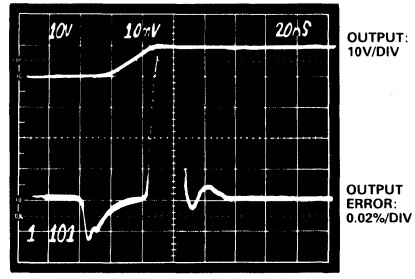


Figure 22. AD842 0.01% Settling Time

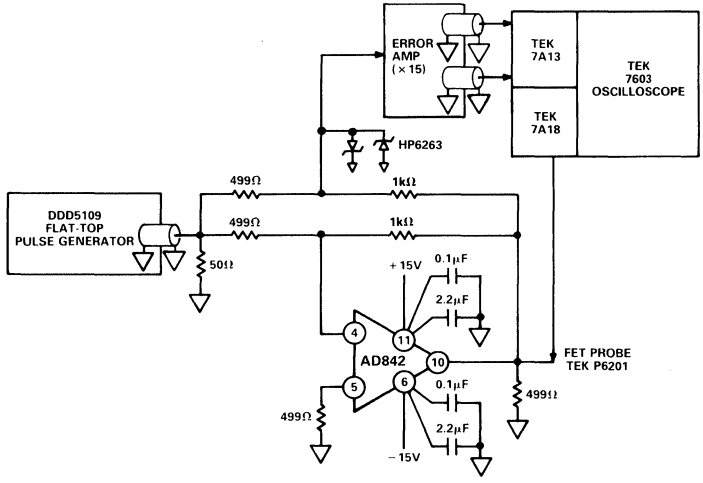


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD842's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high-speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 300 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 15, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long term" stability of the settling characteristics of the AD842 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

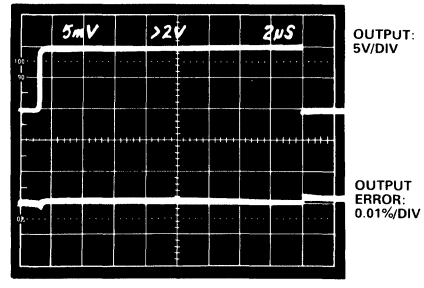


Figure 24. AD842 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD842, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Applying the AD842

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor connected in parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD842 is sensitive to capacitive loading. The AD842 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF.

USING A HEAT SINK

The AD842 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 10 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

TERMINATED LINE DRIVER

The AD842 is optimized for high speed line driver applications. Figure 25 shows the AD842 driving a doubly terminated cable in a gain-of-2 follower configuration. The AD842 maintains a typical slew rate of 375 V/μs, which means it can drive a ±10 V, 6.0 MHz signal or a ±3 V, 19.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD842 output and the cable in order to damp any stray signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a "cleaner" signal. With this circuit, the voltage on the line equals V_{IN} because one half of V_{OUT} is dropped across R_{BT}.

The AD842 has ±100 mA minimum output current and, therefore, can drive ±5 V into a 50 Ω cable.

The feedback resistors, R_1 and R_2, must be chosen carefully. Large value resistors are desirable in order to limit the amount of current drawn from the amplifier output. But large resistors can cause amplifier instability because the parallel resistance $R_1 \| R_2$ combines with the input capacitance (typically 2–5 pF) to create an additional pole. Also, the voltage noise of the AD842 is equivalent to a 5 kΩ resistor, so large resistors can significantly increase the system noise. Resistor values of 1 kΩ or 2 kΩ are recommended.

If termination is not used, cables appear as capacitive loads and can be decoupled from the AD842 by a resistor in series with the output.

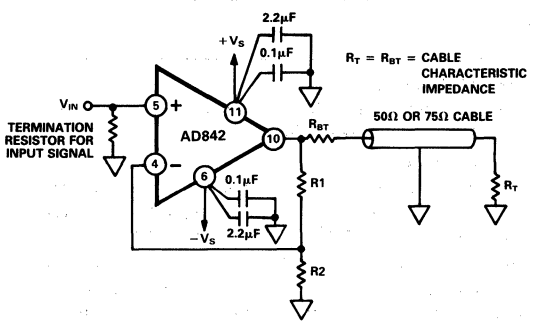


Figure 25. Line Driver Configuration

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD842. Typical recovery time is 80 ns from negative overdrive and 400 ns from positive overdrive.

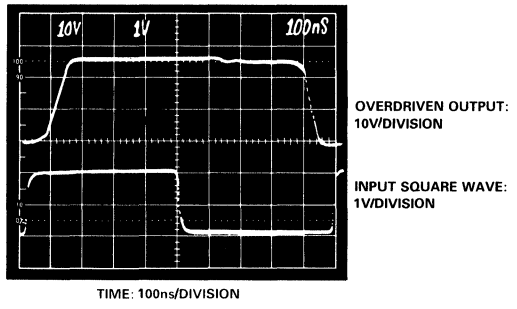


Figure 26. Overdrive Recovery

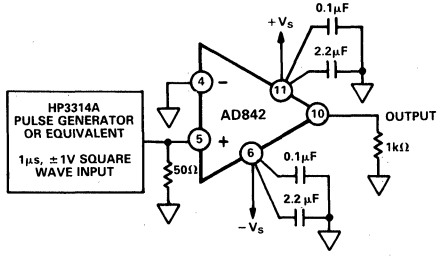


Figure 27. Overdrive Recovery Test Circuit

34 MHz, CBFET Fast Settling Op Amp

AD843

FEATURES

AC PERFORMANCE
- Unity Gain Bandwidth: 34 MHz
- Fast Settling: 135 ns to 0.01%
- Slew Rate: 250 V/μs
- Stable at Gains of 1 or Greater
- Full Power Bandwidth: 3.9 MHz

DC PERFORMANCE
- Input Offset Voltage: 1 mV max (AD843K/B)
- Input Bias Current: 0.6 nA typ
- Input Voltage Noise: 19 nV/$\sqrt{Hz}$
- Open Loop Gain: 30 V/mV into a 500 Ω Load
- Output Current: 50 mA min
- Supply Current: 13 mA max
- Available in 8-Pin Plastic Mini-DIP & Cerdip Packages and 12-Pin Hermetic Metal Cans
- Chips and MIL-STD-883B Parts Also Available

APPLICATIONS
- High Speed Sample-and-Hold Amplifiers
- High Bandwidth Active Filters
- High Speed Integrators
- High Frequency Signal Conditioning

PRODUCT DESCRIPTION

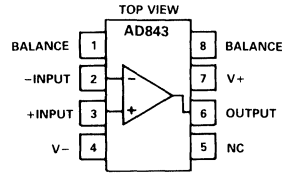
The AD843 is a fast settling, 34 MHz, CBFET input op amp. The AD843 combines the low (0.6 nA) input bias currents characteristic of a FET input amplifier while still providing a 34 MHz bandwidth and a 135 ns settling time (to within 0.01% of final value for a 10 volt step). The AD843 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp.

The 250 V/μs slew rate and 0.6 nA input bias current of the AD843 ensure excellent performance in high speed sample-and-hold applications and in high speed integrators. This amplifier is also ideally suited for high bandwidth active filters and high frequency signal conditioning circuits.

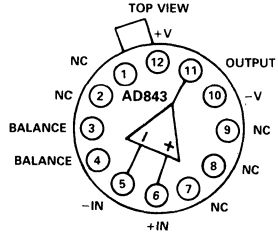
Unlike many high frequency amplifiers, the AD843 requires no external compensation and it remains stable over its full operating temperature range. It is available in five performance grades: the AD843J and AD843K are rated over the commercial temperature range of 0 to +70°C. The AD843A and AD843B are rated over the industrial temperature range of −40°C to +85°C. The AD843S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

AD843 CONNECTION DIAGRAMS

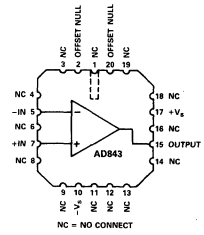
Plastic (N) Package and Cerdip (Q) Package



TO-8 (H) Package



LCC (E) Package



The AD843 is offered in either 8-pin plastic DIP or hermetic cerdip packages or in a 12-pin metal can. Chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time and low input bias current of the AD843 make it the ideal amplifier for 12-bit D/A and A/D buffers, for high speed sample-and-hold amplifiers and for high speed integrator circuits. The AD843 can replace many FET input hybrid amplifiers such as the LH0032, LH4104 and OPA600.
2. Fully differential inputs provide outstanding performance in all standard high frequency op amp applications such as signal conditioning and active filters.
3. Laser wafer trimming reduces the input offset voltage to 1 mV max (AD843K and AD843B).
4. Although external offset nulling is unneccesary in many applications, offset null pins are provided.
5. The AD843 does not require external compensation at closed loop gains of 1 or greater.

SPECIFICATIONS (@ T_A +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD843J/A Min	AD843J/A Typ	AD843J/A Max	AD843K/B Min	AD843K/B Typ	AD843K/B Max	AD843S Min	AD843S Typ	AD843S Max	Units
INPUT OFFSET VOLTAGE[1]			1.0	**2.0**		0.5	**1.0**		1.0	**2.0**	mV
	T_{min}–T_{max}		1.7	4.0		1.2	**2.0**		3.0	**4.5**	mV
Offset Drift			12			12	35		12		µV/°C
INPUT BIAS CURRENT	Initial (T_J = +25°C)		50			40			50		pA
	Warmed-Up[1]		0.8	**2.5**		0.6	**1.0**		0.8	**2.5**	nA
	T_{min}–T_{max}			60/160			23/65			2600	nA
INPUT OFFSET CURRENT	Initial (T_J = +25°C)		30			20			30		pA
	Warmed-Up[1]		0.25	**1.0**		0.2	**0.4**		0.25	**1.0**	nA
	T_{min}–T_{max}			23/64			9/26			1025	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{10}			10^{10}			10^{10}		Ω
Input Capacitance			6			6			6		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	+12, −13		**±10**	+12, −13		**±10**	+12, −13		V
COMMON MODE REJECTION	V_{CM} = ±10 V	**60**	72		**70**	76		**60**	72		dB
	T_{min}–T_{max}	60	72		**68**	76		**60**	72		dB
INPUT VOLTAGE NOISE	f = 10 kHz		19			19			19		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		60			60			60		µV rms
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**15**	25		**20**	30		**15**	30		V/mV
	T_{min}–T_{max}	10	20		**10**	25		**10**	25		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		12			12			12		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p–p		34			34			34		MHz
Full Power Bandwidth[2]	V_O = 20 V p–p										
	Rl≥500 Ω	2.5	3.9		2.5	3.9		2.5	3.9		MHz
Rise Time	A_{VCL} = −1		10			10			10		ns
Overshoot	A_{VCL} = −1		15			15			15		%
Slew Rate	A_{VCL} = −1	160	250		160	250		160	250		V/µs
Settling Time	10 V Step										
	A_{VCL} = −1										
	to 0.1%		95			95			95		ns
	to 0.01%		135			135			135		ns
Overdrive Recovery	−Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
Differential Gain	f = 4.4 MHz		0.025			0.025			0.025		%
Differential Phase	f = 4.4 MHz		0.025			0.025			0.025		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			12	**13**		12	**13**		12	**13**	mA
	T_{min}–T_{max}		12.3	14		12.3	**14**		12.5	**16**	mA
Rejection Ratio	±5 V to ±18 V	**65**	76		**70**	80		**65**	76		dB
Rejection Ratio	T_{min}–T_{max}	62	76		**68**	80		**62**	76		dB
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD843J			AD843K					
Industrial (−40°C to +85°C)			AD843A			AD843B					
Military (−55°C to +125°C)[3]									AD843S		
PACKAGE OPTIONS[4]											
Plastic (N)			AD843JN			AD843KN					
Cerdip (Q)			AD843AQ			AD843BQ			AD843SQ		
Metal Can (H)						AD843BH			AD843SH		
LCC (E)[5]									AD843SE		

NOTES
[1]Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = Slew Rate/2 πV peak.
[3]All "S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
[4]See Section 20 for package outline information.
[5]Contact factory for availability.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested on all production units.

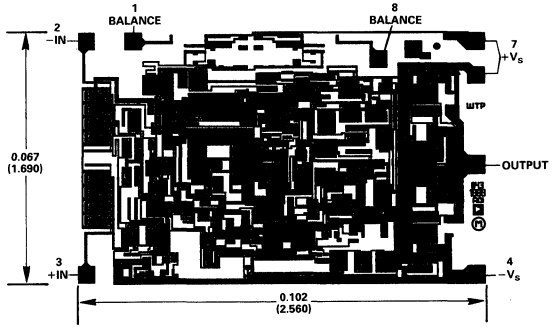
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package . . . . . 1.20 Watts
  Cerdip Package . . . . . 1.35 Watts
  12-Pin Header Package . . . . . 1.80 Watts
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range N . . . . . −65°C to +150°C
Storage Temperature Range Q . . . . . −65°C to +125°C
Operating Temperature Range
  AD843J/K . . . . . 0 to +70°C
  AD843A/B . . . . . −40°C to +85°C
  AD843S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 100°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
12-Pin Header Package: θ_{JA} = 80°C/Watt

METALIZATION PHOTOGRAPHY

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



Typical Characteristics

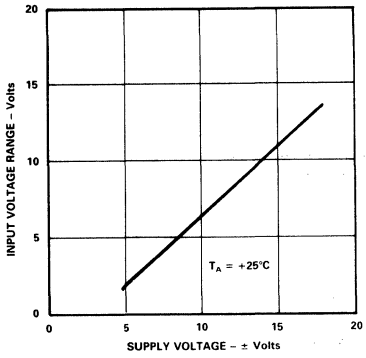


Figure 1. Input Voltage Range vs. Supply Voltage

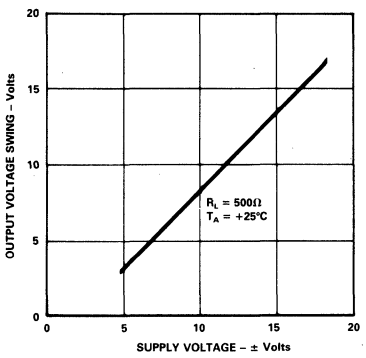


Figure 2. Output Voltage Swing vs. Supply Voltage

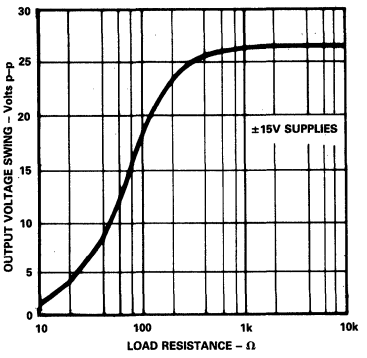


Figure 3. Output Voltage Swing vs. Load Resistance

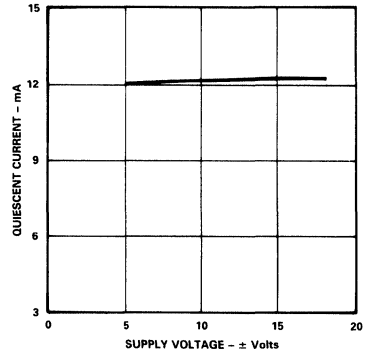


Figure 4. Quiescent Current vs. Supply Voltage

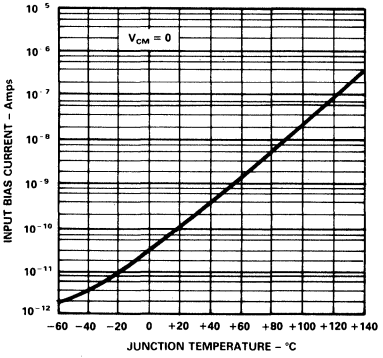


Figure 5. Input Bias Current vs. Junction Temperature

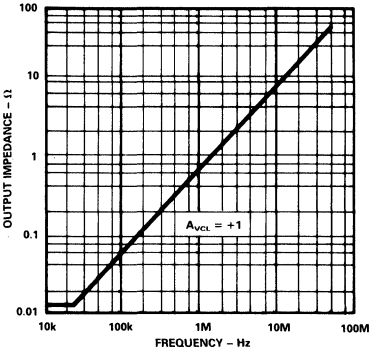


Figure 6. Output Impedance vs. Frequency

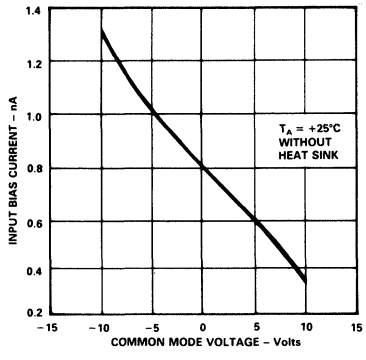


Figure 7. Input Bias Current vs. Common Mode Voltage

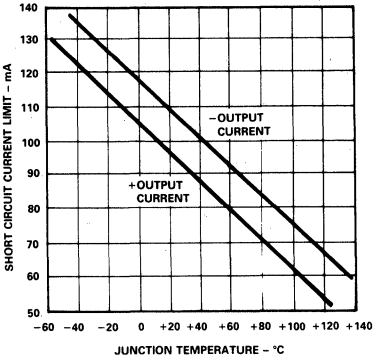


Figure 8. Short Circuit Current Limit vs. Junction Temperature (T_J)

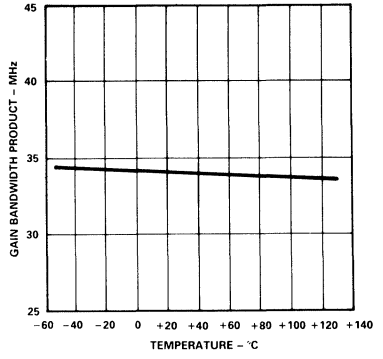


Figure 9. Gain Bandwidth Product vs. Temperature

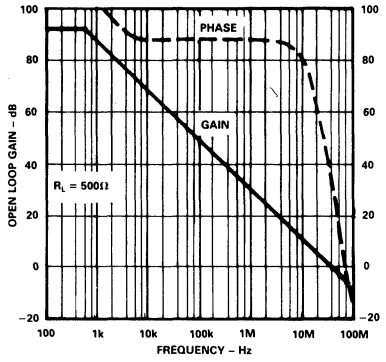


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

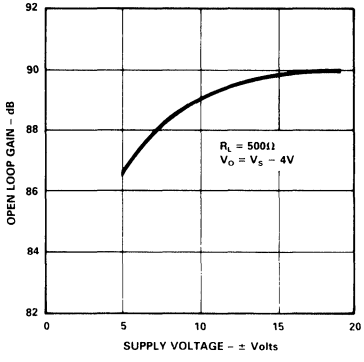


Figure 11. Open Loop Gain vs. Supply Voltage

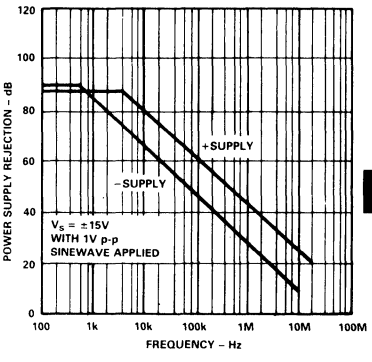


Figure 12. Power Supply Rejection vs. Frequency

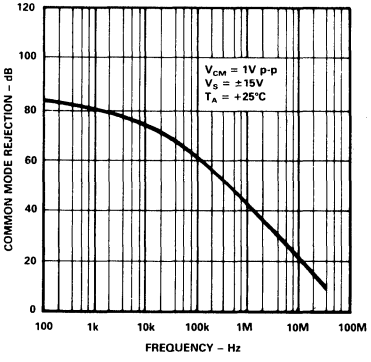


Figure 13. Common Mode Rejection vs. Frequency

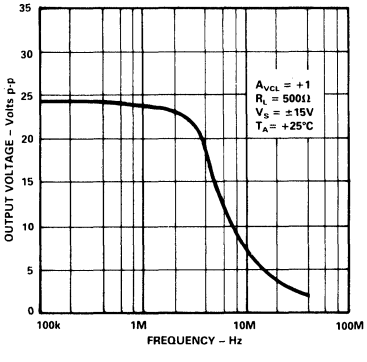


Figure 14. Large Signal Frequency Response

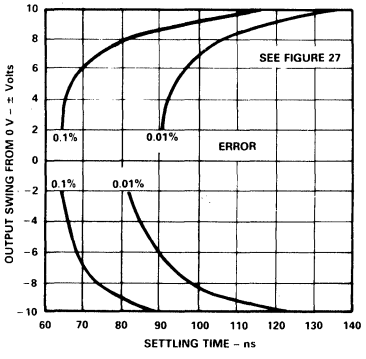


Figure 15. Output Swing and Error vs. Settling Time

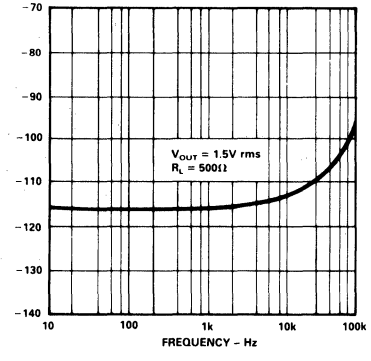


Figure 16. Harmonic Distortion vs. Frequency

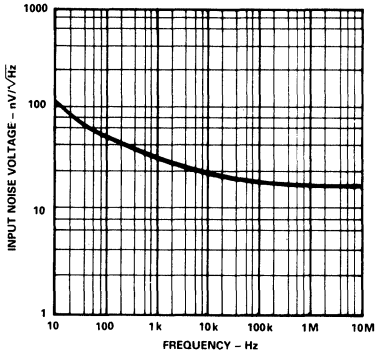


Figure 17. Input Noise Voltage Spectral Density

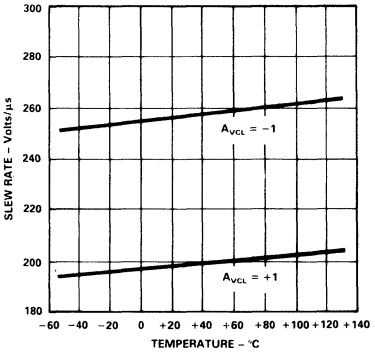


Figure 18. Slew Rate vs. Temperature

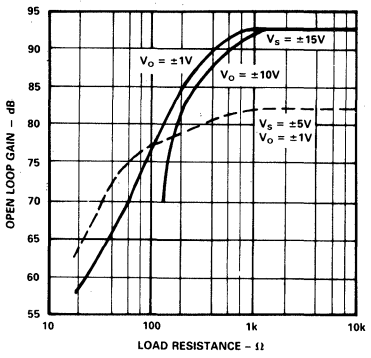


Figure 19. Open Loop Gain vs. Resistive Load

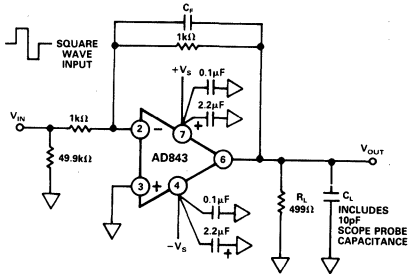


Figure 20a. Inverting Amplifier Connection

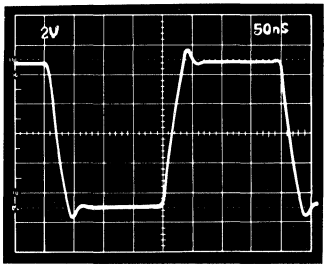


Figure 20b. Inverter Large Signal Pulse Response. C_F = 0, C_L = 10 pF

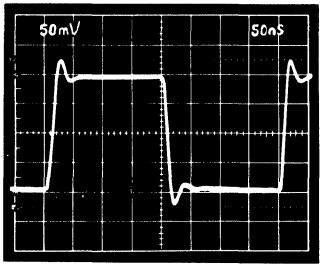


Figure 20c. Inverter Small Signal Pulse Response. C_F = 0, C_L = 10 pF

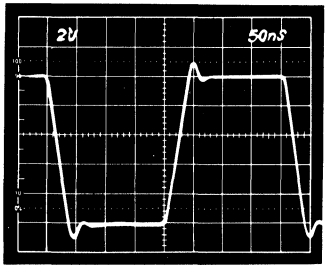


Figure 20d. Inverter Large Signal Pulse Response. C_F = 5 pF, C_L = 110 pF

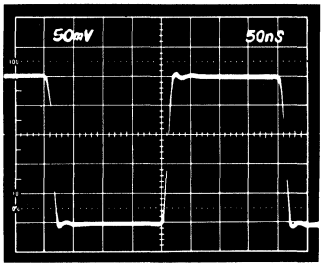


Figure 20e. Inverter Small Signal Pulse Response. C_F = 5 pF, C_L = 110 pF

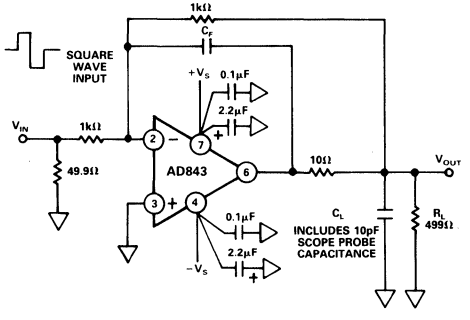


Figure 21a. Unity Gain Inverter Circuit for Driving Capacitive Loads

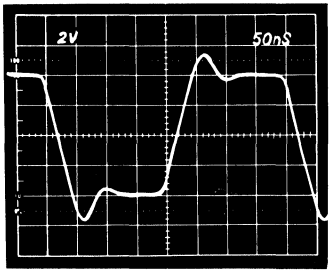


Figure 21b. Inverter Cap Load Large Signal Pulse Response. C_F = 15 pF, C_L = 410 pF

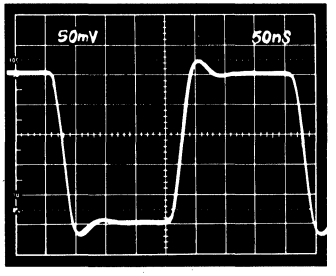


Figure 21c. Inverter Cap Load Small Signal Pulse Response. C_F = 15 pF, C_L = 410 pF

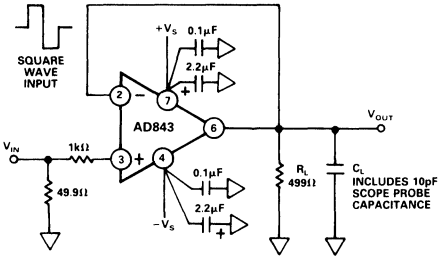


Figure 22a. Unity Gain Buffer Amplifier

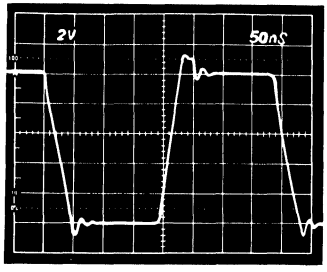


Figure 22b. Buffer Large Signal Pulse Response. C_L = 10 pF

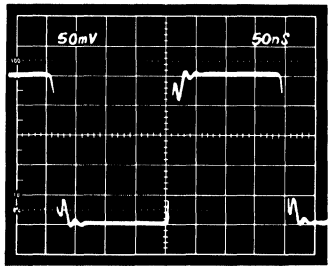


Figure 22c. Buffer Small Signal Pulse Response. C_L = 10 pF

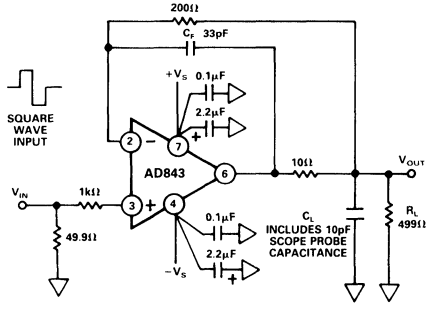


Figure 23a. Unity Gain Buffer Circuit for Driving Capacitive Loads

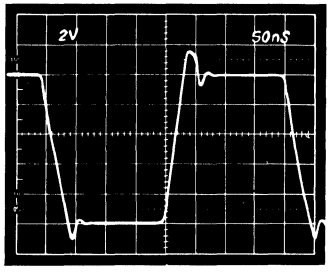


Figure 23b. Buffer Cap Load Large Signal Pulse Response. C_F = 33 pF, C_L = 10 pF

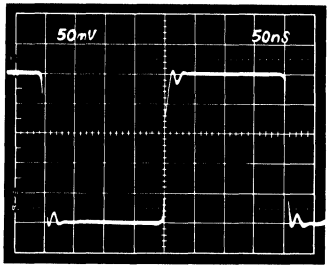


Figure 23c. Buffer Cap Load Small Signal Pulse Response. C_F = 33 pF, C_L = 10 pF

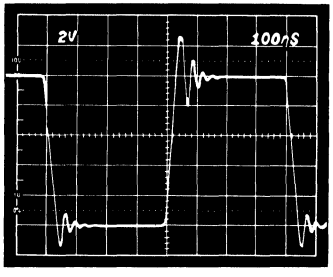


Figure 23d. Buffer Cap Load Large Signal Pulse Response. C_F = 33 pF, C_L = 110 pF

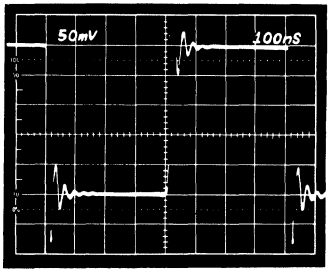


Figure 23e. Buffer Cap Load Small Signal Pulse Response. C_F = 33 pF, C_L = 110 pF

DRIVING CAPACITIVE LOADS

Like most high bandwidth amplifiers, the AD843 is sensitive to capacitive loading. Although it will drive capacitive loads up to 20 pF without degradation of its rated performance, both an increased capacitive load drive capability and a "cleaner" (non-ringing) pulse response can be obtained from the AD843 by using the circuits illustrated in Figures 20 to 23. The addition of a 5 pF feedback capacitor to the unity gain inverter connection (Figure 20a) substantially reduces the circuit's overshoot, even when it is driving a 110 pF load. This can be seen by comparing the waveforms of Figures 20b through 20e. To drive capacitive loads greater than 100 pF, the load should be decoupled from the amplifier's output by a 10 Ω resistor and the feedback capacitor, C_F, should be connected directly between the amplifier's output and its inverting input (Figure 21a). When using a 15 pF feedback capacitor, this circuit can drive 400 pF with less than 20% overshoot, as illustrated in Figures 21b and 21c. Increasing capacitor C_F to 47 pF also increases the capacitance drive capability to 1000 pF, at the expense of a 10:1 reduction in bandwidth compared with the simple unity gain inverter circuit of Figure 20a.

Unity gain voltage followers (buffers) are more sensitive to capacitive loads than are inverting amplifiers because there is no attenuation of the feedback signal. The AD843 can drive 10 pF to 20 pF when connected in the basic unity gain buffer circuit of Figure 22a.

The 1 kΩ resistor in series with the AD843's noninverting input serves two functions: first, together with the amplifier's input capacitance, it forms a low pass filter which slows down the actual signal seen by the AD843. This helps reduce ringing on the amplifier's output voltage. The resistor's second function is to limit the current into the amplifier when the differential input voltage exceeds the total supply voltage.

The AD843 will deliver a much "cleaner" pulse response when connected in the somewhat more elaborate follower circuit of Figure 23a. Note the reduced overshoot in Figure 23b and 23c as compared to Figure 22b and 22c.

For maximum bandwidth, in most applications, input and feedback resistors used with the AD843 should have resistance values equal to or less than 1.5 kΩ. Even with these low resistance values, the resultant RC time constant formed between them and stray circuit capacitances is large enough to cause peaking in the amplifier's response. Adding a small capacitor, C_F, as shown in Figures 20a to 23a will reduce this peaking and flatten the overall frequency response. C_F will normally be less than 10 pF in value.

The AD843 can drive resistive loads over the range of 500 Ω to ∞ with no change in dynamic response. While a 499 Ω load was used in the circuits of Figures 20–23, the performance of these circuits will be essentially the same even if this load is removed or changed to some other value, such as 2 kΩ.

To obtain the "cleanest" possible transient response when driving heavy capacitive loads, be sure to connect bypass capacitors directly between the power supply pins of the AD843 and ground as outlined in "grounding and bypassing."

GROUNDING AND BYPASSING

In designing practical circuits using the AD843, the user must keep in mind that some special precautions are needed when dealing with high frequency signals. Circuits must be wired using short interconnect leads. Ground planes should be used whenever possible to provide both a low resistance, low inductance circuit path and to minimize the effects of high frequency coupling. IC sockets should be avoided, since their increased interlead capacitance can degrade the bandwidth of the device.

Power supply leads should be bypassed to ground as close as possible to the pins of the amplifier. Again, the component leads should be kept very short. As shown in Figure 24, a parallel combination of a 2.2 μF tantalum and a 0.1 μF ceramic disc capacitor is recommended.

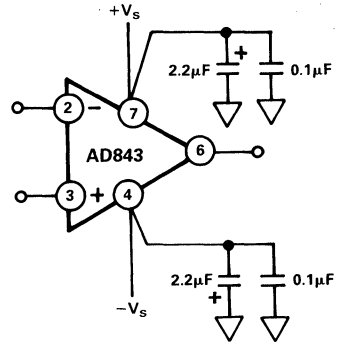
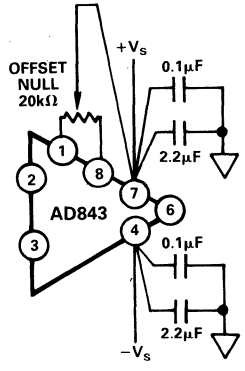


Figure 24. Recommended Power Supply Bypassing for the AD843 (DIP Pinout)

USING A HEAT SINK

The AD843 consumes less quiescent power than most precision high speed amplifiers and is specified to operate without using a heat sink. However, when driving low impedance loads, the current applied to the load can be 4 to 5 times greater than the quiescent current. This will produce a noticeable temperature rise, which will increase input bias currents. The use of a small heat sink, such as the Mouser Electronics #33HS008 is recommended.



Offset Null Configuration (DIP Pinout)

SAMPLE-AND-HOLD AMPLIFIER CIRCUITS

A Fast Switching Sample & Hold Circuit

A sample-and-hold circuit possessing short acquisition time and low aperture delay can be built using an AD843 and discrete JFET switches. The circuit of Figure 25 employs five n-channel JFETs (with turn-on times of 35 ns) and an AD843 op amp (which can settle to 0.01% in 135 ns). The circuit has an aperture delay time of 50 ns and an acquisition time of 1 μs or less.

This circuit is based on a noninverting open loop architecture, using a differential hold capacitor to reduce the effects of pedestal error. The charge that is removed from CH1 by Q2 and Q3 is offset by the charge removed from CH2 by Q4 and Q5. This circuit can tolerate low hold capacitor values (approximately 100 pF), which improve acquisition time, due to the small gate-to-drain capacitance of the discrete JFETs. Although pedestal error will vary with input signal level, making trimming more difficult, the circuit has the advantages of high bandwidth and short acquisition times. In addition, it will exhibit some nonlinearity because both amplifiers are operating with a common mode input. Amplifier A2, however, contributes less than 0.025% linearity error, due to its 72 dB common mode rejection ratio.

To make sure the circuit accommodates a wide ±10 V input range, the gates of the JFETs must be connected to a potential near the −15 V supply. The level-shift circuitry (diode D3, PNP transistor Q7, and NPN transistor Q6) shifts the TTL-level S/H command to provide for an adequate pinch-off voltage for the JFET switches over the full input voltage range.

The JFETs Q2, Q3, Q4 and Q5 across the two hold capacitors ensure signal acquisition for all conditions of V_{IN} and V_{OUT} when the circuit switches from the sample to the hold mode. Transistor Q1 provides an extra stage of isolation between the output of amplifier A1 and the hold capacitor CH1.

When selecting capacitors for use in a sample-and-hold circuit, the designer should choose those types with low dielectric absorption and low temperature coefficients. Silvered-mica capacitors exhibit low (0 to 100 ppm/°C) temperature coefficients and will still work in temperatures exceeding 200°C. It is also recommend that the user test the chosen capacitor to insure that its value closely matches that printed on it since not all capacitors are fully tested by their manufacturers for absolute tolerance.

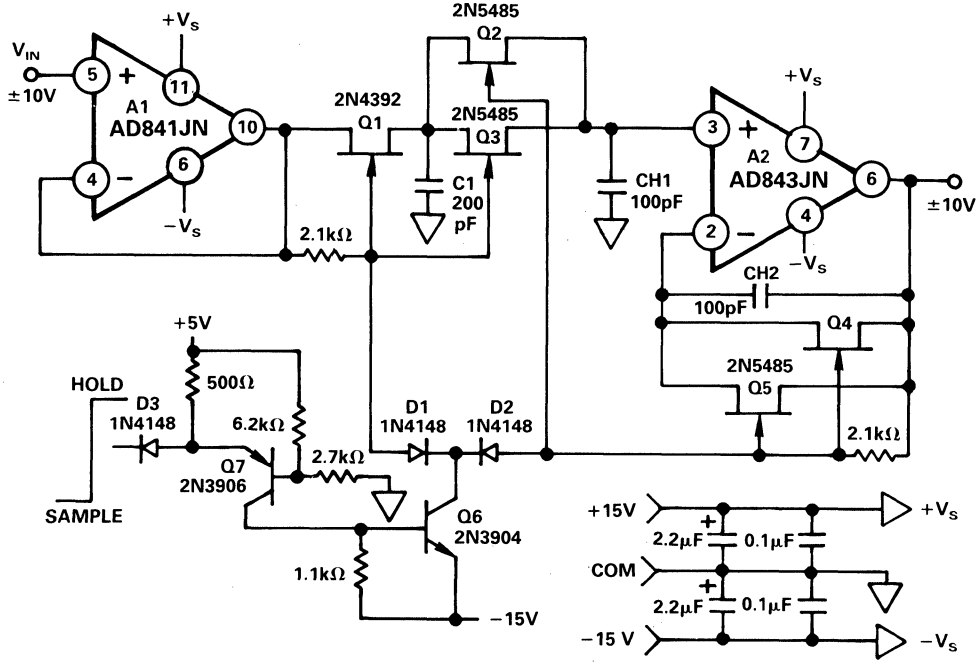


Figure 25. A Fast Switching Sample-and-Hold Amplifier

A PING-PONG S/H AMPLIFIER

For improved throughput over the circuit of Figure 25, a "ping-pong" architecture may be used. A ping-pong circuit overcomes some of the problems associated with high speed S/H amplifiers by allowing the use of a larger hold capacitor for a given sample rate: this will reduce the associated feedthrough, droop and pedestal errors.

Figure 26 illustrates a simple, four-chip ping-pong sample-and-hold amplifier circuit. This design increases throughput by using one channel to acquire a new sample while another channel holds the previous sample. Instead of having to reacquire the signal when switching from hold to sample mode, it alternately connects the outputs from Channel 1 or from Channel 2 to the A/D converter. In this case, the throughput is the slew rate and settling time of the output amplifiers, A2 and A3.

A high speed CB amplifier, A1, follows the input signal. U1, a dual wide-band "T" switch, connects the input buffer amp to one of the two output amplifiers while selecting the complementary amplifier to drive the A/D input. For example, when "select" is at logic high, A1 drives CH1, A2 tracks the input signal and the output of A3 is connected to the input of the A/D converter. At the same time, A3 holds an analog value and its output is connected to the input of the A/D converter. When the select command goes to logic LOW, the two output amplifiers alternate functions.

Since the input to the A/D converter is the alternated "held" outputs from A1 and A2, the offset voltage mismatch of the two amplifiers will show up as nonlinearity and, therefore, distortion in the output signal. To minimize this, potentiometers can be used to adjust the offsets of the output amplifiers until they are equal. Alternatively, an autocalibration circuit using two D/A converters can be employed. This can also be used to calibrate-out the effects of offset voltage drift over temperature.

The switch choice, for U1, is critical in this type of design. The DG542 utilizes "T" switching techniques on each channel for exceptionally low crosstalk and for high isolation. The part further improves these specifications by using ground pins between the signal pins. With an input frequency of 5 MHz, crosstalk and isolation are −85 dB and −75 dB, respectively. A limitation of this switch is that it operates from a maximum −5 V negative supply, making bipolar operation more difficult. It is recommended that amplifiers A1, A2 and A3 operate from the same −5 V supply to minimize any potential latch-up problems.

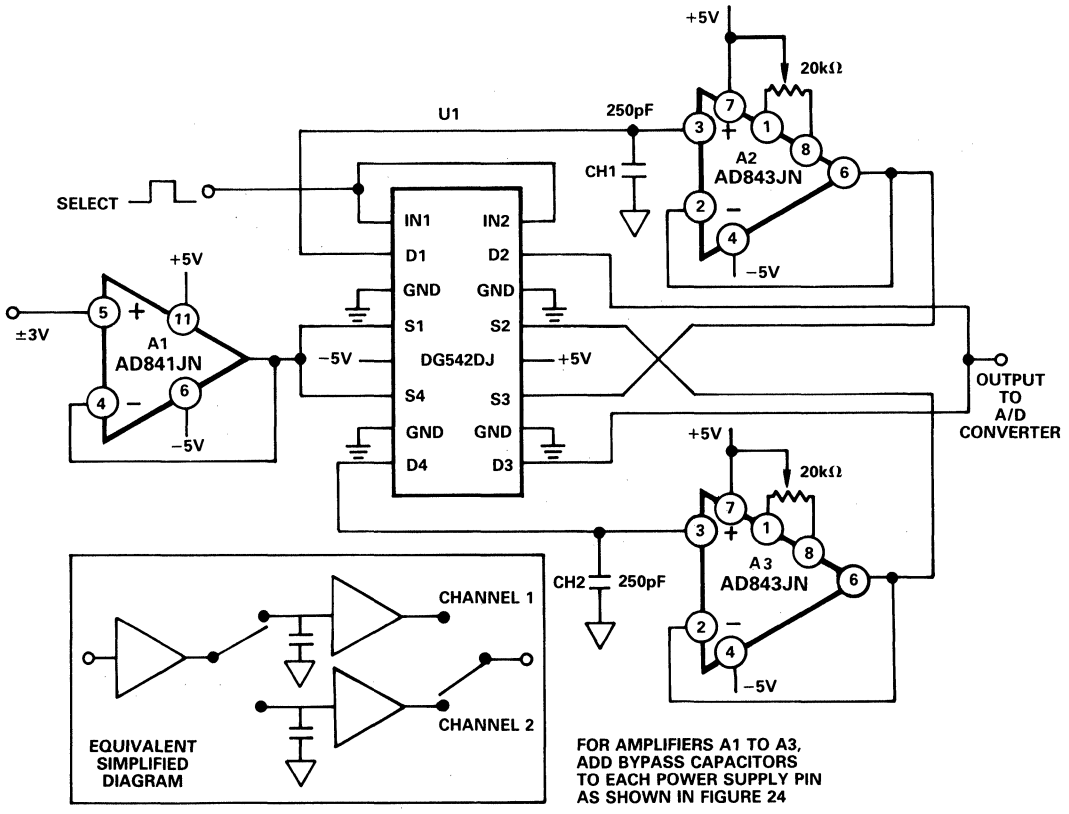


Figure 26. A Ping-Pong Sample-and-Hold Amplifier

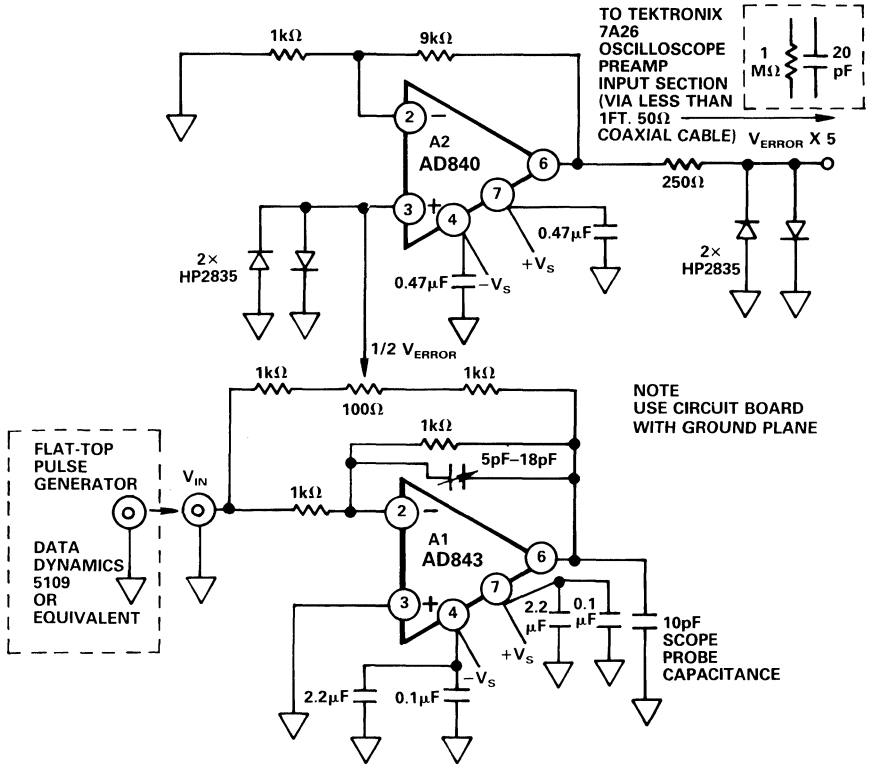


Figure 27. Settling Time Test Circuit

MEASURING AD843 SETTLING TIME

Figure 28 shows the dynamic response of the AD843 while operating in the settling time test circuit of Figure 27. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from A1, the AD843 under test, is amplified by op amp A2 and then clamped by two high speed Schottky diodes.

The error signal is clamped to prevent it from greatly overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was chosen because it will recover from the approximately 0.4 volt overload, quickly enough to allow accurate measurement of the AD843's 135 ns settling time. Amplifier A2 is a very high speed op amp; it provides a voltage gain of 10, providing a total gain of 5 from the error signal to the oscilloscope input.

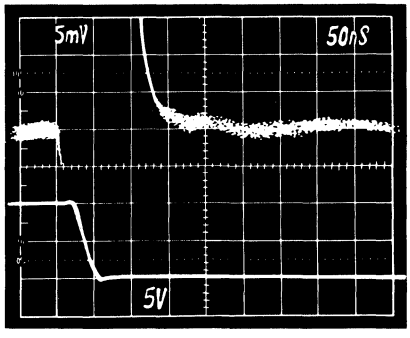


Figure 28. Settling Characteristics: +10 V to 0 V Step.
Upper Trace: Amplified Error Voltage (0.01%/Div)
Lower Trace: Output of AD843 Under Test (5 V/Div)

Applications Circuits

A FAST PEAK DETECTOR CIRCUIT

The peak detector circuit of Figure 29, can accurately capture the amplitude of input pulses as narrow as 200 ns and can hold their value with a droop rate of less than 20 μV/μs. This circuit will capture the peak value of positive polarity waveforms; to detect negative peaks, simply reverse the polarity of the two diodes.

The high bandwidth and 200 V/μs slew rate of amplifier A2, an AD843, allows the detector's output to "keep up" with its input thus minimizing overshoot. The low (<1 nA) input current of the AD843 ensures that the droop rate is limited only by the reverse leakage of diode D2, which is typically <10 nA for the type shown. The low droop rate is apparent in Figure 30. The detector's output (top trace) loses slightly over a volt of the 8 volt peak input value (bottom trace) in 75 ms, or a rate of approximately 16 μV/μs

Amplifier A1, an AD847, can drive 680 pF hold capacitor, C_P, fast enough to "catch-up" with the next peak in 100 ns and still settle to the new value in 250 ns, as illustrated in Figure 31. *Reducing* the value of capacitor C_P to 100 pF will maximize the speed of this circuit at the expense of increased overshoot and droop. Since the AD847 can drive an arbitrarily large value of capacitance, C_P can be *increased* to reduce droop, at the expense of response time.

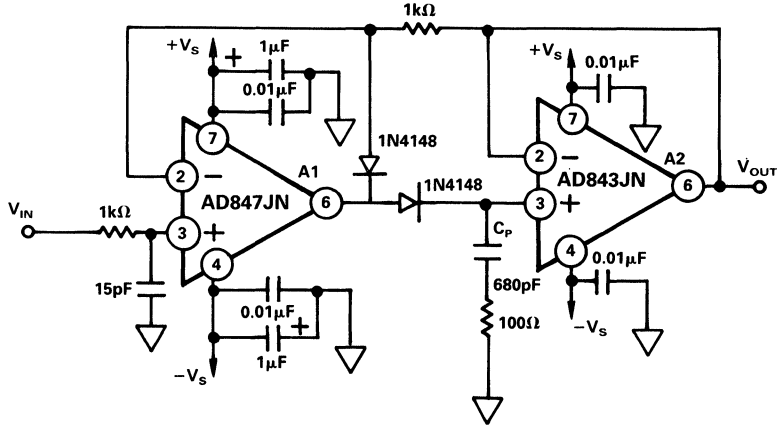
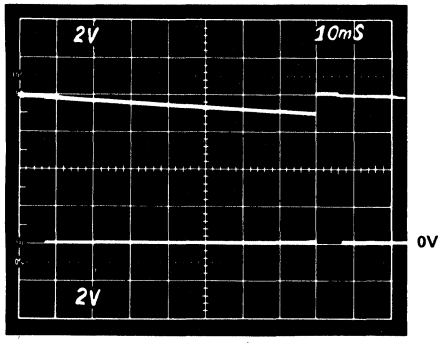


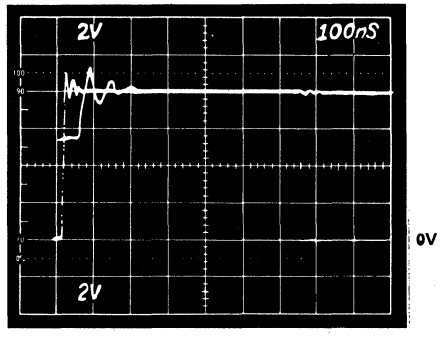
Figure 29. A Fast Peak Detector Circuit



TOP TRACE: PEAK DETECTOR OUTPUT

BOTTOM TRACE: INPUT, 8V PEAK @ 125Hz

Figure 30. Peak Detector Response to 125 Hz Pulse Train



TOP TRACE: PEAK DETECTOR OUTPUT, 8V

BOTTOM TRACE: INPUT VOLTAGE, 8V PEAK, 650ns PULSE WIDTH

Figure 31. Peak Capture Time

60MHz, 2000V/μs Monolithic Op Amp

AD844

FEATURES

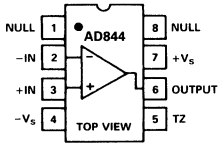
Wide Bandwidth: 60MHz at Gain of −1
33MHz at Gain of −10
Very High Output Slew Rate: Up to 2000V/μs
20MHz Full Power Bandwidth, 20V pk-pk, R_L=500Ω
Fast Settling: 100ns to 0.1% (10V Step)
Differential Gain Error: 0.03% at 4.4MHz
Differential Phase Error: 0.15° at 4.4MHz
High Output Drive: ±50mA into 50Ω Load
Low Offset Voltage: 150μV max (B Grade)
Low Quiescent Current: 6.5mA

APPLICATIONS

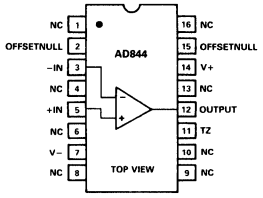
Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

AD844 CONNECTION DIAGRAMS

8-Pin Plastic (N), and Cerdip (Q) Packages



16-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many non-inverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000V/μs for a full 20V output step. Settling time is typically 100ns to 0.1%, and essentially independent of gain. The AD844 can drive 50Ω loads to ±2.5V with low distortion and is short circuit protected to 80mA.

The AD844 is available in four performance grades and three package options. In the 16-pin SOIC (R) package, the AD844J is specified for the commercial temperature range of 0 to +70°C. The AD844A and AD844B are specified for the industrial temperature range of −40°C to +85°C and are available in the cerdip (Q) package. The AD844A is also available in an 8-pin plastic mini-DIP (N). The AD844S is specified over the military temperature range of −55°C to +125°C and is available in the cerdip (Q) package. "A" and "S" grade chips and devices processed to MIL-STD-883B, REV. C are also available.

PRODUCT HIGHLIGHTS

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance. It may be used as an alternative to the EL2020 and CLC400/1.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5V to ±18V power supplies and is capable of driving loads down to 50Ω, as well as drive very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 are laser trimmed to minimize dc errors; V_{OS} drift is typically 1μV/°C and bias current drift is typically 9nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60MHz.
6. The AD844 combines low distortion, low noise and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

SPECIFICATIONS (@ T_A+25°C and V_S=±15V dc, unless otherwise noted)

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
INPUT OFFSET VOLTAGE[1]			50	**300**		50	**150**		50	**300**	μV
T_{min}–T_{max}			75	500		75	**200**		125	**500**	μV
vs. Temperature			1			1	5		1	5	μV/°C
vs. Supply	5V–18V										
Initial			4	**20**		4	**10**		4	**20**	μV/V
T_{min}–T_{max}			4			4	**10**		4	**20**	μV/V
vs. Common Mode	V_{CM}=±10V										
Initial			10	**35**		10	**20**		10	**35**	μV/V
T_{min}–T_{max}			10			10	**20**		10	**35**	μV/V
INPUT BIAS CURRENT											
–Input Bias Current[1]			200	**450**		150	**250**		200	**450**	nA
T_{min}–T_{max}			800	1500		750	**1100**		1900	**2500**	nA
vs. Temperature			9			9	15		20	30	nA/°C
vs. Supply	5V–18V										
Initial			175	**250**		175	**200**		175	**250**	nA/V
T_{min}–T_{max}			220			220	**240**		220	**300**	nA/V
vs. Common Mode	V_{CM}=±10V										
Initial			90	**160**		90	**110**		90	**160**	nA/V
T_{min}–T_{max}			110			110	**150**		120	**200**	nA/V
+Input Bias Current[1]			150	**400**		100	**200**		100	**400**	nA
T_{min}–T_{max}			350	700		300	**500**		800	**1300**	nA
vs. Temperature			3			3	7		7	15	nA/°C
vs. Supply	5V–18V										
Initial			80	**150**		80	**100**		80	**150**	nA/V
T_{min}–T_{max}			100			100	**120**		120	**200**	nA/V
vs. Common Mode	V_{CM}=±10V										
Initial			90	**150**		90	**120**		90	**150**	nA/V
T_{min}–T_{max}			130			130	**190**		140	**200**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50	65		50	65		50	65	Ω
+Input		7	10		7	10		7	10		MΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
Input Voltage Range											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	f≥1kHz		2			2			2		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE											
–Input	f≥1kHz		10			10			10		pA/$\sqrt{Hz}$
+Input	f≥1kHz		12			12			12		pA/$\sqrt{Hz}$
OPEN LOOP TRANSRESISTANCE	V_{OUT}=±10V										
	R_{LOAD}=500Ω	**2.2**	3.0		**2.8**	3.0		**2.2**	3.0		MΩ
T_{min}–T_{max}		1.3	2.0		**1.6**	2.0		**1.3**	1.6		MΩ
Transcapacitance			4.5			4.5			4.5		pF
DIFFERENTIAL GAIN ERROR[2]	f=4.4MHz		0.03			0.03			0.03		%
DIFFERENTIAL PHASE ERROR[2]	f=4.4MHz		0.15			0.15			0.15		Degree
FREQUENCY RESPONSE											
Small Signal Bandwidth											
[3]Gain=–1			60			60			60		MHz
[4]Gain=–10			33			33			33		MHz
TOTAL HARMOMIC DISTORTION	f=100kHz, 2V rms[5]		0.005			0.005			0.005		%
SETTLING TIME											
10V Output Step	±15V Supplies										
Gain=–1, to 0.1%[5]			100			100			100		ns
Gain=–10, to 0.1%[6]			100			100			100		ns
2V Output Step	±5V Supplies										
Gain=–1, to 0.1%[5]			110			110			110		ns
Gain=–10, to 0.1%[6]			100			100			100		ns

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
OUTPUT SLEW RATE	Overdriven Input	1200	2000		1200	2000		1200	2000		V/μs
FULL POWER BANDWIDTH											
V_{OUT}=20V p-p[5]	V_S=±15V		20			20			20		MHz
V_{OUT}=2V p-p[5]	V_S=±5V THD=3%		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}=500Ω	**10**	11		**10**	11		**10**	11		±V
Short Circuit Current			80			80			80		mA
T_{min}–T_{max}			60			60			60		mA
Output Resistance	Open Loop		15			15			15		Ω
POWER SUPPLY											
Operating Range		±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current			6.5	**7.5**		6.5	**7.5**		6.5	**7.5**	mA
T_{min}–T_{max}			7.5	8.5		7.5	**8.5**		8.5	**9.5**	mA

NOTES
[1]Rated performance after a 5 minute warmup at T_A=25°C.
[2]Input signal 285mV p-p carrier (40 IRE) riding on 0 to 642mV (90 IRE) ramp. R_L=100Ω; R1, R2=300Ω.
[3]Input signal 0dBm, C_L=10pF, R_L=500Ω, R1=500Ω, R2=500Ω in Figure 26.
[4]Input signal 0dBm, C_L=10pF, R_L=500Ω, R1=500Ω, R2=50Ω in Figure 26.
[5]C_L=10pF, R_L=500Ω, R1=1kΩ, R2=1kΩ in Figure 26.
[6]C_L=10pF, R_L=500Ω, R1=500Ω, R2=50Ω in Figure 26.

Specifications subject to change without notice. All min and max specifications are guaranteed.
Specifications shown in **boldface** are tested on all production units at final electrical test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Power Dissipation[2] 1.1W
Output Short Circuit Duration . . . . . Indefinite
Common Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage 6V
Inverting Input Current
  Continuous 5mA
  Transient 10mA
Storage Temperature Range Q . . . . . −65°C to +150°C
  N, R . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA}= 100°C/Watt
8-Pin Cerdip Package: θ_{JA}=110°C/Watt
16-Pin SOIC Package: θ_{JA}=100°C/Watt

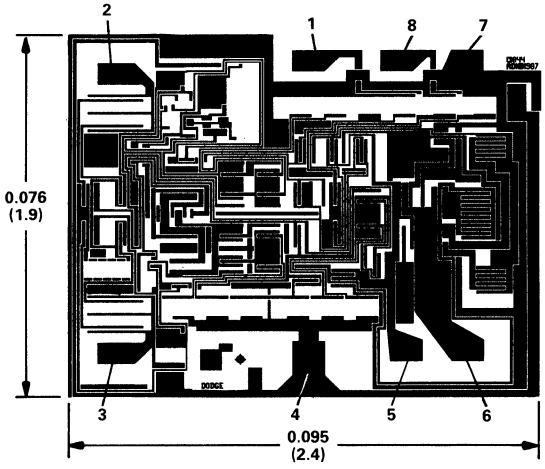
ORDERING GUIDE[1, 2]

Temperature Range	Mini-DIP (N-8)	Cerdip (Q-8)	SOIC (R-16)
Commercial 0 to +70°C			AD844JR
Industrial −40°C to +85°C	AD844AN	AD844AQ AD844BQ	
Military −55°C to +125°C		AD844SQ AD844SQ-883B	

NOTES
[1]"A" and "S" grade chips are also available.
[2]See Section 20 for package outline information.

METALIZATION PHOTO

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



Typical Characteristics ($T_A = +25°C$ and $V_S = \pm 15V$ unless otherwise noted)

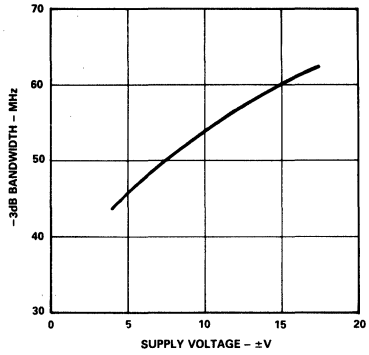


Figure 1. −3dB Bandwidth vs. Supply Voltage R1 = R2 = 500Ω

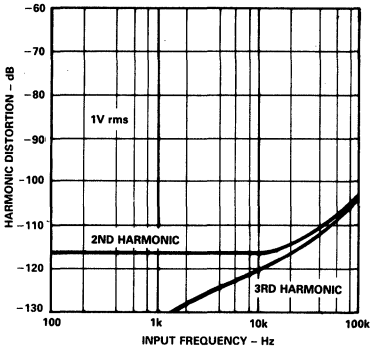


Figure 2. Harmonic Distortion vs. Frequency, R1 = R2 = 1kΩ

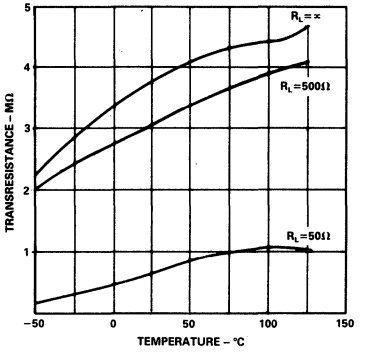


Figure 3. Transresistance vs. Temperature

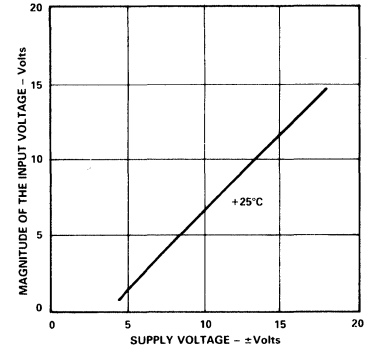


Figure 4. Noninverting Input Voltage Swing vs. Supply Voltage

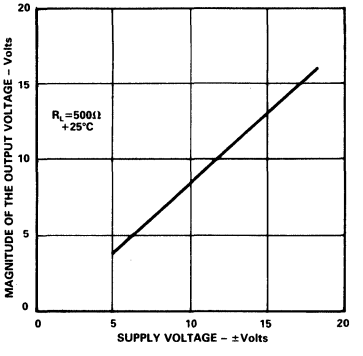


Figure 5. Output Voltage Swing vs. Supply Voltage

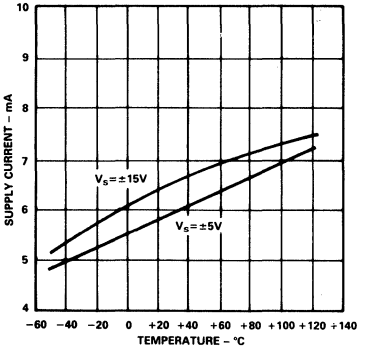


Figure 6. Quiescent Supply Current vs. Temperature and Supply Voltage

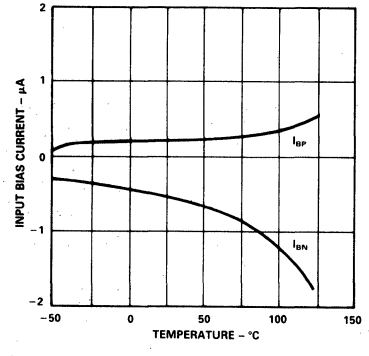


Figure 7. Inverting Input Bias Current (I_{BN}) and Noninverting Input Bias Current (I_{BP}) vs. Temperature

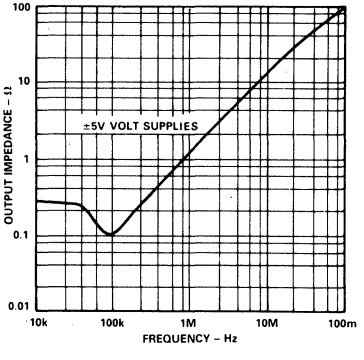


Figure 8. Output Impedance vs. Frequency, Gain = −1, R1 = R2 = 1kΩ

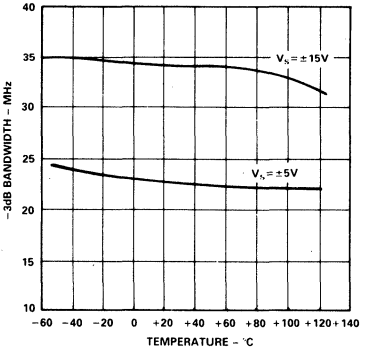


Figure 9. −3dB Bandwidth vs. Temperature, Gain = −1, R1 = R2 = 1kΩ

Inverting Gain of 1 AC Characteristics

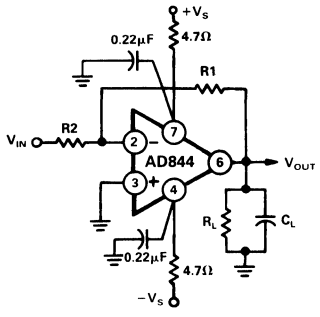


Figure 10. Inverting Amplifier, Gain of −1 (R1=R2)

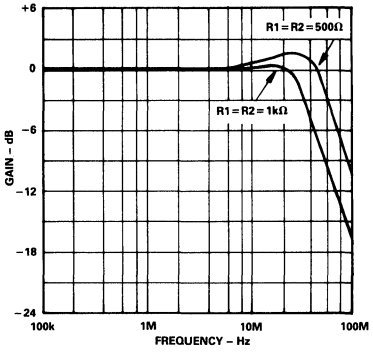


Figure 11. Gain vs. Frequency for Gain = −1, R_L = 500Ω, C_L = 0pF

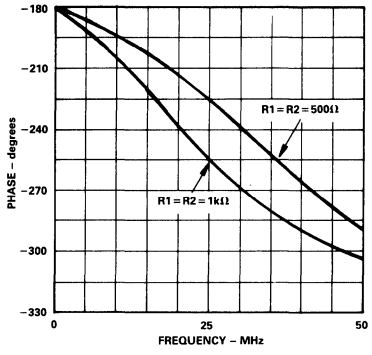


Figure 12. Phase vs. Frequency Gain = −1, R_L = 500Ω, C_L = 0pF

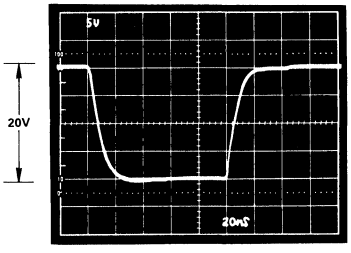


Figure 13. Large Signal Pulse Response, Gain = −1, R1 = R2 = 1kΩ

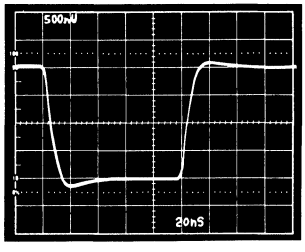


Figure 14. Small Signal Pulse Response, Gain = −1, R1 = R2 = 1kΩ

Inverting Gain of 10 AC Characteristics

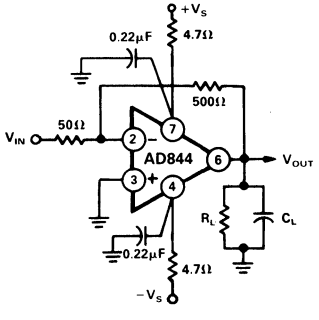


Figure 15. Gain of −10 Amplifier

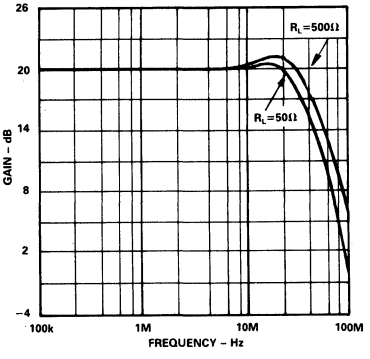


Figure 16. Gain vs. Frequency, Gain = −10

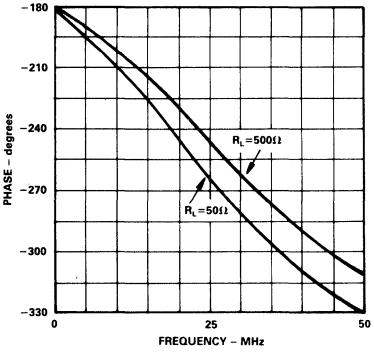


Figure 17. Phase vs. Frequency, Gain = −10

Inverting Gain of 10 Pulse Response

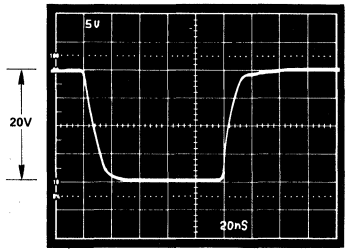


Figure 18. Large Signal Pulse Response, Gain=−10, R_L=500Ω

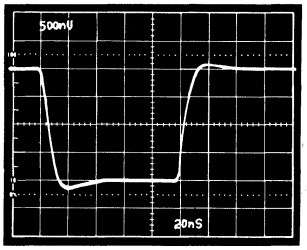


Figure 19. Small Signal Pulse Response, Gain=−10, R_L=500Ω

Noninverting Gain of 10 AC Characteristics

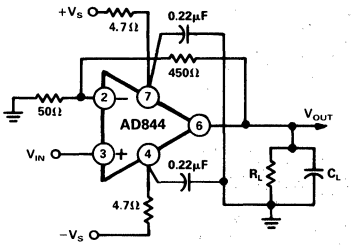


Figure 20. Noninverting Gain of +10 Amplifier

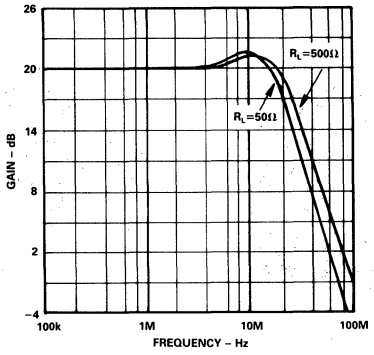


Figure 21. Gain vs. Frequency, Gain=+10

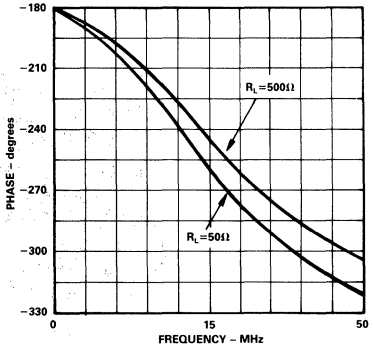


Figure 22. Phase vs. Frequency, Gain=+10

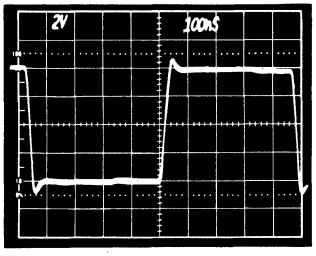


Figure 23. Noninverting Amplifier Large Signal Pulse Response, Gain=+10, R_L=500Ω

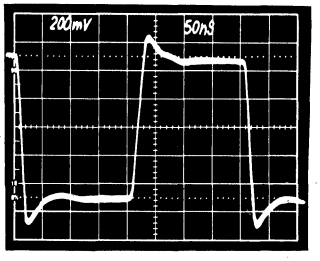


Figure 24. Small Signal Pulse Response, Gain=+10, R_L=500Ω

UNDERSTANDING THE AD844

The AD844 can be used in ways similar to a conventional op amp while providing performance advantages in wideband applications. However, there are important differences in the internal structure which need to be understood in order to optimize the performance of the AD844 op amp.

Open Loop Behavior

Figure 25 shows a current feedback amplifier reduced to essentials. Sources of fixed dc errors such as the inverting node bias current and the offset voltage are excluded from this model and are discussed later. The most important parameter limiting the dc gain is the transresistance, Rt, which is ideally infinite. A finite value of Rt is analogous to the finite open loop voltage gain in a conventional op amp.

The current applied to the inverting input node is replicated by the current conveyor so as to flow in resistor Rt. The voltage developed across Rt is buffered by the unity gain voltage follower. Voltage gain is the ratio Rt/ R_{IN}. With typical values of Rt=3MΩ and R_{IN}=50Ω, the voltage gain is about 60,000. The open loop current gain is another measure of gain and is determined by the beta product of the transistors in the voltage follower stage (see Figure 28); it is typically 40,000.

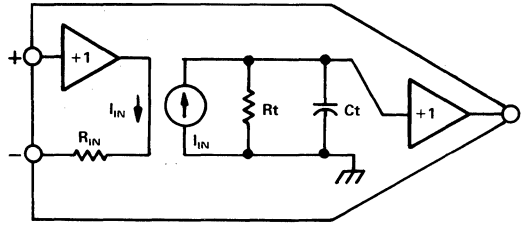


Figure 25. Equivalent Schematic

The important parameters defining ac behavior are the transcapacitance, Ct, and the external feedback resistor (not shown). The time constant formed by these components is analogous to the dominant pole of a conventional op amp, and thus cannot be reduced below a critical value if the closed loop system is to be stable. In practice, Ct is held to as low a value as possible (typically 4.5pF) so that the feedback resistor can be maximized while maintaining a fast response. The finite R_{IN} also affects the closed loop response in some applications as will be shown.

The open loop ac gain is also best understood in terms of the transimpedance rather than as an open loop voltage gain. The open loop pole is formed by Rt in parallel with Ct. Since Ct is typically 4.5pF, the open loop corner frequency occurs at about 12kHz. However, this parameter is of little value in determining the closed loop response.

Response as an Inverting Amplifier

Figure 26 shows the connections for an inverting amplifier. Unlike a conventional amplifier the transient response and the small signal bandwidth are determined primarily by the value of the external feedback resistor, R1, rather than by the ratio of R1/R2 as is customarily the case in an op amp application. This is a direct result of the low impedance at the inverting input. As with conventional op amps, the closed loop gain is −R1/R2.

The closed loop transresistance is simply the parallel sum of R1 and Rt. Since R1 will generally be in the range 500Ω to 2kΩ and Rt is about 3MΩ the closed loop transresistance will be only 0.02% to 0.07% lower than R1. This small error will often be less than the resistor tolerance.

When R1 is fairly large (above 5kΩ) but still much less than Rt, the closed loop HF response is dominated by the time constant R1Ct. Under such conditions the AD844 is over-damped and will provide only a fraction of its bandwidth potential. Because of the absence of slew rate limitations under these conditions, the circuit will exhibit a simple single pole response even under large signal conditions.

In Figure 26, R3 is used to properly terminate the input if desired. R3 in parallel with R2 gives the terminated resistance. As R1 is lowered, the signal bandwidth increases, but the time constant R1Ct becomes comparable to higher order poles in the closed loop response. Therefore, the closed loop response becomes complex, and the pulse response shows overshoot. When R2 is much larger than the input resistance, R_{IN}, at Pin 2, most of the feedback current in R1 is delivered to this input; but as R2 becomes comparable to R_{IN}, less of the feedback is absorbed at Pin 2, resulting in a more heavily damped response. Consequently, for low values of R2 it is possible to lower R1 without causing instability in the closed loop response. Table I lists combinations of R1 and R2 and the resulting frequency response for the circuit of Figure 26. Figure 13 shows the very clean and fast ±10V pulse response of the AD844.

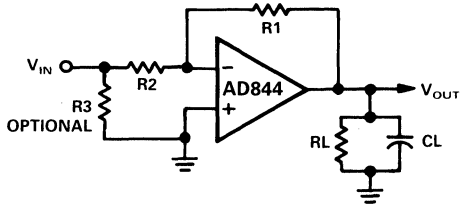


Figure 26. Inverting Amplifier

Gain	R1	R2	BW (MHz)	GBW (MHz)
−1	1kΩ	1kΩ	35	35
−1	500Ω	500Ω	60	60
−2	2kΩ	1kΩ	15	30
−2	1kΩ	500Ω	30	60
−5	5kΩ	1kΩ	5.2	26
−5	500Ω	100Ω	49	245
−10	1kΩ	100Ω	23	230
−10	500Ω	50Ω	33	330
−20	1kΩ	50Ω	21	420
−100	5kΩ	50Ω	3.2	320
+100	5kΩ	5Ω	9	900 (See Page 9.)

Table I.

Response as an I-V Converter

The AD844 works well as the active element in an operational current to voltage converter, used in conjunction with an external scaling resistor, R1, in Figure 27. This analysis includes the stray capacitance, C_S, of the current source, which might be a high speed DAC. Using a conventional op amp, this capacitance forms a "nuisance pole" with R1 which destabilizes the closed loop response of the system. Most op amps are internally compensated for the fastest response at unity gain, so the pole due to R1 and C_S reduces the already narrow phase margin of the system. For example, if R1 were 2.5kΩ a C_S of 15pF would place this pole at a frequency of about 4MHz, well within the response range of even a medium speed operational amplifier. In a current feedback amp this nuisance pole is no longer determined by R1 but by the input resistance, R_{IN}. Since this is about 50Ω for the AD844, the same 15pF forms a pole 212MHz and causes little trouble. It can be shown that the response of this system is:

$$V_{OUT} = -Isig \frac{K\,R1}{(1+sTd)(1+sTn)}$$

where K is a factor very close to unity and represents the finite dc gain of the amplifier, Td is the dominant pole and Tn is the nuisance pole:

$$K = \frac{Rt}{Rt+R1}$$

$$Td = KR1Ct$$

$$Tn = R_{IN}C_S \qquad \text{(assuming } R_{IN} << R1\text{)}$$

Using typical values of R1=1kΩ and Rt=3MΩ, K is 0.9997; in other words, the "gain error" is only 0.03%. This is much less than the scaling error of virtually all DACs and can be absorbed, if necessary, by the trim needed in a precise system.

In the AD844, Rt is fairly stable with temperature and supply voltages, and consequently the effect of finite "gain" is negligible unless high value feedback resistors are used. Since that would result in slower response times than are possible, the relatively low value of Rt in the AD844 will rarely be a significant source of error.

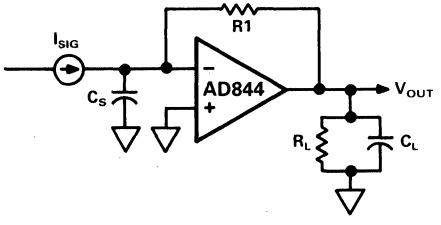


Figure 27. Current to Voltage Converter

Circuit Description of the AD844

A simplified schematic is shown in Figure 28. The AD844 differs from a conventional op amp in that the signal inputs have radically different impedance. The noninverting input (Pin 3) presents the usual high impedance. The voltage on this input is transferred to the inverting input (Pin 2) with a low offset voltage, ensured by the close matching of like polarity transistors

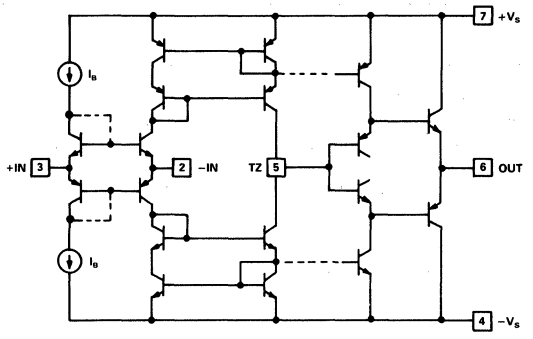


Figure 28. Simplified Schematic

operating under essentially identical bias conditions. Laser trimming nulls the residual offset voltage, down to a few tens of microvolts. The inverting input is the common emitter node of a complementary pair of grounded base stages and behaves as a current summing node. In an ideal current feedback op amp the input resistance would be zero. In the AD844 it is about 50Ω.

A current applied to the inverting input is transferred to a complementary pair of unity-gain current mirrors which deliver the same current to an internal node (Pin 5) at which the full output voltage is generated. The unity-gain complementary voltage follower then buffers this voltage and provides the load driving power. This buffer is designed to drive low impedance loads such as terminated cables, and can deliver ±50mA into a 50Ω load while maintaining low distortion, even when operating at supply voltages of only ±6V. Current limiting (not shown) ensures safe operation under short circuited conditions.

It is important to understand that the low input impedance at the inverting input is locally generated, and does not depend on feedback. This is very different from the "virtual ground" of a conventional operational amplifier used in the current summing mode which is essentially an open circuit until the loop settles. In the AD844, transient current at the input does not cause voltage spikes at the summing node while the amplifier is settling. Furthermore, all of the transient current is delivered to the slewing (TZ) node (Pin 5) via a short signal path (the grounded base stages and the wideband current mirrors).

The current available to charge the capacitance (about 4.5pF) at TZ node, *is always proportional to the input error current*, and the slew rate limitations associated with the large signal response of op amps do not occur. For this reason, the rise and fall times are almost independent of signal level. In practice, the input current will eventually cause the mirrors to saturate. When using ±15V supplies, this occurs at about 10mA (or ±2200V/μs). Since signal currents are rarely this large, classical "slew rate" limitations are absent.

This inherent advantage would be lost if the voltage follower used to buffer the output were to have slew rate limitations. The AD844 has been designed to avoid this problem, and as a result the output buffer exhibits a clean large signal transient response, free from anomalous effects arising from internal saturation.

Response as a Noninverting Amplifier

Since current feedback amplifiers are asymmetrical with regard to their two inputs, performance will differ markedly in noninverting and inverting modes. In noninverting modes, the large signal high speed behavior of the AD844 deteriorates at low gains because the biasing circuitry for the input system (not shown in Figure 28) is not designed to provide high input voltage slew rates.

However, good results can be obtained with some care. The noninverting input will not tolerate a large transient input; it must be kept below ±1V for best results. Consequently this mode is better suited to high gain applications (greater than ×10). Figure 20 shows a noninverting amplifier with a gain of 10 and a bandwidth of 30MHz. The transient response is shown in Figures 23 and 24. To increase the bandwidth at higher gains, a capacitor can be added across R2 whose value is approximately the ratio of R1 and R2 times Ct.

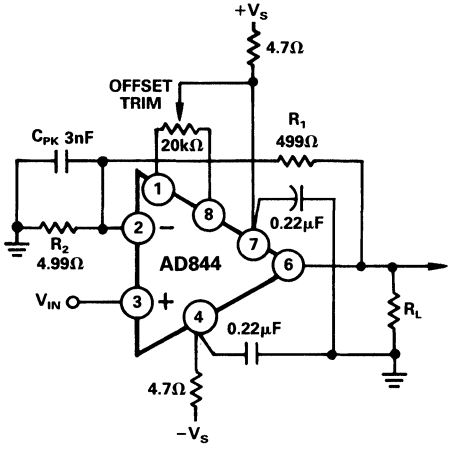


Figure 29. Noninverting Amplifier Gain=100, Optional Offset Trim Is Shown

Noninverting Gain of 100

The AD844 provides very clean pulse response at high noninverting gains. Figure 29 shows a typical configuration providing a gain of 100 with high input resistance. The feedback resistor is kept as low as practicable to maximize bandwidth, and a peaking capacitor (C_{PK}) can optionally be added to further extend the bandwidth. Figure 30 shows the small signal response with C_{PK} = 3nF, R_L = 500Ω and supply voltages of either ±5V or ±15V. *Gain bandwidth products of up to 900MHz can be achieved in this way.*

The offset voltage of the AD844 is laser trimmed to the 50µV level and exhibits very low drift. In practice, there is an additional offset term due to the bias current at the inverting input (I_{BN}) which flows in the feedback resistor (R1). This can optionally be nulled by the trimming potentiometer shown in Figure 29.

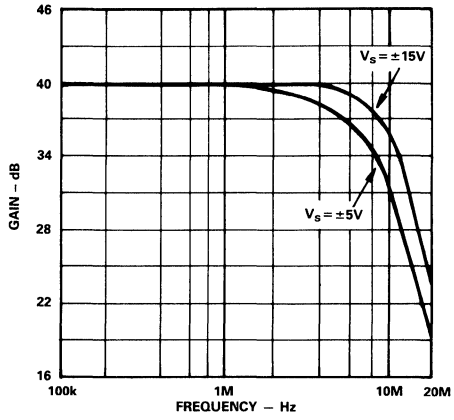


Figure 30. AC Response for Gain = 100, Configuration Shown in Figure 29

USING THE AD844

Board Layout

As with all high frequency circuits considerable care must be used in the layout of the components surrounding the AD844. A ground plane, to which the power supply decoupling capacitors are connected by the shortest possible leads, is essential to achieving clean pulse response. Even a continuous ground plane will exhibit finite voltage drops between points on the plane, and this must be kept in mind in selecting the grounding points. Generally speaking, decoupling capacitors should be taken to a point close to the load (or output connector) since the load currents flow in these capacitors at high frequencies. The +In and −In circuits (for example, a termination resistor and Pin 3) must be taken to a common point on the ground plane close to the amplifier package.

Use low impedance capacitors (AVX SR305C224KAA or equivalent) of 0.22µF wherever ac coupling is required. Include either ferrite beads and/or a small series resistance (approximately 4.7Ω) in each supply line.

Input Impedance

At low frequencies, negative feedback keeps the resistance at the inverting input close to zero. As the frequency increases, the impedance looking into this input will increase from near zero to the open loop input resistance, due to bandwidth limitations, making the input seem inductive. If it is desired to keep the input impedance flatter, a series RC network can be inserted across the input. The resistor is chosen so that the parallel sum of it and R2 equals the desired termination resistance. The capacitance is set so that the pole determined by this RC network is about half the bandwidth of the op amp. This network is not important if the input resistor is much larger than the termination used, or if frequencies are relatively low. In some cases, the small peaking that occurs without the network can be of use in extending the −3dB bandwidth.

Driving Large Capacitive Loads

Capacitive drive capability is 100pF without an external network. With the addition of the network shown in Figure 31, the capacitive drive can be extended to over 10,000pF, limited by internal power dissipation. With capacitive loads, the output speed becomes a function of the overdriven output current limit. Since this is roughly ±100mA, under these conditions, the maximum slew rate into a 1000pF load is ±100V/μs. Figure 32 shows the transient response of an inverting amplifier (R1=R2=1kΩ) using the feed forward network shown in Figure 31, driving a load of 1000pF.

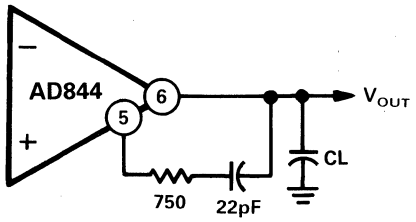


Figure 31. Feed Forward Network for Large Capacitive Loads

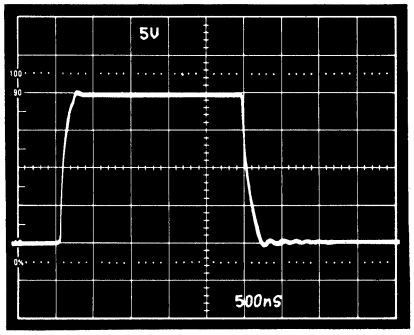


Figure 32. Driving 1000pF CL with Feed Forward Network of Figure 31

Settling Time

Settling time is measured with the circuit of Figure 33. This circuit employs a false summing node, clamped by the two Schottky diodes, to create the error signal and limit the input signal to the oscilloscope. For measuring settling time, the ratio of R6/R5 is equal to R1/R2. For unity gain, R6=R5=1kΩ, and R_L=500Ω. For the gain of −10, R5=50Ω, R6=500Ω and R_L was not used since the summing network loads the output with approximately 275Ω. Using this network in a unity-gain configuration, settling time is 100ns to 0.1% for a −5V to +5V step with C_L=10pF.

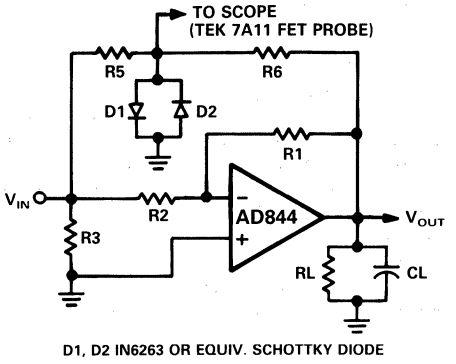


Figure 33. Settling Time Test Fixture

DC Error Calculation

Figure 34 shows a model of the dc error and noise sources for the AD844. The inverting input bias current, I_{BN}, flows in the feedback resistor. I_{BP}, the noninverting input bias current, flows in the resistance at Pin 3 (R_P), and the resulting voltage (plus any offset voltage) will appear at the inverting input. The total error, V_O, at the output is:

$$V_O=(I_{BP}\,R_P+V_{OS}+I_{BN}\,R_{IN})\left(1+\frac{R1}{R2}\right)+I_{BN}\,R1$$

Since I_{BN} and I_{BP} are unrelated both in sign and magnitude, inserting a resistor in series with the noninverting input will not necessarily reduce dc error and may actually increase it.

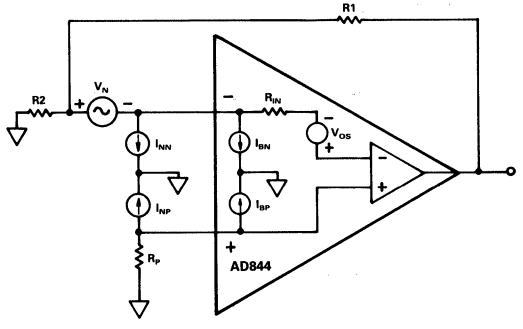


Figure 34. Offset Voltage and Noise Model for the AD844

Noise

Noise sources can be modeled in a manner similar to the dc bias currents, but the noise sources are Inn, Inp, Vn, and the amplifier-induced noise at the output, V_{ON}, is:

$$V_{ON}=\sqrt{((Inp\,R_P)^2+Vn^2)\left(1+\frac{R1}{R2}\right)^2+(Inn\,R1)^2}$$

Overall noise can be reduced by keeping all resistor values to a minimum. With typical numbers, R1=R2=1k, R_P=0, Vn=2nV/√Hz, Inp=10pA/√Hz, Inn=12pA/√Hz, V_{ON} calculates to 12nV/√Hz. The current noise is dominant in this case, as it will be in most low gain applications.

Video Cable Driver Using ±5 Volt Supplies

The AD844 can be used to drive low impedance cables. Using ±5V supplies, a 100Ω load can be driven to ±2.5V with low distortion. Figure 35a shows an illustrative application which provides a noninverting gain of 2, allowing the cable to be reverse-terminated while delivering an overall gain of +1 to the load. The −3dB bandwidth of this circuit is typically 30MHz. Figure 35b shows a differential gain and phase test setup. In video applications, differential-phase and differential-gain characteristics are often important. Figure 35c shows the variation in phase as the load voltage varies. Figure 35d shows the gain variation.

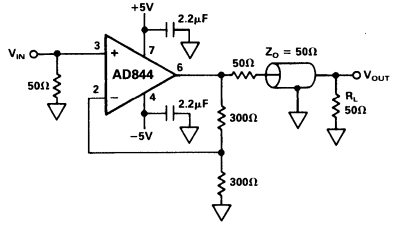


Figure 35a. The AD844 as a Cable Driver

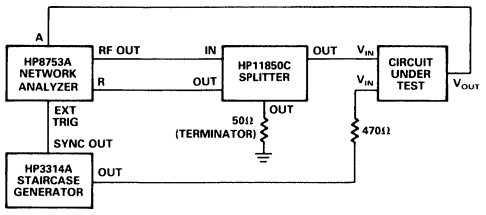


Figure 35b. Differential Gain/Phase Test Setup

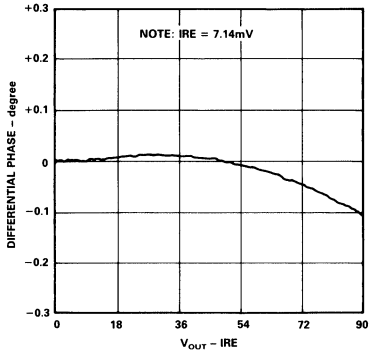


Figure 35c. Differential Phase for the Circuit of Figure 35a

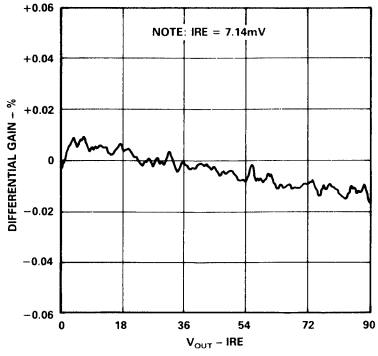


Figure 35d. Differential Gain for the Circuit of Figure 35a

High Speed DAC Buffer

The AD844 performs very well in applications requiring current-to-voltage conversion. Figure 36 shows connections for use with the AD568 current output DAC. In this application the bipolar offset is used so that the full scale current is ±5.12mA, which generates an output of ±5.12V using the 1kΩ application resistor on the AD568. Figure 37 shows the full scale transient response. Care is needed in power supply decoupling and grounding techniques to achieve the full 12-bit accuracy and realize the fast settling capabilities of the system. The unmarked capacitors in this figure are 0.1μF ceramic (for example, AVX Type SR305C104KAA), and the ferrite inductors should be about 2.5μH (for example, Fair-Rite Type 2743002122). The AD568 data sheet should be consulted for more complete details about its use.

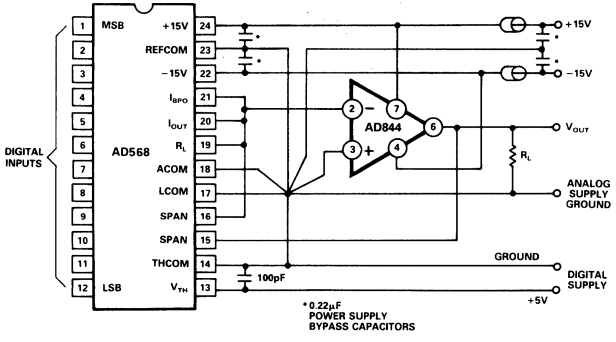


Figure 36. High Speed DAC Amplifier

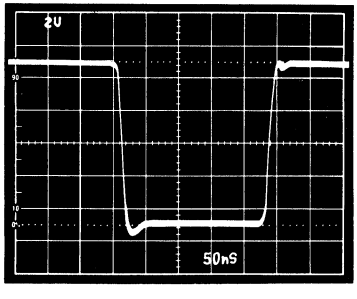


Figure 37. DAC Amplifier Full-Scale Transient Response

20MHz Variable Gain Amplifier

The AD844 is an excellent choice as an output amplifier for the AD539 multiplier, in all of its connection modes. (See AD539 data sheet for full details.) Figure 38 shows a simple multiplier providing the output:

$$V_W = -\frac{V_X V_Y}{2V}$$

where V_X is the "gain control" input, a positive voltage of from 0 to +3.2V (max) and V_Y is the "signal voltage", nominally ±2V FS but capable of operation up to ±4.2V. The peak output in this configuration is thus ±6.7V. Using all four of the internal application resistors provided on the AD539 in parallel results in a feedback resistance of 1.5kΩ, at which value the bandwidth of the AD844 is about 22MHz, and is essentially independent of V_X. The gain at V_X=3.16V is +4dB.

Figure 39 shows the small signal response for a 50dB gain control range (V_X=+10mV to +3.16V). At small values of V_X, capacitive feedthrough on the PC board becomes troublesome, and very careful layout techniques are needed to minimize this problem. A ground strip between the pins of the AD539 will be helpful in this regard. Figure 40 shows the response to a 2V pulse on V_Y for V_X=+1V, +2V and +3V. For these results, a load resistor of 500Ω was used and the supplies were ±9V. The multiplier will operate from supplies between ±4.5V and ±16.5V.

Disconnecting Pins 9 and 16 on the AD539 alters the denominator in the above expression to 1V, and the bandwidth will be approximately 10MHz, with a maximum gain of 10dB. Using only Pin 9 or Pin 16 results in a denominator of 0.5V, a bandwidth of 5MHz and a maximum gain of 16dB.

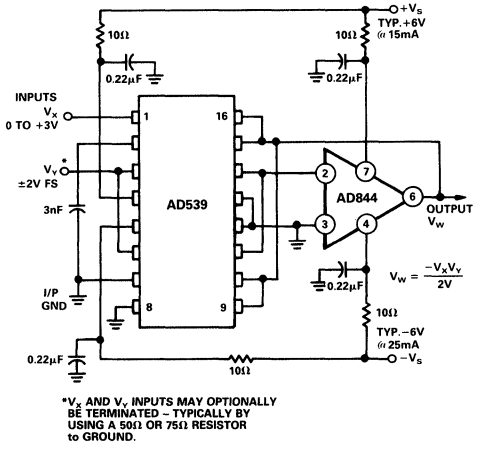


Figure 38. 20MHz VGA Using the AD539

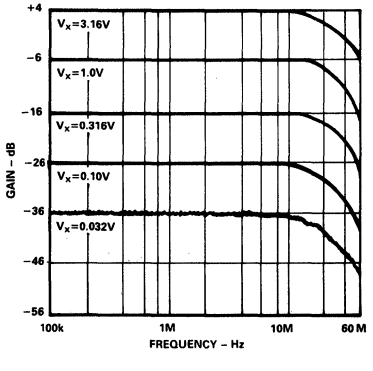


Figure 39. VGA AC Response

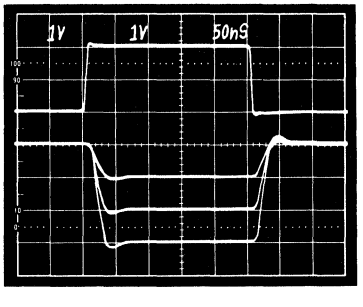


Figure 40. VGA Transient Response with V_X=1V, 2V, and 3V

ANALOG DEVICES

Precision, 16 MHz CBFET Op Amp

AD845

FEATURES

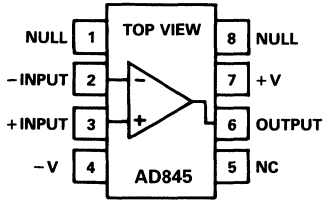
Replaces Hybrid Amplifiers in Many Applications

AC PERFORMANCE:
Settles to 0.01% in 350 ns
100 V/μs Slew Rate
12.8 MHz min Unity-Gain Bandwidth
1.75 MHz Full-Power Bandwidth at 20 V p–p

DC PERFORMANCE:
0.25 mV max Input Offset Voltage
5 μV/°C max Offset Voltage Drift
0.5 nA Input Bias Current
250 V/mV min Open-Loop Gain
4 μV p–p max Voltage Noise, 0.1 Hz to 10 Hz
94 dB min CMRR
Available in Plastic Mini-DIP and Hermetic Cerdip Packages

AD845 CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package
and Cerdip (Q) Package



NOTE: PIN 4 CONNECTED TO CASE
NC = NO CONNECT

PRODUCT DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100 V/μs, a stable unity-gain bandwidth of 16 MHz, and a settling time of 350 ns 0.01%—while driving a parallel load of 100 pF and 500 Ω—represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs which use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar input op amps.

The AD845 is ideal for use in applications such as active filters, high speed integrators, photo diode preamps, sample-and-hold amplifiers, log amplifiers, and in buffering A/D and D/A converters. The 250 μV max input offset voltage makes offset nulling unnecessary in many applications. The common mode rejection ratio of 110 dB over a ±10 V input voltage range represents exceptional performance for a JFET input high speed op amp. This, together with a minimum open-loop gain of 250 V/mV ensures that 12-bit performance is achieved, even in unity-gain buffer circuits.

The AD845 conforms to the standard op amp pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0 to +70°C temperature range. AD845A and AD845B devices are specified for operation over the −40°C to +85°C industrial temperature range. The AD845S is specified to operate over the full military temperature range of −55°C to +125°C. Both the industrial and military versions are available in 8-pin cerdip packages. The commercial version is available in an 8-pin plastic mini-DIP. "J" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time, and dc precision of the AD845 make it ideal for high speed applications requiring 12-bit accuracy.
2. The performance of circuits using the LF400, OP-42, OP-44, OP-16, OP-17, HA2520/2/5, HA2620/2/5, 3550, OPA605, and LH0062 can be upgraded in most cases.
3. The AD845 is unity-gain stable and internally compensated.
4. The AD845 is specified while driving 100 pF/500 Ω loads.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD845J/A Min	AD845J/A Typ	AD845J/A Max	AD845K/B Min	AD845K/B Typ	AD845K/B Max	AD845S Min	AD845S Typ	AD845S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.7	**1.5**		0.1	**0.25**		0.25	**1.0**	mV
	T_{min}–T_{max}			2.5			**0.4**			2.0	mV
Offset Drift				20		1.5	**5.0**			**10**	μV/°C
INPUT BIAS CURRENT[2]											
Initial	V_{CM} = 0 V		0.75	**2**		0.5	**1**		0.75	**2**	nA
	T_{min}–T_{max}			45/75			**18/38**			**500**	nA
INPUT OFFSET CURRENT											
Initial	V_{CM} = 0 V		25	**300**		15	**100**		25	**300**	pA
	T_{min}–T_{max}			3/6.5			**1.2/2.6**			**20**	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{11}			10^{11}			10^{11}		kΩ
Input Capacitance			4.0			4.0			4.0		pF
INPUT VOLTAGE RANGE											
Differential			±20			±20			±20		V
Common Mode		**±10**	+ 10.5/−13		**+10**	+10.5/−13		**±10**	+10.5/−13		V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	110		**94**	113		**86**	110		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		4			4			4		μV p–p
	f = 10 Hz		80			80			80		nV/√Hz
	f = 100 Hz		60			60			60		nV/√Hz
	f = 1 kHz		25			25			25		nV/√Hz
	f = 10 kHz		18			18			18		nV/√Hz
	f = 100 kHz		12			12			12		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.1			0.1			0.1		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	**200**	500		**250**	500		**200**	500		V/mV
	R_{LOAD}≥500 Ω	**100**	250		**125**	250		**100**	250		V/mV
	T_{min}–T_{max}	70			75			**50**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**±12.5**			**±12.5**			**±12.5**			V
Current	Short Circuit		50			50			50		mA
Output Resistance	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Small Signal	Unity Gain	12.8	16		13.6	16		13.6	16		MHz
Full Power Bandwidth[3]	V_O = ±10 V										
	R_{LOAD} = 500 Ω		1.75			1.75			1.75		MHz
Rise Time			20			20			20		ns
Overshoot			20			20			20		%
Slew Rate		**80**	100		**94**	100		**94**	100		V/μs
Settling Time	10 V Step										
	C_{LOAD} = 100 pF										ns
	R_{LOAD} = 500 Ω										ns
	to 0.01%		350			350	500		350	500	ns
	to 0.1%		250			250			250		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.04			0.04			0.04		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.02			0.02			0.02		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.75**		**±18**	**±4.75**		**±18**	**±4.75**		**±18**	V
Rejection Ratio	V_S = ±5 to ±15 V	**88**	110		**95**	113		**88**	110		dB
Quiescent Current	T_{min} to T_{max}		10	**12**		10	**12**		10	**12**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.

[3]FPBW=slew rate/2π V peak.

[4]"S" grade T_{min}-T_{max} are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Mini-DIP . . . . . 1.6 Watts
  Cerdip . . . . . 1.4 Watts
Input Voltage . . . . . $\pm V_S$
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range
  Q . . . . . −65°C to +150°C
  N . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP package: θ_{JA} = 100°C/watt; cerdip package: θ_{JA} = 110°C/watt.

ORDERING GUIDE*

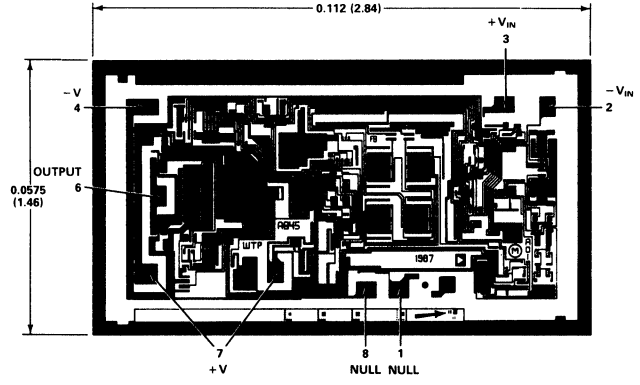
Temperature Range	Mini-DIP Package (N-8)	Cerdip Package (Q-8)
Commercial 0 to +70°C	AD845JN AD845KN	
Industrial −40°C to +85°C		AD845AQ AD645BQ
Military −55°C to +125°C		AD845SQ AD845SQ/883B

"J" Grade Chips Are Also Available.

NOTE
*See Section 20 for package outline information.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



Typical Characteristics

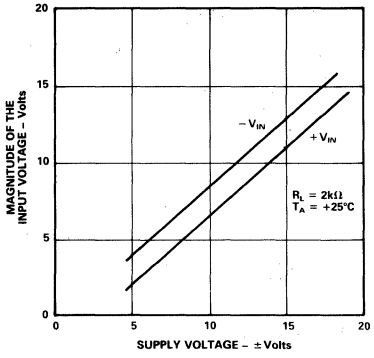


Figure 1. Input Voltage Swing vs. Supply Voltage

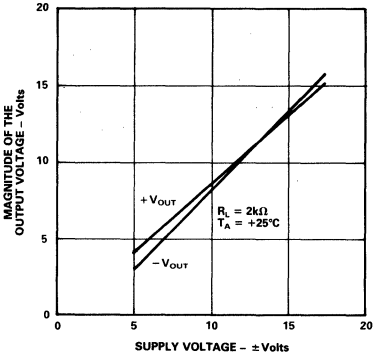


Figure 2. Output Voltage Swing vs. Supply Voltage

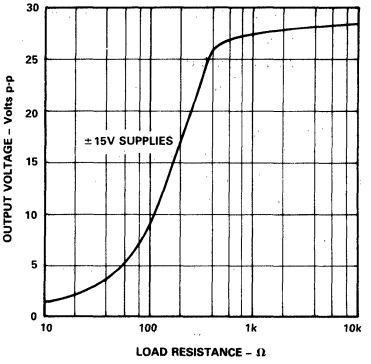


Figure 3. Output Voltage Swing vs. Resistive Load

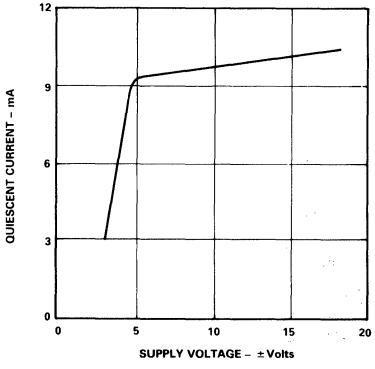


Figure 4. Quiescent Current vs. Supply Voltage

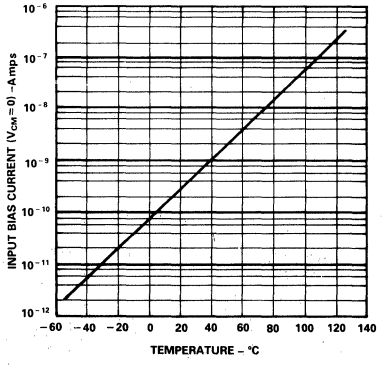


Figure 5. Input Bias Current vs. Temperature

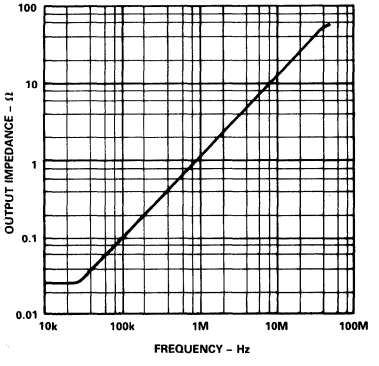


Figure 6. Magnitude of Output Impedance vs. Frequency

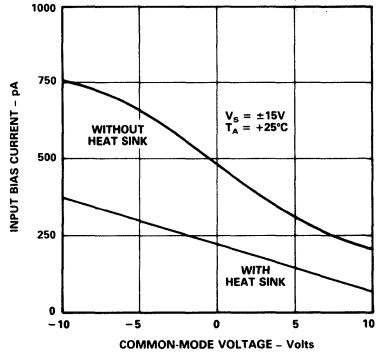


Figure 7. Input Bias Current vs. Common-Mode Voltage

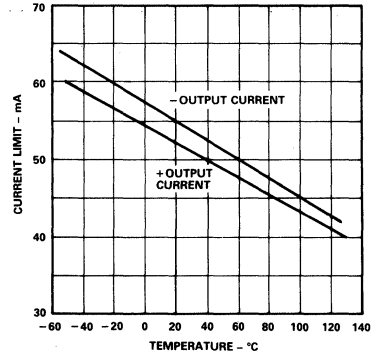


Figure 8. Short-Circuit Current Limit vs. Temperature

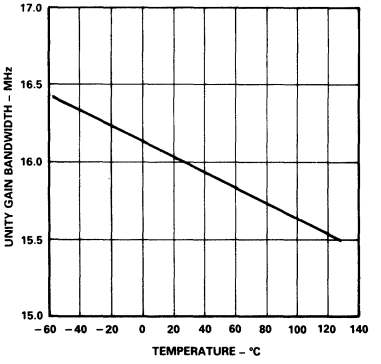


Figure 9. Unity-Gain Bandwidth vs.Temperature

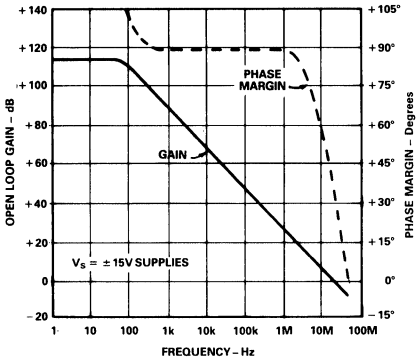


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

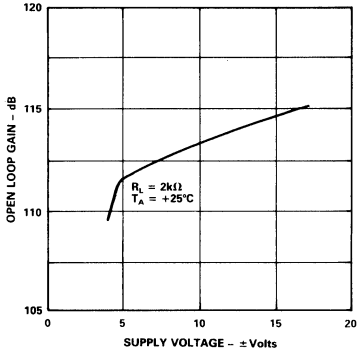


Figure 11. Open-Loop Gain vs. Supply Voltage

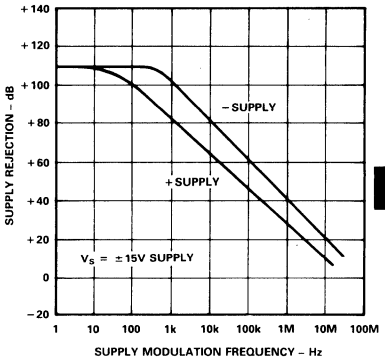


Figure 12. Power Supply Rejection vs. Frequency

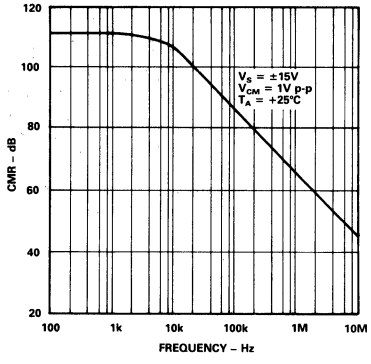


Figure 13. Common-Mode Rejection vs. Frequency

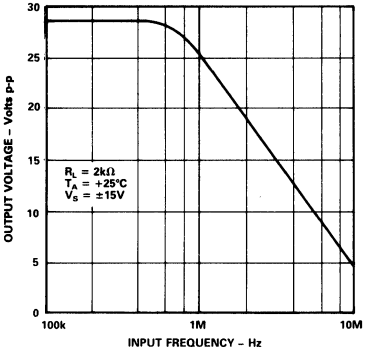


Figure 14. Large Signal Frequency Response

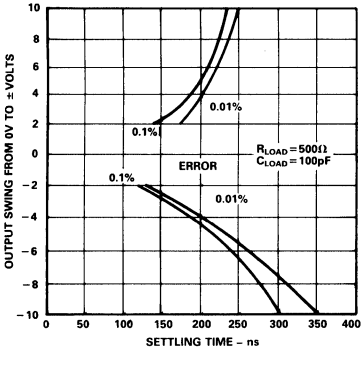


Figure 15. Output Swing and Error vs. Settling Time

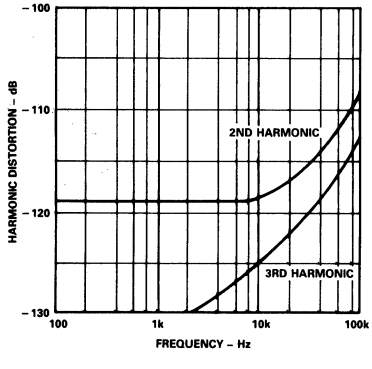


Figure 16. Harmonic Distortion vs. Frequency

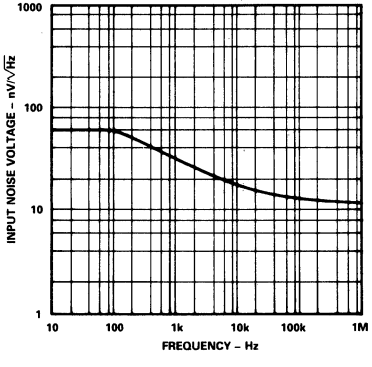


Figure 17. Input Noise Voltage Spectral Density

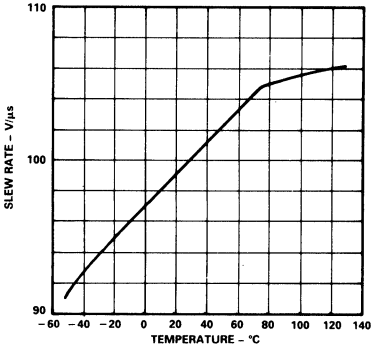


Figure 18. Slew Rate vs. Temperature

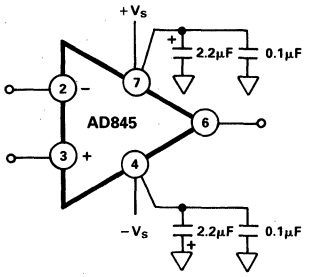


Figure 19. Recommended Power Supply Bypassing

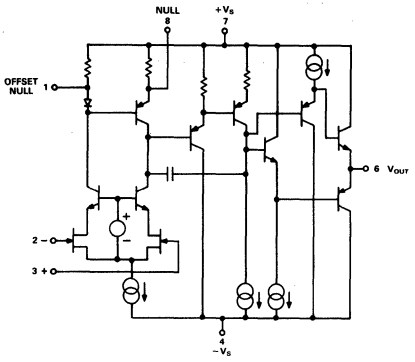


Figure 20. AD845 Simplified Schematic

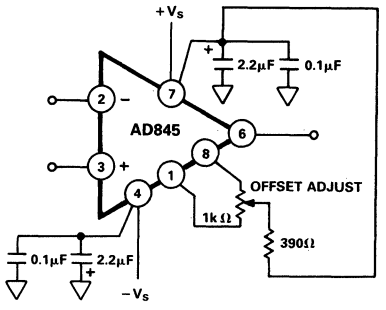


Figure 21. Offset Null Configuration

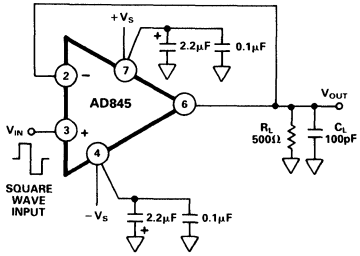


Figure 22a. Unity-Gain Follower

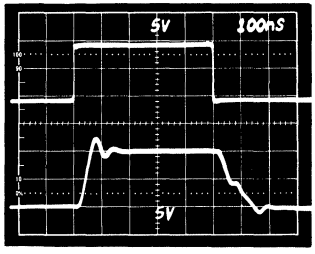


Figure 22b. Unity-Gain Follower Large Signal Pulse Response

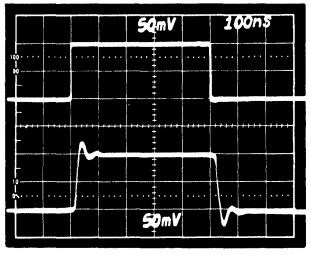


Figure 22c. Unity-Gain Follower Small Signal Pulse Response

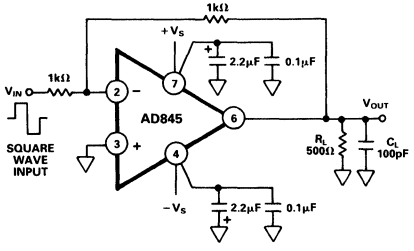


Figure 23a. Unity-Gain Inverter

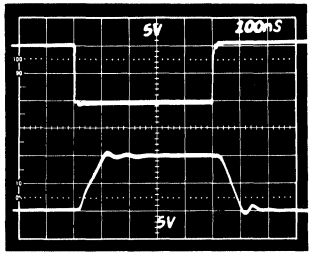


Figure 23b. Unity-Gain Inverter Large Signal Pulse Response

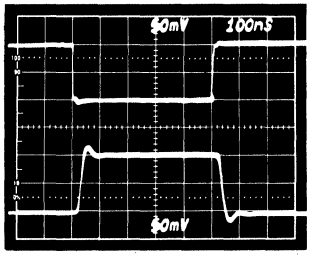


Figure 23c. Unity-Gain Inverter Small Signal Pulse Response

MEASURING AD845 SETTLING TIME

The Figure 24 shows the AD845 settling time performance. This measurement was accomplished by driving the amplifier in the unity-gain inverting mode with a fast pulse generator. The input summing junction was measured using false nulling techniques.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

Components of settling time include:

1. Propagation time through the amplifier
2. Slewing time to approach the final output value
3. Recovery time from overload associated with the slewing
4. Linear settling to within a specified error band.

These individual components can easily be seen in Figure 24. Settling time is extremely important in high speed applications where the current output of a DAC must be converted to a voltage. When driving a 500 Ω load in parallel with a 100 pF capacitor, the AD845 settles to 0.1% in 250 ns and to 0.01% in 310 ns.

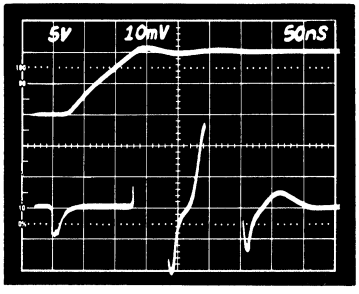


Figure 24. Settling Characteristics 0 to 10 V Step
Upper Trace: Output of AD845 Under Test (5 V/Div)
Lower Trace: Error Voltage (1 mV/Div)

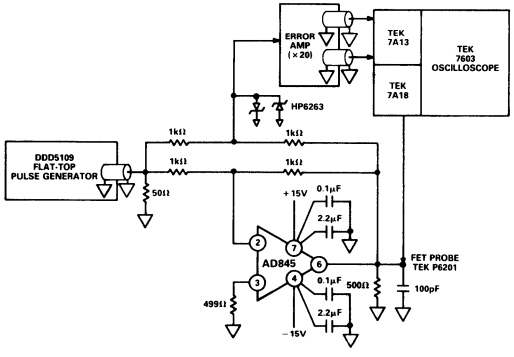


Figure 25. Settling Time Test Circuit

A HIGH SPEED INSTRUMENTATION AMP

The three op amp instrumentation amplifier circuit shown in Figure 26 can provide a range of gains from unity up to 1000 and higher. The instrumentation amplifier configuration features high common-mode rejection, balanced differential inputs and stable, accurately defined gain. Low input bias currents and fast settling are achieved with the FET input AD845.

Most monolithic instrumentation amplifiers do not have the high frequency performance of the circuit in Figure 26. The circuit bandwidth is 10.9 MHz at a gain of 1 and 8.8 MHz at a gain of 10; settling time for the entire circuit is 900 ns to 0.01% for a 10 V step (Gain = 10).

The capacitors employed in this circuit greatly improve the amplifier's settling time and phase margin.

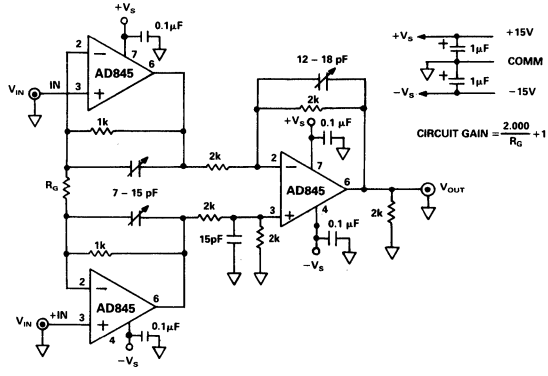


Figure 26. High Performance, High Speed Instrumentation Amplifier

3 OP-AMP IN-AMP

Gain	RG	Small Signal Bandwidth	Settling Time to 0.01%
1	Open	10.9 mHz	500 ns
2	2k	8.8 mHz	500 ns
10	226Ω	2.6 mHz	900 ns
100	20Ω	290 kHz	7.5 μs

Note: Resistors around the amplifiers' input pins need to be small enough in value so that the RC time constant they form, with stray circuit capacitance, does not reduce circuit bandwidth.

Table I. Performance Summary for the Three Op Amp Instrumentation Amplifier Circuit

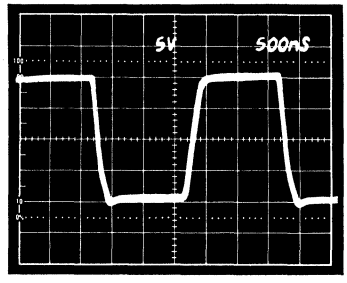


Figure 27. The Pulse Response of the Three Op Amp Instrumentation Amplifier. Gain = 1, Horizontal Scale: 0.5 ms/Div; Vertical Scale: 5 V/Div

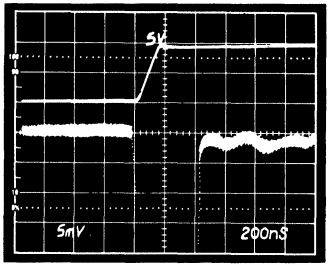


Figure 28a. Settling Time of the Three Op Amp Instrumentation Amplifier. Horizontal Scale:200 ns/Div; Vertical Scale, Positive Pulse Input: 5 V/Div; Output Settling: 1 mV/Div

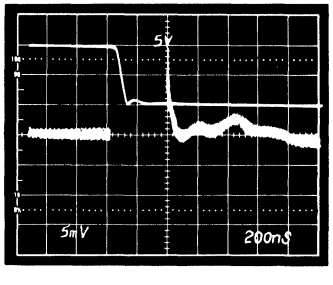


Figure 28b. Settling Time of the Three Op Amp Instrumentation Amplifier. Horizontal Scale: 200 ns/Div; Vertical Scale, Negative Pulse Input: 5 V/Div; Output Settling: 1 mV/Div

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 29, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open-loop value. Most IC amplifiers exhibit a minimum open-loop output impedance of 25 Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD845 is ideally suited to drive high resolution A/D converters with 5 μs on longer conversion times since it offers both wide bandwidth and high open-loop gain.

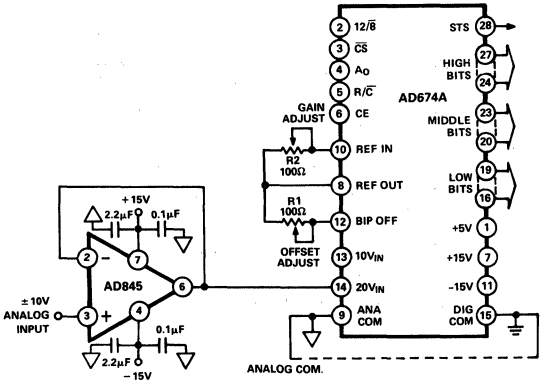


Figure 29. AD845 As ADC Unity Gain Buffer

ANALOG DEVICES

450 V/μs, Precision, Current-Feedback Op Amp

AD846

FEATURES

AC PERFORMANCE
- Small Signal Bandwidth: 80 MHz ($A_V = -1$)
- Slew Rate: 450 V/μs
- Full Power Bandwidth: 6.8 MHz at 20 V p-p, $R_L = 500\ \Omega$
- Fast Settling: for 10 V Step: 110 ns to 0.01%, 80 ns to 0.1%
- Differential Gain: <0.01% @ 4.4 MHz
- Differential Phase: <0.028° @ 4.4 MHz
- Total Harmonic Distortion (THD): 0.0005% @ 100 kHz
- Open-Loop Transimpedance: 200 MΩ
- Input Voltage Noise: 2 nV/$\sqrt{\text{Hz}}$

DC PERFORMANCE
- Input Offset Voltage: 75 μV max (B Grade)
- Input Offset Drift: 3.5 μV/°C max (B Grade)
- Quiescent Supply Current: 6.5 mA max

APPLICATIONS
- High Speed DAC Buffers
- Multiflash ADC Error Amplifiers
- Flash ADC Buffers
- Coaxial Cable Drivers
- High Performance Audio Circuitry
- Available in Plastic Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages
- MIL-STD-883B Parts Available

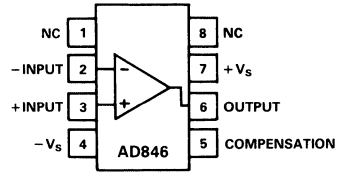
PRODUCT DESCRIPTION

The AD846 is a monolithic, very high speed operational amplifier offering high performance. Although technically classed as a current-feedback or transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.01%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog-to-digital converters.

AD846 CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package
Top View



NC = NO CONNECT

Other advantages include: low input errors and high open-loop transresistance (200 MΩ) into a 500 Ω load, ensuring true 12-bit dc accuracy for closed-loop gains from −1 to gains greater than −100. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high speed DACs and flash ADCs.

The AD846 is available in three performance grades. The AD846A and AD846B are rated over the industrial temperature range of −40°C to +85°C. The AD846S is rated over the full military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C.

Extended reliability PLUS screening is available specified over the commercial temperature range. PLUS screening includes 168 hour burn-in as well as other environmental and physical tests. The AD846 is available in two types of 8-pin package: plastic mini-DIP and hermetic cerdip. "A" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD846 achieves settling times of 110 ns to 0.01% for gains of −1 to −10, with a 450 V/μs slew rate, while consuming only 5 mA of supply current.
2. For closed-loop gains of −1 to −100, the high speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial			25	**200**		25	**75**		25	**200**	μV
T_{min}–T_{max}			50	350		50	**125**		100	**350**	μV
vs. Temperature			0.8	5		0.8	3.5		1	5.5	μV/°C
vs. Supply (PSSR)	5 V–18 V[2]										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{min}–T_{max}		110	120		**116**	120		**94**	116		dB
vs. Common Mode	V_{CM} = ±10 V										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{min}–T_{max}		110	120		**116**	120		**94**	116		dB
INPUT BIAS CURRENT[3]											
–Input Bias Current											
Initial			150	**450**		100	**250**		150	**450**	nA
T_{min}–T_{max}			450	1200		400	**750**		1000	**1500**	nA
vs. Temperature			6	20		6	**17**		9	20	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			9	**15**		9	**10**		9	**15**	nA/V
T_{min}–T_{max}			11	20		11	**15**		11	**25**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**10**		3	**5**		5	**10**	nA/V
T_{min}–T_{max}			5	15		3	**7**		5	**20**	nA/V
+Input Bias Current											
Initial			3	**15**		3	**5**		3	**15**	μA
T_{min}–T_{max}			4	20		4	**7**		5	**20**	μA
vs. Temperature			15	80		15	45		15	80	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			5	**15**		5	**10**		5	**15**	nA/V
T_{min}–T_{max}			5	20		5	**15**		5	**20**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**15**		3	**10**		5	**15**	nA/V
T_{min}–T_{max}			5	15		3	**10**		5	**20**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50			50			50		Ω
+Input			10			10			10		kΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	F = 1 kHz		2			2			2		nV/$\sqrt{Hz}$
Input Current Noise											
–Input	1 kHz		20			20			20		pA/$\sqrt{Hz}$
+Input	1 kHz		6			6			6		pA/$\sqrt{Hz}$
OPEN LOOP TRANSRESISTANCE	V_{OUT} = ±10 V										
	R_{LOAD} = 500 Ω	**100**	200		**150**	200		**100**	200		MΩ
	T_{min}–T_{max}	50			**75**			**50**			MΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	**± 10**			**±10**			**±10**			V
Current	Short Circuit		65			65			65		mA
Output Resistance	Open Loop		16			16			16		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	A_V = −1 R_F = 1 k		80			80			80		MHz
(−3dB)	A_V = −10 R_F = 875 Ω		31			31			31		MHz
	A_V = −30 R_F = 875 Ω		15			15			15		MHz
Full Power Bandwidth[4]	V_{OUT} =20 V p-p										
	R_I = 500 Ω		6.8			6.8			6.8		MHz
Rise Time	A_V = −1		10			10			10		ns
Overshoot	A_V = −1		20			20			20		%
Slew Rate	A_V = −1		450			450			450		V/μs
Settling Time											
10 V Step, A_V = −1	to 0.1%		80			80			80		ns
	to 0.01%		110			110			110		ns
TOTAL HARMONIC DISTORTION[5]	F = 100 kHz		0.0005			0.0005			0.0005		%

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
DIFFERENTIAL GAIN	F = 4.4 MHz, R_L = 100 Ω		0.01			0.01			0.01		%
DIFFERENTIAL PHASE	F = 4.4 MHz, R_L = 100 Ω		0.028			0.028			0.028		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		± 18	±5		±18	±5		±18	V
Quiescent Current	T_{min}–T_{max}		5	6.5		5	6.5		5	7	mA
TRANSISTOR COUNT			72			72			72		

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Test Conditions: $+V_S$ = 15 V, $-V_S$ = 5 V to 18 V and $+V_S$ = 5 V to 18 V, $-V_S$ = ±15 V.
[3]Bias Current Specifications are guaranteed maximum after 5 minutes at T_A = +25°C.
[4]FPBW = Slew Rate/2 π V_{PEAK}.
[5]Total Harmonic Distortion.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic Package . . . . . 1.3 W
Cerdip Package . . . . . 1.3 W
Input Voltage[3] . . . . . ±18 V
Common-Mode Input Voltage . . . . . $|V_S|$ −3 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±1 V
Continuous Input Current
Inverting or Noninverting . . . . . 2.0 mA
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Operating Temperature Range
AD846A/B . . . . . −40°C to +85°C
AD846S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Plastic Package: θ_{JA} = 90°C/Watt.
Cerdip Package: θ_{JA} = 110°C/Watt.
[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING GUIDE*

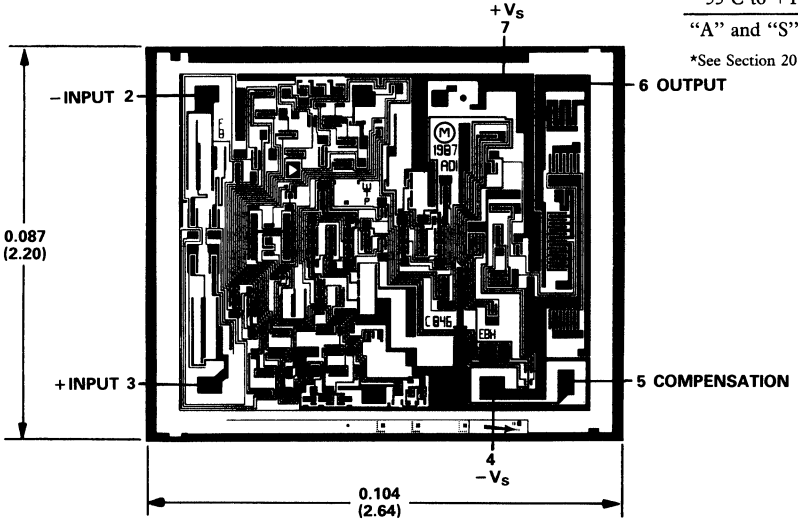
Temperature Range	Mini-DIP (N-8)	Cerdip (Q-8)
Industrial −40°C to +85°C	AD846AN AD846BN	AD846AQ AD846BQ
Military −55°C to +125°C		AD846SQ AD846SQ/883B

"A" and "S" grade chips are also available.

*See Section 20 for package outline information.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Consult factory for latest dimensions.



Typical Characteristics

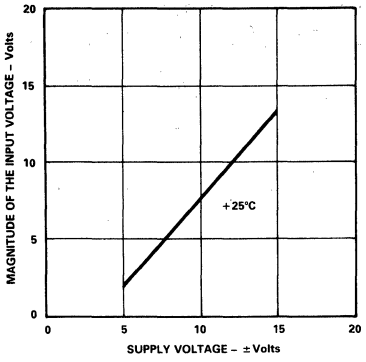


Figure 1. Input Voltage Swing vs. Supply

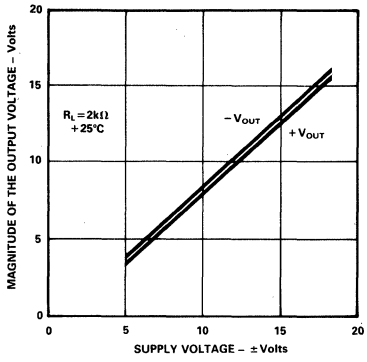


Figure 2. Output Voltage Swing vs. Supply

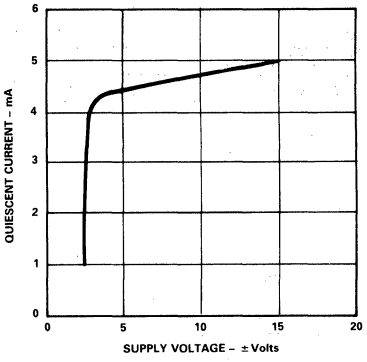


Figure 3. Quiescent Current vs. Supply Voltage

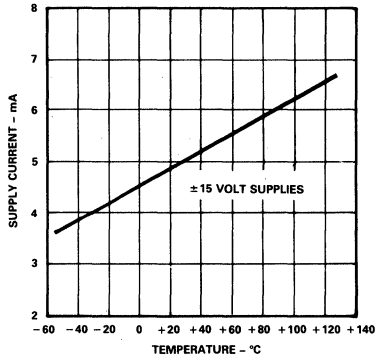


Figure 4. Quiescent Supply Current vs. Temperature

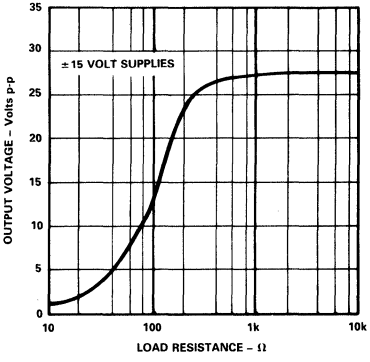


Figure 5. Output Voltage Swing vs. Resistive Load

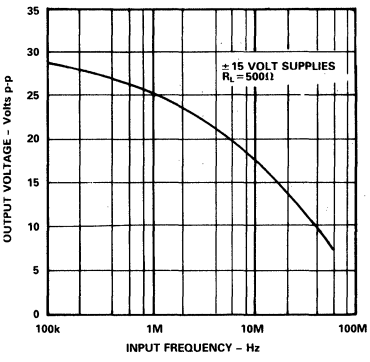


Figure 6. Large Signal Frequency Response

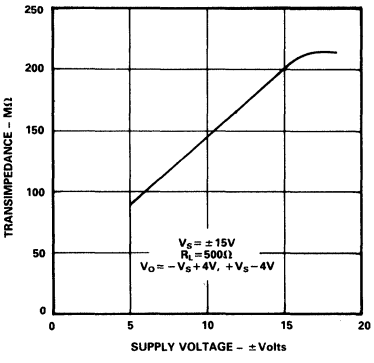


Figure 7. Open-Loop Trans-impedance vs. Supply

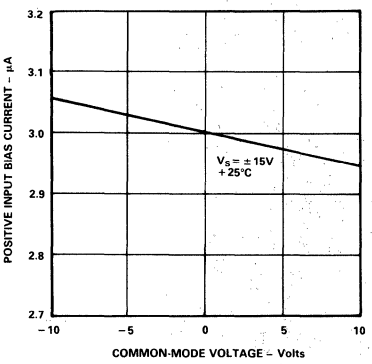


Figure 8. Positive Input Bias Current vs. Common-Mode Voltage

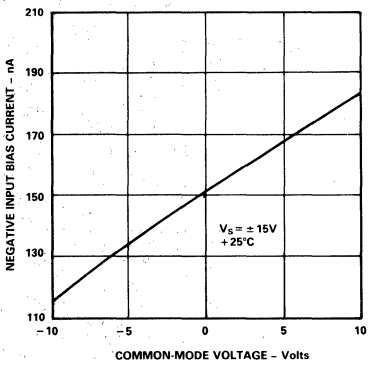


Figure 9. Negative Input Bias Current vs. Common-Mode Voltage

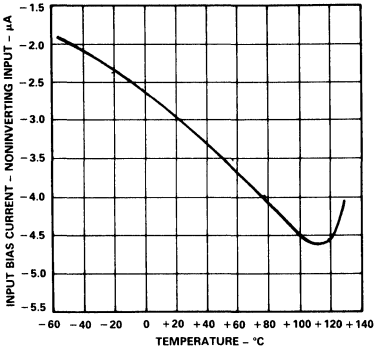


Figure 10. Positive Input Bias Current vs. Temperature

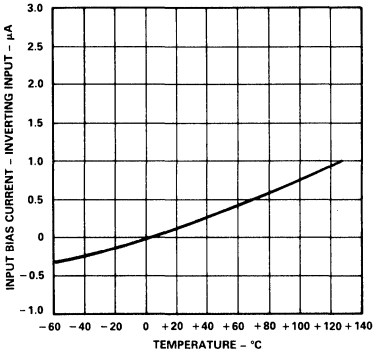


Figure 11. Negative Input Bias Current vs. Temperature

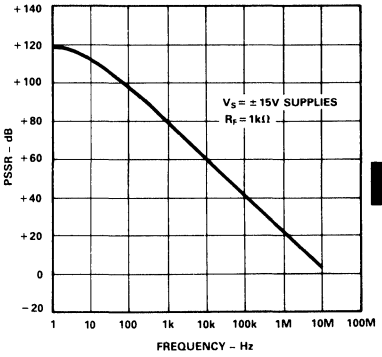


Figure 12. Power Supply Rejection vs. Frequency

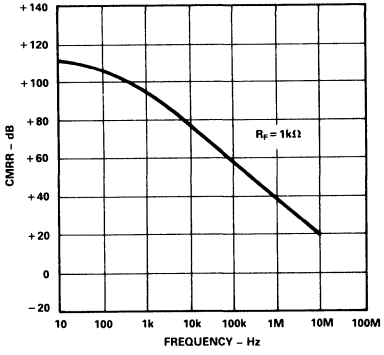


Figure 13. Common-Mode Rejection vs. Frequency

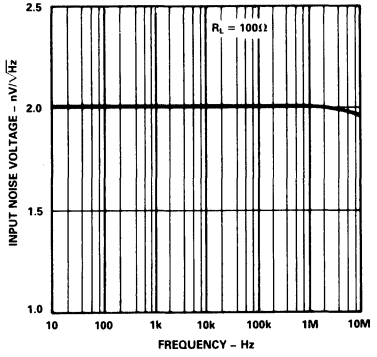


Figure 14. Input Noise Voltage Spectral Density

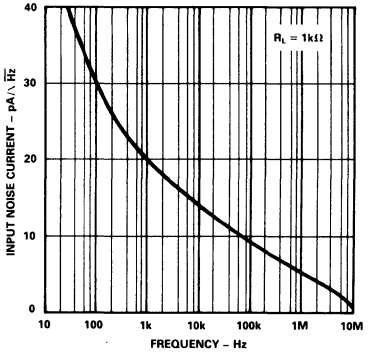


Figure 15. Inverting Input Noise Current Spectral Density

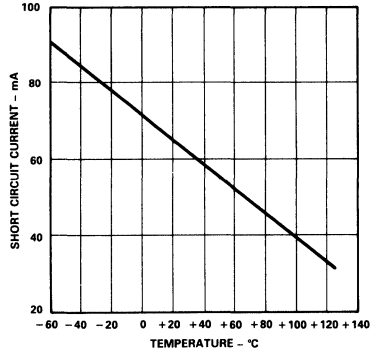


Figure 16. Short Circuit Current Limit vs. Temperature

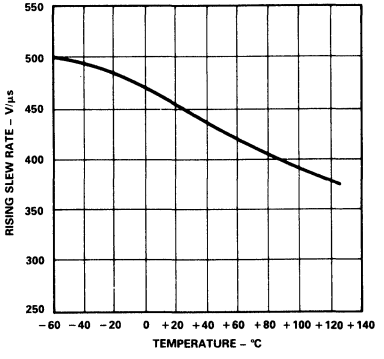


Figure 17. Slew Rate vs. Temperature

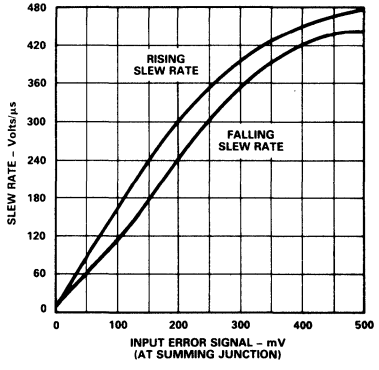


Figure 18. Slew Rate vs. Input Error Signal

Typical Characteristics, Inverting Gain of 1

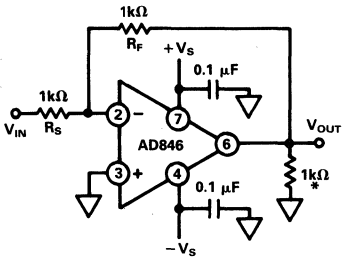


Figure 19a. Inverting Amplifier, Gain of 1

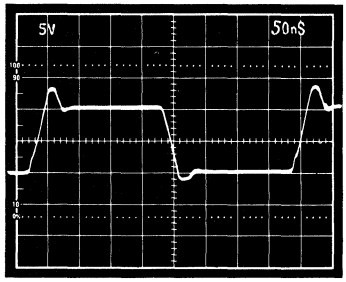


Figure 19b. Large Signal Pulse Response, Gain of −1

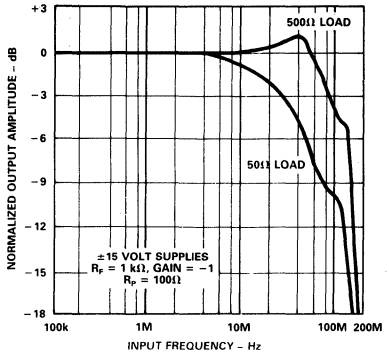


Figure 20. Normalized Output Amplitude vs. Frequency vs. Load

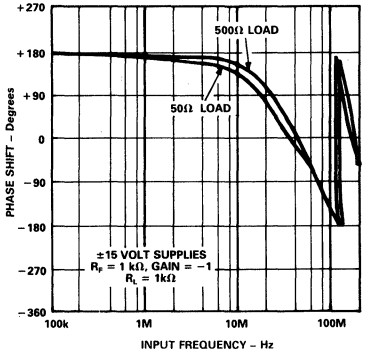


Figure 21. Phase Shift vs. Frequency

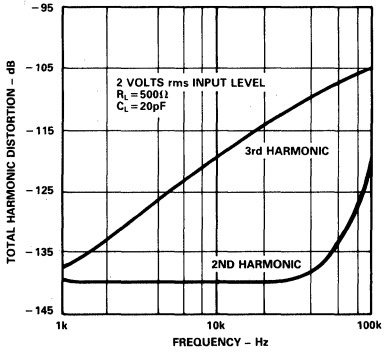


Figure 22. Total Harmonic Distortion vs. Frequency

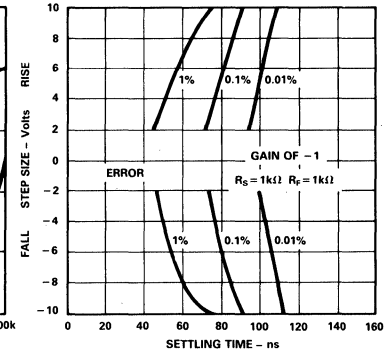


Figure 23. Settling Time vs. Step Size

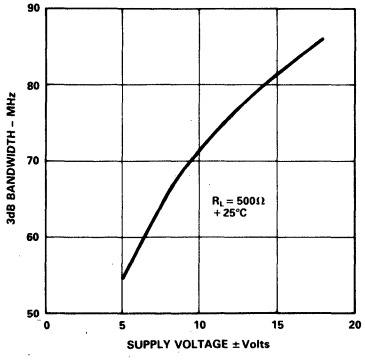


Figure 24. 3 dB Bandwidth vs. Supply Voltage

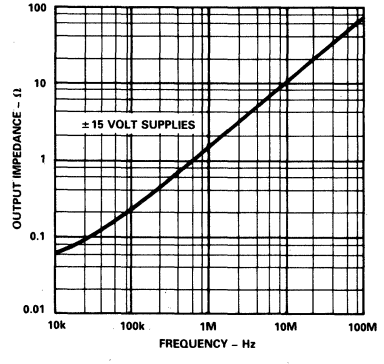


Figure 25. Output Impedance vs. Frequency

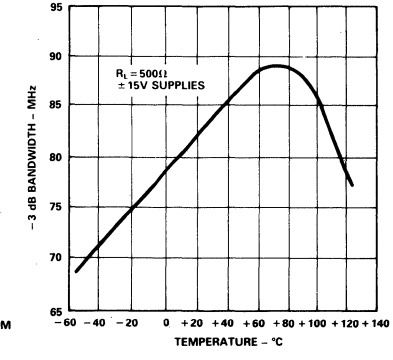


Figure 26. 3 dB Bandwidth vs. Temperature

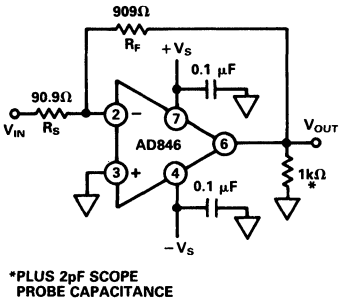


Figure 27a. Inverting Amplifier, Gain of 10

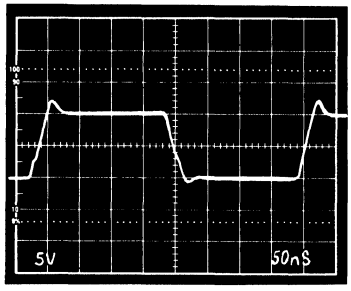


Figure 27b. Large Signal Pulse Response, Gain of 10

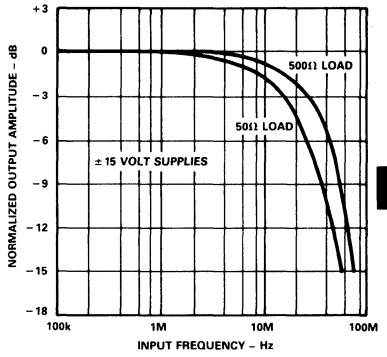


Figure 28. Normalized Output Amplitude vs. Frequency vs. Load

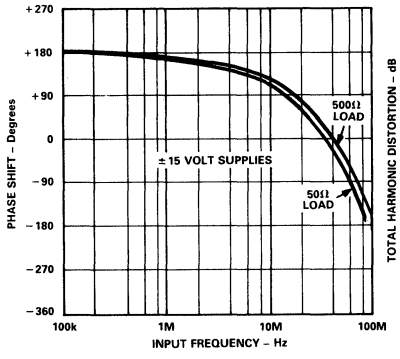


Figure 29. Phase vs. Frequency vs. Load

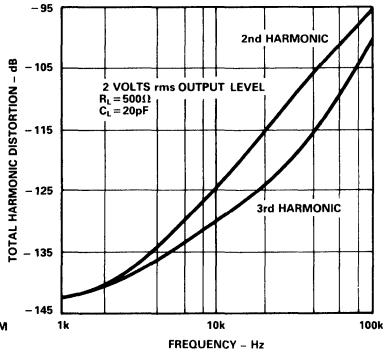


Figure 30. Harmonic Distortion vs. Frequency

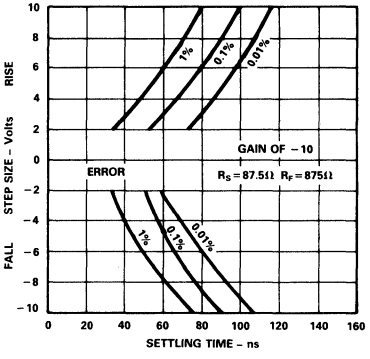


Figure 31. Settling Time vs. Step Size

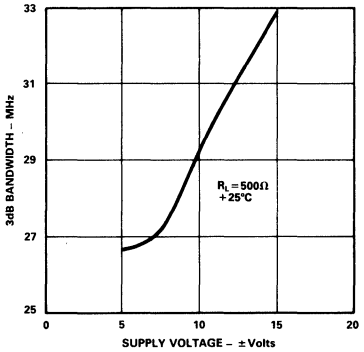


Figure 32. 3 dB Bandwidth vs. Supply Voltage

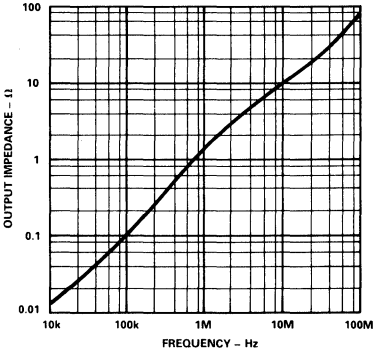


Figure 33. Output Impedance vs. Frequency

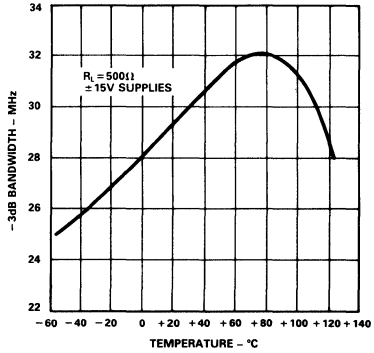


Figure 34. 3 dB Bandwidth vs. Temperature

Applying the AD846

POWER SUPPLY CONSIDERATIONS

The power supply connections to the AD846 must maintain a low impedance to ground over a bandwidth of 40 MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1 μF ceramic and a 2.2 μF electrolytic capacitor as shown in Figure 35 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1 μF should be used for any application. At high temperatures, it is advisable to power-up the positive power supply before the negative.

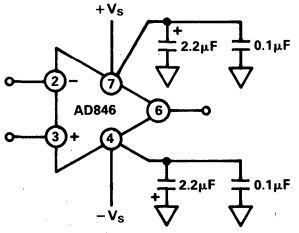


Figure 35. Recommended Power Supply Bypassing

THEORY OF OPERATION

The AD846 differs from conventional operational amplifiers in that it is a transimpedance device rather than a conventional voltage amplifier. Figure 36 is a simplified schematic of the AD846. The input stage consists of a pair of transistors, Q1 and Q2, which are biased by two diode-connected transistors, Q3 and Q4. Transistors Q1 and Q2 have their emitters connected together, and this common point functions as the inverting input of the amplifier. Correspondingly, the common connection of the two biasing diodes acts as the noninverting input.

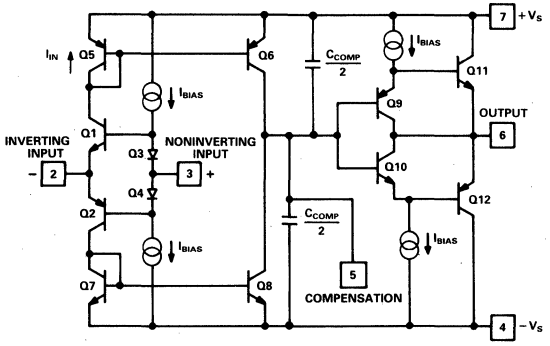


Figure 36. AD846 Simplified Schematic

When operated as a closed-loop amplifier, feedback error current, I_{IN}, flows into the inverting input terminal and is conveyed via current mirrors (transistors Q5, Q6, Q7, and Q8) to the compensation capacitor, C_{COMP}. The voltage developed across C_{COMP} is buffered by the output stage, consisting of transistors Q9–Q12.

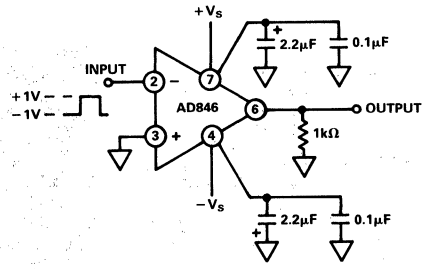


Figure 37. Overload Recovery Test Circuit

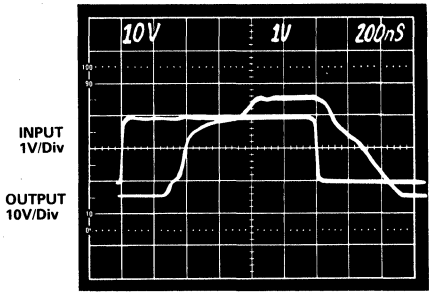


Figure 38. Overload Recovery Time Photo

Because the input error signal developed is in the form of a current, not a voltage, the AD846 differs from conventional operational amplifiers. This also means that, unlike most operational amplifiers which rely on negative feedback to produce a "virtual ground" at the inverting input terminal, this terminal explicitly has a low impedance.

A unique circuit approach allows the AD846 to realize an open-loop transimpedance of close to 200 MΩ. This is nearly three orders of magnitude greater than that of any other operational transimpedance amplifier and results in extremely high levels of dc precision.

As an example, the output voltage gain error is approximately equal to the value of the feedback resistor divided by the value of the open-loop transimpedance of the amplifier. That is, when using a 1 kΩ feedback resistor, this error is one part in 200,000. For a transimpedance amplifier with 1 MΩ transimpedance, this error is only one part in 1000; such an amplifier would barely be able to achieve 10-bit precision.

Figure 39 is a simplified three-terminal model for the AD846. Figure 40 is a simplified three-terminal model for a conventional voltage op amp. The action of current feedback serves to modify the behavior of the amplifier under closed-loop conditions. The feedback resistor, R_F, is somewhat analogous to the input stage transconductance of a conventional voltage amplifier; and therefore, if the value of R_F is held constant, the closed-loop bandwidth also remains virtually constant, independent of closed- loop voltage gain.

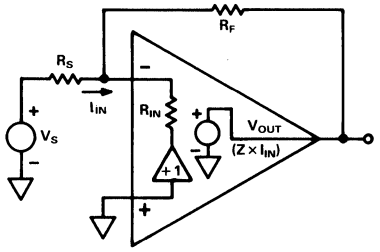


Figure 39. AD846 Three-Terminal Model

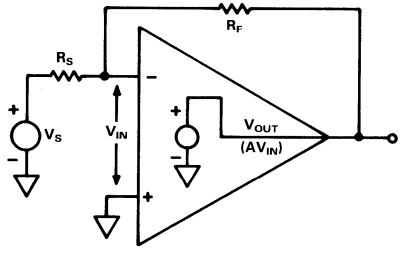


Figure 40. Op Amp Three-Terminal Model

A more detailed examination of the closed-loop transfer function of the AD846 results in the following equation:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{\left(1 + C_{COMP}\left[R_F + \left(1 + \frac{R_F}{R_S}\right)R_{IN}\right]s\right)}$$

Compare this to the equation for a conventional op amp:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{\left(1 + \frac{C_{COMP}}{g_M}\left(1 + \frac{R_F}{R_S}\right)s\right)}$$

where: C_{COMP} is the internal compensation capacitor of the amplifier; g_M is the input stage transconductance of the amplifier.

In the case of the voltage amplifier, the closed-loop bandwidth decreases directly with increasing values of $(1 + R_F/R_S)$, the closed-loop gain. However, for the transimpedance amplifier, the situation is different. At low gains, where $(1 + R_F/R_S)\ R_{IN}$ is small compared to R_F, the closed-loop bandwidth is controlled by the internal compensation capacitance of 7 pF and the value of R_F, and not by the closed-loop gain. At higher gains, where $(1 + R_F/R_S)\ R_{IN}$ is much larger than R_F, the behavior is that of a conventional operational amplifier in which the input stage transconductance is equal to the inverting terminal input impedance of the transimpedance amplifier (R_{IN} = 50 Ω).

A simple equation can, therefore, be used to determine the bandwidth of an amplifier employing the AD846 in the inverting configuration.

$$3\ dB\ Bandwidth = \frac{23}{R_F + 0.05\ (1 + G)}$$

where: The 3 dB bandwidth is in MHz
G is the closed-loop inverting gain of the AD846
R_F is the feedback resistance in kΩ.

NOTE: This equation applies only for values of R_F between 10 kΩ and 100 kΩ, and for R_{LOAD} greater than 500 Ω. For R_F = 1 kΩ the bandwidth should be estimated from Figure 41.

Figure 41 illustrates the closed-loop voltage gain vs. frequency of the AD846 for various values of feedback resistor. For comparison purposes, the characteristic of a conventional amplifier having an 80 MHz unity gain bandwidth is also shown.

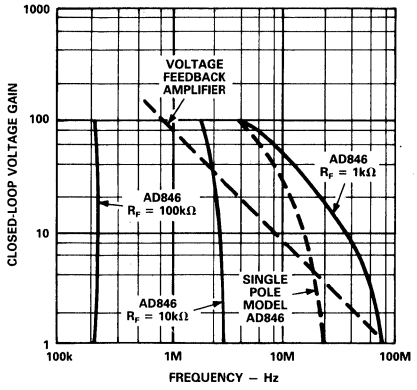


Figure 41. Closed-Loop Voltage Gain vs. Frequency for Various Values of R_F

For the case where R_F = 1 kΩ and R_S = 100 Ω (closed-loop gain of −10), the closed-loop bandwidth is approximately 28 MHz. It should also be noted that the use of a capacitor to shunt R_F, a normal practice for stabilizing conventional op amps, will cause this amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency.

A similar approach can be taken to calculate the noise performance of the amplifier. A simplified noise model is shown in Figure 42.

The equivalent mean-square output noise voltage spectral density will equal:

$$V_{ON}^2 = (R_F I_{NN})^2 + \left(1 + \frac{R_F}{R_S}\right)^2 [V_N^2 + (R_P I_{NP})^2 + 4\ kT\ R_P] + 4\ kT\ R_F\left(\frac{R_F}{R_S} + 1\right)$$

Where:

R_P is the external resistance placed in series with the noninverting input
R_F is the feedback resistor
R_S is the source resistor
I_{NN} is the noise current in the inverting input
I_{NP} is the noise current in the noninverting input
V_N is the input noise voltage.

Typical values for these parameters (@ 1 kHz) in pA/$\sqrt{\text{Hz}}$ are: I_{NN} = 20, I_{PN} = 6, V_N = 2.

Or, referring to the signal input, the equivalent mean-square input voltage noise is:

$$V_{IN}^2 = (R_F I_{NN})^2 + \left(1 + \frac{R_S}{R_F}\right)^2 [V_N^2 + (R_P I_{NP})^2 + 4 kT R_P]$$

$$+ 4 kT R_S \left(1 + \frac{R_S}{R_F}\right)$$

Resistor R_P is required for both inverting and noninverting (follower) operation, to insure stable operation. The amplifier's noninverting input current (flowing through R_P of 100 Ω) will typically add less than 300 μV to the AD846's input offset voltage. This can be trimmed-out using the optional network shown in Figure 44. The following table gives recommended values for R_P.

Supply Voltage	Gain (R_F/R_S)	Recommended Value for R_P
6 V to 15 V	1–10	100 Ω
6 V to 15 V	10–20	47 Ω
6 V to 15 V	20–200	0 Ω
5 V	1–10	47 Ω
5 V	10–200	0 Ω

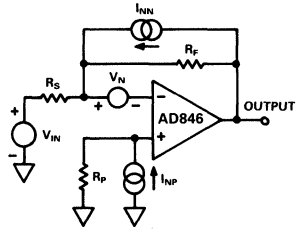


Figure 42. Op Amp Simplified Noise Model

NONINVERTING GAIN OPERATION

The AD846 can be used as a noninverting amplifier or voltage follower, operating at gains between 1 and 200. A minimum value of R_F equal to 1 kΩ should be employed. For low gains (1 to 2), the input signal should be applied to the AD846's noninverting input through a 100 Ω series resistor; this will help reduce peaking. The best transient response will occur when the amplifier's output level is below 5 V peak to peak.

At closed-loop gains of 3 or more, the input resistor is not required unless peak signals greater than 3 V will be applied. The amplifier's bandwidth can be determined by using the inverting amplifier's bandwidth equation or from Figure 41. For example, at a gain of +10 (R_F = 1 kΩ, R_S = 100 Ω) the bandwidth of the AD846 will be approximately 20 MHz; at a gain of +100, (R_F = 1 kΩ, R_S = 10 Ω) it will be 6 MHz. At gains of 3 or greater, a small capacitor (2 pF–5 pF) connected across the feedback resistor will help reduce overshoot; but when operating at noninverting gains below 3, this same capacitance will cause instability.

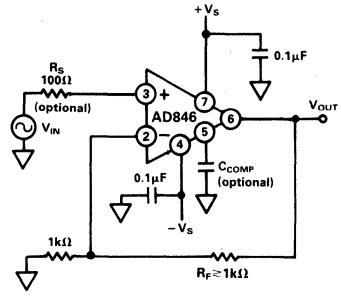


Figure 43. AD846 Noninverting Amplifier Configuration

USING THE COMPENSATION PIN OF THE AD846

Additional compensation may be provided for the AD846 by applying an external capacitance between Pin 5 and analog ground (Figure 44). The nominal value of the AD846's internal compensation capacitor is 7 pF. For a given value of feedback resistance (R_F), any added external capacitance reduces the amplifier's slew rate and bandwidth proportionally.

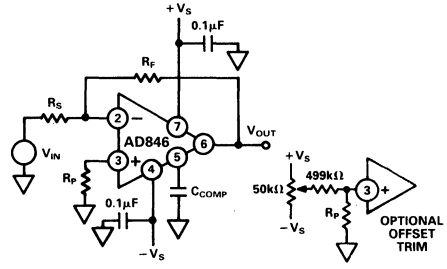


Figure 44. AD846 Inverting Amplifier Showing External Compensation Connection, R_P and Optional V_{OS} Trim

In addition to providing for external compensation, Pin 5 may be used to clamp the output of the amplifier, as shown in Figure 45. The output can be clamped anywhere within the output range (approximately ±10 V) of the amplifier. The input should also be clamped as a precaution against damaging the amplifier's input transistors.

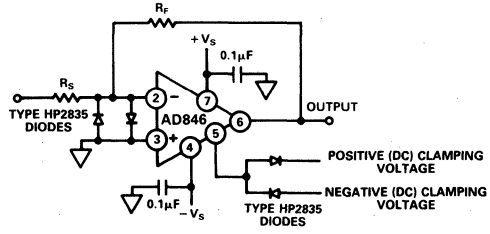


Figure 45. AD846 Used as a Clamped Amplifier

This compensation node may also be used as an additional output terminal as in the precision transconductance amplifier application of Figure 46.

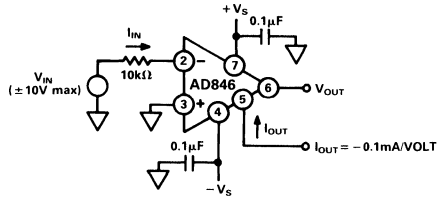


Figure 46. A Precision Transconductance Amplifier

The AD846 can be used in either the inverting transconductance mode as shown in Figure 46, or in a noninverting mode with R_S grounded and V_S applied to the noninverting terminal. The current output is essentially constant over a compliance range of ±10 V at the compensation node. The output current (from Pin 5) is limited to about ±1 mA due to internal saturation. Under these circumstances the normal output pin provides a buffered version of the compensation node output voltage. Output load impedance of 500 Ω or greater will not affect the accuracy of the transconductance conversion.

THE AD846 IN A 2 MHz, 12-BIT SUBRANGING A/D CONVERTER CIRCUIT

The combination of fast settling times at high gains and low dc errors make the AD846 ideal for use as an error amplifier in high speed, 12-bit subranging A-D applications. In the circuit of Figure 47, an AD842 serves as an input amplifier. First pass conversion is accomplished, in a straightforward manner, determining the top 7 bits. The latch then holds these top 7 bits which are applied to a 7 bit, 12-bit accurate DAC and also to the highest 7 bits of the adder (note that a sample-and-hold should be used ahead of this converter to minimize errors due to its 500 ns acquisition time). In the second pass, the input switches S1 and S2 and S3 are set to state 2. The DAC output is then subtracted from the input signal and the resulting difference is then amplified by an AD846 gain of 32 follower. This gain, together with a 1/64th scale offset, insures a unipolar residue which can be converted by the flash A-D. Conversion is accomplished via switches S1, S2 and S3 in state 1. Switch S1 connects the input signal of the AD846 residue amplifier to ground which minimized overload recovery time.

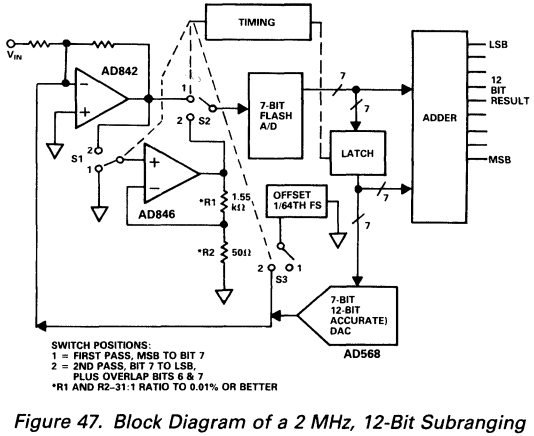


Figure 47. Block Diagram of a 2 MHz, 12-Bit Subranging A/D Converter

THE AD846 AS AN OPEN-LOOP LEVEL SHIFTER

The AD846 can also be used for open-loop level shifting. As shown in Figure 48, resistor R_S is used to develop an input current which is proportional to the input voltage, V_{IN}. This current flows from the compensation node (Pin 5) developing a voltage across resistor R_C (R_C is equal in value to resistor R_S) which, rather than being grounded, has one end tied to reference voltage V2. The voltage appearing at Pin 5 is, therefore, voltage V_{IN} plus voltage V2 and will directly follow changes in V_{IN}. By scaling resistor R_C, a level shift with voltage gain can be produced.

In addition, the normal voltage output at Pin 6 is approximately equal to the voltage at Pin 5 thus providing a low impedance, buffered output for the level shifter.

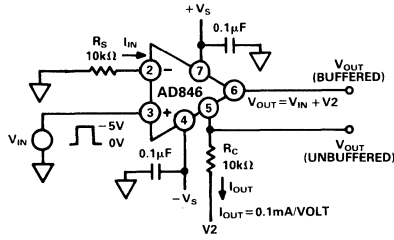


Figure 48. AD846 Connected as a Level Shift Amplifier

THE AD846 AS A HIGH SPEED DAC BUFFER

The AD846 will enable the AD568 12-bit DAC to develop a 10 V output step which settles to within 0.025 percent of its final value in about 100 ns. This AD846/AD568 combination is shown in the circuit of Figure 49. Correct power supply decoupling is essential: a 2.2 μF tantalum capacitor connected in parallel with a 0.1 μF to 0.01 μF ceramic disc capacitor is usually sufficient. These should be placed as close to the power supply pins as possible. Also, a ground plane should be employed; this ensure that there is a low impedance signal path to ground which allows the fastest possible output settling. In 12-bit systems with the AD846 operating at gains of 10 or less, inadequate supply decoupling can cause the output settling to degrade from 100 ns to as much as 300 ns, with a 10 V output step applied.

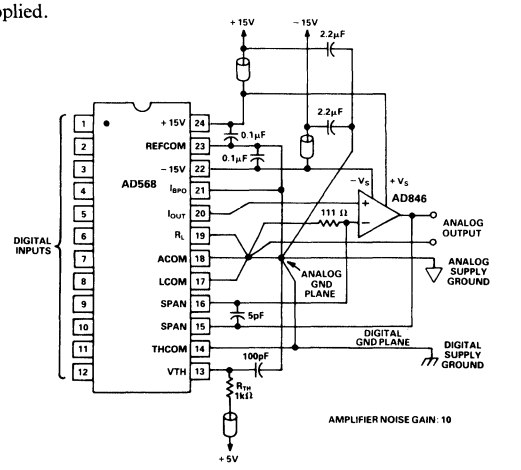


Figure 49. The AD846 Serving as a DAC Buffer

High Speed, Low Power Monolithic Op Amp

AD847

FEATURES
50 MHz Unity Gain Bandwidth
4.8 mA Supply Current
300 V/μs Slew Rate
120 ns Settling Time to 0.1% for a 10 V Step
0.04% Differential Gain
0.19° Differential Phase
Drives Capacitive Loads

DC Performance
5.5 V/mV Open-Loop Gain into a 1 kΩ Load
1 mV max Input Offset Voltage

Performance Specified for ±5 V and ±15 V Operation
Available in Plastic, Hermetic Cerdip and Small Outline Packages; Chips and MIL-STD-883B Processing Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Dual Version Available: AD827

APPLICATIONS
Unity Gain Buffer
Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video and R_F Amplification
Signal Generators

PRODUCT DESCRIPTION

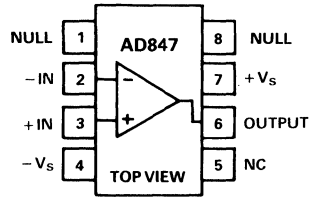
The AD847 is a high speed, low power monolithic operational amplifier. The AD847 achieves its combination of fast ac and good dc performance by utilizing Analog Devices' junction isolated complementary bipolar (CB) process. This process enables the AD847 to achieve its high speed while only requiring 4.8 mA of current from the power supplies.

The AD847 is a member of Analog Devices' family of high speed op amps. This family includes, among others, the AD848, which is stable at a gain of five or greater, and the AD849, which offers 725 MHz of gain bandwidth at gains of 25 or greater. For more demanding applications, the AD840, AD841 and AD842 offer even greater precision and greater output current drive.

The AD847 also has good dc performance. When operating with ±5 V supplies, it offers an open loop gain of 3,500 V/V (with a 500 Ω load) and low input offset voltage of 1 mV maximum (A/S grades). Common mode rejection is a minimum of 80 dB. Output voltage swing is ±3 V even into loads as low as 150 Ω.

AD847 CONNECTION DIAGRAM

Plastic (N)
Small Outline (R) and
Cerdip (Q) Packages



NC = NO CONNECT

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD847 make it ideal for all types of video instrumentation circuitry, fast DAC and flash ADC buffers, and line drivers.
2. As a buffer, the AD847 offers a full-power bandwidth of 30 MHz (for 2 V p-p with V_S = ±5 V) making it outstanding as an input buffer for flash A/D converters.
3. In order to meet the needs of both video and data acquisition applications, the AD847 is optimized and tested for ±5 V and ±15 V power supply operation.
4. The low power and small outline packaging of the AD847 make it very well suited for high density applications such as multiple pole active filters.
5. The AD847 is internally compensated for unity gain operation and remains stable when driving any capacitive load.
6. Laser wafer trimming reduces the input offset voltage to less than 1 mV maximum on all AD847 grades, thus eliminating the need for external offset nulling in many applications.
7. The AD847 is an enhanced replacement for the LM6161 series and can function as a pin for pin replacement for many high speed amplifiers such as the HA2544, HA2520/2/5 and the EL2020.

SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD847J Min	AD847J Typ	AD847J Max	AD847A/S Min	AD847A/S Typ	AD847A/S Max	Units
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	**1**		0.5	**1**	mV
	T_{min} to T_{max}				3.5			**4**	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	**6.6**		3.3	**5**	µA
	T_{min} to T_{max}				7.2			**7.5**	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	**300**		50	**300**	nA
	T_{min} to T_{max}				400			**400**	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD}= 500 Ω		**2**	3.5		**2**	3.5		V/mV
	T_{min} to T_{max}		1			**1**			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		**3**	5.5		**3**	5.5		V/mV
	T_{min} to T_{max}		1.5			**1.5**			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_O = 5 V p-p								
	R_L = 500 Ω,	±5 V		12.7			12.7		MHz
	V_O= 20 V p-p,								
	R_L = 1kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]		±5 V		200			200		V/µs
	R_{LOAD} = 1 kΩ	±15 V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = 21	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degree
Differential Gain	f = 4.4 MHz	±15 V		0.04			0.04		%
Differential Phase	f = 4.4 MHz	±15 V		0.19			0.19		Degree
COMMON MODE REJECTION	V_{CM} = 62.5 V	±5 V	**78**	95		**80**	95		dB
	V_{CM} = ±12 V	±15 V	**78**	95		**80**	95		dB
	T_{min} to T_{max}		75			**75**			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		**75**	86		**75**	86		dB
	T_{min} to T_{max}		72			**72**			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 1 kΩ	±15 V	**12**			12			±V
	R_{LOAD} = 500 Ω	±15 V	**10**			**10**			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			± 4.5		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5 V		4.8	**6.0**		4.8	**5.7**	mA
	T_{min} to T_{max}				7.3			**7.0/7.8**	mA
		±15 V		5.3	**6.3**		5.3	**6.3**	mA
	T_{min} to T_{max}				7.6			**7.6/8.4**	mA

NOTES

[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full Power Bandwidth = Slew Rate/2π V_{PEAK}.

[3]Slew Rate is measured on rising edge.

All min and max specifications are guaranteed. Specifications in **boldface** are 100% tested at final electrical test.

Specifications subject to change without notice.

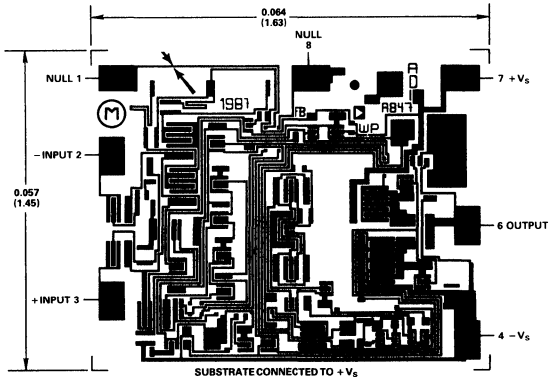
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic (N) . . . . . 1.2 Watts
  Small Outline (R) . . . . . 0.8 Watts
  Cerdip (Q) . . . . . 1.1 Watts
Input Voltage . . . . . $\pm V_S$ Differential
Input Voltage . . . . . 6 V
Storage Temperature Range Q . . . . . −65°C to +150°C
  N, R . . . . . −65°C to +125°C
Junction Temperature . . . . . 175°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP Package: θ_{JA} = 100°C/Watt
Cerdip Package: θ_{JA} = 110°C/Watt
Small Outline Package: θ_{JA} = 155°C/Watt

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ORDERING GUIDE[1]

Model	Gain Bandwidth MHz	Minimum Stable Gain	Maximum Offset Voltage mV	Temperature Range – °C	Package Options[2]
AD847JN	50	1	1	0 to +70	Plastic (N-8)
AD847JR	50	1	1	0 to +70	SOIC (R-8)
AD847AQ	50	1	1	−40 to +85	Cerdip (Q-8)
AD847SQ	50	1	1	−55 to +125	Cerdip (Q-8)
AD847SQ/883B	50	1	1	−55 to +125	Cerdip (Q-8)
AD848J/A/S	175	5	1	See AD848 Data Sheet	
AD849J/A/S	725	25	1	See AD849 Data Sheet	

NOTES
[1]J and S grade chips also available. AD847JR available in tape and reel.
[2]See Section 20 for package outline information.

Typical Characteristics (@ +25°C and $V_S = \pm 15V$, unless otherwise noted)

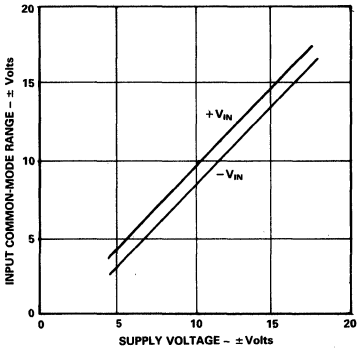


Figure 1. Input Common-Mode Range vs. Supply Voltage

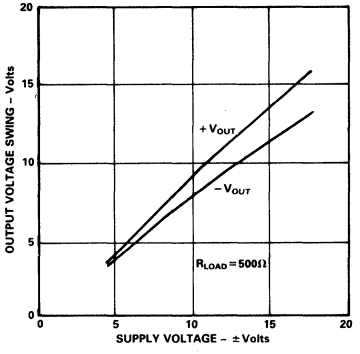


Figure 2. Output Voltage Swing vs. Supply Voltage

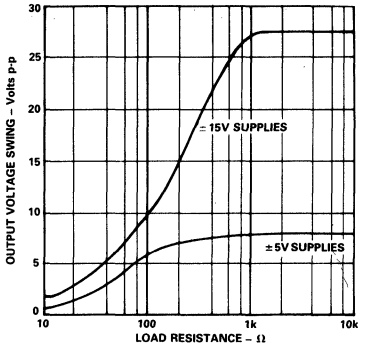


Figure 3. Output Voltage Swing vs. Load Resistance

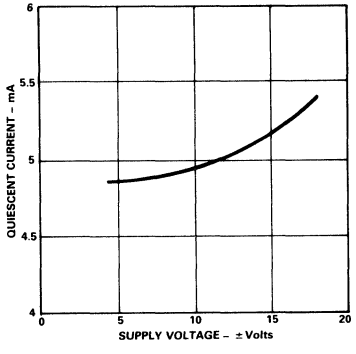


Figure 4. Quiescent Current vs. Supply Voltage

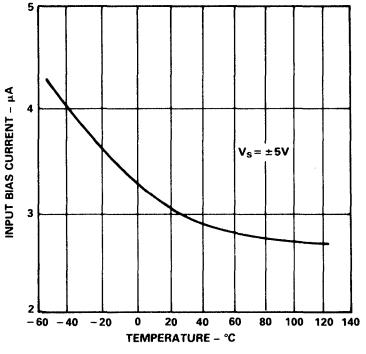


Figure 5. Input Bias Current vs. Temperature

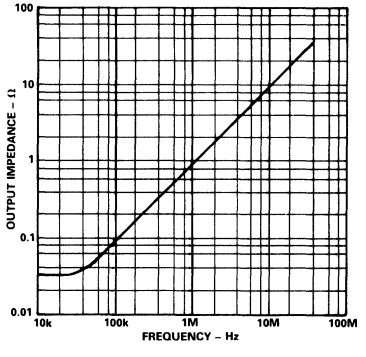


Figure 6. Output Impedance vs. Frequency

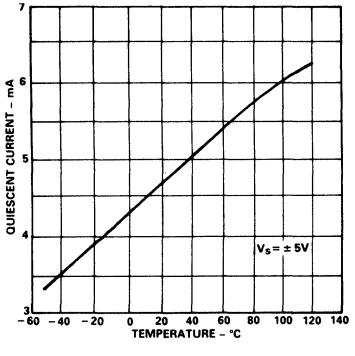


Figure 7. Quiescent Current vs. Temperature

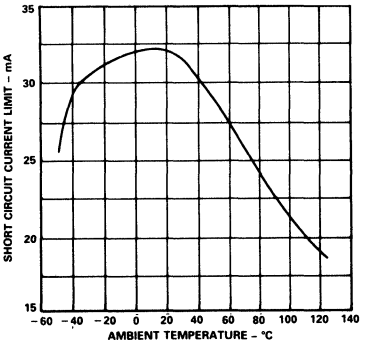


Figure 8. Short-Circuit Current Limit vs. Temperature

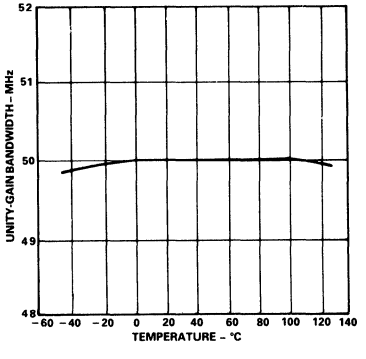


Figure 9. Gain Bandwidth Product vs. Temperature

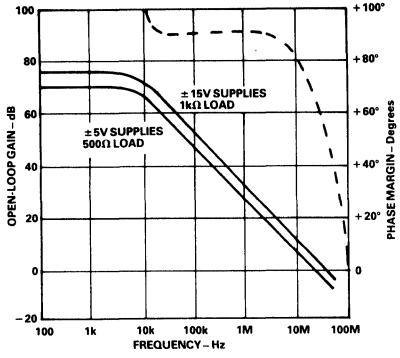


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

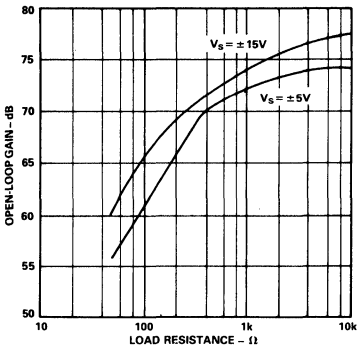


Figure 11. Open-Loop Gain vs. Load Resistance

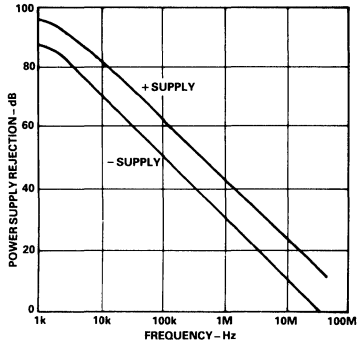


Figure 12. Power Supply Rejection vs. Frequency

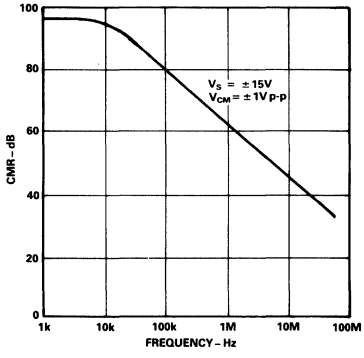


Figure 13. Common-Mode Rejection vs. Frequency

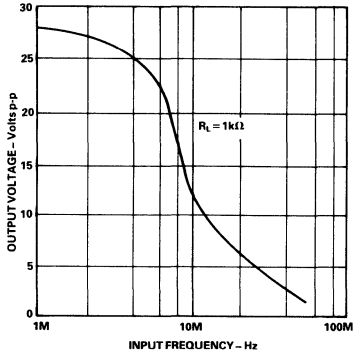


Figure 14. Large Signal Frequency Response

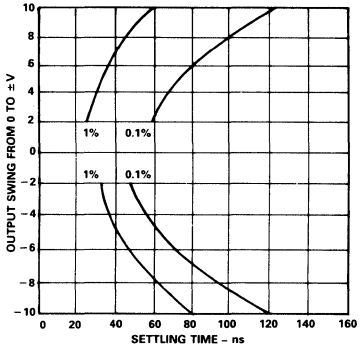


Figure 15. Output Swing and Error vs. Settling Time

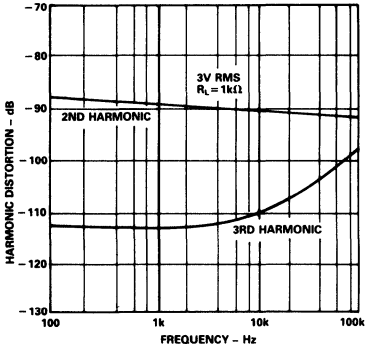


Figure 16. Harmonic Distortion vs. Frequency

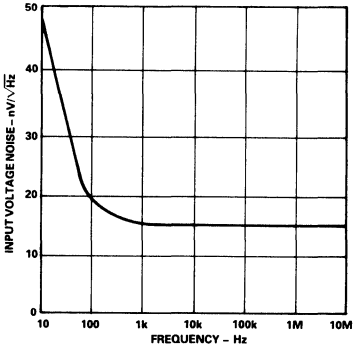


Figure 17. Input Voltage Noise Spectral Density

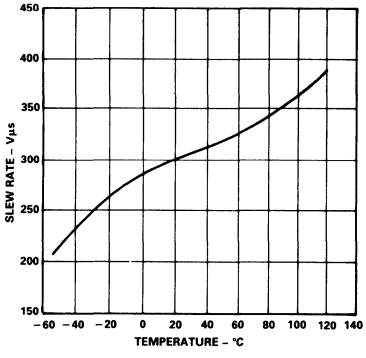


Figure 18. Slew Rate vs. Temperature

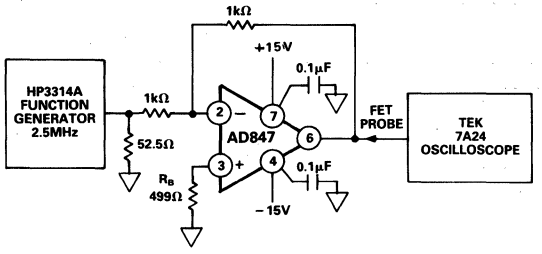


Figure 19. Inverting Amplifier Configuration

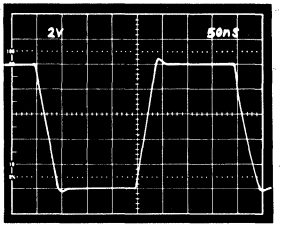


Figure 19a. Inverter Large Signal Pulse Response

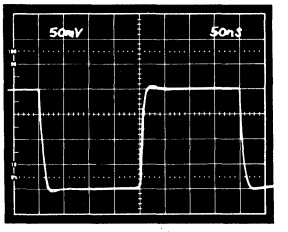


Figure 19b. Inverter Small Signal Pulse Response

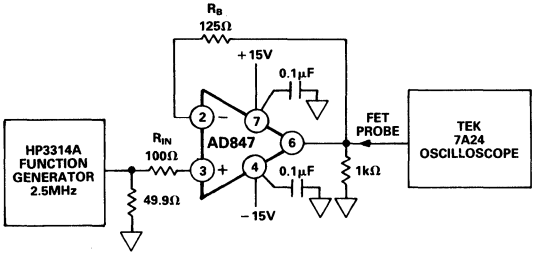


Figure 20. Noninverting Amplifier Configuration

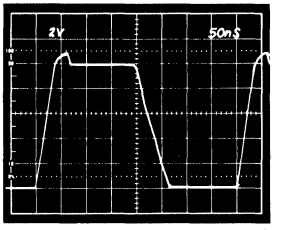


Figure 20a. Noninverting Large Signal Pulse Response

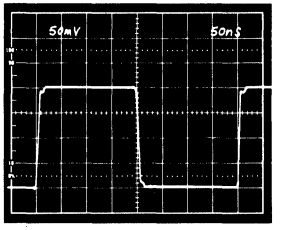


Figure 20b. Noninverting Small Signal Pulse Response

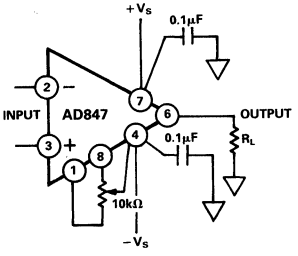


Figure 21. Offset Nulling

OFFSET NULLING

The input offset voltage of the AD847 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

INPUT CONSIDERATIONS

An input resistor (R_{IN} in Figure 20) is recommended in circuits where the input to the AD847 will be subjected to transient or continuous overload voltages exceeding the ±6V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into bases.

For high performance circuits it is recommended that a resistor (R_B in Figures 19 and 20) be used to reduce bias current errors by matching the impedance at each input. The offset voltage error caused by the offset current is more than an order of magnitude less.

THEORY OF OPERATION

The AD847 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which enables the construction of pnp and npn transistors with similar f_{TS} in the 600MHz to 800MHz region. The AD847 circuit (Figure 22) includes an npn input stage followed by fast pnps in the folded cascade intermediate gain stage. The CB pnps are also used in the current amplifying output stage. The internal compensation capacitance that makes the AD847 unity gain stable is provided by the junction capacitances of transistors in the gain stage.

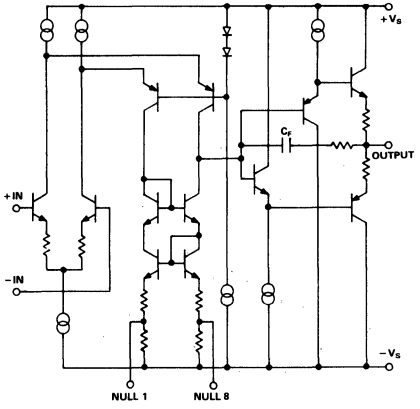


Figure 22. AD847 Simplified Schematic

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case C_F is bootstrapped and does not contribute to the compensation capacitance of the part. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Some fraction of C_F contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is increased, the bandwidth continues to fall, and the amplifier remains stable.

GROUNDING AND BYPASSING

In designing practical circuits with the AD847, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. A large ground plane should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the capacitances at the amplifier summing junction will not limit the amplifier performance. Resistor values of less than 5kΩ are recommended. If a larger resistor must be used, a small (<10pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for the input capacitances and optimize the dynamic performance of the amplifier.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. 0.1μF ceramic disc capacitors are recommended.

VIDEO LINE DRIVER

The AD847 functions very well as a low cost, high speed line driver of either terminated or unterminated cables. Figure 23 shows the AD847 driving a doubly terminated cable in a follower configuration.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. While operating off ±5V supplies, the AD847 maintains a typical slew rate of 200V/μs, which means it can drive a ±1V, 30MHz signal on the terminated cable.

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD847 ouput and the cable in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a "cleaner" signal, although it requires that the op amp supply ±2V to the output in order to achieve a ±1V swing at the line.

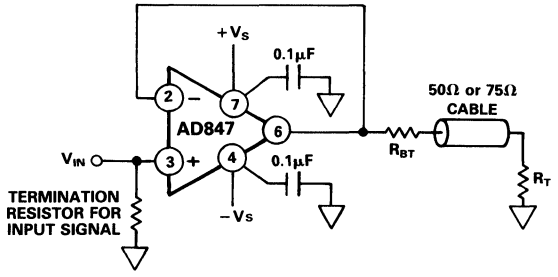


Figure 23. Video Line Driver

Often termination is not used, either because signal integrity requirements are low or because too many high frequency signals returned to ground contaminate the ground plane. Unterminated cables appear as capacitive loads. Since the AD847 is stable into any capacitive load as a follower, it will not oscillate if the cable is not terminated; however pulse integrity will be degraded. Figure 24 shows the AD847 driving 100pF and 1000pF loads.

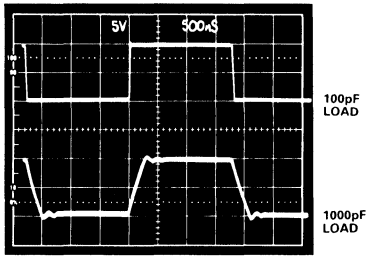


Figure 24. AD847 Driving a Capacitive Load

FLASH ADC INPUT BUFFER

The 35MHz unity gain bandwidth of the AD847 when operated with ±5V supplies makes it an excellent choice for buffering the input of high speed flash A/D converters, such as the AD9048.

Figure 25 shows the AD847 as a unity inverter for the input to the AD9048.

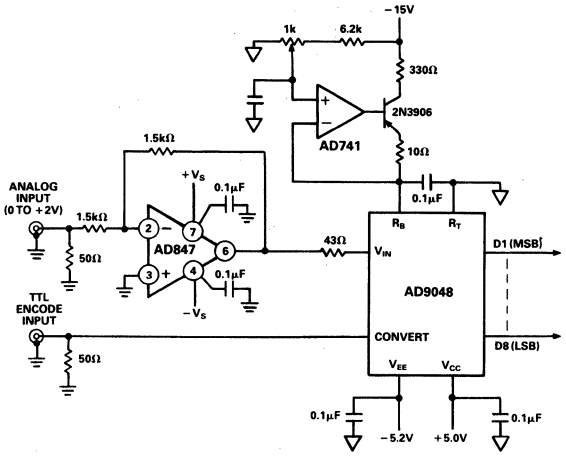


Figure 25. Flash ADC Input Buffer

HIGH SPEED DAC BUFFER

The wide bandwidth and fast settling time of the AD847 makes it a very good output buffer for high speed current-output D/A converters like the ADDAC-08. Figure 27 shows the ADDAC-08 with the AD847 as the current to voltage converter. In this unipolar configuration the output swing ranges from 0.00V to +9.96V.

Figure 26 shows the full scale settling time of this circuit when the digital codes are changed from all 1s to all 0s. For the +9.96V to 0.00V output change shown 1LSB = 40mV the overall settling time of the circuit is 140ns.

The variable feedback capacitor, C_F, is used to optimize the settling time of the circuit by compensating for the additional pole created by R_F and the stray capacitance at the inverting input pin. A −10.0V to +9.92V bipolar output is achievable by connecting a 10kΩ resistor between the AD587 output and the AD847 input and replacing R_F with a 10kΩ resistor.

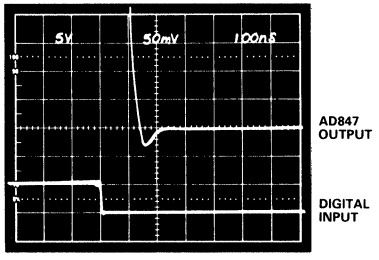


Figure 26. Settling Time for ADDAC-08 and AD847 Combination

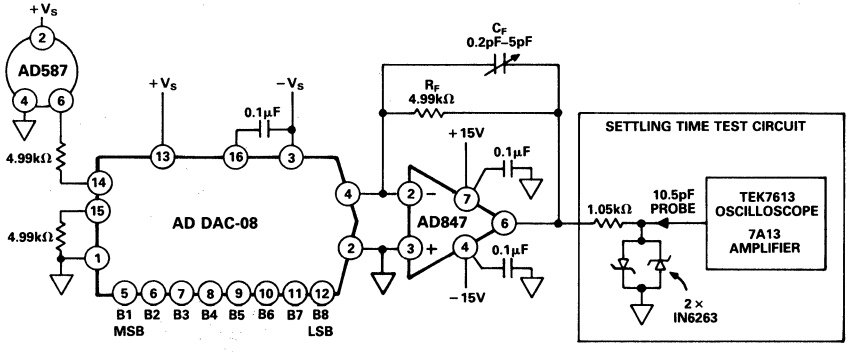


Figure 27. High Speed DAC Buffer

High Speed, Low Power Monolithic Op Amps

AD848/AD849

FEATURES
725MHz Gain Bandwidth – AD849
175MHz Gain Bandwidth – AD848
4.8mA Supply Current
300V/μs Slew Rate
80ns Settling Time to 0.1% for a 10V Step – AD849
Differential Gain: AD848 = 0.07%, AD849 = 0.08%
Differential Phase: AD848 = 0.08°, AD849 = 0.04°
Drives Capacitive Loads

DC PERFORMANCE
3nV/√Hz Input Voltage Noise – AD849
85V/mV Open Loop Gain into a 1kΩ Load – AD849
1mV max Input Offset Voltage
Performance Specified for ±5V and ±15V Operation
Available in Plastic, Hermetic Cerdip and Small Outline Packages. Chips and MIL-STD-883B Parts Available. Tape and Reel Also Available

APPLICATIONS
Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video and R_F Amplification
Signal Generators

PRODUCT DESCRIPTION

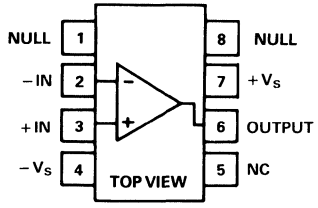
The AD848 and AD849 are high speed, low power monolithic operational amplifiers. The AD848 is internally compensated so that it is stable for closed loop gains of 5 or greater. The AD849 is fully decompensated and is stable at gains greater than 24. The AD848 and AD849 achieve their combination of fast ac and good dc performance by utilizing Analog Devices' junction isolated complementary bipolar (CB) process. This process enables these op amps to achieve their high speed while only requiring 4.8mA of current from the power supplies.

The AD848 and AD849 are members of Analog Devices' family of high speed op amps. This family includes, among others, the AD847 which is unity gain stable, with a gain bandwidth of 50MHz. For more demanding applications, the AD840, AD841 and AD842 offer even greater precision and greater output current drive.

The AD848 and AD849 have good dc performance. When operating with ±5V supplies, they offer open loop gains of 13V/mV (AD848 with a 500Ω load) and low input offset voltage of 1mV maximum. Common-mode rejection is a minimum of 92dB. Output voltage swing is ±3V even into loads as low as 150Ω.

AD847/AD847
CONNECTION DIAGRAM

Plastic (N), Small Outline (R) and Cerdip (Q) Packages



NC = NO CONNECT

APPLICATIONS HIGHLIGHTS

1. The high slew rate and fast settling time of the AD848 and AD849 make them ideal for video instrumentation circuitry, low noise preamps and line drivers.
2. In order to meet the needs of both video and data acquisition applications, the AD848 and AD849 are optimized and tested for ±5V and ±15V power supply operation.
3. Both amplifiers offer full power bandwidth greater than 20MHz (for 2V p-p with ±5V supplies).
4. The AD848 and AD849 remain stable when driving any capacitive load.
5. Laser wafer trimming reduces the input offset voltage to 1mV maximum on all grades, thus eliminating the need for external offset nulling in many applications.
6. The AD848 is an enhanced replacement for the LM6164 series and can function as a pin-for-pin replacement for many high speed amplifiers such as the HA2520/2/5 and EL2020 in applications where the gain is 5 or greater.

SPECIFICATIONS (@T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD848J Min	AD848J Typ	AD848J Max	AD848A/S Min	AD848A/S Typ	AD848A/S Max	Units
INPUT OFFSET VOLTAGE[1]		±5V		0.2	**1**		0.2	**1**	mV
		±15V		0.5	**2.3**		0.5	**2.3**	mV
	T_{min} to T_{max}	±5V			1.5			**2**	mV
		±15V			3.0			**3.5**	mV
Offset Drift		±5V, ±15V		7			7		µV/°C
INPUT BIAS CURRENT		±5V, ±15V		3.3	**6.6**		3.3	**6.6/5**	µA
	T_{min} to T_{max}	±5V, ±15V			7.2			**7.5**	µA
INPUT OFFSET CURRENT		±5V, ±15V		50	**300**		50	**300**	nA
	T_{min} to T_{max}	±5V, ±15V			400			**400**	nA
Offset Current Drift		±5V, ±15V		0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5V	±5V							
	R_{LOAD} = 500Ω		**9**	13		**9**	13		V/mV
	T_{min} to T_{max}		7			**7/5**			V/mV
	R_{LOAD} = 150Ω			8			8		V/mV
	V_{OUT} = ±10V	±15V							
	R_{LOAD} = 1kΩ		**12**	20		**12**	20		V/mV
	T_{min} to T_{max}		8			**8/6**			V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth	A_{VCL} ≥ 5	±5V		125			125		MHz
		±15V		175			175		MHz
Full Power Bandwidth[2]	V_O = 2V p-p,								
	R_L = 500Ω	±5V		24			24		MHz
	V_O = 20V p-p,								
	R_L = 1kΩ	±15V		4.7			4.7		MHz
Slew Rate		±5V		200			200		V/µs
	R_{LOAD} = 1kΩ	±15V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5V to +2.5V	±5V		65			65		ns
	10V Step, A_V = −4	±15V		100			100		ns
Phase Margin	C_{LOAD} = 10pF	±15V							
	R_{LOAD} = 1kΩ			60			60		Degrees
DIFFERENTIAL GAIN	f = 4.4MHz	±15V		0.07			0.07		%
DIFFERENTIAL PHASE	f = 4.4MHz	±15V		0.08			0.08		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5V	±5V	**92**	105		**92**	105		dB
	V_{CM} = ±12V	±15V	**92**	105		**92**	105		dB
	T_{min} to T_{max}		88			**88**			dB
POWER SUPPLY REJECTION	V_S = ±4.5V to ±18V		**85**	98		**85**	98		dB
	T_{min} to T_{max}		80			**80**			dB
INPUT VOLTAGE NOISE	f = 10kHz	±15V		5			5		nV/√Hz
INPUT CURRENT NOISE	f = 10kHz	±15V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500Ω	±5V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150Ω	±5V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 50Ω	±5V		1.4			1.4		±V
	R_{LOAD} = 1kΩ	±15V	**12**			**12**			±V
	R_{LOAD} = 500Ω	±15V	**10**			**10**			±V
SHORT CIRCUIT CURRENT		±15V		32			32		mA
INPUT RESISTANCE				70			70		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5V		4.8	**6.0**		4.8	**6.0**	mA
	T_{min} to T_{max}				7.4			**7.4/8.3**	mA
		±15V		5.1	**6.8**		5.1	**6.8**	mA
	T_{min} to T_{max}				8.0			**8.0/9.0**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = slew rate/2π V_{PEAK}. Refer to Figure 1.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. All others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

Model	Conditions	V_S	AD849J Min	AD849J Typ	AD849J Max	AD849A/S Min	AD849A/S Typ	AD849A/S Max	Units
INPUT OFFSET VOLTAGE[1]		±5V		0.3	**1**		0.1	**0.75**	mV
		±15V		0.3	**1**		0.1	**0.75**	mV
	T_{min} to T_{max}	±5V			1.3			**1.0**	mV
		±15V			1.3			**1.0**	mV
Offset Drift		±5V, ±15V		2			2		µV/°C
INPUT BIAS CURRENT		±5V, ±15V		3.3	**6.6**		3.3	**6.6/5**	µA
	T_{min} to T_{max}	±5V, ±15V			7.2			**7.5**	µA
INPUT OFFSET CURRENT		±5V, ±15V		50	**300**		50	**300**	nA
	T_{min} to T_{max}	±5V, ±15V			400			**400**	nA
Offset Current Drift		±5V, ±15V		0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5V	±5V							
	R_{LOAD} = 500Ω		**30**	50		**30**	50		V/mV
	T_{min} to T_{max}		20			**20/15**			V/mV
	R_{LOAD} = 150Ω			32			32		V/mV
	V_{OUT} = ±10V	±15V							
	R_{LOAD} = 1kΩ		**45**	85		**45**	85		V/mV
	T_{min} to T_{max}		30			**30/25**			V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth	A_{VCL} ≥ 25	±5V		520			520		MHz
		±15V		725			725		MHz
Full Power Bandwidth[2]	V_O = 2V p-p,								
	R_L = 500Ω	±5V		20			20		MHz
	V_O = 20V p-p,								
	R_L = 1kΩ	±15V		4.7			4.7		MHz
Slew Rate		±5V		200			200		V/µs
	R_{LOAD} = 1kΩ	±15V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5V to +2.5V	±5V		65			65		ns
	10V Step, A_V = −24	±15V		80			80		ns
Phase Margin	C_{LOAD} = 10pF	±15V							
	R_{LOAD} = 1kΩ			60			60		Degrees
DIFFERENTIAL GAIN	f = 4.4MHz	±15V		0.08			0.08		%
DIFFERENTIAL PHASE	f = 4.4MHz	±15V		0.04			0.04		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5V	±5V	**100**	115		**100**	115		dB
	V_{CM} = ±12V	±15V	**100**	115		**100**	115		dB
	T_{min} to T_{max}		96			**96**			dB
POWER SUPPLY REJECTION	V_S = ±4.5V to ±18V		**98**	120		**98**	120		dB
	T_{min} to T_{max}		94			**94**			dB
INPUT VOLTAGE NOISE	f = 10kHz	±15V		3			3		nV/√Hz
INPUT CURRENT NOISE	f = 10kHz	±15V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500Ω	±5V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150Ω	±5V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 50Ω	±5V		1.4			1.4		±V
	R_{LOAD} = 1kΩ	±15V	**12**			**12**			±V
	R_{LOAD} = 500Ω	±15V	**10**			**10**			±V
SHORT CIRCUIT CURRENT		±15V		32			32		mA
INPUT RESISTANCE				25			25		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5V		4.8	**6.0**		4.8	**6.0**	mA
	T_{min} to T_{max}				7.4			**7.4/8.3**	mA
		±15V		5.1	**6.8**		5.1	**6.8**	mA
	T_{min} to T_{max}				8.0			**8.0/9.0**	mA

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = slew rate/2π V_{PEAK}. Refer to Figure 2.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. All others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

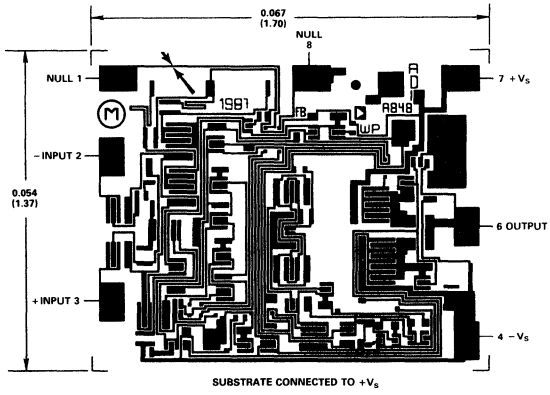
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.1 Watts
Small Outline (R) . . . . . 0.9 Watts
Cerdip (Q) . . . . . 1.1 Watts
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . +6V
Storage Temperature Range Q . . . . . −65°C to +150°C
N, R . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP Package: $\theta_{JA} = 110°C$ Watt.
Cerdip Package: $\theta_{JA} = 110°C$ Watt.
Small Outline Package: $\theta_{JA} = 155°C$ Watt.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions. (AD848 and AD849 are identical except for the part number in the upper right.)
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Gain Bandwidth MHz	Min Stable Gain	Max Offset Voltage mV	Temperature Range – °C	Package Option[1, 2]
AD848JN	175	5	1	0 to +70	Plastic (N-8)
AD848JR	175	5	1	0 to +70	SOIC (R-8)
AD848AQ	175	5	1	−40 to +85	Cerdip (Q-8)
AD848SQ	175	5	1	−55 to +125	Cerdip (Q-8)
AD848SQ/883B	175	5	1	−55 to +125	Cerdip (Q-8)
AD849JN	725	25	1	0 to +70	Plastic (N-8)
AD849JR	725	25	1	0 to +70	SOIC (R-8)
AD849AQ	725	25	0.75	−40 to +85	Cerdip (Q-8)
AD849SQ	725	25	0.75	−55 to +125	Cerdip (Q-8)
AD849SQ/883B	725	25	0.75	−55 to +125	Cerdip (Q-8)
AD847J/A/S	50	1	1	See AD847 Data Sheet	

NOTE
[1]Plastic SOIC (R) available in tape and reel. AD848 available in S grade chips. AD849 available in J and S grade chips.
[2]See Section 20 for package outline information.

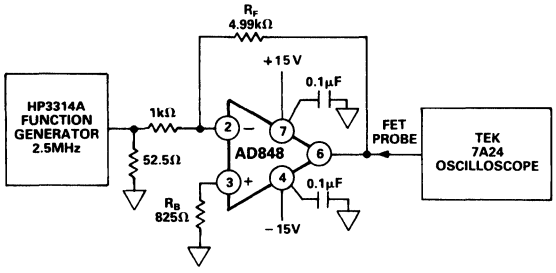


Figure 1. AD848 Inverting Amplifier Configuration

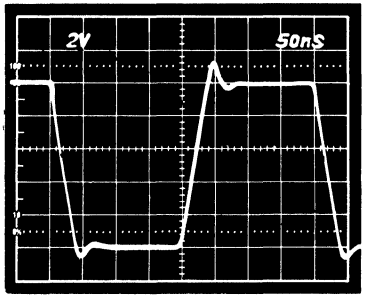


Figure 1a. AD848 Large Signal Pulse Response

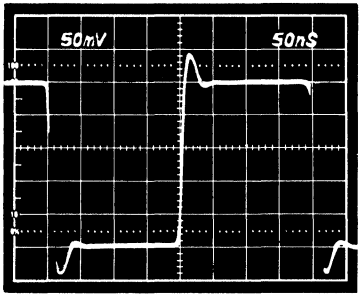


Figure 1b. AD848 Small Signal Pulse Response

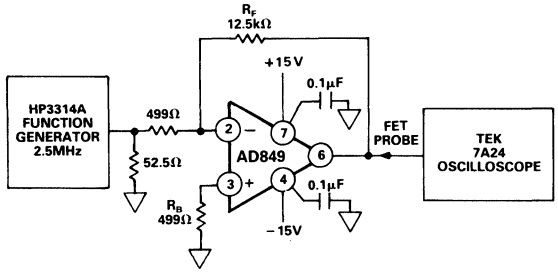


Figure 2. AD849 Inverting Amplifier Configuration

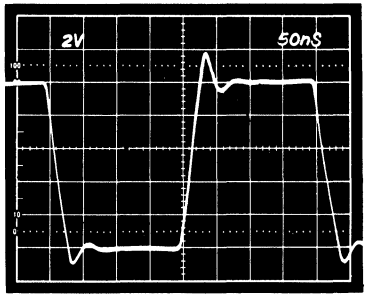


Figure 2a. AD849 Large Signal Pulse Response

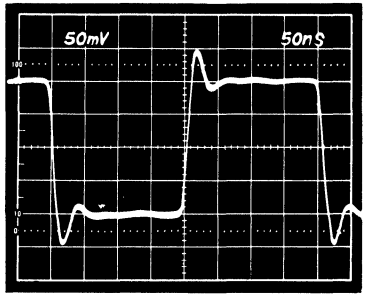


Figure 2b. AD849 Small Signal Pulse Response

OFFSET NULLING

The input voltage of the AD848 and AD849 are very low for high speed op amps, but if additional nulling is required, the circuit shown in Figure 3 can be used.

For high performance circuits it is recommended that a resistor (R_B in Figures 1 and 2) be used to reduce bias current errors by matching the impedance at each input. The offset voltage error caused by the input currents is decreased by more than an order of magnitude.

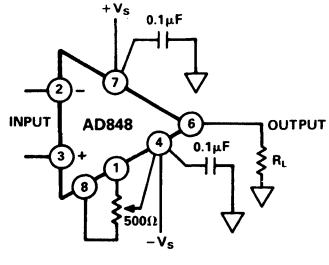


Figure 3. Offset Nulling

Typical Characteristics (@ +25°C and $V_S = \pm 15V$, unless otherwise noted)

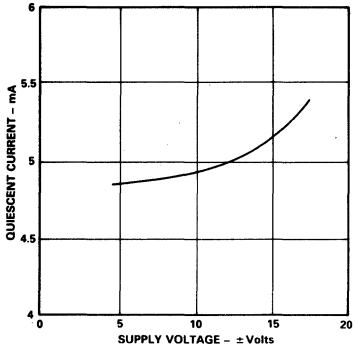


Figure 4. Quiescent Current vs. Supply Voltage (AD848 and AD849)

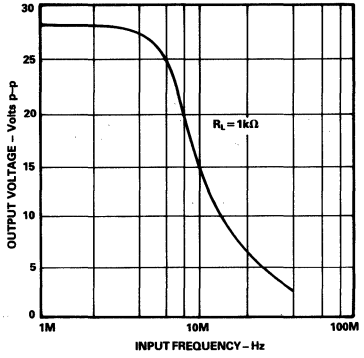


Figure 5. Large Signal Frequency Response (AD848 and AD849)

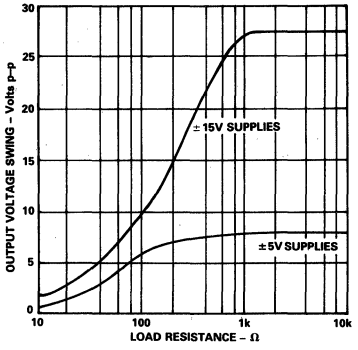


Figure 6. Output Voltage Swing vs. Load Resistance (AD848 and AD849)

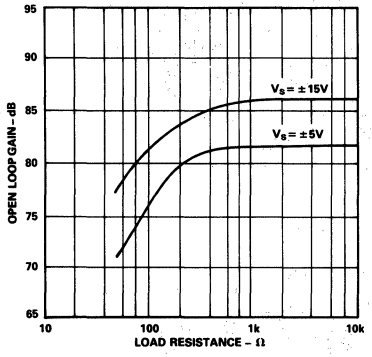


Figure 7. Open Loop Gain vs. Load Resistance (AD848)

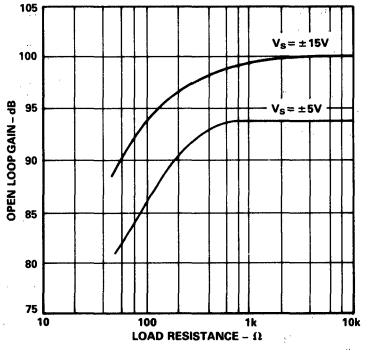


Figure 8. Open Loop Gain vs. Load Resistance (AD849)

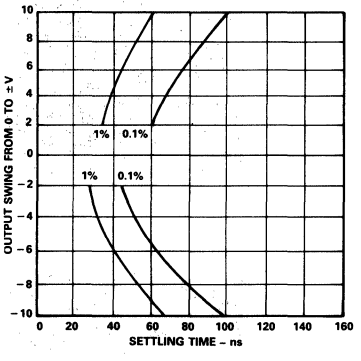


Figure 9. Output Swing and Error vs. Settling Time (AD848)

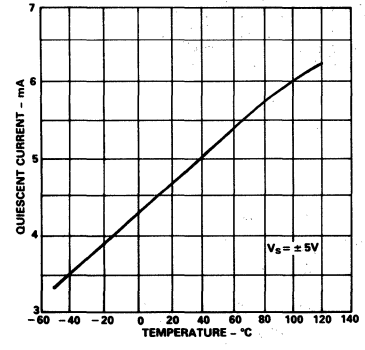


Figure 10. Quiescent Current vs. Temperature (AD848 and AD849)

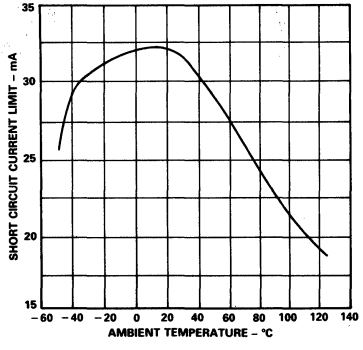


Figure 11. Short Circuit Current Limit vs. Temperature (AD848 and AD849)

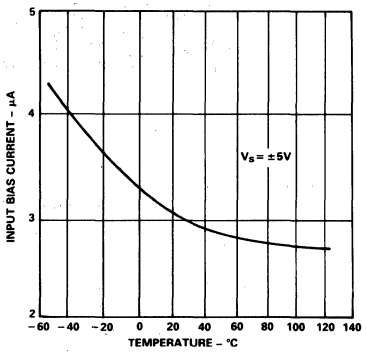


Figure 12. Input Bias Current vs. Temperature (AD848 and AD849)

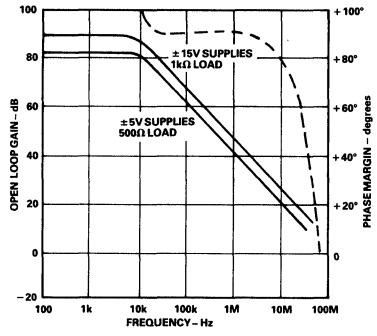


Figure 13. Open Loop Gain and Phase Margin vs. Frequency (AD848)

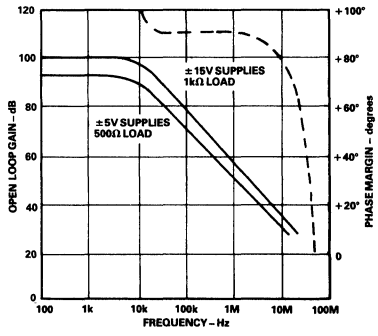


Figure 14. Open Loop Gain and Phase Margin vs. Frequency (AD849)

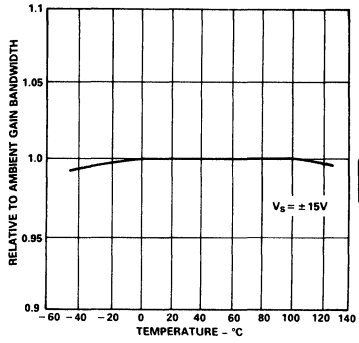


Figure 15. Normalized Gain Bandwidth Product vs. Temperature (AD848 and AD849)

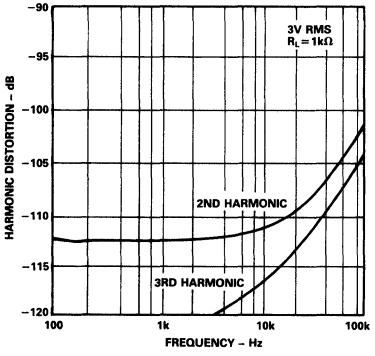


Figure 16. Harmonic Distortion vs. Frequency (AD848)

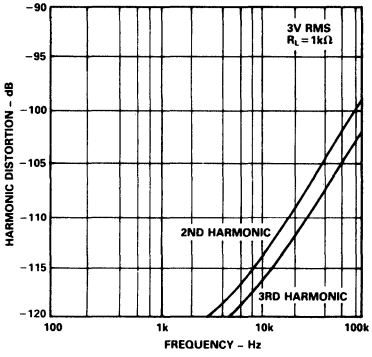


Figure 17. Harmonic Distortion vs. Frequency (AD849)

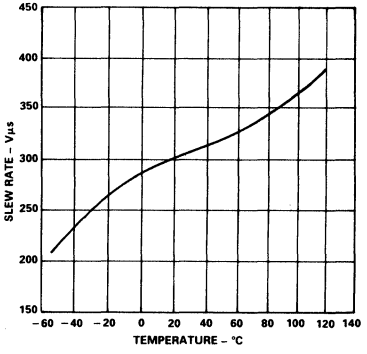


Figure 18. Slew Rate vs. Temperature (AD848 and AD849)

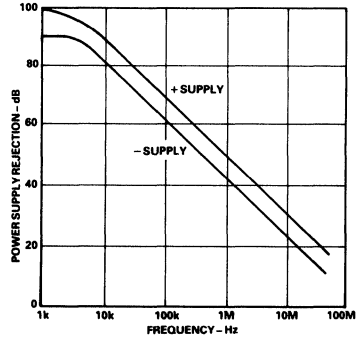


Figure 19. Power Supply Rejection vs. Frequency (AD848)

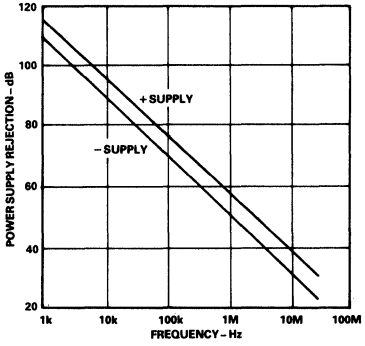


Figure 20. Power Supply Rejection vs. Frequency (AD849)

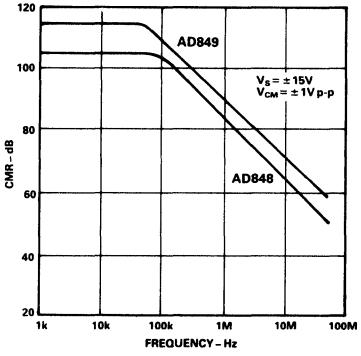


Figure 21. Common-Mode Rejection vs. Frequency

Applications

GROUNDING AND BYPASSING

In designing practical circuits with the AD848 or AD849, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. A large ground plane should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the capacitances at the amplifier summing junction will not limit the amplifier performance. Resistor values of less than 5kΩ are recommended. If a larger resistor must be used, a small (<10pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for the input capacitances and optimize the dynamic performance of the amplifier.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. 0.1μF ceramic disc capacitors are recommended.

VIDEO LINE DRIVER

The AD848 functions very well as a low cost, high speed line driver of either terminated or unterminated cables. Figure 22 shows the AD848 driving a doubly terminated cable.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. While operating off ±5V supplies, the AD848 maintains a typical slew rate of 200V/μs, which means it can drive a ±1V, 24MHz signal on the terminated cable.

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD848 output and the cable in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a "cleaner" signal, although it requires that the op amp supply ±2V to the output in order to achieve a ±1V swing at the line.

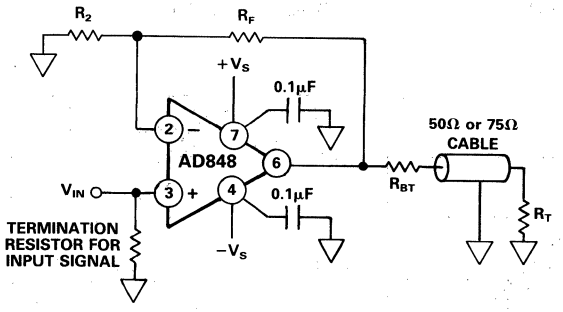


Figure 22. Video Line Driver

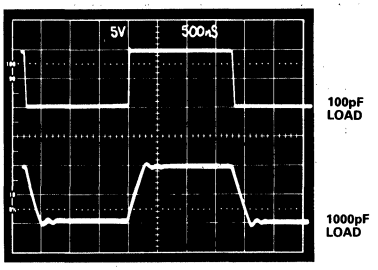


Figure 23. AD848 Driving a Capacitive Load

Often termination is not used, either because signal integrity requirements are low or because too many high frequency signals returned to ground contaminate the ground plane. Unterminated cables appear as capacitive loads. Since the AD848 and AD849 are stable into any capacitive load, the op amp will not oscillate if the cable is not terminated; however pulse integrity will be degraded. Figure 23 shows the AD848 driving both 100pF and 1000pF loads.

LOW NOISE PRE-AMP

The input voltage noise spectral densities of the AD848 and the AD849 are shown in Figure 24. The low wideband noise and high gain bandwidths of these devices makes them well suited as pre-amps for high frequency systems.

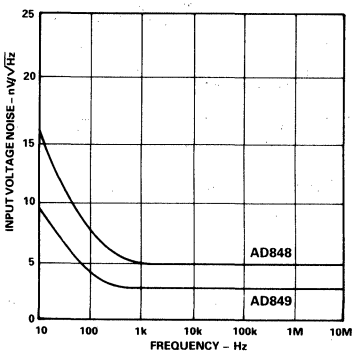


Figure 24. Input Voltage Noise Spectral Density

Input voltage noise will be the dominant source of noise at the output in most applications. Other noise sources can be minimized by keeping resistor values as small as possible.

ANALOG DEVICES

Ultrahigh Frequency Operational Amplifier

AD5539

FEATURES

Improved Replacement for Signetics SE/NE5539

AC PERFORMANCE

- **Gain Bandwidth Product: 1.4 GHz typ**
- **Unity Gain Bandwidth: 220 MHz typ**
- **High Slew Rate: 600 V/μs typ**
- **Full Power Response: 82 MHz typ**
- **Open-Loop Gain: 47 dB min, 52 dB typ**

DC PERFORMANCE

- **All Guaranteed DC Specifications Are 100% Tested For Each Device Over Its Full Temperature Range – For All Grades and Packages**
- **V_{OS}: 5 mV max Over Full Temperature Range (AD5539J)**
- **I_B: 20 μA max (AD5539J)**
- **CMRR: 70 dB min, 85 dB typ**
- **PSRR: 100 μV/V typ**
- **MIL-STD-883B Parts Available**

PRODUCT DESCRIPTION

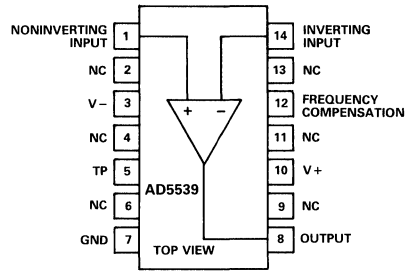
The AD5539 is an ultrahigh frequency operational amplifier designed specifically for use in video circuits and RF amplifiers. Requiring no external compensation for gains greater than 5, it may be operated at lower gains with the addition of external compensation.

As a superior replacement for the Signetics NE/SE5539, each AD5539 is 100% dc tested to meet all of its guaranteed dc specifications over the full temperature range of the device.

The high slew rate and wide bandwidth of the AD5539 provide low cost solutions to many otherwise complex and expensive high frequency circuit design problems.

The AD5539 is available specified to operate over either the commercial (AD5539JN/JQ) or military (AD5539SQ) temperature range. The commercial grade is available either in 14-pin plastic or cerdip packages. The military version is supplied in the cerdip package. Chip versions are also available.

AD5539 CONNECTION DIAGRAM
Plastic DIP (N) Package
or Cerdip (Q) Package



PRODUCT HIGHLIGHTS

1. All guaranteed dc specifications are 100% tested.
2. The AD5539 drives 50 Ω and 75 Ω loads directly.
3. Input voltage noise is less than 4 $nV\sqrt{Hz}$.
4. Low cost RF and video speed performance.
5. ±2 volt output range into a 150 Ω load.
6. Low cost.
7. Chips available.

SPECIFICATIONS (@ +25°C and V_S = ±8 V dc, unless otherwise noted)

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
INPUT OFFSET VOLTAGE							
Initial Offset[1]		2	5		2	3	mV
T_{min} to T_{max}			6			5	mV
INPUT OFFSET CURRENT							
Initial Offset[2]		0.1	2		0.1	1	μA
T_{min} to T_{max}			5			3	μA
INPUT BIAS CURRENT							
Initial[2]							
V_{CM} = 0		6	20		6	13	μA
Either Input							
T_{min} to T_{max}			40			25	μA
FREQUENCY RESPONSE							
R_L = 150 Ω[3]							
Small Signal Bandwidth		220			220		MHz
A_{CL} = 2[4]							
Gain Bandwidth Product		1400			1400		MHz
A_{CL} = 26 dB							
Full Power Response							
A_{CL} = 2[4]		68			68		MHz
A_{CL} = 7		82			82		MHz
A_{CL} = 20		65			65		MHz
Settling Time (1%)		12			12		ns
Slew Rate		600			600		V/μs
Large Signal Propagation Delay		4			4		ns
Total Harmonic Distortion							
R_L = ∞		0.010			0.010		%
R_L = 100 Ω[3]		0.016			0.016		%
V_{OUT} = 2 V p-p							
A_{CL} = 7, f = 1 kHz							
INPUT IMPEDANCE		100			100		kΩ
OUTPUT IMPEDANCE (f <10 MHz)		2			2		Ω
INPUT VOLTAGE RANGE							
Differential[5]							
(Max Nondestructive)		250			250		mV
Common Mode Voltage							
(Max Nondestructive)		2.5			2.5		V
Common Mode Rejection Ratio							
ΔV_{CM} = 1.7 V							
R_S = 100 Ω	70	85		70	85		dB
T_{min} to T_{max}	60			60			dB
INPUT VOLTAGE NOISE							
Wideband RMS Noise (RTI)		5			5		μV
BW = 5 MHz; R_S = 50 Ω							
Spot Noise		4			4		$nV\sqrt{Hz}$
F = 1 kHz; R_S = 50 Ω							
OPEN-LOOP GAIN							
V_O = +2.3 V, −1.7 V							
R_L = 150 Ω[3]	47	52	58	47	52	58	dB
R_L = 2 kΩ	47		58	48		57	dB
T_{min} to T_{max} $-R_L$ = 2 kΩ	43		63	46		60	dB

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
OUTPUT CHARACTERISTICS							
Positive Output Swing							
R_L = 150 Ω[3]	+2.3	+2.8		+2.3	+2.8		V
R_L = 2 kΩ	+2.3	+3.3		+2.5	+3.3		V
T_{min} to T_{max} with							
R_L = 2 kΩ	+2.3			+2.3			V
Negative Output Swing							
R_L = 150 Ω[3]		−2.2	**−1.7**		−2.2	**−1.7**	V
R_L = 2 kΩ		−2.9	**−1.7**		−2.9	**−2.0**	V
T_{min} to T_{max} with							
R_L = 2 kΩ			**−1.5**			**−1.5**	V
POWER SUPPLY (No Load, No Resistor to $-V_S$)							
Rated Performance		±8			±8		V
Operating Range	**±4.5**		**±10**	**±4.5**		**±10**	V
Quiescent Current							
Initial I_{CC}+		14	**18**		14	**17**	mA
T_{min} to T_{max}			**20**			**18**	mA
Initial I_{CC}−		11	**15**		11	**14**	mA
T_{min} to T_{max}			**17**			**15**	mA
PSRR							
Initial		100	**1000**		100	**1000**	μV/V
T_{min} to T_{max}			**2000**			**2000**	μV/V
TEMPERATURE RANGE							
Operating,							
Rated Performance							
Commercial (0 to +70°C)	AD5539JN, AD5539JQ						
Military (−55°C to +125°C)				AD5539SQ			
PACKAGE OPTIONS[6]							
Plastic (N-14)	AD5539JN						
Cerdip (Q-14)	AD5539JQ			AD5539SQ			
J and S Grade Chips Available							

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.
[3]R_X = 470 Ω to $-V_S$.
[4]Externally compensated.
[5]Defined as voltage between inputs, such that neither exceeds +2.5 V, −5.0 V from ground.
[6]See Section 20 for package outline information.

Specifications subject to change without notice.

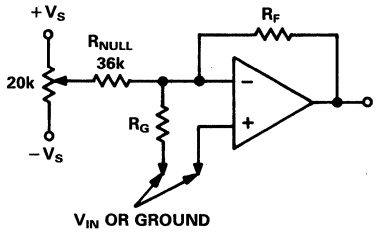
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±10 V
Internal Power Dissipation . . . . . 550 mW
Input Voltage . . . . . +2.5 V, −5.0 V
Differential Input Voltage . . . . . 0.25 V
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Operating Temperature Range
AD5539JN . . . . . 0 to +70°C
AD5539JQ . . . . . 0 to +70°C
AD5539SQ . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 Seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OFFSET NULL CONFIGURATION



$$\text{OUTPUT NULL RANGE} \cong +V_S\left(\frac{R_F}{R_{NULL}}\right) \text{ TO } -V_S\left(\frac{R_F}{R_{NULL}}\right)$$

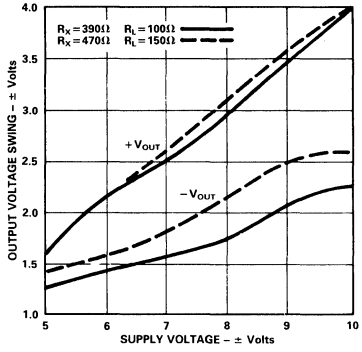


Figure 1. Output Voltage Swing vs. Supply Voltage

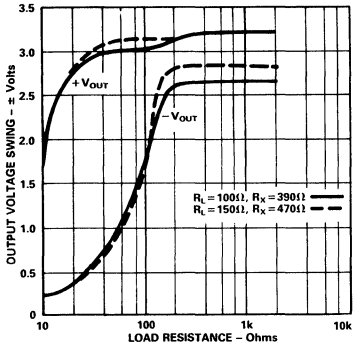


Figure 2. Output Voltage Swing vs. Load Resistance

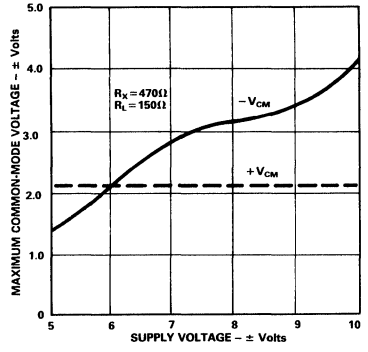


Figure 3. Maximum Common-Mode Voltage vs. Supply Voltage

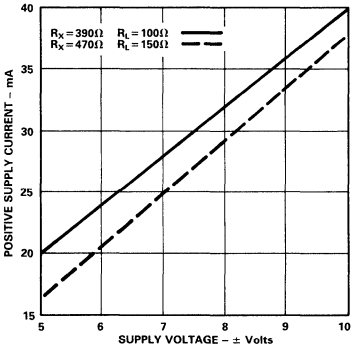


Figure 4. Positive Supply Current vs. Supply Voltage

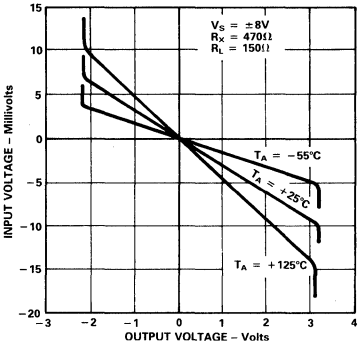


Figure 5. Input Voltage vs. Output Voltage for Various Temperatures

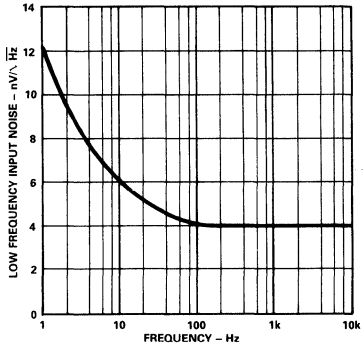


Figure 6. Low Frequency Input Noise vs. Frequency

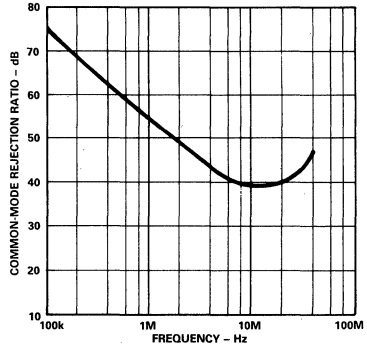


Figure 7. Common-Mode Rejection Ratio vs. Frequency

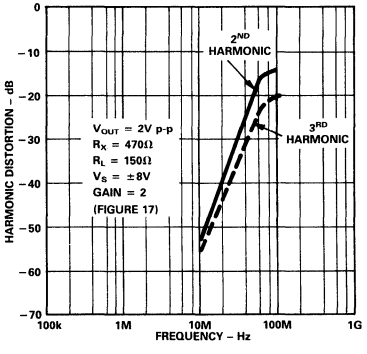


Figure 8. Harmonic Distortion vs. Frequency – Low Gain

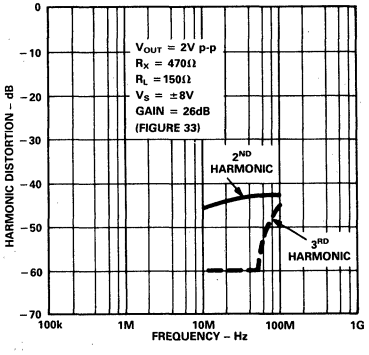


Figure 9. Harmonic Distortion vs. Frequency – High Gain

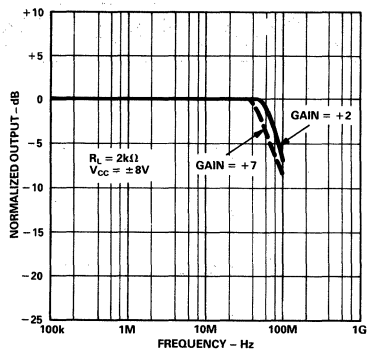


Figure 10. Full Power Response

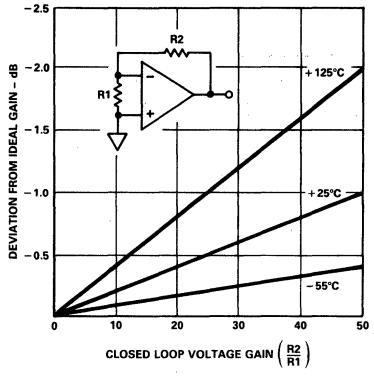


Figure 11. Deviation from Ideal Gain vs. Closed-Loop Voltage Gain

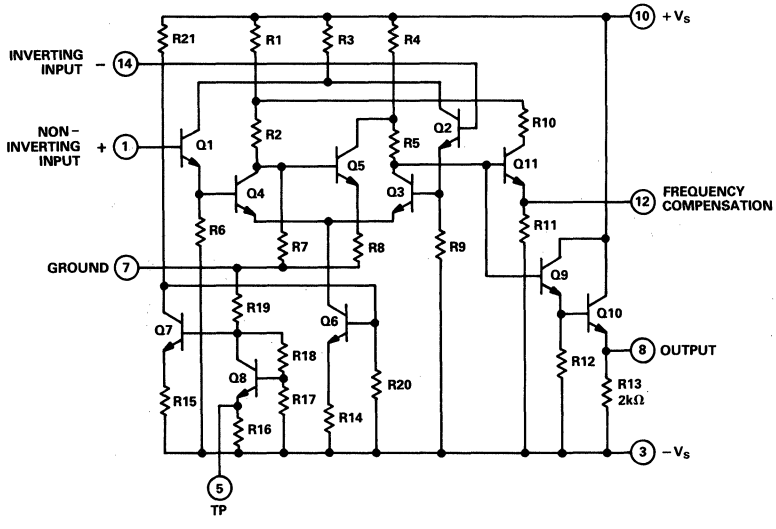


Figure 12. AD5539 Circuit

FUNCTIONAL DESCRIPTION

The AD5539 is a two-stage, very high frequency amplifier. Darlington input transistors Q1, Q4 –Q2, Q3 form the first stage — a differential gain amplifier with a voltage gain of approximately 50. The second stage, Q5, is a single-ended amplifier whose input is derived from one phase of the differential amplifier output; the other phase of the differential output is then summed with the output of Q5. The all NPN design of the AD5539 is configured such that the emitter of Q5 is returned, via a small resistor to ground; this eliminates the need for separate level shifting circuitry.

The output stage, consisting of transistors Q9 and Q10, is a Darlington voltage follower with a resistive pull-down. The bias section, consisting of transistors Q6, Q7 and Q8, provides a stable emitter current for the input section, compensating for temperature and power supply variations.

SOME GENERAL PRINCIPLES OF HIGH FREQUENCY CIRCUIT DESIGN

In designing practical circuits with the AD5539, the user must remember that whenever very high frequencies are involved, some special precautions are in order. All real-world applications circuits must be built using proper RF techniques: the use of short interconnect leads, adequate shielding, groundplanes, and very low profile IC sockets. In addition, very careful bypassing of power supply leads is a must.

Low-impedance transmission line is frequently used to carry signals at RF frequencies: 50 Ω line for telecommunications purposes and 75 Ω for video applications. The AD5539 offers a relatively low output impedance; therefore, some consideration must be given to impedance matching. A common matching technique involves simply placing a resistor in series with the amplifier output that is equal to the characteristic impedance of the transmission line. This provides a good match (although at a loss of 6 dB), adequate for many applications.

All of the circuits here were built and tested in a 50 Ω system. Care should be taken in adapting these circuits for each particular use. Any system which has been properly matched and terminated in its characteristic impedance should have the same small signal frequency response as those shown in this data sheet.

APPLYING THE AD5539

The AD5539 is stable for closed-loop gains of 4 or more as an inverter and at (noise) gains of 5 or greater as a voltage follower. This means that whenever the AD5539 is operated at noise gains below 5, external frequency compensation must be used to insure stable operation.

The following sections outline specific compensation circuits which permit stable operation of the AD5539 down to follower (noise) gains of 3 (inverting gains of 2) with corresponding −3 dB bandwidths up to 390 MHz. External compensation is achieved by modifying the frequency response to the AD5539's external feedback network (i.e., by adding lead-lag compensation) so that the amplifier operates at a noise gain of 5 (or more) at frequencies over 44 MHz, independent of signal gain.

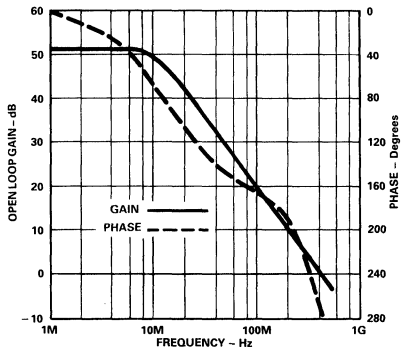


Figure 13. Small Signal Open-Loop Gain and Phase vs. Frequency

GENERAL PRINCIPLES OF LEAD AND LAG COMPENSATION

The AD5539 has its first pole or breakpoint in its open-loop frequency response at about 10 MHz (see Figure 13). At frequencies beyond 100 MHz, phase shift increases such that the output lags the input by 180° — well before the unity gain crossover frequency. Therefore, severe peaking (and possible oscillation) will result if the AD5539 is operated at noise gains below 5, unless external compensation is employed. Figure 14 shows the uncompensated closed-loop frequency response of the AD5539 when operating at a noise gain of 7. Under these conditions, excess phase shift causes nearly 10 dB of peaking at 150 MHz.

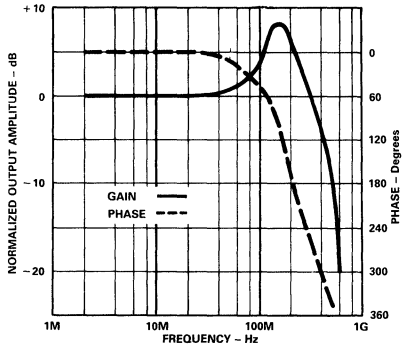


Figure 14. AD5539 Uncompensated Response, Closed-Loop Gain = 7

Figure 15 illustrates the use of both lead and lag compensation to permit stable low-gain operation. The AD5539 is shown connected as an inverting amplifier with the required external components added to provide stability and improve high frequency response. The stray capacitance between the amplifier summing junction and ground, C_X, represents whatever capacitance is associated with the particular type of op amp package used plus the stray wiring capacitance at the summing junction.

Evaluating the lead capacitance first (ignoring R_{LAG} and C_{LAG} for now): the feedback network, consisting of R2 and C_{LEAD}, has a pole frequency equal to:

$$F_A = \frac{1}{2\pi\,(C_{LEAD} + C_X)\,(R1 \parallel R2)} \quad (1)$$

and a zero frequency equal to:

$$F_B = \frac{1}{2\pi\,(R1 \times C_{LEAD})} \quad (2)$$

Usually, frequency F_A is made equal to F_B; that is, $(R1C_X) = (R2\,C_{LEAD})$, in a manner similar to the compensation used for an attenuator or scope probe. However, if the pole frequency, F_A, will lie above the unity gain crossover frequency (440MHz), then the optimum location of F_B will be near the crossover

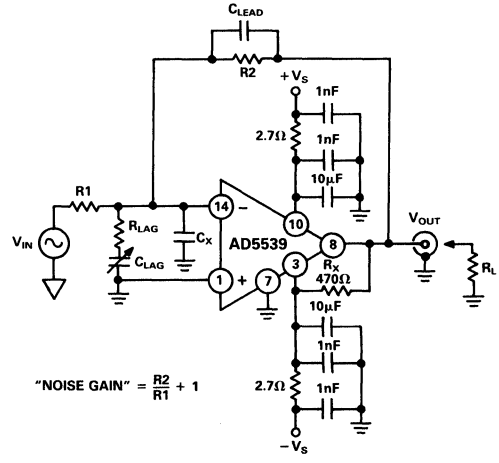


Figure 15. Inverting Amplifier Model Showing Both Lead and Lag Compensation

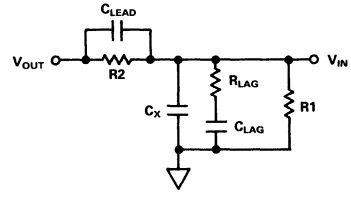


Figure 16. A Model of the Feedback Network of the Inverting Amplifier

The lag network (R_{LAG}, C_{LAG}) increases the feedback attenuation, i.e.: the amplifier operates at a higher noise gain, above some frequency, typically one tenth of the crossover frequency. As an example, to achieve a noise gain of 5 at frequencies above 44 MHz, for the circuit of Figure 15, would require a network of:

$$R_{LAG} = \frac{R1}{(4R1/R2) - 1} \quad (3)$$

and . . .

$$C_{LAG} = \frac{1}{2\pi\, R_{LAG}\, (44 \times 10^6)} \quad (4)$$

It is worth noting that an R_{LAG} resistor may be used alone, to increase the noise gain above 5 at all frequencies. However, this approach has the disadvantage of also increasing the dc offset and low frequency noise errors by an amount equal to the increase in gain, in this case, by a factor of 5.

SOME PRACTICAL CIRCUITS

The preceding general principles may now be applied to some actual circuits.

A General Purpose Inverter Circuit

Figure 17 is a general purpose inverter circuit operating at a gain of −2.

For this circuit, the total capacitance at the inverting input is approximately 3 pF; therefore, C_{LEAD} from Equations 1 and 2 needs to be approximately 1.5 pF. As shown in Figure 17, a small trimmer is used to optimize the frequency response of this circuit. Without a lag compensation network, the noise gain of the circuit is 3.0 and, as shown in Figure 18, the output amplitude remains within ±0.5 dB to 170 MHz and the −3 dB bandwidth is 200 MHz.

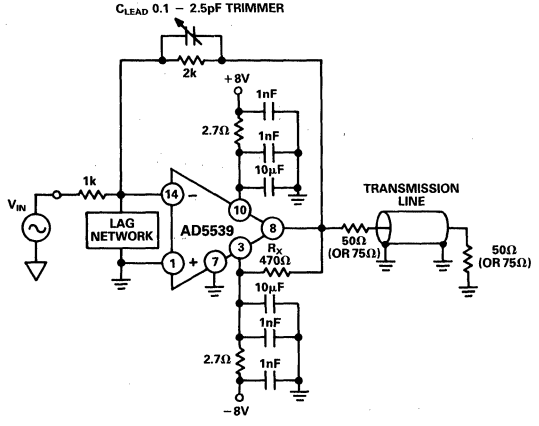


Figure 17. A General Purpose Inverter Circuit

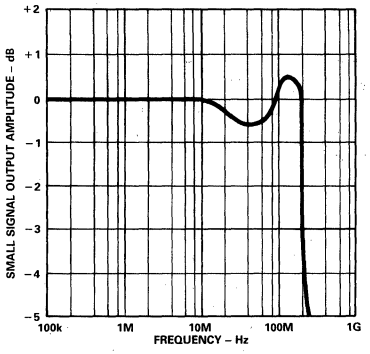


Figure 18. Response of the (Figure 17) Inverter Circuit without a Lag Compensation Network

A lag network (Figure 15) can be added to improve the response of this circuit even further as shown in Figures 19 and 20. In almost all cases, it is imperative to make capacitor C_{LEAD} adjustable; in some cases, C_{LAG} must also be variable. Otherwise, component and circuit capacitance variations will dominate circuit performance.

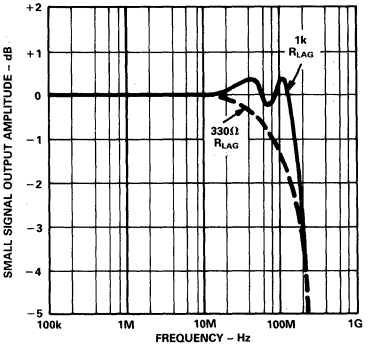


Figure 19. Response of the (Figure 17) Inverter Circuit with an R_{LAG} Compensation Network Employed

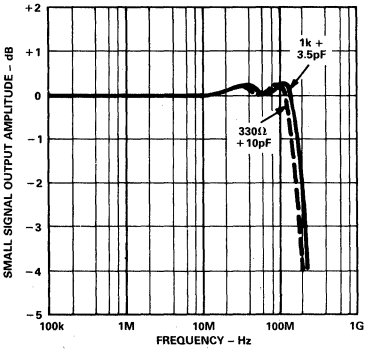


Figure 20. Response of the (Figure 17) Inverter Circuit with an R_{LAG} and a C_{LAG} Compensation Network Employed

Figures 21 and 22 show the small and large signal pulse responses of the general purpose inverter circuit of Figure 17, with C_{LEAD}=1.5 pF, R_{LAG}=330 Ω and C_{LAG}=3.5 pF.

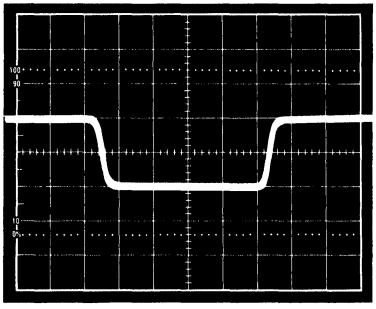


Figure 21. Small Signal Pulse Response of the (Figure 17) Inverter Circuit. Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

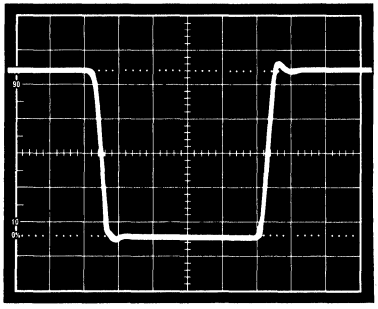


Figure 22. Large Signal Response of the (Figure 17) Inverter. Vertical Scale: 200 mV/div, Horizontal Scale: 5 ns/div

A C_{LEAD} capacitor may be used to limit the circuit bandwidth and to achieve a single pole response free of overshoot

$$\left(-3\ dB\ frequency = \frac{1}{2\pi\ R2\ C_{LEAD}}\right)$$

If this option is selected, it is recommended that a C_{LEAD} be connected between Pin 12 and the summing junction, as shown in Figure 23. Pin 12 provides a separately buffered version of the output signal. Connecting the lead capacitor here avoids the excess output-stage phase shift and subsequent oscillation problems (at approx. 350 MHz) which would otherwise occur when using the circuit of Figure 17 with a C_{LEAD} of more than about 2 pF.

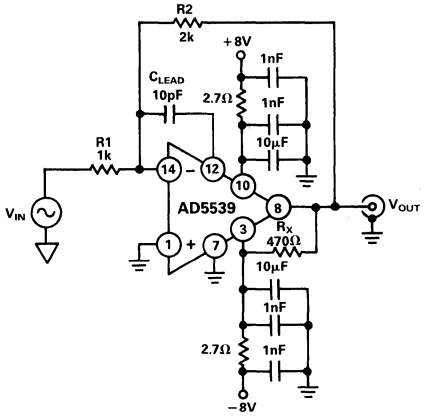


Figure 23. A Gain of 2 Inverter Circuit with the C_{LEAD} Capacitor Connected to Pin 12

Figure 24 shows the response of the circuit of Figure 23 for each connection of C_{LEAD}. Lag components may also be added to this circuit to further tailor its response, but, in this case, the results will be slightly less satisfactory than connecting C_{LEAD} directly to the output, as was done in Figure 17.

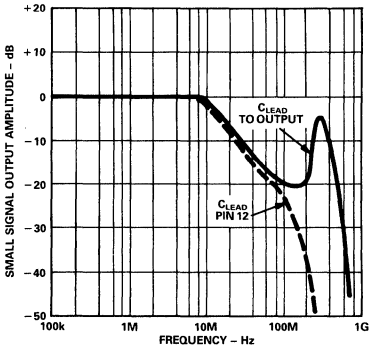


Figure 24. Response of the Circuit of Figure 23 with C_{LEAD} = 10 pF

A General Purpose Voltage Follower Circuit

Noninverting (voltage follower) circuits pose an additional complication, in that when a lag network is used, the source impedance will affect the noise gain. In addition, the slightly greater bandwidth of the noninverting configuration makes any excess phase shift due to the output stage more of a problem.

For example, a gain of 3 noninverting circuit with C_{LEAD} connected normally (across the feedback resistor — Figure 25) will require a source resistance of 200 Ω or greater to prevent UHF oscillation; the extra source resistance provides some damping as well as increasing the noise gain. The frequency response plot of Figure 26 shows that the highest −3 dB frequency of all the applications circuits can be achieved using this connection, unfortunately, at the expense of a noise gain of 14.2.

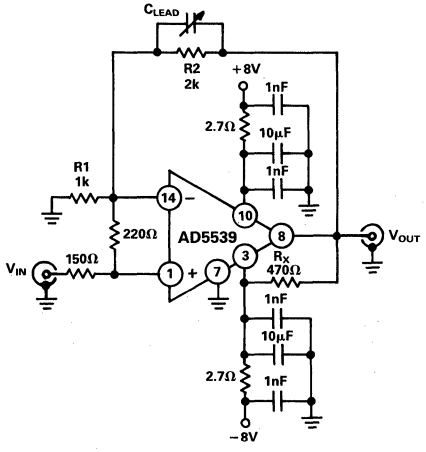


Figure 25. A Gain of 3 Follower with Both Lead and Lag Compensation

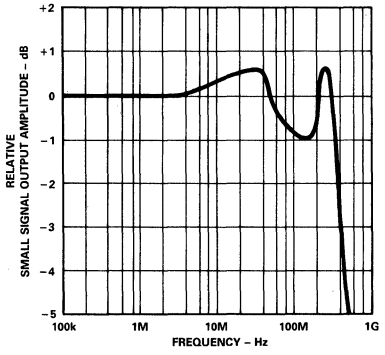


Figure 26. Response of the Gain of 3 Follower Circuit

Adding a lag capacitor (Figure 27) will greatly reduce the midband and low frequency noise gain of the circuit while sacrificing only a small amount of bandwidth as shown in Figure 28.

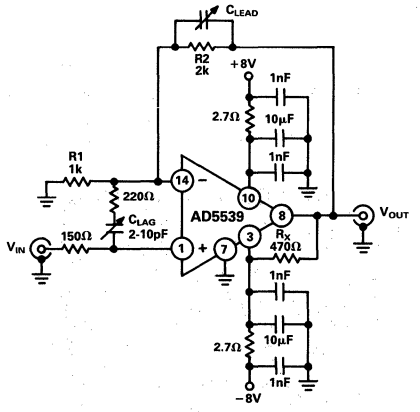


Figure 27. A Gain of 3 Follower Circuit with Both C_{LEAD} and R_{LAG} Compensation

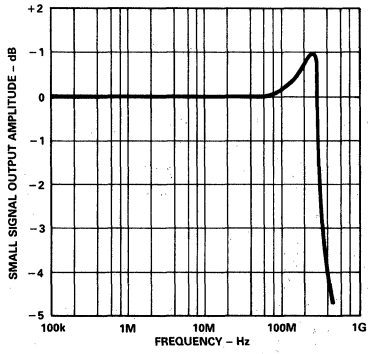


Figure 28. Response of the Gain of 3 Follower with C_{LEAD}, C_{LAG} and R_{LAG}

These same principles may be applied when capacitor C_{LEAD} is connected to Pin 12 (Figure 29). Figure 30 shows the bandwidth of the gain of 3 amplifier for various values of R_{LAG}. It can be seen from these response plots that a high noise gain is still needed to achieve a reasonably flat response (the smaller the value of R_{LAG}, the higher the noise gain). For example, with a

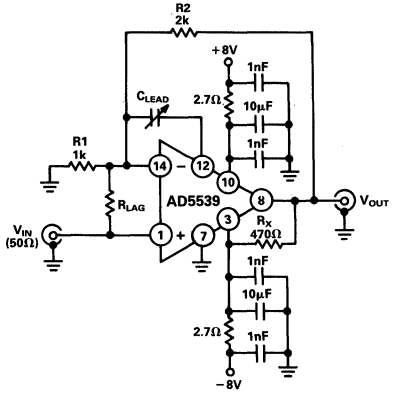


Figure 29. A Gain of 3 Follower Circuit with C_{LEAD} Compensation Connected to Pin 12

220 Ω R_{LAG} and a 50 Ω source resistance, the noise gain will be 12.8, because the source resistance affects the noise gain.

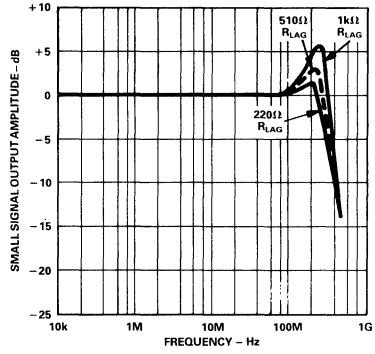


Figure 30. Response of the Gain of 3 Follower Circuit with C_{LEAD} Connected to Pin 12

Figures 31 and 32 show the small and large signal responses of the circuit of Figure 29.

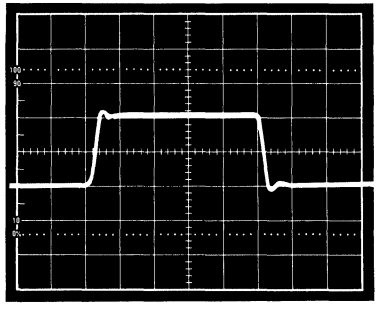


Figure 31. The Small-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12. Vertical Scale: 50 mV/div.; Horizontal Scale: 5 ns/div

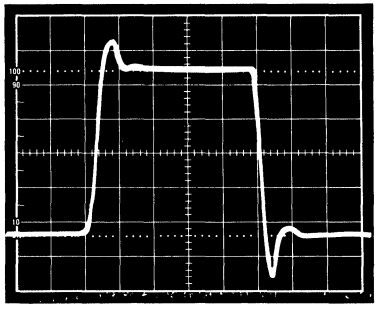


Figure 32. The Large-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12. Vertical Scale: 200 mV/div; Horizontal Scale: 5 ns/div

A Video Amplifier Circuit with 20 dB Gain (Terminated)
High gain applications (14 dB and up) require only a small lead capacitance to obtain flat response. The 26 dB (20 dB terminated) video amplifier circuit of Figure 33 has the response shown in Figure 34 using only approximately 0.5–1 pF lead capacitance. Again, a small C_{LEAD} can be connected, either to the output or to Pin 12 with very little difference in response.

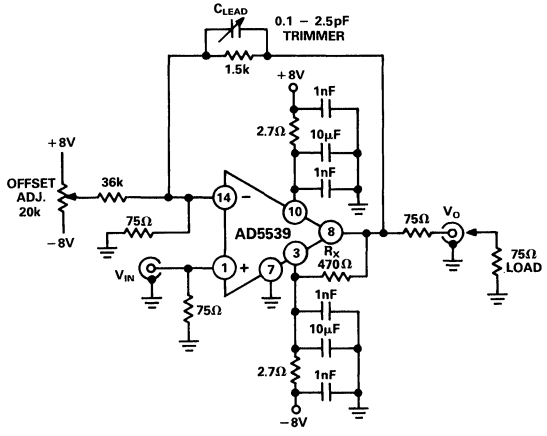


Figure 33. A 20 dB Gain Video Amplifier for 75 Ω Systems

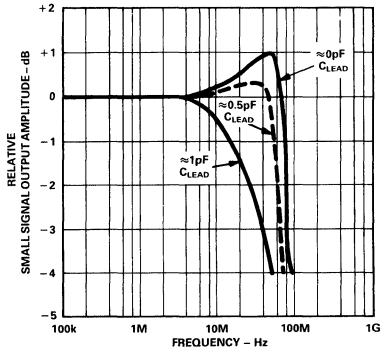


Figure 34. Response of the 20 dB Video Amplifier

In color video applications, the quality of differential gain and differential phase response is very important. Figures 35 and 36 show a circuit and test setup to measure the AD5539's response to a modulated ramp signal (0–90 IRE p–p ramp, 40 IRE p–p modulation, 4.4 MHz).

Figures 37 and 38 show the differential gain and phase response.

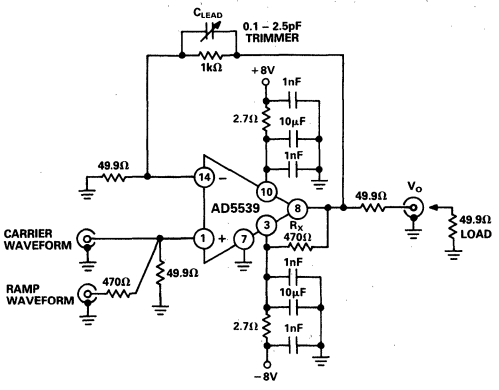


Figure 35. Differential Gain and Phase Measurement Circuit

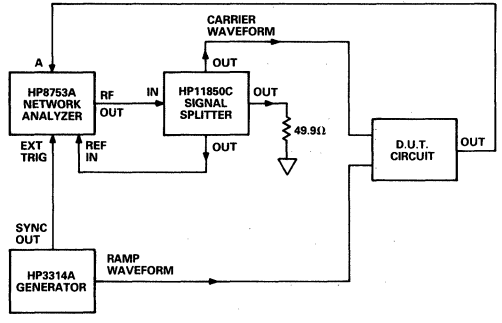


Figure 36. Differential Gain and Phase Test Setup

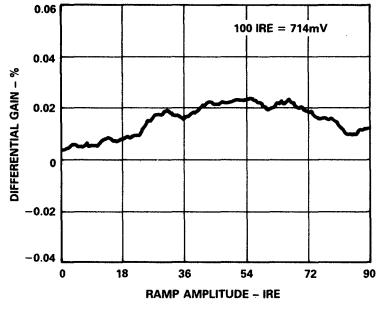


Figure 37. Differential Gain vs. Ramp Amplitude

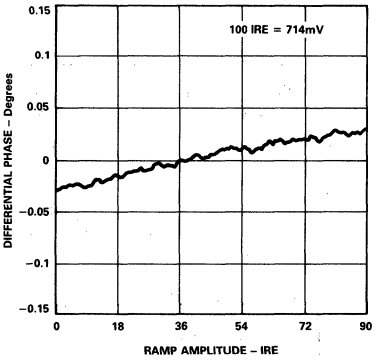


Figure 38. Differential Phase vs. Ramp Amplitude

MEASURING AD5539 SETTLING TIME

Measuring the very rapid settling times associated with AD5539 can be a real problem for the designer; proper component layout must be used and appropriate test equipment selected. In addition, both cable dispersion (a function of cable losses) and the quality of termination (SWR) directly affect the measurement. The circuit of Figure 39 was used to make a "brute force" AD5539 settling time measurement. The fixture containing the circuit was connected directly — using a male BNC connector (but no cable) — onto the front of a 50 Ω input oscilloscope preamp. A digital mainframe was then used to capture, average, and expand the error signal. Most of the small-scale waveform aberrations shown on the figure were caused by the oscilloscope itself, especially the glitch at 15 ns. The pulse source used for this measurement was an EH-SPG2000 pulse generator set for a 1 ns rise-time; it was coupled directly to the circuit using 18″ of microwave 50 Ω hard line.

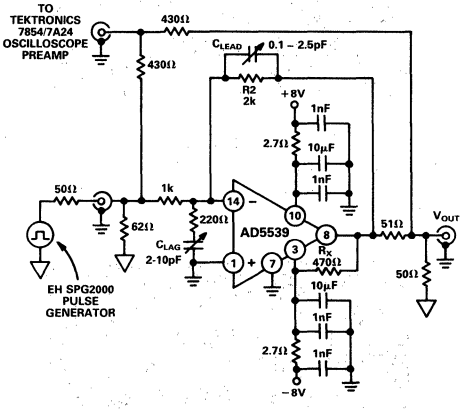


Figure 39. AD5539 Settling Time Test Circuit

APPLICATIONS SUMMARY CHART

	R1	R2[1]	R_{LAG}	C_{LAG}[2]	C_{LEAD}[2]	GAIN	GAIN FLATNESS (TRIMMED)	−3dB BANDWIDTH
Gain = −1 to −5 Circuit of Fig. 17	$\frac{R2}{G}$	2k	$\leqq \frac{R1}{4\frac{R1}{R2}-1}$	$\geqq \frac{1}{2\pi(44\times10^6)R_{LAG}}$	$\approx \frac{3pF}{G}$	−2	±0.2dB	200MHz
Gain = −1 to −5 Circuit of Fig. 23	$\frac{R2}{G}$	2k	$\leqq \frac{R1}{4\frac{R1}{R2}-1}$	$\geqq \frac{1}{2\pi(44\times10^6)R_{LAG}}$	$\approx \frac{3pF}{G}$	−2	±1dB	180MHz
Gain = +2 to +5[3] Circuit of Fig. 27	$\frac{R2}{G-1}$	2k	$\leqq \frac{R1}{10\frac{R1}{R2}-1}$	$\geqq \frac{1}{2\pi(44\times10^6)R_{LAG}}$	$\approx \frac{3pF}{G-1}$	+3	±1dB	390MHz
Gain = +2 to +5[4] Circuit of Fig. 29	$\frac{R2}{G-1}$	2k	$\leqq \frac{R1}{10\frac{R1}{R2}-1}$	NA	$\approx \frac{3pF}{G-1}$	+3	±0.5dB	340MHz
Gain < −5	$\frac{R2}{G}$	1.5k	NA	NA	Trimmer[5]	−20	±0.2dB	80MHz
Gain > +5	$\frac{R}{G-1}$	1.5k	NA	NA	Trimmer[5]	+20	±0.2dB	80MHz

G = Gain NA = Not Applicable
[1]Values given for specific results summarized here – applications can be adapted for values different than those specified.
[2]It is recommended that C_{LEAD} and C_{LAG} be trimmers covering a range that includes the computed value above.
[3]$R_{SOURCE} \geqq 200\Omega$.
[4]$R_{SOURCE} \geqq 50\Omega$.
[5]Use Voltronics CPA2 0.1 – 2.5pF Teflon Trimmer Capacitor (or equivalent).

The photos of Figures 40 and 41 demonstrate how the AD5539 easily settles to 1% (1 mV) in less than 12 ns; settling to 0.1% (100 μV) requires less than 25 ns.

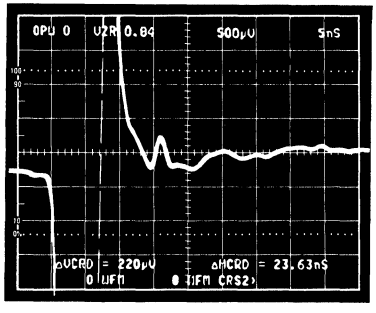


Figure 40. Error Signal from AD5539 Settling Time Test Circuit – Falling Edge. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

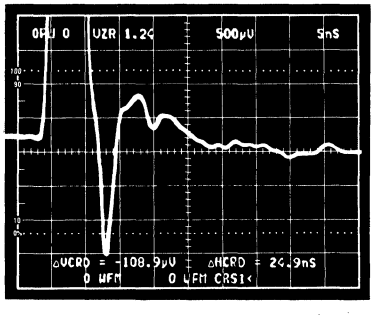


Figure 41. Error Signal from AD5539 Settling Time Test Circuit – Rising Edge. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

Figure 42 shows the oscilloscope response of the generator alone, set up to simulate the ideal test circuit error signal (Figure 43).

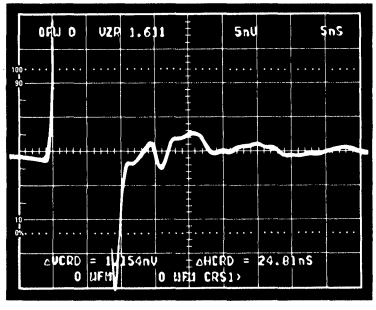


Figure 42. The Oscilloscope Response Alone Directly Driven by the Test Generator. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

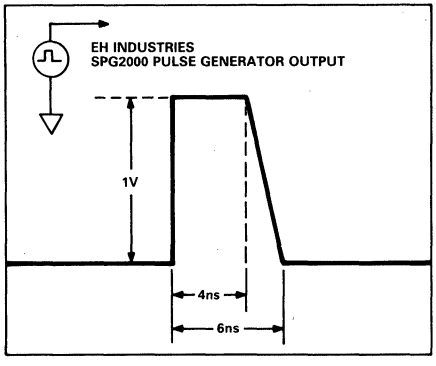


Figure 43. A Simulated Ideal Test Circuit Error Signal

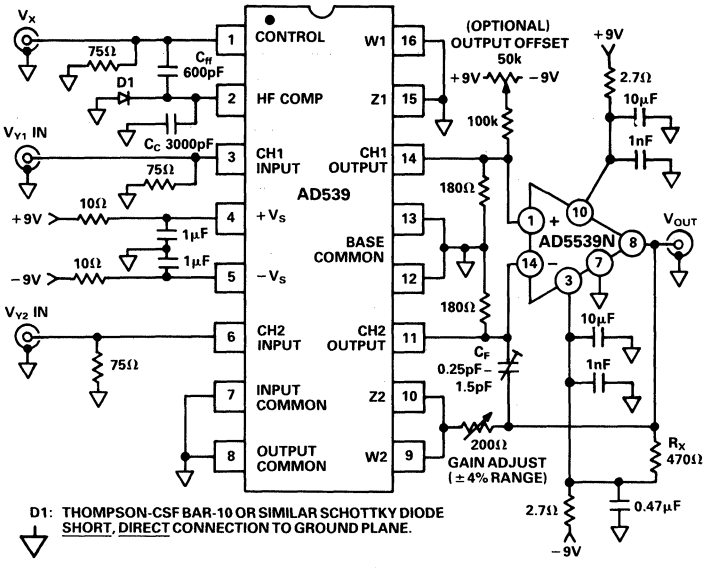


Figure 44. A Wide Bandwidth Voltage-Controlled Amplifier

A 50 MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 44 is a circuit for a 50 MHz voltage-controlled amplifier (VCA) suitable for use in high quality video-speed applications. This circuit uses the AD5539 as an output amplifier for the AD539, a high bandwidth multiplier. The outputs from the two signal channels of the AD539 are applied to the op amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven ($V_X<0$ or $V_X>3.3$ V). Secondly, it provides a choice of either noninverting or inverting responses, using either input V_{Y1} or V_{Y2}, respectively. In this circuit, the output of the op amp will equal:

$$V_{OUT}=\frac{V_X\,(V_{Y1}\,-\,V_{Y2})}{2V}\;for\;V_X>0$$

Hence, the gain is unity at $V_X = +2$ V. Since V_X can overrange to +3.3 V, the maximum gain in this configuration is about 4.3 dB. (Note: If Pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10 dB.)

The bandwidth of this circuit is over 50 MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, extreme care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 45 shows the ac response from the noninverting input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5$ V rms for values of V_X from +10 mV to +3.16 V; this is with a 75 Ω load on the output. The feedthrough at $V_X = -10$ mV is also shown.

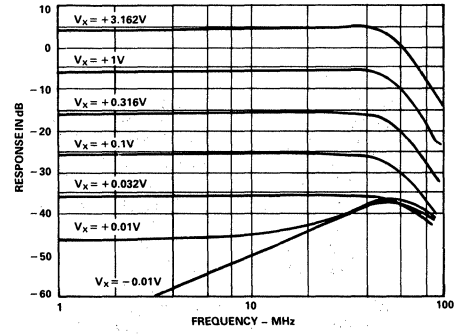


Figure 45. AC Response of the VCA at Different Gains $V_Y = 0.5$ V RMS

The transient response of the signal channel at $V_X = +2$ V, $V_Y = V_{OUT} = +$ or -1 V is shown in Figure 46; with the VCA driving a 75 Ω load. The rise and fall times are both approximately 7 ns.

A few final circuit details: in general, the control amplifier compensation capacitor for Pin 2, C_C, must have a minimum value of 3000 pF (3 nF) to provide both circuit stability and maximum control bandwidth. However, if the *maximum* control bandwidth is not needed, then it is advisable to use a larger value of C_C, with typical values between 0.01 and 0.1 μF. Like many aspects of design, the value of C_C will be a tradeoff: higher values of C_C will lower the high frequency distortion, reduce the high frequency crosstalk and improve the signal channel phase response. Conversely, lower values of C_C will provide a higher control channel bandwidth at the expense of degraded linearity in the output response when amplitude modulating a carrier signal.

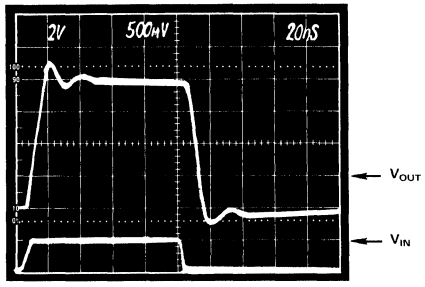


Figure 46. Transient Response of the Voltage-Controlled Amplifier V_X = +2 Volts, V_Y = ±1 Volt

The control channel bandwidth will vary in inverse proportion to the value of C_C, providing a typical bandwidth of 2 MHz with a C_C of 0.01 μF and a V_X voltage of +1.7 volts.

Both the bandwidth and pulse response of the control channel can be further increased by using a feedforward capacitor, C_{ff}, with a value between 5 and 20 percent of C_C. C_{ff} should be carefully adjusted to give the best pulse response for a particular step input applied to the control channel. Note that since C_{ff} is connected between a linear control input (Pin 1) and a logarithmic node, the settling time of the control channel with a pulse input will vary with different control input step levels.

Diode D1 clamps the logarithmic control node at Pin 2 of the AD539, (preventing this point from going too negative); this diode helps decrease the circuit recovery time when the control input goes below ground potential.

THE AD539/5539 COMBINATION AS A FAST, LOW FEEDTHROUGH, VIDEO SWITCH

Figure 47 shows how the AD539/5539 combination can be used to create a fast video speed switch suitable for many high frequency applications including color key switching. It features both inverting and noninverting inputs and can provide an output of ±1 V into a reverse-terminated 75 Ω load (or ±2 V into 150 Ω). An optional output offset adjustment is provided. The input range of the video switch is the same as the output range: ±1 V at either input generates ±1 V (noninverting) or ∓1 V (inverting) across the 75 Ω load. The circuit provides a gain of about 1, when "ON," or zero when "OFF."

The differential configuration uses both channels of the AD539 not only to provide alternative input phases, but also to eliminate the switching pedestal due to step changes in the output current as the AD539 is gated on or off.

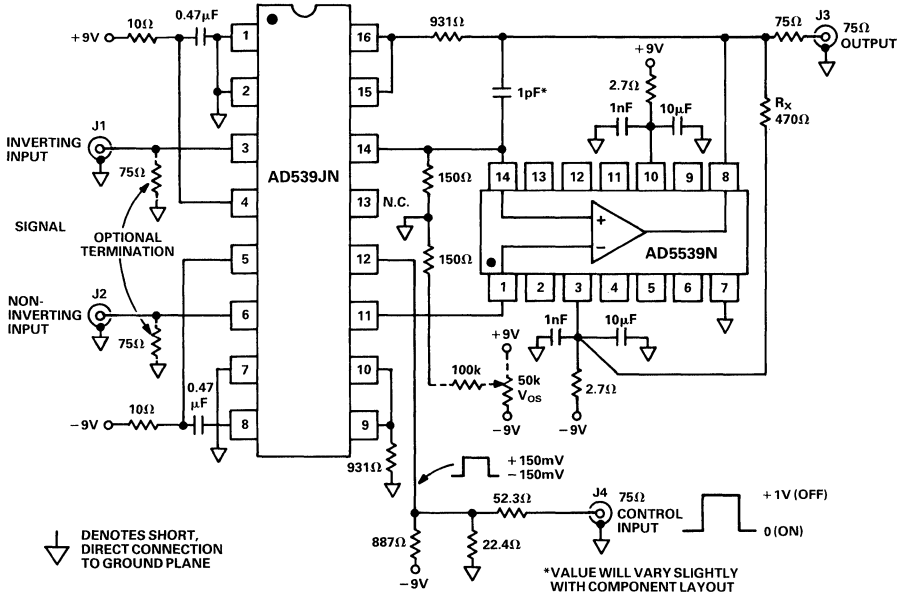


Figure 47. An Analog Multiplier Video Switch

Figure 49 shows the response to a pulse of 0 to +1 V on the signal channel. With the control input held at zero, the rise time is under 10 ns. The response from the inverting input is similar.

The differential-gain and differential-phase characteristics of this switch are compatible with video applications. The incremental gain changes less than 0.05 dB over a signal window of 0 to +1 V, with a phase variation of less than 0.5 degree at the subcarrier frequency of 3.58 MHz. The noise level of this circuit measured at the 75 Ω load is typically 200 μV in a 0 to 5 MHz bandwidth or approximately 100 nV per root hertz. The noise spectral density is essentially flat to 40 MHz.

The waveforms shown in Figures 48 and 49 were taken across a 75 Ω termination; in both photos, the signal of 0 to +1 V (in this case, an offset sine wave at 1 MHz) was applied to the noninverting input. In Figure 48, the envelope response shows the output being fully switched in about 50 ns. Note that the output is ON when the control input is zero (or more negative) and OFF for a control input of +1 V or more. There is very little control-signal breakthrough.

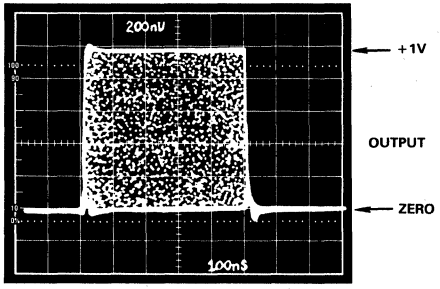


Figure 48. The Control Response of the Video Switcher

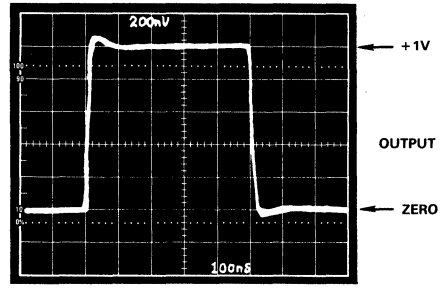


Figure 49. The Signal Response of the Video Switcher

Wide Bandwidth, Fast Settling Operational Amplifier

AD9610

FEATURES
Ultrastable Unity Gain Bandwidth (100MHz)
Bandwidth Is Independent of Gain Settings
18ns Settling to 0.1%
Low Power Dissipation (630mW)
Complete Overdrive Protection
Low Distortion (THD: −59dBc @ 20MHz, −78dBc @ 5MHz, −100dBc @ 10kHz)
Excellent DC Specifications
Available Processed to MIL-STD 883

APPLICATIONS
Driving Flash Converters
High Speed DAC I/V Converters
Radar, IF Processors
Broadband, Digital Radio
Photodiode Preamps (FLIR)
ATE/Pulse Generators
Imaging/Display Drivers

GENERAL DESCRIPTION

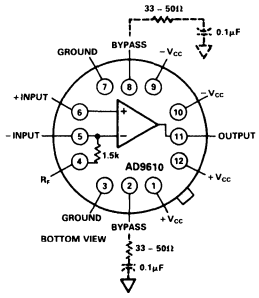
The AD9610 is a fast settling, wide bandwidth, dc coupled, operational amplifier which combines superior dc specifications and exceptional dynamic performance with impeccable spectral purity (harmonic distortion, intermodulation distortion, noise, etc.) over the full bandwidth. This combination provides remarkable versatility and utility for high speed designers.

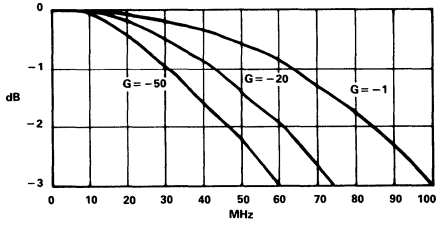
Thin-film technology and innovative design techniques help assure stable operation over the complete operating temperature range. Input offset voltage is ±0.3mV, with 5μV/°C drift; input bias currents are ±15μA with ±30nA/°C drift.

Unique internal architecture employing current feedback keeps the AD9610 inherently stable over its complete gain range and assures wide bandwidth at all gain settings. With G = −1, −3dB bandwidth is 120MHz; with G = −10, −3dB bandwidth is 100MHz. When G = −50, the −3dB bandwidth is 60MHz. Slew rate, fall time and settling time are also independent of gain.

Frequency domain performance for the AD9610 is unmatched. The part can be used in applications requiring wide spurious free dynamic range. At 10kHz total harmonic distortion (THD) is −100dBc; at 1MHz the THD is −85dBc; at 20MHz the THD is −59dBc. Third order intermodulation distortion is similarly impressive, which is often required in communications applications.

AD9610 FUNCTIONAL BLOCK DIAGRAM





AD9610 Inverting Gain

The design of the AD9610 makes it easy to apply. The unit requires no external compensation. An internal 1.5kΩ feedback resistor is available to the user by connecting Pin 4 to Pin 11. This resistor is trimmed for gain accuracy and should be used when the full bandwidth of the amplifier is required. To achieve higher gains, and for lower bandwidth applications, an external resistor can be used. Pins 2 and 8 are bypass pins and should be connected to ground through 33 – 50Ω resistors and 0.1μF ceramic capacitors; effective decoupling of the power supplies is also important to obtain optimum high frequency performance.

Two temperature ranges are available. The AD9610BH is guaranteed over a case temperature range of −25°C to +85°C; the AD9610TH is for a range of −55°C to +125°C. The AD9610TH/883B boasts the same specifications as the TH grade but is processed to the latest REV of MIL-STD-883.

SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V = \pm 15V$; $A_V = -10$; $R_{IN} = 1500\Omega$; $R_F = 15k\Omega$; No R_{LOAD})

	Parameter (Conditions)	Sub-Group	AD9610BH/TH Typical @ +25°C	AD9610BH[1] Min/Max @ −25°C	AD9610BH[1] Min/Max @ +25°C	AD9610BH[1] Min/Max @ +85°C	AD9610TH[2] Min/Max @ −55°C	AD9610TH[2] Min/Max @ +25°C	AD9610TH[2] Min/Max @ +125°C	Units
√	Offset Voltage	1,2,3	±0.3	±4.0	±1.0	±2.5	±4.0	±1.0	±2.5	mV
√	Offset Voltage T_C[3]	2,3	±5				±25		±25	µV/°C
√	Input Bias Current									
	Inverting	1,2,3	±5	±56	±15	±35	±56	±15	±35	µA
	Noninverting	1,2,3	±15	±75	±50	±62	±75	±50	±62	µA
√	Input Bias Current T_C[3]									
	Inverting	2,3	±70				±330		±330	nA/°C
	Noninverting	2,3	±30				±200		±200	nA/°C
#	Inverting Impedance		20							Ω
#	Noninverting									
	Impedance		200k							Ω
	Capacitance		2							pF
#	Common-Mode Input		±5	±5	±5	±5	±5	±5	±5	V
√	Internal Feedback Resistor (R_F)		1500		1490/1510			1490/1510		Ω
#	R_F Temperature Coefficient			±25		±25	±25		±25	ppm/°C
√	Common-Mode Rejection Ratio (CMRR)[4]	4,5,6	>50	≥35	≥35	≥35	≥35	≥35	≥35	dB
	CMRR ($R_F = 1500\Omega$; $R_{IN} = 150\Omega$; $\Delta V_S = 5V$)		>60							dB
√	Common-Mode Sensitivity (CMS),[5]									
	Referred to Input ($\Delta V_S = 5V$)									
	−CMS	4,5,6	3	8	8	8	8	8	8	µA/V
	+CMS	4,5,6	3	8	8	8	8	8	8	µA/V
	$CMS_{VOLTAGE}$	4,5,6	62	≥50	≥50	≥50	≥50	≥50	≥50	dB
#	Output Impedance (dc to 100kHz)		0.05							Ω
√	Output Voltage Swing ($R_{LOAD} = 200\Omega$)	1,2,3	±10	≥±9	≥±9	≥±9	≥±9	≥±9	≥±9	V
#	Output Current (Continuous)	1,2,3	±50	≥±50	≥±50	≥±50	≥±50	≥±50	≥±50	mA
√	Open Loop Transimpedance Gain (200Ω Load)	4,5,6	>1.5	≥0.7	≥0.9	≥0.7	≥0.7	≥0.9	≥0.7	MΩ
√	Supply Current[6]	1,2,3	21	≤27	≤25	≤27	≤27	≤25	≤27	mA
	Power Consumption[6]		630	≤810	≤750	≤810	≤810	≤750	≤810	mW
√	Power Supply Rejection Ratio (PSRR)[4]	4,5,6	>50	≥35	≥35	≥35	≥35	≥35	≥35	dB
	PSRR ($R_F = 1500\Omega$; $R_{IN} = 150\Omega$; $\Delta V_S = 10V$)		>60							dB
√	Power Supply Sensitivity (PSS),[7]									
	Referred to Input ($\Delta V_S = 10V$)									
	$PSS_{VOLTAGE}$	4,5,6	65	50	50	50	50	50	50	dB
	−PSS	4,5,6	3	8	8	8	8	8	8	µA/V
	+PSS	4,5,6	3	8	8	8	8	8	8	µA/V

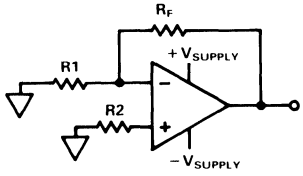
AC ELECTRICAL CHARACTERISTICS ($\pm V = \pm 15V$; $A_V = -10$; $R_{IN} = 150\Omega$; $R_F = 1.5k\Omega$; $R_{LOAD} = 200\Omega$)

	Bandwidth (−3dB) (V_{OUT} = 100mV p-p)									
√	G = −10	4,5,6	>100	≥80	≥80	≥80	≥80	≥80	≥80	MHz
	Amplitude of Peaking:									
√	DC to 60MHz	4,5,6	0	≤0.4	≤0.2	≤1.0	≤0.4	≤0.2	≤1.0	dB
#	>60MHz		0	≤0.6	≤0.3	≤1.8	≤0.6	≤0.3	≤1.8	dB
#	Phase Nonlinearity (dc to 45MHz)		1							°
#	Rise (Fall) Time (V_{OUT} = 5V Step)		<3.5	≤4	≤4	≤4.3	≤4	≤4	≤4.3	ns
#	Slew Rate (V_{OUT} = 18V Step)		>3.5	≥3	≥3	≥2.4	≥3	≥3	≥2.4	kV/µs
#	Settling Time to 0.1% (G = −10; 5V Output Step)		18	≤29	≤25	≤29	≤29	≤25	≤29	ns
#	Settling Time to 0.02% (G = −10; 5V Output Step)		30							ns
#	Overshoot Amplitude (V_{OUT} = 5V Output Step)		<4	≤14	≤8	≤18	≤14	≤8	≤18	%
#	Propagation Delay		3.3	≤4.0	≤4.0	≤4.0	≤4.0	≤4.0	≤4.0	ns
√	Total Harmonic Distortion (Freq. = 20 MHz; Output Voltage = 2V p-p)	4,5,6	55	50	50	50	50	50	50	dB
#	Input Noise ($R_{LOAD} = 100\Omega$)									
	Voltage (5MHz to 150MHz)		0.7	≤1.2	≤1.5	≤2.0	≤1.2	≤1.5	≤2.0	nV/√Hz
	Current (5MHz to 150MHz)		23	≤29	≤30	≤35	≤29	≤30	≤35	pA/√Hz

Parameter	Sub-Group	AD9610BH/TH Typical @ +25°C	AD9610BH Min/Max @ −25°C	AD9610BH Min/Max @ +25°C	AD9610BH Min/Max @ +85°C	AD9610TH AD9610TH/883B Min/Max @ −55°C	AD9610TH AD9610TH/883B Min/Max @ +25°C	AD9610TH AD9610TH/883B Min/Max @ +125°C	Units
OTHER INFORMATION									
Case to Ambient, θ_{CA}[8] (Still Air; No Heat Sink)		65	*	*	*	*	*	*	°C/W
Case to Ambient, θ_{CA}[8] (500 LFPM Air; No Heat Sink)		38	*	*	*	*	*	*	°C/W
MTBF[9]		$\geq 1.48 \times 10^6$	*	*	*	*	*	*	hours
PACKAGE OPTION[10]									
TO-8 (H12-A)			AD9610BH			AD9610TH AD9610TH/883B			

NOTES
√ 100% tested (See Notes 1 and 2).
Specifications guaranteed by design; not tested.
*Specification same as AD9610BH/TH typical specification.

[1]AD9610BH parameters preceded by a check (√) are tested at +25°C ambient temperature; performance is guaranteed over the industrial temperature range (−25°C to +85°C) case temperature.
[2]AD9610TH & AD9610TH/883B parameters preceded by a check (√) are tested at 55°C case, +25°C ambient, and +125°C case temperatures. The AD9610TH/883B is processed to the latest revision of MIL Standard 883.
[3]Offset voltage T_C and bias current T_C are guaranteed over the respective temperature ranges.
[4]CMRR and PSRR apply only for stated conditions.
[5]CMS values can be used to determine the CMRR for specific gain settings according to the following worst case relationships:



$$\Delta V_{OUT} = [-CMS][R_F][\Delta V_{SUPPLY}] + [+CMS][R2]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}] + [CMS_{VOLT}]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}]$$

$$\text{WHERE } \Delta V_{SUPPLY} = \Delta - V_{SUPPLY} \text{ AND } \Delta + V_{SUPPLY}$$

$$CMRR = -20 \text{ LOG}\left[\frac{\Delta V_{OUT}}{\left(1+\frac{R_F}{R1} \times \Delta V_{SUPPLY}\right)}\right]$$

[6]Supply current and power dissipation numbers are for quiescent operation (input is grounded). Values increase with higher frequency operation.
[7]PSS values can be used to determine the PSRR for specific gain settings according to the following worst case relationships (See diagram in 5 above):

$$\Delta V_{OUT} = [-PSS][R_F][\Delta V_{SUPPLY}] + [+PSS][R2]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}] + [PSS_{VOLT}]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}]$$

$$\text{WHERE } \Delta V_{SUPPLY} = \Delta - V_{SUPPLY} \text{ OR } \Delta + V_{SUPPLY}$$

$$PSRR = -20 \text{ LOG}\left[\frac{\Delta V_{OUT}}{\left(1+\frac{R_F}{R1} \times \Delta V_{SUPPLY}\right)}\right]$$

[8]Recommended maximum junction temperature is +165°C. See Thermal Model.
[9]MTBF calculated using MIL-HNBK 217D; Ground Fixed; Temperature (case) = +70°C.
[10]See Section 20 for package outline information.

Specifications subject to change without notice.

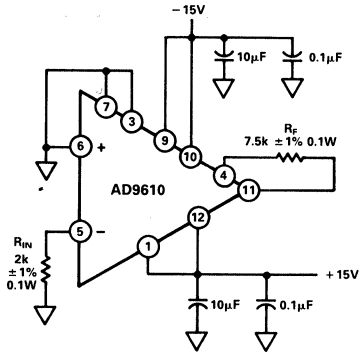
EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at maximum rated temperature.
Subgroup 3 – Static tests at minimum rated temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated temperature.
Subgroup 6 – Dynamic tests at minimum rated temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated temperatures.
Subgroup 11 – Switching tests at minimum rated temperatures.
Subgroup 12 – Periodically sample tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ($\pm V_S$) . . . . . ±18V
Operating Temperature Range (case)
AD9610BH . . . . . −25°C to +85°C
AD9610TH/TH/883B . . . . . −55°C to +125°C
Power Dissipation . . . . . See Thermal Model
Junction Temperature . . . . . +165°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C

AD9610 LIFE TEST/BURN-IN CIRCUIT



R_{IN} = RNC55H2001F
R_F = RN55C7501F
10μF = M39003101-2302
0.1μF = M39014101-1553

THIS MICROCIRCUIT IS COVERED BY TECHNOLOGY GROUP (I.) PER MIL-M-38510

THEORY OF OPERATION

The advantages of the transimpedance AD9610 Operational Amplifier become easier to understand when its operation is compared to the operation of conventional high-speed op amps.

The operation of the AD9610 Operational Amplifier is similar to a standard voltage-input differential amplifier in terms of setting gain and calculating noise. The primary difference between the two types is a low-impedance inverting input on the AD9610; this causes the unit to use current feedback, rather than voltage feedback, to achieve signal amplification.

Figure 1 and the discussion which follows help make a comparison between the AD9610 and "conventional" devices.

Two equations are necessary to describe the amplifier shown in Figure 1.

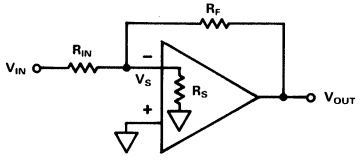


Figure 1.

One equation is a rudimentary amplifier transfer function:

$$-V_{OUT} = A(\omega)\, V_S \qquad \textit{(Equation A)}$$

and the other sums the currents at the inverting input:

$$\frac{V_S - V_{IN}}{R_{IN}} + \frac{V_S}{R_S} + \frac{V_S - V_{OUT}}{R_F} = 0 \qquad \textit{(Equation B)}$$

Rearranging and reducing Equation B; and substituting from Equation A results in a third equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A(\omega)R_S R_F \big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)}{1 + A(\omega)R_{IN}R_S \big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)} \qquad \textit{(Equation C)}$$

For purposes of discussion, assume the amplifier shown in Figure 1 exhibits a single-pole frequency response. When it does, $A(\omega) = A_O/(1 + j\omega\tau)$ where A_O = open loop gain; and $1/\tau$ = the roll-off frequency. When these terms are substituted into Equation C, the result is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_O R_S R_F \big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)}{1 + j\omega\tau + \left| A_O R_{IN}R_S \big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S) \right|}$$

Based on the idea that

$$1 + \left| A_O R_{IN}R_S \big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S) \right|$$

is approximately equal to

$$A_O R_{IN}R_S \big/ (R_S R_F + R_{IN}R_F + R_{IN}R_S)$$

and G (closed loop gain) = R_F/R_{IN}, it becomes possible to simplify and substitute terms in the above equation to obtain:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \dfrac{j\omega\tau R_F}{A_O}\left[\dfrac{1}{R_{IN}} + \dfrac{1}{R_S} + \dfrac{1}{R_F}\right]}$$

The fundamental difference between the AD9610 and traditional amplifiers becomes apparent at this point.

In traditional voltage-imput amplifiers, the input resistance (R_S) approaches infinity. Consequently, $1/R_S$ approaches zero; and the term $R_F\,(1/R_{IN} + 1/R_S + 1/R_F)$ simplifies to the term $R_F\,(1/R_{IN} + 1/R_F)$. The latter can be reduced further to $(G+1)$. When substitutions are made, the gain/frequency relationship for a traditional amplifier design is expressed as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \dfrac{j\omega\tau}{A_O}[G+1]}$$

There is a dramatically different result for the AD9610.

This difference is because the value of R_S in the transimpedance amplifier is only 20Ω. This is important when one realizes $R_S \parallel R_{IN} \parallel R_F$; and $R_S <<< R_{IN}$ and/or R_F. In this case, $(1/R_S + 1/R_{IN} + 1/R_F) \approx 1/R_S$. Substituting terms, a direct comparison with traditional amplifer relationships can be made:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \frac{j\omega\tau}{A_O}\left[\frac{R_F}{R_S}\right]}$$

Both amplifier types yield similar algebraic results, but there is one critical difference in how they are obtained.

As shown above, the closed loop gain (G) of the traditional amplifier is multiplied by the frequency-dependent term of the denominator; **this means increasing frequencies or closed loop gain accelerates the gain roll-off.**

In the AD9610, however, the constant R_F/R_S is multiplied by the frequency-dependent term; **this means bandwidth remains relatively constant for any given value of gain.**

Inside the AD9610, the design includes a 1.5kΩ feedback resistor to help reduce the effect of stray capacitances and make it easier to apply the amplifier. This internal R_F means *the gain of the AD9610 is set by varying R_{IN}.*

The differences in the architecture of the AD9610 vis-a-vis a traditional op amp cause its closed-loop frequency response to be considerably different from conventional units.

Figure 2 pictures a typical plot for a traditional single-pole amplifier.

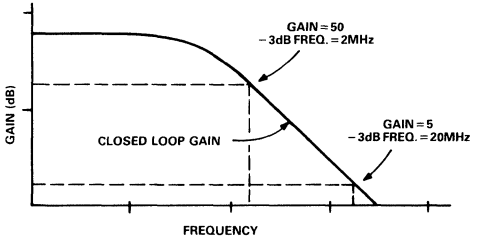


Figure 2.

As shown, increasing the closed loop gain of a traditional op amp decreases the bandwidth of the amplifier; the precise amount of change will be determined by the actual roll-off characteristics of the op amp.

By contrast, the frequency response of the AD9610 changes very little when the gain is changed. Refer to Figure 3.

Variations in gain (established by varying values of R_{IN}) have only a negligible effect on the bandwidth of the amplifier.

(NOTE: For a more complete explanation of the mathematics involved in comparing conventional op amps and the AD9610, refer to the Analog Devices application note entitled "Using the AD9610 Transimpedance Amplifier.")

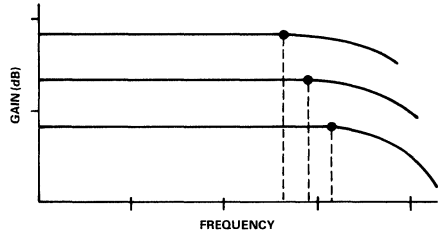


Figure 3.

AD9610 FUNCTIONAL DESCRIPTION

Refer to Figure 4, AD9610 Functional Circuit.

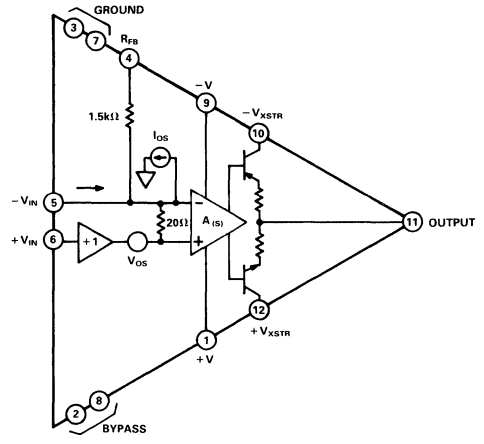


Figure 4. AD9610 Functional Circuit

The most prominent characteristic illustrated in this model of the unit is the combination of a high-impedance noninverting terminal and a low-impedance inverting terminal. This is achieved by buffering the noninverting terminal to create a high-impedance input; while maintaining a low impedance through the 20Ω characteristic of the inverting input.

Because of the low input impedance of the inverting input, all of the input signal voltage is impressed across the input resistor (R_{IN} in Figure 6); this causes a direct voltage-to-current conversion to take place.

Conventional op amps use a volts/volts transfer function, while the transfer function of the AD9610 is volts/μA (or resistance).

Signal current flowing in the inverting terminal (Pin 5) will flow through the 20Ω resistor. The voltage developed across this input impedance becomes the input signal for the internal amplifier.

As a result of this action, the input current is converted to an output voltage; this is the reason for the open loop transfer function being expressed in ohms.

To compensate for variations in offset voltage and current in the AD9610, both a voltage source and a current source are included in the unit. Input offset voltage (V_{OS}) is a dc error which appears at the output as $[V_{OS}\ (1+R_F/R_{IN})]$. In a similar fashion, the input bias current (I_{OS}) reflects as a dc error which appears at the output as $[I_{OS}\ (R_F)]$.

The current source connected to the inverting terminal effectively models the input offset current; and although bias currents flow in both terminals, the inverting input bias current is dominant. The combined actions of the internal voltage and current sources effectively compensate for discrepancies in offset voltage and current.

Power supply voltages applied to the AD9610 are separated, with one set of terminals designated for the output transistors (Pins 10 and 12) and another set for the internal amplifier (Pins 1 and 9). This splitting of the voltages makes it possible to limit voltage swings and current at the output, and helps regulate the junction temperatures of the output transistors.

APPLYING THE AD9610 OP AMP

In applying the AD9610 op amp, there are certain precautions which **must** be observed to protect the unit from damage:

1. Shorting either power supply input pin (Pin 10 or Pin 12) to the output (Pin 11) will destroy the device.
2. Shorting the output (Pin 11) to ground will destroy the device; no internal protection is provided.

As explained earlier, the noninverting input of the AD9610 Operational Amplifier is a high impedance. This requires that it be driven from a low-impedance source, or connected to ground. Driving this input from a high impedance detracts from the wide bandwidth performance; connecting it to ground avoids the possibility of closed-loop ac peaking.

Because the internal biasing network of the AD9610 is connected to the +V and −V supply pins, it is important that these pins have adequate decoupling. Nominal supply voltages for the AD9610 are ±15V, but this can be reduced to a lower limit of ±12V without serious degradation of high-speed performance. When ±12V supplies are used, output voltage swings from the amplifier must be reduced.

Bypass Pins 2 and 8 should be decoupled to ground through 33 – 50Ω resistors and 0.1μF capacitors to maintain stability on the bias network.

Feedback resistor R_F is internal to the AD9610 and has been precisely adjusted to allow the widest possible range of operating conditions. While it is possible to use an external feedback resistor for the device, the user is urged to avoid the temptation to "tune" performance with this technique because it will inevitably detract from ac performance.

A massive low-impedance ground plane is essential for optimum performance from the AD9610 because it provides a moderate level of shielding and helps reduce the effects of distributed capacitance.

But the benefits of a large ground plane can be diminished if components are grounded at multiple points on the ground plane. Single-point grounding is *always* preferred for high-speed circuits to avoid the possibility of voltage differentials which might result from multiple grounds.

The best high-frequency performance is obtained from the AD9610 when total output capacitance is minimized. Realistically, this is not always possible; but performance can be improved with a 5 – 30Ω resistor in series with the output as shown in Figure 5.

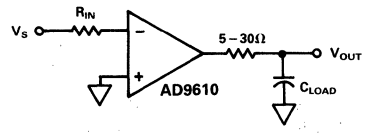


Figure 5.

Isolation provided by the series resistor makes it possible for the AD9610 to drive loads well outside its design limits, but at some loss of speed. Isolating the capacitive load from the output of the amplifier is particularly useful when driving flash A/D converters.

The power supplies for the AD9610 must be decoupled effectively to obtain maximum performance from the device. Recommended choices are a 0.1μF ceramic capacitor and a 10μF tantalum capacitor in parallel on each supply. These connections show up in Figures 6 and 7 which illustrate the connections for inverting and noninvertering operation, respectively. Decoupling components should always be connected as closely as possible to the amplifier's voltage supply pins.

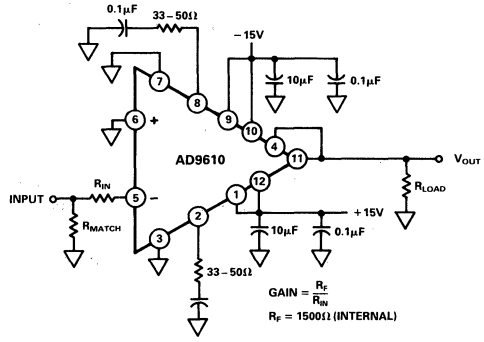


Figure 6. AD9610 Inverting Operation

If the expected output voltage swings are small, it is possible to operate the ouput stages from ±5V supplies; this will reduce power dissipation and junction temperatures on the output transistors. For this, the ±5V and ±15V supplies must be decoupled separately.

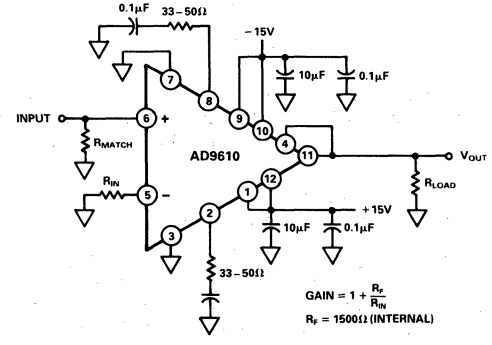


Figure 7. AD9610 Noninverting Operation

As shown in Figures 6 and 7, bypass Pins 2 and 8 should be decoupled individually with a 33 – 50Ω resistor and 0.1μF capacitor in series to ground. Without this decoupling, power supply and common-mode rejection ratios (PSRR and CMRR) may be degraded. In some applications, the lack of this decoupling may show up as very high-frequency "ringing" on the output. R_{MATCH} in Figures 6 and 7 is used to match the output impedance of the driving source.

AD9610 POWER DISSIPATION

Quiescent power supply currents for the AD9610 are ±21mA. Supply currents this low allow the unit to be operated over a wide temperature range without damage. For high-temperature operation and long-term stability, however, the user is urged to use a heat sink. Two acceptable models for TO-8 packages are the Thermalloy 2240 and the IERC Up-TO8-48CB.

Refer to Figure 8.

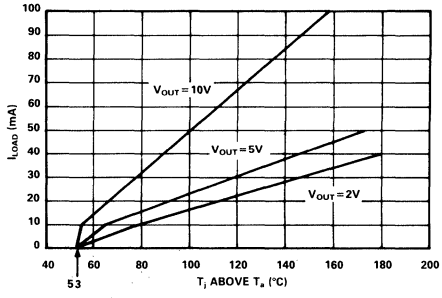
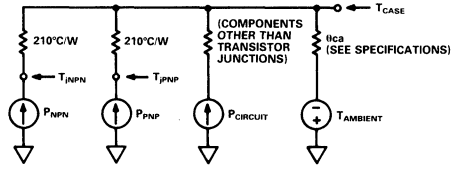


Figure 8. Junction Temp. Rise vs. Load Current

The data in this illustration are typical characteristics when the AD9610 is operated from ±15V supplies. Assume the desired output from the op amp is ±10V swings at ±50mA currents. For this combination, maximum junction temperature will be 100°C above the ambient temperature.

Since maximum allowable junction temperature is +165°C, the maximum ambient temperature which can be tolerated is +65°C. If there is a possibility the ambient may exceed this limit, heat sinking and/or heat removal is required. Additional details on the thermal characteristics of the unit are included in the AD9610 Thermal Model. *(For more information on thermal protection, consult the Analog Devices application note "Using the AD9610 Transimpedance Amplifier".)*



$P_{CIRCUIT} = I_{CC}[+V_{CC} - (-V_{CC})]$ WHERE I_{CC} = 21mA @ ±15V

$P_{xxx} = [(\pm V_{CC}) - V_{OUT} - I_{COL}(8)](I_{COL})$ (% DUTY CYCLE)

NOTE: xxx = NPN OR PNP

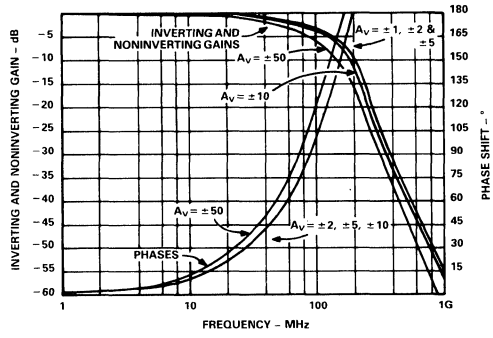
(FOR POSITIVE V_{OUT} AND V_{CC}, THIS IS POWER IN NPN OUTPUT STAGE; FOR NEGATIVE V_{OUT} AND V_{CC}, THIS IS POWER IN PNP OUTPUT STAGE. $I_{COL} = V_{OUT}/R_{LOAD}$ or 3.0mA, WHICHEVER IS GREATER. FEEDBACK RESISTOR R_F IS INCLUDED IN R_{LOA}.)

$T_{j(PNP)} = P_{PNP}(210 + \theta ca) + (P_{CIRCUIT} + P_{NPN})(\theta ca) + T_a$. SIMILAR FOR $T_{j(NPN)}$

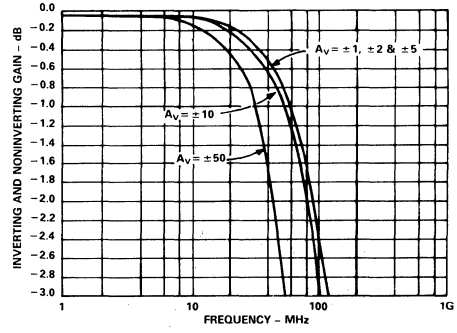
AD9160 Thermal Model

AD9610 PERFORMANCE

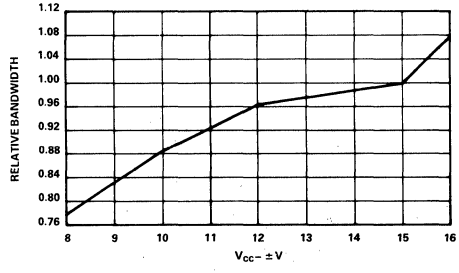
In the following section, graphs and photographs depict typical performance of the AD9610 for various characteristics.



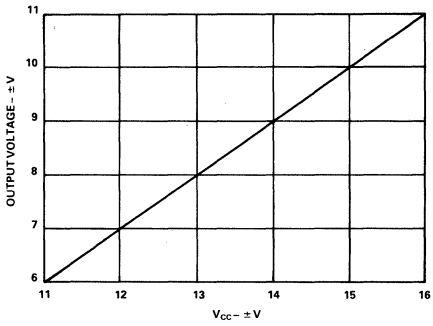
AD9610 Frequency Response (A_V = ±1, ±2, ±5, ±10, ±50)



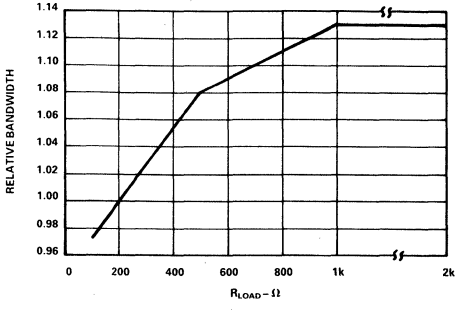
AD9610 Frequency Response (A_V = ±1, ±2, ±5, ±10, ±50)



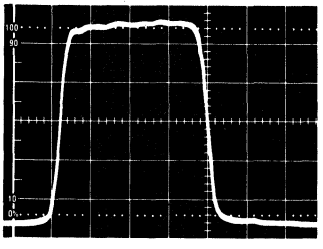
Bandwidth vs. V_{CC}



Output Voltage vs. V_{CC}

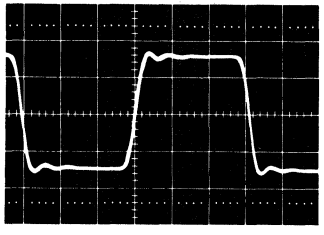


Bandwidth vs. Load



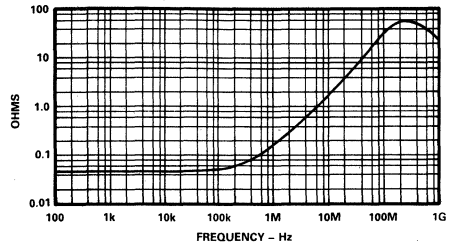
GAIN = –10; 136mV/DIV; 10ns/DIV

AD9610 Small-Signal Pulse Response

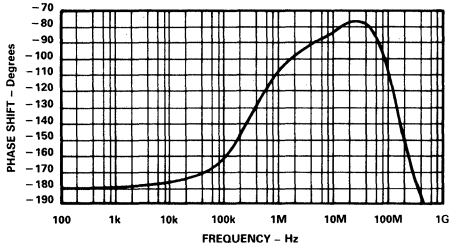


GAIN = –10; 3.4V/DIV; 10ns/DIV

AD9610 Large-Signal Pulse Response

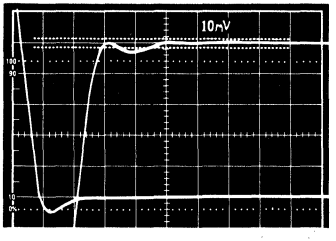


Small-Signal Output Resistance vs. Frequency (G = –10)



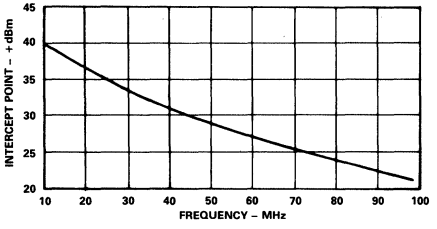
Small-Signal Output Phase Shift vs. Frequency (G = –10)

Information in graphs above can be used to obtain effective output impedance versus frequency.



GAIN = –10; 5V OUTPUT; ERROR WINDOW (±5mV) = 0.1%; 5ns/DIV

AD9610 Settling Time



Two-Tone, 3rd Order IMD Intercept (G = –5; R_L = 50Ω)

ORDERING INFORMATION

Three models of the AD9610 Operational Amplifier are available. The AD9610BH is specified for operation over a case temperature range of –25°C to +85°C; the AD9610TH is intended for applications in which case temperature may be between –55°C and +125°C. Specifications for the AD9610TH and the AD9610TH/883B are the same; the latter unit is processed per MIL-STD-883B.

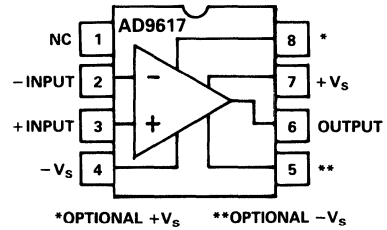
Low Distortion, Precision, Wide Bandwidth Op Amp

AD9617*

FEATURES
Usable Closed-Loop Gain Range: ±1 to ±40
Low Distortion: −67 dBc (2nd) at 20 MHz
Small Signal Bandwidth: 190 MHz (A_V = +3)
Large Signal Bandwidth: 150 MHz at 4 V p-p
Settling Time: 10 ns to 0.1%; 14 ns to 0.02%
Overdrive and Output Short Circuit Protected
Fast Overdrive Recovery
DC Nonlinearity 10 ppm

APPLICATIONS
Driving Flash Converters
D/A Current-to-Voltage Converters
IF, Radar Processors
Baseband and Video Communications
Photodiode, CCD Preamps

AD9617 PIN CONFIGURATION



NOTE: FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

GENERAL DESCRIPTION

The AD9617 is a current feedback amplifier which utilizes a proprietary architecture to produce superior distortion and dc precision. It achieves this along with fast settling, very fast slew rate, wide bandwidth (both small signal and large signal) and exceptional signal fidelity. The device achieves −67 dBc 2nd harmonic distortion at 20 MHz while maintaining 190 MHz small signal and 150 MHz large signal bandwidths.

These attributes position the AD9617 as an ideal choice for driving flash ADCs and buffering the latest generation of DACs. Optimized for applications requiring gain between ±1 to ±15, the AD9617 is unity gain stable without external compensation.

Additional benefits of the AD9617B and T grades include input offset voltage of 500 μV and temperature coefficient (TC) of 3 μV/°C. These accuracy performance levels make the AD9617 an excellent choice for driving emerging high resolution (12–16 bits), high speed analog-to-digital converters and flash converters.

The AD9617 offers outstanding performance in high fidelity, wide bandwidth applications in instrumentation ranging from network and spectrum analyzers to oscilloscopes and in military systems such as radar, SIGINT, and ESM systems. The superior slew rate, low overshoot and fast settling of the AD9617 allow the device to be used in pulse applications such as communications receivers and high speed ATE. Most monolithic op amps suffer in these precision pulse applications due to slew rate limiting.

The AD9617 is available in five performance grades and three package styles. The AD9617J operates over the range of 0 to +70°C and is available in either an 8-pin plastic mini-DIP or an 8-lead plastic small outline package (SOIC). The AD9617A and B versions are rated over the industrial temperature range of −40°C to +85°C. The AD9617S and T versions are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B. A, B, S and T grades are available in 8-pin hermetic ceramic DIPs and 8-pin hermetic ceramic surface mount gull-wing carriers.

*Patent pending.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Common Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 3 V
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9617JN/JR . . . . . 0 to +70°C
AD9617AQ/BQ . . . . . −40°C to +85°C
AD9617SQ/TQ/SZ/TZ/883B* . . . . . −55°C to +125°C
Storage Temperature
AD9617JN/JR . . . . . −65°C to +125°C
AD9617AQ/BQ/SQ/TQ/SZ/TZ/883B* . . . −65°C to +150°C
Junction Temperature[3]
AD9617JN/JR . . . . . 150°C
AD9617AQ/BQ/SQ/TQ/SZ/TZ/883B* . . . . . 175°C
Lead Soldering Temperature (10 Seconds) . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $A_V = +3$; $\pm V_S = \pm 5$ V; $R_F = 400\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	Mil Sub[4]	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/ SQ/SZ/883B* Min	AD9617AQ/ SQ/SZ/883B* Typ	AD9617AQ/ SQ/SZ/883B* Max	AD9617BQ/ TQ/TZ/883B* Min	AD9617BQ/ TQ/TZ/883B* Typ	AD9617BQ/ TQ/TZ/883B* Max	Units
Input Offset Voltage[5, 6]		+25°C	I	1	−1.1	+0.5	+2.2	−1.1	+0.5	+2.2	+0.0	+0.5	+1.1	mV
Input Offset Voltage TC[6]		Full	IV		−4	+3	+25	−4	+3	+25	−4	+3	+25	µV/°C
Input Bias Current[6]														
Inverting		+25°C	I	1	−50	0	+50	−50	0	+50	−25	0	+25	µA
Noninverting		+25°C	I	1	−25	+5	+35	−25	+5	+35	−15	+5	+20	µA
Input Bias Current TC[6]														
Noninverting		Full	IV		−50	+30	+125	−50	+30	+125	−50	+30	+125	nA/°C
Inverting		Full	IV		−50	+50	+150	−50	+50	+150	−50	+50	+150	nA/°C
Input Resistance														
Noninverting		+25°C	V			60			60			60		kΩ
Input Capacitance														
Noninverting		+25°C	V			1.5			1.5			1.5		pF
Common Mode Input Range	$T = T_{max}$	←	II	2	±1.4	±1.5		±1.4	±1.5		±1.4	±1.5		V
	$T = T_{min}$ to +25°C	←	II	1, 3	±1.7	±1.8		±1.7	±1.8		±1.7	±1.8		V
Common Mode Rejection Ratio		Full	II	4, 5, 6	50	60		50	60		50	60		dB
Power Supply Rejection Ratio	$\Delta V_S = \pm 5\%$	Full	II	4, 5, 6	50	60		50	60		50	60		dB
Open Loop Gain														
T_O	At dc	+25°C	V			500			500			500		kΩ
Nonlinearity	At dc	+25°C	IV			10			10			10		ppm
Output Voltage Range		+25°C	II		±3.4	±3.8		±3.4	±3.8		±3.4	±3.8		V
Output Impedance	At dc	+25°C	V			0.07			0.07			0.07		Ω
Output Current (50 Ω Load)	$T = +25°C$ to T_{max}	←	II	1, 2	60			60			60			mA
	$T = T_{min}$	←	II	3	50			50			50			mA

AC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $A_V = +3$; $\pm V_S = \pm 5$ V; $R_F = 400\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	Mil Sub[4]	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/ SQ/SZ/883B* Min	AD9617AQ/ SQ/SZ/883B* Typ	AD9617AQ/ SQ/SZ/883B* Max	AD9617BQ/ TQ/TZ/883B* Min	AD9617BQ/ TQ/TZ/883B* Typ	AD9617BQ/ TQ/TZ/883B* Max	Units
FREQUENCY DOMAIN														
Bandwidth (−3 dB)														
Small Signal	$V_{OUT} \leq 2$ V p-p	Full	II	4, 5, 6	145	190		145	190		145	190		MHz
Large Signal	$V_{OUT} = 4$ V p-p	Full	IV			150		115	150		115	150		MHz
Bandwidth Variation vs. A_V	$A_V = -1$ to ±15	+25°C	V			40			40			40		MHz
Amplitude of Peaking (<50 MHz)	$T = T_{min}$ to +25°C	←	II	4, 5, 6		0			0	0.3		0	0.3	dB
	$T = T_{max}$	←	II	4, 5, 6		0			0	0.6		0	0.6	dB
Amplitude of Peaking (>50 MHz)	$T = T_{min}$ to +25°C	←	II	4, 5, 6		0			0	0.8		0	0.8	dB
	$T = T_{max}$	←	II	4, 5, 6		0			0	1.0		0	1.0	dB
Amplitude of Roll-Off (<75 MHz)		Full	II	4, 5, 6		0.1			0.1	0.6		0.1	0.6	dB
Phase Nonlinearity	dc to 75 MHz	+25°C	V			0.5			0.5			0.5		Degree
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV			−86	−78		−86	−78		−86	−78	dBc
	2 V p-p; 20 MHz	Full	IV			−67	−59		−67	−59		−67	−59	dBc
	2 V p-p; 60 MHz	Full	II	4, 5, 6		−51	−43		−51	−43		−51	−43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV			−83	−75		−83	−75		−83	−75	dBc
	2 V p-p; 20 MHz	Full	IV			−69	−61		−69	−61		−69	−61	dBc
	2 V p-p; 60 MHz	Full	II	4, 5, 6		−54	−46		−54	−46		−54	−46	dBc
Input Noise Voltage	10 MHz	+25°C	V			1.2			1.2			1.2		$nV/\sqrt{Hz}$
Inverting Input Noise Current	10 MHz	+25°C	V			29			29			29		$pA/\sqrt{Hz}$
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V			55			55			55		µV, rms

Parameter	Conditions	Temp	Test Level	Mil Sub[4]	AD9617JN/JR Min Typ Max	AD9617AQ/ SQ/SZ/883B* Min Typ Max	AD9617BQ/ TQ/TZ/883B* Min Typ Max	Units
TIME DOMAIN								
Slew Rate	V_{OUT} = 4 V Step	Full	IV		1400	1100 1400	1100 1400	V/μs
Rise/Fall Time								
V_{OUT} = 2 V Step		Full	IV		2.0	2.0 2.5	2.0 2.5	ns
V_{OUT} = 4 V Step	T = +25°C to T_{max}	←	IV		2.4	2.4 3.3	2.4 3.3	ns
V_{OUT} = 4 V Step	T = T_{min}	←	IV		2.4	2.4 3.5	2.4 3.5	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		3	3 14	3 14	%
Settling Time								
To 0.1%	V_{OUT} = 2 V Step	Full	IV		10	10 15	10 15	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV		14	14 23	14 23	ns
To 0.1%	V_{OUT} = 4 V Step	Full	IV		11	11 16	11 16	ns
To 0.02%	V_{OUT} = 4 V Step	Full	IV		16	16 24	16 24	ns
2×Overdrive Recovery to								
±2 mV of Final Value	V_{IN} = 1.7 V Step	+25°C	V		50	50	50	ns
Propagation Delay		+25°C	V		2	2	2	ns
Differential Gain[7]		Full	V		<0.01	<0.01	<0.01	%
Differential Phase[7]		Full	V		0.01	0.01	0.01	Degree
POWER SUPPLY REQUIREMENTS								
Quiescent Current								
$+I_S$		Full	II	1, 2, 3	34 48	34 48	34 48	mA
$-I_S$		Full	II	1, 2, 3	34 48	34 48	34 48	mA

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.
[3]Typical thermal impedances (part soldered onto board):
Mini-DIP: θ_{JA} = 140°C/W; θ_{JC} = 30°C/W. Side Brazed/Cerdip: θ_{JA} = 110°C/W; θ_{JC} = 20°C/W. SOIC Package: θ_{JA} = 150°C/W; θ_{JC} = 30°C/W.
Ceramic Gull Wing: θ_{JA} = 120°C/W; θ_{JC} = 20°C/W.
[4]Military subgroups apply only to military qualified devices.
[5]Measured with respect to the inverting input.
[6]Typical is defined as the mean of the distribution.
[7]Frequency = 4.3 MHz; R_L = 150 Ω; A_V = +3.
*Consult factory regarding MIL-883 parts in "Z" packages.
Specifications subject to change without notice.

EXPLANATION OF MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
(5% PDA calculated against Subgroup 1 for high-rel versions.)
Subgroup 2 – Static tests at maximum rated operating temperature.
Subgroup 3 – Static tests at minimum rated operating temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated operating temperature.
Subgroup 6 – Dynamic tests at minimum rated operating temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated operating temperature.
Subgroup 11 – Switching tests at minimum rated operating temperature.
Subgroup 12 – Periodically sample tested.

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C and sample tested at specified temperatures. AC testing of J grade devices done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING INFORMATION

Model	Temperature Range	Package Options[1]
AD9617JN	0 to +70°C	Plastic DIP (N-8)
AD9617JR	0 to +70°C	SOIC (R-8)
AD9617AQ	−40°C to +85°C	Cerdip (Q-8)
AD9617BQ	−40°C to +85°C	Cerdip (Q-8)
AD9617SQ	−55°C to +125°C	Cerdip (Q-8)
AD9617TQ	−55°C to +125°C	Cerdip (Q-8)
AD9617SQ/883B	−55°C to +125°C	Cerdip (Q-8)
AD9617TQ/883	−55°C to +125°C	Cerdip (Q-8)
AD9617SZ*	−55°C to +125°C	Ceramic Gull Wing* (Z-8)
AD9617TZ*	−55°C to +125°C	Ceramic Gull Wing* (Z-8)

NOTES
*Consult factory regarding MIL-883 parts in "Z" packages.
[1]See Section 20 for package outline information.

THEORY OF OPERATION

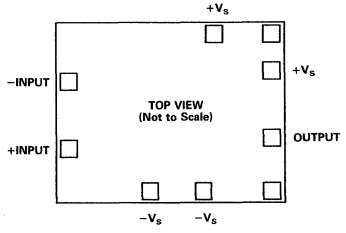
The AD9617 has been designed to combine the key attributes of traditional "low frequency" precision amplifiers with exceptional high frequency characteristics that are independent of closed-loop gain. Previous "high frequency" closed-loop amplifiers have low open loop gain relative to precision amplifiers. This results in relatively poor dc nonlinearity and precision, as well as excessive high frequency distortion due to open loop gain roll-off.

Operational amplifiers use two basic types of feedback correction, each with advantages and disadvantages. Voltage feedback topologies exhibit an essentially constant gain bandwidth product. This forces the closed-loop bandwidth to vary inversely with closed-loop gain. Moreover, this type design typically slew rate limits in a way that causes the large signal bandwidth to be much lower than its small signal characteristics.

A newer approach is to use current feedback to realize better dynamic performance. This architecture provides two key attributes over voltage feedback configurations: (1) avoids slew rate limiting and therefore large signal bandwidth can approach small signal performance; and (2) low bandwidth variation versus gain settings, due to the inherently low open loop inverting input resistance (R_S).

The AD9617 uses a new current feedback topology that overcomes these limitations and combines the positive attributes of both current feedback and voltage feedback designs. These devices achieve excellent high frequency dynamics (slew, BW and distortion) along with excellent low frequency linearity and good dc precision.

DIE CONNECTIONS

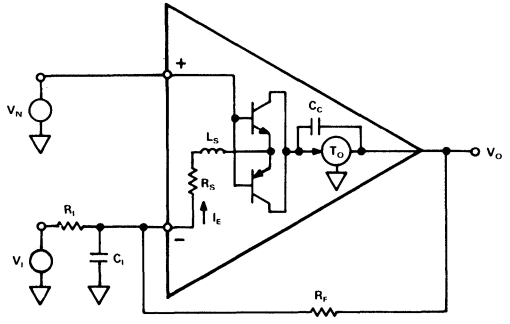


DIE SIZE = 53 × 67 × 15 mils

DC GAIN CHARACTERISTICS

A simplified equivalent schematic is shown below. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to $T_O \times I_E$. Negative feedback is applied through R_F such that the device operates at a gain (G) equal to $-R_F/R_I$.

Noninverting operation is similar, with the input signal applied to the high impedance buffer (noninverting) input. As before, an output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the external gain is $(1+R_F/R_I)$. The feedback mechanics are identical to the voltage feedback topology when exact equations are used.



Equivalent Circuit

The major difference lies in the front end architecture. A voltage feedback amplifier has symmetrical high resistance (buffered) inputs. A current feedback amplifier has a high noninverting resistance (buffered) input and a low inverting (buffer output) input resistance. The feedback mechanics can be easily developed using current feedback and transresistance open loop gain T(s) to describe the I/O relationship. (See typical specification chart.)

DC closed-loop gain for the AD9617 can be calculated using the following equations:

$$G = \frac{V_O}{V_I} \approx \frac{-R_F/R_I}{1 + 1/LG} \quad \text{inverting} \quad (1)$$

$$G = \frac{V_O}{V_N} \approx \frac{1 + R_F/R_I}{1 + 1/LG} \quad \text{noninverting} \quad (2)$$

$$\text{where: } \frac{1}{LG} \approx \frac{R_S(R_F + R_S \| R_I)}{T(s)(R_S \| R_I)} \quad (3)$$

Because the noninverting input buffer is not ideal, input resistance R_S (at dc) is gain dependent and is typically higher for noninverting operation than for inverting operation. R_S will approach the same value (≈7 Ω) for both at input frequencies above 50 MHz. Below the open loop corner frequency, the noninverting R_S can be approximated as:

$$R_S \text{ (noninverting)} \approx 7 + \frac{T(s)}{A_O} = 7 + \frac{T_O}{A_O}\bigg|_{dc} \quad (4)$$

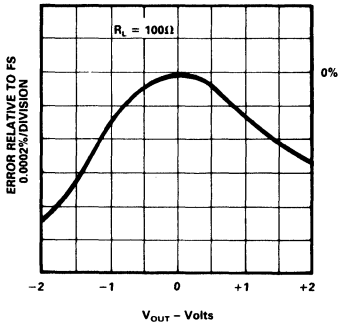
where: A_O = *Open Loop Voltage Gain* ≈ $G \times 600$

Inverting R_S below the open loop corner frequency can be approximated as:

$$R_S \text{ (inverting)} \approx 7 + \frac{T(s)}{A_O} = 7 + \frac{T_O}{A_O}\bigg|_{dc} \quad (5)$$

where: A_O = 40,000.

The AD9617 approaches this condition. With $T_O = 1 \times 10^6$ Ω, R_L = 500 Ω and R_S = 25 Ω (dc), a gain error no greater than 0.05% typically results for G = −1 and 0.15% for G = −40. Moreover, the architecture linearizes the open loop gain over its operating voltage range and temperature resulting in ≥16 bits of linearity.



DC Nonlinearity vs. V_{OUT}

AC GAIN CHARACTERISTICS

Closed-loop bandwidth at high frequencies is determined primarily by the roll-off of T(s). But circuit layout is critical to minimize external parasitics which can degrade performance by causing premature peaking and/or reduced bandwidth.

The inverting and noninverting dynamic characteristics are similar. When driving the noninverting input, the inverting input capacitance (C_I) will cause the noninverting closed-loop bandwidth to be higher than the inverting bandwidth for gains less than two (2). In the remaining cases, inverting and noninverting responses are nearly identical.

For best overall dynamic performance, the value of the feedback resistor (R_F) should be 400 ohms. Although bandwidth reduces as closed-loop gain increases, the change is relatively small due to low equivalent series input impedance, Z_S. (See typical performance charts.) The simplified equations governing the device's dynamic performance are shown below.

Closed-Loop Gain vs. Frequency:
(noninverting operation)

$$\frac{V_O}{V_S} \approx \frac{1 + \frac{R_F}{R_I}}{s\tau\left(1 + \frac{R_S}{R_I}\right) + 1} \quad (6)$$

where: $\tau = R_F \times C_C = 0.9\ ns (R_F = 400\ \Omega)$

$$\text{Slew Rate} \approx \frac{\Delta V_O}{R_F K C_C} \times e^{-\tau/R_F K C_C} \quad (7)$$

where: $K = 1 + \frac{R_S}{R_I}$

Increasing Bandwidth at Low Gains

By reducing R_F, wider bandwidth and faster pulse response can be attained beyond the specified values, although increased overshoot, settling time and possible ac peaking may result. As a rule of thumb, overshoot and bandwidth will increase by 1% and 8%, respectively, for a 5% reduction in R_F at gains of ±10. Lower gains will increase these sensitivities.

Equations 6 and 7 are simplified and do not accurately model the second order (open loop) frequency response term which is the primary contributor to overshoot, peaking and nonlinear bandwidth expansion. (See Open Loop Bode Plots.) The user should exercise caution when selecting R_F values much lower than 400 Ω. Note that a feedback resistor must be used in all situations, including those in which the amplifier is used in a noninverting unity gain configuration.

Increasing Bandwidth at High Gains

Closed loop bandwidth can be extended at high closed loop gain by reducing R_F. Bandwidth reduction is a result of the feedback current being split between R_S and R_I. As the gain increases (for a given R_F), more feedback current is shunted through R_I, which reduces closed loop bandwidth (see Equation 6). To maintain specified BW, the following equations can be used to approximate R_F and R_I for any gain from ±1 to ±15.

$$R_F = 424 \pm 8G \quad (8)$$

(+ for inverting and − for noninverting)

$$R_I \approx \frac{424 - 8G}{G - 1} \quad \text{(noninverting)} \quad (9)$$

$$R_I \approx \frac{424 + 8G}{G} \quad \text{(inverting)} \quad (10)$$

G = *Closed Loop Gain.*

Bandwidth Reduction

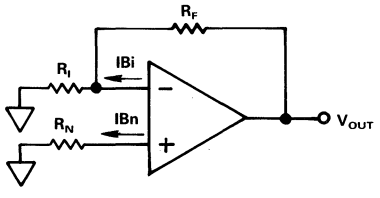
The closed loop bandwidth can be reduced by increasing R_F. Equations 6 and 7 can be used to determine the closed loop bandwidth for any value R_F. Do not connect a feedback capacitor across R_F, as this will degrade dynamic performance and possibly induce oscillation.

DC Precision and Noise

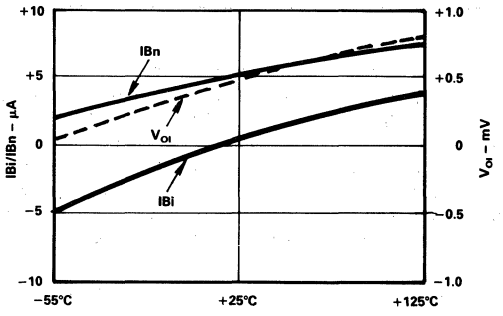
Output offset voltage results from both input bias currents and input offset voltage. These input errors are multiplied by the noise gain term $(1 + R_F/R_I)$ and algebraically summed at the output as shown below.

$$V_O = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm IBn \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm IBi \times R_F \quad (11)$$

Since the inputs are asymmetrical, IBi and IBn do not correlate. Canceling their output effects by making $R_N = R_F \| R_I$ will not reduce output offset errors, as it would for voltage feedback



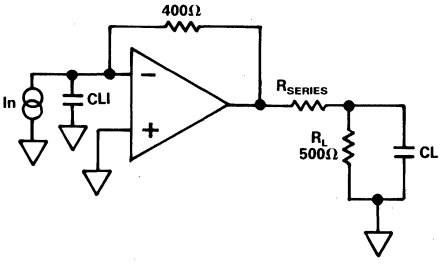
Output Offset Voltage



DC Accuracy

amplifiers. Typically, IBn is 5 µA and V_{IO} is +0.5 mV (1 sigma = 0.3 mV), which means that the dc output error can be reduced by making $R_N \approx 100$ Ω. Note that the offset drift will not change significantly because the IBn TC is relatively small. (See specification table.)

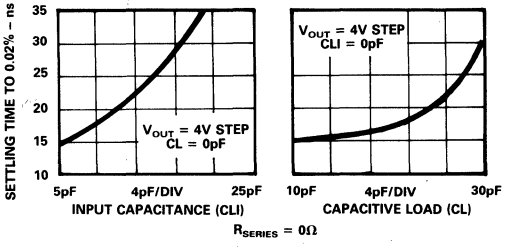
The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of Equation 11 and applying the spectral noise values found in the typical graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed loop gain is increased (by keeping R_F fixed and reducing R_I with $R_N = 0$ Ω).



Capacitive Load Figure

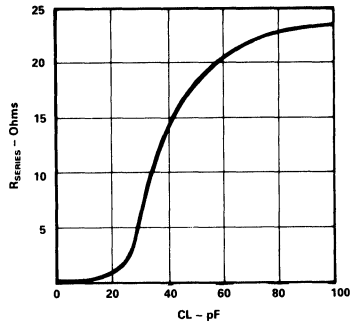
Capacitive Load Considerations

Due to the low inverting input resistance (R_S) and output buffer design, the AD9617 can directly handle input and/or output load capacitances of up to 20 pF. See the chart below.



Input/Output Capacitance Comparisons

A small series resistor can be used at the output of the amplifier and outside of the feedback loop to facilitate driving larger capacitive loads or for obtaining faster settling time. For capacitive loads above 20 pF, R_{SERIES} should be considered.



Recommended R_{SERIES} vs. CL

APPLYING THE AD9617

The superior frequency and time domain specifications of the AD9617 make it an obvious choice for driving flash converters and buffering the outputs of high speed DACs. Its outstanding distortion and noise performance make it well suited as a driver for analog to digital converters (ADCs) with resolutions as high as 16 bits.

Typical circuits for inverting and noninverting applications are shown in Figures 1 and 2.

Closed-loop gain for noninverting configurations is determined by the value of R_I according to the equation:

$$G = 1 + \frac{R_F}{R_I} \qquad (12)$$

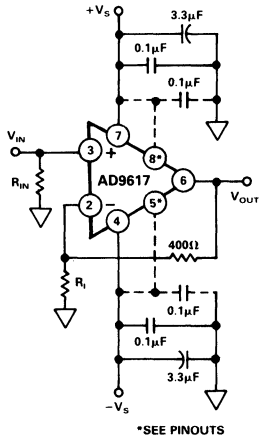


Figure 1. Noninverting Operation

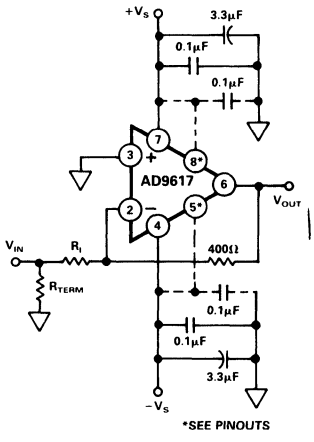


Figure 2. Inverting Operation

To preserve the amplifier's full bandwidth, the noninverting input should be driven from a low impedance source. To obtain a gain of +1, a feedback resistor must be used or device reliability will be diminished.

A recommended circuit for an inverting amplification is shown in Figure 2.

Closed-loop gain for inverting configurations is determined by the value of R_I per the following equation:

$$G = -\frac{R_F}{R_I} \qquad (13)$$

LAYOUT CONSIDERATIONS

As with all high performance amplifiers, printed circuit layout is critical in obtaining optimum results with the AD9617. The ground plane in the area of the amplifier should cover as much of the component side of the board as possible. Each power supply trace should be decoupled close to the package with at least a 3.3 µF tantalum and a low inductance, 0.1 µF ceramic capacitor.

All lead lengths for input, output and the feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

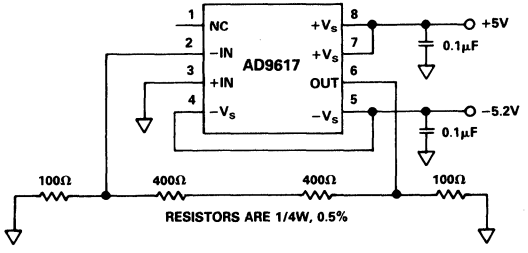
Stripline techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if possible because of their stray inductance and capacitance. If sockets are necessary, individual pin sockets such as AMP p/n 6–330808–3 should be used. These contribute far less stray reactance than molded socket assemblies.

An evaluation board is available from Analog Devices at nominal cost.

COMPLIANCE INFORMATION

The AD9617SQ/SZ/TQ/TZ/883B* devices are classified within Microcircuits Group 49,Technology Group D (operational amplifiers) and are constructed in accordance with MIL-STD-883. They are electrostatic sensitive and fall within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

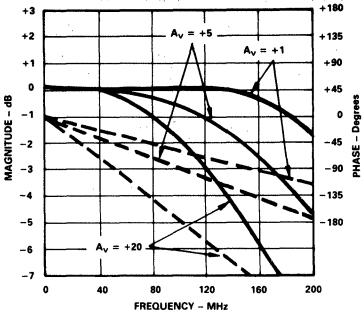
The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.



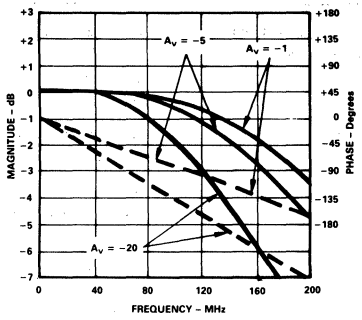
AD9617 Burn-In Circuit

*Consult factory regarding MIL-883 parts in "Z" packages.

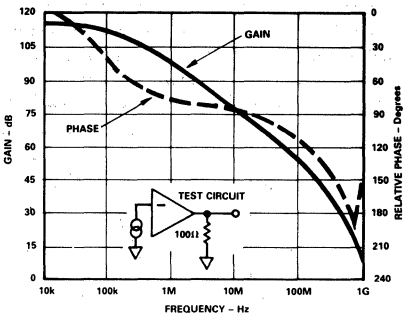
Typical Performance (A_V = +3; $\pm V_S$ = ±5 V; R_F = 400 Ω, unless otherwise noted)



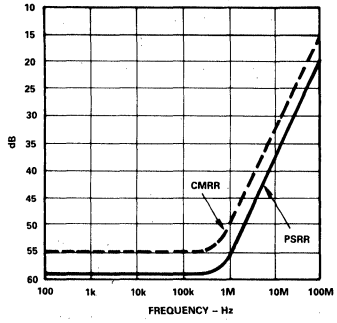
Noninverting Frequency Response



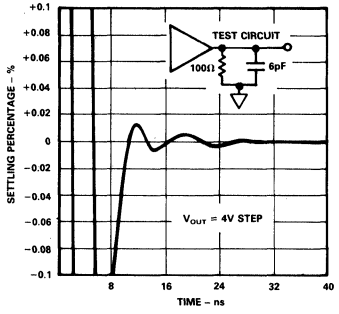
Inverting Frequency Response



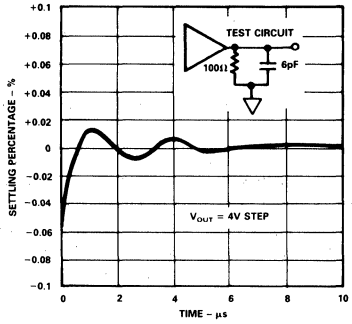
Open Loop Transimpedance Gain [T(s) Relative to 1Ω]



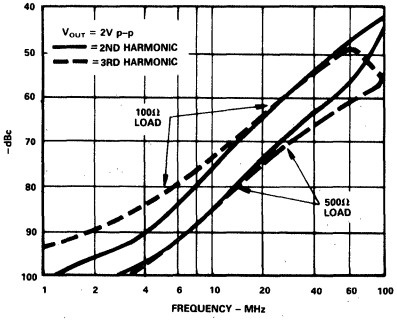
CMRR and PSRR



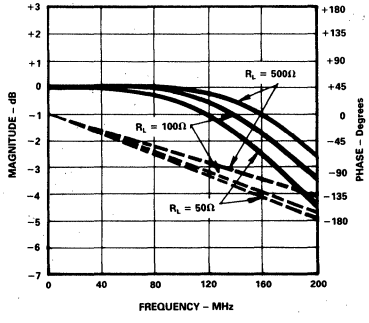
Settling Time



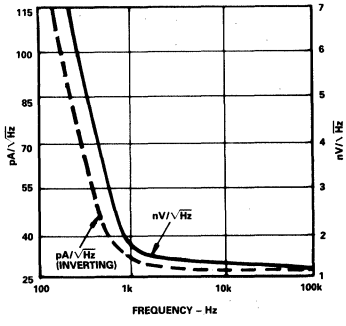
Long Term Settling Time



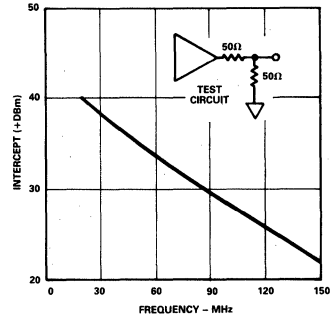
Harmonic Distortion



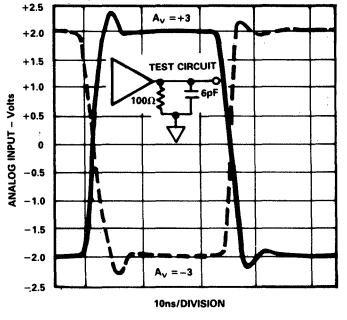
Frequency Response vs. R_{LOAD}



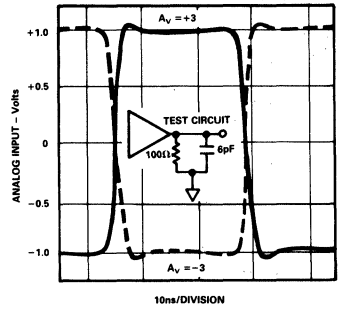
Equivalent Input Noise



Intermodulation Distortion (IMD)



Large Signal Pulse Response



Small Signal Pulse Response

ANALOG DEVICES

Low Distortion, Precision, Wide Bandwidth Op Amp

AD9618*

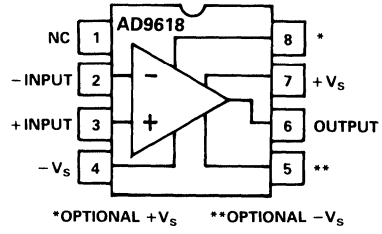
FEATURES

Usable Closed-Loop Gain Range: +5/−1 to ±100
Low Distortion: −63 dBc (2nd) at 20 MHz
Small Signal Bandwidth: 160 MHz (A_V = +10)
Large Signal Bandwidth: 150 MHz at 5 V p–p
Settling Time: 10 ns to 0.1%; 14 ns to 0.02%
Overdrive and Output Short Circuit Protected
Fast Overdrive Recovery
DC Nonlinearity 5 ppm

APPLICATIONS

Driving Flash Converters
D/A Current to Voltage Converters
IF, Radar Processors
Baseband and Video Communications
Photodiode, CCD Preamps

AD9618 PIN CONFIGURATION



*OPTIONAL +V_S **OPTIONAL −V_S

NOTE: FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

GENERAL DESCRIPTION

The AD9618 is a current feedback amplifier which utilizes a proprietary architecture to produce superior distortion and dc precision. It achieves this along with fast settling, very fast slew rate, wide bandwidth (both small signal and large signal), and exceptional signal fidelity. The device achieves −63 dBc 2nd harmonic distortion at 20 MHz while maintaining 160 MHz small signal and 150 MHz large signal bandwidths.

These attributes position the AD9618 as an ideal choice for driving flash ADCs and buffering the latest generation of DACs. Optimized for applications requiring gain between +5/−1 to ±40, the AD9618 is unity gain stable without external compensation.

Additional benefits of the AD9618B and T grades include input offset voltage of 500 μV and temperature coefficient (TC) of 3 μV/°C. These accuracy performance levels make the AD9618 an excellent choice for driving emerging high resolution (12–16 bits), high speed analog to digital converters and flash converters.

The AD9618 offers outstanding performance in high fidelity, wide bandwidth applications in instrumentation ranging from network and spectrum analyzers to oscilloscopes, and in military systems such as radar, SIGINT, and ESM systems. The superior slew rate, low overshoot, and fast settling of the AD9618 allow the device to be used in pulse applications such as communications receivers and high speed ATE. Most monolithic op amps suffer in these precision pulse applications due to slew rate limiting.

The AD9618 is available in five performance grades and three package styles. The AD9618J operates over the range of 0 to +70°C and is available in either an 8-pin plastic mini-DIP or an 8 lead plastic small outline package (SOIC). The AD9618A and B versions are rated over the industrial temperature range of −40°C to +85°C. The AD9618S and T versions are rated over the military temperature range of −55°C to +125°C; and are available processed to MIL-STD-883B. A, B, S and T grades are available in 8-pin hermetic ceramic DIPs and 8-pin hermetic surface mount gull-wing carriers.

*Patent pending.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ± 7 V
Common Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 3 V
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9618JN/JR . . . . . 0 to +70°C
AD9618AQ/BQ . . . . . −40°C to +85°C
AD9618SQ/TQ/SZ/TZ/883B* . . . . . −55°C to +125°C
Storage Temperature
AD9618JN/JR . . . . . −65°C to +125°C
AD9618AQ/BQ/SQ/TQ/SZ/TZ/883B* . . . . −65°C to +150°C
Junction Temperature[3]
AD9618JN/JR . . . . . 150°C
AD9618AQ/BQ/SQ/TQ/SZ/TZ/883B* . . . . . 175°C
Lead Soldering Temperature (10 Seconds) . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $A_V = +10$; $\pm V_S = \pm 5$ V; $R_F = 1000\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	Mil Sub[4]	AD9618JN/JR Min	Typ	Max	AD9618AQ/ SQ/SZ/883B* Min	Typ	Max	AD9618BQ/ TQ/TZ/883B* Min	Typ	Max	Units
Input Offset Voltage[5, 6]		+25°C	I	1	−1.1	+0.5	+2.2	−1.1	+0.5	+2.2	0.0	+0.5	+1.1	mV
Input Offset Voltage TC[6]		Full	IV		−4	+3	+25	−4	+3	+25	−4	+3	+25	µV/°C
Input Bias Current[6]														
Inverting		+25°C	I	1	−45	0	+45	−45	0	+45	−20	0	+20	µA
Noninverting		+25°C	I	1	−25	+5	+35	−25	+5	+35	−13	+5	+18	µA
Input Bias Current TC[6]														
Noninverting		Full	IV		−50	+30	+125	−50	+30	+125	−50	+30	+125	nA/°C
Inverting		Full	IV		−50	+40	+130	−50	+40	+130	−50	+40	+130	nA/°C
Input Resistance														
Noninverting		+25°C	V			75			75			75		kΩ
Input Capacitance														
Noninverting		+25°C	V			1.5			1.5			1.5		pF
Common Mode Input Range	$T = T_{max}$	←	II	2	±1.0	±1.2		±1.0	±1.2		±1.0	±1.2		V
	$T = T_{min}$ to +25°C	←	II	1, 3	±1.4	±1.5		±1.4	±1.5		±1.4	±1.5		V
Common Mode Rejection Ratio		Full	II	4, 5, 6	50	60		50	60		50	60		dB
Power Supply Rejection Ratio	$\Delta V_S = \pm 5\%$	Full	II	4, 5, 6	50	60		50	60		50	60		dB
Open Loop Gain														
T_O	At dc	+25°C	V			3			3			3		MΩ
Nonlinearity	At dc	+25°C	V			5			5			5		ppm
Output Voltage Range		+25°C	II		±3.3	±3.7		±3.3	±3.7		±3.3	±3.7		V
Output Impedance	At dc	+25°C	V			0.08			0.08			0.08		Ω
Output Current (50 Ω Load)	$T = +25°C$ to T_{max}	←	II	1, 2	60			60			60			mA
	$T = T_{min}$	←	II	3	50			50			50			mA

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $A_V = +10$; $\pm V_S = \pm 5$ V; $R_F = 1$ kΩ; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	Mil Sub[4]	AD9618JN/JR Min	Typ	Max	AD9618AQ/ SQ/SZ/883B* Min	Typ	Max	AD9618BQ TQ/TZ/883B* Min	Typ	Max	Units
FREQUENCY DOMAIN														
Bandwidth (−3 dB)														
Small Signal	$V_{OUT} \le 2$ V p–p	Full	II	4, 5, 6	130	160		130	160		130	160		MHz
Large Signal	$V_{OUT} \le 5$ V p–p	Full	IV			150		120	150		120	150		MHz
Bandwidth Variation vs. A_V	$A_V = -1$ to ±40	+25°C	V			35			35			35		MHz
Amplitude of Peaking (<50 MHz)	$T = T_{min}$ to +25°C	←	II	4, 5, 6		0			0	0.4		0	0.4	dB
	$T = T_{max}$	←	II	4, 5, 6		0			0	0.7		0	0.7	dB
Amplitude of Peaking (>50 MHz)	$T = T_{min}$ to +25°C	←	II	4, 5, 6		0			0	0.6		0	0.6	dB
	$T = T_{max}$	←	II	4, 5, 6		0			0	1.2		0	1.2	dB
Amplitude of Roll-Off (<75 MHz)		Full	II	4, 5, 6		0.5			0.5	1.2		0.5	1.2	dB
Phase Nonlinearity	dc to 75 MHz	+25°C	V			0.5			0.5			0.5		Degree
2nd Harmonic Distortion	2 V p–p; 4.3 MHz	Full	IV			−83	−75		−83	−75		−83	−75	dBc
	2 V p–p; 20 MHz	Full	IV			−63	−55		−63	−55		−63	−55	dBc
	2 V p–p; 60 MHz	Full	II	4, 5, 6		−51	−43		−51	−43		−51	−43	dBc
3rd Harmonic Distortion	2 V p–p; 4.3 MHz	Full	IV			−85	−77		−85	−77		−85	−77	dBc
	2 V p–p; 20 MHz	Full	IV			−70	−62		−70	−62		−70	−62	dBc
	2 V p–p; 60 MHz	Full	II	4, 5, 6		−62	−54		−62	−54		−62	−54	dBc
Input Noise Voltage	10 MHz	+25°C	V			1.2			1.2			1.2		$nV/\sqrt{Hz}$
Inverting Input Noise Current	10 MHz	+25°C	V			24			24			24		$pA/\sqrt{Hz}$

Parameter	Conditions	Temp	Test Level	Mil Sub[4]	AD9618JN/JR Min	AD9618JN/JR Typ	AD9618JN/JR Max	AD9618AQ/SQ/SZ/883B* Min	AD9618AQ/SQ/SZ/883B* Typ	AD9618AQ/SQ/SZ/883B* Max	AD9618BQ/TQ/TZ/883B* Min	AD9618BQ/TQ/TZ/883B* Typ	AD9618BQ/TQ/TZ/883B* Max	Units
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V			38			38			38		μV, rms
TIME DOMAIN														
Slew Rate	V_{OUT} = 4 V Step	Full	IV			1800		1400	1800		1400	1800		V/μs
Rise/Fall Time														
V_{OUT} = 2 V Step		Full	IV			2.2			2.2	2.6		2.2	2.6	ns
V_{OUT} = 5 V Step	T = +25°C to	←	IV			2.3			2.3	2.8		2.3	2.8	ns
	T = T_{min}	←	IV			2.3			2.3	3.1		2.3	3.1	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV			2			2	10		2	10	%
Settling Time														
To 0.1%	V_{OUT} = 2 V Step	Full	IV			9			9	15		9	15	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV			14			14	23		14	23	ns
To 0.1%	V_{OUT} = 4 V Step	Full	IV			10			10	16		10	16	ns
To 0.02%	V_{OUT} = 4 V Step	Full	IV			16			16	24		16	24	ns
2×Overdrive Recovery to ±2 mV of Final Value	V_{IN} = 0.6 V Step	+25°C	V			50			50			50		ns
Propagation Delay		+25°C	V			2			2			2		ns
Differential Gain[7]		Full	V			0.01			0.01			0.01		%
Differential Phase[7]		Full	V			0.02			0.02			0.02		Degree
POWER SUPPLY REQUIREMENTS														
Quiescent Current														
$+I_S$		Full	II	1, 2, 3		31	43		31	43		31	43	mA
$-I_S$		Full	II	1, 2, 3		31	43		31	43		31	43	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

[3]Typical thermal impedances (part soldered onto board):
Mini-DIP: θ_{JA} = 140°C/W; θ_{JC} = 30°C/W.
Side Brazed/Cerdip: θ_{JA} = 110°C/W; θ_{JC} = 20°C/W.
SOIC Package: θ_{JA} = 150°C/W; θ_{JC} = 30°C/W.
Ceramic Gull Wing: θ_{JA} = 120°C/W; θ_{JC} = 20°C/W.

[4]Military subgroups apply only to military qualified devices.

[5]Measured with respect to the inverting input.

[6]Typical is defined as the mean of the distribution.

[7]Frequency = 4.3 MHz; R_L = 150 Ω; A_V = +10.

*Contact factory regarding MIL-883 parts in "Z" packages.

Specifications subject to change without notice.

EXPLANATION OF MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
(5% PDA calculated against Subgroup 1 for high-rel versions.)
Subgroup 2 – Static tests at maximum rated operating temperature.
Subgroup 3 – Static tests at minimum rated operating temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated operating temperature.
Subgroup 6 – Dynamic tests at minimum rated operating temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated operating temperature.
Subgroup 11 – Switching tests at minimum rated operating temperature.
Subgroup 12 – Periodically sample tested.

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C and sample tested at specified temperatures. AC testing of J grade devices done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING INFORMATION

Model	Temperature Range	Package Options[1]
AD9618JN	0 to +70°C	Plastic DIP (N-8)
AD9618JR	0 to +70°C	SOIC (R-8)
AD9618AQ	−40°C to +85°C	Cerdip (Q-8)
AD9618BQ	−40°C to +85°C	Cerdip (Q-8)
AD9618SQ	−55°C to +125°C	Cerdip (Q-8)
AD9618TQ	−55°C to +125°C	Cerdip (Q-8)
AD9618SQ/883B	−55°C to +125°C	Cerdip (Q-8)
AD9618TQ/883B	−55°C to +125°C	Cerdip (Q-8)
AD9618SZ*	−55°C to +125°C	Ceramic Gull Wing (Z-8)
AD9618TZ*	−55°C to +125°C	Ceramic Gull Wing (Z-8)

NOTES
*Contact factory regarding MIL-883 parts in "Z" packages.
[1]See Section 20 for package outline information.

THEORY OF OPERATION

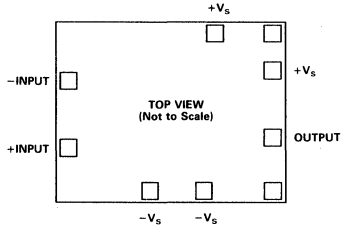
The AD9618 has been designed to combine the key attributes of traditional "low frequency" precision amplifiers with exceptional high frequency characteristics that are independent of closed-loop gain. Previous "high frequency" closed-loop amplifiers have low open loop gain relative to precision amplifiers. This results in relatively poor dc nonlinearity and precision, as well as excessive high frequency distortion due to open loop gain roll-off.

Operational amplifiers use two basic types of feedback correction, each with advantages and disadvantages. Voltage feedback topologies exhibit an essentially constant gain bandwidth product. This forces the closed-loop bandwidth to vary inversely with closed-loop gain. Moreover, this type design typically slew rate limits in a way that causes the large signal bandwidth to be much lower than its small signal characteristics.

A newer approach is to use current feedback to realize better dynamic performance. This architecture provides two key attributes over voltage feedback configurations: (1) avoids slew rate limiting and therefore large signal bandwidth can approach small signal performance; and (2) low bandwidth variation versus gain settings, due to the inherently low open loop inverting input resistance (R_S).

The AD9618 uses a new current feedback topology that overcomes these limitations and combines the positive attributes of both current feedback and voltage feedback designs. These devices achieve excellent high frequency dynamics (slew, BW and distortion) along with excellent low frequency linearity and good dc precision.

DIE CONNECTIONS

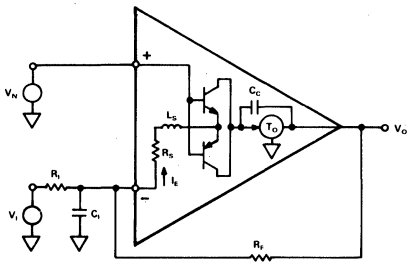


DIE SIZE = 53 × 67 × 15 mils

DC GAIN CHARACTERISTICS

A simplified equivalent schematic is shown below. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to $T_O \times I_E$. Negative feedback is applied through R_F such that the device operates at a gain (G) equal to $-R_F/R_I$.

Noninverting operation is similar, with the input signal applied to the high impedance buffer (noninverting) input. As before,



Equivalent Circuit

an output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the external gain is $(1+ R_F/R_I)$. The feedback mechanics are identical to the voltage feedback topology when exact equations are used.

The major difference lies in the front end architecture. A voltage feedback amplifier has symmetrical high resistance (buffered) inputs. A current feedback amplifier has a high noninverting resistance (buffered) input and a low inverting (buffer output) input resistance. The feedback mechanics can be easily developed using current feedback and transresistance open loop gain T(s) to describe the I/O relationship. (See typical specification chart.)

DC closed-loop gain for the AD9618 can be calculated using the following equations:

$$G = \frac{V_O}{V_I} \approx \frac{-R_F/R_I}{1 + 1/LG} \quad \text{inverting} \quad (1)$$

$$G = \frac{V_O}{V_N} \approx \frac{1 + R_F/R_I}{1 + 1/LG} \quad \text{noninverting} \quad (2)$$

$$\text{where: } \frac{1}{LG} \approx \frac{R_S(R_F + R_S \| R_I)}{T(s)(R_S \| R_I)} \quad (3)$$

Because the noninverting input buffer is not ideal, input resistance R_S (at dc) is gain dependent and is typically higher for noninverting operation than for inverting operation. R_S will approach the same value ($\approx$9 Ω) for both at input frequencies above 50 MHz. Below the open loop corner frequency, the noninverting R_S can be approximated as:

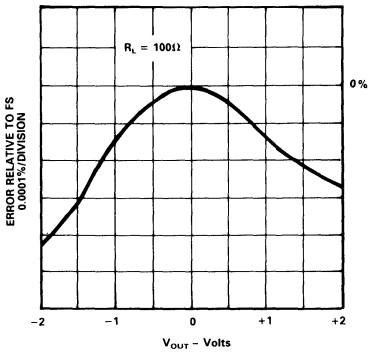
$$R_S \text{ (noninverting)} \approx 9 + \frac{T(s)}{A_O} = 9 + \left.\frac{T_O}{A_O}\right|_{dc} \quad (4)$$

where: A_O=*Open Loop Voltage Gain* $\approx G \times 350$

Inverting R_S below the open loop corner frequency can be approximated as:

$$R_S \text{ (inverting)} \approx 9 + \frac{T(s)}{A_O} = 9 + \left.\frac{T_O}{A_O}\right|_{dc} \quad (5)$$

where: A_O = *140,000*



DC Nonlinearity vs. V_{OUT}

The AD9618 approaches this condition. With $T_O = 3 \times 10^6$ Ω and $R_S = 32$ Ω (dc), a gain error of 0.04% typically results for G = −1 and 0.11% for G = −100. Moreover, the architecture linearizes the open loop gain over its operating voltage range and temperature resulting in >16 bits of linearity.

AC GAIN CHARACTERISTICS

Closed-loop bandwidth at high frequencies is determined primarily by the roll-off of T(s). But circuit layout is critical to minimize external parasitics which can degrade performance by causing premature peaking and/or reduced bandwidth.

The inverting and noninverting dynamic characteristics are similar. When driving the noninverting input, the inverting input capacitance (C_I) will cause the noninverting closed-loop bandwidth to be higher than the inverting bandwidth for gains less than five (5). In the remaining cases, inverting and noninverting responses are nearly identical.

For best overall dynamic performance, the value of the feedback resistor (R_F) should be 1000 Ω. Although bandwidth reduces as closed-loop gain increases, the change is relatively small due to low equivalent series input impedance, Z_S. (See typical performance charts.) The simplified equations governing the device's dynamic performance are shown below.

Closed-Loop Gain vs. Frequency:
(noninverting operation)

$$\frac{V_O}{V_S} \approx \frac{1 + \frac{R_F}{R_I}}{s\tau\left(1 + \frac{R_S}{R_I}\right) + 1} \quad (6)$$

where: $\tau = R_F \times C_C = 1.0$ *ns* ($R_F = 1$ *kΩ*)

$$\text{Slew Rate} \approx \frac{\Delta V_O}{R_F K C_C} \times e^{-\tau/R_F K C_C} \quad (7)$$

where: $K = 1 + \frac{R_S}{R_I}$

Increasing Bandwidth at Low Gains

By reducing R_F, wider bandwidth and faster pulse response can be attained beyond the specified values, although increased overshoot, settling time, and possible ac peaking may result. As a rule of thumb, overshoot and bandwidth will increase by 1% and 8%, respectively, for a 5% reduction in R_F at gains of ±10.

Equations 6 and 7 are simplified and do not accurately model the second order (open loop) frequency response term which is the primary contributor to overshoot, peaking, and nonlinear bandwidth expansion. (See Open Loop Bode Plots.) The user should exercise caution when selecting R_F values much lower than 1000 Ω. Note that a feedback resistor must be used in all situations.

Increasing Bandwidth at High Gains

Closed-loop bandwidth can be extended at high closed-loop gain by reducing R_F. Bandwidth reduction is a result of the feedback current being split between R_S and R_I. As the gain increases (for a given R_F), more feedback current is shunted through R_I, which reduces closed-loop bandwidth (see Equation 6). To maintain specified BW, the following equations can be used to approximate R_F and R_I for any gain from = +5/−1 to ±40.

$$R_F = 1100 \pm 8G \quad (+ \text{ for inverting and } - \text{ for noninverting}) \tag{8}$$

$$R_I \approx \frac{1100 - 10G}{G - 1} \quad \text{(noninverting)} \tag{9}$$

$$R_I \approx \frac{1100 + 10G}{G} \quad \text{(inverting)} \tag{10}$$

G = *Closed-Loop Gain.*

Bandwidth Reduction

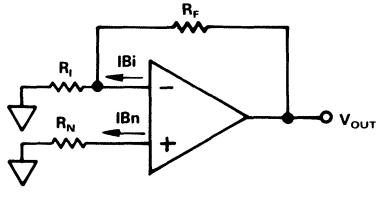
The closed-loop bandwidth can be reduced by increasing R_F. Equations 6 and 7 can be used to determine the closed-loop bandwidth for any value R_F. Do not connect a feedback capacitor across R_F, as this will degrade dynamic performance and possibly induce oscillation.

DC Precision and Noise

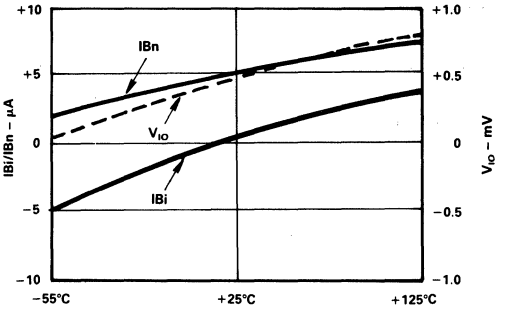
Output offset voltage results from both input bias currents and input offset voltage. These input errors are multiplied by the noise gain term ($1 + R_F/R_I$) and algebraically summed at the output as shown below.

$$V_O = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm IBn \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm IBi \times R_F \tag{11}$$

Since the inputs are asymmetrical, IBi and IBn do not correlate. Canceling their output effects by making $R_N = R_F \| R_I$ will not reduce output offset errors, as it would for voltage feedback amplifiers. Typically, IBn is 5 μA and V_{IO} is +0.5 mV (1 sigma = 0.3 mV), which means that the dc output error can be reduced by making $R_N \approx 100\ \Omega$. Note that the offset drift will not change significantly because the IBn TC is relatively small. (See specification table.)

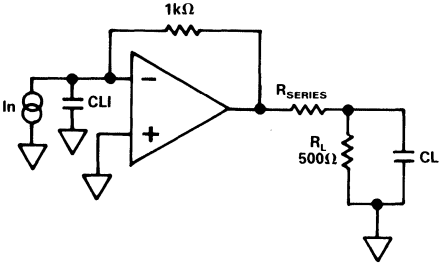


Output Offset Voltage



DC Accuracy

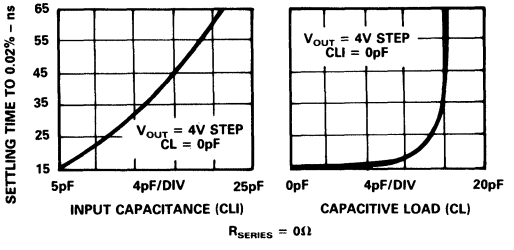
The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of Equation 11 and applying the spectral noise values found in the typical graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltage improve as the closed-loop gain is increased (by keeping R_F fixed and reducing R_I with $R_N = 0\ \Omega$).



Capacitive Load Figure

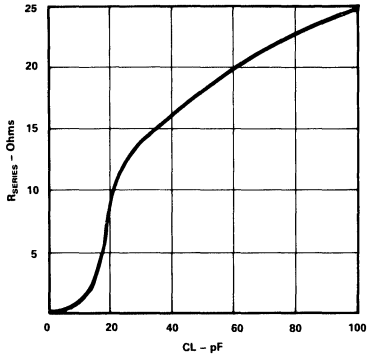
Capacitive Load Considerations

Due to the low inverting input resistance (R_S) and output buffer design, the AD9618 can directly handle input and/or output load capacitances of up to 10 pF. See the chart below.



Input/Output Capacitance Comparisons

A small series resistor can be used at the output of the amplifier and outside of the feedback loop to facilitate driving larger capacitive loads or for obtaining faster settling time. For capacitive loads above 10 pF, R_{SERIES} should be considered.



Recommended R_{SERIES} vs. CL

APPLYING THE AD9618

The superior frequency and time domain specifications of the AD9618 make it an obvious choice for driving flash converters and buffering the outputs of high speed DACs. Its outstanding distortion and noise performance make it well suited as a driver for analog-to-digital converters (ADCs) with resolutions as high as 16 bits.

Typical circuits for inverting and noninverting applications are shown in Figures 1 and 2.

Closed-loop gain for noninverting configurations is determined by the value of R_I according to the equation:

$$G = 1 + \frac{R_F}{R_I} \qquad (12)$$

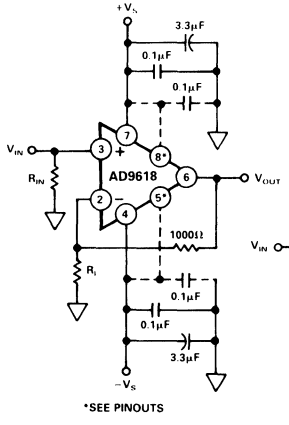


Figure 1. Noninverting Operation

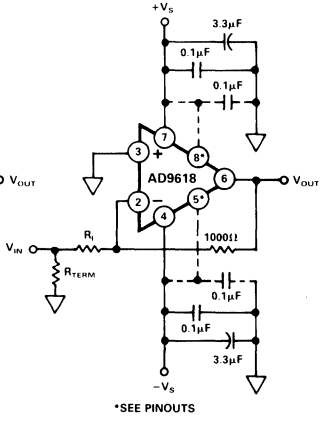


Figure 2. Inverting Operation

To preserve the amplifier's full bandwidth, the noninverting input should be driven from a low impedance source.

A recommended circuit for an inverting amplification is shown in Figure 2.

Closed-loop gain for inverting configurations is determined by the value of R_I per the following equation:

$$G = -\frac{R_F}{R_I} \qquad (13)$$

2

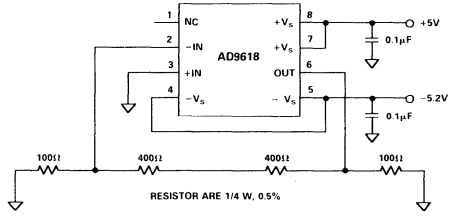
LAYOUT CONSIDERATIONS

As with all high performance amplifiers, printed circuit layout is critical in obtaining optimum results with the AD9618. The ground plane in the area of the amplifier should cover as much of the component side of the board as possible. Each power supply trace should be decoupled close to the package with at least a 3.3 µF tantalum and a low inductance, 0.1 µF ceramic capacitor.

All lead lengths for input, output, and the feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

Stripline techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if possible because of their stray inductance and capacitance. If sockets are necessary, individual pin sockets such as AMP p/n 6-330808-3 should be used. These contribute far less stray reactance than molded socket assemblies.

An evaluation board is available from Analog Devices for a nominal charge.



AD9618 Burn-In Circuit

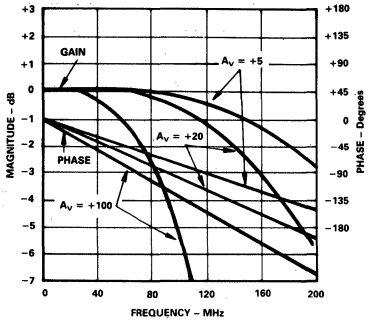
MIL-STD-883 COMPLIANCE INFORMATION

The AD9618SQ/SZ/TQ/TZ/883B* devices are classified within Microcircuits Group 49,Technology Group D (operational amplifiers) and are constructed in accordance with MIL-STD-883. They are electrostatic sensitive and fall within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

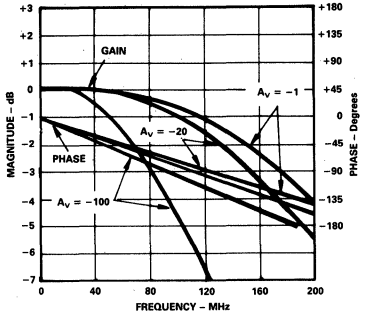
The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.

*Consult factory regarding MIL-883 parts in "Z" packages.

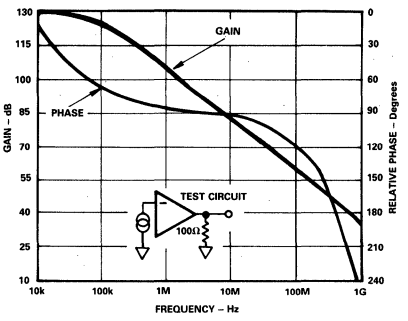
Typical Performance (A_V = +10; $\pm V_S$ = ±5V; R_F = 1 kΩ, unless otherwise noted)



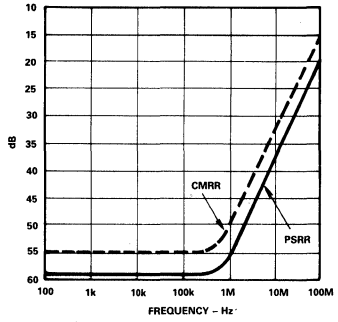
Noninverting Frequency Response



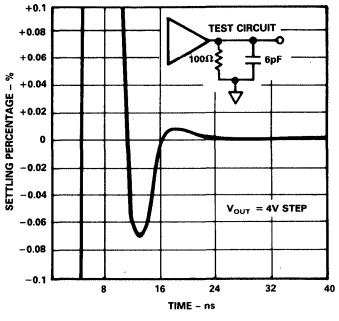
Inverting Frequency Response



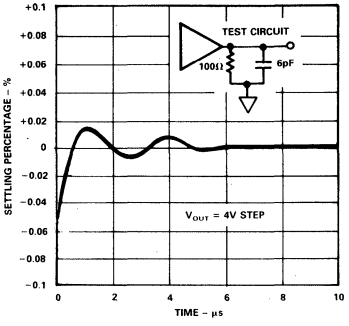
Open-Loop Transimpedance Gain [T(s) Relative to 1 Ω]



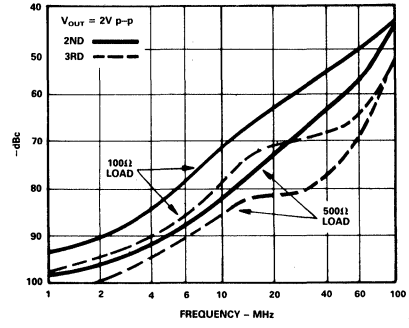
CMRR and PSRR



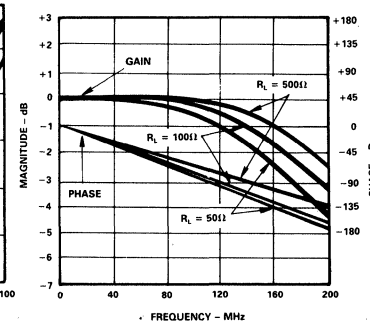
Settling Time



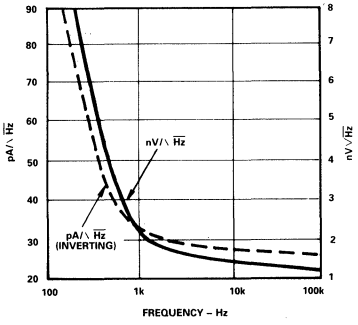
Long Term Settling Time



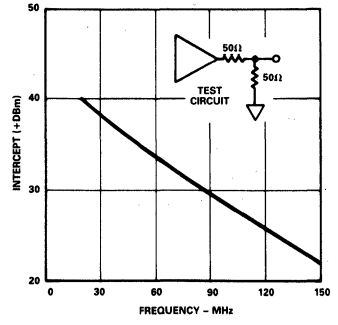
Harmonic Distortion



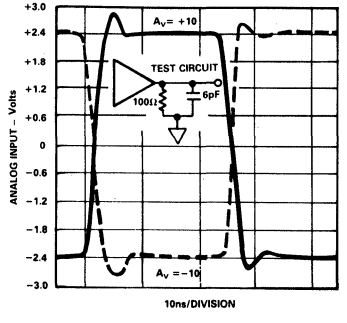
Frequency Response vs. R_{LOAD}



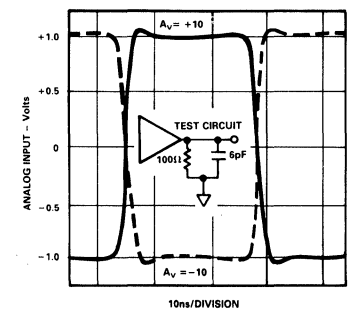
Equivalent Input Noise



Intermodulation Distortion (IMD)



Large Signal Pulse Response



Small Signal Pulse Response

ANALOG DEVICES

Low Distortion, 600 MHz Closed-Loop Buffer Amp

AD9620*

FEATURES
Excellent Gain Accuracy: 0.995 V/V
Wide Bandwidth: 600 MHz
Slew Rate: 2300 V/μs
Ultralow Distortion
−73 dBc @ 20 MHz
−90 dBc @ 2.3 MHz
Fast Settling Time: 8 ns to 0.02%
Low Noise: 2.4 nV/$\sqrt{Hz}$

APPLICATIONS
IF/Communications
Impedance Transformations
Drives Flash ADCs
Line Driving

GENERAL DESCRIPTION

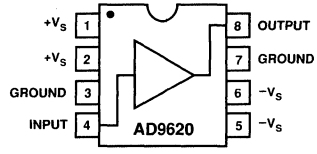
The AD9620 is a monolithic, unity gain buffer amplifier that sets new standards in gain accuracy, wide bandwidth and low distortion. Its large signal bandwidth, ultralow distortion over frequency, and drive capabilities of the AD9620 make this buffer an ideal driver for flash ADCs. Other applications which require increased current drive at unity voltage gain, such as cable driving, also benefit from the AD9620's performance.

In addition to innovative (patent pending) feedback architecture, special packaging techniques improve dynamic performance by minimizing the reactive effects associated with standard packages. The result is −73 dBc harmonic suppression at 20 MHz, and −90 d Bc at 2.3 MHz. The AD9620 also outperforms other amplifiers, including its predecessor AD9630, in terms of small-signal pulse response and dc linearity. These features make the AD9620 the premier driver for high-speed, high-resolution ADCs.

Available in side-brazed ceramic DIP packages, the "A" suffix unit is guaranteed for −40°C to +85°C operating temperatures; the "S" suffix device is guaranteed from −55°C to +125°C. AD9620 die are dc tested at +25°C.

*Patent(s) Pending.

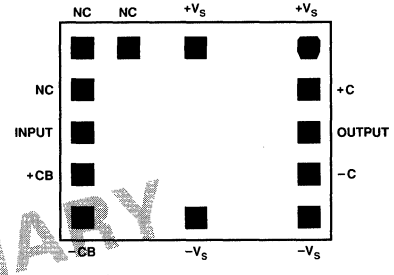
AD9620 PIN CONFIGURATION



NC = NO CONNECT

AD9620 DIE LAYOUT

60 (length) × 50 (width) × 15 (height) mils



ORDERING INFORMATION

Part Number	Temperature Range	Description	Package Option*
AD9620AD	−40°C to +85°C	8-Pin DIP	D-8
AD9620SD	−55°C to +125°C	8-Pin DIP	D-8
AD9620 Chips	+25°C	Die	

*See Section 20 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Input Voltage Range . . . . . $\pm V_S$
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9620AD . . . . . −40°C to +85°C
AD9620SD . . . . . −55°C to +125°C
Storage Temperature
AD9620AD . . . . . −65°C to +150°C
AD9620SD . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10 seconds)[4] . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50\ \Omega$, $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	AD9620AD Min	AD9620AD Typ	AD9620AD Max	AD9620SD Min	AD9620SD Typ	AD9620SD Max	Units
DC SPECIFICATIONS									
Output Offset Voltage		+25°C		±2			±2		mV
Offset Voltage TC		Full		TBD			TBD		µV/°C
Input Bias Current		+25°C		±15			±15		µA
Bias Current TC		Full		TBD			TBD		nA/°C
Input Resistance		+25°C		500			500		kΩ
Input Capacitance		+25°C		1.0			1.0		pF
Gain	V_{OUT} = 2 V p-p	+25°C	TBD	0.995		TBD	0.995		V/V
Output Voltage Range		Full		±2.4			±2.4		V
Output Current (50 Ω Load)		+25°C	TBD	50		TBD	50		mA
Output Impedance	At DC	+25°C		0.4			0.4		Ω
Power Supply Rejection Ratio	ΔV_S = ±5%	Full		65			65		dB
DC Nonlinearity	±2 V Full Scale	+25°C		0.01			0.01		%
FREQUENCY DOMAIN									
Bandwidth (−3 dB)									
Small Signal	V_{OUT} = ≤0.7 V p-p	+25°C		500			500		MHz
Large Signal	V_{OUT} = 4 V p-p	+25°C		150			150		MHz
Amplitude of Peaking	≤150 MHz	Full		0.8			0.8		dB
Amplitude of Rolloff	≤150 MHz	Full		0.3			0.3		dB
Group Delay	DC to 150 MHz	+25°C		0.7			0.7		ns
Phase Nonlinearity	DC to 150 MHz	+25°C		0.7			0.7		Degree
2nd Harmonic Distortion	2 V p-p; 2.3 MHz	Full		−90			−90		dBc
	2 V p-p; 20 MHz	Full		−73			−73		dBc
3rd Harmonic Distortion	2 V p-p; 2.3 MHz	Full		−92			−92		dBc
	2 V p-p; 20 MHz	Full		−78			−78		dBc
	2 V p-p; 60 MHz	T_{max}							dBc
Spectral Input Noise Voltage	10 MHz	+25°C		2.4			2.4		$nV/\sqrt{Hz}$
Integrated Output Noise Voltage	0.1 to 200 MHz	+25°C		32			32		µV
TIME DOMAIN									
Slew Rate	V_{OUT} = 5 V Step	+25°C		2300			2300		V/µs
Rise/Fall Time	V_{OUT} = 1 V Step	+25°C		0.8			0.8		ns
	V_{OUT} = 4 V Step	+25°C		1.5			1.5		ns
Overshoot	V_{OUT} = 2 V Step	Full		3			3		%
Settling Time									
To 0.1%	V_{OUT} = 2 V Step	+25°C		4.5			4.5		ns
To 0.02%	V_{OUT} = 2 V Step	+25°C		8			8		ns
SUPPLY CURRENTS									
I_{CC} ($+I_S$)	V_{CC} = +5 V	Full		38			38		mA
I_{EE} ($-I_S$)	V_{EE} = −5 V	Full		38			38		mA

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected to ground, but not to supplies. Prolonged short circuit to ground may affect device reliability.
[3]Typical side-brazed thermal impedances (part soldered onto board): θ_{JA} = 110°C/W; θ_{JC} = 20°C/W.
Specifications subject to change without notice.

ANALOG DEVICES

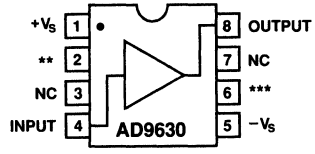
Low Distortion, 750 MHz Closed-Loop Buffer Amp

AD9630*

FEATURES
Excellent Gain Accuracy: 0.99 V/V
Wide Bandwidth: 750 MHz
Slew Rate: 1200 V/μs
Low Distortion
−66 dBc @ 20 MHz
−80 dBc @ 4.3 MHz
Settling Time
5 ns to 0.1%
8 ns to 0.02%
Low Noise: 2.4 nV/√Hz
Improved Source for CLC-110

APPLICATIONS
IF/Communications
Impedance Transformations
Drives Flash ADCs
Line Driving

AD9630 PIN CONFIGURATION



**OPTIONAL $+V_S$ ***OPTIONAL $-V_S$ NC = NO CONNECT

NOTE: FOR BEST SETTLING TIME PERFORMANCE USE OPTIONAL POWER SUPPLIES. ALL SPECIFICATIONS ARE BASED ON USING SINGLE $\pm V_S$ CONNECTIONS EXCEPT FOR SETTLING TIME TO 0.02% AND SMALL SIGNAL S21. CONSULT THE FACTORY FOR VERSIONS WITH OPTIONAL POWER SUPPLY PINS DISCONNECTED INTERNAL TO THE PACKAGE.

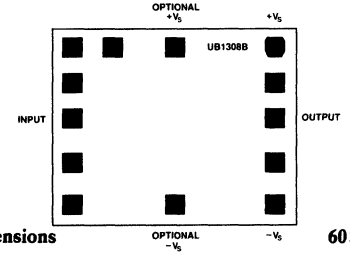
GENERAL DESCRIPTION

The AD9630 is a monolithic buffer amplifier that utilizes innovative (patent pending) closed-loop design techniques to achieve exceptional gain accuracy, wide bandwidth, and low distortion. Slew rate limiting has been overcome as indicated by the 1200 V/μs slew rate; this improvement allows the user greater flexibility in wideband and pulse applications. The second harmonic distortion terms for an analog input tone of 4.3 MHz and 20 MHz are −80 dBc and −66 dBc, respectively. Clearly, the AD9630 establishes a new standard by combining in one part outstanding dc and dynamic performance.

The large signal bandwidth, low distortion over frequency, and drive capabilities of the AD9630 make the buffer an ideal flash ADC driver. The AD9630 provides better signal fidelity than many of the flash ADCs that it has been designed to drive. Other applications which require increased current drive at unity voltage gain such as cable driving benefit from the AD9630's performance.

The AD9630 is available in four 8-pin package styles including Plastic DIP (N), Ceramic DIP (Q), SOIC (R), and Ceramic SOIC (Z). Both Ceramic packages are processed to MIL-STD-883; consult with the factory concerning availability. The "A" grades are guaranteed for −40°C to +85°C; "S" grades are guaranteed from −55°C to +125°C. Die are dc tested at 25°C.

AD9630 DIE LAYOUT



Die Dimensions **60×50×15 mils**

*Patent(s) Pending

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Continuous Output Current[2] . . . . . 70 mA
Temperature Range over Which Specifications Apply
AD9630AN/AR/AQ . . . . . −40°C to +85°C
AD9630SZ/SQ . . . . . −55°C to +125°C
Lead Soldering Temperature (10 sec) . . . . . +300°C
Storage Temperature
AD9630AN/AR . . . . . −65°C to +150°C
AD9630SZ/SQ/AQ . . . . . −65°C to +150°C
Junction Temperature[3]
AD9630AN/AR . . . . . +150°C
AD9630SZ/SQ/AQ . . . . . +175°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50\ \Omega$, $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	Mil Sub[4]	AD9630A/N/R/Q Min	AD9630A/N/R/Q Typ	AD9630A/N/R/Q Max	AD9630S/Q/Z Min	AD9630S/Q/Z Typ	AD9630S/Q/Z Max	Units
DC SPECIFICATIONS											
Output Offset Voltage		+25°C	I	1	−8	±3	+8	−8	±3	+8	mV
Offset Voltage TC		Full	IV		−25	±8	+25	−25	±8	+25	µV/°C
Input Bias Current		+25°C	I	1	−25	±2	+25	−25	±2	+25	µA
Bias Current TC		Full	IV		−100	±20	+100	−100	±20	+100	nA/°C
Input Resistance		+25 to T_{max}	II	1, 2	300	450		300	450		kΩ
Input Resistance		T_{min}	VI	3	150	250		150	250		kΩ
Input Capacitance		+25°C	V			1.0			1.0		pF
Gain	V_{OUT} = 2 V p-p	+25 to T_{max}	II	1, 2	0.983	0.990		0.983	0.990		V/V
Gain	V_{OUT} = 2 V p-p	T_{min}	VI	3	0.980	0.985		0.980	0.985		V/V
Output Voltage Range		Full	VI	1, 2, 3	+3.2	±3.6	−3.2	+3.2	±3.6	−3.2	V
Output Current (50 Ω Load)		+25 to T_{max}	II	1, 2	50			50			mA
Output Current (50 Ω Load)		T_{min}	VI	3	40			40			mA
Output Impedance	At dc	+25°C	V			0.6			0.6		Ω
PSRR	ΔV_S = ±5%	Full	VI	4, 5, 6	44	55		44	55		dB
DC Nonlinearity	±2 V Full Scale	+25°C	V			0.03			0.03		%
FREQUENCY DOMAIN											
Bandwidth (−3 dB)											
Small Signal	$V_O \leq 0.7$ V p-p	T_{min} to 25	II	4, 6	400	750		400	750		MHz
Small Signal	$V_O \leq 0.7$ V p-p	T_{max}	II	5	330	550		330	550		MHz
Large Signal	V_O = 5 V p-p	T_{min} to 25	IV		80	120		80	120		MHz
Large Signal	V_O = 5 V p-p	T_{max}	IV		70	105		70	105		MHz
Output Peaking	≤200 MHz	Full	II	4, 5, 6		0.4	1.2		0.4	1.2	dB
Output Rolloff	≤200 MHz	Full	II	4, 5, 6		0	0.3		0	0.3	dB
Group Delay	dc to 150 MHz	+25°C	V			0.7			0.7		ns
Linear Phase Deviation	dc to 150 MHz	+25°C	V			0.7			0.7		Degrees
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV			−80	−74		−80	−74	dBc
	2 V p-p; 20 MHz	Full	IV			−66	−59		−66	−59	dBc
	2 V p-p; 60 MHz	Full	II	4, 5, 6		−52	−43		−52	−43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV			−86	−79		−86	−79	dBc
	2 V p-p; 20 MHz	Full	IV			−75	−68		−75	−68	dBc
	2 V p-p; 60 MHz	T_{min} to +25	II	4, 6		−50	−43		−50	−43	dBc
	2 V p-p; 60 MHz	T_{max}	II	5		−46	−40		−46	−40	dBc
Spectral Input Noise Voltage	10 MHz	+25°C	V			2.4			2.4		nV/$\sqrt{\text{Hz}}$
Integrated Output Noise	100 kHz – 200 MHz	+25°C	V			32			32		µV
TIME DOMAIN											
Slew Rate	V_{OUT} = 5 V Step	+25°C	IV		800	1200		800	1200		V/µs
Rise/Fall Time	V_{OUT} = 1 V Step	T_{min} to +25	IV			0.9	1.3		0.9	1.3	ns
	V_{OUT} = 1 V Step	T_{max}	IV			1.1	1.6		1.1	1.6	ns
	V_{OUT} = 5 V Step	T_{min} to +25	IV			3.9	5.4		3.9	5.4	ns
	V_{OUT} = 5 V Step	T_{max}	IV			4.5	6.1		4.5	6.1	ns
Overshoot Amplitude	V_{OUT} = 2 V Step	Full	IV			2	12		2	12	%
Settling Time											
To 0.1%	V_{OUT} = 2 V Step	T_{min} to +25	IV			5	8		5	8	ns
To 0.1%	V_{OUT} = 2 V Step	T_{max}	IV			7	12		7	12	ns
To 0.02%	V_{OUT} = 2 V Step	T_{min} to +25	IV			8	13		8	13	ns
To 0.02%	V_{OUT} = 2 V Step	T_{max}	IV			12	18		12	18	ns
Differential Gain	4.4 MHz	+25°C	V			0.015			0.015		%
Differential Phase	4.4 MHz	+25°C	V			0.025			0.025		Degree
SUPPLY CURRENTS											
V_{CC} ($+I_S$)	V_{CC} = +5 V	Full	II	1, 2, 3		19	26		19	26	mA
V_{EE} ($-I_S$)	V_{EE} = −5 V	Full	II	1, 2, 3		19	26		19	26	mA

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected to ground, but not to supplies. Prolonged short circuit to ground may affect device reliability.
[3]Typical thermal impedances (part soldered onto board):
Mini-DIP (N): θ_{JA} = 110°C/W; θ_{JC} = 30°C/W.
Cerdip (Q): θ_{JA} = 110°C/W; θ_{JC} = 20°C/W.
SOIC (R): θ_{JA} = 150°C/W; θ_{JC} = 50°C/W.
Ceramic Gull Wing (Z): θ_{JA} = 100°C/W; θ_{JC} = 20°C/W.
[4]Military subgroups apply only to military qualified devices.

2

EXPLANATION OF TEST LEVELS

Test Level
I 100% Production tested.
II 100% Production tested at +25°C and sample tested at specified temperatures. AC testing of AN and AR grades done on sample basis only.
III Sample tested only.
IV Parameter is guaranteed by design and characterization testing.
V Typical value.
VI S versions are 100% production tested at temperature extremes. Other grades are sample tested at extremes.

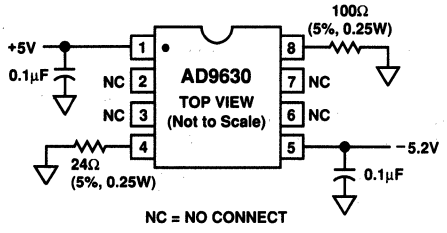
EXPLANATION OF MILITARY SUBGROUPS

Subgroup 1 Static tests at +25°C.
(5% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 Static tests at maximum rated operating temperature.
Subgroup 3 Static tests at minimum rated operating temperature.
Subgroup 4 Dynamic tests at +25°C.
Subgroup 5 Dynamic tests at maximum rated operating temperature.
Subgroup 6 Dynamic tests at minimum rated operating temperature.
Subgroup 7 Functional tests at +25°C.
Subgroup 8 Functional tests at maximum and minimum rated temperatures.
Subgroup 9 Switching tests at +25°C.
Subgroup 10 Switching tests at maximum rated operating temperature.
Subgroup 11 Switching tests at minimum rated operating temperature.
Subgroup 12 Periodically sample tested.

ORDERING INFORMATION

Model	Temperature Range	Description	Package Options*
AD9630AN	−40°C to +85°C	8-Pin Plastic	N-8
AD9630AR	−40°C to +85°C	8-Pin SOIC	R-8
AD9630AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD9630SZ†	−55°C to +125°C	8-Pin Ceramic Gull Wing	Z-8
AD9630SQ†	−55°C to +125°C	8-Pin Cerdip	Q-8
AD9630 Chips	+25°C	Dice	

NOTES
*See Section 20 for package outline information.
†Consult factory about MIL-STD-883 compliant devices.



AD9630 Burn-In Circuit

THEORY OF OPERATION

The AD9630 is a wide-bandwidth, closed-loop, unity-gain buffer which makes use of a new voltage-feedback architecture (Patent Pending). This architecture brings together wide bandwidth and high slew rate along with exceptional dc linearity. Most previous wide bandwidth buffers achieved their bandwidth by utilizing an open-loop topology which sacrificed both dc linearity and frequency distortion when driven into low load impedances. The design's high loop correction factor radically improves dc linearity and distortion characteristics without diminishing bandwidth. This, in combination with high slew rate, results in exceptionally low distortion over a wide frequency range.

The AD9630 is an excellent choice to drive high speed and high resolution analog-to-digital Converters. Its output stage is designed to drive high speed flash converters with minimal or no series resistance. A current booster built into the output driver helps to maintain low distortion.

Parasitic or load capacitance (>7 pF) connected directly to the AD9630 output will result in frequency peaking. A small series resistor (R_S) connected between the buffer output and capacitive load will negate this effect. Figure 1 shows the optimal value of R_S as a function of C_L to obtain the flattest frequency response. Figure 2 illustrates frequency response for various capacitive loads utilizing the recommended R_S.

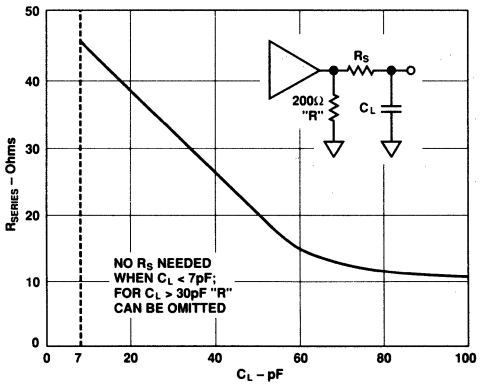


Figure 1. Recommended R_S vs. C_L

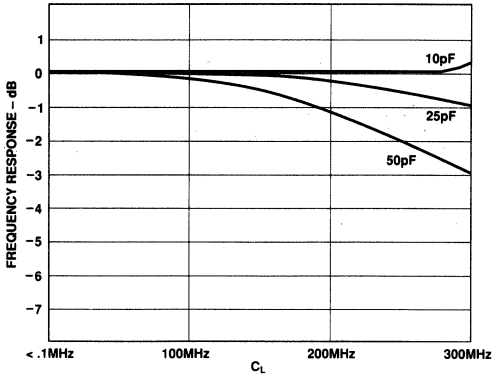


Figure 2. Frequency Response vs. C_L with Recommended R_S

In pulse mode applications, with R_S equal to approximately 12 ohms, capacitive loads of up to 50 pF can be driven with minimal settling time degradation.

The output stage has short circuit protection to ground. The output driver will shut down if more than approximately 130 mA of instantaneous sink or source current is reached. This level of current ensures that output clipping will not result when driving heavy capacitive loads during high slew conditions. Though average load currents above 70 mA may reduce device reliability.

LAYOUT CONSIDERATIONS

Due to the high frequency operation of the AD9630 attention to board layout is necessary to achieve optimum dynamic performance. A two ounce copper ground plane on the top side of the board is recommended; it should cover as much of the board as possible with appropriate openings for supply decoupling capacitors as well as for load and source termination resistors. (See Figure 3.)

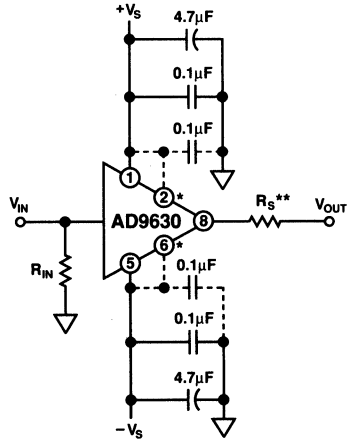


Figure 3. AD9630 Application Circuit

Optimum settling time and ac performance results will be achieved with surface mount 0.1 μF supply decoupling ceramic chip capacitors mounted within 50 mils of the corresponding device pins with the other side soldered directly to the ground plane. For best high resolution (<0.02%) settling times, the optional power supply pins should be decoupled as shown above. If the optional power supply pins are not used, they should be left open.

If surface mount capacitors cannot be used, radial lead ceramic capacitors with leads less than 30 mils long are recommended. Low frequency power supply decoupling is necessary and can be accomplished with 4.7 μF tantalum capacitors mounted within 0.5 inches of the supply pins. Due to the series inductance of these capacitors interacting with the 0.1 μF capacitors and power supply leads, high frequency oscillations might appear on the device output. To avoid this occurrence, the power supply leads should be tightly twisted (if appropriate). Ferrite beads mounted between the tantalum and ceramic capacitors will serve the same purpose.

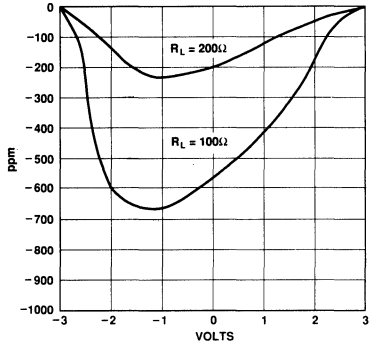
All unused pins (except the optional power supply pins) should be connected to ground to reduce pin-to-pin capacitive coupling and prevent external RF interference. If the source and drive electronics require "remote" operation (> 1 inch from the AD9630), the PC board line impedances should be matched with the buffer input and output resistances. Basic micro strip techniques should be observed. R_{IN} and R_S should be connected as close to the AD9630 as possible.

With only minimal pulse overshoot and ringing, the AD9630 can drive terminated cables directly without the use of an output termination resistor (R_S). Termination resistors (R_S and R_{IN}) can be either standard carbon composition or microwave type. For matching characteristic impedances, precision microwave resistor of 1% or better tolerance are preferred.

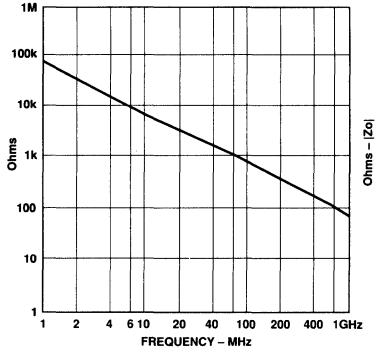
The AD9630 should be soldered directly to the PC board with as little vertical clearance as possible. The use of zero insertion sockets is strongly discouraged because of the high effective pin inductances. Use of this type socket will result in peaking and possibly induce oscillation. Consult the factory about the availability of an evaluation board, AD9630/PCB.

2

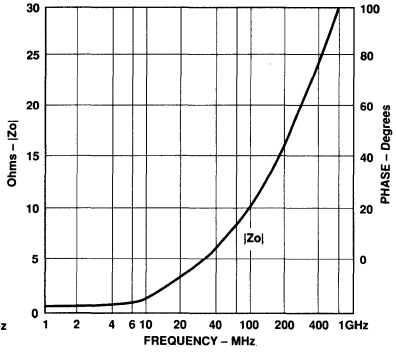
Typical Performance Curves



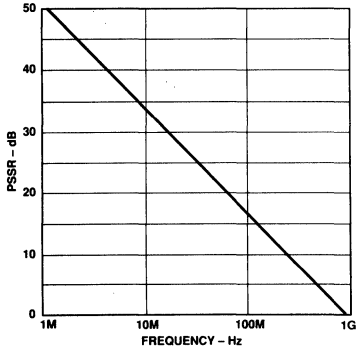
Endpoint DC Linearity Error



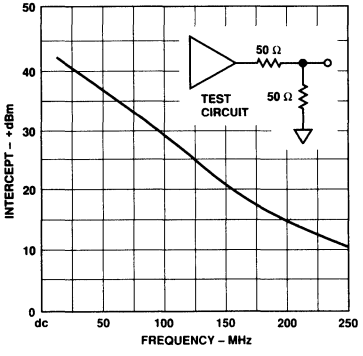
Input Impedance



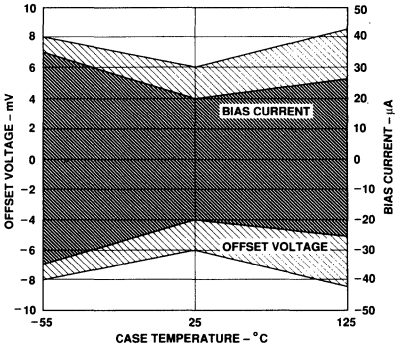
Output Impedance



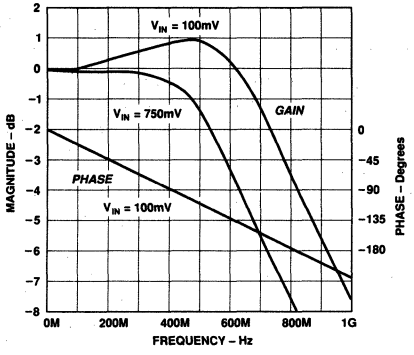
PSRR vs. Frequency



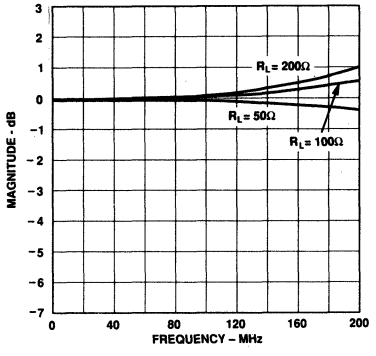
2-Tone Intermodulation Distortion



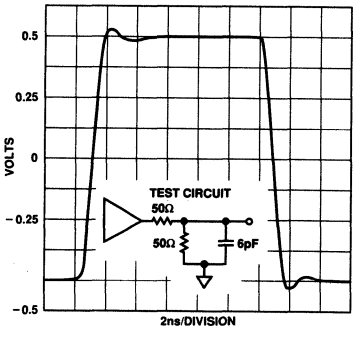
Offset Voltage and Bias Current vs. Temperature



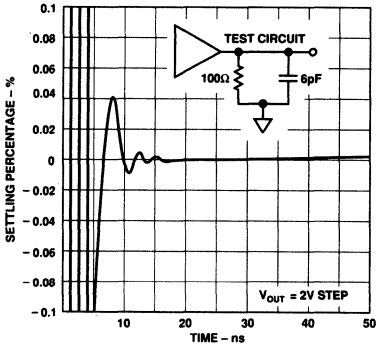
Forward Gain and Phase



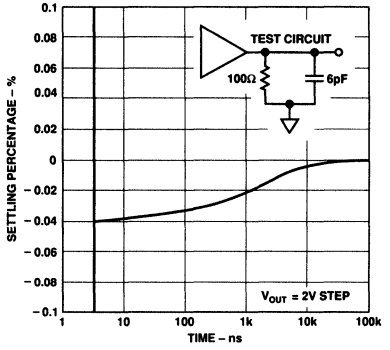
Frequency Response vs. R_{LOAD}



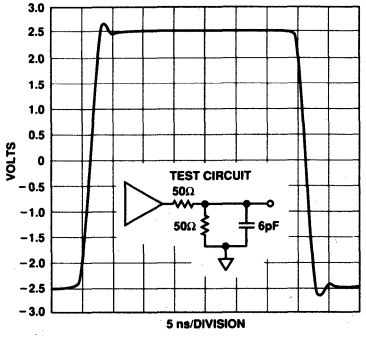
Small-Signal Pulse Response



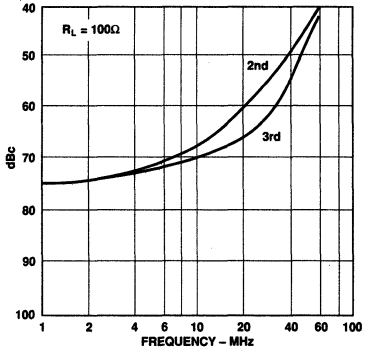
Short-Term Settling Time



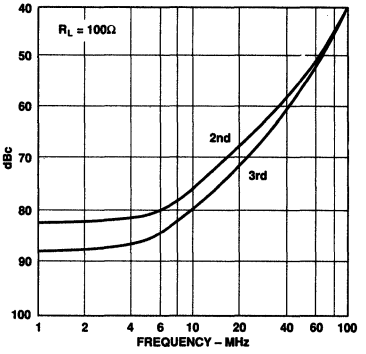
Long-Term Settling Time



Large-Signal Pulse Response



Harmonic Distortion V_{OUT} = 4 V p-p



Harmonic Distortion V_{OUT} = 2 V p-p

ANALOG DEVICES

Ultralow Offset Voltage Op Amp

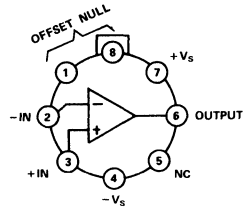
AD OP-07

FEATURES

- Ten Times More Gain than Other OP-07 Devices (3.0M min)
- Ultralow Offset Voltage: 10μV
- Ultralow Offset Voltage Drift: 0.2μV/°C
- Ultrastable vs. Time: 0.2μV/°C
- Ultralow Noise: 0.35μV p-p
- No External Components Required
- Monolithic Construction
- High Common-Mode Input Range: ±14.0V
- Wide Power Supply Voltage Range: ±3V to ±18V
- Fits 725, 108A/308A Sockets
- Military Parts and Plus Parts Available
- 8-Pin Plastic Mini-DIP, Cerdip, TO-99 Hermetic Metal Can, or SOIC
- Available in Wafer-Trimmed Chip Form
- Surface Mount (SOIC) Available in Tape and Reel

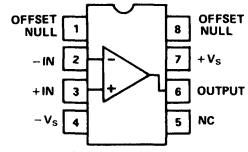
AD OP-07 CONNECTION DIAGRAMS

TO-99 (H) Package



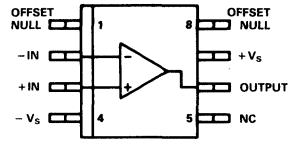
NC = NO CONNECT
TOP VIEW

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



NC = NO CONNECT
TOP VIEW

Small Outline (R) Package



NC = NO CONNECT
TOP VIEW

PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed-loop gain applications. Typical input offset voltages as low as 10μV, typical bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C (typ) and long-term stability of 0.2μV/month (typ) eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common-mode input voltage range (±13V, min) common-mode rejection ratio (typically up to 126dB) and high differential input impedance (50MΩ typ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the industrial grades are also available in plastic 8-pin mini-DIPs, and plastic surface mount (SOIC).

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultralow offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultralow input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

Model		AD OP-07E			AD OP-07C			AD OP-07D		
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
OPEN LOOP GAIN	A_{VO}	**2,000**	5,000		**1,200**	4,000		**1,200**	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	**±12.5**	±13.0		**±12.0**	±13.0		**±12.0**	±13.0	
		±12.0	±12.8		**±11.5**	±12.8		**±11.5**	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**75**		60	**150**		60	**150**
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift										
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6		0.7	2.5
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	2.0		0.5	3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	**3.8**		0.8	**6.0**		0.8	**6.0**
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8	35		12	50		12	50
INPUT BIAS CURRENT										
Initial	I_B		±1.2	**±4.0**		±1.8	**±7.0**		±2.0	**±12**
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13	35		18	50		18	50
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{INCM}		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±13.0**	±14.0		**±13.0**	±14.0		**±13.0**	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common-Mode Rejection Ratio	CMRR	**106**	123		**100**	120		**94**	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	**4.0**		3.5	**5.0**		3.5	**5.0**
Power Consumption	P_D		90	**120**		105	**150**		105	**150**
			6.0	**9.0**		6.0	**9.0**		6.0	**9.0**
Rejection Ratio	PSRR	**94**	107		**90**	104		**90**	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70
PACKAGE OPTIONS[3]										
SOIC (R-8)						AD OP-07CR				
Plastic Mini-DIP (N-8)			AD OP-07EN			AD OP-07CN			AD OP-07DN	
Cerdip (Q-8)			AD OP-07EQ			AD OP-07CQ			AD OP-07DQ	
TO-99 (H-08A)			AD OP-07EH			AD OP-07CH			AD OP-07DH	

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, the AD OP-07A offset voltage is guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV – Parameter is not 100% tested: 90% of units meet this specification.

[3]See Section 20 for package outline information.

Specifications subject to change without notice.

AD OP-07A			AD OP-07				
Min	Typ	Max	Min	Typ	Max	Test Conditions	Units
3,000	5,000		**2,000**	5,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	V/mV
2,000	4,000		**1,500**	4,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$, T_{min} to T_{max}	V/mV
300	1,000		300	1,000		$R_L = 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$	V/mV
±12.5	±13.0		**±12.5**	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		**±12.0**	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		**±10.5**	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		**±12.0**	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	**25**		30	**75**	Note 1	μV
	25	**60**[1]		60	**200**[1]	T_{min} to T_{max}	μV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	**0.6**		0.3	**1.3**	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 2	μV/Month
	0.3	**2.0**		0.4	**2.8**		nA
	0.8	**4.0**		1.2	**5.6**	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	**±2.0**		±1.0	**±3.0**		nA
	±1.0	**±4.0**		±2.0	**±6.0**	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz	μV p-p
	10.3	18.0		10.3	18.0	$f_O = 10Hz$	nV/√Hz
	10.0	13.0		10.0	13.0	$f_O = 100Hz$	nV/√Hz
	9.6	11.0		9.6	11.0	$f_O = 1kHz$	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz	pA p-p
	0.32	0.80		0.32	0.80	$f_O = 10Hz$	pA/√Hz
	0.14	0.23		0.14	0.23	$f_O = 100Hz$	pA/√Hz
	0.12	0.17		0.12	0.17	$f_O = 1kHz$	pA/√Hz
±13.0	±14.0		**±13.0**	±14.0			V
±13.0	±13.5		**±13.0**	±13.5		T_{min} to T_{max}	V
110	126		**110**	126		$V_{CM} = \pm CMVR$	dB
106	123		**106**	123		$V_{CM} = \pm CMVR$, T_{min} to T_{max}	dB
	3.0	**4.0**		30	**4.0**	$V_S = \pm 15V$	mA
	90	**120**		90	**120**	$V_S = \pm 15V$	mW
	6.0	**8.4**		6.0	**8.4**	$V_S = \pm 3V$	mW
100	110		**100**	110		$V_S = \pm 3V$ to $\pm 18V$	dB
94	106		**94**	106		$V_S = \pm 3V$ to $\pm 18V$, T_{min} to T_{max}	dB
−55		+125	−55		+125		°C
	AD OP-07AQ AD OP-07AH			AD OP-07Q AD OP-07H			

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

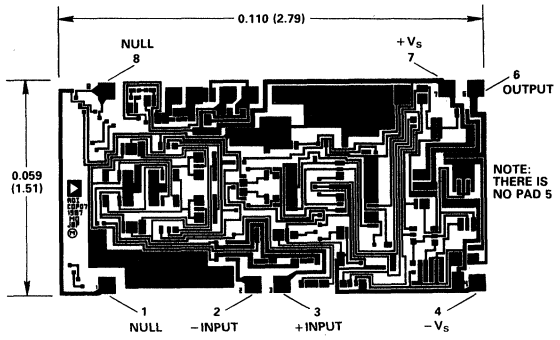
Supply Voltage . . . . . ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . . ±30V
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-07A, AD OP-07 . . . . . −55°C to +125°C
AD OP-07E, AD OP-07C, AD OP-07D . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTE
Note 1: Maximum package power dissipation vs. ambient temperature.

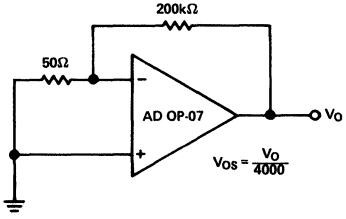
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

CHIP DIMENSIONS AND BONDING DIAGRAM

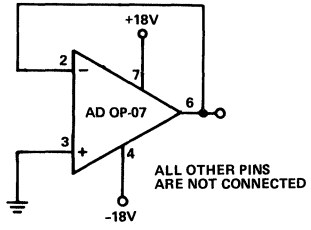
Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



THE AD OP-07 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM FOR PRECISION HYBRIDS. CONSULT THE FACTORY FOR DETAILS.



Offset Voltage Test Circuit



Burn-In Circuit

AD OP-07 ORDERING GUIDE[1]

Model	Package Options	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)
AD OP-07EH	TO-99	0 to +70	75	1.3
AD OP-07EN	Mini-DIP	0 to +70	75	1.3
AD OP-07EQ	Cerdip	0 to +70	75	1.3
AD OP-07CH	TO-99	0 to +70	150	1.8
AD OP-07CN	Mini-DIP	0 to +70	150	1.8
AD OP-07CQ	Cerdip	0 to +70	150	1.8
AD OP-07CR	SOIC	0 to +70	150	1.8
AD OP-07DH	TO-99	0 to +70	150	2.5
AD OP-07DN	Mini-DIP	0 to +70	150	2.5
AD OP-07DQ	Cerdip	0 to +70	150	2.5
AD OP-07AH	TO-99	−55 to +125	25	0.6
AD OP-07AQ	Cerdip	−55 to +125	25	0.6
AD OP-07H	TO-99	−55 to +125	75	1.3
AD OP-07Q	Cerdip	−55 to +125	75	1.3

NOTE
[1] A, C and D grade chips are also available. AD OP-07CR available in tape and reel.

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

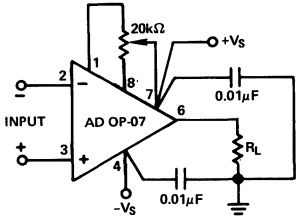


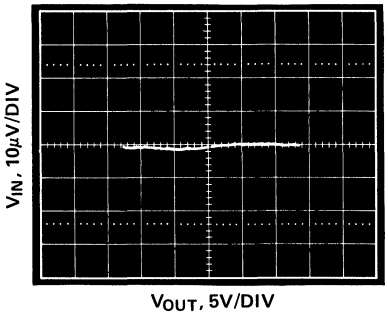
Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

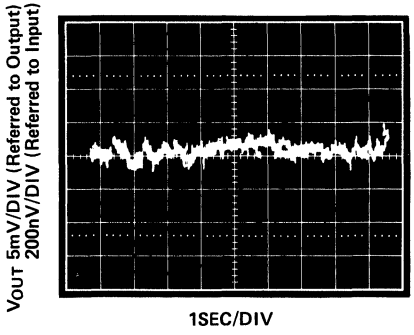
Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01μF ceramic capacitor as shown in Figure 1.

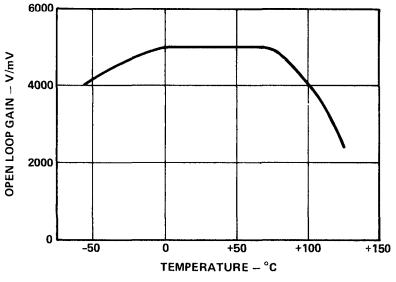
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



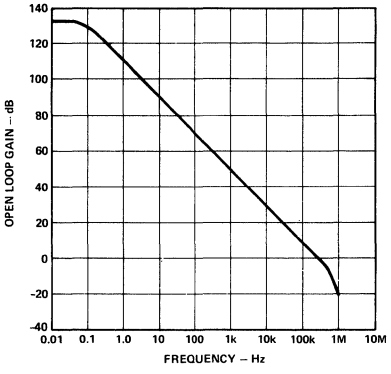
AD OP-07 Open-Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

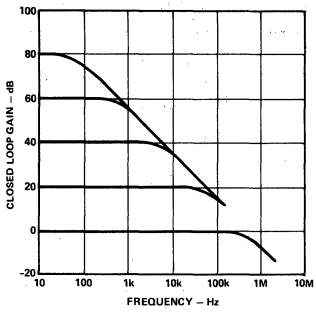


Open-Loop Gain vs. Temperature

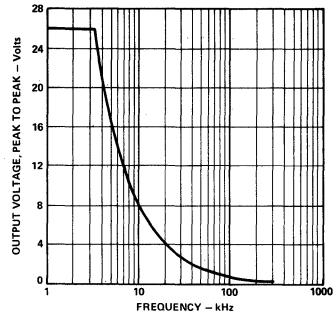


Open-Loop Frequency Response

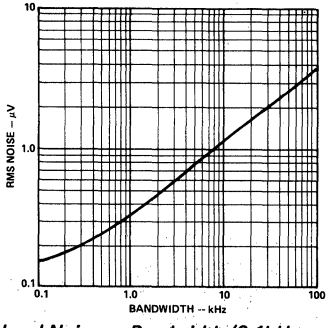
Typical Performance Curves



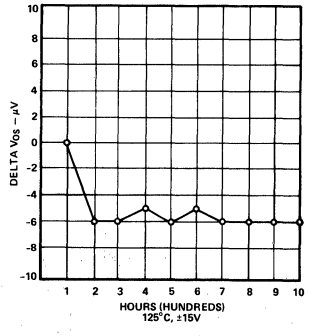
Closed-Loop Response for Various Gain Configurations



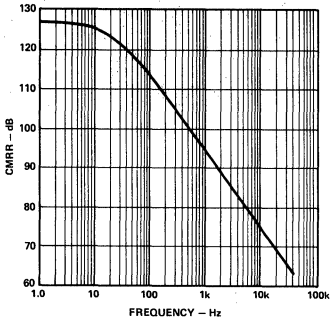
Maximum Undistorted Output vs. Frequency



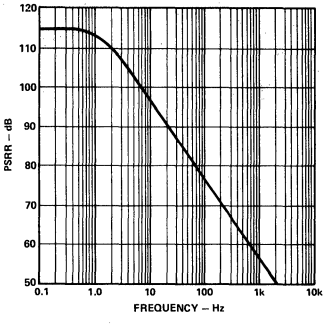
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



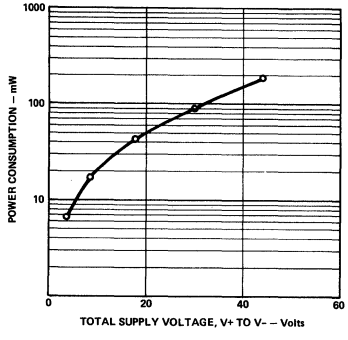
Offset Voltage vs. Time



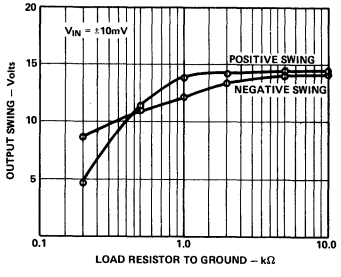
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance

ANALOG DEVICES

Ultralow Noise, Precision Op Amp

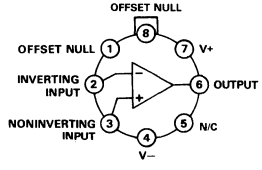
AD OP-27

FEATURES

Ultralow Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
Ultralow Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
High Slew Rate: 2.8V/μs
High Gain Bandwidth Product: 8MHz
Low Offset Voltage: 10μV
High CMRR: 126dB Over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, 725, 714 and 741 Sockets
Military Grade and Plus Parts Available
8-Pin Plastic Mini-DIP, Cerdip, TO-99 Hermetic Metal Can or Chip Form
Available in Wafer-Trimmed Chip Form

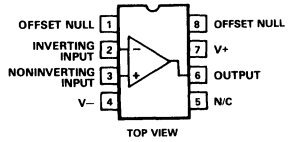
AD OP-27 CONNECTION DIAGRAMS

TO-99 (H) Package



TOP VIEW
NOTE: PIN 4 CONNECTED TO CASE

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



TOP VIEW

PRODUCT DESCRIPTION

The AD OP-27 offers the combined features of high precision, ultralow noise and high speed in a monolithic bipolar operational amplifier. State-of-the-art performance for high accuracy amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-27. As a device directly compatible with other low noise op amps, the AD OP-27 features industry standard dc performance; typical input offset voltages of 10μV and typical input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-27 is characterized by an e_n p-p (typ) of 80nV (0.1Hz to 10Hz), an e_n (typ) of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. AC specifications including a 2.8V/μs (typ) slew rate and an 8MHz (typ) gain bandwidth product are possible without sacrificing dc accuracy. Long-term stability is assured by an input offset voltage drift specification of 0.2μV/month.

Source resistance related errors with the AD OP-27 are minimized by a low input bias current at ambient of ± 10nA (typ) and an input offset current of 7nA (typ). An input bias current cancellation circuit limits bias and offset currents over the extented temperature range to ± 20nA (typ) and 15nA (typ), respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

The AD OP-27 is available in six performance grades. The AD OP-27E, AD OP-27F and AD OP-27G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-27A, AD OP-27B and AD OP-27C are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the E, F and G grades are also available in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. Precision amplification of very low level, low frequency voltage inputs is enhanced by ultralow input voltage noise.
2. The AD OP-27 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

Model		AD OP-27G			AD OP-27F			AD OP-27E		
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		750	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		±11.7	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	5.0	8.0		5.0	8.0		5.0	8.0	
Slew Rate	SR	1.7	2.8		1.7	2.8		1.7	2.8	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**60**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	±60
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	50
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8	
Common-Mode Rejection Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		110	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	**5.6**		3.0	**4.6**		3.0	**4.6**
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	15
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
	T_{min}, T_{max}	−25		+85	−25		+85	−25		+85
PACKAGE OPTIONS[3]										
Plastic Mini-DIP (N-8)			AD OP-27GN			AD OP-27FN			AD OP-27EN	
Cerdip (Q-8)			AD OP-27GQ			AD OP-27FQ			AD OP-27FQ	
TO-99 (H-08A)			AD OP-27GH			AD OP-27FH			AD OP-27EH	
A, C and G Grade Chips Also Available										

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

[3]See Section 20 for package outline information.

Specifications subject to change without notice.

AD OP-27C			AD OP-27B			AD OP-27A			Conditions	Units
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
400	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
5.0	8.0		5.0	8.0		5.0	8.0			MHz
1.7	2.8		1.7	2.8		1.7	2.8		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	1.8		0.3	1.3		0.2	**0.6**	T_a = min to max	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 2)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**± 55**		±10	**±40**		nA
	±35	**±150**		±28	**± 95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	nV/√Hz
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	nV/√Hz
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	nV/√Hz
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	pA/√Hz
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	pA/√Hz
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	pA/√Hz
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		±10.3	±11.5		±10.3	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	**5.6**		3.0	**4.6**		3.0	**4.6**	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C
AD OP-27CQ AD OP-27CH			AD OP-27BQ AD OP-27BH			AD OP-27AQ AD OP-27AH				

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 2) . . . . . ±0.7V
Differential Input Current (Note 2) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-27A, AD OP-27B, AD OP-27C . −55°C to +125°C
AD OP-27E, AD OP-27F, AD OP-27G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

NOTES:

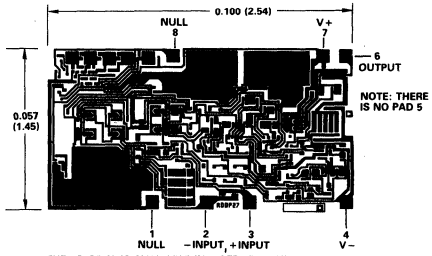
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

Note 2: The AD OP-27's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



THE AD OP-27 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM. CONSULT THE FACTORY FOR DETAILS.

AD OP-27 ORDERING GUIDE[1]

Model	Package Options	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)
AD OP-27GH	TO-99	−25 to +85	100	1.8
AD OP-27GN	Mini-DIP	−25 to +85	100	1.8
AD OP-27GQ	Cerdip	−25 to +85	100	1.8
AD OP-27FH	TO-99	−25 to +85	60	1.3
AD OP-27FN	Mini-DIP	−25 to +85	60	1.3
AD OP-27FQ	Cerdip	−25 to +85	60	1.3
AD OP-27EH	TO-99	−25 to +85	25	0.6
AD OP-27EN	Mini-DIP	−25 to +85	25	0.6
AD OP-27EQ	Cerdip	−25 to +85	25	0.6
AD OP-27CH	TO-99	−55 to +125	100	1.8
AD OP-27CQ	Cerdip	−55 to +125	100	1.8
AD OP-27BH	TO-99	−55 to +125	60	1.3
AD OP-27BQ	Cerdip	−55 to +125	60	1.3
AD OP-27AH	TO-99	−55 to +125	25	0.6
AD OP-27AQ	Cerdip	−55 to +125	25	0.6

NOTE
[1]A, C and G grade chips also available.

APPLICATION NOTES FOR THE AD OP-27

The AD OP-27 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for optimum AD OP-27 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

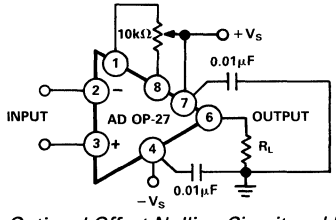


Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-27. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature—a temperature close to the device's package.

Output stability with the AD OP-27 is possible with capacitive loads of up to 2000pF and ±10V output swings. Larger capacitances should be decoupled with a 50Ω resistor.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-27 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

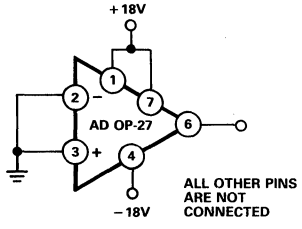


Figure 2. Burn-In Circuit

SLEW RATE DISCUSSION

In unity gain buffer applications with feedback resistances of less than 100Ω where the input is driven with a fast, large (greater than 1V) pulse, the output waveform will appear as in Figure 3.

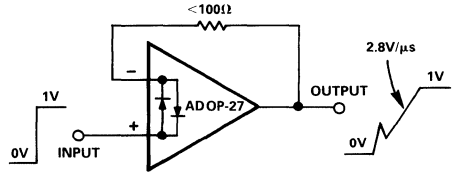


Figure 3. Unity Gain Buffer/Pulsed Operation

During the initial portion of the output slew the input protection back-to-back diodes effectively short the output to the input. A current limited only by the output short circuit protection will be drawn from the source. After the input diodes saturate, the amplifier will slew at its nominal 2.8V/μs. With feedback resistances of more than 500Ω the output is capable of handling the current requirements without limiting (less than 20mA at 10V) and the amplifier will stay in the linear region.

As with all operational amplifiers a feedback resistance of greater than 2kΩ will create a pole with the input capacitance (8pF). Additional phase shift will be introduced and the phase margin will be reduced. A small capacitor (20 to 50pF) in parallel with the feedback resistor will alleviate this problem.

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-27 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

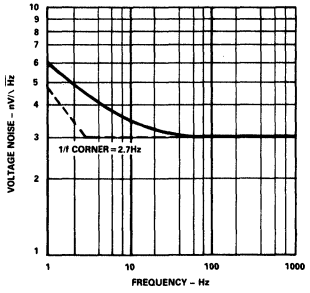
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

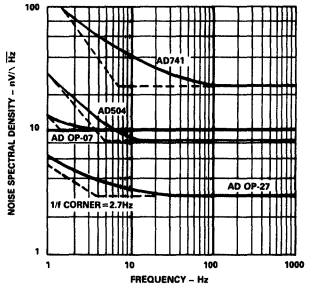
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the 1/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee 1/f and white noise performance over the rated frequency spectrum.

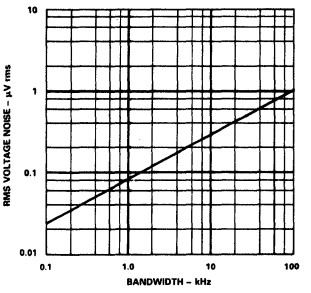
Typical Performance Curves (@ $T_A = +25°C$, $V_S = \pm 15V$)



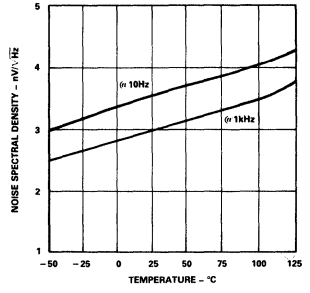
Input Voltage Noise Spectral Density



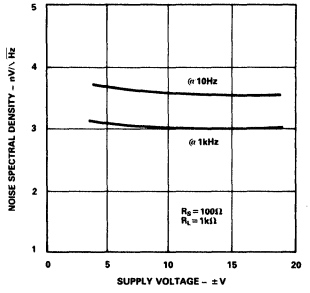
Comparison of Op Amp Input Voltage Noise Spectrums



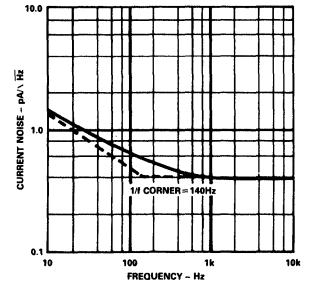
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



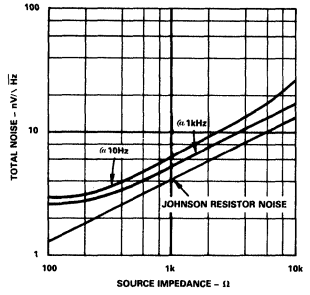
Input Voltage Noise vs. Temperature



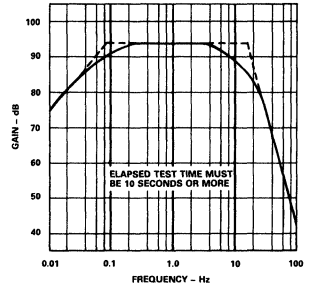
Input Voltage Noise vs. Supply Voltage



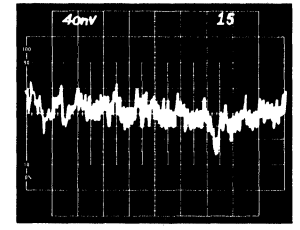
Input Current Noise Spectral Density



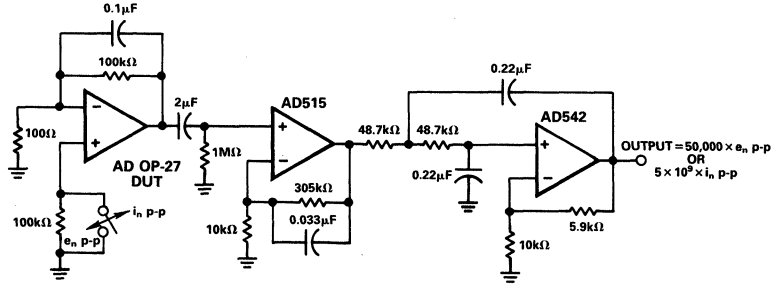
Total Noise vs. Source Impedance



0.1Hz to 10Hz Noise Test Frequency Response

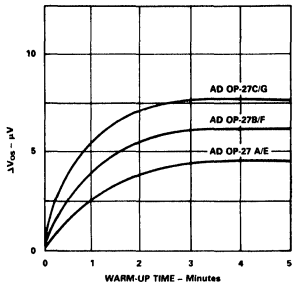


0.1Hz to 10Hz p-p Voltage Noise

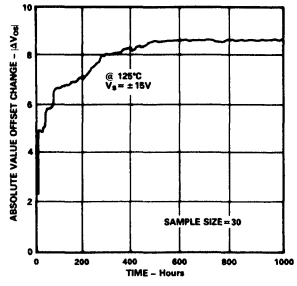


NOTE: ALL CAPACITORS MUST BE NONPOLARIZED

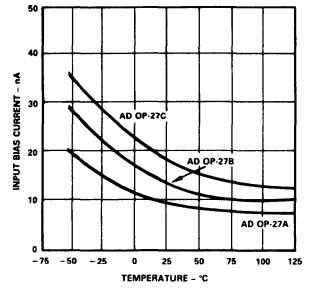
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



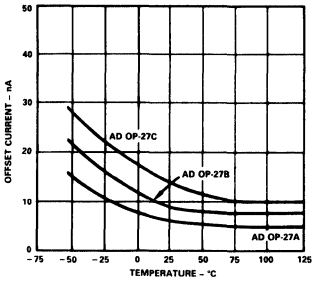
Input Offset Voltage Turn-On Drift vs. Warm-Up Time



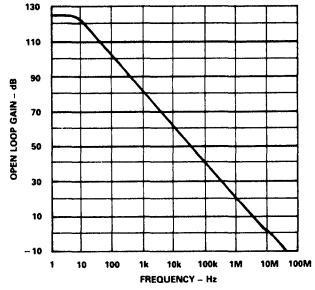
Long Term Offset Stability @ Temperature



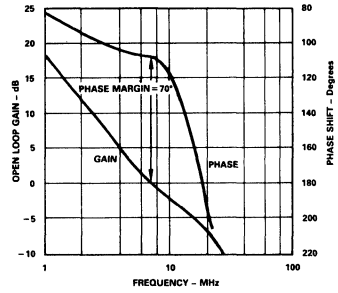
Input Bias Current vs. Temperature



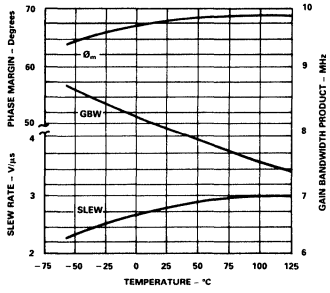
Input Offset Current vs. Temperature



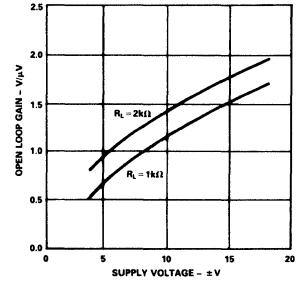
Open Loop Frequency Response



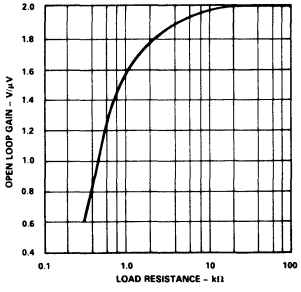
Open Loop Gain and Phase Shift vs. Frequency



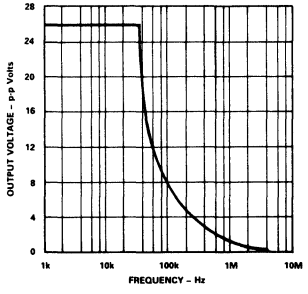
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



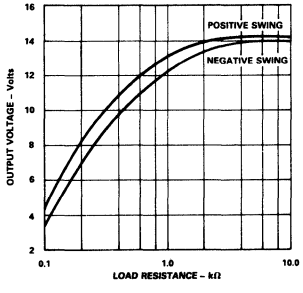
Open Loop Gain vs. Supply Voltage



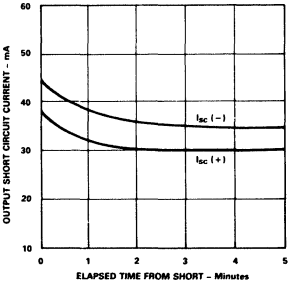
Open Loop Gain vs. Load Resistance



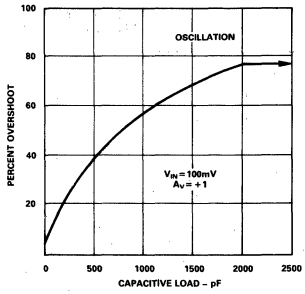
Undistorted Output Swing vs. Frequency



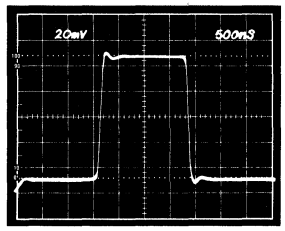
Output Swing vs. Load Resistance



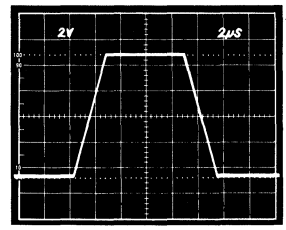
Output Short Circuit Current vs. Time



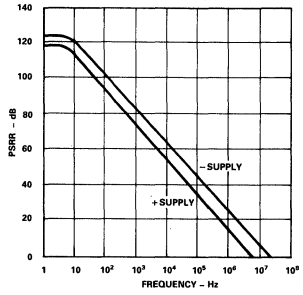
Small Signal Overshoot vs. Capacitive Load



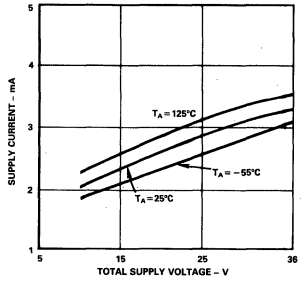
Unity Gain Follower Pulse Response (Small Signal)



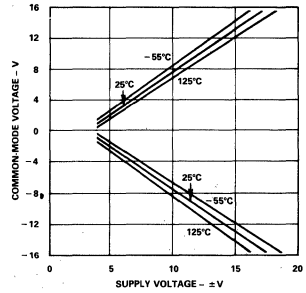
Unity Gain Follower Pulse Response (Large Signal)



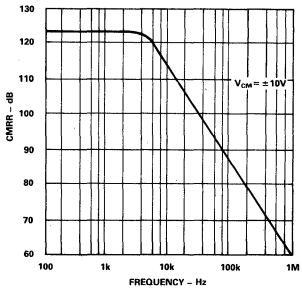
Power Supply Rejection Ratio vs. Frequency



Supply Current vs. Supply Voltage



Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency

ANALOG DEVICES

Ultralow Noise, High Speed, Precision Op Amp ($A_{VCL} \geq 5$)

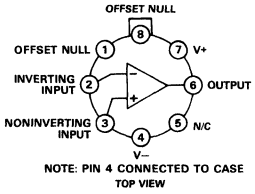
AD OP-37

FEATURES

Ultralow Noise: 80nV p–p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
High Speed: 17V/μs
High Gain Bandwidth Product: 63MHz
Ultralow Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
Low Offset Voltage: 10μV
High CMRR: 126dB Over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, LH0044, 5130, 3510, 725, 714 and 741 Sockets in Gains ≥ 5
Military Grade and Plus Parts Available
8-Pin Plastic Mini-DIP, Cerdip or TO-99 Hermetic Metal Can
Available in Wafer-Trimmed Chip Form

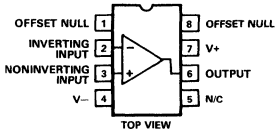
AD OP-37 CONNECTION DIAGRAMS

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE
TOP VIEW

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



TOP VIEW

PRODUCT DESCRIPTION

The AD OP-37 offers the combined features of high precision, ultralow noise and high speed in a monolithic bipolar operational amplifier. High speed, accurate amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-37 in applications requiring gains greater than or equal to five. This instrumenation grade op amp features industry standard dc performance; typical input offset voltages of 10μV and typical input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-37 is characterized by an e_n p-p (typ) of 80nV (0.1Hz to 10Hz), an e_n (typ) of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. High speed performance is assured by a typical 17V/μs slew rate and a typical 63MHz gain bandwidth product. Long-term stability is guaranteed by an input offset voltage drift specification of 0.2μV/month.

Source resistance related input errors with the AD OP-37 are minimized by a low input bias current of ±10nA (typ) and an input offset current of 7nA (typ). An input bias current cancellation circuit restricts bias and offset currents over the extended temperature range to ±20nA (typ) and 15nA (typ), respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of 120dB.

The AD OP-37 is available in six performance grades. The AD OP-37E, AD OP-37F and AD OP-37G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-37A, AD OP-37B and AD OP-37C are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the industrial grades are also available in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. High speed accurate amplification (gains ≥ 5) of very low level low frequency voltage inputs is enhanced by a high gain bandwidth product and ultralow input voltage noise.
2. The AD OP-37 maintains high dc accuracy over an extended temperature range due to ultralow offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common-mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

Model		AD OP-37G			AD OP-37F			AD OP-37E		
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		750	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		±11.7	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	45	63		45	63		45	63	
		–	40		–	40		–	40	
Slew Rate	SR	11	17		11	17		11	17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**60**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long-Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	±60
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	50
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8	
Common-Mode Rejection Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		110	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	**5.6**		3.0	**4.6**		3.0	**4.6**
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	15
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
	T_{min}, T_{max}	−25		+85	−25		+85	−25		+85
PACKAGE OPTIONS[3]										
Plastic Mini-DIP (N-8)			AD OP-37GN			AD OP-37FN			AD OP-37EN	
Cerdip (Q-8)			AD OP-37GQ			AD OP-37FQ			AD OP-37EQ	
TO-99 (H-08)			AD OP-37GH			AD OP-37FH			AD OP-37EH	
C and G Grade Chips Also Available										

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

[3]See Section 20 for package outline information.

Specifications subject to change without notice.

AD OP-37C			AD OP-37B			AD OP-37A			Conditions	Units
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
400	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
45	63		45	63		45	63		$f_o = 10kHz$	MHz
–	63		–	40		–	40		$f_o = 1MHz$	MHz
11	17		11	17		11	17		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	1.8		0.3	1.3		0.2	**0.6**	T_a = min to max	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 2)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	$nV/\sqrt{Hz}$
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	$nV/\sqrt{Hz}$
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	$nV/\sqrt{Hz}$
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	$pA/\sqrt{Hz}$
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	$pA/\sqrt{Hz}$
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	$pA/\sqrt{Hz}$
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		±10.3	±11.5		±10.3	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	**5.6**		3.0	**4.6**		3.0	**4.6**	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C
AD OP-37CQ AD OP-37CH			AD OP-37BQ AD OP-37BH			AD OP-37AQ AD OP-37AH				

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage . . . . . ±Vs
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 2) . . . . . ±0.7V
Differential Input Current (Note 2) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-37A, AD OP-37B, AD OP-37C . −55°C to +125°C
AD OP-37E, AD OP-37F, AD OP-37G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

NOTES:

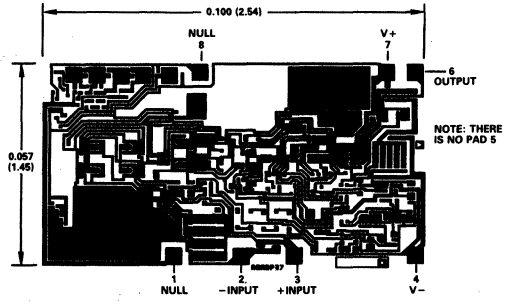
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

Note 2: The AD OP-37's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



THE AD OP-37 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM. CONSULT THE FACTORY FOR DETAILS.

AD OP-37 ORDERING GUIDE[1]

Model	Package Options[2]	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)
AD OP-37GH	TO-99	−25 to +85	100	1.8
AD OP-37GN	Mini-DIP	−25 to +85	100	1.8
AD OP-37GQ	Cerdip	−25 to +85	100	1.8
AD OP-37FH	TO-99	−25 to +85	60	1.3
AD OP-37FN	Mini-DIP	−25 to +85	60	1.3
AD OP-37FQ	Cerdip	−25 to +85	60	1.3
AD OP-37EH	TO-99	−25 to +85	25	0.6
AD OP-37EN	Mini-DIP	−25 to +85	25	0.6
AD OP-37EQ	Cerdip	−25 to +85	25	0.6
AD OP-37CH	TO-99	−55 to +125	100	1.8
AD OP-37CQ	Cerdip	−55 to +125	100	1.8
AD OP-37BH	TO-99	−55 to +125	60	1.3
AD OP-37BQ	Cerdip	−55 to +125	60	1.3
AD OP-37AH	TO-99	−55 to +125	25	0.6
AD OP-37AQ	Cerdip	−55 to +125	25	0.6

NOTES
[1]C and G grade chips also available.
[2]See Section 20 for package outline information.

APPLICATION NOTES FOR THE AD OP-37

The AD OP-37 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for correct AD OP-37 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

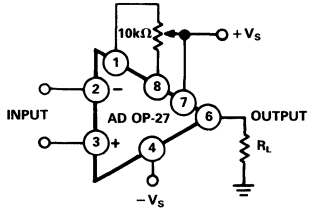


Figure 1. Optional Offset Nulling Circuit

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-37. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature.

Although the AD OP-37 features high-power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to Pins 4 and 7 of the AD OP-37 as possible, to load ground with a good quality 0.01μF ceramic capacitor as shown in Figure 1.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-37 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

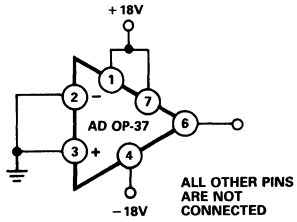


Figure 2. Burn-In Circuit

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-37 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

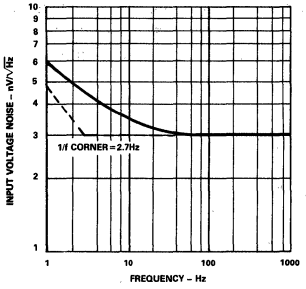
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

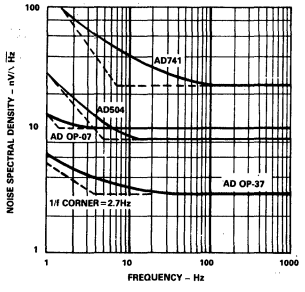
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the 1/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee 1/f and white noise performance over the rated frequency spectrum.

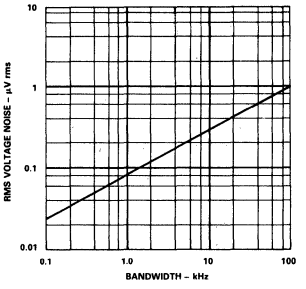
Typical Performance Curves (@ $T_A = +25°C$, $V_S = \pm 15V$)



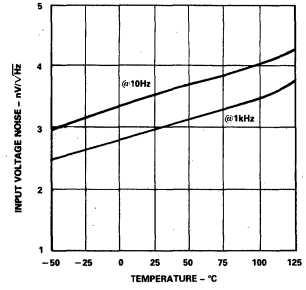
Input Voltage Noise Spectral Density



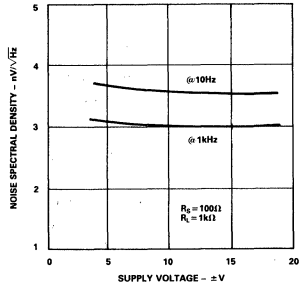
Comparison of Op Amp Input Voltage Noise Spectrums



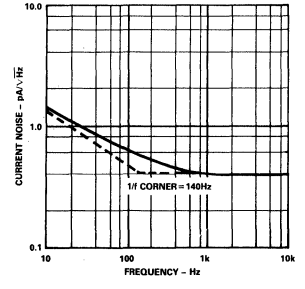
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



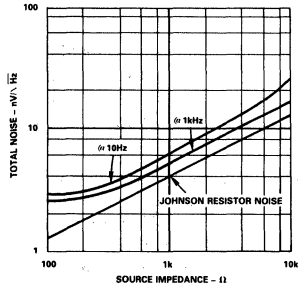
Input Voltage Noise vs. Temperature



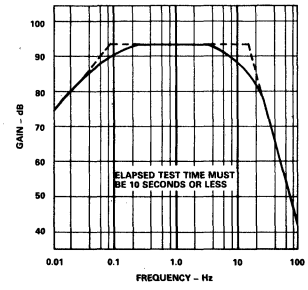
Input Voltage Noise vs. Supply Voltage



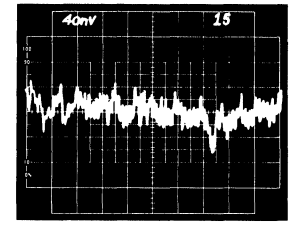
Input Current Noise Spectral Density



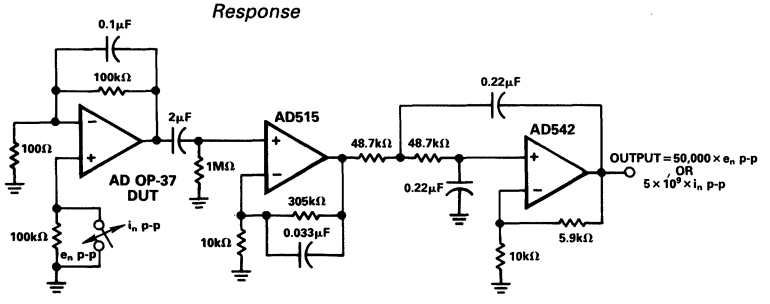
Total Noise vs. Source Impedance



0.1Hz to 10Hz Noise Test Frequency Response

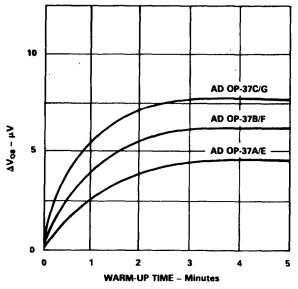


0.1Hz to 10Hz p–p Voltage Noise

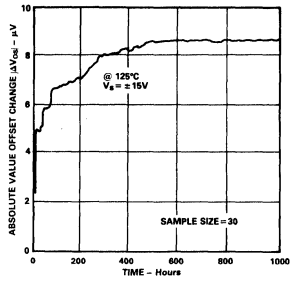


NOTE: ALL CAPACITORS MUST BE NONPOLARIZED

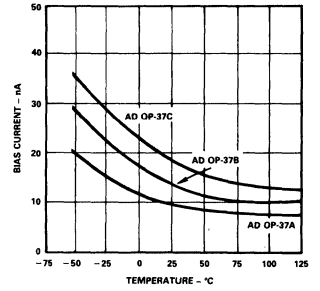
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



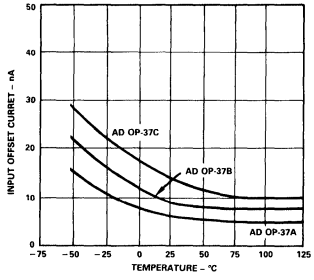
Input Offset Voltage Turn-On Drift vs. Warm-Up Time



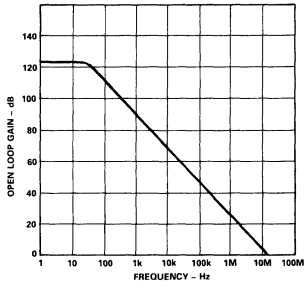
Long Term Offset Stability @ Temperature



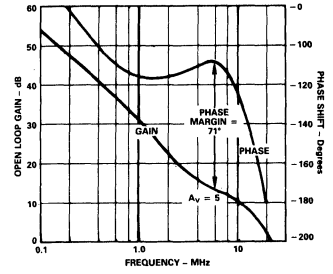
Input Bias Current vs. Temperature



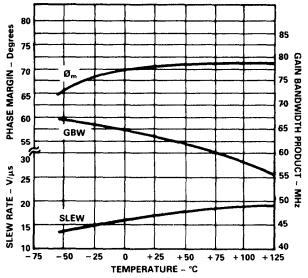
Input Offset Current vs. Temperature



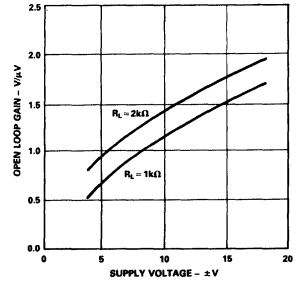
Open-Loop Frequency Response



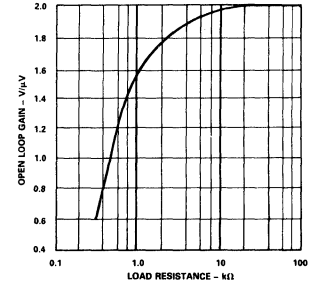
Open-Loop Gain and Phase Shift vs. Frequency



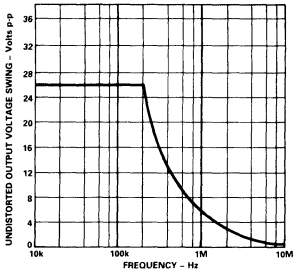
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



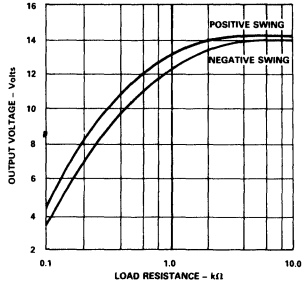
Open-Loop Gain vs. Supply Voltage



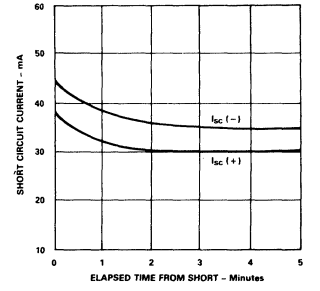
Open-Loop Gain vs. Load Resistance



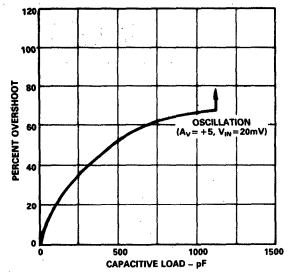
Undistorted Output Voltage Swing vs. Frequency



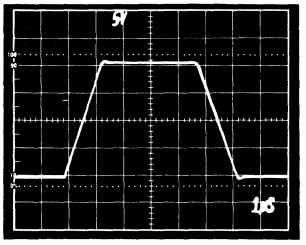
Output Swing vs. Load Resistance



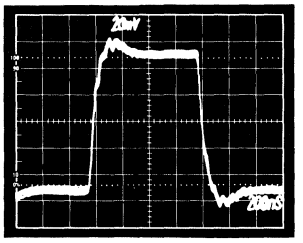
Output Short Circuit Current vs. Time



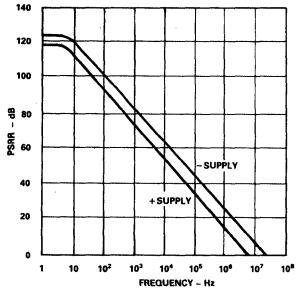
Small Signal Overshoot vs. Capacitive Load



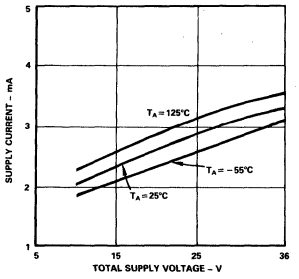
Large Signal Pulse Response (A_V = 5, R_L = 2k)



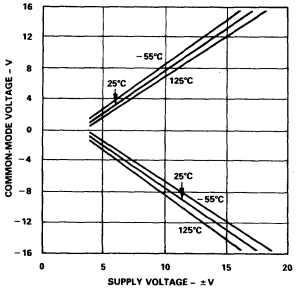
Small Signal Pulse Response (A_V = 5, R_L = 2k)



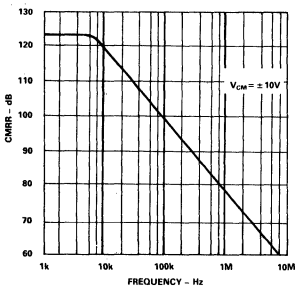
Power Supply Rejection Ratio vs. Frequency



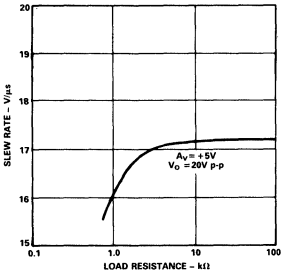
Supply Current vs. Supply Voltage



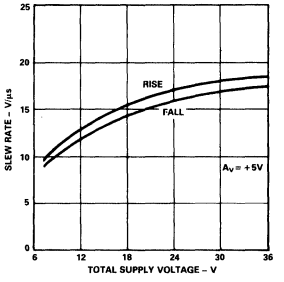
Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency



Slew Rate vs. Resistive Load



Slew Rate vs. Supply Voltage

Comparators
Contents

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Selection Guide
Comparators

Model	Prop Delay ns max	Logic	V_{OS} mV max	Package Options[1]	Temp Range[2]	Page	Comments
AD96685	**3.5**	**ECL**	**2**	**E, H, P, Q**	**I, M**	**3–21**	**Ultrafast**
AD96687	**3.5**	**ECL**	**2**	**E, P, Q**	**I, M**	**3–21**	**Dual AD96685**
AD790	**45**	**TTL**	**0.25–1**	**N, Q, R**	**C, I, M**	**3–5**	**Fast, Precise Single Supply**
AD9696	**4.5**	**TTL**	**2**	**H, N, Q, R**	**C, M**	**3–13**	**Single Comparator**
AD9698	**4.5**	**TTL**	**2**	**H, Q, R**	**C, M**	**3–13**	**Dual Comparator**

[1]Package Options: E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip; R–Small Outline Plastic (SOIC).
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
Comparators

A voltage comparator compares two voltages and provides an output that is a function of their difference. For the products in this section, the output of an ideal comparator has two stable states representing the *sign* of the difference. Thus, the output will be a logic "1" if the voltage at the input labelled "+" is greater than the voltage at the input labelled "–," and logic "0" for the opposite case.

A comparator is used wherever some action depends on whether a voltage is – or becomes – greater or less than another voltage – usually a reference. Since it is in effect a 1-bit A/D converter, the comparator is the basic element of virtually all A/D converters, as well as a sign-magnitude adjunct. Because the voltage that is compared with a reference can be the linearly varying output of an integrator with constant input, a comparator can be used in analog-based event timing. The comparator is also an element of pulse-width modulators, peak detectors, delay generators, switch drivers, etc.

A comparator is essentially a fast, high-gain amplifier whose output is always at an upper or lower limit, except when switching. The simplest comparator would be an open-loop-connected, uncompensated, high-gain, high-slew-rate op amp with excellent offset & drift characteristics, fast recovery from overdrive and an overdrive-protected input.

In addition, practical comparators have a small amount of hysteresis (internal or external) to help keep noise from causing the output to bounce around, and most have a *latch*, which makes it possible to freeze the output at the state it has at a given instant of time, in response to a logic signal. Since the comparator is producing a digital decision, its outputs are generally compatible with either TTL or ECL.

Aside from its op-amp related specifications, such as bias current, offset & drift and the various logic-related timing and interface specs, the key comparator spec is *propagation delay*: the time required for the output to reach the 50% point of a transition, after the net input has crossed the offset voltage – when driven by a square wave to a prescribed value of input overdrive, usually 5mV or 10mV.

The Selection Guide classifies Analog Devices comparators by propagation delay, presence or absence of a latch and interface logic compatibility. It also indicates the presence of *dual* comparators, each comprising two independent comparators on a single monolithic chip. Pairs of comparators may be used for *window* measurements, as well as for simple two-in-one space-saving.

ANALOG DEVICES

Fast, Precision Comparator

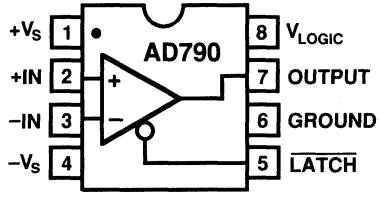
AD790

FEATURES
- 45 ns max Propagation Delay
- Single +5 V or Dual ±15 V Supply Operation
- CMOS or TTL Compatible Output
- 250 μV max Input Offset Voltage
- 500 μV max Input Hysteresis Voltage
- 15 V max Differential Input Voltage
- On-Board Latch
- 60 mW Power Dissipation
- Available in 8-Pin Plastic and Hermetic Cerdip Packages and Chip Form
- MIL-STD-883B Processing Available

APPLICATIONS
- Zero-Crossing Detectors
- Overvoltage Detectors
- Pulse-Width Modulators
- Precision Rectifiers
- Discrete A/D Converters
- Delta-Sigma Modulator A/Ds

AD790 CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP and Cerdip



PRODUCT DESCRIPTION

The AD790 is a fast (45 ns), precise voltage comparator, with a number of features that make it exceptionally versatile and easy to use. The AD790 may operate from either a single +5 V supply or a dual ±15 V supply. In the single-supply mode, the AD790's inputs may be referred to ground, a feature not found in other comparators. In the dual-supply mode it has the unique ability of handling a maximum differential voltage of 15 V across its input terminals, easing their interfacing to large amplitude and dynamic signals.

This device is fabricated using Analog Devices' Complementary Bipolar (CB) process – which gives the AD790's combination of fast response time and outstanding input voltage resolution (1 mV max). To preserve its speed and accuracy, the AD790 incorporates a "low glitch" output stage that does not exhibit the large current spikes normally found in TTL or CMOS output stages. Its controlled switching reduces power supply disturbances that can feed back to the input and cause undesired oscillations. The AD790 also has a latching function which makes it suitable for applications requiring synchronous operation.

The AD790 is available in five performance grades. The AD790J and the AD790K are rated over the commercial temperature range of 0 to +70°C. The AD790A and AD790B are rated over the industrial temperature range of −40°C to +85°C. The AD790S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

PRODUCT HIGHLIGHTS

1. The AD790's combination of speed, precision, versatility and low cost makes it suitable as a general purpose comparator in analog signal processing and data acquisition systems.
2. Built-in hysteresis and a low-glitch output stage minimize the chance of unwanted oscillations, making the AD790 easier to use than standard open-loop comparators.
3. The hysteresis combined with a wide input voltage range enables the AD790 to respond to both slow, low level (e.g., 10 mV) signals and fast, large amplitude (e.g., 10 V) signals.
4. A wide variety of supply voltages are acceptable for operation of the AD790, ranging from single +5 V to dual +5 V/ −12 V, ±5 V, or +5 V/±15 V supplies.
5. The AD790's power dissipation is the lowest of any comparator in its speed range.
6. The AD790's output swing is symmetric between V_{LOGIC} and ground, thus providing a predictable output under a wide range of input and output conditions.

SPECIFICATIONS

DUAL SUPPLY (Operation @ +25°C and $+V_S$ = +15 V, $-V_S$ = −15 V, V_{LOGIC} = +5 V unless otherwise noted)

Parameter	Conditions	AD790J/A Min	AD790J/A Typ	AD790J/A Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	AD790S Min	AD790S Typ	AD790S Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		40	45		40	45		40	45	ns
	T_{min} to T_{max}			45/50			45/50			60	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{min} to T_{max}	**4.3**/**4.3**			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{min} to T_{max}			**0.5**/**0.5**			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[1]			0.2	**1.0**		0.05	**0.25**		0.2	**1.0**	mV
	T_{min} to T_{max}			1.5			**0.5**			1.5	mV
Hysteresis[2]	T_{min} to T_{max}	0.3	0.4	0.6	**0.3**	0.4	**0.5**	**0.3**	0.4	**0.65**	mV
Bias Current	Either Input		2.5	**5**		1.8	**3.5**		2.5	**5**	μA
	T_{min} to T_{max}			6.5			**4.5**			**7**	μA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	μA
	T_{min} to T_{max}			0.3			**0.2**			**0.4**	μA
Power Supply											
Rejection Ratio dc	V_S ±20%	**80**	90		**88**	100		**80**	90		dB
	T_{min} to T_{max}	76	88		**85**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage	$V_S \leq \pm 15$ V			**±V_S**			**±V_S**			**±V_S**	V
Common Mode		$-V_S$		$+V_S-2$ V	$-V_S$		$+V_S-2$ V	$-V_S$		$+V_S-2$ V	V
Common Mode											
Rejection Ratio	−10 V<V_{CM} <+10 V	**80**	95		**88**	105		**80**	95		dB
	T_{min} to T_{max}	76	90		**85**	100		**76**	88		dB
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level, V_{IL}	T_{min} to T_{max}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{min} to T_{max}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	**5**		2.3	**3.5**		2.3	**5**	μA
	T_{min} to T_{max}			7			**5**			**8**	μA
SUPPLY CHARACTERISTICS											
Diff Supply Voltage[3]	V_{LOGIC} = 5 V										
	T_{min} to T_{max}	4.5		33	**4.5**		**33**	**4.7**		**33**	V
Logic Supply	T_{min} to T_{max}	4.0		7	**4.0**		**7**	**4.2**		**7**	V
Quiescent Current											
$+V_S$	$+V_S$ = 15 V		8	**10**		8	**10**		8	**10**	mA
$-V_S$	$-V_S$ = −15 V		4	**5**		4	**5**		4	**5**	mA
V_{LOGIC}	V_{LOGIC} = 5 V		2	**3.3**		2	**3.3**		2	**3.3**	mA
Power Dissipation				**242**			**242**			**242**	mW
TEMPERATURE RANGE											
Rated Performance	T_{min} to T_{max}	0 to +70/−40 to +85			0 to +70/−40 to +85			−55 to +125			°C
PACKAGE OPTIONS[4]											
Plastic (N-8)		AD790JN			AD790KN						
Cerdip (Q-8)		AD790AQ			AD790BQ			AD790SQ			

NOTES

[1]Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[2]Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[3]$+V_S$ must be no lower than (V_{LOGIC} −0.5 V) in any supply operating conditions, except during power up.

[4]See Section 20 for package outline information.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.

Specifications subject to change without notice.

SINGLE SUPPLY (Operation @ +25°C and $+V_S = V_{LOGIC} = +5$ V, $-V_S = 0$ unless otherwise noted)[1]

Parameter	Conditions	AD790J/A Min	AD790J/A Typ	AD790J/A Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	AD790S Min	AD790S Typ	AD790S Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		45	50		45	50		45	50	ns
	T_{min} to T_{max}			50/60			50/60			65	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{min} to T_{max}	4.3			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{min} to T_{max}			0.5			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[2]			0.45	**1.5**		0.35	**0.6**		0.45	**1.5**	mV
	T_{min} to T_{max}			2.0			**0.85**			**2.0**	mV
Hysteresis[3]	T_{min} to T_{max}	0.3	0.5	0.75	**0.3**	0.5	**0.65**	**0.3**	0.7	**1.0**	mV
Bias Current	Either Input		2.7	5		2.0	**3.5**		2.7	5	μA
	T_{min} to T_{max}			7			5			**8**	μA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	μA
	T_{min} to T_{max}			0.3			**0.2**			**0.4**	μA
Power Supply											
Rejection Ratio dc	4.5 V≤V_S≤5.5 V	**80**	90		**86**	100		**80**	90		dB
	T_{min} to T_{max}	**76/76**	88		**82**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage				**±V_S**			**±V_S**			**±V_S**	V
Common Mode		0		+V_S−2 V	0		+V_S−2 V	0		+V_S−2 V	V
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level, V_{IL}	T_{min} to T_{max}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{min} to T_{max}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	**5**		2.3	**3.5**		2.3	5	μA
	T_{min} to T_{max}			7			5			**8**	μA
SUPPLY CHARACTERISTICS											
Supply Voltage[4]	T_{min} to T_{max}	4.5		7	**4.5**		**7**	**4.7**		**7**	V
Quiescent Current			10	**12**		10	**12**		10	**12**	mA
Power Dissipation				**60**			**60**			**60**	mW
TEMPERATURE RANGE											
Rated Performance	T_{min} to T_{max}	0 to +70/−40 to +85			0 to +70/−40 to +75			−55 to +125			°C
PACKAGE OPTIONS[5]											
Plastic (N-8)		AD790JN			AD790KN						
Cerdip (Q-8)		AD790AQ			AD790BQ			AD790SQ			
S Grade Chips Available											

NOTES

[1]Pin 1 tied to Pin 8, and Pin 4 tied to Pin 6.

[2]Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[3]Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[4]$-V_S$ must not be connected above ground.

[5]See Section 20 for package outline information.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.

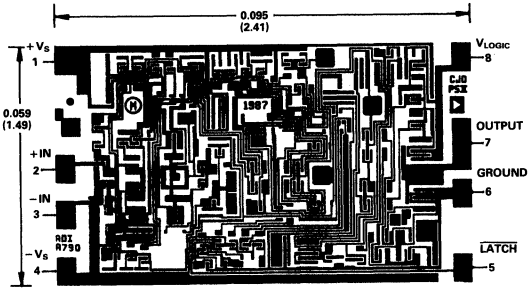
ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Differential Input Voltage . . . . . ±16.5 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
N . . . . . −65°C to +125°C
Q . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
Logic Supply Voltage . . . . . 7 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal characteristics: plastic N-8 package: θ_{JA} = 90°C/watt; ceramic Q-8 package: θ_{JA} = 110°C/watt, θ_{JC} = 22°C/watt.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Call factory for chip specifications.



ORDERING GUIDE

Grade	Temperature Range
AD790JN	0 to +70°C
AD790KN	0 to +70°C
AD790AQ	−40°C to +85°C
AD790BQ	−40°C to +85°C
AD790SQ	−55°C to +125°C
AD790SQ/883B	−55°C to +125°C
AD790S Chips	−55°C to +125°C

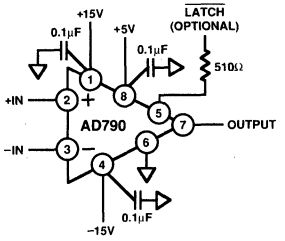


Figure 1. Basic Dual Supply Configuration

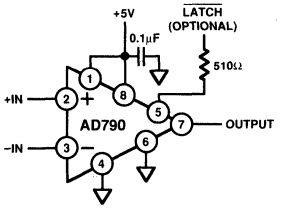


Figure 2. Basic Single Supply Configuration

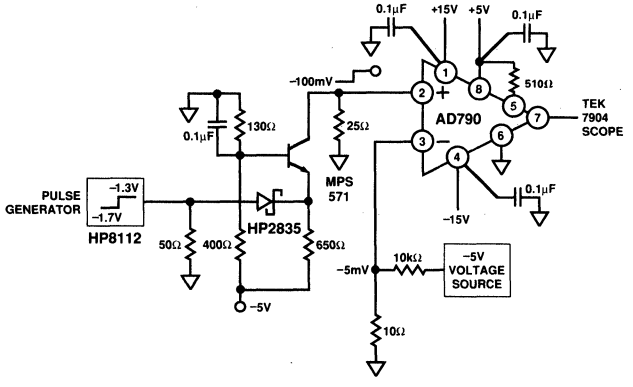


Figure 3. Response Time Test Circuit

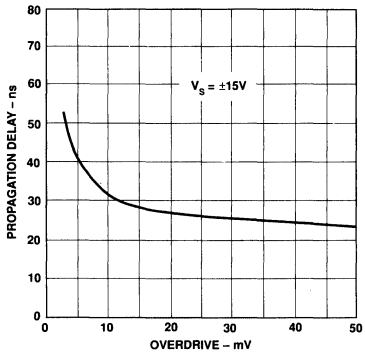


Figure 4. Propagation Delay vs. Overdrive

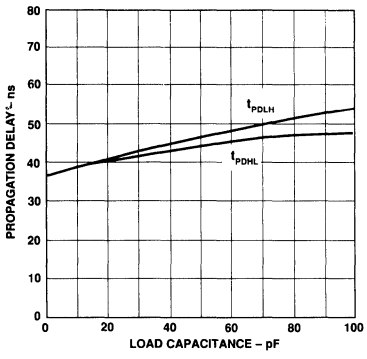


Figure 5. Propagation Delay vs. Load Capacitance

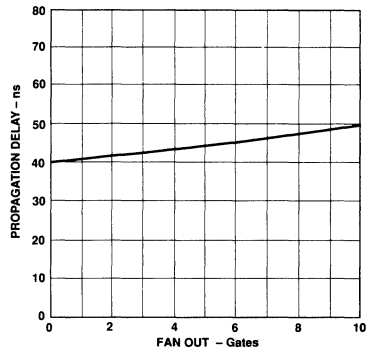


Figure 6. Propagation Delay vs. Fanout (LSTTL and CMOS)

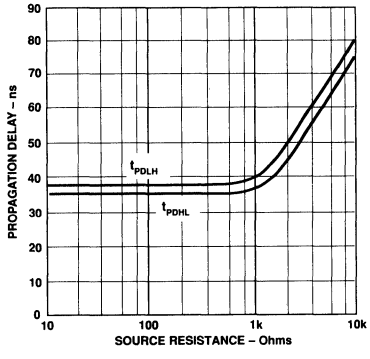


Figure 7. Propagation Delay vs. Source Resistance

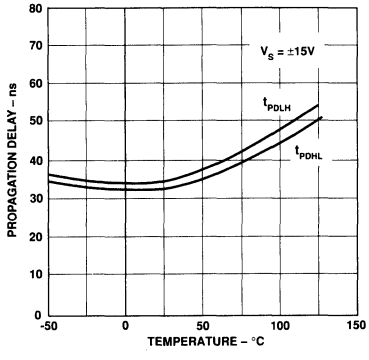


Figure 8. Propagation Delay vs. Temperature

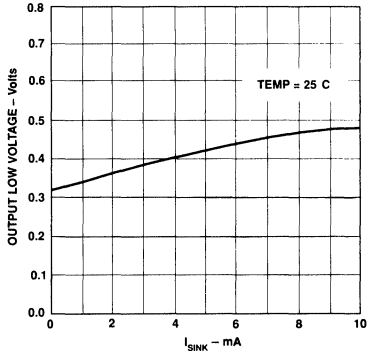


Figure 9. Output Low Voltage vs. Sink Current

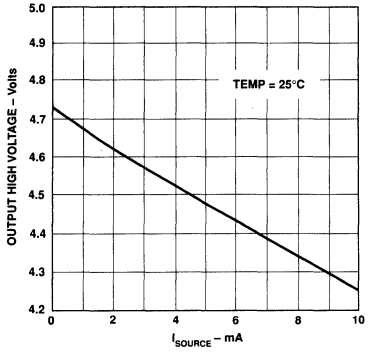


Figure 10. Output High Voltage vs. Source Current

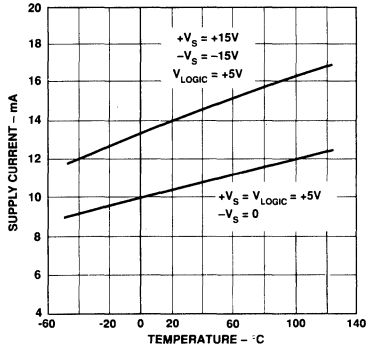
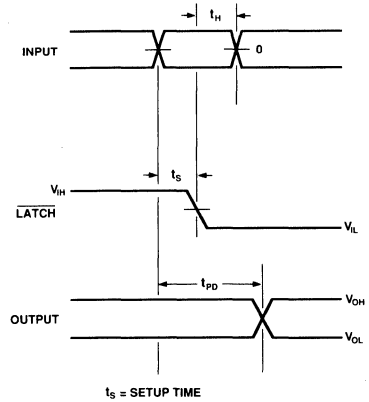


Figure 11. Total Supply Current vs. Temperature



t_S = SETUP TIME
t_H = HOLD TIME
t_{PD} = COMPARATOR RESPONSE TIME

Figure 12. Latch Timing

CIRCUIT DESCRIPTION

The AD790 possesses the overall characteristics of a standard monolithic comparator: differential inputs, high gain and a logic output. However, its function is implemented with an architecture which offers several advantages over previous comparator designs. Specifically, the output stage alleviates some of the limitations of classic "TTL" comparators and provides a symmetric output. A simplified representation of the AD790 circuitry is shown in Figure 13.

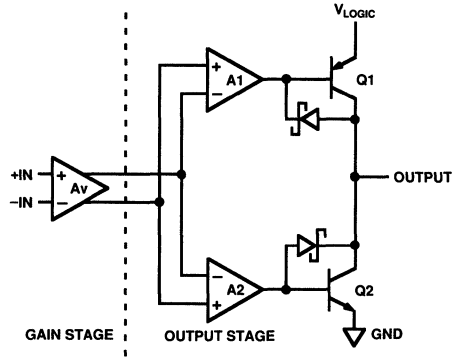


Figure 13. AD790 Block Diagram

The output stage takes the amplified differential input signal and converts it to a single-ended logic output. The output swing is defined by the pull-up PNP and the pull-down NPN. These produce inherent rail-to-rail output levels, compatible with CMOS logic, as well as TTL, without the need for clamping to internal bias levels. Furthermore, the pull-up and pull-down levels are symmetric about the center of the supply range and are referenced off the V_{LOGIC} supply and ground. The output stage has nearly symmetric dynamic drive capability, yielding equal rise and fall times into subsequent logic gates.

Unlike classic TTL or CMOS output stages, the AD790 circuit does not exhibit large current spikes due to unwanted current flow between the output transistors. The AD790 output stage has a controlled switching scheme in which amplifiers A1 and A2 drive the output transistors in a manner designed to reduce the current flow between Q1 and Q2. This also helps minimize the disturbances feeding back to the input which can cause troublesome oscillations.

The output high and low levels are well controlled values defined by V_{LOGIC} (+5 V), ground and the transistor equivalent "Schottky" clamps and are compatible with TTL and CMOS logic requirements. The fanout of the output stage is shown in Figure 6 for standard LSTTL or HCMOS gates. Output drive behavior vs. capacitive load is shown in Figure 5.

HYSTERESIS

The AD790 uses internal feedback to develop hysteresis about the input reference voltage. Figure 14 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can be either positive or negative. The hysteresis voltage (V_H) is one-half the width of the

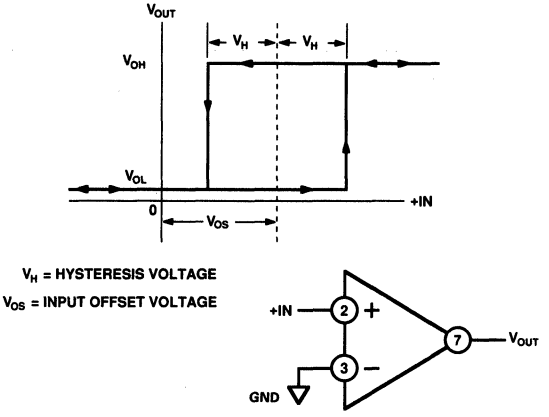


Figure 14. Hysteresis Definitions

hysteresis range. This built-in hysteresis allows the AD790 to avoid oscillation when an input signal slowly crosses the ground level.

SUPPLY VOLTAGE CONNECTIONS

The AD790 may be operated from either single or dual supply voltages. Internally, the V_{LOGIC} circuitry and the analog front-end of the AD790 are connected to separate supply pins. If dual supplies are used, any combination of voltages in which $+V_S \geq V_{LOGIC} - 0.5$ V and $-V_S \leq 0$ may be chosen. For single supply operation (i.e. $+V_S = V_{LOGIC}$), the supply voltage can be operated between 4.5 V and 7 V. Figure 15 shows some other examples of typical supply connections possible with the AD790.

BYPASSING AND GROUNDING

Although the AD790 is designed to be stable and free from oscillations, it is important to properly bypass and ground the power supplies. Ceramic 0.1 μF capacitors are recommended and should be connected directly at the AD790's supply pins. These capacitors provide transient currents to the device during comparator switching. The AD790 has three supply voltage pins, $+V_S$, $-V_S$ and V_{LOGIC}. It is important to have a common ground lead on the board for the supply grounds and the GND pin of the AD790 to provide the proper return path for the supply current.

LATCH OPERATION

The AD790 has a latch function for retaining input information at the output. The comparator decision is "latched" and the output state is held when Pin 5 is brought low. As long as Pin 5 is kept low, the output remains in the high or low state , and does not respond to changing inputs. Proper capture of the input signal requires that the timing relationships shown in Figure 12 are followed. Pin 5 should be driven with CMOS or TTL logic levels.

The output of the AD790 will respond to the input when Pin 5 is at a high logic level. When not in use, Pin 5 should be connected to the positive logic supply. When using dual supplies, it is recommended that a 510 Ω resistor be placed in series with Pin 5 and the driving logic gate to limit input currents during power up.

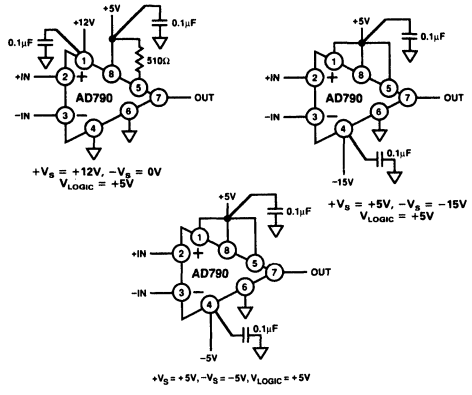


Figure 15. Typical Power Supply Connections

Window Comparator for Over-Voltage Detection

The wide differential input range of the AD790 makes it suitable for monitoring large amplitude signals. The simple overvoltage detection circuit shown in Figure 16 illustrates direct connection of the input signal to the high impedance inputs of the comparator without the need for special clamp diodes to limit the differential input voltage across the inputs.

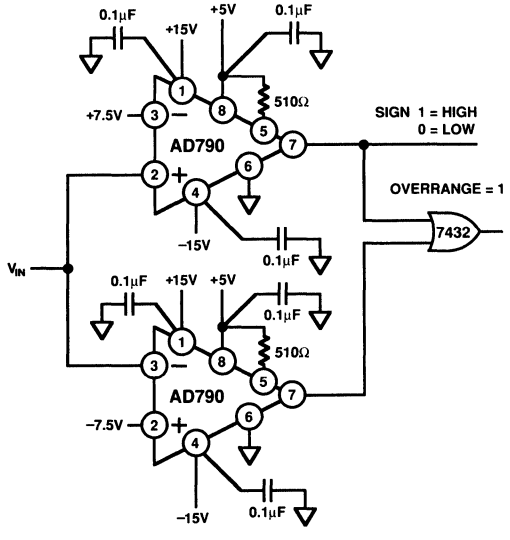


Figure 16. Overvoltage Detector

Single Supply Ground Referred Overload Detector

The AD790 is useful as an overload detector for sensitive loads that must be powered from a single supply. A simple ground referenced overload detector is shown in Figure 16. The comparator senses a voltage across a PC board trace and compares that to a reference (trip) voltage established by the comparator's minus supply current through a 2.7 Ω resistor. This sets up a 10 mV reference level that is compared to the sense voltage. The minus supply current is proportional to absolute temperature and compensates for the change in the sense resistance with temperature. The width and length of the PC board trace determine the resistance of the trace and consequently the trip current level.

I_{LIMIT} = 10 mV/R_{SENSE}

R_{SENSE} = rho (trace length/trace width)

rho = resistance of a unit square of trace

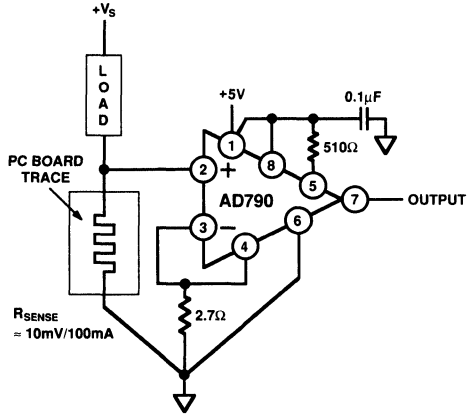


Figure 17. Ground Referred Overload Detector Circuit

Precision Full-Wave Rectifier

The high speed and precision of the AD790 make it suitable for use in the wide dynamic range full-wave rectifier shown in Figure 18. This circuit is capable of rectifying low level signals as small as a few mV or as high as 10 V. Input resolution, propagation delay and op amp settling will ultimately limit the maximum input frequency for a given accuracy level. Total comparator plus switch delay is approximately 100 ns, which limits the maximum input frequency to 1 MHz for clean rectification.

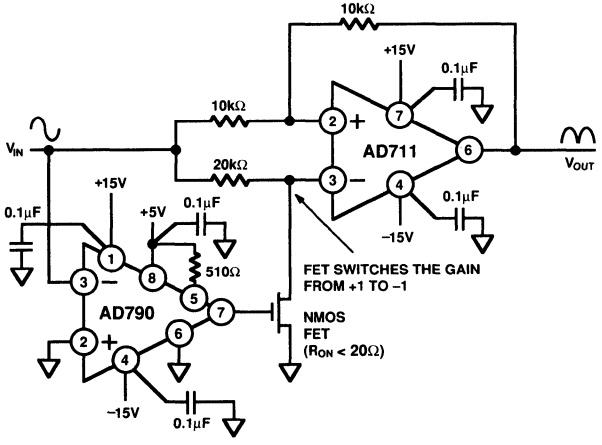


Figure 18. Precision Full-Wave Rectifier

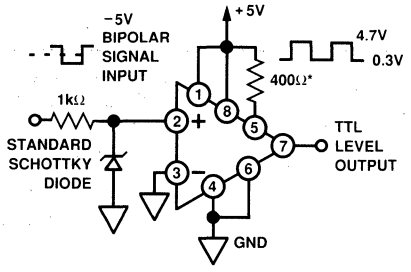


Figure 19. A Bipolar to CMOS TTL Line Receiver

Bipolar to CMOS/TTL

It is sometimes desirable to translate a bipolar signal (e.g., ±5 V) coming from a communications cable or another section of the system to CMOS/TTL logic levels; such an application is referred to as a line receiver. Previously, the interface to the bipolar signal required either a dual (±) power supply or a reference voltage level about which the line receiver would switch. The AD790 may be used in a simple circuit to provide a unique capability: the ability to receive a bipolar signal while powered from a single +5 V supply. Other comparators cannot perform this task. Figure 19 shows a 1 kΩ resistor in series with the input signal which is then clamped by a Schottky diode, holding the input of the comparator at 0.4 V below ground. Although the comparator is specified for a common mode range down to $-V_S$, (in this case ground)it is permissible to bring one of the inputs a few hundred mV below ground. The comparator switches around this level and produces a CMOS/TTL compatible swing. The circuit will operate to switching frequencies of 20 MHz.

ANALOG DEVICES

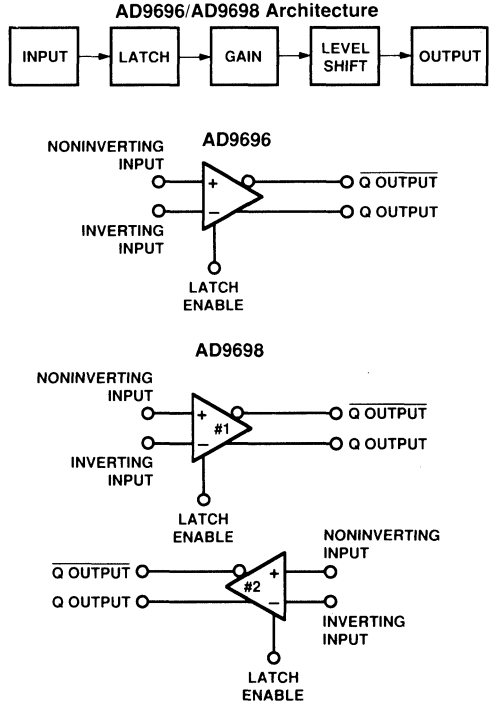
Ultrafast TTL Comparators

AD9696/AD9698

FEATURES
4.5 ns Propagation Delay
200 ps Maximum Propagation Delay Dispersion
Single +5 V or ±5 V Supply Operation
Complementary Matched TTL Outputs

APPLICATIONS
High Speed Line Receivers
Peak Detectors
Window Comparators
High Speed Triggers
Ultrafast Pulse Width Discriminators

AD9696/AD9698 FUNCTONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD9696 and AD9698 are ultrafast TTL-compatible voltage comparators able to achieve propagation delays previously possible only in high performance ECL devices. The AD9696 is a single comparator providing 4.5 ns propagation delay, 200 ps maximum delay dispersion and 1.7 ns setup time. The AD9698 is a dual comparator with equally high performance; both devices are ideal for critical timing circuits in such applications as ATE, communications receivers and triggers.

Both devices allow the use of either a single +5 V supply or ±5 V supplies. The choice of supplies determines the common mode input voltage range available: −2.2 V to +3.7 V for ±5 V operation, +1.4 V to +3.7 V for single +5 V supply operation.

The differential input stage features high precision, with offset voltages which are less than 2 mV and offset currents less than 1 μA. A latch enable input is provided to allow operation in either sample-and-hold or track-and-hold applications.

The AD9696 and AD9698 are both available as commercial temperature range devices operating from ambient temperatures of 0 to +70°C, and as extended temperature range devices for ambient temperatures from −55°C to +125°C. Both versions are available screened to MIL-STD-883 class B. Contact the factory for information regarding higher reliability screening.

Package options for the AD9696 include a 10-pin TO-100 metal can, an 8-pin ceramic DIP, an 8-pin small outline plastic package and an 8-pin plastic DIP. The AD9698 is available in a 16-pin ceramic DIP a 16-pin plastic DIP and a 16-pin small outline plastic package.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S/-V_S$) . . . . . +7 V/−7 V
Input Voltage Range . . . . . ±5 V
Differential Input Voltage . . . . . 5.4 V
Latch Enable Voltage . . . . . −0.5 V to $+V_S$
Output Current (Continuous) . . . . . 20 mA
Power Dissipation . . . . . 600 mW

Operating Temperature Range[2]
AD9696/AD9698KH/KN/KQ/KR[3] . . . . . 0 to +70°C
AD9696/AD9698TH/TQ[3] . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature
KH/KQ/TH/TQ Suffixes . . . . . +175°C
KN/KR Suffixes . . . . . +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2 V and +5.0 V; load as specified in Note 4, unless otherwise indicated)

Parameter	Temp	Test Level	Military Subgroup[5]	0 to +70°C AD9696/AD9698 KH/KN/KQ/KR[3] Min	Typ	Max	−55°C to +125°C AD9696/AD9698 TH/TQ[3] Min	Typ	Max	Units
INPUT CHARACTERISTICS										
Input Offset Voltage[6]	+25°C	I	1		1.0	2.0		1.0	2.0	mV
	Full	VI	2, 3			3.0			3.0	mV
Input Offset Voltage Drift	Full	V			10			10		µV/°C
Input Bias Current	+25°C	I	1		16	55		16	55	µA
	Full	VI	2, 3			110			110	µA
Input Offset Current	+25°C	I	1		0.4	1.0		0.4	1.0	µA
	Full	VI	2, 3			1.3			1.3	µA
Input Capacitance	+25°C	V			3			3		pF
Input Voltage Range										
±5.0 V	Full	VI	1, 2, 3	−2.2		+3.7	−2.2		+3.7	V
+5.0 V	Full	VI	1, 2, 3	+1.4		+3.7	+1.4		+3.7	V
Common Mode Rejection Ratio										
±5.0 V	Full	VI	1, 2, 3	80	85		80	85		dB
+5.0 V	Full	VI	1, 2, 3	57	63		57	63		dB
LATCH ENABLE INPUT										
Logic "1" Voltage Threshold	Full	VI	1, 2, 3	2.0			2.0			V
Logic "0" Voltage Threshold	Full	VI	1, 2, 3			0.8			0.8	V
Logic "1" Current	Full	VI	1, 2, 3			10			10	µA
Logic "0" Current	Full	VI	1, 2, 3			1			1	µA
DIGITAL OUTPUTS										
Logic "1" Voltage (Source 4 mA)	Full	VI	1, 2, 3	2.7	3.5		2.7	3.5		V
Logic "0" Voltage (Sink 10 mA)	Full	VI	1, 2, 3		0.4	0.5		0.4	0.5	V
SWITCHING PERFORMANCE										
Propagation Delay (t_{PD})[7]										
Input to Output HIGH	Full	IV	9, 10, 11		4.5	7.0		4.5	7.0	ns
Input to Output LOW	Full	IV	9, 10, 11		4.5	7.0		4.5	7.0	ns
Latch Enable to Output HIGH	+25°C	IV	9, 10, 11		6.5	8.5		6.5	8.5	ns
Latch Enable to Output LOW	+25°C	IV	9, 10, 11		6.5	8.5		6.5	8.5	ns
Delta Delay Between Outputs	+25°C	IV			0.5	1.5		0.5	1.5	ns
Propagation Delay Dispersion										
10 mV to 100 mV Overdrive	+25°C	V			100			100		ps
100 mV to 1.0 V Overdrive	+25°C	IV			100	200		100	200	ps
Latch Enable										
Pulse Width [$t_{PW(E)}$]	+25°C	IV		3.5	2.5		3.5	2.5		ns
Setup Time (t_S)	+25°C	IV		3	1.7		3	1.7		ns
Hold Time (t_H)	+25°C	IV		3	1.9		3	1.9		ns

Parameter	Temp	Test Level	Military Subgroup[5]	0 to +70°C AD9696/AD9698 KH/KN/KQ/KR[3] Min	Typ	Max	−55°C to +125°C AD9696/AD9698 TH/TQ[3] Min	Typ	Max	Units
POWER SUPPLY[8]										
Positive Supply Current[9]										(+5.0 V)
AD9696	Full	VI	1, 2, 3		26	32		26	32	mA
AD9698	Full	VI	1, 2, 3		52	64		52	64	mA
Negative Supply Current[10]										(−5.2 V)
AD9696	Full	VI	1, 2, 3		2.5	4.0		2.5	4.0	mA
AD9698	Full	VI	1, 2, 3		5.0	8.0		5.0	8.0	mA
Power Dissipation										
AD9696 +5.0 V	Full	V			130			130		mW
AD9696 ±5.0 V	Full	V			146			146		mW
AD9698 +5.0 V	Full	V			260			260		mW
AD9698 ±5.0 V	Full	V			292			292		mW
Power Supply Rejection Ratio[11]	+25°C	VI	1, 2, 3	70			70			dB
	Full			65			65			dB

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances:

AD9696 Metal Can θ_{JA} = 170°C/W; θ_{JC} = 50°C/W
AD9696 Ceramic DIP θ_{JA} = 110°C/W; θ_{JC} = 20°C/W
AD9696 Plastic DIP θ_{JA} = 160°C/W; θ_{JC} = 30°C/W
AD9696 Plastic SOIC θ_{JA} = 180°C/W; θ_{JC} = 30°C/W
AD9698 Ceramic DIP θ_{JA} = 90°C/W; θ_{JC} = 25°C/W
AD9698 Plastic DIP θ_{JA} = 100°C/W; θ_{JC} = 20°C/W
AD9698 Plastic SOIC θ_{JA} = 120°C/W; θ_{JC} = 20°C/W

[3]Suffixes KH and TH apply only to model AD9696; AD9698 not available in metal can.

[4]Load circuit has 420 Ω from $+V_S$ to output; 460 Ω from output to ground.

[5]Military subgroups apply only to military-qualified devices.

[6]$R_S \leq 100\ \Omega$.

[7]Propagation delays tested with 100 mV pulse; 20 mV overdrive.

[8]Supply voltages should remain stable within ±5% for normal operation. Output not loaded.

[9]Specification applies to both +5 V and ±5 V supply operation.

[10]Specification applies to only ±5 V supply operation.

[11]Measured with nominal values ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

AD9696/AD9698 ORDERING INFORMATION

Model	Package	Temperature	Package Options*
AD9696KH	TO-100 Can	0 to +70°C	H-10A
AD9696KN	Plastic DIP	0 to +70°C	N-8
AD9696KR	SOIC	0 to +70°C	R-8
AD9696KQ	Cerdip	0 to +70°C	Q-8
AD9696TH	TO-100 Can	−55°C to +125°C	H-10A
AD9696TQ	Cerdip	−55°C to +125°C	Q-8
AD9698KN	Plastic DIP	0 to +70°C	N-16
AD9698KR	SOIC	0 to +70°C	R-16
AD9698KQ	Cerdip	0 to +70°C	Q-16
AD9698TQ	Cerdip	−55°C to +125°C	Q-16

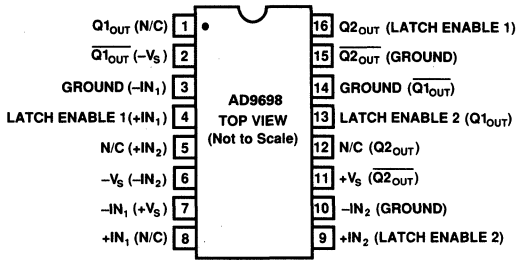
*See Section 20 for package outline information.

EXPLANATION OF MILITARY SUBGROUPS

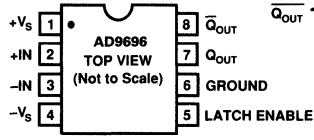
Subgroup 1 – Static tests at +25°C. (5% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 – Static tests at maximum rated operating temperature.
Subgroup 3 – Static tests at minimum rated operating temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated operating temperature.
Subgroup 6 – Dynamic tests at minimum rated operating temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated operating temperature.
Subgroup 11 – Switching tests at minimum rated operating temperature.
Subgroup 12 – Periodically sample tested.

PIN CONFIGURATIONS

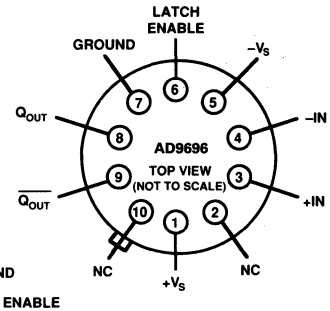
Plastic DIP (N) and Ceramic DIP (R) Packages [SOIC (R) Package Pinouts shown in ( )]



Plastic DIP (N) Ceramic DIP (Q) and SOIC (R) Packages

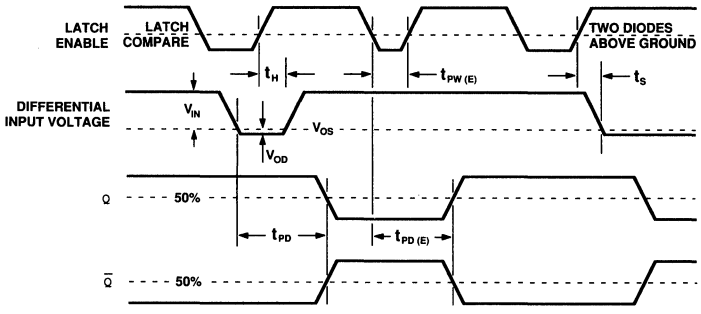


TO-100 Metal Can (H) Package



AD9696/AD9698 PIN DESCRIPTIONS

Name	Function
$Q1_{OUT}$	One of two complementary outputs. $Q1_{OUT}$ will be at logic HIGH if voltage at $+IN_1$ is greater than voltage at $-IN_1$ and LATCH ENABLE 1 is at logic LOW.
$\overline{Q1_{OUT}}$	One of two complementary outputs. $\overline{Q1_{OUT}}$ will be at logic HIGH if voltage at $-IN_1$ is greater than voltage at $+IN_1$ and LATCH ENABLE 1 is at logic LOW.
GROUND	Analog and digital ground return. All GROUND pins should be connected together and to a low impedance ground plane near the comparator.
LATCH ENABLE 1	Output at $Q1_{OUT}$ will track differential changes at the inputs when LATCH ENABLE 1 is at logic LOW. When LATCH ENABLE 1 is at logic HIGH, the output at $Q1_{OUT}$ will reflect the input state at the application of the latch command, delayed by the Latch Enable Setup Time (t_S). Since the architecture of the input stage (see block diagram) is faster than the logic of the latch stage, data will typically be latched if applied to the comparator(s) within 1.7 ns after the latch. This is the Setup Time (t_S); for guaranteed performance, t_S must be 3 ns.
N/C	No internal connection to comparator.
$-V_S$	Negative power supply connection; nominally −5.2 V.
$-IN_1$	Inverting input of differential input stage for Comparator #1.
$+IN_1$	Noninverting input of differential input stage for Comparator #1.
$+IN_2$	Noninverting input of differential input stage for Comparator #2.
$-IN_2$	Inverting input of differential input stage for Comparator #2.
$+V_S$	Positive power supply connection; nominally +5 V.
LATCH ENABLE 2	Output at $Q2_{OUT}$ will track differential changes at the inputs when LATCH ENABLE 2 is at logic LOW. When LATCH ENABLE 2 is at logic HIGH, the output at $Q2_{OUT}$ will reflect the input state at the application of the latch command, delayed by the Latch Enable Setup Time (t_S). Since the architecture of the input stage (see block diagram) is faster than the logic of the latch stage, data will typically be latched if applied to the comparator(s) within 1.7 ns after the latch. This is the Setup Time (t_S); for guaranteed performance, t_S must be 3 ns.
$\overline{Q2_{OUT}}$	One of two complementary outputs. $\overline{Q2_{OUT}}$ will be at logic HIGH if voltage at $-IN_2$ is greater than voltage at $+IN_2$ and LATCH ENABLE 2 is at logic LOW.
$Q2_{OUT}$	One of two complementary outputs. $Q2_{OUT}$ will be at logic HIGH if voltage at $+IN_2$ is greater than voltage at $-IN_2$ and LATCH ENABLE 2 is at logic LOW.

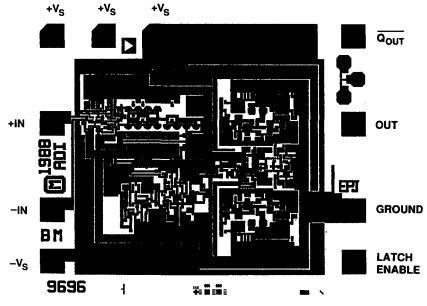


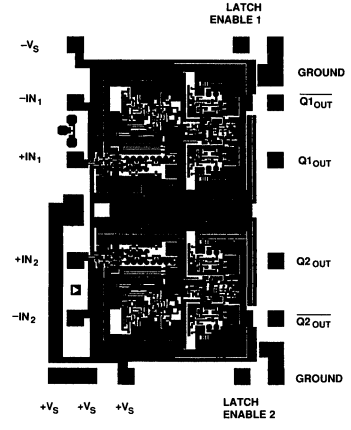
t_S – MINIMUM SETUP TIME (Typically 1.7ns)
t_H – MINIMUM HOLD TIME (Typically 1.9ns)
t_{PD} – INPUT TO OUTPUT DELAY
$t_{PD(E)}$ – LATCH ENABLE TO OUTPUT DELAY
$t_{PW(E)}$ – MINIMUM LATCH ENABLE PULSE WIDTH (Typically 2.5ns)
V_{OS} – INPUT OFFSET VOLTAGE
V_{OD} – OVERDRIVE VOLTAGE

AD9696/AD9698 Timing Diagram

DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions AD9696	59×71×15 (±2) mils
AD9698	79×109×15 (±2) mils
Pad Dimensions	4×4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride





THEORY OF OPERATION

Refer to the block diagram of the AD9696/AD9698 comparators. The AD9696 and AD9698 TTL voltage comparator architecture consists of five basic stages: input, latch, gain, level shift and output. Each stage is designed to provide optimal performance and make it easy to use the comparators.

The input stage operates with either a single +5-volt supply, or with a +5-volt supply and a −5.2-volt supply. For optimum power efficiency, the remaining stages operate with only a single +5-volt supply. The input stage is an input differential pair without the customary emitter follower buffers. This configuration increases input bias currents but maximizes the input voltage range.

A latch stage allows the most recent output state to be retained as long as the latch input is held high. In this way, the input to the comparator can be changed without any change in the output state. As soon as the latch enable input is switched to LOW, the output changes to the new value dictated by the signal applied to the input stage.

The gain stage assures that even with small values of input voltage, there will be sufficient levels applied to the following stages to cause the output to switch TTL states as required. A level shift stage between the gain stage and the TTL output stage guarantees that appropriate voltage levels are applied from the gain stage to the TTL output stage.

Only the output stage uses TTL logic levels; this minimum use of TTL circuits maximizes speed and minimizes power consumption. The outputs are clamped with Schottky diodes to assure that the rising and falling edges of the output signal are closely matched.

The AD9696 and AD9698 represent the state of the art in high speed TTL voltage comparators. Great care has been taken to optimize the propagation delay dispersion performance. This assures that the output delays will remain constant despite varying levels of input overdrive. This characteristic, along with closely matched rising and falling outputs, provides extremely consistent results at previously unattainable speeds.

APPLICATIONS

Window Comparator

In a wide range of applications, it is necessary to determine when a signal's voltage level is within (or outside) a particular voltage range. ATE, transient detectors, communications receivers, ESM and other equipment all require this type of information. Figure 1 shows a versatile window comparator which combines very high speed, TTL compatibility and ease of application.

To establish a "window" with upper and lower voltage thresholds, two comparators are required. The circuit which is shown uses the AD9698 dual ultrafast TTL comparator; this means a substantial cost and space savings versus the same design using two single comparators. Additionally, since the AD9698 contains two tightly matched comparators on a single IC, superior dc and propagation time skew performance can be achieved.

The window is established by providing the desired $+V_{REF}$ to the noninverting input of the top comparator and placing the lower limit, $-V_{REF}$, at the inverting input on the bottom comparator. The signal of interest is strapped across the remaining inputs. The outputs are connected to an AND gate. When a signal resides inside the window established by the references, the output of the gate goes high. Whenever the signal is outside the window, the output is low. An indication of a signal above or below the reference levels can be monitored at the comparators' complementary outputs.

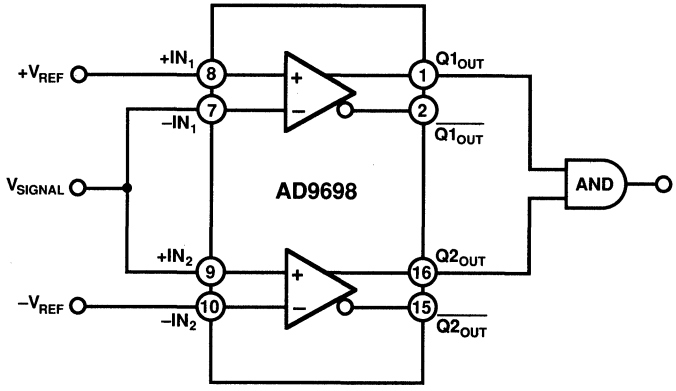


Figure 1. AD9698 Used as Window Detector

Crystal Oscillator

Oscillators are used in a wide variety of applications from audio circuits to waveform generators; from ATE triggers and telecommunications transceivers to radar. Figure 2 shows a versatile and inexpensive oscillator. The circuit uses the AD9696, in a positive feedback mode, and is capable of generating accurate and stable oscillations with frequencies ranging from 1 MHz to more than 40 MHz.

To generate oscillations from 1 to 25 MHz, a fundamental mode crystal is used without the dc blocking capacitor and choke. The parallel capacitor on the inverting input is selected for stability (0.1 μF for 1–10 MHz; 220 pF for frequencies above 10 MHz).

When generating frequencies using a nonfundamental mode crystal, a choke and dc blocking capacitor are added. As an example, a 36 MHz oscillator can be achieved by using a 36 MHz crystal operating on its third overtone. To suppress oscillation at the 12 MHz fundamental, the value of the choke is chosen to provide a low reactive impedance at the fundamental frequency while maintaining a high reactive impedance at the desired output frequency (for 36 MHz operation, L = 1.8 μH). The shunt capacitor at the inverting input has a value of 220 pF for a stable 36 MHz frequency.

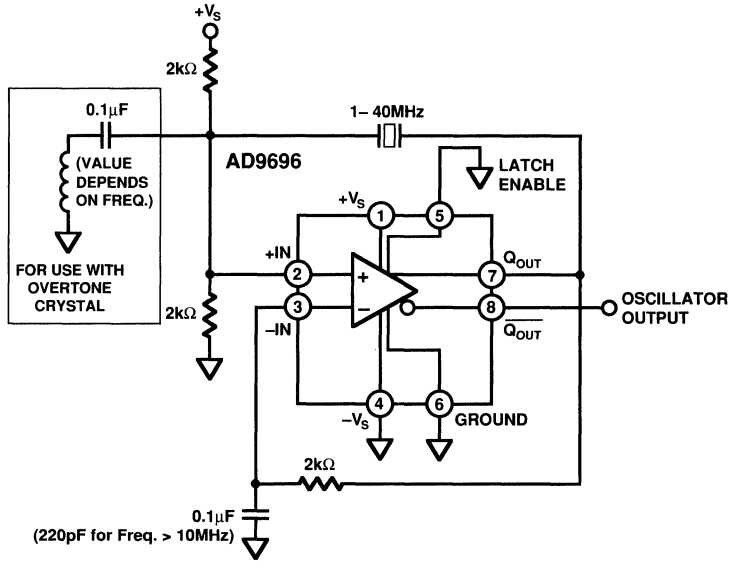


Figure 2. AD9696 Oscillator Circuit (Based on DIP Pinouts)

LAYOUT CONSIDERATIONS

When working with high speed circuits, proper layout is critical. Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. In addition, digital signal paths should be kept short, and run lengths should be matched to avoid propagation delay mismatch. All analog signals should be kept as far away from digital signal paths as possible; this reduces the amount of digital switching noise that might be capacitively coupled into the analog section of the circuit.

In high speed circuits, layout of the ground circuit is the most important factor. A single, low impedance ground plane, on the component side of the board, will reduce noise in the circuit ground. It is especially important to maintain continuity of the ground plane under and around the AD9696 or AD9698.

Sockets limit the dynamic performance of the device and should be used only for prototypes or evaluation.

ANALOG DEVICES

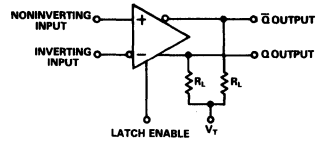
Ultrafast Comparators

AD96685/AD96687

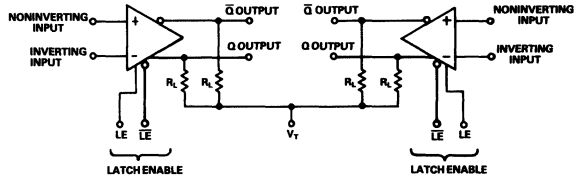
FEATURES
2.5ns Propagation Delay
0.5ns Latch Setup Time
90dB CMRR
+5V, −5.2V Supply Voltages

APPLICATIONS
High Speed Triggers
High Speed Line Receivers
Peak Detectors
Threshold Detectors

AD96685/AD96687 FUNCTIONAL BLOCK DIAGRAMS



AD96685



AD96687

GENERAL DESCRIPTION

The AD96685 and the AD96687 are ultrafast voltage comparators. The AD96685 and the AD96687 are manufactured in a high performance bipolar process which allows improved speed and dc accuracy. The AD96685 is a single comparator with a 2.5ns propagation delay, 50ps dispersion, and the AD96687 is an equally fast dual comparator.

Both devices employ a high precision differential input stage with a common-mode range from −2.5V to +5.0V. The AD96685 and the AD96687 provide complementary digital outputs which are fully ECL compatible. The output stage is capable of driving 50Ω terminated transmission lines given the 30mA output drive capacity. In addition to this, a latch enable input is provided, allowing operation in either a sample-hold mode or a track-hold mode.

The AD96685 and the AD96687 are both available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. The AD96685 is available in a 10-pin TO-100 metal can, a 16-pin ceramic package, a 16-pin SOIC, and a 20-pin PLCC. The AD96687 is available in a 16-pin ceramic package, a 16-pin SOIC and a 20-pin PLCC. Both comparators are also available in an extended temperature range LCC package.

ORDERING INFORMATION

Device	Type	Temperature Range	Description	Package Options*
AD96685BH	Single	−25°C to +85°C	10-Pin Can, Industrial	H-10A
AD96685BP	Single	−25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96685BQ	Single	−25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96685BR	Single	−25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96685TE/883	Single	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD96685TH/883	Single	−55°C to +125°C	10-Pin Can, Extended Temperature	H-10A
AD96685TQ/883	Single	−55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16
AD96687BP	Dual	−25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96687BQ	Dual	−25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96687BR	Dual	−25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96687TE/883	Dual	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD96687TQ/883	Dual	−55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16

*See Section 20 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$)	+6.5V	Operating Temperature Range[3]	
Negative Supply Voltage ($-V_S$)	−6.5V	AD96685/87/BH/BQ/BP/BR	−25°C to +85°C
Input Voltage Range[2]	±5V	AD96685/87/TE/TH/TQ	−55°C to +125°C
Differential Input Voltage	5.5V	Storage Temperature Range	−55°C to +150°C
Latch Enable Voltage	$-V_S$ to 0V	Junction Temperature	+175°C
Output Current	30mA	Lead Soldering Temperature (10sec)	+300°C

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = +5.0V; Negative Supply Voltage = −5.2V, unless otherwise stated)

				Industrial Temp. Range −25°C to +85°C						Military Temp. Range −55°C to +125°C						
				AD96685BH/BQ/BP/BR			AD96687BQ/BP/BR			AD96685TE/TH/TQ/883			AD96687TE/TQ/883			
Parameter	Temp	Test Level	Mil[4] Sub Group	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS																
Input Offset Voltage[5]	+25°C	I	1		1	2		1	2		1	2		1	2	mV
	Full	VI	2,3			3			3			3			3	mV
Input Offset Drift	Full	V			20			20			20			20		µV/°C
Input Bias Current	+25°C	I	1		7	10		7	10		7	10		7	10	µA
	Full	VI	2,3			13			13			16			16	µA
Input Offset Current	+25°C	I	1		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0	µA
	Full	VI	2,3			1.2			1.2			1.2			1.2	µA
Input Resistance	+25°C	V			200			200			200			200		kΩ
Input Capacitance	+25°C	V			2			2			2			2		pF
Input Voltage Range[6]	Full	VI	1,2,3	−2.5		+5.0	−2.5		+5.0	−2.5		+5.0	−2.5		+5.0	V
Common-Mode Rejection Ratio	Full	VI	4,5,6	80	90		80	90		80	90		80	90		dB
ENABLE INPUT																
Logic "1" Voltage	Full	VI	1,2,3	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI	1,2,3			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI	1,2,3			40			40			40			40	µA
Logic "0" Current	Full	VI	1,2,3			5			5			5			5	µA
DIGITAL OUTPUTS[7]																
Logic "1" Voltage	Full	VI	1,2,3	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI	1,2,3			−1.5			−1.5			−1.5			−1.5	V
SWITCHING PERFORMANCE[7]																
Propagation Delays[8]																
Input to Output HIGH	+25°C	IV	9		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Input to Output LOW	+25°C	IV	9		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output HIGH	+25°C	IV	9		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output LOW	+25°C	IV	9		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Dispersion[9]	+25°C	V			50			50			50			50		ps
Latch Enable																
Minimum Pulse Width	+25°C	IV	12		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	+25°C	IV	12		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	+25°C	IV	12		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[10]																
Positive Supply Current (+5.0V)	Full	VI	1,2,3		8	9		15	18		8	9		15	18	mA
Negative Supply Current (−5.2V)	Full	VI	1,2,3		15	18		31	36		15	18		31	36	mA
Power Supply Rejection Ratio[11]	Full	VI	4,5,6	60	70		60	70		60	70		60	70		dB

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Under no circumstances should the input voltages exceed the supply voltages.

[3]Typical thermal impedances . . .

AD96685 Metal Can	θ_{JA} = 172°C/W; θ_{JC} = 52°C/W
AD96685 Ceramic	θ_{JA} = 115°C/W; θ_{JC} = 57°C/W
AD96685 LCC	θ_{JA} = 172°C/W; θ_{JC} = 65°C/W
AD96685 SOIC	θ_{JA} = 170°C/W; θ_{JC} = 60°C/W
AD96685 PLCC	θ_{JA} = 88°C/W; θ_{JC} = 45°C/W
AD96687 Ceramic	θ_{JA} = 115°C/W; θ_{JC} = 57°C/W
AD96687 LCC	θ_{JA} = 82°C/W; θ_{JC} = 31°C/W
AD96687 SOIC	θ_{JA} = 92°C/W; θ_{JC} = 47°C/W
AD96687 PLCC	θ_{JA} = 81°C/W; θ_{JC} = 45°C/W

[4]Military subgroups apply to military qualified components only.

[5]R_S = 100Ω.

[6]Input Voltage Range can be extended to −3.3V if $-V_S$ = −6.0V.

[7]Outputs terminated through 50Ω to −2.0V.

[8]Propagation delays measured with 100mV pulse (10mV overdrive), to 50% transition point of the output.

[9]Change in propagation Delay from 100mV to 1V input overdrive.

[10]Supply voltages should remain stable within ±5% for normal operation.

[11]Measured at ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

- I – 100% production tested.
- II – 100% production tested at +25°C, and sample tested at specified temperatures.
- III – Sample tested only.
- IV – Parameter is guaranteed by design and characterization testing.
- V – Parameter is a typical value only.
- VI – All devices are 100% production tested at +25°C; 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

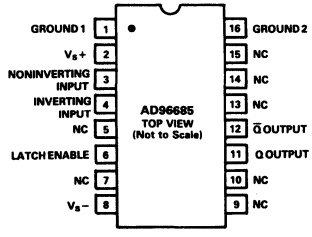
Subgroup 1 – Static tests at +25°C.	Subgroup 5 – Dynamic tests at max rated oper. temp.	Subgroup 9 – Switching tests at +25°C.
Subgroup 2 – Static tests at max rated oper. temp.	Subgroup 6 – Dynamic tests at min rated oper. temp.	Subgroup 10 – Switching tests at max rated oper. temp.
Subgroup 3 – Static tests at min rated oper. temp.	Subgroup 7 – Functional tests at +25°C.	Subgroup 11 – Switching tests at min rated oper. temp.
Subgroup 4 – Dynamic tests at +25°C.	Subgroup 8 – Functional tests at max and min rated oper. temp.	Subgroup 12 – Periodically sample tested.

FUNCTIONAL DESCRIPTION

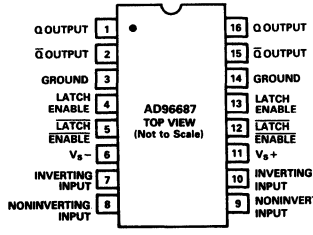
Pin Name	Description
$+V_S$	– Positive supply terminal, nominally +5.0V.
NONINVERTING INPUT	– Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	– Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
LATCH ENABLE	– In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with LATCH ENABLE for the AD96687.
$\overline{\text{LATCH ENABLE}}$	– In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. LATCH ENABLE must be driven in conjunction with $\overline{\text{LATCH ENABLE}}$ for the AD96687.
$-V_S$	– Negative supply terminal, nominally −5.2V.
Q	– One of two complementary outputs. Q will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD96687 only) for additional information.
$\overline{Q}$	– One of two complementary outputs. $\overline{Q}$ will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD96687 only) for additional information.
GROUND 1	– One of two grounds, but primarily associated with the digital ground. Both grounds should be connected together near the comparator.
GROUND 2	– One of two grounds, but primarily associated with the analog ground. Both grounds should be connected together near the comparator.

PIN DESIGNATIONS

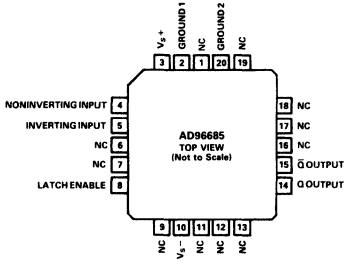
AD96685BQ/TQ/BR



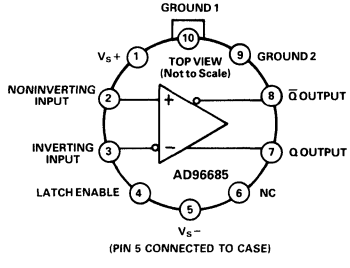
AD96687BQ/TQ/BR



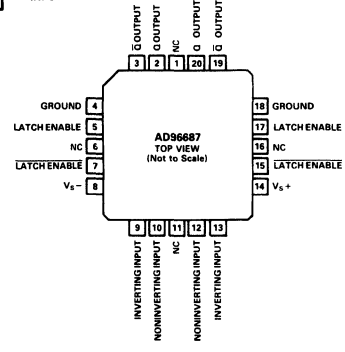
AD96685TE/BP



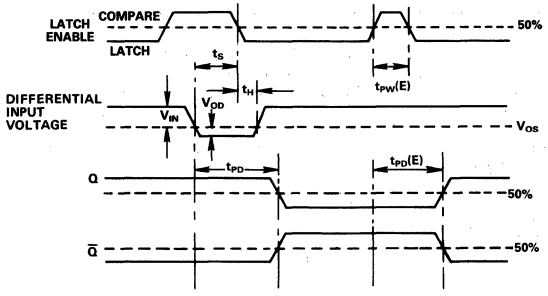
AD96685BH/TH



AD96687TE/BP

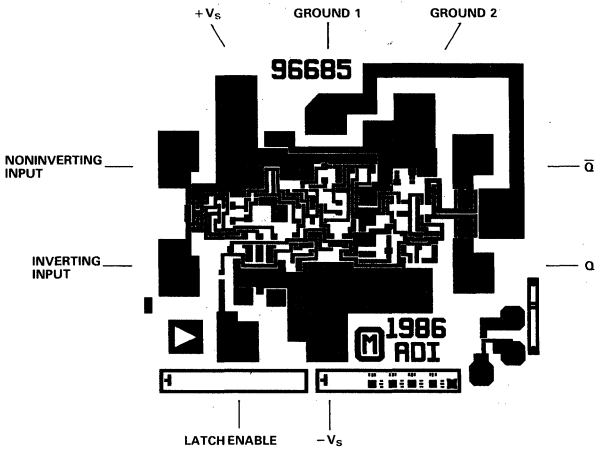


SYSTEM TIMING DIAGRAM

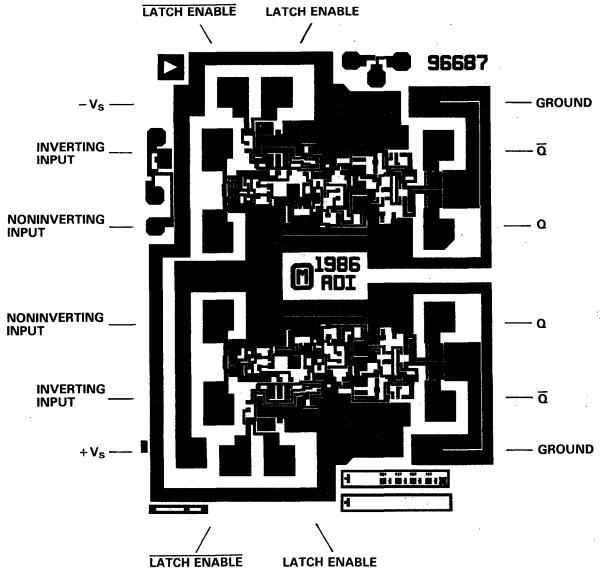


t_S	–	Minimum Setup Time
t_H	–	Minimum Hold Time
t_{PD}	–	Input to Output Delay
$t_{PD}(E)$	–	LATCH ENABLE to Output Delay
$t_{PW}(E)$	–	Minimum LATCH ENABLE Pulse Width
V_{OS}	–	Input Offset Voltage
V_{OD}	–	Overdrive Voltage

DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	AD96685	44 × 50 × 15 (± 2) mils
Pad Dimensions		4 × 4 mils
Metalization		Aluminum
Backing		None
Substrate Potential		–Vs
Passivation		Oxynitride
Die Attach		Gold Eutectic
Bond Wire		1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold, Gold Ball Bonding



Die Dimensions	AD96687	77 × 60 × 15 (± 2) mils
Pad Dimensions		4 × 4 mils
Metalization		Aluminum
Backing		None
Substrate Potential		–Vs
Passivation		Oxynitride
Die Attach		Gold Eutectic
Bond Wire		1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold, Gold Ball Bonding

APPLICATIONS INFORMATION

The AD96685/87 comparators are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any AD96685/87 design is the use of a low impedance ground plane.

Another area of particular importance is power supply decoupling. Normally, both power supply connections should be separately decoupled to ground through 0.1μF ceramic and 0.001μF mica capacitors. The basic design of comparator circuits makes the negative supply somewhat more sensitive to variations. As a result more attention should be placed on insuring a "clean" negative supply.

The LATCH ENABLE input is active LOW (latched). If the latching function is not used, the LATCH ENABLE input should be grounded (ground is an ECL logic HIGH). The $\overline{\text{LATCH ENABLE}}$ input of the AD96687 should be tied to −2.0V or left "floating," to disable the latching function. An alternate use of the LATCH ENABLE input is as a hysteresis control input. By varying the voltage at the LATCH ENABLE input for the AD96685 and the differential voltage between both latch inputs for the AD96687, small variations in the hysteresis can be achieved.

Occasionally, one of the two comparator stages within the AD96687 will not be used. The inputs of the unused comparator should not be allowed to "float." The high internal gain may cause the output to oscillate (possibly affecting the other comparator which is being used) unless the output is forced into a fixed state. This is easily accomplished by insuring that the two inputs are at least one diode drop apart, while also grounding the LATCH ENABLE input.

The best performance will be achieved with the use of proper ECL terminations. The open-emitter outputs of the AD96685/87 are designed to be terminated through 50Ω resistors to −2.0V, or any other equivalent ECL termination. If high speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.

The AD96685/87 have been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100mV to 1V. Propagation delay dispersion is the change in propagation delay which results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the AD96685/87 is far less sensitive to input variations than most comparator designs.

3

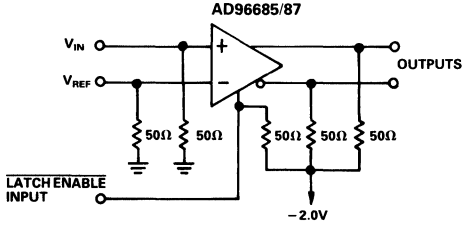
MIL-STD-883 COMPLIANCE INFORMATION

The AD96685TE/TH/TQ/883B and AD96687TE/TQ/883B devices are classified within Microcircuits Group 50, Technology Group D (Bipolar Comparators); and are constructed in accordance with the latest revision of MIL-STD-883. The AD96685 and AD96687 are electrostatic sensitive and fall within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

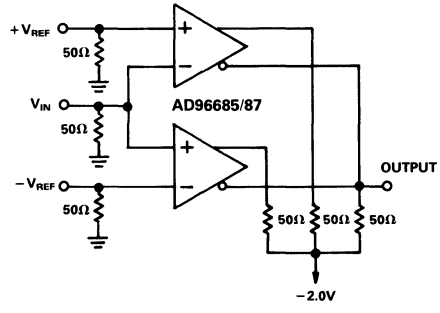
The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are makred with "C" to indicate compliance to the latest revision of the standard.

Typical Applications

HIGH SPEED SAMPLING CIRCUIT



HIGH SPEED WINDOW COMPARATOR



Instrumentation Amplifiers
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Selection Guide
Instrumentation Amplifiers

Model	Gain Ranges	Gain Error % max	Gain TC ppm/°C max	BW MHz typ[1]	Package Options[2]	Temp Range[3]	Page	Comments
AD524	**1, 10, 100, 1000**	**0.02–2.0**	**5–100**	**1.0**	**D, E**	**I, M**	**4–25**	**Pin Programmable, Input Protection**
AD526	**1, 2, 4, 8, 16**	**0.01–0.15**	**2–5**	**4.0**	**D, N**	**C, I, M**	**4–37**	**Software Programmable, μP Interface**
AD624	**1, 100, 200, 500, 1000**	**0.02–1.0**	**5–25**	**1.0**	**D**	**I, M**	**4–49**	**Pin Programmable**
AD625	**1–10,000**	**0.02–0.05**	**5**	**0.65**	**D, N**	**C, I, M**	**4–61**	**Resistor Programmable, Low Cost**
AD365	1, 10, 100, 500	0.05–0.1	5–10	0.8	M	I	4–7	Digitally Programmable with T/H
AD522	1–10,000	0.05–1.0	2–50	0.3	D	I, M	4–21	Resistor Programmable
AD521	0.1–1000	0.25–3.0	3–50	2	D	C, M	4–15	Resistor Programmable

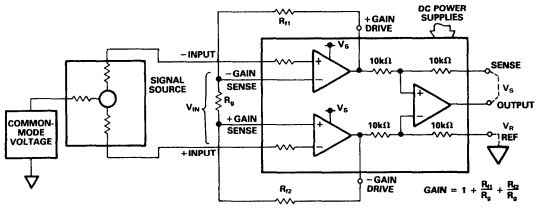
[1]Unity gain small signal bandwidth.
[2]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; M–Metal Hermetic Dual-In-Line; N–Plastic Molded Dual-In-Line.
[3]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
Instrumentation Amplifiers

An instrumentation amplifier is a committed "gain block" that measures the difference between the voltages existing at its two input terminals, amplifies it by a precisely set gain – usually from 1V/V to 1000V/V or more – causes the result to appear between a pair of terminals in the output circuit. Referring to Figure 1,

$$V_S - V_R = G\,(V^+ - V^-)$$

An ideal differential instrumentation amplifier responds only to the *difference* between the input voltages. If the input voltages are equal ($V^+ = V^- = V_{CM}$, the *common-mode voltage*), the output of the ideal instrumentation amplifier will be zero.



R_{f1}, R_{f2}, R_g ARE EXTERNAL GAIN-SETTING RESISTORS

An amplifier circuit which is optimized for performance as an instrumentation amplifier gain block has high input impedance, low offset and drift, low nonlinearity, stable gain and low effective output impedance. It is commonly used for applications which capitalize on these advantages. Examples include: transducer amplification – for thermocouples, strain-gage bridges, current shunts and biological probes; preamplification of small differential signals superimposed on high common-mode voltages, signal conditioning and (moderate) isolation for data acquisition; and signal translation for differential and single-ended signals wherever the common "ground" is noisy or of questionable integrity.

Single-ended software-programmable gain amplifiers, such as the AD526, with fixed binary gains of 1, 2, 4, 8, etc., are often listed with instrumentation amplifiers. They are used in systems having a "clean" signal ground to provide appropriate amounts of digitally controlled gain to normalize the level of the output signal to correspond to a large fraction of the input range of an A/D converter; they can thus be used as components of a floating-point A/D conversion system to preserve accuracy over a wide dynamic range. See also "Data-Acquisition Subsystems" in the *Data Conversion Products Databook*.

Instrumentation amplifiers are usually chosen in preference to user-assembled op-amp circuitry because they offer optimized, specified performance in low-cost, easy-to-use, compact packages. If the application calls for high common-mode voltages (typically, voltages in excess of the amplifier supply voltage), or if isolation impedances must be very high (e.g., $10^{10}\Omega$, with galvanic isolation, as in medical and industrial applications), the designer should consider an *isolation amplifier*.

NOTES

[1]Application Note: "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, available upon request.

[2]*Transducer Interfacing Handbook*, D.H. Sheingold, ed., 1980. $14.50, Analog Devices, Inc., P.O. Box 9106, Norwood, MA 02062-9106

SPECIFYING INSTRUMENTATION AMPLIFIERS

The instrumentation amplifier chosen for a given application will be the lowest cost device that satisfies the performance and environmental requirements. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. It is essential that the designer have a firm understanding of the specifications of instrumentation amplifiers and of the contributions of the various sources of error to the total error. The data sheets provide much useful application data on these devices, as well as examples of basic error analyses.

Definitions of the key specifications follow a brief discussion of instrumentation-amplifier architectures. For more complete information on the fundamentals and applications of instrumentation amplifiers, a number of publications are available from Analog Devices.[1,2]

INSTRUMENTATION AMPLIFIER ARCHITECTURE

Basic Analog Devices instrumentation amplifiers have two high-impedance input terminals, a set of terminals for gain programming, an "output" terminal and a pair of feedback terminals, labeled *sense* and *reference*, as well as terminals for power supply and offset trim. Gain is programmable in three ways:

- The gain of basic amplifiers, such as the AD521, AD522 and AD625, is established by connecting resistors externally. Such circuits are generally used for dedicated fixed-gain applications.
- Pin-programmable amplifiers, such as the AD524 and AD624, have a set of internal resistors; a limited set of fixed gains in the range of 1 to 1,000 are chosen by appropriately interconnecting the resistors via external pins. The connections can be fixed or switched via DIP switches or reed relays (if CMOS switches are used, the *on* resistance of the switches must be considered in series with the internal gain resistors).
- Digitally (or "software-") programmable amplifiers are completely self-contained, with gains set by a 2-, 3- or 4-bit digital control word. These devices include the AD365 (with gains of 1, 10, 100, 500) and the AD526 (with binary gains of 1-16, cascadable to 256).

Except for the AD521, the differential input amplifiers use variations of the well known three-op-amp configuration, consisting of a differential input-output gain stage and a subtractor stage. Gain ($\leqslant$1V/V) is set by the choice of a single gain-setting resistor, R_G. When the *sense* (V_S) feedback terminal is connected to the output terminal, and the *reference* terminal (V_R) is connected to power common, the output voltage appears between the output terminal and power common.

The V_S and V_R terminals may be used for remote sensing – to establish precise outputs in the presence of line drops; they may be used with an inside-the-loop booster follower to obtain power amplification without loss of accuracy; and they may be used to establish an output current that is precisely proportional to the difference signal. A voltage applied to the V_R terminal will bias the output by a predetermined amount. It is important always to maintain very low impedance (in relation to the specified V_S and V_R input impedances) when driving the V_S and V_R inputs,

in order not to introduce common-mode, gain, and/or offset errors. In devices using the 3-amplifier configuration, the V_R terminal is sometimes used for "tweaking" common-mode rejection.

SPECIFICATIONS

Specification tables are generally headed by the legend: "specifications are typical at $V_S = \pm 15V$, $R_L = 2k\Omega$, and $T_A = +25°C$, unless otherwise specified." This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature), the significant effects are usually indicated within the specs. "Typical" means that the manufacturer's characterization process has shown this number to be in the middle of a distribution.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Such specs are not uniquely applicable to instrumentation amps.

GAIN: These specifications refer to the linear transfer function of the device; for example, the AD524 gain equation is:

$$G = 1 + \frac{40{,}000}{R_G} \text{ V/V}$$

The value of R_G for a given gain value is:

$$R_G = \frac{40{,}000}{G-1} \Omega$$

For example, if G is to be 200V/V,

$$R_G = 201 \text{ ohms.}$$

Gain Range: Specified at 1 to 1,000, for example, resistor-programmable devices may work at higher gains (1V/V is minimum, except for the AD521), but the manufacturer does not specify performance outside the range. In practice, noise and drift may make higher gains impractical for a given device.

Equation Error (or "Gain Accuracy"): The number given by this specification describes deviation from the gain equation when R_G is at its nominal value. The user can trim the gain or compensate for gain error elsewhere in the overall system. Systems using microprocessors (or computers, or other digital "intelligence") can be made self-calibrating, to take into account the lumped gain errors of all the stages in the analog portion of the system, from transducer to A/D converter.

Nonlinearity (or Gain Nonlinearity): Nonlinearity is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a "best-straight line," with the output swinging through its full-scale range. Nonlinearity is usually specified in percent of full-scale output range.

Gain vs. Temperature: These numbers give the deviations from the gain equation as a function of temperature.

SETTLING TIME is defined as that length of time required for the output voltage to approach and remain within a certain (±) tolerance of its final value. It is usually specified for a fast step that will drive the output through its full-scale range, and it includes slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%, nor is settling time necessarily proportional to gain. Principal contributing factors include slew-rate limiting, underdamping (ringing) and thermal gradients (long tails).

GAIN-BANDWIDTH PRODUCT (GBWP) – the product of the highest gain and its corresponding bandwidth – is a rough figure of merit for bandwidth as an aid to the preliminary screening process. However, since gain and bandwidth are not necessarily in exact inverse proportion, it can be a misleading specification, especially at the lower gains, if interpreted literally.

VOLTAGE OFFSET: Voltage offset and common-mode rejection (see below) specifications are often considered the key figures of merit for instrumentation amplifiers. While initial offset can be adjusted to zero, shifts in offset voltage with time and temperature introduce errors. Systems that involve "intelligent" processors can correct for offset errors in the whole measurement chain, but such applications are still relatively infrequent; in most applications, the instrumentation amplifier's contribution to system offset error must be defined.

Voltage offset and offset drift in instrumentation amplifiers are functions of gain.[1] The offset, measured at the output, is equal to a constant plus a term proportional to gain. For an amplifier with specified performance over a gain range from 1 to 1,000, the constant is essentially the offset at unity gain, and the proportionality term (or slope) is equal to the change in output offset between G = 1 and G = 1,000, divided by 999. To refer offset to the input (RTI), divide the total output offset by the gain. Since offset at a gain of 1,000 is dominated by the proportional term, the slope is often called the "RTI offset, G = 1,000." At any value of gain, the offset is equal to the unity-gain offset plus the product of the gain and the "RTI offset."

The same considerations apply to the offset drift. For example, the maximum RTI drift of the AD624C is specified at 0.25μV/°C. Thus, the output drift is (0.25μV/°C × G) + 10μV/°C at any gain, G, in the range.

Voltage offset as a function of power supply level is also specified RTI at one or more gain settings.

[1]There is a good explanation of the specification of offset in the Application Note: "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, available upon request.

INPUT BIAS AND OFFSET CURRENTS: Input bias currents are those currents needed to bias the input transistors of a dc amplifier or to supply the junction leakage of FETs. FET-input devices have lower bias currents than those using bipolar transistors, but FET leakage currents increase dramatically with temperature, approximately doubling every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

> *Important Note*
> Although instrumentation amplifiers have differential inputs, there *must* be a return path for the bias currents. If it is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of "floating" sources, such as transformers and thermocouples, as well as ac-coupled sources, there must still be a path from each input to common, or to the *guard* terminal. If a dc return path is impracticable, an *isolator* must be used.

COMMON-MODE REJECTION (CMR) is a measure of the change in output voltage when both inputs are changed by equal amounts. CMR is usually specified for a full-range common-mode voltage change (CMV) at a given frequency, and a specified imbalance of source impedance (e.g. 1kΩ source unbalance, at 60Hz). CMR is a logarithmic expression of the *common-mode rejection ratio* (CMRR): CMR = $20 \log_{10}$ (CMRR). The common-mode rejection ratio is defined as the ratio of the signal gain, G, to the ratio of common-mode signal appearing at the output to the input CMV.

In most instrumentation amplifiers, the CMR increases with gain because the front-end configuration does not amplify common-mode signals, and the amount of common-mode signal appearing at the output stays relatively constant as the signal gain (G) increases.

However, at higher gains, amplifier bandwidth decreases. Since differences in phase shift through the differential input stage will show up as common-mode errors, CMR becomes more frequency-dependent at high gains.

Programmable Gain & T/H DAS Amplifier

AD365

FEATURES
Software Programmable Gain (1, 10, 100, 500)
Low Input Noise (0.2μV p-p)
Low Gain Error (0.05% max)
Low Nonlinearity (0.005% max)
Low Gain Drift (10ppm/°C max)
Low Offset Drift (2μV/°C RTI max)
Fast Settling (15μs @ Gain 100)
Small 16-Pin Metal DIP

APPLICATIONS
Digitally Controlled Gain Amplifier
Auto-Gain Ranging Amplifier
Wide Dynamic Range Measurement System
Gain Selection/Channel Amplifier
Transducer/Bridge Amplifier
Test Equipment

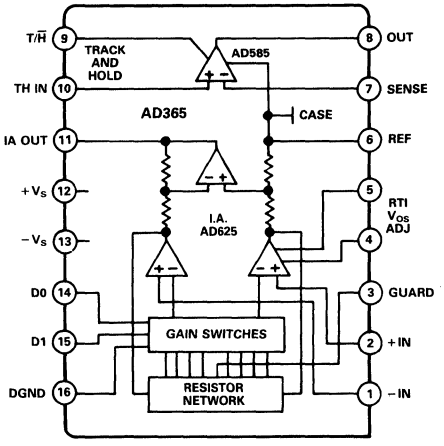
HIGHLIGHTS

The AD365 is a two stage data acquisition system (DAS) front end consisting of a digitally selectable gain amplifier followed by an independent track/hold amplifier. The programmable gain amplifier features differential inputs for excellent common-mode rejection, high open loop gain for superior linearity, and fast settling for use in multiplexed high speed systems. The track/hold amplifier features high open loop gain for 12-bit compatible linearity, internal hold capacitor for high reliability, and fast acquisition time for use with multichannel systems. Both amplifiers are capable of being used separately and are specified as independent function blocks.

GENERAL DESCRIPTION

The AD365 is comprised of the AD625 monolithic precision instrumentation amplifier to provide a precision differential input, the AD7502 monolithic CMOS multiplexer to handle gain switching, a precision thin-film resistor network, and the AD585 monolithic track and hold amplifier with internal hold capacitor.

AD365 FUNCTIONAL BLOCK DIAGRAM



The input stage provides high common-mode rejection, low noise, fast settling at all gains, and low drift over temperature. The gains of 1, 10, 100, and 500 are digitally selected with the two gain control lines which are 5V CMOS compatible.

The track and hold amplifier section is ideally suited for high speed 12-bit applications where fast settling, low noise, and low sample-to-hold offset are critical. The T/H mode is controlled with a single input line which can be tied to the status output line of the accompanying A/D converter.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

AD365AM	Min	Typ	Max	Units
PGA GAIN				
Inaccuracy[1]				
@ G = 1, 10, 100		0.02	0.05	%
@ G = 500		0.04	0.1	%
Nonlinearity				
@ G = 1, 10, 100			0.005	%
@ G = 500			0.01	%
Drift				
@ G = 1		1	5	ppm/°C
@ G = 10, 100, 500		3	10	ppm/°C
PGA OFFSET (May be Nulled at Input and Output)				
Input Offset Voltage (RTI)		25	200	μV
vs. Temperature		0.1	2	μV/°C
vs. Common-Mode Voltage		0.5	3.2	μV/V
vs. Supply Voltage		1	10	μV/V
Output Offset Voltage (RTO)		1	5	mV
vs. Temperature		30	150	μV/°C
vs. Common-Mode Voltage		60	316	μV/V
vs. Supply Voltage		60	316	μV/V
PGA INPUT				
Common- Mode and Differential Impedance		$10^9 \| 5$		Ω‖pF
Differential Input Voltage, Linear	10	12		V
Common-Mode Voltage, Linear		$12 - V_{DIFF} \times G/2$		V
Input Stage Noise 0.1 to 10Hz		0.2		μV p-p
Input Stage Noise Density @ 1kHz		4		$nV/\sqrt{Hz}$
Bias Current		5	50	nA
vs. Temperature		50		pA/°C
Offset Current		2	20	nA
vs. Temperature		20		pA/°C
Noise Current (0.1 to 10Hz)		60		pA p-p
PGA OUTPUT				
Voltage 2kΩLoad	10	12		V
Output Impedance		0.2		Ω
Short Circuit Current		25		mA
Capacitive Load		500		pF
Output Stage Noise 0.1 to 10Hz		10		μV p-p
Output Stage Noise Density @ 1kHz		75		$nV/\sqrt{Hz}$
Guard Voltage		$(V_{+IN} + V_{-IN})/2$		V
Guard Offset		−550		mV
PGA DYNAMIC RESPONSE				
Small Signal − 3dB				
G = 1		800		kHz
G = 10		400		kHz
G = 100		150		kHz
G = 500		40		kHz
Full Power Bandwidth G = 1 @ V_O = 20V p-p		60		kHz
Slew Rate		4		V/μs
Settling Time to 0.01% @ V_O = 20V p-p				
G = 1, 10		8	10	μs
G = 100		12	15	μs
G = 500		40	50	μs
Gain Switching Time		1.5		μs
Overdrive Recovery Time V_{IN} = 15V @ G = 1		7		μs
PGA DIGITAL INPUTS				
Logic Low	0		0.8	V
Logic High	3.0		$+V_S$	V
Current, I_{INH} or I_{INL}		0.01	1	μA

AD365AM	Min	Typ	Max	Units
TRACK AND HOLD AMPLIFIER SECTION				
TRANSFER CHARACTERISTICS				
Open Loop Gain V_O = 10V, R_L = 2k	100k	200k		V/V
Nonlinearity @ G = +1			0.005	% FSR
Output Voltage R_L = 2kΩ	10	12		V
Capacitive Load		100		pF
Short Circuit Current		25		mA
TRACK MODE DYNAMICS				
Acquisition Time to 0.01% 10V Step		2	3	μs
20V Step		4	5	μs
Small Signal Bandwidth −3dB		2		MHz
Full Power Bandwidth (20V p-p)		120		kHz
Slew Rate		10		V/μs
TRACK/HOLD SWITCHING				
Aperture Time		35		ns
Aperture Uncertainty		0.5		ns
Switching Transient		40		mV
Settling Time to 2mV		0.5		μs
HOLD MODE				
Droop Rate @ +25°C		0.3	1	V/sec
from $T_{AMBIENT}$ to T_{MAX}		Doubles/10°C		V/sec
Feedthrough		25		μV/V
Pedestal, Offset @ +25°C		2	3	mV
Over Temperature		3		mV
T/H ANALOG INPUT				
Bias Current		0.1	2	nA
Over Temperature		0.2	5	nA
Offset Voltage			2	mV
Over Temperature			3	mV
vs. Common Mode		25	100	μV/V
vs. Supplies		100	316	μV/V
Input Impedance		10^{12}‖10		Ω‖pF
Noise Density @ 1kHz		50		nV/√Hz
Noise 0.1Hz to 10Hz		10		μV p-p
T/H DIGITAL INPUT CHARACTERISTICS				
Logic Low (Hold Mode)	0		0.8	V
Logic High (Track Mode)	2.0		$+V_S$	V
Input Current		10	50	μA
AD365 POWER REQUIREMENTS				
Positive Supply Range	+11		+17	V
Negative Supply Range	−11		−17	V
Quiescent Current		12	16	mA
Power Dissipation		360	550	mW
Warm-Up Time to Specification		5		Minutes
Ambient Operating Temperature	−25		+85	°C
Package Thermal Resistance (θ_{ja})		60		°C/W
AD365 ABSOLUTE MAXIMUM RATINGS				
Positive Supply $+V_S$	−0.3		+17	V dc
Negative Supply $-V_S$	+0.3		−17	V dc
Analog Input Voltage	$-V_S$		$+V_S$	V
Analog Input Current	−10		+10	mA
Digital Input Voltage	−0.3		$+V_S$	V
T/H Differential V_{IN}			±30	V
Storage Temperature	−65		+150	°C
Lead Soldering, 10 Sec			300	°C
Short Circuit Duration		Indefinite		
PACKAGE OPTION[2]				
DH-16B				

NOTE
[1]Gain = 10, 100 and 500 are trimmed and tested ratiometric to G = 1.
[2]See Section 20 for package outline information.
Specifications subject to change without notice.

Typical Characteristics (@ +25°C unless otherwise noted)

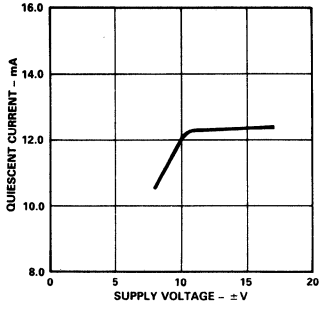


Figure 1. AD365 Quiescent Current vs. Supply Voltage

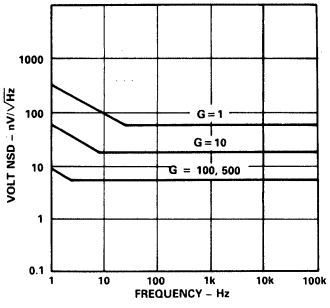


Figure 2. PGA RTI Noise Spectral Density vs. Gain

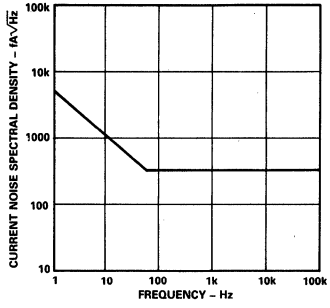


Figure 3. PGA Input Current Noise

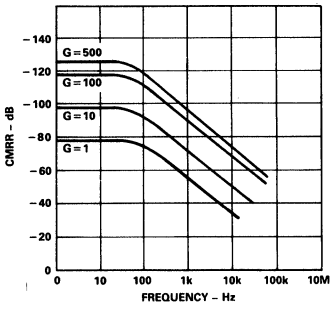


Figure 4. PGA CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

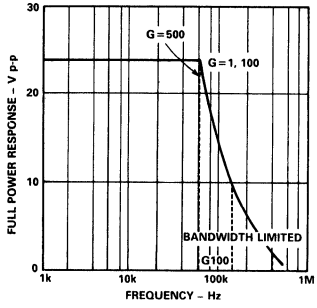


Figure 5. PGA Large Signal Frequency Response

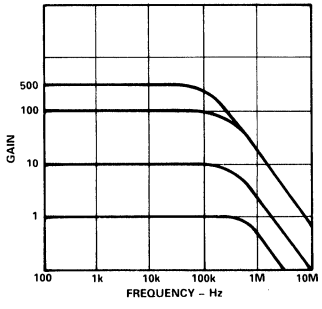


Figure 6. PGA Gain vs. Frequency

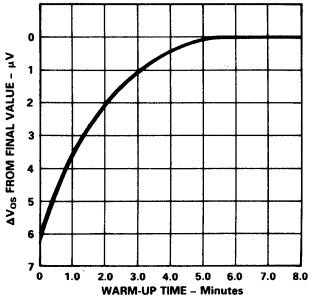


Figure 7. PGA Offset Voltage, RTI, Turn On Drift

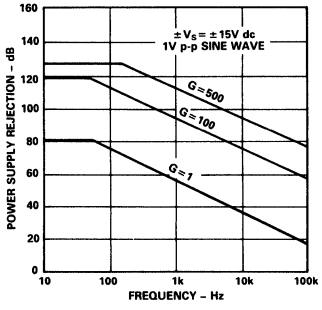


Figure 8. PGA PSRR vs. Frequency

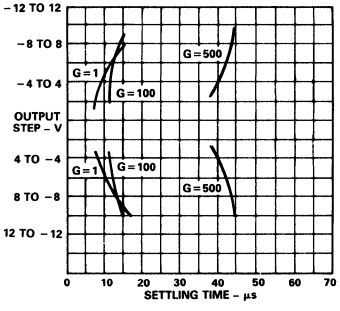


Figure 9. PGA Settling Time to 0.01%

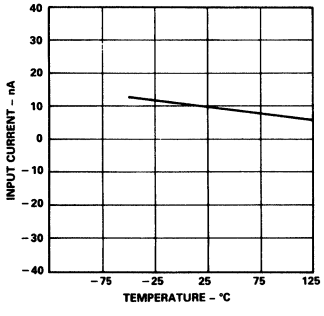


Figure 10. PGA Input Bias Current vs. Temperature

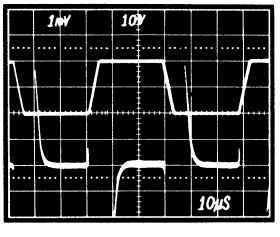


Figure 11. PGA Large Signal Pulse Response and Settling Time, G = 100

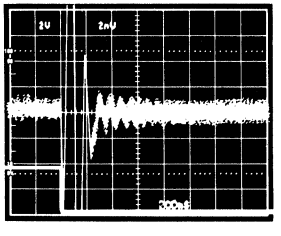


Figure 12. Sample-to-Hold Settling Time

The AD365 PGA section uses the AD625 monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp stage (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G + 1$) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

Digital gain control is provided using the D0 and D1 inputs (pins 14 and 15) which are decoded internally in the gain switching AD7502 as shown in Figure 15 below. The switch selects the resistance R_G from the laser trimmed resistor network according to the following gain select table.

D1	D0	PGA GAIN
0	0	1
0	1	10
1	0	100
1	1	500

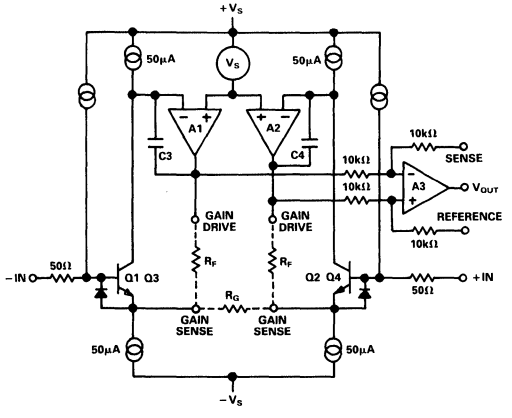


Figure 13. Simplified Circuit of the PGA

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the PGA; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is (R_G + 300)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 80Ω @ G = 500), the maximum overload voltage the PGA can withstand, continuously, is approximately ±5V. Figure 14 shows the external components

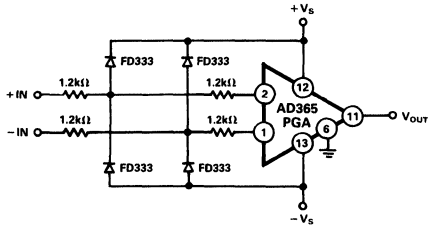


Figure 14. Input Protection Circuit for PGA

necessary to protect the PGA under all overload conditions at any gain. The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered.

4

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±2V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered, however, that the total output swing, to be shared between signal and reference offset, should be ±10 volts (from ground).

The PGA section reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625, a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB ($10k\Omega/1\Omega$ = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 15. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

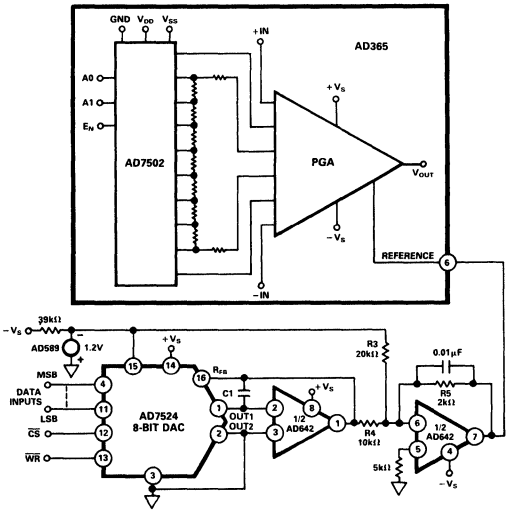


Figure 15. Software Controllable Offset

The circuit of Figure 15 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$. To be symmetrical about 0V, R_3 must be equal to $2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 15 is ±120mV, and the offset is incremented in steps of 0.9375mV/LSB.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains. Input errors dominate at high gains and output errors dominate at low gains.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain ×input error) + output error

The AD365 provides for input offset voltage adjustment (see Figure 16). This simplifies nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9µV/°C, RTO.

Output offset adjustment is normally provided by the A/D converter offset adjustment which will compensate for the output offset of the PGA, offset of the T/H amplifier, and offset of the A/D.

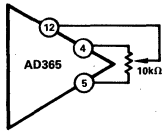


Figure 16. Input Voltage Offset Adjustment

COMMON-MODE REJECTION

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figure 17 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

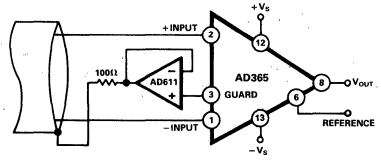


Figure 17. Common-Mode Shield Driver

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 18). Since the AD365 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

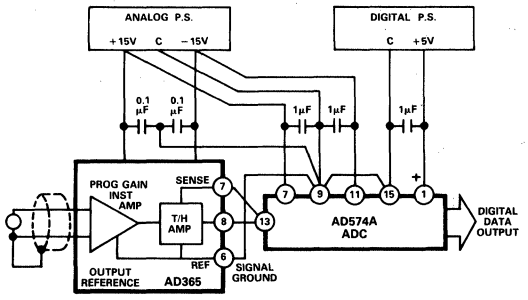


Figure 18. Basic Grounding Practice

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 19.

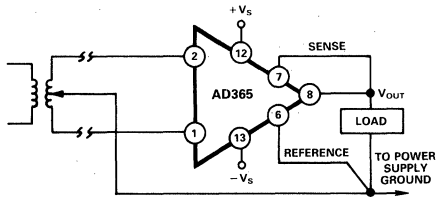


Figure 19a. Ground Returns for Bias Currents with Transformer Coupled Inputs

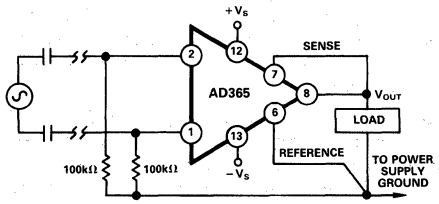


Figure 19b. Ground Returns for Bias Currents with ac Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 20 provides a hardware solution.

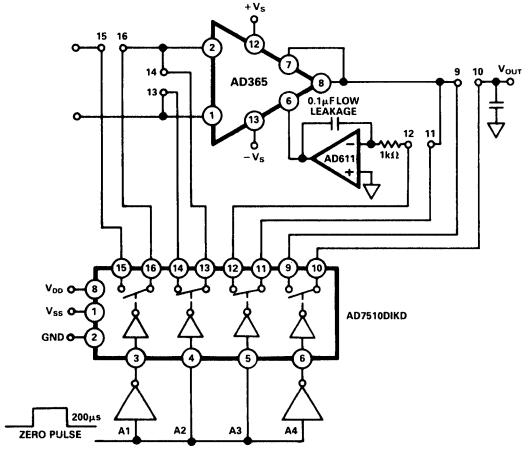


Figure 20. Auto-Zero Circuit

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD365) remain isothermal. This includes the input leads (1, 2). In addition, the user should also avoid air currents over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise.

The base emitter junction of an input transistor can rectify out-of-band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. In the case of a resistive transducer, a capacitor across the input working against the internal resistance of the transducer may suffice to provide an RC filter. These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 1 and 2, to preserve high ac CMR.

THEORY OF OPERATION – T/H SECTION

In sampled data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 21 shows pictorially the track-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Track-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Track Transition.

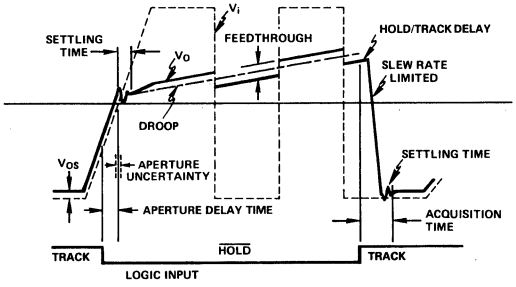


Figure 21. Pictorial Showing Various T/H Characteristics

4

TRACK-TO-HOLD TRANSITION

The aperture delay time is the time required for the track-and-hold amplifier to switch from track to hold. Since this is effectively a constant, it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 22 will result.

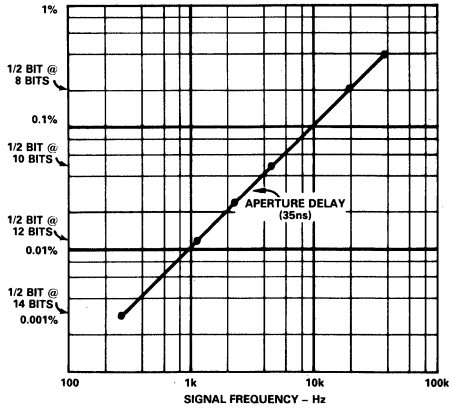


Figure 22. Aperture Delay Error vs. Frequency

To eliminate the aperture delay as an error source the track-to-hold command may be advanced with respect to the input signal.

Once the aperture delay time has been eliminated as an error source then T/H trigger uncertainty/jitter and internal aperture jitter which are the variations in aperture delay time from sample-to-sample remain. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the N-bit A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi \text{ (Aperture Jitter)}}$$

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\,(0.5\times10^{-9})} = 77.7\text{kHz}$$

Track-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting track-to-hold offset is a function of the logic level applied to the gate and the change in the gate capacitance over temperature.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a track and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dt}\,(\text{Volts/Sec}) = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD365 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF}} = 1\text{V/sec maximum}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion.

Since a track and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (t_{CONV}) is required to calculate the maximum allowable dV/dt.

$$\frac{dV \text{ max}}{dt} = \frac{\Delta V \text{ max}}{t_{CONV}}$$

The maximum $\frac{dV \text{ max}}{dt}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) = ΔT.

$$\frac{dV\ 25°C}{dt} \times 2^{\frac{(\Delta T°C)}{10°C}} \leq \frac{dV \text{ max}}{dt}$$

HOLD-TO-TRACK TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD365 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. Figures 23 and 24 show the use of an AD365 with the AD578 and AD574A.

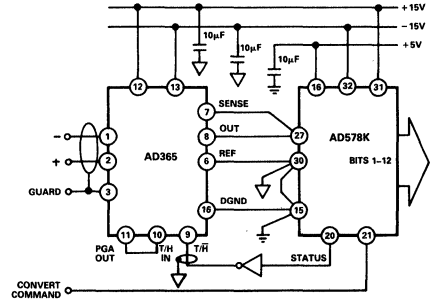


Figure 23. A/D Conversion System, 117.6kHz Throughput 58.8kHz Max Signal Input

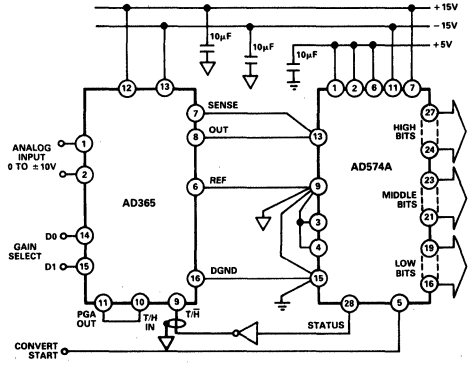


Figure 24. 12-Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz Max Signal Input

ANALOG DEVICES

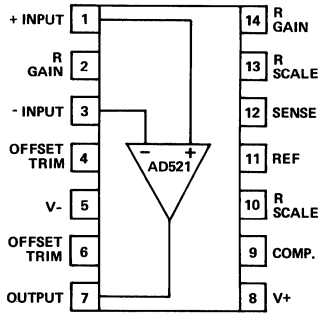
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

Programmable Gains from 0.1 to 1000
Differential Inputs
High CMRR: 110dB min
Low Drift: 2μV/°C max (L)
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000
Chips are Available

AD521 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9 \Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD (AD521SD/883B)
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	*	*	*
Equation	$G = R_S/R_G$ V/V	*	*	*
Error from Equation	(±0.25–0.004G)%	*	*	*
Nonlinearity (Note 2)				
1≤G≤1000	0.2% max	*	0.1% max	*
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	*	*	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	*	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*	*
Impedance	0.1Ω	*	*	*
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	>2MHz	*	*	*
G = 10	300kHz	*	*	*
G = 100	200kHz	*	*	*
G = 1000	40kHz	*	*	*
Small Signal, ±1.0% Flatness				
G = 1	75kHz	*	*	*
G = 10	26kHz	*	*	*
G = 100	24kHz	*	*	*
G = 1000	6kHz	*	*	*
Full Peak Response (Note 3)	100kHz	*	*	*
Slew Rate, 1≤G≤1000	10V/μs	*	*	*
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7μs	*	*	*
G = 10	5μs	*	*	*
G = 100	10μs	*	*	*
G = 1000	35μs	*	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)				
G = 1000	50μs	*	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10μs	*	*	*
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	2μV/°C max	**
vs. Supply	3μV/%	*	*	*
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs. Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	75μV/°C max	**
vs. Supply (Note 6)	$0.005V_{OS_O}$/%	*	*	*
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	**	**
vs. Temperature	1nA/°C max	500pA/°C max	**	**
vs. Supply	2%/V	*	*	*
Input Offset Current	20nA max	10nA max	**	**
vs. Temperature	250pA/°C max	125pA/°C max	**	**
INPUT				
Differential Input Impedance (Note 7)	$3 \times 10^9\Omega$‖1.8pF	*	*	*
Common Mode Input Impedance (Note 8)	$6 \times 10^{10}\Omega$‖3.0pF	*	*	*
Input Voltage Range for Specified Performance (with respect to ground)	±10V	*	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*	*
Voltage at either input (Note 9)	V_S ±15V	*	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**	**
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	**	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**	**
NOISE				
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2}\,\mu V$	*	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}\,\mu V$	*	*	*
Input Current, rms, 10Hz to 10kHz	15pA (rms)	*	*	*
REFERENCE TERMINAL				
Bias Current	3μA	*	*	*
Input Resistance	10MΩ	*	*	*
Voltage Range	±10V	*	*	*
Gain to Output	1	*	*	*
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	*	*	*
Quiescent Supply Current	5mA max	*	*	*
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGE OPTION[1]				
Ceramic (D-14)	AD521JD	AD521KD	AD521LD	AD521SD

NOTES

[1] See Section 20 for package outline information.

*Specifications same as AD521JD.

**Specifications same as AD521KD.

Specifications subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are obtained by simply adjusting the gain setting resistors. (Input voltage should be restricted to ±10V for gains equal to or less than 1.)

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S -0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply includes a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S = 0$) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise ovserved during 2 of 3 separate 10 second periods with the test circuit of Figure 8.

DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$.

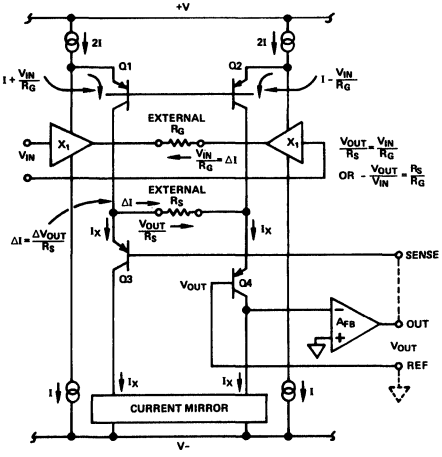


Figure 1. Simplified AD521 Schematic

APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

1. Gains below 1 are realized by adjusting the gain setting resistors as shown in Figure 2 (the resistor, R_S between pins 10 and 13 should remain 100kΩ ±15%, see application note 3). For best results, the input voltage should be restricted to ±10V even though the gain may be less than 1. See Figure 6 for gains above 1000.

2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 3. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.

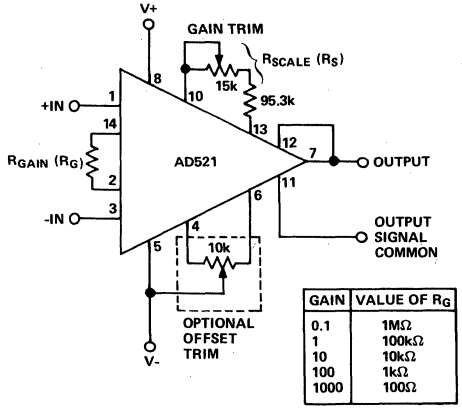
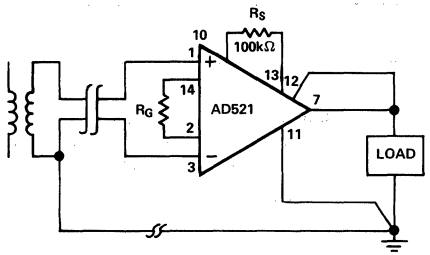


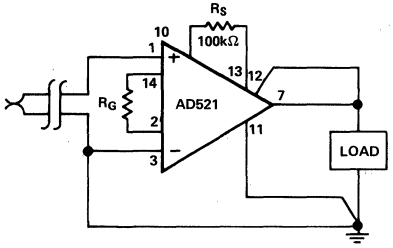
Figure 2. Operating Connections for AD521

3. The resistors between pins 10 and 13, (R_{SCALE}) must equal 100kΩ ±15% (Figure 2). If R_{SCALE} is too low (below 85kΩ) the output swing of the AD521 is reduced. At values below 80kΩ and above 120kΩ the stability of the AD521 may be impaired.

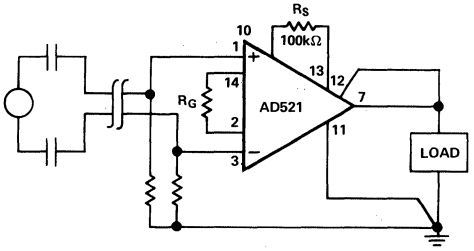
4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 4. The resistor R/2 matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.



a). Transformer Coupled, Direct Return

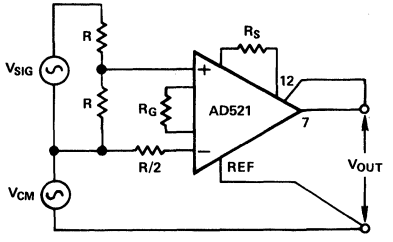


b). Thermocouple, Direct Return



c). AC Coupled, Indirect Return

Figure 3. Ground Returns for "Floating" Transducers



1. INCREASE R_G TO PICK UP GAIN LOST BY R DIVIDER NETWORK
2. INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 4. Operating Conditions for $V_{IN} \approx V_S = 10V$

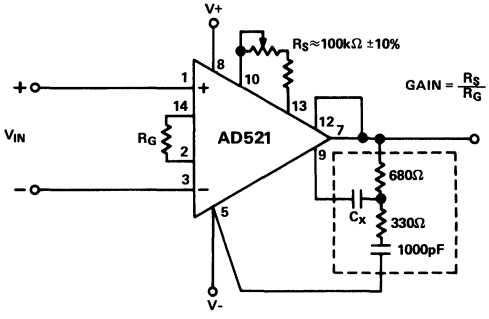
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 5. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set C_X to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V– to the output with little or no attenuation. Therefore, it is advisable to decouple the V– supply line to the output common or to pin 11.[1]



$$C_X = \frac{1}{100\pi f_t} \text{ when } f_t \text{ is the desired bandwidth.}$$

(f_t in kHz, C_X in μF)

Figure 5. Optional Compensation Circuit

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

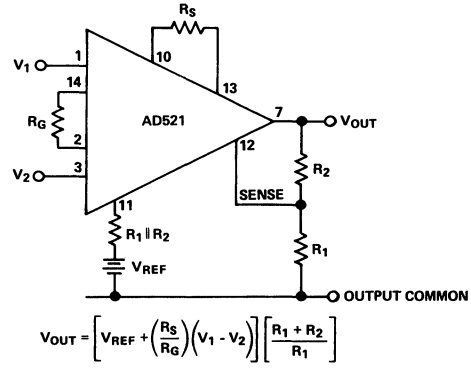
By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error *referred to the input* (R.T.I.) or *output* (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

The offset trim adjustment (pins 4 and 6, Figure 2) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 6, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_G). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.



$$V_{OUT} = \left[V_{REF} + \left(\frac{R_S}{R_G}\right)(V_1 - V_2)\right]\left[\frac{R_1 + R_2}{R_1}\right]$$

Figure 6. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R1 and R2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

[1] For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimizes the offset errors resulting from the input current flowing in R_1 and R_2 at the sense terminal. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 6.

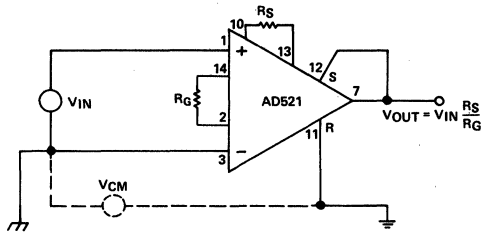


Figure 7. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

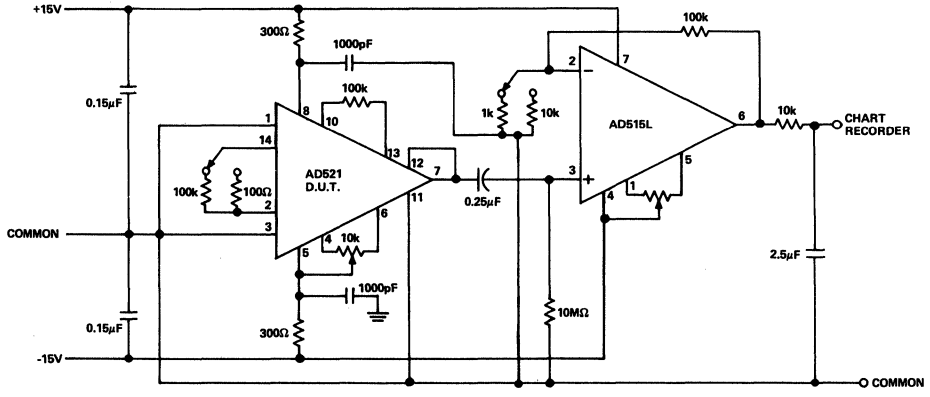


Figure 8. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

ANALOG DEVICES

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

FEATURES

Performance

- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)

Versatility

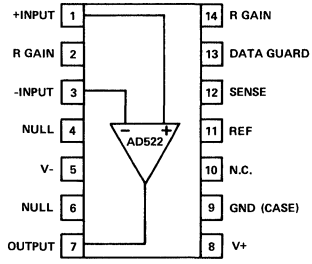
- Single-Resistor Gain Programmable: $1 \leqslant G \leqslant 1000$
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value

- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR

AD522 FUNCTIONAL BLOCK DIAGRAM

14-Pin DIP



PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gages, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 2.0μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from -25°C to +85°C, and the "S" is guaranteed over the extended aerospace temperature range of -55°C to +125°C. All versions are packaged in a 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

SPECIFICATIONS[1] (typical @ $+V_S = \pm 15V$, $R_L = 2k\Omega$ & $T_A = +25°C$ unless otherwise specified)

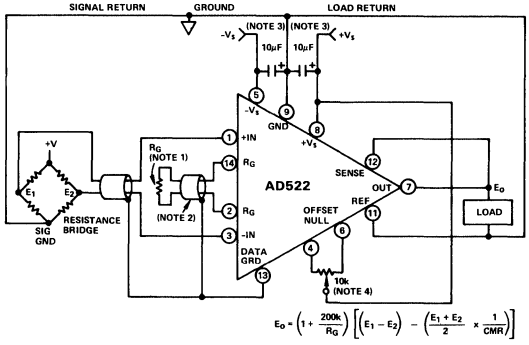
MODEL	AD522AD	AD522BD	AD522SD
GAIN			
Gain Equation	$1 + \frac{2\ (10^5)}{R_g}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0.2% max	0.05% max	**
G = 1000	1.0% max	0.2% max	**
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	**
G = 1000	0.01%	0.005%	**
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	*	*
DYNAMIC RESPONSE (see Fig. 6)			
Small Signal (-3dB)			
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1.5kHz	*	*
Slew Rate	0.1V/μs	*	*
Settling Time to 0.1%, G = 100	0.5ms	*	*
to 0.01%, G = 100	5ms	*	*
to 0.01%, G = 10	2ms	*	*
to 0.01%, G = 1	0.5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
$1 < G < 1000$	$\pm(\frac{50}{G} + 6)\mu V/°C$	$\pm(\frac{25}{G} + 2)\mu V/°C$	$\pm(\frac{100}{G} + 6)\mu V/°C$
vs. Supply, max			
G = 1	±20μV/%	*	*
G = 1000	1.0μV/°C	0.5μV/°C	**
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	*	*
vs. Temperature	±100pA/°C	*	*
Input Offset Current			
Initial max, +25°C	±20nA	*	*
vs. Temperature	±100pA/°C	*	*
INPUT			
Input Impedance			
Differential	$10^9\Omega$	*	*
Common Mode	$10^9\Omega$	*	*
Input Voltage Range			
Maximum Differential Input, Linear	±10V	*	*
Maximum Differential Input, Safe	±20V	*	*
Maximum Common Mode, Linear	±10V	*	*
Maximum Common Mode Input, Safe	±15V	*	*
Common Mode Rejection Ratio, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	*	*
G = 1000	1.5μV	*	*
10Hz to 10kHz (rms)			
G = 1	15μV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	**
PACKAGE OPTIONS[2]			
Ceramic (DH-14B)	AD522AD	AD522BD	AD522SD

NOTES
[1] Specifications guaranteed after 10 minute warm-up.
[2] See Section 20 for package outline information.

*Specifications same as AD522A.
**Specifications same as AD522B.
Specifications subject to change without notice.

GENERAL APPLICATION CONSIDERATIONS

Figure 1 illustrates the AD522 wiring configuration when used in a typical bridge amplifier application. In any low-level, high impedance, noise-dominated environment, proper shielding and grounding are requisite for optimum performance; a recommended technique is shown.



NOTES:
1. GAIN RESISTOR R_G SHOULD BE <5ppm/°C (VISHAY TYPE RECOMMENDED).
2. SHIELDED CONNECTIONS TO R_G RECOMMENDED WHEN MAXIMUM SYSTEM BANDWIDTH AND AC CMR IS REQUIRED, AND WHEN R_G IS LOCATED MORE THAN SIX INCHES FROM AD522. NO INSTABILITIES ARE CAUSED BY REMOTE R_G LOCATIONS. WHEN NOT USED, THE DATA GUARD PIN CAN BE LEFT UNCONNECTED.
3. POWER SUPPLY FILTERS ARE RECOMMENDED FOR MINIMUM NOISE IN NOISY ENVIRONMENTS.
4. NO TRIM REQUIRED FOR MOST APPLICATIONS. IF REQUIRED, A 10kΩ, 25ppm/°C, 25 TURN TRIM POT (SUCH AS VISHAY 1202-Y-10k) IS RECOMMENDED.

Figure 1. Typical Bridge Application

Direct coupling of the AD522 inputs makes it necessary to provide a signal ground return for input amplifier bias currents. This can be achieved by direct connection as shown, or through an indirect path of less than 1MΩ resistance such as other system interconnections.

To minimize noise, shielding should be provided for the input leads and gain resistor connections. A passive data guard is provided to improve ac common mode rejection by "bootstrapping" the capacitance of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

Balanced design eliminates the need for external bypass capacitors for most applications. If, however, the power supplies are remotely located (farther than 10 feet or so) or if they are likely to carry more than a few millivolts of noise, local filtering will enable the user to retain optimal performance.

Reference and sense pins are provided to permit remote load sensing. These points can also be used to trim the device CMR, add an output booster, or to offset the output to a reference level. These applications are illustrated in following sections.

It is good practice to place R_G within several inches of the AD522. Longer leads will increase stray capacitance and cause phase shifts that will degrade CMR at higher frequencies. For frequencies below 10Hz, a remote R_G is generally acceptable; no stability problems are caused. Bear in mind that a leakage impedance of 200MΩ between R_G pins will cause an 0.1% gain error at G = 1. Unity gain is not trimmable.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS (See Figure 1 and Table I)

A floating transducer with a 0 to 1 volt output has a 1kΩ source imbalance. A noisy environment induces a one volt 0 to 60Hz common mode signal in the ground return. This signal must be amplified to interface with a data acquisition system calibrated for a 0 to 10 volt signal range. The operating temperature range is 0 to +50°C and an AD522B is to be used. Table I lists error sources and their effect on system accuracy.

The total effect on absolute accuracy is less than ±0.2%, allowing adjustment-free 8-bit operation. In computer or microprocessor controlled data-acquisition systems, automatic recalibration can nullify gain and offset drifts leaving noise, distortion and CMR as the only error sources. In this case, full 12-bit operation is achieved.

Gain Errors: Absolute gain errors can be nulled by trimming R_G. Gain drift is a linear effect, not detrimental to resolution and is caused by the change in value of internal resistors over the operating temperature range. An "intelligent" system can correct for these errors with an automatic calibration cycle. Gain nonlinearity never exceeds 0.002% at G = 10.

Offset Drift & Pins Current Errors: Special care has been taken in the design of the AD522 input stage to minimize offset drift. Unless transducer impedances are unbalanced by more than 2kΩ, errors caused by offset current drift are negligible compared to offset voltage drift. Although initial offset voltages are laser-nulled for most applications, provisions have been made to allow further adjustment to correct for initial system offset. In this example, all offset drifts amount to ±0.014% and do not effect resolution (can be corrected with an automatic calibration cycle).

CMR and Noise Errors: Common mode rejection and noise performance of instrumentation amplifiers are critical because

Error Source	Specification	Effect on Absolute Accuracy, % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.002% max, G = 10 (from Spec. Sheet and Fig. 4)	±0.002	±0.002
Voltage Drift	$\frac{25\mu V/^\circ C}{Gain} + 2.0\mu V/^\circ C = 4.5\mu V/^\circ C$ R.T.I. = 0.00055%/°C (from Spec. Sheet)	±0.011	---
CMR	86dB (from Spec. Sheet, CMR vs. F vs. G, typical curve)	±0.005	±0.005
Noise, R.T.O. (0.1 to 100Hz)	15μV (p-p) R.T.O. (from Spec. Sheet, Noise vs. G typical curve)	±0.0015	±0.0015
Offset Current Drift	±50pA/°C x 1k source imbalance (Spec. Sheet) = ±50μV/°C = ±1.25μV R.T.I.	±0.000125	---
Gain Drift (add 10ppm/°C for external R_G)	60ppm/°C (Spec. Sheet)	±0.15	---

Table I. Error Sources

these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

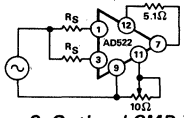


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in three drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

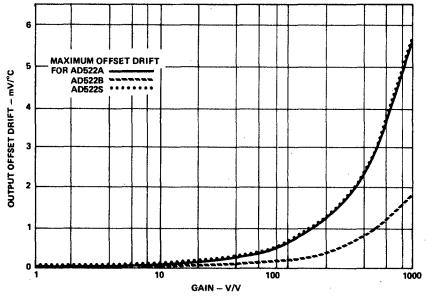


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

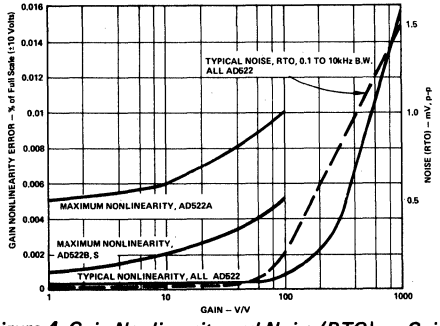


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

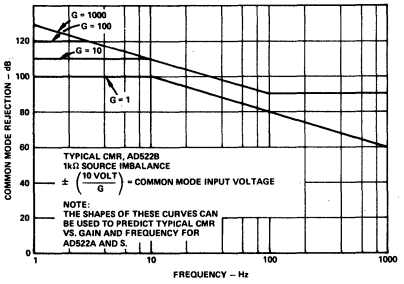


Figure 5. Common Mode Rejection vs. Frequency and Gain

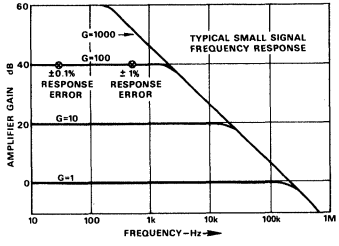


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null .

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

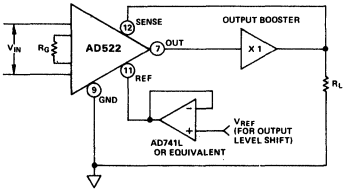


Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

ANALOG DEVICES

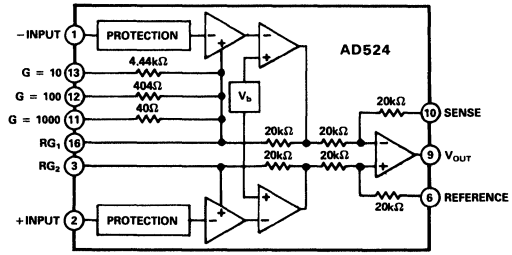
Precision Instrumentation Amplifier

AD524

FEATURES

- Low Noise: 0.3μV p-p 0.1Hz to 10Hz
- Low Nonlinearity: 0.003% (G = 1)
- High CMRR: 120dB (G = 1000)
- Low Offset Voltage: 50μV
- Low Offset Voltage Drift: 0.5μV/°C
- Gain Bandwidth Product: 25MHz
- Pin Programmable Gains of 1, 10, 100, 1000
- Input Protection, Power On – Power Off
- No External Components Required
- Internally Compensated
- MIL-STD-883B, Chips, and Plus Parts Available
- 16-Pin Ceramic DIP Package and 20-Terminal Leadless Chip Carriers Available

AD524 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "A" grade, the low drift "B" grade and lower drift, higher linearity "C" grade are specified from −25°C to +85°C. The "S" grade guarantees performance to specification over the extended temperature range −55°C to +125°C. Devices are available in a 16-pin ceramic DIP package and a 20-terminal leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25MHz, full power response of 75kHz and a settling time of 15μs to 0.01% of a 20V step (G = 100).

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 10			±0.25			±0.15			±0.1%			±0.25	%
G = 100			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±2.0			±1.0			±0.5			±2.0	%
Nonlinearity													
G = 1			±0.01			±0.005			±0.003			±0.01	%
G = 10, 100			±0.01			±0.005			±0.003			±0.01	%
G = 1000			±0.01			±0.01			±0.01			±0.01	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 10			15			10			10			10	ppm/°C
G = 100			35			25			25			25	ppm/°C
G = 1000			100			50			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			250			100			50			100	µV
vs. Temperature			2			0.75			0.5			2.0	µV/°C
Output Offset Voltage			5			3			2.0			3.0	mV
vs. Temperature			100			50			25			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 10	85			95			100			95			dB
G = 100	95			105			110			105			dB
G = 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_{DL})[1]		±10			±10			±10			±10		V
Max Common Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 10	90			95			100			90			dB
G = 100	100			105			110			100			dB
G = 1000	110			115			120			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal −3dB													
G = 1		1			1			1			1		MHz
G = 10		400			400			400			400		kHz
G = 100		150			150			150			150		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step													
G = 1 to 100		15			15			15			15		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		7			7			7			7		$nV/\sqrt{Hz}$
R.T.O.		90			90			90			90		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz													
G = 1		15			15			15			15		µV p-p
G = 10		2			2			2			2		µV p-p
G = 100, 1000		0.3			0.3			0.3			0.3		µV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ±20%
I_{IN}		15			15			15			15		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ±20%
I_{IN}		15			15			15			15		μA
Voltage Range	±10			±10			10			10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	−25		+85	25		+85	25		+85	55		+125	°C
Storage	−65		+150	65		+150	65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**	mA
PACKAGE OPTIONS[2]													
16-Pin Ceramic (D-16)		AD524AD			AD524BD			AD524CD			AD524SD		
LCC DIP (E-20A)		AD524AE			AD524BE			AD524CE			AD524SE		

NOTES
[1]V_{DI} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DI} at other gains = 10V/G.
V_D = Actual differential input voltage.
Example: G = 10, V_D = 0.50
V_{CM} = 12V − (10/2 × 0.50V) = 9.5V
[2]See Section 20 for package outline information.
Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

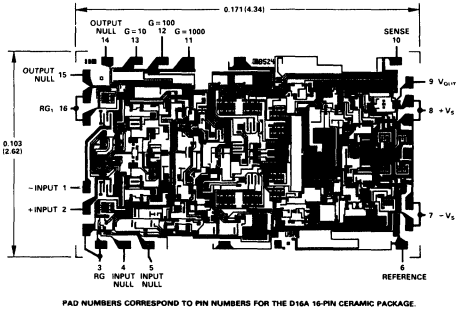
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18V
Internal Power Dissipation 450mW
Input Voltage,
(Either Input Simultaneously) . . . . . $|V_{IN}| + |V_S| < 36V$
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
D . . . . . −65°C to +150°C
E . . . . . −65°C to +150°C
Operating Temperature Range
AD524A/B/C . . . . . −25°C to +85°C
AD524S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . +300°C

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

METALIZATION PHOTOGRAPH

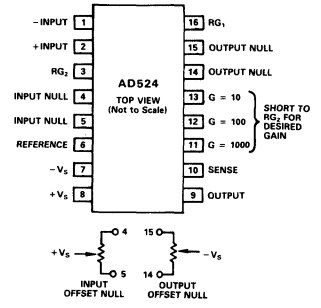
Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



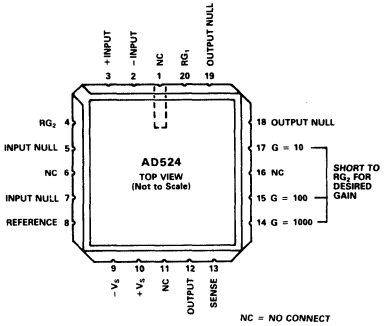
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE D16A 16-PIN CERAMIC PACKAGE.

CONNECTION DIAGRAMS

Ceramic (D) Package



Leadless Chip Carrier (E) Package



NC = NO CONNECT

Typical Characteristics

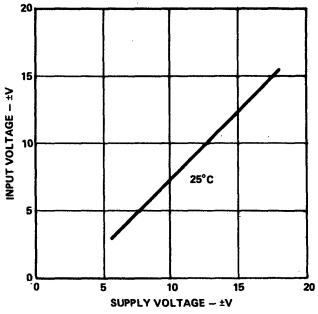


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

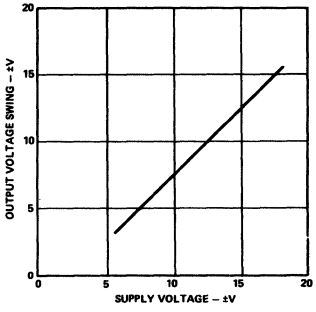


Figure 2. Output Voltage Swing vs. Supply Voltage

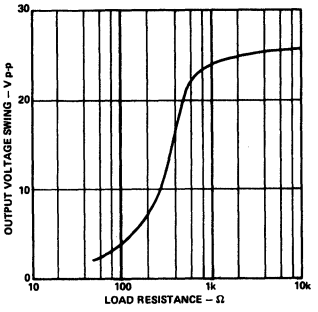


Figure 3. Output Voltage Swing vs. Load Resistance

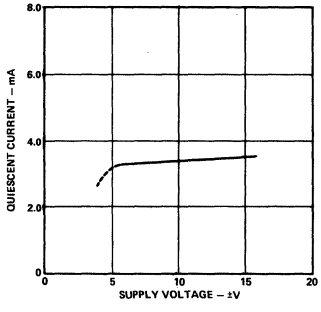


Figure 4. Quiescent Current vs. Supply Voltage

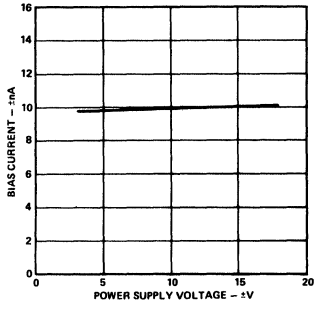


Figure 5. Input Bias Current vs. Supply Voltage

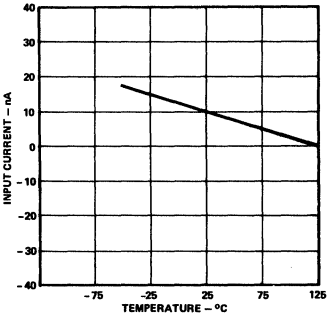


Figure 6. Input Bias Current vs. Temperature

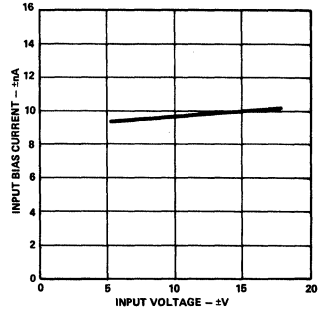


Figure 7. Input Bias Current vs. CMV

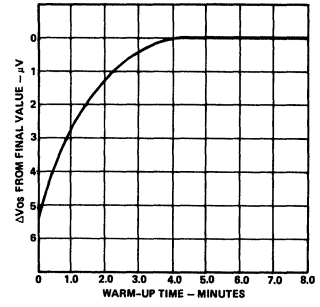


Figure 8. Offset Voltage, RTI, Turn On Drift

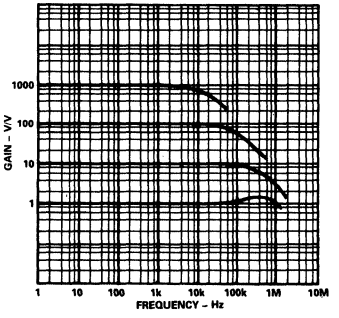


Figure 9. Gain vs. Frequency

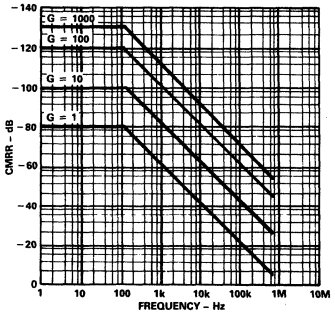


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

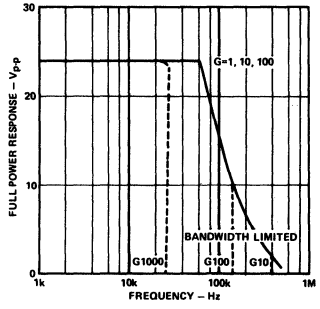


Figure 11. Large Signal Frequency Response

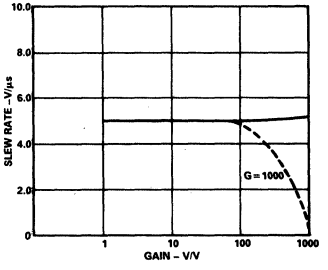


Figure 12. Slew Rate vs. Gain

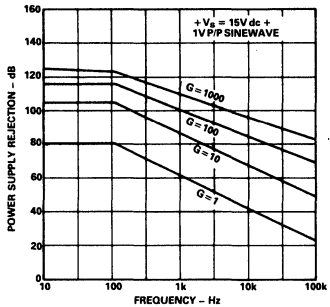


Figure 13. Positive PSRR vs. Frequency

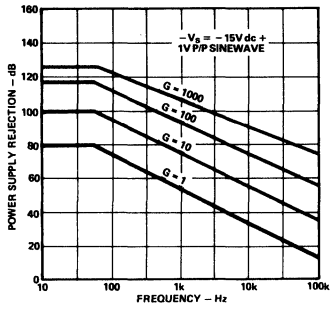


Figure 14. Negative PSRR vs. Frequency

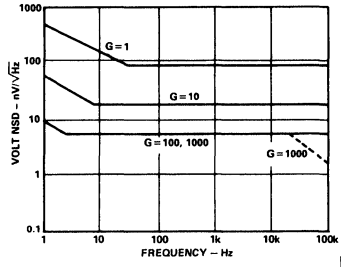


Figure 15. RTI Noise Spectral Density vs. Gain

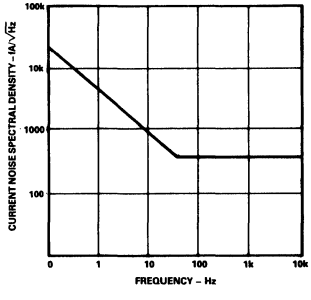


Figure 16. Input Current Noise

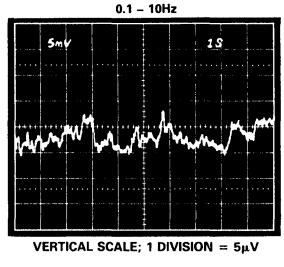


Figure 17. Low Frequency Noise – G = 1 (System Gain = 1000)

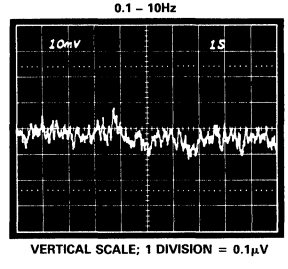


Figure 18. Low Frequency Noise – G = 1000 (System Gain = 100,000)

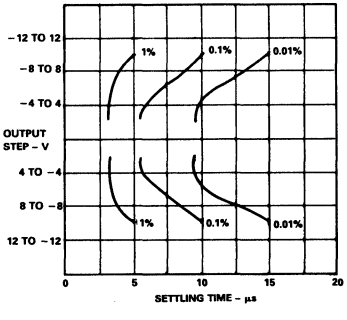


Figure 19. Settling Time Gain = 1

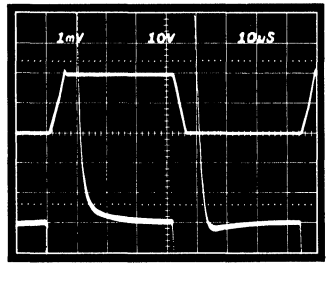


Figure 20. Large Signal Pulse Response and Settling Time – G = 1

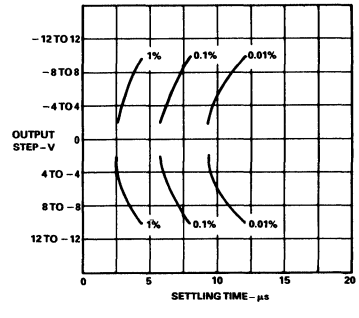


Figure 21. Settling Time Gain = 10

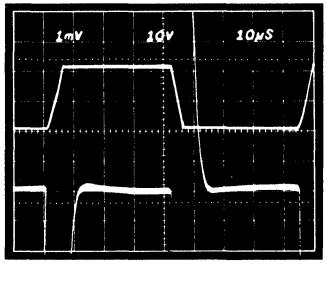


Figure 22. Large Signal Pulse Response and Settling Time G = 10

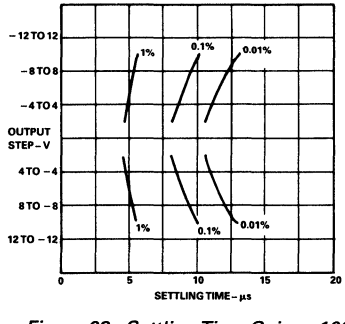


Figure 23. Settling Time Gain = 100

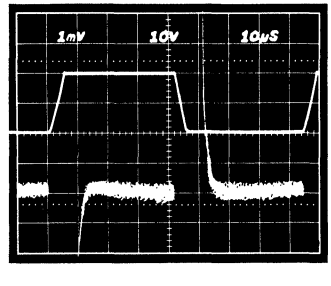


Figure 24. Large Signal Pulse Response and Settling Time G = 100

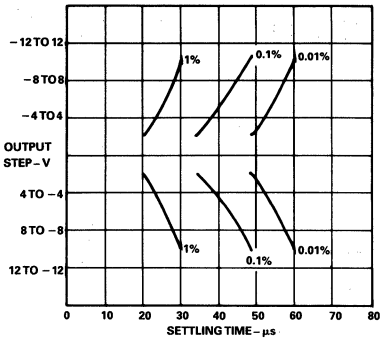


Figure 25. Settling Time Gain = 1000

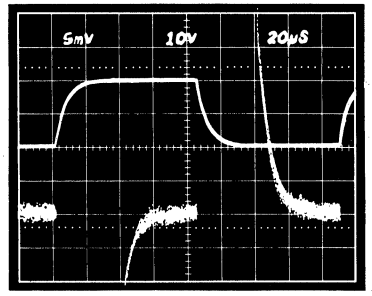


Figure 26. Large Signal Pulse Response and Settling Time G = 1000

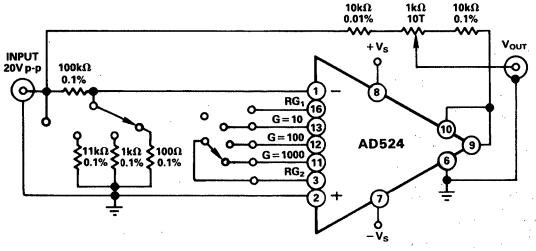


Figure 27. Settling Time Test Circuit

Theory of Operation

The AD524 is a monolithic instrumentation amplifier based on the classic 3 op amp circuit. The advantage of monolithic construction is the closely matched components that enhance the performance of the input preamp. The preamp section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of R_G (smaller values increase the gain) while the feedback forces the collector currents Q1, Q2, Q3 and Q4 to be constant which impresses the input voltage across R_G.

As R_G is reduced to increase the programmed gain, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 30ppm. Second, the

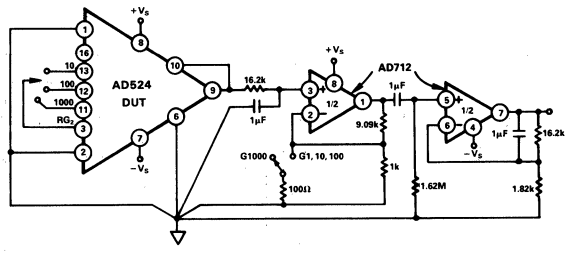


Figure 28. Noise Test Circuit

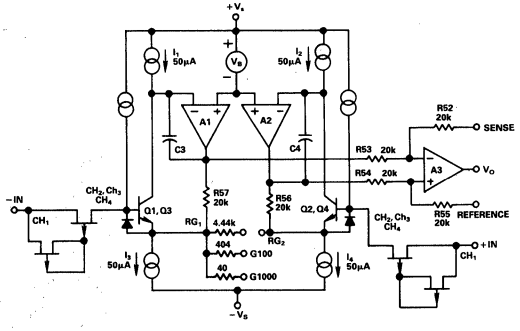


Figure 29. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit

gain bandwith product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $7nV/\sqrt{Hz}$ at G = 1000.

INPUT PROTECTION

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, 10 or less, the gain resistor acts as a current limiting element in series with the inputs. At high gains the lower value of R_G will not adequately protect the inputs from excessive currents. Standard practice would be to place series limiting resistors in each input, but to limit input current to below 5mA with a full differential overload (36V) would require over 7k of resistance which would add $10nV\sqrt{Hz}$ of noise. To provide both input protection and low noise a special series protect FET was used.

A unique FET design was used to provide a bidirectional current limit, thereby, protecting against both positive and negative overloads. Under nonoverload conditions, three channels CH_2, CH_3, CH_4, act as a resistance ($\approx$1kΩ) in series with the input as before. During an overload in the positive direction, a fourth channel, CH_1, acts as a small resistance ($\approx$3kΩ) in series with the gate, which draws only the leakage current, and the FET limits I_{DSS}. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH_1 and when this FET goes into saturation, the gate current is limited and the main FET will go into controlled enhancement. The bidirectional limiting holds the maximum input current to 3mA over the 36V range.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD524 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimize offset voltage changes in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gain of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together (for G = 1 RG_2 is not connected).

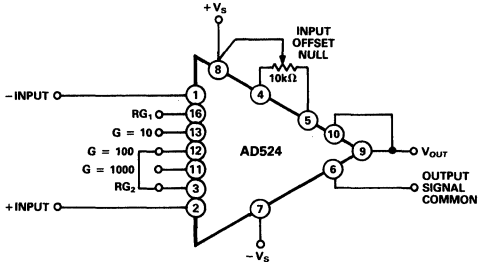


Figure 30. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between pins 3 and 16 which programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 31). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−50ppm/°C typ).

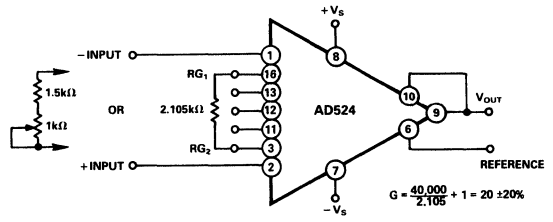


Figure 31. Operating Connections for G = 20

The second technique uses the internal resistors in parallel with an external resistor (Figure 32). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

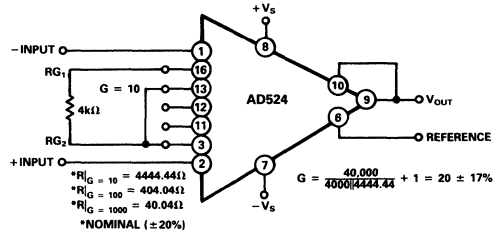


Figure 32. Operating Connections for G = 20, Low Gain T.C. Technique

The AD524 may also be configured to provide gain in the output stage. Figure 33 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

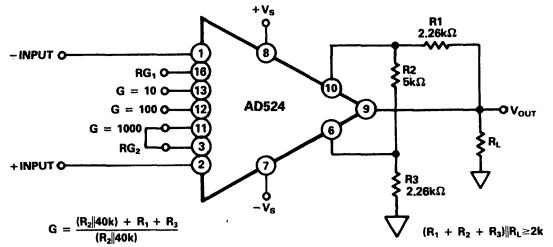


Figure 33. Gain of 2000

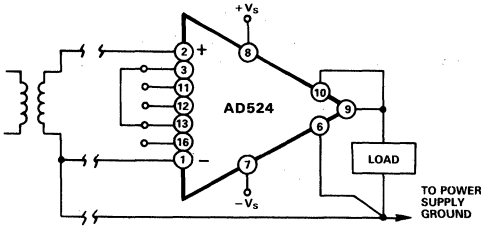
Output Gain	R2	R1,R3	Nominal Gain
2	5kΩ	2.26kΩ	2.02
5	1.05kΩ	2.05kΩ	5.01
10	1kΩ	4.42kΩ	10.1

Table I. Output Gain Resistor Values

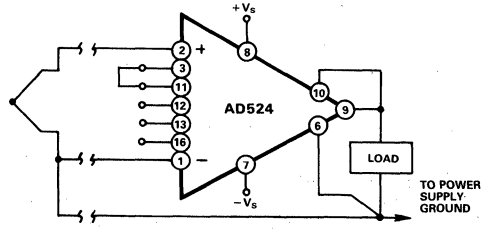
INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.

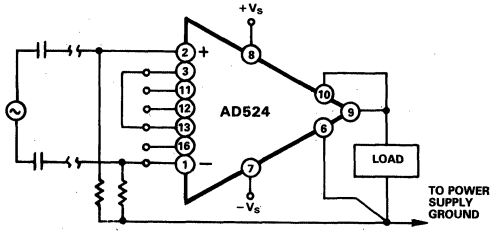
Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.



a. Transformer Coupled



b. Thermocouple



c. AC Coupled

Figure 34. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common mode rejection errors unless the shield is properly driven. Figures 35 and 36 shows active data guards which are configured to improve ac common mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

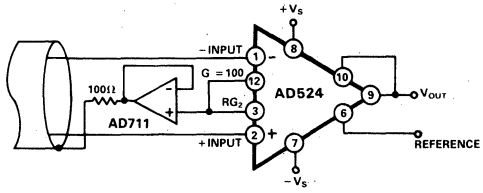


Figure 35. Shield Driver, G ≥ 100

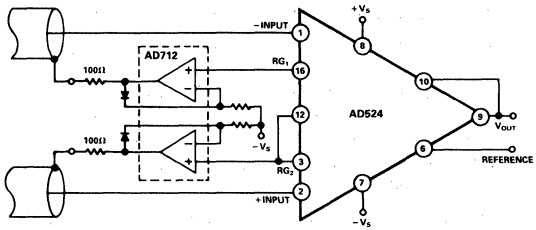


Figure 36. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths

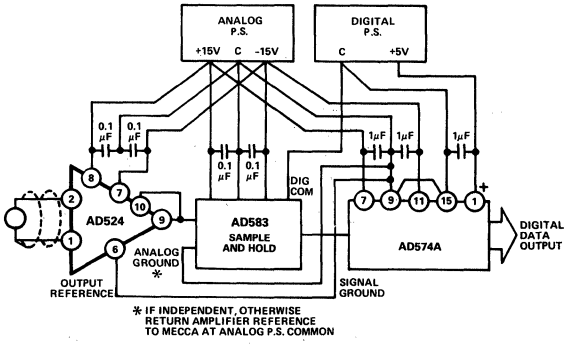


Figure 37. Basic Grounding Practice

have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

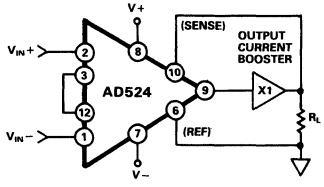


Figure 38. AD524 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 38 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset.

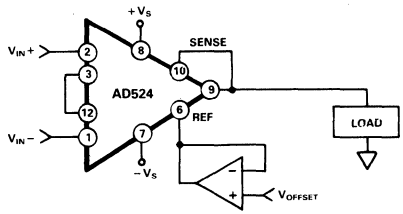


Figure 39. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path thereby upsetting the common-mode rejection of the IA.

In the AD524 a reference source resistance will unbalance the CMR trim by the ratio of $20k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 86dB (20kΩ/1Ω = 86dB). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 39. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 40.

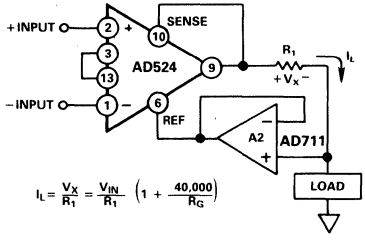


Figure 40. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 41 shows the AD524 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

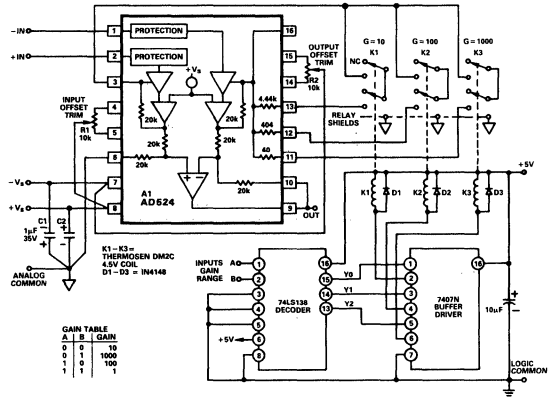


Figure 41. 3 Decade Gain Programmable Amplifier

The AD524 can also be connected for gain in the output stage. Figure 42 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common rejection ratio degradation.

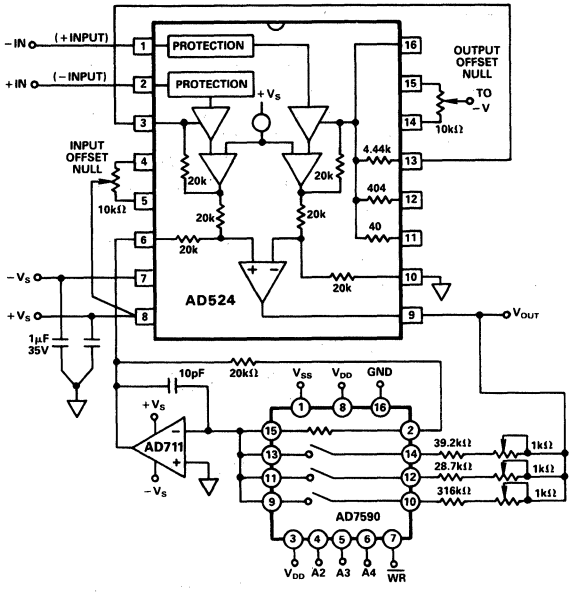


Figure 42. Programmable Output Gain

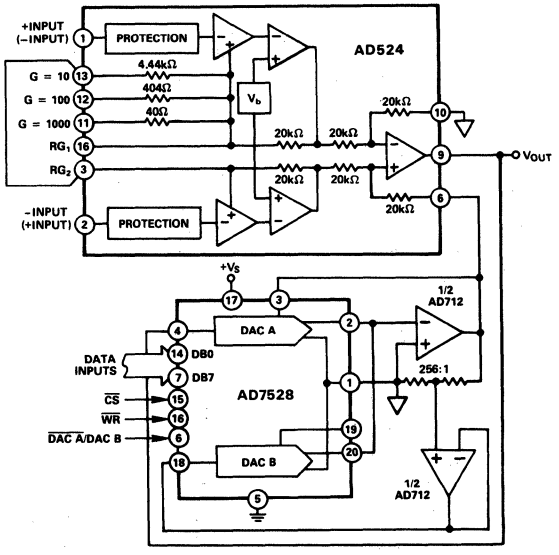
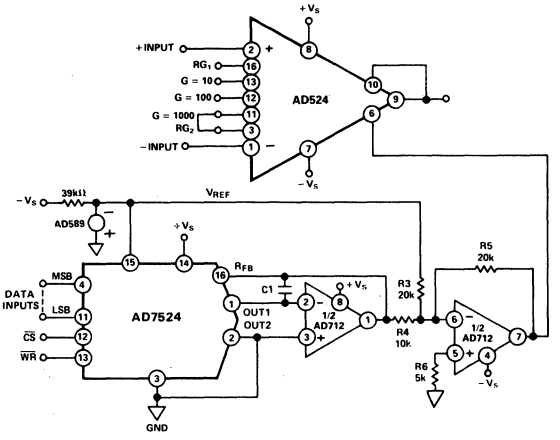


Figure 43. Programmable Output Gain Using a DAC

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 44 show a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.



In many applications complex software algorithms for auto-zero applications are not available. For those applications Figure 45 provides a hardware solution.

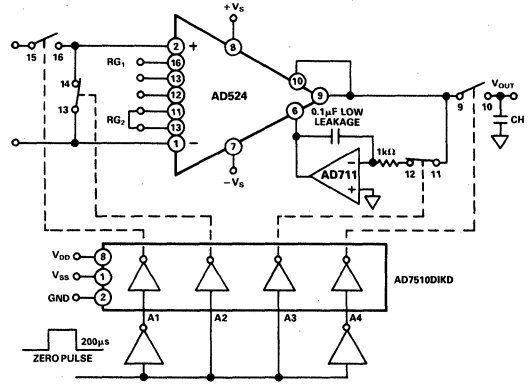


Figure 45. Auto-Zero Circuit

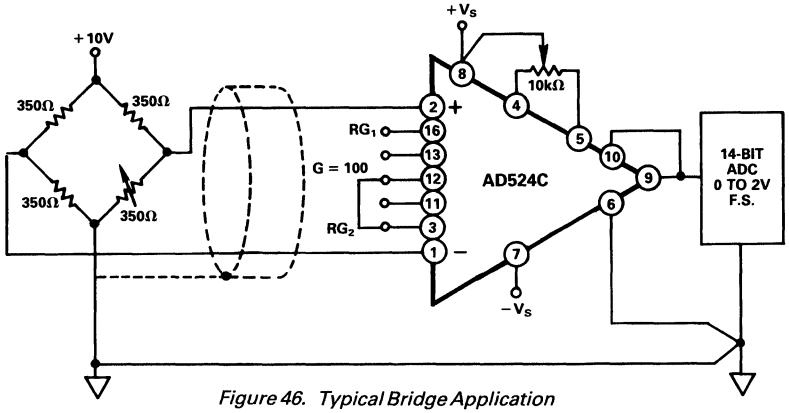


Figure 46. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 46 shows a differential transducer, unbalanced by 100Ω, supplying a 0 to 20mV signal to an AD524C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (45ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.004%.

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500ppm	2500ppm	2500ppm	–
Gain Instability	25ppm	(25ppm/°C)(60°C) = 1500ppm	–	1500ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30ppm	–	–	30ppm
Input Offset Voltage	±50μV, RTI	±50μV/20mV = ±2500ppm	2500ppm	2500ppm	–
Input Offset Voltage Drift	±0.5μV/°C	(±0.5μV/°C)(60°C) = 30μV 30μV/20mV = 1500ppm	–	1500ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±25μV/°C	(±25μV/°C)(60°C) = 1500μV 1500μV/20mV = 750ppm	–	750ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(100Ω) = 1.5μV 1.5μV/20mV = 75ppm	75ppm	75ppm	–
Bias Current – Source Imbalance Drift	±100pA/°C	(±100pA/°C)(100Ω)(60°C) = 0.6μV 0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(100Ω) = 1μV 1μV/20mV = 50ppm	50ppm	50ppm	–
Offset Current – Source Imbalance Drift	±100pA/°C	(100pA/°C)(100Ω)(60°C) = 0.6μV 0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV 3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 8.8μV 8.8μV/20mV = 444ppm	444ppm	444ppm	–
Noise, RTI (0.1–10Hz)	0.3μV p-p	0.3μV p-p/20mV = 15ppm	–	–	15ppm
		Total Error	6656.5ppm	10516.5ppm	45ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Table II. Error Budget Analysis of AD524CD in Bridge Application

Figure 47 shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple–iron(+)–constantan– is compensated for by a voltage developed in series by the temperature-sensitive output current of an AD590 semiconductor temperature sensor.

The circuit is calibrated by adjusting R_T for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within ±0.5°C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of R_T and R_A.

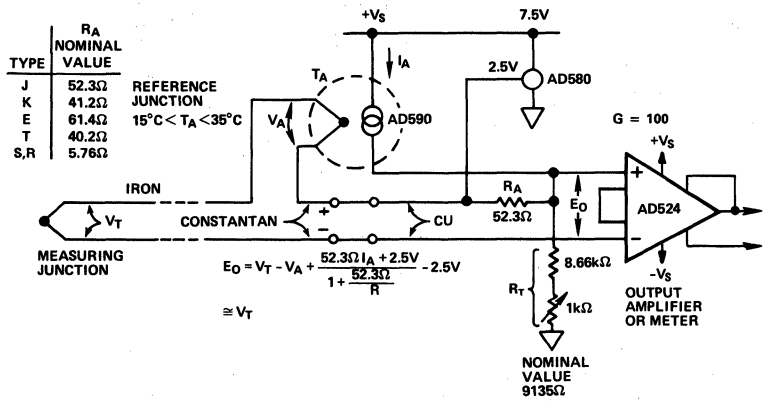


Figure 47. Cold-Junction Compensation

The microprocessor controlled data acquisition system shown in Figure 48 includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

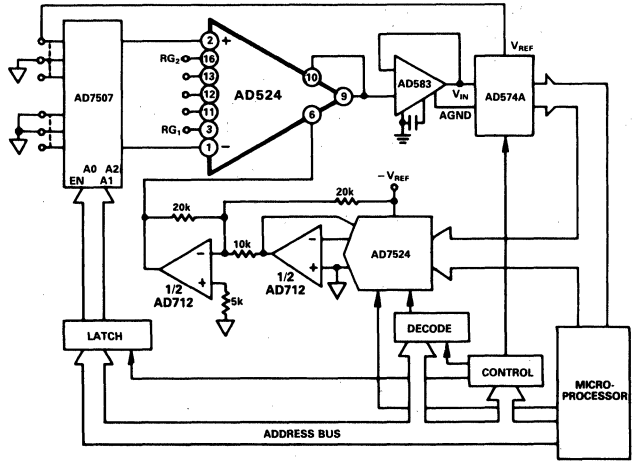


Figure 48. Microprocessor Controlled Data Acquisition System

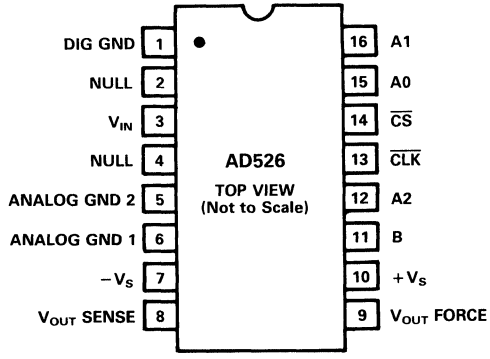
Software Programmable Gain Amplifier

AD526

FEATURES

Digitally Programmable Binary Gains from 1 to 16
Two-Chip Cascade Mode Achieves Binary Gain from 1 to 256
Gain Error:
0.01% max, Gain = 1, 2, 4 (C Grade)
0.02% max, Gain = 8, 16 (C Grade)
0.5ppm/°C Drift Over Temperature
Fast Settling Time
10V Signal Change:
0.01% in 4.5μs (Gain = 16)
Gain Change:
0.01% in 5.6μs (Gain = 16)
Low Nonlinearity: ±0.005% FSR max (J Grade)
Excellent DC Accuracy:
Offset Voltage: 0.5mV max (C Grade)
Offset Voltage Drift: 3μV/°C (C Grade)
TTL Compatible Digital Inputs

AD526 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD526 is a single-ended, monolithic software programmable gain amplifier (SPGA) that provides gains of 1, 2, 4, 8 and 16. It is complete, including amplifier, resistor network and TTL-compatible latched inputs, and requires no external components.

Low gain error and low nonlinearity make the AD526 ideal for precision instrumentation applications requiring programmable gain. The small signal bandwidth is 350kHz at a gain of 16. In addition, the AD526 provides excellent dc precision. The FET-input stage results in a low bias current of 50pA. A guaranteed maximum input offset voltage of 0.5mV max (C grade) and low gain error (0.01%, G = 1, 2, 4, C grade) are accomplished using Analog Devices' laser trimming technology.

To provide flexibility to the system designer, the AD526 can be operated in either latched or transparent mode. The force/sense configuration preserves accuracy when the output is connected to remote or low impedance loads.

The AD526 is offered in one commercial (0 to +70°C) grade, J, and three industrial grades, A, B and C, which are specified from −40°C to +85°C. The S grade is specified from −55°C to +125°C. The military version is available processed to MIL-STD 883B, Rev C. The J grade is supplied in a 16-pin plastic DIP, and the other grades are offered in a 16-pin hermetic side-brazed ceramic DIP.

APPLICATION HIGHLIGHTS

1. **Dynamic Range Extension for ADC Systems:** A single AD526 in conjunction with a 12-bit ADC can provide 96dB of dynamic range for ADC systems.
2. **Gain Ranging Pre-Amps:** The AD526 offers complete digital gain control with precise gains in binary steps from 1 to 16. Additional gains of 32, 64, 128 and 256 are possible by cascading two AD526s.

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD526J Min	AD526J Typ	AD526J Max	AD526A Min	AD526A Typ	AD526A Max	AD526B/S Min	AD526B/S Typ	AD526B/S Max	AD526C Min	AD526C Typ	AD526C Max	Units
GAIN													
Gain Range													
(Digitally Programmable)		1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16		
Gain Error													
G = 1			**0.05**			**0.02**			**0.01**			**0.01**	%
G = 2			**0.05**			**0.03**			**0.02**			**0.01**	%
G = 4			**0.10**			**0.03**			**0.02**			**0.01**	%
G = 8			**0.15**			**0.07**			**0.04**			**0.02**	%
G = 16			**0.15**			**0.07**			**0.04**			**0.02**	%
Gain Error Drift													
Over Temperature													
G = 1		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 2		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 4		0.5	3.0		0.5	3.0		0.5	3.0		0.5	3.0	ppm/°C
G = 8		0.5	5.0		0.5	5.0		0.5	5.0		0.5	5.0	ppm/°C
G = 16		1.0	5.0		1.0	5.0		1.0	5.0		1.0	5.0	ppm/°C
Gain Error (T_{min} to T_{max})													
G = 1			0.06			**0.03**			**0.02**			**0.015**	%
G = 2			0.06			**0.04**			**0.03**			**0.015**	%
G = 4			0.12			**0.04**			**0.03**			**0.015**	%
G = 8			0.17			**0.08**			**0.05**			**0.03**	%
G = 16			0.17			**0.08**			**0.05**			**0.03**	%
Nonlinearity													
G = 1			**0.005**			**0.005**			**0.005**			**0.0035**	% FSR
G = 2			0.001			0.001			0.001			0.001	% FSR
G = 4			0.001			0.001			0.001			0.001	% FSR
G = 8			0.001			0.001			0.001			0.001	% FSR
G = 16			0.001			0.001			0.001			0.001	% FSR
Nonlinearity (T_{min} to T_{max})													
G = 1			0.01			**0.01**			**0.01**			**0.007**	% FSR
G = 2			0.001			0.001			0.001			0.001	% FSR
G = 4			0.001			0.001			0.001			0.001	% FSR
G = 8			0.001			0.001			0.001			0.001	% FSR
G = 16			0.001			0.001			0.001			0.001	% FSR
VOLTAGE OFFSET, ALL GAINS													
Input Offset Voltage		0.4	**1.5**		0.25	**0.7**		0.25	**0.5**		0.25	**0.5**	mV
Input Offset Voltage Drift Over Temperature		5	20		3	10		3	10		3	10	µV/°C
Input Offset Voltage T_{min} to T_{max}			2.0			**1.0**			**0.8**			**0.8**	mV
Input Offset Voltage vs. Supply (V_S ± 10%)	**80**			**80**			**84**			**90**			dB
INPUT BIAS CURRENT													
Over Input Voltage Range ± 10V		50	**150**		50	**150**		50	**150**		50	**150**	pA
ANALOG INPUT CHARACTERISTICS													
Voltage Range													
(Linear Operation)	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Capacitance		5			5			5			5		pF
RATED OUTPUT													
Voltage	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Current (V_{OUT} = ±10V)	**±5**	±10		**±5**	±10		**±5**	±10		**±5**	±10		mA
Short-Circuit Current	**15**	30		**15**	30		**15**	30		**15**	30		mA
DC Output Resistance		0.002			0.002			0.002			0.002		Ω
Load Capacitance (For Stable Operation)		700			700			700			700		pF
NOISE, ALL GAINS													
Voltage Noise, RTI													
0.1Hz to 10Hz		3			3			3			3		µV p-p
Voltage Noise Density, RTI													
f = 10Hz		70			70			70			70		$nV\sqrt{Hz}$
f = 100Hz		60			60			60			60		$nV\sqrt{Hz}$
f = 1kHz		30			30			30			30		$nV\sqrt{Hz}$
f = 10kHz		25			25			25			25		$nV\sqrt{Hz}$

Model	AD526J Min	AD526J Typ	AD526J Max	AD526A Min	AD526A Typ	AD526A Max	AD526B/S Min	AD526B/S Typ	AD526B/S Max	AD526C Min	AD526C Typ	AD526C Max	Units
DYNAMIC RESPONSE													
−3dB Bandwidth (Small Signal)													
G = 1		4.0			4.0			4.0			4.0		MHz
G = 2		2.0			2.0			2.0			2.0		MHz
G = 4		1.5			1.5			1.5			1.5		MHz
G = 8		0.65			0.65			0.65			0.65		MHz
G = 16		0.35			0.35			0.35			0.35		MHz
Signal Settling Time to 0.01% (ΔV_{OUT} = ±10V)													
G = 1		2.1	4		2.1	4		2.1	4		2.1	4	µs
G = 2		2.5	5		2.5	5		2.5	5		2.5	5	µs
G = 4		2.7	5		2.7	5		2.7	5		2.7	5	µs
G = 8		3.6	7		3.6	7		3.6	7		3.6	7	µs
G = 16		4.1	7		4.1	7		4.1	7		4.1	7	µs
Full Power Bandwidth													
G = 1, 2, 4		0.10			0.10			0.10			0.10		MHz
G = 8, 16		0.35			0.35			0.35			0.35		MHz
Slew Rate													
G = 1, 2, 4	**4**	6		**4**	6		**4**	6		**4**	6		V/µs
G = 8, 16	**18**	24		**18**	24		**18**	24		**18**	24		V/µs
DIGITAL INPUTS (T_{min} to T_{max})													
Input Current (V_H = 5V)	60	100	140	60	100	140	60	100	140	60	100	140	µA
Logic "1"	2		6	2		6	2		6	2		6	V
Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
TIMING[1] (V_L = 0.2V, V_H = 3.7V)													
A0, A1, A2													
T_C	50			50			50			50			ns
T_S	30			30			30			30			ns
T_H	30			30			30			30			ns
B													
T_C	50			50			50			50			ns
T_S	40			40			40			40			ns
T_H	10			10			10			10			ns
TEMPERATURE RANGE													
Specified Performance	0		+70	−40		+85	−40/−55		+85/+125	−40		+85	°C
Storage	−65		+125	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Operating Range	**±4.5**		**±16.5**	**±4.5**		**±16.5**	**±4.5**		**±16.5**	**±4.5**		**±16.5**	V
Positive Supply Current		10	**14**		10	**14**		10	**14**		10	**14**	mA
Negative Supply Current		10	**13**		10	**13**		10	**13**		10	**13**	mA
PACKAGE OPTIONS[2]													
Plastic (N-16)	AD526JN												
Ceramic DIP (D-16)				AD526AD			AD526BD AD526SD AD526SD/883B			AD526CD			

NOTE

[1]Refer to Figure 35 for definitions.
FSR = Full-Scale Range = 20V.
RTI = Referred to Input.
[2]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Typical Characteristics

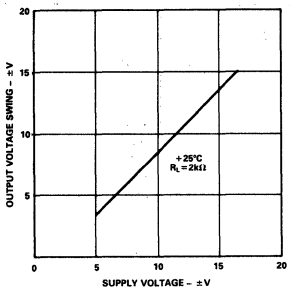


Figure 1. Output Voltage Swing vs. Supply Voltage, G = 16

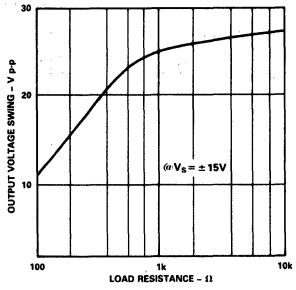


Figure 2. Output Voltage Swing vs. Load Resistance

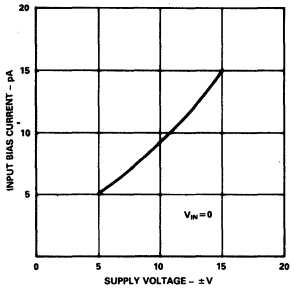


Figure 3. Input Bias Current vs. Supply Voltage

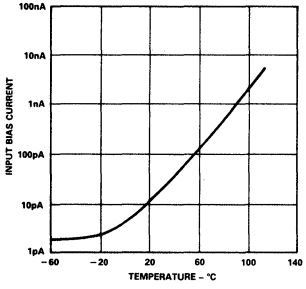


Figure 4. Input Bias Current vs. Temperature

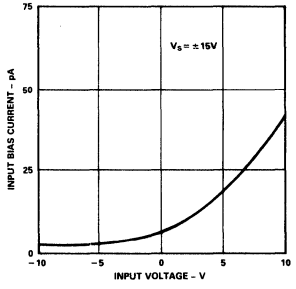


Figure 5. Input Bias Current vs. Input Voltage

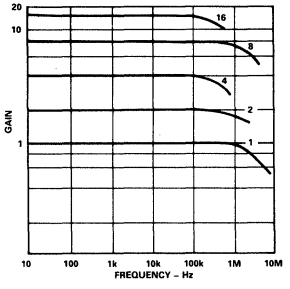


Figure 6. Gain vs. Frequency

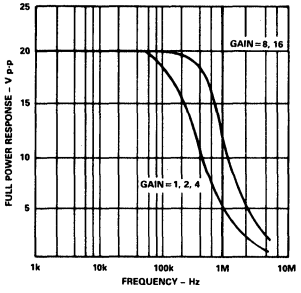


Figure 7. Large Signal Frequency Response

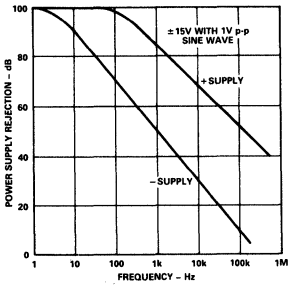


Figure 8. PSRR vs. Frequency

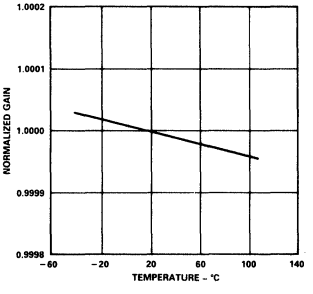


Figure 9. Normalized Gain vs. Temperature, Gain = 1

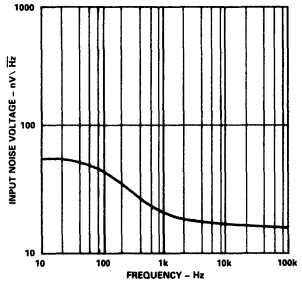


Figure 10. Noise Spectral Density

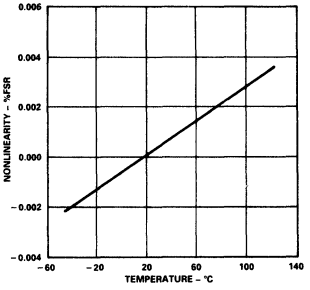


Figure 11. Nonlinearity vs. Temperature, Gain = 1

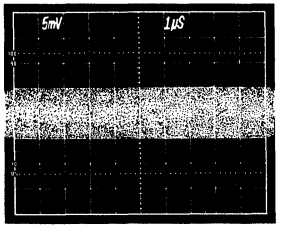


Figure 12. Wideband Output Noise, G = 16 (Amplified by 10)

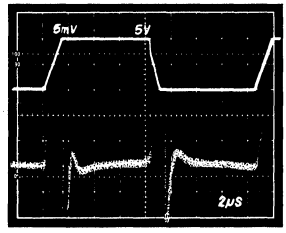


Figure 13. Large Signal Pulse Response and Settling Time*, G = 1

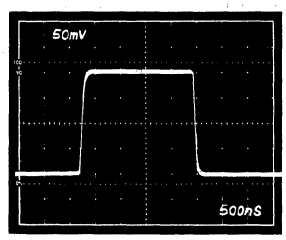


Figure 14. Small Signal Pulse Response, G = 1

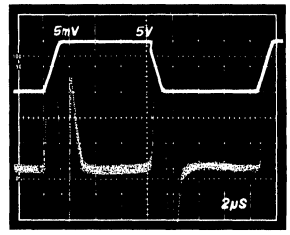


Figure 15. Large Signal Pulse Response and Settling Time*, G = 2

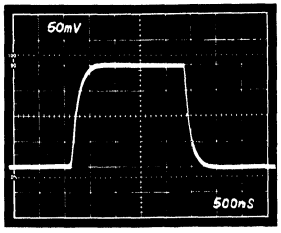


Figure 16. Small Signal Pulse Response, G = 2

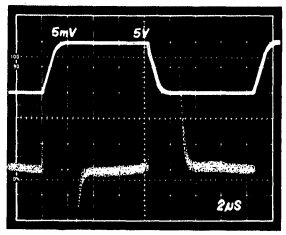


Figure 17. Large Signal Pulse Response and Settling Time*, G = 4

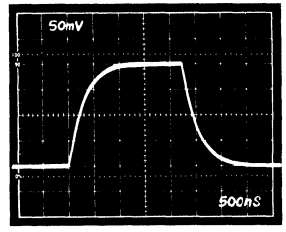


Figure 18. Small Signal Pulse Response, G = 4

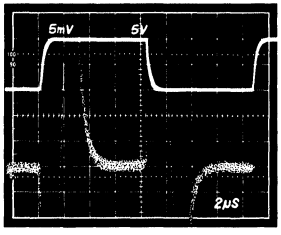


Figure 19. Large Signal Pulse Response and Settling Time*, G = 8

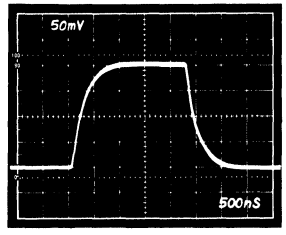


Figure 20. Small Signal Pulse Response, G = 8

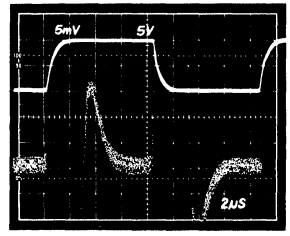


Figure 21. Large Signal Pulse Response and Settling Time*, G = 16

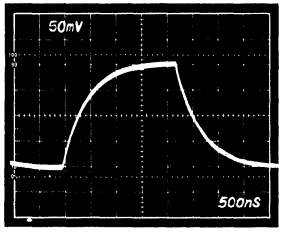


Figure 22. Small Signal Pulse Response, Gain = 16

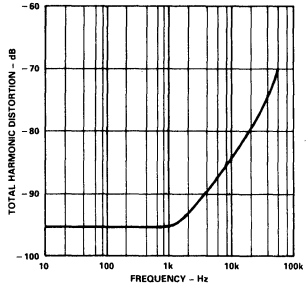


Figure 23. Total Harmonic Distortion vs. Frequency, Gain = 16

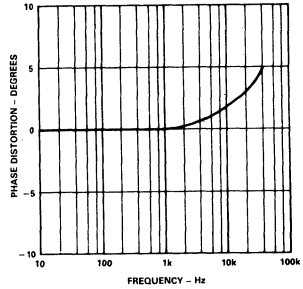


Figure 24. Phase Distortion vs. Frequency, Gain = 16

*For Settling Time Traces, 0.01% = 1/2 Vertical Division

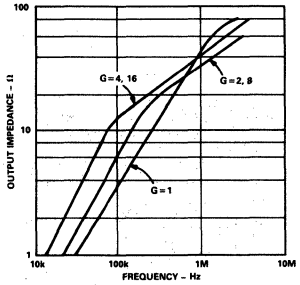


Figure 25. Output Impedance vs. Frequency

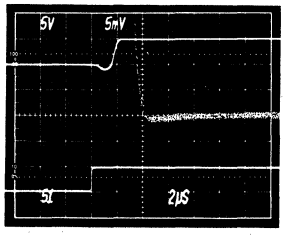


Figure 26. Gain Change Settling Time, Gain Change: 1 to 2*

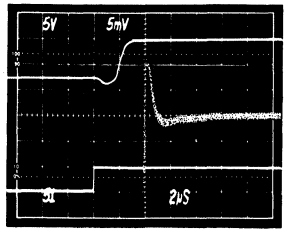


Figure 27. Gain Change Settling Time, Gain Change 1 to 4*

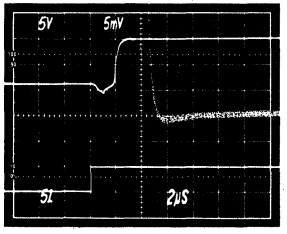


Figure 28. Gain Change Settling Time, Gain Change 1 to 8*

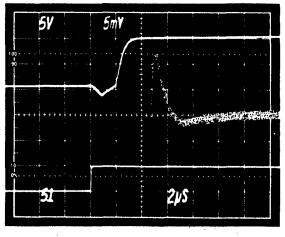


Figure 29. Gain Change Settling Time, Gain Change 1 to 16*

*Scope Traces are:
Top: Output Transition
Middle: Output Settling
Bottom: Digital Input

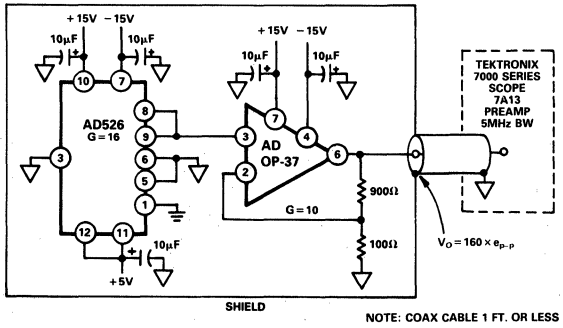


Figure 30. Wideband Noise Test Circuit

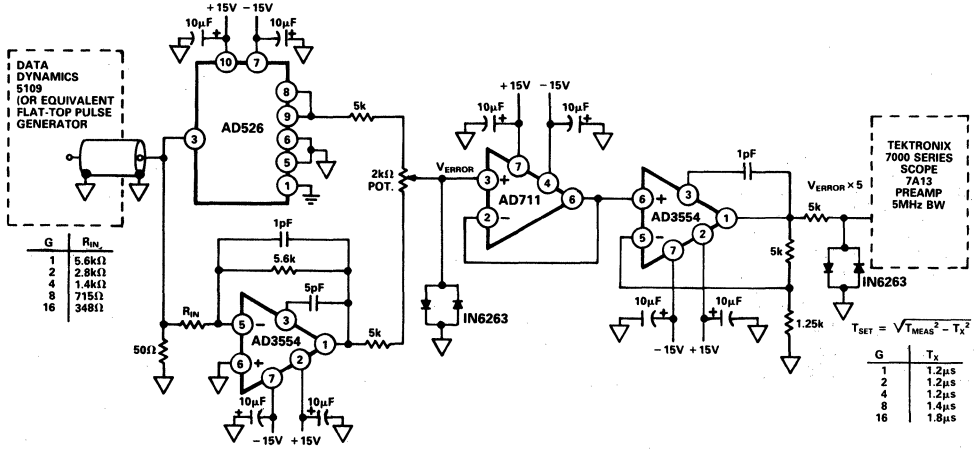


Figure 31. Settling Time Test Circuit

THEORY OF OPERATION

The AD526 is a complete software programmable gain amplifier (SPGA) implemented monolithically with a drift-trimmed BiFET amplifier, a laser wafer trimmed resistor network, JFET analog switches and TTL compatible gain code latches.

A particular gain is selected by applying the appropriate gain code (see Table I) to the control logic. The control logic turns on the JFET switch that connects the correct tap on the gain network to the inverting input of the amplifier; all unselected JFET gain switches are off (open). The "on" resistance of the gain switches causes negligible gain error since only the amplifier's input bias current, which is less than 150pA, actually flows through these switches.

The AD526 is capable of storing the gain code, (latched mode), B, A0, A1, A2, under the direction of control inputs $\overline{CLK}$ and $\overline{CS}$. Alternatively, the AD526 can respond directly to gain code changes if the control inputs are tied low (transparent mode).

For gains of 8 and 16, a fraction of the frequency compensation capacitance (C1 in Figure 32) is automatically switched out of the circuit. This increases the amplifier's bandwidth and improves its signal settling time and slew rate.

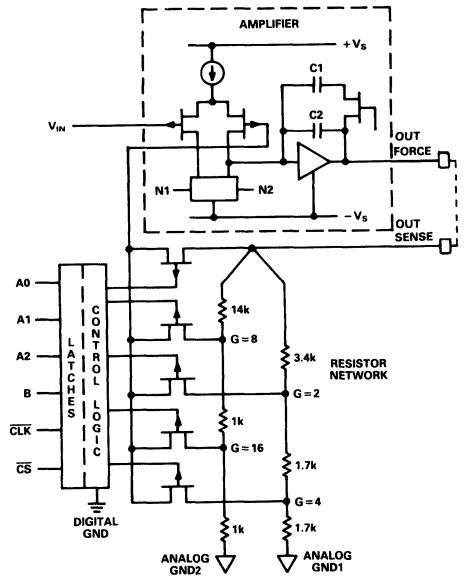


Figure 32. Simplified Schematic of the AD526

TRANSPARENT MODE OF OPERATION

In the transparent mode of operation, the AD526 will respond directly to level changes at the gain code inputs (A0, A1, A2) if B is tied high and both $\overline{CS}$ and $\overline{CLK}$ are allowed to float low.

After the gain codes are changed, the AD526's output voltage typically requires 5.5μs to settle to within 0.01% of the final value. Figures 26 to 29 show the performance of the AD526 for positive gain code changes.

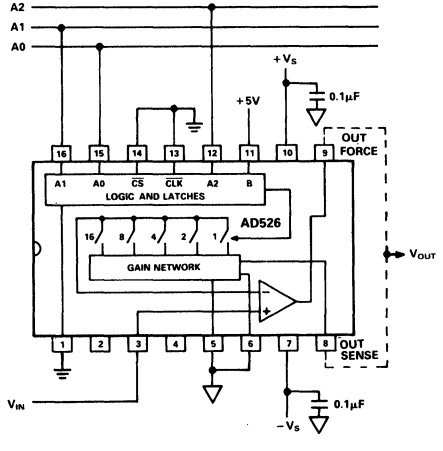


Figure 33. Transparent Mode

LATCHED MODE OF OPERATION

The latched mode of operation is shown in Figure 34. When either $\overline{CS}$ or $\overline{CLK}$ go to a logic "1," the gain code (A0, A1, A2, B) signals are latched into the registers and held until both $\overline{CS}$ and $\overline{CLK}$ return to "0." *Unused $\overline{CS}$ or $\overline{CLK}$ inputs should be tied to ground.* The $\overline{CS}$ and $\overline{CLK}$ inputs are functionally and electrically equivalent.

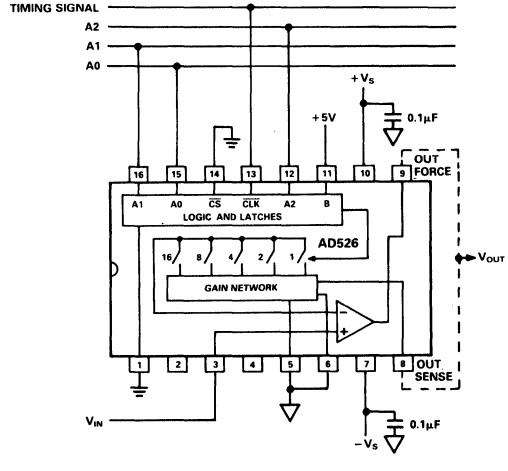


Figure 34. Latched Mode

GAIN CODE				CONTROL	CONDITION	
A2	A1	A0	B	$\overline{CLK}$ ($\overline{CS}$ = 0)	Gain	Condition
X	X	X	X	1	Previous State	Latched
0	0	0	1	0	1	Transparent
0	0	1	1	0	2	Transparent
0	1	0	1	0	4	Transparent
0	1	1	1	0	8	Transparent
1	X	X	1	0	16	Transparent
X	X	X	0	0	1	Transparent
X	X	X	0	1	1	Latched
0	0	0	1	1	1	Latched
0	0	1	1	1	2	Latched
0	1	0	1	1	4	Latched
0	1	1	1	1	8	Latched
1	X	X	1	1	16	Latched

NOTE: X = Don't Care

Table I. AD526 Logic Input Truth Table

The specifications on page 3 in combination with Figure 35 give the timing requirements for loading new gain codes.

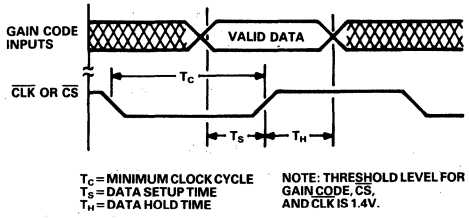


Figure 35. AD526 Timing

DIGITAL FEEDTHROUGH

With either $\overline{CS}$ or $\overline{CLK}$ or both held high, the AD526 gain state will remain constant regardless of the transitions at the A0, A1, A2 or B inputs. However, high-speed logic transitions will unavoidably feed through to the analog circuitry within the AD526 causing spikes to occur at the signal output.

This feedthrough effect can be completely eliminated by operating the AD526 in the transparent mode and latching the gain code in an external bank of latches (Figure 36).

To operate the AD526 using serial inputs, the configuration shown in Figure 36 can be used with the 74LS174 replaced by a serial-in/parallel-out latch, such as the 54LS594.

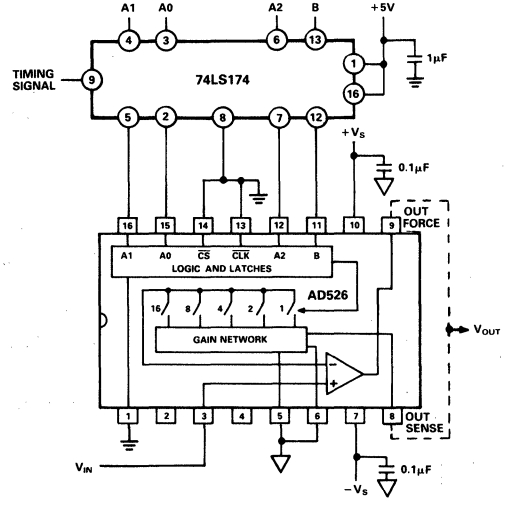


Figure 36. Using an External Latch to Minimize Digital Feedthrough

GROUNDING AND BYPASSING

Proper signal and grounding techniques must be applied in board layout so that specified performance levels of precision data acquisition components, such as the AD526, are not degraded.

As is shown in Figure 37, logic and signal grounds should be separate. By connecting the signal source ground locally to the AD526 analog ground Pins 5 and 6, gain accuracy of the AD526 is maintained. This ground connection should not be corrupted by currents associated with other elements within the system.

Utilizing the force and sense outputs of the AD526, as shown in Figure 38, avoids signal drops along etch runs to low impedance loads.

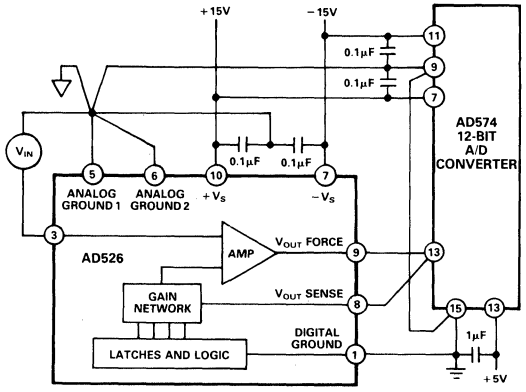


Figure 37. Grounding and Bypassing

CASCADED OPERATION

A cascade of two AD526s can be used to achieve binarily weighted gains from 1 to 256. If gains from 1 to 128 are needed, no additional components are required. This is accomplished by using the B pin as shown in Figure 38. When the B pin is low, the AD526 is held in a unity gain stage independent of the other gain code values.

V_{OUT}/V_{IN}	A2	A1	A0
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0
32	1	0	1
64	1	1	0
128	1	1	1

Table II. Logic Table for Figure 38

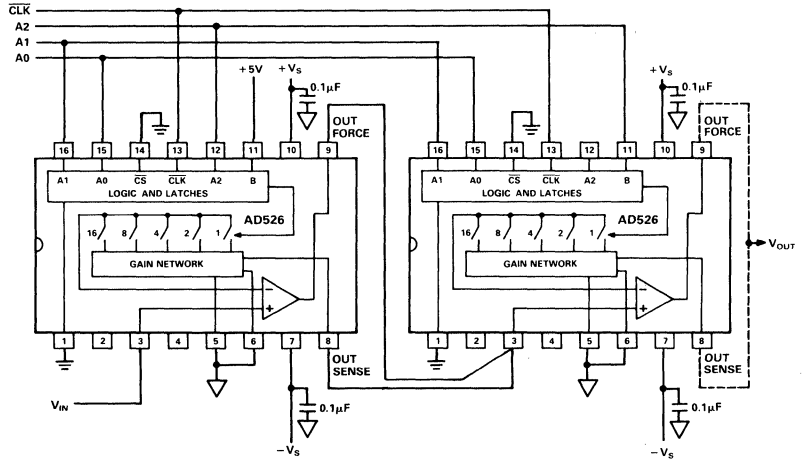


Figure 38. Cascaded Operation

OFFSET NULLING

Input voltage offset nulling of the AD526 is best accomplished at a gain of 16, since the referred-to-input (RTI) offset is amplified the most at this gain and therefore is most easily trimmed. The resulting trimmed value of RTI voltage offset typically varies less than 3μV across all gain ranges.

Note that the low input current of the AD526 minimizes RTI voltage offsets due to source resistance.

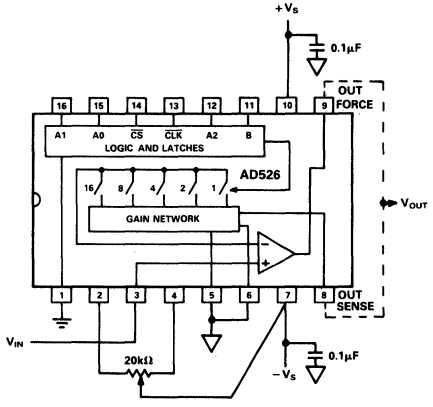


Figure 39. Offset Voltage Null Circuit

OUTPUT CURRENT BOOSTER

The AD526 is rated for a full ±10V output voltage swing into 2kΩ. In some applications, the need exists to drive more current into heavier loads. As shown in Figure 40, a high current booster may be connected "inside the loop" of the SPGA to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the AD526 output amplifier.

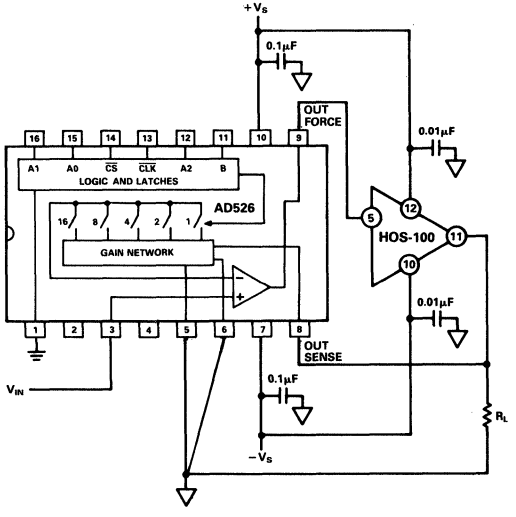


Figure 40. Current Output Boosting

OFFSET NULLING WITH A D/A CONVERTER

Figure 41 shows the AD526 with offset nulling accomplished with an 8-bit D/A converter (AD7524) circuit instead of the potentiometer shown in Figure 39. The calibration procedure is the same as before except that instead of adjusting the potentiometer, the D/A converter corrects for the offset error. This calibration circuit has a number of benefits in addition to eliminating the trimpot. The most significant benefit is that calibration can be under the control of a microprocessor and therefore can be implemented as part of an autocalibration scheme. Secondly, dipswitches or RAM can be used to hold the 8-bit word after its value has been determined. In Figure 42 the offset null sensitivity, at a gain of 16, is 80μV per LSB of adjustment, which guarantees dc accuracy to the 16-bit performance level.

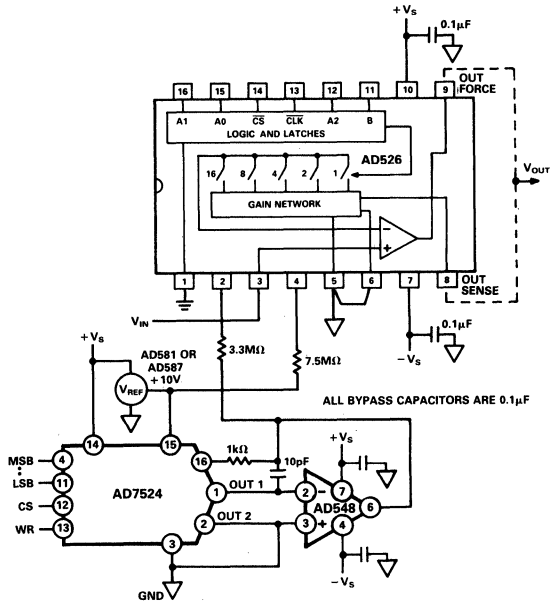


Figure 41. Offset Nulling Using a DAC

FLOATING-POINT CONVERSION

High resolution converters are used in systems to obtain high accuracy, improve system resolution or increase dynamic range. There are a number of high resolution converters available with throughput rates of 66.6kHz that can be purchased as a single component solution; however in order to achieve higher throughput rates, alternative conversion techniques must be employed. A floating point A/D converter can improve both throughput rate and dynamic range of a system.

In a floating point A/D converter (Figure 42), the output data is presented as a 16-bit word, the lower 12 bits from the A/D converter form the mantissa and the upper 4 bits from the digital signal used to set the gain form the exponent. The AD526 programmable gain amplifier in conjunction with the comparator circuit scales the input signal to a range between half scale and full scale for the maximum usable resolution.

The A/D converter diagrammed in Figure 42 consists of a pair of AD585 sample/hold amplifiers, a flash converter, a five-range programmable gain amplifier (the AD526) and a fast 12-bit A/D converter (the AD7572). The floating-point A/D converter achieves its high throughput rate of 125kHz by overlapping the acquisition time of the first sample/hold amplifier and the settling time of the AD526 with the conversion time of the A/D converter. The first sample/hold amplifier holds the signal for the flash autoranger, which determines which binary quantum the input falls within, relative to full scale. Once the AD526 has settled to the appropriate level, then the second sample/hold amplifier can be put into hold which holds the amplified signal while the AD7572 performs its conversion routine. The acquisition time for the AD585 is 3μs, and the conversion time for the AD7572 is 5μs for a total of 8μs, or 125kHz. This performance relies on the fast settling characteristics of the AD526 after the flash autoranging (comparator) circuit quantizes the input signal. A 16-bit register holds the 3-bit output from the flash autoranger and the 12-bit output of the AD7572.

The A/D converter in Figure 42 has a dynamic range of 96dB. The dynamic range of a converter is the ratio of the full-scale input range to the LSB value. With a floating-point A/D converter the smallest value LSB corresponds to the LSB of the monolithic converter divided by the maximum gain of the PGA. The floating point A/D converter has a full-scale range of 5V, a maximum gain of 16V/V from the AD526 and a 12-bit A/D converter; this produces:

LSB = ([FSR/2^N]/Gain) = ([5V/4096]/16) = 76μV. The dynamic range in dBs is based on the log of the ratio of the full-scale input range to the LSB; dynamic range = 20log(5V/76μV) = 96dB.

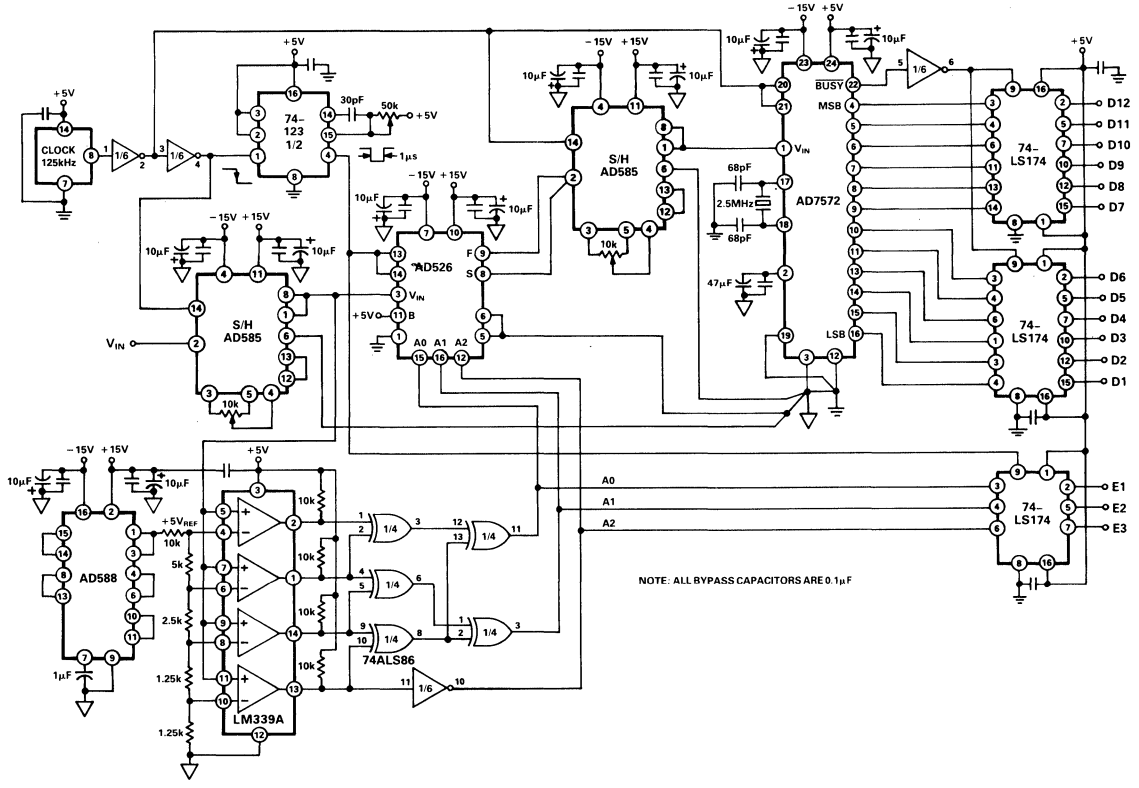


Figure 42. Floating-Point A/D Converter

HIGH ACCURACY A/D CONVERTERS

Very high accuracy and high resolution floating-point A/D converters can be achieved by the incorporation of offset and gain calibration routines. There are two techniques commonly used for calibration, a hardware circuit as shown in Figure 43 and/or a software routine. In this application the microprocessor is functioning as the autoranging circuit, requiring software overhead; therefore, a hardware calibration technique was applied which reduces the software burden. The software is used to set the gain of the AD526. In operation the signal is converted, and if the MSB of the AD574 is not equal to a logical 1, the gain is increased by binary steps, up to the maximum gain. This maximizes the full-scale range of the conversion process and insures a wide dynamic range.

The calibration technique uses two point correction, offset and gain. The hardware is simplified by the use of programmable magnitude comparators, the 74ALS528s, which can be "burned" for a particular code. In order to prevent under or over range hunting during the calibration process, the reference offset and gain codes should be different from the endpoint codes. A calibration cycle consists of selecting whether gain or offset is to be calibrated then selecting the appropriate multiplexer channel to apply the reference voltage to the signal channel. Once the operation has been initiated, the counter, a 74ALS869, drives the D/A converter in a linear fashion providing a small correction voltage to either the gain or offset trim point of the AD574. The output of the A/D converter is then compared to the value preset in the 74ALS528 to determine a match. Once a match is detected, the 74ALS528 produces a low going pulse which stops the counter. The code at the D/A converter is latched until the next calibration cycle. Calibration cycles are under the control of the microprocessor in this application and should be implemented only during periods of converter inactivity.

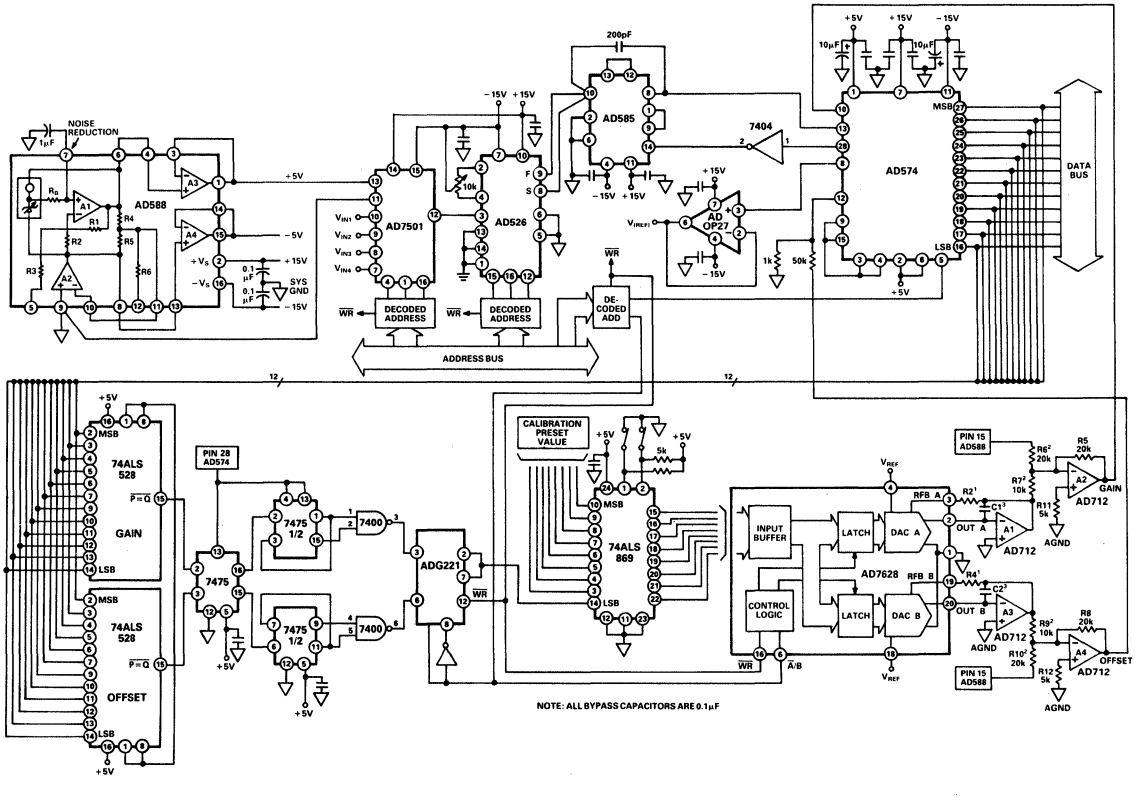


Figure 43. High Accuracy A/D Converter

ANALOG DEVICES

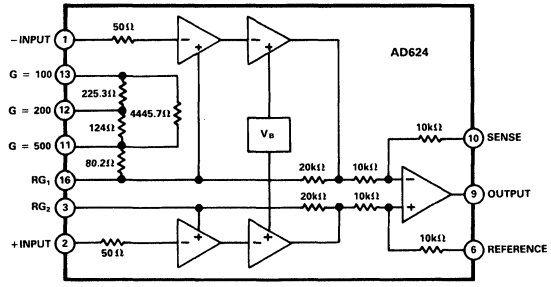
Precision Instrumentation Amplifier

AD624

FEATURES

Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB min (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

AD624 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD624 is a high precision low noise instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25μV/°C, output offset voltage drift of less than 10μV/°C, CMRR above 80dB at unity gain (130dB at G=500) and a maximum nonlinearity of 0.001% at G=1. In addition to these outstanding dc specifications the AD624 exhibits superior ac performance as well. A 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pre-trimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than $4nV/\sqrt{Hz}$ at 1kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pre-trimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD624A			AD624B			AD624C			AD624S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 100			±0.25			±0.15			±0.1			±0.25	%
G = 200, 500			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±1.0			±1.0			±1.0			±1.0	%
Nonlinearity													
G = 1			±0.005			±0.003			±0.001			±0.005	%
G = 100, 200			±0.005			±0.003			±0.001			±0.005	%
G = 500, 1000			±0.005			±0.005			±0.005			±0.005	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 100, 200			10			10			10			10	ppm/°C
G = 500, 1000			25			15			15			15	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			200			75			25			75	µV
vs. Temperature			2			0.5			0.25			2.0	µV/°C
Output Offset Voltage			5			3			2			3	mV
vs. Temperature			50			25			10			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 100, 200	95			105			110			105			dB
G = 500, 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±50			±50			±50			±50		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±20			±20			±20			±20		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common-Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common-Mode Capacitance		10			10			10			10		pF
Input Voltage Range[1]													
Max Differ. Input Linear (V_{DL})		±10			±10			±10			±10		V
Max Common-Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common-Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 100, 200	100			105			110			100			dB
G = 500, 1000	110			120			130			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal −3dB													
G = 1		1			1			1			1		MHz
G = 100		150			150			150			150		kHz
G = 200		100			100			100			100		kHz
G = 500		50			50			50			50		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step													
G = 1 to 200		15			15			15			15		µs
G = 500		35			35			35			35		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		4			4			4			4		$nV/\sqrt{Hz}$
R.T.O.		75			75			75			75		$nV/\sqrt{Hz}$

Model	AD624A Min	AD624A Typ	AD624A Max	AD624B Min	AD624B Typ	AD624B Max	AD624C Min	AD624C Typ	AD624C Max	AD624S Min	AD624S Typ	AD624S Max	Units
R.T.I., 0.1 to 10Hz													
G = 1		10			10			10			10		μV p-p
G = 100		0.3			0.3			0.3			0.3		μV p-p
G = 200, 500, 1000		0.2			0.2			0.2			0.2		μV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}	8	10	12	8	10	12	8	10	12	8	10	12	kΩ
I_{IN}		30			30			30			30		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}	16	20	24	16	20	24	16	20	24	16	20	24	kΩ
I_{IN}		30			30			30			30		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	−25		+85	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	5		3.5	5		3.5	5		3.5	5	mA
PACKAGE[2]													
Ceramic (D-16)		AD624A			AD624B			AD624C			AD624S		
A and S Grade Chips Available													

NOTES

[1] V_{DL} is the maximum differential input voltage at G = 1 for specified nonlinearity. V_{DL} at other gains = 10V/G. V_D = actual differential input voltage. Example: G = 10, V_D = 0.50. V_{CM} = 12V − (10/2 × 0.50V) = 9.5V.

[2] See Section 20 for package outline information.

Specifications subject to change without notice.

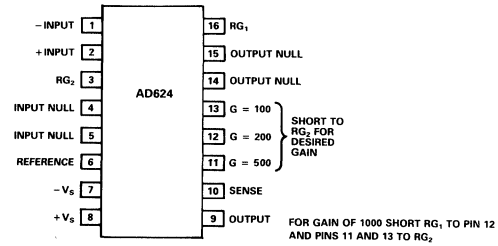
Specifications shown in **boldface** are tested on all production unit at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18V
Internal Power Dissipation 420mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Storage Temperate Range . . . . . −65°C to +150°C
Operating Temperature Range
AD624A/B/C . . . . . −25°C to +85°C
AD624S . . . . . −55°C to +125°C
Lead Temperature (Soldering, 60secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



Typical Characteristics

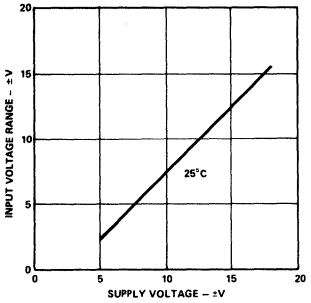


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

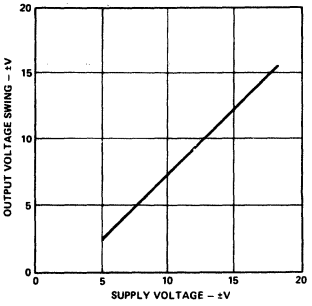


Figure 2. Output Voltage Swing vs. Supply Voltage

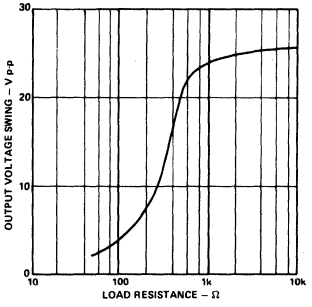


Figure 3. Output Voltage Swing vs. Load Resistance

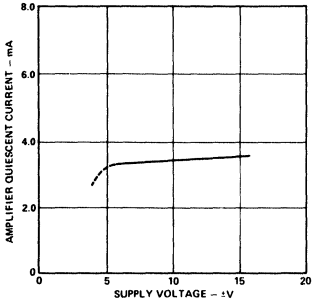


Figure 4. Quiescent Current vs. Supply Voltage

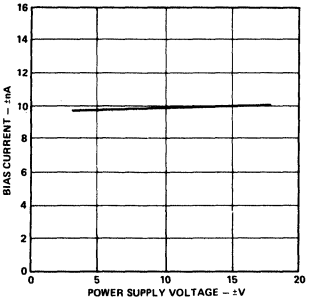


Figure 5. Input Bias Current vs. Supply Voltage

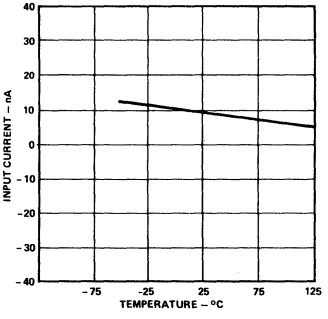


Figure 6. Input Bias Current vs. Temperature

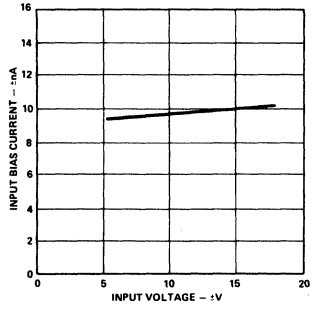


Figure 7. Input Bias Current vs. CMV

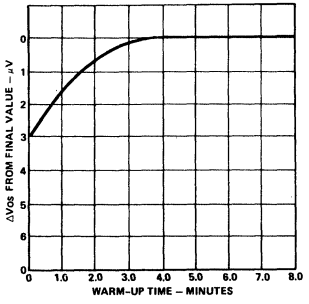


Figure 8. Offset Voltage, RTI, Turn On Drift

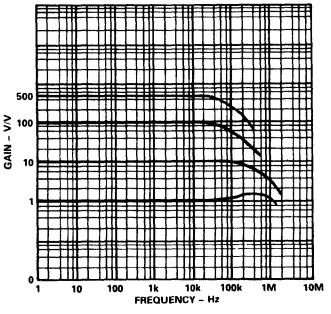


Figure 9. Gain vs. Frequency

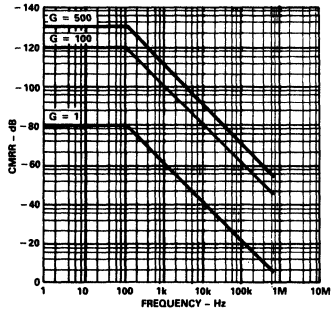


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

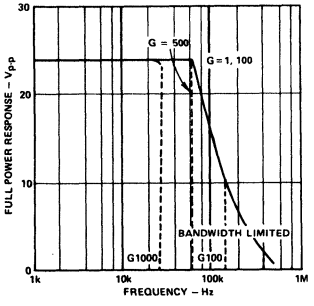


Figure 11. Large Signal Frequency Response

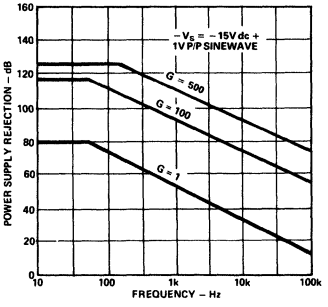


Figure 12. Positive PSRR vs. Frequency

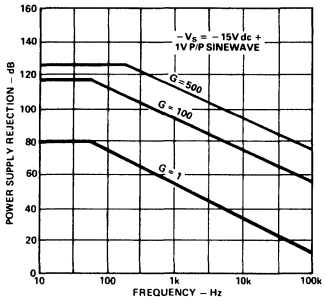


Figure 13. Negative PSRR vs. Frequency

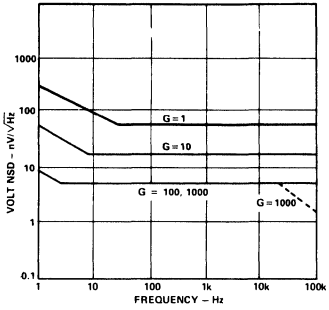


Figure 14. RTI Noise Spectral Density vs. Gain

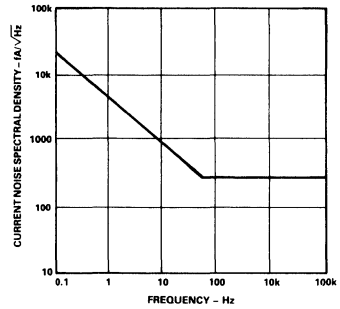


Figure 15. Input Current Noise

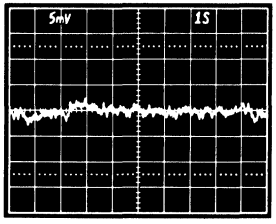


Figure 16. Low Frequency Voltage Noise – G = 1 (System Gain = 1000)

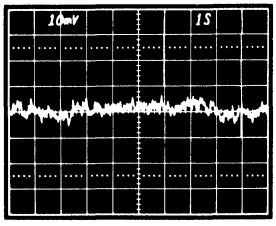


Figure 17. Low Frequency Voltage Noise – G = 1000 (System Gain = 100,000)

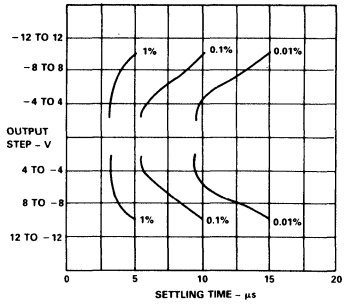


Figure 18. Settling Time Gain = 1

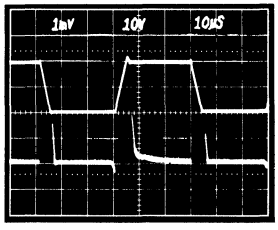


Figure 19. Large Signal Pulse Response and Settling Time – G = 1

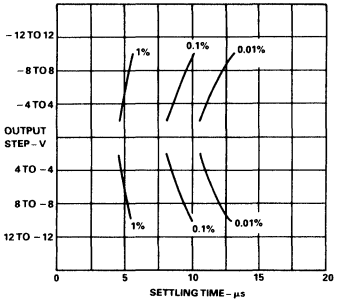


Figure 20. Settling Time Gain = 100

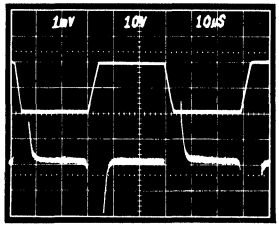


Figure 21. Large Signal Pulse Response and Settling Time G = 100

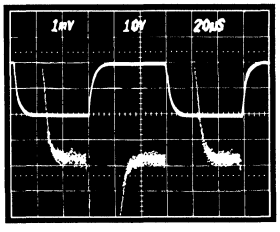


Figure 22. Range Signal Pulse Response and Settling Time G = 500

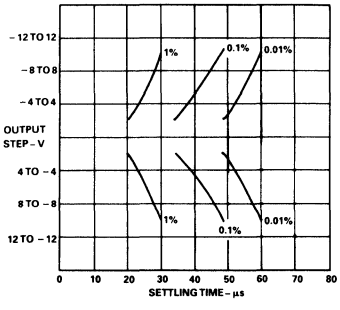


Figure 23. Settling Time Gain = 1000

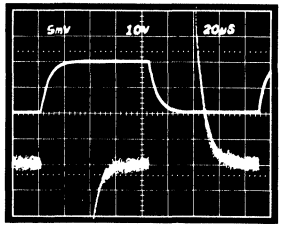


Figure 24. Large Signal Pulse Response and Settling Time G = 1000

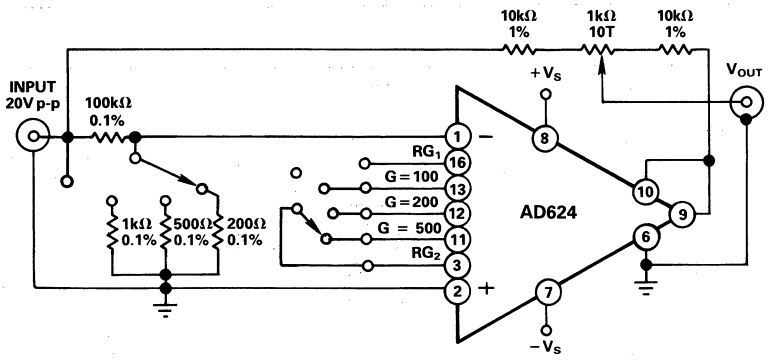


Figure 25. Settling Time Test Circuit

Theory of Operation

The AD624 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp instrumentation amplifier. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components and the high level of performance that this circuit architecture is capable of.

A preamp section (Q1–Q4) develops the programmed gain by the use of feedback concepts. Feedback from the outputs of A1 and A2 forces the collector currents of Q1–Q4 to be constant thereby impressing the input voltage across R_G.

The gain is set by choosing the value of R_G from the equation, Gain $= \frac{40k}{R_G} + 1$. The value of R_G also sets the transconductance of the input preamp stage increasing it asymptotically to the transconductance of the input transistors as R_G is reduced for larger gains. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 3ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $4nV/\sqrt{Hz}$ at G ≥ 500.

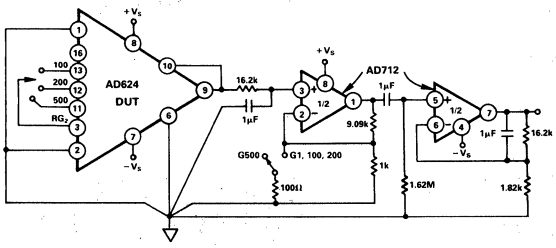


Figure 26. Noise Test Circuit

INPUT CONSIDERATIONS

Under input overload conditions the user will see $R_G + 100\Omega$ and two diode drops (~1.2V) between the plus and minus inputs, in either direction. If safe overload current under all conditions is assumed to be 10mA, the maximum overload voltage is ~ ±2.5V. While the AD624 can withstand this continuously, momentary overloads of ±10V will not harm the device. On the other hand the inputs should never exceed the supply voltage.

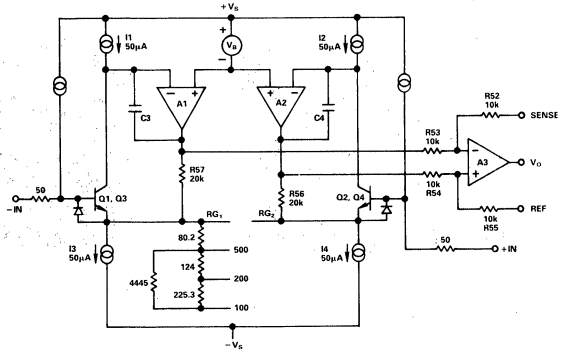


Figure 27. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit.

The AD524 should be considered in applications that require protection from severe input overload. If this is not possible, external protection resistors can be put in series with the inputs of the AD624 to augment the internal (50Ω) protection resistors. This will most seriously degrade the noise performance. For this reason the value of these resistors should be chosen to be as low as possible and still provide 10mA of current limiting under maximum continuous overload conditions. In selecting the value of these resistors, the internal gain setting resistor and the 1.2 volt drop need to be considered. For example, to protect the device from a continuous differential overload of 20V at a gain of 100, 1.9kΩ of resistance is required. The internal gain resistor is 404Ω; the internal protect resistor is 100Ω. There is a 1.2V drop across D1 or D2 and the base-emitter junction of either Q1 and Q3 or Q2 and Q4 as shown in Figure 27, 1400Ω of external resistance would be required (700Ω in series with each input). The RTI noise in this case would be $\sqrt{4KTR_{ext.} + (4nV/\sqrt{Hz})^2} = 6.2nV/\sqrt{Hz}$.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and offset drift each have two components; input and output. Input offset is that component of offset that is

directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD624 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD624 provides for both input and output offset adjustment. This optimizes nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD624 includes high accuracy pre-trimmed internal gain resistors. These allow for single connection programming of gains of 1, 100, 200 and 500. Additionally, a variety of gains including a pre-trimmed gain of 1000 can be achieved through series and parallel combinations of the internal resistors. Table I shows the available gains and the appropriate pin connections and gain temperature coefficients.

The gain values achieved via the combination of internal resistors are extremely useful. The temperature coefficient of the gain is dependent primarily on the mismatch of the temperature coefficients of the various internal resistors. Tracking of these resistors is extremely tight resulting in the low gain TC's shown in Table I.

If the desired value of gain is not attainable using the internal resistors, a single external resistor can be used to achieve any gain between 1 and 10,000. This resistor connected between

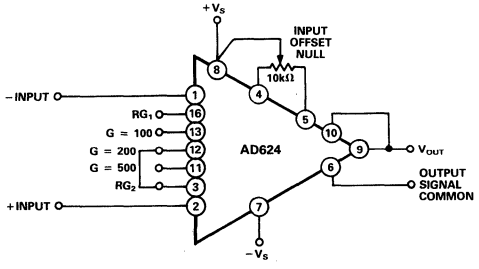


Figure 28. Operating Connections for G =200

Gain (Nominal)	Temperature Coefficient (Nominal)	Pin 3 to Pin	Connect Pins
1	−0ppm/°C	–	–
100	−1.5ppm/°C	13	–
125	−5ppm/°C	13	11 to 16
137	−5.5ppm/°C	13	11 to 12
186.5	−6.5ppm/°C	13	11 to 12 to 16
200	−3.5ppm/°C	12	–
250	−5.5ppm/°C	12	11 to 13
333	−15ppm/°C	12	11 to 16
375	−0.5ppm/°C	12	13 to 16
500	−10ppm/°C	11	–
624	−5ppm/°C	11	13 to 16
688	−1.5ppm/°C	11	11 to 12; 13 to 16
831	+4ppm/°C	11	16 to 12
1000	0ppm/°C	11	16 to 12; 13 to 11

Table I.

pins 3 and 16 programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 29). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors R56 and R57. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−15ppm/°C typ), and the temperature coefficient of the internal interconnections.

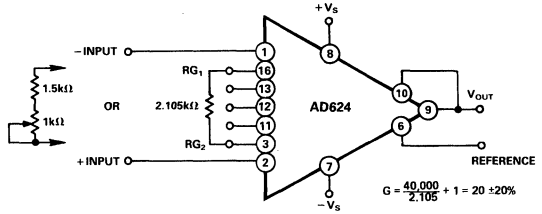


Figure 29. Operating Connections for G = 20

The AD624 may also be configured to provide gain in the output stage. Figure 30 shows an H pad attenuator connected to the reference and sense lines of the AD624. The values of R1, R2 and R3 should be selected to be as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

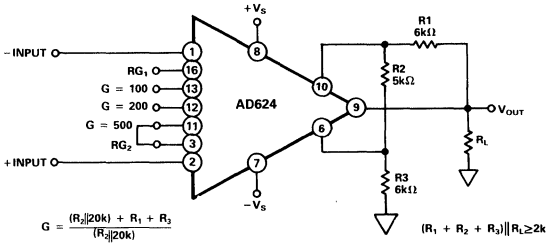


Figure 30. Gain of 2500

NOISE

The AD624 is designed to provide noise performance near the theoretical noise floor. This is an extremely important design criteria as the front end noise of an instrumentation amplifier is the ultimate limitation on the resolution of the data acquisition system it is being used in. There are two sources of noise in an instrument amplifier, the input noise, predominantly generated by the differential input stage, and the output noise, generated by the output amplifier. Both of these components are present at the input (and output) of the instrumentation amplifier. At the input, the input noise will appear unaltered; the output noise will be attenuated by the closed loop gain (at the output, the output noise will be unaltered; the input noise will be amplified by the closed loop gain). Those two noise sources must be root sum squared to determine the total noise level expected at the input (or output).

The low frequency (0.1 to 10Hz) voltage noise due to the output stage is 10μV p-p, the contribution of the input stage is 0.2μV p-p. At a gain of 10, the RTI voltage noise would be 1μV p-p, $\sqrt{\left(\frac{10}{G}\right)^2 + (0.2)^2}$. The RTO voltage noise would be 10.2μV p-p, $\sqrt{10^2 + (0.2\ (G))^2}$. These calculations hold for applications using either internal or external gain resistors.

INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance imbalance appear as an additional offset voltage. (What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature.) Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source resistance.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground, (see Figure 31).

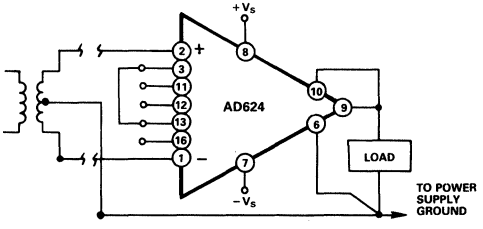


Figure 31a. Transformer Coupled

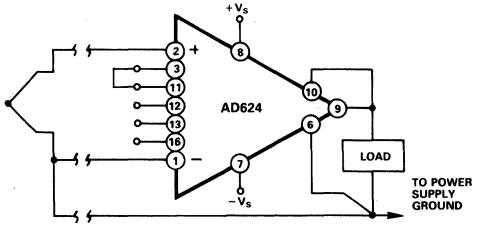


Figure 31b. Thermocouple

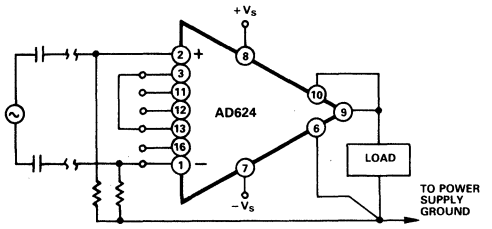


Figure 31c. AC Coupled

Figure 31. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

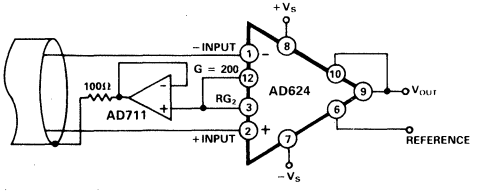


Figure 32. Shield Driver, G ≥ 100

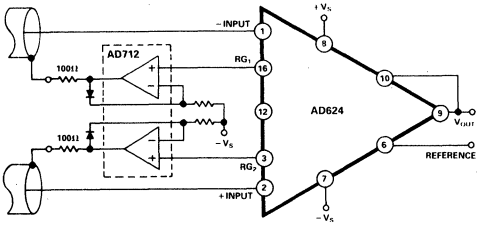


Figure 33. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to

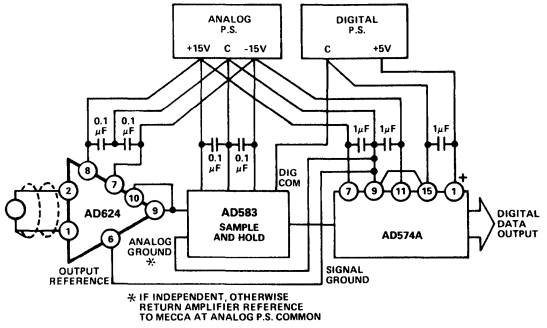


Figure 34. Basic Grounding Practice

minimize the current flow in the path from the most sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors (see Figure 34).

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

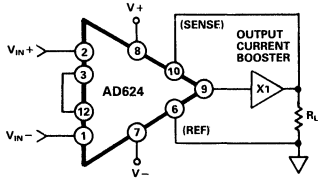


Figure 35. AD624 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 35 shows how a current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current without significantly degrading overall performance. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts, from ground, to be shared between signal and reference offset.

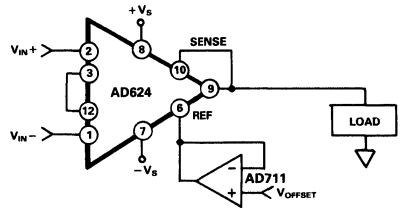


Figure 36. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance, including those caused by PC layouts or other connection techniques, which appears between the reference pin and ground will increase the gain of the noninverting signal path, thereby upsetting the common-mode rejection of the IA. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD624 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB ($10k\Omega/1\Omega = 80dB$). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 36. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 37.

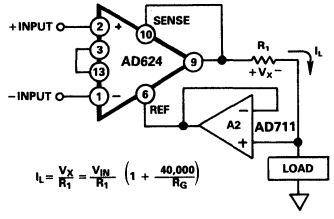


Figure 37. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 38 shows the AD624 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

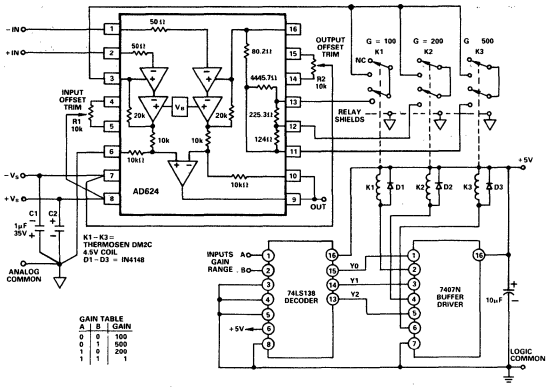


Figure 38. Gain Programmable Amplifier

A significant advantage in using the internal gain resistors in a programmable gain configuration is the minimization of thermocouple signals which are often present in multiplexed data acquisition systems.

If the full performance of the AD624 is to be achieved, the user must be extremely careful in designing and laying out his circuit to minimize the remaining thermocouple signals.

The AD624 can also be connected for gain in the output stage. Figure 39 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common-mode rejection ratio degradation.

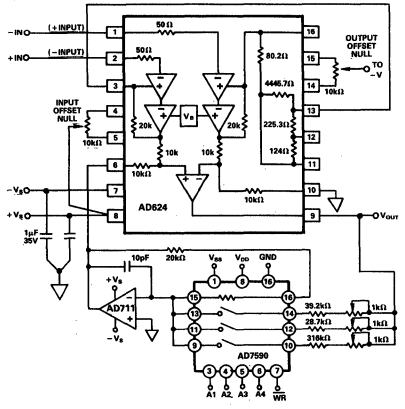


Figure 39. Programmable Output Gain

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

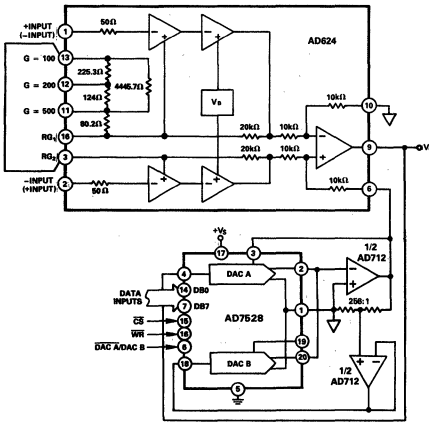


Figure 40. Programmable Output Gain Using a DAC

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 41 shows a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

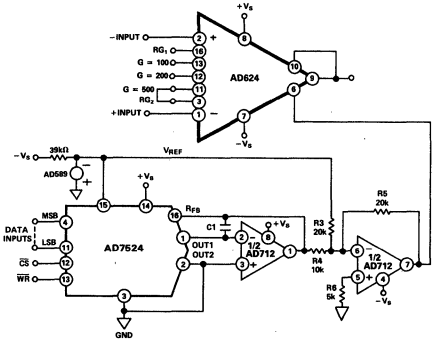


Figure 41. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For these applications Figure 42 provides a hardware solution.

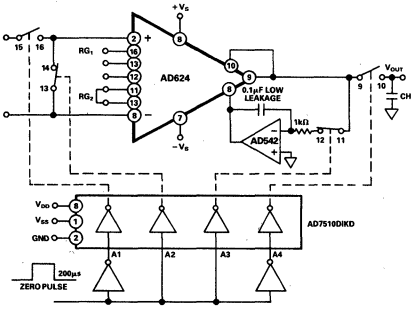


Figure 42. Auto-Zero Circuit

The microprocessor controlled data acquisition system shown in Figure 43 includes includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

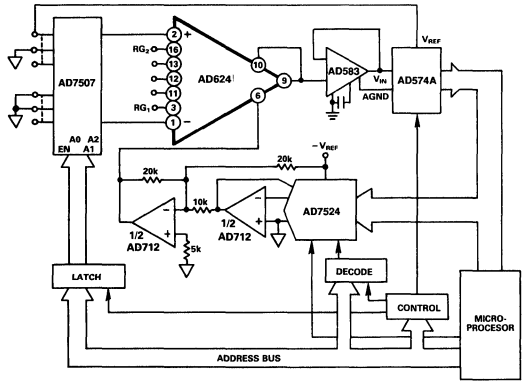


Figure 43. Microprocessor Controlled Data Acquisition System

WEIGH SCALE

Figure 44 shows an example of how an AD624 can be used to condition the differential output voltage from a load cell. The 10% reference voltage adjustment range is required to accommodate the 10% transducer sensitivity tolerance. The high linearity and low noise of the AD624 make it ideal for use in applications of this type particularly where it is desirable to measure small changes in weight as opposed to the absolute value. The addition of an auto gain/auto tare cycle will enable the system to remove offsets, gain errors, and drifts making possible true 14-bit performance.

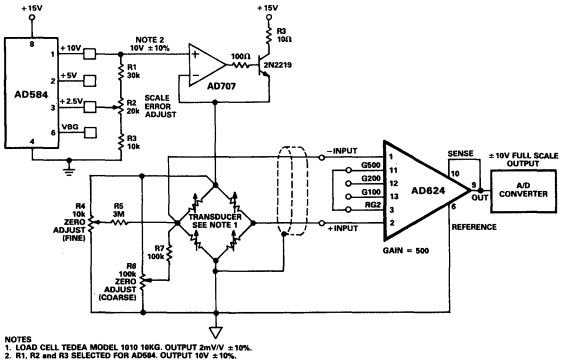


Figure 44. AD624 Weigh Scale Application

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 45 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 6.3mV change in the low pass filtered dc output, well above the RTO drifts and noise.

The AC-CMRR of the AD624 decreases with the frequency of the input signal. This is due mainly to the package-pin capacitance associated with the AD624's internal gain resistors. If AC-CMRR is not sufficient for a given application, it can be trimmed by using a variable capacitor connected to the amplifier's RG_2 pin as shown in Figure 45.

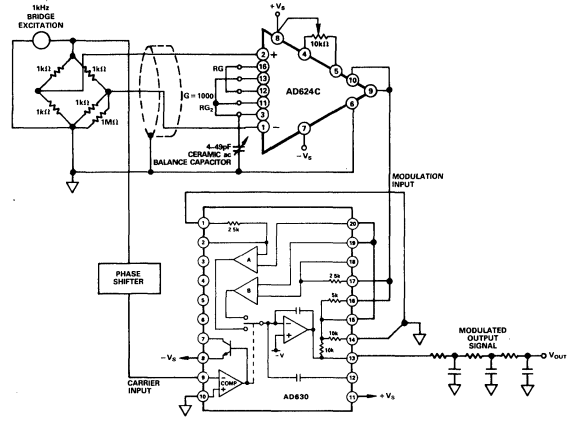


Figure 45. AC Bridge

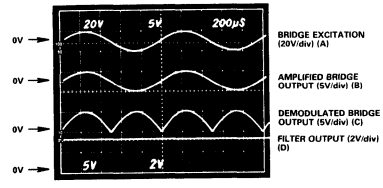


Figure 46. AC Bridge Waveforms

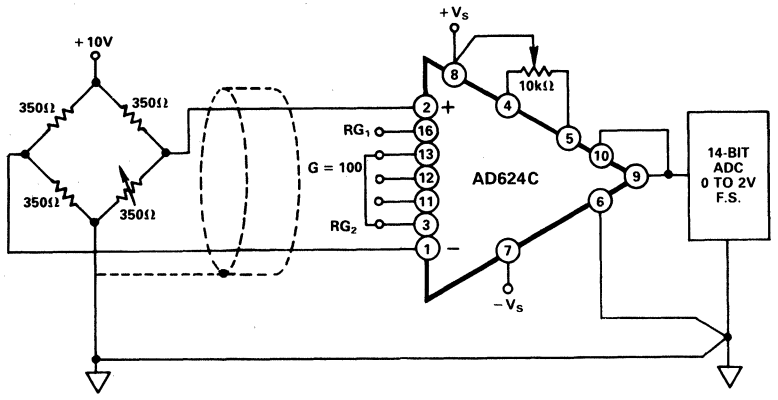


Figure 47. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD624 is required to amplify the output of an unbalanced transducer. Figure 47 shows a differential transducer, unbalanced by ≈5Ω, supplying a 0 to 20mV signal to an AD624C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (20ppm = 0.002%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.002%.

Error Source	AD624C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.1%	±0.1% = 1000ppm	1000ppm	1000ppm	–
Gain Instability	10ppm	(10ppm/°C)(60°C) = 600ppm	–	600ppm	–
Gain Nonlinearity	±0.001%	±0.001% = 10ppm	–	–	10ppm
Input Offset Voltage	±25μV, RTI	±25μV/20mV = ±1250ppm	1250ppm	1250ppm	–
Input Offset Voltage Drift	±0.25μV/°C	(±0.25μV/°C)(60°C) = 15μV 15μV/20mV = 750ppm	–	750ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±10μV/°C	(±10μV/°C)(60°C) = 600μV 600μV/20mV = 300ppm	–	300ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(5Ω) = 0.075μV 0.075μV/20mV = 3.75ppm	3.75ppm	3.75ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(5Ω) = 0.050μV 0.050μV/20mV = 2.5ppm	2.5ppm	2.5ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 1.75μV 1.75μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 9μV 9μV/20mV = 444ppm	450ppm	450ppm	–
Noise, RTI (0.1–10Hz)	0.22μV p-p	0.22μV p-p/20mV = 10ppm	–	–	10ppm
		Total Error	3793.75ppm	5493.75ppm	20ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

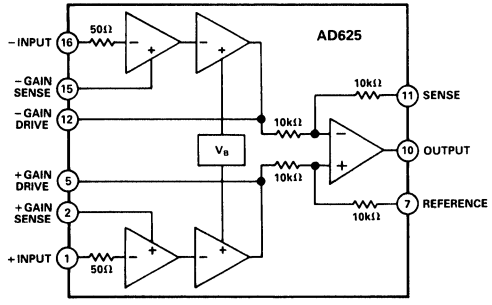
Table II. Error Budget Analysis of AD624CD in Bridge Application

Programmable Gain Instrumentation Amplifier

AD625

FEATURES
User Programmed Gains of 1 to 10,000
Low Gain Error: 0.02% max
Low Gain TC: 5ppm/°C max
Low Nonlinearity: 0.001% max
Low Offset Voltage: 25μV
Low Noise 4nV/√Hz (at 1kHz) RTI
Gain Bandwidth Product: 25MHz
16-Pin Ceramic or Plastic DIP Package
MIL-Standard Parts Available
Low Cost

AD625 FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD625 is a precision instrumentation amplifier specifically designed to fulfill two major areas of application:
1) Circuits requiring nonstandard gains (i.e., gains not easily achievable with devices such as the AD524 and AD624).
2) Circuits requiring a low cost, precision software programmable gain amplifier.

For low noise, high CMRR, and low drift the AD625JN is the most cost effective instrumentation amplifier solution available. An additional three resistors allow the user to set any gain from 1 to 10,000. The error contribution of the AD625JN is less than 0.05% gain error and under 5ppm/°C gain TC; performance limitations are primarily determined by the external resistors. Common-mode rejection is independent of the feedback resistor matching.

A software programmable gain amplifier (SPGA) can be configured with the addition of a CMOS multiplexer (or other switch network), and a suitable resistor network. Because the ON resistance of the switches is removed from the signal path, an AD625 based SPGA will deliver 12-bit precision, and can be programmed for any set of gains between 1 and 10,000, with completely user selected gain steps.

For the highest precision the AD625C offers an input offset voltage drift of less than 0.25μV/°C, output offset drift below 15μV/°C, and a maximum nonlinearity of 0.001% at G = 1. All grades exhibit excellent ac performance; a 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time.

The AD625 is available in three accuracy grades (A, B, C) for industrial (−25°C to +85°C) temperature range, two grades (J, K) for commercial (0 to +70°C) temperature range, and one (S) grade rated over the extended (−55°C to +125°C) temperature range.

PRODUCT HIGHLIGHTS

1. The AD625 affords up to 16-bit precision for user selected fixed gains from 1 to 10,000. Any gain in this range can be programmed by 3 external resistors.
2. A 12-bit software programmable gain amplifier can be configured using the AD625, a CMOS multiplexer and a resistor network. Unlike previous instrumentation amplifier designs, the ON resistance of a CMOS switch does not affect the gain accuracy.
3. The gain accuracy and gain temperature coefficient of the amplifier circuit are primarily dependent on the user selected external resistors.
4. The AD625 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effects of offset voltage in gain-ranging applications.
5. The proprietary design of the AD625 provides input voltage noise of 4nV/√Hz at 1kHz.
6. External resistor matching is not required to maintain high common-mode rejection.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
GAIN										
Gain Equation		$\frac{2\,R_F}{R_G}+1$			$\frac{2\,R_F}{R_G}+1$			$\frac{2\,R_F}{R_G}+1$		
Gain Range	1		10,000	1		10,000	1		10,000	
Gain Error[1]		±.035	**±0.05**		±0.02	**±0.03**		±0.01	**±0.02**	%
Nonlinearity, Gain = 1-256			±0.005			±0.002			±0.001	%
Gain>256			±0.01			±0.008			±0.005	%
Gain vs. Temp. Gain<1000[1]			5			5			5	ppm/°C
GAIN SENSE INPUT										
Gain Sense Current		300	**500**		150	**250**		50	**100**	nA
vs. Temperature		5	20		2	15		2	10	nA/°C
Gain Sense Offset Current		150	**500**		75	**250**		50	**100**	nA
vs. Temperature		2	15		1	10		1	5	nA/°C
VOLTAGE OFFSET (May be Nulled)										
Input Offset Voltage		50	**200**		25	**50**		10	**25**	µV
vs. Temperature		1	**2/2**		0.25	**0.50/1**		0.1	**0.25**	µV/°C
Output Offset Voltage		4	**5**		2	**3**		1	**2**	mV
vs. Temperature		20	**50/50**		10	**25/40**		10	**15**	µV/°C
Offset Referred to the Input vs. Supply										
G = 1	**70**	75		75	85		**80**	90		dB
G = 10	85	95		90	100		95	105		dB
G = 100	95	100		105	110		110	120		dB
G = 1000	**100**	110		**110**	120		**115**	140		dB
INPUT CURRENT										
Input Bias Current		±30	**±50**		±20	**±25**		±10	**±15**	nA
vs. Temperature		±50			±50			±50		pA/°C
Input Offset Current		±2	**±35**		±1	**±15**		±1	**±5**	nA
vs. Temperature		±20			±20			±20		pA/°C
INPUT										
Input Impedance										
Differential Resistance		1			1			1		GΩ
Differential Capacitance		4			4			4		pF
Common-Mode Resistance		1			1			1		GΩ
Common-Mode Capacitance		4			4			4		pF
Input Voltage Range										
Differ. Input Linear (V_{DL})[2]			±10			±10			±10	V
Common-Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		
Common-Mode Rejection Ratio dc to 60Hz with 1kΩ Source Imbalance										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	90	95		95	105		100	115		dB
G = 100	100	105		105	115		110	125		dB
G = 1000	**110**	115		**115**	125		**120**	140		dB
OUTPUT RATING		±10V @5mA			±10V @5mA			±10V @5mA		
DYNAMIC RESPONSE										
Small Signal – 3dB										
G = 1 (R_F = 20kΩ)		650			650			650		kHz
G = 10		400			400			400		kHz
G = 100		150			150			150		kHz
G = 1000		25			25			25		kHz
Slew Rate		5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step										
G = 1 to 200		15			15			15		µs
G = 500		35			35			35		µs
G = 1000		75			75			75		µs
NOISE										
Voltage Noise, 1kHz										
R.T.I.		4			4			4		$nV/\sqrt{Hz}$
R.T.O.		75			75			75		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz										
G = 1		10			10			10		µV p-p
G = 10		1.0			1.0			1.0		µV p-p
G = 100		0.3			0.3			0.3		µV p-p
G = 1000		0.2			0.2			0.2		µV p-p
Current Noise										
0.1Hz to 10Hz		60			60			60		pA p-p

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
SENSE INPUT										
R_{IN}		10			10			10		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±10			V
Gain to Output		1 ± 0.01			1 ± 0.01			1 ± 0.01		%
REFERENCE INPUT										
R_{IN}		20			20			20		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±10			V
Gain to Output		1 ± 0.01			1 ± 0.01			1 ± 0.01		%
TEMPERATURE RANGE										
Specified Performance										
J/K Grades	0		+70	0		+70				°C
A/B/C Grades	−25		+85	−25		+85	−25		+85	°C
S Grade	−55		+125							
Storage	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY										
Power Supply Range		±6 to ±18			±6 to ±18			±6 to ±18		V
Quiescent Current		3.5	5		3.5	5		3.5	5	mA
PACKAGE OPTIONS[3]										
Ceramic (D-16)		AD625AD/SD			AD625BD			AD625CD		
Plastic DIP (N-16)		AD625JN			AD625KN					
Leadless Chip Carrier (E-20A)		AD625AE								

NOTES
[1]Gain Error and Gain TC are for the AD625 only. Resistor network errors will add to the specified errors.
[2]V_{DL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DL} at other gains = 10V/G.
V_D = actual differential input voltage.
Example: G = 10, V_D = 0.50
V_{CM} = 12V–(10/2 × 0.50V) = 9.5V.
[3]See Section 20 for package outline information.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

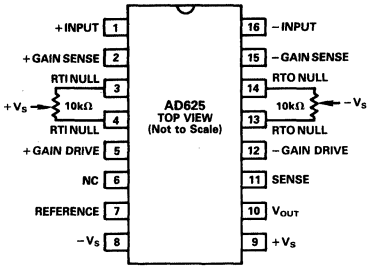
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation 450mW
Input Voltage . . . . . ±V_S
Differential Input Voltage[2] . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range D . . . . . −65°C to +150°C
Storage Temperature Range N . . . . . −65°C to +125°C
Operating Temperature Range
AD625J/K . . . . . 0 to +70°C
AD625A/B/C . . . . . −25°C to +85°C
AD625S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering, 60 seconds) . . . . . +300°C

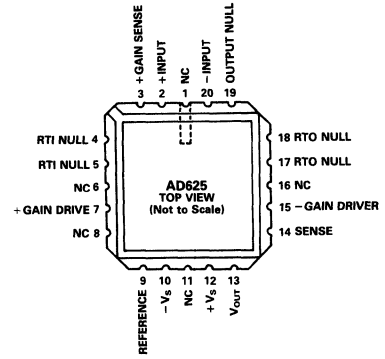
NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

Ceramic and Plastic DIP (D and N) Packages



Leadless Chip Carrier (E) Package



Typical Characteristics

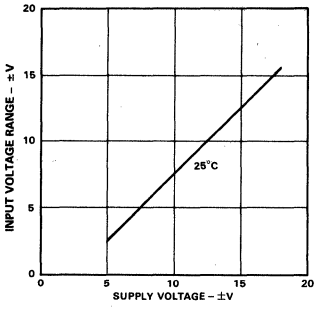


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

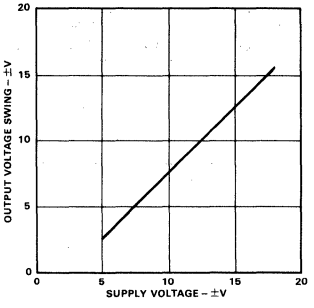


Figure 2. Output Voltage Swing vs. Supply Voltage

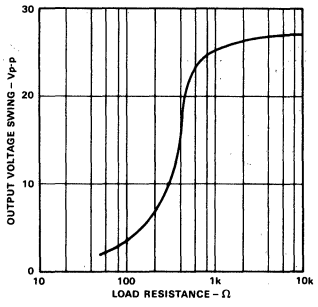


Figure 3. Output Voltage Swing vs. Load Resistance

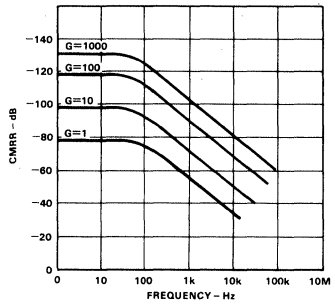


Figure 4. CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

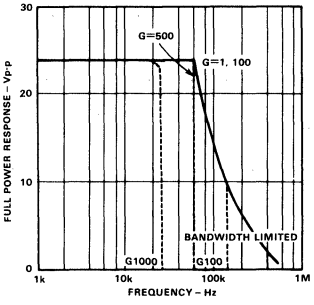


Figure 5. Large Signal Frequency Response

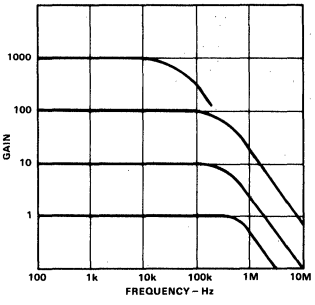


Figure 6. Gain vs. Frequency

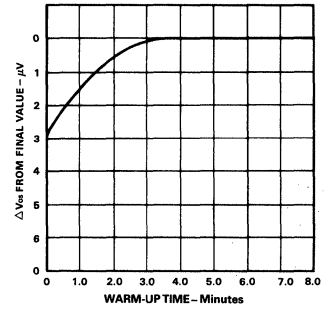


Figure 7. Offset Voltage, RTI, Turn On Drift

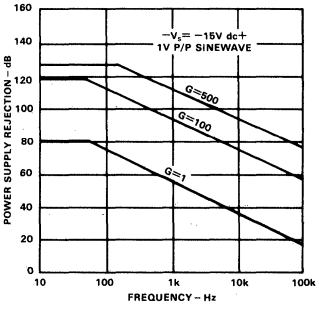


Figure 8. Negative PSRR vs. Frequency

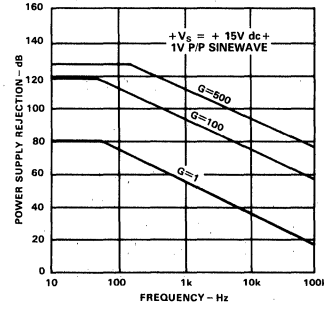


Figure 9. Positive PSRR vs. Frequency

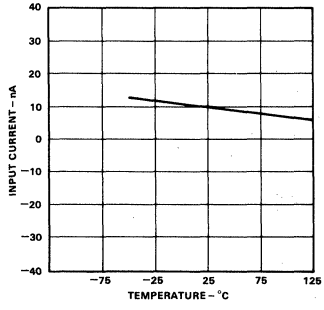


Figure 10. Input Bias Current vs. Temperature

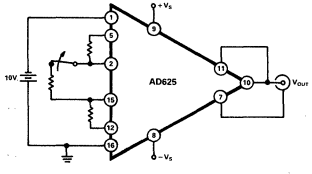


Figure 11. Overange and Gain Switching Test Circuit (G=8, G=1)

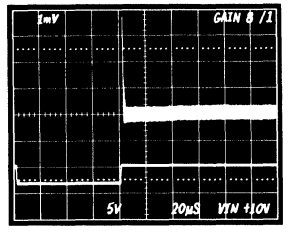


Figure 12. Gain Overange Recovery

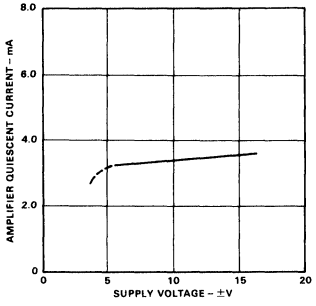


Figure 13. Quiescent Current vs. Supply Voltage

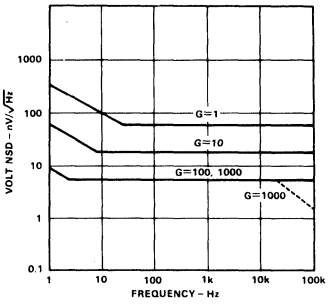


Figure 14. RTI Noise Spectral Density vs. Gain

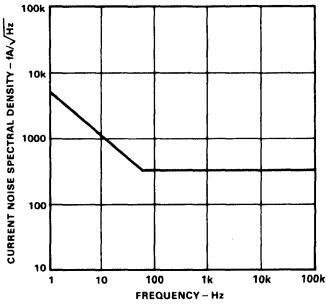


Figure 15. Input Current Noise

4

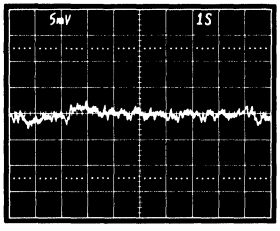


Figure 16. Low Frequency Voltage Noise, G=1 (System Gain=1000)

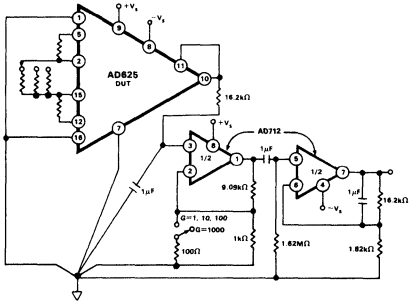


Figure 17. Noise Test Circuit

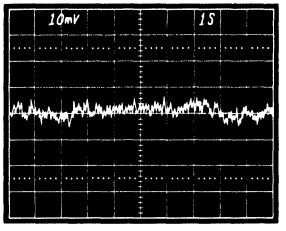


Figure 18. Low Frequency Voltage Noise, G=1000 (System Gain=100,000)

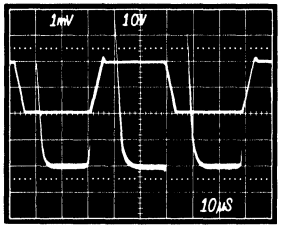


Figure 19. Large Signal Pulse Response and Settling Time, G=1

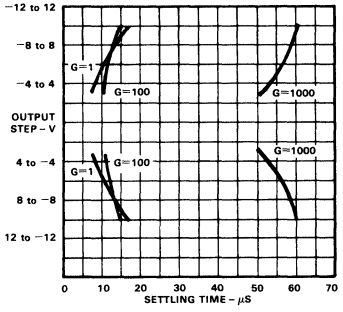


Figure 20. Settling Time to 0.01%

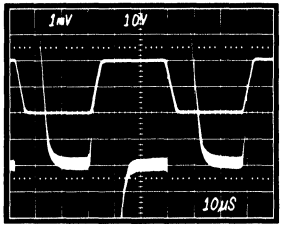


Figure 21. Large Signal Pulse Response and Settling Time, G = 100

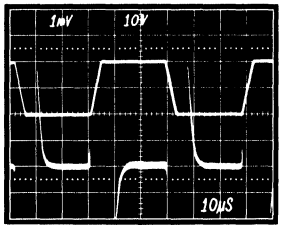


Figure 22. Large Signal Pulse Response and Settling Time, G = 10

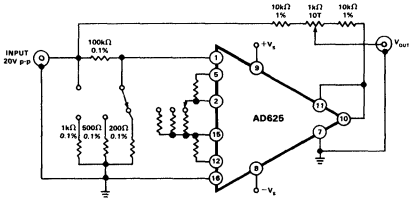


Figure 23. Settling Time Test Circuit

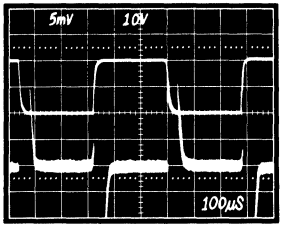


Figure 24. Large Signal Pulse Response and Settling Time, G=1000

Theory of Operation

The AD625 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp section (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G$ + 1) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

The value of R_G is the determining factor of the transconductance of the input preamp stage. As R_G is reduced for larger gains the transconductance increases. This has three important advantages. First, this approach allows the circuit to achieve a very high open-loop gain of (3×10^8 at programmed gains $\geq$ 500) thus reducing gain related errors. Second, the gain-bandwidth product, which is determined by C3, C4, and the input transconductance, increases with gain, thereby, optimizing frequency response. Third, the input voltage noise is reduced to a value determined by the collector current of the input transistors ($4nV/\sqrt{Hz}$).

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the AD625; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is (R_G + 100)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 40Ω), the maximum overload voltage the AD625 can withstand, continuously, is approximately ±2.5V. Figure 26A shows the external components necessary to protect the AD625 under all overload conditions at any gain.

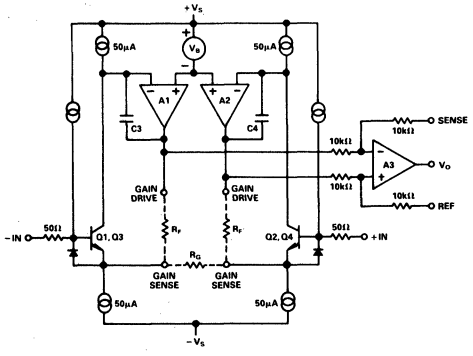


Figure 25. Simplified Circuit of the AD625

The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered. In higher gain applications where differential voltages are small, back-to-back zener diodes and smaller resistors, as shown in Figure 26b, provides adequate protection. Figure 26c shows low cost FETs with a maximum ON resistance of 300Ω configured to offer input protection with minimal degradation to noise, ($5.2nV/\sqrt{Hz}$ compared to normal noise performance of $4nV/\sqrt{Hz}$).

During differential overload conditions, excess current will flow through the gain sense lines (pins 2 and 15). This will have no effect in fixed gain applications. However, if the AD625 is being used in an SPGA application with a CMOS multiplexer, this current should be taken into consideration. The current capabilities of the multiplexer may be the limiting factor in allowable overflow current. The ON resistance of the switch should be included as part of R_G when calculating the necessary input protection resistance.

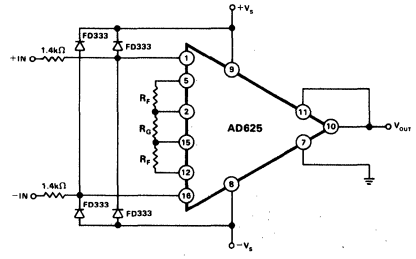


Figure 26a. Input Protection Circuit

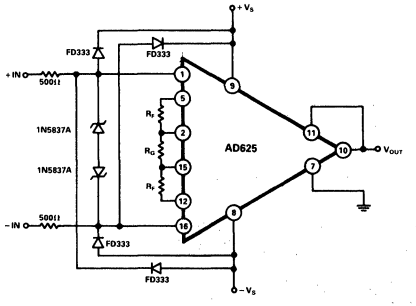


Figure 26b. Input Protection Circuit for G>5

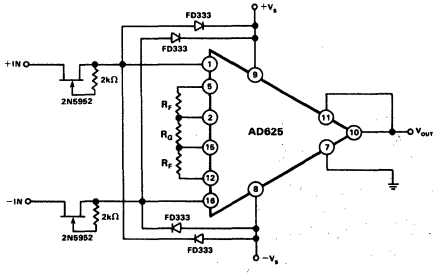


Figure 26c. Input Protection Circuit

Any resistors in series with the inputs of the AD625 will degrade the noise performance. For this reason the circuit in Figure 26b should be used if the gains are all greater than 5. For gains less than 5, either the circuit in Figure 26a or in Figure 26c can be used. The two 1.4kΩ resistors in Figure 26a will degrade the noise performance to:

$$\sqrt{4kTR_{ext} + (4nV/\sqrt{Hz})^2} = 7.9nV/\sqrt{Hz}$$

RESISTOR PROGRAMMABLE GAIN AMPLIFIER

In the resistor-programmed mode (Figure 27), only three external resistors are needed to select any gain from 1 to 10,000. Depending on the application, discrete components or a pretrimmed network can be used. The gain accuracy and gain TC are primarily determined by the external resistors since the AD625C contributes less than 0.02% to gain error and under 5ppm/°C gain TC. The gain sense current is insensitive to common-mode voltage, making the CMRR of the resistor programmed AD625 independent of the match of the two feedback resistors, R_F.

Selecting Resistor Values

As previously stated each R_F provides feedback to the input stage and sets the unity gain transconductance. These feedback resistors are provided by the user. The AD625 is tested and specified with a value of 20kΩ for R_F. Since the magnitude of RTO errors increases with increasing feedback resistance, values much above 20kΩ are not recommended (values below 10kΩ for R_F may lead to instability). Refer to the graph of RTO noise, offset, drift, and bandwidth (Figure 28) when selecting the feedback resistors. The gain resistor (R_G) is determined by the formula $R_G = 2R_F/(G-1)$.

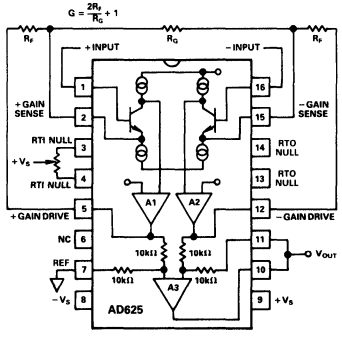


Figure 27. AD625 in Fixed Gain Configuration

A list of standard resistors which can be used to set some common gains is shown in Table I.

For single gain applications, only one offset null adjust is necessary; in these cases the RTI null should be used.

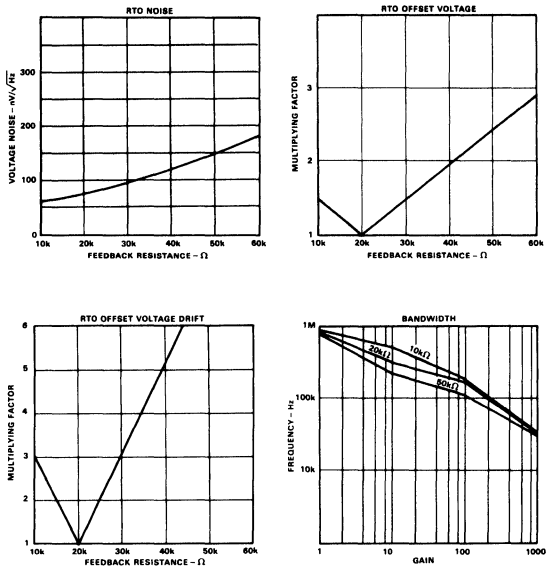


Figure 28. RTO Noise, Offset, Drift, and Bandwidth vs. Feedback Resistance Normalized to 20kΩ

GAIN	R_F	R_G
1	20kΩ	∞
2	19.6kΩ	39.2kΩ
5	20kΩ	10kΩ
10	20kΩ	4.42kΩ
20	20kΩ	2.1kΩ
50	19.6kΩ	806Ω
100	20kΩ	402Ω
200	20.5kΩ	205Ω
500	19.6kΩ	78.7Ω
1000	19.6kΩ	39.2Ω
4	20kΩ	13.3kΩ
8	19.6kΩ	5.62kΩ
16	20kΩ	2.67kΩ
32	19.6kΩ	1.27kΩ
64	20kΩ	634Ω
128	20kΩ	316Ω
256	19.6kΩ	154Ω
512	19.6kΩ	76.8Ω
1024	19.6kΩ	38.3Ω

Table I. Common Gains Nominally within ±0.5% Error Using Standard 1% Resistors

SENSE TERMINAL

The sense terminal is the feedback point for the AD625 output amplifier. Normally it is connected directly to the output. If heavy load currents are to be drawn through long leads, voltage drops through lead resistance can cause errors. In these instances the sense terminal can be wired to the load thus putting the I × R drops "inside the loop" and virtually eliminating this error source.

Typically, IC instrumentation amplifiers are rated for a full ± 10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 29 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier. By using an external power boosting circuit, the power dissipated by the AD625 will remain low, thereby, minimizing the errors induced by self-heating. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the AD625's output amplifier.

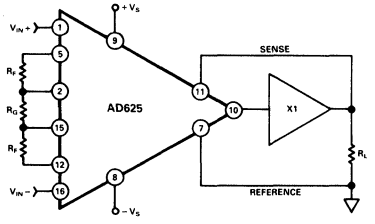


Figure 29. AD625 Instrumentation Amplifier with Output Current Booster

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ± 10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. However, it must be remembered that the total output swing is ± 10 volts, from ground, to be shared between signal and reference offset.

The AD625 reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 30. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

The circuit of Figure 30 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$, however, to be symmetrical about 0V $R_3 = 2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 30 is ± 120mV, and the offset is incremented in steps of 0.9375mV/LSB.

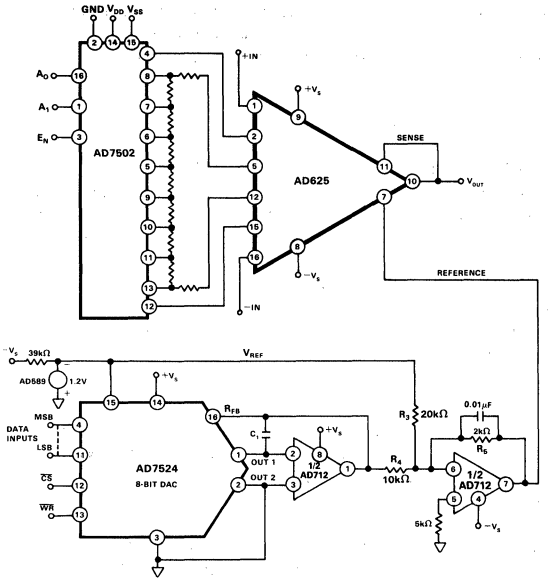


Figure 30. Software Controllable Offset

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 31.

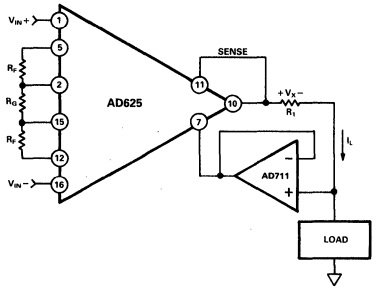


Figure 31. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A1, the forced current I_L will largely flow through the load. Offset and drift specifications of A2 must be added to the output offset and drift specifications of the In-Amp.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains.

The input offset and drift are multiplied by the gain, while the output terms are independent of gain, therefore, input errors dominate at high gains and output errors dominate at low gains. The output offset voltage (and drift) is normally specified at G = 1 (where input effects are insignificant), while input offset (and drift) is given at a high gain (where output effects are negligible). All input-related parameters are specified referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Offset voltage vs. power supply is also specified as an RTI error.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain ×input error) + output error

The AD625 provides for both input and output offset voltage adjustment. This simplifies nulling in very high perecision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9μV/°C, RTO.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create

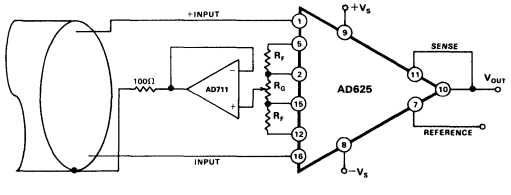


Figure 32. Common-Mode Shield Driver

common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 show active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

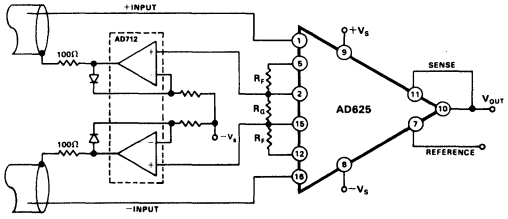


Figure 33. Differential Shield Driver

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 34). Since the AD625 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

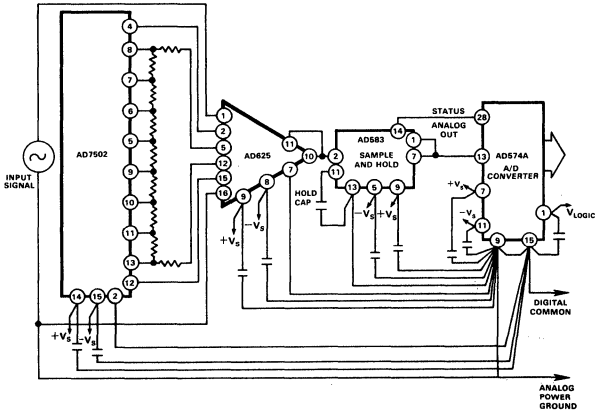


Figure 34. Basic Grounding Practice for a Data Acquisition System

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 35.

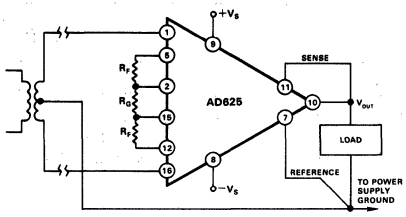


Figure 35a. Ground Returns for Bias Currents with Transformer Coupled Inputs

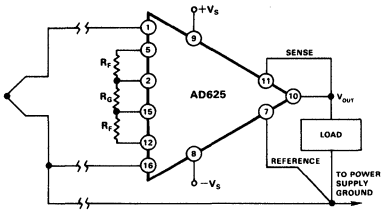


Figure 35b. Ground Returns for Bias Currents with Thermocouple Input

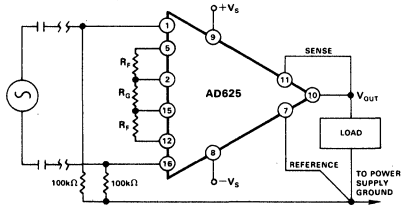


Figure 35c. Ground Returns for Bias Currents with AC Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 36 provides a hardware solution.

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD625) remain isothermal. This includes the input leads (1, 16) and the gain sense lines (2, 15). These pins were chosen for symmetry, helping to desensitize the input circuit to thermal gradients. In addition, the user should also avoid air currents

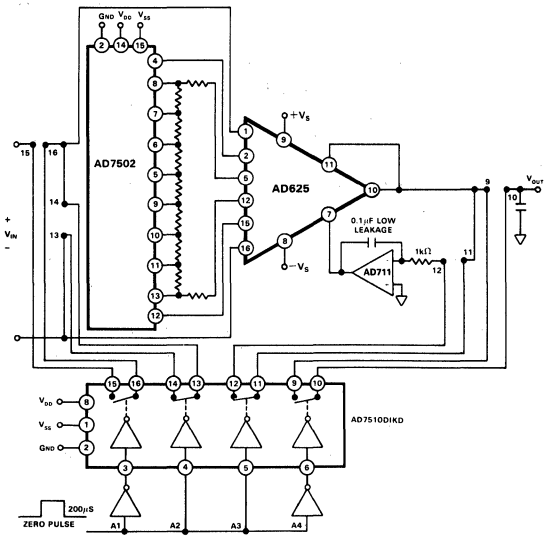


Figure 36. Auto-Zero Circuit

over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise. In SPGA applications relay contacts and CMOS mux leads are both potential sources of additional thermocouple errors.

The base emitter junction of an input transistor can rectify out of band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. The AD625 allows direct access to the input transistors' bases and emitters enabling the user to apply some first order filtering to these unwanted signals. In Figure 37, the RC time constant should be chosen for desired attenuation of the interfering signals. In the case of a resistive transducer, the capacitance alone working against the internal resistance of the transducer may suffice.

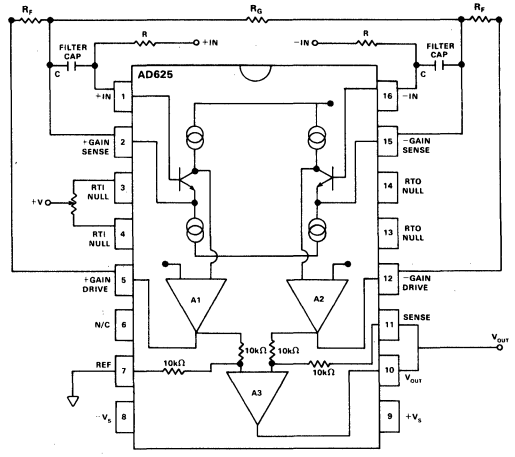


Figure 37. Circuit to Attenuate RF Interference

These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 15 and 2, and pins 1 and 16, to preserve high ac CMR.

SOFTWARE PROGRAMMABLE GAIN AMPLIFIER

An SPGA provides the ability to externally program precision gains from digital inputs. Historically, the problem in systems requiring electronic switching of gains has been the ON resistance (R_{ON}) of the multiplexer, which appears in series with the gain setting resistor R_G. This can result in substantial gain errors and gain drifts. The AD625 eliminates this problem by making the gain drive and gain sense pins available (pins 2, 15, 5, 12; see Figure 39). Consequently the multiplexer's ON resistance is removed from the signal current path. This transforms the ON resistance error into a small nullable offset error. To clarify this point, an error budget analysis has been performed in Table II based on the SPGA configuration shown in Figure 39.

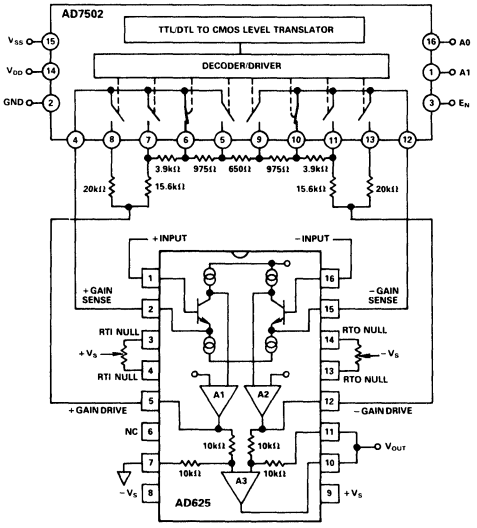


Figure 38. SPGA in a Gain of 16

Figure 38 shows an AD625 based SPGA with possible gains of 1, 4, 16, 64. R_G equals the resistance between the gain sense lines (pins 2 and 15) of the AD625. In Figure 38, R_G equals the sum of the two 975Ω resistors and the 650Ω resistor, or 2600Ω. R_F equals the resistance between the gain sense and the gain drive pins (pins 12 and 15, or pins 2 and 5), that is R_F equals the 15.6kΩ resistor plus the 3.9kΩ resistor, or 19.5kΩ. The gain, therefore equals:

$$\frac{2R_F}{R_G} + 1 = \frac{2(19.5k\Omega)}{(2.6k\Omega)} + 1 = 16$$

As the switches of the differential multiplexer proceed synchronously, R_G and R_F change, resulting in the various programmed gain settings.

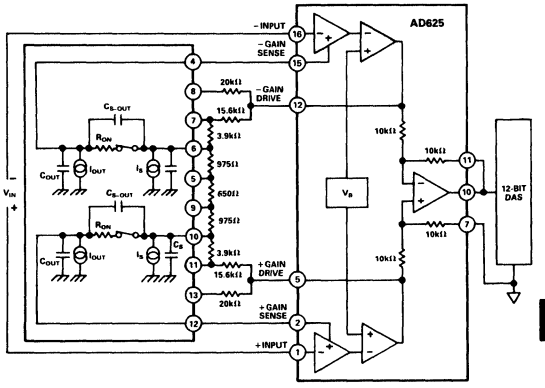


Figure 39. SPGA with Multiplexer Error Sources

Figure 39 shows a complete SPGA feeding a 12-bit DAS with a 0–10V input range. This configuration was used in the error budget analysis shown in Table II. The gain used for the RTI calculations is set at 16. As the gain is changed, the ON resistance of the multiplexer and the feedback resistance will change, which will slightly alter the values in the table.

Induced Error	Specification AD625C	Specification AD7502KN	Calculation	Voltage Offset Induced RTI
RTI Offset Voltage	Gain Sense Offset Current 40nA	Switch Resistance 170Ω	40nA × 170Ω = 6.8μV	6.8μV
RTI Offset Voltage	Gain Sense Current 60nA	Differential Switch Resistance 6.8Ω	60nA × 6.8Ω = 0.41μV	0.41μV
RTO Offset Voltage	Feedback Resistance 20kΩ[1]	Differential Leakage Current (I_S)[2] +0.2nA −0.2nA	2(0.2nA × 20kΩ) = 8μV/16	0.5μV
RTO Offset Voltage	Feedback Resistance 20kΩ[1]	Differential Leakage Current (I_{OUT})[2] +1nA −1nA	2(1nA × 20kΩ) = 40μV/16	2.5μV
Total error induced by a typical CMOS multiplexer to an SPGA at 25°C				**10.21μV**

NOTES

[1]The resistor for this calculation is the user provided feedback resistance (R_F). 20kΩ is recommended value (see resistor programmable gain amplifier section).

[2]The leakage currents (I_S and I_{OUT}) will induce an offset voltage, however, the offset will be determined by the difference between the leakages of each "half" of the differential multiplexer. The differential leakage current is multiplied by the feedback resistance (see Note 1),to determine offset voltage. Because differential leakage curent is not a parameter specified on multiplexer data sheets, the most extreme difference (one most positive and one most negative) was used for the calculations in Table II. Typical performance will be much better.

*The frequency response and settling will be affected by the ON resistance and internal capacitance of the multiplexer. Figure 40 shows the settling time vs. ON resistance at different gain settings for an AD625 based SPGA.

**Switch resistance and leakage current errors can be reduced by using relays.

Table II. Errors Induced by Multiplexer to an SPGA

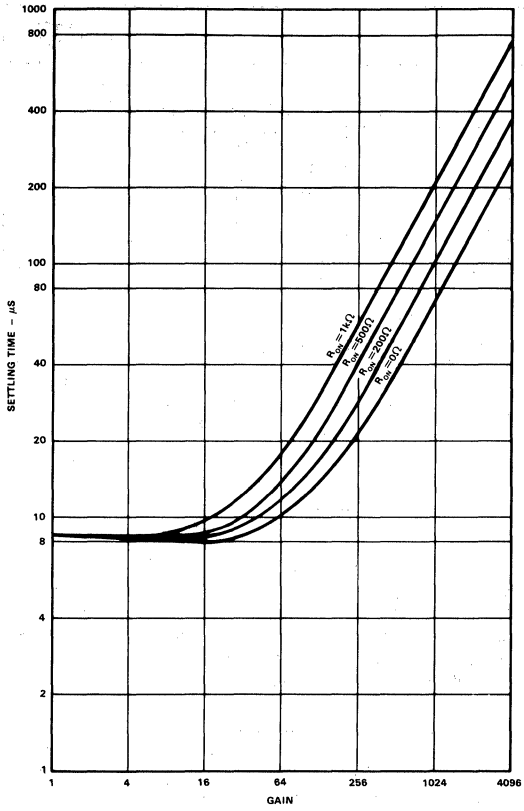


Figure 40. Settling Time to 0.01% of a 20V Step Input for SPGA with AD625

DETERMINING SPGA RESISTOR NETWORK VALUES

The individual resistors in the gain network can be calculated sequentially using the formula given below. The equation determines the resistors as labeled in Figure 41. The feedback resistors and the gain setting resistors are interactive, therefore; the formula must be a series where the present term is dependent on the preceding term(s). The formula

$$R_{F_{i+1}} = (20k\Omega - \sum_{j=0}^{i} R_{F_j})\left(1 - \frac{G_i}{G_{i+1}}\right) \qquad \begin{matrix} G_0 = 1 \\ R_{F_0} = 0 \end{matrix}$$

can be used to calculate the necessary feedback resistors for any set of gains. This formula yields a network with a total resistance of 40kΩ. A dummy variable (j) serves as a counter to keep a running total of the preceding feedback resistors. To illustrate how the formula can be applied, an example similar to the calculation used for the resistor network in Figure 38 is examined below.

1) Unity gain is treated as a separate case. It is implemented with separate 20kΩ feedback resistors as shown in Figure 41. It is then ignored in further calculations.

2) Before making any calculations it is advised to draw a resistor network similar to the network in Figure 41. The network will have (2 × M) + 1 resistors, where M = number of gains. For Figure 38 M = 3 (4, 16, 64), therefore, the resistor string will have 7 resistors (plus the two 20kΩ "side" resistors for unity gain).

3) Begin all calculations with $G_0 = 1$ and $R_{F_0} = 0$.

$R_{F_1} = (20k\Omega - R_{F_0})\ (1 - 1/4)$: $R_{F_0} = 0 \therefore R_{F_1} = 15k\Omega$

$R_{F_2} = [20k\Omega - (R_{F_0} + R_{F_1})]\ (1 - 4/16)$:

$R_{F_0} + R_{F_1} = 15k\Omega \therefore R_{F_2} = 3.75k\Omega$

$R_{F_3} = [20k\Omega - (R_{F_0} + R_{F_1} + R_{F_2})]\ (1 - 16/64)$:

$R_{F_0} + R_{F_1} + R_{F_2} = 18.75k\Omega \therefore R_{F_3} = 937.5\Omega$

4) The center resistor (R_G of the highest gain setting), is determined last. Its value is the remaining resistance of the 40kΩ string, and can be calculated with the equation:

$$R_G = (40k\Omega - 2\sum_{j=0}^{M} R_{F_j})$$

$$R_G = 40k\Omega - 2(R_{F_0} + R_{F_1} + R_{F_2} + R_{F_3})$$

$$40k\Omega - 39.375k\Omega = 625\Omega$$

5) If different resistor values are desired, all the resistors in the network can be scaled by some convenient factor. However, raising the impedance will increase the RTO errors, lowering the total network resistance below 20kΩ can result in amplifier instability. More information on this phenomenon is given in the RPGA section of the data sheet. The scale factor will not affect the unity gain feedback resistors. The resistor network in Figure 38 has a scaling factor of 650/625 = 1.04, if this factor is used on R_{F_1}, R_{F_2}, R_{F_3}, and R_G, then the resistor values will match exactly.

6) Round off errors can be cumulative, therefore, it is advised to carry as many significant digits as possible until all the values have been calculated.

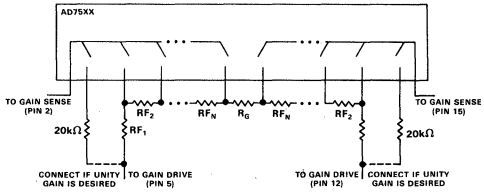


Figure 41. Resistors for a Gain Setting Network

Isolation Amplifiers
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Selection Guide
Isolation Amplifiers

Model	Peak Volt Iso V pk	Gain Range V/V	Gain Nonlin % max	Freq Resp kHz	Package Options[1]	Temp Range[2]	Page	Comments
284J	2500	1–10	0.05	1	Module	C	5–67	Medical, Single Channel, Low Cost
286J	2500	1–100	0.05-0.2	1	Module	C	5–73	Medical, Multichannel, Low Cost
289	2500	1–100	0.012–0.05	20	Module	C	5–79	Precision, Wide Bandwidth, Synchronized
290A	1500	1–100	0.1–0.25	2.5	Module	I	5–85	Single Channel, General Purpose
292A	1500	1–100	0.1–0.25	2.5	Module	I	5–85	Multichannel, General Purpose
AD202	**1000–2000**	**1–100**	**0.025–0.05**	**2**	**N, Y**	**C**	**5–5**	**Lowest Cost, Small Size, Single Channel, −40°C to +85°C**
AD203	**2000**	**1–100**	**0.025**	**10**	**N**	**M**	**5–17**	**Rugged, Military Temperature Range, Wide Bandwidth**
AD204	**1000–2000**	**1–100**	**0.025-0.05**	**5**	**N, Y**	**C**	**5–5**	**Lowest Cost, Small Size, Multichannel, −40°C to +85°C**
AD206	**2000**	**1–10**	**0.015–0.03**	**100 kHz**	**Y**	**I**	**5–29**	**100 kHz Bandwidth, Low Distortion Isolation Amplifier**
AD208	**1000–2000**	**1–1000**	**0.015–0.03**	**0.4–4 kHz**	**Y**	**I**	**5–39**	**Precision, Low Cost, Single Channel, mV Input**
AD210	**3500**	**1–100**	**0.012–0.025**	**20**	**N**	**I, C**	**5–53**	**Precision, 3-Port Isolation, Wide Bandwidth**
AD295	**2500**	**1–1000**	**0.012–0.05**	**4.5**	**Module**	**I**	**5–61**	**−40°C to +100°C, Low Drift, 3-Port Isolation**
281					Module	C	5–73	External Oscillator for 286J and 292A Isolation Amplifiers
AD246					N, Y	C	5–10	External Oscillator for AD204 Isolation Amplifier

[1]Package Options: N–Plastic Molded Dual-In-Line; Y–Single In-Line Package.
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
Isolation Amplifiers

The *isolation amplifier* (or isolator) has an input circuit that is galvanically isolated from the power supply and the output circuit. In the basic *two-port* form, the output and power circuits are not isolated from one another; in *three-port* isolators (see the figure), the input circuits, output circuits, and power source are all isolated from one another. In some 3-port isolators, the power for the output stage must be furnished from the signal's destination; however, in the device shown in Figure 1, all internal power is furnished by its own power source; in addition, a modicum of auxiliary power is available to power external input *and output* circuitry.

Isolators are intended for applications requiring safe, accurate measurement of voltage or current signals in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment and industrial process-control systems.

Analog Devices Isolators described in this section (and in the *Signal Conditioner* section) use transformer coupled high-frequency carrier techniques for the transmission of power to and signals from the input (and in some cases the *output*) circuit.

CHOOSING AN ISOLATOR

The choice of isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels in the system, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning) and the availability of isolated power for additional external front-end (or back-end) circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, an applications guide,[1] available upon request, provides information useful to the circuit designer.

The devices described in this section are all voltage-output isolation amplifiers, useful in general-purpose circuit applications for instrumentation amplifiers or op amps where isolation is a necessity. In addition to these devices, there are a growing number of isolators available from Analog Devices that perform dedicated functions, for use where isolation is necessary or desirable. Some of their applications can be seen in the Signal Conditioner section of this book and the *Transducer Interfacing Handbook*[2]. Power Supplies and DC-DC Converters, usually transformer-coupled, also provide isolation.

***Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.**

[1]*Analog Devices Applications Guide to Isolation Amplifiers and Signal Conditioners*

[2]Sheingold, D.H., ed, *Transducer Interfacing Handbook – A guide to analog signal conditioning*. Norwood, MA 02062 (P.O. Box 796): Analog Devices, Inc., 1980, $14.50

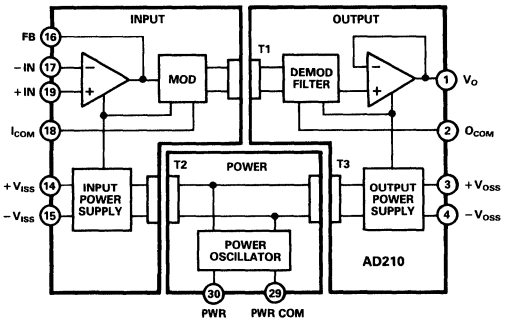


Figure 1. AD210 Block Diagram

Functional Characteristics: The figure shows the circuit architecture of a self-contained isolator, Model AD210. The various models differ, but their properties can be discussed in terms of the device shown. An isolator of this type requires power from a two-terminal dc supply. An internal oscillator converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output. The ac carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered and buffered, using isolated dc power (also available for auxiliary circuitry) derived from the carrier.

The amplifier in this example is an uncommitted op amp, specified for programmable gains from 1 to 100V/V, as determined by its feedback circuitry. Since both input terminals are floating, the amplifier functions effectively as an instrumentation amplifier. Most of the other devices in this series require just a single external resistor to set the gain.

In the figure it can be seen that ac power is magnetically coupled from the oscillator to the output stage. This permits the output to operate at a dc common-mode potential with respect to power common. An isolator of this type is said to provide *three-port* isolation, because there are three isolated ports: input, power supply and output. Two-port devices are those in which there is a dc connection between the oscillator power supply and the output stage.

The AD210, as can be seen, is a completely self-contained device. There are applications for which a degree of "unbundling" can lead to economy and improved performance. For example, if there are many input channels to be isolated, economies can be realized by the use of a common oscillator. In addition, the common oscillator makes it possible to avoid the possibility of small errors due to beat frequencies developed by small amounts of crosstalk in older amplifier designs.

Several synchronized multichannel devices are available. Model 204 is essentially a 202A with a power converter instead of an oscillator. It requires a pair of leads for an oscillator input, which can be furnished by an AD246 clock.

SPECIFICATIONS

The illustration on the next page shows a typical specification block; the specifications of key interest are defined.

For an initial choice of data sheets to inspect for a given application, the Selection Guide permits comparison on the basis of these key characteristics: common-mode voltage, specified gain range and frequency response. The "Notes" column indicates which devices require external oscillators (for lower cost in many-channel applications) and identifies devices that are three-port isolated. Good starting points are: for high performance, the AD210; for lowest cost, the AD202 and AD204, depending on whether the application calls for few or many channels; for military temperature, the AD203; for maximum precision, the AD208; and for the widest bandwidth, the AD206.

SPECIFICATIONS (typical @ + 25°C, & V_S = +15V unless otherwise specified)

Model	AD210AN	AD210BN
GAIN		
Range	1V/V – 100V/V	*
Error	± 2% max	± 1% max
vs. Temperature (0 to + 70°C)	± 25ppm/°C max	*
(– 25°C to + 85°C)	± 50ppm/°C max	*
vs. Supply Voltage	± 0.002%/V	*
Nonlinearity[1]	± 0.025% max	± 0.012% max
Nonlinearity vs. Isolated Supply Load	± 0.002%/mA	*
INPUT VOLTAGE RATINGS		
Linear Differential Range	± 10V	*
Maximum Safe Differential Input	± 15V	*
Max. CMV Input-to-Output		
ac, 60Hz, Continuous	2500V rms	*
dc, Continuous	± 3500V peak	*
Common-Mode Rejection		
60Hz, G = 100V/V		
$R_S \leq 500\Omega$ Impedance Imbalance	120dB	*
Leakage Current Input-to-Output		
@ 240Vrms, 60Hz	2μA rms max	*
INPUT IMPEDANCE		
Differential	$10^{12}\Omega$	*
Common Mode	$5G\Omega \| 5pF$	*
INPUT BIAS CURRENT		
Initial, @ + 25°C	30pA typ (400pA max)	*
vs. Temperature (0 to + 70°C)	10nA max	*
(– 25°C to + 85°C)	30nA max	*
INPUT DIFFERENCE CURRENT		
Initial, @ + 25°C	5pA typ (200pA max)	*
vs. Temperature (0 to + 70°C)	2nA max	*
(– 25°C to + 85°C)	10nA max	*
INPUT NOISE		
Voltage (1kHz)	$18nV/\sqrt{Hz}$	*
(10Hz to 10kHz)	4μV rms	*
Current (1kHz)	$0.01pA/\sqrt{Hz}$	*
FREQUENCY RESPONSE		
Bandwidth (– 3dB)		
G = 1V/V	20kHz	*
G = 100V/V	15kHz	*
Settling Time (± 10mV, 20V Step)		
G = 1V/V	150μs	*
G = 100V/V	500μs	*
Slew Rate (G = 1V/V)	1V/μs	*
OFFSET VOLTAGE (RTI)[2]		
Initial, @ + 25°C	(± 15 ± 45/G)mV max	(± 5 ± 15/G)mV max
vs. Temperature (0 to + 70°C)	(± 10 ± 30/G)μV/°C	*
(– 25°C to + 85°C)	(± 10 ± 50/G)μV/°C	*
RATED OUTPUT[3]		
Voltage, 2kΩ Load	± 10V min	*
Impedance	1Ω max	*
Ripple, (Bandwidth = 100kHz)	10mV p-p max	*
ISOLATED POWER OUTPUTS[4]		
Voltage, No Load	± 15V	*
Accuracy	± 10%	*
Current	± 5mA	*
Regulation, No Load to Full Load	See Text	*
Ripple	See Text	*
POWER SUPPLY		
Voltage, Rated Performance	+ 15V dc ± 5%	*
Voltage, Operating	+ 15V dc ± 10%	*
Current, Quiescent	50mA	*
Current, Full Load – Full Signal	80mA	*
TEMPERATURE RANGE		
Rated Performance	– 25°C to + 85°C	*
Operating	– 40°C to + 85°C	*
Storage	– 40°C to + 85°C	*
PACKAGE DIMENSIONS		
Inches	1.00 × 2.10 × 0.350	*
Millimeters	25.4 × 53.3 × 8.9	*

NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]RTI – Referred to Input
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

NONLINEARITY – This is the peak deviation from a best straight line, expressed as a % of peak-to-peak output. Should be considered when signal fidelity is of prime importance.

MAX SAFE DIFFERENTIAL INPUT – Max voltage that can be safely applied across input terminals. Important to consider for fail-safe designs in the presence of high voltages.

INPUT NOISE – Total noise, referred to the input. Facilitates comparison with expected signal input levels.

ISOLATED POWER OUTPUTS – Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input and output signal conditioners, front-end amplifiers, as well as remote transducers.

CMV, INPUTS TO OUTPUTS – Voltage that may be safely applied to *both* inputs with respect to outputs or power common. Necessary consideration in applications with high CMV input or when high voltage transients may occur at the input.

CMR, INPUTS TO OUTPUTS – Indicates ability to reject common-mode voltages between inputs and outputs. Important when processing small signals riding on high common-mode voltages.

LEAKAGE CURRENT – Maximum input leakage current when power-line voltage is impressed on inputs. Vital consideration for patient safety in medical applications.

OFFSET VOLTAGE REFERRED TO INPUT – Total input drift is composed of two sources (input and output stage drifts) and is gain (G) dependent. Referring offsets to the input allows them to be compared to signal levels.

Figure 2. Typical Isolator Specifications

ANALOG DEVICES

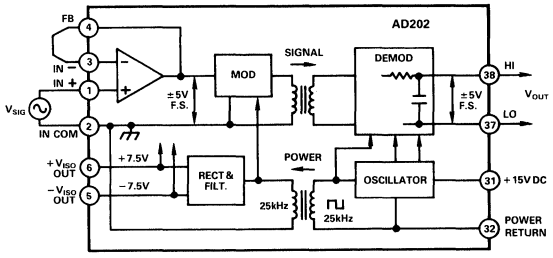
Low Cost, Miniature Isolation Amplifiers

AD202/AD204

FEATURES
Small Size: 4 Channels/Inch
Low Power: 35mW (AD204)
High Accuracy: ±0.025% max Nonlinearity (K Grade)
High CMR: 130dB (Gain = 100V/V)
Wide Bandwidth: 5kHz Full-Power (AD204)
High CMV Isolation: ±2000V pk Continuous (K Grade) (Signal and Power)
Isolated Power Outputs
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
Current Shunt Measurements
Motor Controls
Process Signal Isolation
High Voltage Instrumentation Amplifier

AD202 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD202 and AD204 are members of a new generation of low cost, high performance isolation amplifiers. A new circuit design, novel transformer construction, and the use of surface-mounted components in an automated assembly process result in remarkably compact, economical isolators whose performance in many ways exceeds that previously available from very expensive devices. The primary distinction between the AD202 and AD204 is that the AD202 is powered directly from +15V dc while the AD204 is powered by an externally supplied clock (AD246).

The AD202 and AD204 employ transformer coupling and do not require the design compromises that must be made when optical isolators are used: each provides a complete isolation function, with both signal and power isolation internal to the module, and they exhibit no long-term parameter shifts under sustained common-mode stress. Power consumption, nonlinearity, and drift are each an order of magnitude lower than can be obtained from other isolation techniques, and these advantages are obtained without sacrifice of bandwidth or noise performance.

The design of the AD202 and AD204 emphasizes ease of use in a broad range of applications where signals must be measured or transmitted without a galvanic connection. In addition, the low cost and small size of these isolators makes component-level circuit applications of isolation practical for the first time.

PRODUCT HIGHLIGHTS

The AD202 and AD204 are full-featured isolators offering numerous benefits to the user:

Small Size: The AD202 and AD204 are available in SIP and DIP form packages. The SIP package is just 0.25" wide, giving the user a channel density of four channels per inch. The isolation barrier is positioned to maximize input to output spacing. For applications requiring a low profile, the DIP package provides a height of just 0.350".

High Accuracy: With a maximum nonlinearity of ±0.025% for the AD202K/AD204K (±0.05% for the AD202J/AD204J) and low drift over temperature, the AD202 and AD204 provide high isolation without loss of signal integrity.

Low Power: Power consumption of 35mW (AD204) and 75mW (AD202) over the full signal range makes these isolators ideal for use in applications with large channel counts or tight power budgets.

Wide Bandwidth: The AD204's full-power bandwidth of 5kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Excellent Common-Mode Performance: The AD202K/AD204K provide ±2000V pk continuous common-mode isolation, while the AD202J/AD204J provide ±1000V pk continuous common-mode isolation. All models have a total common-mode input capacitance of less than 5pF inclusive of power isolation. This results in CMR ranging from 130dB at a gain of 100 to 104dB (minimum at unity gain) and very low leakage current (2μA maximum).

Flexible Input: An uncommitted op amp is provided at the input of all models. This provides buffering and gain as required, and facilitates many alternative input functions including filtering, summing, high-voltage ranges, and current (transimpedance) input.

Isolated Power: The AD204 can supply isolated power of ±7.5V at 2mA. This is sufficient to operate a low-drift input preamp, provide excitation to a semiconductor strain gage, or to power any of a wide range of user-supplied ancillary circuits. The AD202 can supply ±7.5V at 0.4mA which is sufficient to operate adjustment networks or low-power references and op amps, or to provide an open-input alarm.

SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

Model	AD204J	AD204K	AD202J	AD202K
GAIN				
Range	1V/V-100V/V	*	*	*
Error	±0.5% typ (±4% max)	*	*	*
vs. Temperature	±20ppm/°C typ (±45ppm/°C max)	*	*	*
vs. Time	±50ppm/1000 Hours	*	*	*
vs. Supply Voltage	±0.01%/V	±0.01%/V	±0.01%/V	±0.01%/V
Nonlinearity (G=1V/V)[1]	±0.05% max	±0.025% max	±0.05% max	±0.025% max
Nonlinearity vs. Isolated Supply Load	±0.0015%/mA	*	*	*
INPUT VOLTAGE RATINGS				
Linear Differential Range	±5V	*	*	*
Max Safe Differential Input	±7.5V	*	*	*
Max CMV Input to Output				
ac, 60Hz, Continuous	750V rms	1500V rms	750V rms	1500V rms
Continuous (dc and ac)	±1000V peak	±2000V peak	±1000V peak	±2000V peak
Common-Mode Rejection (CMR), @ 60Hz				
R_S = ≤100Ω (HI & LO Inputs) G=1	110dB	110dB	105dB	105dB
G=100	130dB	*	*	*
R_S = ≤1kΩ (Input HI, LO, or Both) G=1	104dB min	104dB min	100dB min	100dB min
G=100	110dB min	*	*	*
Leakage Current Input to Output				
@240V rms, 60Hz	2μA rms max	*	*	*
INPUT IMPEDANCE				
Differential (G=1V/V)	10^{12} Ω	*	*	*
Common Mode	2GΩ‖4.5pF	*	*	*
INPUT BIAS CURRENT				
Initial, @ +25°C	±30pA	*	*	*
vs. Temperature (0 to +70°C)	±10nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±5pA	*	*	*
vs. Temperature (0 to +70°C)	±2nA	*	*	*
INPUT NOISE				
Voltage, 0.1 to 100Hz	4μV p-p	*	*	*
f>200Hz	50nV/√Hz	*	*	*
FREQUENCY RESPONSE				
Bandwidth (V_O ≤10V p-p, G=1-50V/V)	5kHz	5kHz	2kHz	2kHz
Settling Time, to ±10mV (10V Step)	1ms	*	*	*
OFFSET VOLTAGE (RTI)				
Initial, @ +25°C Adjustable to Zero	(±15 ±15/G)mV max	(±5 ±5/G)mV max	(±15 ±15/G)mV max	(±5 ±5/G)mV max
vs. Temperature (0 to +70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)$μV/°C	*	*	*
RATED OUTPUT				
Voltage (Out HI to Out LO)	±5V	*	*	*
Voltage at Out HI or Out LO (Ref. Pin 32)	±6.5V	*	*	*
Output Resistance	3kΩ	3kΩ	7kΩ	7kΩ
Output Ripple, 100kHz Bandwidth	10mV pk-pk	*	*	*
5kHz Bandwidth	0.5mV rms	*	*	*
ISOLATED POWER OUTPUT[2]				
Voltage, No Load	±7.5V	*	*	*
Accuracy	±10%	*	*	*
Current	2mA (Either Output)[3]	2mA (Either Output)[3]	400μA Total	400μA Total
Regulation, No Load to Full Load	5%	*	*	*
Ripple	100mV pk-pk	*	*	*
OSCILLATOR DRIVE INPUT				
Input Voltage	15V pk-pk nominal	15V pk-pk nominal	N/A	N/A
Input Frequency	25kHz nominal	25kHz nominal	N/A	N/A
POWER SUPPLY (AD202 Only)				
Voltage, Rated Performance	N/A	N/A	+15V ±5%	+15V ±5%
Voltage, Operating	N/A	N/A	+15V ±10%	+15V ±10%
Current, No Load (V_S = +15V)	N/A	N/A	5mA	5mA
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	*	*	*
Operating	−40°C to +85°C	*	*	*
Storage	−40°C to +85°C	*	*	*
PACKAGE DIMENSIONS[4]				
SIP Package (Y)	2.08″ × 0.250″ × 0.625″	*	*	*
DIP Package (N)	2.10″ × 0.700″ × 0.350″	*	*	*

NOTES
*Specifications same as AD204J.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]1.0μF min decoupling required (see text).
[3]3mA with one supply loaded.
[4]Width is 0.25″ typ, 0.26″ max.
Specifications subject to change without notice.

PIN DESIGNATIONS

AD202/AD204 SIP PACKAGE

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
4	INPUT FEEDBACK
5	$-V_{ISO}$ OUTPUT
6	$+V_{ISO}$ OUTPUT
31	+15V POWER IN (AD202 ONLY)
32	CLOCK/POWER COMMON
33	CLOCK INPUT (AD204 ONLY)
37	OUTPUT LO
38	OUTPUT HI

AD202/AD204 DIP PACKAGE

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
18	OUTPUT LO
19	OUTPUT HI
20	+15V POWER IN (AD202 ONLY)
21	CLOCK INPUT (AD204 ONLY)
22	CLOCK/POWER COMMON
36	$+V_{ISO}$ OUTPUT
37	$-V_{ISO}$ OUTPUT
38	INPUT FEEDBACK

5

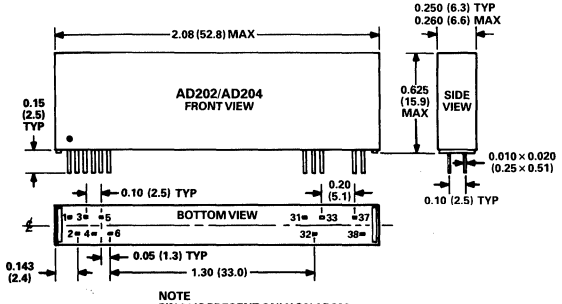
AD202/AD204 ORDERING GUIDE

Model	Package Option	Max Common-Mode Voltage (Peak)	Max Linearity
AD202JY	SIP	1000V	±0.05%
AD202KY	SIP	2000V	±0.025%
AD202JN	DIP	1000V	±0.05%
AD202KN	DIP	2000V	±0.025%
AD204JY	SIP	1000V	±0.05%
AD204KY	SIP	2000V	±0.025%
AD204JN	DIP	1000V	±0.05%
AD204KN	DIP	2000V	±0.025%

OUTLINE DIMENSIONS

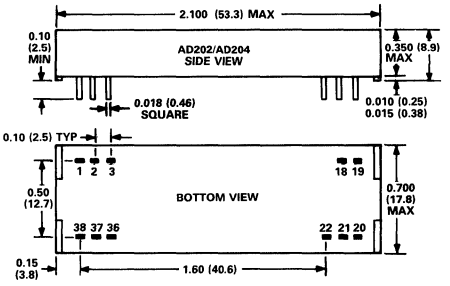
Dimensions shown in inches and (mm).

AD202/AD204 SIP PACKAGE



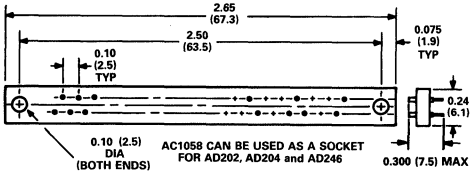
NOTE
PIN 31 IS PRESENT ONLY ON AD202.
PIN 33 IS PRESENT ONLY ON AD204.

AD202/AD204 DIP PACKAGE



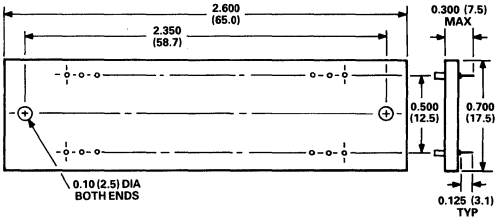
NOTE
PIN 20 IS PRESENT ONLY ON AD202.
PIN 21 IS PRESENT ONLY ON AD204.

AC1058 MATING SOCKET



NOTE: AMP ZP SOCKET (PIN 2 – 382006 – 3) MAY BE USED IN PLACE OF THE AC1058.

AC1060 MATING SOCKET



SPECIFICATIONS

(typical @ +25°C and V_S = +15V unless otherwise noted)

Model	AD246JY	AD246JN
OUTPUT[1]		
Frequency	25kHz nominal	*
Voltage	15V p-p nominal	*
Fan-Out	32 max	*
POWER SUPPLY REQUIREMENTS		
Input Voltage	+15V ±5%	*
Supply Current		
Unloaded	3.5mA	*
Each AD204 Adds	2.2mA	*
Each 1mA Load on AD204 +V_{ISO} or −V_{ISO} Adds	0.7mA	*

NOTES

*Specifications the same as the AD246JY.

[1]The high current drive output will not support a short to ground.

Specifications subject to change without notice.

AD246 PIN DESIGNATIONS

PIN (Y)	PIN (N)	FUNCTION
1	12	+15V POWER IN
2	1	CLOCK OUTPUT
12	14	COMMON
13	24	COMMON

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

DIFFERENCES BETWEEN THE AD202 AND AD204

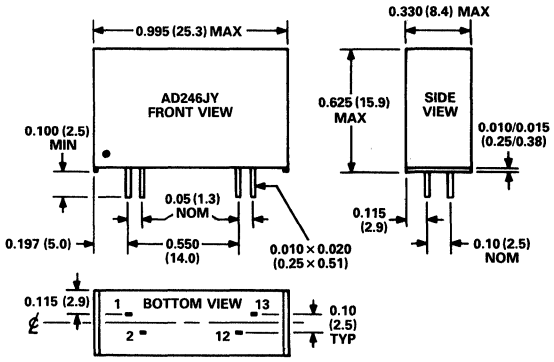
The primary distinction between the AD202 and AD204 is in the method by which they are powered: the AD202 operates directly from +15V dc while the AD204 is powered by a non-isolated externally-supplied clock (AD246) which can drive up to 32 AD204s. The main advantages of using the externally-clocked AD204 over the AD202 are reduced cost in multichannel applications, lower power consumption, and higher bandwidth. In addition, the AD204 can supply substantially more isolated power than the AD202.

Of course, in a great many situations, especially where only one or a few isolators are used, the convenience of stand-alone operation provided by the AD202 will be more significant than any of the AD204's advantages. There may also be cases where it is desirable to accommodate either device interchangeably, so the pinouts of the two products have been designed to make that easy to do.

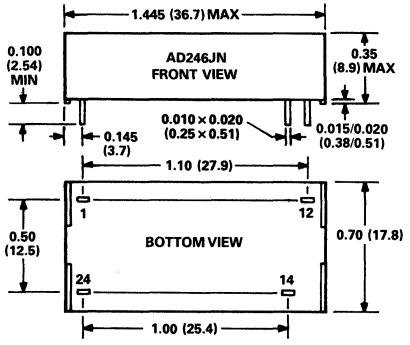
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

AD246JY PACKAGE



AD246JN PACKAGE



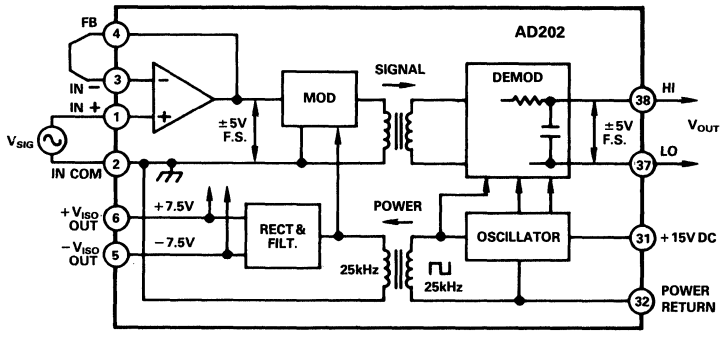


Figure 1a. AD202 Functional Block Diagram

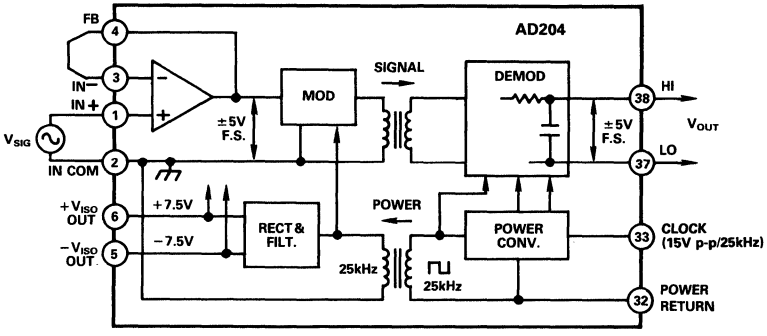


Figure 1b. AD204 Functional Block Diagram
(Pin Designations Apply to the DIP-Style Package.)

INSIDE THE AD202 AND AD204

The AD202 and AD204 use an amplitude modulation technique to permit transformer coupling of signals down to dc (Figure 1a and 1b). Both models also contain an uncommitted input op amp and a power transformer which provides isolated power to the op amp, the modulator, and any external load. The power transformer primary is driven by a 25kHz, 15V p-p square wave which is generated internally in the case of the AD202, or supplied externally for the AD204.

Within the signal swing limits of approximately ±5V, the output voltage of the isolator is equal to the output voltage of the op amp; that is, the isolation barrier has unity gain. The output signal is not internally buffered, so the user is free to interchange the output leads to get signal inversion. Additionally, in multi-channel applications, the unbuffered outputs can be multiplexed with one buffer following the mux. This technique minimizes offset errors while reducing power consumption and cost. The output resistance of the isolator is typically 3kΩ for the AD204 (7kΩ for AD202) and varies with signal level and temperature, so it should not be loaded (see Figure 2 for the effects of load upon nonlinearity and gain drift). In many cases a high-impedance load will be present or a following circuit such as an output filter can serve as a buffer, so that a separate buffer function will not often be needed.

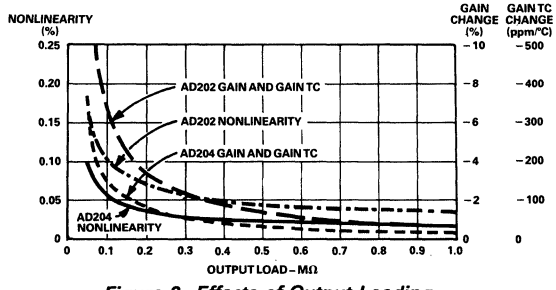


Figure 2. Effects of Output Loading

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

USING THE AD202 AND AD204

Powering the AD202. The AD202 requires only a single +15V power supply connected as shown in Figure 3a. A bypass capacitor is provided in the module.

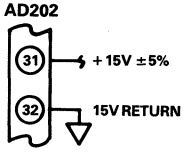


Figure 3a.

Powering the AD204. The AD204 gets its power from an externally supplied clock signal (a 15V p-p square wave with a nominal frequency of 25kHz) as shown in Figure 3b.

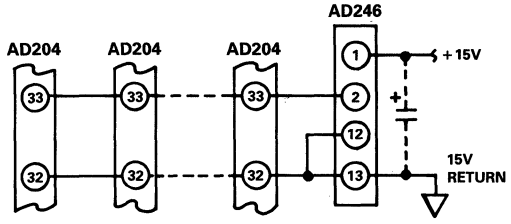


Figure 3b.

AD246 Clock Driver. The AD246 is a compact, inexpensive clock driver that can be used to obtain the required clock from a single 15V supply. Alternatively, the circuit shown in Figure 4 (essentially an AD246) can be used. In either case, one clock circuit can operate at least 32 AD204s at the rated minimum supply voltage of 14.25V and one additional isolator can be operated for each 40mV increase in supply voltage up to 15V. A supply bypass capacitor is included in the AD246, but if many AD204s are operated from a single AD246, an external bypass capacitor should be used with a value of at least 1μF for every five isolators used. Place the capacitor as close as possible to the clock driver.

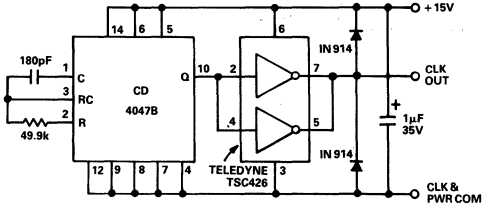


Figure 4. Clock Driver

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

Input Configurations. The AD202 and AD204 have been designed to be very easy to use in a wide range of applications. The basic connection for standard unity gain applications, useful for signals up to ±5V, is shown in Figure 5; some of the possible variations are described below. When smaller signals must be

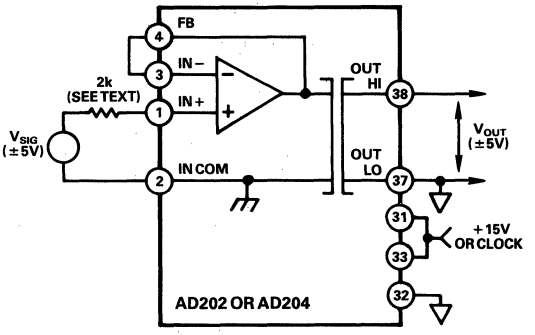


Figure 5. Basic Unity-Gain Application

handled, Figure 6 shows how to get gain while preserving a very high input resistance. The value of feedback resistor R_F should be kept above 20kΩ for best results. Whenever a gain of more than five is taken, a 100pF capacitor from FB to IN COM is required. At lower gains this capacitor is unnecessary, but it will not adversely affect performance if used.

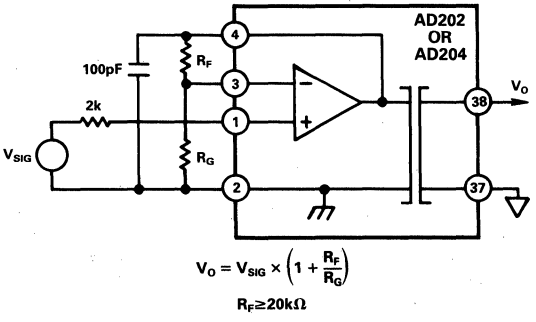


Figure 6. Input Connections for Gain > 1

The "noninverting" circuit of Figures 5 and 6 can also be used to advantage when a signal inversion is needed: just interchange either the input leads or the output leads to get inversion. This approach retains the high input resistance of the "noninverting" circuit, and at unity gain no gain-setting resistors are needed.

When the isolator is not powered, a negative input voltage of more than about 2V will cause an input current to flow. If the signal source can supply more than a few mA under such conditions, the 2kΩ resistor shown in series with IN+ should be used to limit current to a safe value. This is particularly important with the AD202, which may not start if a large input current is present.

Figure 7 shows how to accommodate current inputs or sum currents or voltages. This circuit can also be used when the input signal is larger than the ±5V input range of the isolator; for example, a ±50V input span can be accommodated with R_F = 20k and R_S = 200k. Once again, a capacitor from FB to IN COM is required for gains above 5.

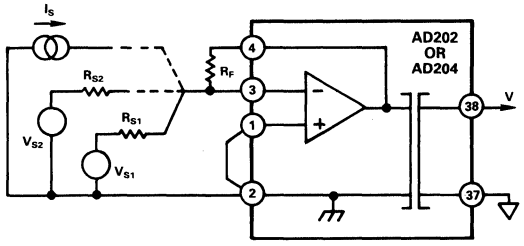


Figure 7. Connections for Summing or Current Inputs

Adjustments. When gain and zero adjustments are needed, the circuit details will depend on whether adjustments are to be made at the isolator input or output, and (for input adjustments) on the input circuit used. Adjustments are usually best done on the input side, because it is better to null the zero ahead of the gain, and because gain adjustment is most easily done as part of the gain-setting network. Input adjustments are also to be preferred when the pots will be near the input end of the isolator (to minimize common-mode strays). Adjustments on the output side might be used if pots on the input side would represent a hazard due to the presence of large common-mode voltages during adjustment.

Figure 8a shows the input-side adjustment connections for use with the "noninverting" connection of the input amplifier. The zero adjustment circuit injects a small adjustment voltage in series with the low side of the signal source. (This will not work if the source has another current path to input common or if current flows in the signal source LO lead). Since the adjustment voltage is injected ahead of the gain, the values shown will work for any gain. Keep the resistance in series with input LO below a few hundred ohms to avoid CMR degradation.

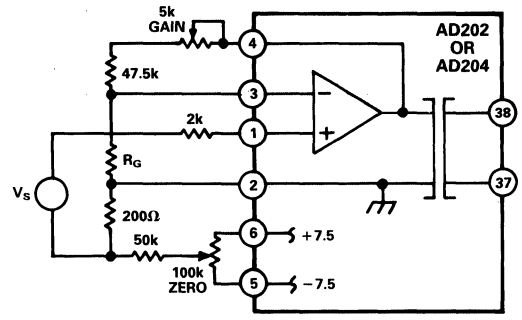


Figure 8a. Adjustments for Noninverting Connection of Op Amp

Also shown in Figure 8a is the preferred means of adjusting the gain-setting network. The circuit shown gives a nominal R_F of 50kΩ, and will work properly for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input resistance; it is better to adjust gain at the signal source or after the output.

Figure 8b shows adjustments for use with inverting input circuits. The zero adjustment nulls the voltage at the summing node. This method is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is again done in the feedback; but in this case it will work all the way down to unity gain (and below) without alteration.

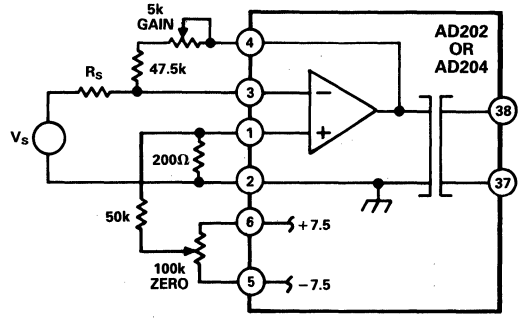


Figure 8b. Adjustments for Summing or Current Input

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

Figure 9 shows how zero adjustment is done at the output by taking advantage of the semi-floating output port. The range of this adjustment will have to be increased at higher gains; if that is done, be sure to use a suitably stable supply voltage for the pot circuit.

There is no easy way to adjust gain at the output side of the isolator itself. If gain adjustment must be done on the output side, it will have to be in a following circuit such as an output buffer or filter.

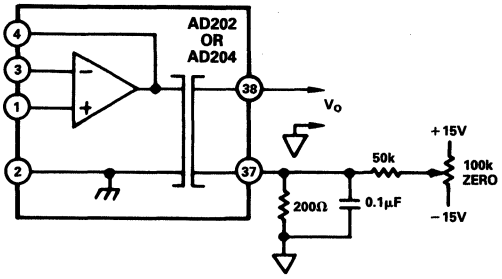


Figure 9. Output-Side Zero Adjustment

Common-Mode Performance. Figures 10a and 10b show how the common-mode rejection of the AD202 and AD204 varies with frequency, gain, and source resistance. For these isolators, the significant resistance will normally be that the path from the source of the common-mode signal to IN COM. The AD202 and AD204 also perform well in applications requiring rejection of fast common-mode steps, as described in the Applications section.

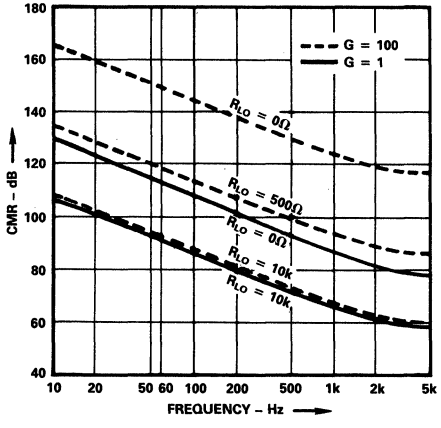


Figure 10a. AD204

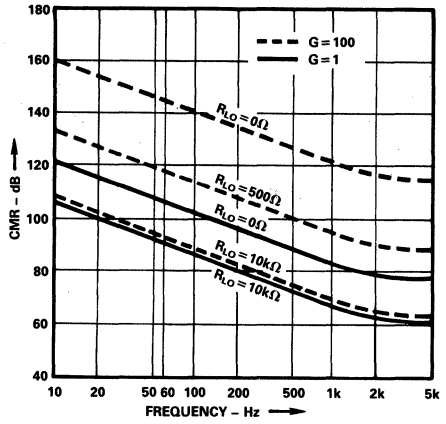


Figure 10b. AD202

Dynamics and Noise. Frequency response plots for the AD202 and AD204 are given in Figure 11. Since neither isolator is slew-rate limited, the plots apply for both large and small signals. Capacitive loads of up to 470pF will not materially affect frequency response. When large signals beyond a few hundred Hz will be present, it is advisable to bypass $-V_{ISO}$ and $+V_{ISO}$ to IN COM with 1μF tantalum capacitors even if the isolated supplies are not loaded.

At 50/60Hz, phase shift through the AD202/AD204 is typically 0.8° (lagging). Typical unit – unit variation is ±0.2° (lagging).

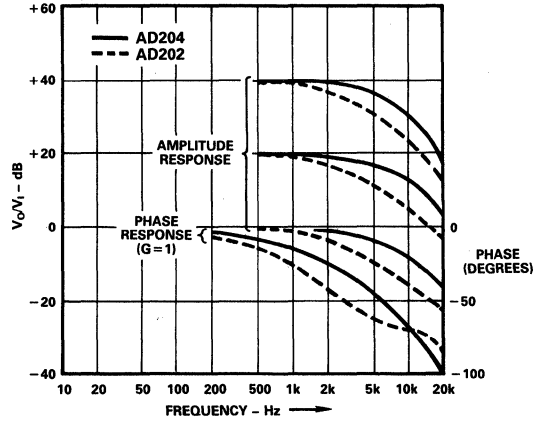


Figure 11. Frequency Response at Several Gains

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

The step response of the AD204 for very fast input signals can be improved by the use of an input filter, as shown in Figure 12. The filter limits the bandwidth of the input (to about 5.3kHz) so that the isolator does not see fast, out-of-band input terms that can cause small amounts (±0.3%) of internal ringing. The AD204 will then settle to ±0.1% in about 300 microseconds for a 10V step.

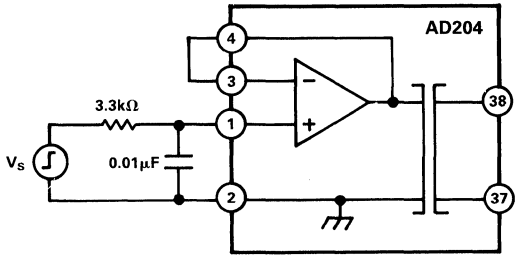


Figure 12. Input Filter for Improved Step Response

Except at the highest useful gains, the noise seen at the output of the AD202 and AD204 will be almost entirely comprised of carrier ripple at multiples of 25kHz. The ripple is typically 2mV p-p near zero output and increases to about 7mV p-p for outputs of ±5V (1MHz measurement bandwidth). Adding a capacitor across the output will reduce ripple at the expense of bandwidth: for example, 0.05μF at the output of the AD204 will result in 1.5mV ripple at ±5V, but signal bandwidth will be down to 1kHz.

When the full isolator bandwidth is needed, the simple two-pole active filter shown in Figure 13 can be used. It will reduce ripple to 0.1mV p-p with no loss of signal bandwith, and also serves as an output buffer.

An output buffer or filter may sometimes show output spikes that do not appear at its input. This is usually due to clock noise appearing at the op amp's supply pins (since most op amps have little or no supply rejection at high frequencies). Another common source of carrier-related noise is the sharing of a ground track by both the output circuit and the power input. Figure 13 shows how to avoid these problems: the clock/supply port of the isolator does not share ground or 15V tracks with any signal circuits, and the op amp's supply pins are bypassed to signal common (note that the grounded filter capacitor goes here as well). Ideally, the output signal LO lead and the supply common meet where the isolator output is actually measured, e.g. at an A/D converter input. If that point is more than a few feet from the isolator, it may be useful to bypass output LO to supply common at the isolator with a 0.1μF capacitor.

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

In applications where more than a few AD204s are driven by a single clock driver, substantial current spikes will flow in the power return line and in whichever signal out lead returns to a low impedance point (usually output LO). Both of these tracks should be made large to minimize inductance and resistance; ideally, output LO should be directly connected to a ground plane which serves as measurement common.

Current spikes can be greatly reduced by connecting a small inductance (68μH–100μH) in series with the clock pin of each AD204. Molded chokes such as the Dale IM-2 series, with dc resistance of about 5Ω, are suitable.

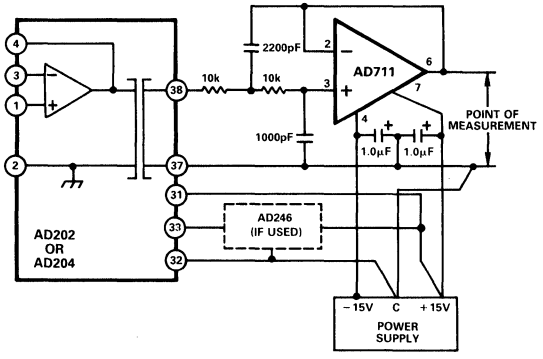


Figure 13. Output Filter Circuit Showing Proper Grounding

Using Isolated Power. Both the AD202 and the AD204 provide ±7.5V power outputs referenced to input common. These may be used to power various accessory circuits which must operate at the input common-mode level; the input zero adjustment pots described above are an example, and several other possible uses are shown in the section titled Application Examples.

The isolated power output of the AD202 (400μA total from either or both outputs) is much more limited in current capacity than that of the AD204, but it is sufficient for operating micropower op amps, low power references (such as the AD589), adjustment circuits, and the like.

The AD204 gets its power from an external clock driver, and can handle loads on its isolated supply outputs of 2mA for each supply terminal (+7.5V and −7.5V) or 3mA for a single loaded output. Whenever the external load on either supply is more than about 200μA, a 1μF tantalum capacitor should be used to bypass each loaded supply pin to input common.

Up to 32 AD204s can be driven from a single AD246 (or equivalent) clock driver when the isolated power outputs of the AD204s are loaded with less than 200μA each, at a worst-case supply voltage of 14.25V at the clock driver. The number of AD204s that can be driven by one clock driver is reduced by one AD204 per 3.5mA of isolated power load current at 7.5V, distributed in any way over the AD204's being supplied by that clock driver. Thus a load of 1.75mA from $+V_{ISO}$ to $-V_{ISO}$ would also count as one isolator because it spans 15V.

It is possible to increase clock fanout by increasing supply voltage above the 14.25V minimum required for 32 loads. One additional isolator (or 3.5mA unit load) can be driven for each 40mV of increase in supply voltage up to 15V. Therefore if the minimum supply voltage can be held to 15V – 1%, it is possible to operate 32 AD204's and 52mA of 7.5V loads. Figure 14 shows the allowable combinations of load current and channel count for various supply voltages.

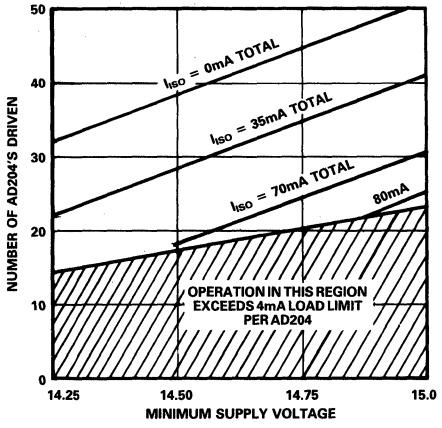


Figure 14. AD246 Fanout Rules

Operation at Reduced Signal Swing. Although the nominal output signal swing for the AD202 and AD204 is ±5V, there may be cases where a smaller signal range may be desirable. When that is done, the fixed errors (principally offset terms and output noise) become a larger fraction of the signal, but nonlinearity is reduced. This is shown in Figure 15.

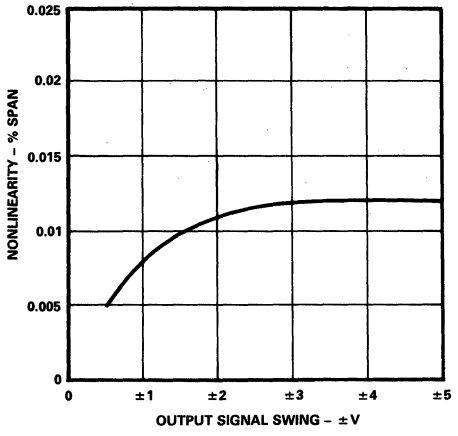


Figure 15. Nonlinearity vs. Signal Swing

PCB Layout for Multichannel Applications. The pinout of the AD204Y has been designed to make very dense packing possible in multichannel applications. Figure 16a shows the recommended printed circuit board (PCB) layout for the simple voltage-follower connection. When gain-setting resistors are present, 0.25″ channel centers can still be achieved, as shown in Figure 16b.

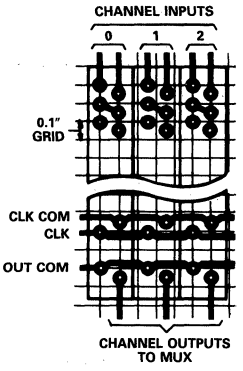


Figure 16a.

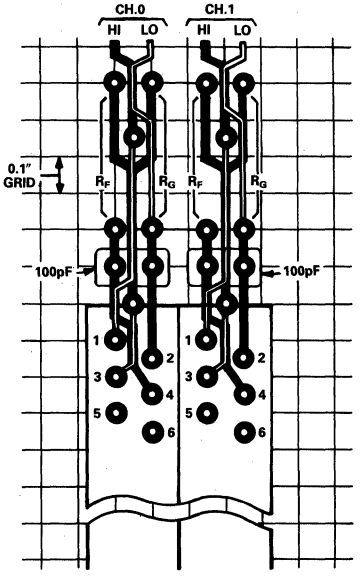


Figure 16b.

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

Synchronization. Since AD204's operate from a common clock, synchronization is inherent. AD202s will normally not interact to produce beat frequencies even when mounted on 0.25-inch centers. Interaction may occur in rare situations where a large number of long, unshielded input cables are bundled together and channel gains are high. In such cases, shielded cable may be required or AD204's can be used.

APPLICATIONS EXAMPLES

Low-Level Sensor Inputs. In applications where the output of low-level sensors such as thermocouples must be isolated, a low-drift input amplifier can be used with an AD204, as shown in Figure 17. A three-pole active filter is included in the design to get normal-mode rejection of frequencies above a few Hz and to provide enhanced common-mode rejection at 60Hz. If offset adjustment is needed, it is best done at the trim pins of the OP-07 itself; gain adjustment can be done at the feedback resistor.

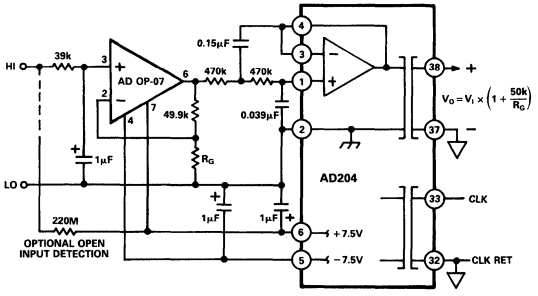


Figure 17. Input Amplifier & Filter for Sensor Signals

Note that the isolated supply current is large enough to mandate the use of 1µF supply bypass capacitors. This circuit can be used with an AD202 if a low-power op amp is used instead of the OP-07.

Process Current Input with Offset. Figure 18 shows an isolator receiver which translates a 4-20mA process current signal into a 0 to +10V output. A 1V to 5V signal appears at the isolator's output, and a −1V reference applied to output LO provides the necessary level shift (in multichannel applications, the reference can be shared by all channels). This technique is often useful for getting offset with a follower-type output buffer.

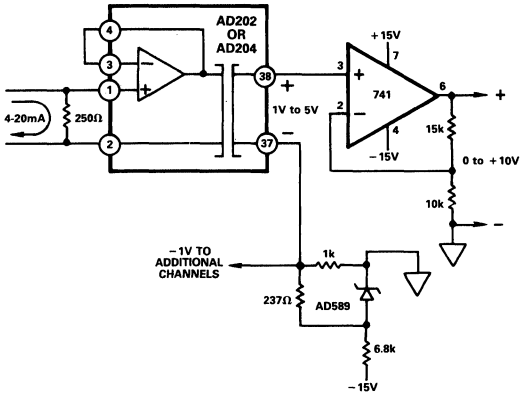


Figure 18. Process Current Input Isolator with Offset

The circuit as shown requires a source compliance of at least 5V, but if necessary that can be reduced by using a lower value of current-sampling resistor and configuring the input amplifier for a small gain.

High-Compliance Current Source. In Figure 19, an isolator is used to sense the voltage across current-sensing resistor R to allow direct feedback control of a high-voltage transistor or FET used as a high-compliance current source. Since the isolator has virtually no response to dc common-mode voltage, the closed-loop current source has a static output resistance greater than $10^{14}\Omega$ even for output currents of several mA. The output current capability of the circuit is limited only by power dissipation in the source transistor.

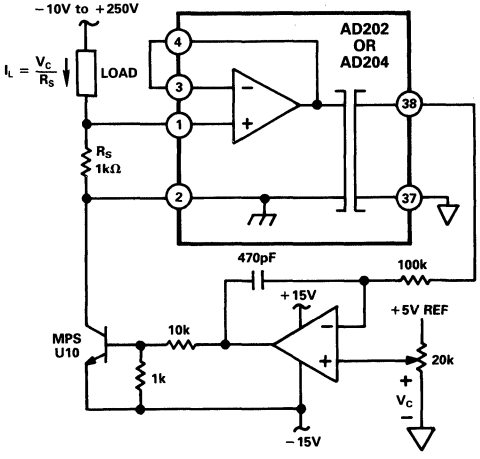


Figure 19. High-Compliance Current Source

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

Motor Control Isolator. The AD202 and AD204 perform very well in applications where rejection of fast common-mode steps is important but bandwidth must not be compromised. Current sensing in a full-wave bridge motor driver (Figure 20) is one example of this class of application. For 200V common-mode steps (1μs rise time) and a gain of 50 as shown, the typical response at the isolator output will be spikes of ±5mV amplitude, decaying to zero in less than 100μs. Spike height can be reduced by a factor of four with output filtering just beyond the isolator's bandwidth.

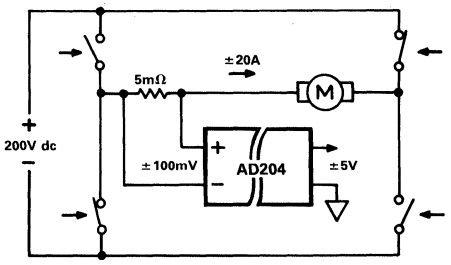


Figure 20. Motor Control Current Sensing

Floating Current Source/Ohmmeter. When a small floating current is needed with a compliance range of up to ±1000V dc, the AD204 can be used to both create and regulate the current. This can save considerable power, since the controlled current does not have to return to ground. In Figure 21, an AD589 reference is used to force a small fixed voltage across R. That sets the current which the input op amp will have to return through the load to zero its input. Note that the isolator's output isn't needed at all in this application; the whole job is done by the input section. However, the signal at the output could be useful: it's the voltage across the load, referenced to ground. Since the load current is known, the output voltage is proportional to load resistance.

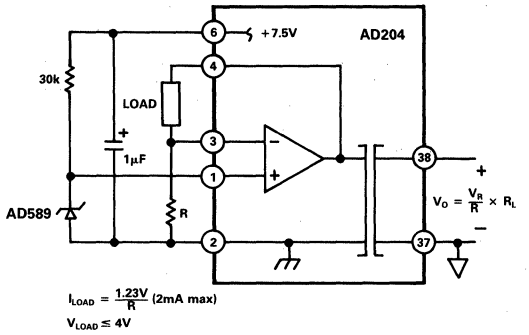


Figure 21. Floating Current Source

Photodiode Amplifier. Figure 22 shows a transresistance connection used to isolate and amplify the output of a photodiode. The photodiode operates at zero bias, and its output current is scaled by R_F to give a +5V full-scale output.

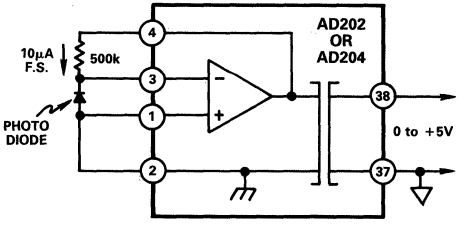


Figure 22. Photodiode Amplifier

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

ANALOG DEVICES

Rugged, Military Temperature Range, 10 kHz Bandwidth Isolation Amplifier

AD203SN

FEATURES

Rugged Design: Meets Stringent MIL-STD-883C
Environmental Test Methods
1004 (Moisture Resistance)
1010 Condition B (Temperature Cycling, −55°C to +125°C)
2002 Condition B (Mechanical Shock @ 1,500 g for 0.5 ms)
2004 (Lead Integrity)
2007 Condition A (Variable Frequency Vibration @ 20 g)
2015 (Resistance to Solvents)
Reliable Design: Conforms to Stringent Quality and Reliability Standards
Characterized to the Full Military Temperature Range −55°C to +125°C Rated Performance
10 kHz Full Power Bandwidth
Low Nonlinearity: ±0.025% max
Wide Output Range: ±10 V min (Into a 2.5 kΩ Load)
High CMV Isolation: 1500 V RMS Continuous
Isolated Power: ±15 V DC @ ±5 mA
Small Size: 2.23″×0.83″×0.65″
56.6 mm×21.1 mm×16.5 mm
Uncommitted Input Amplifier
Two-Port Isolation Through Transformer Coupling

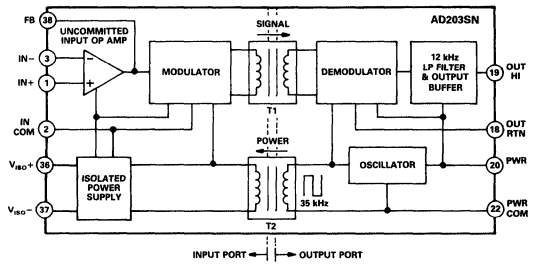
ISOLATION AMPLIFIERS

Provide Galvanic Isolation Between the Input and Output Stages
Eliminate Ground Loops
Reject High Common Mode Voltages and Noise
Protect Sensitive Electronic Signal Processing Systems from Transient and/or Fault Voltages

APPLICATIONS INCLUDE

Engine Monitoring and Control
Mobile Multichannel Data Acquisition Systems
Instrumentation and/or Control Signal Isolation
Current Shunt Measurements
High Voltage Instrumentation Amplifier

AD203SN FUNCTIONAL BLOCK DIAGRAM



mount components and assembly automation have resulted in a rugged, economical, military temperature range isolator that either retains or improves upon the key performance specifications of the AD202/AD204 line.

The AD203SN provides total galvanic isolation between the input and output stages of the isolation amplifier, including the power supplies, through the use of internal transformer coupling. The functionally complete design of the AD203SN, powered by a single +15 V dc supply, eliminates the need for an external dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs. Furthermore, the power consumption, nonlinearity and drift characteristics of transformer coupled devices are vastly superior to those achievable with other isolation technologies, without sacrificing bandwidth or noise performance. Finally, the AD203SN will maintain its high operating performance even under sustained common mode stress.

The design of the AD203SN emphasizes maximum flexibility and ease of use in a broad range of applications where signals must be measured or transmitted under high CMV conditions. The AD203SN has a ±10 V output range, an uncommitted input amplifier, an output buffer, a 10 kHz full power bandwidth and a front-end isolated power supply of ±15 V dc @ ±5 mA.

GENERAL DESCRIPTION

The AD203SN is designed and built expressly for use in hostile operating environments. The AD203SN is also an integral member of Analog Devices' AD200 Series of low cost, high performance, transformer coupled isolation amplifiers. Technological innovations in circuit design, transformer construction, surface

SPECIFICATIONS (typical @ +25°C, V_S = +15 V dc unless noted otherwise)

GAIN	
Range	1 V/V–100 V/V
Error	±1% typ (±4% max)
vs. Temperature[1]	
−55°C to +125°C	50 ppm/°C
−55°C to +25°C	100 ppm/°C
−40°C to +25°C	80 ppm/°C
−25°C to +25°C	60 ppm/°C
+25°C to +125°C	5 ppm/°C
vs. Time	±50 ppm/1000 hours
vs. Supply Voltage	±0.005%/V
Nonlinearity[2], G = 1 V/V, ±10 V Output Swing	±0.012% (±0.025% max)
INPUT VOLTAGE RATINGS	
Linear Differential Range	±10 V
Max CMV Input to Output	
AC, 60 Hz, Continuous	1500 V rms
Continuous (ac and dc)	±2000 V peak
Common Mode Rejection (CMR) @ 60 Hz	
$R_S \leq 100\ \Omega$ (HI & LO Inputs), G = 1 V/V	106dB
G = 100 V/V	120dB
$R_S \leq 1\ k\Omega$ (Input, HI, LO or Both), G = 1–100 V/V	96dB (min)
Leakage Current, Input to Output @ 240 V rms, 60 Hz	4.0μA rms (max)
INPUT IMPEDANCE	
Differential (G = 1 V/V)	$10^{12}\ \Omega$
Common Mode	2 GΩ‖4.5 pF
INPUT BIAS CURRENT	
Initial @ +25°C	30 pA
Current @ +125°C	30 nA
INPUT DIFFERENCE CURRENT	
Initial @ +25°C	±5 pA
Current @ +125°C	±5 nA
INPUT NOISE	
Voltage, 0.1 Hz to 100 Hz	4 μV p–p
Voltage, Frequency > 200 Hz	50 nV/$\sqrt{\text{Hz}}$
FREQUENCY RESPONSE	
Bandwidth ($V_{OUT} \leq 20$ V p–p, G = 1–100 V/V)	10 kHz
Slew Rate	0.5 V/μs
Settling Time to ±0.10%	160 μs
OFFSET VOLTAGE, REFERRED TO INPUT (RTI)	
Initial @ +25°C (Adjustable to Zero)	± (5 + 25/G) mV (max)
vs. Temperature (−55°C to +125°C)	± (6 + 100/G) μV/°C
RATED OUTPUT[3]	
Voltage (Out HI to Out LO) @ R_L = 5.0 kΩ	±10 V (min)
Current	±4 mA
Maximum Capacitive Load[4]	270 pF
Output Resistance	0.2 Ω
Output Ripple, 100 kHz Bandwidth	15 mV p–p
5 kHz Bandwidth	0.7 mV rms
ISOLATED POWER OUTPUT[5]	
Voltage, No Load	±15 V
Accuracy	±5%
Current (Either Output)	5 mA
Regulation, No Load to Full Load	5%
Ripple, 100 kHz Bandwidth, Full Load	110 mV p–p
POWER SUPPLY	
Voltage, Rated Performance	+15 V dc (±5%)
Voltage, Operating Performance[6]	+12 V dc to +16 V dc
Current, No Load (V_S = +15 V dc)	20 mA

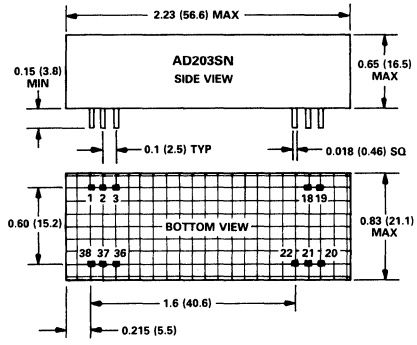
TEMPERATURE RANGE	
Rated Performance	−55°C to +125°C
Storage	−55°C to +125°C
PACKAGE DIMENSIONS	
Inches	2.23 × 0.83 × 0.65
Millimeters	56.6 × 21.1 × 16.5

NOTES
[1]Refer to Figure 1 for a plot of gain versus temperature.
[2]For gains greater than 50 V/V, a 100 pF capacitor from the feedback terminal of the input op amp (Pin 38) to the input common terminal (Pin 2) is recommended in order to minimize the gain nonlinearity. Refer to Figure 17 for a circuit schematic.
[3]For additional information on the Rated Output parameters, refer to Figure 9 for a plot of the Output Voltage Swing vs. Power Supply Voltage, and Figure 10 for the Output Current vs. Temperature and Power Supply Voltage relationship.
[4]For larger capacitive loads, it is recommended that a 4.7 Ω resistor be placed in series with the load in order to suppress possible output oscillations.
[5]1.0 μF (min) decoupling is required.
[6]Refer to Figure 9 for a plot of output voltage swing versus supply voltage.
Specifications subject to change without notice.

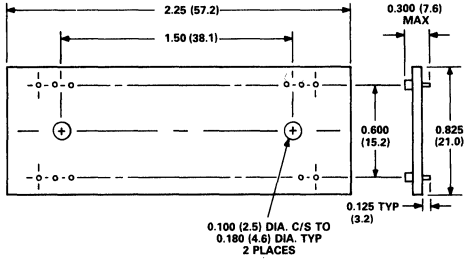
5

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1062 MATING SOCKET



AD203SN PIN DESIGNATIONS

PIN	DESIGNATION	FUNCTION	PORT
1	IN+	INPUT OP AMP: NONINVERTING INPUT	INPUT
2	IN COM	INPUT COMMON	INPUT
3	IN−	INPUT OP AMP: INVERTING INPUT	INPUT
18	OUT RTN	OUTPUT RETURN	OUTPUT
19	OUT HI	OUTPUT SIGNAL	OUTPUT
20	PWR IN	DC POWER SUPPLY INPUT	OUTPUT
21	NONE	NONE	–
22	PWR COM	DC POWER SUPPLY COMMON	OUTPUT
36	V_{ISO}+	ISOLATED POWER: +DC	INPUT
37	V_{ISO}−	ISOLATED POWER: −DC	INPUT
38	FB	INPUT OP AMP: OUTPUT/FEEDBACK	INPUT

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be discharged to the destination socket before devices are removed.

Note: Per MIL-STD-883C, Method 3015, this device have been classified as a Category 2 ESD sensitive device.

PRODUCT HIGHLIGHTS

Rugged Design. The AD203SN is specifically designed for applications where ruggedness and high performance are the key requirements. The ruggedness of the AD203SN design meets MIL-STD-883C Methods 1004 (Moisture Resistance), 1010 Condition B (Temperature Cycling, −55°C to +125°C), 2002 Condition B (Mechanical Shock @ 1,500 g for 0.5 ms), 2004 (Lead Integrity), 2007 Condition A (Variable Frequency Vibration @ 20 g) and 2015 (Resistance to Solvents).

Engine and vehicular monitor/control systems as well as mobile instrumentation and control systems are some examples of applications for which the AD203SN is well suited.

Military Temperature Range Rating. With its performance rated over the −55°C to +125°C MIL specification temperature range, the AD203SN is an excellent choice in applications where severe environmental conditions may be encountered. Examples include engine monitoring/control systems and remote power line monitoring.

10 kHz Bandwidth. With a full power bandwidth of 10 kHz, the AD203SN is effective in control loop applications where a smaller bandwidth could induce control system instabilities.

Excellent Common Mode Performance. The AD203SN provides a 1.5 kV rms continuous common mode isolation. A low common mode input capacitance of 4.5 pF, inclusive of power isolation, results in a minimum 96 dB of CMR as well as a very low leakage current of 4.0 μA rms (max @ 240 V rms, 60 Hz).

High Accuracy. Exhibiting a maximum nonlinearity of ±0.025% and a low gain temperature coefficient, averaging 50 ppm/°C over the full temperature range, the AD203SN provides high isolation without loss of signal integrity and quality.

Isolated Power. An isolated power supply capable of delivering ±15 V dc @ ±5 mA is available at the input port of the isolator. This permits the AD203SN to power up floating signal conditioners, front-end amplifiers or remote transducers at the input.

Flexible Input Stage. An uncommitted op amp is provided on the input stage. This amplifier provides input buffering and gain as needed. It also facilitates a host of alternative input functions including filtering, summing, high voltage ranges and current (transimpedance) inputs.

DESCRIPTION OF KEY SPECIFICATIONS

Gain Nonlinearity. Nonlinearity is defined as the peak deviation of the output voltage from the best straight line and is expressed as a percent of peak-to-peak output voltage span. The nonlinearity of the model AD203SN, which operates at a 20 V p–p output span, is ±0.025% or ±5 mV. Good nonlinearity is critical for retaining signal fidelity.

Max CMV, Input to Output. Maximum common mode voltage (CMV) describes the amount of voltage that may be applied across both input terminals with respect to the output terminals without degrading the integrity of the isolation barrier. High input-to-output CMV capability is necessary in applications where high CMV inputs exist or high voltage transients may occur at the input.

Common Mode Rejection (CMR). CMR describes the isolator's ability to reject common mode voltages that may exist between the inputs and the outputs. High CMR is required when it is necessary to process small signals riding on high common mode voltages.

Leakage Current. This is the current that flows from the input common across the isolation barrier to the output common when the power-line voltage (either 115 V or 240 V rms, 60 Hz) is impressed on the inputs. Leakage current is dependent on the magnitude of the coupling capacitance between the input and the output ports. Line frequency leakage current levels are unaffected by the power ON or OFF condition of the AD203SN.

Common Mode Input Impedance. This is defined to be the impedance seen across either input terminal (i.e., +IN or −IN) and the input common.

Input Noise. This specification characterizes the voltage noise levels that are generated internally by the isolation amplifier. In order to facilitate a comparison between the "isolator background noise" levels and the expected input signal levels the input noise parameter is referred to the input.

Input noise is a function of the noise bandwidth, i.e., the frequency range over which the noise characteristics are measured.

Offset Voltage, Referred to Input (RTI). The offset voltage describes the isolation amplifier's total dc offset voltage with the inputs grounded. The offset voltage is referred to the input in order to allow for a comparison of the dc offset voltages with the expected input signal levels. The total offset comes from two sources, namely from the input and output stages, and is gain dependent. To compute the offset voltage, RTI, the isolator is modelled as two cascaded amplifier stages. The input stage has a variable gain G while the output isolation stage has a fixed gain of 1. RTI offset is then given by:

$$E_{OS}\,(RTI) = E_{OS1} + E_{OS2}/G$$

where:

E_{OS1} = Total input stage offset voltage

E_{OS2} = Output stage offset voltage

G = Input stage gain.

Offset voltage drift, RTI, is calculated in an identical manner.

Isolated Power Output. Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input signal conditioners as well as remote transducers.

PERFORMANCE CHARACTERISTICS

This section details the key specifications of the AD203SN that exhibit a functional dependence on such variables as frequency, power supply load, output voltage swing, bypass capacitance and temperature. Table I summarizes the performance characteristics that will be discussed in this section. For the sake of completeness, a typical dynamic output response of the AD203SN is included.

Gain Temperature Coefficient. Figure 1 presents the AD203SN's gain temperature coefficient over the entire −55°C to +125°C temperature range.

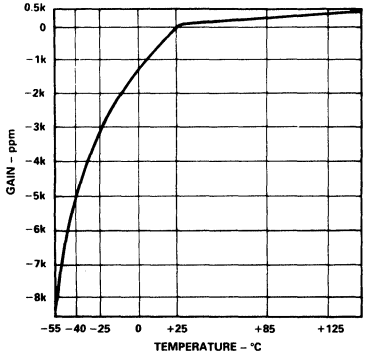


Figure 1. Gain (ppm of Span) vs. Temperature (°C)

Note: 1 ppm (part per million) is equivalent to 0.0001%.

Gain Nonlinearity. The maximum nonlinearity error of the AD203SN, at a gain of 1 V/V, is specified as ±0.025% or ±5 mV. The nonlinearity performance of the AD203SN is dependent on the output voltage swing and this dependency is illustrated in Figure 2. The horizontal axis represents the gain error, expressed either in percent of peak-to-peak output span (i.e., % of 20 V) on the left axis or in mV on the right axis. The vertical axis indicates the magnitude of the output voltage swing.

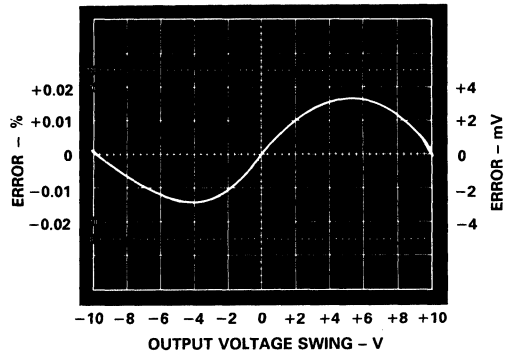


Figure 2. Gain Nonlinearity Error (% p–p Output Range and mV) vs. Output Voltage Swing (V), with a Gain of 1 V/V

Parameter	Key Specifications	As a Function of	Shown In
Gain	Gain (ppm of Span) Gain Nonlinearity (Expressed in mV and % of p–p Output)	Temperature (°C) Output Voltage Swing (V)	Figure 1 Figure 2
Input Voltage Rating	Common Mode Rejection (dB)	Common Mode Signal Frequency (Hz), Amplifier Gain (V/V) and Input Source Resistance (Ω)	Figure 3
Input Noise	Input Noise (nV/$\sqrt{\text{Hz}}$)	Frequency (Hz)	Figure 4
Frequency Response	Frequency Response: Gain (dB) Frequency Response: Phase Shift (Degree) Dynamic Response	Frequency (Hz) Frequency (Hz) N/A	Figure 5 Figure 6 Figure 7
Offset	Output Offset Voltage (mV)	Temperature (°C)	Figure 8
Rated Out	Output Voltage Swing (V) Output Current (mA)	Supply Voltage (V dc) Supply Voltage (V dc)	Figure 9 Figure 10
Isolated Power Supply	Isolated Power Supply Voltage (V) Isolated Power Supply Ripple (mV p–p) Isolated Power Supply Ripple (V p–p)	Current Delivered to the Load (mA) Current Delivered to the Load (mA) Bypass Capacitance (μF)	Figure 11 Figure 12 Figure 13

Table I. Performance Characteristics Detailed in the AD203SN Data Sheet

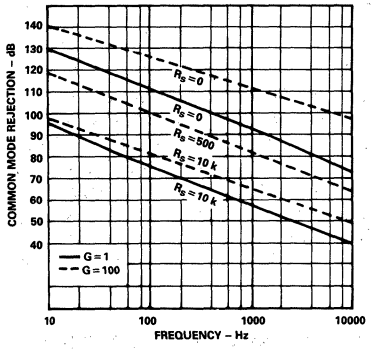


Figure 3. Common Mode Rejection (CMR) vs. Frequency (Hz), Gain (V/V) and Resistance (Ω)

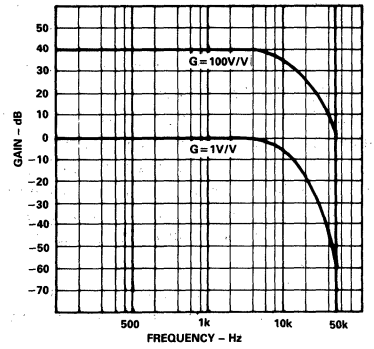


Figure 5. Gain (dB) as a Function of Frequency (Hz)

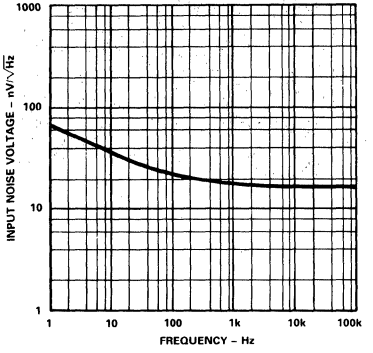


Figure 4. Input Noise (nV/$\sqrt{Hz}$) vs. Frequency (Hz)

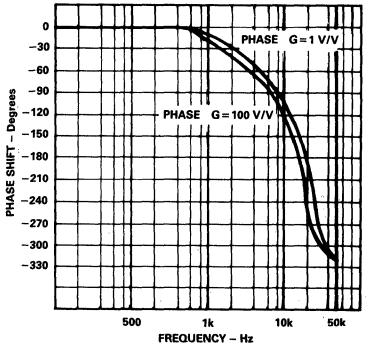


Figure 6. Phase Shift (Δ°) as a Function of Frequency (Hz)

Common Mode Rejection. Figure 3 illustrates the common mode rejection (CMR), expressed in dB, of the AD203SN versus frequency (Hz), gain (V/V) and source impedance imbalance (Ω). To achieve the optimal common mode rejection of unwanted signals, it is recommended that the source imbalance be kept as low as possible and that the input circuitry be carefully laid out so as to avoid adding excessive stray capacitances at the isolator's input terminals.

Input Noise. Figure 4 presents the typical input noise characteristics, in nV/$\sqrt{Hz}$, of the AD203SN for a frequency range from 1 Hz to 100 kHz.

Frequency Response: Gain and Phase Shift. Figure 5 illustrates the AD203SN's gain as a function of frequency while Figure 6 illustrates the corresponding phase shift vs. frequency. The AD203SN's low phase shift and 10 kHz bandwidth performance make it ideal in power monitoring and control system applications.

Dynamic Response of the AD203SN. To illustrate the speed, dynamic range and rapid settling time of the AD203SN, the isolator's output response to a 20 V p–p step function is shown in Figure 7.

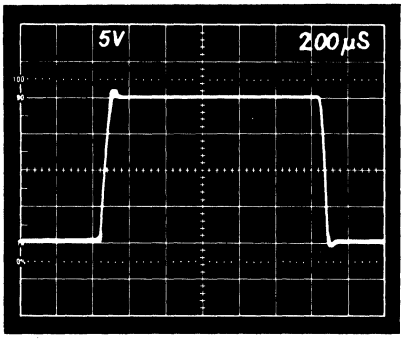


Figure 7. Dynamic Response of the AD203SN (20 V p–p Step)

Output Offset Voltage. The AD203SN exhibits a low output offset voltage temperature coefficient over the +25°C to +125°C temperature range as shown in Figure 8.

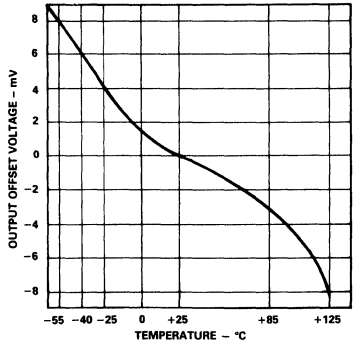


Figure 8. Output Offset Voltage (mV) vs. Temperature (°C) with G=1 V/V

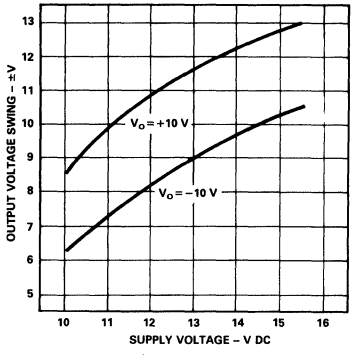


Figure 9. Output Voltage Swing (±V) vs. Power Supply Input Voltage (V DC), with a 2.5 kΩ Load

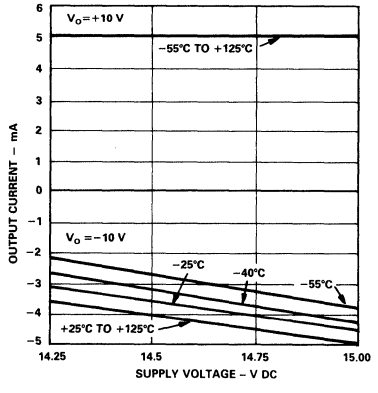


Figure 10. Output Current (mA) vs. Supply Voltage (V DC) and Temperature (°C), with V_{ISO} Loaded at 5 mA

Rated Output. The rated output voltage, across the OUT HI and OUT LO terminals, for the AD203SN is specified at ±10 V. This specification applies when the AD203SN is powered by a +15 V dc supply. The rated output voltage level is, however, affected by the input power supply voltage and the loads placed on the isolated power supply. This dependency is illustrated in Figure 9.

The current delivered by the output terminals of the AD203SN will vary as a function of the supply voltage and operating temperature. These relationships are illustrated in Figure 10.

Isolated Power. The load characteristics of the AD203SN's isolated power supplies (i.e., +15 V dc and −15 V dc) are plotted in Figure 11.

The isolated power supply exhibits some ripple which varies as a function of the load current. Figure 12 demonstrates this relationship. The AD203SN has internal bypass capacitors that optimize the tradeoff between output ripple and power supply performance, even under full load. If a specific application requires more bypassing on the isolated power supplies, external capacitors may be added. Figure 13 plots the isolated power supply ripple as a function of external bypass capacitance under full load conditions (i.e., 5 mA).

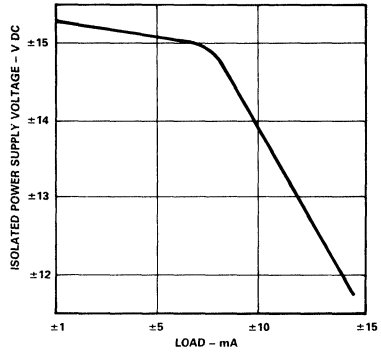


Figure 11. Isolated Power Supply Voltage (V DC) vs. Load (mA)

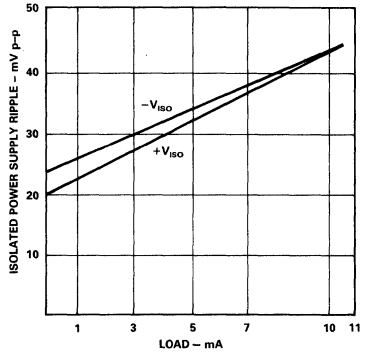


Figure 12. Isolated Power Supply Ripple (mV p–p) vs. Load (mA)

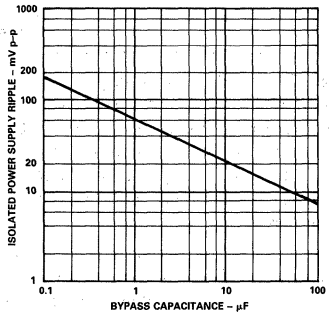


Figure 13. Isolated Power Supply Ripple (mV p–p) vs. Bypass Capacitance (µF), with a 5 mA Load on $\pm V_{ISO}$, and Noise Bandwidth of 1 MHz.

The curves in Figures 12 and 13 were generated by measuring the power supply ripple over a 1 MHz bandwidth.

CAUTION: The AD203SN does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICABLE STANDARDS

The tests and methods employed in the design verification process are summarized in Table II. A copy of the *AD203SN Quality & Reliability Summaries* test report, which documents the results of the tests listed in Table II, is available on request.

Test Method	Test Description
MIL-STD-883C, Method 1004	Moisture Resistance
MIL-STD-883C, Method 1010 Condition B	Temperature Cycling, −55°C to +125°C
MIL-STD-883C, Method 2002, Condition B	Mechanical Shock @ 1,500 g for 0.5 ms
MIL-STD-883C, Method 2003	Solderability of Terminations
MIL-STD-883C, Method 2004	Integrity of Microelectronic Device Leads
MIL-STD-883C, Method 2007, Condition A	Variable Frequency Vibration @ 20 g
MIL-STD-883C, Method 2015	Resistance to Solvents
MIL-STD-883C, Method 3015.5	Electrostatic Discharge Sensitivity Classification
Analog Devices Product Reliability Program	MTBF Calculation (per MIL-HDBK-217D) and Verification

Table II. Tests Used to Verify the Ruggedness, Reliability and Quality of the AD203SN Design

Per 883C Method 3015.5, the AD203SN has been classified as a Class 2 ESD (electrostatic discharge) sensitive device. As a Class 2 device, the AD203SN is insensitive to static discharge voltages of less than 2000 V.

INSIDE THE AD203SN

The functional block diagram of the AD203SN is shown in Figure 14. The AD203SN employs amplitude modulation techniques to implement transformer coupling of signals down to dc. The 35 kHz, 30 V p–p square wave carrier used by the AD203SN is generated by an internal oscillator located in the output port of the isolator. This oscillator is powered by a +15 V dc supply.

A full wave modulator translates the input signal to the carrier frequency which is then transmitted across transformer T1. The synchronous demodulator in the output port extracts the input signal from the carrier. The 12 kHz two-pole filter is employed to minimize output noise and ripple. Furthermore, the filter serves as a low impedance output buffer.

The input port of the AD203SN contains an uncommitted input op amp, a modulator and the power transformer T2. The primary of the power transformer is driven by the 35 kHz square wave while the secondary, in conjunction with a rectifier network, supplies isolated power to the modulator, input op amp and any external load. The uncommitted input amplifier can be used to supply gain or to buffer the input signals.

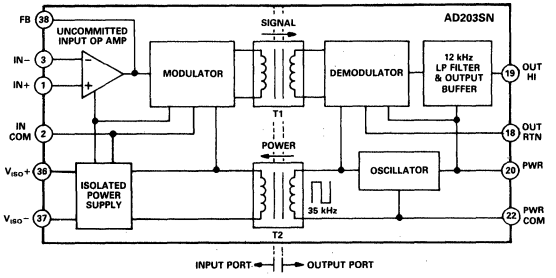


Figure 14. Functional Block Diagram

USING THE AD203SN

Powering the AD203SN. The AD203SN requires only a single +15 V dc power supply connected as shown in Figure 15. A bypass capacitor is provided in the module.

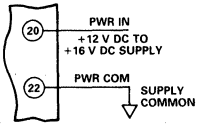


Figure 15. Powering the AD203SN

Unity Gain Input Configuration. The basic unity gain configuration for input signals of up to ±10 V is shown in Figure 16.

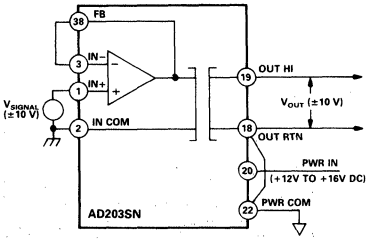


Figure 16. Basic Unity Gain Configuration

Input Configuration for a Gain Greater Than 1 (G>1). When small input signal levels must be amplified and isolated, Figure 17 shows how to get a gain greater than 1 while continuing to preserve a very high input impedance.

In this circuit, the gain equation may be written as:

$$V_O = (1 + R_F/R_G) \times V_{SIG}$$

where

V_O = Output Voltage (V)
V_{SIG} = Input Signal Voltage (V)
R_F = Feedback Resistor Value (Ω)
R_G = Gain Resistor Value (Ω).

Note on the 100 pF Capacitor. Whenever a gain of 50 V/V or greater is required, a 100 pF capacitor from the FB (input op amp feedback) terminal to the IN COM (input common) terminal, as shown with the dotted lines in Figure 17, is highly recommended. The capacitor acts to filter out switching noise and will minimize the isolator's nonlinearity parameter.

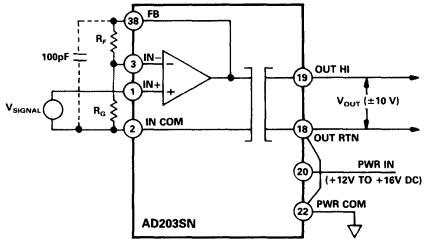


Figure 17. Input Configuration for a Gain Greater than 1

Compensating the Uncommitted Input Op Amp. The open loop gain and phase versus frequency for the uncommitted input op amp are given in Figure 18. These curves are to be used to determine the appropriate values for the feedback resistor and compensation capacitor in order to ensure frequency stability when a gain greater than unity is required. The final values for these components should also be chosen so as to satisfy the following constraints:

- The current drawn in the feedback resistor (R_F) is no greater than 1 mA.
- The feedback (R_F) and gain resistor (R_G) result in the desired amplifier gain.

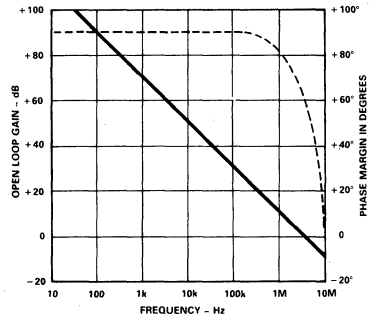


Figure 18. Open Loop Gain and Phase vs. Frequency for the Uncommitted Input Op Amp

Inverting, Summing or Current Input Configuration. Figure 19 shows how the AD203SN can accommodate current inputs or sum currents or voltages.

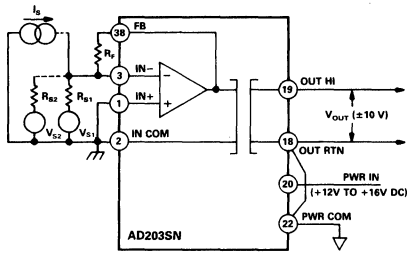


Figure 19. Input Configuration for Summing or Current Input

In this circuit the output voltage equation can be written as:

$$V_O = -R_F \times (I_S + V_{S1}/R_{S1} + V_{S2}/R_{S2} + \ldots)$$

where

V_O = Output Voltage (V)
V_{S1} = Voltage of Input Signal 1 (V)
V_{S2} = Voltage of Input Signal 2 (V)
I_S = Input Current Source (A)
R_F = Feedback Resistor Value (Ω)
Source Resistance Associated with Input
R_{S1} = Signal 1 (Ω)
Source Resistance Associated with Input
R_{S2} = Signal 2 (Ω).

The circuit of Figure 19 can also be used when the input signal is larger than the ±10 V input range of the isolator. For example, suppose that in Figure 19 only V_{S1}, R_{S1} and R_F are connected to the feedback, input and common terminals as shown by the solid lines in Figure 19. Now, a V_{S1} with a ±100 V span can be accommodated with $R_F = 20$ kΩ and a total $R_{S1} = 200$ kΩ.

GAIN AND OFFSET ADJUSTMENTS

General Comments. When gain and offset adjustments are required, the actual compensation circuit ultimately utilized will depend on:

- The input configuration mode of the isolation amplifier (i.e., noninverting or inverting).
- The placement of the adjusting potentiometer (i.e., on the isolator's input or output side).

As a general rule:

- Offset adjustments are best accomplished on the isolator's input side, as it is much easier and more efficient to null the offset ahead of any gain.
- Gain adjustments are mostly easily accomplished as part of the gain-setting resistor network at the isolator's input side.
- Input adjustments, of the offset and/or gain, are preferred when the adjusting potentiometers are as near as possible to the input end of the isolator (so as to minimize strays).
- Output side adjustments may be necessary under the conditions where adjusting potentiometers placed on the input side would present a hazard to the user due to the presence of high common mode voltages during the adjustment procedure.

- It is recommended that the offset adjustment precedes the gain adjustment.

Adjustments for the Noninverting Mode of Operation

Offset Adjustment. Figure 20 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the noninverting mode of operation. The offset adjustment circuit injects a small voltage in series with the low side of the signal source. The adjustment potentiometer P1 modulates the injection voltage and is therefore responsible for nulling out the offset voltage.

Note:
- To minimize CMR degradation it is recommended that the resistor in series with the input LO (i.e., R_C) be below a few hundred ohms.
- The offset adjustment circuit of Figure 20 will not work if the signal source has another current path to input common, or if current flows in the signal source LO lead. If this is the case, use the output adjustment procedure.

Gain Adjustment. Figure 20 also shows the suggested gain adjustment circuit. Note that the gain adjustment potentiometer P2 is incorporated into the gain-setting resistor network at the isolator's input.

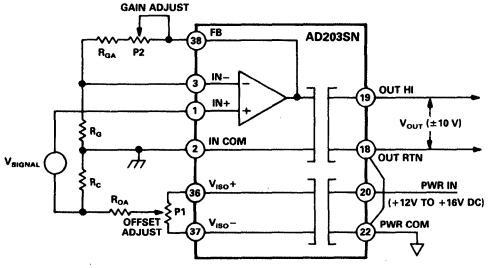


Figure 20. Input Adjustments for the Noninverting Mode of Operation

An R_{GA} of 47.5 kΩ and a 5 kΩ potentiometer, resulting in a median R_F value of 50 kΩ (i.e., R_{GA} + P2/2), will work nicely for gains of 10 V/V or greater. The gain adjustment becomes less effective at lower gains, in fact it is halved at G=2 V/V, so that potentiometer P2 will have to be a larger fraction of the total R_F. At a gain of 1 V/V attempting to adjust the gain downwards will compromise the isolator's input impedance. In this case it would be better to adjust the gain at the signal source or after the output.

Input Adjustments for the Inverting Mode of Operation

Offset Adjustment. Figure 21 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the inverting mode of operation. Here the offset adjustment potentiometer P1 nulls the voltage at the summing node. This method is preferred over current injection since it is less affected by any subsequent gain adjustments.

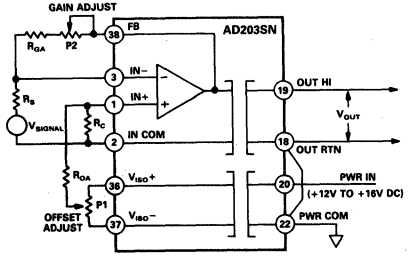


Figure 21. Input Adjustments for the Inverting Mode of Operation

Gain Adjustment. Figure 21 also shows the suggested gain adjustment circuit. In this circuit, the gain adjustment is made in the feedback loop using potentiometer P2. The adjustments will be effective for all gains in the 1 to 100 V/V range.

Output Adjustments

Offset Adjustment. Figure 22 shows the recommended technique for offset adjustment at the output. In this circuit, the ±15 V dc voltage is supplied by an independent source. With reference to the output circuitry shown in Figure 22, the maximum offset adjustment range is given by:

$$E_{OFFSET} = \frac{R_D \times V_S}{R_D + R_O}$$

where, V_S is the power supply voltage. A 20 kΩ potentiometer (P_O) should work well in this adjustment circuit.

Gain Adjustment. Since the AD203SN's output amplifier is fixed at unity, any desired output gain adjustments can only be made in a subsequent stage.

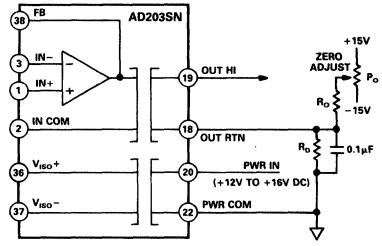


Figure 22. Output Side Offset Adjustment Circuit

USING ISOLATED POWER

The AD203SN provides ±15 V dc power outputs referred to the input common. These may be used to power various accessory circuits which must operate at the input common mode level. The input offset adjustment circuits of the previous section are examples of this need.

The isolated power supply output has a current capacity of 5 mA which should be sufficient to operate adjustment circuits, references, op amps, signal conditioners and remote transducers.

CAUTION: The AD203SN does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICATIONS EXAMPLES

Isolated Process Current to Voltage Converter

Figure 23 shows how the AD203SN can be utilized as an isolated receiver that translates a 4-20 mA process current signal input into a 0 to +10 V output. The 25 Ω shunt resistor converts the 4-20 mA current into a +100 to +500 mV signal. The signal is then offset by −100 mV via the use of P_O to produce a 0 to +400 mV input. The signal is then amplified by a gain of 25 resulting in the desired 0 to +10 V output. With an open circuit on the input side, the AD203SN will have −2.5 V on the output, corresponding to the −100 mV offset voltage multiplied by a gain of 25 V/V.

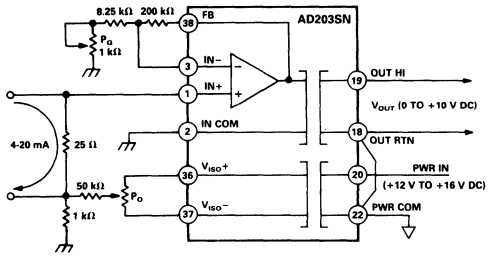


Figure 23. Using the AD203SN as an Isolated Process Current to Voltage Converter

For the circuit of Figure 23, the input to output transfer function can be expressed as:

$$V_{OUT} = 625 \times I_{IN} - 2.5\ V$$

where

V_{OUT} = Output Voltage (V)
I_{IN} = Input Current in milliamps (mA). This current is limited to the 4 to 20 mA range.

Current Shunt Measurements

In addition to isolating and converting process current signals into voltage signals, the AD203SN can be used to indicate the value of any loop current in general. Figure 24 illustrates a typical current shunt measurement application of the AD203SN. A small sensing resistor R_{SHUNT}, placed in series with the current loop, develops a small differential voltage that may be further scaled to provide an isolator output voltage that is directly proportional to the current. The voltage developed across the shunt can potentially be several hundred to a thousand volts above ground. In this circuit, the AD203SN provides the necessary scaling of the shunt signal while providing high common-mode voltage isolation and high common mode rejection of dc and 60 Hz components.

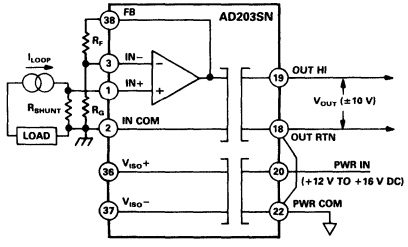


Figure 24. Using the AD203SN for Current Shunt Measurements

The transfer function for the circuit of Figure 24 can be written as:

$$V_{OUT} = R_{SHUNT} \times (1 + R_F/R_G) \times I_{LOOP}$$

where

V_{OUT} = Output Voltage (V)
R_{SHUNT} = Sense or Current Shunt Resistance (Ω)
R_F = Feedback Resistance (Ω)
R_G = Gain Resistance (Ω)
I_{LOOP} = Loop Current (A).

Low Level Inputs

In applications where low level signals need to be isolated (thermocouples are one such application), a low drift input amplifier can be used with the AD203SN. Figure 25 illustrates this implementation of the AD203SN. The circuit design also includes a three-pole active filter which provides for enhanced common mode rejection at 60 Hz and normal mode rejection of frequencies above a few Hz. If any offset adjustments are desired, they are best done at the trim pins of the low drift input amplifier. Gain adjustments can be done at the feedback resistor.

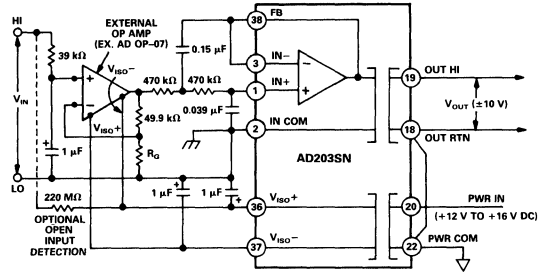


Figure 25. Using the AD203SN with Low Level Inputs

The input-output relationship for the circuit shown in Figure 25 can be written as:

$$V_{OUT} = V_{IN} \times (1 + 50\ k\Omega/R_G)$$

where

V_{OUT} = Output Voltage (V)
V_{IN} = Low Level Input Voltage (V)
R_G = Isolation Amplifier Gain Resistance (Ω).

Noise Reduction in Data Acquisition Systems

The AD203SN uses amplitude modulation techniques with a 35 kHz carrier to pass both ac and dc signals across the isolation barrier. Some of the carrier's harmonics are unavoidably passed through to the isolator output in the form of ripple. In most cases, this noise source is insignificant when compared to the measured signal. However, in some applications, particularly when a fast A/D converter is used following the isolator, it may be desirable to add filtering at the isolator's output in order to reduce the carrier ripple. Figure 26 shows a circuit that will reduce the carrier ripple through the use of a two-pole output filter.

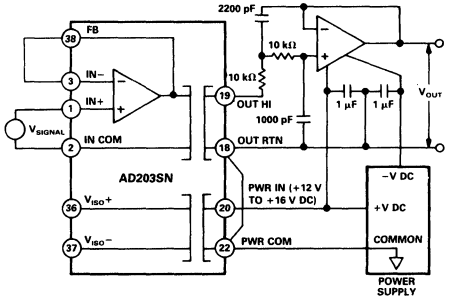


Figure 26. Noise Reduction in Data Acquisition Systems Using the AD203SN

ANALOG DEVICES

100 kHz Bandwidth, Low Distortion, Internally Powered Isolation Amplifier

AD206

FEATURES
Wide Bandwidth: 100 kHz, min (Full Signal)
Rapid Slew Rate: 6 V/μs
Fast Settling Time: 12 μs, max
Low Harmonic Distortion: −80 dB @ 1 kHz
Low Nonlinearity: ±0.005%
Wide Output Range: ±10 V
High CMV Isolation: 1.5 kV RMS, min
Buffered Output
Isolated Power: ±15 V DC @ ±10 mA
Performance Rated over the −40°C to +85°C Temperature Range

APPLICATIONS INCLUDE
High Speed Data Acquisition Systems
Transient Monitoring
Power Line Monitoring
Motor Control
Vibration Analysis

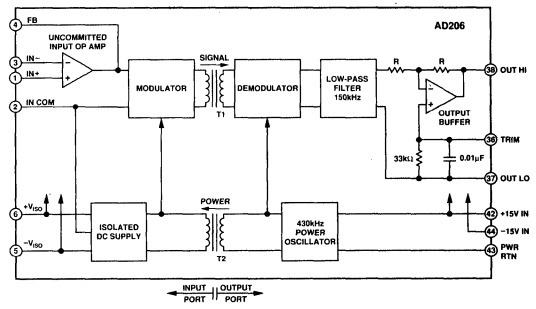
GENERAL DESCRIPTION

The AD206 is a high precision, two-port, transformer-coupled isolation amplifier expressly designed for applications that require the amplification and isolation of extremely fast analog signals. The innovative circuit and transformer design of the AD206 ensures the wideband dynamic characteristics of the AD206 while preserving the key dc performance specifications.

The AD206 provides total galvanic isolation between the input and output stages of the isolation amplifier, including the power supplies, through the use of internal transformer coupling. The functionally complete design of the AD206, powered by a bipolar ±15 V dc supply, eliminates the need for a user supplied dc/dc converter or power oscillator. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD206 emphasizes maximum flexibility and ease of use in a broad range of applications where rapidly varying analog signals must be measured and transmitted under high CMV conditions. The AD206 has a ±10 V output range, a specified gain range of 1 to 10, a buffered output and a front-end power supply of ±15 V dc with ±10 mA of current drive capability.

AD206 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

High Speed Dynamic Characteristics: The AD206 features a minimum full-signal bandwidth of 100 kHz, a typical slew rate of 6 V/μs and a maximum settling time of 12 μs. The high speed performance of the AD206 allows for the amplification and isolation of dynamic signals.

Flexible Input and Buffered Output Stages: An uncommitted op amp is provided on the input stage of the AD206. This allows for input buffering and gain as needed. The AD206 also features a buffered output stage, allowing it to drive low impedance loads.

High Accuracy: Exhibiting a typical nonlinearity of ±0.005% of full-scale range and a total harmonic distortion of −80 dB (typical @ 1 kHz), the AD206 provides high isolation without loss of signal integrity and quality.

Excellent Common-Mode Performance: The AD206BY (AD206AY) provides 1.5 kV rms (0.75 kV rms) of common-mode protection. Both grades feature a low common-mode capacitance of 4.5 pF, inclusive of power isolation, resulting in a typical common-mode rejection specification of 105 dB (1 kΩ source impedance imbalance) as well as a low leakage current of 2.0 μA rms (max @ 240 V rms, 60 Hz).

Isolated Power: An unregulated isolated ±15 V dc power supply with ±10 mA of current drive capability is available at the input port of the AD206. This permits the isolator to power up floating signal conditioners, front-end amplifiers or remote transducers at the input.

Performance Rated over the −40°C to +85°C Temperature Range: With an extended industrial temperature range rating, the AD206 is an ideal isolation amplifier for use in industrial environments.

SPECIFICATIONS (typical @ +25°C, V_S = ±15 V dc, 2 kΩ output load, unless noted otherwise)

	AD206A	AD206B
GAIN		
Range[1]	1 V/V to 10 V/V	*
Error	−0.5% (±2%, max)	*
vs. Temperature[2]		
0 to +85°C	+15 ppm/°C (+55 ppm/°C, max)	*
−40°C to 0°C	+50 ppm/°C (+100 ppm/°C, max)	*
vs. Supply Voltage, ± (14.5 V to 16.5 V dc)	100 ppm/V	*
vs. Isolated Supply Load[3]	20 ppm/mA	*
Nonlinearity,[4] ±10 V Output Swing, G = 1	±0.005%, (±0.015%, max)	*
G = 10	±0.01%	*
INPUT VOLTAGE RATINGS		
Linear Differential Range	±10 V, min	*
Max Safe Input Voltage, IN+/IN− to IN COM	±15 V	*
Max CMV Input to Output		
AC, 60 Hz, Continuous	750 V RMS	1500 V RMS
Continuous (AC & DC)	±1000 V_{PEAK}	±2000 V_{PEAK}
Common-Mode Rejection (CMR) @ 60 Hz		
R_S ≤ 100 Ω (HI & LO Inputs), G = 1 V/V	120 dB (110 dB, min)	*
R_S ≤ 1 kΩ (Input, HI, LO or Both), G = 1 V/V	105 dB	*
Common-Mode Rejection (CMR) @ 1 kHz		
R_S ≤ 100 Ω (HI & LO Inputs), G = 1 V/V	100 dB	*
R_S ≤ 1 kΩ (Input, HI, LO or Both), G = 1 V/V	85 dB	*
Common-Mode Rejection (CMR) @ 10 kHz		
R_S ≤ 100 Ω (HI & LO Inputs), G = 1 V/V	80 dB	*
R_S ≤ 1 kΩ (Input, HI, LO or Both), G = 1 V/V	65 dB	*
Leakage Current, Input to Output,		
@ 240 V RMS, 60 Hz	2 μA RMS, max	*
INPUT IMPEDANCE		
Differential (G = 1 V/V)	16 MΩ	*
Common Mode	2 GΩ‖4.5 pF	*
INPUT OFFSET VOLTAGE		
Initial @ +25°C	±400 μV (±2 mV, max)	*
vs. Temperature		
0 to +85°C	±2 μV/°C (±15 μV/°C, max)	*
−40°C to 0°C	±20 μV/°C	*
OUTPUT OFFSET VOLTAGE		
Initial @ +25°C (Adjustable to Zero)	−35 mV (0 to −65 mV, max)	*
vs. Temperature		
0 to +85°C	±30 μV/°C (±65 μV/°C, max)	*
−40°C to 0°C	±80 μV/°C	*
vs. Supply Voltage	±350 μV/V	*
vs. Isolated Supply Load[3]	−35 μV/mA	*
INPUT BIAS CURRENT		
Initial @ +25°C	300 nA (650 nA, max)	*
vs. Temperature		
−40°C to +85°C	±800 nA, max	*
INPUT DIFFERENCE CURRENT		
Initial @ +25°C	3 nA (±65 nA, max)	*
vs. Temperature		
−40°C to +85°C	300 nA, max	*
INPUT VOLTAGE NOISE		
Frequency > 10 Hz	20 nV/$\sqrt{Hz}$	*
FREQUENCY RESPONSE (2 kΩ load)		
Full Signal Bandwidth (3 dB Corner, G = 1 V/V, 20 V pk-pk Signal)	110 kHz (100 kHz, min)	*
Small Signal Bandwidth (3 dB Corner, G = 1 V/V, 100 mV pk-pk Signal)	115 kHz	*

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	AD206A	AD206B
GAIN		
Transport Delay	2.2 μs[5]	*
Slew Rate	6 V/μs	*
Rise Time (10% to 90%)	3 μs	*
Settling Time to ±0.10% on a 10 V Step	12 μs, max	*
Overshoot	0.5%	*
Harmonic Distortion Components, @ 1 kHz	−80 dB	*
@ 10 kHz	−65 dB	*
Unity Gain Overload Recovery (±15 V Drive)	5 μs	*
Output Overload Recovery Time (G > 5 V/V)	10 μs	*
RATED OUTPUT		
Voltage (Out HI to Out LO)	±10 V	*
Current	±5 mA, min (into 2 kΩ Load)	*
Maximum Capacitive Load	1,000 pF	*
Output Resistance	1 Ω, max	*
Output Ripple[6]		
1 MHz Bandwidth	10 mV pk–pk	*
50 kHz Bandwidth	2.5 mV pk–pk	*
ISOLATED POWER OUTPUT		
Voltage, No Load	±15 V	*
vs. Temperature		
0 to +85°C	+20 mV/°C	*
−40°C to 0°C	+25 mV/°C	*
Accuracy	−5%, +10%	*
Current with Rated Supply Voltage Range[3, 7]	±10 mA	*
Regulation, No Load to Full Load	−90 mV/mA	*
Line Regulation	290 mV/V	*
Ripple, 1 MHz Bandwidth, No Load[3]	50 mV RMS	*
Efficiency	75%	*
POWER SUPPLY		
Supply Voltage for Rated Performance	±14.5 V DC to ±16.5 V DC	*
Voltage, Operating[8]	±14.25 V DC to ±17 V DC	*
Current, Quiescent	+40 mA/−15 mA	*
TEMPERATURE RANGE		
Rated Performance	−40°C to +85°C	*
Storage	−40°C to +85°C	*
PACKAGE DIMENSIONS		
SIP Package	2.475″ × 0.3250″ × 0.840″, max	*
	62.9 mm × 8.3 mm × 21.3 mm, max	*

NOTES

[1]Although the gain range of the AD206 is specified to be 1 to 10 V/V, the AD206 can accommodate gains of up to 100 V/V. With a gain of 100 V/V there will be a 20% reduction in the 3 dB bandwidth specification, and the nonlinearity will degrade to ±0.02% (typ). Refer to Figure 12 for a description on how to implement a gain of 100 using the AD206.

[2]The gain temperature coefficient for the AD206 is plotted over the entire −40°C to +85°C rated performance temperature range in Figure 1.

[3]When the isolated supply load exceeds ±1 mA, external filter capacitors will be required in order to ensure that the gain, offset and nonlinearity specifications will be preserved and to keep the isolated supply full load ripple below the specified 50 mV rms. A value of 6.8 μF is recommended.

[4]Nonlinearity is specified as a percent (of full-scale range) deviation from a best straight line.

[5]Equivalent to a 0.8° phase shift at 1 kHz.

[6]With the ±15 V dc power supply pins bypassed by 2.2 μF capacitors at the AD206 pins.

[7]With an input power supply voltage greater than or equal to ±15 V dc the AD206 may supply up to ±15 mA of current from the isolated power supplies. Exceeding these currents will increase the dependence of the gain and offset specifications of the AD206 on both the supply voltage and isolated load current.

[8]Voltages less than 14.25 V dc may cause the AD206 to cease operating properly. Voltages greater than 17.5 V dc may damage the internal components of the AD206 and consequently should not be used.

*Specification is the same as that for the AD206A.

Specifications subject to change without notice.

AD206 PIN DESIGNATIONS

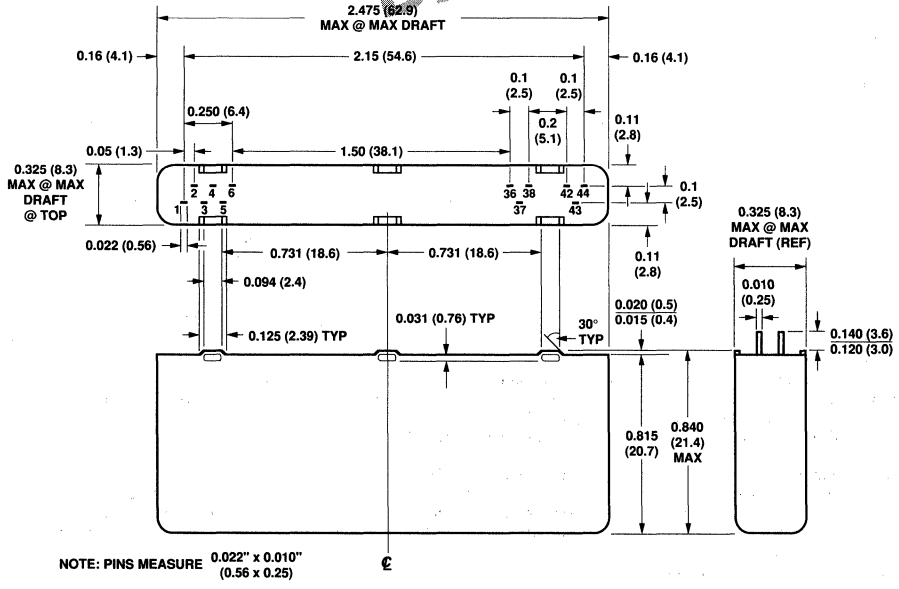
Pin	Designation	Function
1	IN+	Input Op Amp: Noninverting Input
2	IN COM	Input Common
3	IN−	Input Op Amp: Inverting Input
4	FB	Input Feedback
5	$-V_{ISO}$ OUT	Isolated Power: −DC
6	$+V_{ISO}$ OUT	Isolated Power: +DC
36	TRIM	Output Offset Trim Adjustment
37	OUT LO	Output Low
38	OUT HI	Output High
42	+15 V IN	DC Power Supply Input: +15 V
43	PWR RTN	DC Power Supply Input Common
44	−15 V IN	DC Power Supply Input: −15 V

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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INSIDE THE AD206

The functional block diagram of the AD206 has been shown. The AD206 employs a double balanced amplitude modulation technique to implement transformer coupling of signals down to dc. The 430 kHz square wave carrier used by the AD206 is generated by an internal oscillator located on the output side of the isolator. This oscillator is powered by the bipolar +15 V dc supply.

The input port of the AD206 contains an uncommitted input op amp, a modulator and an isolated power supply. The uncommitted input amplifier may be used to supply gain or to buffer the input signals. The primary windings of the power transformer T2 are driven by the 430 kHz square wave while the secondary, in conjunction with a rectifier network, supplies isolated power to the modulator, input op amp and any external load.

A full wave modulator translates the input signal to the carrier frequency which is then transmitted across the signal transformer T1. The synchronous demodulator on the output port extracts the input signal from the carrier. This signal is then passed through a Bessel response low pass filter to an output buffer and is then made available at the output signal terminals.

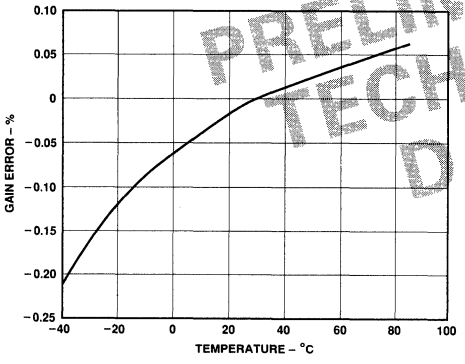


Figure 1. Gain Error vs. Temperature

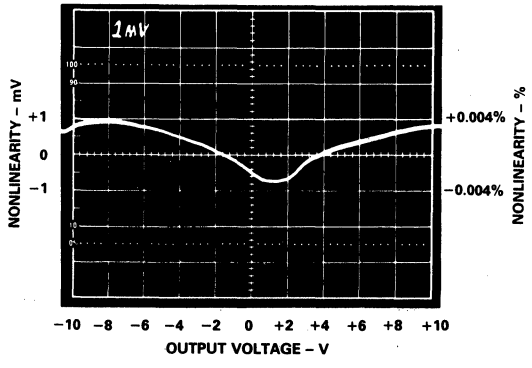


Figure 2. Gain Nonlinearity Error (% of Output Span and mV) vs. Qutput Voltage Swing for a Gain of 1

Nonlinearity does not change with temperature over the −40°C to +85°C range and is not dependent on the gain setting for gains in the rated 1 V/V to 10 V/V range.

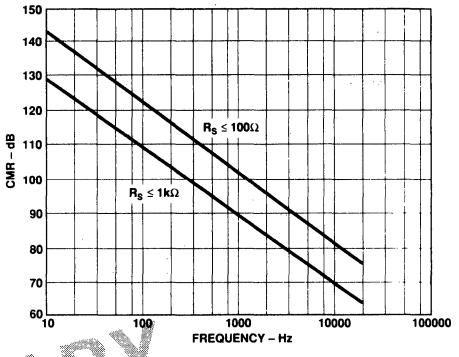


Figure 3. Typical Common-Mode Rejection (dB) vs. Common-Mode Signal Frequency (Hz) and Source Impedance Imbalance (Ω) for the 10 Hz to 20 kHz Frequency Range and with a Gain of 1

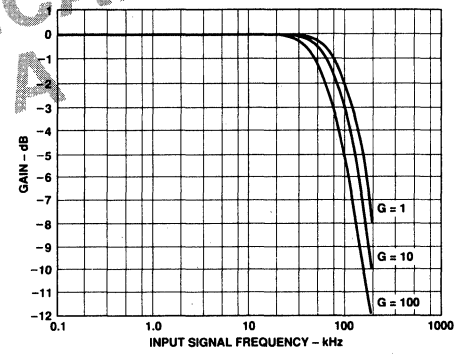


Figure 4. Normalized Gain (dB) as a Function of Input Signal Frequencies (kHz) in the 100 Hz to 150 kHz Range

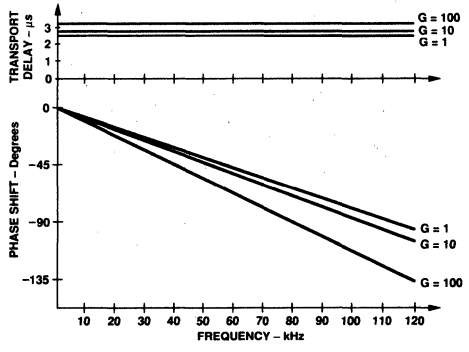
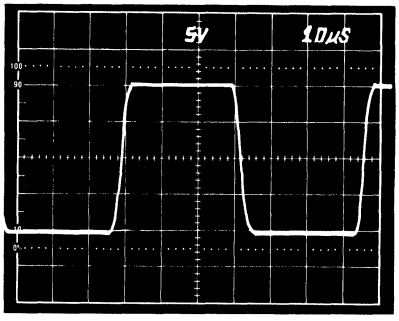


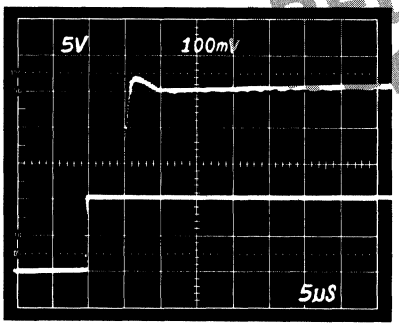
Figure 5. Phase Shift (°) and Transport Delay (µs) vs. Input Signal Frequencies (kHz) in the 10 Hz to 150 kHz Range

To achieve the optimal common-mode rejection of unwanted signals, it is strongly recommended that the source impedance imbalance be kept as low as possible and that the input circuitry be carefully laid out so as to avoid adding excessive stray capacitances at the isolator's input terminals.

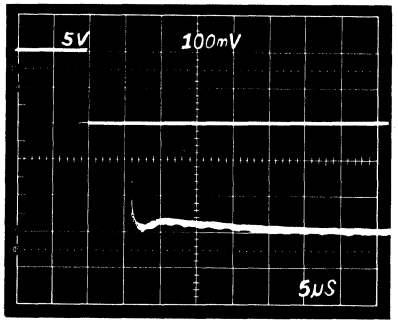


OUTPUT RESPONSE OF THE AD206, G = 1 ±10V, 15kHz

Figure 6. Output Response of the AD206 to a + and − Full-Scale Step at the Isolator's Input, with a Gain of 1



OVERSHOOT



UNDERSHOOT

Figure 7. Overshoot/Undershoot Characteristics of the AD206 to a Full-Scale Step at the Isolator's Input and with a Gain of 1

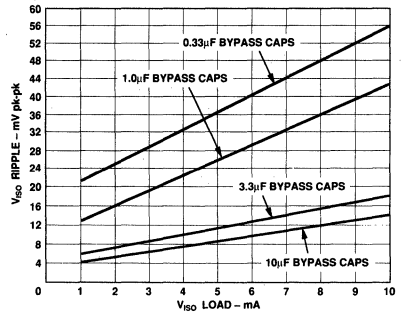


Figure 8. Isolated Power Supply Ripple (mV pk–pk) vs. Load (mA) and Bypass Capacitance (μF)

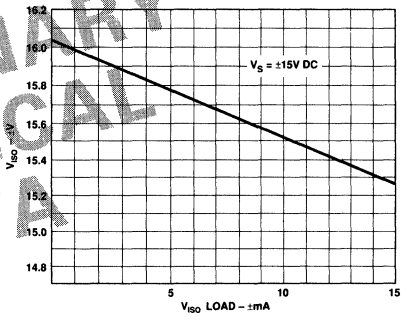


Figure 9. Isolated Power Supply Voltage (V DC) vs. Isolated Power Supply Load (mA)

To avoid increasing the sensitivity of the gain and offset specifications to the supply voltage and isolated load, it is recommended that the isolated power supply load not exceed ±10 mA.

CMV TESTING

As an assurance of high performance reliability, the CMV rating for each grade of the AD206 is tested to 120% of its rated isolation voltage (1800 V rms for the B Grade and 900 V rms for the A Grade) for one minute.

POWERING THE AD206

The AD206 is powered by a bipolar ±15 V dc power supply connected as shown in Figure 10. External bypass capacitors should be provided in the bused applications, as shown in Figure 10. Note that a small signal related current (50 $\mu A/V_{OUTPUT}$) will flow out of the OUT LO pin (Pin 37). The OUT LO terminals should therefore be bused together and referenced at a single "Analog Star Ground" to the ±15 V dc supply common as illustrated in Figure 10.

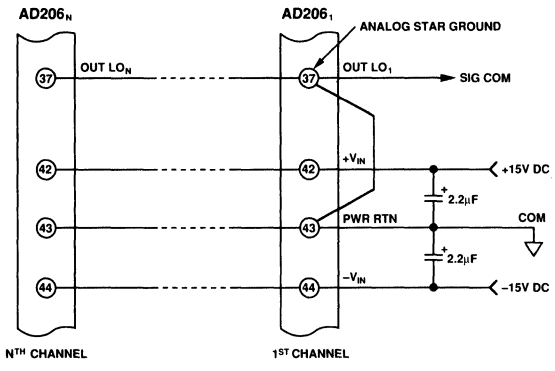


Figure 10. Powering the AD206

Power Supply Voltage Considerations. The rated performance of the AD206 will remain unaffected for power supply voltages in the ±14.5 V dc to ±16.5 V dc range. Voltages below ±14.25 V dc may cause the AD206 to cease operating properly.

Note: Power supply voltages greater than 17.5 V dc may damage the internal components of the AD206 and consequently should not be used.

USING THE AD206

Unity Gain Input Configuration. The basic unity gain configuration for input signals of up to ±10 V is shown in Figure 11.

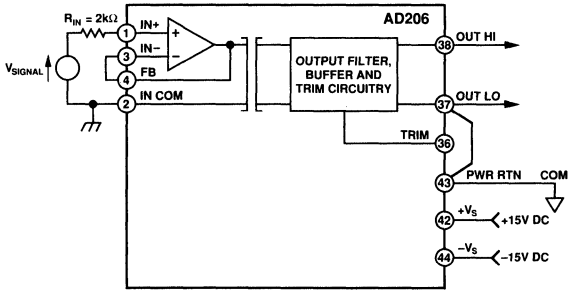


Figure 11. Basic Unity Gain Configuration

Noninverting Input Configuration for a Gain Greater Than 1 (G>1). When input signal levels must be amplified and isolated, Figure 12 shows how to get a gain greater than 1 while continuing to preserve a very high input impedance.

In this circuit, the gain equation may be written as:

$$V_O = (1+R_F/R_G) \times V_{SIG}$$

where:

V_O = Output Voltage (V),
V_{SIG} = Input Signal Voltage (V),
R_F = Feedback Resistor Value (Ω),
R_G = Gain Resistor Value (Ω).

The values for the resistors R_F and R_G should be chosen subject to the following constraints:

- The total impedance of the gain network should be no greater than 10 kΩ.
- The current drawn in the feedback resistor (R_F) is no greater than 1 mA at ± 10 V. Note that for each mA drawn by the feedback resistor, the isolated power supply drive capability will decrease by 1 mA.
- The feedback (R_F) and gain resistor (R_G) result in the desired amplifier gain.

It is recommended that the feedback resistor (R_F) is bypassed with a 47 pF capacitor (C_F).

Note on the input resistor (R_{IN}): The 2 kΩ resistor placed in series with the input signal source and the IN+ terminal, designated as R_{IN} in Figures 11 and 12, is recommended so as to limit the current seen at the input terminals of the AD206 to 5.0 mA when the AD206 is not powered.

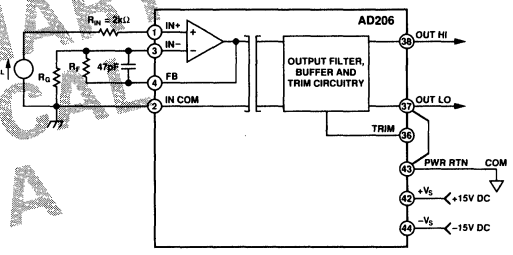


Figure 12. Noninverting Input Configuration for a Gain Greater than 1

Compensating the Uncommitted Input Op Amp. The open loop gain and phase versus frequency for the uncommitted input op amp are given in Figure 13. These curves can be used to determine the appropriate values for the feedback resistor and compensation capacitor in order to ensure frequency stability when reactive or nonlinear components are used in conjunction with the uncommitted input op amp.

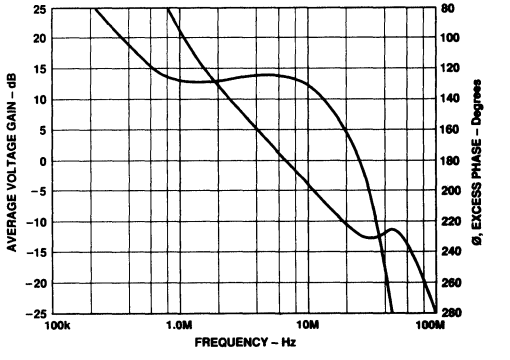


Figure 13. Open-Loop Gain and Phase Response for the Uncommitted Input Op Amp of the AD206

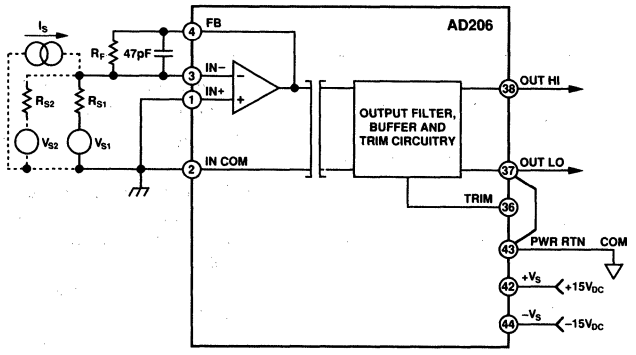


Figure 14. Summing or Current Input Configuration

Inverting, Summing or Current Input Configuration. Figure 14 shows how the AD206 can accommodate current inputs or sum currents or voltages.

In this circuit the output voltage equation can be written as:

$$V_O = -R_F \times (I_S + V_{S1}/R_{S1} + V_{S2}/R_{S2} + \ldots)$$

where:

V = Output Voltage (V),
V_{S1} = Voltage of Input Signal 1 (V),
V_{S2} = Voltage of input Signal 2 (V),
I_S = Input Current Source (A),
R_F = Feedback Resistor Value (Ω) (10 kΩ, typ)
R_{S1} = Source Resistance Associated with Input Signal 1 (Ω),
R_{S2} = Source Resistance Associated with Input Signal 2 (Ω).

The circuit of Figure 14 can also be used when the input signal is larger than the ±10 V input range of the isolator. For example, suppose that in Figure 14 only V_{S1}, R_{S1} and R_F are connected to the feedback, input and common terminals as shown by the solid lines in Figure 14. Now, a V_{S1} with a ±50 V span can be accommodated with R_F = 10 kΩ and a total R_{S1} = 50 kΩ.

GAIN AND OFFSET ADJUSTMENTS

General Comments. The AD206 features a TRIM pin on the output stage of the isolator. This pin is to be used with user-supplied external circuitry to adjust the output offset of the AD206. When gain and offset adjustments are required, the actual compensation circuit ultimately utilized will depend on:

- The input configuration mode of the isolation amplifier (i.e., noninverting or inverting).
- The placement of the adjusting potentiometer (i.e., on the isolator's input or output side).

As a general rule:

- Gain Adjustments are most easily accomplished as part of the gain-setting resistor network at the isolator's input side.
- To ensure the highest degree of stability in the gain adjustment, the adjusting potentiometers should be located as close as possible to the isolator's front-end and its impedance should be kept low. Adjustment ranges should also be kept to a minimum since their resolution and stability is dependent on the actual trim potentiometers used.
- Output side adjustments may be necessary under the conditions where adjusting potentiometers placed on the input side would present a hazard to the user due to the presence of high common-mode voltages during the adjustment procedure.
- It is recommended that the offset is adjusted prior to the gain adjustment.

Input Gain Adjustments for the Noninverting Mode of Operation. Figure 15 shows the suggested gain adjustment circuit. Note that the gain adjustment potentiometer R_P is incorporated into the gain-setting resistor network at the isolator's input.

For a ±1% trim range ($R_P \approx 1$ kΩ), let $R_C \approx 0.02 \dfrac{R_G \times R_F}{R_G + R_F}$.

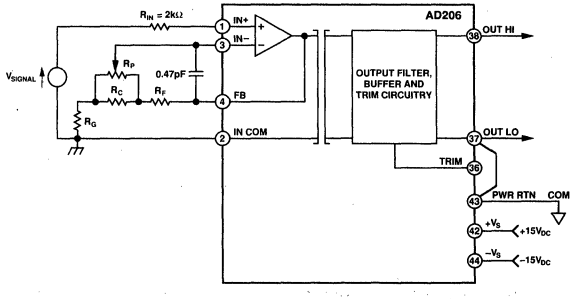


Figure 15. Input Gain Adjustment Circuit for the Noninverting Mode of Operation

Input Gain Adjustments for the Inverting Mode of Operation. Figure 16 shows the suggested gain adjustment circuit. In this circuit, the gain adjustment is made in the feedback loop using potentiometer R_P. The adjustments will be effective for all gains in the 1 to 10 range.

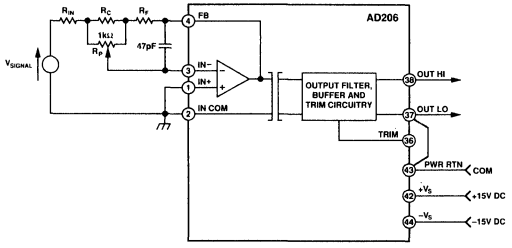


Figure 16. Input Gain Adjustment Circuit for the Inverting Mode of Operation

For an approximate ±1% gain trim range, let

$$R_X = \frac{R_{IN} \times R_F}{R_{IN} + R_F}$$

and select

$$R_C = 0.02 \times R_{IN}$$

while

$$R_F \leq 10\ k\Omega$$

$$C_F = 47\ pF$$

R_FV and R_{IN} are selected for a good temperature coefficient match.

Output Offset Adjustments. Figure 17 illustrates one method of adjusting the output offset voltage. Since the AD206 exhibits a nominal output offset of −35 mV, the circuit shown in Figure 17 was chosen to yield an offset correction of from 0 to +73 mV for a total output offset range of from approximately −35 mV to +38 mV.

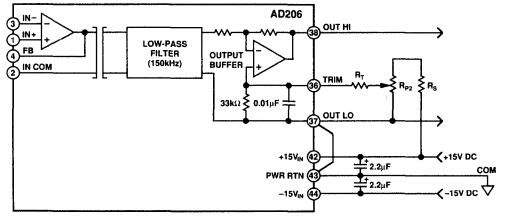


Figure 17. Output Offset Adjustment Circuit

Output Gain Adjustments. Since the output amplifier stage of the AD206 is fixed at unity, any desired output gain adjustments can only be made in a subsequent stage.

USING ISOLATED POWER

The AD206 provides ±15 V dc @ ±10 mA power outputs referred to the input common. These may be used to power various accessory circuits which must operate at the input common-mode level including input adjustment circuits, references, op amps, signal conditioners or remote transducers. Figure 18 shows the recommended connections from the isolated power supplies.

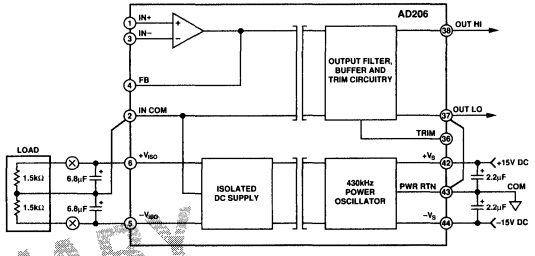


Figure 18. Using the Isolated Power Supplies

The current delivered by the isolated supplies may be increased to ±15 mA if the input dc supply voltage is increased beyond ±15 V dc.

CAUTION: The AD206 design does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

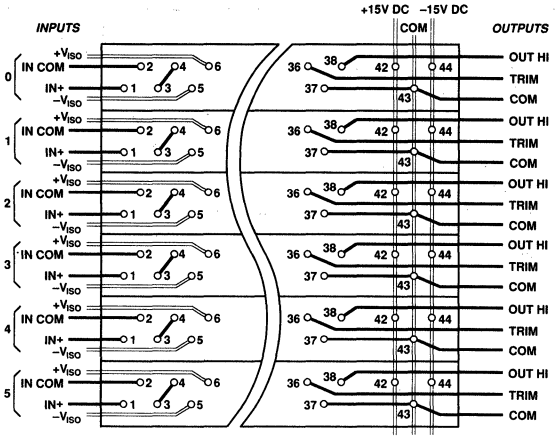


Figure 19a. PCB Layout for Multichannel, Unity Gain Applications

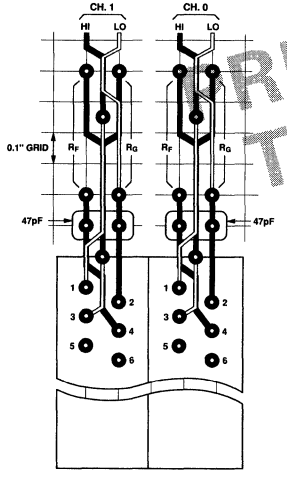


Figure 19b. PCB Layout for Multichannel Applications with Gain Required on the AD206s

APPLICATION EXAMPLES

Motor Control. Figure 20 shows an AD206 used in a dc motor controller application. The excellent phase characteristics and wide bandwidth of the AD206 are ideal for this type of application.

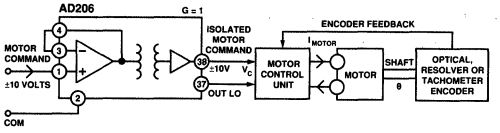


Figure 20. Using the AD206 in a Motor Control Application

Multichannel Data Acquisition

Figure 21 shows the AD206 in a multichannel data acquisition application. Its wide bandwidth, fast slew and settling characteristics are useful in this type of application. The AD206 can be used to solve the problem of low level signal measurement over long distances – extracting the signal, rejecting common-mode noise and protecting against accidental shorts.

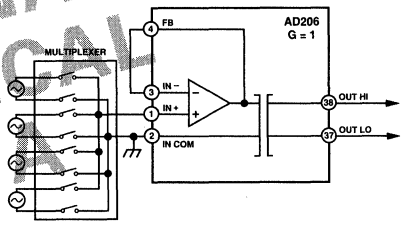


Figure 21. Using the AD206 in Multichannel Data Acquisition Applications

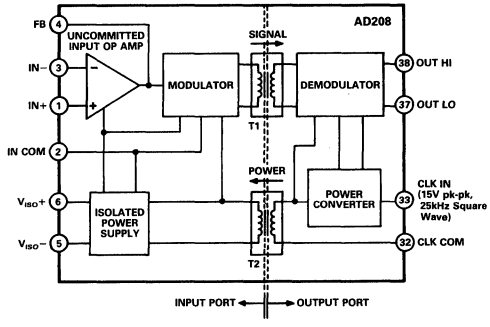
High Precision, Low Offset, mV Input Isolation Amplifier

AD208

FEATURES
Wide Gain Range: 1 to 1000 V/V
Low Nonlinearity: ±0.0125%
Low Input Offset Voltage: ±0.27 mV, max (G = 1000 V/V)
Low Offset Drift: ±1.5 μV/°C , max (G = 1000 V/V)
High CMV Isolation: 1.5 kV RMS (B Grade)
Isolated Power: ±8.0 V DC with up to ±5 mA
Completely Compatible with the AD204 SIP
Small SIP: 2.08″ (52.8 mm) × 0.26″ (6.6 mm) × 0.625″ (15.9 mm)
Performance Rated over −40°C to +85°C

APPLICATIONS
Isolated RTD and Thermocouple Applications
mV Signal Amplification and Isolation
Process Instrumentation and Control
Multichannel Data Acquisition

AD208 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD208 is a high precision, two-port, transformer-coupled isolation amplifier expressly designed for applications that require the amplification and isolation of extremely low level (i.e., ±mV) signals. The innovative front-end circuit design of the AD208 ensures the low offset characteristics and stable high gain properties of the AD208. The AD208 is fully compatible with the SIP style packaging of Analog Devices' low cost AD204 family of isolation amplifiers.

The AD208 provides total galvanic isolation between the input and output stages of the isolation amplifier, including the power supplies, through the use of internal transformer coupling. The functionally complete design of the AD208, powered by an externally supplied 15 V pk–pk, 25 kHz clock or the recommended AD246 Clock Driver, eliminates the need for a user supplied dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD208 emphasizes maximum flexibility and ease of use in a broad range of applications where low level signals must be measured and transmitted under high CMV conditions. The AD208 has a ±5 V output range, an adjustable gain range of from 1 to 1,000 V/V and a front-end power supply of ±8.0 V dc with up to ±5 mA of current drive capability.

PRODUCT HIGHLIGHTS

Wide Gain Range. The AD208 features a wide adjustable gain range of from 1 to 1,000 V/V. The stable high gain properties of the AD208 allow for the amplification and isolation of signals in the ±mV range.

Flexible Input Stage. An uncommitted op amp is provided on the input stage of the AD208. This allows for input buffering and gain as needed. It also facilitates a host of alternative input functions including filtering, summing, high voltage ranges and current inputs.

High Accuracy. Exhibiting a typical nonlinearity of ±0.0125% and a low gain temperature coefficient, averaging ±35 ppm/°C over the rated temperature range, the AD208 provides high isolation without loss of signal integrity and quality.

Low Offset Characteristics. With a maximum initial offset of ±(0.25 + 15 /G)mV and a maximum offset drift of ±(1.5 + 20 /G) μV/°C, the AD208 is the ideal isolation amplifier solution when low level, ±mV, signals must be measured and processed.

Excellent Common Mode Performance. The AD208BY provides 1.5 kV rms of common mode protection. Both grades of the AD208 feature a low common mode capacitance of 5.0 pF, inclusive of power isolation, that results in a typical common mode rejection specification of 100 dB (1 kΩ source impedance imbalance) as well as a low leakage current of 2.0 μA rms (max @ 240 V rms, 60 Hz).

Isolated Power. An isolated ±8.0 V dc power supply with the capability of delivering typically up to ±5 mA is available at the input port of the AD208. This permits the isolator to power floating signal conditioners, front-end amplifiers or remote transducers at the input.

Performance Rated Over the −40°C to +85°C Temperature Range. With its performance rated over the −40°C to +85°C temperature range the AD208 is an ideal isolation amplifier for use in industrial environments.

SPECIFICATIONS (typical @ +25°C, Output Load ≥ 1 MΩ, V_S = 15 V pk–pk, 25 kHz square wave, unless noted otherwise)

	AD208AY	AD208BY
GAIN		
Range	1–1000 V/V	*
Error (G = 1 V/V)	−1.0% (±2.5%, max)	*
vs. Temperature[1]		
−40°C to 0°C	±60 ppm/°C, max	*
0°C to +85°C	±20 ppm/°C, max	*
vs. Supply Voltage	±100 ppm/V	*
Nonlinearity[2], ±5 V Output Swing, G = 1–1000 V/V	±0.0125%	*
G = 1 V/V	±0.03%, max	±0.015%, max
INPUT VOLTAGE RATINGS[3]		
Linear Differential Range	±5 V, min	*
Max Safe Differential Range	±6 V	*
Max CMV Input to Output		
AC, 60 Hz, Continuous	750 V rms	1500 V rms
Continuous (AC & DC)	±1000 V peak	±2000 V peak
Common Mode Rejection (CMR) @ 60 Hz		
R_S ≤100 Ω (HI & LO Inputs),		
G = 1 V/V	100 dB	*
G = 1,000 V/V	120 dB	*
Common Mode Rejection (CMR) @ 60 Hz		
R_S≤1 kΩ (Input, HI, LO or Both)		
G = 1 V/V	100 dB	*
G = 1,000 V/V	100 dB	*
Leakage Current, Input to Output, @ 240 V rms, 60 Hz	2 μA rms, max	*
INPUT IMPEDANCE		
Differential (G = 1 V/V)	15 MΩ	*
Common Mode Across the Isolation Barrier	2 GΩ‖5 pF	*
OFFSET VOLTAGE, REFERRED TO INPUT (RTI)		
Initial @ +25°C (Adjustable to Zero)	±(0.25+15 /G) mV, max	*
vs. Temperature (−40°C to +85°C)	±(1.5+20 /G) μV/°C, max	*
vs. Supply Voltage	±(50+150 /G) μV/Volt	*
Voltage Noise, 0.1 Hz to 100 Hz	1.0 μV pk–pk	*
INPUT BIAS CURRENT		
Initial @ +25°C	±10 nA, max	*
vs. Temperature (−40°C to +85°C)	±100 pA/°C, max	*
vs. Supply Voltage	±1 nA/Volt	*
Current Noise, 0.1 Hz to 100 Hz	50 pA pk–pk	*
INPUT DIFFERENCE CURRENT		
Initial @ +25°C	±6 nA	*
vs. Temperature (−40°C to +85°C)	±60 pA/°C	*
FREQUENCY RESPONSE		
Bandwidth[4] (Full Signal, i.e., V_O≤10 V pk–pk)		
G = 1 V/V	4.0 kHz	*
G = 1000 V/V	0.4 kHz	*
Slew Rate	0.1 V/μs	*
Settling Time to ±0.10% on a 10 V Step, G = 1 V/V	2 ms	*
Overload Recovery Time[5], G = 1000 V/V	5 ms	*
RATED OUTPUT		
Voltage (OUT HI to OUT LO)	±5 V	*
Maximum Voltage Difference Between OUT HI and OUT LO or CLK COM (Pin 32)	±6.5 V	*
Output Resistance	3 kΩ	*
Output Ripple, 100 kHz Bandwidth	10 mV pk–pk	*
5 kHz Bandwidth	0.8 mV pk–pk	*
ISOLATED POWER OUTPUT		
Voltage, No Load	±8.0 V	*
vs. Temperature (−40°C to +85°C)	±0.025%/°C	*

	AD208AY	AD208BY
ISOLATED POWER SUPPLY (Continued)		
Accuracy	±10%	*
Rated Load Current[6]	±2.0 mA, min	*
Regulation, No Load to Rated Load	10%	*
Line Regulation	±10%/Volt	*
Ripple, Rated Load, 100 kHz Bandwidth	100 mV pk-pk	*
CLOCK DRIVE INPUT OF THE AD208[7]		
Input Voltage	15 V pk-pk ± 5%, Square Wave	*
Input Current (No Load on Isolated Supplies)	±10 mA pk	*
Frequency	25 kHz ±5%	*
Duty Cycle	47.5% to 52.5%	*
PACKAGE DIMENSIONS		
SIP Package	2.08″ × 0.260″ × 0.625″, max	*
	52.8 mm × 6.6 mm × 15.9 mm, max	*
TEMPERATURE RANGE		
Rated Performance	−40°C to +85°C	*
Storage	−40°C to +85°C	*

NOTES

*Specification is the same as that for the AD208AY.

[1]This specification represents the average gain drift over the indicated temperature range. Refer to Figure 2 for an illustration of the typical normalized gain drift for the AD208.

[2]Nonlinearity is specified as a % deviation from a best straight line. For gains greater than 50 V/V, a 100 pF capacitor from the feedback terminal of the input op amp (Pin 4) to the input common (Pin 2) is recommended in order to minimize the gain nonlinearity. Refer to Figure 30 for a circuit schematic.

[3]To limit the input current to the AD208 during unpowered or saturated conditions it is recommended that a resistor (typically 2 kΩ) be placed in series with the signal and the input terminal of the AD208. A reasonable value for the current limit would be 2.5 mA.

[4]Refer to Figure 16 for a graph of the AD208's 3 dB Bandwidth versus Gain Setting.

[5]Overload Recovery Time is the time it takes for the isolation amplifier to return to within ±0.10% of its correct value from a saturated condition once the initiating overrange signal has been removed. For the AD208, the overload recovery time is determined by applying a +5 V (−5 V) pulse at the input terminals, when the AD208 is configured for a gain of 1,000 V/V, and then measuring the time it takes for the output to return to zero from its positive (negative) full-scale saturated voltage condition. A 2 kΩ resistor placed in series with the signal and the input terminal will reduce the overload recovery time to approximately 2 ms.

[6]Refer to Figure 17 for a curve illustrating the load drive capabilities of the isolated power supply.

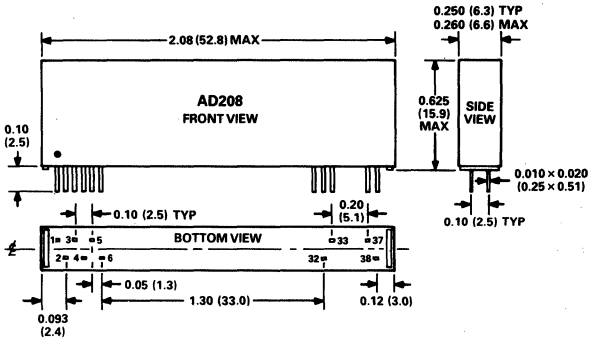
[7]It is recommended that the AD246 Clock Driver be used to drive the AD208. Refer to the "Powering the AD208 Section" of this data sheet for a detailed description of the AD208's clock driver input voltage and current requirements.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

AD208 SIP Package



AD208 Pin Designations

PIN	DESIGNATION	FUNCTION
1	IN+	NONINVERTING INPUT
2	IN COM	INPUT COMMON
3	IN–	INVERTING INPUT
4	FB	INPUT OP AMP; OUTPUT/FEEDBACK
5	V_{ISO-}	ISOLATED POWER: –DC OUTPUT
6	V_{ISO+}	ISOLATED POWER: +DC OUTPUT
32	CLK COM	CLOCK COMMON
33	CLK IN	CLOCK INPUT
37	OUT LO	OUTPUT LO
38	OUT HI	OUTPUT HI

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

INSIDE THE AD208

The functional block diagram of the AD208 is shown previously. The AD208 employs amplitude modulation techniques to implement transformer coupling of signals down to dc. The primary side of the power transformer, T2, is driven by the externally supplied 15 V pk–pk, 25 kHz square wave generator or the AD246 Clock Driver.

A full wave modulator translates the input signal to the carrier frequency which is then transmitted across transformer T1. The synchronous demodulator in the output port extracts the input signal from the carrier. The output signal is not internally buffered, therefore the user is free to interchange the output leads to get signal inversion.

The input port of the AD208 contains an uncommitted input op amp, a modulator and the isolated power supply. The uncommitted input amplifier can be used to supply gain or to buffer the input signals.

PERFORMANCE CHARACTERISTICS

Gain Error. Figure 1 shows the typical gain error for the AD208, expressed in % of full scale, as a function of the isolator's output load (Ω). For minimal gain errors, the AD208 is best operated with output loads greater than or equal to 1 MΩ.

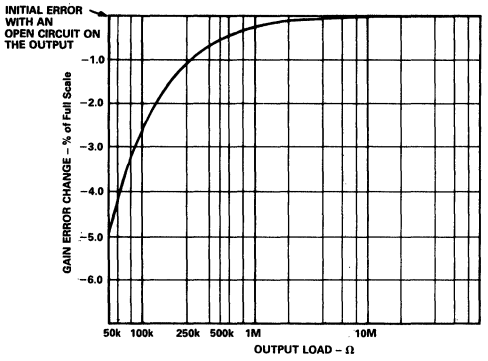


Figure 1. Gain Error Change (% of Full Scale) vs. Output Load (Ω), with V_S = 15 V pk–pk, 25 kHz Square Wave

Gain Drift. Figure 2 presents the normalized gain drift, from the gain error measured at +25°C, of the AD208 over the –40°C to +85°C rated temperature range.

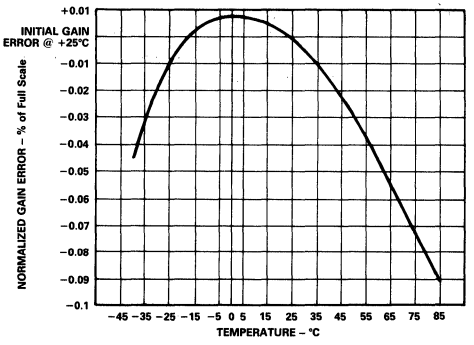


Figure 2. Normalized Gain Error (% of Full Scale) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The effect of the output load on the AD208's gain temperature coefficient is shown in Figure 3 for the –40°C to 0°C and 0°C to +85°C temperature ranges. To minimize the gain temperature coefficient, the AD208 performs best with output loads of greater than or equal to 1 MΩ.

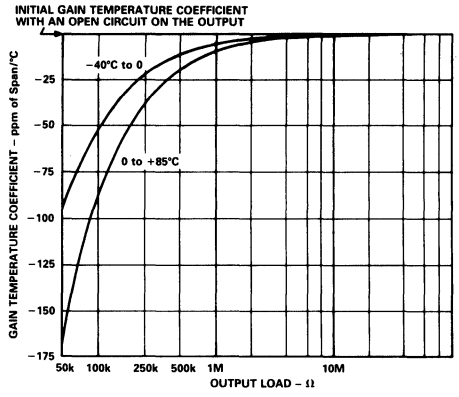


Figure 3. Gain Temperature Coefficient (ppm/°C) vs. Output Load (Ω) and Operating Temperature Range, with V_S = 15 V pk–pk, 25 kHz Square Wave

Gain Nonlinearity. The typical gain nonlinearity error of the AD208, at a gain of 1 V/V, is specified as ±0.0125% or ±1.25 mV. The nonlinearity performance of the AD208 is dependent on the output voltage swing and this dependency is illustrated in Figure 4. The vertical axis represents the nonlinearity error, expressed in % of output span (i.e., % of 10 V) on the left axis or in mV on the right axis. The horizontal axis displays the magnitude of the output voltage swing.

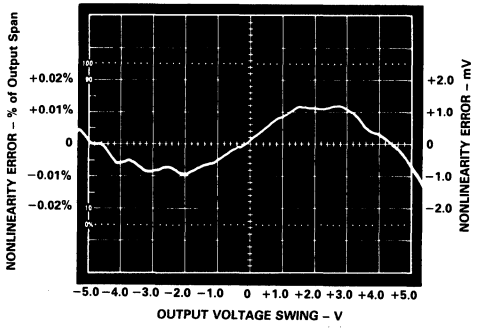


Figure 4. Typical Gain Nonlinearity Error (% of Output Span and mV) vs. Output Voltage Swing for a Gain of 1 V/V and with V_S = 15 V pk–pk, 25 kHz Square Wave

The variation of the AD208's gain nonlinearity, from that measured at +25°C, over the entire −40°C to +85°C rated temperature range is demonstrated by the curve in Figure 5.

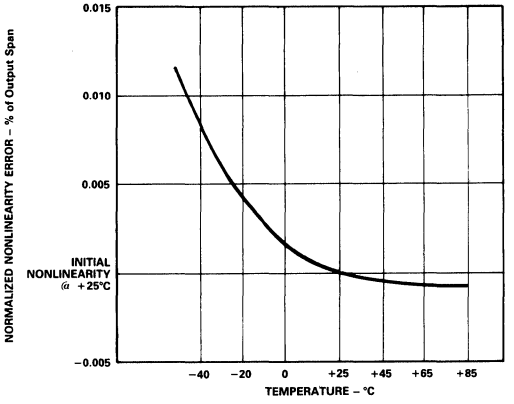


Figure 5. Normalized Gain Nonlinearity (% of Output Span) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The nonlinearity of the AD208 is minimized when its output load is greater than 1 MΩ, as shown in Figure 6.

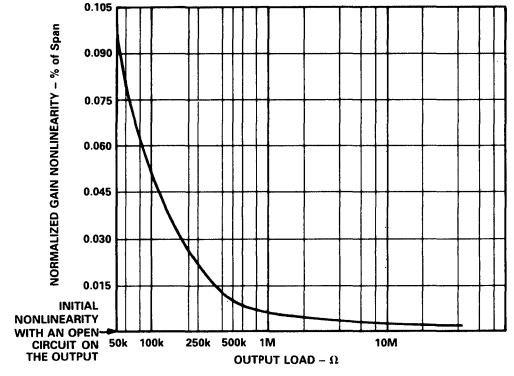


Figure 6. Normalized Gain Nonlinearity (% of Output Span) vs. Output Load (Ω) for a Gain of 1 V/V and with V_S = 15 V pk–pk, 25 kHz Square Wave

Input Voltage Rating. The linear input voltage range for the AD208 is specified as ±5 V. This rating applies when the AD208 is powered by a 15 V pk–pk ±5%, square wave (@ 25 kHz). The specified input voltage range is, however, affected by the clock driver voltage and the load placed on the AD208's front-end isolated power supplies. The variation of the input voltage range as a function of the isolated power supply load and the clock supply voltage are illustrated by the parametric curves in Figure 7.

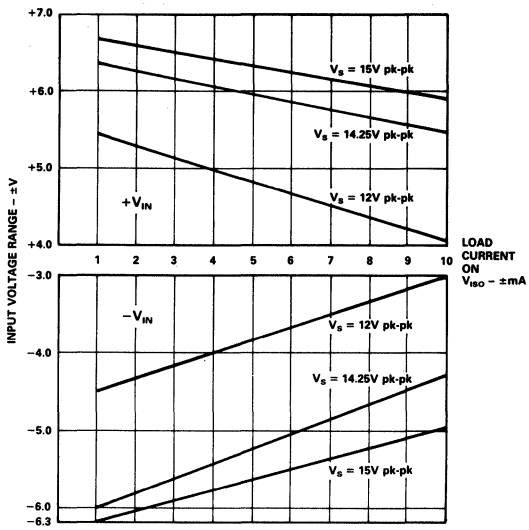


Figure 7. Input Voltage Range (±V) vs. Load Placed on the Isolated Power Supplies (mA) and Clock Driver Voltage (V pk–pk)

Common Mode Rejection. Figures 8 and 9 illustrate the typical common mode rejection, expressed in dB, of the AD208 as a function of the common mode signal frequency (kHz) and source impedance imbalance (kΩ) for gains of 1 V/V and 1,000 V/V, respectively.

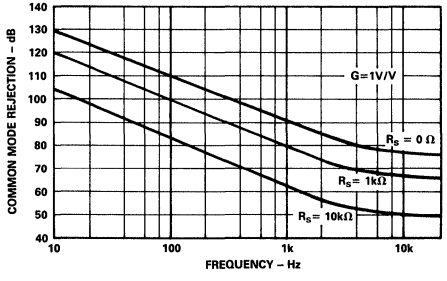


Figure 8. Typical Common Mode Rejection (dB) vs. Common Mode Signal Frequency (kHz) and Source Impedance Imbalance (kΩ) for a Gain of 1 V/V

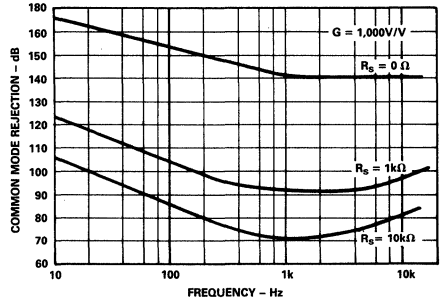


Figure 9. Typical Common Mode Rejection (dB) vs. Common Mode Signal Frequency (kHz) and Source Impedance Imbalance (kΩ) for a Gain of 1,000 V/V

To achieve the optimal common mode rejection of unwanted signals, it is strongly recommended that the source impedance imbalance be kept as low as possible and that the input circuitry be carefully laid out so as to avoid adding excessive stray capacitances at the isolator's input terminals.

Output Offset Voltage. The normalized output offset voltage drift from the initial offset measured at +25°C is presented in Figure 10 over the rated −40°C to +85°C temperature range.

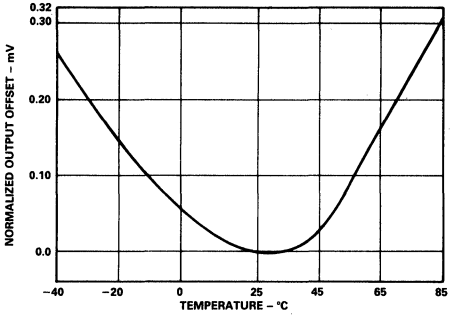


Figure 10. Normalized Output Offset Voltage (mV) vs. Temperature (°C) with an AD208 Gain of 1 V/V, with V_S = 15 V pk–pk, 25 kHz Square Wave

Input Offset Voltage. The AD208 exhibits an extremely low input offset voltage temperature coefficient over the −40°C to +85°C temperature range as indicated in Figure 11.

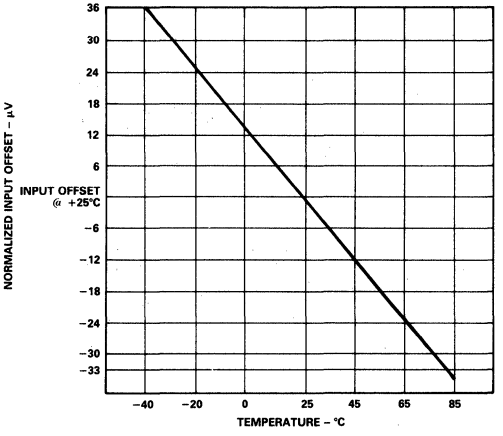


Figure 11. Normalized Input Offset Voltage (µV) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The typical noise characteristics for the AD208's uncommitted input op amp is summarized in Figure 12.

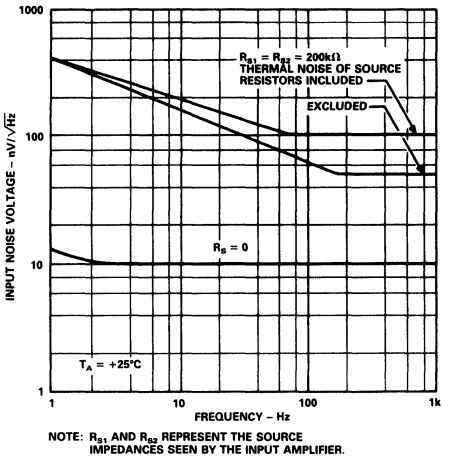


Figure 12. Typical Input Voltage Noise (nV/√Hz) vs. Frequency for the AD208's Uncommitted Input Op Amp

Input Bias Current. The typical input bias current variation from the initial bias current at +25°C as a function of temperature is presented in Figure 13.

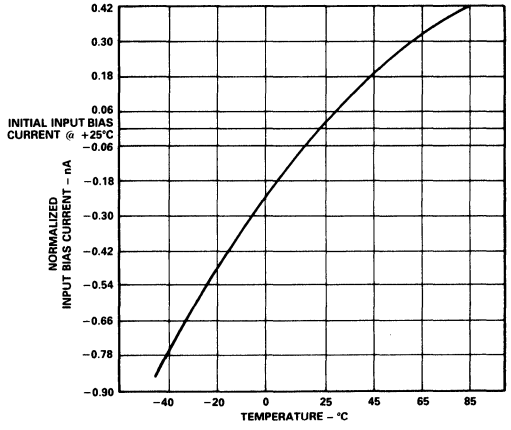


Figure 13. Normalized Input Bias Current (nA) vs. Temperature (°C)

Frequency Response: Gain and Phase Shift. Figure 14 characterizes the AD208's gain as a function of frequency, while Figure 15 illustrates the corresponding phase shift versus frequency.

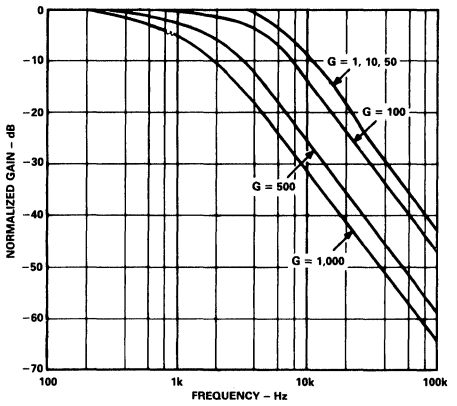


Figure 14. Normalized Gain (dB) as a Function of Input Signal Frequency (Hz)

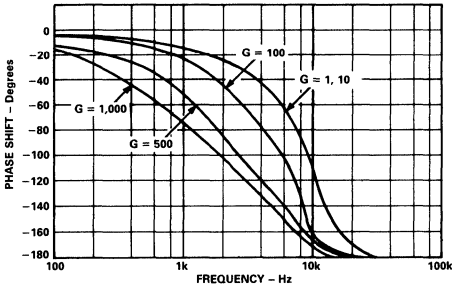


Figure 15. Phase Shift (Degrees) vs. Input Signal Frequency (Hz)

The frequency response performance of the AD208 can also be characterized in terms of its 3 dB bandwidth versus the desired gain setting as plotted in Figure 16.

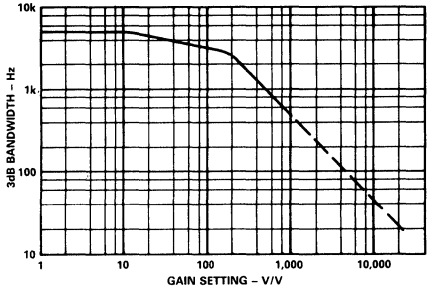


Figure 16. 3 dB Bandwidth (Hz) vs. AD208 Gain Setting (V/V)

Isolated Power Supply. The load characteristics of the AD208's isolated power supplies are plotted in Figure 17. It is recommended that the isolated power supply load not exceed 10 mA as permanent damage to the internal power circuitry of the AD208 may occur.

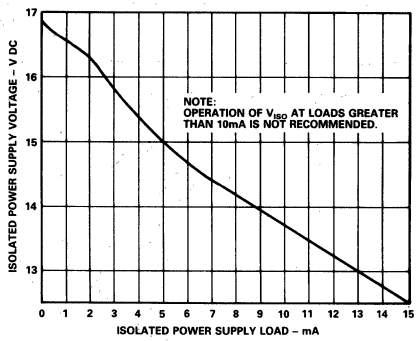


Figure 17. Isolated Power Supply Voltage (V DC) vs. Isolated Power Supply Load (mA), with V_S = 15 V pk–pk, 25 kHz Square Wave

The isolated power supply exhibits some ripple which varies as a function of the load placed on the supply terminals. Figure 18 illustrates the functional relationship between the isolated supply ripple (mV pk–pk) and the resistive load placed on the supplies.

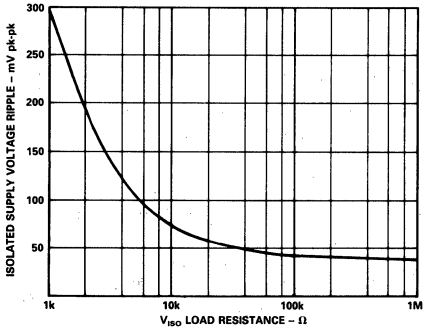


Figure 18. Isolated Power Supply Ripple (mV pk–pk) vs. Resistive Load (Ω), with V_S = 15 V pk–pk, 25 kHz Square Wave

The AD208 has internal bypass capacitors that optimize the tradeoff between output ripple and power supply performance, even under full load conditions. If a specific application requires more bypassing of the isolated power supplies, external capacitors may be added. Figure 19 plots the isolated power supply ripple as a function of the external bypass capacitance under rated load conditions (i.e., ±2 mA).

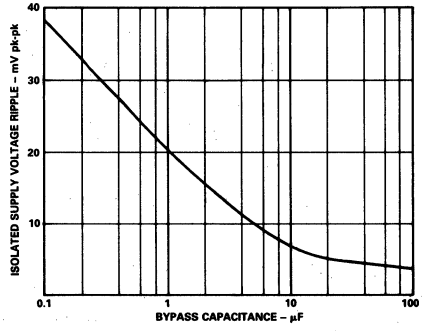


Figure 19. Isolated Power Supply Ripple (mV pk–pk) vs. Bypass Capacitance (µF) with a ±2 mA Load on the Isolated Supplies and a Noise Bandwidth of 100 kHz

CAUTION: The AD208 design does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICABLE STANDARDS

As an assurance of high performance reliability, the CMV rating of each grade of the AD208 is factory tested for one minute to 120% of the appropriate CMV isolation rating (1800 V rms for the B grade and 900 V rms for the A Grade).

POWERING THE AD208

The AD208 is powered by an externally supplied 15 V pk–pk, 25 kHz square wave (50% duty cycle) clock signal connected as shown in Figure 20. An ac coupling capacitor is provided in the AD208 to level shift the clock signal which in turn generates the necessary internal dc supply voltages and carrier signal.

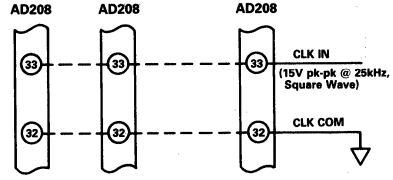


Figure 20. Powering the AD208

The rated performance of the AD208 is specified for a clock driver square wave signal that meets the following requirements:

- 15 V pk–pk ±5%
- 25 kHz ±5%
- 47.5% to 52.5% duty cycle.

Care must be exercised when using a square wave generator whose output does not meet the above requirements as the performance of the AD208 may be adversely affected.

Clock Driver Voltage Considerations. The rated performance of the AD208 will remain unaffected for clock driver voltages in the 14.25 V pk–pk to 15.75 V pk–pk range. Voltage swings below 14.25 V pk–pk will result primarily in the derating of the output voltage and isolated power supply voltage specifications as shown in Figures 21 and 22, respectively.

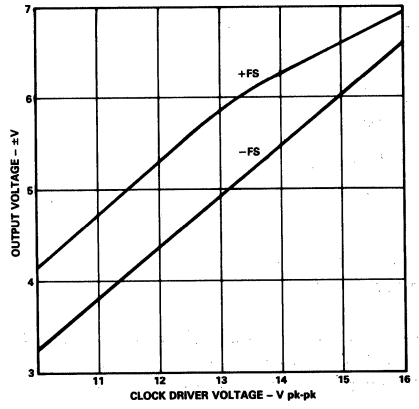


Figure 21. Output Voltage Swing (±V) vs. Clock Driver Voltage (V pk–pk)

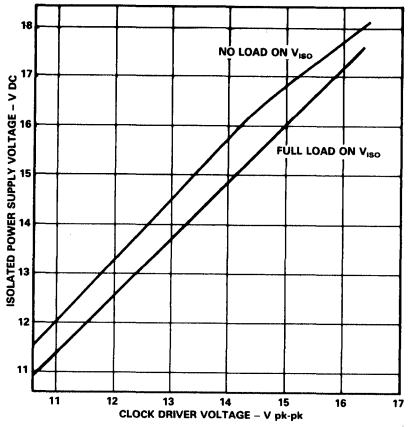


Figure 22. Isolated Power Supply Voltage (V DC) vs. Clock Driver Voltage (V pk–pk)

The reduction in the rated output voltage will increase the values for the nonlinearity and gain error parameters of the AD208 because of the headroom limits placed on the internal circuitry.

Note: Clock driver voltages greater than 16.5 V pk–pk may damage the internal components of the AD208 and consequently should not be used.

Clock Driver Frequency Considerations. The definition of the clock duty cycle for a two-state rectangular waveform is given by:

$$Duty\ Cycle\ (\%) = T_{HI}/(T_{HI} + T_{LO}) \times 100\%$$

where:

T_{HI} = The period of time that the waveform is in the HI state.

T_{LO} = The period of time that the waveform is in the LO state.

The performance of the AD208 will not be adversely affected by off-nominal clock signals so long as these clock signals are in the 47.5% to 52.5% duty cycle range and the 23.75 kHz to 26.25 kHz frequency range. To prevent a significant deterioration of the AD208 performance, it is strongly recommended that the clock driver duty cycle and frequency values ultimately chosen to operate the AD208 do not fall outside of the 40% to 60% and 20 kHz to 30 kHz ranges.

Clock Driver Power Considerations. In selecting and/or designing a clock driver for the AD208 isolation amplifier, it should be noted that the AD208 presents a reactive load to the clock driver. Consequently, both the average and peak drive currents to the AD208 clock input must be considered. Figures 23 and 24 illustrate the typical clock driver input voltage and current waveforms for a single AD208 with its isolated power supplies unloaded and fully loaded.

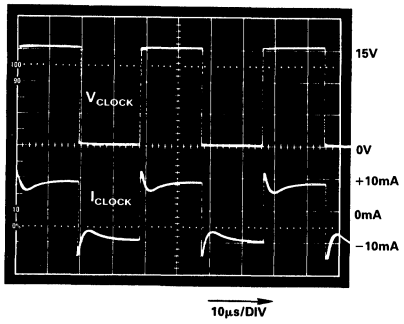


Figure 23. Typical Clock Voltage and Current Waveforms for a Single AD208 with No Load on its Isolated Power Supply

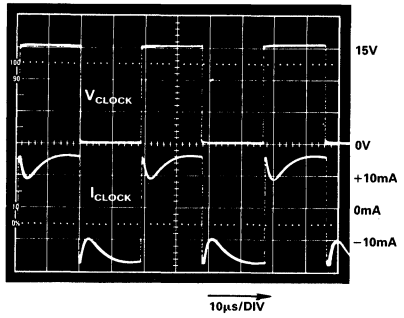


Figure 24. Typical Clock Voltage and Current Waveforms for a Single AD208 with a ±2 mA Load on its Isolated Power Supply

USING THE AD246 CLOCK DRIVER TO POWER THE AD208

To ensure that the power requirements of the AD208 are satisfied, Analog Devices suggests the use of the AD246 Clock Driver. The AD246 is an inexpensive, compact square wave oscillator that can be used to generate the necessary AD208 clock signal from a single +15 V dc supply. Table I lists the key specifications for the AD246.

	AD246JY
OUTPUT	
Frequency	25 kHz
Voltage	15 V pk–pk
Duty Cycle	50%
Maximum Safe Current Drive Capability[1]	120 mA
Fan Out	16
Resistance	15 Ω
POWER SUPPLY REQUIREMENTS	
Input Voltage	+15 V dc ± 5%
Supply Current	
Unloaded	3.5 mA
Each AD208 Adds	4.0 mA
Each 1 mA Load on AD208 $+V_{ISO}$ or $-V_{ISO}$ Adds	1.12 mA

NOTE
[1]The high current drive output of the AD246 will not withstand a short to ground.

Table I. Key Specifications for the AD246 Clock Driver (Specifications typical @ +25°C and V_S = +15 V DC unless otherwise noted)

The AD246JY is connected to the AD208 oscillator input(s) as shown in Figure 25. The AC1058 mating socket can be used with the AD246JY as demonstrated in Figure 27.

A supply bypass capacitor is included in the AD246, however it is recommended that an externally supplied bypass capacitor, as indicated by the dotted circuitry in Figure 26, be used if many AD208s are to be driven by a single AD246. The suggested capacitance value is 1 μF for every five AD208s driven. The placement of the bypass capacitor should be as close as possible to the AD246 Clock Driver.

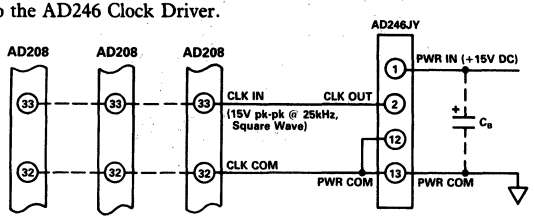


Figure 25. Using the AD246 to Power the AD208

USING THE AD208

Unity Gain Input Configuration. The basic unity gain configuration for input signals of up to ±5 V is shown in Figure 26.

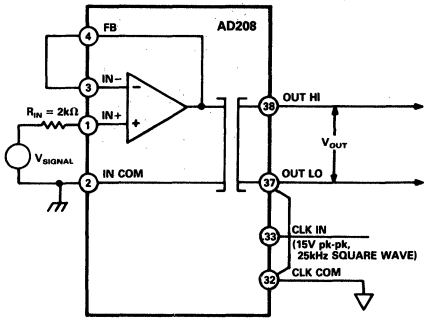


Figure 26. Basic Unity Gain Configuration

Input Configuration for a Gain Greater Than 1 (G>1). When small input signal levels must be amplified and isolated, Figure 27 shows how to get a gain greater than 1 while continuing to preserve a very high input impedance.

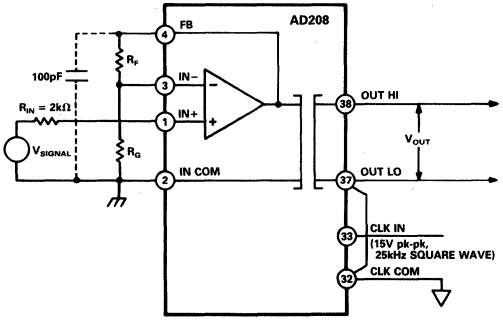


Figure 27. Input Configuration for a Gain Greater Than 1

In this circuit, the gain equation may be written as:

$$V_O = (1 + R_F/R_G) \times V_{SIG}$$

where:

V_O = Output Voltage (V)
V_{SIG} = Input Signal Voltage (V)
R_F = Feedback Resistor Value (Ω)
R_G = Gain Resistor Value (Ω).

The values for the resistors R_F and R_G should be chosen subject to the following constraints:

- The current drawn in the feedback resistor (R_F) is no greater than 1 mA. Note that for each mA drawn by the feedback resistor, the isolated power supply drive capability will decrease by 1 mA.
- The feedback (R_F) and gain resistor (R_G) result in the desired amplifier gain.

Note on the 100 pF Capacitor: Whenever a gain of 50 V/V or greater is required, a 100 pF capacitor from the FB (input op amp feedback) terminal to the IN COM (input common) terminal, as shown with the dotted lines in Figure 27, is highly recommended. The capacitor acts to filter out switching noise and will minimize the isolator's nonlinearity parameter.

Note on the 2 kΩ Resistor: The 2 kΩ resistor placed in series with the input signal source and the IN+ terminal, designated as R_{IN} in Figures 26 and 27, is suggested so as to limit the current seen at the input terminals to 2.5 mA when the AD208 is OFF. The 2 kΩ resistor will also reduce the overload recovery time to 2 ms.

Compensating the Uncommitted Input Op Amp. The open loop gain and phase versus frequency for the uncommitted input op amp is given in Figure 28. These curves can be used to determine the appropriate values for the feedback resistor and compensation capacitor in order to ensure frequency stability when reactive or nonlinear components are used in conjunction with the uncommitted input op amp.

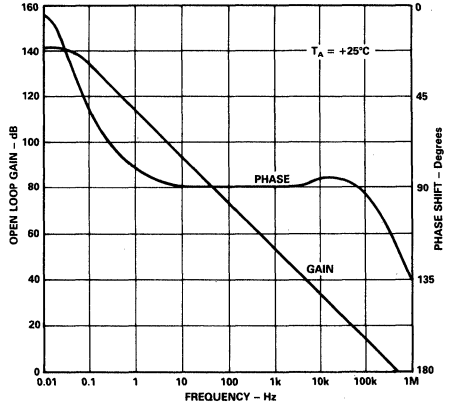


Figure 28. Open Loop Gain and Phase Response for the Uncommitted Input Op Amp of the AD208

A capacitor placed in the feedback loop of the input op amp may increase the nonlinearity of the AD208, particularly for large gains. A resistor (1 kΩ) placed in series with this capacitor should minimize the capacitor's effect on nonlinearity.

Signal Inversion. The circuits illustrated in Figures 26 and 29 are "noninverting." If signal inversion is desired simply interchange the output leads of the circuits shown in Figures 26 or 27 to get inversion. This approach allows for the retention of the high input impedance characteristics of the "noninverting" circuit.

Summing or Current Input Configuration. Figure 29 shows how the AD208 can accommodate current inputs or sum currents or voltages.

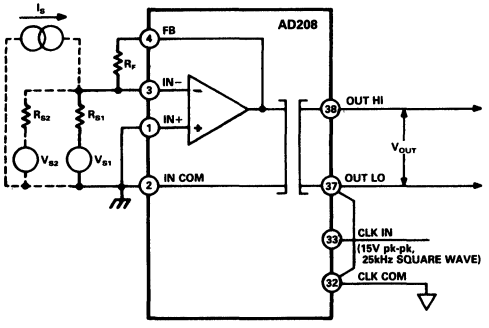


Figure 29. Summing or Current Input Configuration

In this circuit the output voltage equation can be written as:

$$V_O = -R_F \times (I_S + V_{S1}/R_{S1} + V_{S2}/R_{S2} + \ldots)$$

where:

V_O = Output Voltage (V)
V_{S1} = Voltage of Input Signal 1 (V)
V_{S2} = Voltage of Input Signal 2 (V)
I_S = Input Current Source (A)
R_F = Feedback Resistor (Ω)
R_{S1} = Source Resistance Associated with Input Signal 1 (Ω)
R_{S2} = Source Resistance Associated with Input Signal 2 (Ω).

The circuit of Figure 29 can also be used when the input signal is larger than the ±5 V input range of the isolator. For example, suppose that in Figure 29 only V_{S1}, R_{S1} and R_F are connected to the feedback, input and common terminals as shown by the solid lines in Figure 29. Now, a V_{S1} with a ±50 V span can be accommodated with R_F = 20 kΩ and R_{S1} = 200 kΩ.

Output Filter Circuit. Except at the highest useful gains, the noise seen at the output of the AD208 will be almost entirely comprised of the carrier ripple at multiples of 25 kHz. The ripple, when measured over a 100 kHz noise bandwidth, is typically 2 mV pk–pk near zero output and increases to approximately 7 mV pk–pk for outputs of ±5 V. The simple two-pole, 5 kHz low-pass Butterworth filter of Figure 30 can be used to reduce the output ripple of the AD208 to approximately 0.1 mV pk–pk and serve as an output buffer for the AD208.

An output buffer or filter may sometimes exhibit voltage spikes on the output even though none were present on the input signal to the buffer/filter. These spikes are usually due to clock noise appearing at the op amp's power supply pins, since most op amps have little or no supply rejection at high frequencies. Another common source of clock-related noise is from the sharing of the ground track by both the output circuit and the power input. The circuit of Figure 30, shows how to avoid these clock noise related problems.

Ideally, the output signal LO lead and the supply common should be tied together at the final signal measurement point as indicated in Figure 30. It may be useful to bypass the output LO to the output common with a 0.1 μF capacitor should the measurement point be more than a few feet from the isolator.

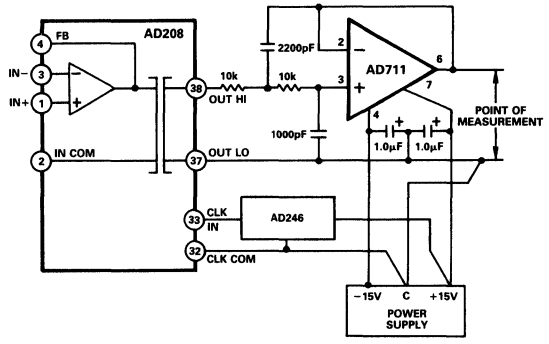


Figure 30. Output Filter Circuit Showing Proper Grounding

In multichannel applications where more than a few AD208s are driven by a single clock driver, substantial current spikes will flow in the power return line and in whichever signal output lead returns to a low impedance point (usually OUT LO). Consequently, both of these tracks should be made as large and as short as possible to minimize the track inductance and resistance. For best results, OUT LO should be connected directly to a ground plane that serves as the measurement common.

Current spikes can be greatly reduced by connecting a small inductance, 68 μHy to 100 μHy, in series with the clock drive input pin of each AD208. Molded chokes, such as the Dale IM-2 series, with a dc resistance of about 5 Ω should be suitable for most applications.

GAIN AND OFFSET ADJUSTMENTS

General Comments. When gain and offset adjustments are required, the actual compensation circuit ultimately utilized will depend on:

- The input configuration mode of the isolation amplifier (i.e., noninverting or inverting).
- The placement of the adjusting potentiometer (i.e., on the isolator's input or output side).

As a general rule:

- Offset Adjustments are best accomplished on the isolator's input side, as it is much easier and more efficient to null the offset ahead of any gain.
- Gain Adjustments are most easily accomplished as part of the gain-setting resistor network at the isolator's input side.
- To ensure the highest degree of stability in the gain and offset adjustments, the adjusting potentiometers should be located

as close as possible to the isolator's front end. Adjustment ranges should be kept to a minimum and high quality multiturn trimming potentiometers should be used.

- Output side adjustments may be necessary under the conditions where adjusting potentiometers placed on the input side would present a hazard to the user due to the presence of high common mode voltages during the adjustment procedure.
- It is recommended that the offset adjustment precedes the gain adjustment.

Input Adjustments for the Noninverting Mode of Operation

Offset Adjustment. Figure 31 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the noninverting mode of operation. The offset adjustment circuit injects a small voltage in series with the low side of the signal source. The adjustment potentiometer P_2 is responsible for nulling out the offset voltage. A 100 kΩ P_2, 50 kΩ R_{OA} and a 100 Ω R_C should provide an offset adjustment range (Referred to Input) of about ±15 mV. Since the offset is zeroed out ahead of the gain, the values given above for P_2, R_{OA} and R_C should work for any gain on the isolator.

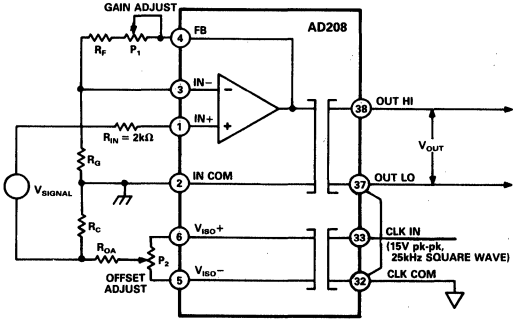


Figure 31. Input Adjustment Circuit for the Noninverting Mode of Operation

Notes:

- To minimize CMR degradation it is recommended that the resistor R_C (shown in Figure 31) be below a few hundred ohms.
- The offset adjustment circuit of Figure 31 will not work if the signal source has another current path to input common, or if current flows in the signal source LO lead. If this is the case, use the output adjustment procedure.

Gain Adjustment. Figure 31 also shows the suggested gain adjustment circuit. Note that the gain adjustment potentiometer P_1 is incorporated into the gain-setting resistor network at the isolator's input.

To maintain gain trim ranges that are independent of the gain setting, the potentiometer P_1 should be proportioned to R_F such that

$$\frac{P_1 \times 100\%}{R_F} = \textit{Desired Gain Adjustment Range (in \% of Output Span)}$$

and

$$(R_F + P_1/2)/R_G + 1 = \textit{Desired Gain Setting}$$

Input Adjustments for the Inverting Mode of Operation

Offset Adjustment. Figure 32 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the inverting mode of operation. Here the offset adjustment potentiometer P_2 nulls the voltage at the summing node. This method may be preferred over current injection since it is less affected by any subsequent gain adjustments. A 100 kΩ P_2, 50 kΩ R_{OA} and a 100 Ω R_C should provide an offset adjustment range (Referred to Input) of about ±15 mV.

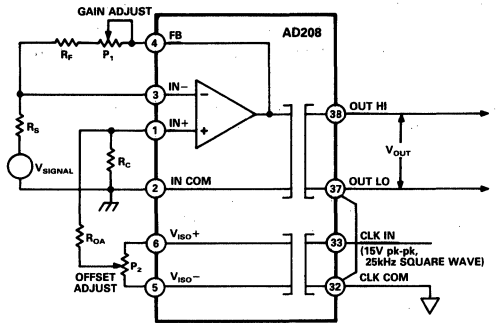


Figure 32. Input Adjustments for the Inverting Mode of Operation

Gain Adjustment. Figure 32 also shows the suggested gain adjustment circuit. In this circuit, the gain adjustment is made in the feedback loop using potentiometer P_1. The adjustments will be effective for all gains in the 1 to 1,000 V/V range.

Output Adjustments

Offset Adjustment. Figure 33 shows the recommended technique for offset adjustment at the output. In this circuit, a ±15 V dc voltage is supplied by an independent source. With reference to the output circuitry shown in Figure 33, the maximum offset adjustment range is given by:

$$E_{OFFSET} = \frac{R_C \times V_S}{R_C + R_O}$$

where, V_S is the power supply voltage. A 100 kΩ P_0, 100 Ω R_C and a 50 kΩ R_O should provide an offset adjustment range of about ±30 mV on the output.

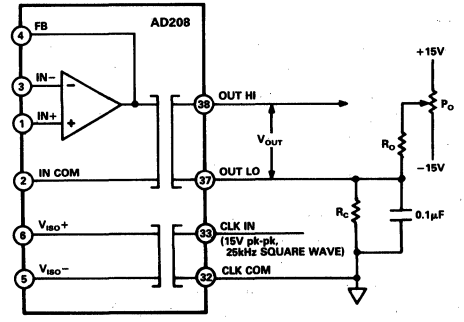


Figure 33. Output Side Offset Adjustment Circuit

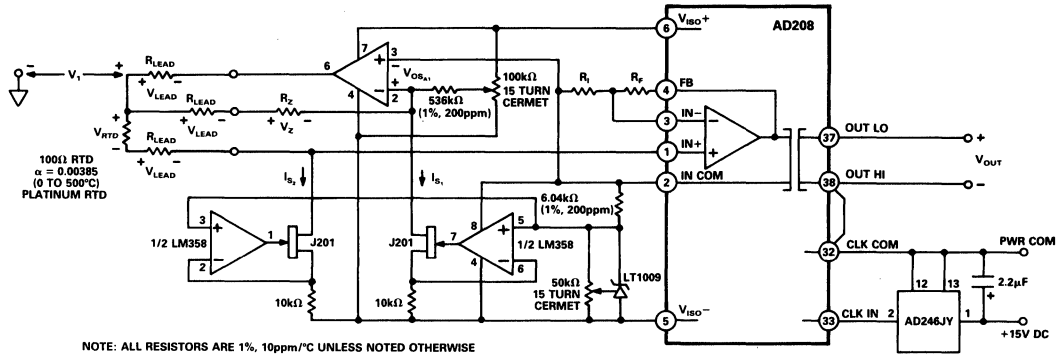


Figure 34. Using the AD208 in an Isolated RTD Application

Gain Adjustment. Since the output stage of the AD208 is unbuffered, any desired output gain adjustments can only be made in a subsequent stage.

USING ISOLATED POWER

The AD208 provides ±8.0 V dc power outputs referred to the input common. These may be used to power various accessory circuits which must operate at the input common mode level. The input offset adjustment circuits of the previous section are examples of this need.

The isolated power output has a current capacity of up to 5 mA which should be sufficient to operate adjustment circuits, references, op amps, signal conditioners or remote transducers.

CAUTION: The AD208 design does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICATION EXAMPLES

Isolated RTD Signal Processing. The stable high gain properties and low offset drift characteristics make the AD208 an ideal component for use in isolated RTD signal processing applications. RTD applications typically require the following three major elements: a stable current excitation source, a lead compensation network and a zero suppression network. The circuit schematic of Figure 34 illustrates how to use the AD208 with a handful of low power external components to condition, amplify and isolate low level RTD signals.

In the RTD application shown in Figure 34, the stable current excitation source needed to drive the RTD consists of a:

- Dual, single supply op amp (LM358)
- Pair of low V_{GSOFF} JFETS (ex. J201)
- Low power 2.5 V reference source
- Several precision 10 kΩ, 1%, 10 ppm/°C resistors.

The dual current sources generate a 250 μA excitation signal for the RTD and they also provide about 5 V of compliance with a ±5% gain adjustment range.

Zero suppression is accomplished in Figure 34 by using a simple ground servo amplifier in combination with the resistor labelled R_Z, while lead wire compensation is realized by remote sensing the RTD with the ground servo. The current, I_{S1} develops a voltage V_1 that is equal to:

$$V_1 = V_{OS_{A1}} + V_Z + V_{LEAD}$$

where the voltages V_1, $V_{OS_{A1}}$, V_Z and V_{LEAD} are as indicated in Figure 34.

The current I_{S2}, in turn, develops the voltage seen by the input amplifier of the AD208 and, with reference to the voltages labelled in Figure 34, V_{IN} is given by:

$$\begin{aligned} V_{IN} &= V_1 - V_{RTD} - V_{LEAD} \\ &= (V_{OS_{A1}} + V_Z + V_{LEAD}) - V_{RTD} - V_{LEAD} \\ &= V_{OS_{A1}} + V_Z - V_{RTD}. \end{aligned}$$

The offset trim circuit can then be used to null out all of the offset terms. Note that a high quality low power, low offset drift amplifier should be used for the ground servo amplifier.

The typical sensitivity of a 100 Ω platinum RTD with a 0.25 mA current excitation is in the 95 μV/°C range. Therefore, using the AD208 isolation amplifier with a gain of 105 V/V will result in an approximate output sensitivity of 10 mV/°C which corresponds to a 0 to 500°C RTD range for a 0 to −5 V output span. If a 0 to +5 V output span is desired, simply reverse the OUT LO (Pin 37) and OUT HI (Pin 38) terminals of the AD208 taking care to ensure that the OUT LO pin is now connected to the CLK COM terminal.

The gain equation for the circuit of Figure 34 is determined by the formula given below.

$$\frac{V_O\,(HI) - V_O\,(LO)}{I_S \cdot (\Omega_{RTD}\,(HI) - \Omega_{RTD}\,(LO))} = R_F/R_I + 1$$

where:

V_O (HI) = AD208 output voltage at the maximum expected temperature seen by the RTD application

V_O (LO) = AD208 output voltage at the minimum expected temperature seen by the RTD application

Ω_{RTD} (HI) = Resistance of the RTD at the maximum expected temperature

Ω_{RTD} (LO) = Resistance of the RTD at the minimum expected temperature

R_Z = RTD resistance at 0°C (100 Ω, typ)

I_S = Current of the stable excitation source (0.25 mA)

R_F = Feedback resistor (10.5 kΩ)

R_I = Input resistor (100 Ω, 1%, 10 ppm/°C).

The circuit of Figure 34 accommodates a 10 mV/°C, unlinearized output for a 100 Ω platinum RTD. The circuit allows for a maximum measured temperature range of 500°C. The initial input offset is ±1.3 mV (max) which is roughly equivalent to 5.2 Ω. The offset adjustment circuit, which has a ±1.5 mV (RTI) adjustment range, can be used to easily trim out this initial offset. The offset drift of the RTD application shown in Figure 34 is ±4 μV/°C (max) or 0.016 Ω/°C.

Thermocouple Applications. Thermocouples provide an inexpensive and reliable way to measure temperature over a wide range. Thermocouples require high gain amplification and in some cases cold junction compensation. The circuit of Figure 35 shows how the stable high gain capability of the AD208 can be effectively utilized to amplify and isolate the low level voltage signals from a thermocouple. The AC1226 Monolithic Cold Junction Compensator is recommended for use in this application. The AC1226 acts to eliminate the cold junction voltage that is formed between the thermocouple wire and the actual measurement circuit. The AC1226 outputs 0 V at 0°C and it provides the correct compensation slope for many thermocouple types through user selected taps off of the internal AC1226 resistor string.

The gain and offset adjustment for the circuit shown in Figure 35 is easily accomplished by first shorting the AD208 inputs to ground (IN COM) and adjusting the offset potentiometer until 0 V is measured at the output. Once the offset has been

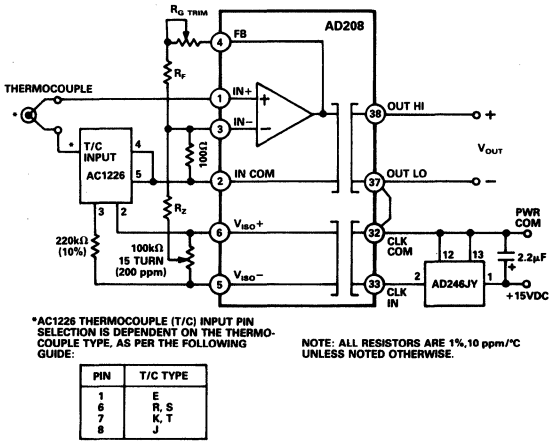


Figure 35. Using the AD208 in an Isolated Thermocouple Application

nulled out, the gain adjustment can then be initiated by applying an appropriate full-scale voltage, for the thermocouple type being used, at the input. Then adjust the gain trim until measuring +5 V out. The offset and gain trim do interact slightly with each other consequently, it would be advisable to recheck the offset error and readjust it if necessary. The residual error that may be introduced by the AC1226 at 25°C will be no more than ±2°C off nominal for all temperature ranges specified in Table II.

Table II lists the most commonly used thermocouple types along with their typical temperature ranges and a suggested AD208 gain setting. The table also includes recommended values for the feedback resistor (R_F), the gain trim resistor ($R_{G_{TRIM}}$) and the offset adjustment resistor (R_Z) all three of which are shown in Figure 35.

Thermocouple Type	Maximum Temperature Range @ 5 V Out (°C)	Maximum V_{IN} (mV)	AD208 Gain Setting (V/V)	SUGGESTED RESISTOR VALUES (With Reference to Figure 38) R_F (kΩ)	$R_{G_{TRIM}}$ (kΩ)	R_Z (MΩ)
E	900	68.783	72.69	6.98	0.5	2.0
J	750	42.283	118.25	11.5	1.0	2.0
K	1,250	50.633	98.75	9.53	1.0	2.0
R	1,450	16.741	298.6	28.7	2.0	2.0
S	1,450	14.973	333.9	32.4	2.0	2.0
T	350	17.816	280.6	27.4	2.0	2.0

Table II. Commonly Used Thermocouple Types, Temperature Ranges, AD208 Gain Settings and Circuit Resistor Values

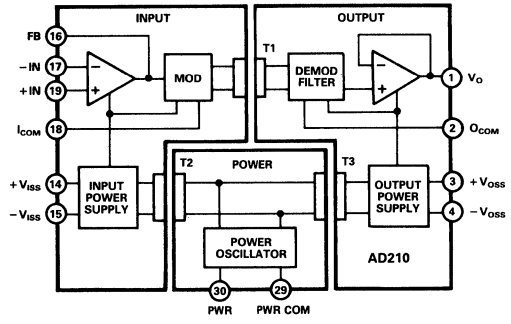
Precision, Wide Bandwidth, 3-Port Isolation Amplifier

AD210*

FEATURES
High CMV Isolation: 2500V RMS Continuous
±3500V Peak Continuous
Small Size: 1.00″ × 2.10″ × 0.350″
Three-Port Isolation: Input, Output, and Power
Low Nonlinearity: ±0.012% max
Wide Bandwidth: 20kHz Full-Power (−3dB)
Low Gain Drift: ±25ppm/°C max
High CMR: 120dB (G = 100V/V)
Isolated Power: ±15V @ ±5mA
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
High Voltage Instrumentation Amplifier
Current Shunt Measurements
Process Signal Isolation

AD210 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD210 is the latest member of a new generation of low cost, high performance isolation amplifiers. This three-port, wide bandwidth isolation amplifier is manufactured with surface-mounted components in an automated assembly process. The AD210 combines design expertise with state-of-the-art manufacturing technology to produce an extremely compact and economical isolator whose performance and abundant user features far exceed those offered in more expensive devices.

The AD210 provides a complete isolation function with both signal and power isolation supplied via transformer coupling internal to the module. The AD210's functionally complete design, powered by a single +15V supply, eliminates the need for an external DC/DC converter, unlike optically coupled isolation devices. The true three-port design structure permits the AD210 to be applied as an input or output isolator, in single or multichannel applications. The AD210 will maintain its high performance under sustained common-mode stress.

Providing high accuracy and complete galvanic isolation, the AD210 interrupts ground loops and leakage paths, and rejects common-mode voltage and noise that may otherwise degrade measurement accuracy. In addition, the AD210 provides protection from fault conditions that may cause damage to other sections of a measurement system.

PRODUCT HIGHLIGHTS

The AD210 is a full-featured isolator providing numerous user benefits including:

High Common-Mode Performance: The AD210 provides 2500V rms (Continuous) and ±3500V peak (Continuous) common-mode voltage isolation between any two ports. Low input to output capacitance of 5pF results in a 120dB CMR at a gain of 100, and a low leakage current (2μA rms max @ 240V rms, 60Hz).

High Accuracy: With maximum nonlinearity of ±0.012% (B Grade), gain drift of ±25ppm/°C max, and input offset drift of (±10±30/G) μV/°C, the AD210 assures signal integrity while providing high level isolation.

Wide Bandwidth: The AD210's full-power bandwidth of 20kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Small Size: The AD210 provides a complete isolation function in a small DIP package just 1.00″ × 2.10″ × 0.350″. The low profile DIP package allows application in 0.5″ card racks and assemblies. The pinout is optimized to facilitate board layout while maintaining isolation spacing between ports.

Three-Port Design: The AD210's three-port design structure allows each port (Input, Output, and Power) to remain independent. This three-port design permits the AD210 to be used as an input or output isolator. It also provides additional system protection should a fault occur in the power source.

Isolated Power: ±15V @ 5mA is available at the input and output sections of the isolator. This feature permits the AD210 to excite floating signal conditioners, front-end amplifiers and remote transducers at the input as well as other circuitry at the output.

Flexible Input: An uncommitted operational amplifier is provided at the input. This amplifier provides buffering and gain as required, and facilitates many alternative input functions as required by the user.

***Covered by U.S. Patent No. 4,703,283.**

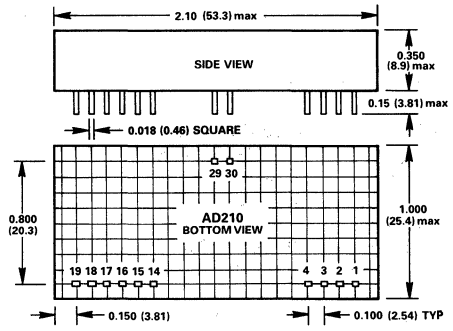
SPECIFICATIONS (typical @ + 25°C, & V_S = +15V unless otherwise specified)

Model	AD210AN	AD210BN	AD210JN
GAIN			
Range	1V/V – 100V/V	*	*
Error	± 2% max	± 1% max	*
vs. Temperature (0 to + 70°C)	± 25ppm/°C max	*	*
(– 25°C to + 85°C)	± 50ppm/°C max	*	*
vs. Supply Voltage	± 0.002%/V	*	*
Nonlinearity[1]	± 0.025% max	± 0.012% max	*
Nonlinearity vs. Isolated Supply Load	± 0.002%/mA	*	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	± 10V	*	*
Maximum Safe Differential Input	± 15V	*	*
Max. CMV Input-to-Output			
ac, 60Hz, Continuous	2500V rms	*	1500V rms
dc, Continuous	± 3500V peak	*	± 2000V peak
Common-Mode Rejection			
60Hz, G = 100V/V			
$R_S \leq 500\Omega$ Impedance Imbalance	120dB	*	*
Leakage Current Input-to-Output			
@ 240Vrms, 60Hz	2μA rms max	*	*
INPUT IMPEDANCE			
Differential	$10^{12}\Omega$	*	*
Common Mode	$5G\Omega \| 5pF$	*	*
INPUT BIAS CURRENT			
Initial, @ + 25°C	30pA typ (400pA max)	*	*
vs. Temperature (0 to + 70°C)	10nA max	*	*
(– 25°C to + 85°C)	30nA max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ + 25°C	5pA typ (200pA max)	*	*
vs. Temperature (0 to + 70°C)	2nA max	*	*
(– 25°C to + 85°C)	10nA max	*	*
INPUT NOISE			
Voltage (1kHz)	$18nV/\sqrt{Hz}$	*	*
(10Hz to 10kHz)	4μV rms	*	*
Current (1kHz)	$0.01pA/\sqrt{Hz}$	*	*
FREQUENCY RESPONSE			
Bandwidth (– 3dB)			
G = 1V/V	20kHz	*	*
G = 100V/V	15kHz	*	*
Settling Time (± 10mV, 20V Step)			
G = 1V/V	150μs	*	*
G = 100V/V	500μs	*	*
Slew Rate (G = 1V/V)	1V/μs	*	*
OFFSET VOLTAGE (RTI)[2]			
Initial, @ + 25°C	(± 15 ± 45/G)mV max	(± 5 ± 15/G)mV max	
vs. Temperature (0 to + 70°C)	(± 10 ± 30/G)μV/°C	*	*
(– 25°C to + 85°C)	(± 10 ± 50/G)μV/°C	*	*
RATED OUTPUT[3]			
Voltage, 2kΩ Load	± 10V min	*	*
Impedance	1Ω max	*	*
Ripple, (Bandwidth = 100kHz)	10mV p-p max	*	*
ISOLATED POWER OUTPUTS[4]			
Voltage, No Load	± 15V	*	*
Accuracy	± 10%	*	*
Current	± 5mA	*	*
Regulation, No Load to Full Load	See Text	*	*
Ripple	See Text	*	*
POWER SUPPLY			
Voltage, Rated Performance	+ 15V dc ± 5%	*	*
Voltage, Operating	+ 15V dc ± 10%	*	*
Current, Quiescent	50mA	*	*
Current, Full Load – Full Signal	80mA	*	*
TEMPERATURE RANGE			
Rated Performance	– 25°C to + 85°C	*	*
Operating	– 40°C to + 85°C	*	*
Storage	– 40°C to + 85°C	*	*
PACKAGE DIMENSIONS			
Inches	1.00 × 2.10 × 0.350	*	*
Millimeters	25.4 × 53.3 × 8.9	*	*

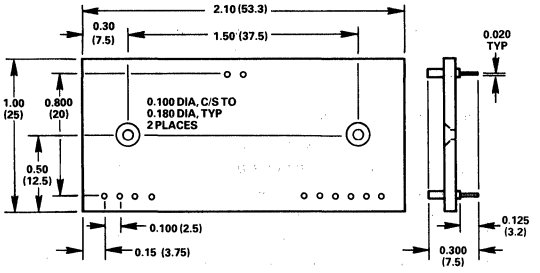
NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]RTI – Referred to Input
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1059 Mating Socket



AD210 Pin Designations

PIN	DESIGNATION	FUNCTION
1	V_O	Output
2	O_{COM}	Output Common
3	$+V_{OSS}$	+ Isolated Power @ Output
4	$-V_{OSS}$	– Isolated Power @ Output
14	$+V_{ISS}$	+ Isolated Power @ Input
15	$-V_{ISS}$	– Isolated Power @ Input
16	FB	Input Feedback
17	– IN	– Input
18	I_{COM}	Input Common
19	+ IN	+ Input
29	Pwr Com	Power Common
30	Pwr	Power Input

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

INSIDE THE AD210

The AD210 basic block diagram is illustrated in Figure 1. A +15V supply is connected to the power port, and ±15V isolated power is supplied to both the input and output ports via a 50kHz carrier frequency. The uncommitted input amplifier can be used to supply gain or buffering of input signals to the AD210. The fullwave modulator translates the signal to the carrier frequency for application to transformer T1. The synchronous demodulator in the output port reconstructs the input signal. A 20kHz, three-pole filter is employed to minimize output noise and ripple. Finally, an output buffer provides a low impedance output capable of driving a 2kΩ load.

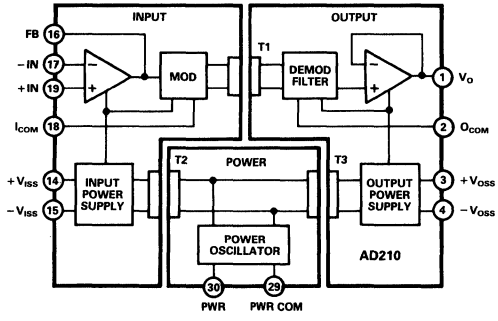


Figure 1. AD210 Block Diagram

USING THE AD210

The AD210 is very simple to apply in a wide range of applications. Powered by a single +15V power supply, the AD210 will provide outstanding performance when used as an input or output isolator, in single and multichannel configurations.

Input Configurations: The basic unity gain configuration for signals up to ±10V is shown in Figure 2. Additional input amplifier variations are shown in the following figures. For smaller signal levels Figure 3 shows how to obtain gain while maintaining a very high input impedance.

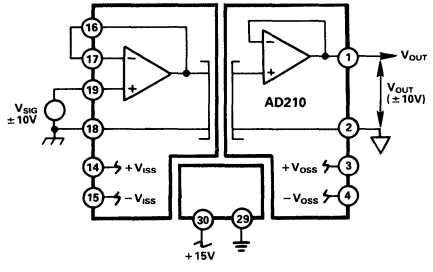


Figure 2. Basic Unity Gain Configuration

The high input impedance of the circuits in Figures 2 and 3 can be maintained in an inverting application. Since the AD210 is a three-port isolator, either the input leads or the output leads may be interchanged to create the signal inversion.

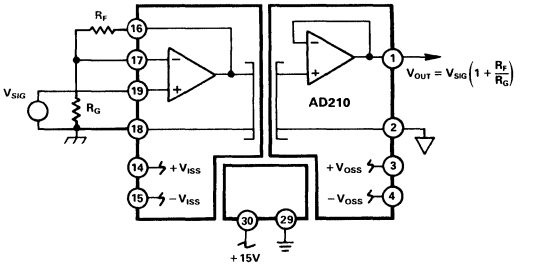


Figure 3. Input Configuration for G>1

Figure 4 shows how to accommodate current inputs or sum currents or voltages. This circuit configuration can also be used for signals greater than ±10V. For example, a ±100V input span can be handled with $R_F = 20k\Omega$ and $R_{S1} = 200k\Omega$.

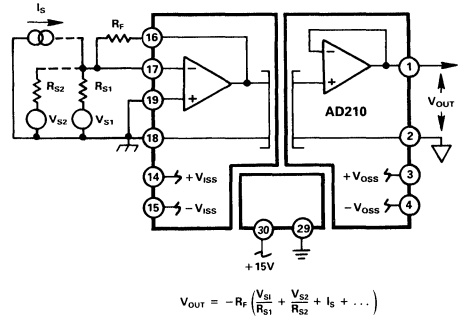


Figure 4. Summing or Current Input Configuration

Adjustments

When gain and offset adjustments are required, the actual circuit adjustment components will depend on the choice of input configuration and whether the adjustments are to be made at the isolator's input or output. Adjustments on the output side might be used when potentiometers on the input side would represent a hazard due to the presence of high common-mode voltage during adjustment. Offset adjustments are best done at the input side, as it is better to null the offset ahead of the gain.

Figure 5 shows the input adjustment circuit for use when the input amplifier is configured in the noninverting mode. This offset adjustment circuit injects a small voltage in series with the

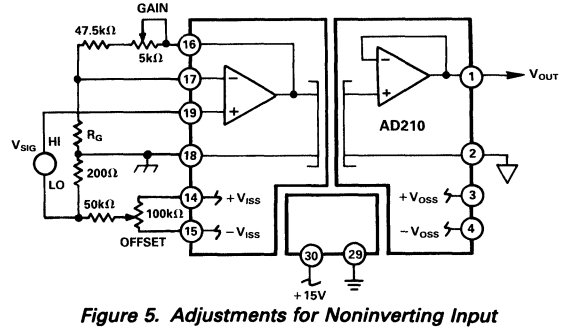


Figure 5. Adjustments for Noninverting Input

low side of the signal source. This will not work if the source has another current path to input common or if current flows in the signal source LO lead. To minimize CMR degradation, keep the resistor in series with the input LO below a few hundred ohms.

Figure 5 also shows the preferred gain adjustment circuit. The circuit shows R_F of 50kΩ, and will work for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G=2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G=1 (follower) the gain cannot be adjusted downward without compromising input impedance; it is better to adjust gain at the signal source or after the output.

Figure 6 shows the input adjustment circuit for use when the input amplifier is configured in the inverting mode. The offset adjustment nulls the voltage at the summing node. This is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is made in the feedback and will work for gains from 1 to 100V/V.

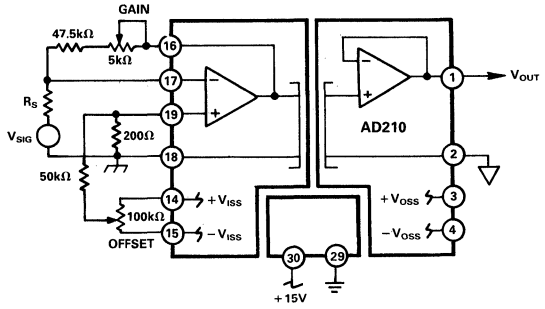


Figure 6. Adjustments for Inverting Input

Figure 7 shows how offset adjustments can be made at the output, by offsetting the floating output port. In this circuit, ±15V would be supplied by a separate source. The AD210's output amplifier is fixed at unity, therefore, output gain must be made in a subsequent stage.

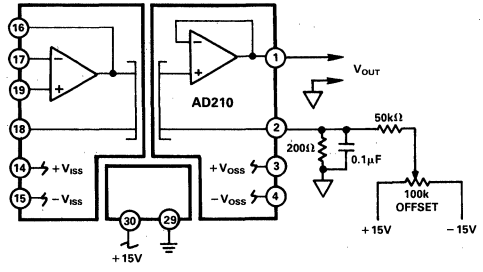


Figure 7. Output-Side Offset Adjustment

PCB Layout for Multichannel Applications: The unique pinout positioning minimizes board space constraints for multichannel applications. Figure 8 shows the recommended printed circuit board layout for a noninverting input configuration with gain.

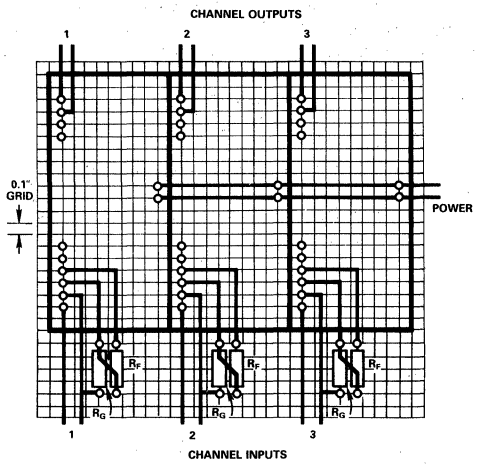


Figure 8. PCB Layout for Multichannel Applications with Gain

Synchronization: The AD210 is insensitive to the clock of an adjacent unit, eliminating the need to synchronize the clocks. However, in rare instances channel to channel pick-up may occur if input signal wires are bundled together. If this happens, shielded input cables are recommended.

PERFORMANCE CHARACTERISTICS

Common-Mode Rejection: Figure 9 shows the common-mode rejection of the AD210 versus frequency, gain and input source resistance. For maximum common-mode rejection of unwanted signals, keep the input source resistance low and carefully lay out the input, avoiding excessive stray capacitance at the input terminals.

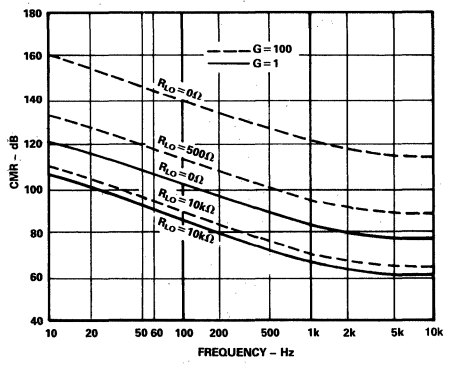


Figure 9. Common-Mode Rejection vs. Frequency

Phase Shift: Figure 10 illustrates the AD210's low phase shift and gain versus frequency. The AD210's phase shift and wide bandwidth performance make it well suited for applications like power monitors and controls systems.

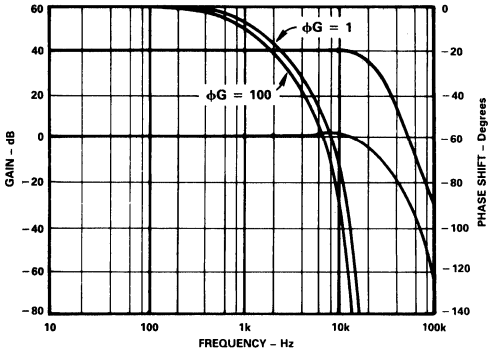


Figure 10. Phase Shift and Gain vs. Frequency

Input Noise vs. Frequency: Voltage noise referred to the input is dependent on gain and signal bandwidth. Figure 11 illustrates the typical input noise in nV/$\sqrt{\text{Hz}}$ of the AD210 for a frequency range from 10 to 10kHz.

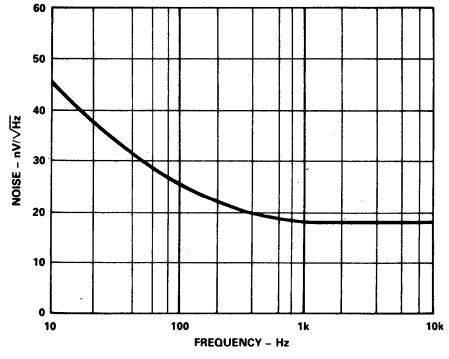


Figure 11. Input Noise vs. Frequency

Gain Nonlinearity vs. Output: Gain nonlinearity is defined as the deviation of the output voltage from the best straight line, and is specified as % peak-to-peak of output span. The AD210B provides guaranteed maximum nonlinearity of ±0.012% with an output span of ± 10V. The AD210's nonlinearity performance is shown in Figure 12.

Gain Nonlinearity vs. Output Swing: The gain nonlinearity of the AD210 varies as a function of total signal swing. When the output swing is less than 20 volts, the gain nonlinearity as a fraction of signal swing improves. The shape of the nonlinearity remains constant. Figure 13 shows the gain nonlinearity of the AD210 as a function of total signal swing.

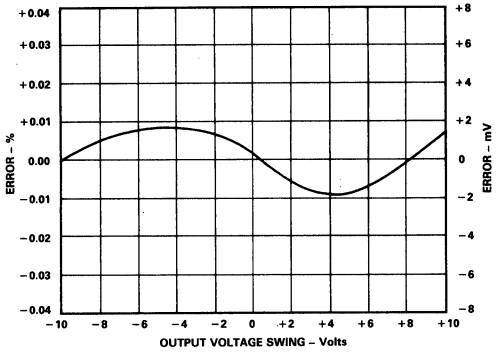


Figure 12. Gain Nonlinearity Error vs. Output

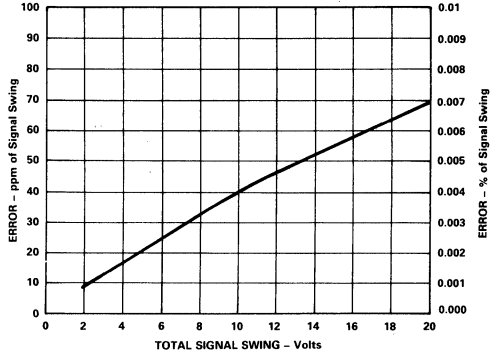


Figure 13. Gain Nonlinearity vs. Output Swing

Gain vs. Temperature: Figure 14 illustrates the AD210's gain vs. temperature performance. The gain versus temperature performance illustrated is for an AD210 configured as a unity gain amplifier.

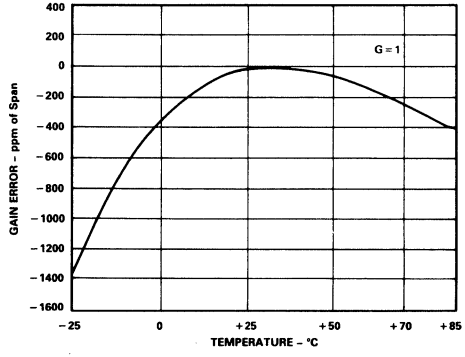


Figure 14. Gain vs. Temperature

Isolated Power: The AD210 provides isolated power at the input and output ports. This power is useful for various signal conditioning tasks. Both ports are rated at a nominal ±15V at 5mA.

The load characteristics of the isolated power supplies are shown in Figure 15. For example, when measuring the load rejection of the input isolated supplies V_{ISS}, the load is placed between $+V_{ISS}$ and $-V_{ISS}$. The curves labeled V_{ISS} and V_{OSS} are the individual load rejection characteristics of the input and the output supplies, respectively.

There is also some effect on either isolated supply when loading the other supply. The curve labeled CROSSLOAD indicates the sensitivity of either the input or output supplies as a function of the load on the opposite supply.

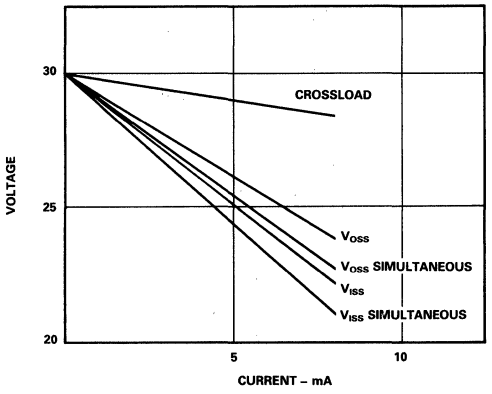


Figure 15. Isolated Power Supplies vs. Load

Lastly, the curves labeled V_{OSS} simultaneous and V_{ISS} simultaneous indicate the load characteristics of the isolated power supplies when an equal load is placed on both supplies.

The AD210 provides short circuit protection for its isolated power supplies. When either the input supplies or the output supplies are shorted to input common or output common, respectively, no damage will be incurred, even under continuous application of the short. However, the AD210 may be damaged if the input and output supplies are shorted simultaneously.

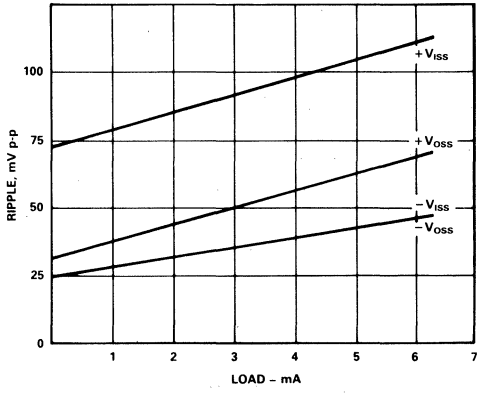


Figure 16a. Isolated Supply Ripple vs. Load (External 4.7μF Bypass)

Under any circumstances, care should be taken to ensure that the power supplies do not accidentally become shorted.

The isolated power supplies exhibit some ripple which varies as a function of load. Figure 16a shows this relationship. The AD210 has internal bypass capacitance to reduce the ripple to a point where performance is not affected, even under full load. Since the internal circuitry is more sensitive to noise on the negative supplies, these supplies have been filtered more heavily. Should a specific application require more bypassing on the isolated power supplies, there is no problem with adding external capacitors. Figure 16b depicts supply ripple as a function of external bypass capacitance under full load.

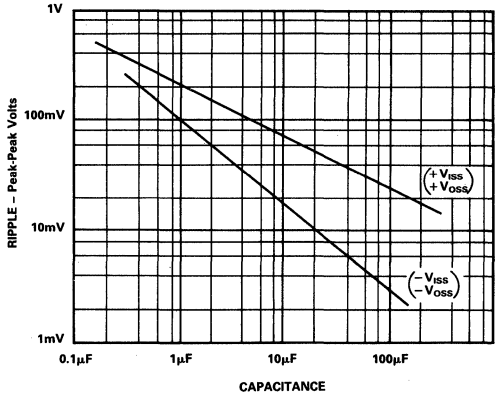


Figure 16b. Isolated Power Supply Ripple vs. Bypass Capacitance (Volts p-p, 1MHz Bandwidth, 5mA Load)

APPLICATIONS EXAMPLES

Noise Reduction in Data Acquisition Systems: Transformer coupled isolation amplifiers must have a carrier to pass both ac and dc signals through their signal transformers. Therefore, some carrier ripple is inevitably passed through to the isolator output. As the bandwidth of the isolator is increased more of the carrier signal will be present at the output. In most cases, the ripple at the AD210's output will be insignificant when compared to the measured signal. However, in some applications, particularly when a fast analog-to-digital converter is used following the isolator, it may be desirable to add filtering; otherwise ripple may cause inaccurate measurements. Figure 17 shows a circuit that will limit the isolator's bandwidth, thereby reducing the carrier ripple.

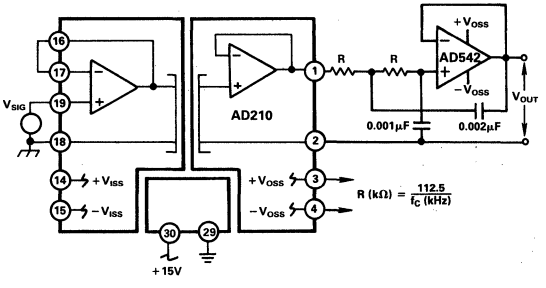


Figure 17. 2-Pole, Output Filter

Self-Powered Current Source

The output circuit shown in Figure 18 can be used to create a self-powered output current source using the AD210. The 2kΩ resistor converts the voltage output of the AD210 to an equivalent current $V_{OUT}/2k\Omega$. This resistor directly affects the output gain temperature coefficient, and must be of suitable stability for the application. The external low power op amp, powered by $+V_{OSS}$ and $-V_{OSS}$, maintains its summing junction at output common. All the current flowing through the 2kΩ resistor flows through the output Darlington pass devices. A Darlington configuration is used to minimize loss of output current to the base. The low leakage diode is used to protect the base-emitter junction against reverse bias voltages. Using $-V_{OSS}$ as a current return allows more than 10V of compliance. Offset and gain control may be done at the input of the AD210 or by varying the 2kΩ resistor and summing a small correction current directly into the summing node. A nominal range of 1-5mA is recommended since the current output cannot reach zero due to reverse bias and leakage currents. If the AD210 is powered from the input potential, this circuit provides a fully isolated, wide bandwidth current output. This configuration is limited to 5mA output current.

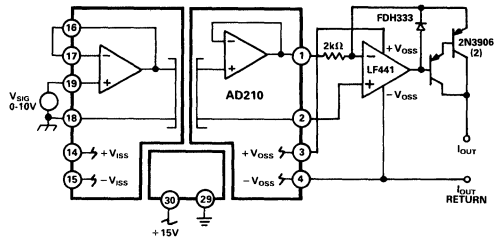


Figure 18. Self-Powered Isolated Current Source

Isolated V-to-I Converter

Illustrated in Figure 19, the AD210 is used to convert a 0 to +10V input signal to an isolated 4-20mA output current. The AD210 isolates the 0 to +10V input signal and provides a proportional voltage at the isolator's output. The output circuit converts the input voltage to a 4-20mA output current, which in turn is applied to the loop load R_{LOAD}.

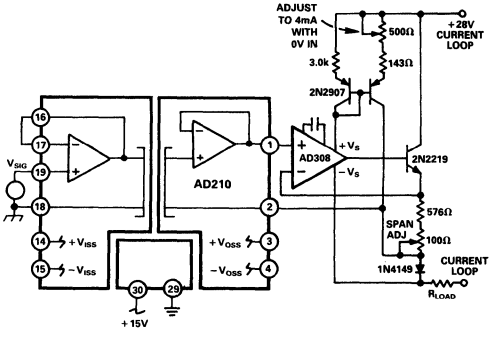


Figure 19. Isolated Voltage-to-Current Loop Converter

Isolated Thermocouple Amplifier

The AD210 application shown in Figure 20 provides amplification, isolation and cold-junction compensation for a standard J type thermocouple. The AD590 temperature sensor accurately monitors the input terminal (cold-junction). Ambient temperature changes from 0 to +40°C sensed by the AD590, are cancelled out at the cold junction. Total circuit gain equals 183; 100 and 1.83, from A1 and the AD210 respectively. Calibration is performed by replacing the thermocouple junction with plain thermocouple wire and a millivolt source set at 0.0000V (0°C) and adjusting R_O for E_{OUT} equal to 0.000V. Set the millivolt source to +0.02185V (400°C) and adjust R_G for V_{OUT} equal to +4.000V. This application circuit will produce a nonlinearized output of about +10mV/°C for a 0 to +400°C range.

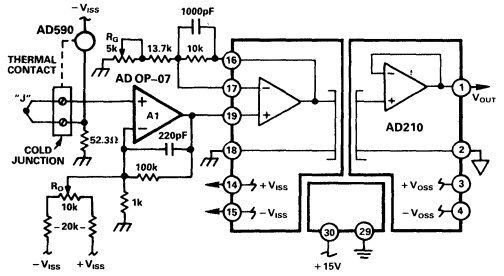


Figure 20. Isolated Thermocouple Amplifier

Precision Floating Programmable Reference

The AD210, when combined with a digital-to-analog converter, can be used to create a fully floating voltage output. Figure 21 shows one possible implementation.

The digital inputs of the AD7541 are TTL or CMOS compatible. Both the AD7541 and AD581 voltage reference are powered by the isolated power supply $+V_{ISS}$. I_{COM} should be tied to input digital common to provide a digital ground reference for the inputs.

The AD7541 is a current output DAC and, as such, requires an external output amplifier. The uncommitted input amplifier internal to the AD210 may be used for this purpose. For best results, its input offset voltage must be trimmed as shown.

The output voltage of the AD210 will go from 0V to −10V for digital inputs of 0 and full scale, respectively. However, since the output port is truly isolated, V_{OUT} and O_{COM} may be freely interchanged to get 0 to +10V.

This circuit provides a precision 0–10V programmable reference with a ±3500V common-mode range.

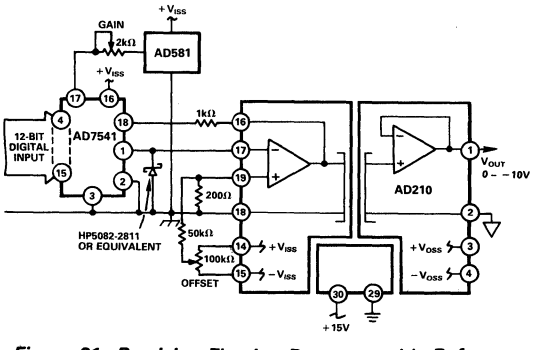


Figure 21. Precision Floating Programmable Reference

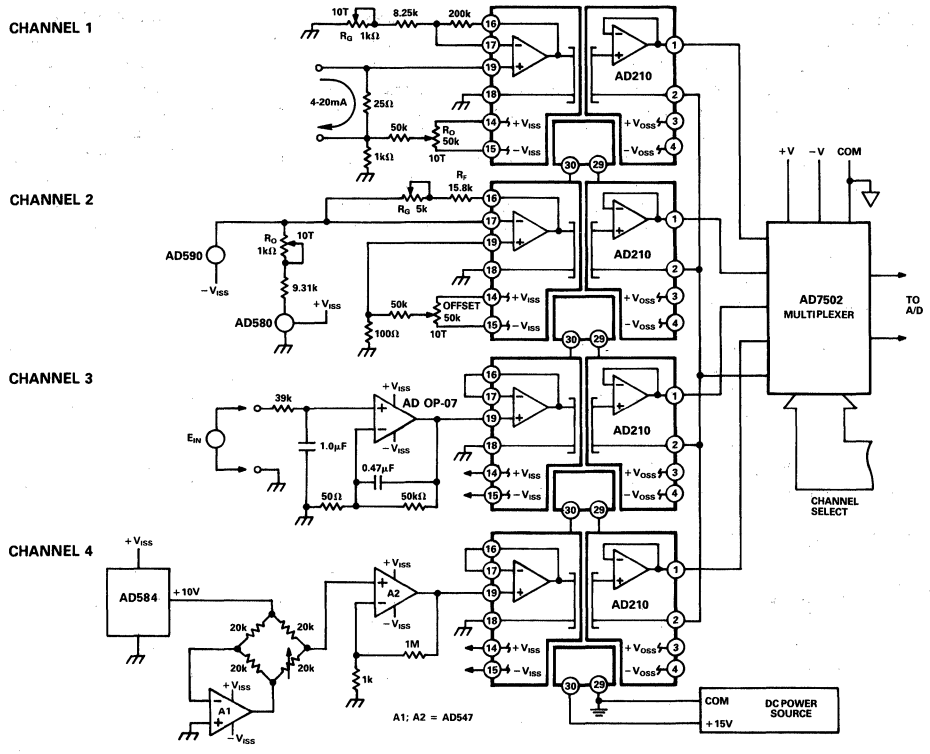


Figure 22. Multichannel Data Acquisition Front End

MULTICHANNEL DATA ACQUISITION FRONT-END

Illustrated in Figure 22 is a four-channel data acquisition front-end used to condition and isolate several common input signals found in various process applications. In this application, each AD210 will provide complete isolation from input to output as well as channel to channel. By using an isolator per channel, maximum protection and rejection of unwanted signals is obtained. The three-port design allows the AD210 to be configured as an input or output isolator. In this application the isolators are configured as input devices with the power port providing additional protection from possible power source faults.

Channel 1: The AD210 is used to convert a 4-20mA current loop input signal into a 0-10V input. The 25Ω shunt resistor converts the 4-20mA current into a +100 to +500mV signal. The signal is offset by −100mV via R_O to produce a 0 to +400mV input. This signal is amplified by a gain of 25 to produce the desired 0 to +10V output. With an open circuit, the AD210 will show −2.5V at the output.

Channel 2: In this channel, the AD210 is used to condition and isolate a current output temperature transducer, Model AD590. At +25°C, the AD590 produces a nominal current of 298.2μA. This level of current will change at a rate of 1μA/°C. At −17.8°C (0°F), The AD590 current will be reduced by 42.8μA to +255.4μA. The AD580 reference circuit provides an equal but opposite current, resulting in a zero net current flow, producing a 0V output from the AD210. At +100°C (+212°F), the AD590 current output will be 373.2μA minus the 255.4μA offsetting current from the AD580 circuit to yield a +117.8μA input current. This current is converted to a voltage via R_F and R_G to produce an output of +2.12V. Channel 2 will produce an output of +10mV/°F over a 0 to +212°F span.

Channel 3: Channel 3 is a low level input channel configured with a high gain amplifier used to condition millivolt signals. With the AD210's input set to unity and the input amplifier set for a gain of 1000, a ±10mV input will produce a ±10V at the AD210's output.

Channel 4: Channel 4 illustrates one possible configuration for conditioning a bridge circuit. The AD584 produces a +10V excitation voltage, while A1 inverts the voltage, producing negative excitation. A2 provides a gain of 1000V/V to amplify the low level bridge signal. Additional gain can be obtained by reconfiguration of the AD210's input amplifier. $\pm V_{ISS}$ provides the complete power for this circuit, eliminating the need for a separate isolated excitation source.

Each channel is individually addressed by the multiplexer's channel select. Additional filtering or signal conditioning should follow the multiplexer, prior to an analog-to-digital conversion stage.

ANALOG DEVICES

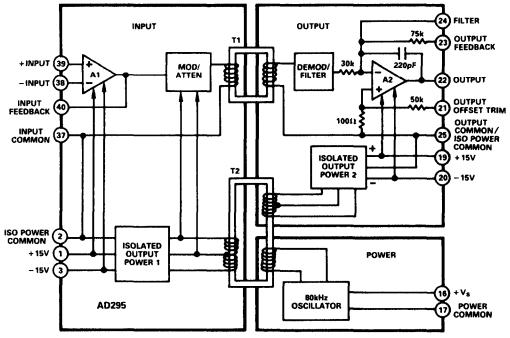
Precision, Hybrid Isolation Amplifier

AD295

FEATURES
Low Nonlinearity: ±0.012% max (AD295C)
Low Gain Drift: ±60ppm/°C max
Floating Input and Output Power: ±15V dc @ 5mA
3-Port Isolation: ±2500V CMV (Input to Output)
Complies with NEMA ICS1-111
Gain Adjustable: 1V/V to 1000V/V
User Configurable Input Amplifier

APPLICATIONS
Motor Controls
Process Signal Isolator
High Voltage Instrumentation Amplifier
Multichannel Data Acquisition Systems
Off Ground Signal Measurements

AD295 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The AD295 is a high accuracy, high reliability hybrid isolation amplifier designed for industrial, instrumentation and medical applications. Three performance versions are available offering guaranteed nonlinearity error at 10V p-p output: ±0.05% max (AD295A), ±0.025% max (AD295B), ±0.012% max (AD295C). Using a pulse width modulation technique the AD295 provides 3-port isolation between input, output and power supply ports. Using this technique, the AD295 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. Additionally, floating (isolated) power ±15V dc @ 5mA is available at both the input and output. The AD295's gain can be programmed at the input, output or both sections allowing for user flexibility. An uncommitted input amplifier allows configuration as a buffer, inverter, subtractor or differential amplifier.

The AD295 is provided in an epoxy sealed ceramic 40-pin package that insures quality performance, high stability and accuracy. Input/output pin spacing complies with NEMA (ICS1-111) separation specifications required for many industrial applications.

WHERE TO USE THE MODEL AD295

Industrial: The AD295 is designed for measuring signals in harsh industrial environments. The AD295 provides high accuracy with complete galvanic isolation and protection from transients or where ground fault currents or high common-mode voltages are present. The AD295 can be applied in process controllers, current loop receivers, motor controls and weighing systems.

Instrumentation: In data acquisition systems the AD295 provides common-mode rejection for conditioning thermocouples, strain gauges or other low-level signals where high performance and system protection is required.

Medical: In biomedical and patient monitoring equipment like diagnostic systems and blood pressure monitors, the AD295 provides protection from lethal ground fault currents. Low level signal recording and monitoring is achieved with the AD295's low input noise (2μV p-p @ G = 1000V/V) and high CMR (106dB @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Isolated power supply sections at the input and output provide ±15V dc @ 5mA. Isolated power is load regulated to 4%. This feature permits the AD295 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers at the input and external circuitry at the output. This eliminates the need for a separate dc/dc converter.

Input Amplifier: The uncommitted input amplifier allows the user to configure the input as a buffer, inverter, subtractor or differential amplifier to meet the application need.

Adjustable Gain: Gain can be selected at the input, output or both. Thus, circuit response can be tailored to the user's application. The AD295 provides the user with flexibility for circuit optimization without requiring external active components.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates the need for power supply and output ports being returned through a common ground.

Wide Operating Temperature: The AD295 is designed to operate over the −40°C to +100°C temperature range with rated performance over −25°C to +85°C.

Leakage: The low coupling capacitance between input and output yields a ground leakage current of less than 2μA rms at 115V ac, 60Hz. The AD295 meets standards established by UL STD 544.

SPECIFICATIONS (typical @ +25°C, & V_S = +15V unless otherwise noted)

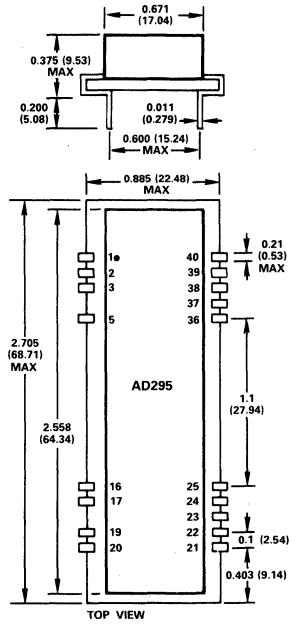
Model	AD295A	AD295B	AD295C
GAIN			
Range	1V/V to 1000V/V	*	*
Open Loop	100dB	*	*
Accuracy G = 1V/V	±1.5%	*	*
vs. Temperature (−25°C to +85°C)			
G = 1V/V to 100V/V	±60ppm/°C max	*	*
Nonlinearity (±5V Swing) G = 1V–100V/V	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range	±10V min	*	*
Max Safe Differential Input	±15V	*	*
Max CMV (Input to Output)			
Continuous ac or dc	±2500V peak	*	*
ac, 60Hz, 1 Minute Duration	2500V rms	*	*
Max CMV (Input to Power Common/Output to Power Common)			
Continuous ac or dc	±2000V peak	*	*
ac, 60Hz, 1 Minute Duration	2000V rms	*	*
CMR, Input to Output 60Hz, G = 1V/V			
$R_S \leq 1k\Omega$ Balanced Source Impedance	106dB	*	*
$R_S \leq 1k$ Source Impedance Imbalance	103dB min	*	*
Max Leakage Current, Input to Output @ 115V ac, 60Hz	2μA rms max	*	*
INPUT IMPEDANCE			
Differential	$5 \times 10^7\Omega \| 33pF$	*	*
Common Mode	$10^8\Omega \| 20pF$	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	5nA max	*	*
vs. Temperature (−25°C to +85°C)	−25pA/°C max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	±2nA max	*	*
vs. Temperature (−25°C to +85°C)	±5pA/°C max	*	*
INPUT NOISE (Gain = 1000V/V)			
Voltage			
0.01Hz to 10Hz	2μV p-p	*	*
10Hz to 1kHz	1μV rms	*	*
Current			
0.01Hz to 10Hz	10pA p-p	*	*
FREQUENCY RESPONSE			
Small Signal (−3dB)			
G = 1V/V to 100V/V	4.5kHz	*	*
G = 1000V/V	600Hz	*	*
Full Power, 20V p-p Output			
G = 1V/V to 100V/V	1.4kHz	*	*
G = 1000V/V	200Hz	*	*
Slew Rate G = 1V/V to 100V/V	0.1V/μs	*	*
Settling Time G = 1V/V			
(to ±0.1% for 10V Step)	550μs	*	*
(to ±0.1% for 20V Step)	700μs	*	*
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial @ +25°C (Adjustable to Zero)	$\pm\left(3+\frac{15}{G_{IN}}\right)$ mV max	*	*
vs. Temperature (−25°C to +85°C)	$\pm\left(10+\frac{450}{G_{IN}}\right)\frac{\mu V/°C}{max}$	$\pm\left(3+\frac{300}{G_{IN}}\right)\frac{\mu V/°C}{max}$	$\pm\left(1.5+\frac{150}{G_{IN}}\right)\frac{\mu V/°C}{max}$
vs. Supply	$\pm\left(1+\frac{200}{G_{IN}}\right)$ μV/%	*	*
RATED OUTPUT			
Voltage, 2kΩ Load	±10V min	*	*
Output Impedance	2Ω (dc to 100Hz)	*	*
Output Ripple (10Hz to 10kHz)	6mV p-p	*	*
(10Hz to 100kHz)	40mV p-p	*	*
ISOLATED POWER SUPPLIES[1] (V_{ISO1} & V_{ISO2})			
Voltage	±15V dc	*	*
Accuracy	±5%	*	*
Current[2]	±5mA max	*	*
Load Regulation (No Load to Full Load)	−4%	*	*
Ripple, 100kHz BW	12mV p-p	*	*
POWER SUPPLY (+V_S)			
Voltage, Rated Performance	+15V dc ±3%	*	*
Voltage, Operating	+12V dc to +16V dc	*	*
Current, Quiescent (V_S = +15V)	40mA	*	*
With V_{ISO} Loaded	45mA	*	*
TEMPERATURE RANGE			
Rated Performance	−25°C to +85°C	*	*
Operating	−40°C to +100°C	*	*
Storage	−40°C to +100°C	*	*
CASE DIMENSIONS	2.7" × 0.88" × 0.375"	*	*

NOTES
[1] V_{ISO} accuracy and regulation 10%.
[2] ±10mA can be supplied by V_{ISO1}, if V_{ISO2} is not used.

*Specifications same as AD295A.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



RECOMMENDED MATING SOCKET: AC1220

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V (+V_{ISO1})	40	INPUT FEEDBACK
2	V_{ISO1} COM	39	+INPUT
3	−15V (−V_{ISO1})	38	−INPUT
		37	INPUT COM
5	NO CONNECTION	36	NO CONNECTION
16	+V_S	25	OUTPUT COM/ V_{ISO2} COM
17	POWER COMMON	24	FILTER
		23	OUTPUT FEEDBACK
19	+15V (+V_{ISO2})	22	OUTPUT
20	−15V (+V_{ISO2})	21	OUTPUT OFFSET TRIM

INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of the AD295, care must be taken to keep the capacitance balanced about the input terminals. Use twisted shielded cable for the input signal to reduce inductive and capacitive pick-up. During circuit layout or interassembly connections, twisted wire pairs are recommended for power input and signal output. For basic isolator connections, see Figure 1. Capacitors C1-C5 are required in all applications to achieve the low noise rating and provide adequate filtering of the power supply.

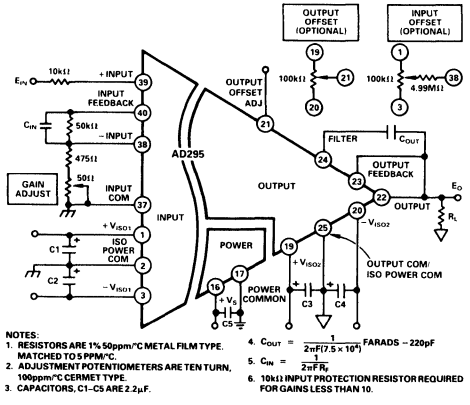


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The AD295 obtains its outstanding performance from a pulse width modulation technique using transformer coupling. This technique permits both signal and power transfer from input to the output stage of the isolator. Additionally, this technique provides higher noise immunity and lower nonlinearity than obtained from optically coupled or amplitude modulated transformer coupled techniques.

The three basic sections of the AD295 are shown in Figure 2. The power section 80kHz oscillator signal is transferred to the input and output sections via T2. The signal is then rectified and filtered providing dc power for that section's circuitry and for external application use. The input section consists of input amplifier A1 and the input modulator attenuator circuit. A triangular waveform derived from the 80kHz oscillator is sent to the modulator. If the input signal of A1 is zero, the triangle wave remains symmetrical. If A1 moves away from zero, the triangle wave moves positive or negative becoming asymmetrical. These modulated signals are converted to a pulsed waveform and transferred to the output section via T1. In the output section the signals are demodulated and filtered. The output amplifier A2 provides gain and additional filtering.

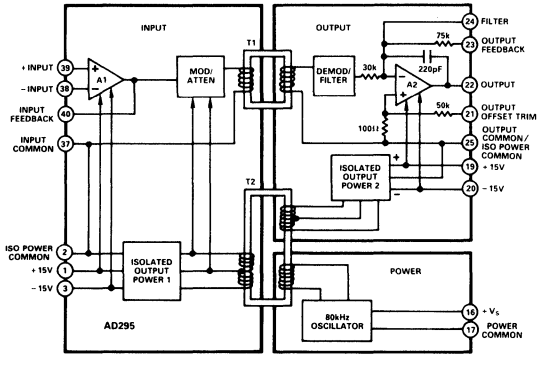


Figure 2. Basic Block Diagram

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance arises from stray coupling capacitance effects between the input terminals and signal output terminals. Each are shunted by leakage resistance values exceeding 50GΩ. Figure 3 illustrates the AD295's capacitance between terminals.

Terminal Ratings: CMV performance is given in both continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequency. Figure 3 illustrates the AD295's ratings between terminals. Note that for the ± 2500V rating between the input and output terminals to apply, the AD295 must be used in a three port configuration. If the output common is tied to the power common, the input to output CMV rating is ± 2000V.

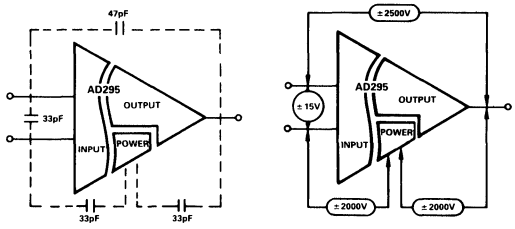


Figure 3. Interelectrode Capacitance and Terminal Ratings

OFFSET AND GAIN ADJUSTMENT PROCEDURE

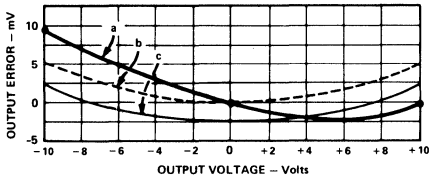
The calibration procedure, illustrated in Circuits 1 and 2, shows the recommended techniques that can be used to minimize output error. In this example, the output span is – 10V to + 10V.

Offset Adjustment

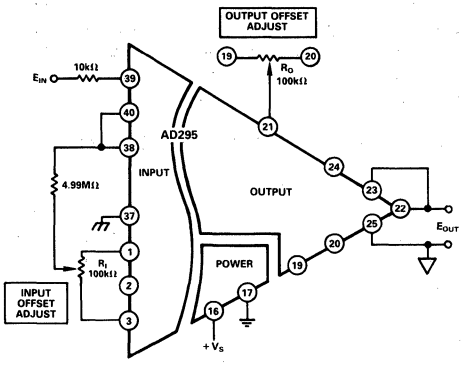
1. Configure the AD295 as shown in Circuit 1. G = 1.
2. Apply E_{IN} = 0V dc and adjust R_O for E_O = 0 volts.
3. Configure the AD295 as shown in Circuit 2. G = 100.
4. Apply E_{IN} = 0V dc and adjust R_I for E_O = 0 volts.
5. Repeat steps 1–4 if necessary.

Gain Adjust

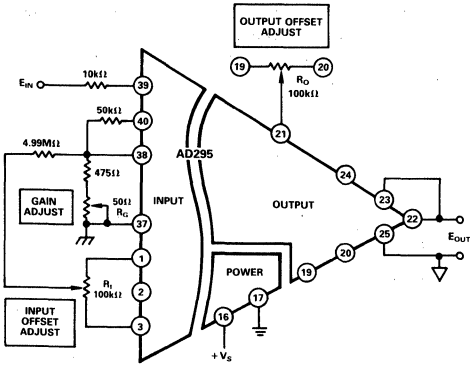
6. Apply E_{IN} = + 0.1V dc adjust R_G for E_0 = + 10.000V dc.
7. Apply E_{IN} = – 0.1V dc and measure the output error (see Curve a.)



8. Adjust R_G until the output error is one half that measured in step 6 (see Curve b).
9. Apply $E_{IN} = +0.1V$ dc and adjust R_O until the output error is one half that measured in step 7 (see Curve c).
10. Repeat steps 6–9 if necessary.



Circuit 1. G = 1



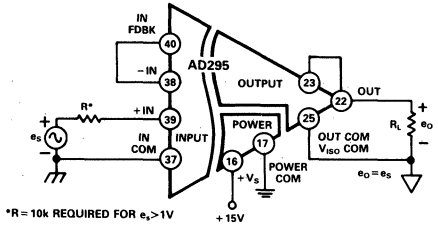
Circuit 2. G = 100

SELECTING GAIN

The AD295 basic gain is unity from input to output. All input signals are attenuated by 2.5 at the input modulator/attenuator then amplified at the output (see Figure 2).

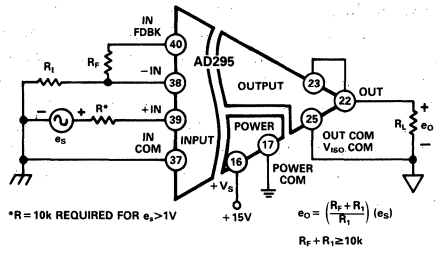
The AD295 contains both input and output amplifiers, the gains of which can be set independently. Figure 4 illustrates the basic gain configurations. Taking input gain helps dilute output stage offset drift and is recommended where offset drift is to be minimized since taking output gain multiplies output drift by the gain taken. Output gain can be used for improved linearity and frequency response at the expense of higher offset drift.

Figure 4a illustrates the basic unity gain configuration. With the uncommitted input amplifier configured as a buffer and pins 22 and 23 of the output amplifier jumpered, $e_O = e_S$.

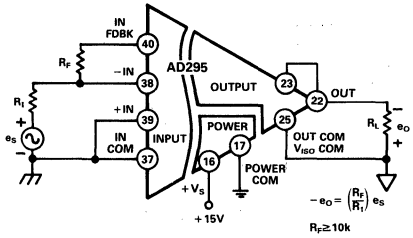


a. Basic Unity Gain Configuration

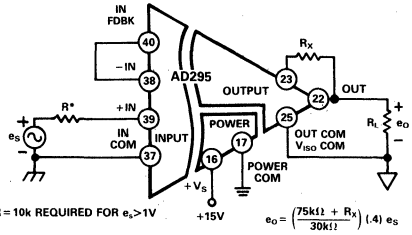
Input to output gain greater than unity can be independently set at the input, output, or both. For input gain configuration see Figures 4b and 4c. Output gain configuration is shown in Figure 4d.



b. Basic Gain Noninverting Configuration



c. Input Gain Inverting Configuration



d. Output Gain Noninverting Configuration

Figure 4. Input/Output Gain Configurations

PERFORMANCE CHARACTERISTICS

Phase Shift vs. Frequency: The phase shift vs. frequency response, for the AD295 is shown in Figure 5.

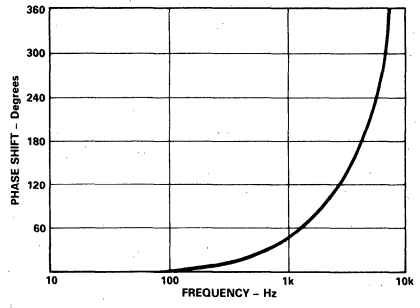


Figure 5. Typical AD295 – Phase Shift vs. Frequency

CMR vs. Frequency: Input-to-output CMR is dependent on source impedance imbalance, input signal frequency and amplifier gain. CMR is rated at 60Hz and 1kΩ source impedance imbalance at a gain of 1V/V. Figure 6 illustrates the CMR vs. frequency for the AD295. CMR approaches 120dB at dc with a source impedance imbalance of 1kΩ.

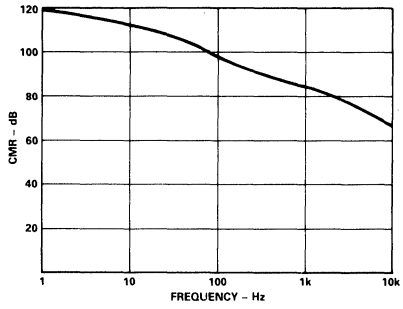


Figure 6. Typical AD295 – CMR vs. Frequency

Input Voltage Noise vs. Bandwidth: Voltage noise referred to the input is dependent on gain and bandwidth. Figure 7 illustrates the typical input noise in μV peak-to-peak in a 10Hz to 10kHz frequency range.

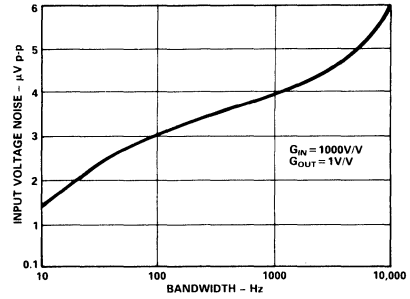


Figure 7. Typical AD295 – Input Voltage Noise vs. Bandwidth

Output Voltage Noise vs. Bandwidth: Voltage noise referred to the output is dependent on gain, bandwidth, input and output noise contributions. Figure 8 illustrates the typical output noise in mV peak-to-peak in a 10Hz to 10kHz frequency range.

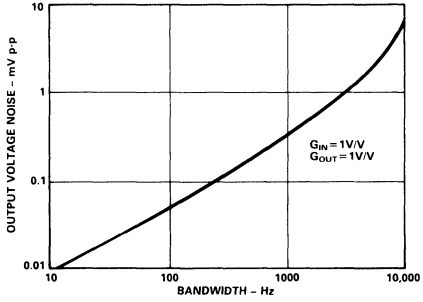


Figure 8. Typical AD295 – Output Voltage Noise vs. Bandwidth

Gain Nonlinearity vs. Output Swing: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as % peak-to-peak of output voltage span, e.g., nonlinearity of model AD295A operating at an output span of 10V peak-to-peak (±5V) is ±0.05% or ±5mV. Figure 9 illustrates the gain nonlinearity for output swing up to ±10V (20V peak-to-peak).

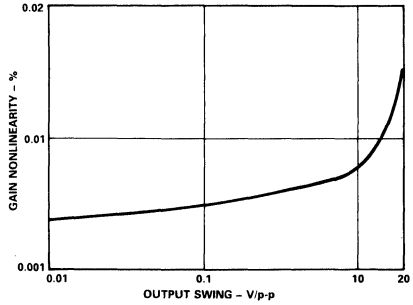


Figure 9. Typical AD295 – Gain Nonlinearity vs. Output Swing

Full Power Bandwidth vs. Gain: Figure 10 illustrates the full power bandwidth vs. gain for the AD295. A 1.4kHz full power response is possible with gain up to 100V/V.

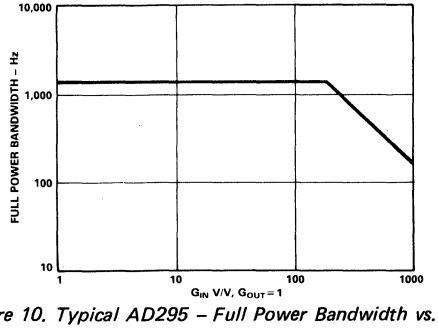


Figure 10. Typical AD295 – Full Power Bandwidth vs. Gain

Small Signal Bandwidth vs. Gain: Figure 11 illustrates the small signal bandwidth vs. gain for the AD295. The small signal response remains at 4.5kHz for gain up to 100V/V.

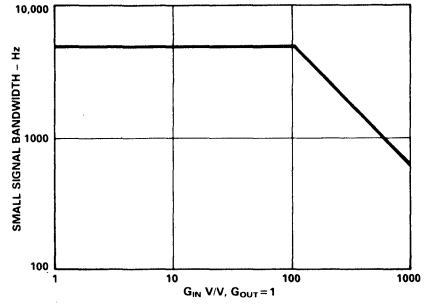


Figure 11. Typical AD295 – Small Signal Bandwidth vs. Gain

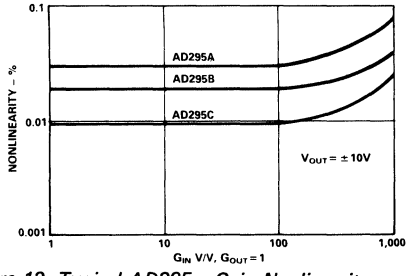


Figure 12. Typical AD295 – Gain Nonlinearity vs. Gain

Isolated Strain Gauge Using Front End of AD295

The AD295 can be used to condition and isolate differential signal sources like those present with strain gauge measurements. Figure 13 illustrates one possible configuration for conditioning a strain gauge. Amplifiers A1 and A2 are powered by the AD295's input isolated power supply. This eliminates the need for a separate dc/dc converter and provides a completely floated differential input. Input gain is selected via R_G and determined by the input gain formula.

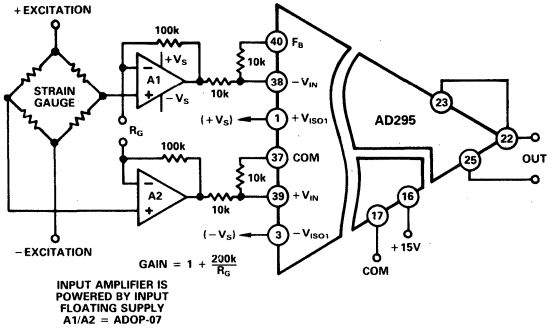


Figure 13. Isolated Strain Gage Using Front End of AD295

Isolated Temperature Measurement with Cold Junction Compensation

The AD295 can be used to condition, isolate and provide cold junction compensation of thermocouples in temperature measurement applications. With the circuit shown in Figure 14, the AD590 must be thermally connected to the cold junction terminal for an accurate temperature measurement of the terminals. Using this circuit, accurate temperature measurements using the industry's popular J type thermocouple can be made.

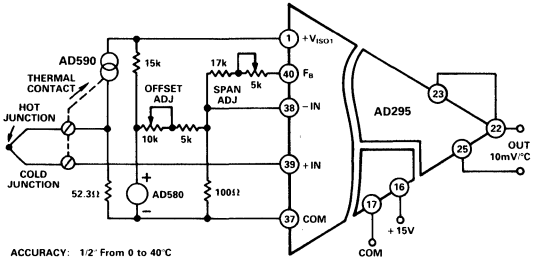


Figure 14. Isolated Temperature Measurement with Cold Junction Compensation

Isolated Voltage-to-Current Loop Converter

Illustrated in Figure 15, the AD295 is used to convert a 0 to +10V input signal to a standard 4-to-20mA current. Here high common-mode rejection and high common-mode voltage suppression are easily obtained with the AD295. The AD295 conditions the 0 to +10V input signal and provides a proportional voltage at the isolator's output. This output signal is converted to a 4-to-20mA current, which in turn is applied to the loop load R_{LOAD}.

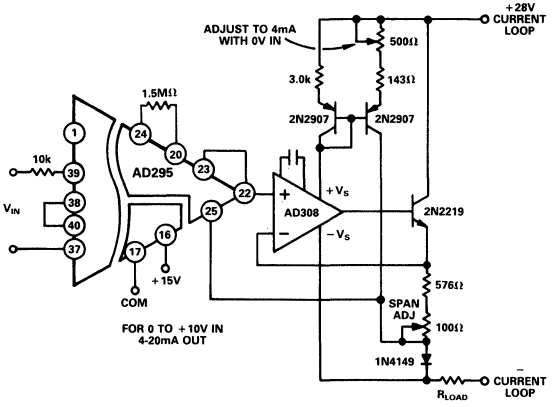


Figure 15. Isolated Voltage-to-Current Loop Converter

Noise Reduction in Data Acquisition Systems

In critical low noise applications like when an isolation amplifier precedes an analog to-digital converter, it may be desirable to add filtration, otherwise output ripple may cause inaccurate conversions. The 2-pole low-pass active filter shown in Figure 16 limits isolator bandwidth of the AD295. The filter will reduce output ripple and provide smoothing of discontinuous high frequency waveforms.

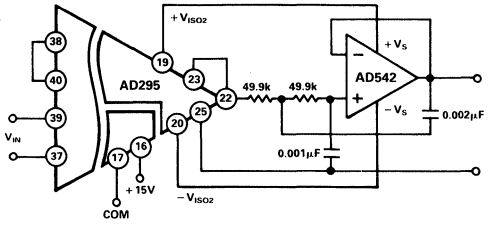


Figure 16. 2-Pole, 2kHz Active Filter

Economy, High Performance, Self-Contained Isolation Amplifier

284J

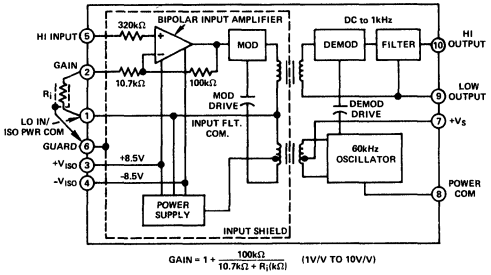
FEATURES

Low Cost: $62 (1–24); $43 (100's)
Low Nonlinearity: ±0.05% @ 10V pk-pk Output
High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
Isolated Power Supply: ±8.5V dc @ ±5mA
High CMR: 110dB min with 5kΩ Imbalance
High CMV: ±5000V_{pk}, 10ms Pulse; ±2500V dc continuous
Small Size: 1.5″ x 1.5″ x 0.6″
Adjustable Gain: 1 to 10V/V; Single Resistor Adjust
Meets IEEE Std 472: Transient Protection (SWC)
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz

APPLICATIONS

Biomedical and Patient Monitoring Instrumentation
Ground Loop Elimination in Industrial Control
Off-Ground Signal Measurements
4-20mA Isolated Current Loop Receiver

284J FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 284J is a low cost isolation amplifier featuring isolated power, ±8.5V dc @ ±5mA loads, ±2500V dc off-ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5″ x 1.5″ x 0.6″ epoxy encapsulated package. This improved design achieves low nonlinearity of ±0.05% @ 10V pk-pk output, gain stability of ±0.0075%/°C and input offset drift of ±30μV/°C at G = 10V/V. Using modulation techniques with reliable transformer isolation, model 284J will interrupt ground loops, leakage paths and high voltage transients to ±5kV_{pk} (10ms pulse) providing dc to 1kHz (-3dB) response over an adjustable gain range of 1V/V to 10V/V. Model 284J's fully floating guarded input stage and floating isolated power for external input circuitry, offers versatility for both medical and industrial OEM applications.

WHERE TO USE MODEL 284J

Medical Applications: In all biomedical and patient monitoring equipment such as multi-lead ECG recorders and portable diagnostic designs, model 284J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 284J's low input noise (8μV p-p) and high CMR (110dB, min).

Industrial Applications: In computer interface systems, process signal isolators and high CMV instrumentation, model 284J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface is afforded with model 284J's 10V pk-pk input signal capability at a gain of 1V/V operation. In portable field designs, model 284J's single supply, low power drain of 85mW @ +12V operation offers long battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±8.5V dc @ ±5mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Model 284J's adjustable gain combined with its 10V pk-pk output signal dynamic range offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 10V/V providing the flexibility of applying model 284J in both high level transducer interfacing as well as low level sensor measurements.

Floating, Guarded Front-End: The input stage of model 284J can directly accept floating differential signals, such as ECG biomedical signals, or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Model 284J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 284J has a calculated MTBF of over 400,000 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 284J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

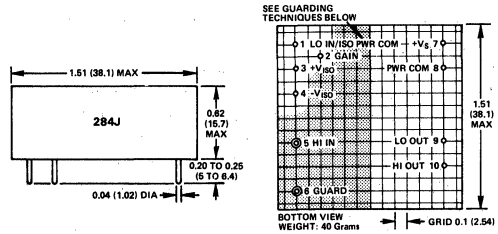
SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

MODEL	284J
GAIN (NON-INVERTING)	
Range (50kΩ Load)	1 to 10V/V
Formula	Gain = $[1 + \frac{100k\Omega}{10.7k\Omega + R_i(k\Omega)}]$
Deviation from Formula	±3%
vs. Time	±0.001%/1000 Hours
vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
Nonlinearity, G = 1V/V to 10V/V[2]	±0.05%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±5V min
Max Safe Differential Input	
Continuous	$240V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 6500V_{pk}$ max
Max CMV, Inputs to Outputs	
AC, 60Hz, 1 minute duration	$2500V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 2500V_{pk}$ max
With 510kΩ in series with Guard	$\pm 5000V_{pk}$ max
Continuous, ac or dc	$\pm 2500V_{pk}$ max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common @ 115V ac, 60Hz	2.0μA rms max
INPUT IMPEDANCE	
Differential	$10^8\,\Omega \| 70pF$
Overload	300kΩ
Common Mode	$5 \times 10^{10}\,\Omega \| 20pF$
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE	
Voltage, G = 10V/V	
0.05Hz to 100Hz	8μV p-p
10Hz to 1kHz	10μV rms
Current	
0.05Hz to 100Hz	5pA p-p
FREQUENCY RESPONSE	
Small Signal, -3dB, G = 1V/V to 10V/V	1kHz
Slew Rate	25mV/μs
Full Power, 10V p-p Output	
Gain = 1V/V	700Hz
Gain = 10V/V	200Hz
Recovery Time, to ±100μV after Application of $\pm 6500V_{pk}$ Differential Input Pulse	200ms
OFFSET VOLTAGE REFERRED TO INPUT	
Initial, @ +25°C, Adjustable to Zero	±(5 + 20/G)mV
vs. Temperature (0 to +70°C)	±(15 + 150/G)μV/°C
vs. Supply Voltage	±1mV/%
RATED OUTPUT	
Voltage, 50kΩ Load	±5V min
Output Impedance	1kΩ
Output Ripple, 1MHz Bandwidth	5mV pk-pk
ISOLATED POWER OUTPUTS	
Voltage, ±5mA Load	±8.5V dc
Accuracy	±5%
Current	±5mA min
Regulation, No Load to Full Load	+0, -15%
Ripple, 100kHz Bandwidth	100mV p-p
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage Operating	+(8 to 15.5)V dc
Current, Quiescent	+10mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

NOTES
[1]Gain temperature drift is specified as a percentage of output signal level.
[2]Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3]Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

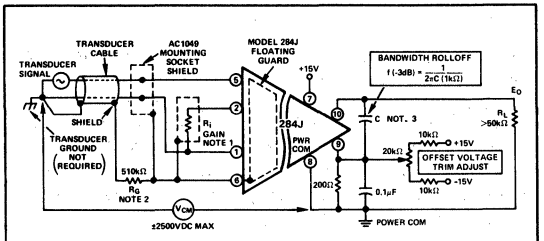


AC1049
SHIELDED MOUNTING SOCKET

INTERCONNECTION AND GUARDING TECHNIQUES

Model 284J can be applied directly to achieve rated performance as shown in Figure 1 below. To preserve the high CMR performance of model 284J, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 284J as illustrated in the outline drawing above (screened area). The GUARD (Pin 6) should be connected to this shield. This guard-shield is provided with the mounting socket, model AC1049. A recommended guarding technique using model AC1049 is illustrated in Figure 1. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low.

Offset Voltage Trim Adjust: The trim adjust circuit shown in Figure 1 can be used to zero the output offset voltage over the gain range from 1 to 10V/V. The output terminals, HI OUT and LO OUT, can be floated with respect to PWR COM up to $\pm 50V_{pk}$ max, offering three-port isolation. A 0.1μF capacitor is required from LO OUT to PWR COM whenever the output terminals are floated with respect to PWR COM. LO OUT can be connected directly to PWR COM when output offset trimming is not required.



NOTE 1. GAIN RESISTOR, R_i, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 10V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$\text{GAIN} = 1 + \frac{100k\Omega}{10.7k\Omega + R_i(k\Omega)}$$

NOTE 2. GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > $\pm 2500V_{PK}$ ($\pm 5kV_{PK}$ MAX).
R_G MAY BE MOUNTED ON AC1049 MOUNTING SOCKET USING STANDOFF PROVIDED.
(USE ¼ WATT, 5%, CARBON COMPOSITION TYPE; ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR, C, SELECT TO ROLLOFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C = 1.5μF FOR dc TO 100Hz BANDWIDTH).

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 284J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 284J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 35μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 10V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 284J at a gain of 10V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 20pF leakage capacitance between the floating guarded input section and the rest of the circuitry keeps the CMR from being infinite.

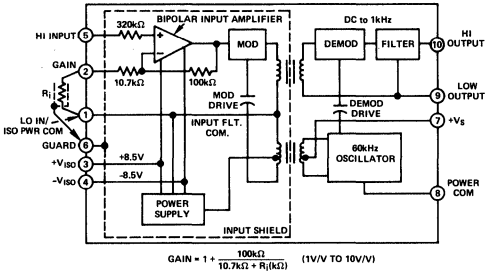


Figure 2. Block Diagram – Model 284J

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 3 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

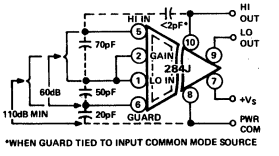


Figure 3. Model 284J Terminal Capacitance and CMR Ratings

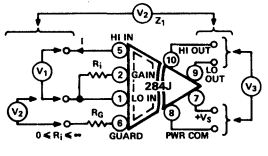


Figure 4. Model 284J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 and Table 1 illustrate model 284J's ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	$\pm 6500V_{PK}$ (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	$\pm 240V_{RMS}$	Withstand Voltage, Steady State
V2 (pulse)	$\pm 2500V_{PK}$ (10ms) $R_G = 0$	Transient
V2 (pulse)	$\pm 5000V_{PK}$ (10ms) $R_G = 510k\Omega$	Isolation, Defibrillator
V2 (cont.)	$\pm 2500V_{PK}$	Isolation, Steady State
V3 (cont.)	$\pm 50V_{PK}$	Isolation, dc
Z1	50kMΩ||20pF	Isolation Impedance
I	35μA rms	Input Fault Limit, DC to 60kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.0μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 5, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 60kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 284J.

For medical applications, model 284J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies. (e.g. model 284J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 284J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

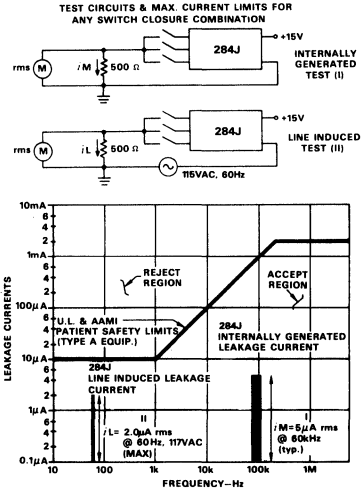


Figure 5. Model 284J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 10V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 146dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 10V/V.

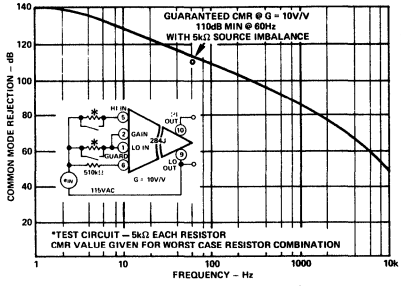


Figure 6. Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 10V/V. CMR is typically 120dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

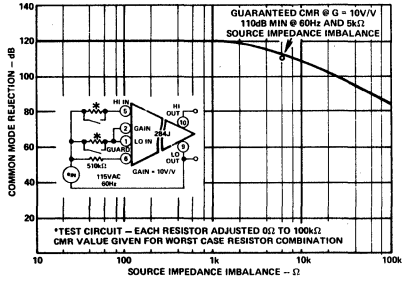


Figure 7. Common Mode Rejection vs. Source Impedance Imbalance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 10V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 8 (1.2μV rms) by 6.6.

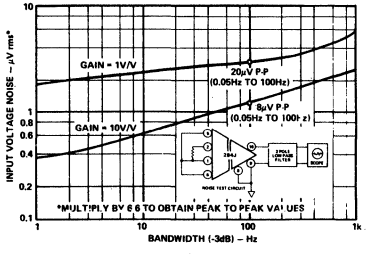


Figure 8. Input Voltage Noise vs. Bandwidth

For lowest noise performance, a low pass filter at the output should be used to selectively roll-off noise, output ripple and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1).

Input Offset Voltage Drift: Total input voltage drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 9 illustrates the total input voltage drift over the gain range of 1 to 10V/V.

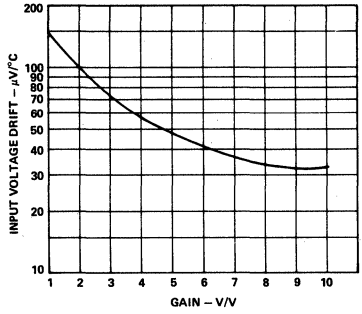
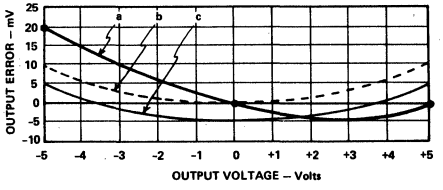


Figure 9. Input Offset Voltage Drift vs. Gain

Gain Nonlinearity: Linearity error is defined as the peak deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g. nonlinearity of model 284J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. In applying model 284J, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error over the operating output voltage span. A calibration technique illustrating how to minimize output error is shown below. In this example, model 284J is operating over an output span of +5V to -5V and a gain of 5V/V.



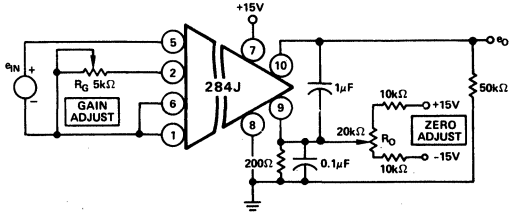


Figure 10. Gain and Offset Adjustment

GROUNDING PRACTICES

The more common sources of electrical noise arise from ground loops, electrostatic coupling and electromagnetic pickup. The guidelines listed below pertain to guarding low level, millivolt signals in hostile environments such as current shunt signals in "heavy industrial" plants.

Guidelines:

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 11 below. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 284J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- To avoid ground loops and excessive hum, signal low, B, or the transducer cable shield, S, should never be grounded at more than one point.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

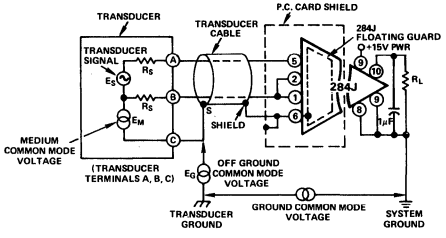


Figure 11. Transducer- Amplifier Interconnection

Isolated Power and Output Voltage Swing: Model 284J offers a floating power supply providing ±8.5V dc outputs with ±5mA output current rating. As shown in Figure 12, the minimum voltage output for $\pm V_{ISO}$, as well as the maximum load capability, is dependent on the input power supply, $+V_S$. Figure 12 also illustrates the typical output voltage range as both input supply, $+V_S$, and the isolated supply loads, $\pm I_L$, are varied. At ±5mA isolated load and V_S = +15V dc, model 284J can provide an output voltage swing of ±7.5V.

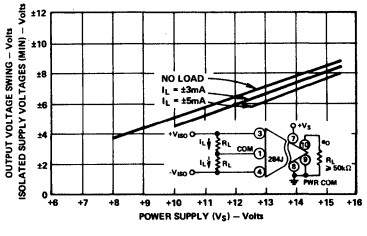


Figure 12. Isolated Power ($\pm V_{ISO}$) and Output Voltage Swing ($\pm E_O$) Versus Power Supply Input (V_S)

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 284J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems of on-line process measurement systems such as pollution monitoring, model 284J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 13 illustrates how model 284J can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD517K, to interface low level transducer signals. Model 284J's isolated ±8.5V dc power and front-end guard eliminate ground loops and preserve high CMR (114dB @ 60Hz).

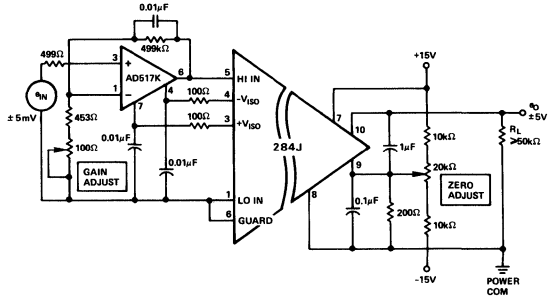


Figure 13. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Model 284J provides a floating guarded input stage capable of directly accepting isolated differential signals. The non-inverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, model 284J can be connected as shown in Figure 14. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/-IN and IN COM terminals as shown in Figure 14.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum e_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum e_O.
4) Repeat steps 2 and 3 for best CMR performance.

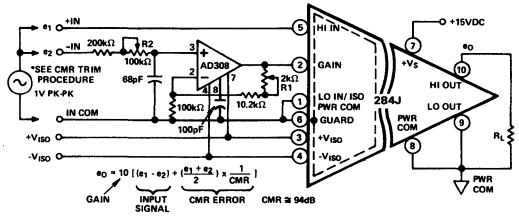


Figure 14. Application of 284J as Instrumentation Amplifier

APPLICATIONS IN BIOMEDICAL DESIGNS

Cardiac Monitoring: Heart signals can be masked by muscle noise, electrochemical noise, residual electrode voltages and 60Hz power line pickup. To achieve high performance in cardiac monitoring, model 284J's design provides high CMR in the dc to 100Hz bandwidth and substantial source impedance — to 5kΩ. An especially demanding ECG requirement is that of fetal heart monitoring as illustrated in Figure 15. The low input noise of model 284J and the dual CMR ratings are exploited in this application to extract the fetal ECG signals. The separation between the mother's and the fetal heartbeat is enhanced by the 78dB of CMR between the input electrodes and guard, while the 110dB of CMR from input to output ground screens out 60Hz pickup and other external interference.

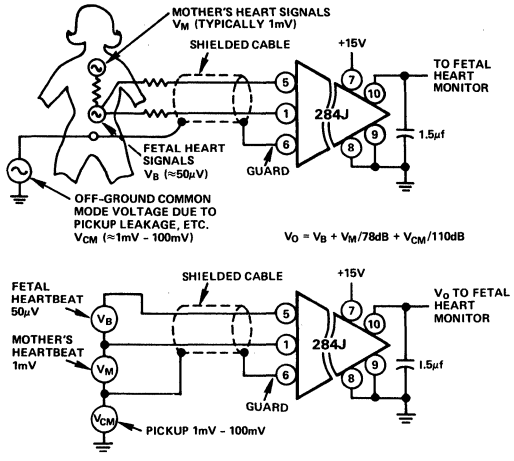


Figure 15. Fetal Heartbeat Monitoring

Single Lead ECG Recorder with Leads Off Indicator: In single lead applications model 284J offers simple two-wire hook-up to the ECG signal as illustrated in Figure 16. The floating signal can be connected directly to the HI IN and LO IN terminals using the GUARD tied to the patients' right leg for best CMR performance. Using the isolated power from model 284J an inexpensive calibration signal is easily provided. In ECG applications, model 284J provides a simple means to determine whenever a "Leads-Off" condition exists at the input. A "Leads-Off" condition ($R_S = \infty$) will cause the HI OUT terminal to be at a negative output saturation level; i.e. e_O = -8.5V to -9.5V @ V_S = +15V.

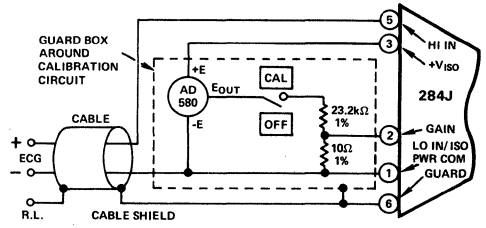


Figure 16. Single Lead ECG Recorder with 1mV Calibration Circuit and Leads Off Indicator

Multi-Lead ECG Recorder with Right Leg Drive: The small size, economy and isolated power makes model 284J an ideal isolation amplifier for application in clinical ECG recorders. Figure 17 illustrates how this new isolator can be applied in a high performance, portable multi-lead ECG recorder. In this application, model 284J's input is configured as an instrumentation amplifier with high CMR to the floating input common. The right leg drive offers improved CMR between input and isolated common by driving to zero any CMV existing between these points. The isolated power, $\pm V_{ISO}$, is used to drive the lead buffer amplifiers and the front-end, 1mV calibration signal.

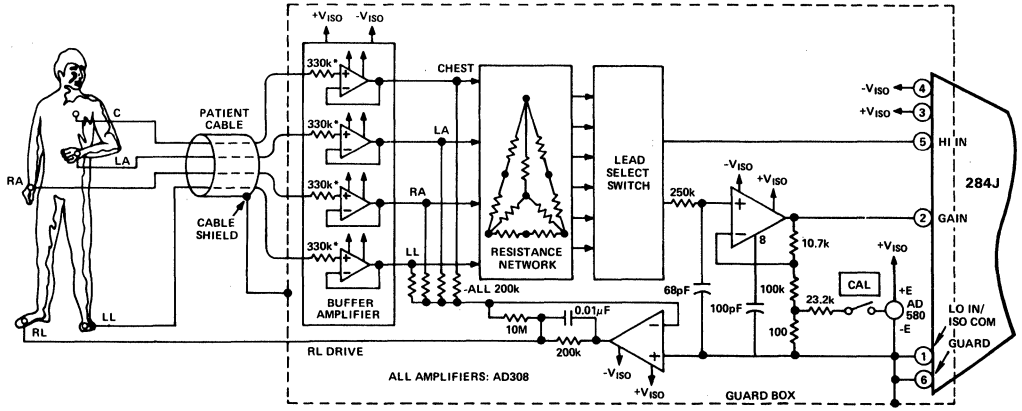


Figure 17. Multilead ECG Recorder Application Using 284J with Right Leg Drive Output

ANALOG DEVICES

High CMV, High Performance, Synchronized Isolation Amplifiers

286J/281

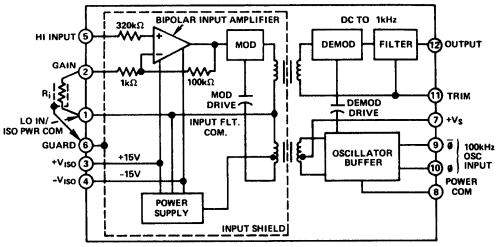
FEATURES

Low Cost
Single or Multi-Channel Capability Using External Oscillator
Isolated Power Supply: ±15V dc @ ±15mA
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.0075%/°C
Small Size: 1.5" x 1.5" x 0.62"
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 2500V dc Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

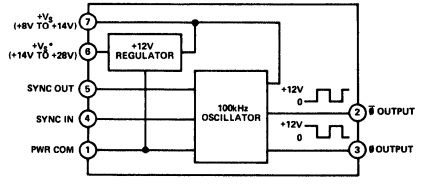
Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Biomedical and Patient Monitoring Instrumentation
Off-Ground Signal Measurements

286J FUNCTIONAL BLOCK DIAGRAM



$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_i\,(k\Omega)} \quad (1V/V \text{ TO } 100V/V)$$

281 FUNCTIONAL BLOCK DIAGRAM



*LEAVE TERMINAL 6 OPEN, WHEN POWER IS APPLIED TO TERMINAL 7.

GENERAL DESCRIPTION

Model 286J is a low cost, compact, isolation amplifier that is optimized for single or multi-channel use in data acquisition systems for industrial and medical applications. A single external synchronizing oscillator can drive from 1 to 16 model 286J's, or a virtually limitless number of model 286's can be configured using multiple ganged oscillators. The oscillator drive circuit can be supplied by the user of specified in a compact, low cost, epoxy encapsulated module, model 281, which also includes a voltage regulator for operation over a wide single voltage range of +8V to +28V.

In addition to providing multi-channel operation, this new design features adjustable gain, 1 to 100V/V, dual isolated power, ±15V dc @ ±15mA, ±2500V dc off ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5" x 1.5" x 0.6" epoxy encapsulated package. Model 286J achieves a low input noise of 8μV pk-pk (100Hz bandwidth, G = 100V/V), nonlinearity of ±0.05% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, model 286J will interrupt ground loops, leakage paths, and high voltage transients to ±5kV pk (10ms pulse), providing dc to 1kHz (-3dB) response.

WHERE TO USE MODEL 286J

Industrial Applications: In multi-channel data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, model 286J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with model 286J's 20V pk-pk input signal range at a gain of 1V/V operation. In portable multi-channel designs, model 286J's single supply, wide range operation (+8V to +16V) offers simple battery operation.

Medical Applications: In biomedical and patient monitoring equipment such as multi-channel VCG, ECG, and polygraph recorders, model 286J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 286J's low input noise (8μV pk-pk @ G = 100V/V) and high CMR (110dB, min @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 286J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 286J has a calculated MTBF of 392,125 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 286J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

Isolated Power Supply: Dual ±15V dc @ ±15mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers as well as remote transducers such as thermistors or bridges.

Adjustable Gain: A single external resistor enables gain adjustment from 1V/V to 100V/V providing the flexibility of applying model 286J in both high-level transducer interfacing as well as low-level sensor measurements.

5

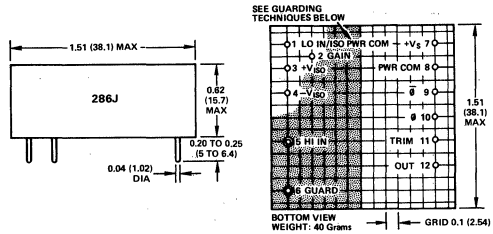
SPECIFICATIONS

MODEL	286J*
GAIN (NONINVERTING)	
Range (50kΩ Load)	1 to 100V/V
Formula	Gain = 1+ [100kΩ/(1kΩ+R_i(kΩ))]
Deviation from Formula	±4%
vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
vs. Time	±0.001%/1000 hours
Nonlinearity,[2] ±5V Output (G = 1 to 100V/V)	±0.05%
Nonlinearity,[2] ±10V Output (G = 1 to 100V/V)	±0.2%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±10V min
Max Safe Differntial Input	
Continuous	240V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±6500V pk max
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 Minute Duration	2500V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±2500V pk max
With 510kΩ in series with Guard	±5000V pk max
Continuous, ac or dc	±2500V pk max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common	
@ 115V ac 60Hz	2.5μA rms max
OFFSET VOLTAGE, REFERRED TO INPUT	
Initial, @ +25°C (Adjustable to zero)	±(5 + 45/G) mV
vs. Temperature (0 to +70°C)	
At Gain = 100V/V	±10μV/°C
At Other Gains (1 to 100V/V)	±(7 + 250/G)μV/°C
vs. Supply Voltage	±1mV/%
INPUT IMPEDANCE	
Differential	$10^8\Omega$‖150pF
Overload	300kΩ
Common Mode	$5 \times 10^{10}\Omega$‖20pF
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE (Gain = 100V/V)	
Voltage	
0.05Hz to 100Hz	8μV pk-pk
10Hz to 1kHz	3.0μV rms
Current	
0.05Hz to 100Hz	5pA pk-pk
FREQUENCY RESPONSE (Gain: 1V/V to 100V/V)	
Small Signal Bandwidth, -3dB	1.0kHz
Slew Rate	25mV/μs
Full Power, 10V pk-pk Output	900Hz
Full Power, 20V pk-pk Output	400Hz
Recovery Time, to ±100μV	200ms
RATED OUTPUT	
Voltage, 50kΩ Load	±10V min
Output Impedance	1kΩ
Output Ripple, 1mHz Bandwidth	20mV pk-pk
OSCILLATOR DRIVE INPUT*	
Input Voltage	(8 to 16)V pk-pk
Input Frequency	100kHz ±5%, max
ISOLATED POWER SUPPLY	
Voltage	±15V dc
Accuracy	0, -6%
Current	±15mA min
Regulation, No Load to Full Load	+0, -10%
Ripple, 100kHz Bandwidth	200mV pk-pk
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage, Operating	+(8V dc to 16V dc)
Current, Quiescent	+13mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

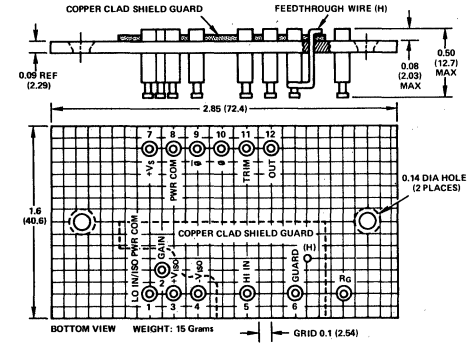
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of output signal span.
[3] Recommended power supply, ADI model 904, ±15V @ ±50mA output.
*Specifications are for model 286J when driven by ADI model 281 oscillator circuit (see Figure 12). Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



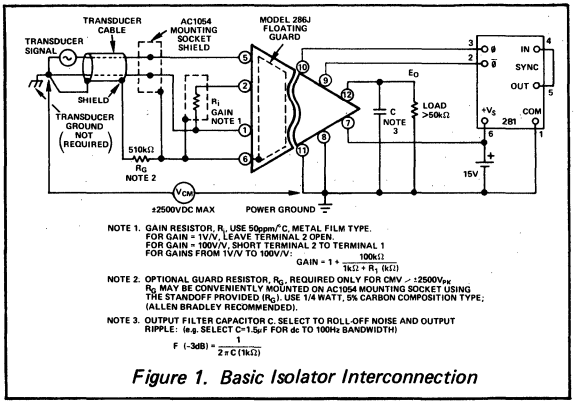
SHIELDED MOUNTING SOCKET AC1054



GUARDING TECHNIQUES

To preserve the high CMR performance of model 286, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 286 as illustrated in the outline drawing above (screened area). The GUARD (pin 6) must be connected to this shield. This shield is provided with the mounting socket, model AC1054 (solder feedthrough wire to the socket guard pin and copper foil surface.) A recommended guarding technique using model AC1054 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable to reduce inductive and capacitive pickup. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to signal low as shown in Figure 1.



NOTE 1. GAIN RESISTOR, R_I, USE 50ppm/°C, METAL FILM TYPE.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1
FOR GAINS FROM 1V/V TO 100V/V: $\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_I\,(k\Omega)}$

NOTE 2. OPTIONAL GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > ±2500V_{PK}. R_G MAY BE CONVENIENTLY MOUNTED ON AC1054 MOUNTING SOCKET USING THE STANDOFF PROVIDED (R_G). USE 1/4 WATT, 5% CARBON COMPOSITION TYPE; (ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR C: SELECT TO ROLL-OFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C=1.5μF FOR dc TO 100Hz BANDWIDTH)
$F\ (-3dB) = \frac{1}{2\pi C\,(1k\Omega)}$

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 286J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 286J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 50μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 286J at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry.

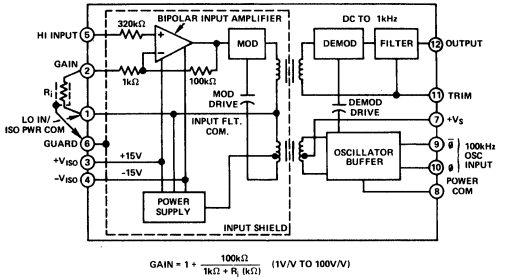


Figure 2. Block Diagram — Model 286J

OPTIONAL TRIM ADJUSTMENTS

Model 286J can be applied directly to achieve rated performance as shown in Figure 1, on previous page. Additional trim adjustment capability for bandwidth, output offset voltage and gain (for gains greater than 100V/V) is easily provided as shown in Figure 3 (below). The OUT and TRIM terminals can be floated with respect to PWR COM up to ±50V pk, max offering three-port isolation.

The TRIM terminal (pin 11) must be connected to the PWR COM terminal (pin 8) when not used to adjust the output offset voltage. A 0.1μF capacitor from pin 11 to PWR COM is recommended whenever the TRIM terminal is used.

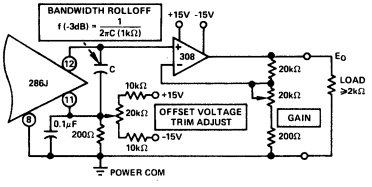


Figure 3. Optional Connections: Offset Voltage Trim Adjust, Bandwidth (-3dB) Rolloff and Gain Adjust (G>100V/V)

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 4 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

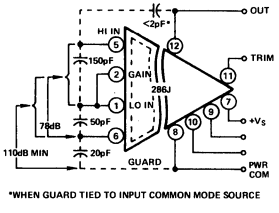


Figure 4. Model 286J Terminal Capacitance and CMR Ratings

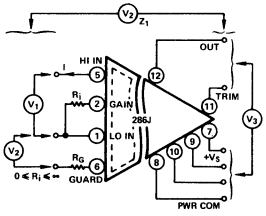


Figure 5. Model 286J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 5 and Table 1 illustrate model 286J ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V_{PK} (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	±240V_{RMS}	Withstand Voltage, Steady State
V2 (pulse)	±2500V_{PK} (10ms) R_G = 0	Transient
V2 (pulse)	±5000V_{PK} (10ms) R_G = 510kΩ	Isolation, Defibrillator
V2 (cont.)	±2500V_{PK}	Isolation, Steady State
V3 (cont.)	±50V_{PK}	Isolation, dc
Z1	50kMΩ‖20pF	Isolation Impedance
I	50μA rms	Input Fault Limit, dc to 200kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.5μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 6, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 100kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 286J.

For medical applications, model 286J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies (e.g., model 286J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment — reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 286J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

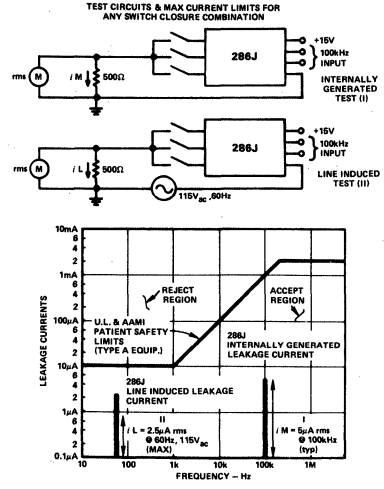


Figure 6. Model 286J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 100V/V. Figure 7 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V CMR is typically 6dB lower than at gain of 100V/V.

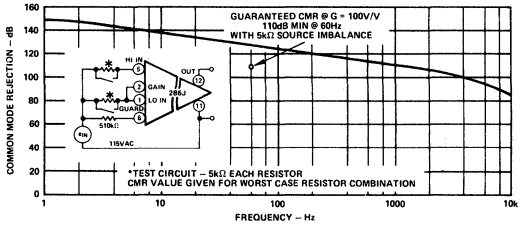


Figure 7. Common Mode Rejection vs. Frequency

Figure 8 illustrates the effect of source imbalance on CMR performance at 60Hz at gains of 1V/V, 10V/V, and 100V/V. CMR is typically 140dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

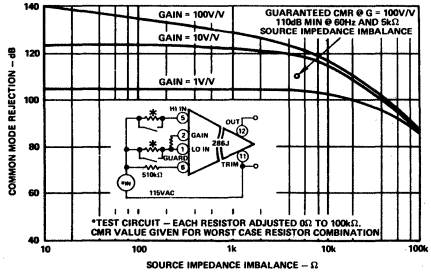


Figure 8. Common Mode Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of model 286J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

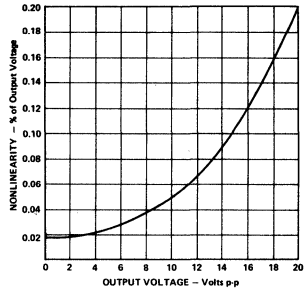


Figure 9. Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 10. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 10 (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1). Increasing gain will also reduce the input noise.

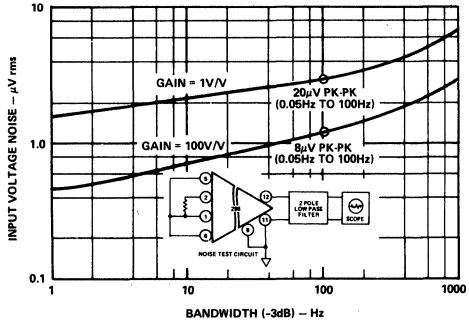


Figure 10. Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 11 illustrates total input drift over the gain range of 1 to 100V/V.

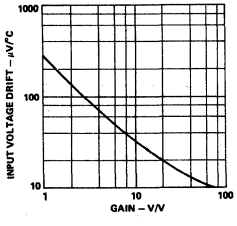


Figure 11. Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR

When applying model 286J, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 12, or purchasing a module from Analog Devices – model 281.

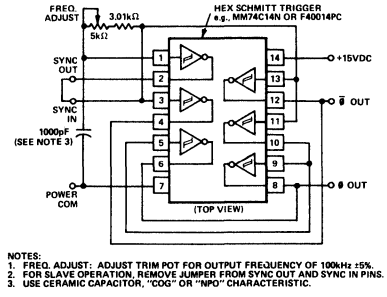


Figure 12. Model 281 100kHz Oscillator – Logic and Interconnection Diagram

The block diagram of model 281 is shown in Figure 13. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.

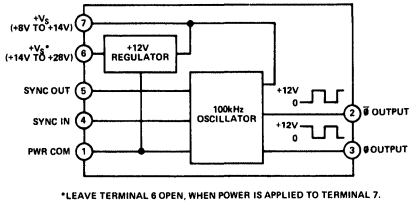


Figure 13. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 286J's as shown in Figure 14. An additional model 281 may be driven in a slave-mode, as shown in Figure 15, to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

EXTERNAL OSCILLATOR INTERCONNECTION

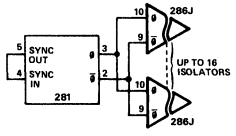


Figure 14. Model 281/286 Connection for Driving from 1 to 16 Isolators

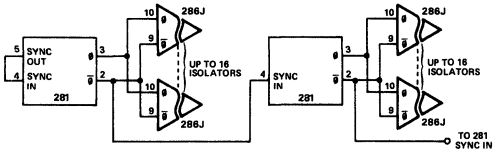


Figure 15. Model 281/286 Connection for Driving > 16 Isolators

SPECIFICATIONS

(typical @ +25° C and V_S = +15V dc unless otherwise noted)

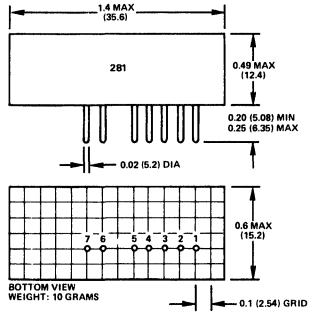
MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
MECHANICAL	
Case Size	1.4" x 0.6" x 0.49"
Weight	10 grams

[1] Model 286J oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 286J's, additional 281's may be used in a master/slave mode. Refer to Figure 15.
[3] Full load consists of 16 model 286J's and 281 oscillator slave.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

MODEL 281



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC OUTPUT
2	$\bar{\phi}$ OUTPUT	6	$+V_S$: HIGH RANGE +(14 to 28)V_{dc}
3	ϕ OUTPUT	7	$+V_S$: LOW RANGE +(8 to 14)V_{dc}
4	SYNC INPUT		

MATING SOCKET: CINCH #16 DIP OR EQUIVALENT

GUIDELINES ON EFFECTIVE SHIELDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 16. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 286J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

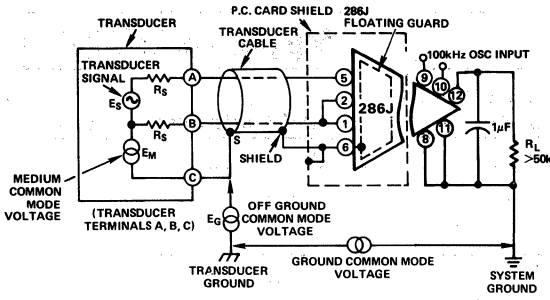
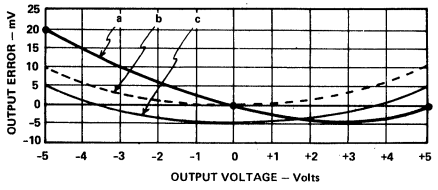


Figure 16. Transducer – Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/V is desired.

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +0.500V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = -0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).



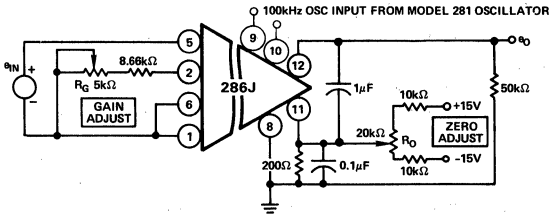


Figure 17. Gain and Offset Adjustment

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 286J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, model 286J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 18 illustrates how model 286J can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD510K, to interface low level transducer signals. Model 286J's isolated ±15V dc power and front-end guard eliminate ground loops and preserve high CMR (110dB min @ 60Hz).

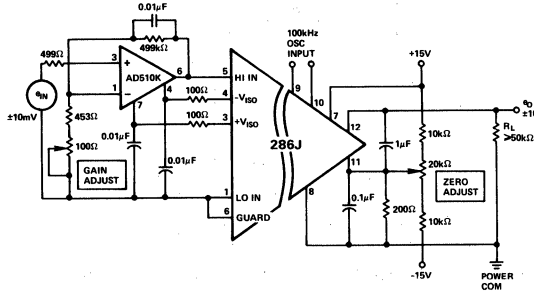


Figure 18. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Current Loop Receiver: Model 286J can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 19 shows an application of model 286J as a current loop receiver. A 25Ω resistor converts the 4–20mA current input from a remote loop to a 100–500mV differential voltage input, which the 286J amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the 286J in this kind of measurement are the high common-mode rejection (110dB minimum at 60Hz with 5kΩ source unbalance) and the high common-mode rating (±2500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

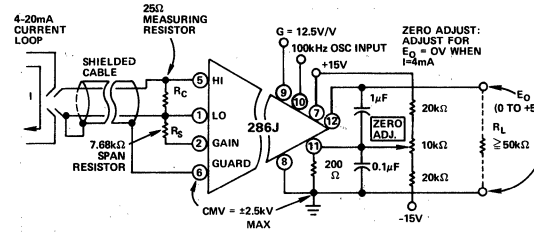


Figure 19. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±2500V of Isolation

ANALOG DEVICES

Precision, Wide Bandwidth, Synchronized Isolation Amplifier

289

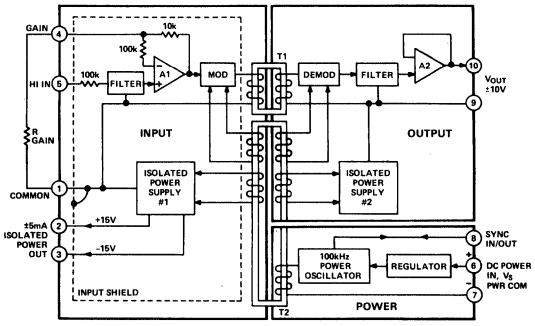
FEATURES

Low Nonlinearity: ±0.012% max (289L)
Frequency Response: (-3dB) dc to 20kHz
(Full Power) dc to 5kHz
Gain Adjustable 1 to 100V/V, Single Resistor
3-Port Isolation: ±2500V CMV Isolation Input/Output
Low Gain Drift: ±0.005%/°C max
Floating Power Output: ±15V @ ±5mA
120dB CMR at 60Hz: Fully Shielded Input Stage
Meets UL Std. 544 Leakage: 2μA rms max, @ 115V ac, 60Hz

APPLICATIONS

Multi-Channel Data Acquisition Systems
Current Shunt Measurements
Process Signal Isolator
High Voltage Instrumentation Amplifier
SCR Motor Control

289 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

Model 289 is a wideband, accurate, low cost isolation amplifier designed for instrumentation and industrial applications. Three accuracy selections are available offering guaranteed gain nonlinearity error at 10V p-p output: ±0.012% max (289L), ±0.025% max (289K), ±0.05% max (289J). All versions of the 289 provide a small signal frequency response from dc to 20kHz (-3dB) and a large signal response from dc to 5kHz (full power) at a gain of 1V/V. This new design offers true 3-port isolation, ±2500V dc between inputs and outputs (or power inputs), as well as 240V rms between power supply inputs and signal outputs. Using carrier modulation techniques with transformer isolation, model 289 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. It provides 120dB Common Mode Rejection between input and output common. The high CMV and CMR ratings of the model 289 facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays.

WHERE TO USE THE MODEL 289

The model 289 is designed to interface single and multichannel data acquisition systems with dc sensors such as thermocouples, strain gauges and other low level signals in harsh industrial environments. Providing high accuracy with complete galvanic isolation, and protection from line transients of fault voltages, model 289's performance is suitable for applications such as process controllers, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.

Use the model 289 when data must be acquired from floating transducers in computerized process control systems. The photograph above shows a typical multichannel application allowing potential differences or interrupting ground loops, among transducers, or between transducers and local ground.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: The floating power supply section provides isolated ±15V outputs @ ±5mA. Isolated power is regulated to within ±5%. This feature permits model 289 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers such as thermistors or bridges, eliminating the need for a separate isolated dc/dc converter.

Adjustable Gain: A single external resistor adjusts the model 289's gain from 1V/V to 100V/V for applications in high and low level transducer interfacing.

Synchronized: The model 289 provides a synchronization terminal for use in multichannel applications. Connecting the synchronization terminals of model 289s synchronizes their internal oscillators, thereby eliminating the problem of oscillator "beat frequency" interference that sometimes occurs when isolation amplifiers are closely mounted.

Internal Voltage Regulator: Improves power supply rejection and helps prevent carrier oscillator spikes from being broadcast via the isolator power terminal to the rest of the system.

Buffered Output: Prevents gain errors when an isolation amplifier is followed by a resistive load of low impedance. Model 289 can drive a 2kΩ load.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates need for power supply and output ports being returned through a common terminal.

Reliability: Model 289 is conservatively designed to be capable of reliable operation in harsh environments. Model 289 has a calculated MTBF of 271,835 hours. In addition, the model 289 meets UL Std. 544 leakage, 2μA rms @ 115V ac, 60Hz.

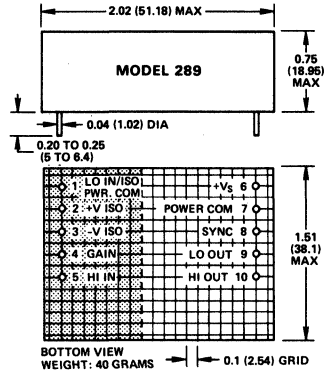
SPECIFICATIONS (typical @ +25°C and V_S = ±14.4V to +25V dc unless otherwise noted)

Model	289J	289K	289L
GAIN (NONINVERTING)			
Range		1 to 100V/V	
Formula		$G = 1 + \frac{10k\Omega}{R_G\,(k\Omega)}$	
Deviation from Formula		±1.5% max	
vs. Temperature (0 to +70°C)[1]		15ppm/°C typ (50ppm/°C max)	
Nonlinearity, (±5V Swing)[2,3]	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range (G = 1V/V)		±10V min	
Max Safe Differential Input			
Continuous		120V rms	
1 Minute		240V rms	
Max CMV (Inputs to Outputs)			
Continuous ac or dc		±2500V peak max	
ac, 60Hz, 1 Minute Duration		2500V rms	
CMR, Inputs to Outputs 60Hz			
$R_S \leq 1k\Omega$, Balanced Source Impedance		120dB	
$R_S \leq 1k\Omega$, HI IN Lead Only		104dB min	
Max Leakage Current, Input to Output @			
115V rms, 60Hz ac		2μA rms max	
INPUT IMPEDANCE			
Differential		$33pF \| 10^8\,\Omega$	
Overload		100kΩ	
Common Mode		$20pF \| 5 \times 10^{10}\,\Omega$	
INPUT DIFFERENCE CURRENT			
Initial @ +25°C		10nA (75nA max)	
vs. Temperature (0 to 70°C)		0.15nA/°C	
INPUT NOISE (GAIN = 100V/V)			
Voltage			
0.05Hz to 100Hz		8μV p-p	
10Hz to 1kHz		3μV rms	
Current			
0.05Hz to 100Hz		3pA rms	
FREQUENCY RESPONSE			
Small Signal -3dB			
G = 1V/V		20kHz	
G = 100V/V		5kHz	
Full Power, 10V p-p Output			
G = 1V/V		5kHz	
G = 100V/V		3.5kHz	
Full Power, 20V p-p Output			
G = 1V/V		2.3kHz	
G = 100V/V		2.3kHz	
Slew Rate		0.14V/μs	
Settling Time[4] ±0.05%, ±10V Step		400μs	
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial, @ +25°C		$\pm\left(5 + \frac{20}{G}\right)$ mV max	
vs. Temperature (0 to +70°C)	$\pm\left(20 + \frac{200}{G}\right)\mu V/°C$ max	$\pm\left(15 + \frac{100}{G}\right)\mu V/°C$ max	$\pm\left(10 + \frac{50}{G}\right)\mu V/°C$ max
vs. Supply Voltage (+15V to +20V change)		$\pm\left(2 + \frac{10}{G}\right)\mu V/V$	
RATED OUTPUT			
Voltage, 2kΩ Load		±10V min	
Output Impedance		<1Ω(dc to 100Hz)	
Output Ripple, 0.1MHz Bandwidth			
No Signal IN		5mV p-p	
$+10V_{IN}$		50mV p-p	
ISOLATED POWER SUPPLY			
Voltage		±15V dc	
Accuracy		±10%	
Current		±5mA, min	
Regulation No Load to Full Load		±5%	
Ripple, 0.1MHz Bandwidth, No Load		25mV p-p	
Full Load		75mV p-p	
POWER SUPPLY, SINGLE POLARITY[5]			
Voltage, Rated Performance		+14.4V to +25V	
Voltage, Operating		+8.5V to +25V	
Current, Quiescent (@ V_S = +15V)		+25mA	
TEMPERATURE RANGE			
Rated Performance		0 to +70°C	
Operating		-15°C to +75°C	
Storage		-55°C to +85°C	
CASE DIMENSIONS		1.5" X 2.0" X 0.75"	

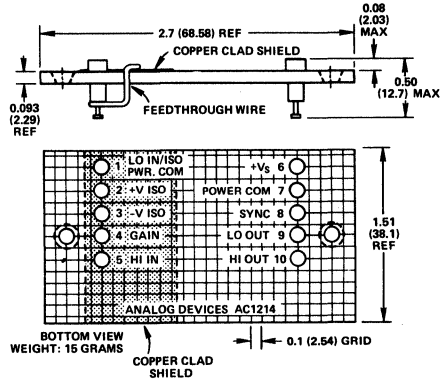
NOTES
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] When isolated power output is used, nonlinearity increases by ±0.002%/mA of current drawn.
[4] G = 1V/V; with 2-pole, 5kHz output filter (see Figure 13).
[5] Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MATING SOCKET AC1214



INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of model 289, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 289 as illustrated in the outline drawing above (screened area). The LO IN/ISO PWR COM (pin 1) must be connected to this shield. This shield is provided with the mounting socket, model AC1214 (solder feedthrough wire to the socket pin 1 and copper foil surface). A recommended shielding technique using model AC1214 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable for the input signal to reduce inductive and capacitive pickup. To further reduce effective cable capacitance, the cable shield should be connected to the common mode signal source as close to signal low as possible (see Figure 1).

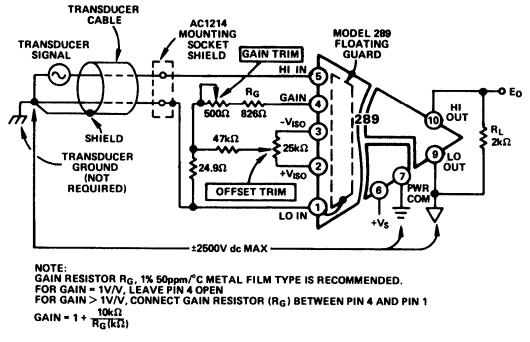


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of the model 289 is derived from the carrier isolation technique used to transfer both signal and power between the amplifier's input stage and the rest of the circuitry. A block diagram is shown in Figure 2.

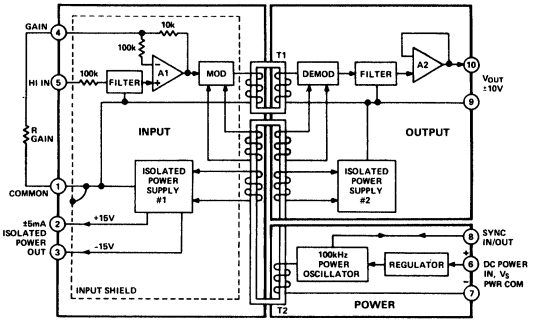


Figure 2. Model 289 Block Diagram

The input signal is filtered and appears at the input of the non-inverting amplifier, A1. This signal is amplified by A1, with its gain determined by the value of resistance connected externally between the gain terminal and the input common terminal. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulated voltage is filtered, amplified and buffered by amplifier A2, and applied to the output terminal. The voltage applied to the V_S terminal is set by the regulator to +12V which powers the 100kHz symmetrical square wave power oscillator. The oscillator drives the primary winding of transformer T2. The secondary windings of T2 energize both input and output power supplies, and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance, arising from stray coupling capacitance effects between the input terminals and the signal output terminals, are each shunted by leakage resistance values exceeding 50GΩ. Figure 3 illustrates model 289's capacitance, between terminals.

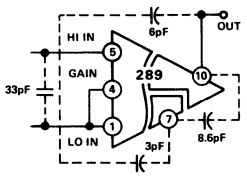


Figure 3. Model 289 Terminal Capacitance

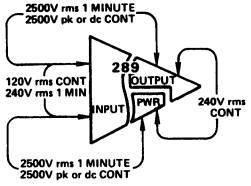


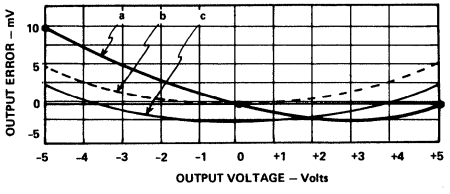
Figure 4. Model 289 Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 illustrates model 289 ratings between terminals.

GAIN AND OFFSET TRIM PROCEDURE

The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and Gain = 10V/V.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.500V dc and adjust R_G for E_O = +5.000V dc.
3. Apply E_{IN} = -0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one-half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one-half that measured in step 4 (see curve c).



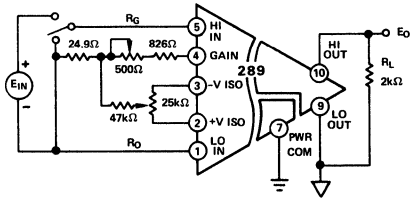


Figure 5a. Recommended Offset and Gain Adjustment for Gains > 1

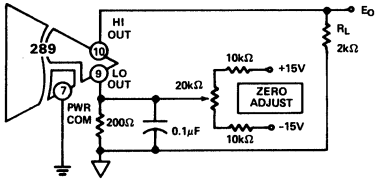


Figure 5b. Recommended Offset Adjustment for G = 1V/V

PERFORMANCE CHARACTERISTICS

Figure 6 shows the phase shift vs. frequency. The low phase shift and wide bandwidth of the model 289 make it suitable for use in SCR Motor Controller and other high frequency applications.

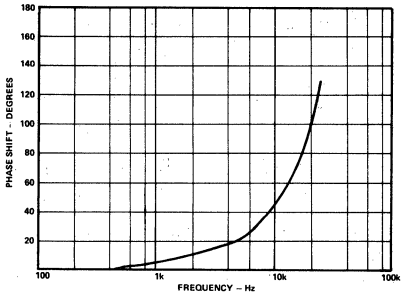


Figure 6. Typical 289 Phase vs. Frequency

Figure 7 illustrates the effect of source impedance imbalance on CMR performance at 60Hz for gains of 1V/V, 10V/V, and 100V/V. CMR is typically 120dB at 60Hz and a balanced source impedance. CMR is >60dB for source impedance imbalances up to 100kΩ.

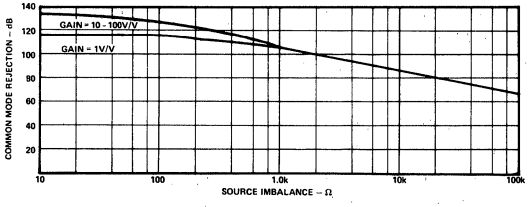


Figure 7. Typical 289 Common Mode Rejection vs. Source Impedance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth. Figure 8 shows rms voltage noise in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. The peak-to-peak value is derived by multiplying the rms value at F = 100Hz (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest. Increasing gain will also reduce the noise, referred to input.

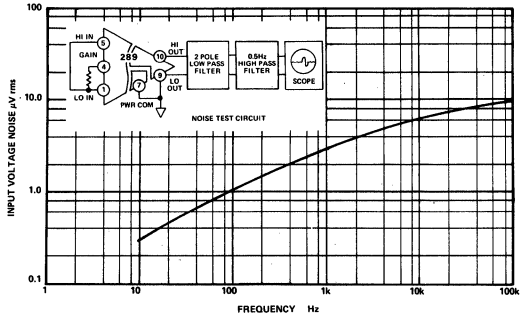


Figure 8. Typical Input Voltage Noise vs. Bandwidth

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % peak-to-peak output voltage span; e.g., nonlinearity of model 289J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V). Figure 10 shows the effect of gain vs. gain nonlinearity.

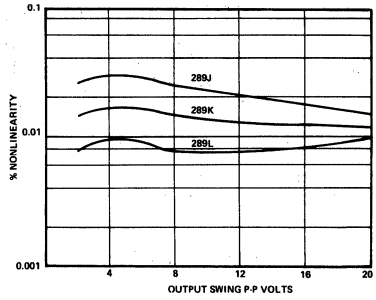


Figure 9. Typical Gain Nonlinearity vs. Output Swing

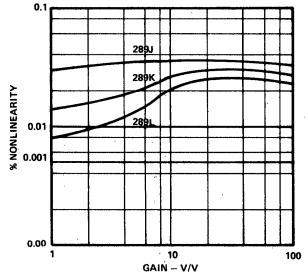


Figure 10. Typical Gain Nonlinearity vs. Gain

Common Mode Rejection: Input-to-output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ balanced source at a gain of 100V/V. Figure 11 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalance as high as 1kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 100V/V.

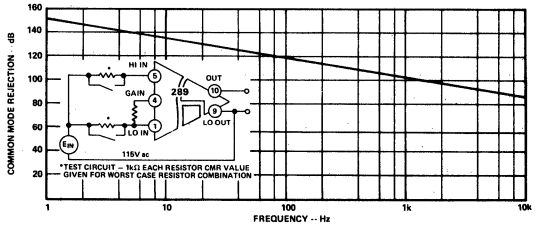


Figure 11. Typical Common Mode Rejection vs. Frequency at a Gain of 1V/V, CMR is typically 6dB Lower than at a Gain of 100V/V

MULTICHANNEL APPLICATIONS

Isolation amplifiers containing internal oscillators may exhibit a slowly varying offset voltage at the output when used in multichannel applications. This offset voltage is the result of adjacent internal oscillators beating together. For example, if two adjacent isolation amplifiers have oscillator frequencies of 100.0kHz and 100.1kHz respectively, a portion of the difference frequency may appear as a slowly varying output offset voltage error. Model 289 eliminates this problem by offering a synchronization terminal (pin 8). When this terminal is interconnected with other model 289 synchronization terminals, the units are synchronized. Alternately, one or more units may be synchronized to an external 100kHz ±2% square-wave generator by the connection of synchronization termial(s) to that generator. The generator output should be 2.5V–5.0V p-p with 1kΩ source impedance to each unit. Use an external oscillator when you need to sync to an external 100kHz source, such as a sub-multiple of a microprocessor clock. A differential line driver, such as SN75158, can be used to drive large clusters of model 289. When using the synchronization pin, keep leads as short as possible and do not use shielded wire. These precautions are necessary to avoid capacitance from the synchronization terminal to other points. It should be noted that units synchronized must share the same power common to ensure a return path.

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Isolated DAS: In data acquisition systems where multiple transducers are powered by a single supply and the magnitude of that supply is low enough for a multiplexer to handle the voltages on all the transducers, it is economical to multiplex ahead of an isolator. The fast settling time of the model 289 makes this configuration practical where slower isolators would not be usable.

Figure 12 shows an application where the difference in voltage between any two terminals of any of the transducers does not exceed 30 volts. Though the input of the model 289 is protected against line voltage, its power terminals are not; neither is the multiplexer so protected. This circuit will not, therefore, withstand the differential application of line voltage.

Multiplexer addressing is binary, an enable providing selection of the circuit shown as a signal source. Optical isolation is provided for digital signals. When several of these circuits are used for several groups of transducers, the model 289's should be synchronized.

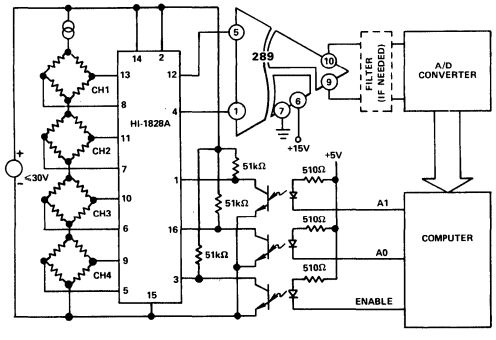


Figure 12. DAS with MUX Ahead of Isolator

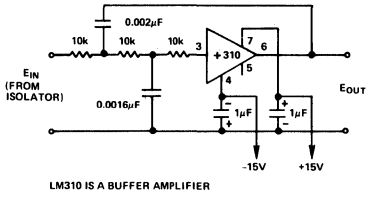


Figure 13. 2-Pole, 5kHz Active Filter

Noise Reduction in Data Acquisition Systems: Transformer coupled isolators must have a carrier to pass dc signals through their signal transformers. Inevitably some carrier frequency ripple passes through to the isolator output. As the bandwidth of an isolator becomes a larger fraction of its carrier frequency, this ripple becomes more difficult to control. Despite this difficulty, the model 289 produces very low ripple; therefore, additional filtration will usually be unnecessary. However, in some applications, particularly where a fast analog-to-digital converter is used following the isolator, it may be desirable to add filtration; otherwise, ripple may cause inaccurate conversions. The 2-pole low-pass shown in Figure 13 limits isolator bandwidth to 5kHz, which is the full power bandwidth of the model 289. Carrier ripple is much reduced. Another beneficial effect of an output filter is smoothing of discontinuous high frequency waveforms.

Motor Control and AC Load Control: Phase shift and bandwidth are important considerations for motor control and ac load control applications. The model 289 possesses sufficient bandwidth and acceptable phase shift for such tasks.

Figure 14 shows two model 289's sensing the armature voltage and current of a motor. Faithful replicas of the waveforms of these variables are applied to the motor control. A1 operates at unity gain from divided R1–R3 to deliver an output that is 1/100 of the armature voltage of the motor. A2 operates at a gain of 100V/V to deliver a voltage 100 times that developed across the current sensing shunt.

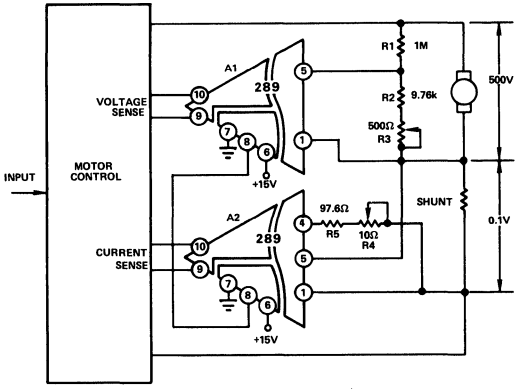


Figure 14. Isolating a Motor Controller

Figure 15 shows three model 289's sensing the voltages on the three phases of an ac load. The Y network shown divides the voltages of the three phases and creates a neutral for the input commons of the isolators. The output of each isolator is a faithful replica of the phase of the waveform it senses. The isolator outputs provide the feedback necessary for the trigger control to correctly fire the triacs. In other applications, the outputs of the isolators might have been fed to rms-to-dc converters.

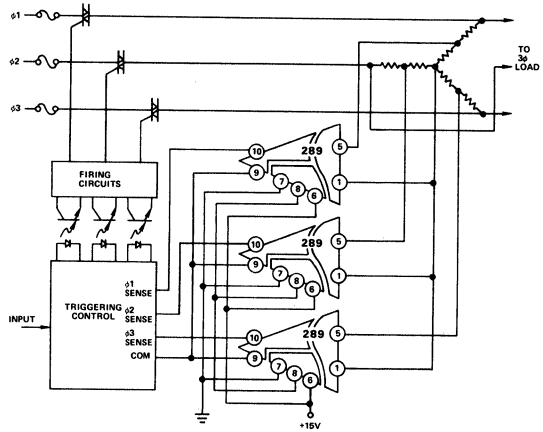


Figure 15. Isolating a 3 Phase Load Controller

Isolated DACs: Figure 16 shows a 12-bit DAC with ±5V isolated output. A buffered -5V reference voltage is provided to the DAC by A1a, A1b and associated circuitry. The digital input causes a proportion of DAC current to flow into OUT1 of the DAC. The remaining DAC current flows into OUT2. Current flowing into OUT1 causes positive voltage at the output of A1c. Current flowing into OUT2 causes a positive voltage at the output of A1d, which in turn causes a negative voltage at the output of A1c. Voltage appearing at the output of A1c is reproduced at the output of the model 289. R5 and R8 must be adjusted to produce less than 0.5mV at OUT1 and OUT2 of the DAC respectively. R15 may be used to adjust gain and R11 to adjust offset with the binary code 1000 0000 0000 to zero.

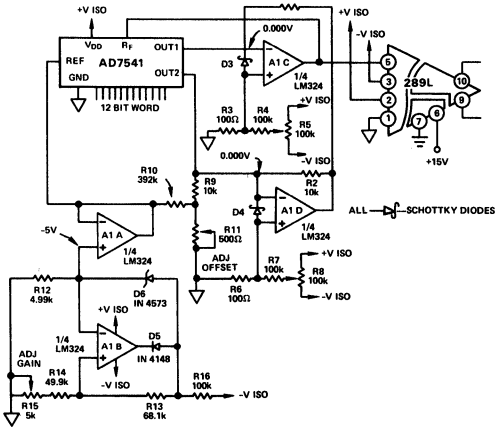


Figure 16. 12-Bit Isolated Voltage DAC

Figure 17 shows the model 289 providing an isolated 4-to-20mA output from a 12-bit DAC. A1a provides a -4V reference to the DAC. The digital input causes a portion of DAC current to flow into OUT1, causing a positive voltage at the output of A1d. A1b produces a voltage across R4 proportional to DAC current. A1c and associated circuitry sink a current which is one-fourth of the full scale current of the DAC, causing a positive voltage of 1 volt at the output of A1d. With the code 1111 1111 1111, +5 volts appears at the output of A1d. Operation is unipolar with a positive offset. The output voltage of A1d is reproduced at the output of the isolator, where the circuitry shown converts it into a 4-to-20mA current which may be applied to the load R_L.

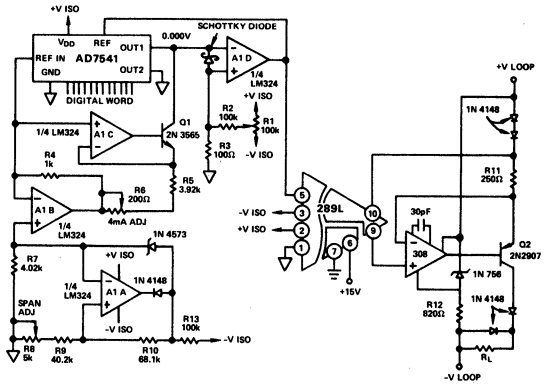


Figure 17. 12-Bit Isolated Process Current DAC

Temperature Measurement: Figure 18 shows the model 289 providing a ground-referred output in an application measuring the temperature of an object floating at a high common mode voltage. The AD590 temperature sensor sinks a current of -1μA/K. This current flows into the gain terminal of the model 289, developing +10mV/K across the internal feedback resistor. This voltage also appears at the output of the model 289.

The circuitry shown connected by a dotted line may be useful if an output of 10mV/°C is desired. A current of +273μA is sourced through the 8.66k resistor and the potentiometer cancelling the AD590 current at 0°C (273K), resulting in 0mV at the output at 0°C.

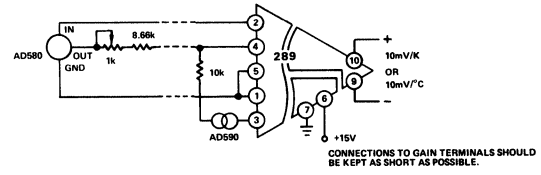


Figure 18. Isolated Temperature Measurement

ANALOG DEVICES

Low Cost, Single and Multichannel Isolation Amplifiers

290A/292A

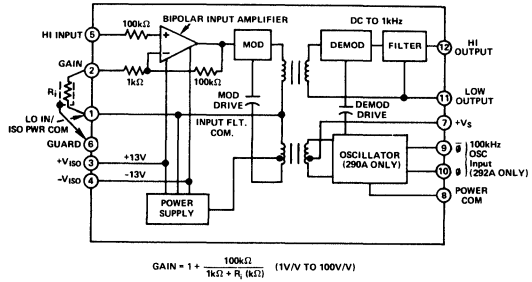
FEATURES

Low Cost
Multichannel Capability Using External Oscillator (292A)
Isolated Power Supply: ±13V dc @ ±5mA (290A) or ±15mA (292A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5" X 1.5" X 0.62"
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Fetal Heart Biomedical and Monitoring Instrumentation
Off-Ground Signal Measurements

290A/292A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Models 290A and 292A are low cost, compact, isolation amplifiers that are optimized for single and multichannel industrial applications, respectively. The model 290A has a self-contained oscillator and is intended for single channel applications. A single external synchronizing oscillator can drive up to 16 model 292As or, a virtually limitless number of model 292As can be configured using multiple oscillators. The user can supply the external oscillator circuit or specify model 281 oscillator module, which includes a voltage regulator for operation over a wide single supply voltage range of +8V to +28V.

Models 290A and 292A design features include: adjustable gain, from 1 to 100V/V, dual isolated power, ±13V dc, ±1500V dc off ground isolation, 100dB minimum CMR at 60Hz, 1kΩ source imbalance, in a compact 1.5" X 1.5" X 0.6" module. Models 290A and 292A achieve low input noise of 1μV pk-pk (10Hz bandwidth, G = 100V/V), nonlinearity of ±0.1% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, models 290A and 292A will interrupt ground loops, leakage paths, and voltage transients, while providing dc to 2kHz (-3dB) response.

WHERE TO USE MODELS 290A AND 292A

Industrial Applications: In data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, models 290A and 292A offer complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with 20V pk-pk input signal range at a gain of 1V/V operation. In portable single or multichannel designs, single power supply operation (+8V to +16V) enables battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±13V dc output, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Models 290A and 292A adjustable gain offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 100V/V providing flexibility in both high level transducer interfacing as well as low level sensor measurement applications.

Floating, Guarded Front-End: The input stage of models 290A and 292A can directly accept floating differential signals or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Models 290A and 292A are conservatively designed, compact modules, capable of reliable operation in harsh environments. They have a calculated MTBF of over 400,000 hours and are designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

SPECIFICATIONS (typical @ +25°C; G = 100V/V and V_S = +15V dc, unless otherwise noted)

MODEL	290A	292A
GAIN (NONINVERTING)		
Range (50kΩ Load)		1 to 100V/V
Formula		$\text{Gain} = \left[1 + \frac{100k\Omega}{1k\Omega + R_i(k\Omega)}\right]$
Deviation from Formula		±3%
vs. Time		±0.001%/1000 Hours
vs. Temperature (-25°C to +85°C)[1]		±0.0075%/°C
Nonlinearity, G = 1V/V to 100V/V[2]		±0.1% (±0.25%)[3]
INPUT VOLTAGE RATINGS		
Linear Differential Range, G = 1V/V		±5V min (±10V min)[3]
Max Safe Differential Input		
Continuous, 1 min		110V rms
Max CMV, Inputs to Outputs		
ac, 60Hz, 1 Minute Duration		1500V rms max
Continuous, ac		±1000V pk max
Continuous, dc		±1500V pk max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 1k\Omega$		
Balanced Source Impedance		106dB
1kΩ Hi In Lead Only		100dB min
Max Leakage Current, Inputs to Power Common		
@ 115V ac, 60Hz		10μA rms max
INPUT IMPEDANCE		
Differential		$10^8\ \Omega \| 70pF$
Overload		100kΩ
Common Mode		$5 \times 10^{10}\ \Omega \| 100pF$
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C		+3nA
vs. Temperature (-25°C to +85°C)		±0.1nA/°C
INPUT NOISE		
Voltage, G = 100V/V		
0.01Hz to 10Hz		1μV p-p
10Hz to 1kHz		1.5μV rms
Current		
0.05Hz to 100Hz		5pA p-p
FREQUENCY RESPONSE		
Small Signal, -3dB, G = 1V/V		2.5kHz
Slew Rate		50mV/μs
Full Power, 10V p-p Output		
Gain - 1V/V thru 100V/V	2.0kHz(1.0kHz)[3]	3.0kHz(1.0kHz)[3]
OFFSET VOLTAGE REFERRED TO INPUT		
Initial, @ +25°C, Adjustable to Zero		±(5 + 50/G)mV
vs. Temperature (-25°C to +85°C)	±(10 + 150/G)μV/°C	±(8 + 250/G)μV/°C
vs. Supply Voltage		±1mV/%
RATED OUTPUT		
Voltage, 50k Load		±5V min (±10V min)[3]
Output Impedance		1kΩ
Output Ripple, 1MHz Bandwidth		10mV pk-pk
OSCILLATOR DRIVE INPUT		
Input Voltage	N/A	8 to 16V pk-pk
Input Frequency	N/A	100kHz ±5%, max
ISOLATED POWER OUTPUTS		
Voltage Full Load		±13V dc
Accuracy		±5%
Current[4]	±5mA min	±15mA min
Regulation, No Load to Full Load		+0, -15%
Ripple, 100kHz Bandwidth	200mV p-p	250mV p-p
POWER SUPPLY, SINGLE POLARITY		
Voltage, Rated Performance		+15V dc
Voltage, Operating		+8V dc to +15.5V dc
Current, Quiescent		+20mA
TEMPERATURE RANGE		
Rated Performance		-25°C to +85°C
Storage		-55°C to +85°C
CASE DIMENSIONS		1.5" X 1.5" X 0.62"

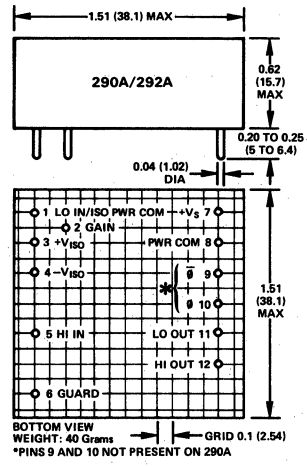
NOTES

[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] These specs apply for a 20V pk-pk output span.
[4] Do not load V_{ISO} when operating at output spans greater than 10V pk-pk.

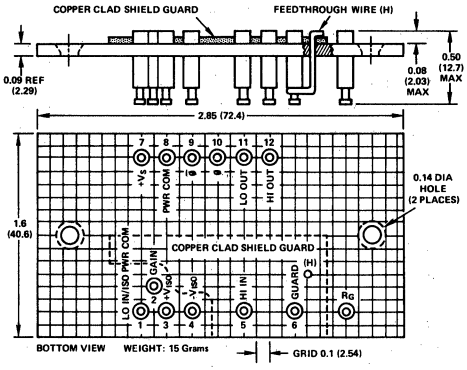
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MOUNTING SOCKET AC1054



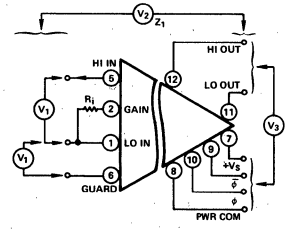


Figure 1. Model 290A and 292A Terminal Ratings

Symbol	Rating	Remarks
V_1	±110V rms (cont.)	Withstand Voltage, Steady State
V_2	±1000V pk (cont.)	Isolation, Steady State, ac
V_2	±1500V pk (cont.)	Isolation, Steady State, dc
V_2	±1500V rms (1 min)	Isolation, ac, 60Hz
V_3	±50V pk (cont.)	Isolation, dc
Z_1	$50G\Omega \| 20pF$	Isolation Impedance

Table I. Isolation Ratings Between Terminals

THEORY OF OPERATION

The remarkable performance of models 290A and 292A are derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for both models is shown in Figure 2 below.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating the isolator at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 10pF leakage capacitance between the floating input section and the rest of the circuitry keeps the CMR from being infinite.

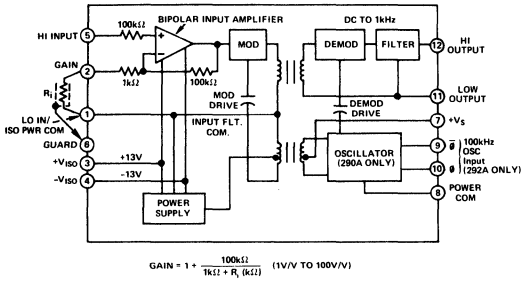


Figure 2. Block Diagram — Models 290A and 292A

GUIDELINES ON EFFECTIVE SHEILDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 3. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 86dB CMR capability of both models between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

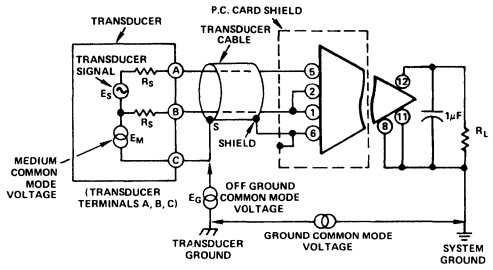
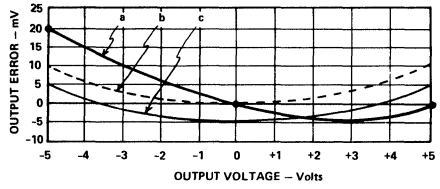


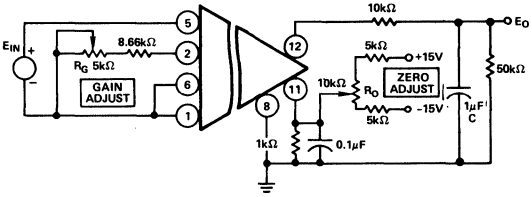
Figure 3. Transducer — Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/V is desired.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.5V dc and adjust R_G for E_O = +5.0V dc.
3. Apply E_{IN} = -0.5V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.5V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).





GAIN RESISTOR, R_i, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_i(k\Omega)}$$

OUTPUT FILTER, 10kΩ RESISTOR AND CAPACITOR, C.
SELECT C TO ROLL-OFF NOISE AND OUTPUT RIPPLE:

$$f = (-3dB) = \frac{1}{2\pi C\,(11k\Omega)}$$

Figure 4. Gain and Offset Adjustment

SELECTING BANDWIDTH

In low frequency signal measurements, such as thermocouple temperature measurements, strain gage measurements and geophysical instrumentation, an external filter is used to select bandwidth and minimize output noise.

When used with a buffer amplifier as shown in Figure 5a below, a series resistor (R_S) is used to lower the effective value of the filter capacitor required to achieve very low frequency (under 200Hz) noise filtering.

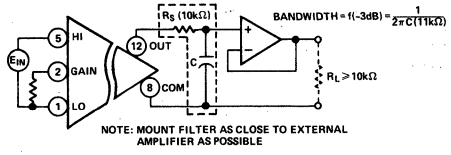


Figure 5a. Selecting Bandwidth with External Capacitor and Buffer

An active filter, as illustrated in Figure 5b will significantly improve 60Hz noise reduction at the output by providing a sharp roll-off characteristic. The 5Hz 3-pole active filter design illustrated in Figure 5b, will increase the 60Hz noise reduction by 50dB. Overall CMR performance of models 290 and 292 and the 5Hz active filter approaches 150dB @ 60Hz and 1kΩ imbalance.

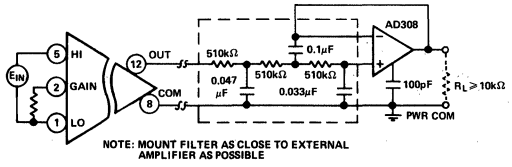


Figure 5b. Selecting Bandwidth with a 3-Pole 5Hz Active Filter

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ imbalance at a gain of 100V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 130dB at dc with source imbalances as high as 1kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 12dB lower than at a gain of 100V/V.

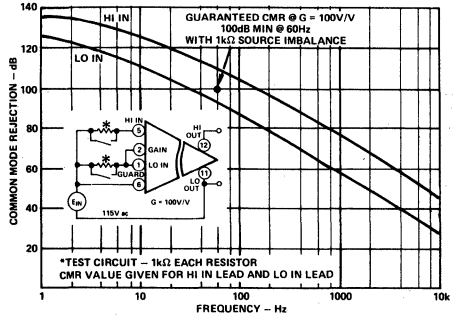


Figure 6. Typical Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 100V/V. CMR is typically 110dB at 60Hz and a balanced source. CMR is maintained greater than 70dB for source imbalances up to 100kΩ.

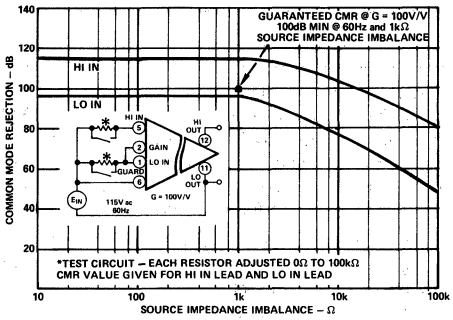


Figure 7. Typical Common Mode Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of models 290A and 292A operating at an output span of 10V pk-pk (±5V) is ±0.1% or ±10mV. Figure 8 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

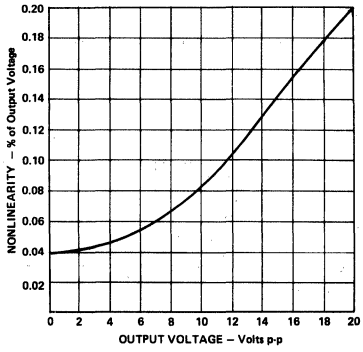


Figure 8. Typical Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 9. RMS voltage noise is shown in a bandwidth from 0.01Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.01Hz to 10Hz is 1μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 10Hz shown in Figure 9 by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest. Increasing gain will also reduce the input noise.

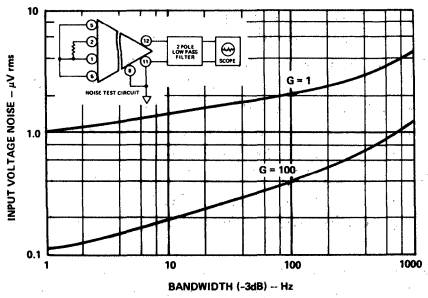


Figure 9. Typical Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 10 illustrates total input drift over the gain range of 1 to 100V/V.

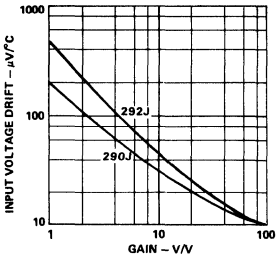
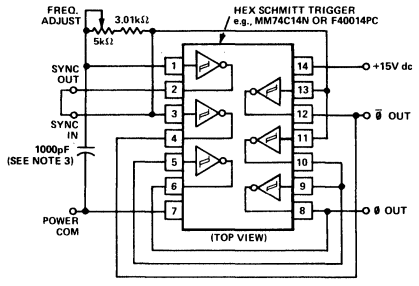


Figure 10. Typical Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR, MODEL 281

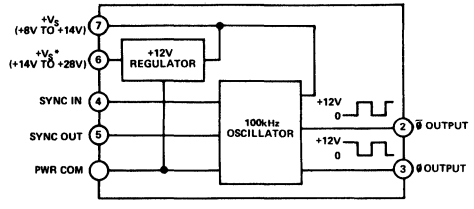
When applying model 292A, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 11, or purchasing a module from Analog Devices—model 281.



NOTES:
1. FREQ. ADJUST: ADJUST TRIM POT FOR OUTPUT FREQUENCY OF 100kHz ±5%.
2. FOR SLAVE OPERATION, REMOVE JUMPER FROM SYNC OUT AND SYNC IN PINS.
3. USE CERAMIC CAPACITOR, "COG" OR "NPO" CHARACTERISTIC.

Figure 11. 100kHz Oscillator Interconnection Diagram

The block diagram of model 281 is shown in Figure 12. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.



*LEAVE TERMINAL 6 OPEN, WHEN POWER IS APPLIED TO TERMINAL 7.

Figure 12. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 292As. As shown in Figure 13, an additional model 281 may be driven in a slave-mode to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

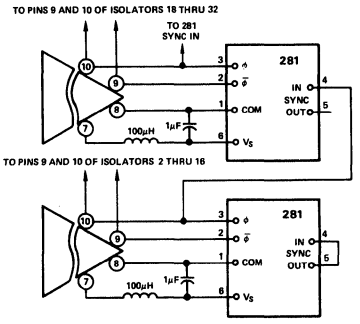


Figure 13. External Oscillator Interconnection

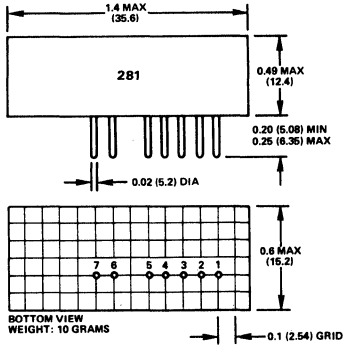
5

SPECIFICATIONS
(typical @ +25°C and V_S = +15V dc unless otherwise noted)

MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C

[1] Model 292A oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 292As, additional 281s may be used in a master/slave mode. Refer to Figure 13.
[3] Full load consists of 16 model 292As and 281 oscillator slave.
Specifications subject to change without notice.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC OUTPUT
2	$\bar{\phi}$ OUTPUT	6	+Vs: HIGH RANGE +(14 to 28)V dc
3	ϕ OUTPUT	7	+Vs: LOW RANGE +(8 to 14)V dc
4	SYNC INPUT		

MATING SOCKET:
CINCH #16 DIP OR EQUIVALENT

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, models 290A and 292A can be applied to measure and control off-ground millivolt signals in the presence ±1500V dc CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, models 290A and 292A offer complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of these models.

Figure 14 illustrates how model 290A or 292A can be combined with a low drift, 1μV/°C front-end amplifier, model AD517L, to interface low level transducer signals. Both products provide isolated ±13V dc power and front-end guard in addition to eliminating ground loops and preserving high CMR (100dB @ 60Hz).

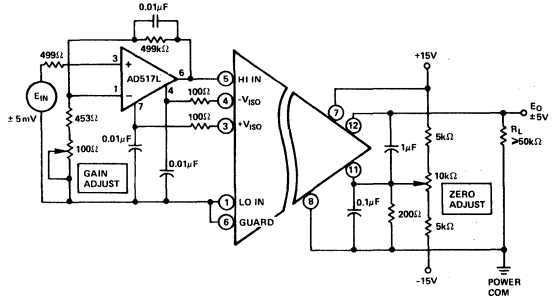


Figure 14. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Models 290A and 292A provide a floating guarded input stage capable of directly accepting isolated differential signals. The noninverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, models 290A and 292A can be connected as shown in Figure 15. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/-IN and IN COM terminals as shown in Figure 15.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum E_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum E_O.
4) Repeat steps 2 and 3 for best CMR performance.

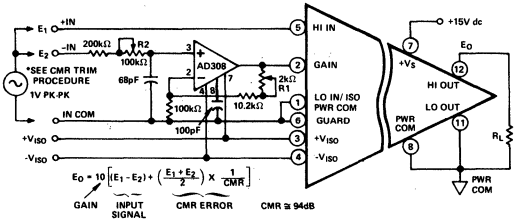


Figure 15. Application of 290A as Instrumentation Amplifier

Isolated Temperature Measurements: Industrial temperature measurements are often performed in harsh environments where line voltages or transients can sometimes be impressed on the temperature sensor. To provide protection for the delicate recording instrumentation, models 290A and 292A can be applied as shown in Figure 16. The Analog Devices' AC2626 probe is a temperature sensor whose output is a current directly proportional to absolute temperature. The isolation amplifier provides the isolated power (+13V dc) as well as the input/output isolation. Zero calibration is performed by placing the AC2626 probe in a zero temperature bath and adjusting R_O for E_O to 0 volts. Full scale output adjustment is performed by placing the AC2626 probe in boiling water (100°C) and adjusting R_S for 1.000V output.

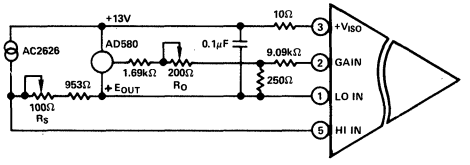


Figure 16. Isolated Temperature Measurements

Current Loop Receiver: Model 290A and 292A can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 17 shows an application of model 290A or 292A as a current loop receiver. A 25Ω resistor converts the 4-20mA current input from a remote loop to a 100–500mV differential voltage input, which the isolator amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the isolator in this kind of measurement are the high common-mode rejection (100dB minimum at 60Hz with 1kΩ source unbalance) and the high common-mode rating (±1500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

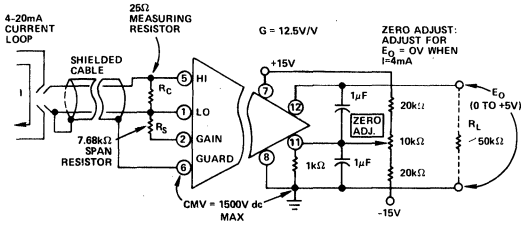


Figure 17. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±1500V of Isolation

Analog Multipliers/Dividers
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Selection Guide
Analog Multipliers/Dividers

Multipliers/Dividers

Model	BW MHz typ[1]	Total Error % FS max	Accuracy vs Temp %/°C typ	Package Options[2]	Temp Range[3]	Page	Comments
AD834	**>500**	**2**		**N, Q, R**	**C, I, M**	**6–65**	**Very High Speed 4-Quad Mult/Div**
AD539	60	1.5–2.5	1–2% (T_{min}–T_{max})	D, N	C, M	6–31	High Speed 2-Channel, 2-Quad Mult/Div
AD534	**1**	**0.25–1.0**	**0.0008–0.022**	**D, E, H**	**C, M**	**6–13**	**High Accuracy 4 Quad Mult/Div**
AD632	1	0.5–1.0	0.01–0.02	D, H	I, M	6–47	High Accuracy Replacement for AD532
AD532	1	1–2	0.01–0.04	D, E, H	C, M	6–7	Accurate 4-Quad Mult/Div
AD538	**0.4**	**0.5–1.0**		**D**	**I, M**	**6–23**	**Simultaneous Mult/Div/Exponentiator**
AD535	0.02	0.5–5.0	0.01–0.05	D, H	C	21–4	Dedicated Divider
AD633	**1**	**1**		N, R	C	**6–51**	**Low Cost 4-Quad Multiplier**
AD734	**10**	**0.15–0.03**	0.003	N, Q	I, M	**6–55**	**High Accuracy Replacement for AD534**

Modulators/Demodulators

Model	Unity Gain BW MHz[1]	Gain	Slew Rate V/μs	Package Options[2]	Temp Range[3]	Page	Comments
AD630	2	±1, ±2	45	**D, E, N**	**C, I, M**	**6–39**	**Balance Modulator/Demodulator with 10 V FS Output**

[1]Unity gain small signal bandwidth.
[2]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; Q–Cerdip; R–Small Outline Plastic (SOIC).
[3]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
Analog Multipliers/Dividers

The devices catalogued in this section are high-performance ICs that accept analog voltages and multiply, divide, square and/or square-root them, depending on device properties and connections. Other multiplying devices available from Analog Devices include digital multipliers (in *DSP Products Databook*) and multiplying D/A converters (*Data Conversion Products Databook*).

Multiplication: For two inputs, V_x and V_y, a multiplier will provide the output, $E_{out} = V_x V_y / E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If $E_{ref} = 10V$, $E_{out} = 10V$ when V_x and V_y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement and mathematical operations in analog computing, curve fitting and linearizing.

If the inputs may be of either positive or negative polarity and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the four quadrants of the X-Y plane.

Squaring: If $V_x = V_y = V_{in}$, a multiplier's output will be V_{in}^2/E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads and mathematical operations.

Division: For a numerator input, V_z, and a denominator input, V_x, an analog divider will provide the output, $E_{out} = E_{ref}(V_z/V_x)$. If $E_{ref} = 10V$, E_{out} will be 10V or less for $V_z \leq V_x$. V_x is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_z. Analog dividers are used to compute ratios – such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements and for mathematical operations in analog computing.

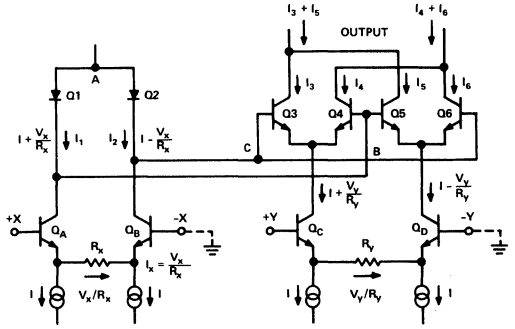
Square Rooting: For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref} V_{in}}$. A square rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, ETC.

A number of devices are listed here, differing in internal architecture, external functional configuration and performance specifications. Most have essentially fixed references; the AD538 is a *multifunction device* that performs the one-quadrant operation, $E_o = V_z/(V_y/V_x)^m$, where m is an exponent adjustable from 1/5 to 5.

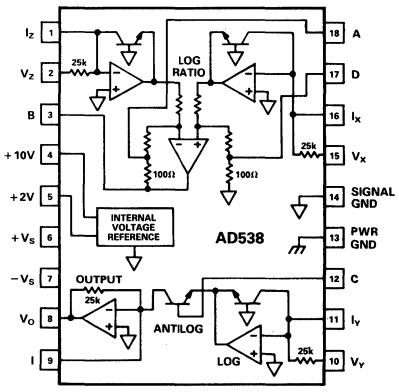
Considerable information on these functions, the nature of devices to perform them and extensive discussions of their applications can be found in the *Nonlinear Circuits Handbook*.[1] A wealth of information is also to be found in the data sheets for the individual devices published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Architecture: All of the devices in this section rely on the logarithmic properties of silicon P-N junctions. An example of the *translinear* principle that they embrace can be seen in the circuitry of a "Gilbert cell," employed in various forms for analog multiplication. Its four-quadrant multiplying circuitry and performance are described in (1), with further references to the original sources. The input voltages are converted to currents; the currents are multiplied together and divided by a reference, and the net output current, $I_x I_y / I_{ref}$, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division.



Basic Four-Quadrant Variable-Transconductance Multiplier Circuit

$$I_O = (I_3 + I_5) - (I_4 + I_6) = \frac{2\,V_X\,V_Y}{I\,R_X\,R_Y}$$



AD538 Functional Block Diagram

In multifunction devices like the AD538, the feedback currents of the V_z and V_x input op amps are used to develop logarithmic voltages across transistor base-emitter junctions; these voltages are differenced to provide the logarithm of the ratio, V_z/V_x.

[1] ***Nonlinear Circuits Handbook*, D.H. Sheingold, ed., 1976, 536pp., $5.95, Analog Devices, Inc., P.O. Box 9106, Norwood, MA 02062-9106**

At the user's choice, this log ratio is either amplified (m>1), attenuated (m<1) or unchanged (m = 1), then applied to a product-antilog circuit which adds the logarithm of V_y, then takes the antilogarithm to produce the output equation,

$$V_{OUT} = V_y \left\{ \frac{V_z}{V_x} \right\}^m$$

Wideband Multipliers have bandwidths greatly exceeding 1MHz. The output is generally in the form of current, for maximum bandwidth (current-to-voltage conversion tends to reduce bandwidth and is unnecessary in many applications). The user can choose an appropriate external amplifier – or other circuitry – to meet the needs of the application. The AD734 is a four-quadrant multiplier/divider with a 10 MHz full power bandwidth and 0.15% satic accuracy specifications. The *AD539* is a dual multiplier/divider with two independent two-quadrant signal channels (inputs Y1 and Y2) and a common X-input, which provides linear control of gain for both channels. Signal bandwidth is 30MHz and control bandwidth is 5MHz. The *AD834* is a four-quadrant multiplier with 500MHz large-signal bandwidth and 0.5% static-accuracy specifications. It has differential X and Y inputs and differential open-collector current output. For 1-volt inputs, its differential output current is ±4mA.

External Functional Configuration: Most of the devices listed here can be used for multiplication, division, squaring and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. Performance of pretrimmed devices is optimized in specified modes of operation. The data sheets show how devices are connected for the various modes of operation; where appropriate, the suggested trim circuits and procedures for optimizing performance are provided.

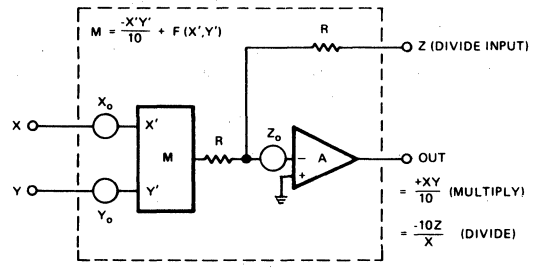
Technologies: The devices described in these two volumes are monolithic integrated circuits. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The pretrimmed ICs use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors as low as 0.15%, and high linearities.

Performance: Multiplier performance, specifications and test circuitry are described in great detail in the *Nonlinear Circuits Handbook*. Here is a brief digest of the factors relating to low-frequency performance.

An ideal multiplier has an output which is the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practical (see the simplified single-ended multiplier in the figure), a multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is a gain-conditioning op amp, A.

Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The



Functional Block Diagram of Typical Multiplier/Divider

figure shows a model with 10-volt scale factor used for considering errors. X_o and Y_o are input offset voltages, Z_o is the offset-referred-to-the-input of the output amplifier, and f(X′, Y′) is the non-linearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form

$$E_o = \frac{XY}{10B} \pm \left[\underbrace{\frac{X_oY}{10B} \pm \frac{XY_o}{10B}}_{\text{Linear "Y"}} \pm \underbrace{Z_o}_{\text{Feedthrough "X"}} + \underbrace{f(X,Y)}_{\text{Nonlinearity and Feedthrough}} \right]$$

Product; X_{offset}, Y_{offset}; Output offset

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by adding external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_x|\epsilon_x + |V_y|\epsilon_y$$

where ϵ_x and ϵ_y are the specified fractional linearity errors (%/100) and V_x and V_Y are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_x$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (i.e., >10:1), will always benefit greatly by the trimming of offsets, especially Z_o (affects offsets) and X_o (affects gain), for small values of X.

DEFINITIONS OF SPECIFICATIONS*

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Scale Factor: The *scale-factor error* (or *gain* error) is the difference between the average scale factor and the ideal scale factor (e.g., $(10V)^{-1}$). It is expressed in percent of the output signal. *Temperature dependence* is specified.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in simple "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the mulitplier may improve small-signal resolution significantly.

Dynamic Parameters include: *small-signal bandwidth, full-power response, slew(ing) rate, small-signal amplitude error* and *settling time.*

Small-Signal Bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

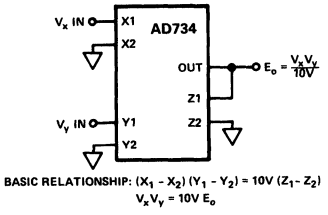
Full-Power Response is the maximum frequency at which the multiplier can produce the full-scale voltage into its rated load without noticeable distortion.

Slew(ing) Rate (V/μs) is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

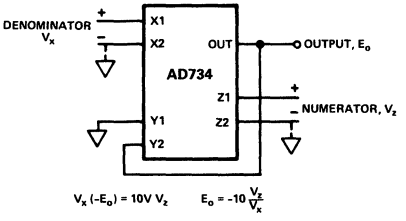
Small-Signal Amplitude Error is defined in relation to the frequency at which the amplitude response, or scale-factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Settling Time, for the product of a ±10V step and 10V dc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

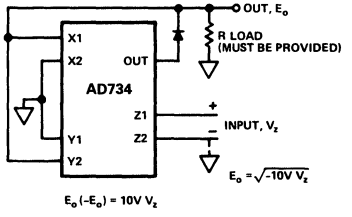
Vector Error is the most sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.



Multiplier



Divider



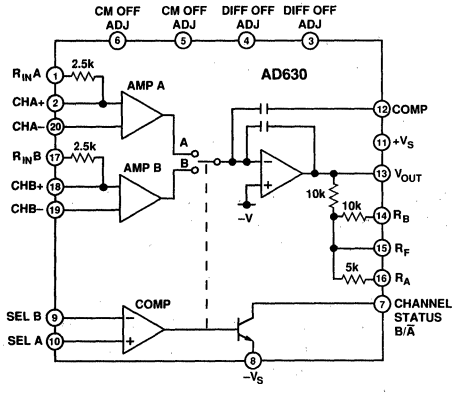
Square Rooter

***These are general definitions. Further definitions are provided as footnotes to the Specifications tables; they should be read carefully.**

MODULATORS/DEMODULATORS

AD630 Balanced Modulator/Demodulator

The AD630 is a fast, flexible, switched dual-input op amp with an on-chip comparator. Intended for wideband, low-level, and wide-dynamic-range instrumentation applications and coherent systems, it is capable of such analog signal-processing functions as balanced modulator, balanced demodulator, absolute-value amplifier, phase detector, square-wave multiplier and two-channel precision multiplexer. It can be used as a lock-in amplifier, synchronous detector, rectifier, dual-mode circuit, and much more. Essentially a complete device with on-chip scaling resistors, it can be used for these functions with little or no additional circuitry.



As a *lock-in amplifier*, it can recover a 0.1-Hz sine wave, transmitted as a modulation on a 400-Hz carrier, from a band-limited, clipped white-noise signal approximately 100,000 times larger – a dynamic range greater than 100dB.

It consists of a frequency-compensated op-amp-output stage, with two identical switched differential front ends (A and B), a differential comparator that controls the switching and a set of jumper-programmable matched precision resistors – trimmed to produce closed-loop gain accuracies to ±0.015% and gain match (between channels) to ±0.03%. When the net input to the comparator is positive, front-end A will be selected; when the comparator input is negative, front-end B is selected. A *status* output indicates the state of the comparator.

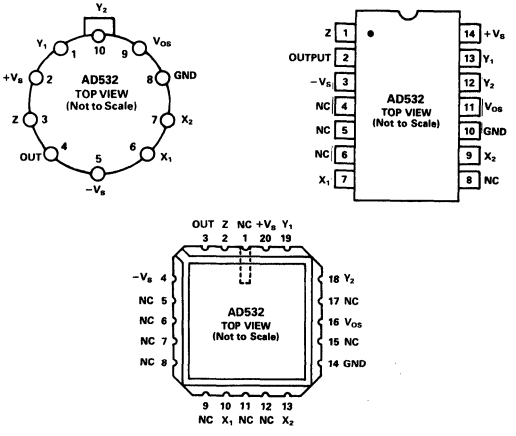
Internally Trimmed Integrated Circuit Multiplier

AD532

FEATURES
- Pretrimmed To ±1.0% (AD532K)
- No External Components Required
- Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
- Diff Inputs For (X_1-X_2) $(Y_1-Y_2)/10V$ Transfer Function
- Monolithic Construction, Low Cost

APPLICATIONS
- Multiplication, Division, Squaring, Square Rooting
- Algebraic Computation
- Power Measurements
- Instrumentation Applications
- Available in Chip Form

AD532 PIN CONFIGURATIONS



PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10V$, divides in two quadrants with a $10VZ/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10VZ}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as $XY/10V$, $(X^2-Y^2)/10V$, $\pm X^2/10V$, and $10VZ/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of -55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can, TO-116 ceramic DIP or LCC packages. J, K and S grade chips are also available.

ADVANTAGES OF ON-THE-CHIP TRIMMING OF THE MONOLITHIC AD532

1. True ratiometric trim for improved power supply rejection.
2. Reduced power requirements since no networks across supplies are required.
3. More reliable since standard monolithic assembly techniques can be used rather than more complex hybrid approaches.
4. High impedance X and Y inputs with negligible circuit loading.
5. Differential X and Y inputs for noise rejection and additional computational flexibility.

SPECIFICATIONS (@ +25°C, $V_S = \pm 15V$, $R \geq 2k\Omega$ V_{OS} grounded)

Model	AD532J Min	AD532J Typ	AD532J Max	AD532K Min	AD532K Typ	AD532K Max	AD532S Min	AD532S Typ	AD532S Max	Units
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$		
Total Error ($-10V \leq X, Y \leq +10V$)		±1.5	**±2.0**		±0.7	**±1.0**		±0.5	**±1.0**	%
T_A = min to max		±2.5			±1.5				**±4.0**	%
Total Error vs Temperature		±0.04			±0.03			±0.01	**±0.04**	%/°C
Supply Rejection (±15V ±10%)		±0.05			±0.05			±0.05		%/%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.8			±0.5			±0.5		%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.3			±0.2			±0.2		%
Feedthrough, X (Y Nulled, X = 20V pk-pk 50Hz)		50	**200**		30	**100**		30	**100**	mV
Feedthrough, Y (X Nulled, Y = 20V pk-pk 50Hz)		30	**150**		25	**80**		25	**80**	mV
Feedthrough vs. Temp.		2.0			1.0			1.0		mV p-p/°C
Feedthrough vs. Power Supply		±0.25			±0.25			±0.25		mV/%
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error		75			75			75		kHz
Slew Rate (V_{OUT} 20 pk-pk)		45			45			45		V/µs
Settling Time (to 2%, ΔV_{OUT} = 20V)		1			1			1		µs
NOISE										
Wideband Noise f = 5Hz to 10kHz		0.6			0.6			0.6		mV (rms)
f = 5Hz to 5MHz		3.0			3.0			3.0		mV (rms)
OUTPUT										
Output Voltage Swing	±10	±13		±10	±13		±10	±13		V
Output Impedance (f≤1kHz)		1			1			1		Ω
Output Offset Voltage		±40				**±30**			**±30**	mV
Output Offset Voltage vs. Temp.		0.7			0.7				**2.0**	mV/°C
Output Offset Voltage vs. Supply		±2.5			±2.5			±2.5		mV/%
INPUT AMPLIFIERS (X, Y and Z)										
Signal Voltage Range (Diff. or CM Operating Diff)		±10			±10			±10		V
CMRR	**40**			**50**			**50**			dB
Input Bias Current										
X, Y Inputs		3			1.5	**4**		1.5	**4**	µA
X, Y Inputs T_{min} to T_{max}		10			8			8		µA
Z Input		±10			±5	**±15**		±5	**±15**	µA
Z Input T_{min} to T_{max}		±30			±25			±25		µA
Offset Current		±0.3			±0.1			±0.1		µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\ Z/(X_1-X_2)$			$10V\ Z/(X_1-X_2)$			$10V\ Z/(X_1-X_2)$		
Total Error										
($V_X = -10V$, $-10V \leq V_Z \leq +10V$)		±2			±1			±1		%
($V_X = -1V$, $-10V \leq V_Z \leq +10V$)		±4			±3			±3		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$		
Total Error		±0.8			±0.4			±0.4		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function		$-\sqrt{10VZ}$			$-\sqrt{10VZ}$			$-\sqrt{10VZ}$		
Total Error ($0V \leq V_Z \leq 10V$)		±1.5			±1.0			±1.0		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±10		**±18**	±10		**±18**	±10		±22	V
Supply Current										
Quiescent		**4**	**6**		**4**	**6**		**4**	**6**	mA
PACKAGE OPTIONS[1]										
TO-116 (D-14)	**AD532JD**			**AD532KD**			**AD532SD**			
TO-100 (H-10a)	**AD532JH**			**AD532KH**			**AD532SH**			
LCC (E-20A)							**AD532SE**			

NOTE
[1]See Section 20 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown in Figure 1, and the complete schematic in Figure 2. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{out} = (X_1-X_2)(Y_1-Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{os} in critical applications . . . . otherwise the V_{os} pin should be grounded.

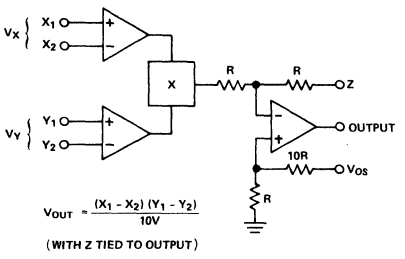


Figure 1. Functional Block Diagram

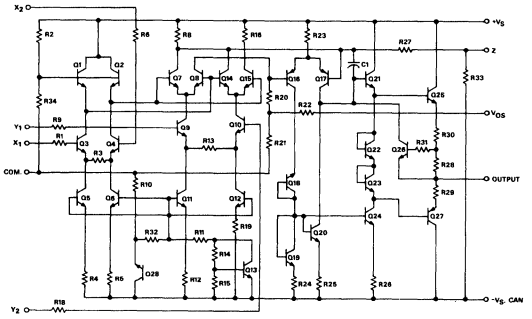


Figure 2. AD532 Schematic Diagram

ORDERING GUIDE

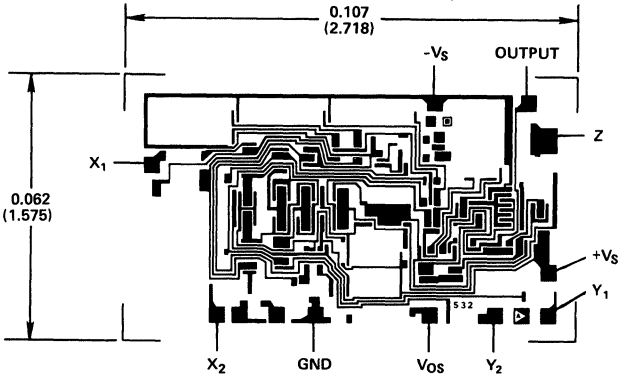
Temperature Range	Header (H)	Sidebrazed DIP	Leadless Chip Carrier (E)	Chips
Commercial 0 to +70°C	AD532JH AD532KH	AD532JD AD532KD		AD532J, K
Military −55°C to +125°C	AD532SH AD532SH/883B	AD532SD AD532SD/883B	AD532SE AD532SE/883B	AD532S

Thermal Characteristics.

Thermal Characteristics θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C for H-10A
θ_{JC} = 22°C/W for D-14 or E-20A
θ_{JA} = 85°C/W for D-14 or E-20A

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output op amp as shown in Figure 13. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwidth and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \cdot 10V/X_1-X_2)$ where ϵ_m represents multiplier full scale error and drift, and (X_1-X_2) is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 3 and 4 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 4 the sine wave amplitude is 20V(p-p).

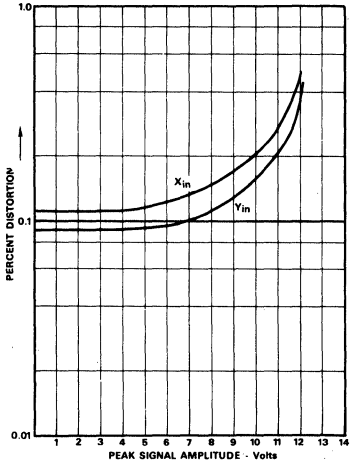


Figure 3. Percent Distortion vs. Input Signal

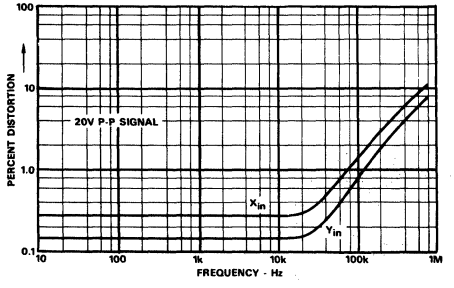


Figure 4. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 5. It is measured for the condition $V_X = 0$, $V_Y = 20V(p-p)$ and $V_Y = 0$, $V_X = 20V(p-p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

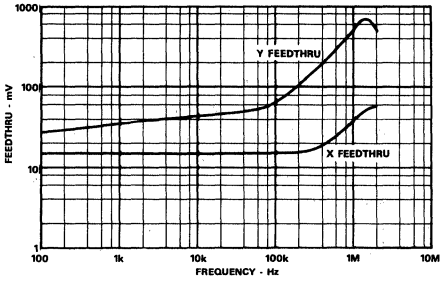


Figure 5. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 6. It is measured with $X_1 = X_2 = 20V(p-p)$, $(Y_1-Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p-p)$, $(X_1-X_2) = \pm 10V$ dc.

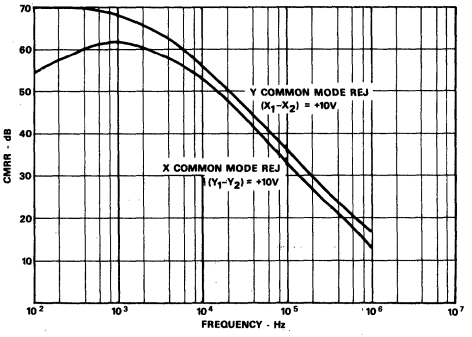


Figure 6. CMRR vs. Frequency

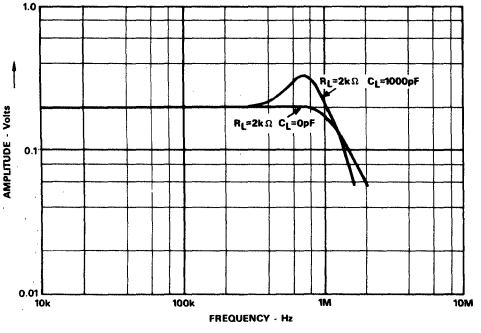


Figure 7. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 7. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 8.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

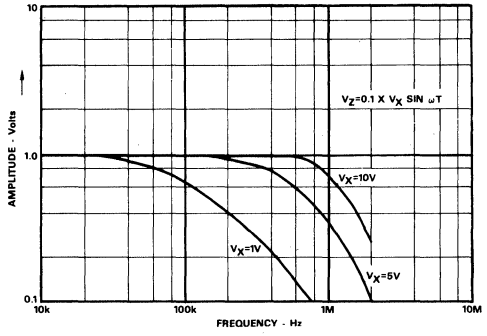


Figure 8. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 9. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

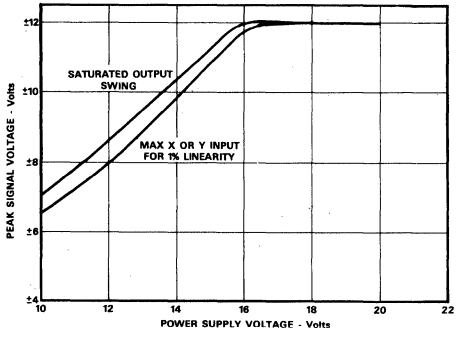


Figure 9. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 10.

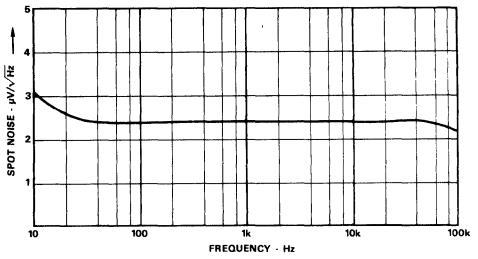


Figure 10. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION

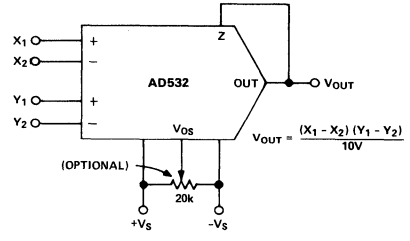


Figure 11. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 11. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see Figure 1). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

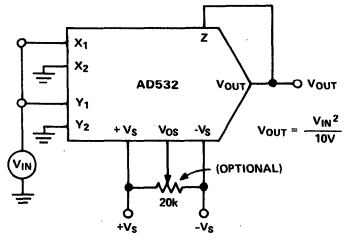


Figure 12. Squarer Connection

The squaring circuit in Figure 12 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

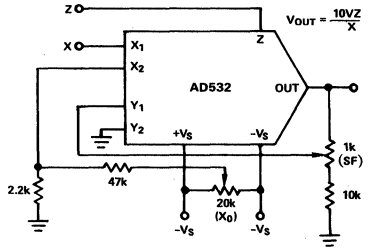


Figure 13. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 13. It should be noted, however, that the output error is given approximately by $10V\epsilon_m/(X_1-X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1-X_2)/10V$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to -10V), connect the input to X and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately $500mV \leq |(X_1-X_2)| \leq 10V$. The voltage offset adjust (V_{OS}), if used, is trimmed with Z at zero and (X_1-X_2) at full scale.

SQUARE ROOT

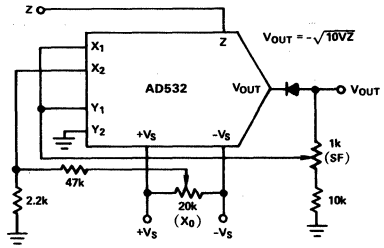


Figure 14. Square Rooter Connection

The connections for square root mode are shown in Figure 14. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{OS} to obtain -1.0V dc in the output, $V_{out} = -\sqrt{10VZ}$. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

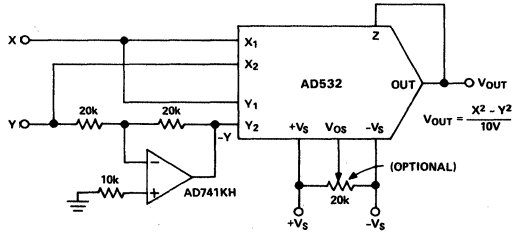


Figure 15. Differential of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2-Y^2/10V$. As shown in Figure 15, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:		Adjust for:	With:	Adjust for:
Adjust	X	Z	V_{out}	Z	V_{out}
Scale Factor	−10V	+10V	-10V	+10V	−10V
X_0 (Offset)	−1V	+0.1V	-1V	+0.1V	−1V

Repeat if required.

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

AD534

FEATURES

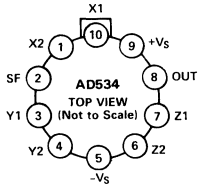
Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz–10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

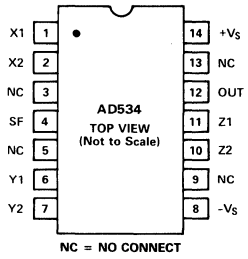
High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters
Available in Chip Form

AD534 PIN CONFIGURATIONS

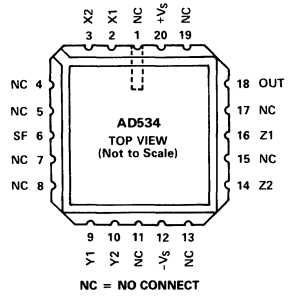
TO-100 (H-10A) Package



TO-116 (D-14) Package



LCC (E-20A) Package



PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00V; by means of an external resistor, this can be reduced to values as low as 3V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, −55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages. AD534J, K, S and T chips are also available.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

SPECIFICATIONS ($T_A = +25°C$, $\pm V_S = 15V$, $R \geq 2k\Omega$)

Model	AD534J Min	AD534J Typ	AD534J Max	AD534K Min	AD534K Typ	AD534K Max	AD534L Min	AD534L Typ	AD534L Max	Units
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] ($-10V \leq X, Y \leq +10V$)			**±1.0**			**±0.5**			**±0.25**	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**		±0.10	**±0.12**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	**±0.1**		±0.005	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**		±0.05	**±0.12**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**		±0.003	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±2	**±10**	mV
Output Offset Voltage Drift		200			100			100		µV/°C
DYNAMICS										
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2		µs
NOISE										
Noise Spectral-Density SF = 10V		0.8			0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1			1			1		mV/rms
f = 10Hz to 10kHz		90			90			90		µV/rms
OUTPUT										
Output Voltage Swing	**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			50		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±2	**±10**	mV
Offset Voltage Drift Z		200			100			100		µV/°C
CMRR	**60**	80		**70**	90		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1			0.05	**0.2**	µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, $-10V \leq Z \leq +10V$)		±0.75			±0.35			±0.2		%
(X − 1V, $-1V \leq Z \leq +1V$)		±2.0			±1.0			±0.8		%
($0.1V \leq X \leq 10V$, $-10V \leq Z \leq 10V$)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error ($-10V \leq X \leq 10V$)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function ($Z_1 \leq Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] ($1V \leq Z \leq 10V$)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±18**	V
Supply Current										
Quiescent		4	**6**		4	6		4	**6**	mA
PACKAGE OPTIONS[6]										
TO-100 (H-10A)		AD534JH			AD534KH			AD534LH		
TO-116 (D-14)		AD534JD			AD534KD			AD534LD		
Chips		AD534J Chips			AD534K Chips					

NOTES

[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.
[6]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD534S Min	AD534S Typ	AD534S Max	AD534T Min	AD534T Typ	AD534T Max	Units
MULTIPLIER PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] (−10V≤X, Y≤+10V)			**±1.0**			**±0.5**	%
T_A = min to max			**±2.0**			**±1.0**	%
Total Error vs Temperature			**±0.02**			**±0.01**	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02				**±0.005**	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift			**500**			**300**	µV/°C
DYNAMICS							
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2		µs
NOISE							
Noise Spectral-Density SF = 10V		0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1.0			1.0		mV/rms
f = 10Hz to 10kHz		90			90		µV/rms
OUTPUT							
Output Voltage Swing	**±11**			**±11**			V
Output Impedance (f≤1kHz)		0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]							
Signal Voltage Range (Diff. or CM Operating Diff.)		±10 ±12			±10 ±12		V V
Offset Voltage X, Y		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z			**500**			**300**	µV/°C
CMRR	**60**	80		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1		µA
Differential Resistance		10			10		MΩ
DIVIDER PERFORMANCE							
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, −10V≤Z≤+10V)		±0.75			±0.35		%
(X = 1V, −1V≤Z≤+1V)		±2.0			±1.0		%
(0.1V≤X≤10V, −10V≤Z≤10V)		±2.5			±1.0		%
SQUARE PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error (−10V≤X≤10V)		±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE							
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] (1V≤Z≤10V)		±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS							
Supply Voltage							
Rated Performance		±15			±15		V
Operating	±8		±22	±8		±22	V
Supply Current							
Quiescent		4	**6**		4	6	mA
PACKAGE OPTIONS[6]							
TO-100 (H-10A)		AD534SH			AD534TH		
TO-116 (D-14)		AD534SD			AD534TD		
E-20A		AD534SE			AD534TE		
Chips		AD534S Chips			AD534T Chips		

NOTES

[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).

[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.

[3]Irreducible component due to nonlinearity: excludes effect of offsets.

[4]Using external resistor adjusted to give SF = 3V.

[5]See functional block diagram for definition of sections.

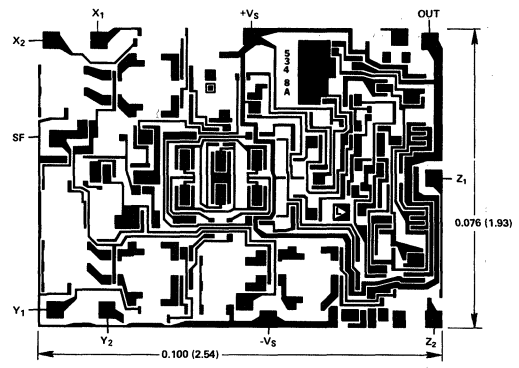
[6]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



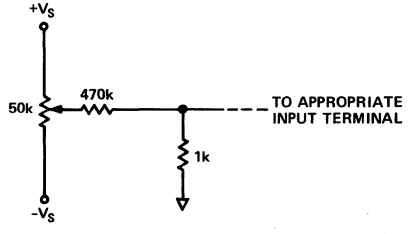
THE AD534 IS AVAILABLE IN LASER-TRIMMED CHIP FORM

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD534J specs.

OPTIONAL TRIMMING CONFIGURATION



Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14 or E-20A
θ_{JA} = 95°C/W for D-14 or E-20A

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.05% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

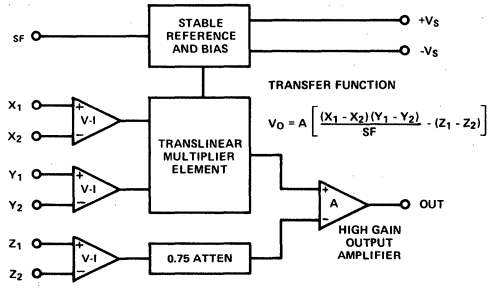


Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak= ±1.25SF)

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

ORDERING GUIDE

Temperature Range	Header (H)	Sidebrazed DIP (D)	Leadless Chip Carrier (E)	Chips
0 to +70°C	AD534JH AD534KH AD534LH	AD534JD AD534KD AD534LD		AD534J, K Chips
−55°C to +125°C	AD534SH AD534SH/883B AD534TH AD534TH/883B	AD534SD AD534SD/883B AD534TD AD534TD/883B	AD534SE AD534SE/883B AD534TE AD534TE/883B	AD534S, T Chips

In most cases the open loop gain can be regarded as infinite, and SF will be 10V. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10V\,(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25SF (i.e., ±5V for SF = 4V) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15V are generally assumed. However, satisfactory operation is possible down to ±8V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

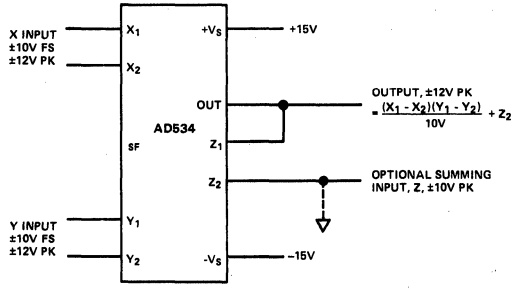


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input (see Optional Trimming Configuration, page 3). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F = 200pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300mV of trim range at the output.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10kΩ resistor, giving a gain of -9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

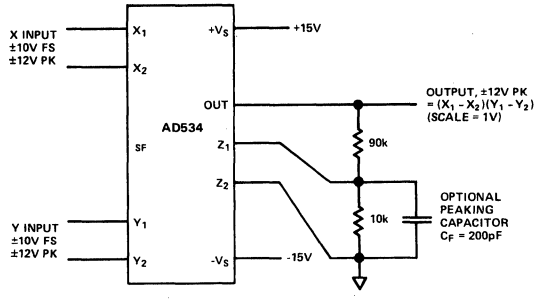


Figure 3. Connections for Scale-Factor of Unity

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

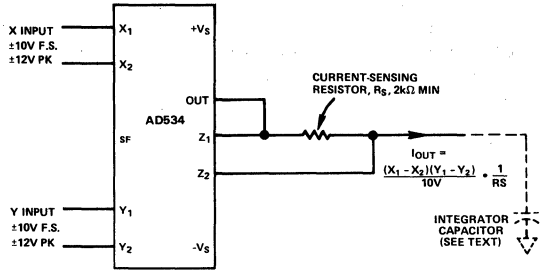


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than ±3V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input (see Optional Trimming Configuration). To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

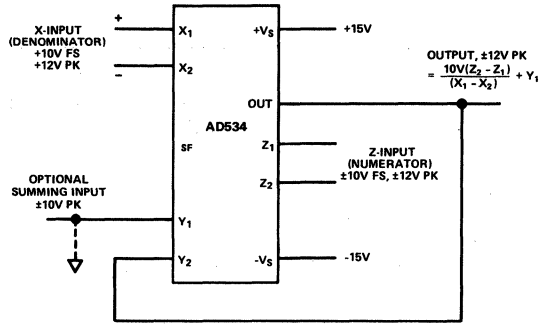


Figure 5. Basic Divider Connection

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

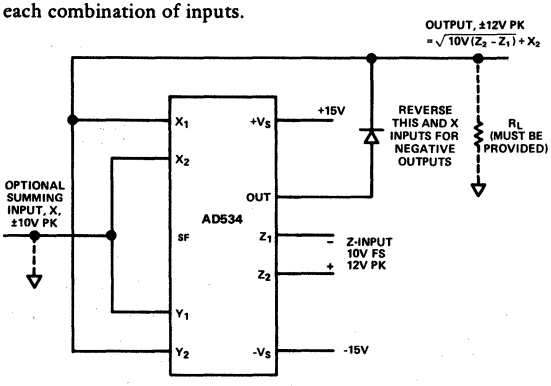


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration) will improve accuracy for inputs below 1V.

*See the AD535 Data Sheet for more details.

The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few.

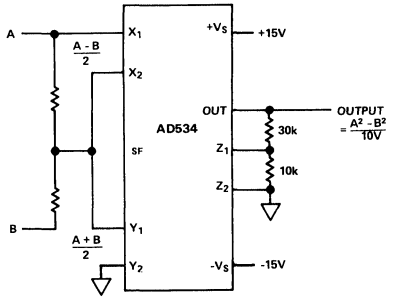
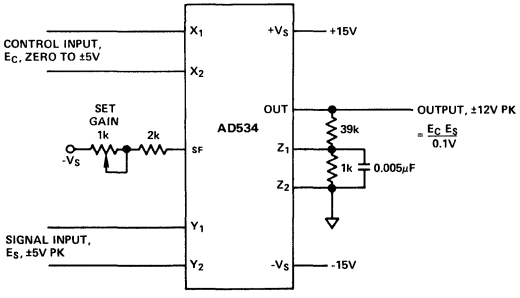
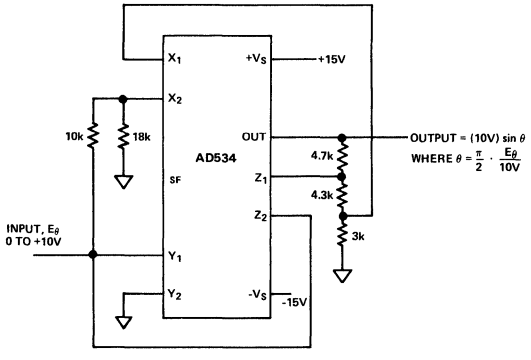


Figure 7. Difference-of-Squares



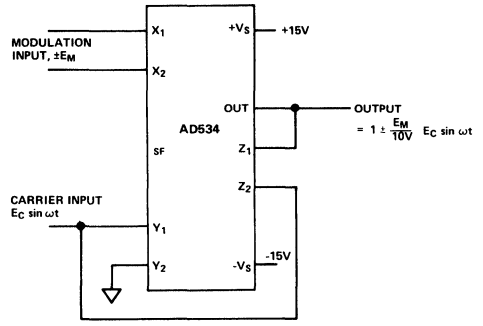
NOTES:
1) GAIN IS X10 PER VOLT OF E_C, ZERO TO X50
2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A F.S. S/N RATIO OF 70dB
3) NOISE REFERRED TO SIGNAL INPUT, WITH E_C = ±5V, IS 60μV RMS, TYP
4) BANDWIDTH IS DC TO 20kHz, -3dB, INDEPENDENT OF GAIN

Figure 8. Voltage-Controlled Amplifier



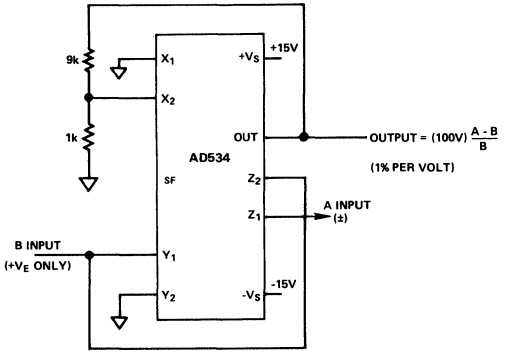
USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 9. Sine-Function Generator



THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION. OPERATION FROM A SINGLE SUPPLY IS POSSIBLE; BIAS Y_2 TO $V_S/2$.

Figure 10. Linear AM Modulator



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

Figure 11. Percentage Computer

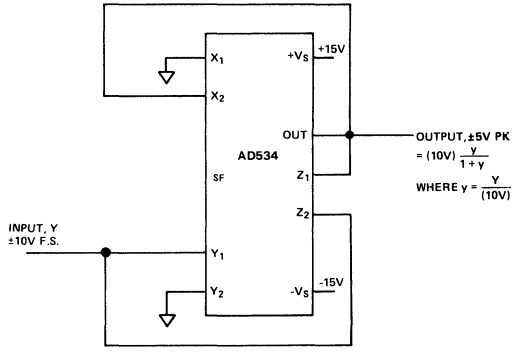
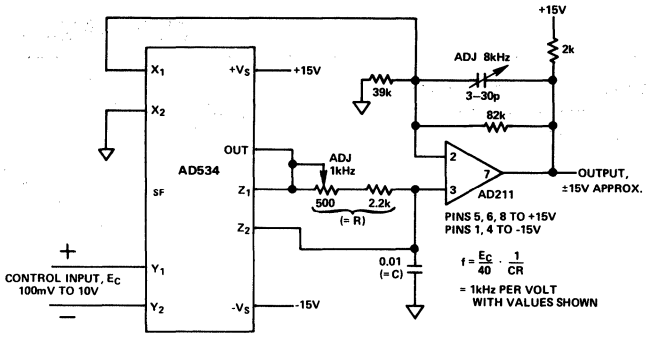


Figure 12. Bridge-Linearization Function



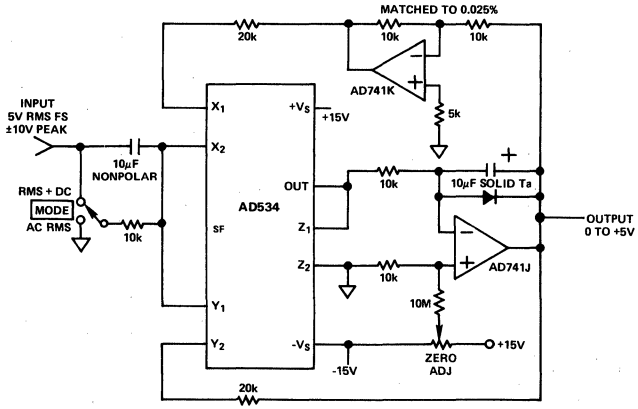
CALIBRATION PROCEDURE:

WITH E_C = 1.0V, ADJUST POT TO SET f = 1.000kHz. WITH E_C = 8.0V, ADJUST TRIMMER CAPACITOR TO SET f = 8.000kHz. LINEARITY WILL TYPICALLY BE WITHIN ±0.1% OF F.S. FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz. FOR FREQUENCIES ABOVE 10kHz THE AD537 VOLTAGE TO FREQUENCY CONVERTER IS RECOMMENDED.

A TRIANGLE-WAVE OF ±5V PK APPEARS ACROSS THE 0.01μF CAPACITOR; IF USED AS AN OUTPUT, A VOLTAGE-FOLLOWER SHOULD BE INTERPOSED.

Figure 13. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE:

WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V; OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

ACCURACY IS MAINTAINED FROM 60Hz to 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR WAVE).

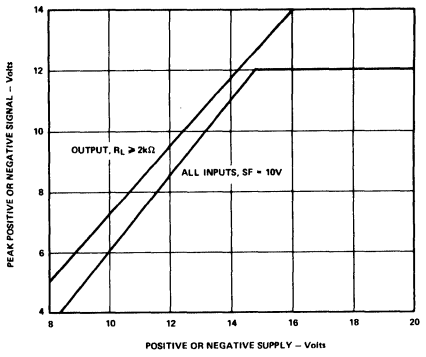
PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY.

INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

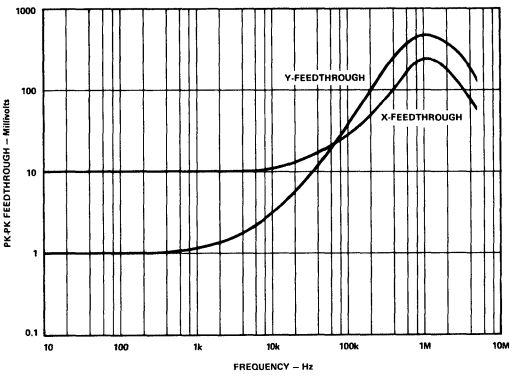
FOR GUARANTEED SPECIFICATIONS THE AD536A AND AD636 IS OFFERED AS A SINGLE PACKAGE RMS-TO-DC CONVERTER.

Figure 14. Wideband, High-Crest Factor, RMS-to-DC Converter

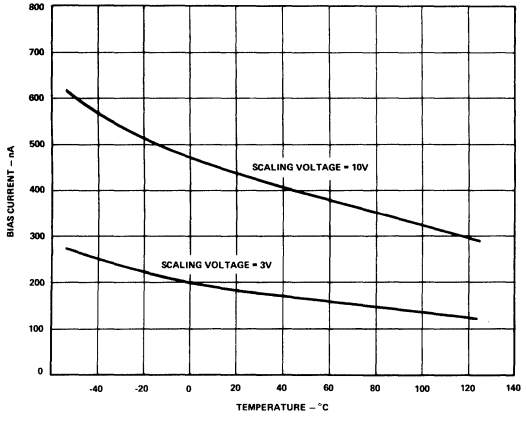
(typical at +25°C, with V_S = ±15V dc, unless otherwise stated)



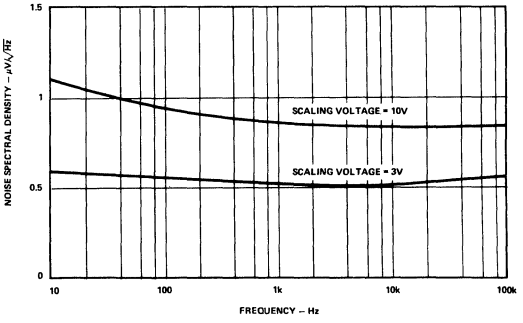
Curve 1. Input/Output Signal Range vs. Supply Voltages



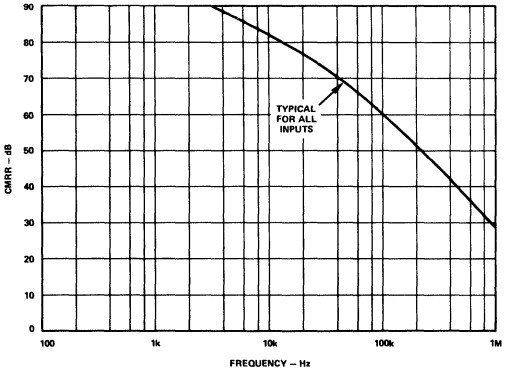
Curve 4. AC Feedthrough vs. Frequency



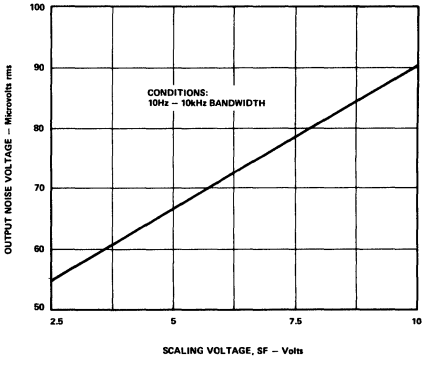
Curve 2. Bias Current vs. Temperature (X, Y or Z Inputs)



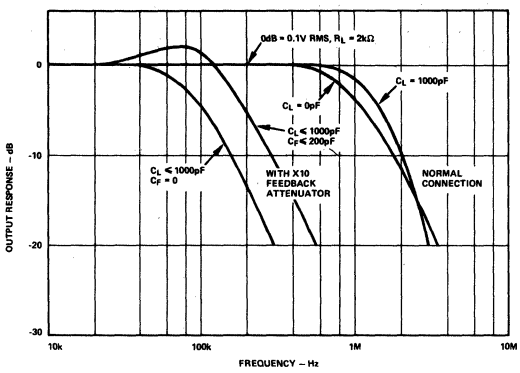
Curve 5. Noise Spectral Density vs. Frequency



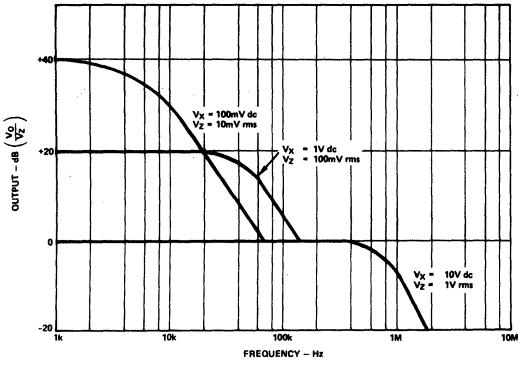
Curve 3. Common-Mode Rejection Ratio vs. Frequency



Curve 6. Wideband Noise vs. Scaling Voltages



Curve 7. Frequency Response as a Multiplier



Curve 8. Frequency Response vs. Divider Denominator Input Voltage

ANALOG DEVICES

Real-Time Analog Computational Unit (ACU)

AD538

FEATURES

$V_{OUT} = V_Y \left(\frac{V_Z}{V_X}\right)^m$ Transfer Function

Wide Dynamic Range (Denominator) −1000:1
Simultaneous Multiplication and Division
Resistor-Programmable Powers & Roots
No External Trims Required
Low Input Offsets <100 μV
Low Error ±0.25% of Reading (100:1 Range)
+2 V and +10 V On-Chip References
Monolithic Construction

APPLICATIONS

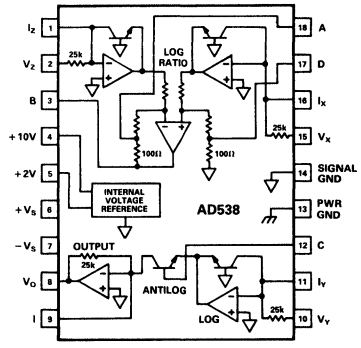
One- or Two-Quadrant Mult/Div
Log Ratio Computation
Squaring/Square Rooting
Trigonometric Function Approximations
Linearization Via Curve Fitting
Precision AGC
Power Functions

PRODUCT DESCRIPTION

The AD538 is a monolithic real-time computational circuit which provides precision analog multiplication, division and exponentiation. The combination of low input and output offset voltages and excellent linearity results in accurate computation over an unusually wide input dynamic range. Laser wafer trimming makes multiplication and division with errors as low as 0.25% of reading possible, while typical output offsets of 100 μV or less add to the overall off-the-shelf performance level. Real-time analog signal processing is further enhanced by the device's 400 kHz bandwidth.

The AD538's overall transfer function is $V_O = V_Y (V_Z/V_X)^m$. Programming a particular function is via pin strapping. No external components are required for one-quadrant (positive input) multiplication and division. Two-quadrant (bipolar numerator) division is possible with the use of external level shifting and scaling resistors. The desired scale factor for both multiplication and division can be set using the on-chip +2 V or +10 V references, or controlled externally to provide simultaneous multiplication and division. Exponentiation with an m value from 0.2 to 5 can be implemented with the addition of one or two external resistors.

AD538 FUNCTIONAL BLOCK DIAGRAM



Direct log ratio computation is possible by utilizing only the log ratio and output sections of the chip. Access to the multiple summing junctions adds further to the AD538's flexibility. Finally, a wide power supply range of ±4.5 V to ±18 V allows operation from standard ±5 V, ±12 V and ±15 V supplies.

The AD538 is available in two accuracy grades (A and B) over the industrial (−25°C to +85°C) temperature range and one grade (S) over the military (−55°C to +125°C) temperature range. The device is packaged in an 18-pin TO-118 hermetic side-brazed ceramic DIP. A-grade chips are also available.

PRODUCT HIGHLIGHTS

1. Real-time analog multiplication, division and exponentiation.
2. High accuracy analog division with a wide input dynamic range.
3. On-chip +2 V or +10 V scaling reference voltages.
4. Both voltage and current (summing) input modes.
5. Monolithic construction with lower cost and higher reliability than hybrid and modular circuits.

SPECIFICATIONS (V_S = ±15 V, T_A = +25°C unless otherwise specified)

Parameters	Conditions	AD538AD Min	AD538AD Typ	AD538AD Max	AD538BD Min	AD538BD Typ	AD538BD Max	AD538SD Min	AD538SD Typ	AD538SD Max	Units
MULTIPLIER/DIVIDER PERFORMANCE											
Nominal Transfer Function											
	$10\ V \geq V_X, V_Y, V_Z \geq 0$		$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$		
	$400\ \mu A \geq I_X, I_Y, I_Z \geq 0$		$V_O = 25\ k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25\ k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25\ k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$		
Total Error Terms	$100\ mV \leq V_X \leq 10\ V$		±0.5	**±1**		±0.25	**±0.5**		±0.5	**±1**	% of Reading +
100:1 Input Range[1]	$100\ mV \leq V_Y \leq 10\ V$		±200	**±500**		±100	**±250**		±200	**±500**	μV
	$100\ mV \leq V_Z \leq 10\ V$										
	$V_Z \leq 10\ V_X$, m = 1.0										
	$T_A = T_{min}$ to T_{max}		±1	**±2**		±0.5	**±1**		±1.25	**+2.5**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	μV
Wide Dynamic Range[2]	$10\ mV \leq V_X \leq 10\ V$		±1	**±2**		±0.5	**±1**		±1	**±2**	% of Reading +
	$1\ mV \leq V_Y \leq 10\ V$		±200	**±500**		±100	**±250**		±200	**±500**	μV +
	$0\ mV \leq V_Z \leq 10\ V$		±100	**±250**		±750	**±150**		±200	**±250**	μV × $(V_Y + V_Z)/V_X$
	$V_Z \leq 10\ V_X$, m = 1.0										
	$T_A = T_{min}$ to T_{max}		±1	**±3**		±1	**±2**		±2	**±4**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	μV +
			±450	±750		±350	**±500**		±750	**±1000**	μV × $(V_Y + V_Z)/V_X$
Exponent (m) Range	$T_A = T_{min}$ to T_{max}	0.2		5	0.2		5	0.2		5	
OUTPUT CHARACTERISTICS											
Offset Voltage	$V_Y = 0, V_C = -600\ mV$		±200	**±500**		±100	**±250**		±200	**±500**	μV
	$T_A = T_{min}$ to T_{max}		±450	**±750**		±350	**±500**		±750	**±1000**	μV
Output Voltage Swing	$R_L = 2\ k\Omega$	−11		**±11**	−11		**+11**	−11		**+11**	V
Output Current		5	10		5	10		5	10		mA
FREQUENCY RESPONSE											
Slew Rate			1.4			1.4			1.4		V/μs
Small Signal Bandwidth	$100\ mV \leq 10\ V_Y, V_Z,$ $V_X \leq 10\ V$		400			400			400		kHz
VOLTAGE REFERENCE											
Accuracy	V_{REF} = 10 V or 2 V		±25	**±50**		±15	**±25**		±25	**±50**	mV
Additional Error	$T_A = T_{min}$ or T_{max}		±20	**±30**		±20	**±30**		±30	**±50**	mV
Output Current	V_{REF} = 10 V to 2 V	**1**	2.5		**1**	2.5		**1**	2.5		mA
Power Supply Rejection											
+2 V = V_{REF}	$\pm 4.5\ V \leq V_S \leq \pm 18\ V$		300	**600**		300	**600**		300	**600**	μV/V
+10 V = V_{REF}	$\pm 13\ V \leq V_S \leq \pm 18\ V$		200	**500**		200	**500**		200	**500**	μV/V
POWER SUPPLY											
Rated	$R_L = 2\ k\Omega$		±15			±15			±15		V
Operating Range[3]		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
PSRR	$\pm 4.5\ V < V_S < \pm 18\ V$ $V_X = V_Y = V_Z = 1\ V$ $V_{OUT} = 1\ V$		0.5	**0.1**		0.05	**0.1**		0.5	**0.1**	%/V
Quiescent Current			4.5	7		4.5	7		4.5	7	mA
TEMPERATURE RANGE											
Rated		−25		+85	−25		+85	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS[4]											
Ceramic (D-18)			AD538AD			AD538BD			AD538SD AD538SD/883B		
Chips			AD538A Chips								

NOTES

[1]Over the 100 mV to 10 V operating range total error is the sum of a percent of reading term and an output offset. With this input dynamic range the input offset contribution to total error is negligible compared to the percent of reading error. Thus, it is specified indirectly as a part of the percent of reading error.

[2]The most accurate representation of total error with low level inputs is the summation of a percent of reading term, an output offset and an input offset multiplied by the incremental gain $(V_Y + V_Z)/V_X$.

[3]When using supplies below ±13 V the 10 V reference pin *must* be connected to the 2 V pin in order for the AD538 to operate correctly.

[4]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

RE-EXAMINATION OF MULTIPLIER/DIVIDER ACCURACY

Traditionally, the "accuracy" of (actually the errors of) analog multipliers and dividers have been specified in terms of percent of full scale. Thus specified, a 1% multiplier error with a 10 V full-scale output would mean a worst case error of +100 mV at "any" level within its designated output range. While this type of error specification is easy to test, evaluate, and interpret, it can leave the user guessing as to how useful the multiplier actually is at low output levels, those approaching the specified error limit (in this case) 100 mV.

The AD538's error sources do not follow the percent of full-scale approach to specification, thus it more optimally fits the needs of the very wide dynamic range applications for which it is best suited. Rather than as a percent of full scale, the AD538's error as a multiplier or divider for a 100:1 (100 mV to 10 V) input range is specified as the sum of two error components: a percent of reading (ideal output) term plus a fixed output offset. Following this format the AD538AD, operating as a multiplier or divider with inputs down to 100 mV, has a maximum error of ±1% of reading ±500 μV. Some sample total error calculations for both grades over the 100:1 input range are illustrated in the chart below. This error specification format is a familiar one to designers and users of digital voltmeters where error is specified as a percent of reading ± a certain number of digits on the meter readout.

For operation as a multiplier or divider over a wider dynamic range (>100:1), the AD538 has a more detailed error specification which is the sum of three components: a percent of reading term, an output offset term and an input offset term for the V_Y/V_X log ratio section. A sample application of this specification, taken from the chart below, for the AD538AD with V_Y = 1 V, V_Z = 100 mV and V_X = 10 mV would yield a maximum error of ±2.0% of reading ±500 μV ±(1 V + 100 mV)/10 mV × 250 μV or ±2.0% of reading ±500 μV ± 27.5 mV. This example illustrates that with very low level inputs the AD538's incremental gain $(V_Y + V_Z)/V_X$ has increased to make the input offset contribution to error substantial.

6

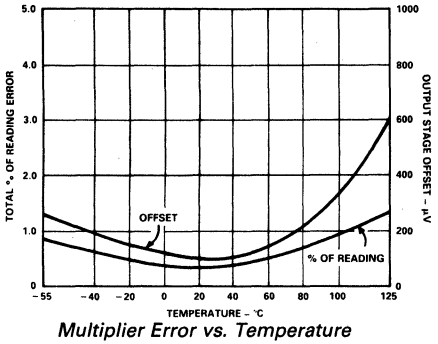
AD538 SAMPLE ERROR CALCULATION CHART (Worst Case)

	V_Y Input (in V)	V_Z Input (in V)	V_X Input (in V)	Ideal Output (in V)	Total Offset Error Term (in mV)	% of Reading Error Term (in mV)	Total Error Summation (in mV)	Total Error Summation as a % of the Ideal Output
100:1 INPUT RANGE Total Error = ±% rdg ±Output V_{OS}	10	10	10	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	10	0.1	0.1	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	1	1	1	1	0.5 (AD) 0.25 (BD)	10 (AD) 5 (BD)	10.5 (AD) 5.25 (BD)	1.05 (AD) 0.5 (BD)
	0.1	0.1	0.1	0.1	0.5 (AD) 0.25 (BD)	1 (AD) 0.5 (BD)	1.5 (AD) 0.75 (BD)	1.5 (AD) 0.75 (BD)
WIDE DYNAMIC RANGE Total Error = ±% rdg ±Output V_{OS} ±Input V_{OS} × $(V_Y+V_Z)/V_X$	1	0.10	0.01	10	28 (AD) 16.75 (BD)	200 (AD) 100 (BD)	228 (AD) 116.75 (BD)	2.28 (AD) 1.17 (BD)
	10	0.05	2	0.25	1.76 (AD) 1 (BD)	5 (AD) 2.5 (BD)	6.76 (AD) 3.5 (BD)	2.7 (AD) 1.4 (BD)
	5	0.01	0.01	5	125.75 (AD) 75.4 (BD)	100 (AD) 50 (BD)	225.75 (AD) 125.4 (BD)	4.52 (AD) 2.51 (BD)
	10	0.01	0.1	1	25.53 (AD) 15.27 (BD)	20 (AD) 10 (BD)	45.53 (AD) 25.27 (BD)	4.55 (AD) 2.53 (BD)

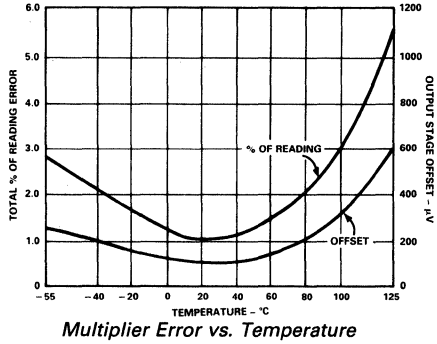
ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 250 mW
Output Short Circuit-to-Ground . . . . . Indefinite
Input Voltages V_X, V_Y, V_Z . . . . . (+V_S −1 V), −1 V
Input Currents I_X, I_Y, I_Z, I_O . . . . . 1 mA
Operating Temperature Range . . . . . −25°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Storage . . . . . 60 sec, +300°C
Thermal Resistance
θ_{JC} . . . . . .35°C/W
θ_{JA} . . . . . 120°C/W

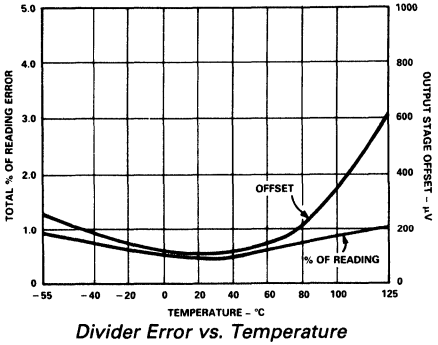
Typical Characteristics



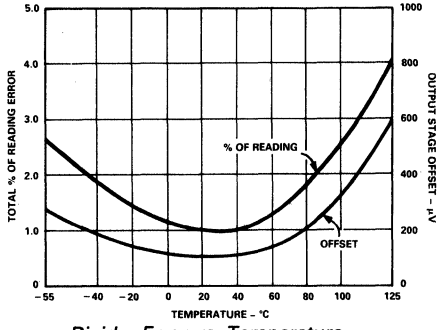
Multiplier Error vs. Temperature
(100 mV < V_X, V_Y, V_Z ≤ 10 V)



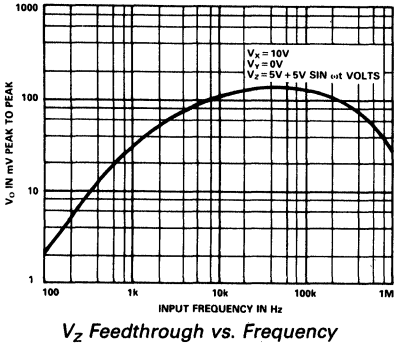
Multiplier Error vs. Temperature
(10 mV < V_X, V_Y, V_Z ≤ 100 mV)



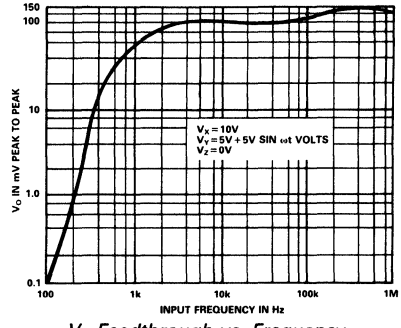
Divider Error vs. Temperature
(100 mV < V_X, V_Y, V_Z ≤ 10 V)



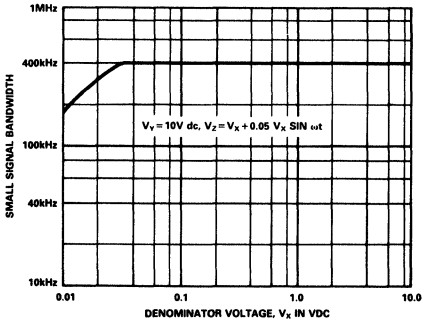
Divider Error vs. Temperature
(10 mV < V_X, V_Y, V_Z ≤ 100 mV)



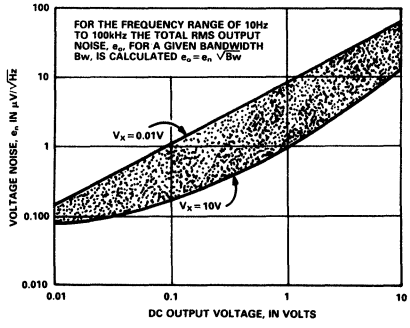
V_Z Feedthrough vs. Frequency



V_Y Feedthrough vs. Frequency



Small Signal Bandwidth vs. Denominator Voltage
(One-Quadrant Mult/Div)



1 kHz Output Noise Spectral Density vs. DC Output Voltage

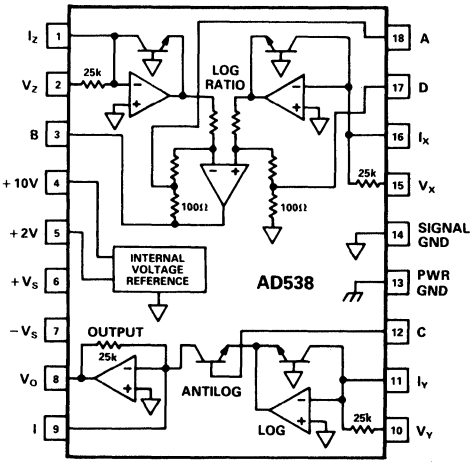


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figures 1 and 2, the V_Z and V_X inputs connect directly to the AD538's input log ratio amplifiers. This subsection provides an output voltage proportional to the natural log of input voltage V_Z, minus the natural log of input voltage V_X. The output of the log ratio subsection at B can be expressed by the transfer function:

$$V_B = \frac{kT}{q} ln \left(\frac{V_Z}{V_X}\right)$$

(where $k = 1.3806 \times 10^{-23}$ J/K, $q = 1.60219 \times 10^{-19}$ C, T is in Kelvins)

The log ratio configuration may be used alone, if correctly temperature compensated and scaled to the desired output level (see Applications section).

Under normal operation, the log-ratio output will be connected directly to a second functional block at input C, the antilog subsection. This section performs the antilog according to the transfer function:

$$V_O = V_Y e^{\left(V_C \frac{q}{kT}\right)}$$

As with the log-ratio circuit included in the AD538, the user may use the antilog subsection by itself. When both subsections are combined, the output at B is tied to C, the transfer function of the AD538 computational unit is:

$$V_O = V_Y e^{\left[\left(\frac{kT}{q}\right)\left(\frac{q}{kT}\right) ln \left(\frac{V_Z}{V_X}\right)\right]} \quad ; V_B = V_C$$

which reduces to:

$$V_O = V_Y \left(\frac{V_Z}{V_X}\right)$$

Finally, by increasing the gain or attenuating the output of the log ratio subsection via resistor programming, it is possible to raise the quantity V_Z/V_X to the m^{th} power. Without external programming, m is unity. Thus the overall AD538 transfer function equals:

$$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$$

where $0.2 < m < 5$

When the AD538 is used as an analog divider, the V_Y input can be used to multiply the ratio V_Z/V_X by a convenient scale factor. The actual multiplication by the V_Y input signal is accomplished by adding the log of the V_Y input signal to the signal at C which is already in the log domain.

STABILITY PRECAUTIONS

At higher frequencies, the multi-staged signal path of the AD538, as illustrated in Figure 2, can result in large phase shifts. If a condition of high incremental gain exists along that path (e.g., $V_O = V_Y \times V_Z/V_X = 10\ V \times 10\ mV/10\ mV = 10\ V$ so that $\Delta V_O/\Delta V_X = 1000$), then small amounts of capacitive feedback from V_O to the current inputs I_Z or I_X can result in instability. Appropriate care should be exercised in board layout to prevent capacitive feedback mechanisms under these conditions.

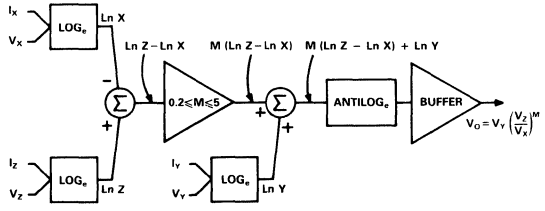


Figure 2. Model Circuit

USING THE VOLTAGE REFERENCES

A stable bandgap voltage reference for scaling is included in the AD538. It is laser-trimmed to provide a selectable voltage output of +10 V buffered (Pin 4), +2 V unbuffered (Pin 5) or any voltages between +2 V and +10.2 V buffered as shown in Figure 3. The output impedance at Pin 5 is approximately 5 kΩ. Note that any loading of this pin will produce an error in the +10 V reference voltage. External loads on the +2 V output should be greater than 500 kΩ to maintain errors less than 1%.

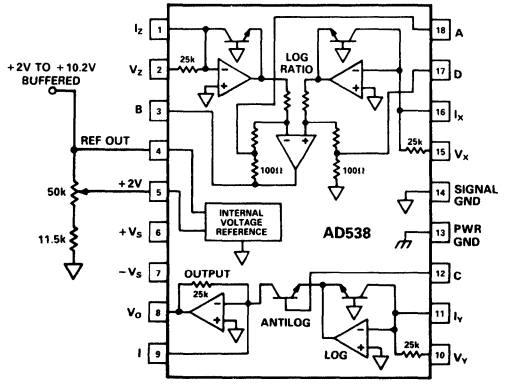


Figure 3. +2 V to +10.2 V Adjustable Reference

In situations not requiring both reference levels, the +2 V output can be converted to a buffered output by tying Pins 4 and 5 together. If both references are required simultaneously, the +10 V output should be used directly and the +2 V output should be externally buffered.

ONE-QUADRANT MULTIPLICATION/DIVISION

Figure 4 shows how the AD538 may be easily configured as a precision one-quadrant multiplier/divider. The transfer function $V_{OUT} = V_Y (V_Z/V_X)$ allows "three" independent input variables, a calculation not available with a conventional multiplier. In addition, the 1000:1 (i.e., 10 mV to 10 V) input dynamic range of the AD538 greatly exceeds that of analog multipliers computing one-quadrant multiplication and division.

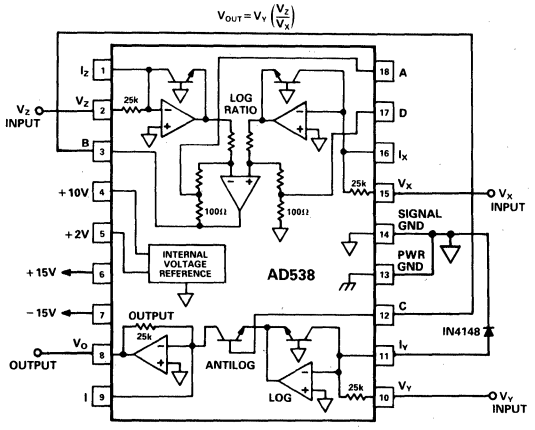


Figure 4. One-Quadrant Combination Multiplier/Divider

By simply connecting the input V_X (Pin 15) to the +10 V reference (Pin 4), and tying the log-ratio output at B to the antilog input at C, the AD538 can be configured as a one-quadrant analog multiplier with 10 volt scaling. If 2 volt scaling is desired, V_X can be tied to the +2 V reference.

When the input V_X is tied to the +10 V reference terminal, the multiplier transfer function becomes:

$$V_O = V_Y\left(\frac{V_Z}{10\ V}\right)$$

As a multiplier, this circuit provides a typical bandwidth of 400 kHz with values of V_X, V_Y or V_Z varying over a 100:1 range (i.e., 100 mV to 10 V). The maximum error with a 100 mV to 10 V range for the two input variables will typically be +0.5% of reading. Using the optional Z offset trim scheme, as shown in Figure 5, this error can be reduced to +0.25% of reading.

By using the +10 V reference as the V_Y input, the circuit of Figure 4 is configured as a one-quadrant divider with a fixed scale factor. As with the one-quadrant multiplier, the inputs accept only single (positive) polarity signals. The output of the one-quadrant divider with a +10 V scale factor is:

$$V_O = 10\ V\left(\frac{V_Z}{V_X}\right)$$

The typical bandwidth of this circuit is 370 kHz with 1 V to 10 V denominator input levels. At lower amplitudes, the bandwidth gradually decreases to approximately 200 kHz at the 2 mV input level.

TWO-QUADRANT DIVISION

The two-quadrant linear divider circuit illustrated in Figure 5 uses the same basic connections as the one-quadrant version. However, in this circuit the numerator has been offset in the positive direction by adding the denominator input voltage to it. The offsetting scheme changes the divider's transfer function from:

$$V_O = 10\ V\left(\frac{V_Z}{V_X}\right)$$

to:

$$V_O = 10\ V\frac{(V_Z + AV_X)}{V_X} = 10\ V\left(1A + \frac{V_Z}{V_X}\right)$$

$$= 10\ A + 10\ V\left(\frac{V_Z}{V_X}\right);\ where\ A = \frac{35\ k\Omega}{25\ k\Omega}$$

As long as the magnitude of the denominator input is equal to or greater than the magnitude of the numerator input, the circuit will accept bipolar numerator voltages. However, under the conditions of a 0 V numerator input, the output would incorrectly equal +14 V. The offset can be removed by connecting the +10 V reference through resistors R1 and R2 to the output section's summing node I at Pin 9 thus providing a gain of 1.4 at the center of the trimming potentiometer. The pot R2 adjusts out or corrects this offset, leaving the desired transfer function of 10 V (V_Z/V_X).

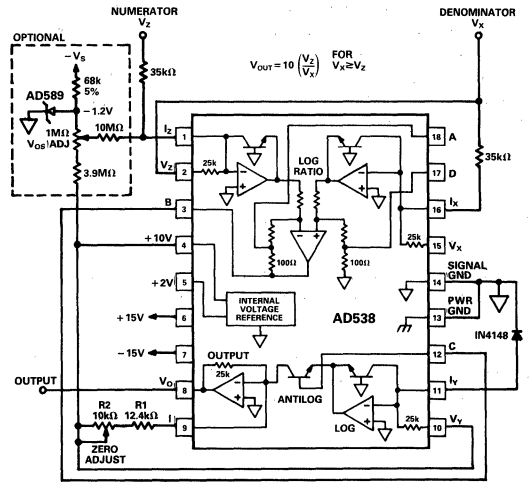


Figure 5. Two-Quadrant Division with 10 V Scaling

LOG RATIO OPERATION

Figure 6 shows the AD538 configured for computing the log of the ratio of two input voltages (or currents). The output signal from B is connected to the summing junction of the output amplifier via two series resistors. The 90.9 Ω metal film resistor effectively degrades the temperature coefficient of the ±3500 ppm/°C resistor to produce a 1.09 kΩ +3300 ppm/°C equivalent value. In this configuration, the V_Y input must be tied to some voltage less than zero (−1.2 V in this case) removing this input from the transfer function.

The 5 kΩ potentiometer controls the circuit's scale factor adjustment providing a +1 V per decade adjustment. The output offset potentiometer should be set to provide a zero output with $V_X = V_Z = 1$ V. The input V_O adjustment should be set for an output of 3 V with $V_Z = 1$ mV and $V_X = 1$ V.

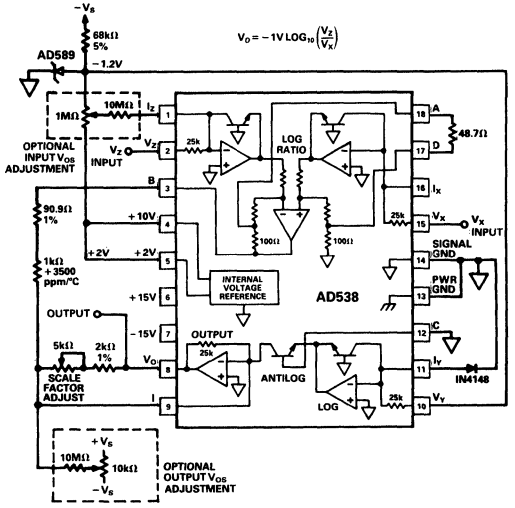


Figure 6. Log Ratio Circuit

The log ratio circuit shown achieves ±0.5% accuracy in the log domain for input voltages within three decades of input range: 10 mV to 10 V. This error is not defined as a percent of full-scale output, but as a percent of input. For example, using a 1 V/decade scale factor, a 1% error in the positive direction at the INPUT of the log ratio amplifier translates into a 4.3 mV deviation from the ideal OUTPUT (i.e., 1 V × $\log_{10}$ (1.01) = 4.3214 mV). An input error 1% in the negative direction is slightly different, giving an output deviation of 4.3648 mV.

ANALOG COMPUTATION OF POWERS AND ROOTS

Often it is necessary to raise the quotient of two input signals to a power or take a root. This could be squaring, cubing, square-rooting or exponentiation to some noninteger power. Examples include power series generation. With the AD538, only one or two external resistors are required to set ANY desired power, over the range of 0.2 to 5. Raising the basic quantity V_Z/V_X to a power greater than one requires that the gain of the AD538's log ratio subtractor be increased, via an external resistor between pins A and D. Similarly, a voltage divider which attenuates the log ratio output between points B and C will program the power to a value less than one.

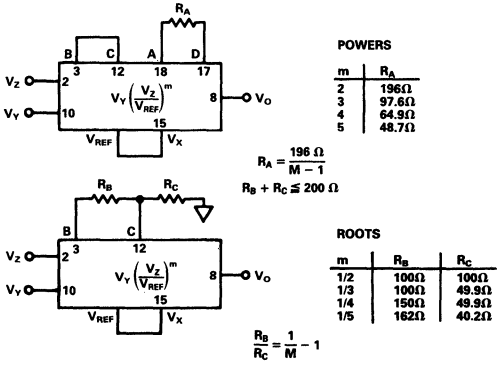


Figure 7. Basic Configurations and Transfer Functions for the AD538

SQUARE ROOT OPERATION

The explicit square root circuit of Figure 8 illustrates a precise method for performing a real time square root computation. For added flexibility and accuracy, this circuit has a scale factor adjustment.

The actual square rooting operation is performed in this circuit by raising the quantity V_Z/V_X to the 1/2 power via the resistor divider network consisting of resistors R_B and R_C. For maximum linearity, the two resistors should be 1% (or better) ratio-matched metal film types.

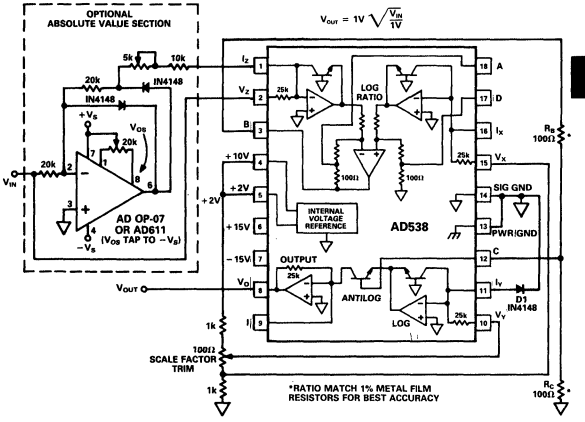


Figure 8. Square Root Circuit

One volt scaling is achieved by dividing-down the 2 V reference and applying approximately 1 V to both the V_Y and V_X inputs. In this circuit, the V_X input is intentionally set low, to about 0.95 V, so that the V_Y input can be adjusted high, permitting a ±5% scale factor trim. Using this trim scheme, the output voltage will be within ±3 mV ±0.2% of the ideal value over a 10 V to 1 mV input range (80 dB). For a decreased input dynamic range of 10 mV to 10 V (60 dB) the error is even less; here the output will be within ±2 mV ±0.2% of the ideal value. The bandwidth of the AD538 square root circuit is approximately 280 kHz with a 1 V p–p sine wave with a +2 V dc offset.

This basic circuit may also be used to compute the cube, fourth or fifth roots of an input waveform. All that is required for a given root is that the correct ratio of resistors, R_C and R_B, be selected such that their sum is between 150 Ω and 200 Ω.

The optional absolute value circuit shown preceding the AD538 allows the use of bipolar input voltages. Only one op amp is required for the absolute value function because the I_Z input of the AD538 functions as a summing junction. If it is necessary to preserve the sign of the input voltage, the polarity of the op amp output may be sensed and used after the computation to switch the sign bit of a D.V.M. chip.

TRANSDUCER LINEARIZATION

Many electronic transducers used in scientific, commercial or industrial equipment monitor the physical properties of a device and/or its environment. Sensing (and perhaps compensating for) changes in pressure, temperature, moisture or other physical phenomenon can be an expensive undertaking, particularly where high accuracy and very low nonlinearity are important. In conventional analog systems accuracy may be easily increased by offset and scale factor trims, however, nonlinearity is usually the absolute limitation of the sensing device.

With the ability to easily program a complex analog function, the AD538 can effectively compensate for the nonlinearities of an inexpensive transducer. The AD538 can be connected between the transducer preamplifier output and the next stage of monitoring or transmitting circuitry. The recommended procedure for linearizing a particular transducer is first to find the closest function which best approximates the nonlinearity of the device and then, to select the appropriate exponent resistor value(s).

ARC-TANGENT APPROXIMATION

The circuit of Figure 9 is typical of those AD538 applications where the quantity V_Z/V_X is raised to powers greater than one. In an approximate arc-tangent function, the AD538 will accurately compute the angle that is defined by X and Y displacements represented by input voltages V_X and V_Z. With accuracy to within one degree (for input voltages between 100 μV and 10 volts), the AD538 arc-tangent circuit is more precise than conventional analog circuits and is faster than most digital techniques. For a direct arc-tangent computation that requires fewer external components refer to the AD639 data sheet. The circuit shown is set up for the transfer function:

$$V_\theta = (V_{\theta ref} - V_\theta)\left[\frac{(V_Z)}{(V_X)}\right]^{1.21}$$

where:

$$\theta = Tan^{-1}\left(\frac{Z}{X}\right)$$

The $(V_{\theta ref} - V_\theta)$ function is implemented in this circuit by adding together the output, V_θ, and an externally applied reference voltage, $V_{\theta ref}$, via an external AD547 op amp. The 1 μF capacitor connected around the AD547's 100 kΩ feedback resistor frequency compensates the loop (formed by the amplifier between V_θ and V_Y).

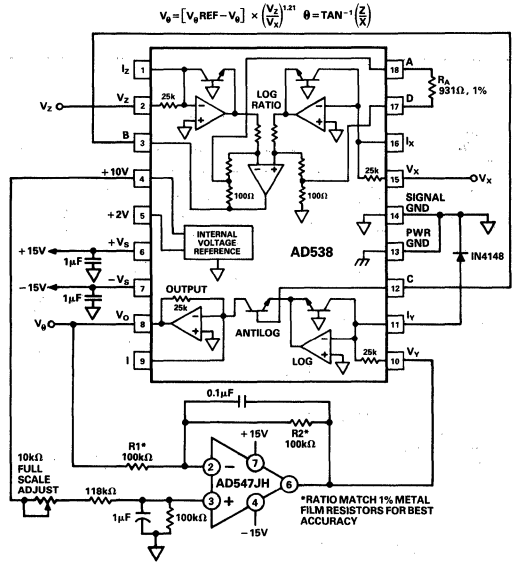


Figure 9. The Arc-Tangent Function

The V_B/V_A quantity is calculated in the same manner as in the one-quadrant divider circuit, except that the resulting quotient is raised to the 1.21 power. Resistor R_A (nominally 931 Ω) sets the power or m factor.

For the highest arc-tangent accuracy the external resistors R1 and R2 should be ratio matched, however, the offset trim scheme shown in other circuits is not required since nonlinearity effects are the predominant source of error. Also note, that instability will occur as the output approaches 90° because, by definition, the arc-tangent function is infinite and therefore, the AD538's gain will be extremely high.

ANALOG DEVICES

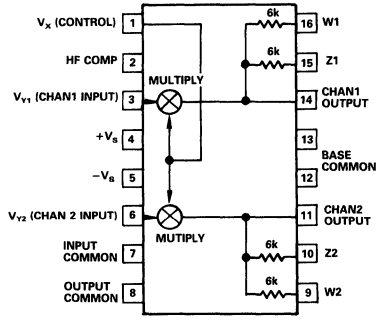
Wideband Dual-Channel Linear Multiplier/Divider

AD539

FEATURES
Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control Channel Bandwidth of 5MHz
Low Distortion (to 0.01%)
Fully-Calibrated, Monolithic Circuit

APPLICATIONS
Precise High Bandwidth AGC and VCA Systems
Voltage-Controlled Filters
Video-Signal Processing
High-Speed Analog Division
Automatic Signal-Leveling
Square-Law Gain/Loss Control

AD539 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD539 is a low-distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X-input providing linear control of gain. Excellent ac characteristics up to video frequencies and a 3dB bandwidth of over 60MHz are provided. Although intended primarily for applications where speed is important the circuit exhibits good static accuracy in "computational" applications. Scaling is accurately determined by a band-gap voltage reference and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100Ω. Output voltage is restricted to a few hundred millivolts under these conditions. Using external op amps such as the AD5539 in conjunction with the on-chip scaling resistors, accurate multiplication can be achieved, with bandwidths typically as high as 50MHz.

The two channels provide flexibility. In single-channel applications they may be used in parallel, to double the output current, or in series, to achieve a square-law gain function with a control range of over 100dB, or differentially, to reduce distortion. Alternatively, they may be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the "state-variable" approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15MHz.

Power consumption is only 135mW using the recommended ±5V supplies. The AD539 is available in three versions: the "J" and "K" grades are specified for 0 to +70°C operation and "S" grade is guaranteed over the extended range of −55°C to +125°C. The J and K grades are available in either a hermetic ceramic DIP (D) or a low cost plastic DIP (N), while the S grade is available only in ceramic. AD539 J-grade chips are also available.

DUAL SIGNAL CHANNELS

The signal voltage inputs, V_{Y1} and V_{Y2}, have nominal full-scale (FS) values of ±2V with a peak range to ±4.2V (using a negative supply of 7.5V or greater). For video applications where differential phase is critical a reduced input range of ±1 volt is recommended, resulting in a phase variation of typically ±0.2° at 3.579MHz for full gain. The input impedance is typically 400kΩ shunted by 3pF. Signal channel distortion is typically well under 0.1% at 10kHz and can be reduced to 0.01% by using the channels differentially.

COMMON CONTROL CHANNEL

The control channel accepts positive inputs, V_X, from 0 to +3V FS, ±3.3V peak. The input resistance is 500Ω. An external, grounded capacitor determines the small-signal bandwidth and recovery time of the control amplifier; the minimum value of 3nF allows a bandwidth at mid-gain of about 5MHz. Larger compensation capacitors slow the control channel but improve the high-frequency performance of the signal channels.

FLEXIBLE SCALING

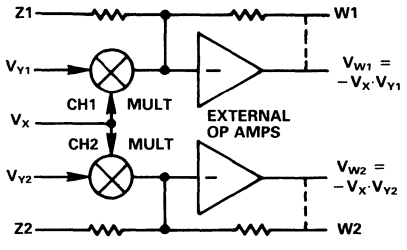
Using either one or two external op amps in conjunction with the on-chip 6kΩ scaling resistors, the output currents (nominally ±1mA FS, ±2.25mA peak) can be converted to voltages with accurate transfer functions of $V_W = -V_X V_Y/2$, $V_W = -V_X V_Y$ or $V_W = -2V_X V_Y$ (where inputs V_X and V_Y and output V_W are expressed in volts), with corresponding full-scale outputs of ±3V, ±6V and ±12V. Alternatively, low-impedance grounded loads can be used to achieve the full signal bandwidth of 60MHz, in which mode the scaling is less accurate.

SPECIFICATIONS (@ T_A = 25°C, V_S = ±5V, unless otherwise specified)

Parameter	Conditions	AD539J Min	AD539J Typ	AD539J Max	AD539K Min	AD539K Typ	AD539K Max	AD539S Min	AD539S Typ	AD539S Max	Units
SIGNAL-CHANNEL DYNAMICS											
Minimal Configuration	Reference Figure 6a										
Bandwidth, −3dB	R_L = 50Ω, C_C = 0.01μF	30	60		30	60		30	60		MHz
Maximum Output	+0.1V<V_X<+3V, $V_Y$ac = 1V rms		−10			−10			−10		dBm
Feedthrough, f<1MHz	V_X = 0, $V_Y$ac = 1.5V rms		−75			−75			−75		dBm
f = 20MHz			−55			−55			−55		dBm
Differential Phase Linearity											
−1V<$V_Y$dc<+1V	f = 3.58MHz, V_X = +3V,		±0.2			±0.2			±0.2		Degrees
−2V<$V_Y$dc<+2V	$V_Y$ac = 100mV		±0.5			±0.5			±0.5		Degrees
Group Delay	V_X = +3V, $V_Y$ac = 1V rms, f = 1MHz		4			4			4		ns
Standard Dual-Channel Multiplier	Reference Figure 2										
Maximum Output	V_X = +3V, $V_Y$ac = 1.5V rms		4.5			4.5			4.5		V
Feedthrough, f<100kHz	V_X = 0, $V_Y$ac = 1.5V rms		1			1			1		mV rms
Crosstalk (CH1 to CH2)	V_{Y1} = 1V rms, V_{Y2} = 0										
	V_X = +3V, f<100kHz		−40			−40			−40		dB
RTO Noise, 10Hz to 1MHz	V_X = +1.5V, V_Y = 0, Figure 2		200			200			200		nV/√Hz
THD + Noise, V_X = +1V,	f = 10kHz, $V_Y$ac = 1V rms		0.02			0.02			0.02		%
V_Y = +3V	f = 10kHz, $V_Y$ac = 1V rms		0.04			0.04			0.04		%
Wide Band Two-Channel Multiplier	Figure 2										
Bandwidth, −3dB (LH0032)	+0.1V<V_X<+3V, $V_Y$ac = 1V rms		25			25			25		MHz
Maximum Output V_Y = +3V	$V_Y$ac = 1.5V rms, f = 3MHz		4.5			4.5			4.5		V rms
Feedthrough V_X = 0V	$V_Y$ac = 1.0V rms, f = 3MHz		14			14			14		mV rms
Wide Band Single Channel VCA (AD5539)	Reference Figure 8										
Bandwidth, −3dB	+0.1V<V_X<+3V, $V_Y$ac = 1V rms		50			50			50		MHz
Maximum Output	75Ω Load		±1			±1			±1		V
Feedthrough	V_X = −0.01V, f = 5MHz		−54			−54			−54		dB
CONTROL CHANNEL DYNAMICS											
Bandwidth, −3dB	C_C = 3000pF, $V_X$dc = +1.5V, $V_X$ac = 100mV rms		5			5			5		MHz
SIGNAL INPUTS, V_{Y1} & V_{Y2}											
Nominal Full-Scale Input			±2			±2			±2		V
Operational Range, Degraded Performance	−V_S≤7V	**±4.2**			**±4.2**			**±4.2**			V
Input Resistance			400			400			400		kΩ
Bias Current			10	**30**		10	**20**		10	**30**	μA
Offset Voltage	V_X = +3V, V_Y = 0		5	**20**		5	**10**		5	**20**	mV
(T_{min} to T_{max})			10			5			15	**35**	mV
Power Supply Sensitivity	V_X = +3V, V_Y = 0		2			2			2		mV/V
CONTROL INPUT, V_X											
Nominal Full-Scale Input			+3.0			+3.0			+3.0		V
Operational Range, Degraded Performance		**+3.2**			**+3.2**			**+3.2**			V
Input Resistance[1]			500			500			500		Ω
Offset Voltage			1	**4**		1	**2**		1	**4**	mV
(T_{min} to T_{max})			3			2			2	**5**	mV
Power Supply Sensitivity			30			30			30		μV/V
Gain	(Figure 2)										
Absolute Gain Error	V_X = +0.1V to +3.0V and		0.2	**0.4**		0.1	**0.2**		0.2	**0.4**	dB
(T_{min} to T_{max})	V_Y = ±2V		0.3			0.15			0.25	**0.5**	dB
CURRENT OUTPUT[1]											
Full-Scale Output Current	V_X = +3V, V_Y = ±2V		±1			±1			±1		mA
Peak Output Current	V_X = +3.3V, V_Y = ±5V, V_S = ±7.5V	±2	±2.8		±2	±2.8		±2	±2.8		mA
Output Offset Current	V_X = 0, V_Y = 0		0.2	**1.5**		0.2	**1.5**		0.2	**1.5**	μA
Output Offset Voltage[2]	Figure 2, V_X = 0, V_Y = 0		3	**10**		3	**10**		3	**10**	mV
Output Resistance[1]			1.2			1.2			1.2		kΩ
Scaling Resistors											
CH1	Z1, W1 to CH1		6			6			6		kΩ
CH2	Z2, W2 to CH2		6			6			6		kΩ
VOLTAGE OUTPUTS, V_{W1} & V_{W2}[2]	(Figure 2)										
Multiplier Transfer Function,			$V_W = -V_X \cdot V_Y/V_U$			$V_W = -V_X \cdot V_Y/V_U$			$V_W = -V_X \cdot V_Y/V_U$		
Either Channel											
Multiplier Scaling Voltage, V_U		**0.98**	1.0	**1.02**	**0.99**	1.0	**1.01**	**0.98**	1.0	**1.02**	V
Accuracy			0.5	**2**		0.5	**1**		0.5	**2**	%
(T_{min} to T_{max})			1			0.5			1.0	**3**	%
Power Supply Sensitivity			0.04			0.04			0.04		%/V
Total Multiplication Error[3]	V_X<=+3V, −2V<V_Y<2V		1	**2.5**		0.6	**1.5**		1	**2.5**	% FSR
T_{min} to T_{max}			2			1			2	**4**	%
Control Feedthrough	V_X = 0 to +3V, V_Y = 0		25	**60**		15	**30**		15	**60**	mV
T_{min} to T_{max}			30			15			60	**120**	mV
TEMPERATURE RANGE											
Rated Performance		0		+70	0		+70	−55		+125	°C
POWER SUPPLIES											
Operational Range		±4.5		±15	±4.5		±15	±4.5		±15	V
Current Consumption											
$+V_S$			8.5	**10.2**		8.5	**10.2**		8.5	**10.2**	mA
$-V_S$			18.5	**22.2**		18.5	**22.2**		18.5	**22.2**	mA
PACKAGE OPTIONS[4]											
Plastic (N-16)			**AD539JN**			**AD539KN**			**AD539SD**		
TO-116 (D-16)			**AD539JD**			**AD539KD**			**AD539SD/883B**		
Chips			**AD539J Chips**								

NOTES
[1]Resistance value and absolute current outputs subject to 20% tolerance.
[2]Spec assumes the external op amp is trimmed for negligible input offset.
[3]Includes all errors.
[4]See Section 20 for package outline information.

Specifications subject to change without notice.
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



AD539 Functional Block Diagram

CIRCUIT DESCRIPTION

Figure 1 is a simplified schematic of the AD539. Q1-Q6 are large-geometry transistors designed for low distortion and low noise. Emitter-area scaling further reduces distortion: Q1 is 3 times larger than Q2; Q4, Q5 are each 3 times larger than Q3, Q6, and these transistors are twice as large as Q1, Q2. A stable reference current I_{REF} = 1.375mA is produced by a band-gap reference circuit and applied to the common emitter node of a *controlled-cascode* formed by Q1 and Q2. When V_X = 0, all of I_{REF} flows in Q1, due to the action of the high-gain control amplifier which lowers the voltage on the base of Q2. As V_X is raised the fraction of I_{REF} flowing in Q2 is forced to balance the control current, V_X/2.5k. At the full-scale value of V_X (+3V) this fraction is 0.873. Since the bases of Q1, Q4 and Q5 are at ground potential and the bases of Q2, Q3 and Q6 are commoned, all three controlled-cascodes divide the current applied to their emitter nodes in the same proportion. The control loop is stabilized by the external capacitor, C_C.

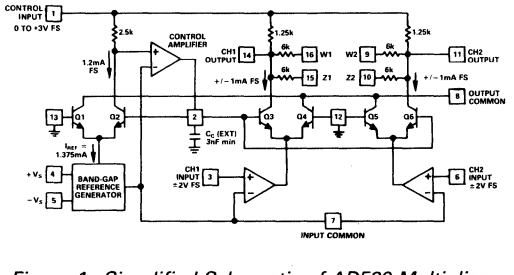


Figure 1. Simplified Schematic of AD539 Multiplier

The signal voltages V_{Y1} and V_{Y2} (generically referred to as V_Y) are first converted to currents by voltage-to-current converters with a g_m of 575μmhos; thus, the full-scale input of ±2V becomes a current of ±1.15mA, which is superimposed on a bias of 2.75mA, and applied to the common emitter node of controlled cascode Q3-Q4 or Q5-Q6. As just explained, the proportion of this current steered to the output node is linearly dependent on V_X. Thus for full-scale V_X and V_Y inputs, a signal of ±1mA (0.873 × ±1.15mA) and a bias component of 2.4mA (0.873 × 2.75mA) appear at the output. The bias component absorbed by the 1.25k resistors also connected to V_X, and the resulting signal current can be applied to an external load resistor (in which case scaling is not accurate) or can be forced into either or both of the 6kΩ feedback resistors (to the Z and W nodes) by an external op amp. In the latter case, scaling accuracy is guaranteed.

GENERAL RECOMMENDATIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high-quality ground plane should be used with the device either soldered directly into the board or mounted in a low-profile socket. In the figures used here an open triangle denotes a *direct, short* connection to this ground plane; pins 12 and 13 are especially prone to unwanted signal pick-up. Power supply decoupling capacitors of 0.1μF to 1μF should be connected from pins 4 and 5 to the ground plane. In applications using external high-speed op amps, separate supply decoupling should be used. It is good practice to insert small (10Ω) resistors between the primary supply and the decoupling capacitor.

The control amplifier compensation capacitor, C_C, should likewise have short leads to ground and a minimum value of 3nF. Unless maximum control bandwidth is esssential it is advisable to use a larger value of 0.01μF to 0.1μF to improve the signal channel phase response, high-frequency crosstalk and high-frequency distortion. The control bandwidth is inversely proportional to this capacitance, typically 2MHz for C_C = 0.01μF, V_X = 1.7V. The bandwidth and pulse response of the control channel can be improved by using a feedforward capacitor of 5% to 20% the value of C_C between pins 1 and 2. Optimum transient response will result when the rise/fall time of V_X are commensurate with the control-channel response time.

V_X should not exceed the specified range of 0 to +3V. The ac gain is zero for V_x<0 but there remains a feedforward path (see Figure 1) causing control feedthrough. Recovery time from negative values of V_X can be improved by adding a small-signal Schottky diode with its cathode connected to pin 2 and its anode grounded. This constrains the voltage swing on C_C. Above V_X = +3.2V, the ac gain limits at its maximum value, but any overdrive appears as control feedthrough at the output.

The power supplies to the AD539 can be as low as ±4.5V and as high as ±16.5V. The maximum allowable range of the signal inputs, V_Y, is approximately 0.5V above $+V_S$; the minimum value is 2.5V above $-V_S$. To accommodate the peak specified inputs of ±4.2V the supplies should be nominally +5V and −7.5V. While there is no performance advantage in raising supplies above these values, it may often be convenient to use the same supplies as for the op amps. The AD539 can tolerate the excess voltage with only a slight effect on dc accuracy but dissipation at ±16.5V can be as high as 535mW and some form of heat-sink is essential in the interests of reliability.

TRANSFER FUNCTION

In using any analog multiplier or divider careful attention must be paid to the matter of *scaling*, particularly in computational applications. To be *dimensionally consistent* a scaling voltage must appear in the transfer function, which, for each channel of the AD539 in the standard multiplier configuration (Figure 2) is

$$V_W = -V_X V_Y / V_U$$

where the inputs V_X and V_Y, the output V_W and the scaling voltage V_U are expressed in a consistent unit, usually volts. In this case, V_U is fixed by the design to be 1V and it is often acceptable in the interest of simplification to use the less rigorous expression

$$V_W = -V_X V_Y$$

where it is understood that *all signals must be expressed in volts*, that is, they are rendered dimensionless by division by (1V).

The accuracy specifications for V_U allow the use of either of the two feedback resistors supplied with each channel, since these are very closely matched, or they may be used in parallel to half the gain (double the effective scaling voltage), when

$$V_W = -V_X V_Y/2.$$

When an external load resistor, R_L, is used the scaling is no longer exact since the internal thin-film resistors, while trimmed to high *ratiometric* accuracy, have an absolute tolerance of 20%. However, the nominal transfer function is

$$V_W = -V_X V_Y/V_U'$$

where the effective scaling voltage, V_U' can be calculated for each channel using the formula $V_U' = V_U\,(5R_L + 6.25)/R_L$, where R_L is expressed in kilohms. For example, when R_L = 100Ω, V_U' = 67.5V. Table II provides more detailed data for the case where both channels are used in parallel. The AD539 can also be used with no external load (output pin 11 or 14 open-circuit), when V_U' is quite accurately 5V.

BASIC MULTIPLIER CONNECTIONS

Figure 2 shows the connections for the standard two-channel multiplier, using op amps to provide useful output power and the AD539 feedback resistors to achieve accurate scaling. The transfer function for each channel is

$$V_W = -V_X V_Y$$

where inputs and outputs are expressed in volts (see TRANSFER FUNCTION). At the nominal full-scale inputs of V_X = +3V, V_Y = ±2V the full-scale outputs are ±6V. Depending on the choice of op amp, their supply voltages usually need to be about 2V more than the peak output. Thus, supplies of at least ±8V are required; the AD539 can share these supplies. Higher outputs are possible if V_X and V_Y are driven to their peak values of +3.2V and ±4.2V respectively, when the peak output is ±13.4V. This requires operating the op amps at supplies of ±15V. Under these conditions it is advisable to reduce the supplies to the AD539 to ±7.5V to limit its power dissipation; however, with some form of heat sinking it is permissible to operate the AD539 directly from ±15V supplies.

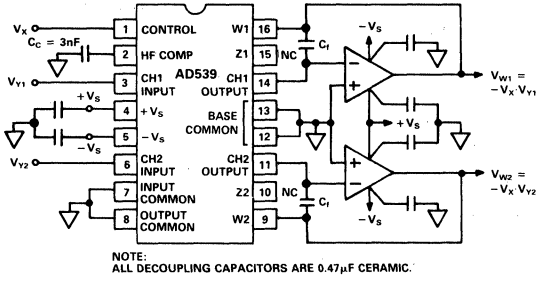


Figure 2. Standard Dual-Channel Multiplier

Viewed as a voltage-controlled amplifier, the decibel gain is simply

$$G = 20 \log V_X$$

where V_X is expressed in volts. This results in a gain of 10dB at V_X = +3.162V, 0dB at V_X = +1V, −20dB at V_X = +0.1V, and so on. In many ac applications the output offset voltage (for V_X = 0 or V_Y = 0) will not be of major concern; however, it can be eliminated using the offset nulling method recommended for the particular op amp, with $V_X = V_Y = 0$.

At small values of V_X the offset voltage of the control channel will degrade the gain/loss accuracy. For example, a ±1mV offset uncertainty will cause the nominal 40dB attenuation at V_X = +0.01V to range from 39.2dB to 40.9dB. Figure 3a shows the maximum gain error boundaries based on the guaranteed control-channel offset voltages of ±2mV for the AD539K and ±4mV for the AD539J. These curves include all scaling errors and apply to all configurations using the internal feedback resistors (W1 and W2; alternatively, Z1 and Z2).

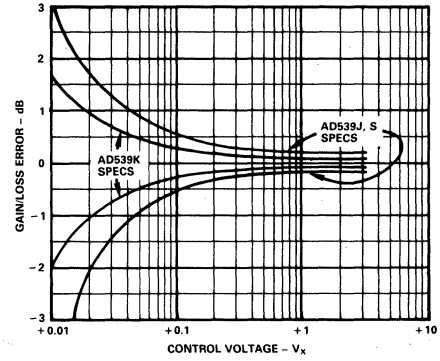


Figure 3a. Maximum ac Gain Error Boundaries

Distortion is a function of the signal input level (V_Y) and the control input (V_X). It is also a function of frequency, although in practice the op amp will generate most of the distortion at frequencies above 100kHz. Figure 3b shows typical results at f = 10kHz as a function of V_X with V_Y = 0.5 and 1.5V rms.

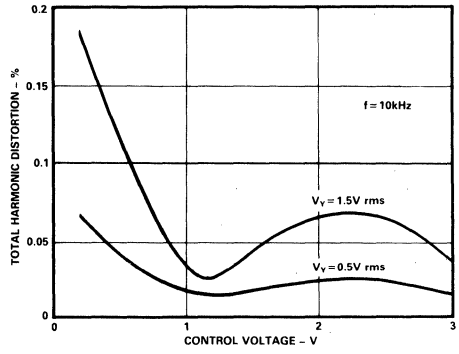


Figure 3b. Total Harmonic Distortion vs. Control Voltage

In some cases it may be desirable to alter the scaling. This can be achieved in several ways. One option is to use both the Z and W feedback resistors (see Figure 1) in parallel, in which case $V_W = -V_X V_Y/2$. This may be preferable where the output swing must be held at ±3V FS (±6.75V pk), for example, to allow the use of reduced supply voltages for the op amps. Alternatively, the gain can be doubled by connecting both channels in parallel and using only a single feedback resistor, in which case $V_W = -2V_X Y_Y$ and the full-scale output is ±12V. Another option is to insert a resistor in series with the control-channel input, permitting the use of a large (for example, 0 to +10V) control voltage. A disadvantage of this scheme is the need to

adjust this resistor to accommodate the tolerance of the nominal 500Ω input resistance at pin 1. The signal channel inputs can also be resistively attenuated to permit operation at higher values of V_Y, in which case it may often be possible to partially compensate for the response roll-off of the op amp by adding a capacitor across the upper arm of this attenuator.

Signal-Channel ac and Transient Response

The HF response is dependent almost entirely on the op amp. Note that the "noise gain" for the op amp in Figure 2 is determined by the value of the feedback resistor (6kΩ) and the 1.25kΩ control-bias resistors (Figure 1). Op amps with provision for external frequency compensation (such as the AD301 and AD518) should be compensated for a closed-loop gain of 6.

The layout of the circuit components is very important if low feedthrough and flat response at low values of V_X is to be maintained (see GENERAL RECOMMENDATIONS).

For wide-bandwidth applications requiring an output voltage swing greater than ±1V, the LH0032 hybrid op-amp is recommended. Figure 4a shows the HF response of the circuit of Figure 2 using this amplifier with V_Y = 1V rms and other conditions as shown in Table I. C_F was adjusted for 1dB peaking at V_X = +1V; the −3dB bandwidth exceeds 25MHz. The effect of signal feedthrough on the response becomes apparent at V_X = +0.01V. The minimum feedthrough results when V_X is taken slightly negative to ensure that the residual control-channel offset is exceeded and the dc gain is reliably zero. Measurements show that the feedthrough can be held to −90dB relative to full output at low frequencies and to −60dB up to 20MHz with careful board layout. The corresponding pulse response is shown in Figure 4b for a signal input of V_Y of ±1V and two values of V_X (+3V and +0.1V).

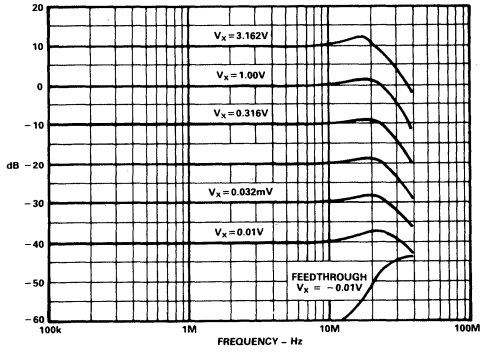
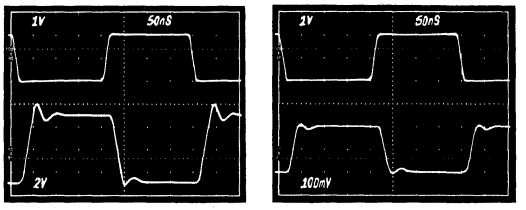


Figure 4a. Multiplier HF Response Using LH0032 Op Amps



V_X = +3V V_X = +0.1V

Figure 4b. Multiplier Pulse Response Using LH0032 Op Amps

	AD711[1]	AD5539[2]	LH0032[1]
Op Amp Supply Voltages	±15V	±9V	±10V
Op Amp Compensation Capacitor	None	None	1-5pF
Feedback Capacitor, C_F	None	0.25-1.5pF	1-4pF
−3dB Bandwidth, V_X = +1V	900kHz	50MHz	25MHz
Load Capacitance	<1nF	<10pF	<100pF
HF Feedthrough, V_X = −0.01V, f = 5MHz	N/A	−54dB	−70dB
rms Output Noise, V_X = +1V, BW 10Hz-10kHz	50μV	40μV	30μV
V_X = +1V, BW 10Hz-5MHz	120μV	620μV	500μV

In all cases, 0.47μF ceramic supply-decoupling capacitors were used at each IC pin, the AD539 supplies were ±5V and the control-compensation capacitor C_C was 3nF.

NOTES
[1]For the circuit of Figure 2. [2]For the circuit of Figure 8.

Table I. Summary of Operating Conditions and Performance for the AD539 When Used with Various External Op-Amp Output Amplifiers

Minimal Wide-Band Configurations

The maximum bandwidth can be achieved using the AD539 with simple resistive loads to convert the output currents to voltages. These currents (nominally ±1mA FS, ±2.25mA pk, into short-circuit loads) are shunted by their source resistance of 1.25kΩ (each channel). Calculations of load power and effective scaling-voltage must allow for this shunting effect when using resistive loads. The output power is quite low in this mode, and the device behaves more like a voltage-controlled attenuator than a classical multiplier. The matching of gain and phase between the two channels is excellent. From dc to 10MHz the gains are typically within ±0.025dB (measured using precision 50Ω load resistors) and the phase difference within ±0.1°.

Load Resistance	50Ω	75Ω	100Ω	150Ω	600Ω	O/C
FS Output Voltage	±92.6mV	±134mV	±172mV	±242mV	±612mV	±1V
	65.5mV rms	94.7mV rms	122mV rms	171mV rms	433mV rms	*
FS Output-Power in Load	0.086mW	0.12mW	0.15mW	0.195mW	0.312mW	–
	−10.5dBm	−9.2dBm	−8.3dBm	−7.1dBm	−5.05dBm	–
Pk Output Voltage	±210mV	±300mV	±388mV	±544mV	±1V	±1V
	148mV rms	212mV rms	274mV rms	385mV rms	*	*
Pk Output-Power in Load	0.44mW	0.6mW	0.75mW	1mW	±1V	±1V
	−7dBm	−4.4dBm	−2.5dBm	0dBm	*	*
Effective Scaling Voltage, V_U'	67.5V	46.7V	36.3V	25.8V	10.2V	5V

*Peak negative voltage swing limited by output compliance.

Table II. Summary of Performance for Minimal Configuration

For a given load resistance the output power can be quadrupled by using both channels in parallel, as shown in Figure 5a. The small-signal silicon diode D connected between ground and pins 12 and 13 provides extra voltage compliance at the output nodes in the negative direction (to −1V at 25°C); it is not required if the output swing does not exceed −300mV. Table II compares performance for various load resistances, using this configuration.

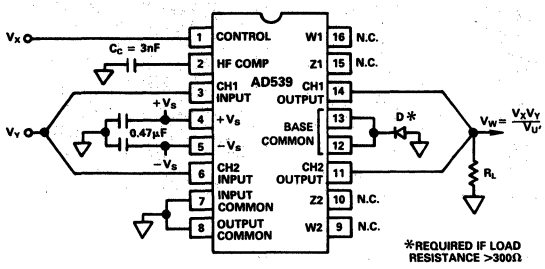


Figure 5a. Minimal Single-Channel Multiplier

Figure 5b shows the HF response for Figure 5a with the AD539 in a carefully-shielded 50Ω test-environment; the test system response was first characterized and this background removed by digital signal processing to show the inherent circuit response.

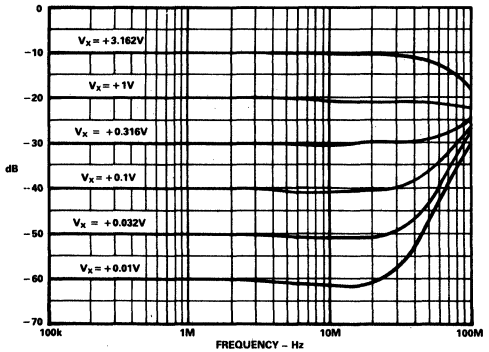


Figure 5b. HF Response in Minimal Configuration

In many applications *phase linearity* over frequency is important. Figure 5c shows the deviation from an ideal linear-phase response for a typical AD539 over the frequency range dc to 10MHz, for

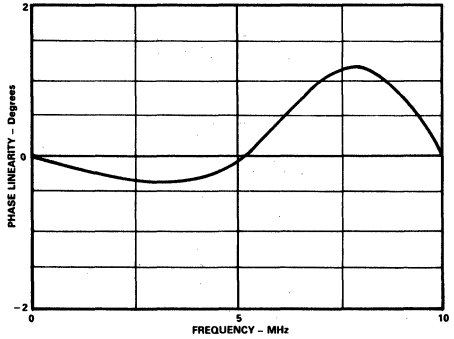


Figure 5c. Phase Linearity Error in Minimal Configuration

V_X = +3V; the peak deviation is slightly more than 1°. *Differential phase linearity* (the stability of phase over the signal window at a fixed frequency) is shown in Figure 5d for f = 3.579MHz and various values of V_X. The most rapid variation occurs for V_Y above +1V; in applications where this characteristic is critical, it is recommended that a ground-referenced, negative-going signal be used.

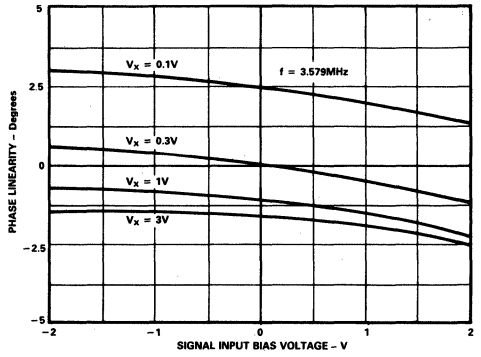


Figure 5d. Differential Phase Linearity in Minimal Configuration for a Typical Device

Differential Configurations

When only one signal channel must be handled it is often advantageous to use the channels differentially. By subtracting the CH1 and CH2 outputs any residual transient control feedthrough is virtually eliminated. Figure 6a shows a minimal configuration where it is assumed that the host system uses differential signals and a 50Ω environment throughout. This figure also shows a recommended control-feedforward network to improve large-signal

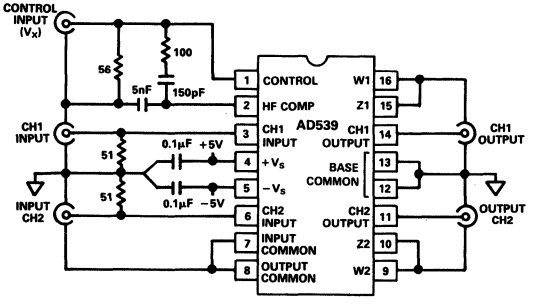


Figure 6a. High-Speed Differential Configuration

response time. The control feedthrough glitch is shown in Figure 6b, where the input was applied to CH1 and only the output of CH1 was displayed on the oscilloscope. The improvement obtained when CH1 and CH2 outputs are viewed differentially is clear in Figure 6c. The envelope rise-time is of the order of 40ns.

Lower distortion results when CH1 and CH2 are driven by *complementary* inputs and the outputs are utilized differentially, using a circuit such as Figure 7a. Resistors R1 and R2 should have a value in the range 100 to 1000Ω.

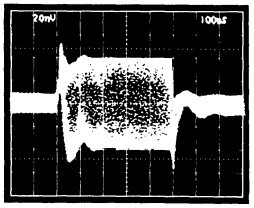


Figure 6b. Control Feedthrough One Channel of Figure 6a

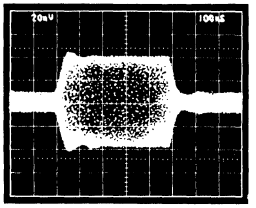


Figure 6c. Control Feedthrough Differential Mode, Figure 6a

They minimize a secondary distortion mechanism caused by a collector-modulation effect in the controlled cascodes (see CIRCUIT DESCRIPTION) by keeping the voltage-swing at the outputs to an acceptable level. Figure 7b shows the improvement in distortion over the standard configuration (compare Figure 3b). Note that the Z nodes (pins 10 and 15) are returned to the control input; this prevents the early onset of output-transistor saturation.

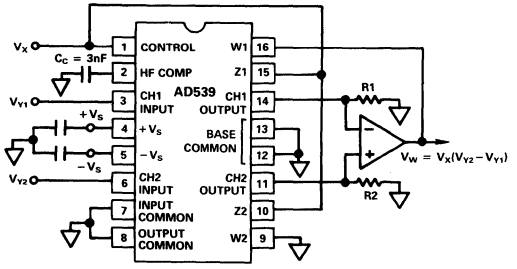


Figure 7a. Low-Distortion Differential Configuration

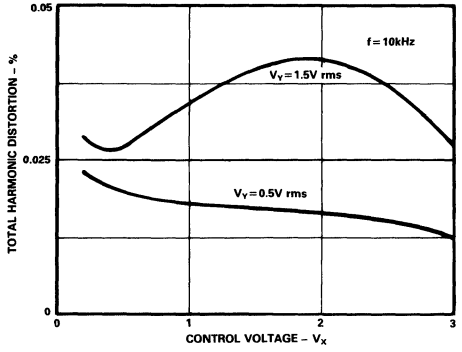


Figure 7b. Distortion in Differential Mode Using LH0032 Op Amp

Even lower distortion (0.01%, or −80dB) has been measured using two output op amps in a configuration similar to Figure 2 connected as virtual-ground current-summers (to prevent the modulation effect). Note that to generate the difference output it is merely necessary to connect the output of the CH1 op amp to the Z node of CH2. In this way, the net input to the CH2 op amp is the difference signal, and the low-distortion resultant appears as its output.

A 50MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 8 is a circuit for a 50MHz voltage-controlled amplifier (VCA) suitable for use in high-quality-video-speed applications. The outputs from the two-signal channels of the AD539 are applied to the op-amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven ($V_X<0$ or $V_X>3.3V$). Secondly, it provides a choice of either non-inverting or inverting responses, using either inputs V_{Y1} or V_{Y2} respectively. In this circuit, the output of the op-amp will equal:

$$V_{OUT} = \frac{V_X (V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

Hence, the gain is unity at $V_X = +2V$. Since V_X can over-range to +3.3V, the maximum gain in this configuration is about 4.3dB. (Note: If pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10dB.)

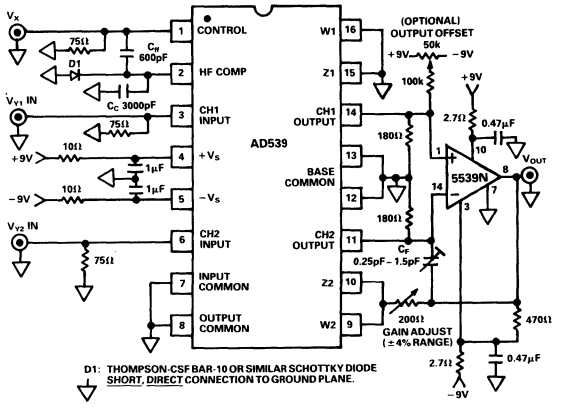


Figure 8. A Wide Bandwidth Voltage-Controlled Amplifier

The −3dB bandwidth of this circuit is over 50MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, *extreme* care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 9a shows the ac response from the noninverting

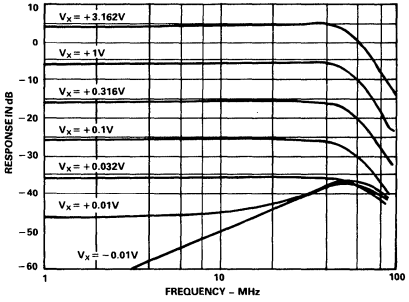


Figure 9a. AC Response of the VCA at Different Gains $V_Y = 0.5V$ RMS

input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5V$ rms for values of V_X from +10mV to +3.16V; this is with a 75Ω load on the output. The feedthrough at $V_X = -10mV$ is also shown.

The transient response of the signal channel at $V_X = +2V$, $V_Y = V_{OUT} = \pm 1V$ is shown in Figure 9b; with the VCA driving a 75Ω load. The rise and fall-times are approximately 7ns.

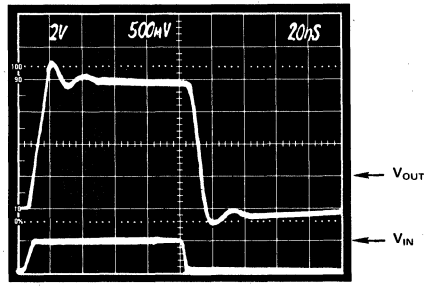


Figure 9b. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts $V_Y = \pm 1$ Volt

A more detailed description of this circuit, including differential gain and phase characteristics, is given in the application note "Low Cost, Two Chip Voltage-Controlled Amplifier and Video Switch" available from Analog Devices.

BASIC DIVIDER CONNECTIONS

Standard Scaling

The AD539 provides excellent operation as a two-quadrant analog divider in wide-band wide gain-range applications, with the advantage of dual-channel operation. Figure 10a shows the simplest connections for division with a transfer function of

$$V_Y = -V_U V_W / V_X$$

Recalling that the nominal value of V_U is 1V, this can be simplified to

$$V_Y = -V_W / V_X$$

where all signals are expressed in volts. The circuit thus exhibits unity gain for $V_X = +1V$ and a gain of 40dB when $V_X = +0.01V$.

The output swing is limited to ±2V nominal full-scale and ±4.2V peak (using a $-V_S$ supply of at least 7.5V for the AD539). Since the maximum *loss* is 10dB (at $V_X = 3.162V$), it follows that the maximum input to V_W should be ±6.3V (4.4V rms) for low distortion applications, and no more than ±13.4V (9.5V rms) to avoid clipping. Note that offset adjustment will be needed

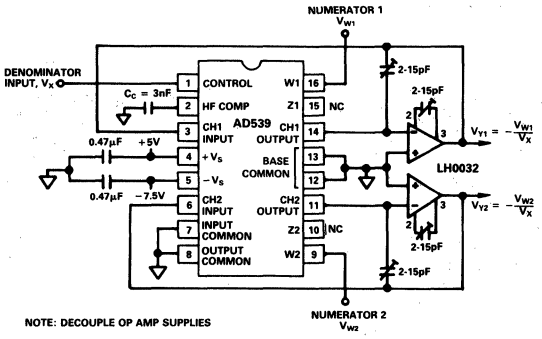


Figure 10a. Two-Channel Divider with 1V Scaling

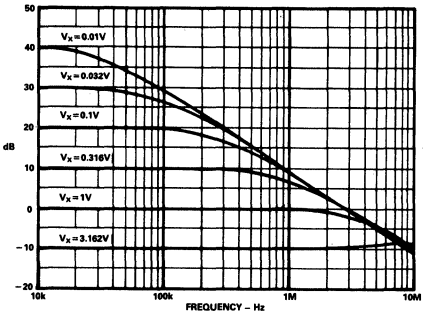


Figure 10b. HF Response of Figure 10a Divider

for the op amps to maintain accurate dc levels at the output in high gain applications: the "noise gain" is $6V/V_X$, or 600 at $V_X = +0.01V$.

The gain-magnitude response for this configuration using the LH0032 op amps with nominally 12pF compensation (pins 2 to 3) and $C_F = 7pF$ is shown in Figure 10b; of course, other amplifiers may also be used. Since there is some manufacturing variation in the HF response of the op amps, and load conditions will also affect the response, these capacitors should be adjustable: 5-15pF is recommended for both positions. The bandwidth in this configuration is nominally 17MHz at $V_X = +3.162V$, 4.5MHz at $V_X = +1V$, 350kHz at $V_X = +0.1V$ and 35kHz at $V_X = +0.01V$. The general recommendations regarding the use of a good ground plane and power-supply decoupling should be carefully observed.

ANALOG DEVICES

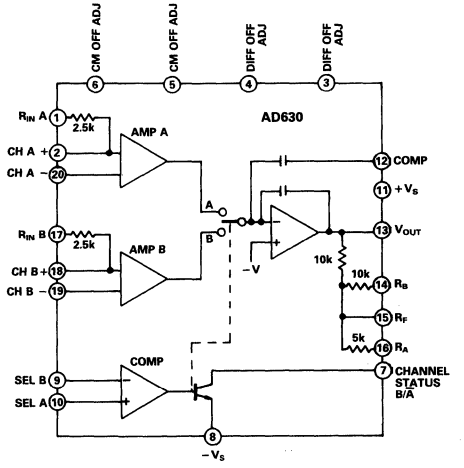
Balanced Modulator/Demodulator

AD630

FEATURES

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth
Chips Available

AD630 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of −100dB @ 10kHz.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common mode and differential offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active.

PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100dB @ 10kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

SPECIFICATIONS (@ +25°C and $\pm V_S$ = ±15V unless otherwise specified)

Model	AD630J/A Min	AD630J/A Typ	AD630J/A Max	AD630K/B Min	AD630K/B Typ	AD630K/B Max	AD630S Min	AD630S Typ	AD630S Max	Units
GAIN										
Open Loop Gain	**90**	110		**100**	120		**90**	110		dB
±1, ±2 Closed Loop Gain Error		0.1				**0.05**		0.1		%
Closed Loop Gain Match		0.1				**0.05**		0.1		%
Closed Loop Gain Drift		2			2			2		ppm°C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			Volts
Input Offset Voltage			**500**			**100**			**500**	μV
Input Offset Voltage										
T_{min} to T_{max}			**800**			**160**			**1000**	μV
Input Bias Current		100	**300**		100	**300**		100	**300**	nA
Input Offset Current		10	**50**		10	**50**		10	**50**	nA
Channel Separation @ 10kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.3V)$			Volts
Switching Window			**±1.5**			**±1.5**			**±1.5**	mV
Switching Window										
T_{min} to T_{max}[2]			**±2.0**			**±2.0**			**±2.5**	mV
Input Bias Current		100	**300**		100	**300**		100	**300**	nA
Response Time (−5mV to +5mV step)		200			200			200		ns
Channel Status										
I_{SINK} @ V_{OL} = $-V_S$ + 0.4V[3]	**1.6**			**1.6**			**1.6**			mA
Pull-Up Voltage			$(-V_S+33V)$			$(-V_S+33V)$			$(-V_S+33V)$	Volts
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[4]		45			45			45		V/μs
Settling Time to 0.1% (20V step)		3			3			3		μs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	**85**	105		**90**	110		**90**	110		dB
Power Supply Rejection	**90**	110		**90**	110		**90**	110		dB
Supply Voltage Range	**±5**		±16.5	**±5**		±16.5	**±5**		±16.5	Volts
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, @ R_L = 2kΩ										
T_{min} to T_{max}	**±10**			**±10**			±10			Volts
Output Short Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
Rated Performance – N Package	0		+70	0		+70		N/A		°C
D Package	−25		+85	−25		+85	−55		+125	°C

NOTES

[1] If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.

[2] This parameter guaranteed but not tested.

[3] I_{SINK} @ V_{OL} = ($-V_S$ + 1) volt is typically 4mA.

[4] Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/μs.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation 600mW
Output Short Circuit to Ground . . . . . Indefinite
Storage Temperature, Ceramic Package . . . −65°C to +150°C
Storage Temperature, Plastic Package . . . . −55°C to +125°C
Lead Temperature, 10 sec. Soldering . . . . . +300°C
Max Junction Temperature . . . . . +150°C

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
20-Pin Plastic DIP (N)	24°C/W	61°C/W
20-Pin Ceramic DIP (D)	35°C/W	120°C/W
20-Pin Leadless Chip Carrier (E)	35°C/W	120°C/W

ORDERING GUIDE*

Temperature Range	Size Brazed DIP (D-20)	Plastic DIP (N-20)	Leadless Chip Carrier (E-20A)	Chips
0 to +70°C		AD630JN AD630KN		AD630 J Chips
−25°C to +85°C	AD630AD AD630BD			
−55°C to +125°C	AD630SD AD630SD/883B		AD630SE AD630SE/883B	AD630S Chips

*See Section 20 for package outline information.

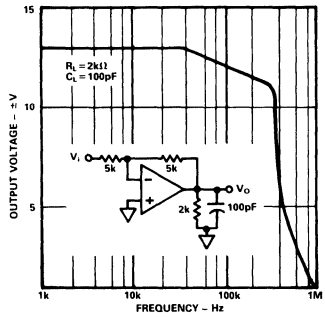


Figure 1. Output Voltage vs. Frequency

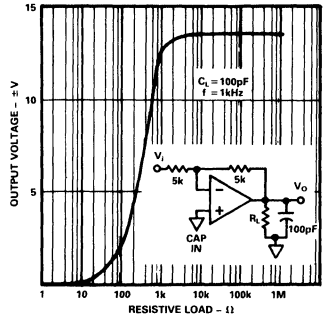


Figure 2. Output Voltage vs. Resistive Load

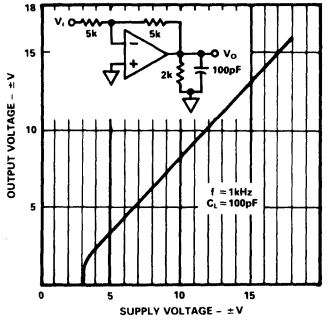


Figure 3. Output Voltage Swing vs. Supply Voltage

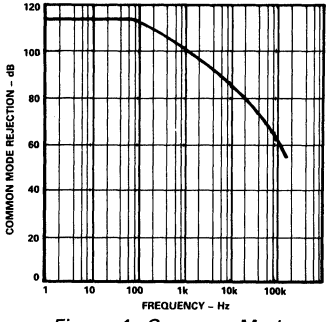


Figure 4. Common Mode Rejection vs. Frequency

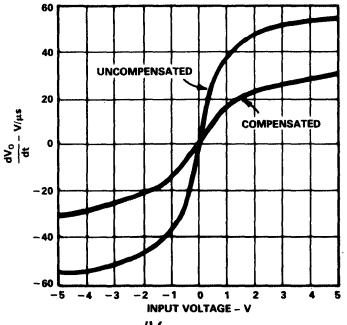


Figure 5. $\frac{dV_O}{dt}$ vs. Input Voltage

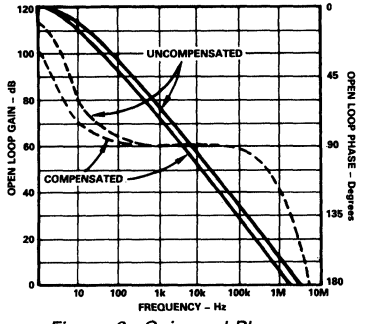
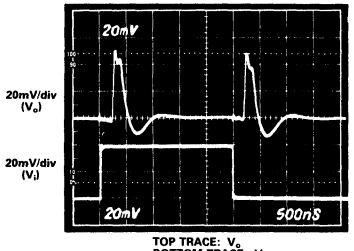
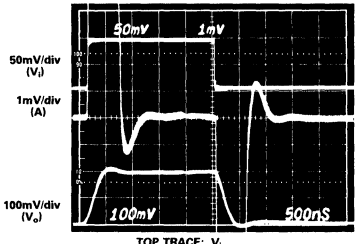
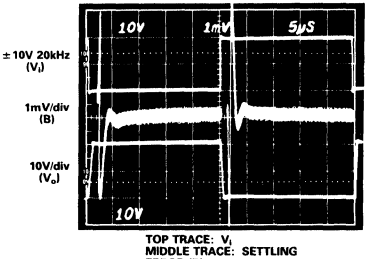


Figure 6. Gain and Phase vs. Frequency







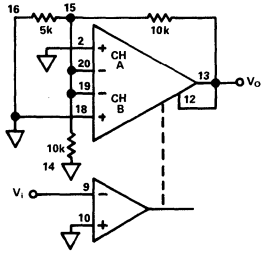


Figure 7. Channel-to-Channel Switch-Settling Characteristic

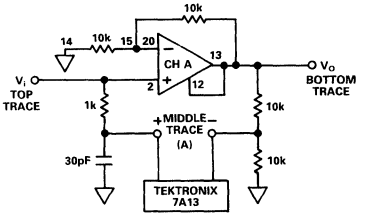


Figure 8. Small Signal Noninverting Step Response

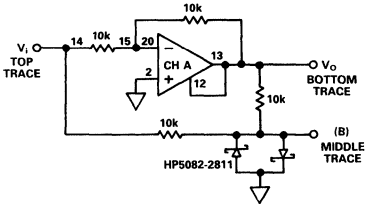
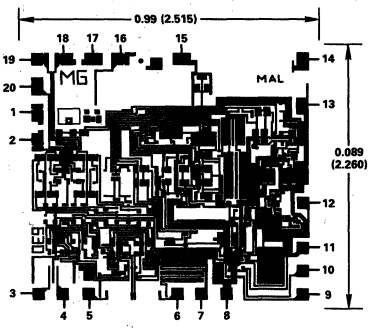


Figure 9. Large Signal Inverting Step Response

CHIP METALIZATION AND PINOUT

Dimensions shown in inches and (mm).
Contact factory for latest dimensions



CHIP AVAILABILITY

The AD630 is available in laser trimmed, passivated chip form. The figure shows the AD630 metalization pattern, bonding pads and dimensions. AD630 chips are available; consult factory for details.

TWO WAYS TO LOOK AT THE AD630

Figure 10 is a functional block diagram of the AD630 which also shows the pin connections of the internal functions. An alternative architectural diagram is shown in Figure 11. In this diagram, the individual A and B channel pre-amps, the switch, and the integrator-output amplifier are combined in a single op amp. This amplifier has two differential input channels, only one of which is active at a time.

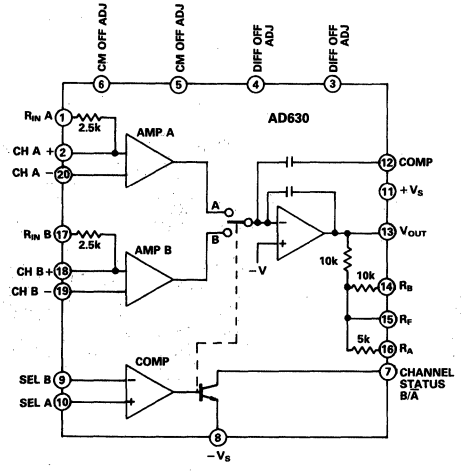


Figure 10. Functional Block Diagram

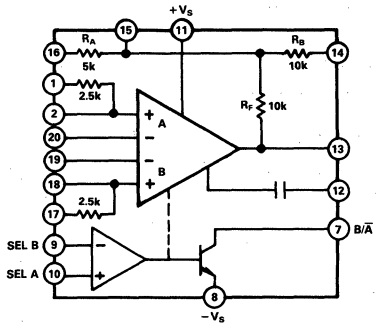


Figure 11. Architectural Block Diagram

HOW THE AD630 WORKS

The basic mode of operation of the AD630 may be more easy to recognize as two fixed gain stages which may be inserted into the signal path under the control of a sensitive voltage comparator. When the circuit is switched between inverting and noninverting gain, it provides the basic modulation/demodulation function. The AD630 is unique in that it includes laser wafer trimmed thin film feedback resistors on the monolithic chip. The configuration shown below yields a gain of ±2 and can be easily changed to ±1 by shifting R_B from its ground connection to the output.

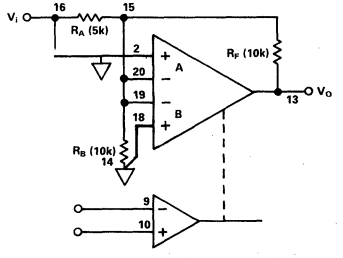


Figure 12. AD630 Symmetric Gain (±2)

The comparator selects one of the two input stages to complete an operational feedback connection around the AD630. The de-selected input is off and has negligible effect on the operation.

When channel B is selected, the resistors R_A and R_F are connected for inverting feedback as shown in the inverting gain configuration diagram in Figure 13. The amplifier has sufficient loop gain to minimize the loading effect of R_B at the virtual ground produced by the feedback connection. When the sign of the comparator input is reversed, input B will be de-selected and A will be

selected. The new equivalent circuit will be the noninverting gain configuration shown below. In this case R_A will appear across the op-amp input terminals, but since the amplifier drives this difference voltage to zero the closed loop gain is unaffected.

The two closed loop gain magnitudes will be equal when $R_F/R_A = 1 + R_F/R_B$, which will result from making R_A equal to $R_F R_B/(R_F + R_B)$ the parallel equivalent resistance of R_F and R_B.

The 5k and the two 10k resistors on the AD630 chip can be used to make a gain of two as shown here. By paralleling the 10k resistors to make R_F equal 5k and omitting R_B the circuit can be programmed for a gain of ± 1 (as shown in Figure 19a). These and other configurations using the on chip resistors present the inverting inputs with a 2.5k source impedance. The more complete AD630 diagrams show 2.5k resistors available at the noninverting inputs which can be conveniently used to minimize errors resulting from input bias currents.

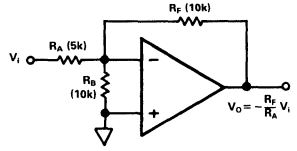


Figure 13. Inverting Gain Configuration

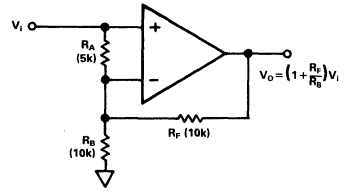


Figure 14. Noninverting Gain Configuration

CIRCUIT DESCRIPTION

The simplified schematic of the AD630 is shown in Figure 15. It has been subdivided into three major sections, the comparator, the two input stages and the output integrator. The comparator consists of a front end made up of Q52 and Q53, a flip-flop load formed by Q3 and Q4, and two current steering switching cells Q28, Q29 and Q30, Q31. This structure is designed so that a differential input voltage greater than 1.5mV in magnitude

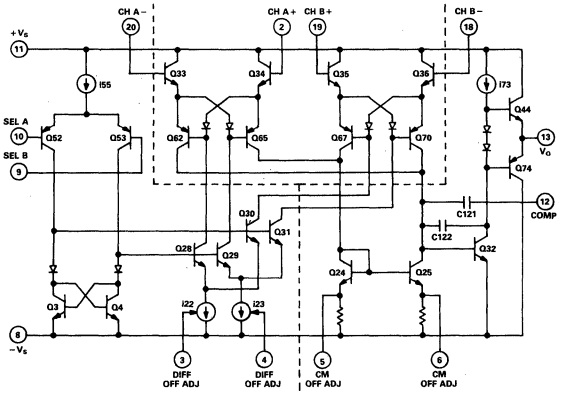


Figure 15. AD630 Simplified Schematic

applied to the comparator inputs will completely select one of the switching cells. The sign of this input voltage determines which of the two switching cells is selected.

The collectors of each switching cell connect to an input transconductance stage. The selected cell conveys bias currents i_{22} and i_{23} to the input stage it controls causing it to become active. The deselected cell blocks the bias to its input stage which, as a consequence, remains off.

The structure of the transconductance stages is such that they present a high impedance at their input terminals and draw no bias current when deselected. The deselected input does not interfere with the operation of the selected input insuring maximum channel separation.

Another feature of the input structure is that it enhances the slew rate of the circuit. The current output of the active stage follows a quasi-hyperbolic-sine relationship to the differential input voltage. This means that the greater the input voltage, the harder this stage will drive the output integrator, and hence, the faster the output signal will move. This feature helps insure rapid, symmetric settling when switching between inverting and noninverting closed loop configurations.

The output section of the AD630 includes a current mirror-load (Q24 and Q25), an integrator-voltage gain stage (Q32), and a complementary output buffer (Q44 and Q74). The outputs of both transconductance stages are connected in parallel to the current mirror. Since the deselected input stage produces no output current and presents a high impedance at its outputs, there is no conflict. The current mirror translates the differential output current from the active input transconductance amplifier into single ended form for the output integrator. The complementary output driver then buffers the integrator output to produce a low impedance output.

OTHER GAIN CONFIGURATIONS

Many applications require switched gains other than the ± 1 and ± 2 which the self-contained applications resistors provide. The AD630 can be readily programmed with 3 external resistors over a wide range of positive and negative gain by selecting R_B and R_F to give the noninverting gain $1 + R_F/R_B$ and subsequently R_A to give the desired inverting gain. Note that when the inverting magnitude equals the noninverting magnitude, the value of R_A is found to be $R_B R_F/(R_B + R_F)$. That is, R_A should equal the parallel combination of R_B and R_F to match positive and negative gain.

The feedback synthesis of the AD630 may also include reactive impedance. The gain magnitudes will match at all frequencies if the A impedance is made to equal the parallel combination of the B and F impedances. Essentially the same considerations apply to the AD630 as to conventional op-amp feedback circuits. Virtually any function which can be realized with simple non-inverting "L network" feedback can be used with the AD630. A common arrangement is shown in Figure 16. The low frequency gain of this circuit is 10. The response will have a pole (-3dB) at a frequency $f \simeq 1/(2\pi 100k\Omega C)$ and a zero (3dB from the high frequency asymptote) at about 10 times this frequency. The 2k resistor in series with each capacitor mitigates the loading effect on circuitry driving this circuit, eliminates stability problems, and has a minor effect on the pole-zero locations.

As a result of the reactive feedback, the high frequency components of the switched input signal will be transmitted at unity gain

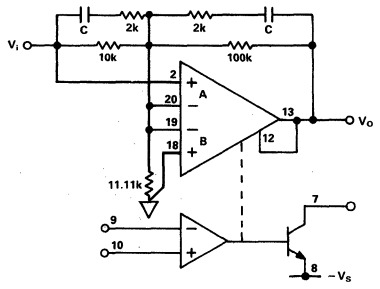


Figure 16. AD630 with External Feedback

while the low frequency components will be amplified. This arrangement is useful in demodulators and lock-in amplifiers. It increases the circuit dynamic range when the modulation or interference is substantially larger than the desired signal amplitude. The output signal will contain the desired signal multiplied by the low frequency gain (which may be several hundred for large feedback ratios) with the switching signal and interference superimposed at unity gain.

SWITCHED INPUT IMPEDANCE

The noninverting mode of operation is a high input impedance configuration while the inverting mode is a low input impedance configuration. This means that the input impedance of the circuit undergoes an abrupt change as the gain is switched under control of the comparator. If gain is switched when the input signal is not zero, as it is in many practical cases, a transient will be delivered to the circuitry driving the AD630. In most applications, this will require the AD630 circuit to be driven by a low impedance source which remains "stiff " at high frequencies. Generally this will be a wideband buffer amplifier.

FREQUENCY COMPENSATION

The AD630 combines the convenience of internal frequency compensation with the flexibility of external compensation by means of an optional self-contained compensation capacitor.

In gain of ± 2 applications the noise gain which must be addressed for stability purposes is actually 4. In this circumstance, the phase margin of the loop will be on the order of 60° without the optional compensation. This condition provides the maximum bandwidth and slew-rate for closed-loop gains of $|2|$ and above.

When the AD630 is used as a multiplexer, or in other configurations where one or both inputs are connected for unity gain feedback, the phase margin will be reduced to less than 20°. This may be acceptable in applications where fast slewing is a first priority, but the transient response will not be optimum. For these applications, the self-contained compensation capacitor may be added by connecting pin 12 to pin 13. This connection reduces the closed loop bandwidth somewhat, and improves the phase margin.

For intermediate conditions, such as gain of ± 1 where loop attenuation is 2, use of the compensation should be determined by whether bandwidth or settling response must be optimized. The optional compensation should also be used when the AD630 is driving capacitive loads or whenever conservative frequency compensation is desired.

OFFSET VOLTAGE NULLING

The offset voltages of both input stages and the comparator have been pre-trimmed so that external trimming will only be required in the most demanding applications. The offset adjustment of the two input channels is accomplished by means of a differential and common mode scheme. This facilitates fine adjustment of system errors in switched gain applications. With system input tied to 0V, and a switching or carrier waveform applied to the comparator, a low level square wave will appear at the output. The differential offset adjustment pot can be used to null the amplitude of this square wave (pins 3 and 4). The common mode offset adjustment can be used to zero the residual dc output voltage (pins 5 and 6). These functions should be implemented using 10k trim pots with wipers connected directly to pin 8 as shown in Figures 19a and 19b.

CHANNEL STATUS OUTPUT

The channel status output, pin 7, is an open collector output referenced to $-V_S$ which can be used to indicate which of the two input channels is active. The output will be active (pulled low) when channel A is selected. This output can also be used to supply positive feedback around the comparator. This produces hysteresis which serves to increase noise immunity. Figure 17 shows an example of how hysteresis may be implemented. Note that the feedback signal is applied to the inverting (−) terminal of the comparator to achieve positive feedback. This is because the open collector channel status output inverts the output sense of the internal comparator.

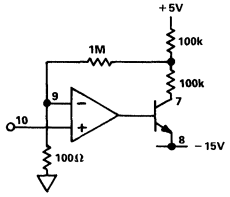


Figure 17. Comparator Hysteresis

The channel status output may be interfaced with TTL inputs as shown in Figure 18. This circuit provides appropriate level shifting from the open-collector AD630 channel status output to TTL inputs.

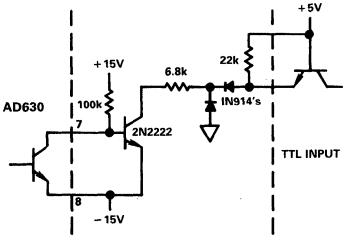


Figure 18. Channel Status – TTL Interface

APPLICATIONS:
BALANCED MODULATOR

Perhaps the most commonly used configuration of the AD630 is the balanced modulator. The application resistors provide precise symmetric gains of ± 1 and ± 2. The ± 1 arrangement is shown in Figure 19a and the ± 2 arrangement is shown in Figure 19b. These cases differ only in the connection of the 10k feedback resistor (pin 14) and the compensation capacitor (pin 12). Note the use of the 2.5kΩ bias current compensation resistors in these examples. These resistors perform the identical function in the ± 1 gain case. Figure 20 demonstrates the performance of the AD630 when used to modulate a 100kHz square wave carrier with a 10kHz sinusoid. The result is the double sideband suppressed carrier waveform.

These balanced modulator topologies accept two inputs, a signal (or modulation) input applied to the amplifying channels, and a reference (or carrier) input applied to the comparator.

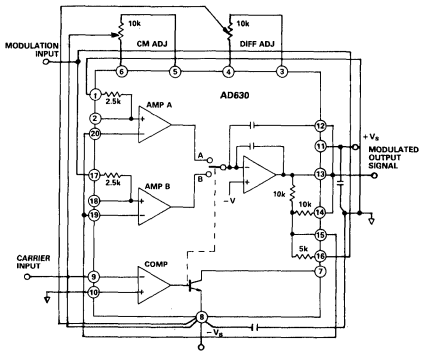


Figure 19a. AD630 Configured as a Gain-of-One Balanced Modulator

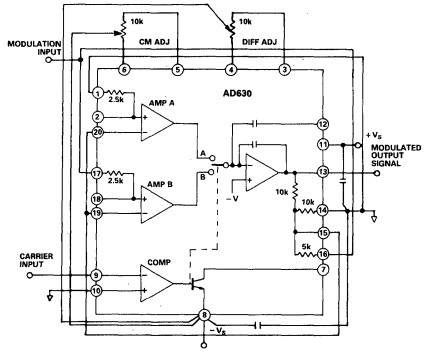


Figure 19b. AD630 Configured as a Gain-of-Two Balanced Modulator

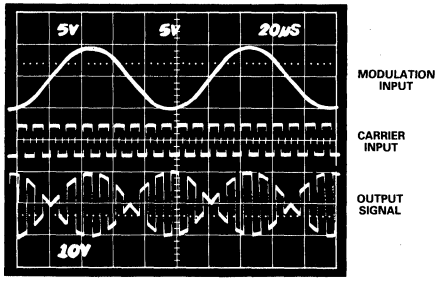


Figure 20. Gain-of-Two Balanced Modulator Sample Waveforms

BALANCED DEMODULATOR

The balanced modulator topology described above will also act as a balanced demodulator if a double sideband suppressed carrier waveform is applied to the signal input and the carrier signal is applied to the reference input. The output under these circumstances will be the baseband modulation signal. Higher order carrier components will also be present which can be removed with a low-pass filter. Other names for this function are synchronous demodulation and phase-sensitive detection.

PRECISION PHASE COMPARATOR

The balanced modulator topologies of Figures 19a and 19b can also be used as precision phase comparators. In this case, an ac waveform of a particular frequency is applied to the signal input and a waveform of the same frequency is applied to the reference input. The dc level of the output (obtained by low pass filtering) will be proportional to the signal amplitude and phase difference between the input signals. If the signal amplitude is held constant, then the output can be used as a direct indication of the phase. When these input signals are 90° out of phase, they are said to be in quadrature and the AD630 dc output will be zero.

PRECISION RECTIFIER-ABSOLUTE VALUE

If the input signal is used as its own reference in the balanced modulator topologies, the AD630 will act as a precision rectifier. The high frequency performance will be superior to that which can be achieved with diode feedback and op amps. There are no diode drops which the op amp must "leap over" with the commutating amplifier.

LVDT SIGNAL CONDITIONER

Many transducers function by modulating an ac carrier. A Linear Variable Differential Transformer (LVDT) is a transducer of this type. The amplitude of the output signal corresponds to core displacement. Figure 21 shows an accurate synchronous demodulation system which can be used to produce a dc voltage which corresponds to the LVDT core position. The inherent precision and temperature stability of the AD630 reduce demodulator drift to a second order effect.

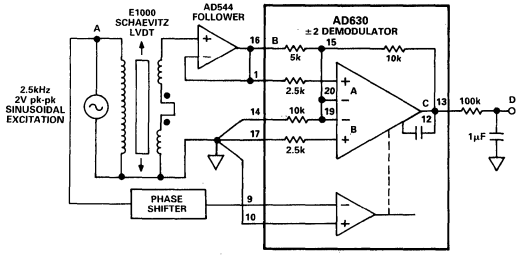


Figure 21. LVDT Signal Conditioner

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 22 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper-middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 3.2mV change in the low pass filtered dc output, well above the RTO drifts and noise.

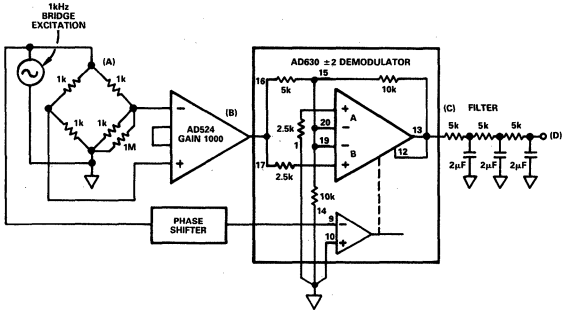


Figure 22. AC Bridge System

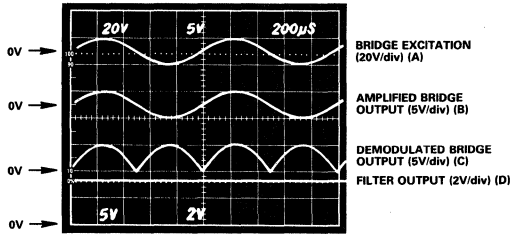


Figure 23. AC Bridge Waveforms

LOCK-IN AMPLIFIER APPLICATIONS

Lock-in amplification is a technique which is used to separate a small, narrow band signal from interfering noise. The lock-in amplifier acts as a detector and narrow band filter combined. Very small signals can be detected in the presence of large amounts of uncorrelated noise when the frequency and phase of the desired signal are known.

The lock-in amplifier is basically a synchronous demodulator followed by a low pass filter. An important measure of performance in a lock-in amplifier is the dynamic range of its demodulator. The schematic diagram of a demonstration circuit which exhibits the dynamic range of an AD630 as it might be used in a lock-in amplifier is shown in Figure 24. Figure 25 is an oscilloscope photo showing the recovery of a signal modulated at 400Hz from a noise signal approximately 100,000 times larger; a dynamic range of 100dB.

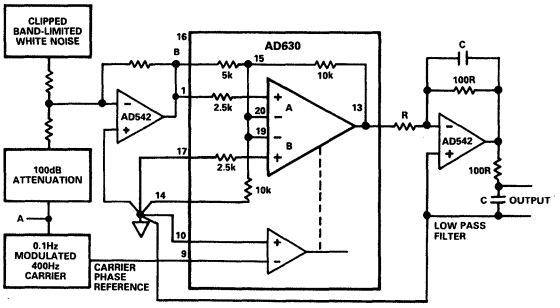


Figure 24. Lock-In Amplifier

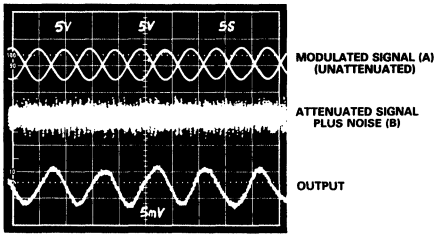


Figure 25. Lock-In Amplifier Waveforms

The test signal is produced by modulating a 400Hz carrier with a 0.1Hz sine wave. The signals produced, for example, by chopped radiation (IR, optical, etc.) detectors may have similar low frequency components. A sinusoidal modulation is used for clarity of illustration. This signal is produced by a circuit similar to Figure 19b and is shown in the upper trace of Figure 25. It is attenuated 100,000 times normalized to the output, B, of the summing amplifier. A noise signal which might represent, for example, background and detector noise in the chopped radiation case, is added to the modulated signal by the summing amplifier. This signal is simply band limited clipped white noise. Figure 25 shows the sum of attenuated signal plus noise in the center trace. This combined signal is demodulated synchronously using phase information derived from the modulator, and the result is low pass filtered using a 2-pole simple filter which also provides a gain of 100 to the output. This recovered signal is the lower trace of Figure 25.

The combined modulated signal and interfering noise used for this illustration is similar to the signals often requiring a lock-in amplifier for detection. The precision input performance of the AD630 provides more than 100dB of signal range and its dynamic response permits it to be used with carrier frequencies more than two orders of magnitude higher than in this example. A more sophisticated low pass output filter will aid in rejecting wider bandwidth interference.

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

AD632

FEATURES

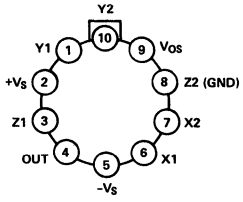
Pretrimmed to ±0.5% Max 4-Quadrant Error
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X10 Gain
Low Noise Design: 90μV rms, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Accurate Voltage Controlled Oscillators and Filters

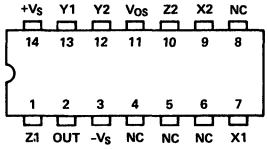
AD632 PIN CONFIGURATIONS

H-Package TO-100



TOP VIEW

D-Package TO-116



TOP VIEW

6

PRODUCT DESCRIPTION

The AD632 is an internally-trimmed monolithic four-quadrant multiplier/divider. The AD632B has a maximum multiplying error of ±0.5% without external trims.

Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions. The simplicity and flexibility of use provide an attractive alternative approach to the solution of complex control functions.

The AD632 is pin for pin compatible with the industry standard AD532 with improved specifications and a fully differential high impedance Z-input. The AD632 is capable of providing gains of up to X10, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD632 can be effectively employed as a variable gain differential input amplifier with high common mode rejection. The effectiveness of the variable gain capability is enhanced by the inherent low noise of the AD632: 90μV rms.

PRODUCT HIGHLIGHTS

Guaranteed Performance Over Temperature: The AD632A and AD632B are specified for maximum multiplying errors of ±1.0% and ±0.5% of full scale, respectively at +25°C and are rated for operation from -25°C to +85°C. Maximum multiplying errors of ±2.0% (AD632S) and ±1.0% (AD632T) are guaranteed over the extended temperature range of -55°C to +125°C.

High Reliability: The AD632S and AD632T series are also available with MIL-STD-883 Level B screening and all devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP package.

SPECIFICATIONS (@ +25°C, $V_S = \pm 15V$, R≥2kΩ unless otherwise noted)

Model	AD632A Min	AD632A Typ	AD632A Max	AD632B Min	AD632B Typ	AD632B Max	AD632S Min	AD632S Typ	AD632S Max	AD632T Min	AD632T Typ	AD632T Max	Units
MULTIPLIER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] (−10V≤X, Y≤+10V)			**±1.0**			**±0.5**			**±1.0**			**±0.5**	%
T_A = min to max		**±1.5**			**±1.0**			**±2.0**			**±1.0**		%
Total Error vs Temperature		±0.022			±0.015				**±0.02**			**±0.01**	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.25			±0.1		%
Temperature-Coefficient of Scaling-Voltage		±0.02			**±0.01**			±0.2				**±0.005**	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	±0.3		±0.4			±0.2	±0.3	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	±0.1		±0.2			±0.1	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	±0.3		±0.3			±0.15	±0.3	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	±0.1		±0.01			±0.01	±0.1	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift		200			100				**500**			**300**	µV/°C
DYNAMICS													
Small Signal BW, (V_{OUT} = 0.1rms)		1			1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2			2		µs
NOISE													
Noise Spectral-Density SF = 10V		0.8			0.8			0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4			0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise A 10Hz to 5MHz		1.0			1.0			1.0			1.0		mV rms
P 10Hz to 10kHz		90			90			90			90		µV/rms
OUTPUT													
Output Voltage Swing	**±11**			**±11**			**±11**			**±11**			V
Output Impedance (f≤1kHz)		0.1			0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L 0, T_A = min to max)		30			30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]													
Signal Voltage Range (Diff. or CM		±10			±10			±10			±10		V
Operating Diff.)		±12			±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z		200			100				500			300	µV/°C
CMRR	**60**	80		**70**	90		**60**	80		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1			0.1			0.1		µA
Differential Resistance		10			10			10			10		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1]													
(X = 10V, −10V≤Z≤+10V)		±0.75			±0.35			±0.75			±0.35		%
(X = 1V, −1V≤Z≤+1V)		±2.0			±1.0			±2.0			±1.0		%
(0.1V≤X≤10V, −10V≤Z≤10V)		±2.5			±1.0			±2.5			±1.0		%
SQUARER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error (−10V≤X≤10V)		±0.6			±0.3			±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function, ($Z_1 \le Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] (1V≤Z≤10V)		±1.0			±0.5			±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS													
Supply Voltage													
Rated Performance		±15			±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±22**	±8		**±22**	V
Supply Current													
Quiescent		4	**6**		4	6		4	**6**		4	6	mA
PACKAGE OPTIONS[6]													
TO-100 (H-10A)		AD632AH			AD632BH			AD632SH			AD632TH		
TO-116 (D-14)		AD632AD			AD632BD			AD632SD			AD632TD		

NOTES
[1]Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.
[6]See Section 20 for package outline information.

Specifications subject to change without notice.

All min and max specifications are guaranteed.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Typical Performance Curves (typical at +25°C with $\pm V_S = 15V$)

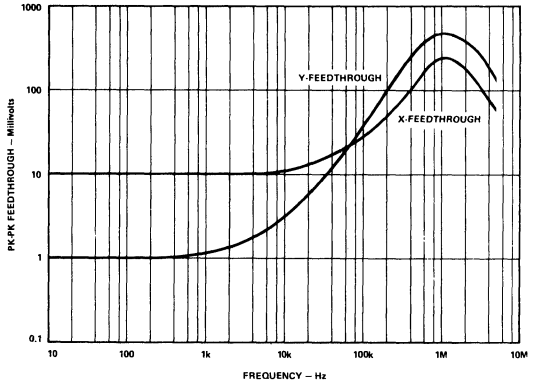


Figure 1. AC Feedthrough vs. Frequency

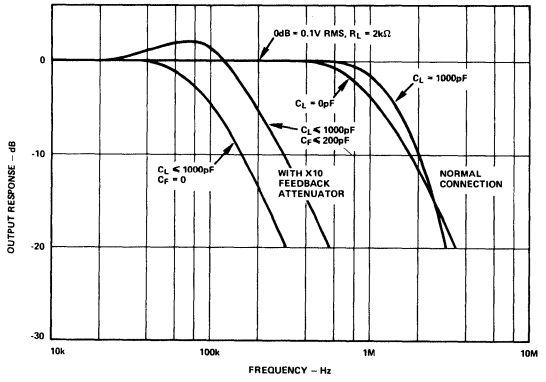


Figure 2. Frequency Response as a Multiplier

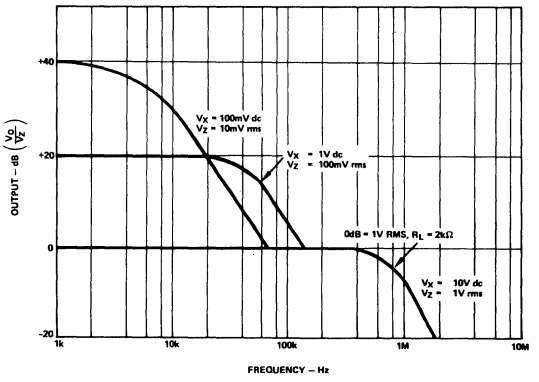
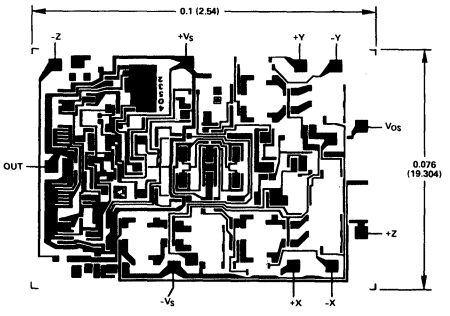


Figure 3. Frequency Response vs. Divider Denominator Input Voltage

6

CHIP DIMENSIONS & PAD LAYOUT

Contact factory for latest dimensions
Dimensions shown in inches and (mm).



For further information, consult factory

ORDERING GUIDE

Temperature Range	Header (H)	Side Brazed DIP (D)
−25°C to +85°C	AD632AH AD632BH	AD632AD AD632BD
−55°C to +125°C	AD632SH AD632SH/883B AD632TH AD632TH/883B	AD632SD AD632SD/883B AD632TD AD632TD/883B

Thermal Characteristics

Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14
θ_{JA} = 95°C/W for D-14

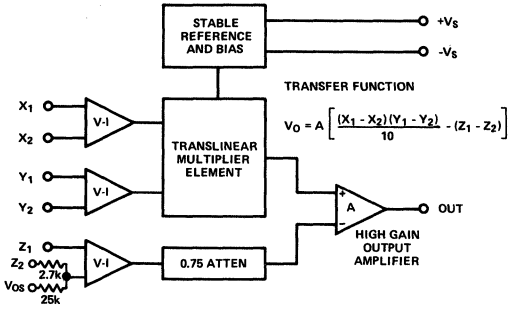


Figure 4. AD632 Functional Block Diagram

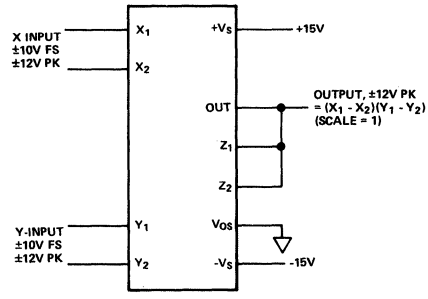


Figure 6. Connections for Scale-Factor of Unity

OPERATION AS A MULTIPLIER

Figure 5 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

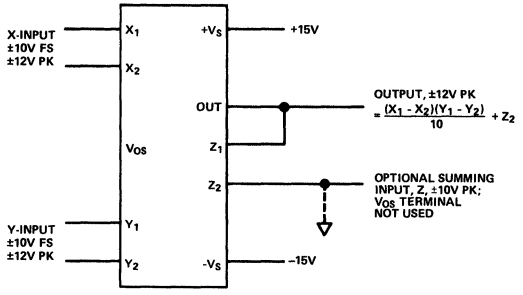


Figure 5. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input. Curve 1 shows the typical ac feedthrough with this adjustment mode. Note that the feedthrough of the Y input is a factor of 10 lower than that of the X input and should be used in applications where null suppression is critical.

The Z_2 terminal of the AD632 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective signal common potentials to realize the full accuracy of the AD632.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 6. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the Z_1 terminal where they are amplified by -10 or to the common ground connection where they are amplified by -1. Input signals may also be applied to the lower end of the 2.7kΩ resistor, giving a gain of +9.

OPERATION AS A DIVIDER

Figure 7 shows the connection required for division. Unlike earlier products, the AD632 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in Figure 3.

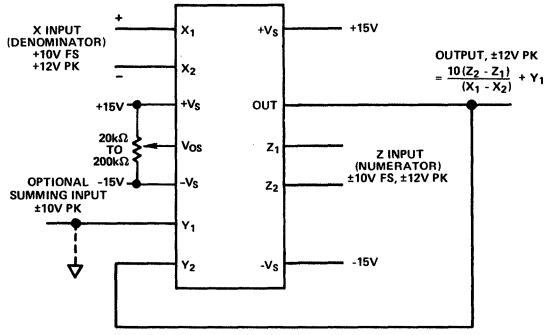


Figure 7. Basic Divider Connection

Without additional trimming, the accuracy of the AD632B is sufficient to maintain a 1% error over a 10V to 1V denominator range (The AD535 is functionally equivalent to the AD632 and has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications).

This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input. To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

*See the AD535 Data Sheet for more details.

ANALOG DEVICES

Low Cost Analog Multiplier

AD633

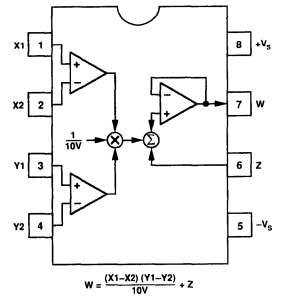
FEATURES

Four-Quadrant Multiplication in a Low Cost 8-Pin Package
Complete – No External Components Required
Laser Trimmed Accuracy and Stability
Typical Total Error Within 1% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity Gain Summing Input
Laser Trimmed 10 V Scaling Reference

APPLICATIONS

Multiplication, Modulation/Demodulation, Squaring, Phase Detection, Programmable Resistances and Conductances, Voltage Controlled Amplifiers/ Attenuators/Filters

AD633 FUNCTIONAL BLOCK DIAGRAM
Plastic DIP (N) Package



6

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. The AD633 includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale. A laser trimmed 10 V scaling reference is included on the chip. The AD633 is the first product to offer these features in modestly priced 8-pin plastic DIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale for the AD633JN. Nonlinearity for the Y input is typically less than 0.1%, and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of closed-loop applications.

The AD633 is available in an 8-pin plastic mini-DIP package (N) and 8-pin SOIC (R) and is specified to operate over the 0 to +70°C commercial temperature range.

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four quadrant multiplier offered in low cost 8-pin plastic packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, $R_L \geq 2$ kΩ)

Model	Conditions	AD633J Min	Typ	Max	Unit
TRANSFER FUNCTION			$W = \frac{(X1-X2)(Y1-Y2)}{10\ V} + Z$		
MULTIPLIER					
Total Error	−10 V ≤ X, Y ≤ +10 V			**+2.0**	% Full Scale
T_{min} to T_{max}			+3.0		% Full Scale
Scale Factor Error	SF = 10.00 V Nominal		+1.0		% Full Scale
Supply Rejection	V_S = ±15 V ±1 V		+0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	**±1.0**	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	**±0.4**	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	**±1.0**	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	**±0.4**	% Full Scale
Output Offset Voltage			±5.0	**±50.0**	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms, Error = 1%, C_L = 1000 pF		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/μs
Settling Time to 1%	Δ V_O = 20 V		2		μs
NOISE					
Spectral Density			0.8		μV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		mV rms
OUTPUT					
Output Voltage Swing		**±11**			V
Short Circuit Current	R_L = 0 Ω, T_A = min to max		30	**40**	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	**±10**			V
	Common Mode	**±10**			V
Offset Voltage X, Y			±5	**±30**	mV
Offset Voltage Z			±5	**±50**	mV
CMRR	V_{CM} = ±10 V	**60**	80		dB
Bias Current X, Y, Z			0.8	**2.0**	μA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		**±8**		**±18**	V
Supply Current	Quiescent		4	**6**	mA

NOTES
Specifications shown in **boldface** are tested on all productions units at electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltages[3] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W.
8-Pin Small Outline Package: θ_{JA} = 155°C/W.
[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

FUNCTIONAL DESCRIPTION

The AD633 is a low cost integrated circuit multiplier comprising a translinear multiplying core, a buried Zener reference, and a unity gain connected output amplifier with an accessible summing node. The functional block diagram of the AD633 is shown on the first page of this data sheet. The differential X and Y inputs are converted to differential currents by two identical voltage-to-current converters. The product of these currents is generated by the multiplying core. A stable buried Zener reference provides an overall scale factor of 10 V. The sum of $(X \cdot Y)/10 + Z$ is then applied to the unity gain connected output amplifier. Access to the amplifier summing node through Z allows the user to sum two or more multiplier outputs, decrease the effective scale factor, convert the output voltage to a current, and configure various analog computational functions.

Inspection of the block diagram shows the overall transfer function to be:

$$W = A\left[\frac{(X1-X2)\,(Y1-Y2)}{10\ V} + Z - W\right]$$

where A is the open loop gain of the output amplifier and W is the output. In most cases, the open loop gain can be regarded as infinite, simplifying the transfer expression to:

$$W = \frac{(X1-X2)\,(Y1-Y2)}{10\ V} + Z$$

The output amplifier has a 1 MHz small signal bandwidth and a 20 V/μs slew rate. In addition to straight multiplication, a variety of useful closed-loop configurations can be implemented as shown in the Applications section.

ERROR SOURCES – Multiplier errors consist primarily of input offsets, scale factor error, and nonlinearity in the multiplying core. The input offsets can be eliminated by using the optional trim configuration of Figure 1. This scheme reduces the net error to scale factor errors (gain error) and an irreducible nonlinearity component in the multiplying core. The X and Y nonlinearities are typically 0.1% of full scale, respectively. Scale factor error is typically 1% of full scale. The high impedance Z input should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise, the differential X and Y inputs should be referenced to their respective grounds to realize the full accuracy of the AD633.

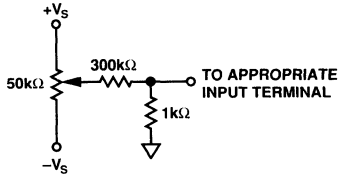


Figure 1. Optional Offset Trim Configuration

APPLICATIONS SECTION

The versatility, simplicity, and low cost of the AD633 make it especially well suited for a large number of applications. These include modulation and demodulation, automatic gain control, power measurement, voltage controlled amplifiers, and frequency doublers. Connection diagrams for several of these popular applications follow.

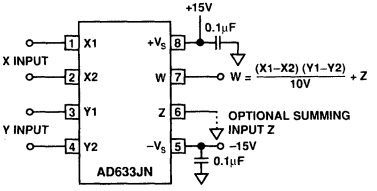


Figure 2. Basic Multiplier Connection

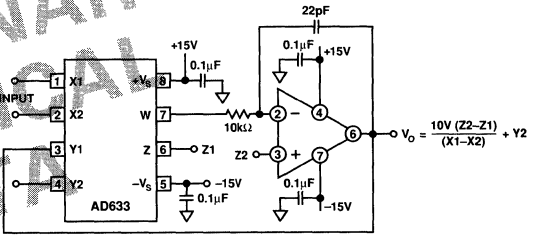


Figure 3. Basic Divider Connection

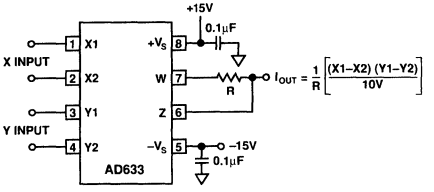
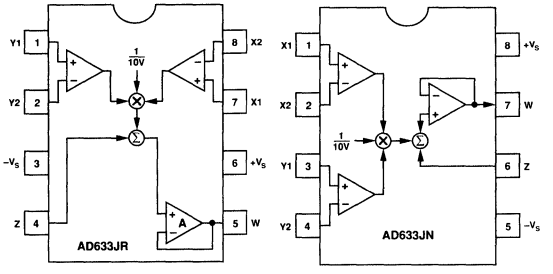


Figure 4. Current Output Connections

CONNECTION DIAGRAMS

(Top View)

AD633JR – 8 Pin Plastic SOIC **AD633JN – 8 Pin Plastic DIP**



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

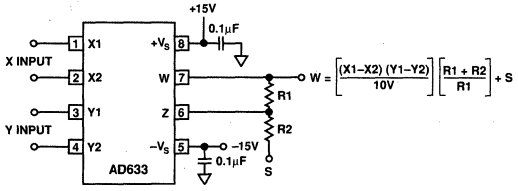


Figure 5. Connections for Variable Scale Factor

ORDERING GUIDE*

Temperature Range	Plastic Mini-DIP (N-8)	SOIC (R-8)
Commerical 0 to +70°C	AD633JN	AD633JR

*See Section 20 for package outline information.

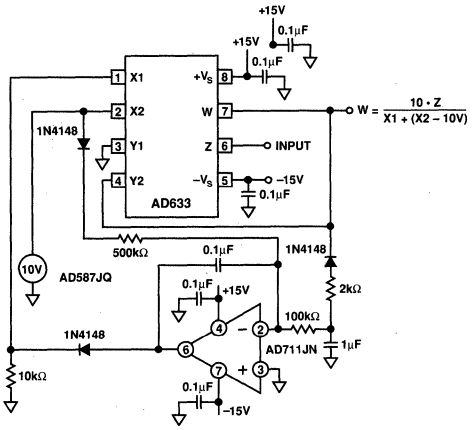


Figure 6. Connections for Use in Automatic Gain Control Circuit

ANALOG DEVICES

10 MHz, 4-Quadrant Multiplier/Divider

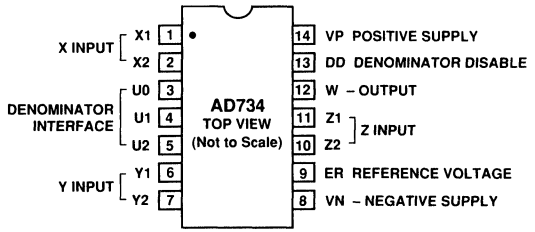
AD734

FEATURES
High Accuracy
0.1% Typical Error
High Speed
10 MHz Full-Power Bandwidth
450 V/μs Slew Rate
200 ns Settling to 0.1% at Full Power
Low Distortion
−80 dBc from Any Input
Third-Order IMD Typically −75 dBc at 10 MHz
Low Noise
94 dB SNR, 10 Hz to 20 kHz
70 dB SNR, 10 Hz to 10 MHz
Direct Division Mode
2 MHz BW at Gain of 100

APPLICATIONS
High Performance Replacement for AD534
Multiply, Divide, Square, Square Root
Modulator, Demodulator
Wideband Gain Control, RMS-DC Conversion
Voltage-Controlled Amplifiers, Oscillators, and Filters
Demodulator with 40 MHz Input Bandwidth

AD734 CONNECTION DIAGRAM

14-Pin DIP
(Q Package)



6

PRODUCT DESCRIPTION

The AD734 is an accurate high speed, four-quadrant analog multiplier that is pin-compatible with the industry-standard AD534 and provides the transfer function $W = XY/U$. The AD734 provides a low-impedance voltage output with a full-power (20 V pk–pk) bandwidth of 10 MHz. Total static error (scaling, offsets, and nonlinearities combined) is 0.1% of Full Scale. Distortion is typically less than −80 dBc and guaranteed. The low-capacitance X, Y and Z inputs are fully differential. In most applications, no external components are required to define the function.

The internal scaling (denominator) voltage U is 10 V, derived from a buried-Zener voltage reference. A new feature provides the option of substituting an external denominator voltage, allowing the use of the AD734 as a two-quadrant divider with a 1000:1 denominator range and a signal bandwidth that remains 10 MHz to a gain of 20 dB, 2 MHz at a gain of 40 dB and 200 kHz at a gain of 60 dB, for a gain-bandwidth product of 200 MHz.

The advanced performance of the AD734 is achieved by a combination of new circuit techniques, the use of a high speed complementary bipolar process and a novel approach to laser-trimming based on ac signals rather than the customary dc methods. The wide bandwidth (>40 MHz) of the AD734's input stages and the 200 MHz gain-bandwidth product of the multiplier core allow the AD734 to be used as a low distortion demodulator with input frequencies as high as 40 MHz as long as the desired output frequency is less than 10 MHz.

The AD734AQ and AD734BQ are specified for the industrial temperature range of −40°C to +85°C and come in a 14-pin ceramic DIP. The AD734SQ/883B, available processed to MIL-STD-883B for the military range of −55°C to +125°C, is available in a 14-pin ceramic DIP.

PRODUCT HIGHLIGHTS

The AD734 embodies more than two decades of experience in the design and manufacture of analog multipliers, to provide

1. A new output amplifier design with more than twenty times the slew-rate of the AD534 (450 V/μs versus 20 V/μs) for a full power (20 V pk–pk) bandwidth of 10 MHz.
2. Very low distortion, even at full power, through the use of circuit and trimming techniques that virtually eliminate all of the spurious nonlinearities found in earlier designs.
3. Direct control of the denominator, resulting in higher multiplier accuracy and a gain-bandwidth product at small denominator values that is typically 200 times greater than that of the AD534 in divider modes.
4. Very clean transient response, achieved through the use of a novel input stage design and wide-band output amplifier, which also ensure that distortion remains low even at high frequencies.
5. Superior noise performance by careful choice of device geometries and operating conditions, which provide a guaranteed 88 dB of dynamic range in a 20 kHz bandwidth.

SPECIFICATIONS (T_A = +25°C, $+V_S$ = VP = +15 V, $-V_S$ = VN = −15 V, $R_L \geq 2\ k\Omega$)

TRANSFER FUNCTION

$$W = A_O\left\{\frac{(X_1-X_2)(Y_1-Y_2)}{(U_1-U_2)} - (Z_1 - Z_2)\right\}$$

Parameter	Conditions	A Min	A Typ	A Max	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
MULTIPLIER PERFORMANCE											
Transfer Function			W = XY/10			W = XY/10			W = XY/10		
Total Static Error[1]	−10 V ≤ X,Y ≤ 10 V		0.1	**0.4**		0.1	**0.25**		0.1	**0.4**	%
Over T_{min} to T_{max}				**1**			**0.6**			**1.25**	%
vs. Temperature	T_{min} to T_{max}		0.004			0.003			0.004		%/°C
vs. Either Supply	$\pm V_S$ = 14 V to 16 V		0.01	**0.05**		0.01	**0.05**		0.01	**0.05**	%/V
Peak Nonlinearity	−10 V ≤ X ≤ +10 V, Y = +10 V		0.05			0.05			0.05		%
	−10 V ≤ Y ≤ +10 V, X = +10 V		0.025			0.025			0.025		%
THD[2]	X = 7 V rms, Y = +10 V, f ≤ 5 kHz			**−58**			**−66**			**−58**	dBc
	T_{min} to T_{max}			**−55**			**−63**			**−55**	dBc
	Y = 7 V rms, X = +10 V, f ≤ 5 kHz			**−60**			**−80**			**−60**	dBc
	T_{min} to T_{max}			**−57**			**−74**			**−57**	dBc
Feedthrough	X = 7 V rms, Y = nulled, f ≤ 5 kHz		−85	**−60**		−85	**−70**		−85	**−60**	dBc
	Y = 7 V rms, X = nulled, f ≤ 5 kHz		−85	**−66**		−85	**−76**		−85	**−66**	dBc
Noise (RTO)	X = Y = 0										
Spectral Density	100 Hz to 1 MHz		1.0			1.0			1.0		$\mu V/\sqrt{Hz}$
Total Output Noise	10 Hz to 20 kHz		−94	**−88**		−94	**−88**		−94	**−88**	dBc
	T_{min} to T_{max}			**−85**			**−85**			**−85**	dBc
DIVIDER PERFORMANCE (Y = 10 V)											
Transfer Function			W = XY/U			W = XY/U			W = XY/U		
Gain Error	Y = 10 V, U = 100 mV to 10 V		1			1			1		%
X Input Clipping Level	Y = 10 V		1.25 × U			1.25 × U			1.25 × U		V
U Input Scaling Error[3]				**0.3**			**0.15**			**0.3**	%
	T_{min} to T_{max}			**0.8**			**0.65**			**1**	%
(Output to 1%)	U = 1 V to 10 V Step, X = 1 V		100			100			100		ns
INPUT INTERFACES (X, Y, & Z)											
3 dB Bandwidth			40			40			40		MHz
Operating Range	Differential or Common Mode		±12.5			±12.5			±12.5		V
X Input Offset Voltage				**15**			**5**			**15**	mV
	T_{min} to T_{max}			**25**			**15**			**25**	mV
Y Input Offset Voltage				**10**			**5**			**10**	mV
	T_{min} to T_{max}			**12**			**6**			**12**	mV
Z Input Offset Voltage				**20**			**10**			**20**	mV
	T_{min} to T_{max}			**50**			**50**			**90**	mV
Z Input PSRR (Either Supply)	f ≤ 1 kHz	**54**	70		**66**	70		**54**	70		dB
	T_{min} to T_{max}	**50**			**56**			**50**			dB
CMRR	f = 5 kHz	**70**	85		**70**	85		**70**	85		dB
Input Bias Current (X, Y, Z Inputs)			50	**200**		50	**150**		50	**300**	nA
	T_{min} to T_{max}			**300**			**300**			**500**	nA
Input Resistance	Differential		50			50			50		kΩ
Input Capacitance	Differential		2			2			2		pF
DENOMINATOR INTERFACES (U0, U1, & U2)											
Operating Range			VN to VP-3			VN to VP-3			VN to VP-3		V
Denominator Range			1000:1			1000:1			1000:1		
Interface Resistor	U1 to U2		28			28			28		kΩ
OUTPUT AMPLIFIER (W)											
Output Voltage Swing	T_{min} to T_{max}	±12			±12			±12			V
Open-Loop Voltage Gain	X = Y = 0, Input to Z		72			72			72		dB
Dynamic Response	From X or Y Input, CL ≤ 20 pF										
3 dB Bandwidth	W ≤ 7 V rms	8	10		8	10		8	10		MHz
Slew Rate			450			450			450		V/μs
Settling Time	+20 V or −20 V Output Step										
To 1%			125			125			125		ns
To 0.1%			200			200			200		ns
Short-Circuit Current	T_{min} to T_{min}	**20**	50	80	**20**	50	80	**20**	50	80	mA
POWER SUPPLIES, $\pm V_S$											
Operating Supply Range		±8		±16.5	±8		±16.5	±8		±16.5	V
Quiescent Current	T_{min} to T_{max}	6	9	**12**	6	9	**12**	6	9	**12**	mA

NOTES

[1]Figures given are percent of full scale (e.g., 0.01% = 1 mV).

[2]dBc refers to deciBels relative to the full scale input (carrier) level of 7 V rms.

[3]See Figure 10 for test circuit.

All min and max specifications are guaranteed. Specifications in **Boldface** are tested on all production units at final electrical test. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
for T_J max = 175°C . . . . . 500 mW
X, Y and Z Input Voltages . . . . . VN to VP
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
Q . . . . . −65°C to +150°C
Operating Temperature Range
AD734A, B . . . . . −40°C to +85°C
AD734S . . . . . −55°C to +125°C
Lead Temperature Range (soldering 60 sec) . . . . . +300°C
Transistor Count 81

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
[2]14-Pin Ceramic DIP: θ_{JA} = 110°C/W

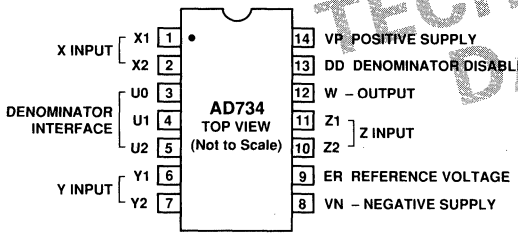
ORDERING GUIDE*

Temperature Range	14-Pin Ceramic DIP (Q-14)
Industrial −40°C to +85°C	AD734AQ AD734BQ
Military −55°C to +125°C	AD734SQ/883B

*See Section 20 for package outline information.

CONNECTION DIAGRAM

14-Pin DIP
(Q Package)



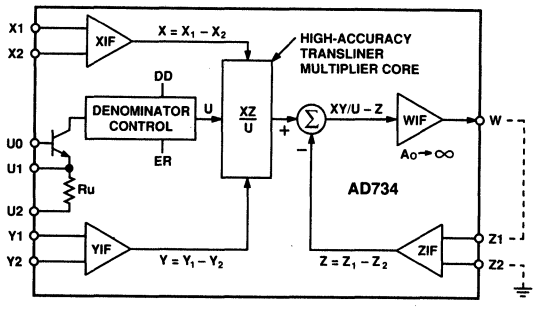


Figure 1. AD734 Block Diagram

FUNCTIONAL DESCRIPTION

Figure 1 is a simplified block diagram of the AD734. Operation is similar to that of the industry-standard AD534 and in many applications these parts are pin-compatible. The main functional difference is the provision for direct control of the denominator voltage, U, explained fully on the following page. Internal signals are actually in the form of currents, but the function of the AD734 can be understood using voltages throughout, as shown in this figure. Pins are named using upper-case characters (such as X1, Z2) while the *voltages* on these pins are denoted by subscripted variables (for example, X_1, Z_2).

The AD734's differential X, Y and Z inputs are handled by wideband interfaces that have low offset, low bias current and low distortion. The AD734 responds to the difference signals $X = X_1 - X_2$, $Y = Y_1 - Y_2$ and $Z = Z_1 - Z_2$, and rejects common-mode voltages on these inputs. The X, Y and Z interfaces provide a nominal full-scale (FS) voltage of ±10 V, but, due to the special design of the input stages, the linear range of the differential input can be as large as ±17 V. Also unlike previous designs, the response on these inputs is not clipped abruptly above ±15 V, but drops to a slope of one half.

The bipolar input signals X and Y are multiplied in a translinear core of novel design to generate the product XY/U. The denominator voltage, U, is internally set to an accurate, temperature-stable value of 10 V, derived from a buried-Zener reference. An uncalibrated fraction of the denominator voltage U appears between the voltage reference pin (ER) and the negative supply pin (VN), for use in certain applications where a temperature-compensated voltage reference is desirable. The internal denominator, U, can be disabled, by connecting the denominator disable Pin 13 (DD) to the positive supply pin (VP); the denominator can then be replaced by a fixed or variable external voltage ranging from 10 mV to more than 10 V.

The high-gain output op-amp nulls the difference between XY/U and an additional signal Z, to generate the final output W. The actual transfer function can take on several forms, depending on the connections used. The AD734 can perform all of the functions supported by the AD534, and new functions using the direct-division mode provided by the U-interface.

Each input pair (X1 and X2, Y1 and Y2, Z1 and Z2) has a differential input resistance of 50 kΩ; this is formed by "real" resistors (not a small-signal approximation) and is subject to a tolerance of ±20%. The common-mode input resistance is several megohms and the parasitic capacitance is about 2 pF.

The bias currents associated with these inputs are nulled by laser-trimming, such that when one input of a pair is optionally ac-coupled and the other is grounded, the residual offset voltage is typically less than 5 mV, which corresponds to a bias current of only 100 nA. This low bias current ensures that mismatches in the sources resistances at a pair of inputs does not cause an offset error. These currents remain low over the full temperature range and supply voltages.

The common-mode range of the X, Y and Z inputs does not fully extend to the supply rails. Nevertheless, it is often possible to operate the AD734 with one terminal of an input pair connected to either the positive or negative supply, unlike previous multipliers. The common-mode resistance is several megohms.

The full-scale output of ±10 V can be delivered to a load resistance of 1 kΩ (although the specifications apply to the standard multiplier load condition of 2 kΩ). The output amplifier is stable driving capacitive loads of at least 100 pF, when a slight increase in bandwidth results from the peaking caused by this capacitance. The 450 V/μs slew rate of the AD734's output amplifier ensures that the bandwidth of 10 MHz can be maintained up to the full output of 20 V pk-pk. Operation at reduced supply voltages is possible, down to ±8 V, with reduced signal levels.

Available Transfer Functions

The uncommitted (open-loop) transfer function of the AD734 is

$$W = A_O \left\{ \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} - (Z_1 - Z_2) \right\}, \quad (1)$$

where A_O is the open-loop gain of the output op-amp, typically 72 dB. When a negative feedback path is provided, the circuit will force the quantity inside the brackets essentially to zero, resulting in the equation

$$(X_1 - X_2)(Y_1 - Y_2) = U\,(Z_1 - Z_2). \quad (2)$$

This is the most useful generalized transfer function for the AD734; it expresses a balance between the product XY and the product UZ. The absence of the output, W, in this equation only reflects the fact that we have not yet specified which of the inputs is to be connected to the op-amp output.

Most of the functions of the AD734 (including division, unlike the AD534 in this respect) are realized with Z_1 connected to W. So, substituting W in place of Z_1 in the above equation results in an output.

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} + Z_2. \quad (3)$$

The free input Z2 can be used to sum another signal to the output; in the absence of a product signal, W simply follows the voltage at Z2 with the full 10 MHz bandwidth. When not needed for summation, Z2 should be connected to the ground associated with the load circuit. We can show the allowable polarities in the following shorthand form:

$$(\pm W) = \frac{(\pm X)(\pm Y)}{(+U)} + \pm Z. \quad (4)$$

In the recommended direct divider mode, the Y input is set to a fixed voltage (typically 10 V) and U is varied directly; it may have any value from 10 mV to 10 V. The magnitude of the ratio X/U cannot exceed 1.25; for example, the peak X-input for U = 1 V is ±1.25 V. Above this level, clipping occurs at the positive and negative extremities of the X-input. Alternatively, the AD734 can be operated using the standard (AD534) divider con-

nections (Figure 8), when the negative feedback path is established via the Y_2 input. Substituting W for Y_2 in Equation (2), we get

$$W = U\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1. \quad (5)$$

In this case, note that the variable X is now the denominator, and the above restriction ($X/U \leq 1.25$) on the magnitude of the X input does not apply. However, X must be positive in order for the feedback polarity to be correct. Y_1 can be used for summing purposes or connected to the load ground if not needed. The shorthand form in this case is

$$(\pm W) = (+U)\frac{(\pm Z)}{(+X)} + (\pm Y). \quad (6)$$

In some cases, feedback may be connected to two of the available inputs. This is true for the square-rooting connections (Figure 9), where W is connected to both X_1 and Y_2. Setting $X_1 = W$ and $Y_2 = W$ in Equation (2), and anticipating the possibility of again providing a summing input, so setting $X_2 = S$ and $Y_1 = S$, we find, in shorthand form

$$(\pm W) = \sqrt{(+U)(+Z)} + (\pm S). \quad (7)$$

This is seen more generally to be the geometric-mean function, since both U and Z can be variable; operation is restricted to one quadrant. Feedback may also be taken to the U-interface. Full details of the operation in these modes is provided in the appropriate section of this data sheet.

Direct Denominator Control

A valuable new feature of the AD734 is the provision to replace the internal denominator voltage, U, with any value from +10 mV to +10 V. This can be used (1) to simply alter the multiplier scaling, thus improve accuracy and achieve reduced noise levels when operating with small input signals; (2) to implement an accurate two-quadrant divider, with a 1000:1 gain range and an asymptotic gain-bandwidth product of 200 MHz; (3) to achieve certain other special functions, such as AGC or rms.

Figure 2 shows the internal circuitry associated with denominator control. Note first that the denominator is actually proportional to a current, Iu, having a nominal value of 356 μA for U = 10 V, whereas the primary reference is a voltage, generated by a buried-Zener circuit and laser-trimmed to have a very low temperature coefficient. This voltage is nominally 8 V with a tolerance of ±10%.

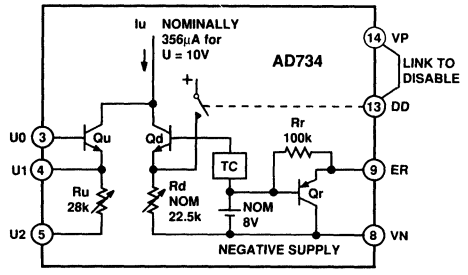


Figure 2. Denominator Control Circuitry

After temperature-correction (block TC), the reference voltage is applied to transistor Qd and trimmed resistor Rd, which generate the required reference current. Transistor Qu and resistor Ru are not involved in setting up the internal denominator, and their associated control pins U0, U1 and U2 will normally be grounded. The reference voltage is also made available, via the 100 kΩ resistor Rr, at Pin 9 (ER); the purpose of Qr is explained below.

When the control pin DD (denominator disable) is connected to VP, the internal source of Iu is shut off, and the collector current of Qu must provide the denominator current. The resistor Ru is laser-trimmed such that the multiplier denominator is exactly equal to the voltage across it (that is, across pins U1 and U2). Note that this trimming only sets up the correct internal ratio; the absolute value of Ru (nominally 28 kΩ) has a tolerance of ±20%. Also, the alpha of Qu, (typically 0.995) which might be seen as a source of scaling error, is canceled by the alpha of other transistors in the complete circuit.

In the simplest scheme (Figure 3), an externally-provided control voltage, V_G, is applied directly to U0 and U2 and the resulting voltage across Ru is therefore reduced by one V_{BE}. For example, when $V_G = 2$ V, the actual value of U will be about 1.3 V. This error will not be important in some closed-loop applications, such as automatic gain control (AGC), but clearly is not acceptable where the denominator value must be well-defined. When it is required to set up an accurate, fixed value of U, the on-chip reference may be used. The transistor Qr is provided to cancel the V_{BE} of Qu, and is biased by an external resistor, R2, as shown in Figure 4. R1 is chosen to set the desired value of U and consists of a fixed and adjustable resistor.

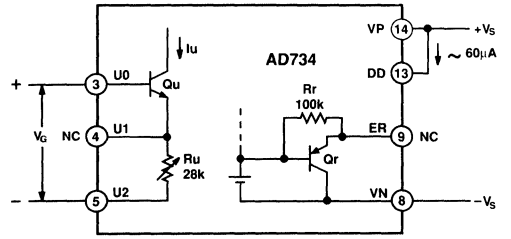


Figure 3. Low-Accuracy Denominator Control

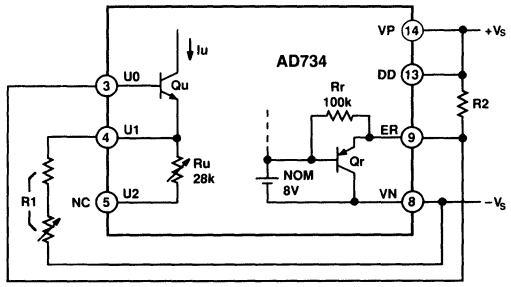


Figure 4. Connections for a Fixed Denominator

Table I shows useful values of the external components for setting up nonstandard denominator values.

Denominator	R1 (Fixed)	R1 (Variable)	R2
5 V	34.8 kΩ	20 kΩ	120 kΩ
3 V	64.9 kΩ	20 kΩ	220 kΩ
2 V	86.6 kΩ	50 kΩ	300 kΩ
1 V	174 kΩ	100 kΩ	620 kΩ

Table I. Component Values for Setting Up Nonstandard Denominator Values

The denominator can also be current controlled, by grounding Pin 3 (U0) and withdrawing a current of Iu from Pin 4 (U1). The nominal scaling relationship is U = 28 × Iu, where u is expressed in volts and Iu is expressed in milliamps. Note, however, that while the linearity of this relationship is very good, it is subject to a scale tolerance of ±20%. Note that the common mode range on Pins 3 through 5 actually extends from 4 V to 36 V below VP, so it is not necessary to restrict the connection of U0 to ground if it should be desirable to use some other voltage.

The output ER may also be buffered, re-scaled and used as a general-purpose reference voltage. It is generated with respect to the negative supply line Pin 8 (VN), but this is acceptable when driving one of the signal interfaces. An example is shown in Figure 12, where a fixed numerator of 10 V is generated for a divider application. There, Y_2 is tied to VN but Y_1 is 10 V above this; therefore the common-mode voltage at this interface is still 5 V above VN, which satisfies the internal biasing requirements (see Specifications Table).

OPERATION AS A MULTIPLIER

All of the connection schemes used in this section are essentially identical to those used for the AD534, with which the AD734 is pin-compatible. The only precaution to be noted in this regard is that in the AD534, Pins 3, 5, 9, and 13 are not internally connected and Pin 4 has a slightly different purpose. In many cases, an AD734 can be directly substituted for an AD534 with immediate benefits in static accuracy, distortion, feedthrough, and speed. Where Pin 4 was used in an AD534 application to achieve a reduced denominator voltage, this function can now be much more precisely implemented with the AD734 using alternative connections (see Direct Denominator Control, page 5).

Operation from supplies down to ±8 V is possible. The supply current is essentially independent of voltage. As is true of all high speed circuits, careful power-supply decoupling is important in maintaining stability under all conditions of use. The decoupling capacitors should always be connected to the load ground, since the load current circulates in these capacitors at high frequencies. Note the use of the special symbol (a triangle with the letter 'L' inside it) to denote the load ground.

Standard Multiplier Connections

Figure 5 shows the basic connections for multiplication. The X and Y inputs are shown as optionally having their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

The AD734 has an input resistance of 50 kΩ ± 20% at the X, Y, and Z interfaces, which allows ac-coupling to be achieved

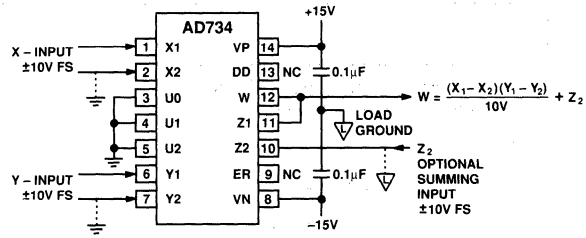


Figure 5. Basic Multiplier Circuit

with moderately good control of the high-pass (HP) corner frequency; a capacitor of 0.1 μF provides a HP corner frequency of 32 Hz. When a tighter control of this frequency is needed, or when the HP corner is above about 100 kHz, an external resistor should be added across the pair of input nodes.

At least one of the two inputs of any pair must be provided with a dc path (usually to ground). The careful selection of ground returns is important in realizing the full accuracy of the AD734. The Z2 pin will normally be connected to the load ground, which may be remote, in some cases. It may also be used as an optional summing input (see Equations (3) and (4), above) having a nominal FS input of ±10 V and the full 10 MHz bandwidth.

In applications where high absolute accuracy is essential, the scaling error caused by the finite resistance of the signal source(s) may be troublesome; for example, a 50 Ω source resistance at just one input will introduce a gain error of −0.1%; if both the X- and Y-inputs are driven from 50 Ω sources, the scaling error in the product will be −0.2%. Provided the source resistance(s) are known, this gain error can be completely compensated by including the appropriate resistance (50 Ω or 100 Ω, respectively, in the above cases) between the output W (Pin 12) and the Z1 feedback input (Pin 11). If Rx is the total source resistance associated with the X1 and X2 inputs, and Ry is the total source resistance associated with the Y1 and Y2 inputs, and neither Rx nor Ry exceeds 1 kΩ, a resistance of Rx+Ry in series with pin Z1 will provide the required gain restoration.

Pins 9 (ER) and 13 (DD) should be left unconnected in this application. The U-inputs (Pins 3, 4 and 5) are shown connected to ground; they may alternatively be connected to VN, if desired. In applications where Pin 2 (X2) happens to be driven with a high-amplitude, high-frequency signal, the capacitive coupling to the denominator control circuitry via an ungrounded Pin 3 can cause high-frequency distortion. However, the AD734 can be operated without modification in an AD534 socket, and these three pins left unconnected, with the above caution noted.

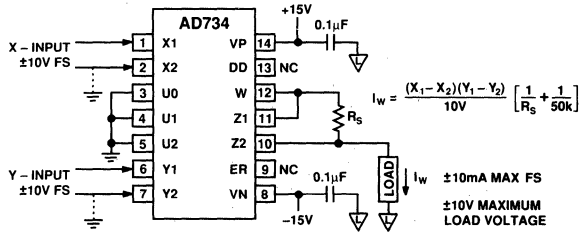


Figure 6. Conversion of Output to a Current

Current Output

It may occasionally be desirable to convert the output voltage to a current. In correlation applications, for example, multiplication is followed by integration; if the output is in the form of a current, a simple grounded capacitor can perform this function. Figure 6 shows how this can be achieved. The op-amp forces the voltage across Z1 and Z2, and thus across the resistor R_S, to be the product XY/U. Note that the input resistance of the Z interface is in shunt with R_S, which must be calculated accordingly.

The smallest FS current is simply ±10 V/50 kΩ, or ±200 μA, with a tolerance of about 20%. To guarantee a 1% conversion tolerance without adjustment, R_S must be less than 2.5 kΩ. The maximum full scale output current should be limited to about ±10 mA (thus, R_S = 1 kΩ). This concept can be applied to all connection modes, with the appropriate choice of terminals.

Squaring and Frequency-Doubling

Squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel; the phasing can be chosen to produce an output of E^2/U or $-E^2/U$ as desired. The input may have either polarity, but the basic output will either always be positive or negative; as for multiplication, the Z2 input may be used to add a further signal to the output.

When the input is a sinewave, a squarer behaves as a frequency-doubler, since

$$(Esin\omega t)^2 = E^2\,(1 - cos2\omega t)/2 \qquad (8)$$

Equation (8) shows a dc term at the output which will vary strongly with the amplitude of the input, E. This dc term can be avoided using the connection shown in Figure 7, where an RC-network is used to generate two signals whose product has no dc term. The output is

$$W = 4\left\{\frac{E}{\sqrt{2}}\,sin\left(\omega t + \frac{\pi}{4}\right)\right\}\left\{\frac{E}{\sqrt{2}}\,sin\left(\omega t - \frac{\pi}{4}\right)\right\}\left(\frac{1}{10\ V}\right) \qquad (9)$$

for ω = 1/CR1, which is just

$$W = E^2(cos2\omega t)/(10\ V) \qquad (10)$$

which has no dc component. To restore the output to ±10 V when E = 10 V, a feedback attenuator with an approximate ratio of 4 is used between W and Z1; this technique can be used wherever it is desired to achieve a higher overall gain in the transfer function.

In fact, the values of R3 and R4 include additional compensation for the effects of the 50 kΩ input resistance of all three interfaces; R2 is included for a similar reason. These resistor values should not be altered without careful calculation of the consequences; with the values shown, the center frequency f_0 is 100 kHz for C = 1 nF. The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at f = $0.9f_0$ and f = $1.1f_0$. The cross-connection is simply to produce the cosine output with the sign shown in Equation (10); however, the sign in this case will rarely be important.

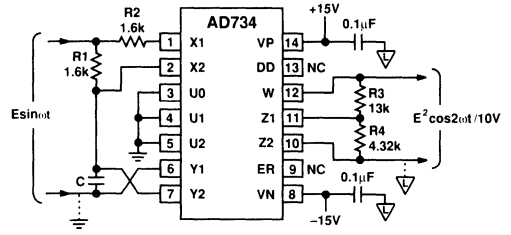


Figure 7. Frequency Doubler

OPERATION AS A DIVIDER

The AD734 supports two methods for performing analog division. The first is based on the use of a multiplier in a feedback loop. This is the standard mode recommended for multipliers having a fixed scaling voltage, such as the AD534, and will be described in this Section. The second uses the AD734's unique capability for externally varying the scaling (denominator) voltage directly, and will be described in the next section.

Feedback Divider Connections

Figure 8 shows the connections for the standard (AD534) divider mode. Feedback from the output, W, is now taken to the Y2 (inverting) input, which, provided that the X-input is positive, establishes a negative feedback path. Y1 should normally be connected to the ground associated with the load circuit, but may optionally be used to sum a further signal to the output. If desired, the polarity of the Y-input connections can be reversed, with W connected to Y1 and Y2 used as the optional summation input. In this case, either the polarity of the X-input connections must be reversed, or the X-input voltage must be negative.

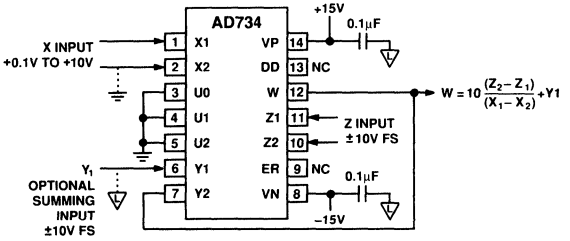


Figure 8. Standard (AD534) Divider Connection

The numerator input, which is differential and can have either polarity, is applied to pins Z1 and Z2. As with all dividers based on feedback, the bandwidth is directly proportional to the denominator, being 10 MHz for X = 10 V and reducing to 100 kHz for X = 100 mV. This reduction in bandwidth, and the increase in output noise (which is inversely proportional to the denominator voltage) preclude operation much below a denominator of 100 mV. Division using direct control of the denominator (Figure 10) does not have these shortcomings.

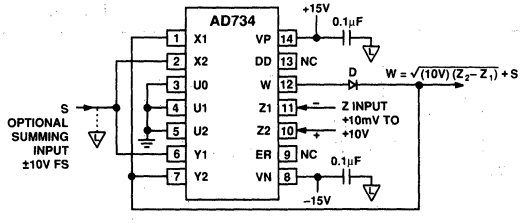


Figure 9. Connection for Square Rooting

Connections for Square-Rooting

The AD734 may be used to generate an output proportional to the square-root of an input using the connections shown in Figure 9. Feedback is now via both the X and Y inputs, and is always negative because of the reversed-polarity between these two inputs. The Z input must have the polarity shown, but because it is applied to a differential port, either polarity of input can be accepted with reversal of Z1 and Z2, if necessary. The diode D, which can be any small-signal type (1N4148 being suitable) is included to prevent a latching condition which could occur if the input momentarily was of the incorrect polarity of the input, the output will be always negative.

Note that the loading on the output side of the diode will be provided by the 25 kΩ of input resistance at X1 and Y2, and by the user's load. In high speed applications it may be beneficial to include further loading at the output (to 1 kΩ minimum) to speed up response time. As in previous applications, a further signal, shown here as S, may be summed to the output; if this option is not used, this node should be connected to the load ground.

DIVISION BY DIRECT DENOMINATOR CONTROL

The AD734 may be used as an analog divider by directly varying the denominator voltage. In addition to providing much higher accuracy and bandwidth, this mode also provides greater flexibility, because all inputs remain available. Figure 10 shows the connections for the general case of a three-input multiplier divider, providing the function

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{(U_1 - U_2)} + Z_2, \qquad (11)$$

where the X, Y, and Z signals may all be positive or negative, but the difference $U = U_1 - U_2$ must be positive and in the range +10 mV to +10 V. If a negative denominator voltage must be used, simply ground the noninverting input of the op amp. As previously noted, the X input must have a magnitude of less than 1.25U.

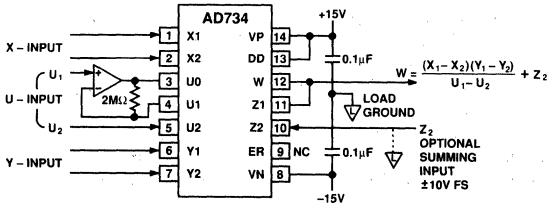


Figure 10. Three-Variable Multiplier/Divider Using Direct Denominator Control

This connection scheme may also be viewed as a variable-gain element, whose output, in response to a signal at the X input, is controllable by both the Y input (for attenuation, using Y less than U) and the U input (for amplification, using U less than Y). The ac performance is shown in Figure 11; for these results, Y was maintained at a constant 10 V. At U = 10 V, the gain is unity and the circuit bandwidth is a full 10 MHz. At U = 1 V, the gain is 20 dB and the bandwidth is essentially unaltered. At U = 100 mV, the gain is 40 dB and the bandwidth is 2 MHz. Finally, at U = 10 mV, the gain is 60 dB and the bandwidth is 250 kHz, corresponding to a 250 MHz gain-bandwidth product.

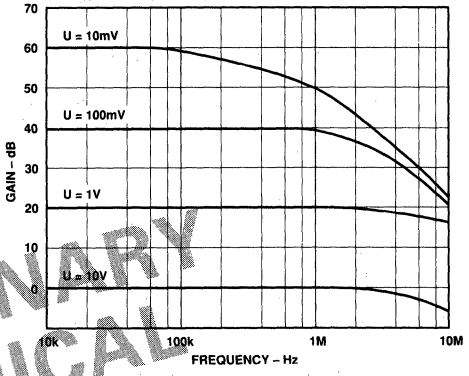


Figure 11. Three-Variable Multiplier/Divider Performance

The 2 MΩ resistor is included to improve the accuracy of the gain for small denominator voltages. At high gains, the X input offset voltage can cause a significant output offset voltage. To eliminate this problem, a low-pass feedback path can be used from W to X2; see Figure 13 for details.

Where a numerator of 10 V is needed, to implement a two-quadrant divider with fixed scaling, the connections shown in Figure 12 may be used. The reference voltage output appearing between Pin 9 (ER) and Pin 8 (VN) is amplified and buffered by the second op amp, to impose 10 V across the Y1/Y2 input. Note that Y2 is connected to the negative supply in this application. This is permissable because the common-mode voltage is still high enough to meet the internal requirements. The transfer function is

$$W = 10V\left(\frac{X_1 - X_2}{U_1 - U_2}\right) + Z_2. \qquad (12)$$

The ac performance of this circuit remains as shown in Figure 11.

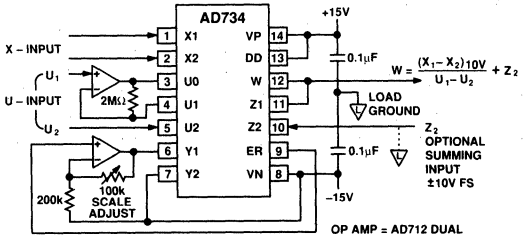


Figure 12. Two-Quadrant Divider with Fixed 10 V Scaling

A PRECISION AGC LOOP

The variable denominator of the AD734 and its high gain-bandwidth product make it an excellent choice for precise automatic gain control (AGC) applications. Figure 13 shows a suggested method. The input signal, E_{IN}, which may have a peak amplitude of from 10 mV to 10 V at any frequency from 100 Hz to 10 MHz, is applied to the X input, and a fixed positive voltage E_C to the Y input. Op amp A2 and capacitor C2 form an integrator having a current summing node at its inverting input. (The AD712 dual op amp is a suitable is a suitable choice for this application.) In the absence of an input, the current in D2 and R2 causes the integrator output to ramp negative, clamped by diode D3, which is included to reduce the time required for the loop to establish a stable, calibrated, output level once the circuit has received an input signal. With no input to the denominator (U0 and U2), the gain of the AD734 is very high (about 70 dB), and thus even a small input causes a substantial output.

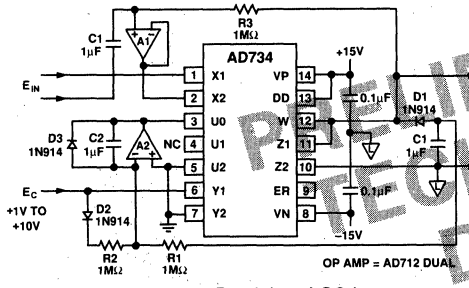


Figure 13. Precision AGC Loop

Diode D1 and C1 form a peak detector, which rectifies the output and causes the integrator to ramp positive. When the current in R1 balances the current in R2, the integrator output holds the denominator output at a constant value. This occurs when there is sufficient gain to raise the amplitude of E_{IN} to that required to establish an output amplitude of E_C over the range of +1 V to +10 V. The X input of the AD734, which has finite offset voltage, could be troublesome at the output at high gains. The output offset is reduced to that of the X input (one or two millivolts) by the offset loop comprising R3, C3, and buffer A1. The low pass corner frequency of 0.16 Hz is transformed to a high-pass corner that is multiplied by the gain (for example, 160 Hz at a gain of 1000).

In applications not requiring operation down to low frequencies, amplifier A1 can be eliminated, but the AD734's input resistance of 50 kΩ between X1 and X2 will reduce the time constant and increase the input offset. Using a non-polar 20 μF tantalum capacitor for C1 will result in the same unity-gain high-pass corner; in this case, the offset gain increases to 20, still very acceptable.

Figure 14 shows the error in the output for sinusoidal inputs at 100 Hz, 100 kHz, and 1 MHz, with E_C set to +10 V. The output error for any frequency between 300 Hz and 300 kHz is similar to that for 100 kHz. At low signal frequencies and low input amplitudes, the dynamics of the control loop determine the gain error and distortion; at high frequencies, the 200 MHz gain-bandwidth product of the AD734 limit the available gain.

The output amplitude tracks E_C over the range +1 V to slightly more than +10 V.

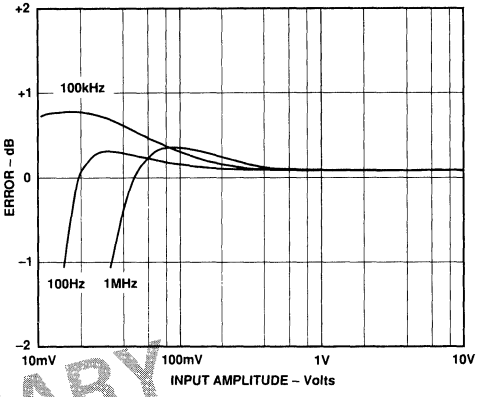


Figure 14. AGC Amplifier Output Error vs. Input Voltage

WIDEBAND RMS-DC CONVERTER USING U INTERFACE

The AD734 is well suited to such applications as implicit RMS-DC conversion, where the AD734 implements the function

$$V_{RMS} = \frac{avg\,[V_{IN}^2]}{V_{RMS}} \qquad (13)$$

using its direct divide mode. Figure 15 shows the circuit.

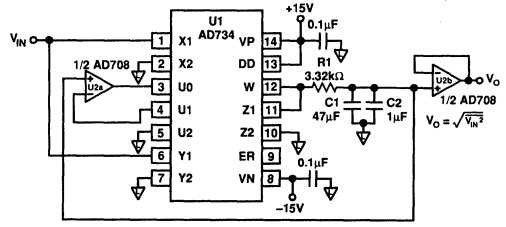


Figure 15. A 2-Chip, Wideband RMS-DC Converter

In this application, the AD734 and an AD708 dual op amp serve as a 2-chip RMS-DC converter with a 10 MHz bandwidth. Figure 16 shows the circuit's performance for square-, sine-, and triangle-wave inputs. The circuit accepts signals as high as 10 V p–p with a crest factor of 1 or 1 V p–p with a crest factor of 10. The circuit's response is flat to 10 MHz with an input of 10 V, flat to almost 5 MHz for an input of 1 V, and to almost 1 MHz for inputs of 100 mV. For accurate measurements of input levels below 100 mV, the AD734's output offset (Z interface) voltage, which contributes a dc error, must be trimmed out.

In Figure 15's circuit, the AD734 squares the input signal, and its output (V_{IN}^2) is averaged by a low-pass filter that consists of R1 and C1 and has a corner frequency of 1 Hz. Because of the implicit feedback loop, this value is both the output value, V_{RMS}, and the denominator in Equation (13). U2a and U2b, an AD708 dual dc precision op amp, serve as unity-gain buffers, supplying both the output voltage and driving the U interface.

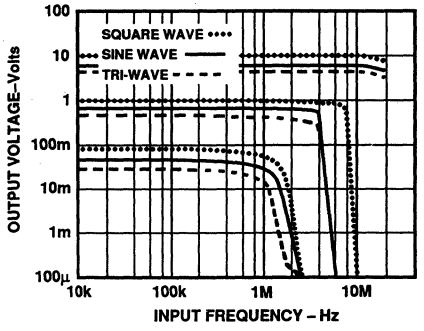


Figure 16. RMS-DC Converter Performance

LOW DISTORTION MIXER

The AD734's low noise and distortion make it especially suitable for use as a mixer, modulator, or demodulator. Although the AD734's −3 dB bandwidth is typically 10 MHz and is established by the output amplifier, the bandwidth of its X and Y interfaces and the multiplier core are typically in excess of 40 MHz. Thus, provided that the desired output signal is less than 10 MHz, as would typically be the case in demodulation, the AD734 can be used with both its X and Y input signals as high as 40 MHz. One test of mixer performance is to linearly combine two closely spaced, equal-amplitude sinusoidal signals and then mix them with a third signal to determine the mixer's 2-tone Third-Order Intermodulation Products.

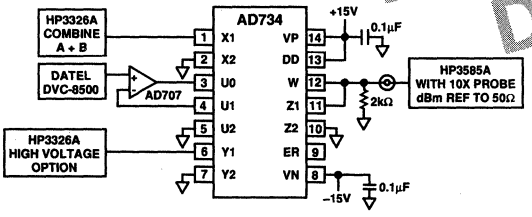


Figure 17. AD734 Mixer Test Circuit

Figure 17 shows a test circuit for measuring the AD734's performance in this regard. In this test, two signals, at 10.05 MHz and 9.95 MHz are summed and applied to the AD734's X interface. A second 9 MHz signal is applied to the AD734's Y interface. The voltage at the U interface is set to 2 V to use the full dynamic range of the AD734. That is, by connecting the W and Z1 pins together, grounding the Y2 and X2 pins, and setting U = 2 V, the overall transfer function is

$$W = \frac{X_1 Y_1}{2\,V} \qquad (14)$$

and W can be as high as 20 V p–p when X1 = 2 V p–p and Y1 = 10 V p–p. The 2 V p–p signal level corresponds to +10 dBm into a 50 Ω input termination resistor connected from X1 or Y1 to ground.

If the two X1 inputs are at frequencies f_1 and f_2 and the frequency at the Y1 input is f_0, then the two-tone third-order intermodulation products should appear at frequencies $2f_1 - f_2 \pm f_0$ and $2f_2 - f_1 \pm f_0$. Figures 18 and 19 show the output spectra of the AD734 with f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz for a signal level of f_1 & f_2 of 6 dBm and f_0 of +24 dBm in Figure 18 and f_1 & f_2 of 0 dBm and f_0 of +24 dBm in Figure 19. This performance is *without* external trimming of the AD734's X and Y input-offset voltages.

The possible Two Tone Intermodulation Products are at 2 × 9.95 MHz − 10.05 MHz ± 9.00 MHz and 2 × 10.05 − 9.95 MHz ±9.00 MHz; of these only the third-order products at 0.850 MHz and 1.150 MHz are within the 10 MHz bandwidth of the AD734; the desired output signals are at 0.950 MHz and 1.050 MHz. Note that the difference (Figure 18) between the desired outputs and third-order products is approximately 78 dB, which corresponds to a computed third-order intercept point of +46 dBm.

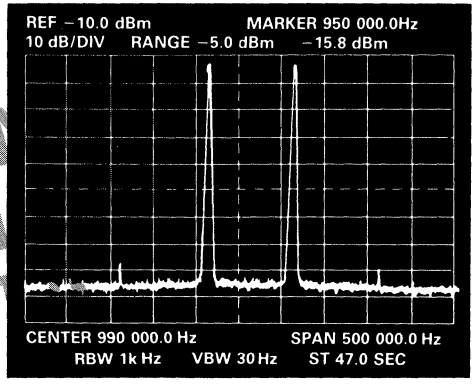


Figure 18. AD734 Third-Order Intermodulation Performance for f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz and for Signal Levels of f_1 & f_2 of 6 dBm and f_0 of +24 dBm. All Displayed Signal Levels Are Attenuated 20 dB by the 10X Probe Used to Measure the Mixer's Output

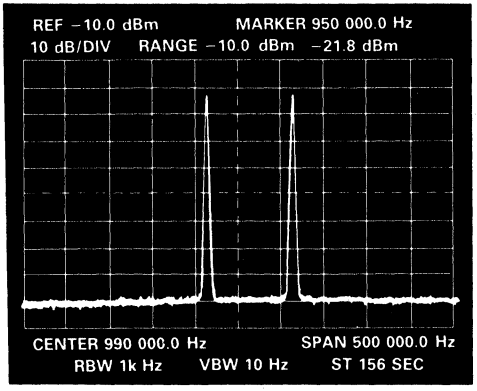


Figure 19. AD734 Third-Order Intermodulation Performance for f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz and for Signal Levels of f_1 & f_2 of 0 dBm and f_0 of +24 dBm. All Displayed Signal Levels Are Attenuated 20 dB by the 10X Probe Used to Measure the Mixer's Output

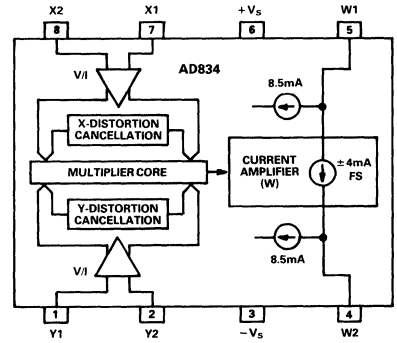
500MHz Four-Quadrant Multiplier

AD834

FEATURES
DC to >500MHz Operation
Differential ±1V Full Scale Inputs
Differential ±4mA Full Scale Output Current
Low Distortion (≤0.05% for 0dBm Input)
Supply Voltages from ±4V to ±9V
Low Power (280mW typical at V_S=±5V)

APPLICATIONS
High Speed Real Time Computation
Wideband Modulation and Gain Control
Signal Correlation and RF Power Measurement
Voltage Controlled Filters and Oscillators
Linear Keyers for High Resolution Television
Wideband True RMS

AD834 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD834 is a monolithic laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, having a transconductance bandwidth (R_L=50Ω) in excess of 500MHz from either of the differential voltage inputs. In multiplier modes, the typical total full scale error is 0.5%, dependent on the application mode and the external circuitry. Performance is relatively insensitive to temperature and supply variations, due to the use of stable biasing based on a bandgap reference generator and other design features.

To preserve the full bandwidth potential of the high speed bipolar process used to fabricate the AD834, the outputs appear as a differential pair of currents at open collectors. To provide a single ended ground referenced voltage output, some form of external current to voltage conversion is needed. This may take the form of a wideband transformer, balun, or active circuitry such as an op amp. In some applications (such as power measurement) the subsequent signal processing may not need to have high bandwidth.

The transfer function is accurately trimmed such that when X=Y=±1V, the differential output is ±4mA. This absolute calibration allows the outputs of two or more AD834s to be summed with precisely equal weighting, independent of the accuracy of the load circuit.

The AD834J is specified for use over the commercial temperature range of 0 to +70°C and is available in an 8-pin cerdip package, an 8-pin plastic DIP package, and an 8-pin plastic SOIC package. AD834A is available in cerdip for operation over the industrial temperature range of −40°C to +85°C. The AD834S/883B is specified for operation over the military temperature range of −55°C to +125°C and is available in the 8-pin cerdip package. S-Grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD834 combines high static accuracy (low input and output offsets and accurate scale factor) with very high bandwidth. As a four-quadrant multiplier or squarer, the response extends from dc to an upper frequency limited mainly by packaging and external board layout considerations. A large signal bandwidth of over 500MHz is attainable under optimum conditions.
2. The AD834 can be used in many high speed nonlinear operations, such as square rooting, analog division, vector addition and rms-to-dc conversion. In these modes, the bandwidth is limited by the external active components.
3. Special design techniques result in low distortion levels (better than −60dB on either input) at high frequencies and low signal feedthrough (typically −65dB up to 20MHz).
4. The AD834 exhibits low differential phase error over the input range—typically 0.08° at 5MHz and 0.8° at 50MHz. The large signal transient response is free from overshoot, and has an intrinsic rise time of 500ps, typically settling to within 1% in under 5ns.
5. The nonloading, high impedance, differential inputs simplify the application of the AD834.

SPECIFICATIONS (T_A=+25°C and $\pm V_S$=±5V, unless otherwise noted; dBm assumes 50Ω load.)

Model	Conditions	AD834J Min	AD834J Typ	AD834J Max	AD834A, S Min	AD834A, S Typ	AD834A, S Max	Units
MULTIPLIER PERFORMANCE								
Transfer Function			$W = \frac{XY}{(1V)^2} \times 4mA$			$W = \frac{XY}{(1V)^2} \times 4mA$		
Total Error[1] (Figure 6)	−1V≤X,Y<+1V		±0.5	**±2**		±0.5	**±2**	% FS
vs. Temperature	T_{min} to T_{max}					±1.5	**±3**	% FS
vs. Supplies[2]	±4V to ±6V		0.1	**0.3**		0.1	**0.3**	% FS/V
Linearity[3]			±0.5	**±1**		±0.5	**±1**	% FS
Bandwidth[4]	See Figure 5	500			500			MHz
Feedthrough, X	X=±1V, Y=Nulled		0.2	**0.3**		0.2	**0.3**	% FS
Feedthrough, Y	X=Nulled, Y=±1V		0.1	**0.2**		0.1	**0.2**	% FS
AC Feedthrough, X[5]	X=0dBm, Y=Nulled							
	f=10MHz		−65			−65		dB
	f=100MHz		−50			−50		dB
AC Feedthrough, Y[5]	X=Nulled, Y=0dBm							
	f=10MHz		−70			−70		dB
	f=100MHz		−50			−50		dB
INPUTS (X1, X2, Y1, Y2)								
Full Scale Range	Differential		±1			±1		V
Clipping Level	Differential	**±1.1**	±1.3		**±1.1**	±1.3		V
Input Resistance	Differential		25			25		kΩ
Offset Voltage			0.5	**3**		0.5	**3**	mV
vs. Temperature	T_{min} to T_{max}		10			10		µV/°C
				4			**4**	mV
vs. Supplies[2]	±4V to ±6V		100	**300**		100	**300**	µV/V
Bias Current			45			45		µA
Common Mode Rejection	f≤100kHz; 1V p-p		70			70		dB
Nonlinearity, X	Y=1V; X=±1V		0.2	**0.5**		0.2	**0.5**	% FS
Nonlinearity, Y	X=1V; Y=±1V		0.1	**0.3**		0.1	**0.3**	% FS
Distortion, X	X=0dBm, Y=1V							
	f=10MHz		−60			−60		dB
	f=−100MHz		−44			−44		dB
Distortion, Y	X=1V, Y=0dBM							
	f=10MHz		−65			−65		dB
	f=100MHz		−50			−50		dB
OUTPUTS (W1, W2)								
Zero Signal Current	Each Output		8.5			8.5		mA
Differential Offset	X=0, Y=0		±20	**±60**		±20	**±60**	µA
vs. Temperature	T_{min} to T_{max}		40			40		nA/°C
							±60	µA
Scaling Current	Differential	3.96	4	4.04	3.96	4	4.04	mA
Output Compliance		4.75		9	4.75		9	V
Noise Spectral Density	f=10Hz to 1MHz Outputs into 50Ω Load		16			16		nV/$\sqrt{Hz}$
POWER SUPPLIES								
Operating Range		±4		±9	±4		±9	V
Quiescent Current[6]	T_{min} to T_{max}							
$+V_S$			11	**14**		11	**14**	mA
$-V_S$			28	**35**		28	**35**	mA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD834J					
Military (−55°C to +125°C)						AD834S		
Industrial (−40°C to +85°C)						AD834A		
PACKAGE OPTIONS[7]								
8-Pin SOIC (R)			AD834JR					
8-Pin Cerdip (Q)						AD834AQ		
8-Pin Plastic DIP (N)			AD834JN			AD834SQ/883B		

NOTE

[1]Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full scale output.

[2]Both supplies taken simultaneously; sinusoidal input at f≤10kHz.

[3]Linearity is defined as residual error after compensating for input offset voltage, output offset current and scaling current errors.

[4]Bandwidth is guaranteed when configured in squarer mode. See Figure 5.

[5]Sine input; relative to full scale output; zero input port nulled; represents feedthrough of the fundamental.

[6]Negative supply current is equal to the sum of positive supply current, the signal currents into each output, W1 and W2, and the input bias currents.

[7]See Section 20 for package outline information.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

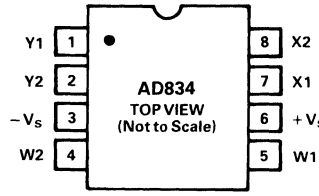
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$ to $-V_S$) 18V
Internal Power Dissipation 500mW
Input Voltages (X1, X2, Y1, Y2) . . . . . $+V_S$
Operating Temperature Range
AD834J . . . . . 0 to +70°C
AD834A . . . . . −40°C to +85°C
AD834S/883B . . . . . −55°C to +125°C
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range R, N . . . . . −65°C to +125°C
Lead Temperature, Soldering 60sec . . . . . +300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM

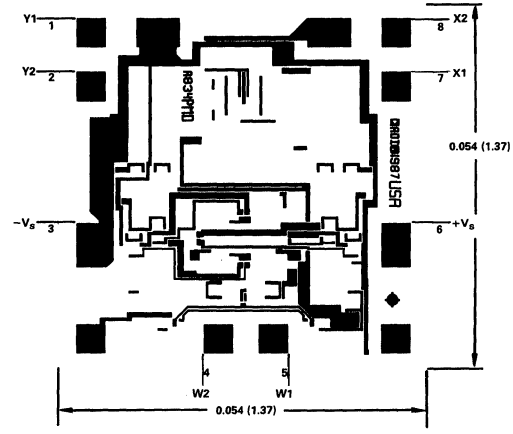
Small Outline (R) Package
Plastic DIP (N) Package
Cerdip (Q) Package



METALIZATION PHOTO

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
8-Pin Cerdip Package (Q)	30°C/W	110°C/W
8-Pin Plastic SOIC (R)	45°C/W	165°C/W
8-Pin Plastic Mini-DIP (N)	50°C/W	99°C/W

ORDERING GUIDE*

Temperature Range	Plastic DIP (N-8) Package	Cerdip (Q-8) Package	Plastic SOIC (R-8) Package	Chips
0 to +70°C	AD834JN		AD834JR	
−40°C to +85°C		AD834AQ		
−55°C to +125°C		AD834SQ/883B		AD834S Chips

*See Section 20 for package outline information.

Typical Characteristics

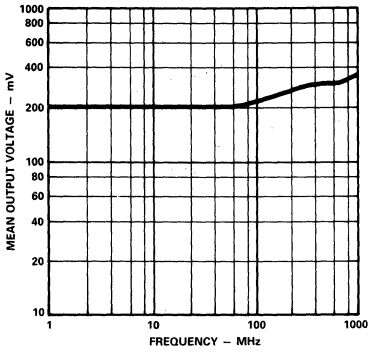


Figure 1. Mean-Square Output vs. Frequency

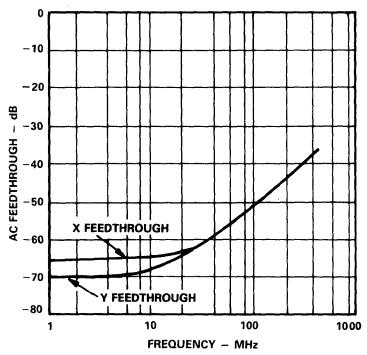


Figure 2. AC Feedthrough vs. Frequency

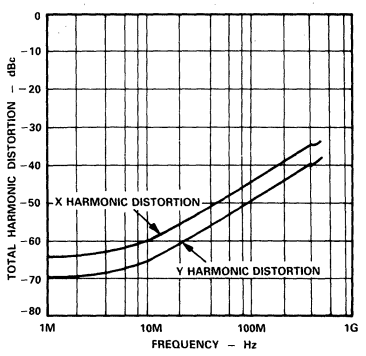


Figure 3. Total Harmonic Distortion vs. Frequency

Figure 1. Figure 1 is a plot of the mean-square output versus frequency for the test circuit of Figure 5. Note that the rising response is due to package resonances.

Figure 2. For frequencies below 1MHz, ac feedthrough is dominated by static nonlinearities in the transfer function and the finite offset voltages. The offset voltages cause a small fraction of the fundamental to appear at the output, and can be nulled out.

Figure 3. THD data represented in Figure 3 is dominated by the second harmonic, and is generated with 0dBm input on the ac input and +1V on the dc input. For a given amplitude on the ac input, THD is relatively insensitive to changes in the dc input amplitude. Varying the ac input amplitude while maintaining a constant dc input amplitude will affect THD performance.

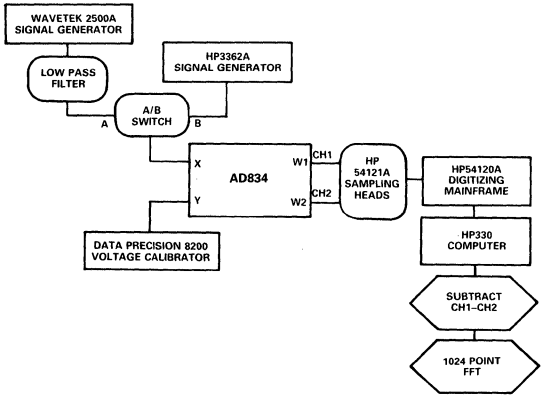


Figure 4. Test Configuration for Measuring ac Feedthrough and Total Harmonic Distortion

Figure 5. The squarer configuration shown in Figure 5 is used to determine wideband performance because it eliminates the need for (and the response uncertainties of) a wideband measurement device at the output. The wideband output of a squarer configuration is a fluctuating current at twice the input frequency with a mean value proportional to the square of the input amplitude.

By placing capacitors C3/C5 and C4/C6 across load resistors R1 and R2, a simple low-pass filter is formed, and the mean-square value is extracted. The mean-square response can be measured using a DVM connected across R1 and R2.

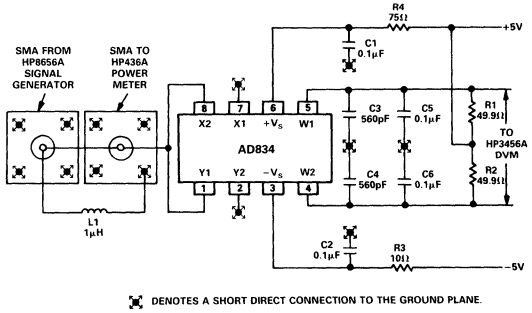


Figure 5. Bandwidth Test Circuit

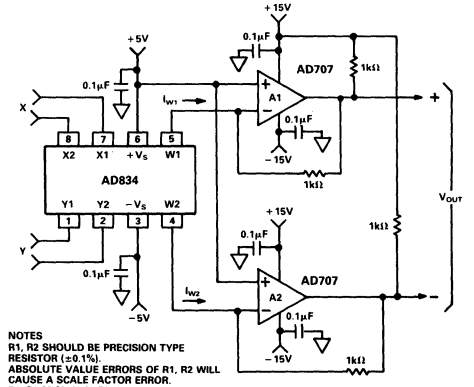


Figure 6. Low Frequency Test Circuit

BASIC OPERATION

Figure 7 is a functional equivalent of the AD834. There are three differential signal interfaces: the voltage inputs X= X1−X2 and Y=Y1−Y2, and the current output, W (see Fig. 7) which flows in the direction shown when X and Y are positive. The outputs W1 and W2 each have a standing current of typically 8.5mA.

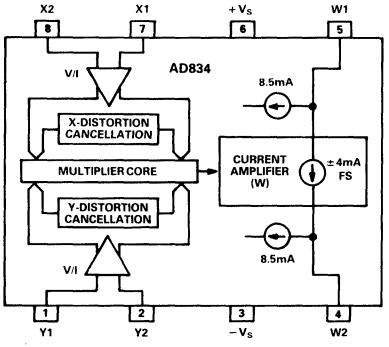


Figure 7. AD834 Functional Block Diagram

The input voltages are first converted to differential currents which drive the translinear core. The equivalent resistance of the voltage-to-current (V-I) converters is about 285Ω. This low value results in low input related noise and drift. However, the low full scale input voltage results in relatively high nonlinearity in the V-I converters. This is significantly reduced by the use of distortion cancellation circuits which operate by Kelvin sensing the voltages generated in the core — an important feature of the AD834.

The current mode output of the core is amplified by a special cascode stage which provides a current gain of nominally ×1.6, trimmed during manufacture to set up the full scale output current of ±4mA. **This output appears at a pair of open collectors which must be supplied with a voltage slightly above the voltage on Pin 6.** As shown in Figure 8, this can be arranged by inserting a resistor in series with the supply to this pin and taking the load resistors to the full supply. With R3=60Ω, the voltage drop across it is about 600mV. Using two 50Ω load resistors, the full scale differential output voltage is ±400mV.

The full bandwidth potential of the AD834 can only be realized when very careful attention is paid to grounding and decoupling. The device must be mounted close to a high quality ground plane and all lead lengths must be extremely short, in keeping with UHF circuit layout practice. In fact, the AD834 shows useful response to well beyond 1GHz, and the actual upper frequency in a typical application will usually be determined by the care with which the layout is effected. Note that R4 (in series with the $-V_S$ supply) carries about 30mA, and thus introduces a voltage drop of about 150mV. It is made large enough to reduce the Q of the resonant circuit formed by the supply lead and the decoupling capacitor. Slightly larger values can be used, particularly when using higher supply voltages. Alternatively, lossy RF chokes or ferrite beads on the supply leads may be used.

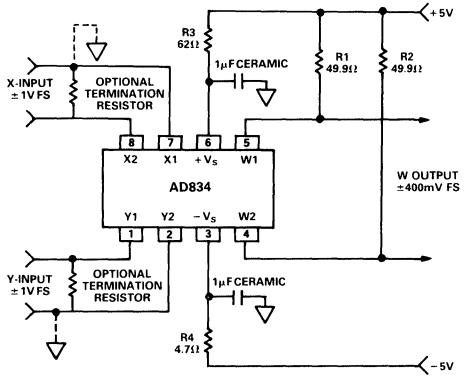


Figure 8. Basic Connections for Wideband Operation

Figure 8 shows the use of optional termination resistors at the inputs. Note that although the resistive component of the input impedance is quite high (about 25kΩ), the input bias current of typically 45μA can generate significant offset voltages if not compensated. For example, with a source and termination resistance of 50Ω (net source of 25Ω) the offset would be 25Ω×45μA=1.125mV. This can be almost fully cancelled by including (in this example) another 25Ω resistor in series with the "unused" input (in Figure 8, either X1 or Y2). In order to minimize crosstalk the input pins closest to the output (X1 and Y2) should be grounded; the effect is merely to reverse the phase of the X input and thus alter the polarity of the output.

TRANSFER FUNCTION

The output current W is the linear product of input voltages X and Y divided by $(1V)^2$ and multiplied by the "scaling current" of 4mA:

$$W = \frac{XY}{(1V)^2} \ 4mA$$

Provided that it is understood that the inputs are specified in *volts*, a simplified expression can be used:

$$W = (XY)\ 4mA$$

Alternatively, the full transfer function can be written:

$$W = \frac{XY}{1V} \cdot \frac{1}{250\Omega}$$

When both inputs are driven to their clipping level of about 1.3V, the peak output current is roughly doubled, to ±8mA, but distortion levels will then be very high.

TRANSFORMER COUPLING

In many high frequency applications where baseband operation is not required at either inputs or output, transformer coupling can be used. Figure 9 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals.

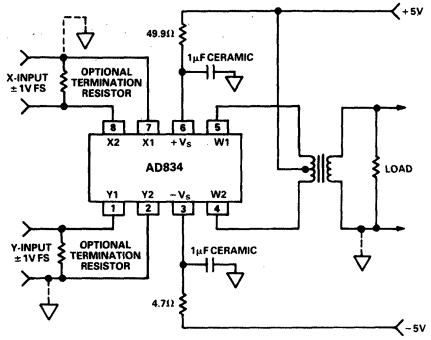


Figure 9. Transformer–Coupled Output

A particularly effective type of transformer is the balun[1] which is a short length of transmission line wound on to a toroidal ferrite core. Figure 10 shows this arrangement used to convert the bal(anced) output to an un(balanced) one (hence the use of the term). Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the first place, the load should now be equal to the characteristic impedance of the line (although this will usually not be critical for short line lengths). The collector load resistors R_C may also be chosen to reverse terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

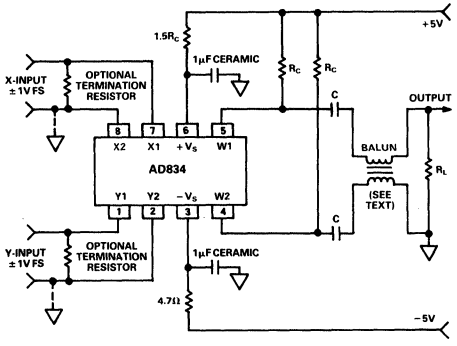


Figure 10. Using a Balun at the Output

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer where the signal is conveyed as a flux in a magnetic core and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the *series* inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

[1]For a good treatment of baluns, see "Transmission Line Transformers" by Jerry Sevick; American Radio Relay League publication.

WIDEBAND MULTIPLIER CONNECTIONS

Where operation down to dc and a ground based output are necessary, the configuration shown in Figure 11 can be used. The element values were chosen in this example to result in a full-scale output of ±1V at the load, so the overall multiplier transfer function is

$$W = (X1-X2)(Y1-Y2)$$

where it is understood that the *inputs and output are in volts*. The polarity of the output can be reversed simply by reversing either the X or Y input.

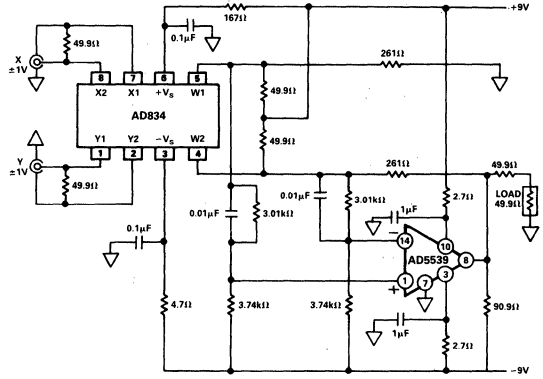


Figure 11. Wideband dc-Coupled Multiplier

The op amp should be chosen to support the desired output bandwidth. The AD5539 is shown here, providing an overall system bandwidth of 100MHz. Many other choices are possible where lower post multiplication bandwidths are acceptable. The level shifting network places the input nodes of the op amp to within a few hundred millivolts of ground using the recommended balanced supplies. The output offset may be nulled by including a 100Ω trim pot between each of the lower pair of resistors (3.74kΩ) and the negative supply.

The pulse response for this circuit shown in Figure 12; the X input was a pulse of 0 to +1V and the Y input was +1V dc. The transition times at the output are about 4ns.

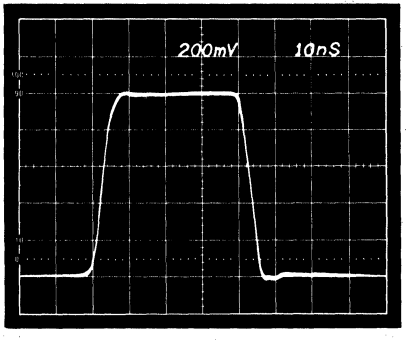


Figure 12. Pulse Response for the Circuit of Figure 11

POWER MEASUREMENT (MEAN SQUARE AND RMS)

The AD834 is well suited to measurement of average power in high frequency applications, connected either as a multiplier for the determination of the V×I product, or as a squarer for use with a single input. In these applications, the multiplier is followed by a low pass filter to extract the long term average value. Where the bandwidth extends to several hundred megahertz, the first pole of this filter should be formed by grounded capacitors placed directly at the output pins W1 and W2. This pole can be at a few kilohertz. The effective multiplication or squaring bandwidth is then limited solely by the AD834, since the following active circuitry is required to process only low frequency signals.

(Refer to Figure 5 test configuration.) Using the device as a squarer the wideband output in response to a sinusoidal stimulus is a raised cosine:

$$\sin^2\omega t = (1 + \cos 2\omega t)/2$$

Recall here that the full scale output current (when full scale input voltages of 1V are applied to both X and Y) is 4mA. In a 50Ω system, a sinusoid power of +10dBm has a peak value of 1V. Thus, at this drive level the peak output voltage across the differential 50Ω load in the absence of the filter capacitors would be 400mV (that is, 4mA ×50Ω×2), whereas the average value of the raised cosine is only 200mV. The averaging configuration is useful in evaluating the bandwidth of the AD834, since a dc voltage is easier to measure than a wideband, differential output. In fact, the squaring mode is an even more critical test than the direct measurement of the bandwidth of either channel taken independently (with a dc input on the nonsignal channel), because the phase relationship between the two channels also affects the average output. For example, a time delay difference of only 250ps between the X and Y channels would result in zero output when the input frequency is 1GHz, at which frequency the phase angle is 90 degrees and the intrinsic product is now between a sine and cosine function, which has zero average value.

The physical construction of the circuitry around the IC is critical to realizing the bandwidth potential of the device. The input is supplied from an HP8656A signal generator (100kHz to 990MHz) via an SMA connector and terminated by an HP436A power meter using an HP8482A sensor head connected via a second SMA connector. Since neither the generator nor the sensor provide a dc path to ground, a lossy 1μH inductor L1, formed by a 22-gauge wire passing through a ferrite bead (Fair-Rite type 2743001112) is included. This provides adequate impedance down to about 30MHz. The IC socket is mounted on a ground plane,with a clear area in the rectangle formed by the pins. This is important, since significant transformer action can arise if the pins pass through individual holes in the board; this has been seen to cause an oscillation at 1.3GHz in improperly constructed test jigs. The filter capacitors must be connected directly to the same point on the ground plane via the shortest possible leads. Parallel combinations of large and small capacitors are used to minimize the impedance over the full frequency range. (Refer to Figure 1 for mean-square response for the AD834 in cerdip package, using the configuration of Figure 5.)

To provide a square-root response and thus generate the rms value at the output, a second AD834, also connected as a squarer, can be used, as shown in Figure 13. Note that an attenuator is inserted both in the signal input and in the feedback path to the second AD834. This increases the maximum input capability to +15dBm and improves the response flatness by damping some of the resonances. The overall gain is unity; that is, the output voltage is exactly equal to the rms value of the input signal. The offset potentiometer at the AD834 outputs extends the dynamic range, and is adjusted for a dc output of 125.7mV when a 1MHz sinusoidal input at −5dBm is applied.

Additional filtering is provided; the time constants were chosen to allow operation down to frequencies as low as 1kHz and to provide a critically damped envelope response, which settles typically within 10ms for a full scale input (and proportionally slower for smaller inputs). The 5μF and 0.1μF capacitors may be scaled down to reduce response time if accurate rms operation at low frequencies is not required. The output op amp must be specified to accept a common-mode input near its supply. Note that the output polarity may be inverted by replacing the NPN transistor with a PNP type.

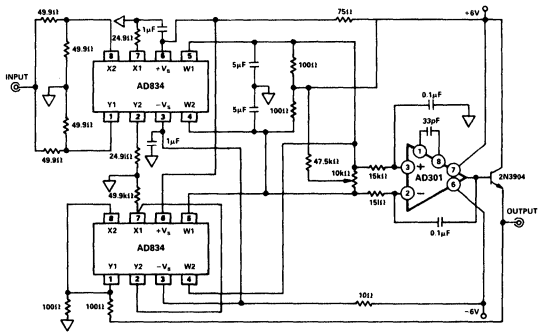


Figure 13. Connections for Wideband rms Measurement

FREQUENCY DOUBLER

Figure 14 shows another squaring application. In this case, the output filter has been removed and the wideband differential output is converted to a single sided signal using a "balun," which consists of a length of 50Ω coax cable fed through a ferrite core (Fair-Rite type 2677006301). No attempt is made to reverse terminate the output. Higher load power could be achieved by replacing the 50Ω load resistors by ferrite bead inductors. The same precautions should be observed with regard to PC board layout as recommended above. The output spectrum shown in Figure 15 is for an input power of +10dBm at a frequency of 200MHz. The second harmonic component at 400MHz has an output power of −15dBm. Some feedthrough of the fundamental occurs: it is 15dBs below the main output. It is believed that improvements in the design of the balun would reduce this feedthrough. A spurious output at 600MHz is also present, but it is 30dBs below the main output. At an input frequency of 100MHz, the measured power level at 200MHz is −16dBm, while the fundamental feedthrough is reduced to 25dBs below the main output; at an output of 600MHz the power is −11dBm and the third harmonic at 900MHz is 32dBs below the main output.

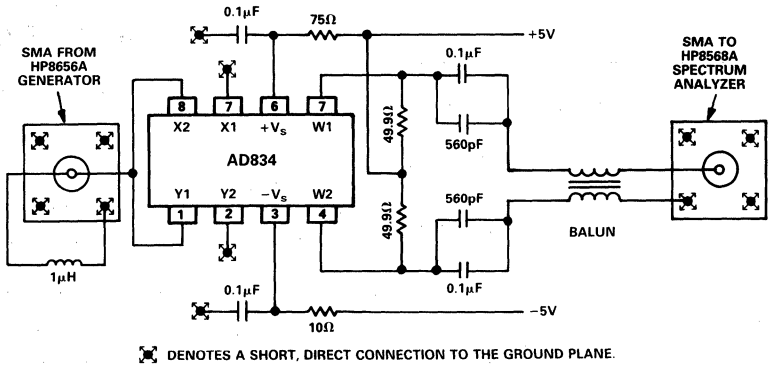


Figure 14. Frequency Doubler Connections

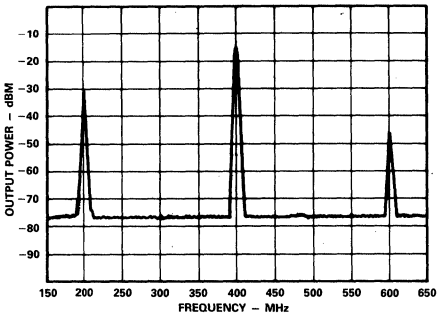


Figure 15. Output Spectrum for Configuration of Figure 14

WIDEBAND THREE SIGNAL MULTIPLIER/DIVIDER

Two AD834s and a wideband op amp can be connected to make a versatile multiplier/divider having the transfer function

$$W = \frac{(X1-X2)(Y1-Y2)}{(U1-U2)} + Z$$

with a denominator range of about 100:1. The denominator input U = U1−U2 must be positive and in the range 100mV to 10V; X, Y and Z inputs may have either polarity. Figure 16 shows a general configuration which may be simplified to suit a particular application. This circuit accepts full scale input voltages of 10V, and delivers a full scale output voltage of 10V. The optional offset trim at the output of the AD834 improves the accuracy for small denominator values. It is adjusted by nulling the output voltage when the X and Y inputs are zero and U = +100mV.

The AD840 is internally compensated to be stable without the use of any additional HF compensation. As the input U is reduced, the bandwidth falls because the feedback around the op amp is proportional to the input U.

This circuit may be modified in several ways. For example, if the differential input feature is not needed, the unused input

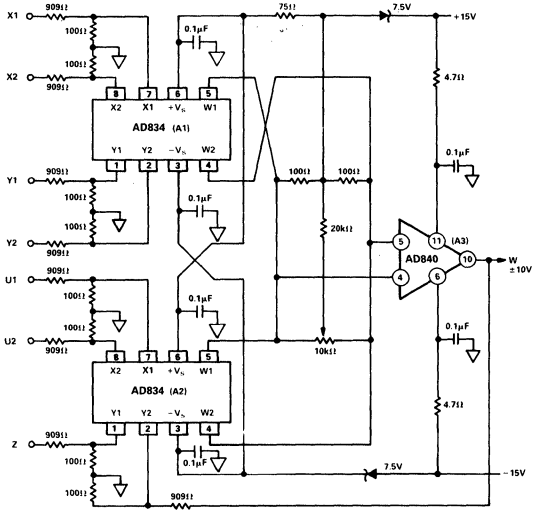


Figure 16. Wideband Three Signal Multiplier/Divider

can be connected to ground through a single resistor, equal to the parallel sum of the resistors in the attenuator section. The full scale input levels on X, Y and U can be adapted to any full scale voltage down to ±1V by altering the attenuator ratios. Note, however, that precautions must be taken if the attenuator ratio from the output of A3 back to the second AD834 (A2) is lowered. First, the HF compensation limit of the AD840 may be exceeded if the negative feedback factor is too high. Second, if the attenuated output at the AD834 exceeds its clipping level of ±1.3V, feedback control will be lost and the output will suddenly jump to the supply rails. However, with these limitations understood, it will be possible to adapt the circuit to smaller full scale inputs and/or outputs, and for use with lower supply voltages.

Log/Antilog Amplifiers
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Selection Guide
Log/Antilog Amplifiers

Model	Input Range	Log Conformity RTI	BW kHz	Package Options[1]	Temp Range[2]	Page	Comments
755	1 nA–1 mA	0.5%	10	Module	I	7–27	Complete, Current and Voltage, 6 Decade, High Accuracy
757	1 nA–1 mA	0.5%	25	Module	I	7–31	Complete, Log/Antilog Ratio, 6 Decade, High Accuracy
759	20 nA–0.2 mA	1.0%	200	Module	I	7–27	Complete, Current and Voltage, 4 Decade, Lowest Cost
AD9521	**0.4 V p-p**	**±1 dB**	**10–250 MHz**	**E, H**	**C, M**	**7–23**	**Wideband Amplifier with Logarithmic Detected Output**
AD640	**0.75 mV–200 mV**	**±0.6 dB**	**120 MHz**	**D, E, N, P**	**C, I, M**	**7–7**	**120 MHz, 45 dB, DC Demodulating Logarithmic Amplifier**

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC).
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

The devices described in this section span frequencies from dc to RF. Low frequency devices are the 755N and 755P modular logarithmic amplifiers, which provide an output voltage proportional to the logarithm or antilogarithm of the input voltage for signals from dc to well under 1MHz.

For RF applications, the AD9521, an ac monolithic log amp, has 12dB of gain and is pin-compatible with the Plessy SL521 and SL1521. Several AD9521s can be cascaded to form a logarithmic strip with gains of 90dB and more for frequencies typically from 7 to 250MHz.

For higher levels of integration, the AD640, a monolithic demodulating log amp, has five 10 dB stages, each with a 350MHz small-signal bandwidth. The AD640 features an overall dc to 120MHz bandwidth along with a built-in attenuator and on-chip temperature compensation, as well as calibrated slope and intercept. Two AD640s can be cascaded for dynamic ranges as large as 95dB, depending on bandwidth.

LOGS AND LOG RATIOS

In the *logarithmic* mode, the ideal output equation is

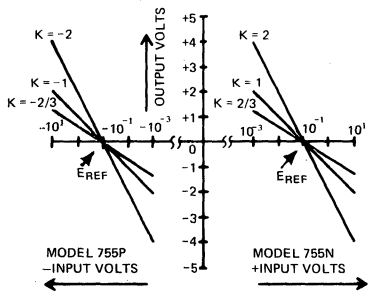
$$E_o = -K \log_{10} \left\{ \frac{I_{in}}{I_{ref}} \right\}$$

E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin programmable to be either 1V, 2V or 2/3V, or externally adjustable to any value $\geq$2/3V; in the model 757 log-ratio amplifier, K may be either a preset value of 1V or an arbitrary value adjustable by an external resistance ratio.

I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA (E_{ref} = 0.1V) or externally adjusted; but model 757 is *log-ratio* amplifier, in which both I_{in} and I_{ref} (or E_{in} and E_{ref}, using external scaling resistors) are input variables.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive*; "P" indicates that only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 759N, with K = +1V, would produce an output voltage, $E_o = -1V \log (100) = -2V$; on the other hand, −10V applied to model 759P with K = 1V, would produce an output voltage, $E_o = -(-1V) \log (100) = +2V$. The figure shows, in condensed form, the outputs of P and N log amps, with differing K values, for both voltage and current inputs, plotted on a semi-log scale.

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbence as the log ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multiterm products and ratios.



Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

ANTILOGS

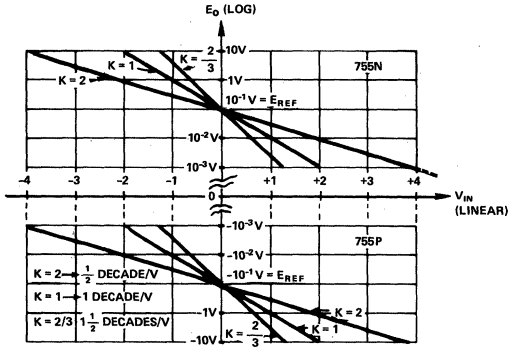
In the *antilogarithmic* (exponential) mode, the ideal output equation is

$$E_o = E_{ref} (10)^{-E_{in}/K}$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = −2V, if E_{in} = +4V, and E_{ref} = −0.1V, then $E_o = -0.1V \cdot 10^{-4/-2}$, or −10V. If E_{in} = −4V, then $E_o = -0.1V \cdot 10^{-(-4)/-2} = -1mV$. The figure on the next page shows in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.

***A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1,000 (3 decades), the output would change by 6V.**



Antilog Operator Response Curves, Semilog Scale

$E_O = E_{REF}\ 10^{V_{IN}/-K}$

LOG-ANTILOG AMPLIFIER PERFORMANCE

Considerable information regarding log- and antilog-amplifier circuit design, performance, selection and applications is to be found in the *Nonlinear Circuits Handbook*[1]. Several salient points will be covered here, and specifications will be defined.

A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

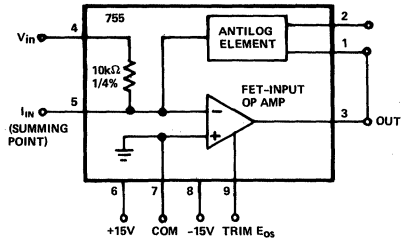
$$I = I_o(\epsilon^{qV/kT} - 1) \cong I_o\epsilon^{qV/kT}$$

and $V = (kT/q)\ \ln\ (I/I_o)$

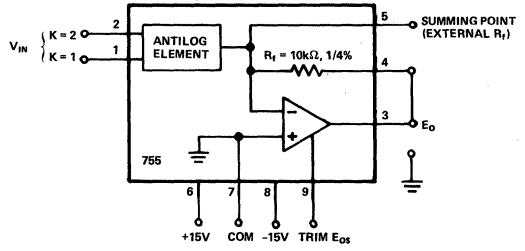
where I is the collector current, I_o is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11,605 K/V) is the ratio of charge of an electron to Boltzmann's constant and T is junction temperature in kelvins. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_o's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q)\ \ln\ (I_{in}/I_o) - (kT/q)\ \ln\ (I_{ref}/I_o)\\ &= (kT/q)(\ln\ I_{in} - \ln\ I_{ref}) + (kT/q)(\ln\ I_o - \ln\ I_o)\\ &= (kT/q)\ \ln\ (I_{in}/I_{ref})\end{aligned}$$

[1]***Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 796, Norwood, MA 02062**



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)



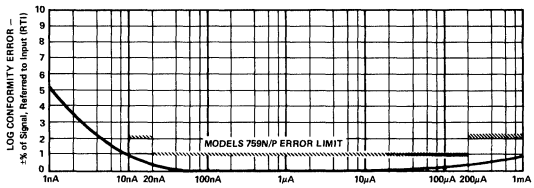
b) Log/Antilog Amplifier Connected in the Exponential Mode

The temperature dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade, (kT/q) ln10 at room temperature, to 1V/decade.

Errors are introduced by the offset current of the amplifier (and the offset voltage) for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog coordinates. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA. A plot of log conformity error for model 759 is shown on the following page.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at whatever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output}\\ &= 1V\cdot\log\ (1.01\ I/I_{ref}) - 1V\cdot\log\ (I/I_{ref})\\ &= 1V\cdot\log\ 1.01 = 0.0043V = 4.3mV\end{aligned}$$



Log Conformity Error for Models 759N and 759P

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

%ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17	5.7
3.0	13	26	8.6
4.0	17	34	11
5.0	21	42	14
10.0	41	83	28

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1μA tend to be roughly comparable. However, below 1μA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction – step changes in the direction of increasing current are responded to more quickly than step decreases of current.

DEFINITIONS OF SPECIFICATIONS

Log-Conformity Error: When the parameters have been adjusted to compensate for offset, scale-factor and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Offset Voltage (E_{os}) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current-logging operations, with high-impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V_{in}. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In antilog operation, E_{os} appears at the output as an essentially constant voltage; its percentage effect on error is greatest for small outputs.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator or simply by adding a constant bias at the output's destination.

Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

WIDEBAND (AC) LOGARITHMIC AMPLIFIERS

Amplifiers in the class of the AD9521 are essentially *limiting amplifiers*, providing high gain for small signals and low gain for large signals. They accept high-frequency ac signals (7MHz to 250MHz) and provide two amplified outputs: a radio-frequency output (voltage) and a nonlinearly detected output (current). The amplification characteristic (current output vs. rf input) on a semilog scale is S-shaped, starting with zero slope, increasing to a linear slope, then soft-saturating (with a slight overshoot).

They are used in *strips*, or cascades, of *n* (for example, 6 to 9) stages, with the rf output of one unit becoming the input of the next, thus multiplying their gains. The nonlinearly detected (or *video*) outputs are connected together for current summation.

The resulting output-vs.-input characteristic (semilog scale) is S-shaped, with a lengthy log-linear region whose extent depends on the number of stages (about 12dB per device). Once an amplifier saturates, its contribution to the summation is fixed; thus, the maximum output for large signals is *n* times the output of one device. The maximum dynamic range has been realized when the number of stages, *n*, is such that the input-stage noise alone produces full output from the last stage.

The AD640 provides a higher level of integration than the AD9521, being a completely calibrated system with a 50dB dynamic range. The AD640 uses a successive detection scheme that produces a current proportional to the logarithm of the input voltage. The AD640 consists of five detector/limited stages, each having a small-signal voltage gain of 10dB and a 3dB bandwidth of 350MHz. Two AD640s can be cascaded for dynamic ranges as large as 95dB, depending on bandwidth.

DC Coupled Demodulating 120MHz Logarithmic Amplifier

AD640

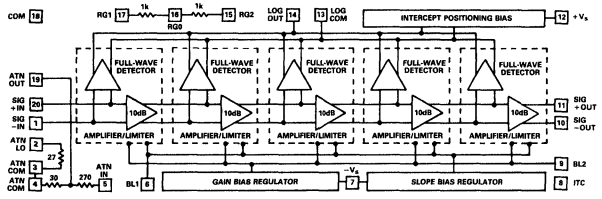
FEATURES

Complete, Fully Calibrated Monolithic System
Five Stages, Each Having 10dB Gain, 350MHz BW
Direct Coupled Fully Differential Signal Path
Logarithmic Slope, Intercept and AC Response are Stable Over Full Military Temperature Range
Dual Polarity Current Outputs Scaled 1mA/Decade
Voltage Slope Options (1V/Decade, 100mV/dB, etc.)
Low Power Operation (Typically 220mW at ±5V)
Low Cost Plastic Packages Also Available

APPLICATIONS

Radar, Sonar, Ultrasonic and Audio Systems
Precision Instrumentation from DC to 120MHz
Power Measurement with Absolute Calibration
Wide Range High Accuracy Signal Compression
Alternative to Discrete and Hybrid IF Strips
Replaces Several Discrete Log Amp ICs

AD640 BLOCK DIAGRAM



7

PRODUCT DESCRIPTION

The AD640 is a complete monolithic logarithmic amplifier. A single AD640 provides up to 50dB of dynamic range for frequencies from dc to 120MHz. Two AD640s in cascade can provide up to 95dB of dynamic range at reduced bandwidth. The AD640 uses a successive detection scheme to provide an output current proportional to the logarithm of the input voltage. It is laser calibrated to close tolerances and maintains high accuracy over the full military temperature range using supply voltages from ±4.5V to ±7.5V.

The AD640 comprises five cascaded dc coupled amplifier/limiter stages, each having a small signal voltage gain of 10dB and a −3dB bandwidth of 350MHz. Each stage has an associated full-wave detector, whose output current depends on the absolute value of its input voltage. The five outputs are summed to provide the video output (when low pass filtered) scaled at 1mA per decade (50μA per dB). On chip resistors can be used to convert this output current to a voltage with several convenient slope options. A balanced signal output at +50dB (referred to input) is provided to operate AD640s in cascade.

The logarithmic response is absolutely calibrated to within ±1dB for dc or square wave inputs from ±0.75mV to ±200mV, with an intercept (logarithmic offset) at 1mV dc. An integral X10 attenuator provides an alternative input range of ±7.5mV to ±2V dc. Scaling is also guaranteed for sinusoidal inputs.

The AD640B is specified for the industrial temperature range of −40°C to +85°C and the AD640T, available processed to MIL-STD-883B, for the military range of −55°C to +125°C. Both are available in 20-pin side brazed ceramic DIPs or leadless chip carriers (LCC). The AD640J is specified for the commercial temperature range of 0 to +70°C, and is available in both 20-pin plastic DIP (N) and PLCC (P) packages.

PRODUCT HIGHLIGHTS

1. Absolute calibration of a wideband logarithmic amplifier is unique. The AD640 is a high accuracy measurement device, not simply a logarithmic building block.
2. Advanced design results in unprecedented stability over the full military temperature range.
3. The fully differential signal path greatly reduces the risk of instability due to inadequate power supply decoupling and shared ground connections, a serious problem with commonly used unbalanced designs.
4. Differential interfaces also ensure that the appropriate ground connection can be chosen for each signal port. They further increase versatility and simplify applications. The signal input impedance is ~500kΩ in shunt with ~2pF.
5. The dc coupled signal path eliminates the need for numerous interstage coupling capacitors and simplifies logarithmic conversion of subsonic signals.
6. The low input offset voltage of 50μV (200μV max) ensures good accuracy for low level dc inputs.
7. Thermal recovery "tails," which can obscure the response when a small signal immediately follows a high level input, have been minimized by special attention to design details.
8. The noise spectral density of $2nV/\sqrt{Hz}$ results in a noise floor of ~23μV rms (−80dBm) at a bandwidth of 100MHz. The dynamic range using cascaded AD640s can be extended to 95dB by the inclusion of a simple filter between the two devices.

SPECIFICATIONS

DC SPECIFICATIONS (V_S = ±5V, T_A = +25°C, unless otherwise specified)

Model		AD640J			AD640B			AD640T			
Transfer Function[1]		$I_{OUT}=I_Y$ LOG $\lvert V_{IN}/V_X\rvert$ for V_{IN} = ±0.75mV to ±200mV dc									
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
SIGNAL INPUTS (Pins 1, 20)											
Input Resistance	Differential		500			500			500		kΩ
Input Offset Voltage	Differential		50	**500**		50	**200**		50	**200**	μV
vs. Temperature			0.8			0.8			0.8		μV/°C
Over Temperature	T_{min} to T_{max}									**300**	μV
vs. Supply			2			2			2		μV/V
Input Bias Current			7	25		7	25		7	25	μA
Input Bias Offset			1			1			1		μA
Common Mode Range		−2		+0.3	−2		+0.3	−2		+0.3	V
INPUT ATTENUATOR (Pins 2, 3, 4, 5 & 19)											
Attenuation[2]	Pin 5 to Pin 19		20			20			20		dB
Input Resistance	Pins 5 to 3/4		300			300			300		Ω
SIGNAL OUTPUT (Pins 10, 11)											
Small Signal Gain[4]			50			50			50		dB
Peak Differential Output[5]			±180			±180			±180		mV
Output Resistance	Either Pin to COM		75			75			75		Ω
Quiescent Output Voltage	Either Pin to COM		−90			−90			−90		mV
LOGARITHMIC OUTPUT[6] (Pin 14)											
Voltage Compliance Range		−0.3		$+V_S-1$	−0.3		$+V_S-1$	−0.3		$+V_S-1$	V
Slope Current, I_Y		**0.95**	1.00	**1.05**	**0.98**	1.00	**1.02**	**0.98**	1.00	**1.02**	mA
Accuracy vs. Temperature			0.002			0.002			0.002		%/°C
	T_{min} to T_{max}							**0.98**		**1.02**	mA
Accuracy vs. Supply	$\pm V_S$=4.5V to 7.5V		0.08	**1.0**		0.08	**0.4**		0.08	**0.4**	%/V
Intercept Voltage[7], V_X		**0.85**	1.00	**1.15**	**0.95**	1.00	**1.05**	**0.95**	1.00	**1.05**	mV
vs. Temperature			0.5			0.5			0.5		μV/°C
Over Temperature	T_{min} to T_{max}							**0.90**		**1.10**	mV
vs. Supply	$\pm V_S$=4.5V to 7.5V		2			2			2		μV/V
Logarithmic Offset (Alt. Definition of V_X)		−61.5	−60.0	−58.7	−60.5	−60.0	−59.5	−60.5	−60.0	−59.5	dBV
vs. Temperature			0.004			0.004			0.004		dB/°C
Over Temperature	T_{min} to T_{max}							−60.9		−59.1	dB
vs. Supply	$\pm V_S$=4.5V to 7.5V		0.017			0.017			0.017		dB/V
Intercept Voltage Using Attenuator		**8.25**	10.0	**11.75**	**9.0**	10.0	**11.0**	**9.0**	10.0	**11.0**	mV
Zero Signal Output Current[3]			−0.2			−0.2			−0.2		mA
ITC Disabled	Pin 8 to COM		−0.27			−0.27			−0.27		mA
Maximum Output Current			2.3			2.3			2.3		mA
APPLICATIONS RESISTORS (Pins 15, 16, 17)			1.000		**0.995**	1.000	**1.005**	**0.995**	1.000	**1.005**	kΩ
DC LINEARITY V_{IN} = ±1mV to ±100mV			0.35	1.2		0.35	**0.6**		0.35	**0.6**	dB
TOTAL ABSOLUTE DC ACCURACY											
V_{IN} = ±1mV to ±100mV[8]			0.55	2		0.55	**0.9**		0.55	**0.9**	dB
Over Temperature	T_{min} to T_{max}			3			1.7			1.8	dB
Over Supply Range	$\pm V_S$=4.5V to 7.5V			2			**1.0**			**1.0**	dB
V_{IN} = ±0.75mV to ±200mV			1.0	3		1.0	**2.0**		1.0	**2.0**	dB
Using Attenuator											
V_{IN} = ±10mV to ±1V			0.4	2.5		0.4	1.5		0.4	1.5	dB
Over Temperature	T_{min} to T_{max}		0.6	3		0.6	**2.0**		0.6	**2.0**	dB
V_{IN} = ±7.5mV to 2V			1.2	3.5		1.2	2.5		1.2	2.5	dB
POWER REQUIREMENTS											
Voltage Supply Range		±4.5		±7.5	±4.5		±7.5	±4.5		±7.5	V
Quiescent Current[9]											
$+V_S$ (Pin 12)	T_{min} to T_{max}		9	15		9	15		9	15	mA
$-V_S$ (Pin 7)	T_{min} to T_{max}		35	60		35	**60**		35	**60**	mA

AC SPECIFICATIONS (V_S=±5V, T_A=+25°C, unless otherwise specified)

Model / Parameter	Conditions	AD640J Min	AD640J Typ	AD640J Max	AD640B Min	AD640B Typ	AD640B Max	AD640T Min	AD640T Typ	AD640T Max	Units
SIGNAL INPUT (Pins 1, 20)											
Input Capacitance	Either Pin to COM		2			2			2		pF
Noise Spectral Density	1kHz to 10MHz		2			2			2		nV/√Hz
Tangential Sensitivity	BW=100MHz		−72			−72			−72		dBm
3dB BANDWIDTH											
Each Stage			350			350			350		MHz
All Five Stages	Pins 1 & 20 to 10 & 11		145			145			145		MHz
LOGARITHMIC OUTPUTS[6]											
Slope Current, I_Y											
f<=1MHz		0.96	1.0	1.04	0.98	1.0	1.02	0.98	1.0	1.02	mA
f=30MHz		0.88	0.94	1.00	0.91	0.94	0.97	0.91	0.94	0.97	mA
f=60MHz		0.82	0.90	0.98	0.86	0.90	0.94	0.86	0.90	0.94	mA
f=90MHz			0.88			0.88			0.88		mA
f=120MHz			0.85			0.85			0.85		mA
Intercept, Dual AD640s[10,11]											
f<=1MHz		−90.6	−88.6	−86.6	−89.6	−88.6	−87.6	−89.6	−88.6	−87.6	dBm
f=30MHz			−87.6			−87.6			−87.6		dBm
f=60MHz			−86.3			−86.3			−86.3		dBm
f=90MHz			−83.9			−83.9			−83.9		dBm
f=120MHz			−80.3			−80.3			−80.3		dBm
AC LINEARITY											
−40dBm to −2dBm[12]	f=1MHz		0.5	2.0		0.5	1.0		0.5	1.0	dB
−35dBm to −10dBm[12]	f=1MHz		0.25	1.0		0.25	0.5		0.25	0.5	dB
−75dBm to 0dBm[10]	f=1MHz		0.75	3.0		0.75	1.5		0.75	1.5	dB
−70dBm to −10dBm[10]	f=1MHz		0.5	2.0		0.5	1.0		0.5	1.0	dB
−75dBm to +15dBm[13]	f=10kHz		0.5	3.0		0.5	1.5		0.5	1.5	dB
PACKAGE OPTIONS[14]											
20-Pin Ceramic DIP Package (D)						AD640BD			AD640TD		
20-Pin Leadless Ceramic Chip Carrier (E)						AD640BE			AD640TE		
20-Pin Plastic DIP Package (N)			AD640JN								
20-Pin Plastic Leadless Chip Carrier (P)			AD640JP								
NUMBER OF TRANSISTORS			155			155			155		

NOTES

[1]Logarithms to base 10 are used throughout. The response is independent of the sign of V_{IN}.

[2]Attenuation ratio trimmed to calibrate intercept to 10mV when in use. It has a temperature coefficient of +0.3%/°C.

[3]The zero-signal current is a function of temperature unless internal temperature compensation (ITC) pin is grounded.

[4]Overall gain is trimmed using a ±200μV square wave at 2kHz, corrected for the onset of compression.

[5]The fully limited signal output will appear to be a square wave; its amplitude is proportional to absolute temperature.

[6]Currents defined as flowing *into* Pin 14. See FUNDAMENTALS OF LOGARITHMIC CONVERSION for full explanation of scaling concepts. Slope is measured by linear regression over central region of transfer function.

[7]The logarithmic intercept in dBV (decibels relative to 1V) is defined as 20 LOG_{10} (V_X/1V).

[8]Operating in circuit of Figure 24 using ±0.1% accurate values for R_{LA} and R_{LB}. Includes slope and nonlinearity errors. Input offset errors also included for V_{IN} >3mV dc, and over the full input range in ac applications.

[9]Essentially independent of supply voltages.

[10]Using the circuit of Figure 27, using cascaded AD640s and offset nulling. Input is sinusoidal, 0dBm in 50Ω=223mV rms.

[11]For a sinusoidal signal (see EFFECT OF WAVEFORM ON INTERCEPT). Pin 8 on second AD640 must be grounded to ensure temperature stability of intercept for dual AD640 system.

[12]Using the circuit of Figure 24, using single AD640 and offset nulling. Input is sinusoidal, 0dBm in 50Ω=223mV rms.

[13]Using the circuit of Figure 32, using cascaded AD640s and attenuator. Square wave input.

[14]See Section 20 for package outline information.

All min and max specifications are guaranteed, but only those in **boldface** are 100% tested on all production units. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

THERMAL CHARACTERISTICS

	θ_{JC} (°C/W)	θ_{JA} (°C/W)
20-Pin Ceramic DIP Package (D-20)	25	85
20-Pin Leadless Ceramic Chip Carrier (E-20A)	25	85
20-Pin Plastic DIP Package (N-20)	24	61
20-Pin Plastic Leadless Chip Carrier (P-20A)	28	75

Typical DC Performance

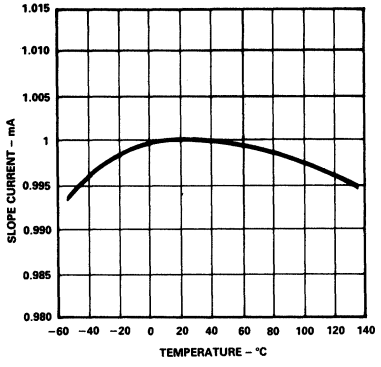


Figure 1. Slope Current, I_Y, vs. Temperature

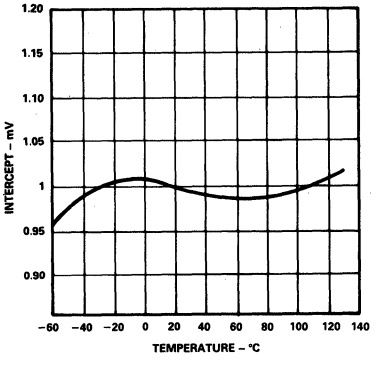


Figure 2. Intercept Voltage, V_X, vs. Temperature

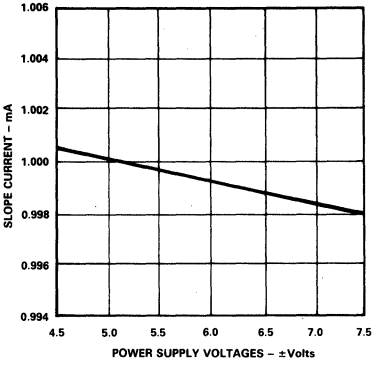


Figure 3. Slope Current, I_Y, vs. Supply Voltages

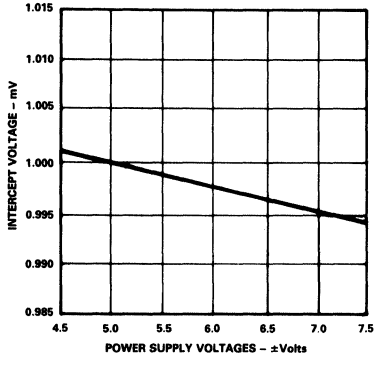


Figure 4. Intercept Voltage, V_X, vs. Supply Voltages

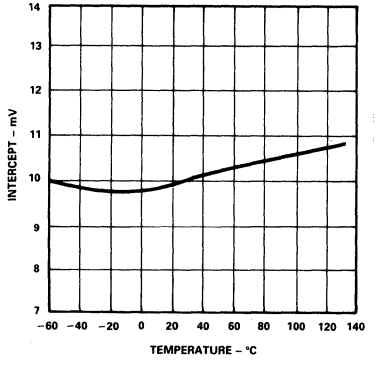


Figure 5. Intercept Voltage (Using Attenuator) vs. Temperature

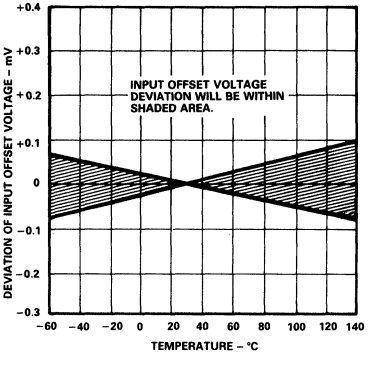


Figure 6. Input Offset Voltage Deviation vs. Temperature

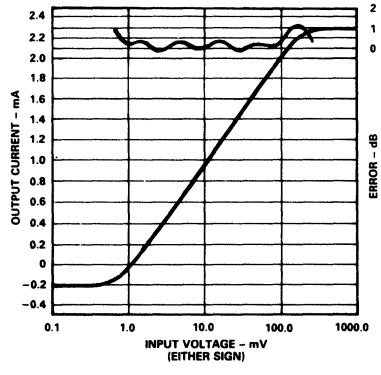


Figure 7. DC Logarithmic Transfer Function and Error Curve for Single AD640

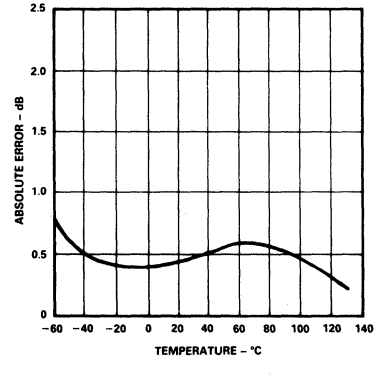


Figure 8. Absolute Error vs. Temperature, $V_{IN} = \pm 1mV$ to $\pm 100mV$

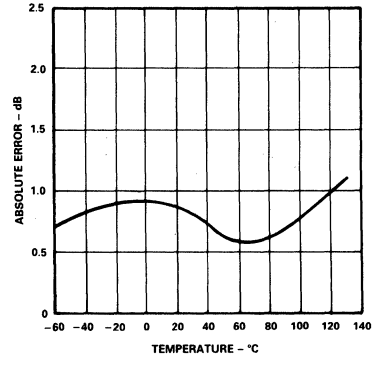


Figure 9. Absolute Error vs. Temperature, Using Attenuator. $V_{IN} = \pm 10mV$ to $\pm 1V$, Pin 8 Grounded to Disable ITC Bias

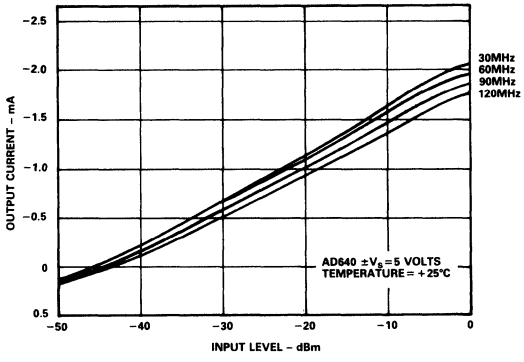


Figure 10. AC Response at 30MHz, 60MHz, 90MHz and 120MHz, vs. dBm Input (Sinusoidal Input)

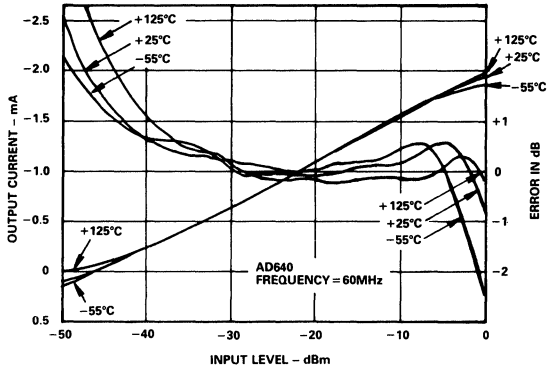


Figure 11. Logarithmic Response and Linearity at 60MHz, T_A for $T_A = -55°C$, $+25°C$, $+125°C$

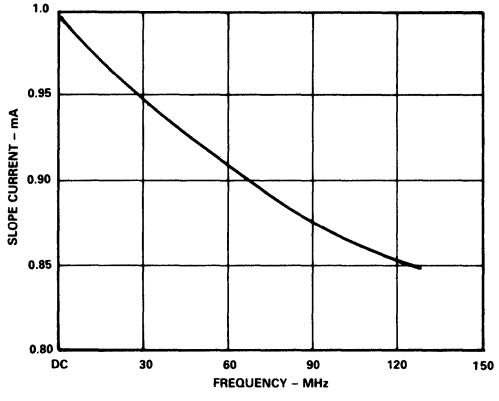


Figure 12. Slope Current, I_Y, vs. Input Frequency

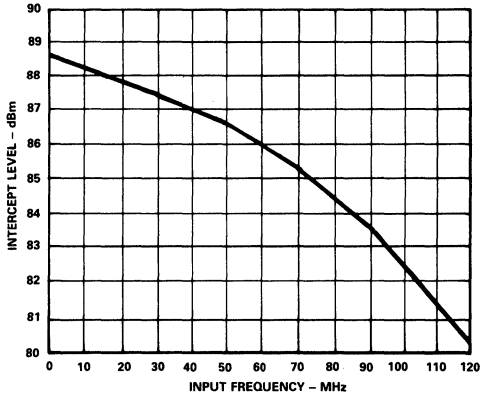


Figure 13. Intercept Level (dBm) vs. Frequency (Cascaded AD640s – Sinusoidal Input)

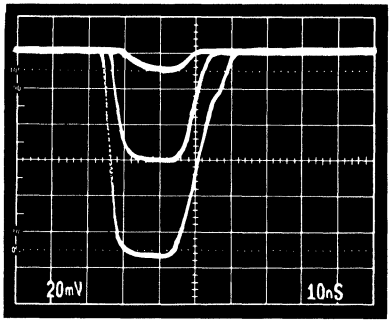


Figure 14. Baseband Pulse Response of Single AD640, Inputs of 1mV, 10mV and 100mV

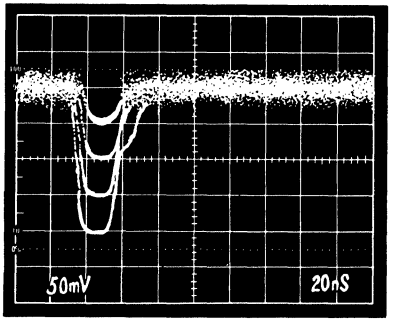


Figure 15. Baseband Pulse Response of Cascaded AD640s, at Inputs of 0.2mV, 2mV, 20mV and 200mV

CIRCUIT DESCRIPTION

The AD640 uses five cascaded limiting amplifiers to approximate a logarithmic response to an input signal of wide dynamic range and wide bandwidth. This type of logarithmic amplifier has traditionally been assembled from several small scale ICs and numerous external components. The performance of these semidiscrete circuits is often unsatisfactory. In particular, the logarithmic slope and intercept (see FUNDAMENTALS OF LOGARITHMIC CONVERSION) are usually not very stable in the presence of supply and temperature variations even after laborious and expensive individual calibration. The AD640 employs high precision analog circuit techniques to ensure stability of scaling over wide variations in supply voltage and temperature. Laser trimming, using ac stimuli and operating conditions similar to those encountered in practice, provides fully calibrated logarithmic conversion.

Each of the amplifier/limiter stages in the AD640 has a small signal voltage gain of 10dB (×3.162) and a −3dB bandwidth of 350MHz. Fully differential direct coupling is used throughout. This eliminates the many interstage coupling capacitors usually required in ac applications, and simplifies low frequency signal processing, for example, in audio and sonar systems. The AD640 is intended for use in demodulating applications. Each stage incorporates a detector (a full wave transconductance rectifier) whose output current depends on the absolute value of its input voltage.

Figure 16 is a simplified schematic of one stage of the AD640. All transistors in the basic cell operate at near zero collector to base voltage and low bias currents, resulting in low levels of thermally induced distortion. These arise when power shifts from one set of transistors to another during large input signals. Rapid recovery is essential when a small signal immediately follows a large one. This low power operation also contributes significantly to the excellent long term calibration stability of the AD640.

The complete AD640, shown in Figure 17, includes two bias regulators. One determines the small signal gain of the amplifier stages; the other determines the logarithmic slope. These bias regulators maintain a high degree of stability in the resulting function by compensating for potentially large uncertainties in transistor parameters, temperature and supply voltages. A third biasing block is used to accurately control the logarithmic intercept.

By summing the signals at the output of the detectors, a good approximation to a logarithmic transfer function can be achieved. The lower the stage gain, the more accurate the

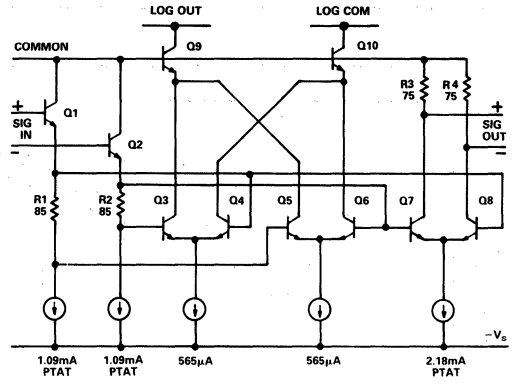


Figure 16. Simplified Schematic of a Single AD640 Stage

approximation, but more stages are then needed to cover a given dynamic range. The choice of 10dB results in a theoretical periodic deviation or ripple in the transfer function of ±0.15dB from the ideal response when the input is either a dc voltage or a square wave. The *slope* of the transfer function is unaffected by the input waveform; however, the intercept and ripple are waveform dependent (see EFFECT OF WAVEFORM ON INTERCEPT). The input will usually be an amplitude modulated sinusoidal carrier. In these circumstances the output is a fluctuating current at *twice* the carrier frequency (because of the full wave detection) whose average value is extracted by an external low pass filter, which recovers a logarithmic measure of the baseband signal.

Circuit Operation

With reference to Figure 16, the transconductance pair Q7, Q8 and load resistors R3 and R4 form a limiting amplifier having a small signal gain of 10dB, set by the tail current of nominally 2.18mA at 27°C. This current is basically proportional to absolute temperature (PTAT) but includes additional current to compensate for finite beta and junction resistance. The limiting output voltage is ±180mV at 27°C and is PTAT. Emitter followers Q1 and Q2 raise the input resistance of the stage, provide level shifting to introduce collector bias for the gain stage and detectors, reduce offset drift by forming a thermally balanced quad with Q7 and Q8 and generate the detector biasing across resistors R1 and R2.

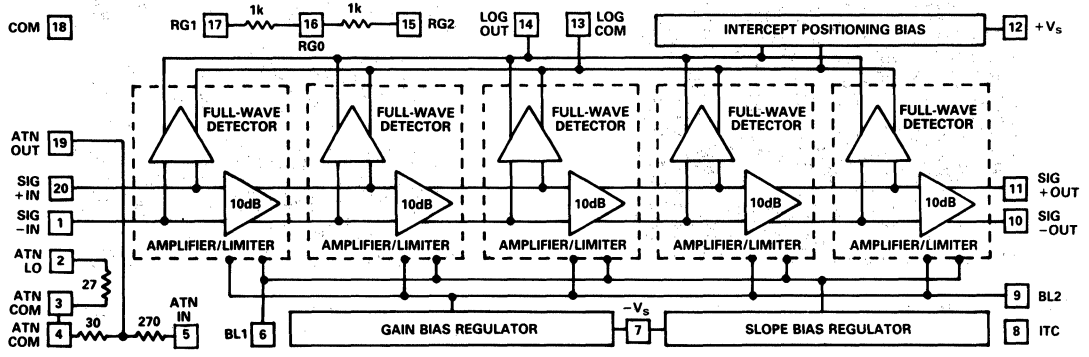


Figure 17. Block Diagram of the Complete AD640

Transistors Q3 through Q6 form the full wave detector, whose output is buffered by the cascodes Q9 and Q10. For zero input Q3 and Q5 conduct only a small amount (a total of about 32μA) of the 565μA tail currents supplied to pairs Q3–Q4 and Q5–Q6. This "pedestal" current flows in output cascode Q9 to the LOG OUT node (Pin 14). When driven to the peak output of the preceding stage, Q3 or Q5 (depending on signal polarity) conducts most of the tail current, and the output rises to 532μA. The LOG OUT current has thus changed by 500μA as the input has changed from zero to its maximum value. Since the detectors are spaced at 10dB intervals, the output increases by 50μA/dB, or 1mA per decade. This scaling parameter is trimmed to absolute accuracy using a 2kHz square wave. At frequencies near the system bandwidth, the slope is reduced due to the reduced output of the limiter stages, but it is still relatively insensitive to temperature variations so that a simple external slope adjustment can restore scaling accuracy.

The intercept position bias generator (Figure 17) removes the pedestal current from the summed detector outputs. It is adjusted during manufacture such that the output (flowing into Pin 14) is 1mA when a 2kHz square-wave input of exactly ±10mV is applied to the AD640. This places the dc intercept at precisely 1mV. The LOG COM output (Pin 13) is the complement of LOG OUT. It also has a 1mV intercept, but with an inverted slope of −1mA/decade. Because its pedestal is very large (equivalent to about 100dB), its intercept voltage is not guaranteed. The intercept positioning currents include a special internal temperature compensation (ITC) term which can be disabled by connecting Pin 8 to ground.

The logarithmic function of the AD640 is absolutely calibrated to within ±0.3dB (or ±15μA) for 2kHz square-wave inputs of ±1mV to ±100mV, and to within ±1dB between ±750μV and ±200mV. Figure 18 is a typical plot of the dc transfer function,

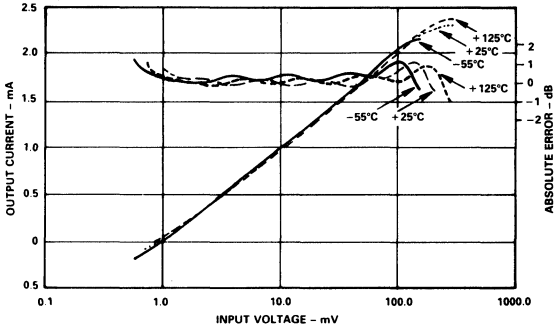


Figure 18. Logarithmic Output and Absolute Error vs. DC or Square Wave Input at T_A = −55°C, +25°C, Input Direct to Pins 1 and 20

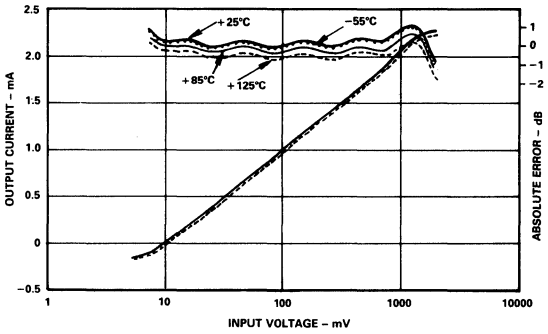


Figure 19. Logarithmic Output and Absolute Error vs. DC or Square Wave Input at T_A = −55°C, +25°C, +85°C and +125°C. Input via On-Chip Attenuator

showing the outputs at temperatures of −55°C, +25°C and +125°C. While the slope and intercept are seen to be little affected by temperature, there is a lateral shift in the end points of the "linear" region of the transfer function, which reduces the effective dynamic range. The cause of this shift is explained in FUNDAMENTALS OF LOGARITHMIC CONVERSION.

The on chip attenuator can be used to handle input levels 20dB higher, that is, from ±7.5mV to ±2V for dc or square wave inputs. It is specially designed to have a positive temperature coefficient and is trimmed to position the intercept at 10mV dc (or −24dBm for a sinusoidal input) over the full temperature range. When using the attenuator the internal bias compensation should be disabled by grounding Pin 8. Figure 19 shows the output at −55°C, +25°C, +85°C and +125°C for a single AD640 with the attenuator in use; the curves overlap almost perfectly, and the lateral shift in the transfer function does not occur. Therefore, the full dynamic range is available at all temperatures.

The output of the final limiter is available in differential form at Pins 10 and 11. The output impedance is 75Ω to ground from either pin. For most input levels, this output will appear to have roughly a square waveform. The signal path may be extended using these outputs (see OPERATION OF CASCADED AD640s). The logarithmic outputs from two or more AD640s can be directly summed with full accuracy.

A pair of 1kΩ applications resistors, RG1 and RG2 (Figure 17) are accessed via Pins 15, 16 and 17. These can be used to convert an output current to a voltage, with a slope of 1V/decade (using one resistor), 2V/decade (both resistors in series) or 0.5V/decade (both in parallel). Using all the resistors from two AD640s (for example, in a cascaded configuration) ten slope options from 0.25V to 4V/decade are available.

FUNDAMENTALS OF LOGARITHMIC CONVERSION

The conversion of a signal to its equivalent logarithmic value involves a *nonlinear* operation, the consequences of which can be very confusing if not fully understood. It is important to realize from the outset that many of the familiar concepts of linear circuits are of little relevance in this context. For example, the incremental gain of an ideal logarithmic converter approaches *infinity* as the input approaches zero. Further, an offset at the output of a linear amplifier is simply equivalent to an offset at the input, while in a logarithmic converter it is equivalent to a change of *amplitude* at the input – a very different relationship.

We assume a dc signal in the following discussion to simplify the concepts; ac behavior and the effect of input waveform on calibration are discussed later. A logarithmic converter having a voltage input V_{IN} and output V_{OUT} must satisfy a transfer function of the form

$$V_{OUT} = V_Y \text{ LOG } (V_{IN}/V_X) \qquad \text{Equation (1)}$$

where V_Y and V_X are fixed voltages which determine the *scaling* of the converter. The input is *divided* by a voltage because the argument of a logarithm has to be a simple ratio. The logarithm must be *multiplied* by a voltage to develop a voltage output. These operations are not, of course, carried out by explicit computational elements, but are inherent in the behavior of the converter. For stable operation, V_X and V_Y must be based on sound design criteria and rendered stable over wide temperature and supply voltage extremes. This aspect of RF logarithmic amplifier design has traditionally received little attention.

When $V_{IN} = V_X$, the logarithm is zero. V_X is, therefore, called the *Intercept Voltage*, because a graph of V_{OUT} versus LOG (V_{IN}) – ideally a straight line – crosses the horizontal axis at this point (see Figure 20). For the AD640, V_X is calibrated to exactly 1mV. The slope of the line is directly proportional to V_Y. Base 10 logarithms are used in this context to simplify the relationship to decibel values. For $V_{IN} = 10V_X$, the logarithm has a value of 1, so the output voltage is V_Y. At $V_{IN} = 100V_X$, the output is $2V_Y$, and so on. V_Y can therefore be viewed either as the *Slope Voltage* or as the *Volts per Decade Factor*.

The AD640 conforms to Equation (1) except that its two outputs are in the form of currents, rather than voltages:

$$I_{OUT} = I_Y \text{ LOG } (V_{IN}/V_X) \qquad \text{Equation (2)}$$

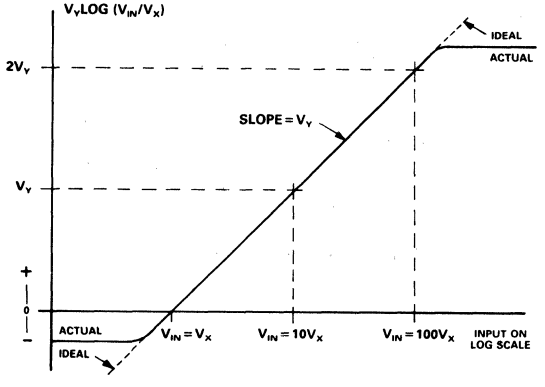


Figure 20. Basic DC Transfer Function of the AD640

I_Y, the *Slope Current*, is 1mA. The current output can readily be converted to a voltage with a slope of 1V/decade, for example, using one of the 1kΩ resistors provided for this purpose, in conjunction with an op amp, as shown in Figure 21.

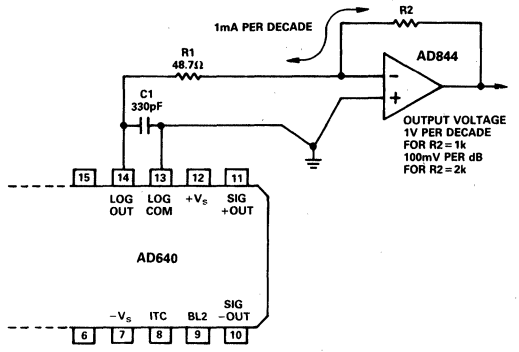


Figure 21. Using an External Op Amp to Convert the AD640 Output Current to a Buffered Voltage Output

Intercept Stabilization

Internally, the intercept voltage is a fraction of the thermal voltage kT/q, that is, $V_X = V_{XO}T/T_O$, where V_{XO} is the value of V_X at a reference temperature T_O. So the uncorrected transfer function has the form

$$I_{OUT} = I_Y \text{ LOG } (V_{IN} \, T_O/V_{XO}T) \qquad \text{Equation (3)}$$

Now, if the amplitude of the signal input V_{IN} could somehow be rendered PTAT, the intercept would be stable with temperature, since the temperature dependence in both the numerator and denominator of the logarithmic argument would cancel. This is what is *actually* achieved by interposing the on-chip attenuator, which has the necessary temperature dependence to cause the input to the first stage to vary in proportion to absolute temperature. *The end limits of the dynamic range are now totally independent of temperature.* Consequently, this is the preferred method of intercept stabilization for applications where the input signal is sufficiently large.

When the attenuator is *not* used, the PTAT variation in V_X will result in the intercept being temperature dependent. Near 300K (27°C) it will vary by 20LOG (301/300) dB/°C, about 0.03dB/°C. Unless corrected, the whole output function would drift up or down by this amount with changes in temperature. In the AD640 a temperature compensating current I_YLOG(T/T_O) is added to the output. This effectively maintains a constant intercept V_{XO}. This correction is active in the default state (Pin 8 open circuited). When using the attenuator, Pin 8 should be grounded, which disables the compensation current. The drift term needs to be compensated only once; when the outputs of two AD640s are summed, Pin 8 should be grounded on at least one of the two devices (both if the attenuator is used).

Conversion Range

Practical logarithmic converters have an upper and lower limit on the input, beyond which errors increase rapidly. The upper limit occurs when the *first* stage in the chain is driven into limiting. Above this, no further increase in the output can occur and the transfer function flattens off. The lower limit arises because a finite number of stages provide finite gain, and therefore at low signal levels the system becomes a simple linear amplifier.

Note that this lower limit is *not* determined by the intercept voltage, V_X; it can occur either above or below V_X, depending on the design. When using two AD640s in cascade, input offset voltage and wideband noise are the major limitations to low level accuracy. Offset can be eliminated in various ways. Noise can only be reduced by lowering the system bandwidth, using a filter between the two devices.

EFFECT OF WAVEFORM ON INTERCEPT

The absolute value response of the AD640 allows inputs of either polarity to be accepted. Thus, the logarithmic output in response to an amplitude-symmetric square wave is a steady value. For a sinusoidal input the fluctuating output current will usually be low pass filtered to extract the baseband signal. The unfiltered output is at *twice* the carrier frequency, simplifying the design of this filter when the video bandwidth must be maximized. The averaged output depends on waveform in a roughly analogous way to waveform dependence of rms value. The effect is to change the apparent intercept voltage. The intercept voltage appears to be doubled for a sinusoidal input, that is, the averaged output in response to a sine wave of *amplitude* (not rms value) of 20mV would be the same as for a dc or square wave input of 10mV. Other waveforms will result in different intercept factors. An amplitude-symmetric-rectangular waveform has the same intercept as a dc input, while the average of a baseband unipolar pulse can be determined by multiplying the response to a dc input of the same amplitude by the duty cycle. It is important to understand that in responding to pulsed RF signals it is the waveform of the *carrier* (usually sinusoidal) *not* the modulation envelope, that determines the effective intercept voltage. Table I shows the effective intercept and resulting decibel offset for commonly occurring waveforms. The input waveform does *not* affect the slope of the transfer function. Figure 22 shows the *absolute* deviation from the ideal response of cascaded AD640s for three common waveforms at input levels from −80dBV to −10dBV. The measured sine wave and triwave responses are 6dB and 8.7dB, respectively, below the square wave response – in agreement with theory.

Input Waveform	Peak or rms	Intercept Factor	Error (Relative to a dc Input)
Square Wave	Either	1	0.00dB
Sine Wave	Peak	2	−6.02dB
Sine Wave	rms	$1.414(\sqrt{2})$	−3.01dB
Triwave	Peak	2.718 (e)	−8.68dB
Triwave	rms	$1.569 (e/\sqrt{3})$	−3.91dB
Gaussian Noise	rms	1.887	−5.52dB

Table I

Logarithmic Conformance and Waveform

The waveform also affects the ripple, or *periodic* deviation from an ideal logarithmic response. The ripple is greatest for dc or square wave inputs because every value of the input voltage maps to a single location on the transfer function and thus traces out the full nonlinearities in the logarithmic response.

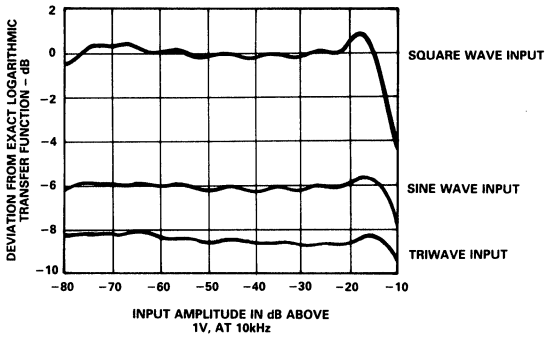


Figure 22. Deviation from Exact Logarithmic Transfer Function for Two Cascaded AD640s, Showing Effect of Waveform on Calibration and Linearity

By contrast, a general time varying signal has a continuum of values within each cycle of its waveform. The averaged output is thereby "smoothed" because the periodic deviations away from the ideal response, as the waveform "sweeps over" the transfer function, tend to cancel. This smoothing effect is greatest for a triwave input, as demonstrated in Figure 22.

The accuracy at *low signal inputs* is also waveform dependent. The detectors are not perfect absolute value circuits, having a sharp "corner" near zero; in fact they become parabolic at low levels and behave as if there were a dead zone. Consequently, the output tends to be higher than ideal. When there are enough stages in the system, as when two AD640s are connected in cascade, most detectors will be adequately loaded due to the high overall gain, but a single AD640 does not have sufficient gain to maintain high accuracy for low level sine wave or triwave inputs. Figure 23 shows the absolute deviation from calibration for the same three waveforms for a single AD640. For inputs between −10dBV and −40dBV the vertical displacement of the traces for the various waveforms remains in agreement with the predicted dependence, but significant calibration errors arise at low signal levels.

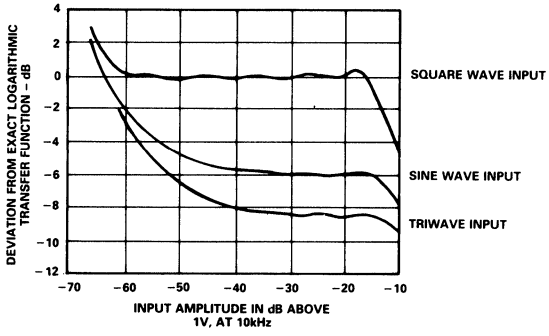


Figure 23. Deviation from Exact Logarithmic Transfer Function for a Single AD640; Compare Low Level Response with That of Figure 22

SIGNAL MAGNITUDE

The AD640 is a *calibrated* device. It is, therefore, important to be clear in specifying the signal magnitude under all waveform conditions. For dc or square wave inputs there is, of course, no ambiguity. Bounded periodic signals, such as sinusoids and triwaves, can be specified in terms of their simple *amplitude* (peak value) or alternatively by their *rms value* (which is a measure of *power when the impedance is specified*). It is generally better to define this type of signal in terms of its amplitude because the AD640 response is a consequence of the input *voltage*, not power. However, provided that the appropriate value of intercept for a specific waveform is observed, rms measures may be used. Random waveforms can only be specified in terms of rms value because their peak value may be unbounded, as is the case for Gaussian noise. These must be treated on a case-by-case basis. The effective intercept given in Table I should be used for Gaussian noise inputs.

On the other hand, for bounded signals the amplitude can be expressed either in volts or dBV (decibels relative to 1V). For example, a sine wave or triwave of 1mV amplitude can also be defined as an input of −60dBV, one of 100mV amplitude as −20dBV, and so on. RMS value is usually expressed in dBm (decibels above 1mW) for a specified impedance level. *Throughout this data sheet we assume a 50Ω environment, the customary impedance level for high speed systems, when referring to signal powers in dBm.* Bearing in mind the above discussion of the effect of waveform on the intercept calibration of the AD640, it will be apparent that a sine wave at a power of, say, −10dBm will *not* produce the same output as a triwave or square wave of the same *power*. Thus, a sine wave at a power level of −10dBm has an rms value of 70.7mV or an amplitude of 100mV (that is, $\sqrt{2}$ times as large, the ratio of amplitude to rms value for a sine wave), while a triwave of the same power has an amplitude which is $\sqrt{3}$ or 1.73 times its rms value, or 122.5mV.

"Intercept" and "Logarithmic Offset"

If the signals are expressed in dBV, we can write the output current in a simpler form, as

$$I_{OUT} = 50\mu A\ (Input_{dBV} - X_{dBV}) \qquad \text{Equation (4)}$$

where $Input_{dBV}$ is the input voltage *amplitude* (not rms) in dBV and X_{dBV} is the appropriate value of the intercept (for a given waveform) in dBV. This form shows more clearly why the intercept is often referred to as the *logarithmic offset*. For dc or square wave inputs, V_X is 1mV so the numerical value of X_{dBV} is −60, and Equation (4) becomes

$$I_{OUT} = 50\mu A\ (Input_{dBV} + 60) \qquad \text{Equation (5)}$$

Alternatively, for a sinusoidal input measured in dBm (power in dB above 1mW in a 50Ω system) the output can be written

$$I_{OUT} = 50\mu A\ (Input_{dBm} + 44) \qquad \text{Equation (6)}$$

because the intercept for a sine wave expressed in volts rms is at 1.414mV (from Table I) or −44dBm.

OPERATION OF A SINGLE AD640

Figure 24 shows the basic connections for a single device, using 100Ω load resistors. Output A is a negative going voltage with a slope of −100mV per decade; output B is positive going with a slope of +100mV per decade. For applications where absolute calibration of the intercept is essential, the main output (from LOG OUT, Pin 14) should be used; the LOG COM output can then be grounded. To evaluate the demodulation response, a simple low pass output filter having a time constant of roughly 500μs (3dB corner of 320Hz) is provided by a 4.7μF (−20% +80%) ceramic capacitor (Erie type RPE117-Z5U-475-K50V) placed across the load. A DVM may be used to measure the averaged output in verification tests. The voltage compliance at Pins 13 and 14 extends from 0.3V below ground up to 1V below $+V_S$. Since the current into Pin 14 is from −0.2mA at zero signal to +2.3mA when fully limited (dc input of >300mV) the output never drops below −230mV. On the other hand, the current *out* of Pin 13 ranges from −0.2mA to +2.3mA, and if desired, a load resistor of up to 2kΩ can be used on this output; the slope would then be 2V per decade. Use of the LOG COM output in this way provides a numerically correct decibel reading on a DVM (+100mV=+1.00dB).

Board layout is very important. The AD640 has both high gain and wide bandwidth; therefore every signal path must be very carefully considered. A high quality ground plane is essential, but it should not be assumed that it behaves as an equipotential plane. Even though the application may only call for modest bandwidth, each of the three differential signal interface pairs (SIG IN, Pins 1 and 20, SIG OUT, Pins 10 and 11, and LOG, Pins 13 and 14) must have their own "starred" ground points to avoid oscillation at low signal levels (where the gain is highest).

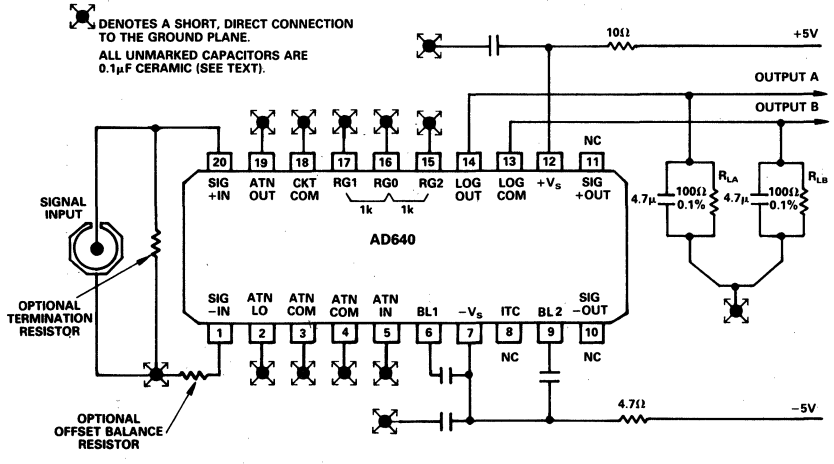


Figure 24. Connections for a Single AD640 to Verify Basic Performance

Unused pins (excluding Pins 8, 10 and 11) such as the attenuator and applications resistors should be grounded close to the package edge. BL1 (Pin 6) and BL2 (Pin 9) are internal bias lines a volt or two above the $-V_S$ node; access is provided solely for the addition of decoupling capacitors, which should be connected exactly as shown (not all of them connect to the ground). Use low impedance ceramic 0.1μF capacitors (for example, Erie RPE113-Z5U-105-K50V). Ferrite beads may be used instead of supply decoupling resistors in cases where the supply voltage is low.

Active Current-to-Voltage Conversion

The compliance at LOG OUT limits the available output voltage swing. The output of the AD640 may be converted to a larger, buffered output voltage by the addition of an operational amplifier connected as a current-to-voltage (transresistance) stage, as shown in Figure 21. Using a 2kΩ feedback resistor (R2) the 50μA/dB output at LOG OUT is converted to a voltage having a slope of +100mV/dB, that is, 2V per decade. This output ranges from roughly −0.4V for zero signal inputs to the AD640, crosses zero at a dc input of precisely +1mV (or −1mV) and is +4V for a dc input of 100mV. A passive prefilter, formed by R1 and C1, minimizes the high frequency energy conveyed to the op amp. The corner frequency is here shown as 10MHz. The AD844 is recommended for this application because of its excellent performance in transresistance modes. Its bandwidth of 35MHz (with the 2kΩ feedback resistor) will exceed the baseband response of the system in most applications. For lower bandwidth applications other op amps and multipole active filters may be substituted (see, for example, Figure 32 in the APPLICATIONS section).

Effect of Frequency on Calibration

The slope and intercept of the AD640 are calibrated during manufacture using a 2kHz square wave input. Calibration depends on the gain of each stage being 10dB. When the input frequency is an appreciable fraction of the 350MHz bandwidth of the amplifier stages, their gain becomes imprecise and the logarithmic slope and intercept are no longer fully calibrated. However, the AD640 can provide very stable operation at frequencies up to about one half the 3dB frequency of the amplifier stages. Figure 10 shows the averaged output current versus input level at 30MHz, 60MHz, 90MHz and 120MHz. Figure 11 shows the absolute error in the response at 60MHz and at temperatures of −55°C, +25°C and +125°C. Figure 12 shows the variation in the slope current, and Figure 13 shows the variation in the intercept level (sinusoidal input) versus frequency.

If absolute calibration is essential, or some other value of slope or intercept is required, there will usually be some point in the user's system at which an adjustment may be easily introduced. For example, the 5% slope deficit at 30MHz (see Figure 12) may be restored by a 5% increase in the value of the load resistor in the passive loading scheme shown in Figure 24, or by inserting a trim potentiometer of 100Ω in series with the feedback resistor in the scheme shown in Figure 21. The intercept can be adjusted by adding or subtracting a small current to the output. Since the slope current is 1mA/decade, a 50μA increment will move the intercept by 1dB. Note that any error in this current will invalidate the calibration of the AD640. For example, if one of the the 5V supplies were used with a resistor to generate the current to reposition the intercept by 20dB, a ±10% variation in this supply will cause a ±2dB error in the absolute calibration. Of course, slope calibration is unaffected.

Source Resistance and Input Offset

The bias currents at the signal inputs (Pins 1 and 20) are typically 7μA. These flow in the source resistances and generate input offset voltages which may limit the dynamic range because the AD640 is direct coupled and an offset is indistinguishable from a signal. It is good practice to keep the source resistances as low as possible and to equalize the resistance seen at each input. For example, if the source resistance to Pin 20 is 100Ω, a compensating resistor of 100Ω should be placed in series with Pin 1. The residual offset is then due to the *bias current offset*, which is typically under 1μA, causing an extra offset uncertainty of 100μV in this example. For a single AD640 this will rarely be troublesome, but in some applications it may need to be nulled out, along with the internal voltage offset component. This may be achieved by adding an adjustable voltage of up to ±250μV at the unused input. (Pins 1 and 20 may be interchanged with no change in function.)

In most applications there will be no need to use any offset adjustment. However, a general offset trimming circuit is shown in Figure 25. R_S is the source resistance of the signal. *Note: 50Ω rf sources may include a blocking capacitor and have no dc path to ground, or may be transformer coupled and have a near zero resistance to ground.* Determine whether the source resistance is zero, 25Ω or 50Ω (with the generator terminated in 50Ω) to find the correct value of bias compensating resistor, R_B, which should optimally be equal to R_S, unless $R_S = 0$, in which case use $R_B = 5\Omega$. The value of Ros should be set to $20{,}000R_B$ to provide a ±250μV trim range. To null the offset, set the source voltage to zero and use a DVM to observe the logarithmic output voltage. Recall that the LOG OUT current of the AD640 exhibits an *absolute value response* to the input voltage, so the offset potentiometer is adjusted to the point where the logarithmic output "turns around" (reaches a local maximum or minimum).

At high frequencies it may be desirable to insert a coupling capacitor and use a choke between Pin 20 and ground, when Pin 1 should be taken directly to ground. Alternatively, transformer coupling may be used. In these cases, there is no added offset due to bias currents. When using two dc coupled AD640s (overall gain 100,000), it is impractical to maintain a sufficiently low offset voltage using a manual nulling scheme. The section CASCADED OPERATION explains how the offset can be automatically nulled to submicrovolt levels by the use of a negative feedback network.

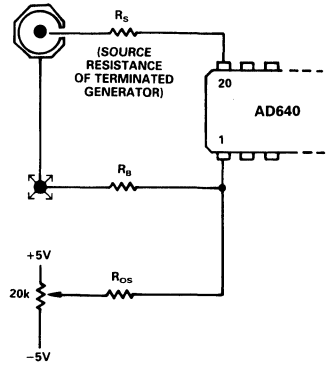


Figure 25. Optional Input Offset Voltage Nulling Circuit; See Text for Component Values

Using Higher Supply Voltages

The AD640 is calibrated using ±5V supplies. Scaling is very insensitive to the supply voltages (see dc SPECIFICATIONS) and higher supply voltages will not directly cause significant errors. However, the AD640 power dissipation must be kept below 500mW in the interest of reliability and long term stability. When using well regulated supply voltages above ±6V, the decoupling resistors shown in the application schematics can be increased to maintain ±5V at the IC. The resistor values are calculated using the specified maximum of 15mA current into the $+V_S$ terminal (Pin 12) and a maximum of 60mA into the $-V_S$ terminal (Pin 7). For example, when using ±9V supplies, a resistor of (9V-5V)/15mA, about 261Ω, should be included in the $+V_S$ lead to each AD640, and (9V–5V)/60mA, about 64.9Ω, in each $-V_S$ lead. Of course, asymmetric supplies may be dealt with in a similar way.

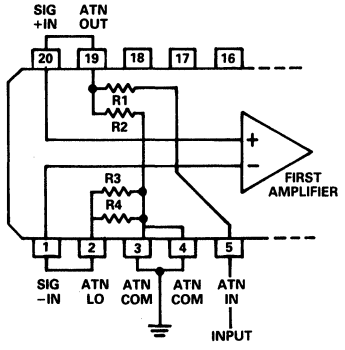


Figure 26. Details of the Input Attenuator

Using the Attenuator

In applications where the signal amplitude is sufficient, the on-chip attenuator should be used because it provides a temperature independent dynamic range (compare Figures 18 and 19). Figure 26 shows this attenuator in more detail. R1 is a thin film resistor of nominally 270Ω and low temperature coefficient (TC). It is trimmed to calibrate the intercept to 10mV dc (or −24dBm for sinusoidal inputs), that is, to an attenuation of nominally 20dBs at 27°C. R2 has a nominal value of 30Ω and has a high positive TC, such that the overall attenuation factor is 0.33%/°C at 27°C. This results in a transmission factor that is proportional to absolute temperature, or PTAT. (See Intercept Stabilization for further explanation.) To improve the accuracy of the attenuator, the ATN COM nodes are bonded to both Pin 3 and Pin 4. *These should be connected directly to the "SIGNAL LOW" of the source* (for example, to the grounded side of the signal connector, as shown in Figure 32) not to an arbitrary point on the ground plane.

R4 is identical to R2, and in shunt with R3 (270Ω thin film) forms a 27Ω resistor with the same TC as the output resistance of the attenuator. By connecting Pin 1 to ATN LOW (Pin 2) this resistance minimizes the offset caused by bias currents. The offset nulling scheme shown in Figure 25 may still be used, with the external resistor R_B omitted and $R_{OS} = 500k\Omega$. Offset stability is improved because the compensating voltage introduced at Pin 20 is now PTAT. Drifts of under 1μV/°C (referred to Pins 1 and 20) can be maintained using the attenuator.

It may occasionally be desirable to attenuate the signal even further. For example, the source may have a full scale value of ±10V, and since the basic range of the AD640 extends only to ±200mV dc, an attenuation factor of ×50 might be chosen. This may be achieved either by using an independent external attenuator or more simply by adding a resistor in series with ATN IN (Pin 5). In the latter case the resistor must be trimmed to calibrate the intercept, since the input resistance at Pin 5 is not guaranteed. A fixed resistor of 1kΩ in series with a 500Ω variable resistor calibrate to an intercept of 50mV (or −26dBV) for dc or square wave inputs and provide a ±10V input range. The intercept stability will be degraded to about 0.003dB/°C.

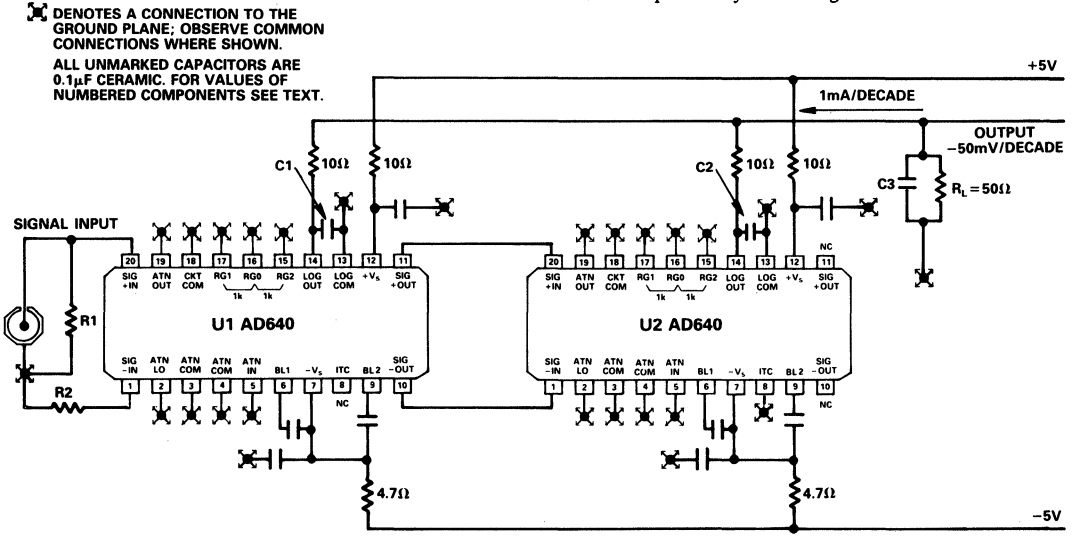


Figure 27. Basic Connections for Cascaded AD640s

OPERATION OF CASCADED AD640s

Frequently, the dynamic range of the input will be 50dB or more. AD640s can be cascaded, as shown in Figure 27. The balanced signal output from U1 becomes the input to U2. Resistors are included in series with each LOG OUT pin and capacitors C1 and C2 are placed *directly between Pins 13 and 14* to provide a local path for the RF current at these output pairs. C1 through C3 are chosen to provide the required low pass corner in conjunction with the load RL. Board layout and grounding disciplines are critically important at the high gain (X100,000) and bandwidth (~150MHz) of this system.

The intercept voltage is calculated as follows. First, note that if its LOG OUT is disconnected, U1 simply inserts 50dB of gain ahead of U2. This would lower the intercept by 50dB, to −110dBV for square wave calibration. With the LOG OUT of U1 added in, there is a finite zero signal current which slightly shifts the intercept. With the intercept temperature compensation on U1 disabled this zero signal output is −270μA (see DC SPECIFICATIONS) equivalent to a 5.4dB upward shift in the intercept, since the slope is 50μA/dB. Thus, the intercept is at −104.6dBV (−88.6dBm for 50Ω sine calibration). ITC may be disabled by grounding Pin 8 of either U1 or U2.

Cascaded AD640s can be used in dc applications, but input offset voltage will limit the dynamic range. The dc intercept is 6μV. *The offset should not be confused with the intercept*, which is found by *extrapolating* the transfer function from its central "log linear" region. This can be understood by referring to Equation (1) and noting that an input offset is simply additive to the value of V_{IN} in the numerator of the logarithmic argument; it does not affect the denominator (or intercept) V_X. In dc coupled applications of wide dynamic range, special precautions must be taken to null the input offset and minimize drift due to input bias offset. It is recommended that the input attenuator be used, providing a practical input range of −74dBV (±200μV dc) to +6dBV (±2V dc) when nulled using the adjustment circuit shown in Figure 25.

Eliminating the Effect of First Stage Offset

Usually, the input signal will be sinusoidal and U1 and U2 can be ac coupled. Figure 28a shows a low resistance choke at the input of U2 which shorts the dc output of U1 while preserving the hf response. Coupling capacitors may be inserted (Figure 28b) in which case two chokes are used to provide bias paths for U2. These chokes must exhibit high impedance over the operating frequency range.

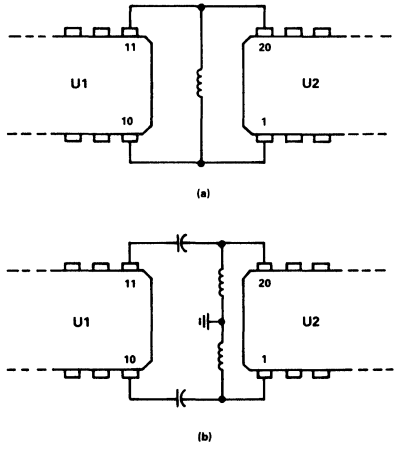


Figure 28. Two Methods for AC Coupling AD640s

Alternatively, the input offset can be nulled by a negative feedback network from the SIG OUT nodes of U2 to the SIG IN nodes of U1, as shown in Figure 29. The low pass response of the feedback path transforms to a closed-loop high pass response. The high gain (×100,000) of the signal path results in a commensurate reduction in the effective time constant of this network. For example, to achieve a high pass corner of 100kHz, the low pass corner must be at 1Hz.

In fact, it is somewhat more complicated than this. When the ac input sufficiently exceeds that of the offset, the feedback becomes ineffective and the response becomes essentially dc coupled. Even for quite modest inputs the last stage will be limiting and the output (Pins 10 and 11) of U2 will be a square wave of about ±180mV amplitude, dwelling approximately equal times at its two limit values, and thus having a net average value near zero. *Only when the input is very small does the high pass behavior of this nulling loop become apparent.* Consequently, the low pass time constant can usually be reduced considerably without serious performance degradation.

The resistor values are chosen such that the dc feedback is adequate to null the worst case input offset, say, 500μV. There must be some resistance at Pins 1 and 20 across which the offset compensation voltage is developed. The values shown in the figure assume that we wish to terminate a 50Ω source at Pin 20. The 50Ω resistor at Pin 1 is essential, both to minimize offsets due to bias current mismatch and because the outputs at Pins 10 and 11 can only swing negatively (from ground to −180mV) whereas we need to cater for input offsets of either polarity.

For a sine input of 1μV amplitude (−120dBV) and in the absence of offset, the differential voltage at Pins 10 and 11 of U2 would be almost sinusoidal but 100,000 times larger, or 100mV. The last limiter in U2 would be entering saturation. A 1μV input offset added to this signal would put the last limiter well into saturation, and its output would then have a *different average value*, which is extracted by the low pass network and delivered back to the input. For larger signals, the output approaches a square wave for zero input offset and becomes rectangular when offset is present. The duty cycle modulation of this output now produces the nonzero average value. Assume a maximum required differential output of 100mV (after averaging in C1 and C2) as shown in Figure 29. R3 through R6 can now be chosen to provide ±500μV of correction range, and with these values the input offset is reduced by a factor of 500. Using 4.7μF capacitors, the time constant of the network is about 1.2ms, and its corner frequency is at 13.5Hz. The closed loop high pass corner (for small signals) is, therefore, at 1.35MHz.

Bandwidth/Dynamic Range Tradeoffs

The first stage noise of the AD640 is 2nV/$\sqrt{\text{Hz}}$ (short circuited input) and the full bandwidth of the cascaded ten stages is about 150MHz. Thus, the noise referred to the input is 24.5μV rms, or −79dBm, which would limit the dynamic range to 77dBs (−79dBm to −2dBm). In practice, the source resistances will also generate noise, and the full bandwidth dynamic range will be less than this.

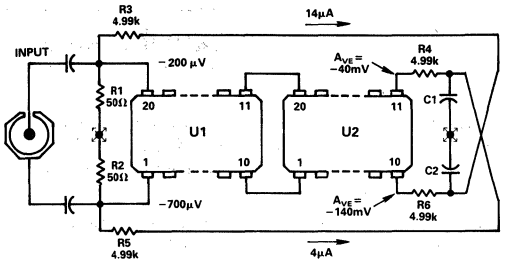


Figure 29. Feedback Offset Correction Network

A low pass filter between U1 and U2 can limit the noise bandwidth and extend the dynamic range. The simplest way to do this is by the addition of a pair of grounded capacitors at the signal outputs of U1 (shown as C1 and C2 in Figure 32). The −3dB frequency of the filter must be above the highest frequency to be handled by the converter; if not, nonlinearity in the transfer function will occur. This can be seen intuitively by noting that the system would then contract to a single AD640 at very high frequencies (when U2 has very little input). At intermediate frequencies, U2 will contribute less to the output than would be the case if there were no interstage attenuation, resulting in a kink in the transfer function.

More complex filtering may be considered. For example, if the signal has a fairly narrow bandwidth, the simple chokes shown in Figure 28 might be replaced by one or more parallel tuned circuits. Two separate tuned circuits or transformer coupling should be used to eliminate all undesirable hf common mode coupling between U1 and U2. The choice of Q for these circuits requires compromise. Frequency sensitive nonlinearities can arise at the edges of the band if the Q is set too high; if too low, the transmission of the signal from U1 to U2 will be affected even at the center frequency, again resulting in nonlinearity in the conversion response. In calculating the Q, note that the resistance from Pins 10 and 11 to ground is 75Ω. The input resistance at Pins 1 and 20 is very high, but the capacitances at these pins must also be factored into the total LCR circuit.

PRACTICAL APPLICATIONS

We show here two applications, using cascaded AD640s to achieve a wide dynamic range. As already mentioned, the use of a differential signal path and differential logarithmic outputs diminishes the risk of instability due to poor grounding. Nevertheless, it must be remembered that at high frequencies even very small lengths of wire, including the leads to capacitors, have significant impedance. The ground plane itself can also generate small but troublesome voltages due to circulating currents in a poor layout. A printed circuit evaluation board is available from Analog Devices (Part Number ADEB640) to facilitate the prototyping of an application using one or two AD640s, plus various external components.

At very low signal levels various effects can cause significant deviation from the ideal response, apart from the inherent nonlinearities of the transfer function already discussed. Note that *any spurious signal presented to the AD640s is demodulated and added to the output*. Thus, in the absence of thorough shielding, emissions from any radio transmitters or RFI from equipment operating in the locality will cause the output to appear too high. The only cure for this type of error is the use of very careful grounding and shielding techniques.

50MHz–150MHz Converter with 70dB Dynamic Range

Figure 30 shows a logarithmic converter using two AD640s which can provide at least 70dB of dynamic range, limited mostly by first stage noise. In this application, an rf choke (L1) prevents the transmission of dc offset from the first to the second AD640. One or two turns in a ferrite core will generally suffice for operation at frequencies above 30MHz. For example, one complete loop of 20 gauge wire through the two holes in a Fair-Rite type 2873002302 core provides an inductance of 5μH, which presents an impedance of 1.57kΩ at 50MHz. The shunting effect across the 150Ω differential impedance at the signal interface is thus fairly slight.

The signal source is optionally terminated by R1. To minimize the input offset voltage R2 should be chosen to match the dc resistance of the terminated source. (However, the offset voltage is not a critical consideration in this ac coupled application.)

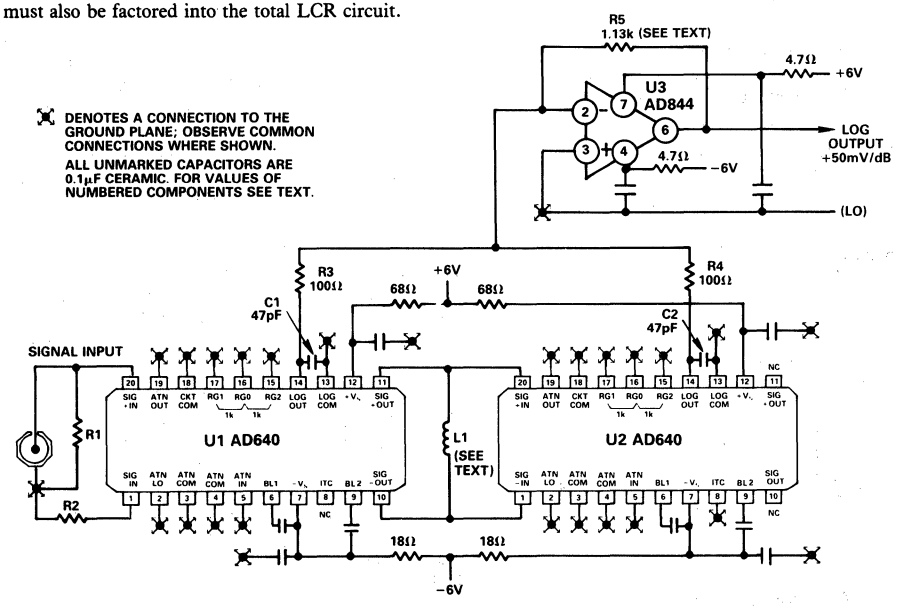


Figure 30. Complete 70dB Dynamic Range Converter for 50MHz–150MHz Operation

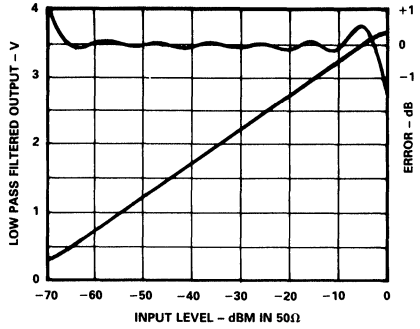


Figure 31. Logarithmic Output and Nonlinearity for Circuit of Figure 30, for a Sine Wave Input at f =80MHz

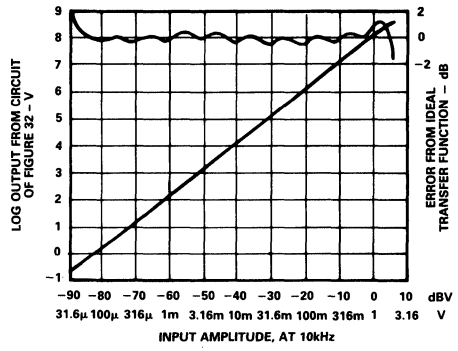


Figure 33. Logarithmic Output and Nonlinearity for Circuit of Figure 32, for a Square Wave Input at f= 10kHz

Note that all unused inputs are grounded; this improves the isolation from the outputs back to the inputs.

A transimpedance op amp (U3, AD844) converts the summed logarithmic output currents of U1 and U2 to a ground referenced voltage scaled 1V per decade. The resistor R5 is nominally 1kΩ but is increased slightly to compensate for the slope deficit at the operating frequency, which can be determined from Figure 12.

The inverting input of U3 forms a virtual ground, so that each logarithmic output of U1 and U2 is loaded by 100Ω (R3 or R4). These resistors in conjunction with capacitors C1 and C2 form independent low pass filters with a time constant of about 5ns. These capacitors should be connected directly across Pins 13 and 14, as shown, to prevent high frequency output currents from circulating in the ground plane. A second 5ns time constant is formed by feedback resistor R5 in conjunction with the transcapacitance of U3.

This filtering is adequate for input frequencies of 50MHz or above; more elaborate filtering can be devised for pulse applications requiring a faster rise time. In applications where only a long term measure of the input is needed, C1 and C2 can be increased and U3 can be replaced by a low speed op amp. Figure 31 shows typical performance of this converter.

10Hz–100kHz Converter with 95dB Dynamic Range

To increase the dynamic range it is necessary to reduce the bandwidth by the inclusion of a low pass filter at the signal interface between U1 and U2 (Figure 32). To provide operation down to low frequencies, dc coupling is used at the interface between AD640s and the input offset is nulled by a feedback circuit.

Using values of 0.02μF in the interstage filter formed by capacitors C1 and C2, the hf corner occurs at about 100kHz. U3 (AD712) forms a 4-pole 35Hz low pass filter. This provides operation to signal frequencies below 20Hz. The filter response is not critical, allowing the use of an electrolytic capacitor to form one of the poles.

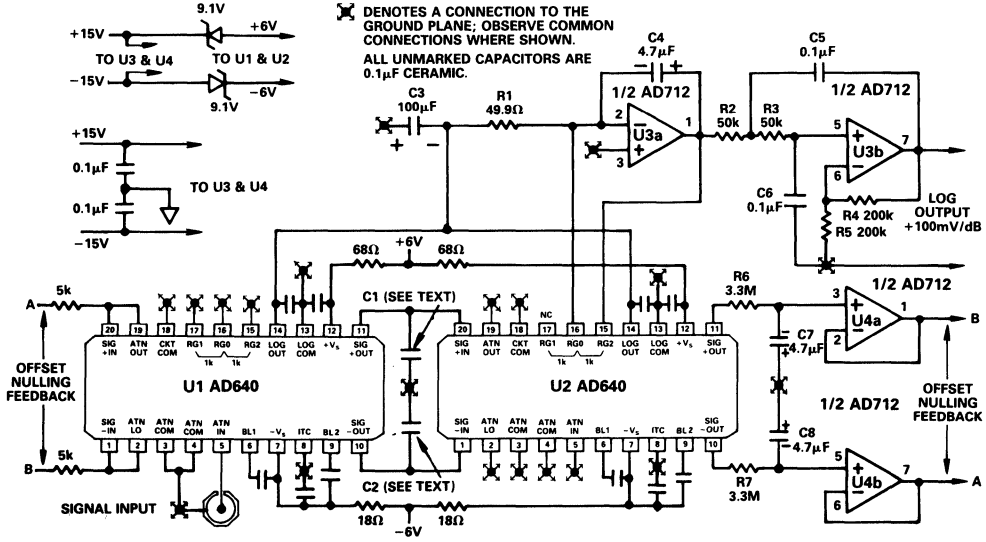


Figure 32. Complete 95dB Dynamic Range Converter

R1 is restricted to 50Ω by the compliance at Pin 14, so C3 needs to be large to form a 5ms time constant. A tantalum capacitor is used (note polarity). The output of U3a is scaled +1V per decade, and the X2 gain of U3b raises this to +2V per decade, or +100mV/dB. The differential offset at the output of U2 is low pass filtered by R6/C7 and R7/C8 and buffered by voltage followers U4a and U4b. The 16s open loop time constant translates to a closed loop high pass corner of 10Hz. (This high pass filter is only operative for very small inputs; see page 13.) Figure 33 shows the performance for square wave inputs. Since the attenuator is used, the upper end of the dynamic range now extends to +6dBV and the intercept is at −82dBV. The noise limited dynamic range is over 100dB, but in practice spurious signals at the input will determine the achievable range.

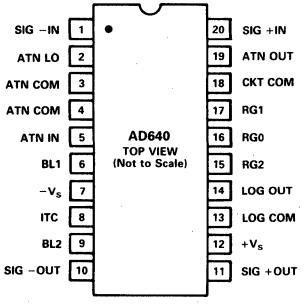
ABSOLUTE MAXIMUM RATINGS*

Supply Voltages . . . . . ±7.5V
Input Voltage (Pin 1 or Pin 20 to COM) . . . . −3V to +300mV
Attenuator Input Voltage (Pin 5 to Pin 3/4) . . . . . ±4V
Storage Temperature Range D, E . . . . . −65°C to +150°C
Storage Temperature Range N, P . . . . . −65°C to +125°C
Ambient Temperature Range, Rated Performance
Industrial, AD640B . . . . . −40°C to +85°C
Military, AD640T . . . . . −55°C to +125°C
Commercial, AD640J . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

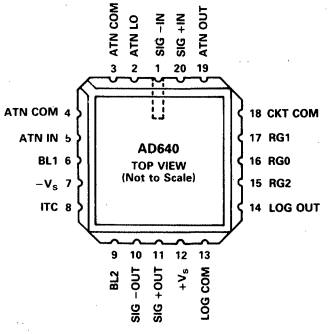
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.

CONNECTION DIAGRAMS

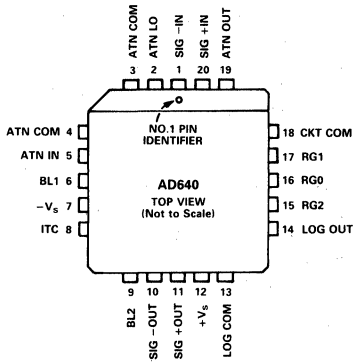
20-Pin Ceramic DIP (D) Package
20-Pin Plastic DIP (N) Package



20-Pin LCC (E) Package



20-Pin PLCC (P) Package



ANALOG DEVICES

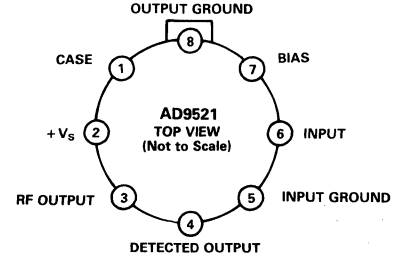
250MHz Wideband Logarithmic Amplifier

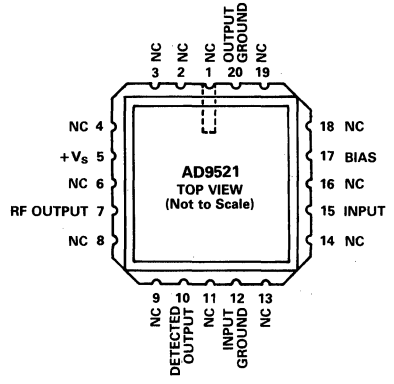
AD9521

FEATURES
250MHz Bandwidth
Monolithic Construction
Low Noise Figure 4.7dB
Excellent Detected Output Matching
Direct Replacement for SL521/SL1521

APPLICATIONS
Missile Guidance
Electronic Warfare (ECM, ECCM, ESM)
Miniaturized LOG Strips
Nuclear Instrumentation

PIN DESIGNATIONS





GENERAL DESCRIPTION

The AD9521 is a wideband amplifier stage with a logarithmic detected output. The high-performance bipolar process used to construct the AD9521 allows operation from 10MHz to 250MHz with minimal gain variation. The AD9521 is pin compatible with the SL521 and the SL1521.

The AD9521 is constructed in a well controlled monolithic process which provides very good gain tolerance (±1.5dB) over the full performance range. An added benefit of the high gain tolerance is a high degree of detected output current matching from device to device. The matching combined with the low 4dB noise figure allows the construction of 80dB to 90dB dynamic range LOG strips with better than ±1dB linearity.

The AD9521 is offered in two gain tolerance grades as both a commercial temperature range device, 0 to +70°C, and as an extended temperature range device, −55°C to +125°C. All grades are available packaged in 8-pin TO-99 metal cans with the military grades also available packaged in ceramic LCC.

ORDERING INFORMATION

Device	Detected Output Matching	Temperature Range	Description	Package Options*
AD9521JH	0.2mA	0 to +70°C	8-Pin Can, Industrial	H-08A
AD9521KH	0.1mA	0 to +70°C	8-Pin Can, Industrial	H-08A
AD9521SE	0.2mA	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD9521SH	0.2mA	−55°C to +125°C	8-Pin Can, Extended Temperature	H-08A
AD9521TE	0.1mA	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD9521TH	0.1mA	−55°C to +125°C	8-Pin Can, Extended Temperature	H-08A

*See Section 20 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$) . . . . . +9V
Differential Voltage Between Grounds 0.5V
Maximum Input Before Overload . . . . . 1.9V rms
Instantanious Voltage at the Detected Video Output 12V
RF Output Current 10mA
Power Dissipation 500mW

Operating Temperature Range[2]
AD9521JH/KH . . . . . 0 to +70°C
AD9521SE/SH/TE/TH . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −55°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = +6V; INPUT connected to BIAS pin; $R_S = 50\Omega$; $C_L \leq 8pF$, unless otherwise stated)

	Mil[3] Sub		Industrial Temp. Range 0 to +70°C						Military Temp. Range −55°C to +125°C						
			AD9521JH			AD9521KH			AD9521SE/SH			AD9521TE/TH			
Parameter	Group	Temp	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
AC PERFORMANCE															
Voltage Gain (f_{IN} = 30MHz)	7	+25°C	11.5	12.2	12.5	11.5	12.2	12.5	11.5	12.2	12.5	11.5	12.2	12.5	dB
	8	Full	11.0		13.0	11.0		13.0	11.0		13.0	11.0		13.0	dB
Voltage Gain (f_{IN} = 60MHz)	7	+25°C	12.0	12.8	13.0	12.0	12.8	13.0	12.0	12.8	13.0	12.0	12.8	13.0	dB
	8	Full	11.7		13.7	11.7		13.7	11.7		13.7	11.7		13.7	dB
Voltage Gain (f_{IN} = 120MHz)	7	+25°C	12.2	13.0	13.8	12.2	13.0	13.8	12.2	13.0	13.8	12.2	13.0	13.8	dB
	8	Full	11.5		14.5	11.5		14.5	11.5		14.5	11.5		14.5	dB
Voltage Gain (f_{IN} = 160MHz)	7	+25°C	12.7	13.4	14.2	12.7	13.4	14.2	12.7	13.4	14.2	12.7	13.4	14.2	dB
	8	Full	11.5		14.5	11.5		14.5	11.5		14.5	11.5		14.5	dB
Input Capacitance		+25°C		6			6			6			6		pF
Noise Figure[4]	12	+25°C		4.7	4.9		4.7	4.9		4.7	4.9		4.7	4.9	dB
Gain Variation vs. Temperature[5]		Full		0.67			0.67			0.67			0.67		dB
Gain Variation vs. Supply[6]	7, 8			0.74	1.15		0.74	1.15		0.74	1.15		0.74	1.15	dB/V
Frequency Response															
Upper Cutoff Frequency	7	+25°C	230	245		230	245		230	245		230	245		MHz
	8	Full	200			200			200			200			MHz
Lower Cutoff Frequency	7, 8	Full		7	10		7	10		7	10		7	10	MHz
DETECTED VIDEO OUTPUT															
Output Current @ 60MHz (Max)[7]	7	+25°	0.90	1.02	1.10	0.95	1.02	1.05	0.90	1.02	1.10	0.95	1.02	1.05	mA
	8	Full	0.80		1.20	0.85		1.15	0.80		1.20	0.85		1.15	mA
(80% Input Level)[8]	7	+25°C	0.70	0.82	0.90	0.75	0.82	0.85	0.70	0.82	0.90	0.75	0.82	0.85	mA
(No Input)[9]	7	+25°C		0.02	0.04		0.02	0.04		0.02	0.04		0.02	0.04	mA
Output Current @ 120MHz (Max)[7]	7	+25°C	0.51	0.70	0.90	0.62	0.70	0.85	0.51	0.70	0.90	0.62	0.70	0.85	mA
	8	Full	0.40		0.91	0.51		0.90	0.40		0.91	0.51		0.90	mA
(80% Input Level)[8]	7	+25°C	0.50	0.68	0.86	0.60	0.68	0.81	0.50	0.68	0.86	0.60	0.68	0.81	mA
(No Input)[9]	7	+25°C		0.02	0.04		0.02	0.04		0.02	0.04		0.02	0.04	mA
Detected Output Variation vs. Supply[6]	7	+25°C		28	30		28	30		28	30		28	30	%/V
Detected Output vs. Temperature[5]		Full		9			9			9			9		%
RF OUTPUT[5,7]															
Maximum RF Output Voltage		+25°C		1.6			1.6			1.6			1.6		V p-p
RF Output Propagation Delay		+25°C		1.4			1.4			1.4			1.4		ns
POWER SUPPLY[10]															
Supply Current (+6.0V)	1	+25°C		14.0	16.0		14.0	16.0		14.0	16.0		14.0	16.0	mA
	2, 3	Full			16.5			16.5			16.5			16.5	mA
Nominal Power Dissipation		+25°C		84			84			84			84		mW

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Typical thermal impedance . . .
AD9521 Metal Can θ_{JA} = 185°C/W; θ_{JC} = 50°C/W
AD9521 LCC θ_{JA} = 80°C/W; θ_{JC} = 50°C/W.
[3]Military subgroups apply to military qualified devices only.
[4]R_S = 450Ω; 60MHz.
[5]A_{IN} = 60MHz.
[6]Measured at ±5% of $+V_S$; A_{IN} = 60MHz.
[7]Input = 0.5V rms.
[8]Input = 0.09V rms.
[9]Input = 0.0V rms.
[10]Supply voltage should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

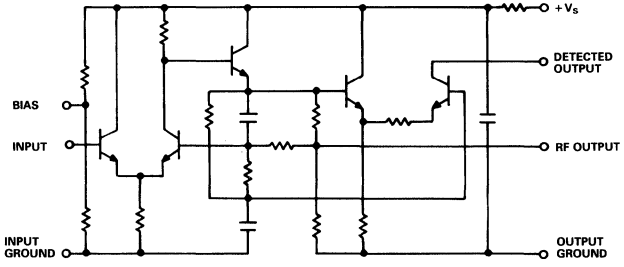
EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

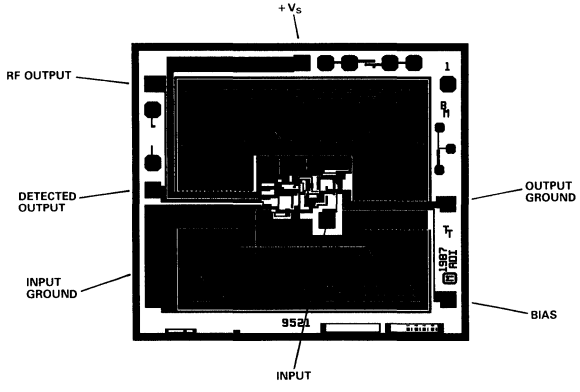
FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
CASE	– Case connection for the TO-99 metal can package only.
$+V_S$	– Positive supply terminal, nominally +6.0V.
RF OUTPUT	– The RF OUTPUT is used to drive subsequent LOG detection stages. The RF OUTPUT level is roughly +12dB above the IF signal strength at the input.
DETECTED OUTPUT	– The DETECTED OUTPUT provides a dc current logarithmicly proportional to the IF signal level at the input.
INPUT GROUND	– Isolated input ground connection. The input and output grounds should be connected together near the AD9521.
INPUT	– IF signal input.
BIAS	– The BIAS connection is tied to the INPUT pin to provide an adequate biasing level between ac coupled stages. The bias connection should be omitted between direct dc coupled stages.
OUTPUT GROUND	– Isolated output ground connection. The input and output grounds should be connected together near the AD9521.

SCHEMATIC

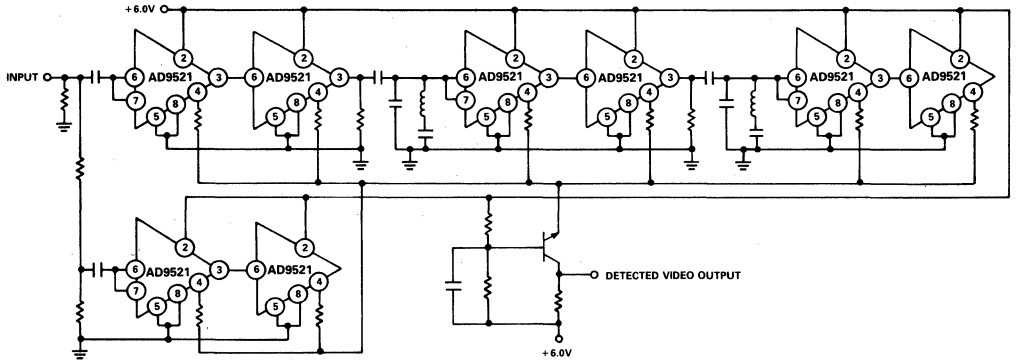


DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	86×97×15 (±2) mils
Pad Dimensions	4×4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding or 1mil Gold; Gold Ball Bonding

TYPICAL LOG STRIP CONFIGURATION



APPLICATIONS INFORMATION

The AD9521 is primarily designed for use in successive detection LOG strips. The application circuit above, illustrates the typical configuration for one such design with roughly 90dB of dynamic range. In operation the IF input signal level is successively amplified by each stage in the upper chain. The IF signal at each stage generates a detected output current. The detected output current from each stage is summed in the common base follower stage at the end of the strip.

The key to the circuit is the limiting quality of the AD9521 logarithmic detected output. As the IF signal at each stage drives the detected output into saturation, the output current ceases to increase. In operation, the combined gain of all of the previous stages drives the last stage into saturation first. Any further increase in signal level will not increase the detected output level of the last stage, but all of the previous stages will enter saturation one-by-one as the signal level increases.

The limiting factor to the number of stages that can be combined is the input noise level. When the gain of the entire strip is sufficient to drive the last stage into saturation on the input noise of the first stage alone, further extensions of the strip will not increase the dynamic input range.

There are, however, two methods of increasing the dynamic range of the LOG strip which include bandwidth reduction and parallel strip configurations. The dynamic range can be extended by 20dB or more by incorporating a parallel log strip with an attenuated input. The main strip functions as before, but the second strip, because of the attenuation, only contributes to the output for signals in excess of the main strip saturation level. The ultimate limitation is the maximum input signal level which the main strip will tolerate. Any further signal level increases could damage the input stage of the AD9521. This should not be a major problem since with this technique the dynamic range of the total strip can be as high as 100dB.

The dynamic range can also be increased by reducing the bandwidth of the strip itself. The noise voltage is directly proportional to the square root of the circuit bandwidth. This means that large operating bandwidths produce large amounts of noise which translates into limited dynamic range. The AD9521 is a particularly low-noise device, but even it can benefit from bandwidth reduction which has been incorporated into the circuit above. The two interstage filters limit the noise to a smaller region of frequencies and thereby allow the strip to be extended further.

Because of the high-frequency nature of the AD9521, several guidelines should be followed to insure optimum performance. The first is the use of an adequate low impedance ground plane. Just as important is the use of power supply decoupling capacitors to prevent signal feedthrough on the supply lines. Chip capacitors are highly recommended because of their reduced lead inductance. Sockets are not likely to produce the best results because of the interlead capacitance, but if they must be used, pin sockets are preferred.

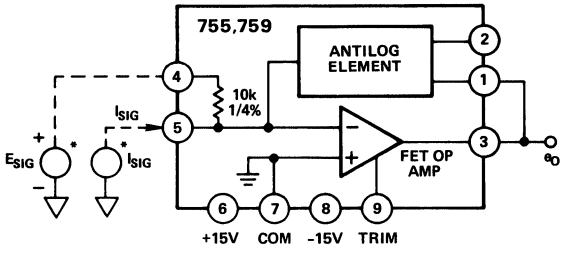
6-Decade, High Accuracy, Wideband Log, Antilog Amplifiers

755N/755P/759N/759P

FEATURES

- **High Accuracy: Models 755N, 755P**
- **Wideband: Models 759N, 759P**
- **Complete Log/Antilog Amplifiers: External Components Not Required**
- **Temperature-Compensated Internal Reference**
- **6 Decades Current Operation: 1nA to 1mA**
- **1% max Error: 1nA to 1mA (755)**
  20nA to 200μA (759)
- **4 Decades Voltage Operation: 1mV to 10V**
- **1% max Error: 1mV to 10V (755)**
  1mV to 2V (759)
- **Small Size: 1.1" X 1.1" X 0.4"**

755/759 FUNCTIONAL BLOCK DIAGRAM



*POSITIVE INPUT SIGNALS, AS SHOWN; USE 759N, 755P.
NEGATIVE INPUT SIGNALS, USE 759N, 755P.

7

GENERAL DESCRIPTION

The models 755N, 755P and 759N, 759P are low cost dc logarithmic amplifiers offering conformance to ideal log operation over 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). For high accuracy requirements, models 755N, 755P offer maximum nonconformity of 0.5%, from 10nA to 1mA, and 1mV to 1V. For wideband applications, the models 759N, 759P provide fast response (300kHz @ I_{SIG} = 10μA to 1mA) and feature maximum nonconformity of 1% from 20nA to 200μA, and 1mV to 2V. The models 755N and 759N compute the log of positive (+) input signals, while the models 755P, 759P compute the log of negative (–) signals.

Designed for ease of use, the models 755N/P and 759N/P are complete, temperature compensated log/antilog amplifiers packaged in a compact epoxy-encapsulated module. External components are not required for logging currents over the complete 6 decade range of 1μA to 1mA. Both the scale factor (K=2, 1, or 2/3 volt/decade) and log/antilog operation are selected by simple pin connection. In addition, both the internal 10μA reference current as well as the offset voltage may be externally adjusted to improve overall accuracy.

The models 755 and 759 are ideally suited as an alternative to in-house designs of OEM applications. Advanced design techniques and superior performance place the 755 and 759 ahead of competitive designs in terms of price, performance and package design.

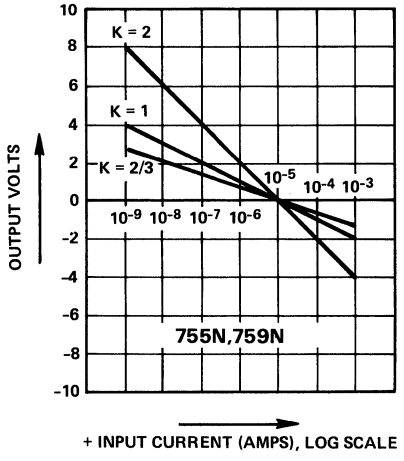


Figure 1. Transfer Function

APPLICATIONS

When connected in the current or voltage logging configuration, as shown in Figure 1, the models 755 and 759 may be used in several key applications. A plot of input current versus output voltage is also presented to illustrate the log amplifier's transfer characteristics.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	755N/P	759N/P
TRANSFER FUNCTIONS		
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$	•
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$	•
Antilog Mode	$e_O = E_{REF}\ 10^{-\left(\frac{E_{SIG}}{K}\right)}$	•
TRANSFER FUNCTION PARAMETERS		
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade	•
Error @ +25°C	±1% max	•
vs. Temperature (0 to +70°C)	±0.04%/°C max	•
Reference Voltage (E_{REF})[2]	0.1V	•
Error @ +25°C	±3% max	±4% max
vs. Temperature (0 to +70°C)	±0.1%/°C max	±0.05%/°C
Reference Current (I_{REF})[2]	10μA	•
Error @ +25°C	±3% max	•
vs. Temperature (0 to +70°C)	±0.1%/°C max	±0.05%/°C

MAXIMUM LOG CONFORMITY ERROR

I_{SIG} RANGE	E_{SIG} RANGE	RTI	RTO (K=1)	RTI	RTO (K=1)
1nA to 10nA	–	±1%	±4.3mV	±5%	±21mV
10nA to 20nA	–	±0.5%	±2.17mV	±2%	±8.64mV
20nA to 100μA	1mV to 1V	±0.5%	±2.17mV	±1%	±4.3mV
100μA to 200μA	1V to 2V	±1%	±4.3mV	±1%	±4.3mV
200μA to 1mA	2V to 10V	±1%	±4.3mV	±2%	±8.64mV

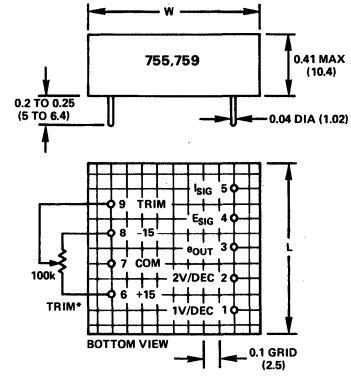
INPUT SPECIFICATIONS		
Current Signal Range		
Model 755N, 759N	+1nA to +1mA min	•
Model 755P, 759P	−1nA to −1mA min	•
Max Safe Input Current	±10mA max	•
Bias Current @ +25°C	(0, +) 10pA max	(0, +) 200pA max
vs. Temperature (0 to +70°C)	x2/+10°C	•
Voltage Signal Range (Log Mode)		
Model 755N, 759N	+1mV to +10V min	•
Model 755P, 759P	−1mV to −10V min	•
Voltage Signal Range, Antilog Mode Model 755N, 755P	$-2 \leqslant \frac{E_{SIG}}{K} \leqslant 2$	•
Offset Voltage @ +25°C (Adjustable to 0)	±400μV max	±2mV max
vs. Temperature (0 to +70°C)	±15μV/°C max	±10μV/°C
vs. Supply Voltage	±15μV/%	•
FREQUENCY RESPONSE, Sinewave		
Small Signal Bandwidth, −3dB		
I_{SIG} = 1nA	80Hz	250Hz
I_{SIG} = 1μA	10kHz	100kHz
I_{SIG} = 10μA	40kHz	200kHz
I_{SIG} = 1mA	100kHz	200kHz
RISE TIME		
Increasing Input Current		
10nA to 100nA	100μs	20μs
100nA to 1μA	7μs	3μs
1μA to 1mA	4μs	2.5μs
Decreasing Input Current		
1mA to 1μA	7μs	3μs
1μA to 100nA	30μs	10μs
100nA to 10nA	400μs	80μs
INPUT NOISE		
Voltage, 10Hz to 10kHz	2μV rms	10μV rms
Current, 10Hz to 10kHz	2pA rms	10pA rms
OUTPUT SPECIFICATIONS[3]		
Rated Output		
Voltage	±10V min	•
Current		
Log Mode	±5mA	•
Antilog Mode	±4mA	•
Resistance	0.5Ω	•
POWER SUPPLY[4]		
Rated Performance	±15Vdc	•
Operating	±(12 to 18)Vdc	•
Current, Quiescent	±7mA	±4mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	•
Operating	−25°C to +85°C	•
Storage	−55°C to +125°C	•
CASE SIZE[5] (W x L x H)	1.5" x 1.5" x 0.4" (38 x 38 x 10.4)	1.125" x 1.125" x 0.4" (29 x 29 x 10.4)

NOTES
[1] Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 or 2 (shorted together) for K = 2/3V/decade.
[2] Specification is + for models 755N, 759N; − for 755P, 759P.
[3] No damage due to any pin being shorted to ground.
[4] Recommended power supply, model 904, ±15V @ ±50mA output.
[5] Case size in inches (mm).

Specifications subject to change without notice.

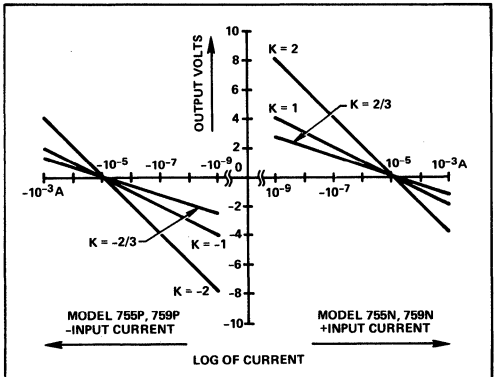
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

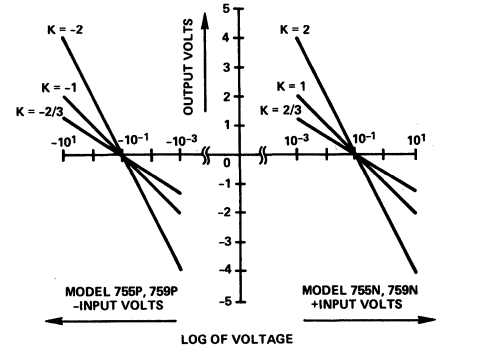


*Optional 100kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±0.4mV (755) or ±2mV (759) maximum.

MATING SOCKET AC1016



Plot of Output Voltage vs Input Current for Model 755 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Models 755, 759 Connected in the Log Mode

Figure 2. Transfer Curves

PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

$$e_{OUT} = 1V \log_{10} I_{SIG}/I_{REF}$$

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current, I_{REF}, the ratio being dimensionless. For this purpose a temperature compensated reference of 10μA is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

REFERRING ERRORS TO INPUT

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

$$e_{OUT} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01) \text{ which is equivalent to:}$$

$$e_{OUT} = \underbrace{1V \log_{10} (I_{SIG}/I_{REF})}_{\text{Initial Value}} \quad \underbrace{\pm 1V \log_{10} (1.01)}_{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of ±4.3mV. Conversely, a dc error at the output of ±4.3mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

	ERROR R.T.O.		
ERROR R.T.I.	K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.86mV	0.28mV
0.5	2.17	4.34	1.45
1.0	4.32	8.64	2.88
3.0	12.84	25.68	8.56
4.0	17.03	34.06	11.35
5.0	21.19	42.38	14.13
10.0	41.39	82.78	27.59

Table I. Converting Output Error in mV to Input Error in %

SOURCES OF ERROR

Log Conformity Error – Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated to taken into account. The best linearity performance for the models 755, 759 are obtained in the 5 decades from 10nA to 1mA. To obtain optimum performance, the input data should be scaled to this range.

Offset Voltage – The offset voltage, E_{os}, of models 755, 759 is the offset voltage of the internal FET amplifier. This voltage appears as a small dc offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

Bias Current – The bias current of models 755, 759 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nanoamp region. For this reason, the bias current for model 755 is 10pA, maximum, and 200pA maximum for model 759.

Reference Current – I_{REF} is the internally generated current source to which all input currents are compared. I_{REF} tolerance errors appear as a dc offset at the output. The specified value of I_{REF} is ±3% referred to the input, and, from Table I, corresponds to a dc offset of ±12.84mV for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage – E_{REF} is the effective internally generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation:
$E_{REF} = I_{REF} \times R_{IN}$, where R_{IN} is an internal 10kΩ, precision resistor. Virtually all tolerance in E_{REF} is due to I_{REF}. Consequently, variations in I_{REF} cause a shift in E_{REF}.

Scale Factor – Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

7

OPTIONAL EXTERNAL ADJUSTMENTS FOR LOG OPERATION

Trimming E_{OS} – The amplifier's offset voltage, E_{OS}, may be trimmed for improved accuracy with the models 755, 759 connected in its log circuit. To accomplish this, a 100kΩ, 10 turn pot is connected as shown in Figure 3. The input terminal, Pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{OUT} = -K \log_{10} E_{OS}/E_{REF}$$

To obtain an offset voltage of 100μV or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for models 755N, 759N, and -3V to -4V for models 755P, 759P.

For other values of K, the trim pot should be adjusted for an output of e_{OUT} = 3 x K to 4 x K where K is the scale factor.

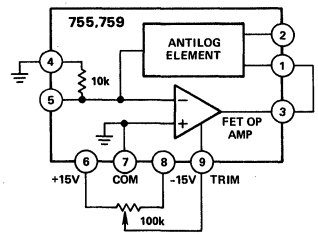


Figure 3. Trimming E_{OS} in Log Mode

Reference Current or Reference Voltage – The reference current or voltage of models 755, 759 may be shifted by injecting a constant current into the unused scale factor terminal (Pin 1 or Pin 2). The current injected will shift the reference one decade, in accordance with the expression: $I_I = 66\mu A \log 10\mu A/I_{REF}$ (755), $I_I = 330\mu A \log 10\mu A/I_{REF}$ (759), where I_I = current to be injected and I_{REF} = the desired reference current.

By changing I_{REF}, there is a corresponding change in E_{REF} since, $E_{REF} = I_{REF} \times R_{IN}$. An alternate method for rescaling E_{REF} is to connect an external R_{IN}, at the I_{IN} terminal (Pin 5) to supplant the 10kΩ supplied internally (leaving it unconnected). The expression for E_{REF} is then, $E_{REF} = R_{IN} I_{REF}$. Care must be taken to choose R_{IN} such that $(e_{SIG}$ max$)/R_{IN} \leq 1$mA.

Scale Factor (K) Adjustment – Scale factor may be increased from its nominal value by inserting a series resistor R_S between the output terminal, Pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

RANGE OF K	CONNECT SERIES R TO PIN	VALUE OF R_S	NOTE
2/3V to 1.01V	1	R x (K - 2/3)	use pins 1, 2
1.01V to 2.02V	1	R x (K - 1)	use pin 1
>2.02V	2	R x (K - 2)	use pin 2

R = 15kΩ (755); 3kΩ (759)

Table 2. Resistor Selection Chart for Shifting Scale Factor

ANTILOG OPERATION

The models 755 and 759 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} \qquad [-2 \leq e_{IN}/K \leq 2]$$

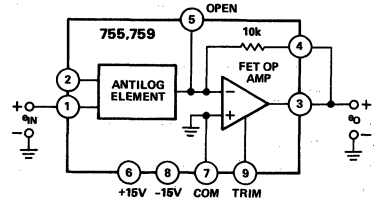


Figure 4. Functional Block Diagram

Principle of Operation – The antilog element converts the voltage input, appearing at terminal 1, to a current which is proportional to the antilog of the applied voltage. The current-to-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

A more complete expression for the antilog function is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} + E_{OS}$$

The terms K, E_{OS}, and E_{REF} are those described previously in the LOG section.

Offset Voltage (E_{OS}) Adjustment – Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to $e_{OUT}/100$. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external 100Ω resistor, and the jumper from Pin 1 to +15V. For 755P, 759P use the same procedure but connect Pin 1 to -15V.

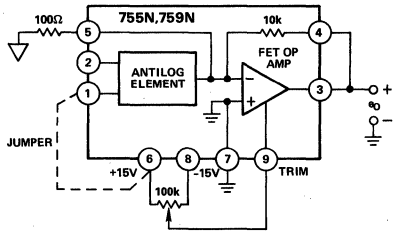


Figure 5. Trimming E_{OS} in Antilog Mode

Reference Voltage (E_{REF}) Adjustment – In antilog operation, the voltage reference appears as a multiplying constant. E_{REF} adjustment may be accomplished by connecting a resistor, R, from Pin 5 to Pin 3, in place of the internal 10kΩ. The value of R is determined by:

$$R = E_{REF} \text{ desired}/10^{-5} \text{ A}$$

Scale Factor (K) Adjustment – The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

$$R1/R_G = (1/K - 1) \text{ where K = desired scale factor}$$

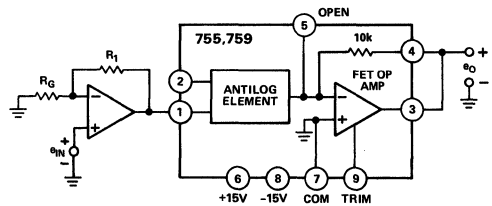


Figure 6. Method for Adjusting K<2/3V

ANALOG DEVICES

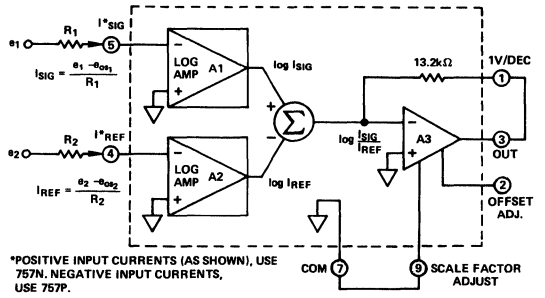
6-Decade, High Accuracy, Log Ratio Amplifiers

757N/757P

FEATURES
6 Decade Operation – 1nA to 1mA
1/2% Log Conformity – 10nA to 100μA
Symmetrical FET Inputs
Voltage or Current Operation
Temperature Compensated

APPLICATIONS
Absorbence Measurements
Log Ratios of Voltages or Currents
Data Compression
Transducer Linearization

757 FUNCTIONAL BLOCK DIAGRAM



*POSITIVE INPUT CURRENTS (AS SHOWN), USE 757N. NEGATIVE INPUT CURRENTS, USE 757P.

7

GENERAL DESCRIPTION
Model 757 is a complete, temperature compensated, dc-coupled log ratio amplifier. It is comprised of two input channels for processing signals spanning up to 6 decades in dynamic range (1nA to 1mA). By virtue of its symmetrical FET input stages, the 757 can accommodate this 6 decade signal range at either channel. Log conformity is maintained to within 1/2% over 4 decades of input (10nA to 100μA) and to within 1% over the full input range. Unlike other log ratio designs, model 757 does not restrict the relative magnitude of the two signal inputs to achieve rated performance. Either input can be operated within the specified range regardless of the signal level at the other channel.

The model 757 log-ratio amplifier design makes available both input amplifier summing junctions. As a result, it can directly interface with photo diodes operating in the short-circuit current mode without the need of additional input circuitry.

The excellent performance of model 757 can be further improved by means of external scale factor and output offset adjustments. A significant feature of model 757 not found on competing devices is that, when the offset adjustment is used to establish a fixed bias at the output, the output offset level does not vary as a function of input signal magnitude. On other designs, the sensitivity of output offset to input levels results in output effects resembling log conformity errors.

Model 757 can operate with either current or voltage inputs. Its excellent performance makes it ideally suited for log ratio applications such as blood analysis, chromatography, chemical analysis of liquids and absorbence measurements.

CURRENT LOG RATIO
Current log ratio is accomplished by model 757 when two currents, I_{SIG} and I_{REF}, are applied directly to the input terminals (see functional block diagram). The two log amps process these signals providing vl
signals providing voltages which are proportional toth
signals providing voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, higher scale factors may be achieved by connecting external scale factor adjusting resistors.

VOLTAGE LOG RATIO
The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external resistor is attached from the voltage signal to the appropriate input current terminal of the 757. Input currents are then determined by:

$$I_{SIG} = \frac{e_1 - e_{os_1}}{R_1}, \quad I_{REF} = \frac{e_2 - e_{os_2}}{R_2}$$

e_{os_1} = Input Offset Voltage (I_{SIG} Channel)

e_{os_2} = Input Offset Voltage (I_{REF} Channel)

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	757N/P
TRANSFER FUNCTION [1]	
Current Mode	$e_o = -K \log_{10} \frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_o = -K \log_{10} \left[\frac{(e_1 - e_{os_1})}{(e_2 - e_{os_2})} \times \frac{R_2}{R_1} \right]$
ACCURACY	
Log Conformity[2]	
I_{SIG}, I_{REF} = 10nA to 100μA	±0.5%, max
I_{SIG}, I_{REF} = 1nA to 1mA	±1%, max
Scale Factor (1V/Dec)	(+0, -2%) max
vs. Temperature (0 to +70°C)	±0.04%/°C max
INPUT SPECIFICATIONS — Both Input Channels	
Current	
Signal Range, Rated Performance	
Model 757N	+1nA to +1mA min
Model 757P	-1nA to -1mA min
Max Safe	±10mA max
Bias Current, @ +25°C	(0, +) 10pA max
vs. Temperature (0 to +70°C)	x2/+10°C
Offset Voltage, @ +25°C	±1mV max
vs. Temperature (0 to +70°C)	
I_{SIG} Channel	±25μV/°C max
I_{REF} Channel	±25μV/°C max
vs. Supply Voltage	±5μV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Response (-3dB)	
Signal Channel	
I_{SIG} = 1nA	160Hz
I_{SIG} = 1μA	60kHz
I_{SIG} = 100μA	75kHz
Reference Channel	
I_{REF} = 1nA	60Hz
I_{REF} = 1μA	30kHz
I_{REF} = 100μA	80kHz

RISE TIME	Signal Channel (I_{REF} = 10μA)	Reference Channel (I_{SIG} = 10μA)
Increasing Input Current		
1nA to 10nA	2.5ms	1.0ms
10nA to 100nA	250μs	40μs
100nA to 1μA	25μs	30μs
1μA to 100μA	10μs	25μs
Decreasing Input Current		
100μA to 1μA	5μs	10μs
1μA to 100nA	10μs	50μs
100nA to 10nA	50μs	500μs
10nA to 1nA	500μs	10ms

INPUT NOISE	
Voltage (10Hz to 10kHz)	3μV rms
Current (10Hz to 10kHz)	0.1pA rms
OUTPUT SPECIFICATIONS	
Rated Output	
Voltage	±10V min
Current	±5mA min
Resistance	0.1Ω
Offset Voltage[3] (K = 1V/Decade)	±15mV max
vs. Temperature (0 to +70°C)	±0.3mV/°C
vs. Supply	±5μV/V
POWER SUPPLY[4]	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±8mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Case Size	1.5" x 1.5" x 0.4"
Weight	21 grams

NOTES

[1] For model 757N, K = +1V/Decade and input currents must be positive. For model 757P, K = -1V/Decade and input currents must be negative. (Input currents are defined as positive when flowing into the input terminals, 4 and 5. Refer to TRANSFER CURVES.)

[2] The log conformity error is referred to input (RTI). 1% error RTI is equivalent to 4.3mV of error at the output for K = 1V/Dec.

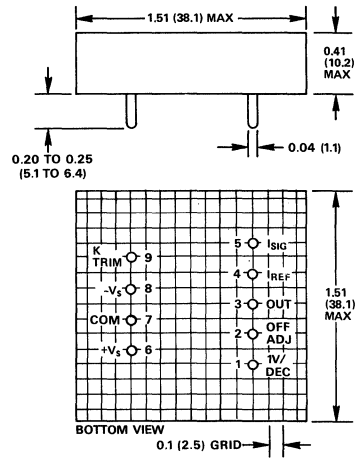
[3] Externally adjustable to zero.

[4] Recommended power supply: Analog Devices model 904, ±15V @ 50mA.

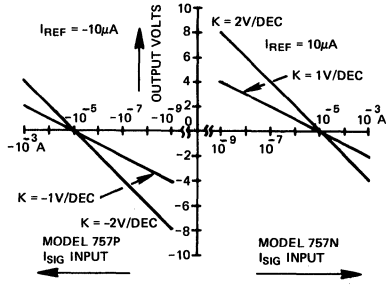
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TRANSFER CURVES



Log mode output voltage vs. input current for I_{REF} = 10μA.

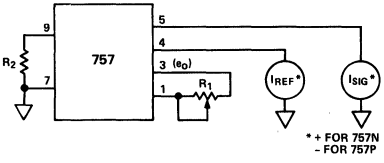


Figure 1. Scale Factor Adjustment

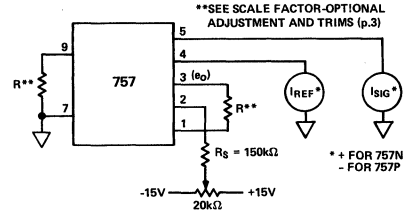


Figure 2. Output Voltage Offset Adjustments

OPTIONAL ADJUSTMENTS AND TRIMS

Scale Factor – A one volt per decade scale factor is available when pin 1 is tied to 3 and pin 7 is connected to 9. Higher scale factors are possible by using a potentiometer, R_1, between pins 1 and 3 and a resistor, R_2, between pins 7 to 9 as shown in Figure 1. The value of the required resistor is (13.2kΩ) (K-1) where K is the desired scale factor. The approximate potentiometer value is also (13.2kΩ) (K-1). The scale factor adjustment procedure is as follows:

1. Connect the appropriate value of resistor between pins 7 and 9.
2. Set I_{REF} = 1μA, I_{SIG} = 10μA. Measure e_O.
3. Set I_{REF} = 1μA, I_{SIG} = 100μA. Adjust R_1 until the difference in e_O corresponding to steps 2 and 3 is K volts.
4. Repeat steps 2 and 3 until the change in e_O = K volts.

Output Voltage Offset – Output voltage offset must be adjusted after the desired scale factor is established as indicated above. To adjust the offset, inject equal dc input currents into the reference and signal channels. The value of the input currents should approximate the average input current levels expected to be encountered in normal operation. Adjust the potentiometer shown in Figure 2 until the output voltage is zero.

LOG CONFORMITY

Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the theoretical value of the log of a ratio and the actual value that appears at the output of the log-ratio module after scale factor errors have been eliminated. Measurement of this error is made after initially zeroing the module at unity-ratio and adjusting the desired scale factor.

Figure 3 shows the log conformity performance of model 757 over a 6 decade input range. Log conformity for each channel does not vary noticeably as the current is varied in the other channel.

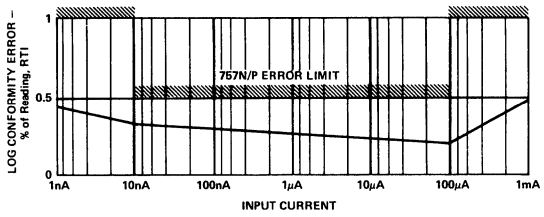


Figure 3. Log Conformity Error for 757. Curve Is for Either Input Channel with Current Held Constant at 10μA on Other Channel.

FREQUENCY CHARACTERISTICS

Figure 4 shows a plot of small signal response (-3dB) as a function of input signal current. The graph demonstrates the frequency response performance for each input channel over the range of 1nA to 1mA, independent of current on the other channel.

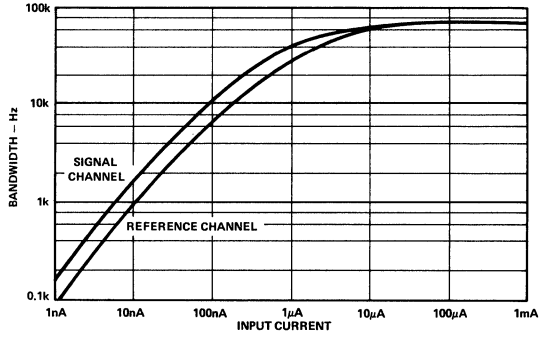


Figure 4. Small Signal Bandwidth (–3dB) vs. Input Signal Level

APPLICATIONS

Data Compression – Processing signals with wide dynamic range is a common problem in instrumentation and data transmission. For example, digitizing an analog signal with a range of 10nA to 100μA with 1% accuracy requires a 20 bit A/D converter. (Required resolution = 1/100 x 1/10,000 = $1/10^6 \cong 1/2^{20}$).

By using the 757 with I_{REF} adjusted to 10nA and K set for 5/4 V/decade, the input data can be compressed into a 5 volt output range. For a 1% resolution of any signal, the allowable output error is 4.32mV x K. Log conformity contributes 2.17mV x K (0.5%) over this range. The remaining error with K = 5/4 is 2.69mV and should correspond to less than the LSB of the converter. With a 5 volt output range 2.69mV corresponds just over the LSB of an 11-bit converter. Thus the 757 module can compress the data for use with a 12 bit A/D (such as Analog Devices AD574JD) to obtain the desired 1% resolution.

Absorbence Measurements – Critical properties of materials which are of particular interest in the fields of chemistry, medicine, spectrometry and pollution control are characterized by absorbence. The relationship between absorbence, A, and light intensity, I, is: $A = \log I_O/I_T$ where I_O = intensity of incident light, and I_T = intensity of transmitted light.

Figure 5 shows the 757 log-ratio module used in such a photometer application. Two inputs represent the intensities of light transmitted through space and through a medium that absorbs light. The absorbence of the medium is given by the formula

$$A = \log \frac{I_{SIGNAL}}{I_{REFERENCE}}$$

where I_{SIGNAL} and $I_{REFERENCE}$ are the currents representing the light intensities.

The transducers used in this application are photodiodes, which provide a short-circuit current proportional to the intensity of applied light. The lowest value of absorbence is determined by the value of I_{REF}, since when $I_{SIG} = I_{REF}$, A = 0. The output of the log-ratio module is externally trimmed to 1V/decade and applied to the input of a 3½-digit DPM through the scaling network R1 and R2.

Model 757 was chosen for this design because it makes available both amplifier summing junctions. When the photodiodes are connected to the summing junctions, they are operated in the short-circuit mode, that is, with zero volts across the diodes. Short-circuit loading is necessary, because accuracy of the photodiodes can be degraded several percent when operated with as little as 100mV across the diode junction.

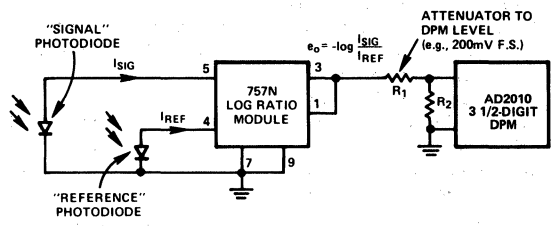


Figure 5. 757N Applied to Absorbence Measurements

INTERCONNECTION GUIDELINES

Model 757 is a complete log ratio amplifier that requires no additional frequency compensation for proper operation.

Input Capacitance – Model 757 is able to operate with 1000pF at both input terminals. Therefore, the 757 can be used in applications requiring long cable lengths between the module and the signal transducers.

Input-to-Output Capacitance – When using a log ratio module the user should take care in system configurations to avoid excessive stray capacitance between input and output terminals. Such precautions include avoiding running input and output signal lines close together. If long cable runs are required where inputs and output are closely bundled together, it is advisable to enclose the inputs and/or output in separate, grounded electrostatic shields. By observing simple rules of good circuit layout, problems with oscillations that may result from excessive input-to-output capacitance can easily be avoided. Model 757 can accommodate up to 33pF of input-to-output capacitance without oscillation.

Leakage Resistance – Since model 757 can operate at extremely low input current levels, precautions must be taken to prevent current leakage into the input terminals. Such leakage can cause errors when small input or reference currents are used. This problem may arise on printed circuit layouts if the inputs are run too close to the power supply busses. Providing an etched guard around the input lines, connected to analog signal ground will also reduce unwanted current leakage.

RMS-to-DC Converters
Contents

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AD636 – Low Level, True RMS-to-DC Converter . . . . . 8 – 13
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Selection Guide
RMS-to-DC Converters

Model	Conversion Accuracy mV ±%Read max	Full-Scale Range V RMS	dB Output Error dB max	Package Options[2]	Temp Range[3]	Page	Comments
AD737	(0.2±0.3)–(0.4±0.5)	0.2		N, Q, R	C, I	8–37	Low Cost, Low Power, No Output Buffer
AD736	(0.3±0.3)–(0.5±0.5)	0.2		N, Q, R	C, I	8–29	General Purpose, Low Cost, Low Power
AD636	(0.2±0.3)–(0.5±0.6)	0.2	0.2–0.5	D, H	C	8–13	Low Power
AD637	(0.5±0.2)–(1±0.5)	7	0.3 (typ)	D, Q, R	C, M	8–21	High Accuracy, Wide Bandwidth
AD536A	(2±0.2)–(5±0.5)	7	0.3–0.6	D, E, H	C, M	8–5	General Purpose

[1]Unity gain small signal bandwidth.
[2]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line; Q–Cerdip; R–Small Outline Plastic (SOIC).
[3]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
RMS-to-DC Converters

RMS-to-DC converters continuously compute the instantaneous square of the input signal, average it, and take the square root of the result, to provide a dc voltage proportional to the rms of the input (and, in the case of the AD536 and AD636, an auxiliary dc voltage that is proportional to the *log* of the rms, for dB measurements).

Excellent pretrimmed performance, improvable by simple optional trims, makes these devices ideal for all types of laboratory and OEM rms instrumentation where amplitude measurements must be made with high accuracy, independently of waveshape.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of a signal (i.e., rectifying it) filtering it and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform; it will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

An important application is noise measurement – for example, thermal noise, transistor noise, and switch-contact noise. True rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

True rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise and acoustical noise.

The electrical signals produced by these mechanical actions are often noisy, nonperiodic, nonsinusoidal, and superimposed on dc levels, and require true rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

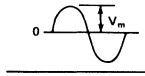
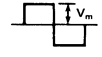
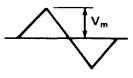
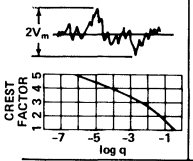
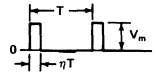
The basic approach used in these converters for computing the rms is to take the absolute value, square it and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$V_{RMS} = Avg.\left[\frac{V_{in}^{\,2}}{V_{RMS}}\right] \cong \sqrt{Avg.\ (V_{in}^{\,2})}$$

is valid if the averaging time constant is sufficiently long compared with the periods of the lowest frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter using an external filtering capacitor (C_{AV}). Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, an additional stage of 2-pole filtering is useful. The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{AV} .

8

WAVEFORM		RMS	MAD	RMS / MAD	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ 0.707 V_m	$\frac{2}{\pi} V_m$ 0.637 V_m	$\frac{\pi}{2\sqrt{2}}$ = 1.111	$\sqrt{2}$ = 1.414
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}}$ = 1.155	$\sqrt{3}$ = 1.732
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. / q 1 / 32% 2 / 4.6% 3 / 0.37% 3.3 / 0.1% 3.9 / 0.01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2x10⁻⁹
	PULSE TRAIN η / MARK/SPACE 1 / ∞ 0.25 / 0.3333 0.0625 / 0.0667 0.0156 / 0.0159 0.01 / 0.0101	$V_m\sqrt{\eta}$ V_m $0.5V_m$ $0.25V_m$ $0.125V_m$ $0.1V_m$	$V_m\eta$ V_m $0.25V_m$ $0.0625V_m$ $0.0156V_m$ $0.01V_m$	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10

η: "DUTY CYCLE"

PERFORMANCE SPECIFICATIONS

Considerable information regarding rms-to-dc converter circuit design, performance, selection and applications is to be found in the *RMS-to-DC Conversion Application Guide*.[1] In addition, useful applications information can be found in the *Nonlinear Circuits Handbook*.[2]

The most-salient feature of a true rms-to-dc converter is that *it ideally has no error due to an indirect approximation to the rms*. Static errors are due only to scale-factor, linearity and offset errors; dynamic errors are due to insufficient averaging time at the low end and finite bandwidth and slewing rate at the upper end. Linearity errors affect crest factor in midband. Dynamic errors are also a function of signal amplitude, due in part to the variation of bandwidth of the "log" transistors with signal level.

Total Error, Internal Trim, a specification for quick reference, is the maximum deviation of the dc component of the output voltage from the theoretical output value over a specified range of signal amplitude and frequency. It is shown as the sum of a fixed error and a component proportional to the theoretical output (% of reading). It is specified for a sinusoidal input in a given frequency and amplitude range. The fixed error component includes all offset errors and irreducible nonlinearities; the %-of-reading component includes the linear scale-factor error.

Total Error, External Adjustment is the amount by which the output may differ from the theoretical value when the output offset and scale factor have been trimmed. Note that the fixed error-component cannot be reduced to zero, even though the output offset can be nulled at zero input. This is because of residual input offsets and inherent nonlinearities in the converter.

Total Error vs. Temperature (T_{min} to T_{max}) is the average change of %-of-full-scale error component plus the average change of percent-of-reading error component per degree Celsius, over the rated temperature range.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for −3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal −30% of reading. It is a function of amplitude.

Crest Factor (to a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case – rectangular pulse – input signal.

Averaging Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance (C_{AV}).

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Power Supply: Power-supply range for specified performance, power-supply range for operation and quiescent current drain.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements (T_H − 25°C), (25°C − T_L), when measured.

[1] ***RMS-to-DC Conversion Application Guide 2nd Edition*, by C. Kitchin and L. Counts (1986-61 pages). Available free from Analog Devices.**
[2] ***Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D.H. Sheingold. ($5.95).**

ANALOG DEVICES

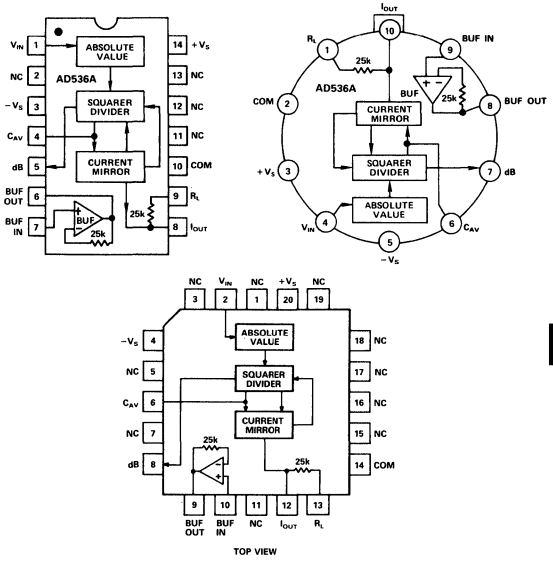
Integrated Circuit True RMS-to-DC Converter

AD536A

FEATURES

True RMS-to-DC Conversion
Laser-Trimmed to High Accuracy
0.2% max Error (AD536AK)
0.5% max Error (AD536AJ)
Wide Response Capability:
Computes RMS of AC and DC Signals
450kHz Bandwidth: $V_{rms} > 100mV$
2MHz Bandwidth: $V_{rms} > 1V$
Signal Crest Factor of 7 for 1% Error
dB Output with 60dB Range
Low Power: 1.2mA Quiescent Current
Single or Dual Supply Operation
Monolithic Integrated Circuit
−55°C to +125°C Operation (AD536AS)

AD536A PIN CONFIGURATIONS AND FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60 dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full-scale accuracy at 7V rms. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the −55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2mV ±0.2% of reading, and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can. The AD536AS is also available in a 20-pin hermetically sealed ceramic leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536 and provides improved bandwidth and temperature drift specifications.

SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

Model	AD536AJ			AD536AK			AD536AS			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Figure 1)			**±5 ±0.5**			**±2±0.2**			**±5 ±0.5**	mV ± % of Reading
vs. Temperature, T_{min} to +70°C			**±0.1 ±0.01**			**±0.05 ±0.005**			**±0.1 ±0.005**	mV ± % of Reading/°C
+70°C to +125°C									**±0.3 ±0.005**	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error		±0.2			±0.1			±0.2		± % of Reading
Total Error, External Trim[1] (Figure 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR VS. CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.1			−0.1			−0.1		% of Reading
Crest Factor = 7		−1.0			−1.0			−1.0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% additional error (0.09dB)										
V_{IN} = 10mV		5			5			5		kHz
V_{IN} = 100mV		45			45			45		kHz
V_{IN} = 1V		120			120			120		kHz
±3dB Bandwidth										
V_{IN} = 10mV		90			90			90		kHz
V_{IN} = 100mV		450			450			450		kHz
V_{IN} = 1V		2.3			2.3			2.3		MHz
AVERAGING TIME CONSTANT (Figure 5)		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ±15V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, ±5V Supplies		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, ±5V Supplies			±7			±7			±7	V peak
Maximum Continuous Nondestructive										
Input Level (All Supply Voltages)			±25			±25			±25	V peak
Input Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
Input Offset Voltage		0.8	±2		0.5	±1		0.8	±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V_{IN} = COM (Figure 1)		±1	**±2**		±0.5	**±1**			**±2**	mV
vs. Temperature		±0.1			±0.1				**±0.2**	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ±15V Supplies	**0 to +11**	+12.5		**0 to +11**	+12.5		**0 to +11**	+12.5		V
±5V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT (Figure 13)										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.4	**±0.6**		±0.2	**±0.3**		±0.5	**±0.6**	dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor TC (Uncompensated, see Figure 1 for Temperature Compensation)		−0.033			−0.033			−0.033		dB/°C
		+0.33			+0.33			+0.33		% of Reading/°C
I_{REF} for 0dB = 1V rms	5	20	**80**	5	20	**80**	5	20	**80**	μA
I_{REF} Range	1		100	1		100	1		100	μA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		μA/V rms
I_{OUT} Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
Output Resistance	20	25	30	20	25	30	20	25	30	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5)			$-V_S$ to ($+V_S$ −2.5V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)		V
Input Offset Voltage, R_S = 25k		±0.5	**±4**		±0.5	**±4**		±0.5	**±4**	mV
Input Bias Current		20	**60**		20	**60**		20	**60**	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current		(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)		
Short Circuit Current		20			20			20		mA
Output Resistance			0.5			0.5			0.5	Ω
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/μs
POWER SUPPLY										
Voltage Rated Performance		±15			±15			±15		V
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S, 5V to 36V, T_{min} to T_{max}		1.2	**2**		1.2	**2**		1.2	**2**	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−55		+150	−55		+150	−55		+150	°C
NUMBER OF TRANSISTORS		65			65			65		
PACKAGE OPTIONS[5]										
Ceramic DIP (D-14)		AD536AJD			AD536AKD			AD536ASD		
Metal Can TO-100 (H-10A)		AD536AJH			AD536AKH			AD536ASH		
LCC (E-20A)								AD536ASE		

NOTES
[1]Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.
[2]Error vs. crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs.
[3]Input voltages are expressed in volts rms, and error is percent of reading.
[4]With 2k external pulldown resistor.
[5]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
- Dual Supply . . . . . ±18V
- Single Supply . . . . . +36V

Internal Power Dissipation[2] 500mW
Maximum Input Voltage . . . . . ±25V Peak
Buffer Maximum Input Voltage . . . . . $\pm V_S$
Maximum Input Voltage . . . . . ±25V Peak
Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range
- AD536AJ/K . . . . . 0 to +70°C
- AD536AS . . . . . −55°C to +125°C

Lead Temperature Range
- (Soldering 60 sec) . . . . . 300°C

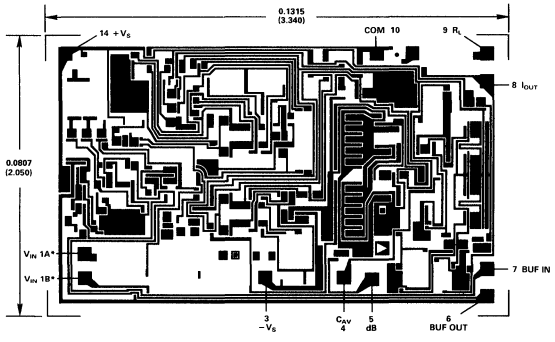
NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]10-Pin Header: θ_{JA} = 150°C/W
20-Pin LCC: θ_{JA} = 95°C/W
14-Pin Size Brazed Ceramic DIP: θ_{JA} = 95°C/W

CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14-PIN CERAMIC DIP PACKAGE.

NOTE
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.
THE AD536A IS AVAILABLE IN LASER TRIMMED CHIP FORM.
SUBSTRATE CONNECTED TO $-V_S$.

ORDERING GUIDE[1]

Temperature Range	Header	Sidebrazed Ceramic DIP	Leadless Chip Carrier
Commercial 0 to +70°C	AD536AJH AD536AKH	AD536AJD AD536AKD	
Military −55°C to +125°C	AD536ASH AD536ASH/883B	AD536ASD AD536ASD/883B	AD536ASE AD536ASE/883B

NOTE
[1]"S" grade chips are available tested at +25°C and +125°C. "J" grade chips are also available.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will

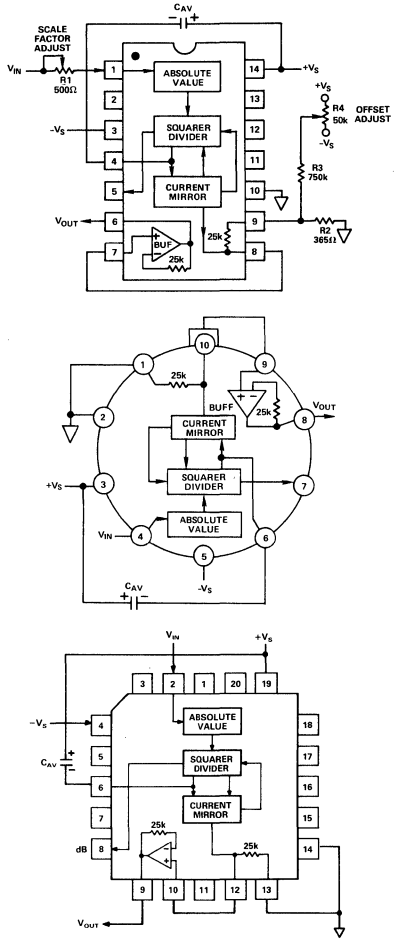


Figure 1. Standard RMS Connection

show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%; at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with the input, as shown in Figure 3, the capacitor must be nonpolar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 14. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at Pin 8 (Pin 10 on the "H" package) with a nominal scale of 40μA per volt rms input positive out.

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds 365Ω in series with the internal 25kΩ resistor. This will cause a 1.5% increase in scale factor, which is trimmed out by using R_1 as shown. Range of scale factor adjustment is ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R4 to give zero volts output from Pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from Pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000V peak-to-peak sine wave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full-scale range.

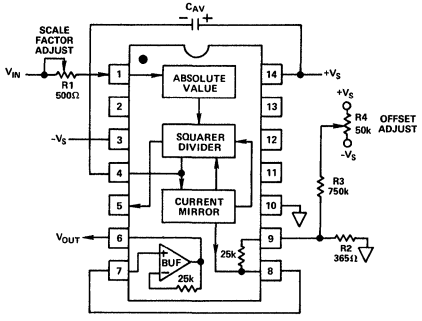


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at Pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 μA of current flows into Pin 10 (Pin 2 on the "H" package). AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 14. The load resistor, R_L, is necessary to provide output sink current.

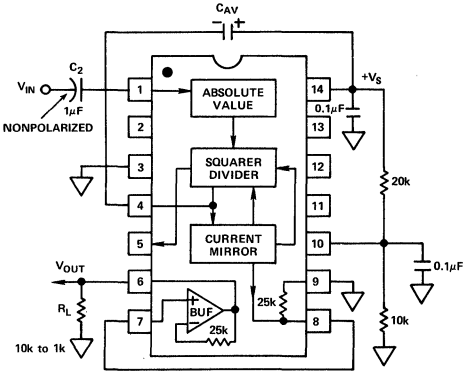


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly varying dc signal, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

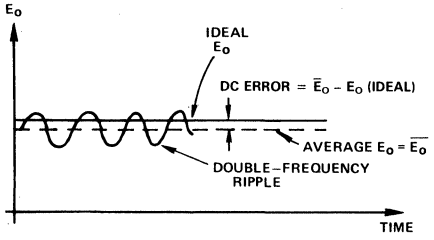


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given percent dc error above a given frequency using the standard rms connection.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

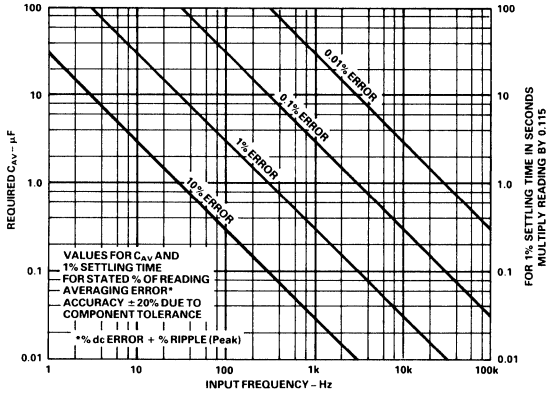


Figure 5. Error/Settling Time Graph for Use with the Standard RMS Connection in Figure 1

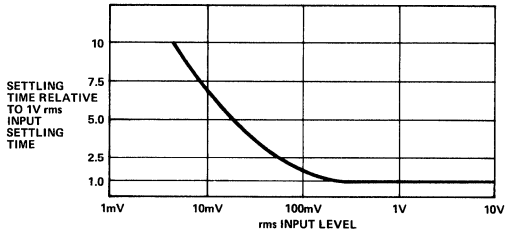


Figure 6. Settling Time vs. Input Level

A better method for reducing output ripple is the use of a "post-filter." Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8 and settling time is increased. For example, with C_{AV} = 1µF and C_2 = 2.2µF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explanation of these topics refer to the *RMS to DC Conversion Application Guide 2nd Edition*, available from Analog Devices.

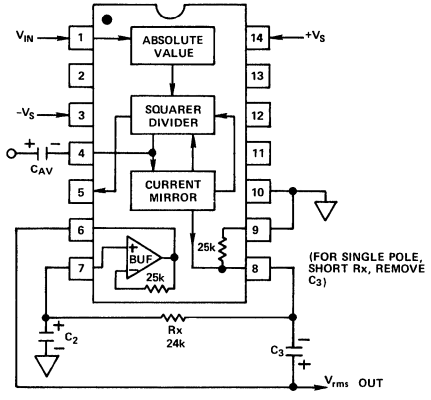


Figure 7. 2-Pole "Post" Filter

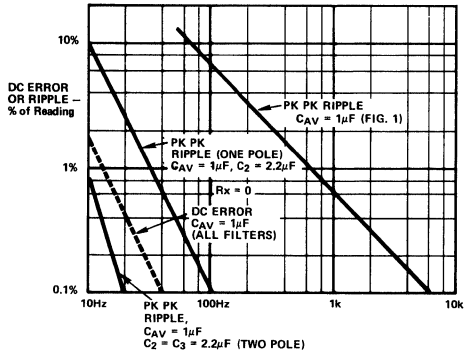


Figure 8. Performance Features of Various Filter Types

8

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = Avg.\left[\frac{V_{IN}^2}{V_{rms}}\right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2/I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = Avg.\ [I_1^2/I_4] = I_1\ rms$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2\ I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q3, since the voltage at this point is proportional to $-\log V_{IN}$. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

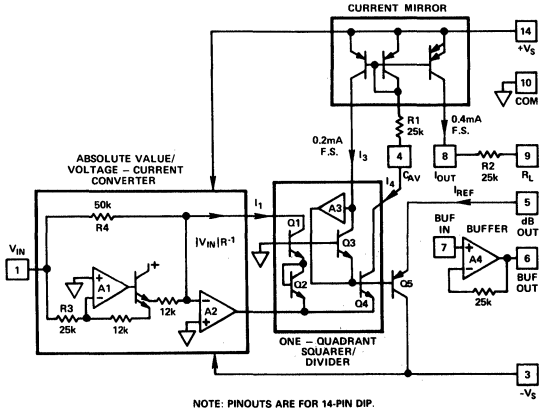


Figure 9. Simplified Schematic

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A is the logarithmic or decibel output. The internal circuit computing dB works accurately over a 60dB range. The connections for dB measurements are shown in Figure 10. The user selects the 0dB level by adjusting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C scale factor drift of the dB output pin. The special T.C. resistor, R_2, is available from Tel Labs in Londonderry, N.H. (Model Q-81) or from Precision Resistor Inc., Hillside, N.J. (model PT146). The averaged temperature coefficients of resistors R_2 and R_3 develop the +3300ppm needed to reverse compensate the dB output. The linear rms output is available at Pin 8 on DIP or Pin 10 on header device with an output impedance of 25kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc or 1.00V rms
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc or 0.10V rms
4. Adjust R_5 for dB out = −2.00V

Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_5 for the proper gain automatically gives the correct temperature compensation.

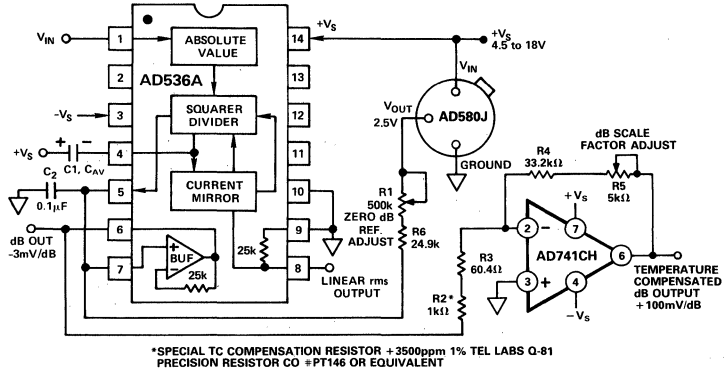


Figure 10. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 7 volts rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 120kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to only 5kHz.

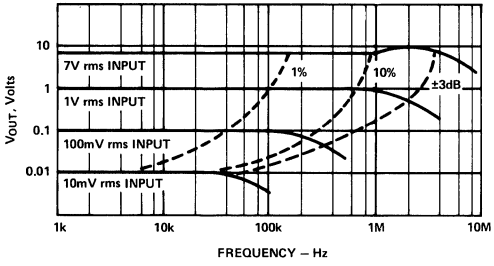


Figure 11. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (C.F. = V_p/Vrms). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 12 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 11 while maintaining a constant 1 volt rms input amplitude.

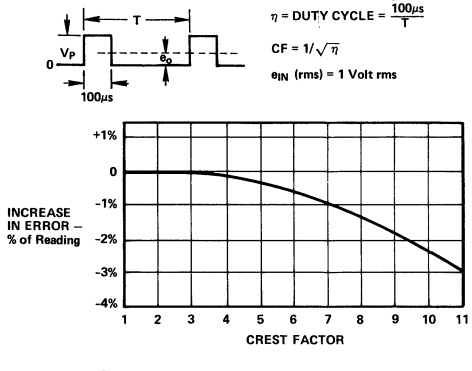


Figure 12. Error vs. Crest Factor

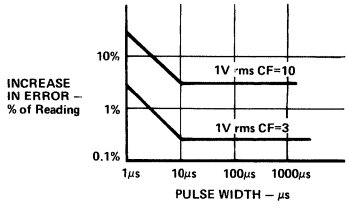
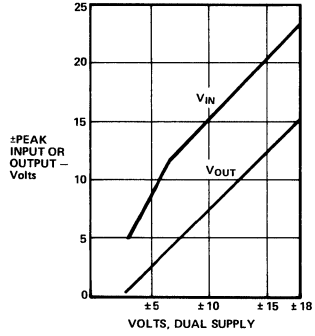


Figure 13. AD536A Error vs. Pulse Width Rectangular Pulse



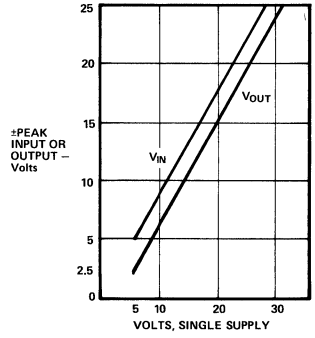


Figure 14. AD536A Input and Output Voltage Ranges vs. Supply

8

ANALOG DEVICES

Low Level, True RMS-to-DC Converter

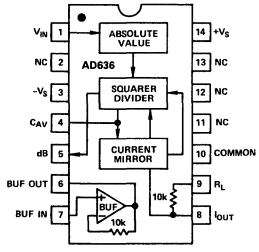
AD636

FEATURES

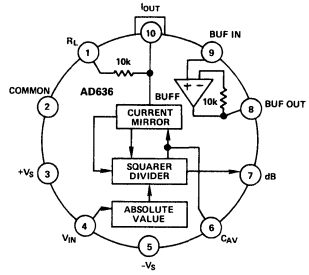
- True rms-to-dc Conversion
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz -3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- Low Cost
- Available in Chip Form

AD636 PIN CONNECTIONS & FUNCTIONAL BLOCK DIAGRAM

"D" Package (TO-116)



"H" Package (TO-100)



PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. The AD636 is specified for a signal range of 0 to 200 millivolts rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5V to ±16.5V or a single +5V to +24V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0dBm (774.6mV) to -20dBm (77.46mV). Frequency response ranges from 1.2MHz at a 0dBm level to over 10kHz at -50dBm.

The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full scale accuracy at 200mV rms. Thus no external trims are required to achieve full rated accuracy.

AD636 is available in two accuracy grades; the AD636J total error of ±0.5mV ±0.06% of reading, and the AD636K is accurate within ±0.2mV to ±0.03% of reading. Both versions are specified for the 0 to +70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10-pin TO-100 metal can. Chips are also available.

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PRODUCT HIGHLIGHTS

1. The AD636 computes the true root-mean-square of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it is a measure of the power in the signal. The rms value of an ac-coupled signal is also its standard deviation.
2. The 200 millivolt full scale range of the AD636 is compatible with many popular display-oriented analog-to-digital converters. The low power supply current requirement permits use in battery-powered hand-held instruments.
3. The only external component required to perform measurements to the fully specified accuracy is the averaging capacitor. The value of this capacitor can be selected for the desired trade-off of low frequency accuracy, ripple, and settling time.
4. The on-chip buffer amplifier can be used to buffer either the input or the output. Used as an input buffer, it provides accurate performance from standard 10MΩ input attenuators. As an output buffer, it can supply up to 5 milliamps of output current.
5. The AD636 will operate over a wide range of power supply voltages, including single +5V to +24V or split ±2.5V to ±16.5V sources. A standard 9V battery will provide several hundred hours of continuous operation.

SPECIFICATIONS (@ +25°C, and $+V_S = +3V$, $-V_S = -5V$ unless otherwise noted)

Model	AD636J			AD636K			Units
	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY							
Total Error, Internal Trim[1,2]			±0.5 ±0.6			±0.2 ±0.3	mV ± % of Reading
vs. Temperature, 0 to +70°C			±0.1 ±0.01			±0.1 ±0.005	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error at 200mV		±0.2			±0.1		% of Reading
Total Error, External Trim[1]		±0.3 ±0.1			±0.1 ±0.1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]							
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.2			−0.2		% of Reading
Crest Factor = 6		−0.5			−0.5		% of Reading
AVERAGING TIME CONSTANT		25			25		ms/μF CAV
INPUT CHARACTERISTICS							
Signal Range, All Supplies							
Continuous rms Level		0 to 200			0 to 200		mV rms
Peak Transient Inputs							
+3V, −5V Supply			±2.8			±2.8	V pk
±2.5V Supply			±2.0			±2.0	V pk
±5V Supply			±5.0			±5.0	V pk
Maximum Continuous Non-Destructive							
Input Level (All Supply Voltages)			±12			±12	V pk
Input Resistance	5.33	6.67	8	5.33	6.67	8	kΩ
Input Offset Voltage			±0.5			±0.2	mV
FREQUENCY RESPONSE[2,4]							
Bandwidth for 1% additional error (0.09dB)							
V_{IN} = 10mV		14			14		kHz
V_{IN} = 100mV		90			90		kHz
V_{IN} = 200mV		130			130		kHz
±3dB Bandwidth							
V_{IN} = 10mV		100			100		kHz
V_{IN} = 100mV		900			900		MHz
V_{IN} = 200mV		1.5			1.5		MHz
OUTPUT CHARACTERISTICS[2]							
Offset Voltage, V_{IN} = COM			±0.5			±0.2	mV
vs. Temperature		±10			±10		μV/°C
vs. Supply		±0.1			±0.1		mV/V
Voltage Swing							
+3V, −5V Supply	0 to +1.0			0 to +1.0			V
±5V to ±16.5V Supply	0 to +1.0			0 to +1.0			V
Output Impedance	8	10	12	8	10	12	kΩ
dB OUTPUT							
Error, V_{IN} = 7mV to 300mV rms		±0.3	±0.5		±0.1	±0.2	dB
Scale Factor		−3.0			−3.0		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33		% of Reading/°C
		−0.033			−0.033		dB/°C
I_{REF} for 0dB = 0.1V rms	2	4	8	2	4	8	μA
I_{REF} Range	1		50	1		50	μA
I_{OUT} TERMINAL							
I_{OUT} Scale Factor		100			100		μA/V rms
I_{OUT} Scale Factor Tolerance	−20	±10	+20	−20	±10	+20	%
Output Resistance	8	10	12	8	10	12	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2V)			$-V_S$ to ($+V_S$ −2V)		V
BUFFER AMPLIFIER							
Input and Output Voltage Range	$-V_S$ to ($+V_S$ −2V)			$-V_S$ to ($+V_S$ −2V)			V
Input Offset Voltage, R_S = 10k		±0.8	±2		±0.5	±1	mV
Input Bias Current		20	60		20	60	nA
Input Resistance		10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20		mA
Small Signal Bandwidth		1			1		MHz
Slew Rate[5]		5			5		V/μs
POWER SUPPLY							
Voltage, Rated Performance		+3, −5			+3, −5		V
Dual Supply	+2, −2.5		±16.5	+2, −2.5		±16.5	V
Single Supply	+5		+24	+5		+24	V
Quiescent Current[6]		0.80	1.00		0.80	1.00	mA

Model	AD636J Min	AD636J Typ	AD636J Max	AD636K Min	AD636K Typ	AD636K Max	Units
TEMPERATURE RANGE							
Rated Performance	0		+70	0		+70	°C
Storage	−55		+150	−55		+150	°C
PACKAGE OPTIONS[7]							
TO-116 (D-14)		AD636JD			AD636KD		
TO-100 (H-10A)		AD636JH			AD636KH		
TRANSISTOR COUNT		62			62		

NOTES
[1]Accuracy specified for 0 to 200mV rms, dc or 1kHz sine wave input. Accuracy is degraded at higher rms signal levels.
[2]Measured at pin 8 of DIP (I_{OUT}), with pin 9 tied to common.
[3]Error vs. crest factor is specified as additional error for a 200mV rms rectangular pulse train, pulse width = 200μs.
[4]Input voltages are expressed in volts rms.
[5]With 10kΩ pull down resistor from pin 6 (BUF OUT) to $-V_S$.
[6]With BUF input tied to Common.
[7]See Section 16 for package outline information.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test and are used to calculate outgoing quality levels.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
- Dual Supply . . . . . ±16.5 V
- Single Supply . . . . . +24 V

Internal Power Dissipation[2] . . . . . 500 mW
Maximum Input Voltage . . . . . ±12 V Peak
Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range
- AD636J/K . . . . . 0 to +70°C

Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

Notes
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation ofthe device at these or anyother conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]10-Pin Header: θ_{JA} = 150°C/W.
14-Pin Sidebrazed Ceramic DIP: θ_{JA} = 95°C/W.

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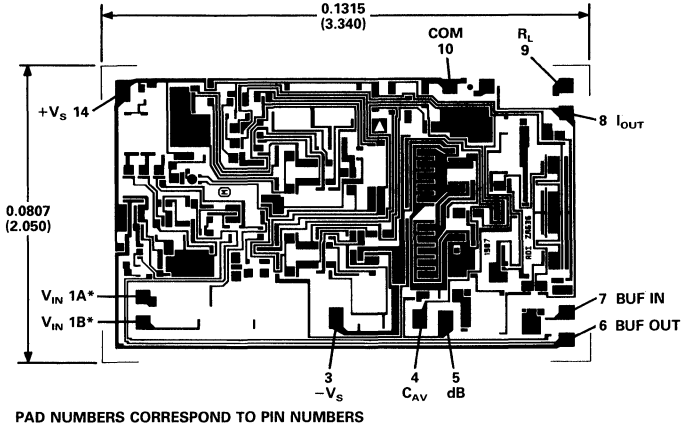
ORDERING GUIDE

Temperature Range	Header	Sidebrazed Ceramic DIP
Commercial 0 to +70°C	AD636JH AD636KH	AD636JD AD636KD

"J" and "K" grade chips are also available.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14-PIN CERAMIC DIP PACKAGE.

NOTE
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.

Applying the AD636

STANDARD CONNECTION

The AD636 is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD636 will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD636 is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible. C_F is an optional output ripple filter, as discussed elsewhere in this data sheet.

The input and output signal ranges are a function of the supply voltages as detailed in the specifications. The AD636 can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 10k resistor. The buffer amplifier can then be used for other purposes. Further, the AD636 can be used in a current output mode by disconnecting the 10k resistor from the ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 100μA per volt rms input, positive out.

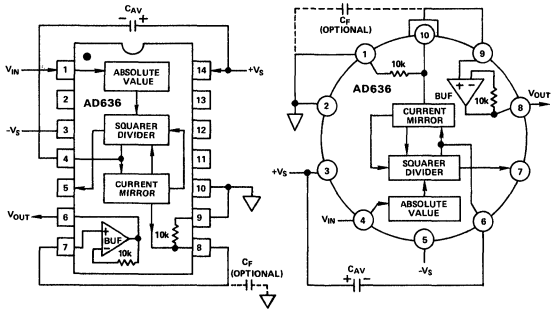


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD636, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. The scale factor is trimmed by using R_1 as shown. The insertion of R_2 allows R_1 to either increase or decrease the scale factor by ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 200mV dc input should give 200mV dc output. Of course, a ±200mV peak-to-peak sinewave should give a 141.4mV dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 assume the use of dual power supplies. The AD636 can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. Figure 3 is optimized for use with a 9 volt battery. The major limitation of this connection is that only ac signals can be measured since the input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 1 microamp of current flows into pin 10 (pin 2 on the "H" package). Alternately, the COM pin of some CMOS ADCs provides a suitable artificial ground for the AD636. AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 6.7kΩ; for a cut-off at 10Hz, C_2 should be 3.3μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The load resistor, R_L, is necessary to provide current sinking capability.

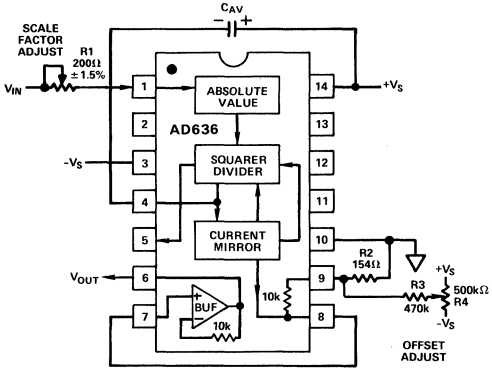


Figure 2. Optional External Gain and Output Offset Trims

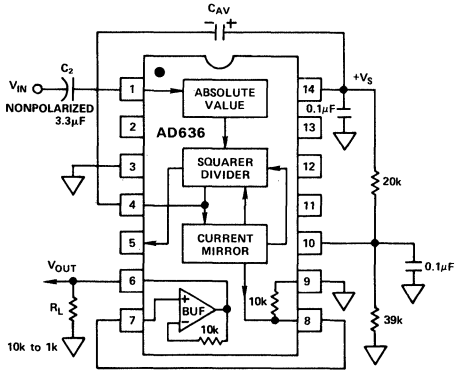


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD636 will compute the rms of both ac and dc signals. If the input is a slowly-varying dc voltage, the output of the AD636 will track the input exactly. At higher frequencies, the average output of the AD636 will approach the rms value of the input signal. The actual output of the AD636 will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

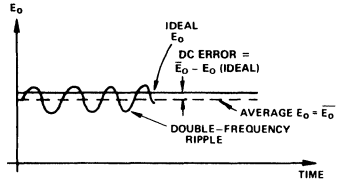


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given % dc error above a given frequency using the standard rms connection.

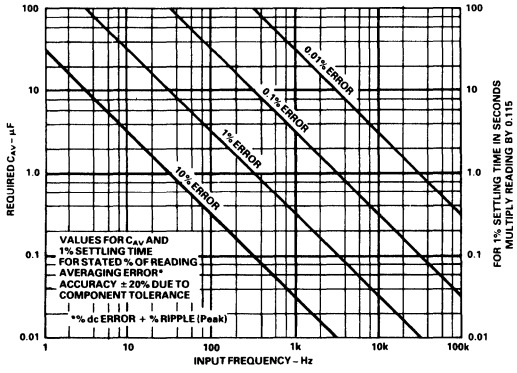


Figure 5. Error/Settling Time Graph for Use with the Standard rms Connection

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4µF capacitor (time constant = 25ms per µF).

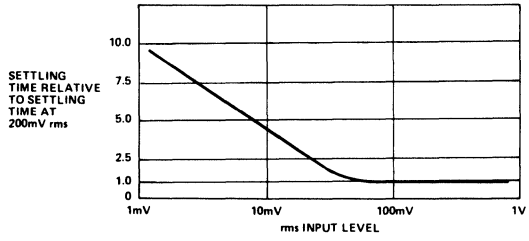


Figure 6. Settling Time vs. Input Level

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows the the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately 5 times the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1µF and C_2 = 4.7µF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

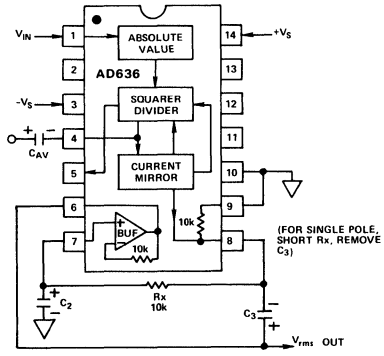


Figure 7. 2 Pole "Post" Filter

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explaination of these topics refer to the *RMS-to-DC Conversion Application Guide, 2nd Edition,* available from Analog Devices.

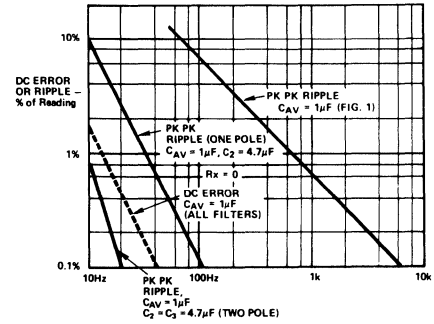


Figure 8. Performance Features of Various Filter Types

RMS Measurements

AD636 PRINCIPLE OF OPERATION

The AD636 embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD636 follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD636; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD636 thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

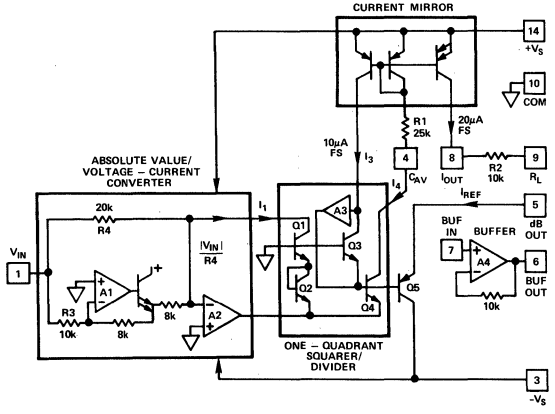


Figure 9. Simplified Schematic

THE AD636 BUFFER AMPLIFIER

The buffer amplifier included in the AD636 offers the user additional application flexibility. It is important to understand some of the characteristics of this amplifier to obtain optimum performance. Figure 10 shows a simplified schematic of the buffer.

Since the output of an rms-to-dc converter is always positive, it is not necessary to use a traditional complementary Class AB output stage. In the AD636 buffer, a Class A emitter follower is used instead. In addition to excellent positive output voltage swing, this configuration allows the output to swing fully down to ground in single-supply applications without the problems associated with most IC operational amplifiers.

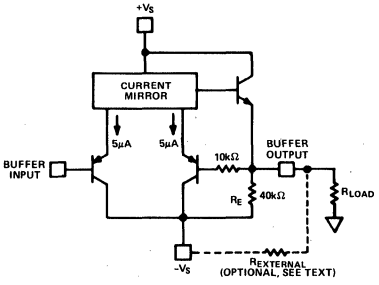


Figure 10. AD636 Buffer Amplifier Simplified Schematic

When this amplifier is used in dual-supply applications as an input buffer amplifier driving a load resistance referred to ground, steps must be taken to insure an adequate negative voltage swing. For negative outputs, current will flow from the load resistor through the 40kΩ emitter resistor, setting up a voltage divider between $-V_S$ and ground. This reduced effective $-V_S$ will limit the available negative output swing of the buffer. Addition of an external resistor in parallel with R_E alters this voltage divider such that increased negative swing is possible.

Figure 11 shows the value of $R_{EXTERNAL}$ for a particular ratio of V_{PEAK} to $-V_S$ for several values of R_{LOAD}. Addition of $R_{EXTERNAL}$ increases the quiescent current of the buffer amplifier by an amount equal to $R_{EXT}/-V_S$. Nominal buffer quiescent current with no $R_{EXTERNAL}$ is 30μA at $-V_S = -5V$.

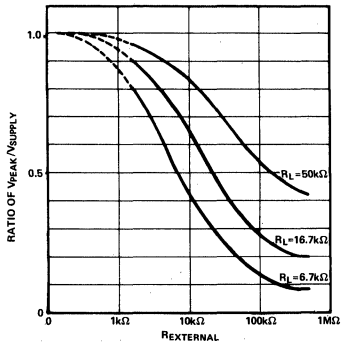


Figure 11. Ratio of Peak Negative Swing to $-V_S$ vs. $R_{EXTERNAL}$ for Several Load Resistances

FREQUENCY RESPONSE

The AD636 utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD636 at input levels from 1 millivolt to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and ±3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 220kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to 14kHz.

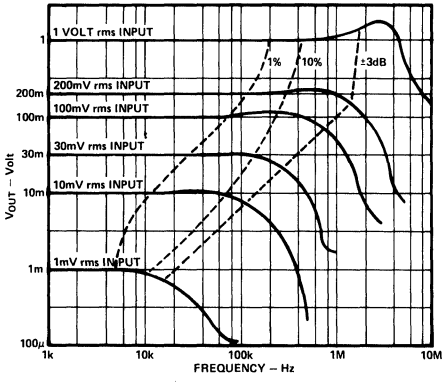


Figure 12. AD636 Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 13 is a curve of reading error for the AD636 for a 200mV rms input signal with crest factors from 1 to 7. A rectangular pulse train (pulse width 200μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 7 while maintaining a constant 200mV rms input amplitude.

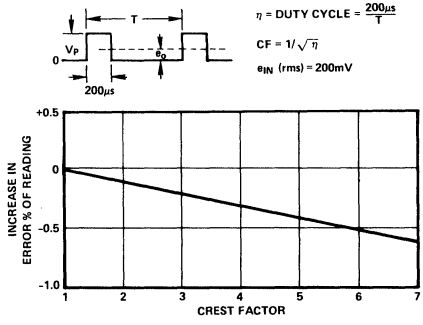


Figure 13. Error vs. Crest Factor

A COMPLETE AC DIGITAL VOLTMETER

Figure 14 shows a design for a complete low power ac digital voltmeter circuit based on the AD636. The 10MΩ input attenuator allows full scale ranges of 200mV, 2V, 20V and 200V rms. Signals are capacitively coupled to the AD636 buffer amplifier, which is connected in an ac bootstrapped configuration to minimize loading. The buffer then drives the 6.7kΩ input impedance of the AD636. The COM terminal of the ADC chip provides the false ground required by the AD636 for single supply operation. An AD589 1.2 volt reference diode is used to provide a stable 100 millivolt reference for the ADC in the linear rms mode; in the dB mode, a 1N4148 diode is inserted in series to provide correction for the temperature coefficient of the dB scale factor. Calibration of the meter is done by first adjusting offset pot R17 for a proper zero reading, then adjusting the R13 for an accurate readout at full scale.

Calibration of the dB range is accomplished by adjusting R9 for the desired 0dB reference point, then adjusting R14 for the desired dB scale factor (a scale of 10 counts per dB is convenient).

Total power supply current for this circuit is typically 2.8mA using a 7106-type ADC.

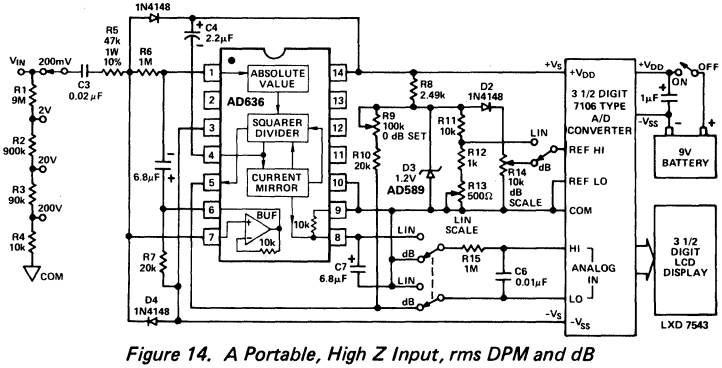


Figure 14. A Portable, High Z Input, rms DPM and dB Meter Circuit

A LOW POWER, HIGH INPUT IMPEDANCE dB METER

Introduction

The portable dB meter circuit featured here combines the functions of the AD636 rms converter, the AD589 voltage reference, and a μA776 low power operational amplifier. This meter offers excellent bandwidth and superior high and low level accuracy while consuming minimal power from a standard 9 volt transistor radio battery.

In this circuit, the built-in buffer amplifier of the AD636 is used as a "bootstrapped" input stage increasing the normal 6.7kΩ input Z to an input impedance of approximately $10^{10}\Omega$.

Circuit Description

The input voltage, V_{IN}, is ac coupled by C_4 while resistor R_8, together with diodes D_1 and D_2, provide high input voltage protection.

The buffer's output, pin 6, is ac coupled to the rms converter's input (pin 1) by capacitor C_2. Resistor R_9 is connected between the buffer's output, a Class A output stage, and the negative output swing. Resistor R_1 is the amplifier's "bootstrapping" resistor.

With this circuit, single supply operation is made possible by setting "ground" at a point between the positive and negative sides of the battery. This is accomplished by sending 250μA from the positive battery terminal through resistor R_2, then through the 1.2 volt AD589 bandgap reference, and finally back to the negative side of the battery via resistor R_{10}. This sets ground at 1.2 volts +3.18 volts (250μA × 12.7kΩ) = 4.4 volts below the positive battery terminal and 5.0 volts (250μA × 20kΩ) above the negative battery terminal. Bypass capacitors C_3 and C_5 keep both sides of the battery at a low ac impedance to ground. The AD589 bandgap reference establishes the 1.2 volt regulated reference voltage which together with resistor R_3 and trimming potentiometer R_4 set the zero dB reference current I_{REF}.

Performance Data

0dB Reference Range = 0dBm (770mV) to −20dBm (77mV) rms

0dBm = 1 milliwatt in 600Ω
Input Range (at I_{REF} = 770mV) = 50dBm
Input Impedance = approximately $10^{10}\Omega$
V_{SUPPLY} Operating Range +5V dc to +20V dc
$I_{QUIESCENT}$ = 1.8mA typical

Accuracy with 1kHz sinewave and 9 volt dc supply:
0dB to −40dBm ±0.1dBm
0dBm to −50dBm ±0.15dBm
+10dBm to −50dBm ±0.5dBm

Frequency Response ±3dBm:
Input
0dBm = 5Hz to 380kHz
−10dBm = 5Hz to 370kHz
−20dBm = 5Hz to 240kHz
−30dBm = 5Hz to 100kHz
−40dBm = 5Hz to 45kHz
−50dBm = 5Hz to 17kHz

Calibration

1. First calibrate the zero dB reference level by applying a 1kHz sinewave from an audio oscillator at the desired zero dB amplitude. This may be anywhere from zero dBm (770mV rms – 2.2 volts p–p) to −20dBm (77mV rms 220mV – p–p). Adjust the I_{REF} cal trimmer for a zero indication on the analog meter.
2. The final step is to calibrate the meter scale factor or gain. Apply an input signal −40dB below the set zero dB reference and adjust the scale factor calibration trimmer for a 40μA reading on the analog meter.

The temperature compensation resistors for this circuit may be purchased from: *Tel Labs Inc.*, 154 Harvey Road, P.O. Box 375, Londonderry, NH 03053, Part #Q332A 2kΩ 1% +3500ppm/°C or from *Precision Resistor Company,* 109 U.S. Highway 22, Hillside, NJ 07205, Part #PT146 2kΩ 1% +3500ppm/°C.

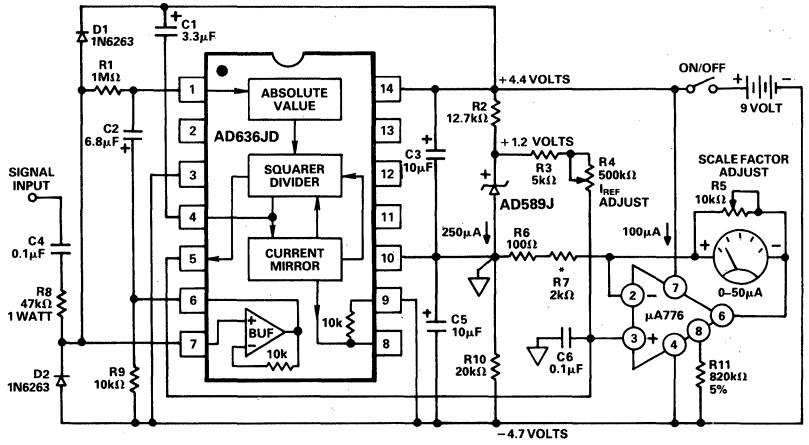


Figure 15. A Low Power, High Input Impedance dB Meter

High Precision, Wideband RMS-to-DC Converter

AD637

FEATURES

High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V RMS Input**
- **0.10% Additional Error to Crest Factor of 3**

Wide Bandwidth
- **8MHz at 1V RMS Input**
- **600kHz at 100mV RMS**

Computes:
- **True RMS**
- **Square**
- **Mean Square**
- **Absolute Value**

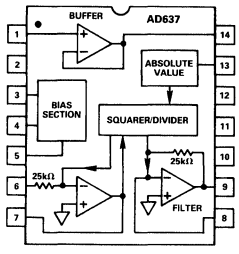
dB Output (60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiescent Current Reduction from 2.2mA to 350μA**

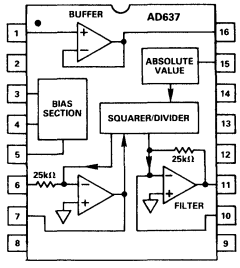
Side Brazed DIP, Low-Cost Cerdip and SOIC

AD637 FUNCTIONAL BLOCK DIAGRAMS

Ceramic DIP (D) and Cerdip (Q) Package



SOIC (R) Package



PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms to dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms to dc converters and comparable to discrete and modular techniques in accuracy, bandwidth and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600kHz with inputs of 200mV rms and up to 8MHz when the input levels are above 1V rms.

As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin allowing direct dB measurement with a useful range of 60dB. An externally programmed reference current allows the user to select the 0dB reference voltage to correspond to any level between 0.1V and 2.0V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2mA to 350μA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wide-band true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

The AD637 is available in two accuracy grades (J, K) for commercial (0 to +70°C) temperature range applications and one (S) rated over the −55°C to +125°C temperature range. All versions are available in hermetically-sealed, 14-pin side-brazed ceramic DIPs as well as low-cost cerdip packages. A 16-pin SOIC package is also available.

8

PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor which sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level and settling time.
3. The chip select feature of the AD637 permits the user to power down the device down during periods of nonuse, thereby, decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used as either an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby, increasing the accuracy of the measurement.

SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

Model	AD637J Min	AD637J Typ	AD637J Max	AD637K Min	AD637K Typ	AD637K Max	AD637S Min	AD637S Typ	AD637S Max	Units
TRANSFER FUNCTION	$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Fig. 2)			±1 ±0.5			±0.5 ±0.2			±1 ±0.5	mV ± % of Reading
T_{min} to T_{max}			±3.0 ±0.6			±2.0 ±0.3			±6 ±0.7	mV ± % of Reading
vs. Supply, + V_{IN} = + 300mV		30	150		30	150		30	150	µV/V
vs. Supply, − V_{IN} = − 300mV		100	300		100	300		100	300	µV/V
dc Reversal Error at 2V			0.25			0.1			0.25	% of Reading
Nonlinearity 2V Full Scale[2]			0.04			0.02			0.04	% of FSR
Nonlinearity 7V Full Scale			0.05			0.05			0.05	% of FSR
Total Error, External Trim		±0.5 ±0.1			±0.25 ±0.05			±0.5 ±0.1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		±0.1			±0.1			±0.1		% of Reading
Crest Factor = 10		±1.0			±1.0			±1.0		% of Reading
AVERAGING TIME CONSTANT		25			25			25		ms/µF C_{AV}
INPUT CHARACTERISTICS										
Signal Range, ± 15V Supply										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±15			±15			±15	V p-p
Signal Range, ± 5V Supply										
Continuous rms Level		0 to 4			0 to 4			0 to 4		V rms
Peak Transient Input			±6			±6			±6	V p-p
Maximum Continuous Non-Destructive Input Level (All Supply Voltages)			±15			±15			±15	V p-p
Input Resistance	6.4	8	9.6	6.4	8	9.6	6.4	8	9.6	kΩ
Input Offset Voltage			±0.5			±0.2			±0.5	mV
FREQUENCY RESPONSE[4]										
Bandwidth for 1% additional error (0.09dB)										
V_{IN} = 20mV		11			11			11		kHz
V_{IN} = 200mV		66			66			66		kHz
V_{IN} = 2V		200			200			200		kHz
± 3dB Bandwidth										
V_{IN} = 20mV		150			150			150		kHz
V_{IN} = 200mV		1			1			1		MHz
V_{IN} = 2V		8			8			8		MHz
OUTPUT CHARACTERISTICS										
Offset Voltage			±1			±0.5			±1	mV
vs. Temperature		±0.05	±0.089		±0.04	±0.056		±0.04	±0.07	mV/°C
Voltage Swing, ± 15V Supply, 2kΩ Load	0 to +12.0	+13.5		0 to +12.0	+13.5		0 to +12.0	+13.5		V
Voltage Swing, ± 3V Supply, 2kΩ Load	0 to +2	+2.2		0 to +2	+2.2		0 to +2	+2.2		V
Output Current	6			6			6			mA
Short Circuit Current		20			20			20		mA
Resistance, Chip Select "High"		0.5			0.5			0.5		Ω
Resistance, Chip Select "Low"		100			100			100		kΩ
dB OUTPUT										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.5			±0.3			±0.5		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33			+0.33		% of Reading/°C
		−0.033			−0.033			−0.033		dB/°C
I_{REF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	µA
I_{REF} Range	1		100	1		100	1		100	µA
BUFFER AMPLIFIER										
Input and Output Voltage Range	−V_S to (+V_S −2.5V)			−V_S to (+V_S −2.5V)			−V_S to (+V_S −2.5V)			V
Input Offset Voltage		±0.8	±2		±0.5	±1		±0.8	±2	mV
Input Current		±2	±10		±2	±5		±2	±10	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130µA)			(+5mA, −130µA)			(+5mA, −130µA)			
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[5]		5			5			5		V/µs
DENOMINATOR INPUT										
Input Range		0 to +10			0 to +10			0 to +10		V
Input Resistance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage		±0.2	±0.5		±0.2	±0.5		±0.2	±0.5	mV
CHIP SELECT PROVISION (CS)										
rms "ON" Level	Open or +2.4V<V_C<+V_S			Open or +2.4V<V_C<+V_S			Open or +2.4V<V_C<+V_S			
rms "OFF" Level	V_C<+0.2V			V_C<+0.2V			V_C<+0.2V			
I_{OUT} of Chip Select										
CS "LOW"	10			10			10			µA
CS "HIGH"	Zero			Zero			Zero			
On Time Constant	10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})			
Off Time Constant	10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})			
POWER SUPPLY										
Operating Voltage Range	±3.0		±18	±3.0		±18	±3.0		±18	V
Quiescent Current		2.2	3		2.2	3		2.2	3	mA
Standby Current		350	450		350	450		350	450	µA

Model	AD637J Min	AD637J Typ	AD637J Max	AD637K Min	AD637K Typ	AD637K Max	AD637S Min	AD637S Typ	AD637S Max	Units
PACKAGE OPTIONS[6]										
TO-116 (D-14)		AD637JD			AD637KD			AD637SD		
Cerdip (Q-14)		AD637JQ			AD637KQ			N/A		
SOIC (R-16)		AD637JR								
TRANSISTOR COUNT		107			107			107		

NOTES
[1]Accuracy specified 0-7V rms dc with AD637 connected as shown in Figure 2.
[2]Nonlinearity is defined as the maximum deviation from the straight line connecting the readings at 10mV and 2V.
[3]Error vs. crest factor is specified as additional error for 1V rms.
[4]Input voltages are expressed in volts rms. % are in % of reading.
[5]With external 2kΩ pull down resistor tied to $-V_S$.
[6]See Section 20 for package outline information.
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

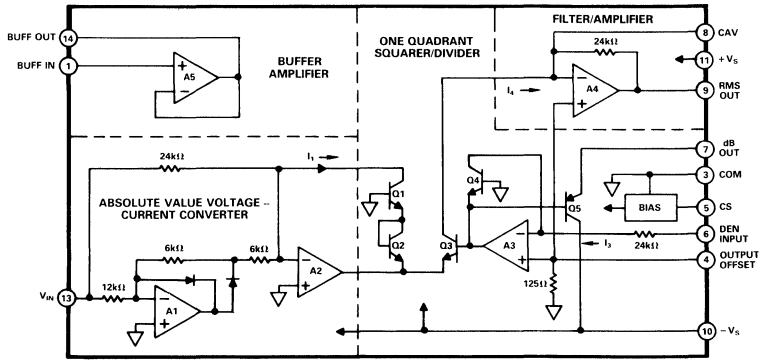


Figure 1. Simplified Schematic

ORDERING GUIDE

Temperature Range	Side Brazed Ceramic DIP	Ceramic DIP	Plastic SOIC
Commercial 0 to +70°C	AD637JD AD637KD	AD637JQ AD637KQ	AD637JR
Military −55°C to +125°C	AD637SD AD637SD/883B	AD637SQ AD637SQ/883B	

"J" and "S" Grade Chips are also available.
A Standard Military Drawing, 5962-89637, is also available.

FUNCTIONAL DESCRIPTION

The AD637 embodies an implicit solution of the rms equation that overcomes the inherent limitations of straightforward rms computation. The actual computation performed by the AD637 follows the equation

$$V\ rms = Avg\left[\frac{V_{IN}^2}{V\ rms}\right]$$

Figure 1 is a simplified schematic of the AD637, it is subdivided into four major sections; absolute value circuit (active rectifier), square/divider, filter circuit and buffer amplifier. The input voltage V_{IN} which can be ac or dc is converted to a unipolar current I1 by the active rectifier A1, A2. I1 drives one input of the squarer divider which has the transfer function

$$I_4 = \frac{I_1^2}{I_3}$$

The output current of the squarer/divider, I4 drives A4 which forms a low pass filter with the external averaging capacitor. If the RC time constant of the filter is much greater than the longest period of the input signal than A4s output will be proportional to the average of I4. The output of this filter amplifier is used by A3 to provide the denominator current I3 which equals Avg. I4 and is returned to the squarer/divider to complete the implicit rms computation.

$$I_4 = Avg\left[\frac{I_1^2}{I_4}\right] = I_1\ rms$$

and

$$V_{OUT} = V_{IN}\ rms$$

If the averaging capacitor is omitted the AD637 will compute the absolute value of the input signal. A nominal 5pF capacitor should be used to insure stability. The circuit operates identically to that of the rms configuration except that I3 is now equal to I4 giving

$$I_4 = \frac{I_1^2}{I_4}$$

$$I_4 = |I_1|$$

The denominator current can also be supplied externally by providing a reference voltage, V_{REF}, to pin 6. The circuit operates identically to the rms case except that I3 is now proportional to V_{REF}. Thus:

$$I_4 = Avg\ \frac{I_1^2}{I_3}$$

and

$$V_O = \frac{V_{IN}^2}{V_{DEN}}$$

This is the mean square of the input signal.

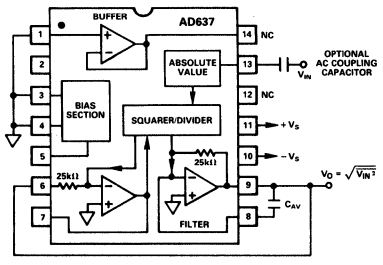


Figure 2. Standard RMS Connection

STANDARD CONNECTION

The AD637 is simple to connect for a majority of rms measurements. In the standard rms connection shown in Figure 2, only a single external capacitor is required to set the averaging time constant. In this configuration, the AD637 will compute the true rms of any input signal. An averaging error, the magnitude of which will be dependent on the value of the averaging capacitor, will be present at low frequencies. For example, if the filter capacitor C_{AV}, is 4μF this error will be 0.1% at 10Hz and increases to 1% at 3Hz. If it is desired to measure only ac signals the AD637 can be ac coupled through the addition of a nonpolar capacitor in series with the input as shown in Figure 2.

The performance of the AD637 is tolerant of minor variations in the power supply voltages, however, if the supplies being used exhibit a considerable amount of high frequency ripple it is advisable to bypass both supplies to ground through a 0.1μF ceramic disc capacitor placed as close to the device as possible.

The output signal range of the AD637 is a function of the supply voltages, as shown in Figure 3. The output signal can be used buffered or nonbuffered depending on the characteristics of the load. If no buffer is needed, tie buffer input (pin 1) to common. The output of the AD637 is capable of driving 5mA into a 2kΩ load without degrading the accuracy of the device.

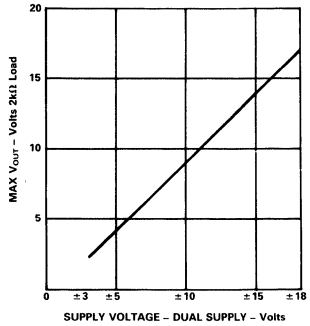


Figure 3. AD637 max V_{OUT} vs. Supply Voltage

CHIP SELECT

The AD637 includes a chip select feature which allows the user to decrease the quiescent current of the device from 2.2mA to 350μA. This is done by driving the CS, pin 5, to below 0.2V dc. Under these conditions, the output will go into a high impedance state. In addition to lowering power consumption, this feature permits bussing the outputs of a number of AD637s to form a wide bandwidth rms multiplexer. If the chip select is not being used, pin 5 should be tied high or left floating.

OPTIONAL TRIMS FOR HIGH ACCURACY

The AD637 includes provisions to allow the user to trim out both output offset and scale factor errors. These trims will result in significant reduction in the maximum total error as shown in Figure 4. This remaining error is due to a nontrimmable input offset in the absolute value circuit and the irreducible nonlinearity of the device.

The trimming procedure on the AD637 is as follows:

1. Ground the input signal, V_{IN} and adjust R1 to give 0V output from pin 9. Alternatively R1 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input to V_{IN}, using either a dc or a calibrated ac signal, trim R3 to give the correct output

at pin 9, i.e., 1V dc should give 1.000V dc output. Of course, a 2V peak-to-peak sine wave should give 0.707V dc output. Remaining errors are due to the nonlinearity.

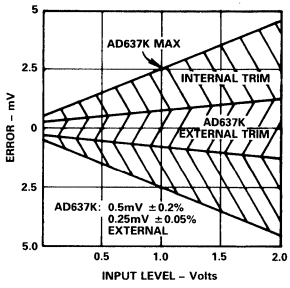


Figure 4. Max Total Error vs. Input Level AD637K Internal and External Trims

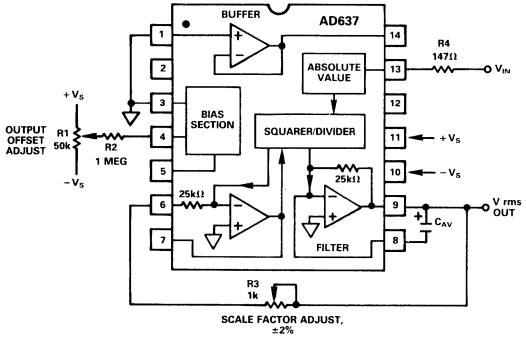


Figure 5. Optional External Gain and Offset Trims

CHOOSING THE AVERAGING TIME CONSTANT

The AD637 will compute the true rms value of both dc and ac input signals. At dc the output will track the absolute value of the input exactly; with ac signals the AD637's output will approach the true rms value of the input. The deviation from the ideal rms value is due to an averaging error. The averaging error is comprised of an ac and dc component. Both components are functions of input signal frequency f, and the averaging time constant τ (τ: 25ms/μF of averaging capacitance). As shown in Figure 6, the averaging error is defined as the peak value of the ac component, ripple, plus the value of the dc error.

The peak value of the ac ripple component of the averaging error is defined approximately by the relationship:

$$\frac{50}{6.3\tau f} \text{ in \% of reading where } (\tau > 1/f)$$

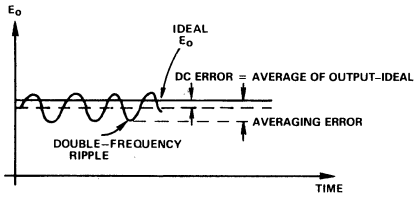


Figure 6. Typical Output Waveform for a Sinusoidal Input

This ripple can add a significant amount of uncertainty to the accuracy of the measurement being made. The uncertainty can be significantly reduced through the use of a post filtering network or by increasing the value of the averaging capacitor.

The dc error appears as a frequency dependent offset at the output of the AD637 and follows the equation:

$$\frac{1}{0.16 + 6.4\tau^2 f^2} \text{ in \% of reading}$$

Since the averaging time constant, set by C_{AV}, directly sets the time that the rms converter "holds" the input signal during computation, the magnitude of the dc error is determined only by C_{AV} and will not be affected by post filtering.

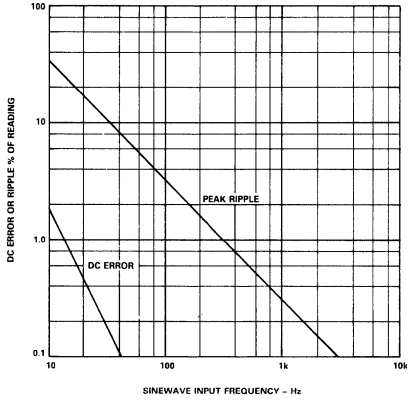


Figure 7. Comparison of Percent dc Error to the Percent Peak Ripple over Frequency Using the AD637 in the Standard RMS Connection with a 1×μF C_{AV}

The ac ripple component of averaging error can be greatly reduced by increasing the value of the averaging capacitor. There are two major disadvantages to this: first, the value of the averaging capacitor will become extremely large and second, the settling time of the AD637 increases in direct proportion to the value of the averaging capacitor (Ts = 115ms/μF of averaging capacitance). A preferrable method of reducing the ripple is through the use of the post filter network, shown in Figure 8. This network can be used in either a one or two pole configuration. For most applications the single pole filter will give the best overall compromise between ripple and settling time.

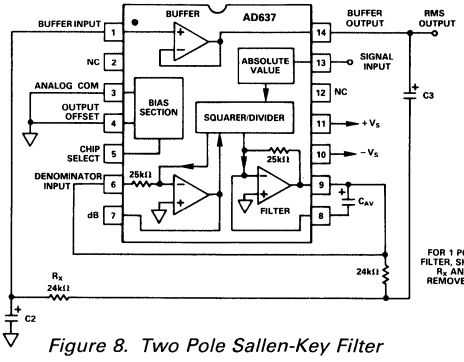


Figure 8. Two Pole Sallen-Key Filter

Figure 9a shows values of C_{AV} and the corresponding averaging error as a function of sine-wave frequency for the standard rms connection. The 1% settling time is shown on the right side of the graph.

Figure 9b shows the relationship between averaging error, signal frequency settling time and averaging capacitor value. This graph is drawn for filter capacitor values of 3.3 times the averaging capacitor value. This ratio sets the magnitude of the ac and dc errors equal at 50Hz. As an example, by using a 1μF averaging capacitor and a 3.3μF filter capacitor the ripple for a 60Hz input signal will be reduced from 5.3% of reading using the averaging capacitor alone to 0.15% using the single pole filter. This gives a factor of thirty reduction in ripple and yet the settling time would only increase by a factor of three. The values of C_{AV} and C_2, the filter capacitor, can be calculated for the desired value of averaging error and settling time by using Figure 9b.

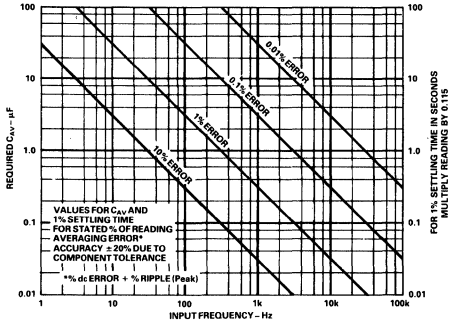


Figure 9a.

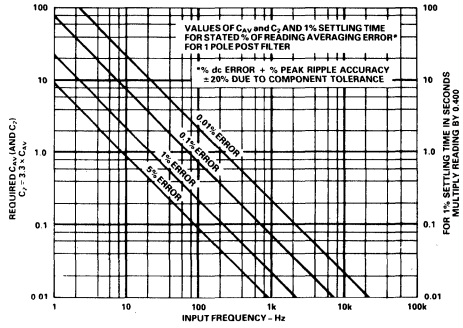


Figure 9b.

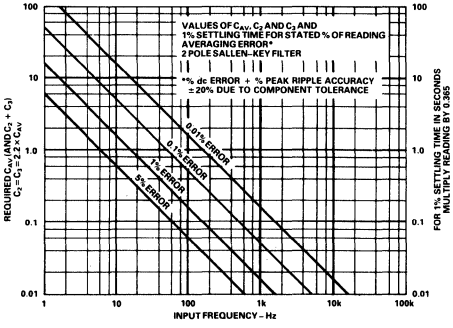


Figure 9c.

The symmetry of the input signal also has an effect on the magnitude of the averaging error. Table I gives practical component values for various types of 60Hz input signals. These capacitor values can be directly scaled for frequencies other than 60Hz, i.e., for 30Hz double these values, for 120Hz they are halved.

	Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum R × C_{AV} Time Constant	Recommended C_{AV} and C2 Values for 1% Averaging Error in 60Hz with T = 16.6ms		1% Settling Time
				Recommended Standard Value C_{AV}	Recommended Standard Value C2	
A	Symmetrical Sine Wave	1/2T	1/2T	0.47μF	1.5μF	181ms
B	Sine Wave with dc Offset		T	0.82μF	2.7μF	325ms
C	Pulse Train Waveform		10(T – T_2)	6.8μF	22μF	2.67sec
D			10(T – 2T_2)	5.6μF	18μF	2.17sec

Table I. Practical Values of C_{AV} and C2 for Various Input Waveforms

For applications that are extremely sensitive to ripple, the two pole configuration is suggested. This configuration will minimize capacitor values and settling time while maximizing performance.

Figure 9c can be used to determine the required value of C_{AV}, C_2 and C_3 for the desired level of ripple and settling time.

FREQUENCY RESPONSE

The frequency response of the AD637 at various signal levels is shown in Figure 10. The dashed lines show the upper frequency limits for 1%, 10% and ±3dB of additional error. For example, note that for 1% additional error with a 2V rms input the highest frequency allowable is 200kHz. A 200mV signal can be measured with 1% error at signal frequencies up to 100kHz.

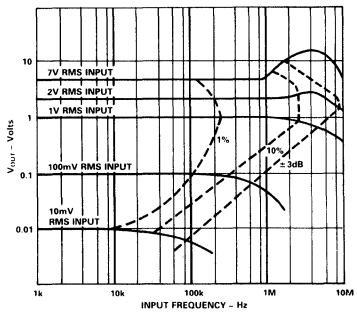


Figure 10. Frequency Response

To take full advantage of the wide bandwidth of the AD637 care must be taken in the selection of the input buffer amplifier. To insure that the input signal is accurately presented to the converter, the input buffer must have a −3dB bandwidth that is wider than that of the AD637. A point that should not be overlooked is the importance of slew rate in this application. For example, the minimum slew rate required for a 1V rms 5MHz sine-wave input signal is 44V/μs. The user is cautioned that this is the minimum rising or falling slew rate and that care must be exercised in the selection of the buffer amplifier as

some amplifiers exhibit a two-to-one difference between rising and falling slew rates. The AD845 is recommended as a precision input buffer.

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (≤2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

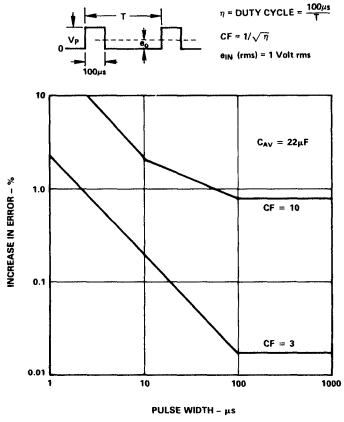


Figure 11. AD637 Error vs. Pulse Width Rectangular Pulse

Figure 12 is a curve of additional reading error for the AD637 for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100µs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

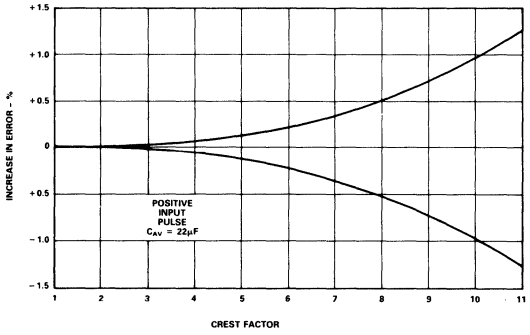


Figure 12. Additional Error vs. Crest Factor

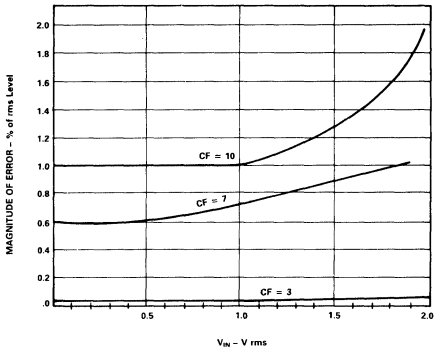


Figure 13. Error vs. RMS Input Level for Three Common Crest Factors

CONNECTION FOR dB OUTPUT

Another feature of the AD637 is the logarithmic or decibel output. The internal circuit which computes dB works well over a 60dB range. The connection for dB measurement is shown in Figure 14. The user selects the 0dB level by setting R1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer/divider circuit at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C temperature drift of the dB circuit. The special T.C. resistor R3 is available from Tel Labs in Londenderry, New Hampshire (model Q-81) and from Precision Resistor Inc., Hillside, N.J. (model PT146).

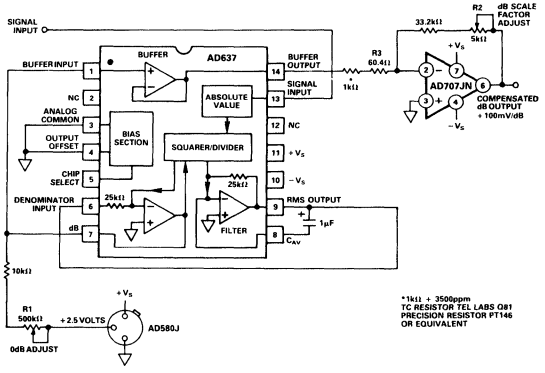


Figure 14. dB Connection

dB CALIBRATION

1. Set V_{IN} = 1.00V dc or 1.00V rms
2. Adjust R1 for 0dB out = 0.00V
3. Set V_{IN} = 0.1V dc or 0.10V rms
4. Adjust R2 for dB out = −2.00V

Any other dB reference can be used by setting V_{IN} and R1 accordingly.

LOW FREQUENCY MEASUREMENTS

If the frequencies of the signals to be measured are below 10Hz, the value of the averaging capacitor required to deliver even 1% averaging error in the standard rms connection becomes extremely large. The circuit shown in Figure 15 shows an alternative method of obtaining low frequency rms measurements. The averaging time constant is determined by the product of R and C_{AV1}, in this circuit 0.5s/μF of C_{AV}. This circuit permits a 20:1 reduction in the value of the averaging capacitor, permitting the use of high quality tantalum capacitors. It is suggested that the two pole Sallen-Key filter shown in the diagram be used to obtain a low ripple level and minimize the value of the averaging capacitor.

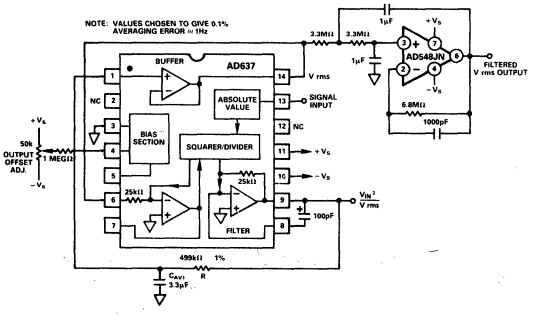


Figure 15. AD637 as a Low Frequency rms Converter

If the frequency of interest is below 1Hz, or if the value of the averaging capacitor is still too large, the 20:1 ratio can be increased. This is accomplished by increasing the value of R. If this is done it is suggested that a low input current, low offset voltage amplifier like the AD548 be used instead of the internal buffer amplifier. This is necessary to minimize the offset error introduced by the combination of amplifier input currents and the larger resistance.

VECTOR SUMMATION

Vector summation can be accomplished through the use of two AD637s as shown in Figure 16. Here the averaging capacitors are omitted (nominal 100pF capacitors are used to insure stability of the filter amplifier), and the outputs are summed as shown. The output of the circuit is

$$V_O = \sqrt{V_X^2 + V_Y^2}$$

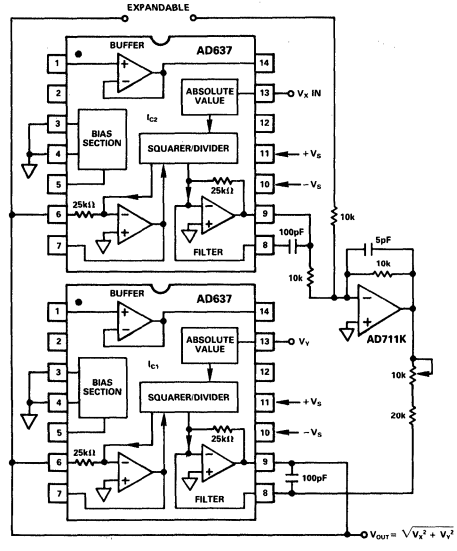


Figure 16. AD637 Vector Sum Configuration

This concept can be expanded to include additional terms by feeding the signal from pin 9 of each additional AD637 through a 10kΩ resistor to the summing junction of the AD711, and tying all of the denominator inputs (pin 6) together.

If C_{AV} is added to IC1 in this configuration the output is $\sqrt{V_X^2 + V_Y^2}$ If the averaging capacitor is included on both IC1 and IC2 the output will be $\sqrt{\overline{V_X^2} + \overline{V_Y^2}}$

This circuit has a dynamic range of 10V to 10mV and is limited only by the 0.5mV offset voltage of the AD637. The useful bandwidth is 100kHz.

Low Cost, Low Power, True RMS-to-DC Converter

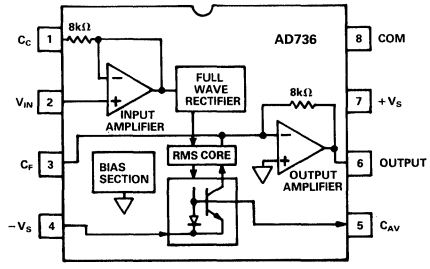
AD736

FEATURES

COMPUTES
- **True RMS Value**
- **Average Rectified Value**
- **Absolute Value**

PROVIDES
- **200mV Full-Scale Input Range**
- **High Input Impedance of $10^{12}\Omega$**
- **Low Input Bias Current: 25pA max**
- **High Accuracy: ±0.3mV ±0.3% of Reading**
- **RMS Conversion with Signal Crest Factors Up to 5**
- **Wide Power Supply Range: +2.8V, −3.2V to ±16.5V**
- **Low Power: 200μA max Supply Current**
- **Buffered Voltage Output**
- **No External Trims Needed for Specified Accuracy**
- **AD737 – An Unbuffered Voltage Output Version with Chip Power Down Is Also Available**

AD736 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD736 is a low power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of ±0.3mV ±0.3% of reading with sine-wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD736 offers higher accuracy at equal or lower cost.

The AD736 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD736 can resolve input signal levels of 100μV rms or less, despite variations in temperature or supply voltage. High acccuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200mV full-scale input level.

The AD736 has its own output buffer amplifier, thereby providing a great deal of design flexibility. Requiring only 200μA of power supply current, the AD736 is optimized for use in portable multimeters and other battery powered applications.

The AD736 allows the choice of two signal input terminals: a high impedance ($10^{12}\Omega$) FET input which will directly interface with high Z input attenuators and a low impedance (8kΩ) input which allows the measurement of 300mV input levels, while operating from the minimum power supply voltage of +2.8V, −3.2V. The two inputs may be used either singly or differentially.

The AD736 achieves a 1% of reading error bandwidth exceeding 10kHz for input amplitudes from 20mV rms to 200mV rms while consuming only 1mW.

The AD736 is available in four performance grades. The AD736J and AD736K grades are rated over the commercial temperature range of 0 to +70°C. The AD736A and AD736B grades are rated over the industrial temperature range of −40°C to +85°C.

The AD736 is available in three low-cost 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

PRODUCT HIGHLIGHTS

1. The AD736 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD736 to perform true rms measurement.
3. The low power consumption of 1mW makes the AD736 suitable for many battery powered applications.
4. A high input impedance of $10^{12}\Omega$ eliminates the need for an external buffer when interfacing with input attenuators.
5. A low impedance input is available for those applications requiring up to 300mV rms input signal operating from low power supply voltages.

SPECIFICATIONS (@ +25°C ±5V supplies, ac coupled with 1kHz sine-wave input applied unless otherwide noted.)

Model	Conditions	AD736J/A Min	AD736J/A Typ	AD736J/A Max	AD736K/B Min	AD736K/B Typ	AD736K/B Max	Units
TRANSFER FUNCTION			$V_{OUT} = \sqrt{Avg.(V_{IN}^2)}$			$V_{OUT} = \sqrt{Avg.(V_{IN}^2)}$		
CONVERSION ACCURACY	1kHz Sine Wave							
Total Error, Internal Trim[1]	ac Coupled Using C_C							
All Grades	0-200mV rms		0.3/0.3	**0.5/0.5**		0.2/0.2	**0.3/0.3**	±mV/±% of Reading
	200mV-1V rms		−1.2	**±2.0**		−1.2	**±2.0**	% of Reading
T_{min}-T_{max}								
A&B Grades	@ 200mV rms			**0.7/0.7**			**0.5/0.5**	±mV/±% of Reading
J&K Grades	@ 200mV rms		0.007			0.007		±% of Reading/°C
vs. Supply Voltage								
@ 200mV rms Input	V_S = ±5V to ±16.5V	**0**	+0.06	**+0.1**	**0**	+0.06	**+0.1**	%/V
@ 200mV rms Input	V_S = ±5V to ±3V	**0**	−0.18	**−0.3**	**0**	−0.18	**−0.3**	%/V
dc Reversal Error, dc Coupled	@ 600mV dc		1.3	**2.5**		1.3	**2.5**	% of Reading
Nonlinearity[2], 0-200mV	@ 100mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0-200mV rms		0.1/0.5			0.1/0.3		±mV/±% of Reading
ERROR vs. CREST FACTOR[3]								
Crest Factor 1 to 3	C_{AV}, C_F = 100µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S = +2.8V, −3.2V			**200**			**200**	mV rms
Continuous rms Level	V_S = ±5V to ±16.5V			**1**			**1**	V rms
Peak Transient Input	V_S = +2.8V, −3.2V	**±0.9**			**±0.9**			V
Peak Transient Input	V_S = ±5V		±2.7			±2.7		V
Peak Transient Input	V_S = ±16.5V	**±4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	V_S = ±3V to ±16.5V		1	**25**		1	**25**	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8V, −3.2V			300			300	mV rms
Continuous rms Level	V_S = ±5V to ±16.5V			1			1	V rms
Peak Transient Input	V_S = +2.8V, −3.2V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous Non-Destructive Input	All Supply Voltages			±12			±12	V p-p
Input Offset Voltage[4]	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**150**		50	**150**	µV/V
vs. Supply	V_S = ±5V to ±3V		80			80		µV/V
OUTPUT CHARACTERISTICS								
Output Offset Voltage								
J&K Grades			±0.1	**±0.5**		±0.1	**±0.3**	mV
A&B Grades				**±0.5**			**±0.3**	mV
vs. Temperature			1	20		1	20	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**130**		50	**130**	µV/V
	V_S = ±5V to ±3V		50			50		µV/V
Output Voltage Swing								
2kΩ Load	V_S = +2.8V, −3.2V	0 to +1.6	+1.7		0 to +1.6	+1.7		V
2kΩ Load	V_S = ±5V	0 to +3.6	+3.8		0 to +3.6	+3.8		V
2kΩ Load	V_S = ±16.5V	**0 to +4**	+5		**0 to +4**	+5		V
No Load	V_S = ±16.5V	**0 to +4**	+12		**0 to +4**	+12		V
Output Current		2			2			mA
Short-Circuit Current			3			3		mA
Output Resistance	@ dc		0.2			0.2		Ω
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			37			37		kHz
V_{IN} = 200mV rms			33			33		kHz
±3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			170			170		kHz
V_{IN} = 200mV rms			190			190		kHz

Model	Conditions	AD736J/A Min	AD736J/A Typ	AD736J/A Max	AD736K/B Min	AD736K/B Typ	AD736K/B Max	Units
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			90			90		kHz
V_{IN} = 200mV rms			90			90		kHz
± 3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			350			350		kHz
V_{IN} = 200mV rms			460			460		kHz
POWER SUPPLY								
Operating Voltage Range		+2.8, −3.2	±5	±16.5	+2.8, −3.2	±5	±16.5	Volts
Quiescent Current	Zero Signal		160	**200**		160	**200**	μA
200mV rms, No Load	Sine-Wave Input		230	270		230	270	μA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD736J			AD736K		
Industrial (−40°C to +85°C)			AD736A			AD736B		
PACKAGE OPTIONS[5]								
8-Pin Plastic Mini-DIP (N-8)			AD736JN			AD736KN		
8-Pin Plastic SO (R-8)			AD736JR			AD736KR		
8-Pin Cerdip (Q-8)			AD736AQ			AD736BQ		

NOTES
[1]Accuracy is specified with the AD736 connected as shown in Figure 16 with capacitor C_C.
[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200mV rms. Output offset voltage is adjusted to zero.
[3]Error vs. Crest Factor is specified as additional error for a 200mV rms signal. C.F. = V_{PEAK}/V rms.
[4]DC offset does not limit ac resolution.
[5]See Section 20 for package outline information.

Specifications are subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final electrical test.
Results from those tests are used to calculate outgoing quality levels.

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ORDERING GUIDE

Temperature Range	Plastic Mini-DIP	Ceramic Mini-DIP	Plastic SOIC
Commerical 0 to +70°C	AD736JN AD736KN		AD736JR AD736KR
Industrial −40°C to +85°C		AD736AQ S736BQ	

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±16.5V
Internal Power Dissipation[2] 200mW
Input Voltage . . . . . ±V_S
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . +V_S and −V_S
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD736J/K . . . . . 0 to +70°C
AD736A/B . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W
8-Pin Cerdip Package: θ_{JA} = 110°C/W
8-Pin Small Outline Package: θ_{JA} = 155°C/W

Typical Characteristics

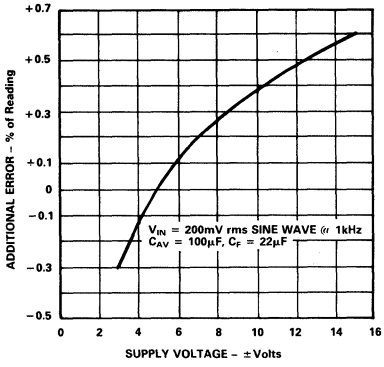

Figure 1. Additional Error vs. Supply Voltage

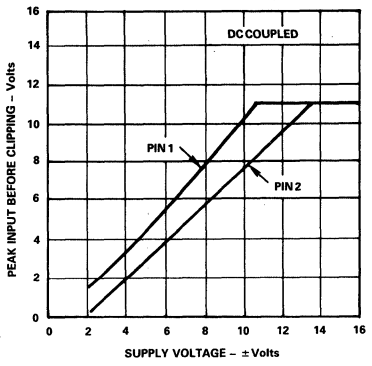

Figure 2. Maximum Input Level vs. Supply Voltage

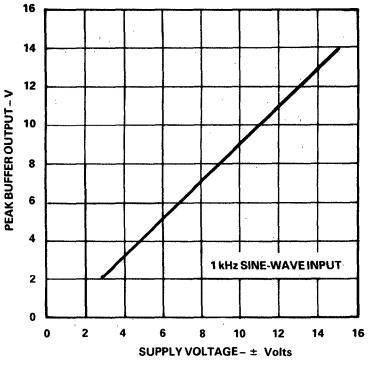

Figure 3. Peak Buffer Output vs. Supply Voltage

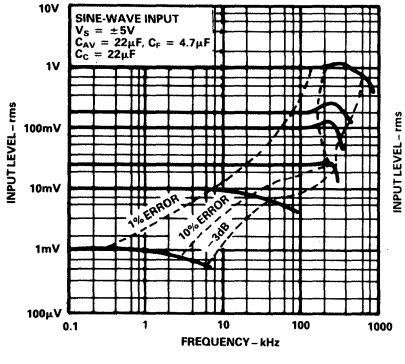

Figure 4. Frequency Response Driving Pin 1

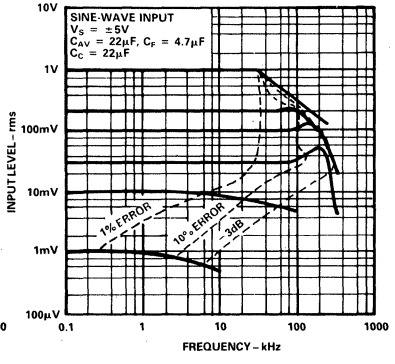

Figure 5. Frequency Response Driving Pin 2

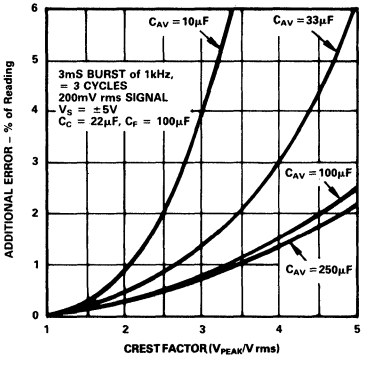

Figure 6. Additional Error vs. Crest Factor vs. C_{AV}

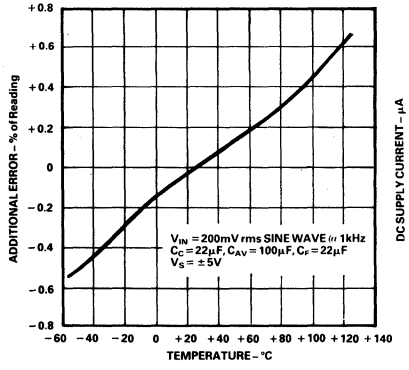

Figure 7. Additional Error vs. Temperature

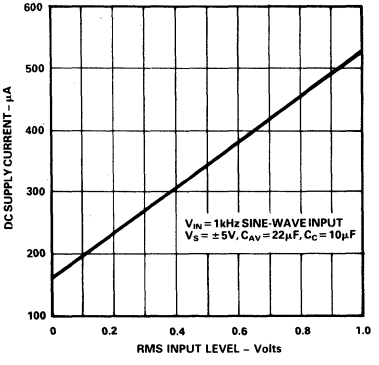

Figure 8. DC Supply current vs. RMS Input Level

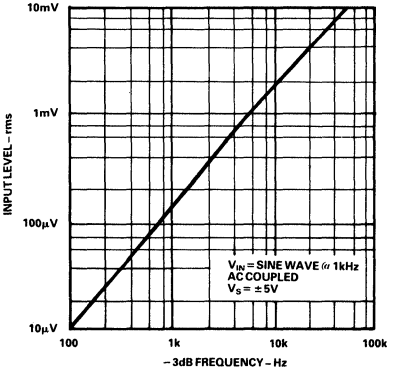

Figure 9. –3dB Frequency vs. RMS Input Level (Pin 2)

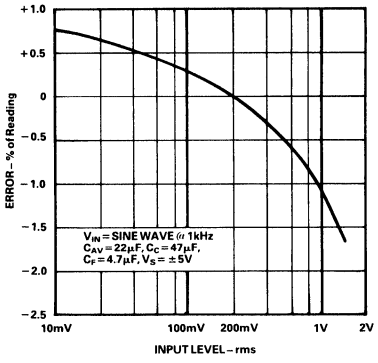

Figure 10. Error vs. RMS Input Voltage (Pin 2), Output Buffer Offset Is Adjusted To Zero

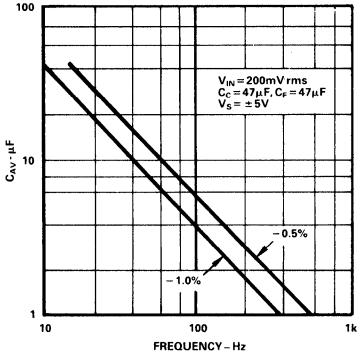

Figure 11. C_{AV} vs. Frequency for Specified Averaging Error

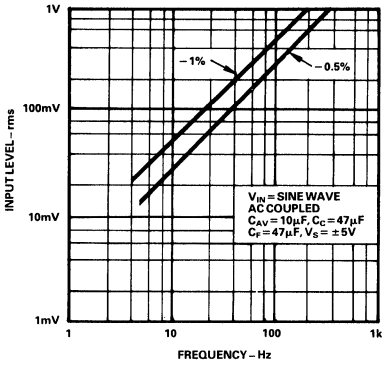

Figure 12. RMS Input Level vs. Frequency for Specified Averaging Error

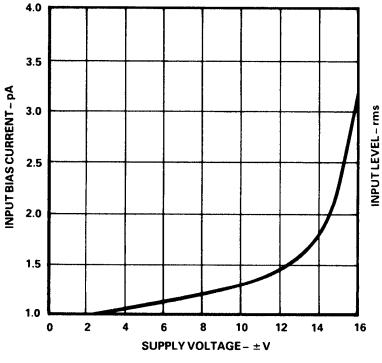

Figure 13. Pin 2 Input Bias Current vs. Supply Voltage

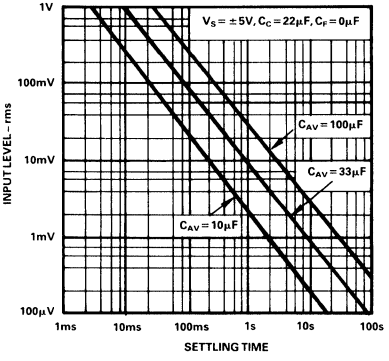

Figure 14. Settling Time vs. RMS Input Level for Various Values of C_{AV}

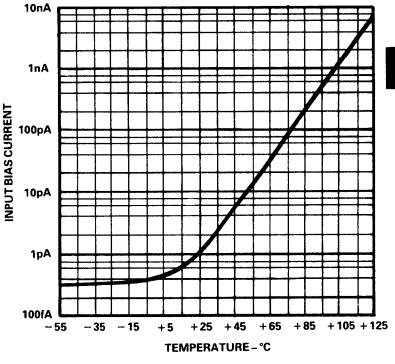

Figure 15. Pin 2 Input Bias Current vs. Temperature

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CALCULATING SETTLING TIME USING FIGURE 14

The graph of Figure 14 may be used to closely approximate the time required for the AD736 to settle when its input level is reduced in amplitude. The *net time* required for the rms converter to settle will be the *difference* between two times extracted from the graph – the initial time minus the final settling time. As an example, consider the following conditions: a 33µF averaging capacitor, an initial rms input level of 100mV and a final (reduced) input level of 1mV. From Figure 14, the initial settling time (where the 100mV line intersects the 33µF line) is around 80ms. The settling time corresponding to the new or final input level of 1mV is approximately 8 seconds. Therefore, the net time for the circuit to settle to its new value will be 8 seconds minus 80ms which is 7.92 seconds. Note that, because of the smooth decay characteristic inherent with a capacitor/diode combination, this is the total settling time to the final value (i.e., *not* the settling time to 1%, 0.1%, etc., of final value). Also, this graph provides the worst case settling time, since the AD736 will settle very quickly with increasing input levels.

Applying the AD736

TYPES OF AC MEASUREMENT

The AD736 is capable of measuring ac signals by operating as either an average responding or a true rms-to-dc converter. As its name implies, an average responding converter computes the average absolute value of an ac (or ac and dc) voltage or current by full wave rectifing and low-pass filtering the input signal; this will approximate the average. The resulting output, a dc "average" level, is then scaled by adding (or reducing) gain; this scale factor converts the dc average reading to an rms equivalent value for the waveform being measured. For example, the average absolute value of a sine-wave voltage is 0.636 that of V_{PEAK}; the corresponding rms value is 0.707 times V_{PEAK}. Therefore, for sine-wave voltages, the required scale factor is 1.11 (0.707 divided by 0.636).

In contrast to measuring the "average" value, true rms measurement is a "universal language" among waveforms, allowing the magnitudes of all types of voltage (or current) waveforms to be compared to one another and to dc. RMS is a direct measure of the power or heating value of an ac voltage compared to that of dc: an ac signal of 1 volt rms will produce the same amount of heat in a resistor as a 1 volt dc signal.

Mathematically, the rms value of a voltage is defined (using a simplified equation) as:

$$V \text{ rms} = \sqrt{\text{Avg. } (V^2)}$$

This involves squaring the signal, taking the average, and then obtaining the square root. True rms converters are "smart rectifiers": they provide an accurate rms reading regardless of the type of waveform being measured. However, average responding converters can exhibit very high errors when their input signals deviate from their precalibrated waveform; the magnitude of the error will depend upon the type of waveform being measured. As an example, if an average responding converter is calibrated to measure the rms value of sine-wave voltages, and then is used to measure either symmetrical square waves or dc voltages, the converter will have a computational error 11% (of reading) higher than the true rms value (see Table I).

AD736 THEORY OF OPERATION

As shown by Figure 16, the AD736 has five functional subsections: input amplifier, full-wave rectifier, rms core, output amplifier and bias sections. The FET input amplifier allows both a high impedance, buffered input (Pin 2) or a low impedance, wide-dynamic-range input (Pin 1). The high impedance input, with its low input bias current, is well suited for use with high impedance input attenuators.

The output of the input amplifier drives a full wave precision rectifier, which in turn, drives the rms core. It is in the core that the essential rms operations of squaring, averaging and square rooting are performed, using an external averaging capacitor, C_{AV}. Without C_{AV}, the rectified input signal travels through the core unprocessed, as is done with the average responding connection (Figure 17).

A final subsection, an output amplifier, buffers the output from the core and also allows optional low-pass filtering to be performed via external capacitor, C_F, connected across the feedback path of the amplifier. In the average responding connection, this is where all of the averaging is carried out. In the rms circuit, this additional filtering stage helps reduce any output ripple which was not removed by the averaging capacitor, C_{AV}.

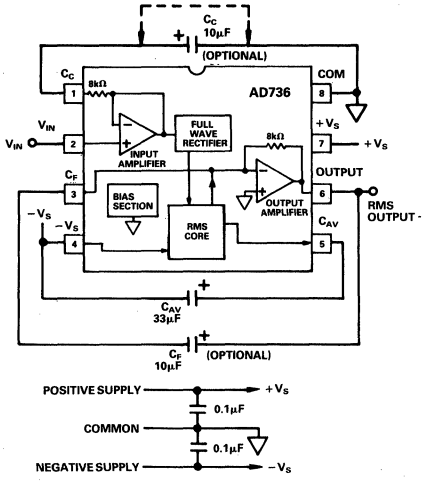


Figure 16. AD736 True RMS Circuit

Waveform Type 1 Volt Peak Amplitude	Crest Factor (V_{PEAK}/V rms)	True rms Value	Average Responding Circuit Calibrated to Read rms Value of Sine Waves Will Read	% of Reading Error* Using Average Responding Circuit
Undistorted Sine Wave	1.414	0.707V	0.707V	0%
Symmetrical Square Wave	1.00	1.00V	1.11V	+11.0%
Undistorted Triangle Wave	1.73	0.580V	0.555V	−2.1%
Gaussian Noise (98% of Peaks <1 V)	3	0.333	0.266	−20.2%
Rectangular Pulse Train	2	0.5V	0.25V	−50%
	10	0.1V	0.01V	−99%
SCR Waveforms 50% Duty Cycle	2	0.495V	0.354V	−28%
25% Duty Cycle	4.7	0.212V	0.150V	−30%

*% of Reading Error = $\frac{\text{Average Responding Value} - \text{True rms Value}}{\text{True rms Value}} \times 100\%$

Table I. Error Introduced by an Average Responding Circuit When Measuring Common Waveforms

RMS MEASUREMENT – CHOOSING THE OPTIMUM VALUE FOR C_{AV}

Since the external averaging capacitor, C_{AV}, "holds" the rectified input signal during rms computation, its value directly affects the accuracy of the rms measurement, especially at low frequencies. Furthermore, because the averaging capacitor appears across a diode in the rms core, the averaging time constant will increase exponentially as the input signal is reduced. This means that as the input level decreases, errors due to nonideal averaging will *reduce* while the time it takes for the circuit to settle to the new rms level will *increase*. Therefore, lower input levels allow the circuit to perform better (due to increased averaging) but increase the waiting time between measurements. Obviously, when selecting C_{AV}, a trade-off between computational accuracy and settling time is required.

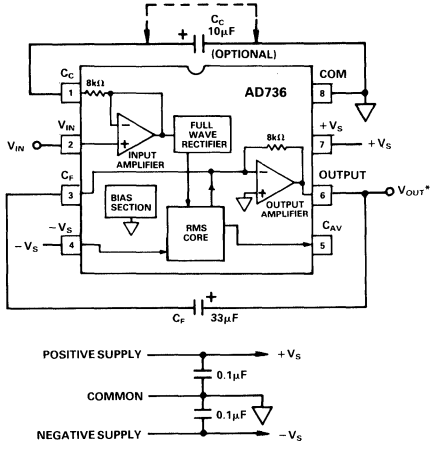


Figure 17. AD736 Average Responding Circuit

RAPID SETTLING TIMES VIA THE AVERAGE RESPONDING CONNECTION (FIGURE 17)

Because the average responding connection does not use the C_{AV} averaging capacitor, its settling time does not vary with input signal level; it is determined solely by the RC time constant of C_F and the internal 8kΩ resistor in the output amplifier's feedback path.

DC ERROR, OUTPUT RIPPLE, AND AVERAGING ERROR

Figure 18 shows the typical output waveform of the AD736 with a sine-wave input applied. As with all real-world devices, the ideal output of $V_{OUT} = V_{IN}$ is never exactly achieved; instead, the output contains both a dc and an ac error component.

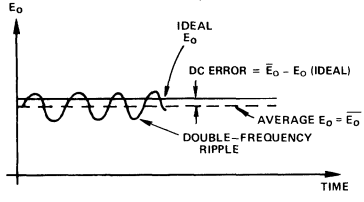


Figure 18. Output Waveform for Sine-Wave Input Voltage

As shown, the dc error is the difference between the average of the output signal (when all the ripple in the output has been removed by external filtering) and the ideal dc output. The dc error component is therefore set solely by the value of averaging capacitor used – *no* amount of post filtering (i.e., using a very large C_F) will allow the output voltage to equal its ideal value. The ac error component, an output ripple, may be easily removed by using a large enough post filtering capacitor, C_F.

In most cases, the combined magnitudes of both the dc and ac error components need to be considered when selecting appropriate values for capacitors C_{AV} and C_F. This combined error, representing the maximum uncertainty of the measurement is termed the "averaging error" and is equal to the peak value of the output ripple plus the dc error.

As the input frequency increases, both error components decrease rapidly: if the input frequency doubles, the dc error and ripple reduce to 1/4 and 1/2 their original values, respectively, and rapidly become insignificant.

AC MEASUREMENT ACCURACY AND CREST FACTOR

The crest factor of the input waveform is often overlooked when determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms amplitude (C.F. = V_{PEAK}/V rms). Many common waveforms, such as sine and triangle waves, have relatively low crest factors (≤2). Other waveforms, such as low duty cycle pulse trains and SCR waveforms, have high crest factors. These types of waveforms require a long averaging time constant (to average out the long time periods between pulses). Figure 6 shows the additional error vs. crest factor of the AD736 for various values of C_{AV}.

SELECTING PRACTICAL VALUES FOR INPUT COUPLING (C_C), AVERAGING (C_{AV}) AND FILTERING (C_F) CAPACITORS

Table II provides practical values of C_{AV} and C_F for several common applications.

Application	rms Input Level	Low Frequency Cutoff (–3dB)	Max Crest Factor	C_{AV}	C_F	Settling Time* to 1%
General Purpose rms Computation	0-1V	20Hz 200Hz	5 5	150µF 15µF	10µF 1µF	360ms 36ms
	0-200mV	20Hz 200Hz	5 5	33µF 3.3µF	10µF 1µF	360ms 36ms
General Purpose Average Responding	0-1V	20Hz 200Hz		None None	33µF 3.3µF	1.2sec 120ms
	0-200mV	20Hz 200Hz		None None	33µF 3.3µF	1.2sec 120ms
SCR Waveform Measurement	0-200mV	50Hz 60Hz	5 5	100µF 82µF	33µF 27µF	1.2sec 1.0sec
	0-100mV	50Hz 60Hz	5 5	50µF 47µF	33µF 27µF	1.2sec 1.0sec
Audio Applications						
Speech	0-200mV	300Hz	3	1.5µF	0.5µF	18ms
Music	0-100mV	20Hz	10	100µF	68µF	2.4sec

* Settling time is specified over the stated rms input level with the input signal increasing from zero. Settling times will be greater for decreasing amplitude input signals.

Table II. AD737 Capacitor Selection Chart

The input coupling capacitor, C_C, in conjunction with the 8kΩ internal input scaling resistor, determine the −3dB low frequency rolloff. This frequency, F_L is equal to:

$$F_L = \frac{1}{2\pi\,(8{,}000)\,(\text{The Value of } C_C \text{ in Farads})}$$

Note that at F_L, the amplitude error will be approximately −30% (−3dB) of reading. To reduce this error to 0.5% of reading, choose a value of C_C that sets F_L at one tenth the lowest frequency to be measured.

In addition, if the input voltage has more than 100mV of dc offset, than the ac coupling network shown in Figure 21 should be used in addition to capacitor C_C.

Applications Circuits

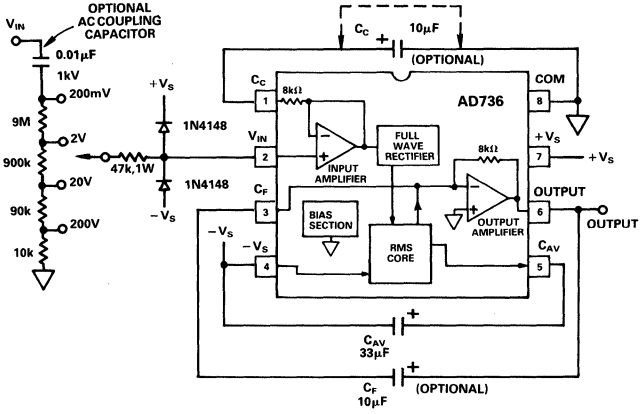


Figure 19. AD736 with a High Impedance Input Attenuator

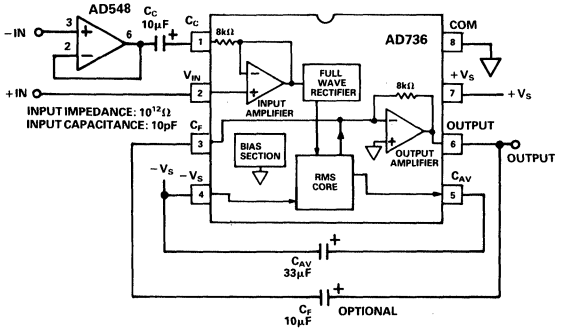


Figure 20. Differential Input Connection

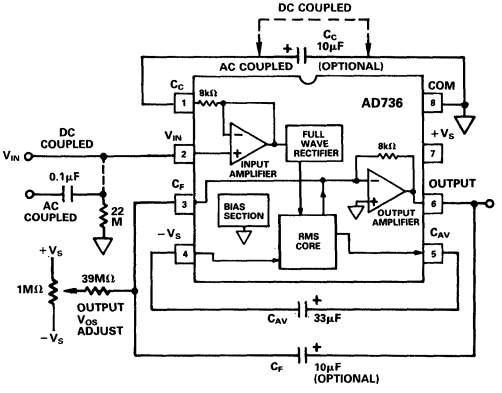


Figure 21. External Output V_{OS} Adjustment

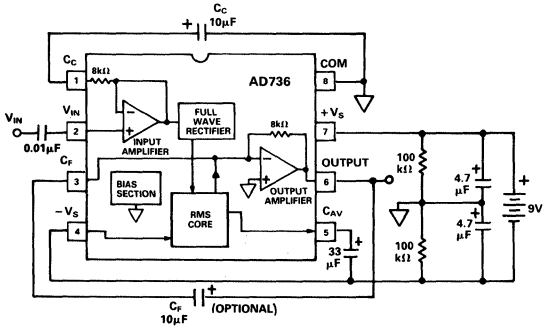


Figure 22. Battery Powered Option

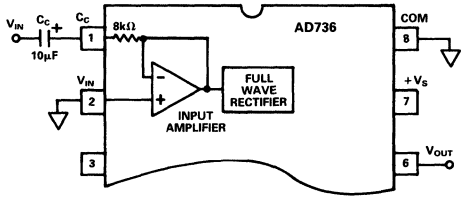


Figure 23. Low Z, AC Coupled Input Connection

ANALOG DEVICES

Low Cost, Low Power, True RMS-to-DC Converter

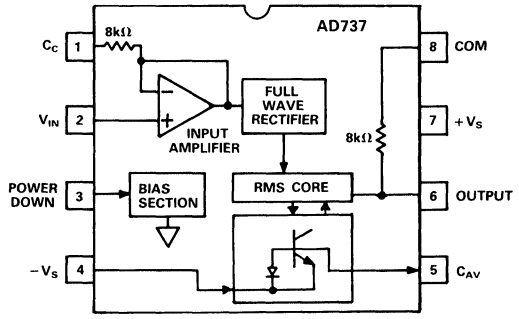
AD737

FEATURES

COMPUTES
- True RMS Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200mV Full-Scale Input Range
- Direct Interfacing with 3 1/2 Digit CMOS A/D Converters
- Power Down Feature Which Reduces Supply Current
- High Input Impedance: 10^{12} Ω
- Low Input Bias Current: 25 pA max
- High Accuracy: ±0.2 mV ±0.3% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8 V, −3.2 V to ±16.5 V
- Low Power: 160 μA max Supply Current
- No External Trims Needed for Specified Accuracy
- AD736 - A General Purpose, Buffered Voltage Output Version Also Available

AD737 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD737 is a low power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of ±0.2 mV ±0.3% of reading with sine wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD737 offers higher accuracy at equal or lower cost.

The AD737 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD737 can resolve input signal levels of 100 μV rms or less, despite variations in temperature or supply voltage. High accuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200 mV full-scale input level.

The AD737 has no output buffer amplifier, thereby significantly reducing dc offset errors occurring at the output. This allows the device to be highly compatible with high input impedance A/D converters.

Requiring only 160 μA of power supply current, the AD737 is optimized for use in portable multimeters and other battery powered applications. This converter also provides a "power down" feature which reduces the power supply standby current to less than 30 μA.

The AD737 allows the choice of two signal input terminals: a high impedance (10^{12} Ω) FET input which will directly interface with high Z input attenuators and a low impedance (8 kΩ) input which allows the measurement of 300 mV input levels while operating from the minimum power supply voltage of +2.8 V, −3.2 V. The two inputs may be used either singly or differentially.

The AD737 achieves a 1% of reading error bandwidth exceeding 10 kHz for input amplitudes from 20 mV rms to 200 mV rms while consuming only 0.72 mW.

The AD737 is available in four performance grades. The AD737J and AD737K grades are rated over the commercial temperature range of 0 to +70°C. The AD737A and AD737B grades are rated over the industrial temperature range of −40°C to +85°C.

The AD737 is available in three low cost, 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

PRODUCT HIGHLIGHTS

1. The AD737 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD737 to perform true rms measurement.
3. The low power consumption of 0.72 mW makes the AD737 suitable for many battery powered applications.

SPECIFICATIONS (@ +25°C, ±5 V supplies, ac coupled with 1 kHz sine wave input applied unless otherwise noted.)

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
TRANSFER FUNCTION		$V_{OUT} = -\sqrt{Avg.(V_{IN}^2)}$			$V_{OUT} = -\sqrt{Avg.(V_{IN}^2)}$			
CONVERSION ACCURACY	1 kHz Sine Wave							
Total Error, Internal Trim[1]	AC Coupled Using C_C							
All Grades	0–200 mV rms		0.2/0.3	**0.4/0.5**		0.2/0.2	**0.2/0.3**	±mV/±% of Reading
	200 mV–1 V rms		−1.2	**±2.0**		−1.2	**±2.0**	% of Reading
T_{min}–T_{max}								
A&B Grades	@ 200 mV rms			**0.5/0.7**			**0.3/0.5**	±mV/±% of Reading
J&K Grades	@ 200 mV rms		0.007			0.007		±% of Reading/°C
vs. Supply Voltage								
@ 200 mV rms Input	V_S = ±5 V to ±16.5 V	**0**	+0.06	**+0.1**	**0**	+0.06	**+0.1**	%/V
@ 200 mV rms Input	V_S = ±5 V to ±3 V	**0**	−0.18	**−0.3**	**0**	−0.18	**−0.3**	%/V
dc Reversal Error, dc Coupled	@ 600 mV dc		1.3	**2.5**		1.3	**2.5**	% of Reading
Nonlinearity[2], 0–200 mV	@ 100 mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0–200 mV rms		0.1/0.2			0.1/0.2		±mV/±% of Reading
ERROR VS. CREST FACTOR[3]								
Crest Factor 1 to 3	C_{AV}, C_F = 100 µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100 µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, −3.2 V			**200**			**200**	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			**1**			**1**	V rms
Peak Transient Input	V_S = +2.8 V, −3.2 V	**± 0.9**			**±0.9**			V
Peak Transient Input	V_S = ±5 V		±2.7			±2.7		V
Peak Transient Input	V_S = ±16.5V	**± 4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	V_S = ±3 V to ±16.5 V		1	**25**		1	**25**	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, −3.2 V			300			300	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			1			1	V rms
Peak Transient Input	V_S = +2.8 V, −3.2 V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5 V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5 V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous								
Nondestructive Input	All Supply Voltages			±12			±12	V p–p
Input Offset Voltage[4]	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
vs. Supply	V_S = ±5 V to ±16.5 V		50	**150**		50	**150**	µV/V
vs. Supply	V_S = ±5 V to ±3 V		80			80		µV/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
No Load	V_S = +2.8 V, −3.2 V	0 to −1.6	−1.7		0 to −1.6	−1.7		V
No Load	V_S = ±5 V	0 to −3.3	−3.4		0 to −3.3	−3.4		V
No Load	V_S = ±16.5 V	**0 to −4**	−5		**0 to −4**	−5		V
Output Resistance	@ dc	6.4	8	9.6	6.4	8	9.6	kΩ
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			37			37		kHz
V_{IN} = 200 mV rms			33			33		kHz
±3 dB Bandwidth	Sine Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			170			170		kHz
V_{IN} = 200 mV rms			190			190		kHz
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			90			90		kHz
V_{IN} = 200 mV rms			90			90		kHz
±3 dB Bandwidth	Sine Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			350			350		kHz
V_{IN} = 200 mV rms			460			460		kHz
POWER SUPPLY								
Operating Voltage Range		+2.8,−3.2	±5	±16.5	+2.8,−3.2	±5	±16.5	V
Quiescent Current	Zero Signal		120	**160**		120	**160**	µA
V_{IN} = 200 mV rms, No Load	Sine Wave Input		170	210		170	210	µA
Power Down Mode Current	Pin 3 tied to $+V_S$		25	**40**		25	**40**	µA

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD737J			AD737K		
Industrial (−40°C to +85°C)			AD737A			AD737B		
PACKAGE OPTIONS[5]								
8-Pin Plastic Mini-DIP (N-8)			AD737JN			AD737KN		
8-Pin Plastic SO (R-8)			AD737JR			AD737KR		
8-Pin Cerdip (Q-8)			AD737AQ			AD737BQ		

NOTES
[1]Accuracy is specified with the AD737 connected as shown in Figure 16 with capacitor C_C.
[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200 mV rms.
[3]Error vs. Crest Factor is specified as additional error for a 200 mV rms signal. C.F. = V_{PEAK}/V rms.
[4]DC offset does not limit ac resolution.
[5]See Section 20 for package outline information.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±16.5 V
Internal Power Dissipation[2] . . . . . 200 mW
Input Voltage . . . . . $\pm V_S$
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range Q . . . . . −65°C to +150°C
Storage Temperature Range N, R . . . . . −65°C to +125°C
Operating Temperature Range
AD737J/K . . . . . 0 to +70°C
AD737A/B . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W
8-Pin Ceramic Package: θ_{JA} = 110°C/W
8-Pin SOIC: θ_{JA} = 155°C/W.

ORDERING GUIDE

Temperature Range	Plastic Mini-DIP	Ceramic Mini-DIP	SOIC
Commercial 0 to +70°C	AD737JN AD737KN		AD737JR AD737KR
Industrial −40°C to +85°C		AD737AQ AD737BQ	

8

Typical Characteristics

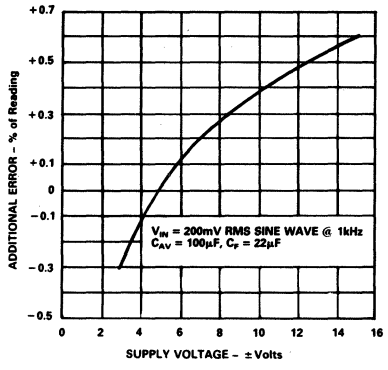


Figure 1. Additional Error vs. Supply Voltage

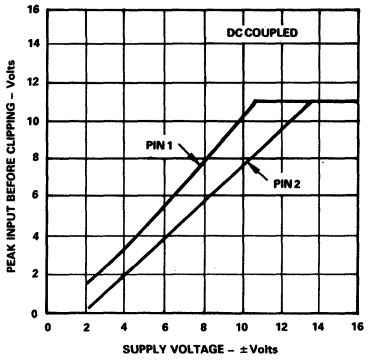


Figure 2. Maximum Input Level vs. Supply Voltage

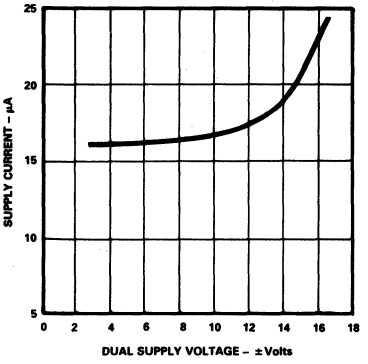


Figure 3. Power Down Current vs. Supply Voltage

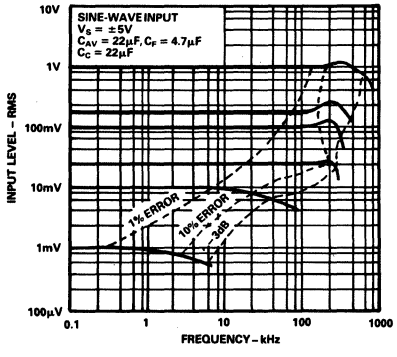


Figure 4. Frequency Response Driving Pin 1

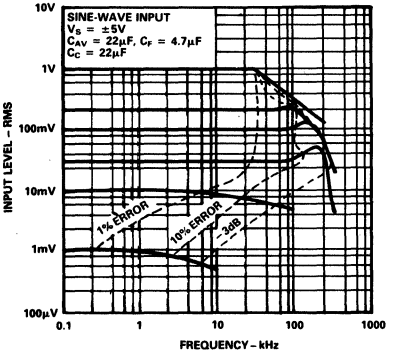


Figure 5. Frequency Response Driving Pin 2

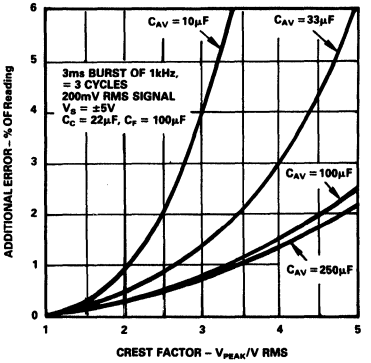


Figure 6. Additional Error vs. Crest Factor vs. C_{AV}

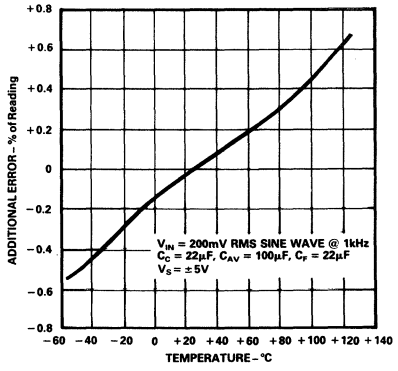


Figure 7. Additional Error vs. Temperature

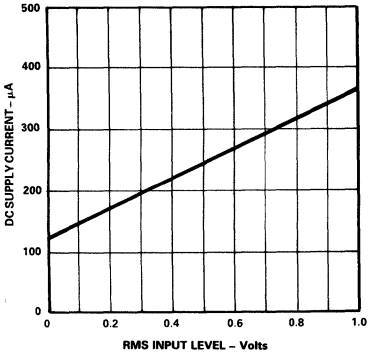


Figure 8. DC Supply Current vs. RMS Input Level

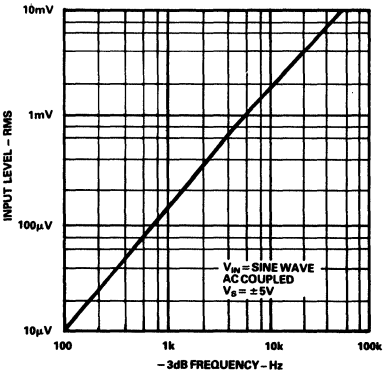


Figure 9. 23dB Frequency vs. RMS Input Level (Pin 2)

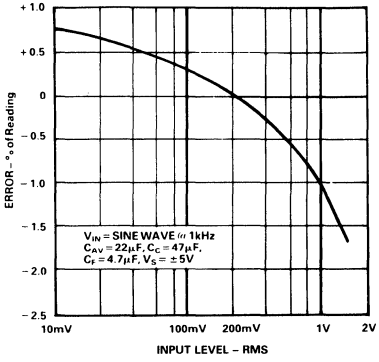


Figure 10. Error vs. RMS Input Voltage (Pin 2) Using Circuit of Figure 21

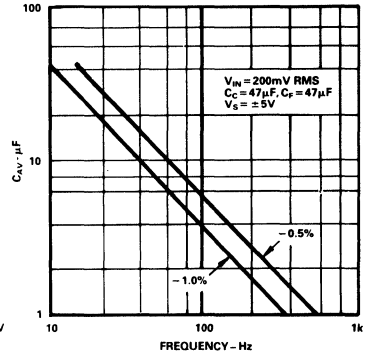


Figure 11. C_{AV} vs. Frequency for Specified Averaging Error

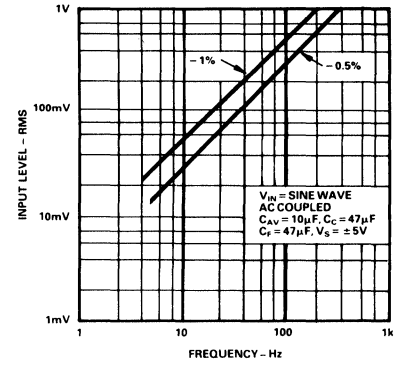


Figure 12. RMS Input Level vs. Frequency for Specified Averaging Error

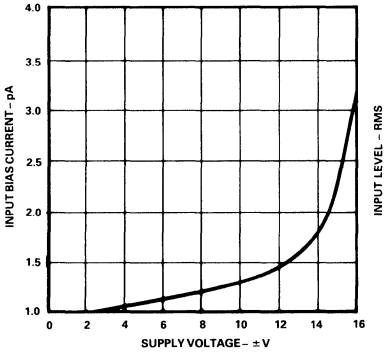


Figure 13. Pin 2 Input Bias Current vs. Supply Voltage

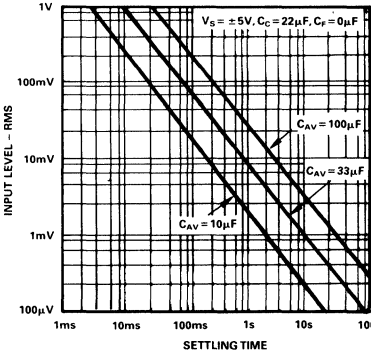


Figure 14. Settling Time vs. RMS Input Level for Various Values of C_{AV}

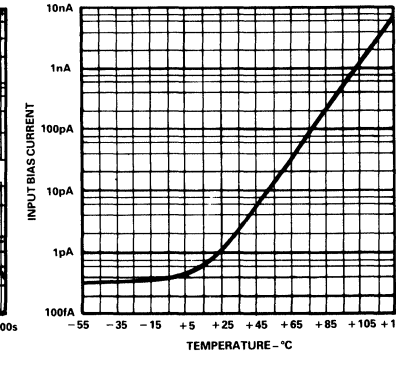


Figure 15. Pin 2 Input Bias Current vs. Temperature

8

CALCULATING SETTLING TIME USING FIGURE 14

The graph of Figure 14 may be used to closely approximate the time required for the AD737 to settle when its input level is reduced in amplitude. The *net time* required for the rms converter to settle will be the *difference* between two times extracted from the graph — the initial time minus the final settling time. As an example, consider the following conditions: a 33 µF averaging capacitor, an initial rms input level of 100 mV and a final (reduced) input level of 1 mV. From Figure 14, the initial settling time (where the 100 mV line intersects the 33 µF line) is around 80 ms. The settling time corresponding to the new or final input level of 1 mV is approximately 8 seconds. Therefore, the net time for the circuit to settle to its new value will be 8 seconds minus 80 ms which is 7.92 seconds. Note that, because of the smooth decay characteristic inherent with a capacitor/diode combination, this is the total settling time to the final value (i.e., *not* the settling time to 1%, 0.1%, etc., of final value). Also, this graph provides the worst case settling time, since the AD737 will settle very quickly with increasing input levels.

Applying the AD737

TYPES OF AC MEASUREMENT

The AD737 is capable of measuring ac signals by operating as either an average responding or true rms to dc converter. As its name implies, an average responding converter computes the average absolute value of an ac (or ac & dc) voltage or current by full wave rectifying and low pass filtering the input signal; this will approximate the average. The resulting output, a dc "average" level, is then scaled by adding (or reducing) gain; this scale factor converts the dc average reading to an rms equivalent value for the waveform being measured. For example, the average absolute value of a sine wave voltage is 0.636 that of V_{PEAK}; the corresponding rms value is 0.707 times V_{PEAK}. Therefore, for sine wave voltages, the required scale factor is 1.11 (0.707 divided by 0.636).

In contrast to measuring the "average" value, true rms measurement is a "universal language" among waveforms, allowing the magnitudes of all types of voltage (or current) waveforms to be compared to one another and to dc. RMS is a direct measure of the power or heating value of an ac voltage compared to that of dc: an ac signal of 1 volt rms will produce the same amount of heat in a resistor as a 1 volt dc signal.

Mathematically, the rms value of a voltage is defined (using a simplified equation) as:

$$V\ rms = \sqrt{Avg.\ (V^2)}$$

This involves squaring the signal, taking the average, and then obtaining the square root. True rms converters are "smart rectifiers": they provide an accurate rms reading regardless of the type of waveform being measured. However, average responding converters can exhibit very high errors when their input signals deviate from their precalibrated waveform; the magnitude of the error will depend upon the type of waveform being measured. As an example, if an average responding converter is calibrated to measure the rms value of sine wave voltages, and then is used to measure either symmetrical square waves or dc voltages, the converter will have a computational error 11% (of reading) higher than the true rms value (see Table I).

AD737 THEORY OF OPERATION

As shown by Figure 16, the AD737 has four functional subsections: input amplifier, full wave rectifier, rms core and bias section. The FET input amplifier allows both a high impedance, buffered input (Pin 2) or a low impedance, wide-dynamic-range input (Pin 1). The high impedance input, with its low input bias current, is well suited for use with high impedance input attenuators. The input signal may be either dc or ac coupled to the input amplifier. Unlike other rms converters, the AD737 permits both direct and indirect ac coupling of the inputs. AC coupling is provided by placing a series capacitor between the input signal and Pin 2 (or Pin 1) for direct coupling and between Pin 1 and ground (while driving Pin 2) for indirect coupling.

The output of the input amplifier drives a full-wave precision rectifier, which in turn, drives the rms core. It is in the core that the essential rms operations of squaring, averaging and square rooting are performed, using an external averaging capacitor, C_{AV}. Without C_{AV}, the rectified input signal travels through the core unprocessed, as is done with the average responding connection (Figure 17).

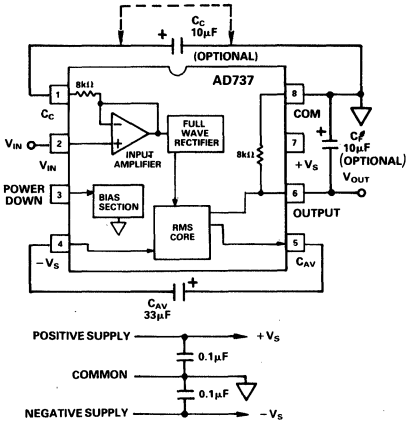


Figure 16. AD737 True RMS Circuit

Waveform Type 1 Volt Peak Amplitude	Crest Factor (V_{PEAK}/V RMS)	True RMS Value	Average Responding Circuit Calibrated to Read RMS Value of Sine Waves Will Read	% of Reading Error* Average Responding Circuit
Undistorted Sine Wave	1.414	0.707 V	0.707 V	0%
Symmetrical Square Wave	1.00	1.00 V	1.11 V	+11.0%
Undistorted Triangle Wave	1.73	0.580 V	0.555 V	−2.1%
Gaussian Noise (98% of Peaks <1 V)	3	0.333	0.266	−20.2%
Rectangular Pulse Train	2 10	0.5 V 0.1 V	0.25 V 0.01 V	−50% −99%
SCR Waveforms 50% Duty Cycle 25% Duty Cycle	2 4.7	0.495 V 0.212 V	0.354 V 0.150 V	−28% −30%

$$*\%\ \text{of Reading Error} = \frac{\text{Average Responding Value} - \text{True RMS Value}}{\text{True RMS Value}} \times 100\%$$

Table I. Error Introduced by an Average Responding Circuit when Measuring Common Waveforms

A final subsection, the bias section, permits a "power down" function. This reduces the idle current of the AD737 from 160 μA down to a mere 30 μA. This feature is selected by tying Pin 3 to the $+V_S$ terminal. In the average responding connection, all of the averaging is carried out by an RC post filter consisting of an 8 kΩ internal scale-factor resistor connected between Pins 6 and 8 and an external averaging capacitor, C_F. In the rms circuit, this additional filtering stage helps reduce any output ripple which was not removed by the averaging capacitor, C_{AV}.

RMS MEASUREMENT – CHOOSING THE OPTIMUM VALUE FOR C_{AV}

Since the external averaging capacitor, C_{AV}, "holds" the rectified input signal during rms computation, its value directly affects the accuracy of the rms measurement, especially at low frequencies. Furthermore, because the averaging capacitor appears across a diode in the rms core, the averaging time constant will increase exponentially as the input signal is reduced. This means that as the input level decreases, errors due to nonideal averaging will *reduce* while the time it takes for the circuit to settle to the new rms level will *increase*. Therefore, lower input levels allow the circuit to perform better (due to increased averaging) but increase the waiting time between measurements. Obviously, when selecting C_{AV}, a trade-off between computational accuracy and settling time is required.

RAPID SETTLING TIMES VIA THE AVERAGE RESPONDING CONNECTION (FIGURE 17)

Because the average responding connection does not use an averaging capacitor, its settling time does not vary with input signal level; it is determined solely by the RC time constant of C_F and the internal 8 kΩ output scaling resistor.

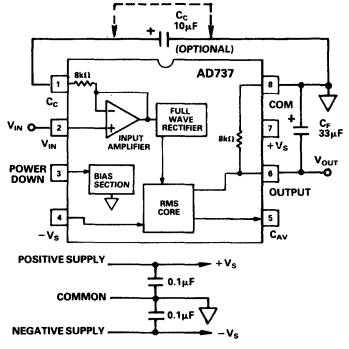


Figure 17. AD737 Average Responding Circuit

DC ERROR, OUTPUT RIPPLE, AND AVERAGING ERROR

Figure 18 shows the typical output waveform of the AD737 with a sine-wave input voltage applied. As with all real-world devices, the ideal output of $V_{OUT} = V_{IN}$ is never exactly achieved; instead, the output contains both a dc and an ac error component.

As shown, the dc error is the difference between the average of the output signal (when all the ripple in the output has been removed by external filtering) and the ideal dc output. The dc error component is therefore set solely by the value of averaging capacitor used—*no* amount of post filtering (i.e., using a very large C_F) will allow the output voltage to equal its ideal value.

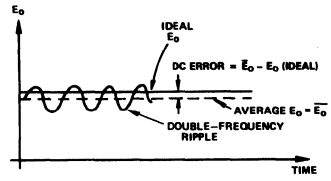


Figure 18. Output Waveform for Sine Wave Input Voltage

The ac error component, an output ripple, may be easily removed by using a large enough post filtering capacitor, C_F.

In most cases, the combined magnitudes of both the dc and ac error components need to be considered when selecting appropriate values for capacitors C_{AV} and C_F. This combined error, representing the maximum uncertainty of the measurement is termed the "averaging error" and is equal to the peak value of the output ripple plus the dc error. As the input frequency increases, both error components decrease rapidly: if the input frequency doubles, the dc error and ripple reduce to 1/4 and 1/2 their original values respectively and rapidly become insignificant.

AC MEASUREMENT ACCURACY AND CREST FACTOR

The crest factor of the input waveform is often overlooked when determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms amplitude (CF = V_{PEAK}/V rms). Many common waveforms, such as sine and triangle waves, have relatively low crest factors (≥2). Other waveforms, such as low duty cycle pulse trains and SCR waveforms, have high crest factors. These types of waveforms require a long averaging time constant (to average out the long time periods between pulses). Figure 6 shows the additional error vs. crest factor of the AD737 for various values of C_{AV}.

SELECTING PRACTICAL VALUES FOR INPUT COUPLING (C_C), AVERAGING (C_{AV}) AND FILTERING (C_F) CAPACITORS

Table II provides practical values of C_{AV} and C_F for several common applications.

Application	RMS Input Level	Low Frequency Cutoff (–3 dB)	Max Crest Factor	C_{AV}	C_F	Settling Time* to 1%
General Purpose RMS Computation	0–1 V	20 Hz	5	150 μF	10 μF	360 ms
		200 Hz	5	15 μF	1 μF	36 ms
	0–200 mV	20 Hz	5	33 μF	10 μF	360 ms
		200 Hz	5	3.3 μF	1 μF	36 ms
General Purpose Average Responding	0–1 V	20 Hz		None	33 μF	1.2 sec
		200 Hz		None	3.3 μF	120 ms
	0–200 mV	20 Hz		None	33 μF	1.2 sec
		200 Hz		None	3.3 μF	120 ms
SCR Waveform Measurement	0–200 mV	50 Hz	5	100 μF	33 μF	1.2 sec
		60 Hz	5	82 μF	27 μF	1.0 sec
	0–100 mV	50 Hz	5	50 μF	33 μF	1.2 sec
		60 Hz	5	47 μF	27 μF	1.0 sec
Audio Applications						
Speech	0–200 mV	300 Hz	3	1.5 μF	0.5 μF	18 ms
Music	0–100 mV	20 Hz	10	100 μF	68 μF	2.4 sec

*Settling time is specified over the stated rms input level with the input signal increasing from zero. Settling times will be greater for decreasing amplitude input signals.

Table II. AD737 Capacitor Selection Chart

The input coupling capacitor, C_C, in conjunction with the 8 kΩ internal input scaling resistor, determine the −3 dB low frequency rolloff. This frequency, F_L, is equal to:

$$F_L = \frac{1}{2\pi\ (8{,}000)\ (\textit{The Value of } C_C \textit{ in Farads})}$$

Note that at F_L, the amplitude error will be approximately −30% (−3 dB) of reading. To reduce this error to 0.5% of reading, choose a value of C_C that sets F_L at one tenth the lowest frequency to be measured.

In addition, if the input voltage has more than 100 mV of dc offset, then an ac coupling network at Pin 2 should be used in addition to capacitor C_C.

Applications Circuits

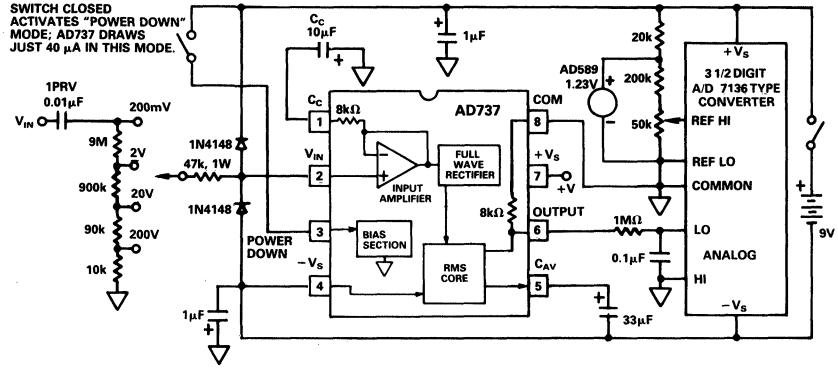


Figure 19. 3 1/2 Digit DVM Circuit

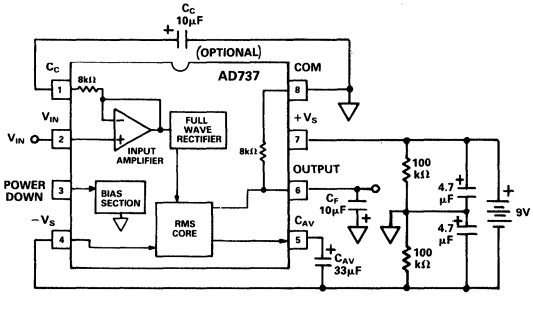


Figure 20. Battery Powered Operation for 200 mV max RMS Full-Scale Input

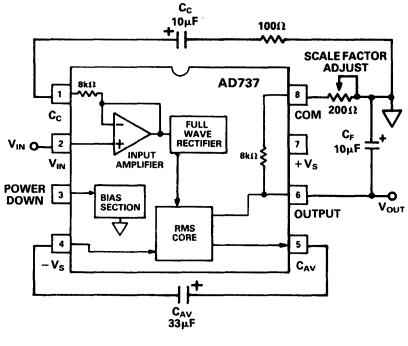


Figure 21. External Scale Factor Trim

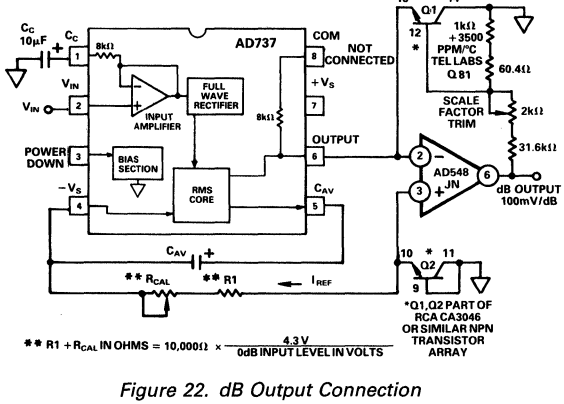


Figure 22. dB Output Connection

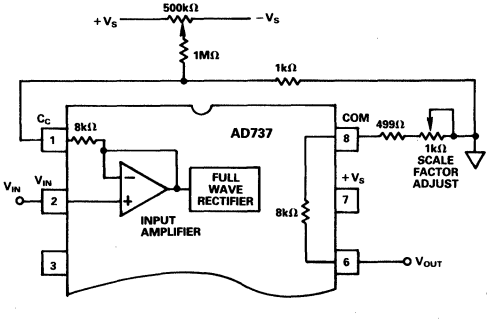


Figure 23. DC Coupled V_{OS} and Scale Factor Trims

Mass Storage Components
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Orientation
Mass Storage Components

Our mass storage components offer the industry's highest performance products specifically designed for optical or magnetic disk drives.

AD880: The AD880 is a servo/data channel processing element for an optical disk drive. It is configured around 4 matched transimpedance amplifiers and normalization circuitry enabling it to perform all of the signal processing needed to generate the data, normalized track and normalized focus signal.

Figure 1 depicts a functional block diagram of the read electronics in a magnetic disk drive and the corresponding functional integration being offered by each of our hard disk products.

AD890/AD891 or AD890/AD891A: Both pairs of products comprise a chip set to perform the peak detection function in high performance disk drives (up to 50 Mb/s). The AD890 offers read channel designers flexibility by offering dual ×4 buffers which enable the channel designer to separate the low pass filtering function from the pulse slimming filters. The AD890 also offers a very fast 1 μs AGC loop. Two choices of data qualifiers–AD891 and AD891A–are offered as a companion chip to the AD890. Each data qualifier offers a different but highly accurate data qualification algorithm with extremely low pulse pairing.

AD892: The AD892 integrates the same function as the AD890/AD891 pair at a data transfer rate of 30 Mb/s. By maintaining the same architectural features of the AD890/AD891, the AD892 offers a smaller form factor, while not compromising design flexibility.

AD897: The AD897, our next generation disk drive product, offers a significantly higher level of functional integration and a high data transfer rate. It incorporates an AGC, data qualifier and phase lock loop while offering a 40 Mb/s data transfer rate. The AGC and data qualifier architecture is very similar to the AD890/AD891A pair while employing a novel approach to the PLL architecture. The AD897 is offered in the fine pitch PQDP package.

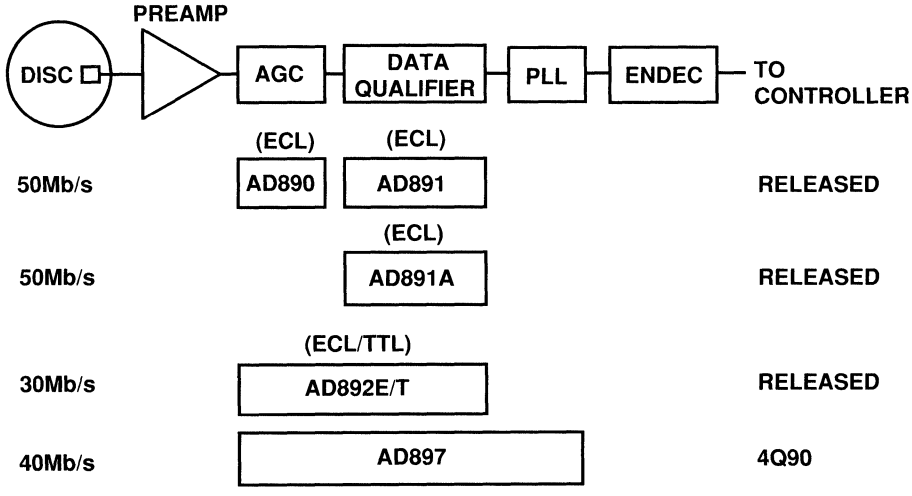


Figure 1.

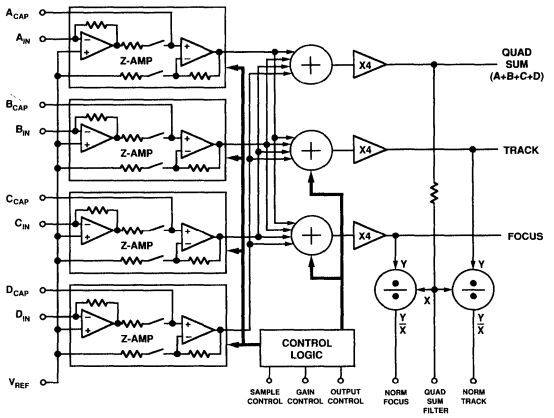
ANALOG DEVICES

Optical Disk Servo/Data Channel Processing Element

AD880

FEATURES
4 Matched Transimpedance Amplifiers
40 MHz Bandwidth
Selectable 40 kΩ/120 kΩ Transimpedance
Continuous or Sampled Servo Capability
Outputs:
Quad Sum
Track
Normalized Track
Focus
Normalized Focus
10 MHz Normalization Dividers
10 ns Write Recovery with Sampling
Low Output Noise

AD880 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD880 is a monolithic integrated circuit intended for applications in the servo/read systems of an optical disk drive product.

The AD880 consists of four matched transimpedance amplifiers (A, B, C, D) with selectable 40 kΩ or 120 kΩ transimpedance. The basic transimpedance stage consists of a 10 kΩ transimpedance front end that drives a programmable ×1 or ×3 buffer. Each stage has been configured to minimize noise and noise peaking. To further enhance overall signal to noise performance an external capacitor may be added between the transimpedance amplifier and the programmable buffer to implement a first order low-pass filter.

The AD880 is stable over the full range of input source capacitances. To ensure stability and maximize available bandwidth in both transimpedance modes, the internal compensation capacitor in the programmable buffer is appropriately modified for each mode.

Fast read after write recovery is implemented through the transimpedance sample function. Use of the sample function allows for a read-after-write recovery in approximately 10 ns. The "sample capacitor" also serves the dual purpose of providing the low-pass filter.

In addition, the part contains three offset trimmed summing amplifiers with 40 MHz bandwidth. One amplifier provides the quad sum output. This output can be low pass filtered prior to driving the normalization dividers. Two other summing amplifiers generate the track and focus outputs.

- Quad Sum : (A+B+C+D)
- Track : (A+D) − (B+C) or (A−B)
- Focus : (A+C) − (B+D) or (C−D)

The selectable outputs are programmed through a CMOS compatible control line.

Finally, a pair of two quadrant dividers are provided. These generate the normalized focus and track signals with an accuracy of 10%, and have bandwidths in excess of 10 MHz.

The AD880 is available in a 20-pin SOIC package and is specified to operate over the 0 to +70°C commercial temperature range.

SPECIFICATIONS (@ + 25°C and +12 V dc, unless otherwise noted)

Parameter	Conditions	AD880J Min	AD880J Typ	AD880J Max	Units
TRANSIMPEDANCE AMPLIFIER					
Transimpedance			10		kΩ
Transimpedance Matching	Channel to Channel			±1	%
Channel to Channel Crosstalk	@ 30 MHz Input Signal			−40	dB
Open-Loop Gain	AV_0		20		V/V
Open-Loop Bandwidth			40		MHz
Input Capacitance			2		pF
Input Offset Current			TBD		nA
Input Offset Voltage			TBD		mV
Input Current Noise			1		$pA/\sqrt{Hz}$
Input Voltage Noise			1.5		$nV/\sqrt{Hz}$
Feedback Resistor Noise			13		$nV/\sqrt{Hz}$
Output Impedance	@ Filter Capacitor Pin (Active)		1		kΩ
Output Impedance	@ Filter Capacitor Pin (Sampled)		250		MΩ
Max Output Voltage Swing		±0.7			V
Max Output Current			TBD		mA
V_{REF} Range		+4.5		+5.5	V
V_{REF} Input Current		−5		5	mA
PROGRAMMABLE BUFFER					
Gain	Gain Control = 0		10		dB
Gain Matching	Gain Control = 0, Channel to Channel		TBD		dB
3 dB Bandwidth	Gain Control = 0		40		MHz
Gain	Gain Control = 1		0		dB
Gain Matching	Gain Control = 1, Channel to Channel		TBD		dB
3 dB Bandwidth	Gain Control = 1		60		MHz
Input Bias Current				0.1	pA
Input Offset Voltage			TBD		μV
Input Current Noise			1		$pA/\sqrt{Hz}$
Input Voltage Noise			13		$nV/\sqrt{Hz}$
Max Output Voltage Swing	Relative to V_{REF}	±1			V
SUMMING AMPLIFIER					
Gain			12		dB
Gain Matching	Input to Input		TBD		%
3 dB Bandwidth			40		MHz
Output DC Voltage	Relative to V_{REF}		0		V
Output Voltage Offset			TBD		V
Output Impedance			TBD		Ω
Max Output Voltage	Relative to V_{REF}	±2.5			V
Max Output Current		20			mA
NORMALIZATION DIVIDERS					
Division Error	$0.5 \le Y \le X \le 1.5$			±10	%
3 dB Bandwidth			10		MHz
Output Voltage Range	Relative to V_{REF}		2		V
Output Current	Division Ratio = 1		200		μA
QUAD SUM FILTER					
Resistance	Quad Sum to Quad Sum Filter	8	10	12	kΩ
MODE CONTROL SECTION	(CMOS Compatible)				
V_{IH}		4.0		V_{CC}	V
V_{IL}		0		1	V
I_{IH}				0.1	pA
I_{IL}				0.1	pA
Mode Switching Times	Gain Control		10		ns
	Output Mode		10		ns
	Sample Mode		10		ns

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	Conditions	AD880J Min	Typ	Max	Units
POWER SUPPLY REQUIREMENTS					
Supply Voltage V_{CC}		10.8	12	13.2	V
Supply Voltage V_{EE}			0		V
Quiescent Current I_{CC}	T_{min} to T_{max}	50	60	70	mA
ABSOLUTE MAXIMUM RATINGS[1]					
Supply Voltage V_{CC}				14.5	V
V_{REF} Input Voltage		−0.8		7.0	V
Storage Temperature Range		−65		130	°C
Operating Temperature Range[2]		0		70	°C
Lead Temperature Range	Soldering 60 Sec			+300	°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.
[2]20-pin wide body SO package: θ_{JA} = +65°C/watt.
Specifications subject to change without notice.

Logic Assignments	Sample Control	Gain Control	Output Control
Transimpedance Amplifiers Active	0	X	X
Transimpedance Amplifiers Sampled	1	X	X
Select 120 kΩ Transimpedance	X	0	X
Select 40 kΩ Transimpedance	X	1	X

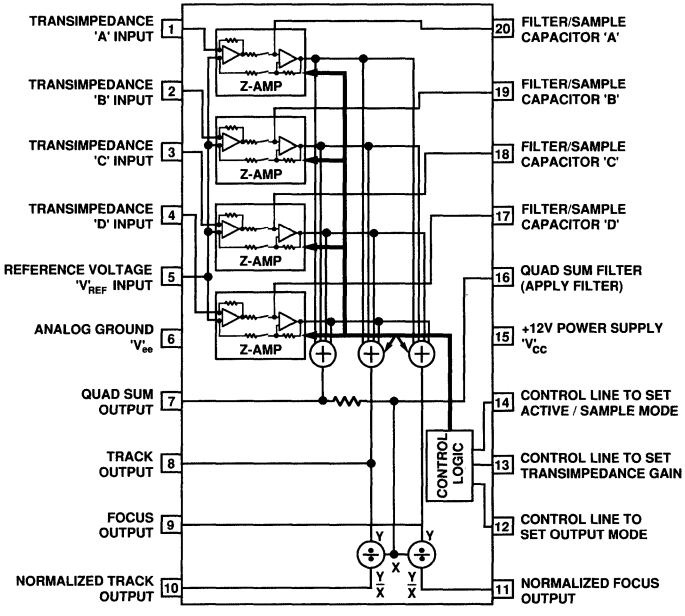
Logic Assignments	Sample Control	Gain Control	Output Control
Track Output = (A+D) − (B+C) and Focus Output = (A+C) − (B+D)	X	X	0
Track Output = (A−B) and Focus Output = (C−D)	X	X	1

X = Do Not Care.

Table I. AD880 Logic Assignments

9

PIN ASSIGNMENTS



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

THEORY OF OPERATION

Transimpedance Stage

The transimpedance stage is configured as a fixed 10 kΩ transimpedance amplifier followed by a programmable buffer (Figure 1). The source capacitance C_S coupled with the transimpedance feedback resistor, R_F = 10 kΩ, determines the bandwidth of the transimpedance amplifier.

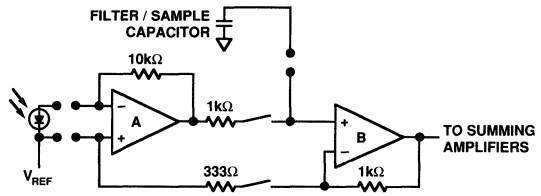


Figure 1.

To optimize the signal to noise performance the input amplifier uses a bipolar input stage. This allows for a significantly lower input voltage noise figure at the expense of input bias and noise current. To compensate for the output offset voltage created by the input bias current, the programmable buffer mirrors and cancels the offset voltage created in the transimpedance cell. The overall output voltage offset through the complete transimpedance stage is less than 5 mV.

By keeping the transimpedance of the first stage relatively low, 10 kΩ, and limiting the open-loop gain of amplifier "A" to 20, noise peaking is limited. To further limit noise and noise peaking, the output of the first stage may be low pass filtered by applying a capacitor, see Figure 1, at the appropriate pins (Pins 17, 18, 19 and 20). The capacitor forms a first order low-pass filter with a cut-off frequency $f = 1/(2\pi \bullet 1000 \bullet C_{FILTER})$. The complete noise model for the front-end transimpedance stage is shown in Figure 2.

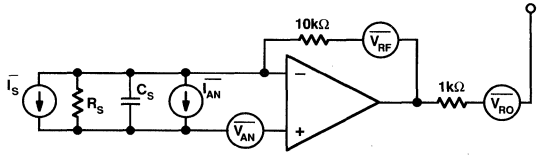


Figure 2.

To ensure stability of the complete transimpedance stage over the full range of source capacitances, the programmable buffer is internally compensated. To maintain the stability and maximize available bandwidth, the compensation capacitor is internally modified for each transimpedance mode. Also, depending upon the buffer gain of ×1 or ×3, programmable through the "Gain Control" line (Pin 13), the input noise is amplified by a factor of 1 or 3, respectively.

Logic Assignments	Gain Control
Select 120 kΩ Transimpedance	0
Select 40 kΩ Transimpedance	1

To improve read-after-write recovery the AD880 offers an input sample function, programmable through the "Sample Control" line (Pin 14).

Logic Assignments	Sample Control
Transimpedance Amplifier Active	0
Transimpedance Amplifier Sampled	1

The sample capacitor also serves as the low-pass filter for the transimpedance stage. The FET input on the programmable buffer ensures an excellent droop-rate in the sample mode.

Summing Amplifiers

The summing amplifiers provide the Quad Sum, Focus and Track outputs with a gain of X4. The X4 amplification through the summers provide the final gain for achieving a 40 kΩ or 120 kΩ overall transimpedance.

The output of both the Focus and Track summing amplifiers are programmable through the CMOS compatible "Output Control" line (Pin 12).

Logic Assignments	Output Control
Track Output = (A+D) − (B+C) and Focus Output = (A+C) − (B+D)	0
Track Output = (A−B) and Focus Output = (C−D)	1

Normalization Dividers

The normalization dividers provide current output of the Normalized Focus and Track signals. A low-pass filter capability is provided at the "Quad Sum Filter" pin (Pin 16). The Quad Sum Filter Resistance is 10 kΩ, and thereby offers the user the capability to implement a RC filter prior to the applying the Quad Sum signal to the normalization dividers.

General Layout Requirements

Care must be taken to ensure good R_F practice in the PC layout to avoid oscillations. A parallel combination of 0.1 μF and 0.01 μF ceramic capacitors should be used as close to the V_{CC} (Pin 6) and V_{REF} (Pin 5) pins as possible. Also, a current path to $V_{REFERENCE}$ must be provided for the outputs of the normalization dividers.

ORDERING GUIDE

Model	Description	Package Option*
AD880JR	20-Pin Small Outline	R-20

*See Section 20 for package outline information.

ANALOG DEVICES

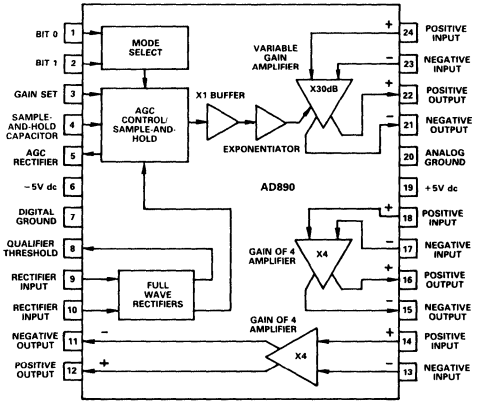
Precision, Wideband Channel Processing Element

AD890

FEATURES

- An 80 MHz Bandwidth Permitting a 50 Mb/s Data Transfer Rate
- A Variable Gain Amplifier with 30 dB max Gain and 40 dB Control Range
- Two Gain of 4 RF Buffers
- 200 Ω Differential Load Drive Capability
- A Pair of Precision Rectifiers
- AGC Level and Threshold Outputs
- An Averaging, High Gain Sample-and-Hold for Accurate AGC Operation
- Typical Gain Drift in Hold Mode: 0.2 dB/ms
- Gains Trimmed and Temperature Compensated
- AGC Operation Independent of AGC Level
- Symmetrical AGC Attack/Decay Times
- 1 μs AGC Attack/Decay Times Using a 1000 pF External Capacitor
- Suitable for Use as an Accurate Video Programmable Gain Amplifier
- Dynamic Clamp Ensures Fast Recovery After Write to Read Transients
- AGC RF Output Level Is Internally Preset

AD890 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD890 is primarily intended for high performance disk subsystem use, and as such it is configured around the classic read channel processing block diagram. It is intended to be connected between the head preamplifier and the qualification circuitry required for digital data recovery. When used with the AD891 rigid disk data qualifier, data transfer rates in excess of 50 Mb/s can be processed.

A temperature-compensated AGC loop, with an exponential transfer characteristic, permits optimal settling and allows for predictable performance in the classic single integrator control loop configuration. Fast acquisition and low droop while in the hold mode allow for AGC operation to be performed within the sector header without compromising channel behavior when reading data.

The AD890 processing element has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Two user-defined filter/equalizer stages may be employed, thus allowing maximum design flexibility. This greatly simplifies the design of the overall channel characteristics. Using the AD890, the designer no longer needs to resort to passive techniques to isolate network functions; this avoids problems of signal loss and interaction. Two low offset, 100 MHz, full wave rectifiers provide the capability to track a 1 V peak signal. The rectifier generating the "Qualifier Threshold" output may be used for creating a data qualification level. A second rectifier is used to drive the sample-and-hold circuitry.

The 80 MHz bandwidth of the AD890 ensures good phase linearity up to 50 MHz. Thus, data transfer rates in excess of 50 Mb/s can be supported with good error rates and predictable channel behavior.

The AD890 is available in both a 24-pin, slim-line cerdip package and in a 28-pin PLCC package and is specified to operate over the 0 to +70°C commercial temperature range.

9

SPECIFICATIONS (@ +25°C and ±5 V dc, unless otherwise noted)

Parameter	Conditions	AD890J Min	AD890J Typ	AD890J Max	Units
VARIABLE GAIN AMPLIFIER					
Maximum Gain[1]		**29.0**	30.0	**31.0**	dB
±3 dB Bandwidth	Up to 40 dB Gain Reduction	100			MHz
Input Resistance	Differential	12	18		kΩ
Input Capacitance	Differential		1	5	pF
Input Voltage Noise	0 dB Gain Reduction		5		$nV/\sqrt{Hz}$
Input Signal Range	Recommended p–p Differential	10		200	mV
Max Output Signal Level	1 kΩ Load, p–p Differential	2.4			V
Output Impedance			5		Ω
Output DC Level			3.5		V
Harmonic Distortion	0 dB Gain Reduction		0.15		%
	26 dB Gain Reduction		1.5		%
INPUT CLAMP[2]					
Turn-On Time			30		ns
Turn-Off Time			200		ns
Input Signal Attenuation			35		dB
On-State Input Impedance	Differential		14		Ω
GAIN OF 4 BUFFER					
Nominal Gain		**12.25**	12.75	**13.25**	dB
Gain Variation	T_{min} to T_{max}		±0.25		dB
±3 dB Bandwidth	Up to 26 dB Gain Reduction	160			MHz
Input Resistance	Differential	100			kΩ
Input Capacitance	Differential		1	5	pF
Input Voltage Noise[3]	100 MHz – 0 dB Gain Reduction		7		$nV/\sqrt{Hz}$
Input Common-Mode Range		−1.5		+1.5	V
Output Impedance			10		Ω
Output Signal Level	Recommended p–p Differential		1.3		V
Max Output Signal Level	200 Ω Load, p–p Differential	4.8			V
Output DC Level			2.5		V
Harmonic Distortion	300 mV Peak Output, 200 Ω Load		0.20		%
FULL WAVE RECTIFIER					
Input Signal Level	p–p Differential	0.3		3	V
−3 dB Bandwidth	100 mV @1 V Peak Input	100			MHz
Max Output Signal Level		1.5			V
Output Impedance[4]			25		Ω
DC Offset[4]	Relative to Ground		10	**±20**	mV
AGC CONTROL SECTION					
Attack Time	26 dB Gain Step – 1000 pF C_{SAMPLE}		1.0		μs
	26 dB Gain Step – <50 pF C_{SAMPLE}		120		ns
Hold Time	1 dB Gain Change – 1000 pF C_{SAMPLE}		10		ms
AGC Charge Current			0.8		mA
AGC Control Range		**36**	40		dB
AGC Control Sensitivity	Per 20 mV Input		1		dB
AGC Control Linearity	26 dB AGC Range			**±0.25**	dB
Set Level Input Range	For Specified Accuracy	**0**		**800**	mV
	Nondestructive Input Range	−0.3		V_{CC}	V
MODE CONTROL SECTION					
TTL Compatible					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IH}	V_{IH} = 2.7 Volts			1	μA
I_{IL}	V_{IL} = 0.4 Volts		−4.5	−12.0	μA
Mode Switching Times				50	ns
POWER SUPPLY REQUIREMENTS					
Operating Range V_{CC}		**+4.5**		+5.5	V
Operating Range V_{EE}		**−4.68**	−5.2	−5.72	V
Quiescent Current	T_{min} to T_{max}				
V_{CC}	Hold/Acquire/Set Gain Mode	44	60	76	mA
V_{EE}	Hold/Acquire/Set Gain Mode	18	28	40	mA
V_{CC}	Clamp Mode	51	72	88	mA
V_{EE}	Clamp Mode	17	27	39	mA

NOTES
[1]Gain calibrated in gain set mode with 0 volts applied to the Gain Set Pin.
[2]Clamp operation is specified with a source impedance of 200 Ω in series with 0.1 μF.
[3]Over the full 100 MHz bandwidth of the AD890, the worst-case rms signal-to-noise ratio is 40 dB or better with a 40 dB AGC range.
[4]Measured using a 4 kΩ resistor connected between the Qualifier Threshold Pin and V_{EE}.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±7.5 V
RF Gain Stage Differential Input Voltage . . . . . ±5.6 V
Storage Temperature Range
AD890JP, AD890JQ . . . . . −65°C to +150°C
Operating Temperature Range[1]
AD890JP, AD890JQ . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTE
[1]28-pin PLCC package: θ_{JA} = 100°C/W;
24-pin cerdip package: θ_{JA} = 55°C/W.
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Assignments	Bit 0	Bit 1
AGC Acquire	0	0
AGC Hold	0	1
Gain Set	1	0
Input Clamp	1	1

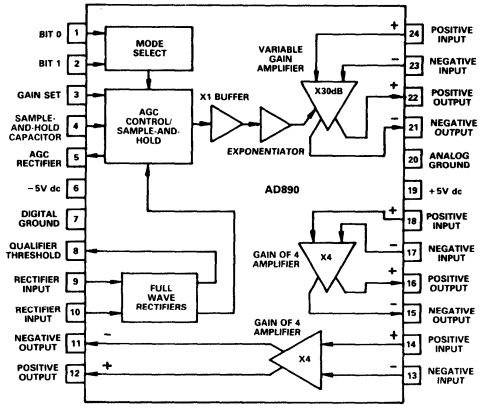
ORDERING GUIDE

Model	Package	Package Options*
AD890JQ	24-Pin Cerdip	Q-24
AD890JP	28-Pin PLCC	P-28A

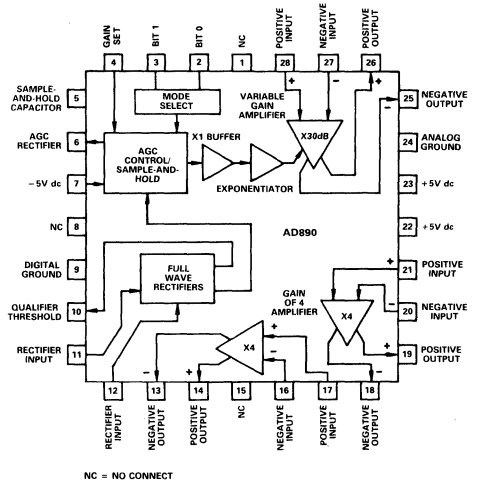
*See Section 20 for package outline information.

CONNECTION DIAGRAMS

24-Pin Cerdip Package



28-Pin PLCC Package



NC = NO CONNECT

Typical Characteristics @ +25°C with ±5 V Supplies

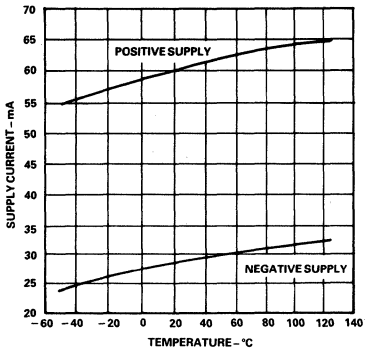


Figure 1. Supply Current vs. Temperature

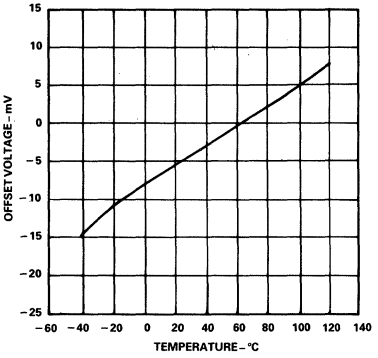


Figure 2. Rectifier Offset vs. Temperature

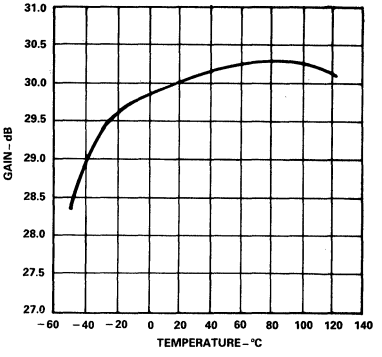


Figure 3. VGA Gain vs. Temperature

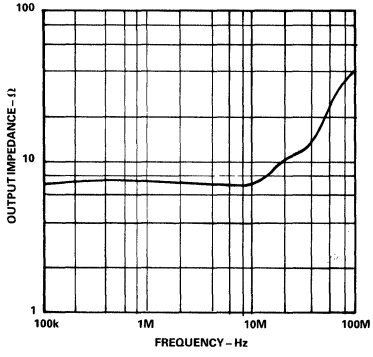


Figure 4. VGA Output Impedance vs. Frequency

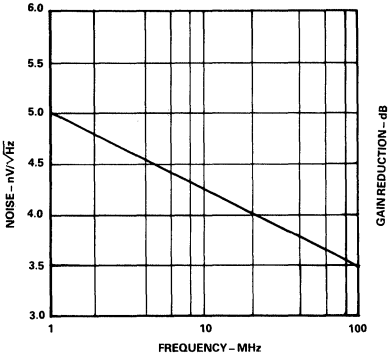


Figure 5. VGA Voltage Noise vs. Frequency

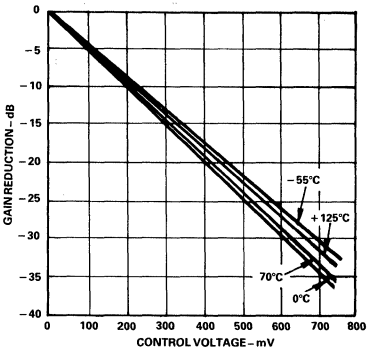


Figure 6. VGA Gain Reduction vs. Control Voltage

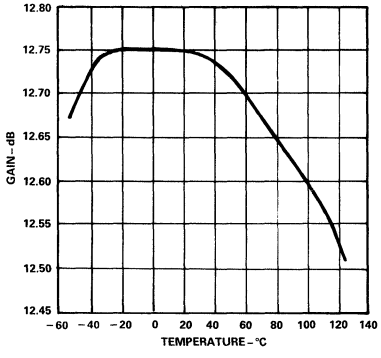


Figure 7. X4 Buffer Gain vs. Temperature

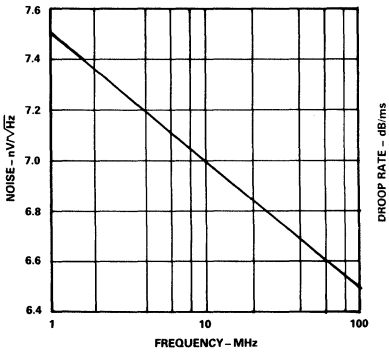


Figure 8. X4 Buffer Voltage Noise vs. Frequency

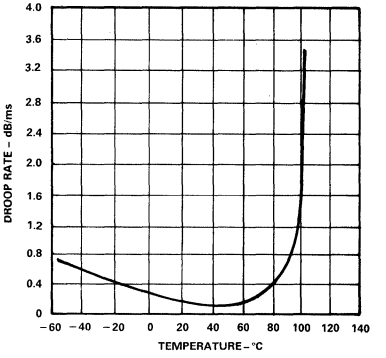


Figure 9. Hold-Mode Droop Rate vs. Temperature

GENERAL LAYOUT REQUIREMENTS

Almost 60 dB of total gain is available at 100 MHz. Care must be taken to ensure good RF practice in the PC layout to avoid oscillations in the 150 MHz–350 MHz region. A parallel combination of 0.1 μF and 0.01 μF ceramic bypass capacitors should be used as close to the supply pins as possible.

Additionally, a single pole RC filter applied at the input of each stage, with a cutoff in the region of 100 MHz–150 MHz, will help avoid oscillation problems. As a general rule, keep the connections to interstage components as short as possible; it is also recommended that any low pass filtering function which may be required by the system be performed between the VGA stage and the first X4 buffer amplifier. A ground plane should be used to surround any interstage components wherever possible. If these simple rules are followed, stable operation should be assured.

BIASING THE RF GAIN STAGES

The VGA Stage

The 30 dB variable gain stage is biased at a potential of one diode drop above analog ground. No additional dc bias is required, but ac coupling is necessary. The bias voltage is maintained during normal operation and during operation of the clamp. In order for the clamp to operate correctly with an emitter follower driven input, 50 Ω–100 Ω resistors should be placed in series with the input coupling capacitors. These resistors can be used in conjunction with a 5.1 pF shunt capacitor to limit the input bandwidth to 150 MHz. In the case of an open collector driven input with resistive termination, no additional series resistors are required.

The differential outputs have a nominal dc value of 1.5 V less than the positive supply. Internal 1300 Ω resistors provide bias current to the output emitter followers which operate with 2.7 mA nominal current. Output drive can be increased by an additional 2.5 mA by paralleling external resistors to either the analog ground or the negative power supply. However, caution should be exercised in order to avoid causing excess dissipation for the package. The recommended output level for the VGA is 300 mV p–p differential into 200 Ω loads.

The X4 Buffers

The inputs of these stages have no committed dc biasing, and an input bias current path must be provided. This path can normally be supplied via shunt resistors to analog ground which are generally part of the interstage filter termination networks. The inputs can be biased successfully within ±1.5 V of analog ground.

Output drive can be increased in a similar manner to that described for the VGA stage. The nominal dc output level is 2.5 V with the internal 500 Ω load resistors connected to analog ground which provides a nominal standing current of 5 mA to the output emitter followers. This current can be increased by up to an additional 5 mA by paralleling external resistors to either analog ground or the negative power supply. As before, precautions to limit excessive overall power dissipation apply when steps are taken to increase the output drive capability.

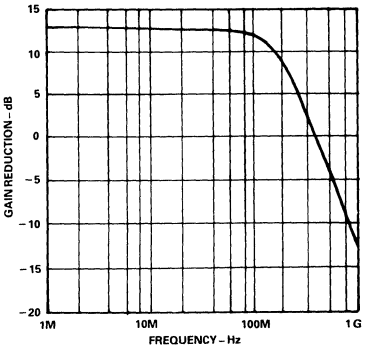


Figure 10. X4 Buffer Frequency Response (100 Ω in Series with 1 μF Load)

OPERATING THE FULL WAVE RECTIFIERS

The full wave rectifiers consist of two nearly identical stages. Full wave rectification is performed in each stage using two transistors whose emitters are connected together. The inputs to the two full wave rectifiers are biased at one diode drop above analog ground; therefore, ac coupling is recommended. The full wave rectifier outputs – "AGC Rectifier" and "Qualifier Threshold" – are connected directly to these commoned emitters. Thus, the normal output voltage with zero input signal applied is close to analog ground. The "AGC Rectifier" pin allows access to the output of the rectifier which drives the AGC sample-and-hold section of the AD890. The "Qualifier Threshold" pin allows access to the output of the threshold rectifier.

The AGC rectifier has an internal 2 kΩ resistive pull-down connected between analog ground and the negative power supply pin. The threshold line has no built in pull-down, in order to allow for a peak hold capability during thresholding. If a well controlled rectifier offset is required, an external 4 kΩ pull-down resistor at the "Qualifier Threshold" pin is recommended and will produce a nominal 10 mV offset.

THE AGC SAMPLE-AND-HOLD

The AGC sample-and-hold section performs averaging of the input waveform to set the RF average output level to 200 mV single ended, or 330 mV peak for a sinusoidal signal. Thus, without a peak hold capacitor at the "AGC Rectifier" pin, accurate AGC operation only occurs with sinusoidal input signals. An approximate 2 mA pull-down current is permanently present at the "AGC Rectifier" pin, and a capacitor may be added here to provide a degree of peak hold for AGC operation within non-sinusoidal fields. A capacitance value of less than 0.03 μF or less per μs of transition spacing is recommended. The addition of the capacitor alters the symmetry of the attack and decay rates of the rectifier, which is otherwise symmetric in operation. In order to ensure that the overall AGC response is the same for both high-to-low and low-to-high input level steps, it is necessary to make the rectifier attack and decay times at least a factor of two less than the AGC response time.

The AGC acquire time is approximately 1 μs per 1000 pF of hold capacitor. A low leakage variety of hold capacitor, such as a silver mica, is necessary to ensure low droop rates. The "Gain Set" pin should be tied to analog ground if not used, in order to prevent excessive leakage which would otherwise affect the hold performance.

The AGC control potential is present at the "Sample-and-Hold Capacitor" pin. If control over open-loop gain is desired, based on AGC control potentials obtained during trial AGC operations, a FET input op amp should be used to buffer this node in order to avoid disturbing the hold operation.

USING THE AD890 AS A PROGRAMMABLE GAIN AMPLIFIER

The AD890 is ideally suited for use as an accurate video programmable gain amplifier. If the X4 buffers are utilized with the variable gain amplifier, nearly 60 dB of total gain is available at frequencies up to 100 MHz. The VGA gain and exponentiator scale factors are trimmed with respect to dc control potentials applied to the "Gain Set" pin. In this mode of operation (see Logic Assignments for bit pattern to be applied to the "Bit 0" and "Bit 1" pins), a 0 V dc potential applied to the "Gain Set" pin will produce a nominal VGA gain of 30 dB. With an additional 12.75 dB from each X4 buffer, total nominal gain is 55 dB. Each 20 mV increment of voltage applied will produce a 1 dB reduction in gain. A simple equation can be used to calculate the nominal gain of VGA in this mode:

$$VGA\ Gain\ (dB) = (30 - V_{GAIN\ SET} \times 50)$$

where $V_{GAIN\ SET}$ is in volts.

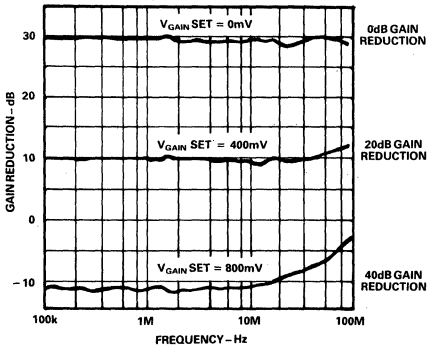


Figure 11. Frequency Response of VGA Gain for Different Gain Set Voltages

OPERATION WITH +5 V, +12 V SUPPLIES

Operation with +5 V (±0.5 V) and +12 V (±0.6 V) supplies is readily achieved. Figure 12 shows the AD890 configured for +5 V, +12 V operation. The analog and digital grounds must be connected to the +5 V line or to an available center tap of

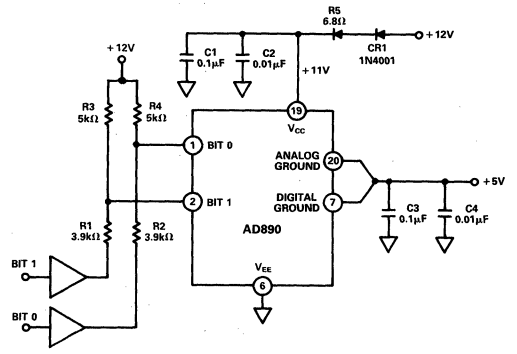


Figure 12. AD890 Connection for +5 V, +12 V Operation

the +12 V supply. Thus connected, a current of approximately 30 mA will flow in this line under normal operation. The input clamping action occurs with respect to this line, increasing its current by an additional 12 mA or so.

Both the +5 V and +12 V supplies should be RF bypassed to ground with at least two capacitors: values of 0.1 μF and 0.01 μF are recommended. In addition, some higher level of decoupling capacitance such as 3.3 μF value may be desirable. Next, insert two 100 mA diodes in series with the +12 V supply. This helps to reduce overdissipation in the chip. Power supply decoupling should occur on the circuit side of the diode network.

Finally, mode control is achieved by using open collector drivers and resistors as shown; 5.1 V Zener diodes can be substituted for resistors R1 and R2. Internal diode clamping in the AD890 permits this mode of operation.

The mode switching times will be affected by resistor values chosen; this is due to the RC time constants formed by the resistors in conjunction with the input capacitance of the chip package.

INTEGRATING WITH THE AD891 RIGID DISK DRIVE DATA QUALIFIER

Figure 13 shows a typical application using the AD890 and AD891 connected together to create a 30 MHz channel (cerdip connections shown). This circuit includes a 5-pole 30 MHz Gaussian-to-6 dB transitional filter plus a second-order RLC time domain equalizer. A typical second-order, fully differential, passive delay-line differentiator interface for the AD891 is also included. (For a more detailed description of the delay-line differentiator, see the AD891 data sheet.) The analog and digital grounds should be connected at the power supply common.

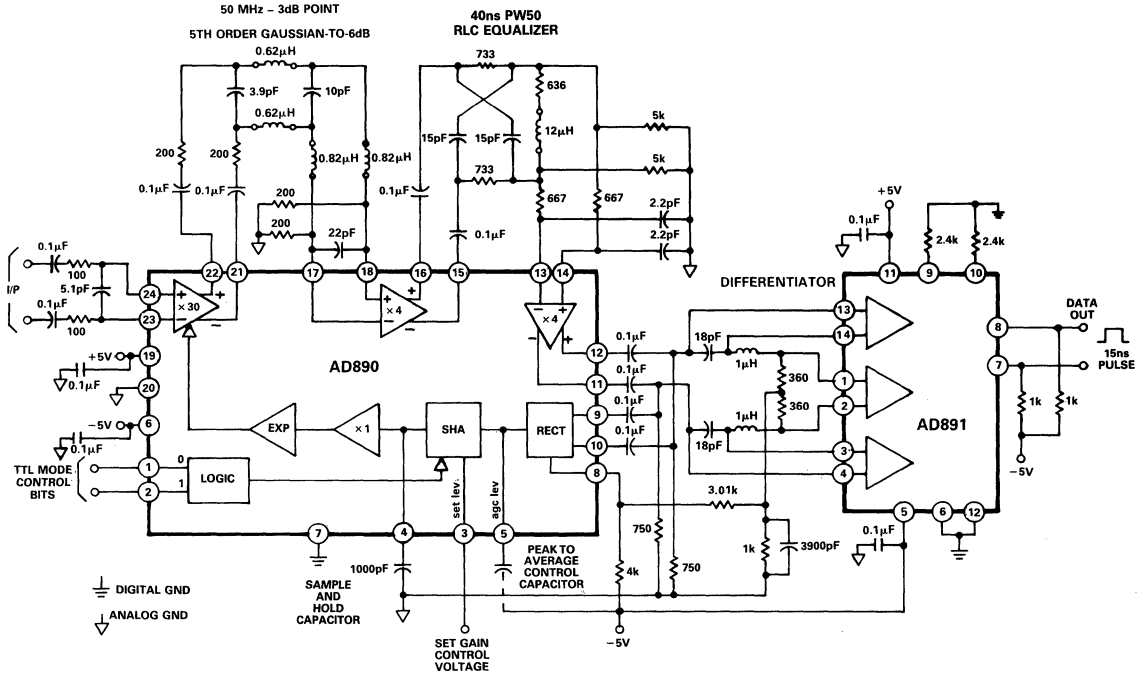


Figure 13. Typical AD890/AD891 Connection for a 30 MHz Channel

USING EQUALIZERS WITH THE AD890

The AD890 is ideal for applications where equalization is employed. The X4 buffer output drivers are designed to operate into 200 Ω loads, making tapped delay-line designs easy. Sum and differencing of different tap weights can be achieved by simple resistive dividers.

As an alternative, a simple RLC network can be implemented to provide a low cost, fully differential alternative to the three-tap, tapped delay-line equalizer which often is used for pulse slimming. Essentially, the equalizer shown in Figure 14 consists of an RC lattice, which provides the magnitude characteristic, together with an LR shunt section which acts to define the overall passband group delay and the ratio of minimum to maximum gains within the passband.

The network shown approximates a function of the form:

$$F(\omega\tau) = 1 - k \cos \omega\tau, \text{ where } k = 0.6, \text{ and } \tau = 36 \text{ ns.}$$

The circuit is optimized for a 120 ns transition PW5O. Altering the 953 Ω resistor and the 24 μH inductor can change both k and τ, permitting cylinder dependent equalization to be performed, thus minimizing problems of overequalization. To alter k, the ratio of the 1.1 kΩ and 953 Ω resistors should be changed. To alter τ, the reactive element should be scaled proportionally. The equalizer in Figure 13 is optimized for k = 0.6 and τ = 12 ns.

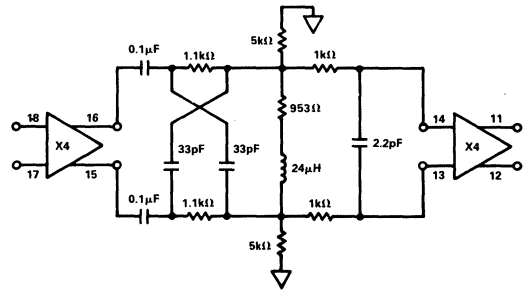


Figure 14. RLC Equalizer

It is important to note the benefits of fully differential (as opposed to single-ended) operation: (1) reduced harmonic distortion due to symmetric operation; (2) improved power supply noise rejection; (3) less insertion loss, allowing for reduced gain and, hence, improved distortion in stages prior to the equalizer.

The magnitude and group delay characteristics of this equalizer are shown in Figures 15 and 16, respectively.

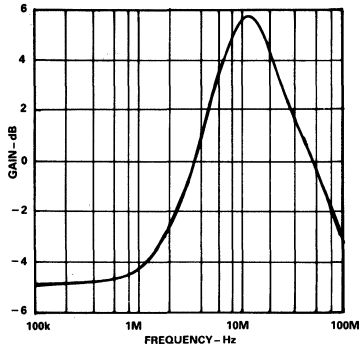


Figure 15. RLC Equalizer Magnitude Response

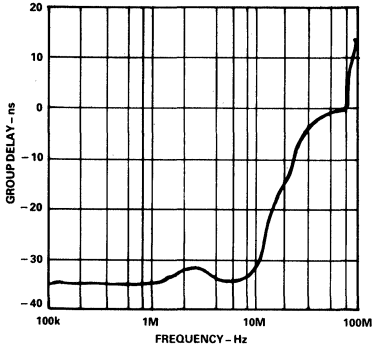


Figure 16. RLC Equalizer Group Delay Response

CHOICE OF LOW PASS FILTER WITH THE RECOMMENDED EQUALIZER

A fifth order, Gaussian-to-6 dB transitional filter is recommended for use with the equalizer. Such a low pass filter is shown in Figure 17. Low group delay ripple and high out-of-band rejection make this design work well with the recommended equalizer and the differentiator specified in the AD891 data sheet. The recommended location for the low pass filter is between the VGA and first X4 buffer. The equalizer should be placed between the first and second X4 buffers. This minimizes the potential for oscillations induced by interstage parasitic feedback.

The magnitude and group delay characteristics of this filter are shown in Figures 18 and 19, respectively.

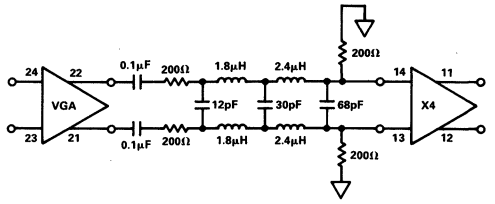


Figure 17. 5th Order Gaussian-to-6 dB Transitional Filter

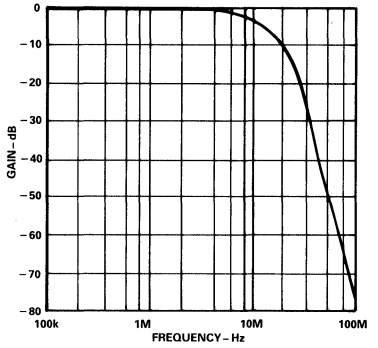


Figure 18. Gaussian Low-Pass Filter Magnitude Response

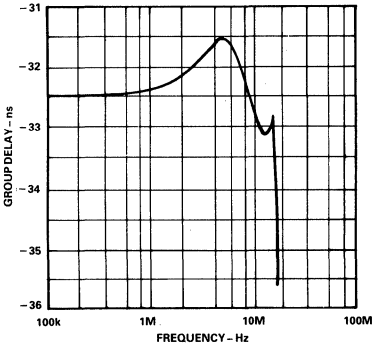


Figure 19. Gaussian Low-Pass Filter Group Delay Response

ANALOG DEVICES

Rigid Disk Data Channel Qualifier

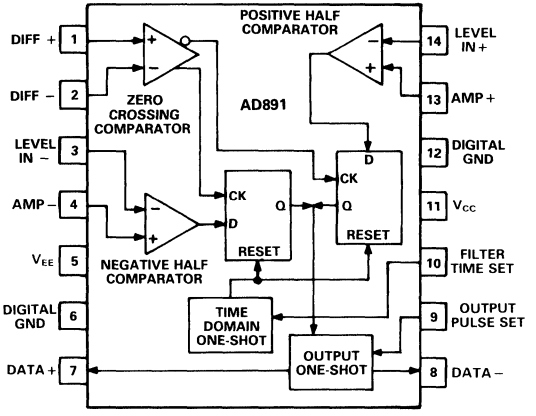
AD891

FEATURES

Three Matched, Offset-Trimmed Comparators
3.1 ns (typ) Comparator Propagation Delay
ECL Logic Permits 50 Mb/s Transfer Rates
6.8 ns Delay (typ) from Inputs to Data Output
500 ps (typ) Additional Pulse Pairing
Temperature-Compensated Operation
Compatible with 10 KH ECL Logic
Two Temperature-Compensated One-Shots
One-Shot Periods Set Using External Resistors

AD891 FUNCTIONAL BLOCK DIAGRAM

Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD891 disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891 provides both level and time-domain qualification. Level qualification is performed on alternating half cycles of the data waveform using a user-defined threshold level which is applied to each of two 3.1 ns propagation delay comparators. This technique prevents single bit errors from being propagated into two bit errors. A third comparator is used to provide zero-crossing detection. Factory trimmed offsets and a careful internal layout ensure symmetric operation and low pulse pairing with a differential input waveform.

An external RLC passive delay-line differentiator should be used with the AD891; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

The outputs from the amplitude-qualification comparators are applied to the "D" inputs of two master-slave D-type flip-flops which are then clocked by the outputs from the zero-crossing comparator. Each valid zero-crossing event causes a one-shot with a user-definable period to be triggered. This disables the operation of the flip-flops, thus preventing the detection of additional zero-crossing events during the one-shot period.

Simultaneously, an output one-shot is activated, the leading edge of which is synchronous with the change in the flip-flop outputs. The period of this one-shot is also user-definable and is intended to ensure adequate output pulse duration for transmission within the external environment. Each one-shot requires a single metal-film resistor to set its period. All one-shots have trimmed pulse periods; temperature stability is maintained by the use of an internal bandgap reference.

The AD891's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600 ps per gate. The output data conforms to standard 10 KH ECL logic levels. The AD891 can drive a properly terminated 75 Ω transmission line.

The AD891 is specified to operate over the commercial (0 to +70°C) temperature range. It is available either in a 14-pin cerdip package or in a 20-pin PLCC package.

SPECIFICATIONS (@ +25°C and 5 V dc, unless otherwise noted)

Model	Conditions	AD891J Min	AD891J Typ	AD891J Max	Units
COMPARATOR SPECIFICATIONS					
Propagation Delay	20 mV Overdrive		3.3		ns
	200 mV Overdrive		3.1		ns
Comparator Mismatch				300	ps
Input Offset Voltage			0.25	**1.0**	mV
Noise Induced Offset Voltage	10^8 Error Rate		±300		μV
Input Offset Current			100		nA
Input Bias Current			1.6	3	μA
Open-Loop Gain	f = 10 MHz		66		dB
Input Resistance	Differential		500		kΩ
Input Capacitance	Differential		1	5	pF
Input Common-Mode Range	Referred to Digital GND	−1.5		+2.2	V
INTERNAL LOGIC SPECIFICATIONS					
Logic "1" Level		−0.98	−0.85	−0.81	V
Logic "0" Level		−1.95	−1.85	−1.63	V
Rise Time			1.2		ns
Fall Time			1.0		ns
D-Type Flip-Flops					
Clock – Q Delay			1.3		ns
Clock – $\overline{Q}$ Delay			1.2		ns
Reset – Q Delay			0.6		ns
Reset – $\overline{Q}$ Delay			0.55		ns
ONE-SHOT SPECIFICATIONS					
Resistor Scaling[1]		One-Shot Pulse ≈ 7+3.1 R_{SET}			
Pulse Duration	$R_{SET} = R_{min}$ to R_{max}	9		180	ns
	R_{SET} = 30 kΩ	**95**	100	**105**	ns
	R_{SET} = 10 kΩ	**35**	38	**41**	ns
Resistor Range	$R_{SET} = R_{min}$ to R_{max}	0.75		56	kΩ
EXTERNAL LOGIC SPECIFICATIONS[2]	T_J = +25°C				
Output Logic "1"		−0.98	−0.85	−0.81	V
Output Logic "0"		−1.95	−1.85	−1.63	V
Rise Time			1.4		ns
Fall Time			1.2		ns
DATA THROUGHPUT SPECIFICATIONS					
Propagation Delay[3]	Differentiator Input to Data Output		6.8		ns
Additional Pulse Pairing[4]	200 mV Overdrive 5 ns Input Rise Time	**0**	500	**1000**	ps
Max Transfer Rate		50			Mb/s
Min Transfer Rate[5]				1	Mb/s
POWER SUPPLY REQUIREMENTS					
Operating Range					
V_{CC}		4.5	5.0	5.5	V
V_{EE}		−4.68	−5.2	−5.72	V
Quiescent Current	T_{min} to T_{max}				
V_{CC}		15	23	35	mA
V_{EE}		55	68	85	mA

NOTES

[1]One-shot pulse in ns; R_{SET} specified in kΩ.

[2]Logic specifications obtained for the "Data +" and "Data −" outputs using 1 kΩ pull-down resistors tied to V_{EE} and 100 Ω resistors connected to −2 V.

[3]Propagation delay is measured from the zero-crossing comparator input to the "Data +" output with 200 mV overdrive.

[4]Measurements were performed using a ±100 mV square wave having a rise time under 5 ns; this was applied to the input of the zero-crossing comparator. The resultant pulse pairing is the difference in delay times for two consecutive output pulses.

[5]The minimum transfer rate is limited only by the maximum recommended one-shot period of 180 ns.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

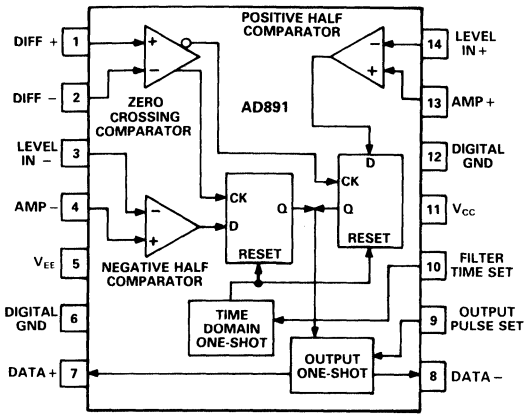
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±7.5 V
Comparator Differential Input Voltage . . . . . ±5.6 V
Storage Temperature Range P, Q . . . . . −65°C to +150°C
Operating Temperature Range[2]
AD891P, AD891Q . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

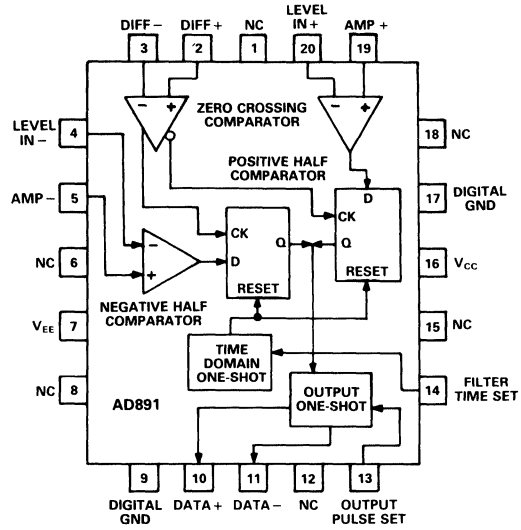
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]20-pin PLCC package: θ_{JA} = +70°C/Watt;
14-pin cerdip package: θ_{JA} = +105°C/Watt.

PIN CONFIGURATIONS

14-Pin Cerdip (Q) Package



20-Pin PLCC (P) Package



ORDERING GUIDE*

Model No.	Description	Package Option
AD891JQ	14-Pin Cerdip	Q-14
AD891JP	20-Pin PLCC	P-20A

*See Section 20 for package outline information.

Typical Characteristics (@ +25°C with ±5 V Supplies)

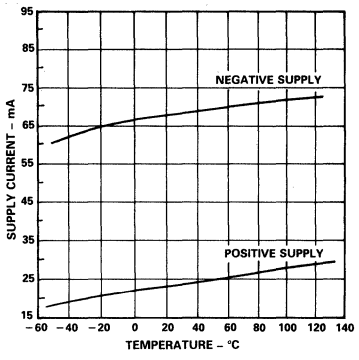


Figure 1. Supply Current vs. Temperature

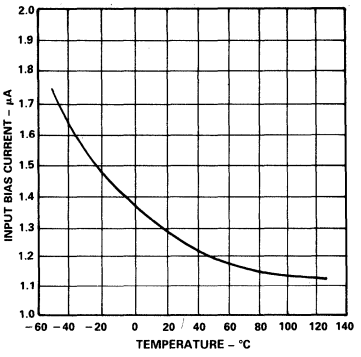


Figure 2. Comparator Input Bias Current vs. Temperature

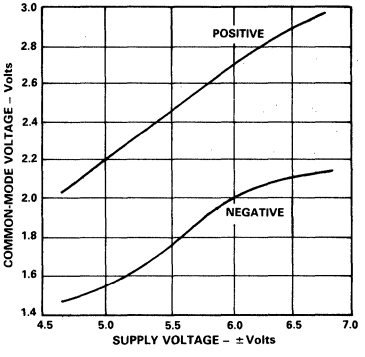


Figure 3. Comparator Common-Mode Voltage vs. Supply Voltage

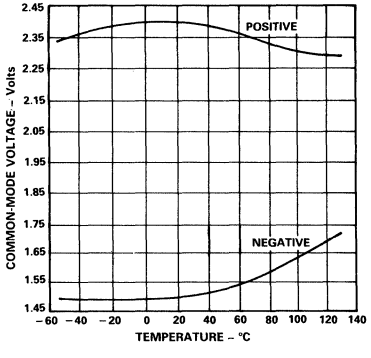


Figure 4. Comparator Common-Mode Voltage vs. Temperature

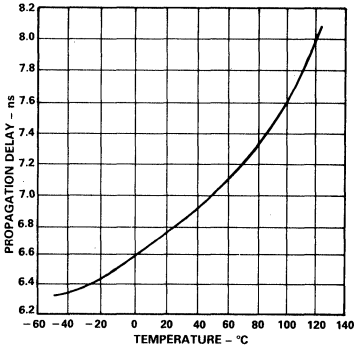


Figure 5. Propagation Delay vs. Temperature

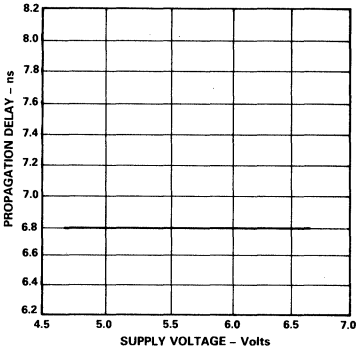


Figure 6. Propagation Delay vs. Power Supply Voltage

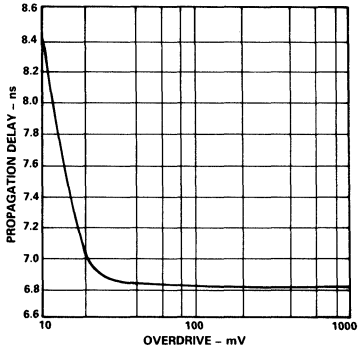


Figure 7. Propagation Delay vs. Overdrive

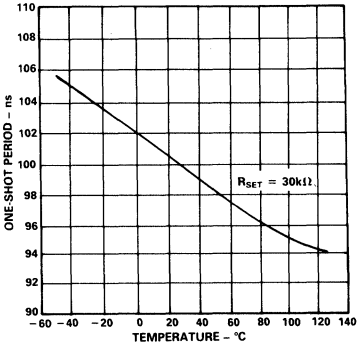


Figure 8. One-Shot Period vs. Temperature

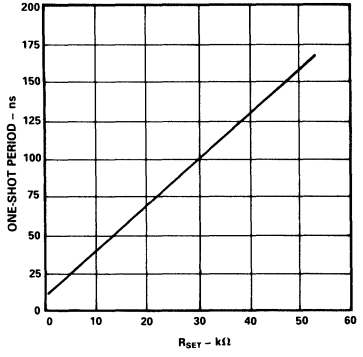


Figure 9. One-Shot Period vs. R_{SET}

THEORY OF OPERATION

The AD891 consists of three comparators, two D-type flip-flops, an internal bandgap reference and a pair of externally adjustable one-shots. Two comparators are used to provide data amplitude qualification, and the third acts as a zero-crossing detector when used with an external passive differentiator circuit. (Refer to the AD891 block diagram and Figure 11.)

Figure 10 illustrates the operation of the AD891, using the recommended passive delay-line differentiator described in the following section. Sequence "A" represents the pattern written on the disk where a logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the AD891 consists of a sequence of alternating pulses "B." The data pattern shown is worst case for a 1-7 code input. "C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in state of this output are used to clock the two internal D-type flip-flops. The flip-flops are enabled using the output "E" from the positive and negative threshold comparators, such that the flip-flop outputs change state only when the analog input exceeds the programmed threshold levels (positive or negative). When the threshold levels are exceeded and a zero-crossing event occurs, the flip-flops change state, producing an output pulse "F." The duration of this pulse, seen at the Data+/Data− outputs, is set using an external resistor, as is the internal time-out which is used to prevent noise induced retriggering. The final output data sequence is shown in "G." As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a time-shifted version of the write data.

Since the 1-7 code input is the most demanding of the popular encoding schemes to qualify, the AD891 is clearly suitable for other codes, such as MFM and 2-7. The recommended time domain filter one-shot period for MFM and 1-7 code is equal to 75% of the bit cell clock period. For 2-7 code the one-shot period can be increased to 150% of the bit cell clock period.

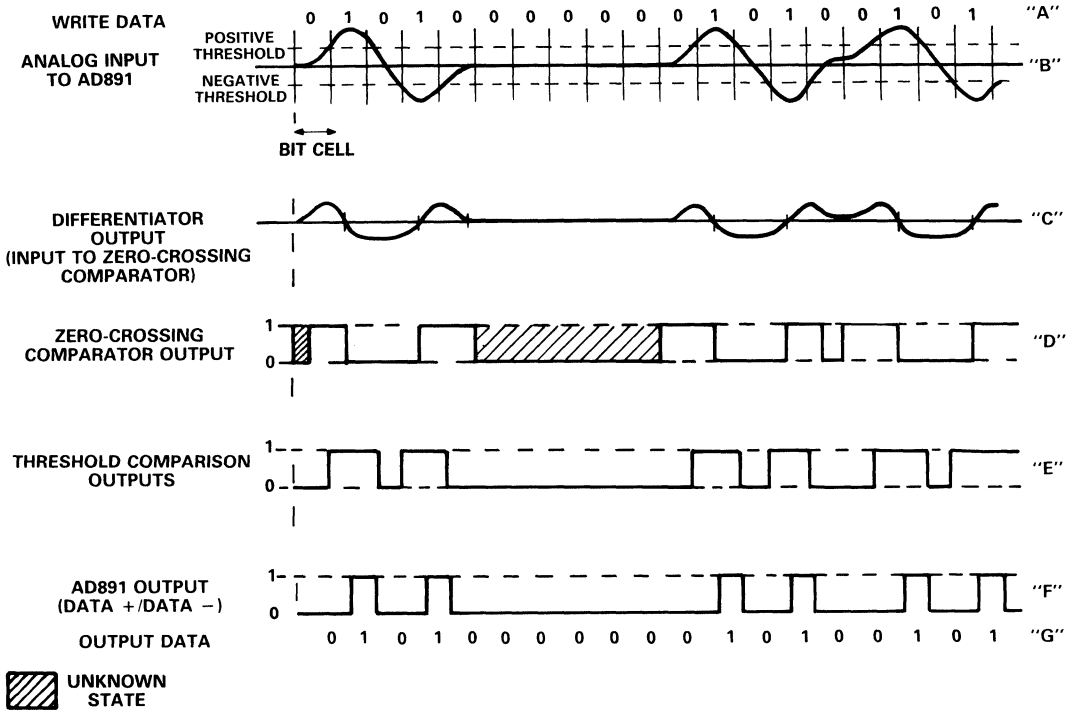


Figure 10. AD891 Operation for Worst Case 1-7 Code Pattern

DESIGN CONSIDERATIONS

In designing a suitable passive delay-line differentiator, either the fully differential (Figure 11a) or single-ended (Figure 11b) configuration can be used. The equations governing component selection for both connections are as shown.

If the single-ended configuration is employed, then the inputs to the negative half-cycle comparator need to be biased such that the comparator is turned off. This can be accomplished by placing the "Amp−" input at a potential at least 100 mV more negative than the "Level In−" input. The "Amp−" pin may be connected to the "V_{EE}" pin and the "Level In−" pin may be connected to the "Digital GND" pin, provided that the potential difference does not exceed 5.6 volts, which is the absolute maximum differential input rating of the device.

Good RF layout practice should be obeyed, with decoupling networks of 0.1 μF in parallel with 0.01 μF at both the "V_{CC}" and "V_{EE}" pins. A ground plane should be used extensively. Two digital grounds are supplied: Pin 12 is for the internal logic while Pin 5 is provided for the "Data" outputs only. (These pins are for the cerdip package; the corresponding PLCC package pins are 17 and 9, respectively.) The filter time and output pulse setting resistors should be tied, as directly as possible, to the "Digital GND" pin.

The "Data−" and "Data+" pins require pull-down resistors to "V_{EE}" as per normal practice in ECL. The use of 30 kΩ resistors connected between the "Filter Time Set" and "Output Pulse Set" pins and digital ground will produce a nominal 100 ns one-shot period; 10 kΩ resistors will nominally produce 38 ns one-shot periods. The timing of the two one-shots may be set independently.

For best performance, the three input comparators should be operated at a common-mode potential close to digital ground. The digital ground should be connected to the analog ground as near to the power supply as possible to minimize noise injection.

INTEGRATING WITH THE AD890 WIDEBAND CHANNEL PROCESSING ELEMENT

Figure 12 shows a typical application using the AD891 and AD890 connected together to create a 30 MHz channel (cerdip connections shown). This circuit includes a 5-pole 30 MHz Gaussian-to-6 dB transitional filter plus a second-order RLC time domain equalizer. The fully differential passive delay-line differentiator previously discussed is also included. The analog and digital grounds should be connected only to the power supply common.

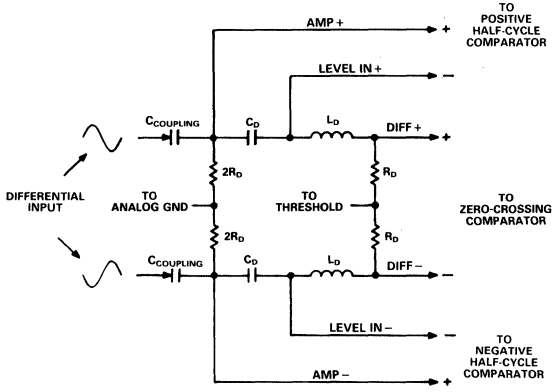


Figure 11a. Fully Differential Configuration of Passive Delay-Line Differentiator

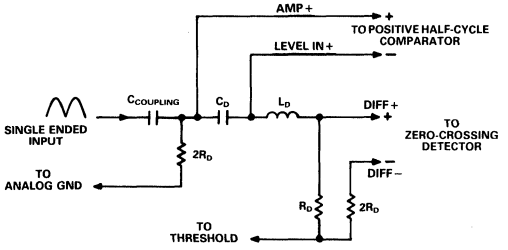


Figure 11b. Single-Ended Configuration of Passive Delay-Line Differentiator

RECOMMENDED COMPONENTS

$$f_D = \frac{1}{2\pi\sqrt{L_D C_D}}$$

f = 1.5 Times the Maximum Desired Differentiated Frequency

$$R_D = K\left[\sqrt{\frac{L_D}{C_D}}\right]$$

R_D Minimum Value: 120 Ω
150 Ω or Greater Is Recommended

1.3 (Best Magnitude Response) ≤K ≤1.7 (Best Group Delay Response)

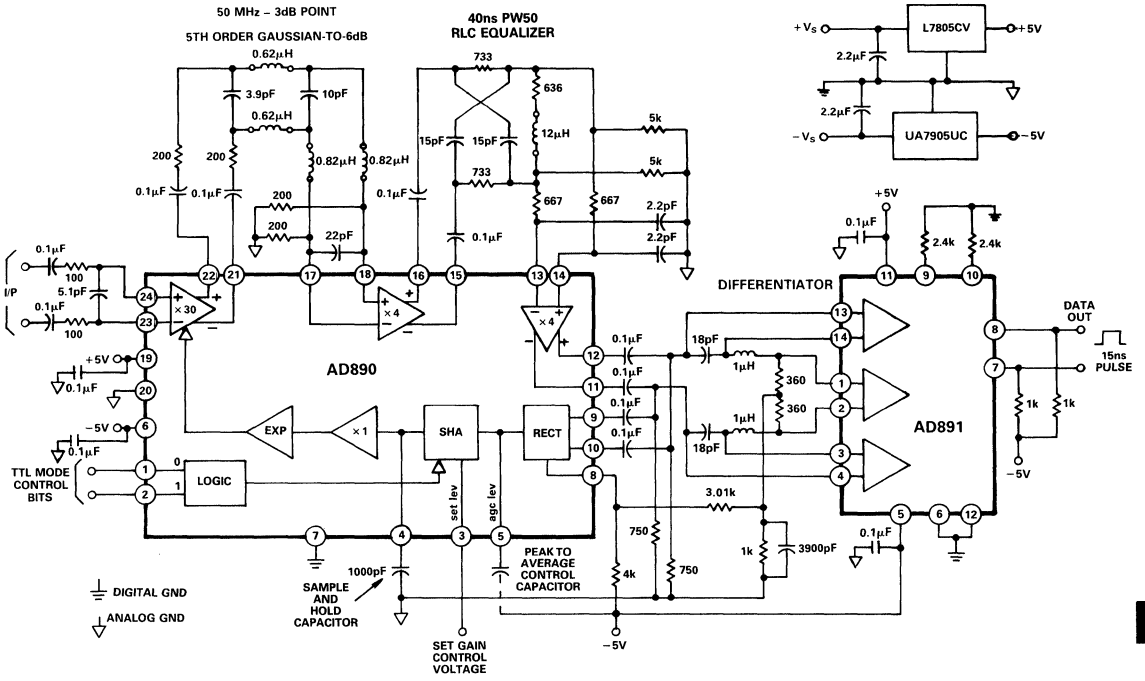


Figure 12. Typical AD890/AD891 Connection for a 30 MHz Channel

OPERATION WITH +5 V, +12 V SUPPLIES

Operation with +5 V (±0.5 V) and +12 V (±0.6 V) supplies is readily achieved. The digital ground pins must be connected to the +5 V line or to an available center tap of the +12 V supply. The specified output ECL logic levels are therefore referred to the +5 V supply. Pull-down resistors for the "Data+" and "Data–" pins should be connected to V_{EE}. Thus connected, a current of approximately 23 mA will flow in the +5 V supply under normal operation.

In order to ensure correct comparator operation, a pair of 100 mA diodes should be added in series with the +12 V supply which is connected to the V_{CC} terminal. This connection is shown in Figure 13 (shown for cerdip package).

Both the +5 V and +12 V supplies should be RF bypassed to ground; the values of 0.1 μF and 0.01 μF in parallel are recommended. In addition, some higher value of decoupling capacitance – such as 3.3 μF – may be desirable. This decoupling should be applied directly at the AD891 "V_{CC}" and "Digital GND" pins. Finally, the common-mode range for the comparators is now referred to the +5 V supply line, and care must be taken to operate within the common-mode limits.

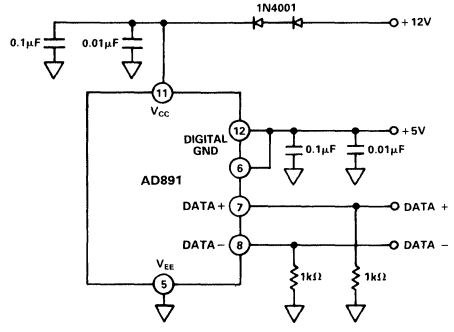


Figure 13. AD891 Connection for +5 V, +12 V Operation

RESPONSE CHARACTERISTICS OF THE FULLY DIFFERENTIAL DELAY-LINE DIFFERENTIATOR

Figures 14 through 17 show typical performance to be expected from the recommended passive, fully differential, delay-line differentiator previously discussed. Figures 14 and 15 depict magnitude and phase response for the undifferentiated output, respectively. Figure 16 shows magnitude response for the differentiated output, and Figure 17 shows phase error between the two outputs.

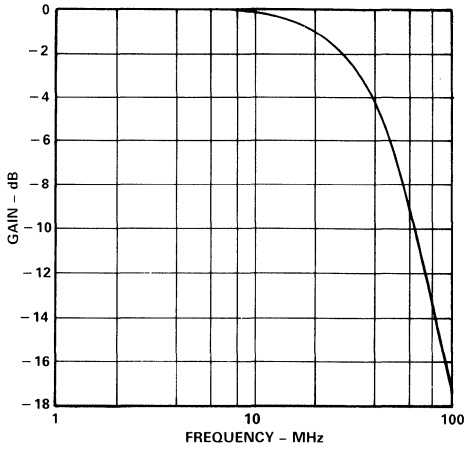


Figure 14. Magnitude Response of Undifferentiated Output

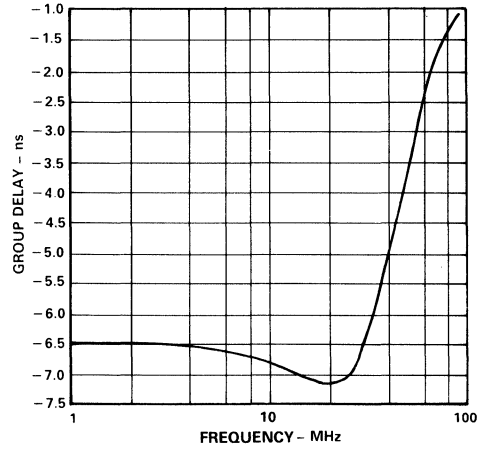


Figure 15. Group Delay Characteristics of Undifferentiated Output

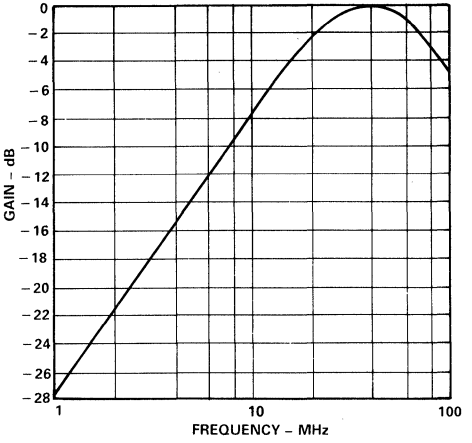


Figure 16. Magnitude Response of Differentiated Output

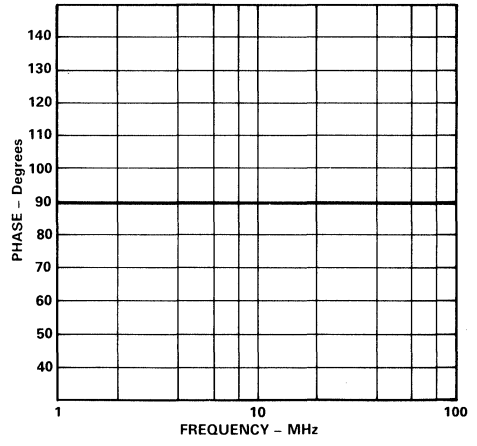


Figure 17. Relative Phase Between Differentiated and Undifferentiated Outputs

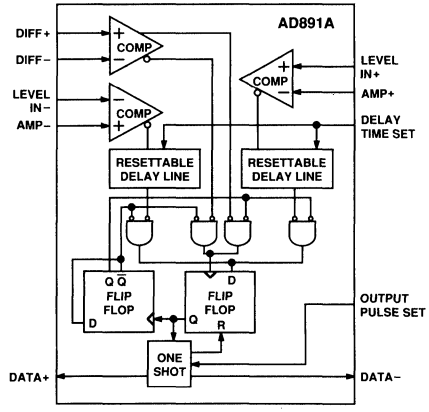
50 Mb/s Rigid Disk Data Qualifier

AD891A

FEATURES

Three Matched, Offset-Trimmed Comparators
ECL Logic Permits 50 Mb/s Transfer Rates
Three Levels of Data Qualification
Amplitude
Time Above Threshold
Polarity of Data
100 ps Typical Additional Pulse Pairing
Temperature Compensated Operation
Compatible with 10KH ECL Logic
One-Shot Period Set Using External Resistor
Time Above Threshold Qualification Set Using an External Resistor

AD891A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD891A disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891A provides three levels of data qualification. Level qualification is performed on alternating half-cycles of the data waveform using a user-defined threshold level which is applied to each of two comparators. The outputs of each comparator drive a user-programmable "resettable" delay-line. The "resettable" delay-line function allows the user to define the minimum time a data pulse must exceed the amplitude qualification level before a zero-crossing can be detected. The resettable delay-lines drive NAND gated flip-flops. A third zero-crossing comparator is employed to clock the NAND gated flip-flop. The NAND-gated flip-flop in turn drives the second flip-flop. The second flip-flop feeds back to the input of the NAND-gated flip-flop. The toggle action of the second flip-flop, therefore, provides alternate polarity data qualification. To ensure symmetric operation and low pulse pairing, all three comparators have trimmed offsets.

An external RLC passive delay-line/differentiator should be used with the AD891A; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

Each valid data pulse causes a one-shot to generate a pulse with a user-defined width. During the one-shot period the NAND-gated flip-flop is disabled, preventing detection of additional zero-crossing events. The one-shot also drives the ECL "Data Output" driver. The one-shot requires a single metal-film resistor to set its pulse width. Temperature stability is maintained by the use of an internal bandgap reference.

The AD891A's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600 ps per gate. The output data conforms to standard 10KH ECL logic levels. The AD891A can drive a properly terminated 75 Ω transmission line.

The AD891A is specified to operate over the commercial (0 to +70°C) temperature range. It is available in a 20-pin PLCC package (samples are available in a 14-pin side braze package).

9

SPECIFICATIONS (@ +25°C and +5 V, −5.2 V dc, unless otherwise noted)

Parameter	Conditions	AD891AJ Min	AD891AJ Typ	AD891AJ Max	Units
COMPARATOR SPECIFICATIONS					
Input Offset Voltage			0.25	**1.0**	mV
Input Offset Current			100		nA
Input Bias Current			1.6	**3.0**	μA
Open Loop Gain	f = 10 MHz		66		dB
Input Resistance	Differential		500		kΩ
Input Capacitance	Differential		1	5	pF
Input Common Mode Range	Referred to Digital GND	−1.5		+2.2	V
RESETTABLE DELAY-LINE SPECIFICATIONS					
Resistor Scaling[1]		Delay ≈ 2 + 5 × R_{SET}			ns
Pulse Duration	R_{SET} = 1 kΩ	**5**	7	**12**	ns
	R_{SET} = 5 kΩ	**18**	27	**36**	ns
Resistor Range	R_{SET} = R_{min} to R_{max}	0.30		33	kΩ
OUTPUT ONE-SHOT SPECIFICATIONS					
Resistor Scaling[1]		One-Shot Pulse ≈ 3 + 5 × R_{SET}			ns
Pulse Duration	R_{SET} = 4 kΩ	**17**	23	**31**	ns
	R_{SET} = 10 kΩ	**40**	53	**72**	ns
Resistor Range	R_{SET} = R_{min} to R_{max}	0.60		33	kΩ
EXTERNAL LOGIC SPECIFICATIONS[2]					
Output Logic "1"		−0.98	−0.85	−0.81	V
Output Logic "0"		−1.95	−1.85	−1.63	V
Rise Time			1.4		ns
Fall Time			1.2		ns
DATA THROUGHPUT SPECIFICATIONS					
Propagation Delay[3]	Differentiator Input to 10% of Data Output		6.0		ns
Additional Pulse Pairing[4]	200 mV Overdrive 5 ns Input Rise Time		100	1000	ps
Max Transfer Rate		50			Mb/s
POWER SUPPLY REQUIREMENTS					
Operating Range V_{CC}		+4.5		+5.5	V
Operating Range V_{EE}		−4.68		−5.72	V
Quiescent Current	T_{min} to T_{max}				
I_{CC}		**12**	16	**30**	mA
I_{EE}		**−40**	−55	**−80**	mA

NOTES
[1]R_{SET} specified in kΩ.
[2]Logic specifications obtained for the "Data +" and "Data −" outputs using 50 Ω pull down to −2.0 volts.
[3]Propagation delay is measured from the zero crossing comparator input to the "Data +" output with 200 mV overdrive.
[4]Measurements were performed using a ±100 mV square wave having a rise time under 5 ns; this was applied to the input of the zero crossing comparator. The resultant pulse pairing is the difference in delay times for two consecutive output pulses.

ABSOLUTE MAXIMUM RATINGS[1]

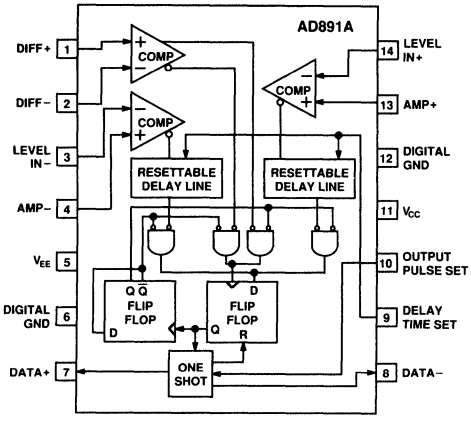
Supply Voltage . . . . . ±7.5 V
Comparator Differential Input Voltage . . . . . ±5.6 V
Storage Temperature Range P, Q . . . . . −65°C to +150°C
Operating Temperature Range[2]
AD891AJP, AD891AJD . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

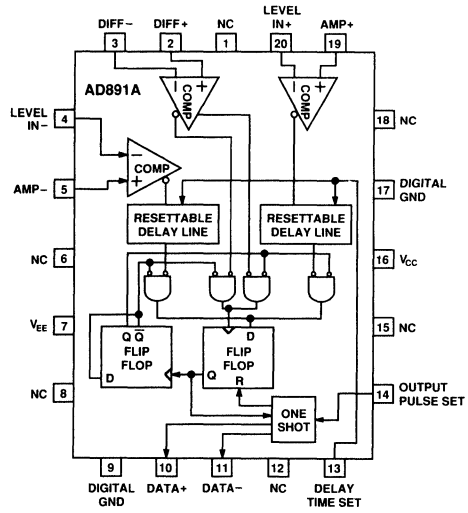
[2]20-pin PLCC package: θ_{JC} = 70°C/Watt;
14-pin side brazed package (samples only): θ_{JA} = 105°C/Watt.

PIN CONFIGURATIONS

14-Pin Side Brazed Package (D)



20-Pin PLCC Package (P)



ORDERING GUIDE*

Model	Package	Package Option
AD891AJP	20-Pin PLCC	P-20A
AD891AJD	14-Pin Side Brazed (Samples Only)	D-14

*See Section 20 for package outline information.

Typical Characteristics (@ +25°C with +5 V, −5.2 V Supplies)

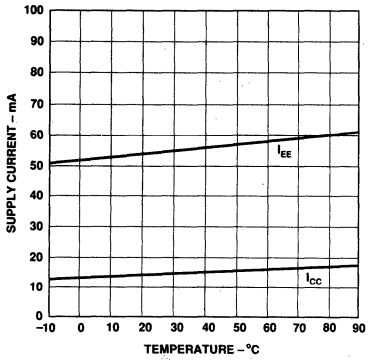


Figure 1. Supply Current vs. Temperature

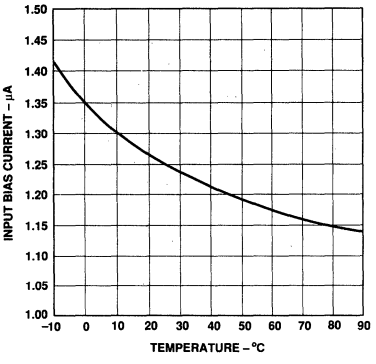


Figure 2. Comparator Input Bias Current vs. Temperature

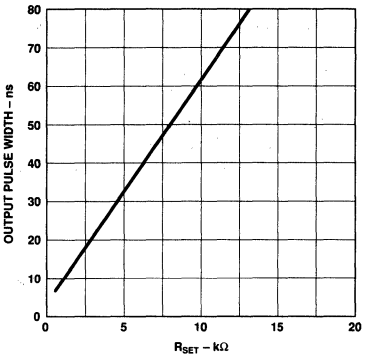


Figure 3. Output One-Shot Pulse Width vs. R_{SET}

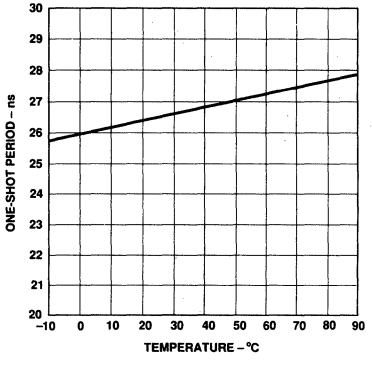


Figure 4. Output One-Shot Pulse Width vs. Temperature (R_{SET} = 4 kΩ)

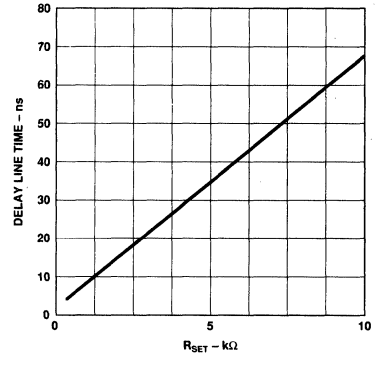


Figure 5. Delay-Line Time vs. R_{SET}

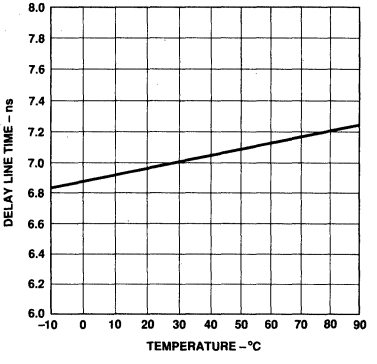


Figure 6. Delay-Line Time vs. Temperature (R_{SET} = 1 kΩ)

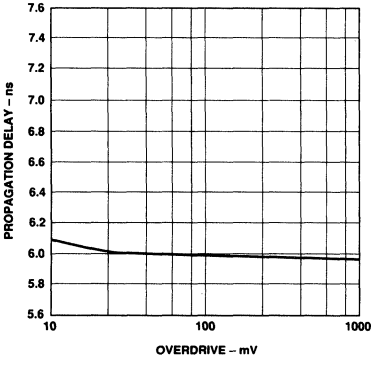


Figure 7. Propagation Delay (Comparator to Data Out) vs. Input Overdrive

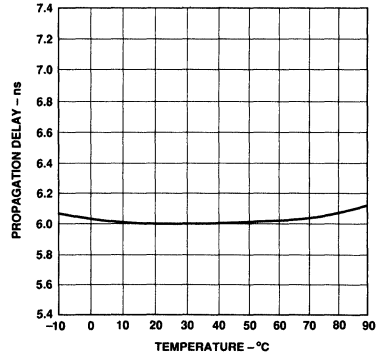


Figure 8. Propagation Delay (Comparator to Data Out) vs. Temperature

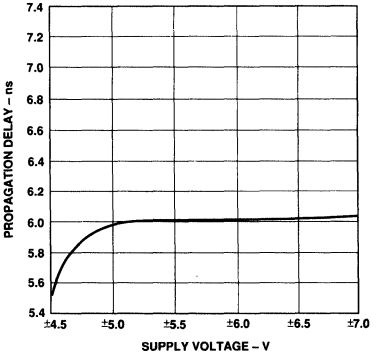


Figure 9. Propagation Delay (Comparator to Data Out) vs. Power Supply Voltage

THEORY OF OPERATION

The AD891A consists of three comparators, a pair of externally adjustable "resettable" delay-lines, four NAND gates, two D-type flip-flops, an internal bandgap reference and an externally adjustable one-shot (refer to the AD891A block diagram).

Figure 10 illustrates the operation of the AD891A, using the recommended passive delay-line/differentiator described in the following section. Sequence "A" represents the pattern written on the disk, where a logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the AD891A consists of a sequence of alternating pulses "B." The data pattern shown is for worst case RLL 1–7 code input. The AD891A requires that the analog data input pass three criteria in order to qualify a signal and produce an output bit. The triple data qualification requirement significantly reduces errors by ensuring that noise will not be misinterpreted.

The first data qualification criteria is signal amplitude and is accomplished through the use of two amplitude threshold comparators. The outputs of each comparator drive a "resettable" delay-line. The "resettable" delay-line implements the second valid-data criteria: minimum time above valid-signal threshold before a zero-crossing can be detected. The minimum time above valid-signal threshold is set through an external resistor. The output of the "resettable" delay-line is then used to determine if the data exhibits the correct polarity, the third data qualification criteria. To determine if the data exhibits the correct polarity, a D-type flip-flop is used. The flip-flop is toggled with each valid data pulse, thereby, ensuring an alternate polarity qualification for each valid incoming data bit.

"C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in state of this output are used to clock an internal D-type flip-flop. The flip-flop is enabled using the output from the data polarity check, such that the flip-flop output changes state only when all three of the data qualification criteria, described earlier, have been satisfied. If all three data qualification criteria were met, and a zero-crossing event occurs, the flip-flop changes state, producing an output pulse "E." The duration of this pulse, seen at the Data +/Data − outputs, is set using an external resistor. The one-shot also triggers the second D-type flip-flop, toggling the required valid-data polarity. The final output data sequence is shown in "F." As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a reconstructed version of the write data.

Since the 1–7 code input is the most demanding of the popular encoding schemes to qualify, the AD891A easily handles such other codes as MFM and RLL 2–7.

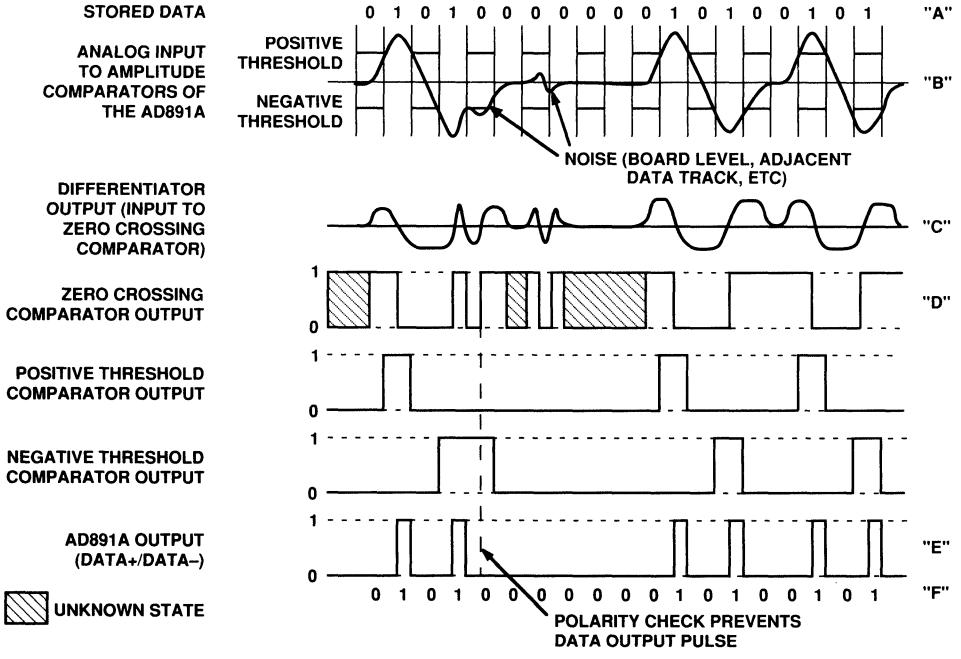


Figure 10. AD891A Operation for Worst Case 1–7 RLL Code

DESIGN CONSIDERATIONS

In designing a suitable passive delay-line differentiator, either the fully differential (Figure 11a) or single-ended (Figure 11b) configuration can be used. The equations governing component selection for both connections are as shown.

If the single-ended configuration is employed, then the inputs to the negative half-cycle comparator need to be biased such that the comparator is turned off. This can be accomplished by placing the "Amp −" input at a potential at least 100 mV more negative than the "Level In −" input. The "Amp −" pin may be connected to the "V_{EE}" pin and the "Level In −" pin may be connected to the "Digital GND" pin, provided that the potential difference does not exceed 5.6 volts, which is the absolute maximum differential input rating of the device.

Good RF layout practice should be obeyed, with decoupling networks of 0.1 μF in parallel with 0.01 μF at both the "V_{CC}" and "V_{EE}" pins. A ground plane should be used extensively. Two digital grounds are supplied: Pin 17 is for the internal logic while Pin 9 is provided for the "Data" outputs only. (These pins are for the PLCC package; the corresponding Side Braze package pins are 12 and 5, respectively.) The "resettable" delay-line and output pulse setting resistors should be tied, as directly as possible, to the "V_{EE}" pin.

The "Data −" and "Data +" pins require pull-down resistors to "V_{EE}" as per normal practice in ECL. The use of a 4 kΩ resistors connected between the "Output Pulse Set" pin and "V_{EE}" will produce a nominal 23 ns one-shot pulse width; 10 kΩ resistors will nominally produce 53 ns one-shot pulse width. A 7 ns minimum time above threshold qualification may be implemented with a 1 kΩ resistor connected between the "Delay Set" pin and "V_{EE}."

For best performance, the three input comparators should be operated at a common mode potential close to digital ground. The digital ground should be connected to the analog ground as near to the power supply as possible, to minimize noise injection.

INTEGRATING WITH THE AD890 WIDEBAND CHANNEL PROCESSING ELEMENT

Figure 12 shows a typical application using the AD891AJP and AD890JP connected together to create a 30 MHz channel. This circuit includes a 5-pole 30 MHz gaussian-to-6 dB transitional filter plus a second-order RLC time domain equalizer. The fully differential passive delay-line differentiator previously discussed is also included. The analog and digital grounds should be connected only to the power supply common.

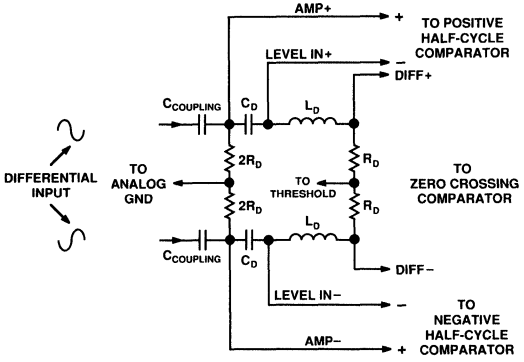


Figure 11a. Fully Differential Configuration of Passive Delay-Line Differentiator

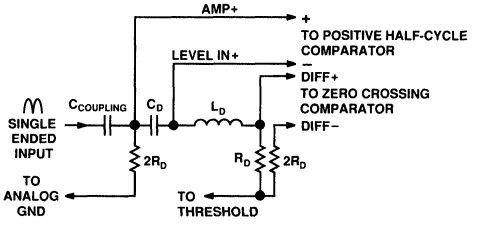


Figure 11b. Single-Ended Configuration of Passive Delay-Line Differentiator

RECOMMENDED COMPONENTS

$$f_D = \frac{1}{2\pi\sqrt{L_D C_D}}$$

f_D = 1.5 Times the Maximum Desired Differentiated Frequency

$$R_D = K\left[\sqrt{\frac{L_D}{C_D}}\right]$$

R_D Minimum Value: 120 Ω
150 Ω or Greater is Recommended

1.3 (Best Magnitude Response) ≤K ≤1.7 (Best Group Delay Response)

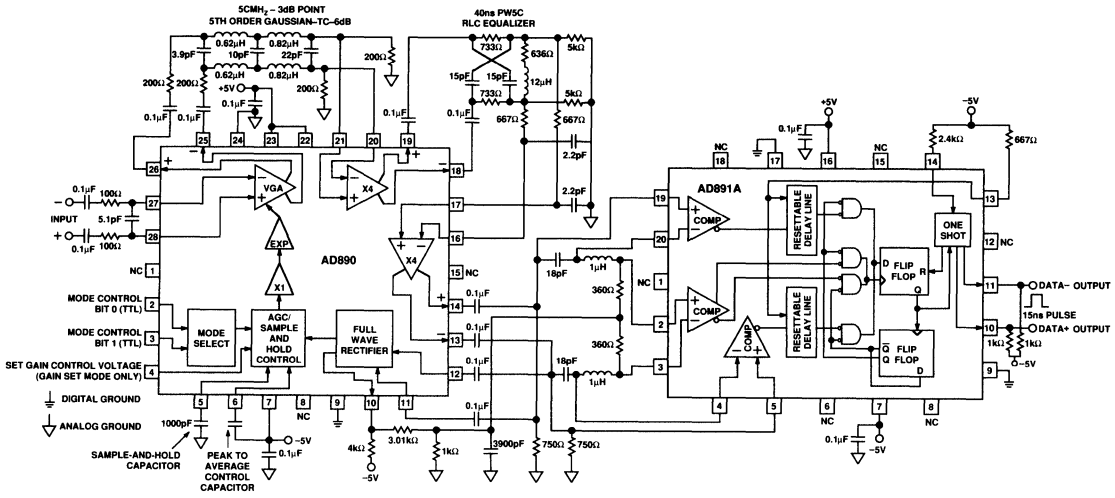


Figure 12. Typical AD890/AD891A Connection for a 30 MHz Channel

9

OPERATION WITH +5 V, +12 V SUPPLIES

Operation with +5 V (±0.5 V) and +12 V (±0.6 V) supplies is readily achieved. The digital ground pins must be connected to the +5 V line. The specified output ECL logic levels are therefore referred to the +5 V supply. Pull-down resistors for the "Data +" and "Data −" pins should be connected to "V_{EE}." Thus connected, a current of approximately 23 mA will flow in the +5 V supply under normal operation.

In order to ensure correct comparator operation, a pair of 100 mA diodes should be added in series with the +12 V supply which is connected to the "V_{CC}" terminal. This connection is shown in Figure 13 (shown for PLCC package).

Both the +5 V and +12 V supplies should be RF bypassed to ground; the values of 0.1 μF and 0.01 μF in parallel are recommended. In addition, some higher value of decoupling capacitance – such as 3.3 μF – may be desirable. This decoupling should be applied directly at the AD891A "V_{CC}" and "Digital GND" pins. Finally, the common mode range for the comparators is now referred to the +5 V supply line and care must be taken to operate within the common mode limits.

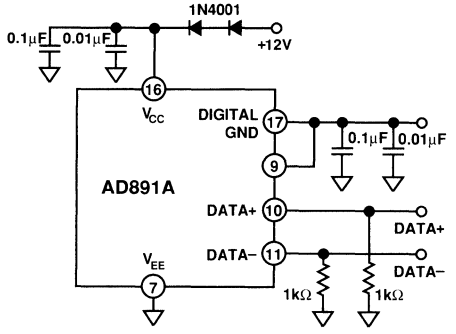


Figure 13. AD891AJP Connection for +5 V, +12 V Operation (+12 V ±5%, +5 V ±10%)

RESPONSE CHARACTERISTICS OF THE FULLY DIFFERENTIAL DELAY-LINE DIFFERENTIATOR

Figures 14 through 17 show typical performance to be expected from the recommended passive, fully differential, delay-line differentiator previously discussed. Figures 14 and 15 depict magnitude and phase response for the undifferentiated output, respectively. Figure 16 shows magnitude response for the differentiated output, and Figure 17 shows phase error between the two outputs.

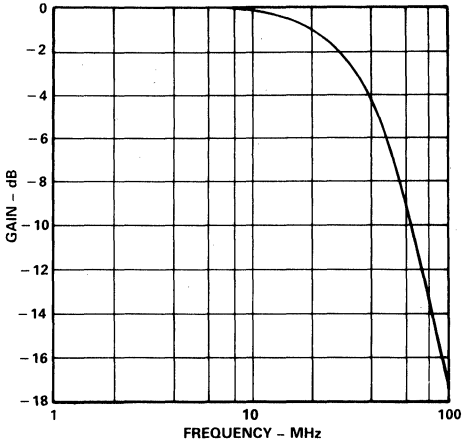


Figure 14. Magnitude Response of Undifferentiated Output

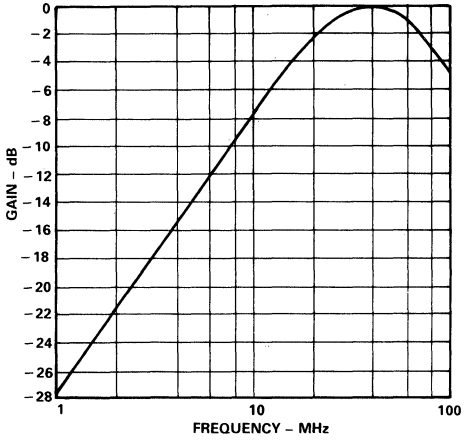


Figure 16. Magnitude Response of Differentiated Output

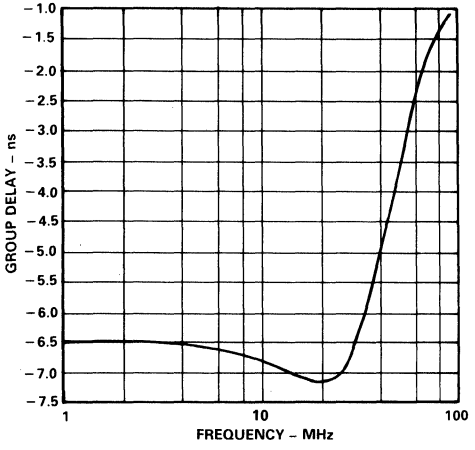


Figure 15. Group Delay Characteristics of Undifferentiated Output

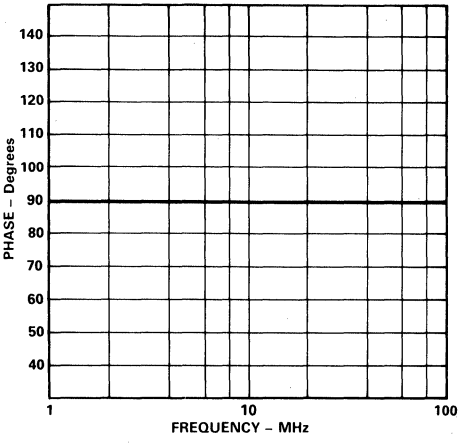


Figure 17. Relative Phase Between Differentiated and Undifferentiated Outputs

ANALOG DEVICES

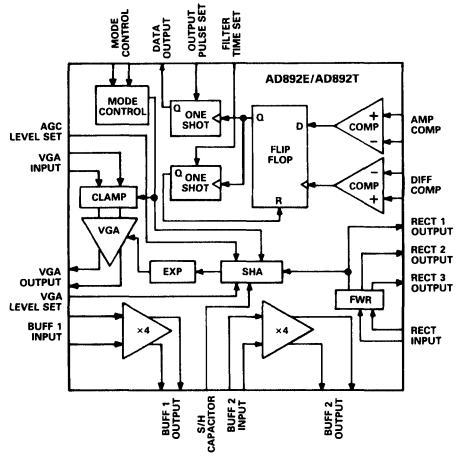
30 Mb/s Peak Detectors

AD892E/AD892T

FEATURES

30 Mb/s Data Transfer Rate Capability (AD892E)
25 Mb/s Data Transfer Rate Capability (AD892T)
1 ns (max) Additional Pulse Pairing
Two Versions
Differential ECL Data Output (AD892E)
TTL Data Output (AD892T)
Variable Gain Amplifier with 30 dB max Gain and 40 dB Control Range
Two Gain of 4 RF Buffers with 200 Ω Differential-Load Drive Capability
0.2 dB/ms Typical Gain Drift in Hold Mode
1 μs AGC Attack/Decay Times Using a 1000 pF External Capacitor
Dynamic Input Clamp Ensures Fast Recovery after Write to Read Transients
Two Matched Offset Trimmed Comparators
One-Shot Pulse Width Set Using External Resistor
Operates from +5 V and +12 V Supplies

AD892E/AD892T FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD892E/AD892T is a complete subsystem for recovering binary information from differentiating channels with transfer rates up to 30 megabits per second. It is connected to the output of the head amplifier and performs the signal conditioning and the data qualification task with a minimum of external components.

The AD892E/AD892T has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Fast acquisition and low droop while in the hold mode allows for the AGC operation to be performed within the sector header without compromising channel behavior when reading data. Two user-defined filter/equalizer stages may be employed, thus allowing maximum design flexibility. This greatly simplifies the design of the overall channel characteristics.

Three low offset, 50 MHz full-wave rectifiers are provided. One rectifier drives the internal sample-and-hold circuitry; this signal is available to the user to set the attack and decay characteristics of the sample and hold. The other two rectifier outputs are provided to generate the qualification level and to feed the single-ended passive differentiator. The threshold setting and differentiation is performed by an external RLC network.

The AD892E/AD892T provides both level and time-domain qualification. Level qualification is performed on half cycles of the rectified data waveform using a user-defined threshold level which is applied to the level qualification comparator. The output of this comparator drives the data input of a master-slave flip-flop. A second, matched comparator detects zero-crossings and clocks the flip-flop. Each valid zero-crossing causes a time-domain filter one-shot to generate a pulse with a user-defined period. During the one-shot period the flip-flop is disabled, preventing the detection of additional zero-crossing events. This technique prevents single-bit errors from being propagated into two-bit errors. The zero-crossing event also triggers an output one-shot, again with a user defined pulse width. For maximum flexibility, the data output is a Schottky open-collector transistor with a separate digital ground to minimize digital feedthrough (AD892T) or differential ECL (AD892E).

The AD892E/AD892T is available in a 44-pin plastic leaded chip carrier (PLCC) and is specified to operate over the commercial (0 to +70°C) temperature range.

SPECIFICATIONS (@ +25°C, +5 V, +12 V dc, unless otherwise noted)

Parameter	Conditions	AD892EJ/AD892TJ Min	Typ	Max	Units
VARIABLE GAIN AMPLIFIER					
Maximum Gain[1]		**28.5**	30	**31.5**	dB
−3 dB Bandwidth	Up to 40 dB Gain Reduction	50			MHz
Input Voltage Noise	0 dB Gain Reduction		7		nV/√Hz
Input Signal Range	Recommended p-p Differential	10		200	mV
Input Resistance	Differential	19.2	24		kΩ
Input Capacitance	Differential		1	5	pF
Output Impedance	Differential @ 1 MHz		25		Ω
Harmonic Distortion	0 dB Gain Reduction		0.15		%
	26 dB Gain Reduction		1.5		%
Output DC Level			6.7		V
Control Range	Set Gain Mode	**36**	40		dB
Control Sensitivity	Set Gain Mode (per 20 mV Input)		−1		dB
Control Linearity	Set Gain Mode (26 dB VGA Range)			**±0.5**	dB
VGA Level Set Input Range	Set Gain Mode (for Specified Accuracy)	**0**		**800**	mV
	Nondestructive Input Range	−0.3		V_{12}	V
VGA Level Set Input Current				−50	μA
INPUT CLAMP[2]					
Turn-On Time			30		ns
Turn-Off Time			200		ns
Input Signal Attenuation			45		dB
On-State Input Impedance	Differential		28		Ω
GAIN OF 4 BUFFER					
Nominal Gain		**12.25**	12.75	**13.25**	dB
±3 dB Bandwidth		50			MHz
Input Voltage Noise[3]			7		nV/√Hz
Input Resistance	Differential	19.2	24		kΩ
Input Capacitance	Differential		1	5	pF
Input Common Mode Range	Relative to Reference Voltage			±1	V
Output Impedance	Differential @ 1 MHz		10		Ω
Harmonic Distortion	300 mV Peak Output, 200 Ω Load		0.20		%
Output Signal Level	Recommended p-p Differential		1.3		V
Output DC Level			5.75		V
FULL WAVE RECTIFIER					
Input Signal Level	p-p Differential	0.3		3	V
−3 dB Bandwidth	100 mV−1 V Peak Input	50			MHz
Input Resistance	Differential	3.2	4		kΩ
Input Capacitance	Differential		1	5	pF
Output Impedance	Differential @ 1 MHz		15		Ω
DC Offset[4]	Relative to Reference Voltage		±10	**±30**	mV
Reference Voltage Output		3.75		4.75	V
Reference Voltage Output Current				1	mA
AGC CONTROL SECTION					
Attack Time	26 dB Gain Step – 1000 pF C_{SAMPLE}		1.0		μs
	26 dB Gain Step – <50 pF C_{SAMPLE}		120		ns
Hold Droop	1 dB Gain Change – 1000 pF C_{SAMPLE}		5		ms
Dynamic Range	AGC Acquire Mode	**36**	40		dB
Control Sensitivity	AGC Acquire Mode (per 10 mV Input)		40		mV
AGC Level Set Input Range	For Specified Accuracy	**200**		**600**	mV
	Nondestructive Input Range	−0.3		V_{CC}	V
AGC Level Set Input Current				−50	μA
MODE CONTROL SECTION (TTL COMPATIBLE)					
V_{IH}		2.0		5.25	V
V_{IL}		−0.3		0.8	V
I_{IH}				10	nA
I_{IL}				10	nA
Mode Switching Times				50	ns

LOGIC ASSIGNMENT	BIT A	BIT B
Input Clamp	0	0
VGA Gain Set	0	1
AGC Hold	1	0
AGC Acquire	1	1

Parameter	Conditions	AD892EJ/AD892TJ Min	Typ	Max	Units
COMPARATORS					
Input Offset Voltage			0.25	**2.0**	mV
Input Offset Current			100		nA
Input Bias Current			0.68		μA
Open Loop Gain	f = 10 MHz		66		dB
Input Resistance	Differential		500		kΩ
Input Capacitance	Differential		1	5	pF
Input Common Mode Range	Referred to Digital Ground	2.8		+ 5	V
OUTPUT/FILTER ONE-SHOT	AD892T				
Resistor Scaling[5]	One-Shot Pulse ≈ $10+3.0\times R_{SET}$				ns
Pulse Duration	$R_{SET} = R_{min}$ to R_{max}	9		180	ns
	R_{SET} = 10 kΩ	**31**	38	**45**	ns
Resistor Range	$R_{SET} = R_{min}$ to R_{max}	0.75		56	kΩ
OUTPUT/FILTER ONE-SHOT	AD892E				
Resistor Scaling[5]	One-Shot Pulse ≈ $3.5+3.5\times R_{SET}$				ns
Pulse Duration	$R_{SET} = R_{min}$ to R_{max}	7		52	ns
	R_{SET} = 3 kΩ	**9**	14	**19**	ns
Resistor Range	$R_{SET} = R_{min}$ to R_{max}	1		14	kΩ
EXTERNAL LOGIC					
Data Output Level (AD892T)	400 Ω Pull-Up to +5 V				
Output Logic "1"	User Defined (Open Collector Output)				
Output Logic "0"			0.25	0.5	V
Data Output Level (AD892E)	1 kΩ Pull-Down to Ground				
Output Logic "1"		4.02	4.15	4.19	V
Output Logic "0"		3.05	3.15	3.37	V
DATA THROUGHPUT					
Propagation Delay[6]	Differentiator Input to Data Output		12.3		ns
Additional Pulse Pairing[7]				1000	ps
Max Transfer Rate (AD892T)		25			Mb/s
Max Transfer Rate (AD892E)		30			Mb/s
POWER SUPPLY REQUIREMENTS					
Supply Voltage V_{12}		10.8	12	13.2	V
Supply Voltage V_5		4.5	5	5.5	V
Quiescent Current I_{12}	T_{min} to T_{max}	40	49	61	mA
Quiescent Current I_5	T_{min} to T_{max}	10	16	24	mA
ABSOLUTE MAXIMUM RATINGS[8]					
Supply Voltage V_{12}				14.5	V
Supply Voltage V_5				7.5	V
RF Input Stage Differential Input Voltage		−0.8		5.6	V
Comparator Differential Input Voltage		−0.8		5.6	V
Storage Temperature Range		−65		130	°C
Operating Temperature Range[9]		0		70	°C
Lead Temperature Range	Soldering 60 Sec			300	°C

NOTES

[1]Gain calibrated in gain set mode with 0 volts applied to the gain set pin.

[2]Clamp operation is specified with a source impedance of 200 Ω in series with 0.1 μF.

[3]Over the full 50 MHz bandwidth of the AD892E/AD892T, the worst-case rms signal-to-noise ratio is 40 dB or better with a 40 dB AGC range.

[4]Measured using a 4 kΩ resistor connected between qualifier threshold pin and ground; also between the differentiator pin and ground.

[5]R_{SET} specified in kΩ.

[6]Propagation delay is measured from the zero crossing comparator input to the "Data Output" with 200 mV overdrive.

[7]Measurements were performed using a ±100 mV square wave having a rise time under 5 ns; this was applied to the input of the zero crossing comparator. The resultant pulse pairing is the difference in delay times for two consecutive output pulses.

[8]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.

[9]44-pin PLCC package: θ_{JA} = +65°C/watt.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

Typical Characteristics (@ +25°C with +5 V, +12 V Supplies)

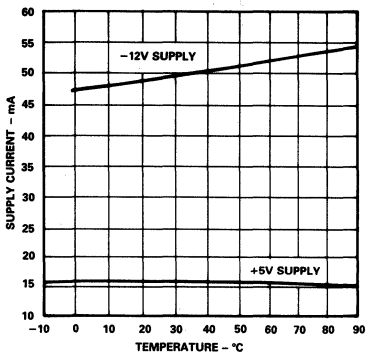


Figure 1. Supply Current vs. Temperature

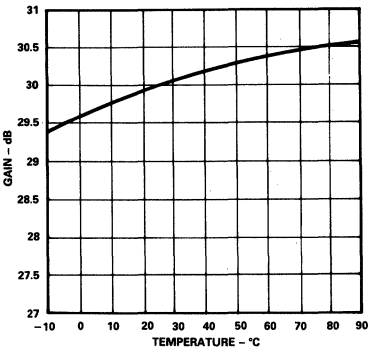


Figure 2. VGA Gain vs. Temperature

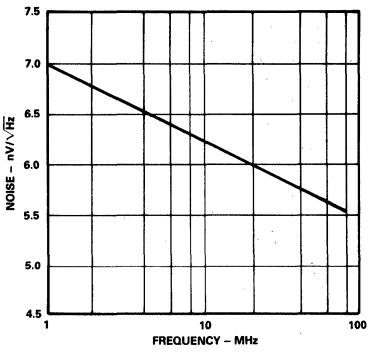


Figure 3. VGA Input Voltage Noise vs. Frequency

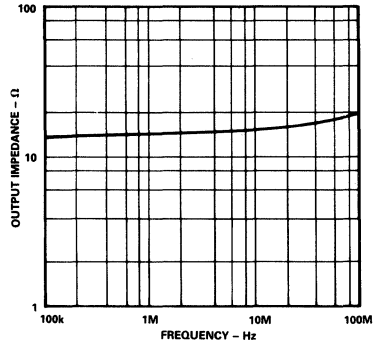


Figure 4. VGA Output Impedance vs. Frequency

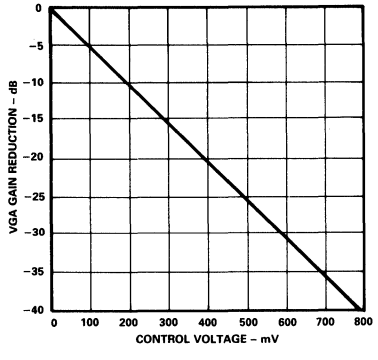


Figure 5. VGA Gain Reduction vs. Control Voltage

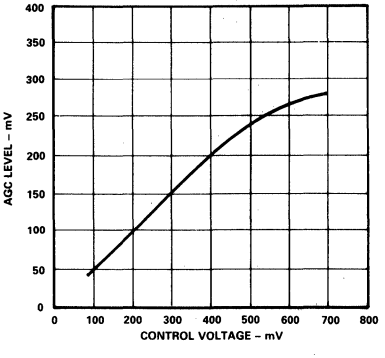


Figure 6. AGC Level vs. Control Voltage

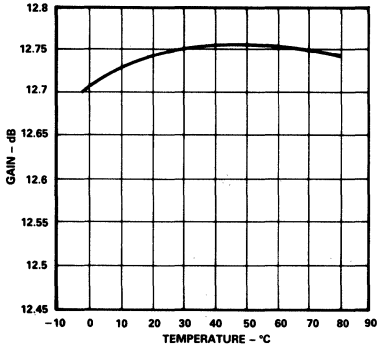


Figure 7. ×4 Buffer Gain vs. Temperature

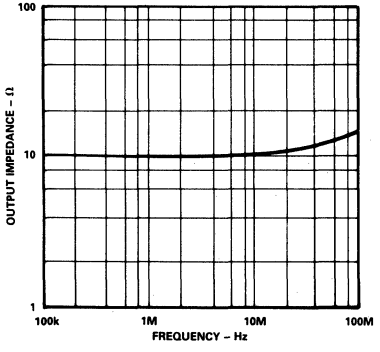


Figure 8. ×4 Buffer Output Impedance vs. Frequency

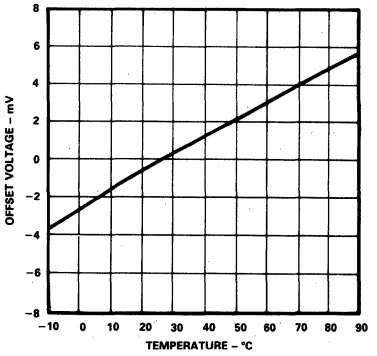


Figure 9. Rectifier Offset vs. Temperature

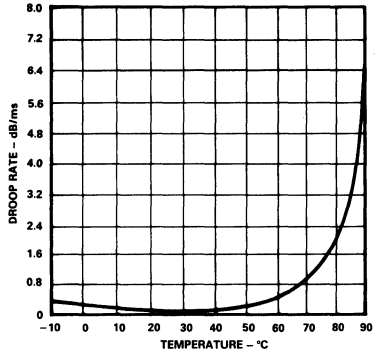


Figure 10. Hold Mode Droop Rate vs. Temperature (C_{HOLD} = 1000pF)

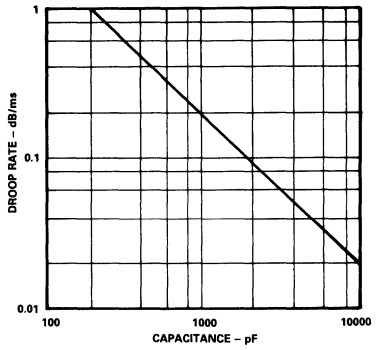


Figure 11. Hold Mode Droop Rate vs. Capacitance

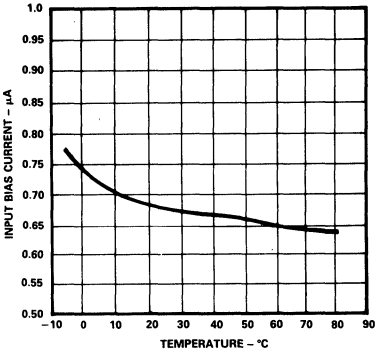


Figure 12. Comparator Input Bias Current vs. Temperature

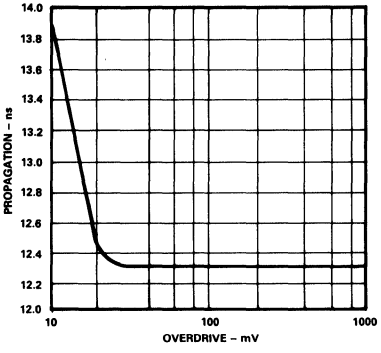


Figure 13. Propagation Delay (Comparator to Data Out) vs. Input Overdrive

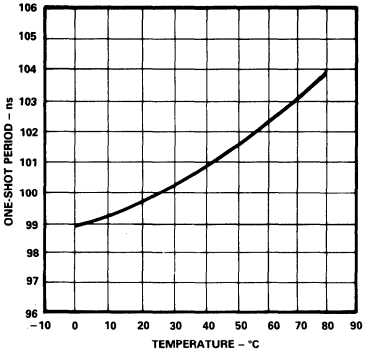


Figure 14. One-Shot Period vs. Temperature (R_{SET} = 30 kΩ)

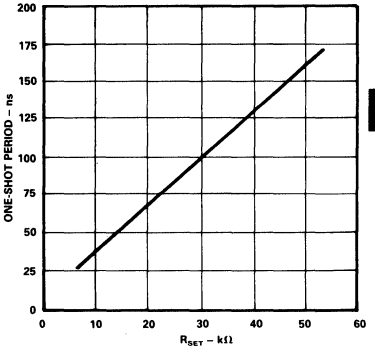


Figure 15. One-Shot Period vs. R_{SET}

CHANNEL PROCESSING STAGES

The VGA Stage

The 30 dB variable gain stage input is biased at a potential of 5.0 V above analog ground. No additional dc bias is required, but ac coupling is necessary. The bias voltage is maintained during normal operation and during operation of the read-after-write recovery clamp.

The VGA differential output stage is an emitter follower with nominal dc biasing of 6.7 V. An internal 1.4 mA current source provides bias current to the output emitter followers. Output drive can be increased by an additional 1.4 mA by paralleling external resistors to the analog ground. However, caution should be exercised in order to avoid causing excess power dissipation for the package. The recommended output level for the VGA is 300 mV p-p differential into 200 Ω loads.

When the AD892E/AD892T is used in the "VGA Set Gain" mode, Control Bit A = 0 (Pin 5) and Bit B = 1 (Pin 4), the VGA gain is programmable through the "VGA Level Set" pin (Pin 11). The VGA gain and exponentiator scale factor are trimmed with respect to the dc control potential applied to the "VGA Level Set" pin. A 0 V potential applied to the "VGA Level Set" pin will produce a nominal VGA gain of 30 dB. Each 20 mV increment of voltage applied will produce a 1 dB reduction in VGA gain. Therefore, a simple equation can be used to calculate the nominal gain of the VGA in this mode:

$$VGA\ Gain\ (dB) = 30 - (50 \times V_{SET\ LEVEL})$$

The AD892E/AD892T offers a read-after-write overdrive protection clamp. The clamp mode, Control Bit A = 0 (Pin 5), Bit B = 0 (Pin 4), lowers the input impedance of the VGA from nominally 24 kΩ to 28 Ω. In order for the clamp to operate correctly with an emitter driven input, a 50 Ω minimum resistor should be placed in series with the input coupling capacitors. The input resistor can be used in conjunction with a shunt capacitor to limit the input bandwidth. For example, a 100 Ω series resistor with a 10 pF shunt capacitor will limit the input bandwidth to 75 MHz. When the VGA input is being driven by an open collector driver with resistive termination, no additional series resistors are required.

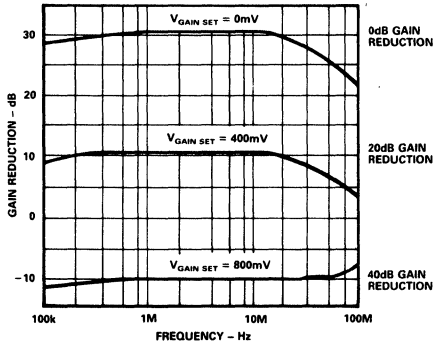


Figure 16. VGA Gain Reduction vs. Frequency

The ×4 Buffers

The inputs of these stages have on chip dc biasing of 4.2 V (the internal reference voltage, V_{REF}); therefore, no input bias current path needs to be provided. The inputs to the buffers should then be ac coupled. When not used, the inputs should be shorted together in order to avoid noise pickup and instability.

The nominal dc output level is 5.75 V with an internal 2.9 mA pull down current source. Output drive can be increased in a similar manner to that described for the VGA stage. Therefore, output current can be increased by up to an additional 2.9 mA by paralleling external resistors to analog ground. As before, precautions to limit excessive overall power dissipation apply when steps are taken to increase the output drive capability.

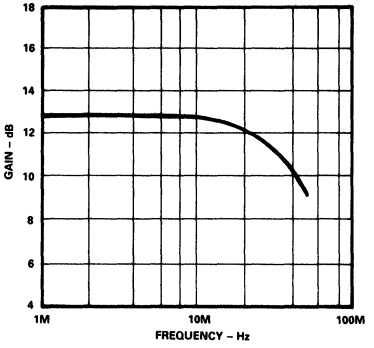


Figure 17. ×4 Buffer Gain vs. Frequency (200 Ω in Series with 1 μF Load)

The Full Wave Rectifiers

The inputs to the three full wave rectifiers are biased at an internal voltage of 5 V; therefore, only ac coupling is recommended. The full wave rectifier outputs consist of three nearly identical stages. All three employ emitter follower outputs. The nominal output voltage with zero input voltage is close to the reference voltage of 4.2 V (Pin 39).

The rectified output to the sample-and-hold amplifier (Pin 34) has an internal 2.15 kΩ resistor in series with one diode tied to ground. This allows for accurate AGC operation in sinusoidal fields; however, if your application requires a peak-hold mode AGC operation, the AD892E/AD892T can be ordered with the resistor removed.

The other two full wave rectifier outputs – one rectified signal to drive the differentiator network and another to derive the threshold for the peak detector – are connected directly to their respective emitter follower output stages. Neither output has a built in pull-down resistor. Therefore, to obtain a zero nominal offset, their quiescent currents must be matched. A 1 mA quiescent current is recommended to ensure accurate operation.

The AGC Sample and Hold

When the AD892E/AD892T is used in the "AGC Acquire" mode, Control Bit A = 1 (Pin 5) and Bit B = 1 (Pin 4), the AGC level is programmable through the "AGC Level Set" pin (Pin 8). The AGC Level is defined as the AVERAGE of the full wave rectifier output voltage (Pin 34). A 400 mV dc potential applied to the "AGC Level Set" pin will produce a nominal average AGC level of 200 mV. Each 10 mV increment/decrement of the applied "AGC level set" voltage will produce a 5 mV increase/decrease in the average AGC level. Therefore, a simple equation can be used to calculate the nominal AGC level in this mode:

$$AGC\ Level = 0.5 \times V_{AGC\ LEVEL\ SET}$$

Without a peak hold capacitor at the full wave rectifier output for the sample-and-hold amplifier (Pin 34), accurate AGC operation only occurs with sinusoidal input signals. If your application requires the AGC operation to use a peak hold scheme, the AD892E/AD892T can be ordered with the pull down resistor removed on the rectified signal output to the sample-and-hold amplifier (Pin 34). The removal of this resistor now allows the user to program the degree of peak hold, by applying a RC combination to the rectified signal output for the sample-and-hold amplifier. The addition of the capacitor alters the symmetry of the attack and decay rates of the rectifier, which is otherwise symmetric in operation. In order to ensure that the overall AGC response is the same for both high to low and low to high input level steps, it is necessary to make the rectifier attack and decay times at least a factor of two less than the AGC response time.

The AGC acquire time is approximately 1 μs per 1000 pF of hold capacitor applied at Pin 22. A low leakage variety of hold capacitor, such as a silver mica, is necessary to ensure a low droop rate. The "VGA Level Set" pin should be tied to analog ground if not used.

The AGC control potential is present at the "sample-and-hold capacitor" pin. If control over open loop gain is desired, based on AGC control potentials measured during trial AGC operations, a FET input op amp should be used to buffer this node in order to avoid disturbing the hold operation.

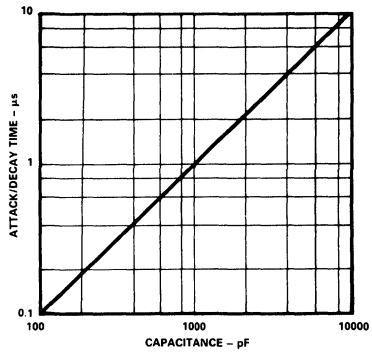


Figure 18. AGC Attack/Decay vs. Capacitance

DATA QUALIFIER STAGES

The data qualifier section of the AD892E/AD892T consists of two comparators, one D-type flip-flop, an internal bandgap reference and a pair of externally adjustable one-shots. One comparator is used to provide data amplitude qualification, while the other acts as a zero-crossing detector when used with an external passive differentiator circuit.

Figure 19 illustrates the operation of the data qualifier using the recommended passive delay line differentiator described in the Application section. Sequence "A" represents the pattern written on the disk where a Logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the data qualifier consists of a sequence of rectified pulses "B." The data pattern shown is worst case for a RLL 1, 7 code input. "C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in state of this output are used to clock the internal D-type flip-flop. The flip-flop is enabled using the output "E" from the amplitude-threshold comparator. The amplitude-comparator output changes state only when the analog input exceeds the programmed threshold level. When the threshold level is exceeded and a zero-crossing event occurs, the flip-flop changes state, producing an output pulse "F." The duration of this pulse, seen at the "Data Output" pin (Pin 43), is set using an external resistor (applied between Pin 42 and V_S), as is the internal time-out (a resistor applied between Pin 41 and V_S) which is used to prevent noise induced retriggering. The final output data sequence is shown in "G". As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a time-shifted version of the write data.

Since the RLL 1, 7 code input is the most demanding of the popular encoding schemes to qualify, the AD892E/AD892T easily handles such other codes as MFM and RLL 2, 7.

GENERAL LAYOUT REQUIREMENTS

The channel processing section of the AD892E/AD892T has almost 60 dB of total gain available at 50 MHz. Good RF layout must be used in the circuit board to avoid oscillations in the 150 MHz to 350 MHz region. A single pole RC filter applied at the input of each stage, with a cut-off in the region of 75 MHz to 125 MHz, will help avoid oscillation problems. As a general rule, keep the connections to interstage components as short as possible; it is also recommended that any low pass filtering that may be required by the system be performed between the VGA stage and the first ×4 buffer amplifier. A ground plane should be used to surround any interstage components wherever possible. If these simple rules are followed, stable operation should be assured.

A parallel combination of 0.1 μF and 0.01 μF ceramic capacitors should be used as close to the supply pins as possible, for both the +12 V analog (Pin 18), +12 V digital (Pin 40) and +5 V (Pin 1) supplies. It is also recommended that the $V_{REFERENCE}$ (Pin 39) is decoupled with a 0.1 μF ceramic capacitor.

Extensive use of a ground plane is recommended. An analog ground (Pin 28) is supplied for the AGC section, while two digital grounds are supplied: one for the data qualifier section (Pin 6), and one for the emitter of the open collector output transistor (Pin 44 for the AD892T only). The digital ground should be connected to the analog ground as near to the power supply common as possible to minimize noise injection to the analog ground.

The filter and output pulse setting resistors should be tied, as directly possible, to the +5 V supply. To prevent the data output pulse from coupling into the output pulse setting circuit, a 1000 pF capacitor can be used in parallel with the output pulse setting resistor.

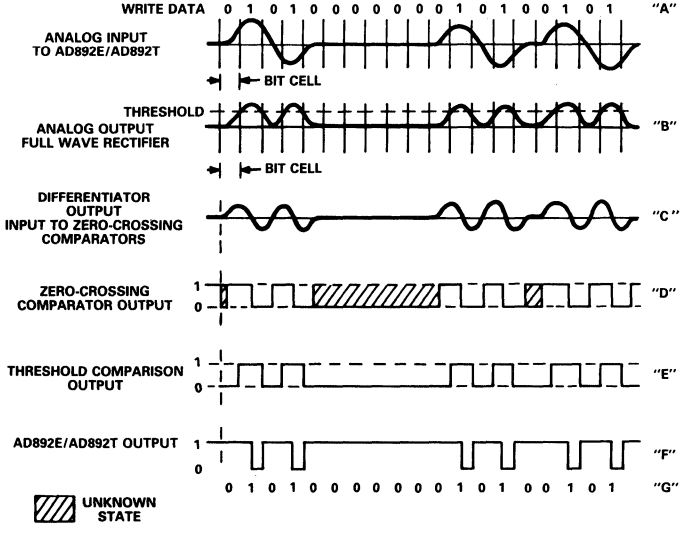


Figure 19. AD892E/AD892T Operation for Worst Case 1–7 RLL

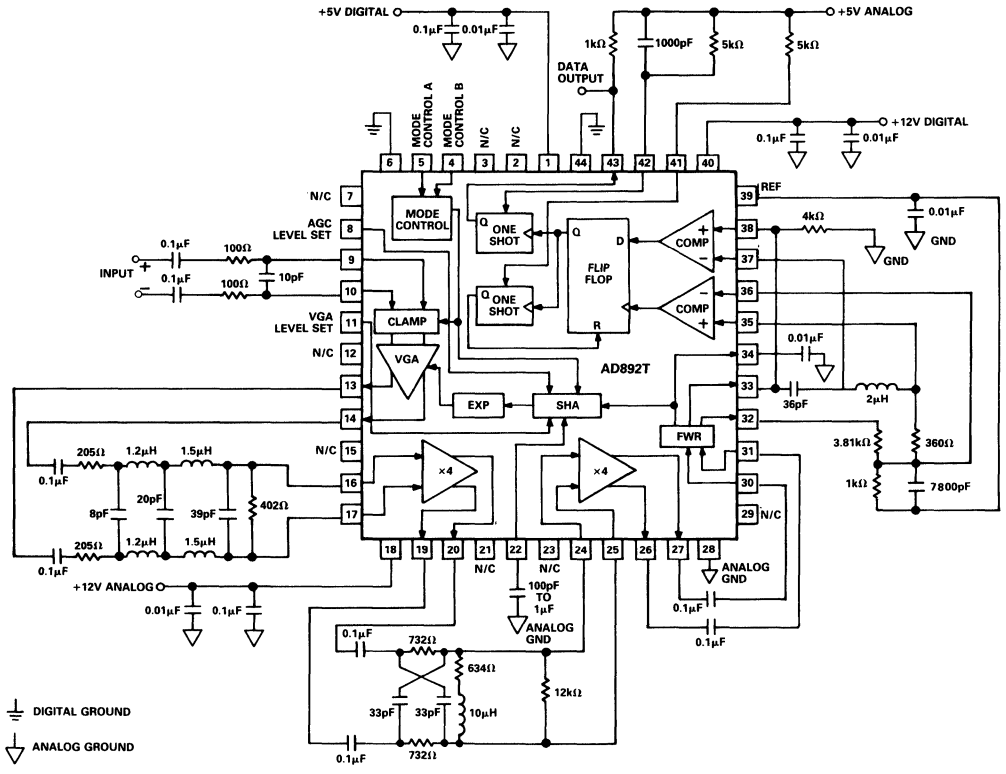


Figure 20. Typical AD892T Connection for a 15 MHz Channel

A 15 MHz APPLICATION

Figure 20 shows a typical application using the AD892T in a 15 MHz channel. This circuit includes a 5-pole 15 MHz Gaussian-to-6 dB transitional filter plus a second-order RLC time domain equalizer. A single ended passive delay-line differentiator is also included.

Using Equalizers with the AD892E/AD892T

The AD892E/AD892T is ideal for applications where equalization is employed. The ×4 buffer output drivers are designed to operate into 200 Ω loads, making tapped delay-line designs easy. Sum and differencing of different tap weights can be achieved by simple resistive dividers.

The RLC Equalizer

As an alternative, a simple RLC network can be implemented to provide a low cost, fully differential alternative to the three tap, tapped delay-line equalizer which often is used for pulse slimming. The equalizer shown in Figure 21 approximates a function in the form of $F(\omega\tau) = 1 - k\cos(\omega\tau)$. The approximation

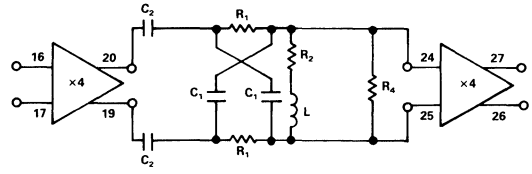


Figure 21. RLC Equalizer

is achieved by first creating a magnitude function and then adding phase compensation to provide a flat group delay characteristic over the frequency range of interest. Our 15 MHz application example employs the cosine equalizer; where K = 0.6 and τ = 24 ns. The magnitude and group delay characteristics of the equalizer employed in the 15 MHz application are shown in Figures 22 and 23, respectively.

Magnitude Approximation

The magnitude approximation is achieved by an RC lattice (Figure 24).

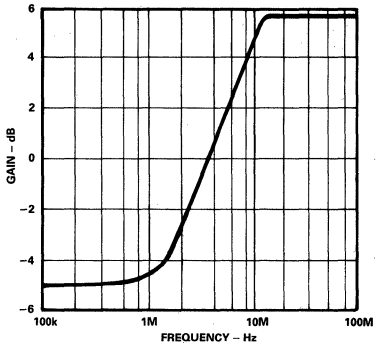


Figure 22. RLC Equalizer Magnitude Response

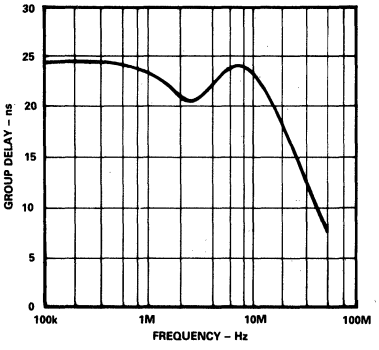


Figure 23. RLC Equalizer Group Delay Response

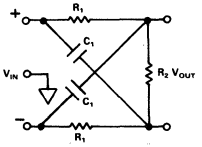


Figure 24. RC Lattice

The transfer function is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2(1-CR_1S)}{CR_1R_2S+R_2+2R_1}$$

at dc

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2}{2R_1+R_2}$$

and at high frequency

$$\frac{V_{OUT}}{V_{IN}} = -1$$

In the above case we can see that K in the $1-K\cos(\omega\tau)$ expression is given by:

$$K = \frac{R_1}{R_1+R_2}$$

and the average gain is then equal to:

$$\frac{R_1+R_2}{2R_1+R_2}$$

From these results we can see that K can be changed by altering either R_1 or R_2. However, doing so will change the frequency response of the network. Normal rules of impedance scaling should be followed when changing the value of either R_1 or R_2.

Group Delay Approximation

An inductor can now be added to give a suitable group delay response. We now have the RLC lattice depicted in Figure 25.

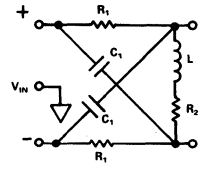


Figure 25. RLC Lattice

The complete derivation for the response of this equalizer is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot\frac{1}{SC}}{\frac{R_2}{2}+\frac{SL}{2}+\frac{1}{SC}}}{R_1+\dfrac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot\frac{1}{SC}}{\frac{R_2}{2}+\frac{SL}{2}+\frac{1}{SC}}} - \frac{\dfrac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot R_1}{\frac{R_2}{2}+\frac{SL}{2}+R_1}}{\frac{1}{SC}+\dfrac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot R_1}{\frac{R_2}{2}+\frac{SL}{2}+R_1}}$$

$$= \frac{\left[\frac{R_2}{2}+\frac{SL}{2}\right]\cdot\left[\frac{1}{SC}-R_1\right]}{\frac{R_1R_2}{2}+\frac{SLR_1}{2}+\frac{R_1}{SC}+\frac{R_2}{2SC}+\frac{SL}{2SC}}$$

$$= -\left[\frac{S^2R_1LC-S[L-CR_1R_2]-R_2}{S^2R_1LC+S[L+CR_1R_2]+2R_1+R_2}\right]$$

$$\text{ALL PASS NETWORK} \rightarrow = -\left[\frac{S^2R_1LC-S[L+CR_1R_2]+2R_1+R_2}{S^2R_1LC+S[L+CR_1R_2]+2R_1+R_2}\right] +$$

$$\text{MAGNITUDE TERM} \rightarrow \left[\frac{2[R_1+R_2+SCR_1R_2]}{S^2R_1LC+S[L+CR_1R_2]+2R_1+R_2}\right]$$

There is no "best" solution to the group delay question. The choice of inductor value in the 15 MHz application example was based on SPICE simulation of the transfer function. However, if K remains the same as in the example, then altering τ becomes a simple frequency scaling of the network.

If R_1 and R_2 remain unchanged

$$\textit{and if } \tau \rightarrow \tau'$$

$$\textit{then } C \rightarrow \frac{\tau' C}{\tau} \textit{ and } L \rightarrow \frac{\tau L}{\tau'}$$

Any deviation from the K value given in the example will require the value of L to be recalculated.

CHOICE OF LOW PASS FILTER WITH THE RECOMMENDED EQUALIZER

A fifth order, Gaussian-to −6 dB transitional filter is recommended for use with the equalizer. This type of low pass filter, shown in Figure 26, is also used in the 15 MHz application example. Low group delay ripple and high out-of-band rejection make this design work well with the recommended equalizer and differentiator networks. The recommended location for the low pass filter is between the VGA and the first ×4 buffer. The equalizer is then placed between the first and second ×4 buffers. This minimizes the potential for oscillations induced by interstage feedback.

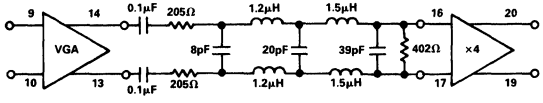


Figure 26. 5th Order Guassian to 6 dB Transitional Filter

The magnitude and group delay characteristics of this filter are shown in Figures 27 and 28, respectively.

THE SINGLE ENDED PASSIVE DELAY-LINE DIFFERENTIATOR

The recommended configuration of the passive delay-line differentiator is shown in Figure 29. Again, this configuration is employed in the 15 MHz application example.

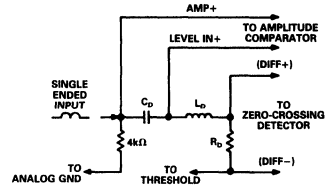


Figure 29. Single Ended Configuration of Passive Delay Line Differentiator

RECOMMENDED COMPONENTS

$$f_D = \frac{1}{2\pi\sqrt{L_D C_D}}$$

f_D = 1.5 Times the Maximum Desired Differentiated Frequency

$$R_D = K\left[\sqrt{\frac{L_D}{C_D}}\right]$$

R_D Minimum Value: 120 Ω
150 Ω or Greater is Recommended

$$1.3 \leq K \leq 1.7$$

(Best Magnitude Response) (Best Group Delay Response)

Figures 30 through 33 show the typical performance to be expected from the recommended passive delay-line differentiator. The choice of components used to obtain these characteristics are the ones used in the 15 MHz application example.

9

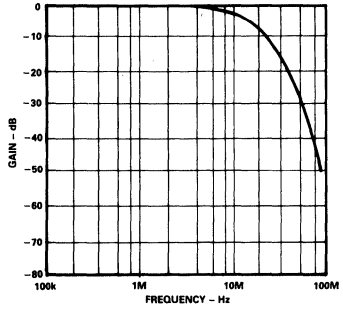


Figure 27. Gaussian Low Pass Filter Magnitude Response

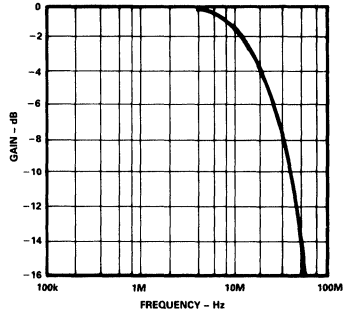


Figure 30. Magnitude Response of Undifferentiated Output

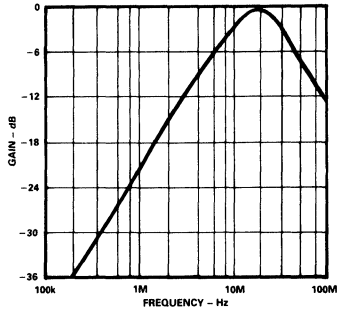


Figure 32. Magnitude Response of Differentiated Output

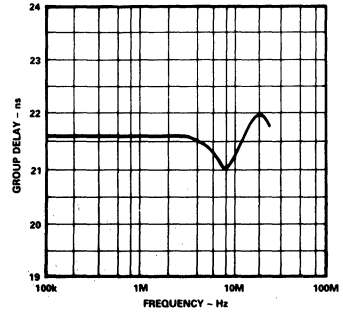


Figure 28. Gaussian Low Pass Filter Group Delay Response

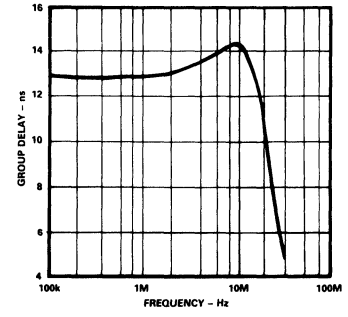


Figure 31. Group Delay Characteristics of Undifferentiated Output

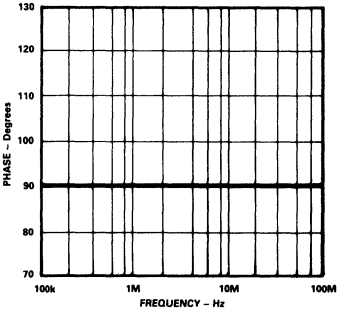
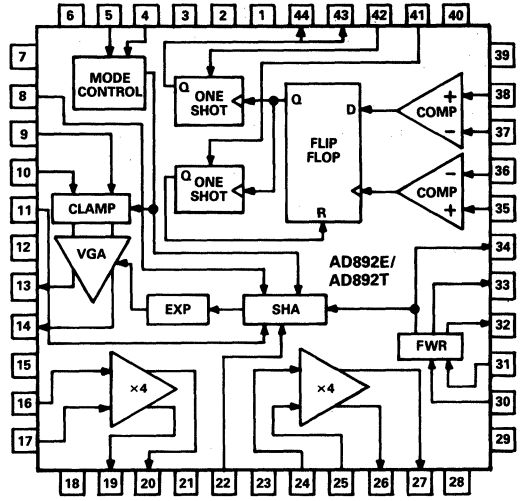


Figure 33. Relative Phase Between Differentiated and Undifferentiated Output

PIN ASSIGNMENTS

Pin	Description
1	+5 V Supply
2	No Connection (Can Be Left Floating)
3	No Connection (Can Be Left Floating)
4	Mode Control Bit B (TTL Compatible)
5	Mode Control Bit A (TTL Compatible)
6	Digital Ground
7	No Connection (Can Be Left Floating)
8	"AGC Level Set" Input Voltage
9	Variable Gain Amplifier Input (+)
10	Variable Gain Amplifier Input (−)
11	"VGA Level Set" Input Voltage
12	No Connection (Can Be Left Floating)
13	Variable Gain Amplifier Output (−)
14	Variable Gain Amplifier Output (+)
15	No Connection (Can Be Left Floating)
16	#1 12.75 dB Buffer Input (−)
17	#1 12.75 dB Buffer Input (+)
18	+12 V Supply (Analog)
19	#1 12.75 dB Buffer Output (+)
20	#1 12.75 dB Buffer Output (−)
21	No Connection (Can Be Left Floating)
22	Sample-and-Hold Capacitor
23	No Connection (Can Be Left Floating)
24	#2 12.75 dB Buffer Input (−)
25	#2 12.75 dB Buffer Input (+)
26	#2 12.75 dB Buffer Output (+)
27	#2 12.75 dB Buffer Output (−)
28	Analog Ground
29	No Connection (Can Be Left Floating)
30	Full Wave Rectifier Input (+)
31	Full Wave Rectifier Input (−)
32	Rectified Signal to Derive Threshold
33	Rectified Signal for Differentiator
34	Rectified Signal to S/H; AGC Attack and Decay Is Programmed at This Point
35	Zero Crossing Comparator Input (+)
36	Zero Crossing Comparator Input (−)
37	Minimum Threshold Level Input
38	Signal Amplitude Comparator Input
39	Internal Voltage Reference
40	+12 V Supply (Digital)
41	Apply Resistor to Program Time Domain Filter Pulse Width
42	Apply Resistor to Program Output Pulse Width
43	Data Output (Open Collector AD892T) Data Output (+ ECL AD892E)
44	Data Output Ground (Emitter of Output Device AD892T) Data Output (− ECL AD892E)



ORDERING GUIDE

Model No.	Package Options*
AD892EJP	44-Pin PLCC (P-44A)
AD892TJP	44-Pin PLCC (P-44A)

*See Section 20 for package outline information.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

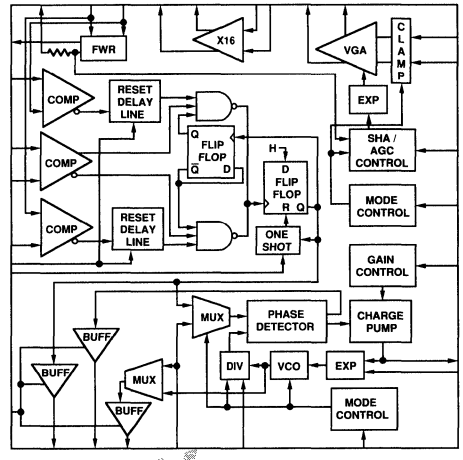
40 Mb/s Fully Integrated Disk Drive Read Channel

AD897

FEATURES

- **40 Mb/s Data Transfer Rate Capability**
- **500 ps (max) Additional Pulse Pairing**
- **30 dB Gain VGA with 40 dB Control Range**
- **24 dB Buffer with 200 Ω Differential Load Drive Capabilities**
- **0.1 dB/ms Typical Gain Drift in Hold Mode**
- **Symmetrical and User Programmable AGC Attack/ Decay Times**
- **Three Levels of Data Qualification**
  - **Amplitude Threshold**
  - **Time Above Threshold**
  - **Data Polarity**
- **Offset Trimmed Zero Crossing Comparator**
- **±1 ns (max) PLL Window Uncertainty**
- **Zero Phase Error VCO Start-Up**
- **No Phase Detector Dead Band at Center of Decode Window**
- **Exponential VCO Control**
- **52-Pin PQFP Package, +5 V and +12 V Supplies**

AD897 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD897 is a complete solution for recovering binary information in a hard disk drive with data transfer rates up to 40 megabits per second. It is connected to the output of the head amplifier and performs the signal conditioning, data qualification and data synchronization tasks with a minimum of external components.

The AD897 has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Fast acquisition and low droop while in the hold mode allow for the AGC operation to be performed within the sector header without compromising channel behavior when reading data.

Three levels of data qualification are provided: amplitude threshold, time above amplitude threshold, and data polarity. Level qualification is performed on positive and negative cycles of the data waveform using a user-defined threshold level which is applied to the level qualification comparators. Each comparator then drives a resettable delay line, which implements the time above threshold qualification. Once the first two valid criteria have been satisfied, a third comparator is able to detect a zero crossings and clock a flip-flop if the data also exhibits the correct polarity. Each clocking of the flip-flop causes a second flip-flop to toggle and thereby implement the polarity check. The valid data event also triggers an output one-shot, with a user-defined pulse width.

The data synchronizer section provides four modes of operation: lock to external clock, lock to preamble, lock to data, and tristate. The phase detector/charge pump utilizes a tri-phase pump-up, pump-down, pump-up approach in the lock to data mode, thereby ensuring no dead band zone in the center of the window. In addition, when switching to the lock to data mode, zero-phase error start-up is initiated. In the lock to external clock mode, feedback dividers provide the capability to achieve VCO to external clock ratios of 1:2, 1:1, 3:2, 2:1. When switching PLL operating modes, the charge pump is temporarily tristated to prevent the VCO control voltage from being disturbed.

The AD897 is available in a 52-pin plastic flat pack package (PQFP) and is specified to operate over the commercial (0 to +70°C) temperature range.

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SPECIFICATIONS

PEAK DETECTOR SECTION (@ +25°C, +5 V, +12 V dc, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
VARIABLE GAIN AMPLIFIER					
Maximum Gain[1]		**29**	30	**31**	dB
Gain Variation	T_{min} to T_{max}	−0.3		0.7	dB
±3 dB Bandwidth	Up to 40 dB Gain Reduction	40	60		MHz
Input Voltage Noise	0 dB Gain Reduction		6		nV/√Hz
Input Signal Range	p–p Differential	10		200	mV
Input Resistance	Differential	20	24		kΩ
Input Capacitance	Differential		1	5	pF
Output Impedance	Differential, f = 1 MHz		10	20	Ω
Harmonic Distortion	40 dB Gain, 10 mV p–p Differential Input			0.25	%
	14 dB Gain, 200 mV p–p Differential Input			2	%
Output DC Level			6.7		V
Control Range	Set Gain Mode	**36**	40		dB
Control Sensitivity	Set Gain Mode (Per 20 mV Input)		−1		dB
Control Linearity	Set Gain Mode (26 dB VGA Range)			**±0.5**	dB
VGA Level Set Input Range	Set Gain Mode (For Specified Accuracy)	**0**		**800**	mV
	Nondestructive Input Range	−0.3		V_{12}	V
VGA Level Set Input Current				−50	μA
INPUT CLAMP[2]					
Turn-On Time				100	ns
Turn-Off Time				100	ns
Input Signal Attenuation	200 Ω Source Resistance		34		dB
On-State Input Impedance	Differential		40		Ω
GAIN OF 16 BUFFER					
Gain	f = 1 MHz	**23.5**	24	**24.5**	dB
Gain Variation	T_{min} to T_{max}	−0.5		0.5	dB
±3 dB Bandwidth		60			MHz
Input Voltage Noise			8		nV/√Hz
Input Resistance	Differential	20	24		kΩ
Input Capacitance	Differential		1	5	pF
Input Common-Mode Range			TBD		V
Output Impedance	Differential, f = 1 MHz		10	20	Ω
Harmonic Distortion	1 V p–p Differential Output, 200 Ω Load			0.5	%
Output Signal Level	p–p Differential			4	V
Output DC Level			5.75		V
FULL WAVE RECTIFIER					
Input Signal Level	p–p Differential			4	V
−3 dB Bandwidth		70			MHz
Input Resistance	Differential	8	10		kΩ
Input Capacitance	Differential		1	5	pF
DC Offset[3]	Relative to the Reference Voltage			**±30**	mV
Output Impedance			10	20	Ω
Peak Detector V_{REF}		4.2		5.0	V
AGC CONTROL SECTION					
Attack Time (Slow)	AGC Acquire Gain = "0"				
	26 dB Gain Step – 1000 pF C_{SAMPLE}		10		μs
	26 dB Gain S – <50 pF C_{SAMPLE}		1.2		μs
Attack Time (Fast)	AGC Acquire Gain = "1"				
	26 dB Gain Step – 1000 pF C_{SAMPLE}		1.0		μs
	26 dB Gain Step – <50 pF C_{SAMPLE}		120		ns
Hold–Droop	1 dB Gain Change – 1000 pF C_{SAMPLE}		10		ms
Dynamic Range	AGC Acquire Mode		TBD		dB
AGC Level Range	AGC Acquire Mode (@ S/H Rectifier)	0.5		2.0	V
Control Sensitivity	AGC Acquire Mode (Per 10 mV Input)		5		mV
AGC Level Set Input Range	For Specified Accuracy	**200**		**600**	mV
	Nondestructive Input Range	−0.3		V_{CC}	V
AGC Level Set Input Current				−50	μA

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Parameter	Conditions	Min	Typ	Max	Units
COMPARATORS					
Input Offset Voltage			1	2.0	mV
Input Offset Current			TBD		pA
Input Bias Current			200	1000	pA
Open-Loop Gain	f = 10 MHz		TBD		dB
Input Resistance	Differential		100		kΩ
Input Capacitance	Differential		1	5	pF
Input Common-Mode Range	Referred to Digital Ground		TBD		V
RESETTABLE DELAY LINE					
Resistor Scaling[4]			Delay ≈ 2+7.5 × R_{SET}		ns
Pulse Duration	R_{SET} = 1 kΩ		TBD		ns
	R_{SET} = 5 kΩ		TBD		ns
Resistor Range	R_{SET} = R_{min} to R_{max}		TBD		kΩ
OUTPUT ONE SHOT					
Resistor Scaling			One Shot Pulse ≈ 6+4.5 × R_{SET}		ns
Pulse Duration	R_{SET} = R_{min} to R_{max}		TBD		ns
	R_{SET} = 30 kΩ		TBD		ns
	R_{SET} = 10 kΩ		TBD		ns
Resistor Range	R_{SET} = R_{min} to R_{max}		TBD		kΩ
DATA THROUGHPUT					
Additional Pulse Pairing[5]			100	500	ps
Max Transfer Rate		40			Mb/s

NOTES

[1]Over the full 60 MHz bandwidth of the AD897, the worst case rms signal-to-noise ratio is 40 dB or better with a 40 dB AGC range.

[2]Clamp Operation is specified with a source impedance of 200 Ω in series with 0.1 μF.

[3]Measured using a 4 kΩ resistor connected between rectified signal to derive threshold pin (Pin 15) and Ground.

[4]R_{SET} specified in kΩ.

[5]Measurements were performed using a 100 mV sine wave applied to the input of the VGA. The resultant pulse pairing is the difference in delay times for two consecutive output pulses at the raw data output.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

AGC MODE CONTROL

Control Line	AGC Mode Control 0	AGC Mode Control 1	AGC Acquire Gain
AGC Acquire with Slow Attack	0	0	0
AGC Acquire with Fast Attack	0	0	1
AGC Hold	0	1	X
VGA Gain Set	1	0	X
Input Clamp	1	1	X

X = Do not care.

SPECIFICATIONS

PLL SECTION (@ + 25°C, +5 V, +12 V dc, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
PHASE DETECTOR					
Phase Detector Range			$\pm\pi$		Radians
Gain	Data Updates n Clock Cycles Apart		$1/n2\pi$		1/Radians
CHARGE PUMP					
Gain	Minimum Gain Mode	80	100	120	μA
	Nominal Gain Mode	160	200	240	μA
	Maximum Gain Mode	320	400	480	μA
VCO/EXPONENTIATOR					
Frequency		10		60	MHz
Range	Fixed Frequency		4:1		
Gain		1.10ω	1.40ω	1.65ω	(Rad/s)/V
WINDOW STROBE					
Range			$\pm T_W/2$		Seconds
Sensitivity	Per 10 mV Input on Window Strobe Control				
Control Line Input Range	Relative to Analog V_S	−1		1	V
Control Line Input Current				50	μA
WINDOW LOSS					
Jitter (6σ)	Lock to Data Mode with Minimum Gain		1	1.5	ns
Window Center Offset	Lock to Data with Nominal Gain			1% ±1 ns	% of T_W
Zero Phase Start-Up					
Accuracy	Lock to External CLK or Data Mode		1	1.5	ns
Static Window Loss	Lock to Data Mode with Minimum Gain				% of T_W
DATA THROUGHPUT					
Max Data Transfer Rate	RLL 1, 7 Encoding	40			Mb/s
Max External Clock Frequency		60			MHz
External Clock to Synchronized					
Clock Delay	Lock to External Clock		4	6	ns

Specifications subject to change without notice.

PLL LOCK MODE CONTROL

Control Line	PLL Lock Mode Control 0	PLL Lock Mode Control 1	PLL Acquire Gain
Lock to External Clock (Charge Pump – 1/2 Nominal)	0	0	0
Lock to External Clock (Charge Pump – Nominal)	0	0	1
Lock to Preamble (Charge Pump – Nominal)	0	1	0
Lock to Preamble (Charge Pump – 2× Nominal)	0	1	1
Tristate	1	0	X
Lock to Data (Charge Pump – 1/2 Nominal)	1	1	0
Lock to Data (Charge Pump – Nominal)	1	1	1

X = Do not care.

VCO DIVIDER CONTROL

Control Line	Division Factor Bit 0	Division Factor Bit 1
Division Factor = 1	0	0
Division Factor = 2	0	1
Division Factor = 3	1	0
Division Factor = 4	1	1

MODE CONTROL AND OUTPUT PINS

Parameter	Conditions	Min	Typ	Max	Units
MODE CONTROL PINS	TTL Compatible CMOS Inputs				
V_{IH}		2.0		V_5+0.5	V
V_{IL}		V_{GND} −0.5		0.8	V
I_{IH}				1	nA
I_{IL}				1	nA
Mode Switching Times				50	ns
OUTPUT PINS	CMOS Compatible				
V_{OH}		4.0		V_5+0.5	V
V_{OL}		V_{GND} −0.5		1.0	V
I_{OH}		4			mA
I_{OL}		4			mA

Specifications subject to change without notice.

POWER SUPPLIES (@ +25°C, +5 V, +12 V dc, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{12}		10.8	12	13.2	V
Supply Voltage V_5		4.5	5	5.5	V
Quiescent Current I_{12}	T_{min} to T_{max}		40	50	mA
Quiescent Current I_5	T_{min} to T_{max}		60	72	mA

Specifications subject to change without notice.

9

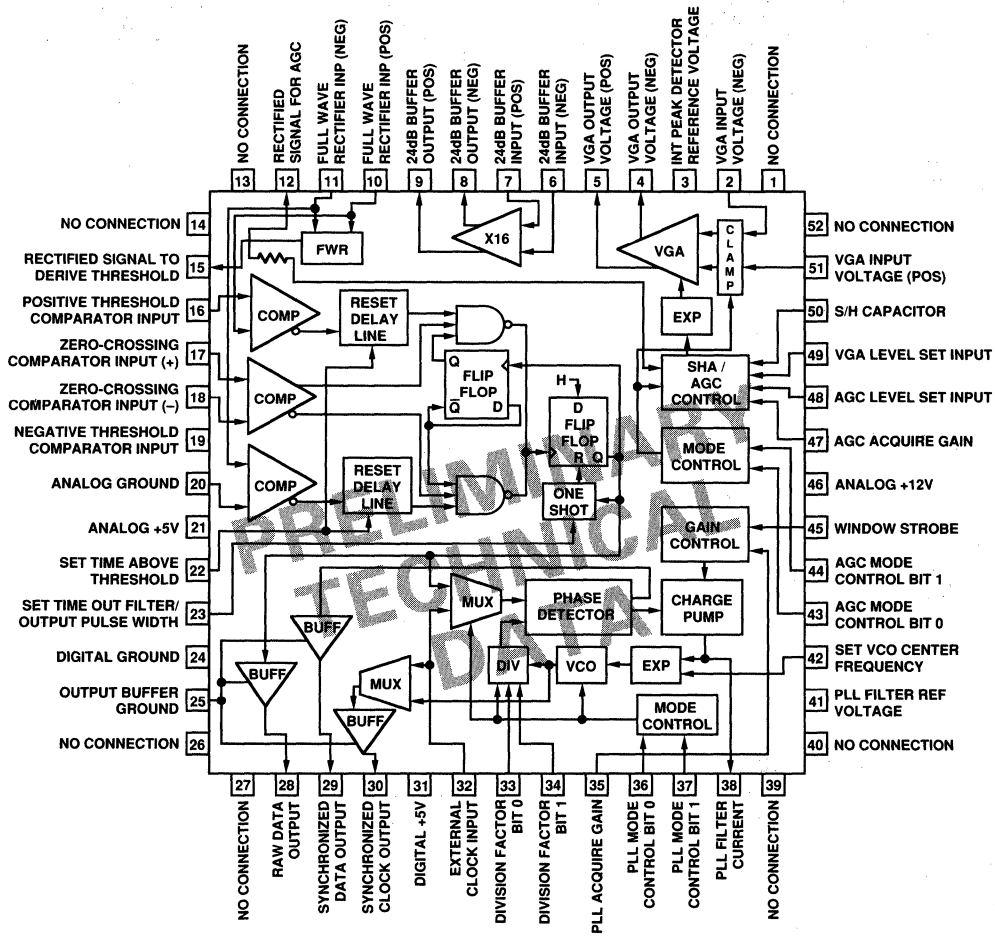
ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{12}				14.5	V
Supply Voltage V_5				7.5	V
RF Input Stage Differential Input Voltage		−0.8		5.6	V
Comparator Differential Input Voltage		−0.8		5.6	V
Storage Temperature Range		−65		130	°C
Operating Temperature Range[2]		0		+70	°C
Lead Temperature Range	Soldering 60 sec			+300	°C

Notes
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.
[2]52-pin PQFP package: θ_{JA} = 65°C/watt.

CONNECTION DIAGRAM

52-Pin PQFP



ORDERING GUIDE

Model	Description	Package Option*
AD897JS	52-Pin PQFP	S-52

*See Section 20 for package outline information.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Pin	Description	I/O Type	Application Notes
1	No Connection		May be left floating.
2	VGA Input Voltage (Neg)	Analog Voltage Input	
3	Internal Peak Detector Reference Voltage	Analog Voltage Output	+4.3 V reference is used to bias the full wave rectifier.
4	VGA Output Voltage (Neg)	Analog Voltage Output	Emitter follower output, biased at 6.5 V.
5	VGA Output Voltage (Pos)	Analog Voltage Output	Emitter follower output, biased at 6.5 V.
6	24 dB Buffer Output (Neg)	Analog Input Voltage	Internally based at 5 V.
7	24 dB Buffer Input (Pos)	Analog Voltage Input	Internally biased at 5 V.
8	24 dB Buffer Output (Neg)	Analog Voltage Output	Emitter follower output, biased at 6.5 V.
9	24 dB Buffer Output (Pos)	Analog Voltage Output	Emitter follower output, biased at 6.5 V.
10	Full Wave Rectifier Input (Pos)	Analog Voltage Input	Internally biased at 5 V.
11	Full Wave Rectifier Input (Neg)	Analog Voltage Input	Internally biased at 5 V.
12	Rectified Signal to AGC	Analog Voltage Output	Emitter follower output with 250 Ω in series. No internal pull-down is provided.
13	No Connection		May be left floating.
14	No Connection		May be left floating.
15	Rectified Signal to Derive Threshold	Analog Voltage Output	Emitter follower output. No internal pull-down is provided.
16	Positive Threshold Comparator Input	Analog Voltage Input	Threshold for positive amplitude comp.
17	Zero-Crossing Comparator Input (Pos)	Analog Voltage Input	DC biased through passive differentiator network.
18	Zero-Crossing Comparator Input (Neg)	Analog Voltage Input	DC biased through passive differentiator network.
19	Negative Threshold Comparator Input	Analog Voltage Input	Threshold for positive amplitude comp.
20	Analog Ground	Power Input	
21	Analog +5 V	Power Input	Decoupling with 0.1 μF||0.01 μF required.
22	Set Time Above Threshold	Analog Current Input	Resistor/current programmable.
23	Set Time Out Filter/Output Pulse Width	Analog Current Input	Resistor/current programmable.
24	Digital Ground	Power Input	
25	Output Buffer Ground	Power Input	
26	No Connection		May be left floating.
27	No Connection		May be left floating.
28	Raw Data Output	Digital CMOS Output	Active high represents data pulse.
29	Synchronized Data Output	Digital CMOS Output	Active high data output pulse lasting one clock period. Synchronized to rising edge of synchronized clock.
30	Synchronized Clock Output	Digital CMOS Output	
31	Digital +5 V	Power Input	Decoupling with 0.1 μF||0.01 μF required.
32	External Clock Input	TTL Input	Source clock divided by 2 internally.
33	Division Factor Bit 0	TTL Input	Sets division factor of VCO.
34	Division Factor Bit 1	TTL Input	Sets division factor of VCO.
35	PLL Acquire Gain	TTL Input	Active high doubles charge pump gain.
36	PLL Lock Mode Control Bit 0	TTL Input	
37	PLL Lock Mode Control Bit 1	TTL Input	
38	PLL Filter Current	Analog Current Output	Apply PLL filter referenced to Pin 41.
39	No Connection		May be left floating.
40	No Connection		May be left floating.
41	PLL Filter Reference Voltage	Analog Output Voltage	5 V reference voltage for the PLL filter, decoupling with 01 μF capacitor required.
42	Set VCO Center Frequency	Analog Current Input	Resistor/current programmable.
43	AGC Mode Control Bit 0	TTL Input	Defines read channel operating mode.
44	AGC Mode Control Bit 1	TTL Input	Defines read channel operating mode.
45	Window Strobe	Analog Input Voltage	±1 V range relative to analog +5 V.
46	Analog +12 V	Power Input	Decoupling with 0.1 μF||0.01 μF required.
47	AGC Acquire Gain	Digital CMOS Input	Logic "1" = 800 μA, Logic "0" = 80 μA.
48	AGC Level Set Input	Analog Voltage Input	Sets the average signal to the S/H to the applied input voltage.
49	VGA Level Set Input	Analog Voltage Input	Sets the VGA gain (dB) =30 − (50 × V_{SET} level).
50	Sample-and-Hold Capacitor	Analog Current Output	
51	VGA Input Voltage (Pos)	Analog Voltage Input	
52	No Connections		May be left floating.

CHANNEL PROCESSING STAGES

The VGA Stage

The 30 dB variable gain stage input is biased at a potential of 5.0 V above analog ground. No additional dc bias is required, but ac coupling is necessary. The bias voltage is maintained during normal operation and during operation of the read after write recovery clamp.

The VGA differential output stage is an emitter follower with nominal dc biasing of 6.7 V. An internal 1.25 mA current source provides bias current to the output emitter followers. Output drive can be increased by an additional 1.25 mA by paralleling external resistors to the analog ground. However, caution should be exercised in order to avoid causing excess power dissipation for the package. The recommended output level for the VGA is 300 mV p–p differential into a 200 Ω differential load.

When the AD897 is used in the "VGA Set Gain" mode, AGC Mode Control Bit 0 = 1 (Pin 43) and Bit 1 = 0 (Pin 44), the VGA gain is programmable through the "VGA Level Set" pin (Pin 49). A 0 V potential applied to the "VGA Level Set" pin will produce a nominal VGA gain of 30 dB. Each 20 mV increment of voltage applied will produce a 1 dB reduction in VGA gain. Therefore, a simple equation can be used to calculate the nominal gain of the VGA in this mode:

$$VGA\ Gain\ (dB) = 30 - (50 \times V_{SET\ LEVEL})$$

If the "VGA Level Set" pin is not used, as may be the case when the AD897 is used in the AGC acquire and AGC hold modes only, it should be tied to analog ground.

The AD897 offers a read-after-write overdrive protection clamp. The "Input Clamp" mode, AGC Mode Control Bit 0 = 1 (Pin 43), Bit 1 = 1 (Pin 44), lowers the differential input impedance of the VGA from nominally 24 kΩ to 40 Ω. While the input clamp is active, the AGC loop is placed in the hold mode. In order for the clamp to operate correctly with an emitter driven input, a 50 Ω minimum resistor should be placed in series with the input coupling capacitors. The input resistors can be used in conjunction with a shunt capacitor to limit the input bandwidth. For example, a 100 Ω series resistor with a 10 pF shunt capacitor will limit the input bandwidth to 75 MHz. When the VGA input is being driven by an open collector driver with resistive termination, no additional series resistors are required.

The X16 Buffer

The inputs of this stage has on-chip dc biasing of 4.3 V (Internal Peak Detector Reference Voltage, Pin 3), therefore, no input bias current path needs to be provided. The inputs to the buffer should then be ac coupled. When not used, the inputs should be shorted together in order to avoid noise pickup and instability.

The nominal dc output level is 5.75 V with an internal 3.0 mA pull down current source. Output drive can be increased in a similar manner to that described for the VGA stage, by paralleling external resistors to analog ground. As before, precautions to limit excessive overall power dissipation apply when steps are taken to increase the output drive capability.

The Full Wave Rectifiers

The inputs to the full wave rectifiers are biased at an internal voltage of 5.75 V; therefore, only ac coupling is recommended. The full wave rectifier outputs consist of two nearly identical stages. Both employ emitter follower outputs. The nominal output voltage with zero input voltage is close to the peak detector's internal reference voltage of 4.3 V (Pin 3).

The rectified output voltage for the AGC loop is available through a 250 Ω resistor (Pin 12). The emitter follower output stage does not have a committed pull-down resistor. This enables the user to implement "peak-hold" AGC operation by applying the appropriate parallel RC combination between the "Rectified Signal for the AGC" (Pin 12) and ground.

The other full wave rectifier output – a rectified signal to derive the threshold for the data qualifier – is connected directly to its respective emitter follower output stage (Pin 15). This output also does not have a committed pull-down resistor, allowing for increased design flexibility.

When choosing the respective pull-down resistor values, caution should be exercised in order to avoid causing excess power dissipation for the package. In addition, to maintain well controlled rectifier offset voltages their quiescent currents must be matched.

The AGC Sample and Hold

When the AD897 is used in the "AGC Acquire" mode, AGC Mode Control Bit 0 = 0 (Pin 43) and Bit 1 = 0 (Pin 44), the AGC level is programmable through the AGC Level Set pin (Pin 48). A third control line, AGC Acquire Gain (Pin 47), sets the AGC charge current.

The AGC Level is defined as the AVERAGE of the full wave rectifier output voltage to the sample-and-hold amplifier. A 200 mV dc potential applied to the AGC Level Set pin will produce a nominal AGC level of 100 mV. Each 10 mV increment/decrement of the applied "AGC Level Set" voltage will produce a 5 mV increase/decrease in the AGC level. Therefore, a simple equation can be used to calculate the nominal AGC level in this mode:

$$AGC\ Level = 0.5 \times V_{AGC\ LEVEL\ SET}$$

Without a peak hold capacitor at the full wave rectifier output for the AGC (Pin 12), accurate AGC operation only occurs with sinusoidal input signals. If your application requires the AGC operation to use a peak hold scheme, a "Peak-Hold" capacitor in series with a resistor maybe applied to the full wave rectifier output pin for the AGC (Pin 12). The addition of the RC alters the symmetry of the attack and decay rates of the rectifier, which is otherwise symmetric in operation. In order to ensure that the overall AGC response is the same for both high to low and low to high input level steps, it is necessary to make the rectifier attack and decay times at least a factor of two less than the AGC response time.

The AD897 offers two user programmable attack/decay times for the AGC loop. The AGC "slow" attack/decay times are achieved by setting the AGC Acquire Gain = "0" (Pin 47) and results in an 80 μA charge/discharge current on the Sample/Hold capacitor. Conversely, "fast" attack/decay times are achieved by setting the AGC acquire gain = "1" (Pin 47) and results in an 800 μA charge/discharge current. With the AD897 in the "fast" attack/decay mode and a 1000 pF sample-and-hold capacitor applied to Pin 50, a symmetrical 1 μs attack/decay time is achieved. A low leakage variety of hold capacitor, such as a silver mica, is necessary to ensure a low droop rate.

The AGC control potential is present at the "Sample-and-Hold Capacitor" pin (Pin 50). If control over open loop gain is desired, based on AGC control potentials measured during trial AGC operations, a FET input op amp should be used to buffer this node in order to avoid disturbing the hold operation.

DATA QUALIFIER STAGE

The AD897 data qualifier stage consists of three comparators, a pair of externally adjustable "resettable" delay lines, two Nand gates, two D-type flip-flops, and an externally adjustable one-shot (refer to the AD897 block diagram).

Figure 1 illustrates the operation of the AD897 data qualifier, using the recommended passive delay-line/differentiator described in the application section. Sequence "A" represents the pattern written on the disk, where a logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the AD897 consists of a sequence of alternating pulses "B." The data pattern shown is for worst case RLL 1, 7 code input. The AD897 requires that the analog data input pass three criteria in order to qualify a signal and produce an output bit. The triple data qualification requirement significantly reduces errors by ensuring that noise will not be misinterpreted.

The first data qualification criteria is signal amplitude and is accomplished through the use of two amplitude threshold comparators. The outputs of each comparator drives a "resettable" delay line. The "resettable" delay line implements the second valid-data criteria, minimum time above valid-signal threshold before a zero-crossing can be detected. The minimum time above valid-signal threshold is set through an external resistor. The output of the "resettable" delay line is then used to determine if the data exhibits the correct polarity, the third data qualification criteria. To determine if the data exhibits the correct polarity a D-type flip-flop is used. The flip-flop is toggled with each valid data pulse, thereby, ensuring an alternate polarity qualification for each valid incoming data bit.

"C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in the state of this output are used to clock an internal D-type flip-flop. The flip-flop is enabled using the output from the data polarity check, such that the flip-flop output changes state only when ALL three of the data qualification criteria, described earlier, have been satisfied. If ALL three data qualification criteria were met, and a zero-crossing event occurs, the flip-flop changes state, producing an output pulse "E." The duration of this pulse, seen at the Raw Data Output pin (Pin 28), is set using an external resistor. The one-shot also triggers the second D-type flip-flop, toggling the required valid-data polarity. The final output data sequence is shown in "F." As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a reconstructed version of the write data.

Since the 1–7 code input is the most demanding of the popular encoding schemes to qualify, the AD897 easily handles such other codes as MFM and RLL 2, 7.

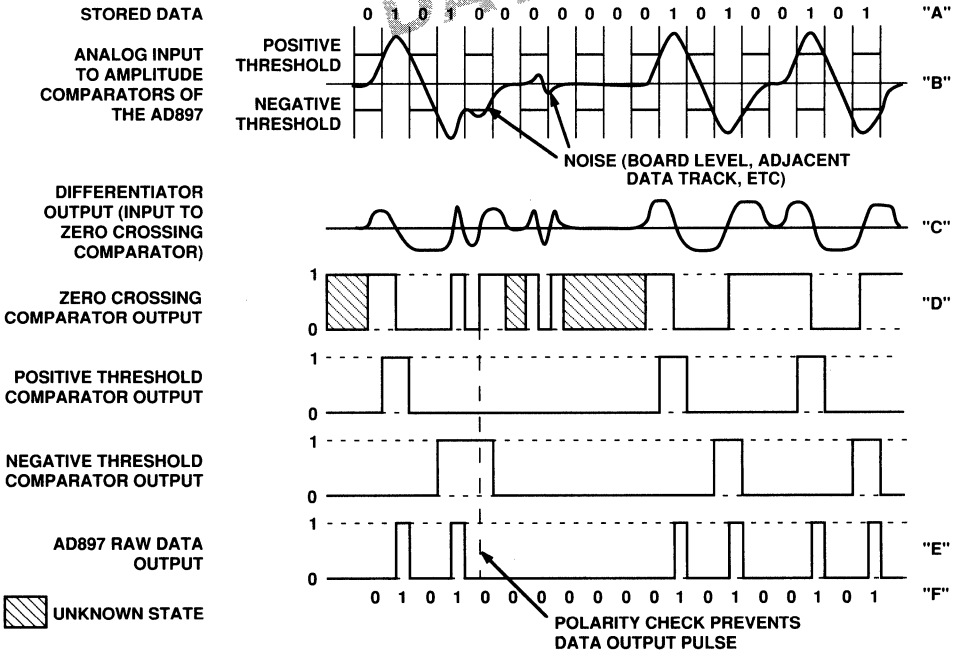


Figure 1. AD897 Operation for Worst Case 1–7 RLL Code

DATA SYNCHRONIZER STAGES

Phase Detector/Charge Pump

Figure 2 illustrates the operation of the phase/frequency detector and the charge pump in the lock to data mode. The data signal initiates a pump up – pump down – pump up cycle. The window center is marked by the falling edge of the clock present at the phase detector as shown. If the rising edge of the data pulse arrives at the window center then each charge pump cycle is exactly one half of the clock period long. Since the charge down current equals twice the charge up current charge balance is achieved at the end of the sequence. When the data pulse is early the first charge up cycle is stretched and the voltage on the filter increases. Conversely, if the data pulse is late the first pump-up cycle is shortened, thereby decreasing the voltage on the filter.

The above "Tri-Phase" phase detector avoids the shortcomings of the traditional "sliver" approach phase detector, by eliminating the dead band (zero phase detector gain) in the middle of the window. In addition, the "Tri-Phase" implementation does not require a half clock period long delay line, therefore window centering is improved and independent of the VCO frequency. To further improve window centering, the pump-up and pump-down currents are laser trimmed to ensure charge balancing.

The "Tri-Phase" phase detector was designed to allow the detection of data pulses arriving in adjacent windows, although that would be considered illegal with most encoding schemes. If such an event does occur, the synchronized data output would remain high for two consecutive clock periods.

In the frequency lock mode, the charge pump currents are equal in both directions. In this mode, the earlier of the data or clock pulse generates a charge-up or charge-down cycle. The charge cycle is terminated upon arrival of the later pulse, data or clock. Therefore, the lock to frequency mode does utilize the "sliver" approach and has the aforementioned drawbacks. However, in the frequency lock (lock to external clock or lock to preamble) mode the emphasis is on acquiring frequency matching between the reference source and the VCO.

In the tristate mode both the charge up and charge down current sources are disabled. This results in a frequency hold mode with respect to the VCO (coast).

The charge pump gain depends on the state of the PLL mode control lines (PLL Lock Mode Control Bit 0, PLL Lock Mode Control Bit 1) and the PLL Acquire Gain line (Pin 35). The following table gives a summary of the possible gain settings:

PLL Acquire Gain	Lock to Preamble	Charge Pump Gain
0	No	1/2 Nominal
0	Yes	Nominal
1	No	Nominal
1	Yes	2× Nominal

When considering the overall gain of the phase detector/charge pump block, it is important to remember that the gain is a function of the update rate of the detector:

$$\textit{Nominal Overall Gain} = 200\ \mu A/(n2\pi)$$

where n = number of clock cycles per update

In lock to external clock and lock to preamble modes n is equal to 1.

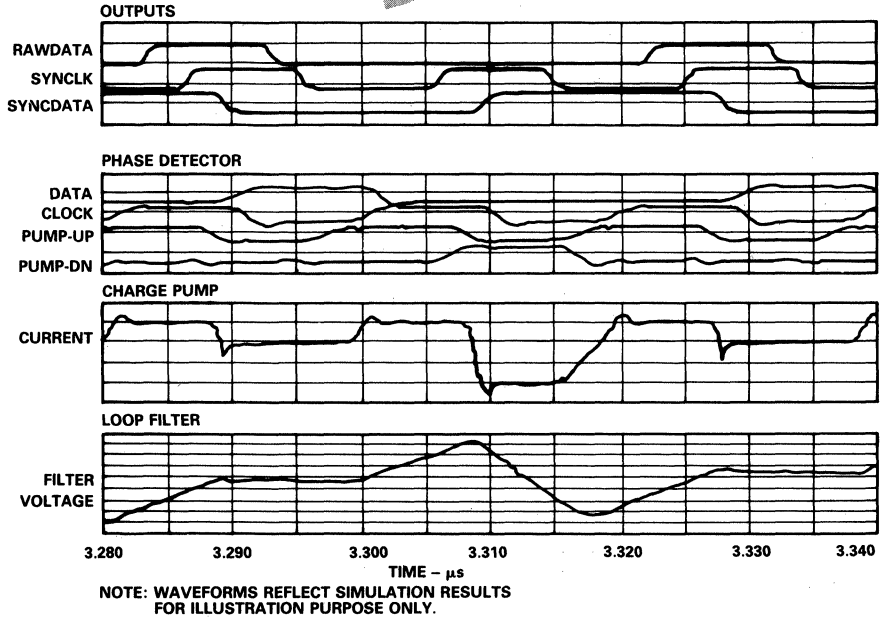


Figure 2. PLL Operation in Lock to Data Mode

Exponentiator/VCO

The exponentiator provides an exponential relationship between the control voltage appearing on the loop filter and the VCO frequency. Figure 3 graphically illustrates this exponential relation, with the control voltage on the X axis and the VCO frequency (normalized to ω_O) on the Y axis.

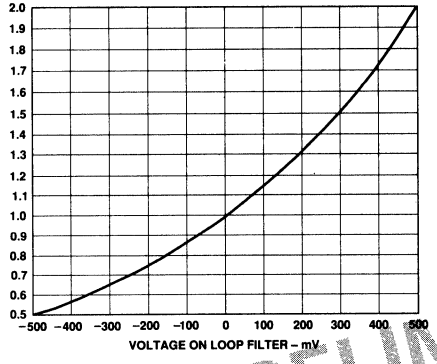


Figure 3. Exponentiator/VCO Transfer Curve Normalized to Center Frequency

The input stage of the exponentiator block uses PMOS transistors resulting in negligible charge leakage on the loop filter when the PLL is in tristate mode. This in turn enables the AD897 to achieve excellent frequency hold characteristics when the VCO is coasting.

The VCO center frequency is resistor or current programmable through the Set VCO Center Frequency pin (Pin 42). To help determine the appropriate resistor value, Figure 4 is provided.

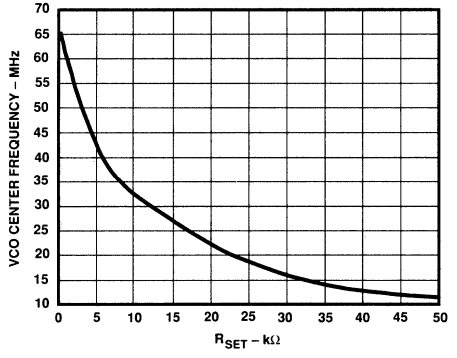


Figure 4. VCO Center Frequency vs. Resistor Value

The achievable VCO frequency range relative to center frequency is limited to 4:1. For example, if the user sets the center frequency to 30 MHz, the PLL will be abie to lock to a reference frequency anywhere from 15 MHz to 60 MHz, more than adequate for zone bit recording applications with their 2:1 range.

Dividers

The VCO clock is passed through a divider/multiplexer block prior to being applied to the phase/frequency detector. The division factor is programmed through the Division Factor Bit 0 (Pin 33) and the Division Factor Bit 1 (Pin 34) control pins.

Division Factor Bit 0	Division Factor Bit 1	Division Factor
0	0	1
0	1	2
1	0	3
1	1	4

Under normal conditions these control lines are expected to change together with PLL mode control lines and the PLL acquire line.

In the lock to external clock and lock to preamble modes the user has the option to determine the VCO/external clock or VCO/preamble frequency ratio. In both cases the VCO frequency is divided down by the programmed division factor. Also, in the lock to external clock, the reference frequency is divided by a factor of two. In the lock to data and tristate modes, the VCO clock is passed directly to the phase detector input.

Having a programmable divider in the feedback path and a fixed division of the reference clock path coupled with the 4:1 VCO frequency range provides considerable flexibility in choosing the reference crystal or preamble frequency for any encoding schemes.

GENERAL LAYOUT REQUIREMENTS

The AGC section of the AD897 has almost 60 dB of total gain available at 60 MHz. Good RF layout must be used in the circuit board to avoid oscillations in the 150 MHz to 350 MHz region. A single pole RC filter applied at the input of each stage, with a cutoff in the region of 75 MHz to 125 MHz, will help avoid oscillation problems. As a general rule, keep the connections to interstage components as short as possible; it is also recommended that any low-pass filtering that may be required by the system be performed between the VGA stage and the X16 buffer amplifier. A ground plane should be used to surround any interstage components wherever possible. If these simple rules are followed, stable operation should be assured.

A parallel combination of 0.1 μF and 0.01 μF ceramic capacitors should be used as close to the supply pins as possible; this includes the Analog +12 V (Pin 46), Analog +5 V (Pin 21) and Digital +5 V (Pin 31) supplies. It is also recommended that the PLL Filter Reference Voltage (Pin 41) is decoupled with a 0.1μF ceramic capacitor.

Extensive use of a ground plane is recommended. An analog ground (Pin 20) is supplied for the AGC section, while two digital grounds are supplied: one for the Data Qualifier/PLL section (Pin 24), and one for the output buffers (Pin 25). The digital ground should be connected to the analog ground as near to the power supply common as possible to minimize noise injection to the analog ground.

The filter and output pulse setting resistors should be tied, as directly possible, to the +5 V analog supply.

PPL OPERATING MODES

Lock to External Clock – PLL Lock Mode Control Bit 0 = 0, Bit 1 = 0. Lock to both frequency and phase of the reference clock is divided down internally by 2. In the feedback path the VCO output is divided down by the programmed division factor: 1, 2, 3, or 4. This enables the user to achieve a range of VCO vs. external clock frequency ratios namely 1:2, 1:1, 3:2, 2:1. The clock signal on the External Clock Input (Pin 32) is multiplexed to the Synchronized Clock Output (Pin 30). Upon entering or exiting this mode a glitch-free transition between the VCO and the external clock is provided.

Lock to Preamble – PLL Mode Control Bit 0 = 0, Bit 1 = 1. In this mode, the raw input data stream provides the phase information. A constant frequency input which equals the VCO frequency divided by the programmed division factor is required. The loop is operated in the frequency lock mode. The charge pump gain is doubled or quadrupled if the PLL Acquire Gain pin (Pin 35) is high at the same time.

Lock to Data – PLL Mode Control Bit 0 = 1, Bit 1 = 1. Phase lock only to the Raw Data Output (Pin 28) of the read channel. When entering this mode zero phase start-up is automatically initiated after four data pulse updates have been received following the command. The charge pump is tristated during the delay period, ensuring a minimal glitch during synchronization. The loop time constant is defined by an external RC filter network. This is the only mode when the Synchronized Data Output (Pin 29) is enabled.

Tristate – PLL Mode Control 0 = 1, Bit 1 = 0. This mode allows the user to hold the loop filter voltage so that the VCO frequency remains constant without having to switch to lock to external clock.

Switching Between PPL Operating Modes

Figure 5 illustrates a typical sequence of PLL operating modes. The control signals should be derived from an external register. When changing between operating modes care should be taken to avoid shorter pulses than required to complete the transition from one operating mode to another. In most cases the charge pump is tristated and the VCO is disabled for a period of four data pulses applied to the phase detector (see Figure 6); this translates into a delay of 4 data or 8 external clock pulses. This features prevents the charge pump from generating any glitches thus preserving the integrity of the loop voltage.

Upon the appropriate delay, the subsequent pulse restarts the VCO. When switching to lock to data mode the VCO is synchronized with the 5th data pulse, resulting in a zero phase start-up error. The combination of the above described frequency hold and zero phase start-up error eliminates any disturbance of the loop during the transition from one operating mode to another. To further minimize the lock in time, the user has the option of momentarily doubling the charge pump gain through the "PLL Acquire Gain" control line.

When switching from/to lock to external clock, the transition involves changing the clock source present on the Synchronized Clock Output pin (Pin 30). The signal present at this pin changes from the external clock (Pin 32) to the VCO, or vice versa. Extra care has been taken to provide glitch-free multiplexing of these clock sources and to minimize the time while the clock is inactive.

The following table summarizes the possible operating mode transitions and their effects on the different circuit blocks.

Previous Mode	Present Mode	Charge Pump	VCO	Synchronized Clock
Lock to Ext. Clock	Lock to Preamble	Gain = 2×	No Effect	Switch to VCO Clock
	Lock to Data	Tristate for 4 Updates	Zero Phase Start-Up	Switch to VCO Clock
	Tristate	High Impedance	Coast	Switch to VCO Clock
Lock to Preamble	Lock to Data	Tristate for 4 Updates	Zero Phase Start-Up	Inactive for 4 Updates
	Tristate	High Impedance	Coast	Inactive for 4 Updates
	Lock to Ext. Clock	Tristate for 8T Ext. Clock	Disabled for 8T Ext. Clock	Switch to Ext. Clock
Lock to Data	Tristate	High Impedance	Coast	VCO Clock
	Lock to Ext. Clock	Tristate for 8T Ext. Clock	Disabled for 8T Ext. Clock	Switch to Ext. Clock
	Lock to Preamble	Gain = 2×	No Effect	VCO Clock
Tristate	Lock to Ext. Clock	Tristate for 8T Ext. Clock	Disabled for 8T Ext. Clock	Switch to Ext. Clock
	Lock to Preamble	Tristate for 4 Updates	Disabled for 4 Updates	Inactive for 4 Updates
	Lock to Data	Tristate for 4 Updates	Zero-Phase Start-Up	Inactive for 4 Updates

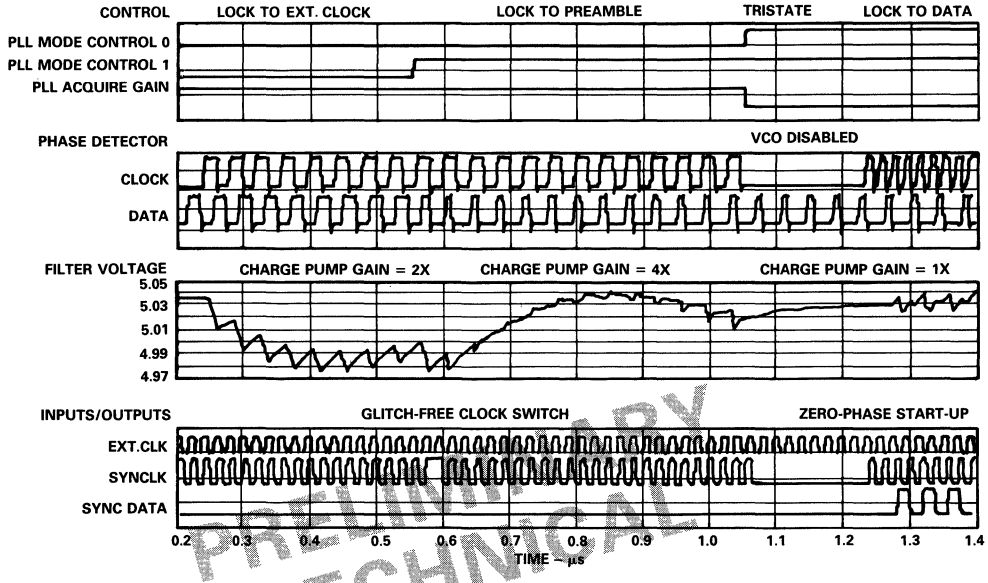


Figure 5. PLL Operating Mode Sequencing

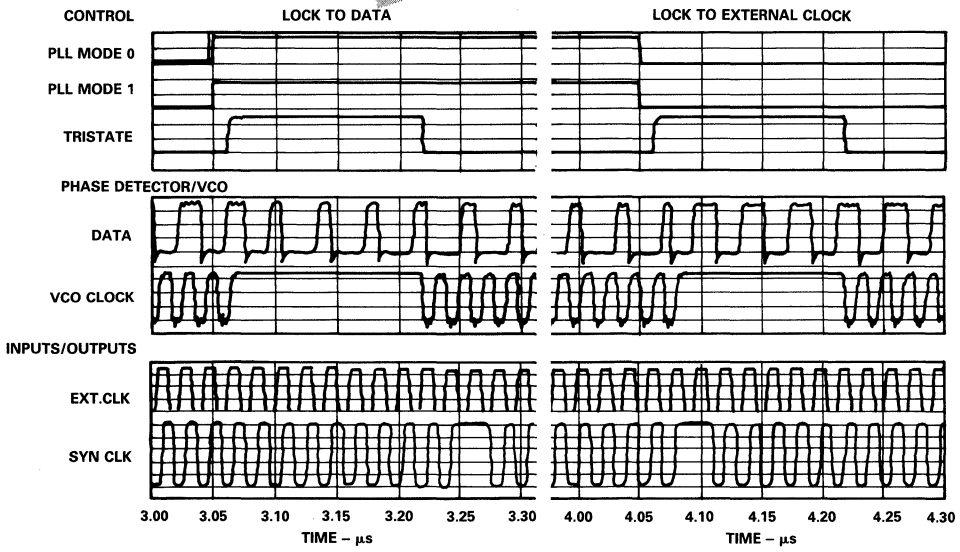
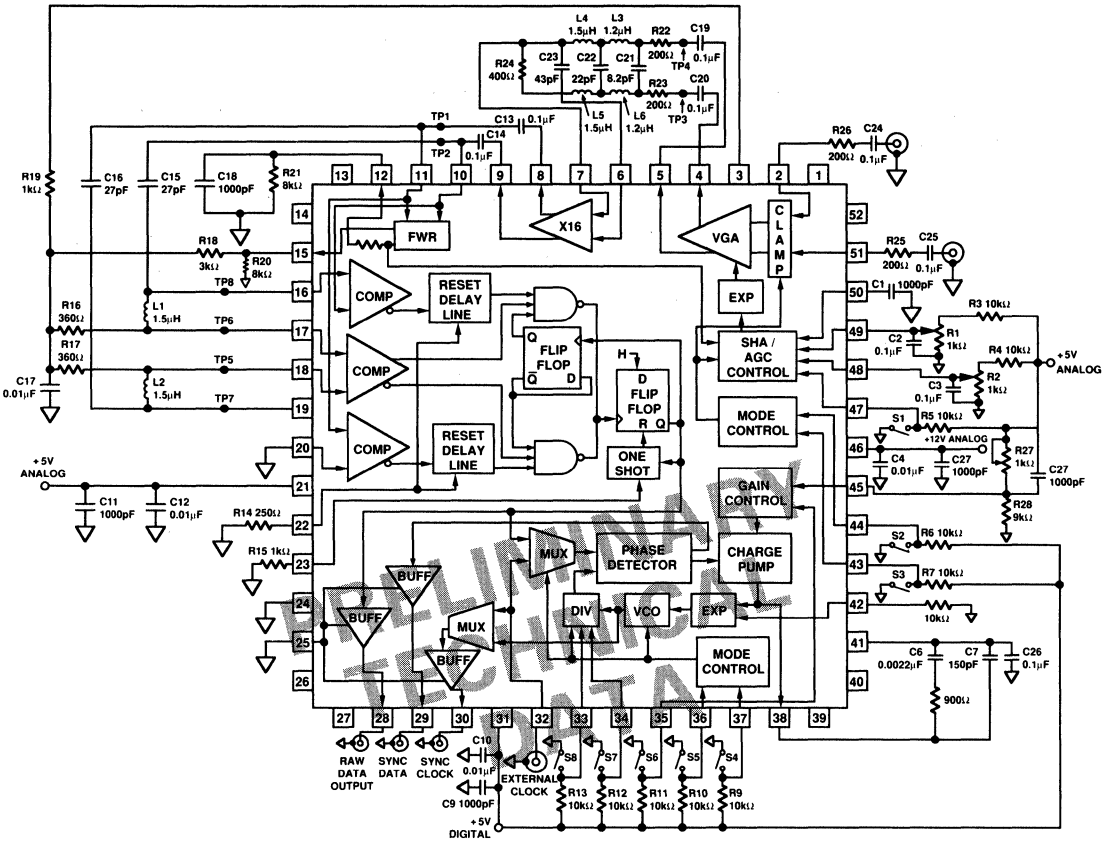


Figure 6. Transition Between Operation Modes. Lock to External Clock—Lock to Data—Lock to External Clock



FUNCTIONALITY OF SWITCHES

Switch	Description
1	AGC Acquire Gain
2	AGC Mode Control Bit 1
3	AGC Mode Control Bit 0
4	PLL Lock Mode Control Bit 1
5	PLL Lock Mode Control Bit 0
6	PLL Acquire Gain
7	Division Factor Control Bit 1
8	Division Factor Control Bit 0

DEFINITION OF TEST POINTS

Test Point	Definition
1	Negative input to the full wave rectifier, also serves as input to the passive differentiator and the negative comparator input.
2	Positive input to the full wave rectifier, also serves as input to the passive differentiator and the positive comparator input.
3	Negative AC coupled output of the VGA.
4	Positive AC coupled output of the VGA.
5	Negative input to the zero-crossing comparator.
6	Positive input to the zero-crossing comparator.
7	Negative threshold comparator input.
8	Positive threshold comparator input.

ATE Components
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AD1321 – High Speed Pin Driver with Inhibit Mode . . . . . 10 – 25
AD1322 – Ultrahigh Speed Pin Driver with Inhibit Mode . . . . . 10 – 37
AD1322B – Ultrahigh Speed Pin Driver with Inhibit Mode . . . . . 10 – 49

Other ATE-Related Components:

AD9500 – Digitally Programmable Delay Generator, ECL . . . . . 11 – 33
AD9501 – Digitally Programmable Delay Generator, TTL . . . . . 11 – 43
AD9696/9698 – Ultrafast TTL Comparators . . . . . 3 – 13
AD96685/96687 – Ultrafast Comparators . . . . . 3 – 21

Orientation
ATE Components

A complete ATE test-head design requires an appropriate mix of high speed, high performance components that are small enough to provide the needed functional density. Analog Devices provides a wide selection of components, based on various IC process technologies and logic families, to provide appropriate choices for ATE.

Designers of automatic test equipment (ATE) systems for advanced components have always had a dilemma; in order to test the newest, fastest, most precise products, they themselves need components that are even better than those they are testing. The unique design constraints of ATE add to the difficulties of assembling a system for testing high speed, high pin-count devices. The electrical interface between the device under test (DUT) and the rest of the ATE system is the *pin electronics*, a complex subsystem containing the functions needed to source precise signals to the DUT pins as well as measure DUT-generated signals. There is an identical—or nearly so—pin electronics circuit for each active pin of the DUT, arranged in a circle around the DUT at the test head to maximize achievable density and partially equalize propagation delays between pin electronics and the DUT.

The heart of the pin electronics is the pin driver. This device must produce highly repeatable, low jitter pulses with precisely set amplitude and slew rate for the DUT. The pin-driver timing is set digitally; its amplitude is determined by analog control voltages. Because of the high speeds of pin drivers—a 100 MHz repetition rate corresponds to a 5 ns pulse width—the driver and DUT are typically interconnected by a 50 Ω transmission line. The pin driver can be digitally disconnected via a high impedance three-state output mode, needed when the DUT has an input/output pin (two modes) that must be tested without physically disconnecting the driver.

Figure 1, a typical pin-electronics block diagram, shows the variety of devices needed for the complete function. Under control of the test computer and dedicated hardware, desired data patterns must be generated for simultaneous application to DUT inputs; at the same time, appropriate DUT outputs must be captured and measured. For complete parametric testing, signal levels must be precisely varied by the test program to determine maximum and minimum performance boundaries.

The complete pin-electronics function requires many digital-to-analog converters (DACs) to program the source current, sink current, and the threshold (commutation) voltage between current sourcing and sinking modes.

Although Figure 1 shows DACs setting key levels, many testers now use rapidly refreshed *sample/hold* circuits—driven by a shared, precise DAC. The S/H amplifier is used in *data distribution* instead of data acquisition, i.e., the S/H *holds* a digitally determined value during the test to establish a quasi-steady-state value instead of capturing an unknown signal value prior to digitizing it.

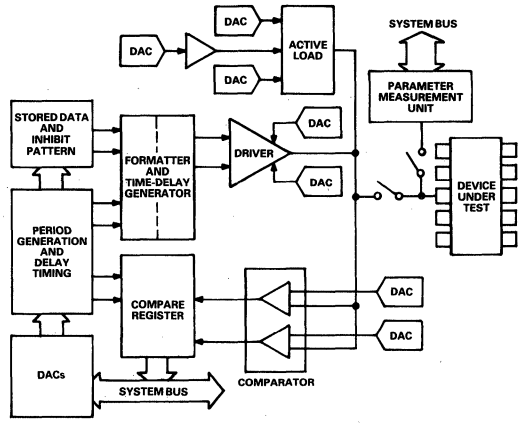


Figure 1. Typical Pin-Electronics Block Diagram; All Items Shown May Recur for Each Driven Pin in High-Performance Systems

Unavoidable time skew occurs between signals from the many drivers as they reach the DUT. This is due to different path lengths (and therefore delays), as well as propagation delays within active components. To compensate for this, a time-delay deskewing circuit or delay line is included with each pin's electronics. The precise delay time must be set with high resolution; it is determined during the system calibration cycles or by actual test.

The pulse output of a DUT pin is measured to provide rise and fall times (time from 10 to 90 per cent of upswing or downswing), amplitudes, slew rate, and related information. For the short time periods associated with these parameters, the measurements are made using pairs of comparators; the comparator output changes state when the waveform under observation crosses a specific threshold value. The threshold values for all these comparators are established by DACs or S/H circuits, under control of the test computer. The comparator outputs, in turn are connected to circuits that measure the period between changes in output states of the comparators.

DESIGN CHALLENGES

The designer's task is made more difficult by many simultaneous and often conflicting demands, as ATE speeds reach 200 MHz (and beyond), and DUT package content increases:

- high speed signal transitions are affected by parasitic inductance and capacitance, which slow the transitions and affect waveshape fidelity.
- noise glitches induced by high speed signals corrupt signals in nearby wiring; although decoupling, short leads, and ground planes are a minimum line of defense against these, more advanced techniques, such as differential signal paths, may also be required.
- accuracy in measurement requires components whose dynamic performance is predictable and stable with time and temperature. For a 200 MHz pin driver, the leading-edge-to-trailing-edge matching specification should be better than 200 ps. Low *dispersion* (variation in propagation delay as a function of the input signal swing) reduces skewing and makes compensation more precise; for example, low dispersion is critical in memory testers, to minimize the need for compensating delay lines on their many data pins. Dispersion matching should be close, both within a device and from device to device, for ease of replacement and calibration.
- slew rates must also be controlled (2 V/ns for the 200 MHz driver) for performance consistency.
- undershoot and overshoot of the pin-driver output must be limited in amplitude.
- the DUT must be tested at its normal operating voltages–and stressed beyond these values, so the ATE components must typically be capable of functioning with signals from −2 to +7 volts.
- *mixed-signal* testing imposes *additional* requirements for signal linearity, ramping, precision, and distortion for typically 20 out of 64 DUT pins.

The constraints are not solely electronic; electromechanical factors are also significant:

- test-head pin counts are increasing from 64 (typically) to 512 pins, requiring that more electronic circuitry be packed into the limited available space; using a larger test head means more propagation-delay uncertainty, timing mismatches, and corresponding inaccuracies.
- power consumption of the high speed circuitry is relatively high, exceeding 3 watts per pin; cooling the large number of densely populated pin-electronic circuits is difficult.
- power consumption and heating, along with other factors, affect reliability, which must be very high in a multimillion dollar test machine; users expect satisfactory up time and test throughput.
- the layout of the test head must maintain signal fidelity; transmission-line impedances must be held constant to minimize signal reflections between DUT and pin electronics.
- and, of course, cost becomes a significant factor when the per-pin cost is multiplied by the large number of pins.

FUTURE ATE PRODUCTS

For further information on the above products and future ATE products not listed here, please contact the factory directly.

ANALOG DEVICES

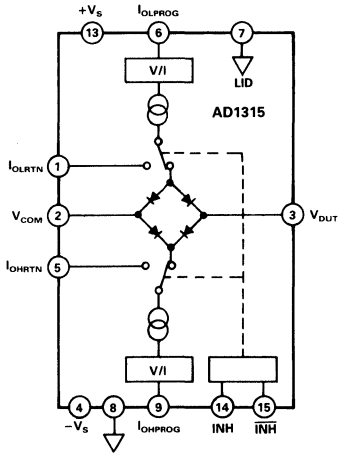
High Speed Active Load with Inhibit Mode

AD1315

FEATURES
±50 mA Voltage Programmable Current Range
1.5 ns Propagation Delay
Inhibit Mode Function
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package
Compatible with AD1321, AD1322 Pin Drivers

APPLICATIONS
Automatic Test Equipment
Semiconductor Test System
Board Level Test System

AD1315 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1315 is a complete, high speed, current switching load designed for use in linear, digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities in an ultrasmall 16-lead, hermetically sealed (gull wing) package.

Featuring current programmability of up to ±50 mA, the AD1315 is designed to force the device under test to source or sink the programmed I_{OHPROG} and I_{OLPROG} currents. The I_{OH} and I_{OL} currents are determined by applying a corresponding voltage (5 V = 50 mA) to the I_{OH} and I_{OL} pins. The voltage-to-current conversion is performed within the AD1315 thus allowing the current levels to be set by a standard voltage out digital-to-analog converter.

The AD1315's transition from I_{OH} to I_{OL} occurs when the output voltage of the device under test slews above or below the programmed threshold, or commutation voltage. The commutation voltage is programmable from −2 V to +7 V, covering the large spectrum of logic devices while able to support the large current specifications (48 mA) typically associated with line drivers. To test I/O devices, the active load can be switched into a high impedance state (Inhibit mode) electrically removing the active load from the path through the Inhibit mode feature. The active load leakage current in Inhibit is typically 20 nA.

The Inhibit input circuitry is implemented utilizing high speed differential inputs with a common-mode voltage range of 7 volts and a maximum differential voltage of 4 volts. This allows for the direct interface to the precision of differential ECL timing or the simplicity of switching the Active Load from a single ended TTL or CMOS logic source. With switching speeds from I_{OH} or I_{OL} into Inhibit of less than 1.5 ns, the AD1315 can be electrically removed from the signal path "on-the-fly."

The AD1315 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0 to +70°C.

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SPECIFICATIONS (All measurements made in free air at +25°C. $+V_S$ = +10 V, $-V_S$ = −5.2 V, unless otherwise specified.)

Parameter	AD1315KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
INH to $\overline{INH}$					
Input Voltage	−2.0		5.0	Volts	
Differential Input Range	0.4	ECL	4.0	Volts	
Bias Current	−2.0	1.0	2.0	mA	
Current Program Voltage Range					
I_{OH}, 0 mA to +50 mA (Sink)	0		+5.0	Volts	Note 1
I_{OL}, 0 mA to −50 mA (Source)	0		+5.0	Volts	Note 1
Input Resistance		50		kΩ	
I_{OHRTN}, I_{OLRTN} Range	−2.0		+7.0	Volts	Note 2
V_{COM}, V_{DUT} Range	−2.0		+7.0	Volts	
I_{OH}, 0 mA to 50 mA	0.5		+7.0	Volts	V_{DUT}–V_{COM}>1 V
I_{OL}, 0 mA to −50 mA	−2.0		+4.0	Volts	V_{COM}–V_{DUT}>1 V
OUTPUT CHARACTERISTICS					See Note 3
Active (Sink/Source) Mode					
Transfer Function		10		mA/V	See Figure 1
Accuracy					See Figure 1
Linearity Error	−0.12		+0.12	% FSR	
Gain Error	−2.0		+2.0	% FSR	
Offset Error	−1.0		+1.0	mA	
Output Current TC		10		μA/°C	
Inhibit Mode					
Output Capacitance			3.0	pF	
Inhibit Leakage	−200	20	200	nA	
DYNAMIC PERFORMANCE					See Note 3
Propagation Delay					See Figure 2
$\pm I_{MAX}$ to INHIBIT (t_{PD1})		0.5	1.5	ns	See Note 4
INHIBIT to $\pm I_{MAX}$ (t_{PD2})		1.5	3.0	ns	See Note 4
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range			15.4	Volts	
Supply Range					
Positive Supply	+9.5	+10	+10.5	Volts	
Negative Supply	−5.45	−5.2	−4.95	Volts	
Current					
Positive Supply	+60	+75	+90	mA	See Note 5
Negative Supply	−90	−75	−60	mA	See Note 5
Power Dissipation		1.1	1.4	Watts	See Note 6
PSRR			0.05	%/%	See Note 7

NOTES

[1] I_{OHPROG}/I_{OLPROG} voltage range may be extended to −100 mV due to a possible 1 mA offset current.

[2] I_{OHRTN}/I_{OLRTN} should be connected to V_{COM} to minimize power dissipation.

[3] V_{DUT} = −2 V to +7 V, C_{TOTAL} = 10 pF, R_{DUT} = 10 Ω.

[4] Measured from the ECL crossing to the 10% change in the output current.

[5] $I_{PROGRAM}$ = ±50 mA.

[6] Maximum power dissipation with $+V_S$ = +10 V, $-V_S$ = −5.2 V, $I_{PROGRAM}$ = ±50 mA, V_{COM} = V_{DUT} = 0V.

[7] For a 1% change in $+V_S$ or $-V_S$, the output current may change a maximum of 0.05% of Full Scale Range (FSR).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- $+V_S$ to GND . . . . . +12 V
- $-V_S$ to GND . . . . . −11 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from INH to $\overline{INH}$ . . . . . 5 V
- INH, $\overline{INH}$ . . . . . $+V_S$ −13.4 V, $-V_S$ +11 V
- V_{COM}, V_{DUT} . . . . . $+V_S$ −13.1 V, $-V_S$ +13.2 V
- I_{OL}, I_{OH} Program Voltage . . . . . $+V_S$ −15 V, $-V_S$ +15 V

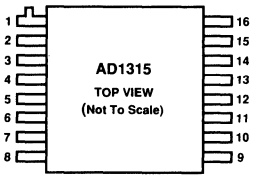
Operating Temperature Range . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 20 sec)** . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**To ensure lead coplanarity (±0.002 inches) and solderability handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

PIN NO.	SYMBOL	FUNCTION
1	I_{OLRTN}	LOGIC LOW CURRENT RETURN
2	V_{COM}	COMMUTATION VOLTAGE
3	V_{DUT}	LOAD/DUT CONNECTION
4	$-V_S$	NEGATIVE SUPPLY
5	I_{OHRTN}	LOGIC HIGH CURRENT RETURN
6	I_{OLPROG}	LOGIC LOW CURRENT PROGRAM VOLTAGE
7	LID	LID CONNECTION (INTERNAL)
8	GND	GROUND
9	I_{OHPROG}	LOGIC HIGH CURRENT PROGRAM VOLTAGE
10	N/C	NO CONNECTION
11	N/C	NO CONNECTION
12	N/C	NO CONNECTION
13	$+V_S$	POSITIVE SUPPLY
14	INH	INHIBIT
15	$\overline{INH}$	INHIBIT
16	N/C	NO CONNECTION

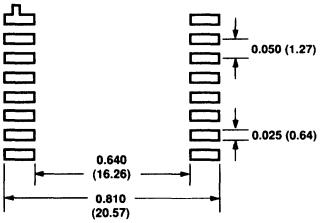
CONNECTION DIAGRAM



SUGGESTED PAD LOCATION

Dimensions shown in inches and (mm).

SUGGESTED LANDING PADS LOCATION



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DEFINITION OF TERMS

Gain

The measured transconductance.

$$Gain = \frac{I_{OUT}\ (@\ 5\ V\ Input) - I_{OUT}\ (@\ 0.2\ V\ Input)}{V_{PROG}\ (@\ 5\ V) - V_{PROG}\ (@\ 0.2\ V)}$$

where V_{PROG} values are measured at I_{OL}/I_{OH} PROG

Gain Error

The difference between the measured transconductance and the ideal expressed as a % of full-scale range.

$$Ideal\ Gain = 10\ mA/V$$

$$Gain\ Error = \frac{Ideal\ Gain - Actual\ Gain}{Ideal\ Gain} \times 100$$

Offset Error

Offset Error is measured by setting the I_{OHPROG} or I_{OLPROG} inputs to 0.2 V and measuring I_{OUT}. Since both I_{OH} and I_{OL} outputs are unipolar, this small initial offset of 2 mA must be set to allow for measurement of possible negative offset. With a gain of 10 mA/V, a 0.2 V input should yield an output of ±2 mA. The difference between the observed output and the ideal ± 2 mA output is the offset error.

$$Offset\ Error = I_{OUT}\ (@\ 0.2\ V) - Gain \times V_{PROG}\ (@\ 0.2\ V)$$

Linearity Error

The deviation of the transfer function from a straight line defined by Offset and Gain expressed as a % of FSR.

$$I_{OUT}\ (calc) = Gain \times V_{PROG}\ (@\ set\ point) + Offset$$

$$where\ set\ point = V_{PROG}\ (from\ 0.2\ V\ to\ 5\ V)$$

$$I_{OUT}\ (FSR) = Gain \times V_{PROG}\ (@\ 5\ V) + Offset$$

$$Linearity\ Error = \frac{I_{OUT}\ (measured) - I_{OUT}\ (calc)}{I_{OUT}\ (FSR)} \times 100$$

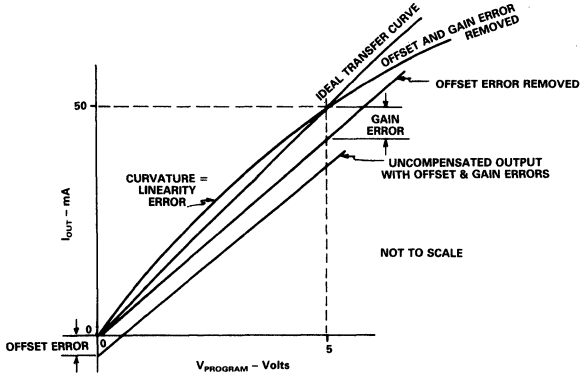


Figure 1. Definition of Terms

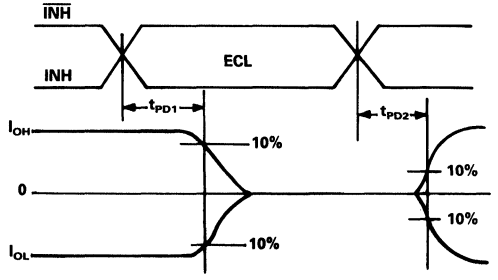


Figure 2. Timing Diagram for Inhibit Transition

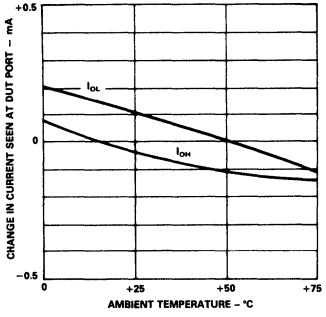


Figure 3. I_{OL}, I_{OH} Offset Current vs. Temperature

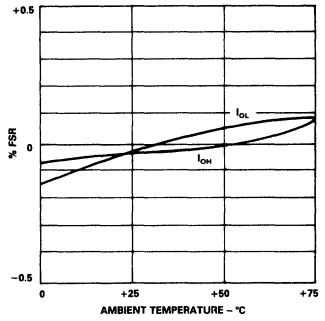


Figure 4. I_{OL}, I_{OH} Gain Error vs. Temperature

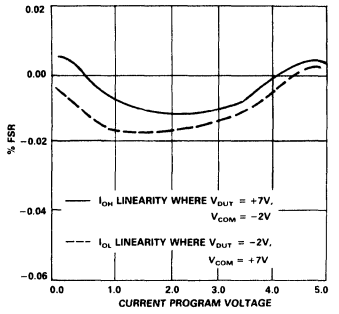


Figure 5. I_{OH}, I_{OL} Linearity Error vs. Current Program Voltage

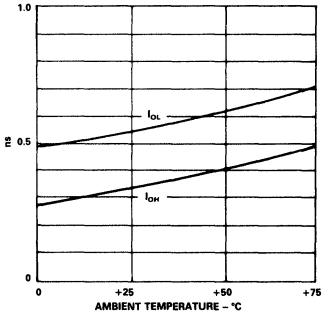


Figure 6. $+I_{MAX}$, $-I_{MAX}$ to Inhibit Propagation Delay vs. Temperature

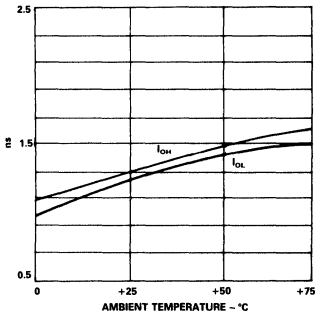


Figure 7. Inhibit to $+I_{MAX}$, $-I_{MAX}$ Propagation Delay vs. Temperature

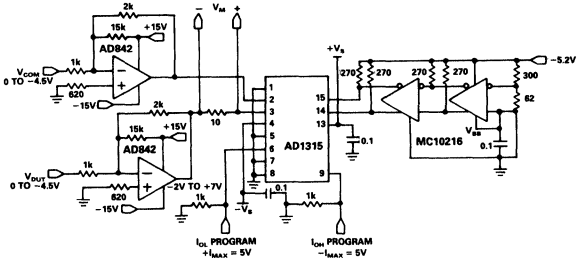


Figure 8. AD1315 DC Test Circuit

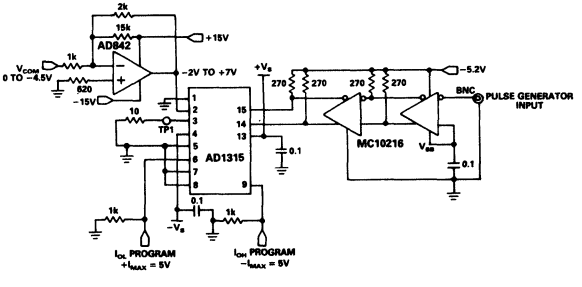


Figure 9. AD1315 Propagation Delay Test Circuit

FUNCTIONAL DESCRIPTION

The AD1315 is a complete high speed active load designed for use in general purpose instrumentation and digital functional test equipment. The function of the active load is to provide independently variable source and sink currents for the device to be tested.

The equivalent circuit for the AD1315 is shown in Figure 10. An active load performs the function of loading the output of the device under test with a programmed I_{OH} or I_{OL}. These currents are independently programmable. V_{COM} is the commutation voltage point at which the load switches from source to sink mode. The active load may also be inhibited, steering current to the I_{OLRTN} and I_{OHRTN} pins, effectively disconnecting it from the test pin.

The AD1315 accepts differential digital signals at its inhibit inputs ensuring precise timing control and high noise immunity. The wide inhibit input voltage range allows for ECL power supplies of −5.2 V and 0 V, −3.2 V and +2 V, and 0 V and +5 V. Where speed and timing accuracy are less important, TTL or CMOS logic levels may be used to toggle the Inhibit inputs of the AD1315. Single ended operation is possible by biasing one of the inputs to approximately +1.3 V for TTL or $V_{CC}/2$ for CMOS.

The I_{OH} and I_{OL} programming inputs accept 0 V to +5 V analog inputs, corresponding to 0 to 50 mA output currents. The V_{COM} input, which sets the I_{OH}/I_{OL} switch point, may be set anywhere within the input range of −2 V to +7 V.

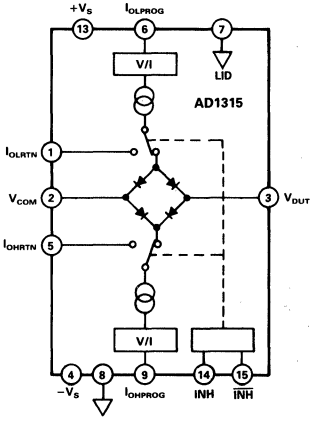


Figure 10. Block Diagram

V_{DUT} VOLTAGE RANGE

In Figure 11, V_{DUT} range, I_{OH} and I_{OL} typical current maximums are plotted versus DUT voltage. In the I_{OH} mode (V_{DUT} higher than V_{COM}), the load will sink 50 mA, until its output starts to saturate at approximately −1.5 V. In the I_{OL} mode (V_{DUT} lower than V_{COM}), the load will source 50 mA until its output starts to saturate at approximately +5.5 V. At +7 V, the source current will be close to zero.

Ideally, the commutation point set at V_{COM} would provide instantaneous current sink/source switching. Because of I/V characteristics of the internal bridge diodes, this is not the case. To guarantee full current switching at the DUT, at least a 1 volt difference between V_{COM} and V_{DUT} must be maintained in steady state conditions. Because of the relatively fast edge rates exhibited by typical logic device outputs, this should not be a problem in normal ATE applications.

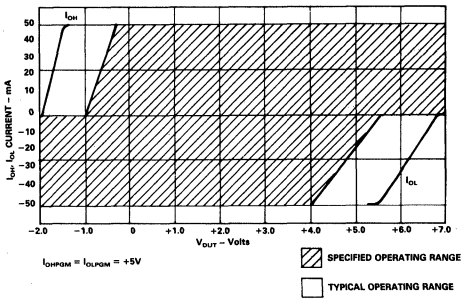


Figure 11. Allowable Current Range for I_{OH}, I_{OL} vs. V_{DUT}

THERMAL CONSIDERATIONS

The AD1315 is provided in a 0.550″ × 0.550″, 16-lead (bottom brazed) gull wing, surface mount package with a θ_{JC} of 10°C/W (typ). Thermal resistance (case-to-ambient) vs. air flow for the AD1315 in this package is shown in Figure 12. The data presented is for a ZIF socketed device. For PCB mounted devices (w/30 mils clearance) the thermal resistance should be ≈3 to 7% lower with air flows below 320 lfm[1]. Notice that the improvement in thermal resistance vs. air flow starts to flatten out just above 400 lfm[2].

NOTES
[1]lfm is air flow in linear feet/minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

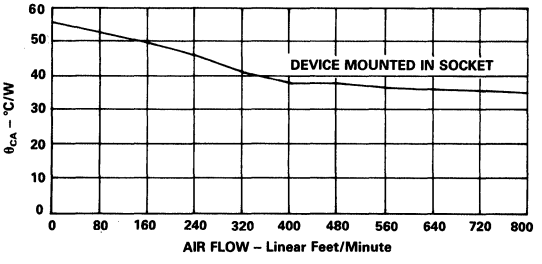


Figure 12. Case-to-Ambient Thermal Resistance vs. Air Flow

APPLICATIONS

The AD1315 has been optimized to function as an active load in an ATE test system. Figure 13 shows a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1315 active load, AD1321 or AD1322 pin driver, AD96687 high speed dual comparator and the AD664 quad 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 100 MHz with the AD1321 (200 MHz with the AD1322) in a data mode or 50 MHz (100 MHz) in the I/O mode.

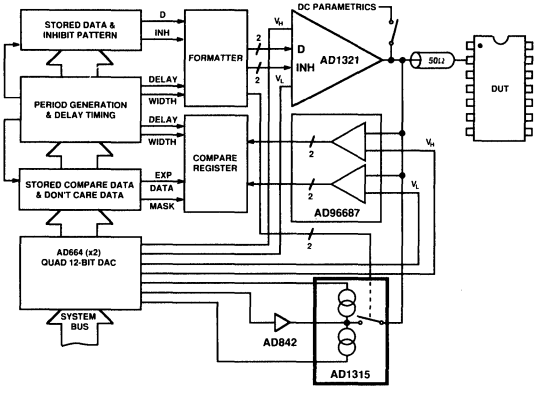


Figure 13. High Speed Digital Test System Block Diagram

LAYOUT CONSIDERATIONS

I_{OHRTN} and I_{OLRTN} may be connected to any potential between −2 V and +7 V. These return points must be able to source or sink 50 mA, since the I_{OH} and I_{OL} programmed currents are diverted here in the inhibit mode. The RTNs may be connected to a suitable GND. However, to keep transient ground currents to a minimum, they are typically tied to the V_{COM} programming voltage point.

The V_{COM} input sets the commutation voltage of the active load. With DUT output voltage above V_{COM}, the load will sink current (I_{OH}). With DUT output voltage below V_{COM}, the load will source current (I_{OL}). Like the I_{OH} and I_{OL} return lines, the V_{COM} must be able to sink or source 50 mA, therefore a standard op amp will not suffice. An op amp with an external complementary output stage or a high power op amp such as the AD842 will work well here. A typical application is shown in Figure 14.

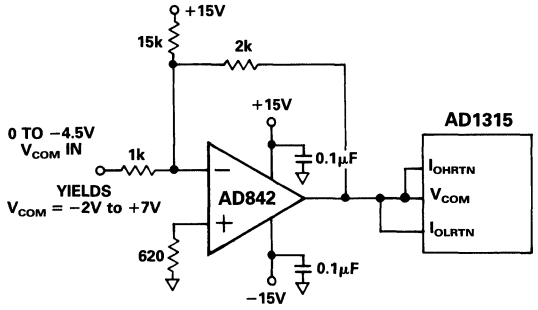


Figure 14. Suggested I_{OHRTN}, I_{OLRTN}, V_{COM} Hookup

10

EVALUATION BOARD

The AD1315 Evaluation Board allows the designer to easily evaluate the performance of the AD1315 and its suitability for the specific application. The AD1315EB includes a mounted AD1315KZ active load, an ECL input buffer for Inhibit and the oscilloscope probe jacks necessary to properly analyze the true performance of the AD1315KZ. An equipment list has been provided in order to minimize variations due to test setups.

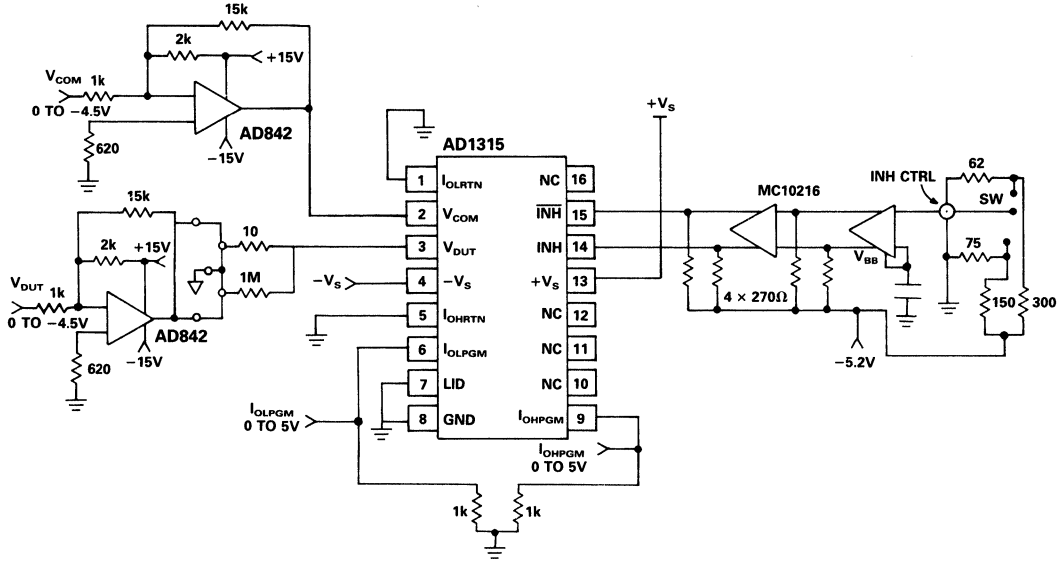


Figure 15. AD1315EB Evaluation Board Circuit

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD1315KZ	0 to +70°C	16-Lead Gull Wing	Z-16B

*See Section 20 for package outline information.

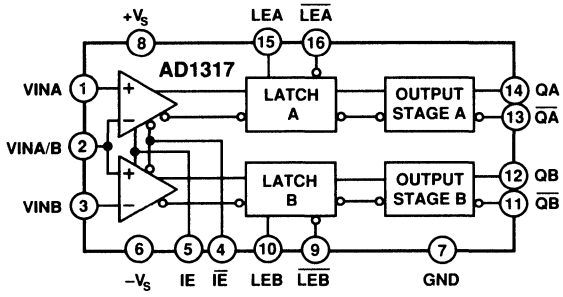
Ultrahigh Speed Window Comparator with Latch

AD1317

FEATURES
Full Window Comparator
2.0 pF max Input Capacitance
9 V max Differential Input Voltage
2.5 ns Propagation Delays
Low Dispersion
Low Input Bias Current
Independent Latch Function
Input Inhibit Mode
80 dB CMRR

APPLICATIONS
High Speed Pin Electronic Receiver
High Speed Triggers
Threshold Detectors
Peak Detectors

AD1317 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1317 is an ultrahigh speed window comparator with a latch. It uses a high speed monolithic process to provide high dc accuracy without sacrificing input voltage range. The AD1317 guarantees a 2.8 ns maximum propagation delay.

On-chip connection of the common input eliminates the contributions of a second bonding pad and package pin to the input capacitance, resulting in a maximum input capacitance of 2 pF.

The dispersion, or variation in propagation delay with input overdrive levels and slew rates, is typically 350 ps for 5 V signals and 200 ps for 1 V inputs.

The AD1317 employs a high precision differential input stage with a common-mode range of 9 V. Its complementary digital outputs are ECL compatible. The output stage is capable of driving a 50 Ω line terminated to −2 V. The AD1317 also provides a latch function, allowing operation in a sample-hold mode and can also be used to generate hysteresis.

The comparator input can be switched into a high impedance state through the inhibit mode feature, electrically removing the comparator from the circuit. The bias current in inhibit mode is typically 50 pA.

The AD1317 is available in a small 16-lead, hermetically sealed "gull-wing" surface mount package and operates over the commercial temperature range, 0 to +70°C.

10

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SPECIFICATIONS

(All specifications at +25°C, free air. Outputs terminated into 50 Ω to −2 V, with $+V_S$ = +10 V, $-V_S$ = −5.2 V unless otherwise specified.)

Parameter	Symbol	AD1317KZ Min	Typ	Max	Units	Comments
DC INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	−10		10	mV	CMV = 0 V
Offset Drift	dV_{OS}/dT		20		µV/°C	
VINA/B Bias Currents						−2 V to +7 V
Active	Ibca		10	33	µA	
Inhibit	Ibci		50		pA	
VINA, VINB Bias Currents						−2 V to +7 V
Active	Ibsa		5	16.5	µA	
Inhibit	Ibsi		50		pA	
VINA/B Resistance	Rinc		4		MΩ	
VINA, VINB Resistance	Rins		8		MΩ	
Capacitance VINA/B, VINA, VINB	C_{IN}		1.5	2.0	pF	
Voltage Range	V_{CM}	−2		7	Volts	See Note 5
Differential Voltage	V_{DIFF}			9	Volts	
Common-Mode Rejection Ratio	CMRR	70	80		dB	−2 V to +7 V
LATCH ENABLE INPUTS						
Common-Mode Range		−2.0		5.0	Volts	
Differential Voltage		0.4		4	Volts	
Logic "1" Current	I_{IH}			10	µA	
Logic "0" Current	I_{IL}	−200			µA	
Capacitance				4		pF
INPUT ENABLE CURRENTS						
Common-Mode Range		−2.0		5.0	Volts	
Differential Voltage		0.4		4	Volts	
Logic "1" Current	I_{IH}			20	µA	
Logic "0" Current	I_{IL}	−200			µA	
Capacitance				4		pF
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	−0.98			Volts	
Logic "0" Voltage	V_{OL}			−1.50	Volts	
SWITCHING PERFORMANCE						See Figure 3
Propagation Delays						
Input to Output	t_{PDR}, t_{PDF}		1.8	2.8	ns	See Note 1
Latch Enable to Output	t_{LO}		2.0	2.5	ns	See Note 1
Active to Inhibit	t_{ID}		2.5		ns	See Note 2
Inhibit to Active	t_{IE}		15		ns	See Note 3
Propagation Delay T.C.			5		ps/°C	
Dispersion						See Note 4
5 V Signal						See Figure 1
All Edges			450	600	ps	
Rising Edge			350		ps	
Falling Edge			350		ps	
1 V Signal						See Figure 2
All Edges			250	400	ps	
Rising Edge			200		ps	
Falling Edge			200		ps	
LATCH TIMING						See Figure 3
Input Pulse Width	t_{PW}	2.5	1.0		ns	
Setup Time	t_S	1.5	0.4		ns	
Hold Time	t_H	0			ns	
POWER SUPPLIES						
$-V_S$ to $+V_S$ Range			15.2	15.6		See Note 5
Positive Supply	$+V_S$	8.0	10.0	11.0	Volts	
Negative Supply	$-V_S$	−7.2	−5.2	−4.2	Volts	
Positive Supply Current	I+		50	70	mA	
Negative Supply Current	I−	−100	−70		mA	
PSRR		65	75		dB	Measured at ±2.5% of $+V_S$ and $-V_S$

NOTES

[1]Propagation Delay is measured from the input threshold crossing at the 50% point of a 0 V to 5 V input to the output Q and $\overline{Q}$ crossing.

[2]Propagation Delay is measured from the input crossing of IE and $\overline{IE}$ to when the input bias currents drop to 10% of their nominal value.

[3]Propagation Delay is measured from the input crossing of IE and $\overline{IE}$ to when the input bias currents rise to 90% of their nominal value.

[4]Dispersion is measured with input slew rates of 0.5 V/ns and 2.5 V/ns.

[5]The comparator input voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different input ranges such as −1 V to +8 V with power supplies of −4.2 V and +11 V, as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND . . . . . +12 V
- $-V_S$ to GND . . . . . −9 V
- Difference from $+V_S$ to $-V_S$ . . . . . +16 V

Inputs
- VINA/B, VINA, VINB . . . . . $+V_S$ −13.5 V, $-V_S$ +13.7 V
- LEA, $\overline{\text{LEA}}$, LEB, $\overline{\text{LEB}}$ . . . . . $+V_S$ −14 V, $-V_S$ +12 V
- IE, $\overline{\text{IE}}$ . . . . . $+V_S$ −14 V, $-V_S$ +10.3 V

Outputs
- QA, $\overline{\text{QA}}$, QB, $\overline{\text{QB}}$ . . . . . GND −0.5 V, GND +3.5 V

Operating Temperature Range . . . . . 0 to +70°C

Storage Temperature Range
- After Soldering . . . . . −65°C to +125°C

Lead Temperature Range (Soldering 20 sec)[2] . . . . . +300°C

NOTES

[1]Stresses above those limits under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

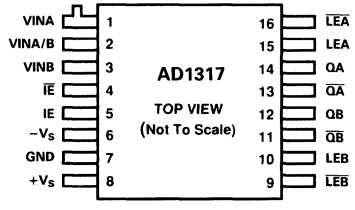
[2]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in an environment at 24°C ±5°C (75°F ±10°F) with relative humidity not to exceed 65%.

WINDOW COMPARATOR PIN ASSIGNMENT

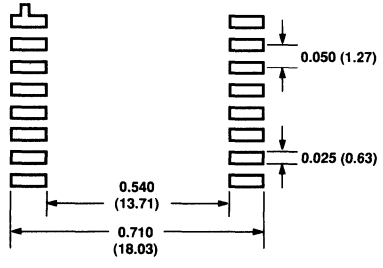
Pin No.	Description	
1	VINA	Noninverting Comparator A Input
2	VINA/B	Window Comparator Common Input
3	VINB	Inverting Comparator B Input
4	$\overline{\text{IE}}$	$\overline{\text{Input Enable}}$
5	IE	Input Enable
6	$-V_S$	Negative Supply, −5.2V
7	GND	Ground
8	$+V_S$	Positive Supply, +10V
9	$\overline{\text{LEB}}$	$\overline{\text{Latch Enable B}}$
10	LEB	Latch Enable B
11	$\overline{\text{QB}}$	$\overline{\text{Comparator B Output}}$
12	QB	Comparator B Output
13	$\overline{\text{QA}}$	$\overline{\text{Comparator A Output}}$
14	QA	Comparator A Output
15	LEA	Latch Enable A
16	$\overline{\text{LEA}}$	$\overline{\text{Latch Enable A}}$

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).



SUGGESTED LANDING PADS LOCATION



ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD1317KZ	0 to +70°C	16-Lead Gull Wing	Z-16A

*See Section 20 for package outline information.

10

AD1317 DEFINITION OF TERMS

V_{OS} INPUT OFFSET VOLTAGE – The voltage which must be applied between either VINA and VINA/B or VINB and VINA/B to obtain zero voltage between outputs QA and $\overline{QA}$, or QB and $\overline{QB}$, respectively.

dV_{OS}/dT OFFSET DRIFT – The ratio of the change in input offset voltages, over the operating temperature range, to the change in temperature.

Ibca INPUT BIAS CURRENT (VINA/B, ACTIVE) – The bias current of the window comparator's common input with inputs enabled.

Ibci INPUT BIAS CURRENT (VINA/B, INHIBIT) – The bias current of the window comparator's common input with inputs inhibited.

Ibsa INPUT BIAS CURRENT (VINA or VINB, ACTIVE) – The bias current of either single input with inputs active.

Ibsi INPUT BIAS CURRENT (VINA or VINB, INHIBIT) – The bias current of either single input with inputs inhibited.

Rinc INPUT RESISTANCE (VINA/B) – The input resistance looking into the window comparator's common input.

Rins INPUT RESISTANCE (VINA or VINB) – The input resistance looking into either single input.

C_{IN} INPUT CAPACITANCE (VINA/B) – The capacitance looking into the window comparator's common input.

V_{CM} INPUT COMMON-MODE VOLTAGE RANGE – The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

V_{DIFF} INPUT DIFFERENTIAL VOLTAGE RANGE – The maximum difference between any input terminal voltages.

CMRR COMMON-MODE REJECTION RATIO – The ratio of common-mode input voltage range to the peak-to-peak change in input offset voltage over this range.

I_{IH} LOGIC "1" INPUT CURRENT – The logic high current flowing into (+) or out of (−) a logic input.

I_{IL} LOGIC "0" INPUT CURRENT – The logic low current flowing into (+) or out of (−) a logic input.

V_{OH} LOGIC "1" OUTPUT VOLTAGE – The logic high output voltage with a specified load.

V_{OL} LOGIC "0" OUTPUT VOLTAGE – The logic low output voltage with a specified load.

I_{OH} LOGIC "1" OUTPUT CURRENT – The logic high output source current.

I_{OL} LOGIC "0" OUTPUT CURRENT – The logic low output source current.

I+ POSITIVE SUPPLY CURRENT – The current required from the $+V_S$ supply.

I− NEGATIVE SUPPLY CURRENT – The current required from the $-V_S$ supply.

PSRR POWER SUPPLY REJECTION RATIO – The ratio of power supply voltage change to the peak-to-peak change in input offset voltage.

AD1317 SWITCHING TERMS (See Figure 3)

t_{PDR} INPUT TO OUTPUT RISING EDGE DELAY – The propagation delay measured from the time VINA/B crosses either VINA or VINB, in a low to high transition, to the time QA and $\overline{QA}$ or QB and $\overline{QB}$ cross, respectively.

t_{PDF} INPUT TO OUTPUT FALLING EDGE DELAY – The propagation delay measured from the time VINA/B crosses either VINA or VINB, in a high to low transition, to the time QA and $\overline{QA}$ or QB and $\overline{QB}$ cross, respectively.

t_S MINIMUM LATCH SET-UP TIME – The minimum time before LE goes high with respect to $\overline{LE}$ that an input signal change must be present in order to be acquired and held at the outputs.

t_H MINIMUM LATCH HOLD TIME – The minimum time after LE goes high with respect to $\overline{LE}$ that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{PW} MINIMUM LATCH ENABLE PULSE WIDTH – The minimum time that LE must be held high with respect to $\overline{LE}$ in order to acquire and hold an input change.

t_{LO} LATCH ENABLE TO OUTPUT DELAY – The time between when LE goes high with respect to $\overline{LE}$ that QA and $\overline{QA}$ or QB and $\overline{QB}$ cross.

t_{ID} INPUT STAGE DISABLE TIME – The time between when $\overline{IE}$ goes high with respect to IE that the input bias currents drop to 10% of their nominal value.

t_{IE} INPUT STAGE ENABLE TIME – The time between when IE goes high with respect to $\overline{IE}$ that the input bias currents rise to 90% of their nominal values.

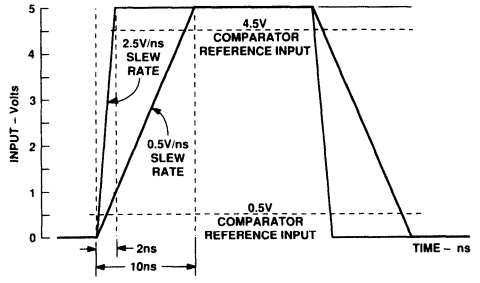


Figure 1. Dispersion Test Input Conditions – 5 V Signal

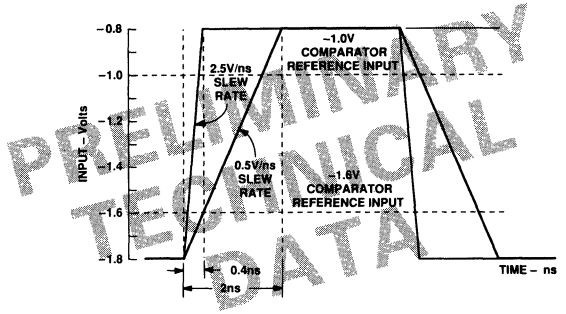


Figure 2. Dispersion Test Input Conditions – 1 V Signal

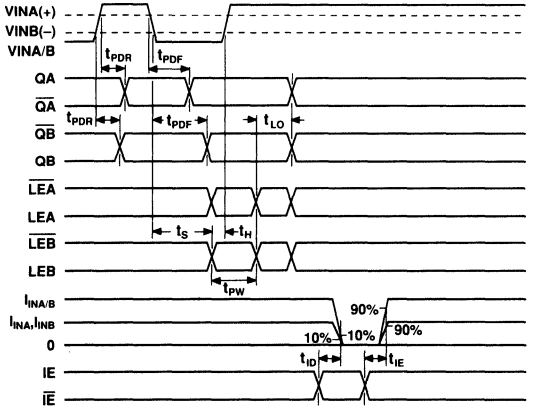


Figure 3. Timing Diagram

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Typical Performance Characteristics

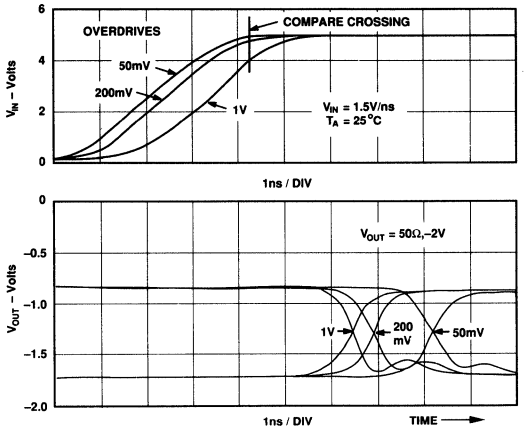


Figure 4. Response to Overdrive Variation – Rising Edge

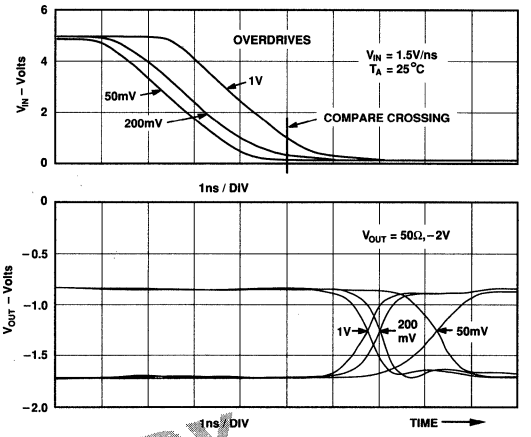


Figure 5. Response to Overdrive Variation – Falling Edge

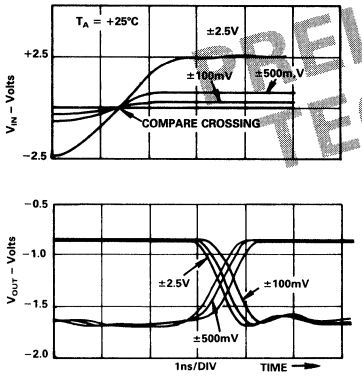


Figure 6. Response to Various Signal Levels – Rising Edge

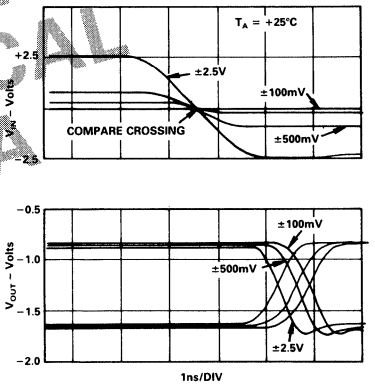


Figure 7. Response to Various Signal Levels – Falling Edge

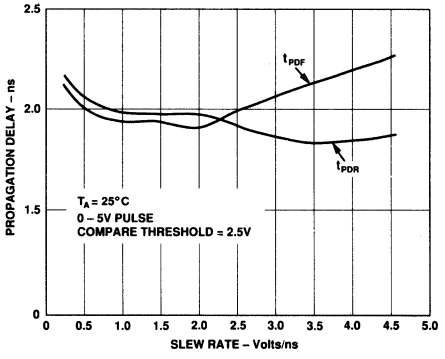


Figure 8. Propagation Delay vs. Slew Rate

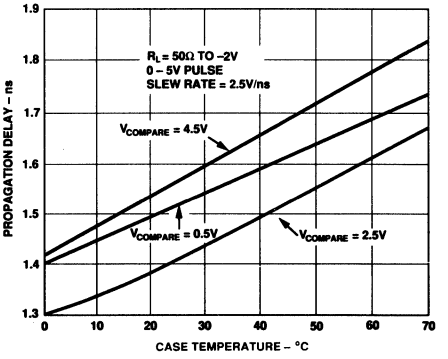


Figure 9. Propagation Delay vs. Temperature – Rising Edge

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

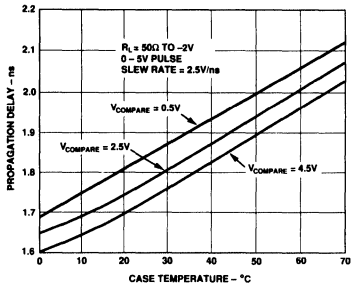


Figure 10. Propagation Delay vs. Temperature – Falling Edge

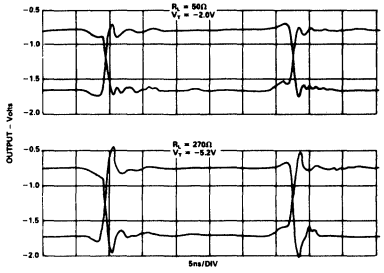


Figure 11. Output Waveform vs. Load

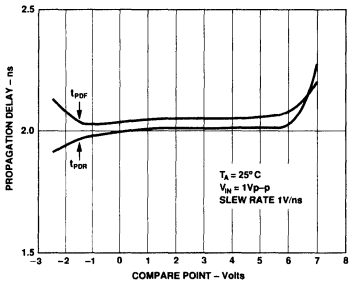


Figure 12. Propagation Delay vs. Common-Mode Voltage

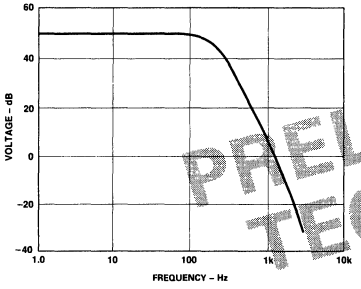


Figure 13. Voltage Gain vs. Frequency

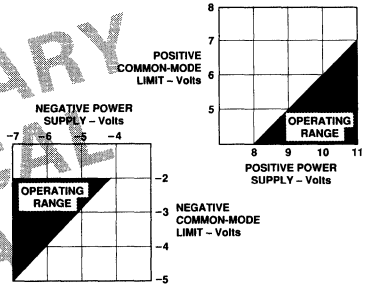


Figure 14. Common-Mode Range vs. Power Supply

10

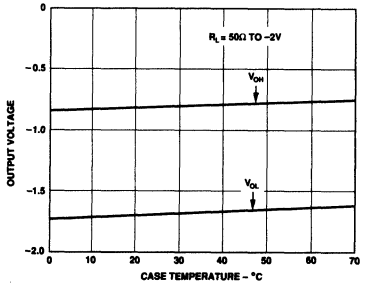


Figure 15. Output Levels vs. Temperature

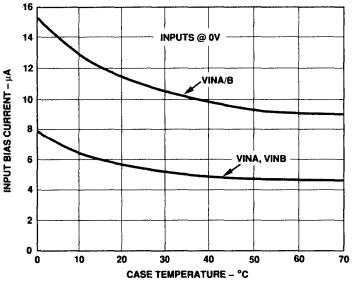


Figure 16. Input Bias Current vs. Temperature

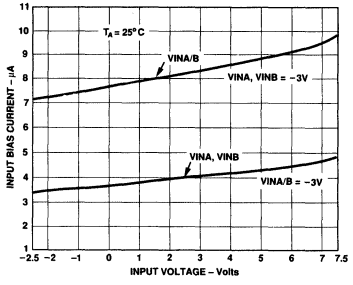


Figure 17. Input Bias Current vs. Input Voltage

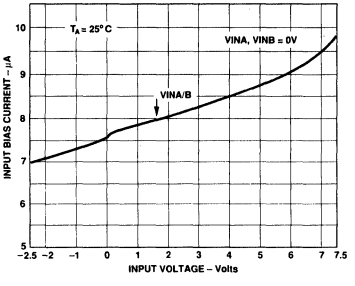


Figure 18. Input Bias Current vs. Input Voltage

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Typical Performance Characteristics

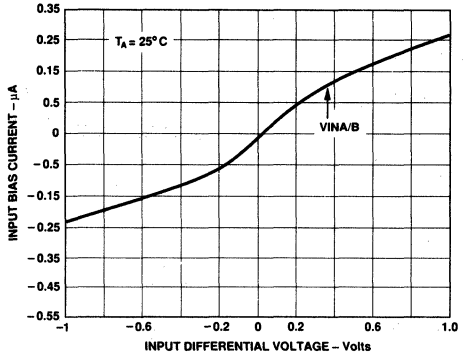


Figure 19. Change in Bias Current vs. Input Differential Voltage (VINA/B – VINA, VINB)

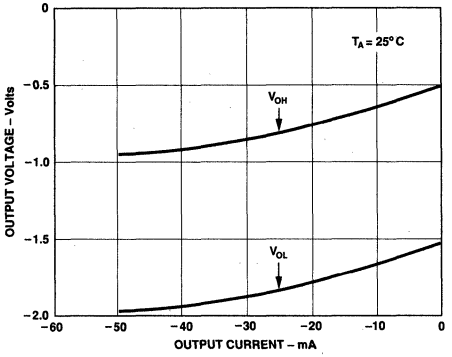


Figure 20. Output Voltage vs. Source Current

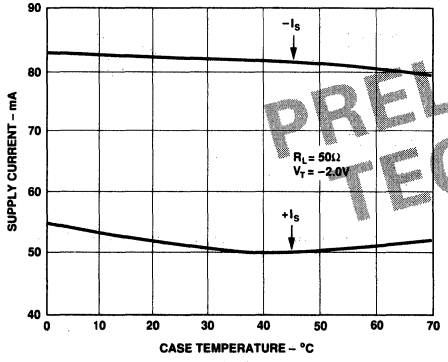


Figure 21. Power Supply Currents vs. Temperature

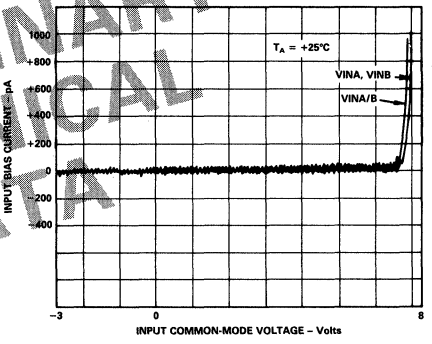


Figure 22. Inhibit Input Bias Current vs. Common-Mode Voltage

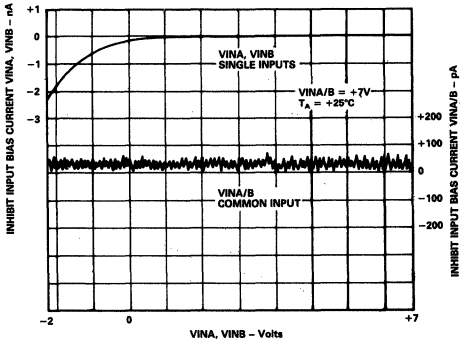


Figure 23. Inhibit Input Bias Current vs. Input Voltage (VINA/B = 7 V)

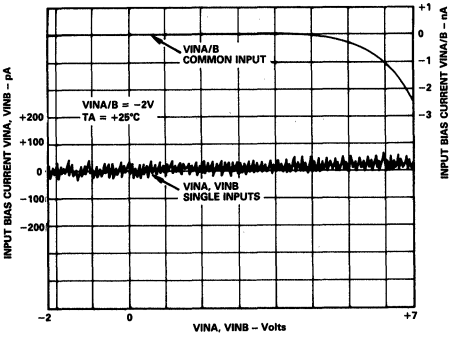


Figure 24. Inhibit Input Bias Current vs. Input Voltage (VINA/B = −2 V)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

FUNCTIONAL DESCRIPTION

The AD1317 is an ultrahigh speed window comparator designed for use in general purpose instrumentation and automatic test equipment. The internal connections for windowing operation keep the capacitance at the critical common input (VINA/B) well below what could normally be obtained using separate input pins.

Another key feature is that the front end circuitry may be disabled, decreasing input bias currents to 50 pA (typical). This enables sensitive dc current testing without having to physically disconnect the AD1317's input from the circuit. The comparator's outputs would normally be latched to maintain absolute logic levels prior to inhibiting the input.

High speed comparators using bipolar process technology usually have input bias currents in the 1 μA to 20 μA range, and the AD1317 is no exception in this regard. This occurs because the input devices usually have low current gain but must be operated at high currents to obtain the widest possible bandwidth. Careful design minimizes variations in the AD1317's bias current with respect to both differential and common-mode input variations. This translates directly to a high equivalent input resistance, the minimum of which occurs with zero differential input. The typical input resistance of the AD1317's common input under this condition is on the order of 4 megohms.

Many ATE applications have required input dividers/buffers to reduce standard logic voltages to levels which can be processed by "687" type comparators. These dividers have also reduced the slew rates at which the comparators must properly function. The AD1317's 9 volt differential and common-mode input ranges and 2.5 V/ns slew rate capability make these buffer circuits unnecessary in most applications.

Separate, complementary latch inputs are provided for each comparator. These may be driven by differential or single-ended sources ranging from ECL to HCMOS logic. When using the comparator's transparent mode, the latch inputs may be tied anywhere within their common-mode range with a maximum differential of 4 V. Symmetrical hysteresis may also be generated by applying a small differential voltage to the latch inputs (see HYSTERESIS).

The AD1317's outputs are standard emitter followers with ECL-compatible voltage swings. The recommended output termination is 50 ohms to −2 V. Larger value termination resistors connected to $-V_S$ may be used, but will reduce edge fidelity. Typical output rise and fall times (20%–80%) are 1 ns with a 50 ohm, 10 pF load. The maximum output source current is 40 mA.

THERMAL CONSIDERATIONS

The AD1317 is provided in a 0.450″ × 0.450″, 16-lead (bottom brazed) gull wing, surface mount package with a typical θ_{JC} (junction-to-case thermal resistance) of 17.5°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1317 in this package is shown in Figure 25. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1, 2].

NOTES
[1]lfm is airflow in linear feet/minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

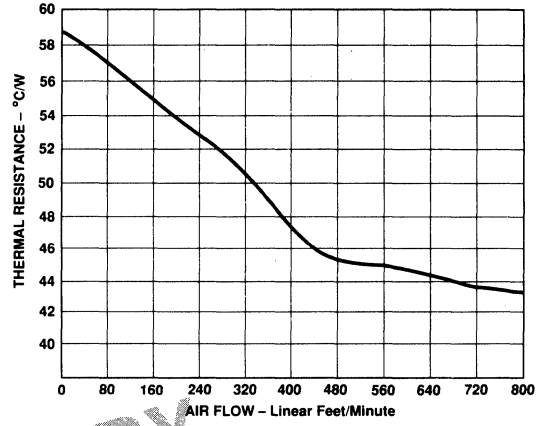


Figure 25. Case-to-Ambient Thermal Resistance vs. Air Flow

DISPERSION

Propagation delay dispersion is the change in device propagation delay which results from changes in the input signal conditions. Dispersion is an indicator of how well the comparator's front-end design balances the conflicting requirements of high gain and wide bandwidth. High gain is needed to ensure that small overdrives will produce valid logic outputs without an increase in propagation delay, while wide bandwidth enables the comparator to handle fast input slew rates. The input signal criteria used to determine the AD1317's dispersion performance are amplitude, overdrive and slew rate for both standard CMOS and ECL signal levels.

HYSTERESIS

The customary technique for introducing hysteresis into a comparator uses positive feedback as shown in Figure 27. The major problems with this approach are that the amount of hysteresis varies with the output logic levels and that the hysteresis is not symmetrical around zero.

The AD1317 does not use this technique. Instead, hysteresis is generated by introducing a differential voltage between LE and $\overline{LE}$ as shown in Figure 28. Hysteresis generated in this manner is independent of output swing and is symmetrical around zero. The variation of hysteresis with input voltage is shown in Figure 29; the useful hysteresis range is about 20 mV.

LAYOUT CONSIDERATIONS

Like any high speed device, the AD1317 requires careful layout and bypassing to obtain optimum performance. Oscillations are generally caused by coupling from an output to the high impedance inputs. All drive impedances should be as low as possible, and lead lengths should be minimized. A ground plane should be used to provide low impedance return paths. Care should be taken in selecting sockets for incoming or other testing to minimize lead inductance, and sockets are not recommended for production use.

Output wire lengths should be kept below one inch. Longer connections require the use of transmission line techniques to prevent ringing and reflections. Lines should be terminated with their characteristic impedance to −2 V. Thevenin-equivalent termination to $-V_S$ is also possible.

High quality RF capacitors should be used for power supply bypassing. These should be located as closely as possible to the AD1317's power pins and connections to the ground plane should have the minimum possible length. Both $+V_S$ and $-V_S$ must be bypassed with 470 pF capacitors located within 0.25 inches of the device's supply pins. In addition, each supply should be bypassed with 0.1 μF ceramic and 10 μF tantalum capacitors. Low impedance power distribution techniques will make the locations of these components less critical. Adding 470 pF capacitors at the VINA and VINB inputs, as close as possible to the package, will improve circuit performance and noise immunity in dc-compare applications.

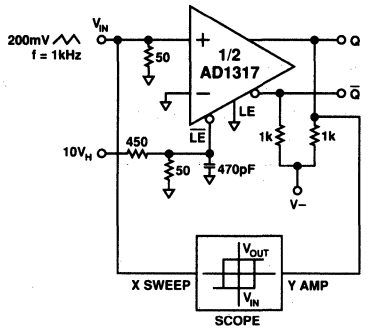


Figure 28. AD1317 Comparator Hysteresis Test Setup

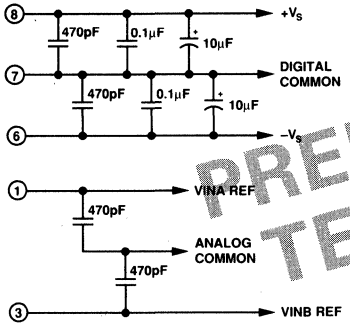


Figure 26. AD1317 Basic Circuit Decoupling

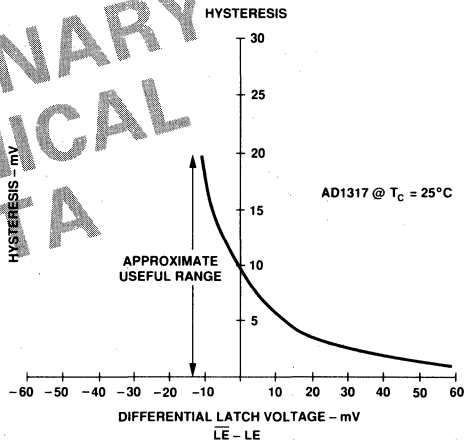
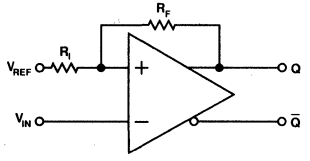


Figure 29. AD1317 Typical Hysteresis Curve



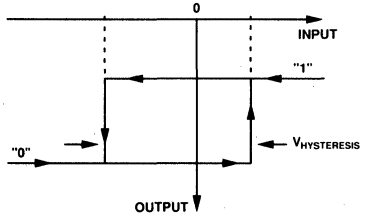


Figure 27. Typical Comparator Hysteresis

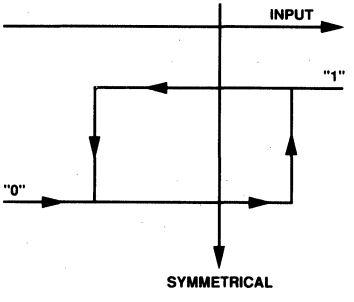


Figure 30. AD1317 Hysteresis

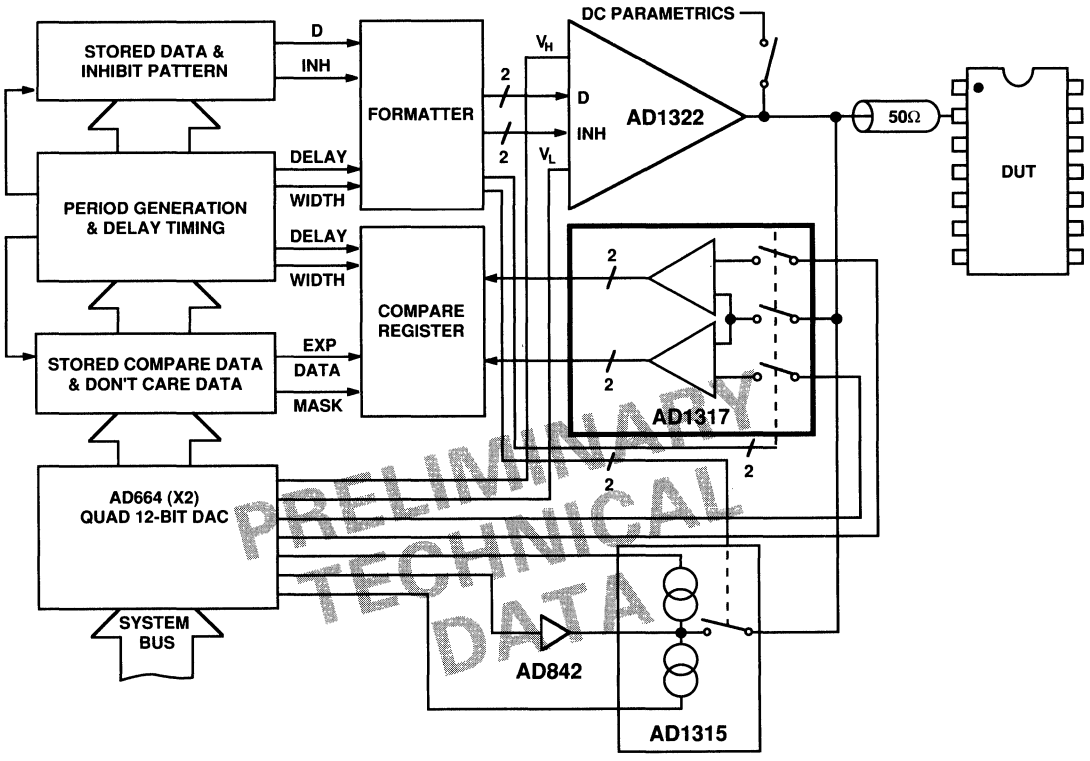


Figure 31. High Speed Digital List System Block Diagram

10

High Speed Pin Driver with Inhibit Mode

AD1321

FEATURES
100 MHz Driver Operation
Driver Inhibit Function
250 ps Edge Matching
Guaranteed Industry Specifications
50 Ω Output Impedance
1 V/ns Slew Rate
Variable Output Voltages for ECL, TTL and CMOS
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation & Characterization Equipment

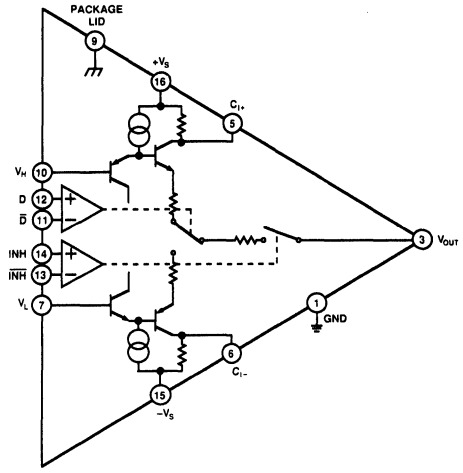
PRODUCT DESCRIPTION

The AD1321 is a complete high speed pin driver designed for use in digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities and long term reliability in an ultrasmall 16-lead, hermetically sealed (gull wing) package.

Featuring unity gain programmable output levels of −2 V to +7 V with output swing capability of less than 100 mV to 9 V, the AD1321 is designed to stimulate ECL, TTL and CMOS logic families. The 100 MHz (5.0 ns pulsewidth) data rate capacity, 1 V/ns slew rate, and matched output impedance allows for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (inhibit mode) electrically removing the driver from the path through the inhibit mode feature. The pin driver leakage current in inhibit is typically 50 nA, and output charge transfer entering inhibit is typically less than 15 pC.

The AD1321 transition from HI/LO or to inhibit is controlled through the data and inhibit inputs. The input circuitry is implemented utilizing high speed differential inputs with a common mode range of 3 volts. This allows for direct interface to

AD1321 FUNCTIONAL BLOCK DIAGRAM



the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic HI/LO inputs are equally easy to interface. Typically requiring 350 μA of bias current, the AD1321 can be directly coupled to the output of a digital-to-analog converter.

The 150 MHz analog bandwidth of the logic HI/LO inputs allows for four quadrant multiplying providing maximum flexibility as a standard pin driver and a waveform generator all in one package.

The AD1321 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0 to +70°C.

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SPECIFICATIONS (All measurements made in free air at +25°C. Output load 10 kΩ/6 pF with $+V_S$ = +10 V, $-V_S$ = −5.2 V unless otherwise specified)

Parameter	AD1321KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Input Voltage	−2.0		+7.0	Volts	
Differential Input Range	0.4	ECL	3.0	Volts	
Bias Current		175	300	μA	
REFERENCE INPUTS					See Note 1
V_{HIGH} Range (V_H)	−2.5		+7.5	Volts	
V_{LOW} Range (V_L)	−2.5		+7.5	Volts	
V_{HIGH} Bias Currents (V_H)		0.5	1.2	mA	
V_{LOW} Bias Currents (V_L)		0.3	0.5	mA	
Input Bandwidth		150		MHz	See Figure 9
OUTPUT CHARACTERISTICS					See Notes 1, 2
Logic High Range	−2.0		+7.0	Volts	
Logic Low Range	−2.0		+7.0	Volts	
Amplitude [V_H−V_L]	0.1		+9.0	Volts	
Accuracy					See Figure 1
Initial Offset	−50.0		+50.0	mV	
Gain Error	−4.5	−2.5	−0.5	% of Set Level	See Note 3
Linearity Error					
0 V to +5.5 V	−0.5		+0.5	% of Set Level	
−2 V to +7 V	−1.0		+1.0	% of Set Level	
Output Voltage TC		0.5		mV/°C	See Figures 7 & 8
Current Drive					
Static	30.0			mA	
Dynamic	100.0			mA	See Note 4
Current Limit			85	mA	
Output Impedance	48.5	50.0	51.5	ohms	See Note 5
DYNAMIC PERFORMANCE					
Driver Mode					See Note 6
Delay Time	0.8	1.2	1.6	ns	See Figure 2
Prop Delay TC		2.0		ps/°C	See Figure 4
Delay Time Matching					
Edge-to-Edge	−250	±80	+250	ps	See Figure 5
Rise & Fall Times					See Figure 10
1 V Swing		0.9	1.2	ns	Measurement 20%–80%
3 V Swing		2.7	3.0	ns	Measurement 10%–90%
5 V Swing		4.0	4.4	ns	Measurement 10%–90%
Large Signal Slew	0.8	1.1		V/ns	Measurement 20%–80% of 9 V Swing
Toggle Rate	100			MHz	ECL Output
Minimum PW, V_{OUT} = 2 V		5.0		ns	See Figure 12
Overshoot & Preshoot	−(3% V_O+50)		+(3% V_O+50)	mV	See Figure 3, Note 7
Settling Time					See Figure 3, Note 7
to ±1% V_O			15	ns	
Delay Time vs. PW		150		ps	See Note 8; See Figure 6

Parameter	AD1321KZ Min	Typ	Max	Units	Comments
DYNAMIC PERFORMANCE					
Inhibit Mode					See Figure 2
Delay Time					See Note 9
Drive-to-Inhibit	1.1		1.7	ns	
Inhibit-to-Drive	1.6		2.2	ns	
Edge-to-Edge Matching	−250	±100	+250	ps	
Overshoot & Preshoot		40	80	mV	See Figure 3
Output Capacitance		8	10	pF	
Output Charge Going into Inhibit Mode		15		pC	See Figure 13
Leakage Current in Inhibit Mode					
−2 V to +5 V		50	200	nA	
+5 V to +7 V			1.0	μA	
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range			15.2	Volts	
Supply Range					See Note 10
Positive Supply	+8.0	+10.0	+12.0	Volts	
Negative Supply	−7.2	−5.2	−3.2	Volts	
Current					
Positive Supply	42	60	78	mA	
Negative Supply	−78	−60	−42	mA	
+PSRR V_{OH} = +7 V	0.5		0.5	%/%V_{OUT}	+V = ±2.5%
−PSRR V_{OL} = −2 V	0.5		0.5	%/%V_{OUT}	−V = ±2.5%

NOTES

[1]The output voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different values of V_{OUT} such as 0 V to +9 V as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

[2]V_H can be set to be as much as 4 volts below V_L without any harm to the driver with the restriction that neither level can go below −2 V with the typical power supply setting. In this condition the rise and fall times will approximately double.

[3]The gain error of the driver is always in the negative direction with respect to the voltage set level.

[4]Transient output current can easily exceed the AD1321's steady-state current limit when driving capacitive loads. The transient output current capability can be increased by connecting 0.039 μF capacitors between Pin 5 and ground and Pin 6 and ground. This will prevent the driver from current limiting by providing the "edge" current necessary when driving capacitive loads. These capacitors will not affect the driver's dc current limit.

[5]Driver output impedance is 50 ohms, ±1.5 ohms for a 3 V swing into a 50 ohm cable.

[6]Delay times are measured from the crossing of differential ECL outputs at the inputs to the driver to the 50% point of an ±400 mV driver output.

[7]Due to uncontrolled inductances in the test socket, overshoot, preshoot and settling time cannot be 100% tested. These characteristics are guaranteed by characterization data instead.

[8]Delay matching vs. PW is defined as the amount of change in propagation, with respect to the leading edge, due to change in pulsewidth of the input signal. The AD1321 is characterized over the pulsewidth range of 5 ns to 100 ns.

[9]Inhibit mode delay times are measured from the crossing of differential (ECL) INH inputs to a 200 mV transition at the pin driver output. V_{OUT} is connected to a 100 ohm/15 pF load terminated to ground. V_{OH} is set at +1 V and V_{OL} is set at −1 V for this test.

[10]A supply range of 15.2 V must be maintained to guarantee a 9 V output swing.

Specifications subject to change without notice.

10

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- $+V_S$ to GND . . . . . +13 V
- $-V_S$ to GND . . . . . −8.2 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from D to $\overline{D}$ . . . . . 5 V
- Difference from INH to $\overline{INH}$ . . . . . 5 V
- D, $\overline{D}$, INH, $\overline{INH}$ . . . . . $+V_S$ −12 V, $-V_S$ +11.5 V
- V_H to V_L . . . . . −4 V, +9 V
- V_H, V_L . . . . . $+V_S$ −13.0 V, $-V_S$ +13.2 V

Driver Output
- Voltage . . . . . $+V_S$ −13.0 V, $-V_S$ +13.2 V
- Short Circuit to GND . . . . . Indefinite

Operating Temperature Range . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 20 sec)† . . . . . +300°C

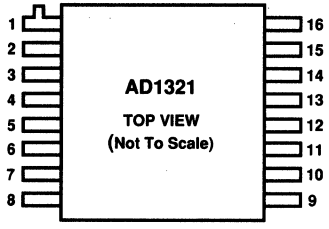
NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

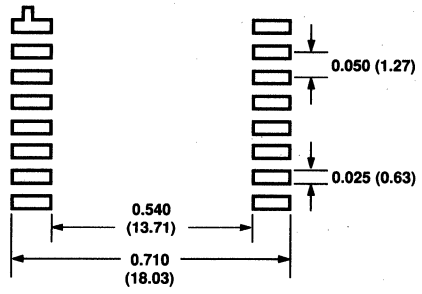
†To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).



SUGGESTED LANDING PADS LOCATION



PIN CONFIGURATION

PIN NO.	SYMBOL	FUNCTION
1	GND	CIRCUIT GROUND
2	N/C	NO CONNECTION
3	V_{OUT}	DRIVER OUTPUT
4	N/C	NO CONNECTION
5	C_{I+}	POSITIVE DECOUPLE
6	C_{I-}	NEGATIVE DECOUPLE
7	V_L	VOLTAGE LOGIC LOW
8	N/C	NO CONNECTION
9	LID	LID CONNECTION*
10	V_H	VOLTAGE LOGIC HIGH
11	$\overline{D}$	DRIVER INPUT
12	D	DRIVER INPUT
13	$\overline{INH}$	INHIBIT INPUT
14	INH	INHIBIT INPUT
15	$-V_S$	NEGATIVE SUPPLY
16	$+V_S$	POSITIVE SUPPLY

*IT IS RECOMMENDED TO CONNECT PIN 9 TO CIRCUIT GROUND.

ORDERING GUIDE*

Model	Temperature Range	Package Option
AD1321KZ	0 to +70°C	16-Lead Gull Wing (Z-16A)

*See Section 20 for package outline information.

OFFSET ERROR

The offset error for logic high is determined by holding the output of the driver at logic high, and applying zero volts to the logic high reference input. The driver output value represents the offset "high" error. The same approach is used to identify offset "low" error

$$V_{HIGH\ OFFSET} = V_{OUT}$$

where:

V_H = 0 V
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH.

GAIN ERROR

Defined as the ratio of the driver's output voltage to its logic set level voltage and is expressed in terms of percent of set level. The gain error is typically seen as 2.5% and is always in the negative direction with respect to the logic set level

$$V_{HIGH\ GAIN}\ (\%) = \frac{V_{OUT} - V_H - V_{HIGH\ OFFSET}}{V_H} \times 100$$

where:

V_H = 5.0 V+$V_{HIGH\ OFFSET}$
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH.

LINEARITY ERROR

The deviation of the transfer function from a reference line. For the AD1321, the linearity error is calculated by subtracting the worst case gain error from the best case gain error (for the specified range) and divide the result by two. This method guarantees that the maximum linearity error for any set level within the specified range will be within the specified limits

where:

$$V_{HIGH\ LINEARITY}\ (\%) = \frac{V_{HIGH\ GAIN}\ (max) - V_{HIGH\ GAIN}\ (min)}{2} \times 100.$$

DELAY TIME

The amount of time it takes the input signal to propagate through the driver and be converted to the desired logic levels. The measurement technique is defined in the notes and is shown in Figure 2.

EDGE-TO-EDGE MATCHING

Edge-to-edge matching is the difference, in time, between the delay time of the rising edge and the falling edge.

MINIMUM PULSEWIDTH

Defined as the smallest pulse applied to the input of the driver which can maintain an output signal amplitude of 2 V. The minimum pulsewidth is measured at the 50% points of the waveform.

OVERSHOOT AND PRESHOOT

The amount by which the driver's output voltage exceeds the desired set voltage. Preshoot is similar to overshoot but is the amount by which the driver's output goes below the initial voltage when driving to the new set level (or inhibit mode). See Figure 3.

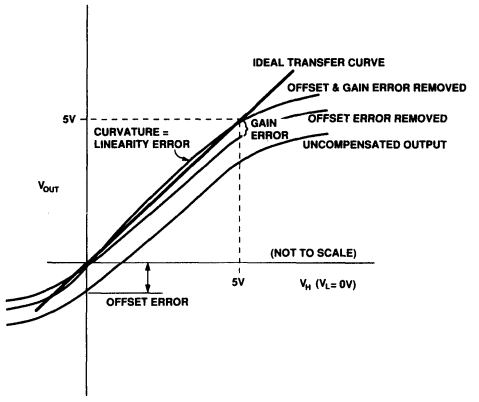


Figure 1. Definition of Terms

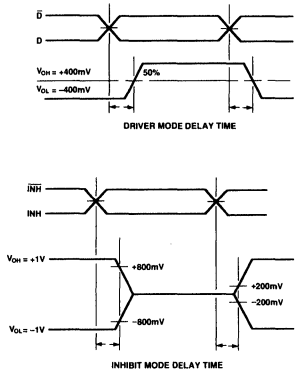


Figure 2. Timing Diagram for Driver and Inhibit Propagation Delay

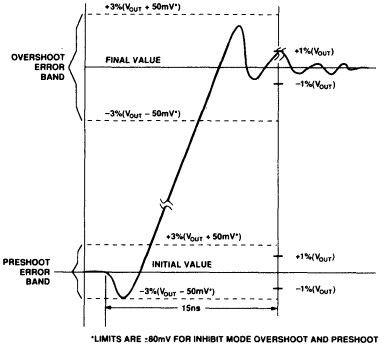


Figure 3. Definition of Waveform Abberations

Typical Performance Characteristics

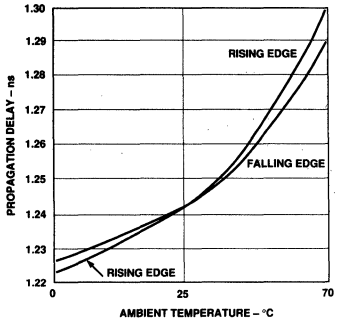


Figure 4. Driver Propagation Delay vs. Temperature

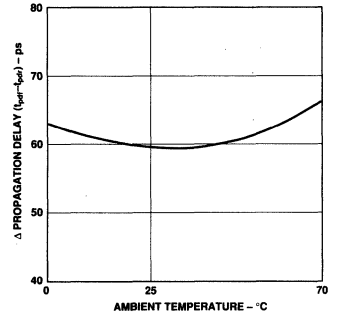


Figure 5. Propagation Delay Edge Matching vs. Temperature

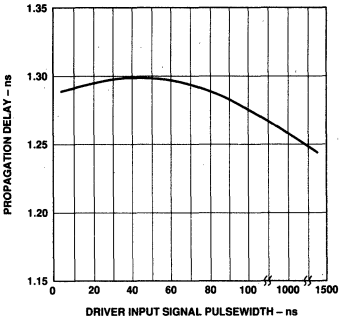


Figure 6. Propagation Delay vs. Input Signal Pulsewidth

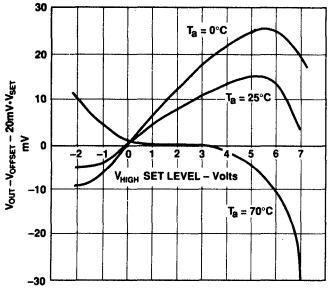


Figure 7. Change in V_{HIGH} over Temperature

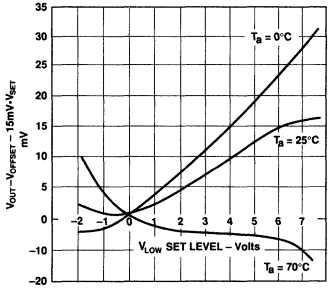


Figure 8. Change in V_{LOW} over Temperature

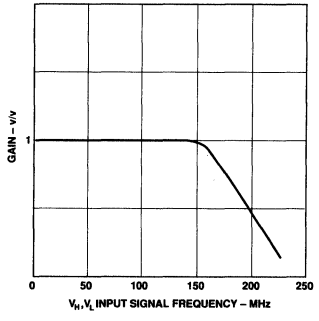


Figure 9. V_{HIGH} , V_{LOW} Input Bandwidth

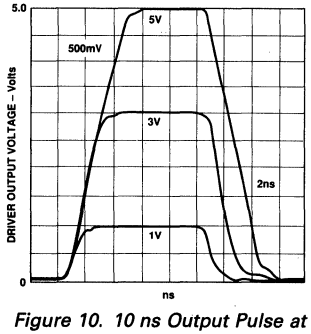


Figure 10. 10 ns Output Pulse at 1 V, 3 V and 5 V

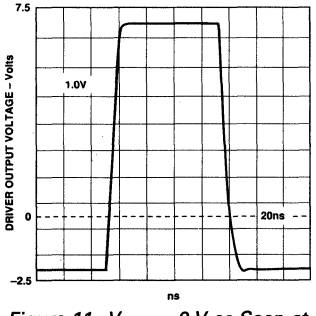


Figure 11. V_{OUT} = 9 V as Seen at the End of a 28", 50 Ω Cable

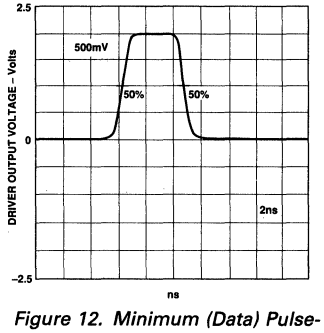


Figure 12. Minimum (Data) Pulsewidth as Defined by V_{OUT} = 2 V, 50% Crossing ≤ 5 ns

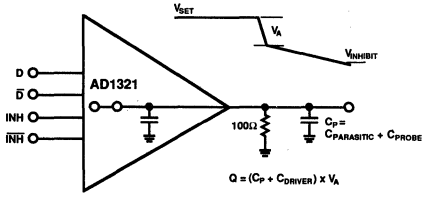


Figure 13. Charge into Inhibit Test Setup

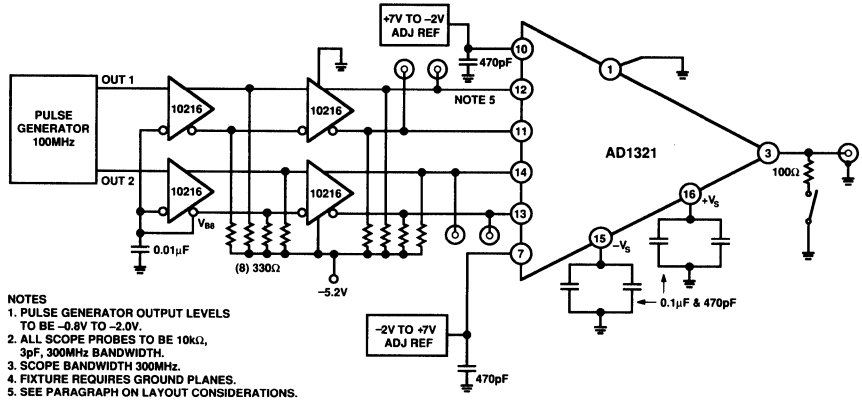


Figure 14. AD1321 Test Setup

FUNCTIONAL DESCRIPTION

The AD1321 is a complete high speed pin driver designed for use in general purpose instrumentation and digital functional test equipment. The purpose of a pin driver is to accept digital, analog and timing information from a system source and combine these to drive the device to be tested.

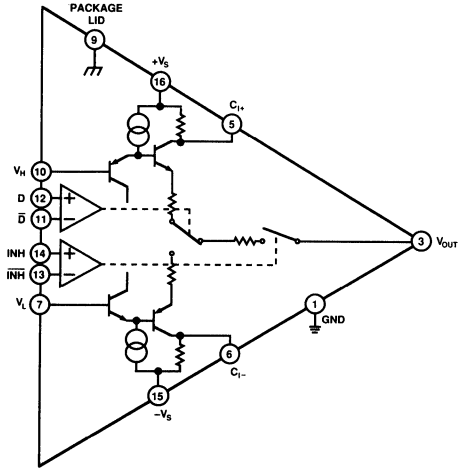


Figure 15. AD1321 Block Diagram

The circuit configuration for the AD1321 is outlined in Figure 15. Simply stated, a pin driver performs the function of a precise, high speed level translator with an output which can be disabled. The AD1321 accepts differential digital information utilizing a high speed differential design on the D and INH inputs providing precise timing at logic crossover and high noise immunity. The wide input voltage range allows for ECL operation with power supplies at 0 to −5.2 V, +2 V to −3.2 V or +5 V to 0 V. Where timing is less critical, TTL or CMOS logic levels may be used to toggle the AD1321. By biasing the D and INH inputs to approximately +1.3 V for TTL and 1/2 V_{CC} for CMOS, the D and INH inputs can be directly driven from these single-ended output sources. The output of the pin driver will follow the logic state of the D input providing the INH input is low. When inhibit is asserted, the output is disconnected and any activity on the input does not affect the output.

Analog information is provided to the pin driver through the V_H and V_L terminals as reference voltages. These analog voltages are buffered internally using unity gain followers. The resulting gain and linearity errors are provided in the specification table. System timing requirements are achieved through a specified 1.2 ns, ±400 ps driver propagation delay, 1.0 V/ns slew rate, defined preshoot and overshoot, and a dynamically trimmed 50 Ω output impedance.

10

LAYOUT CONSIDERATIONS

While it is generally considered good engineering practice to capacitively decouple the power supplies of an active device, it is absolutely essential for a high power, high speed device such as the AD1321. The engineer merely has to consider the current pulse demand from the power supply when a dynamic current change of −100 mA to +100 mA is required in only a few nanoseconds. Therefore, a 470 pF high frequency decoupling capacitor must be located within 0.25 inches of the $+V_S$ and $-V_S$ terminals to a low impedance ground. A 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor should also be situated between the power supplies and ground however, the proximity to the device is less critical assuming low impedance power supply distribution techniques are employed. Circuit performance will be similarly enhanced and noise minimized by locating a 470 pF capacitor as close as possible to V_H, V_L and connected to ground. Bypass considerations have been summarized in Figure 16.

An equally important consideration is the use of microwave stripline techniques on the output of the AD1321. Failure to preserve the 50 Ω output impedance of the pin driver will result in unwanted reflections, ringing and general corruption of the wave shape. Care should be exercised when selecting etch widths and routing, wire and cable to the device to be tested, and in choosing relays if they are required.

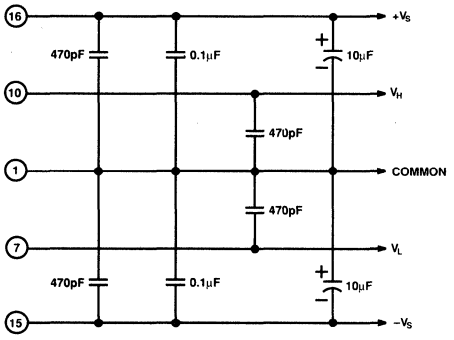


Figure 16. Basic Circuit Decoupling

THERMAL CONSIDERATIONS

The AD1321 is provided in a 0.450″ × 0.450″, 16-lead (bottom brazed) gull wing, surface mount package with a typical junction-to-case thermal resistance of 5.6°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1321 in this package is shown in Figure 17. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1,2].

NOTES

[1]lfm is air flow in Linear Feet/Minute.

[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

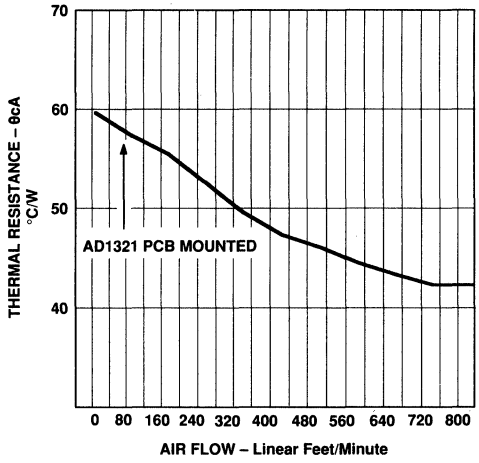


Figure 17. Case-to-Ambient Thermal Resistance vs. Air Flow

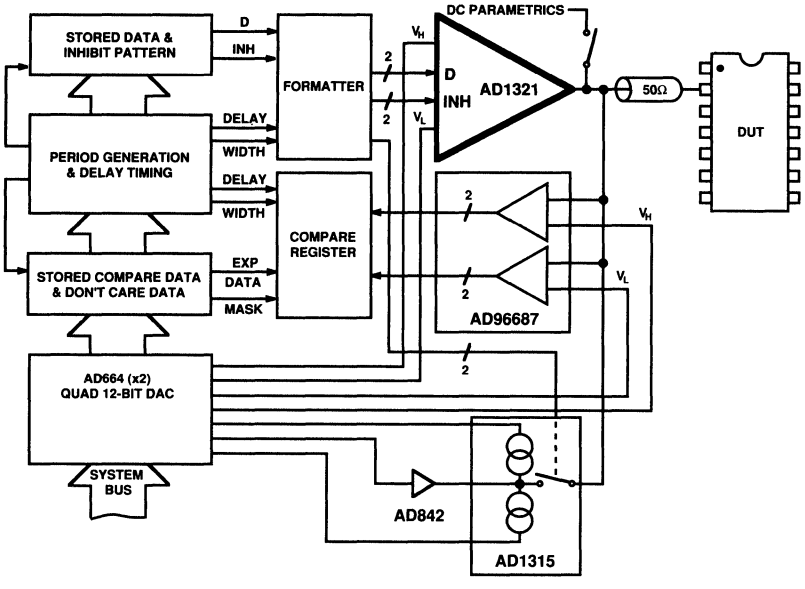
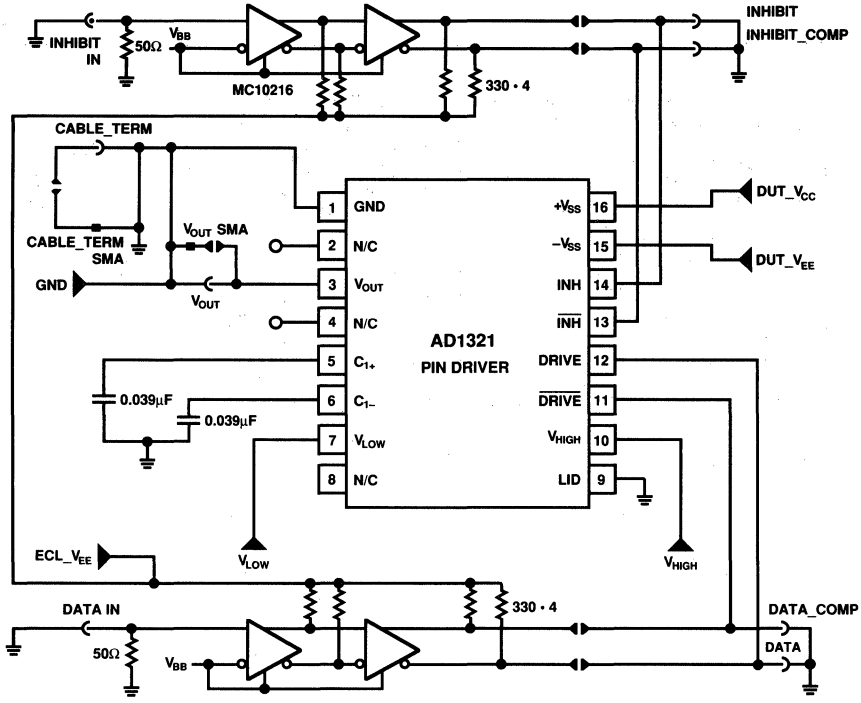


Figure 18. High Speed Digital Test System Block Diagram

APPLICATIONS

The AD1321 has been optimized to function as a pin driver in an ATE test system. Shown in Figure 18 is a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1321 pin driver, AD96687 high speed dual comparator, AD1315 active load, and the AD664 quad 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 100 MHz in a data mode or 50 MHz in the I/O mode, yet fit into a neat trim package.



NOTES:
"HALF-MOON" CONNECTORS CAN BE CONNECTED OR DISCONNECTED AS REQUIRED . . . ◖◗
DECOUPLING CAPS ARE NOT SHOWN ON THIS SCHEMATIC, BUT THE BOARD USES 0.1µF AND 470pF CAPS TO DECOUPLE THE V_{CC}, V_{EE}, V_{LOW} AND V_{HIGH} SUPPLIES.
SMA CONNECTORS ■
PROBE JACKS)
BNC CONNECTORS (

Figure 19. AD1321EB Evaluation Board Schematic

AD1321 EVALUATION BOARD

Introduction

The AD1321EB evaluation board was developed to aid the customer in quickly evaluating the performance of the AD1321. Included is complete documentation of the evaluation board along with suggestions on equipment to use and measurement limitations.

Overview

The AD1321 is a high speed pin driver used in automatic test equipment

The device has true differential inputs for both the drive and inhibit which can be driven from either TTL or ECL logic levels (ECL is recommended). Standard ECL design and layout techniques should be used.

The device runs from dual power supplies +10 V and −5.2 V. It is very important that these power supplies are decoupled properly at the device pin. (High frequency oscillations will couple through to the device output.)

The reference input pins are dc inputs; therefore they also should be decoupled properly. The reference input range is −2 V to +7 V.

The output slew rate is 1 V/ns for large signals and has a rep rate for an ECL level of 100 MHz minimum.

Equipment

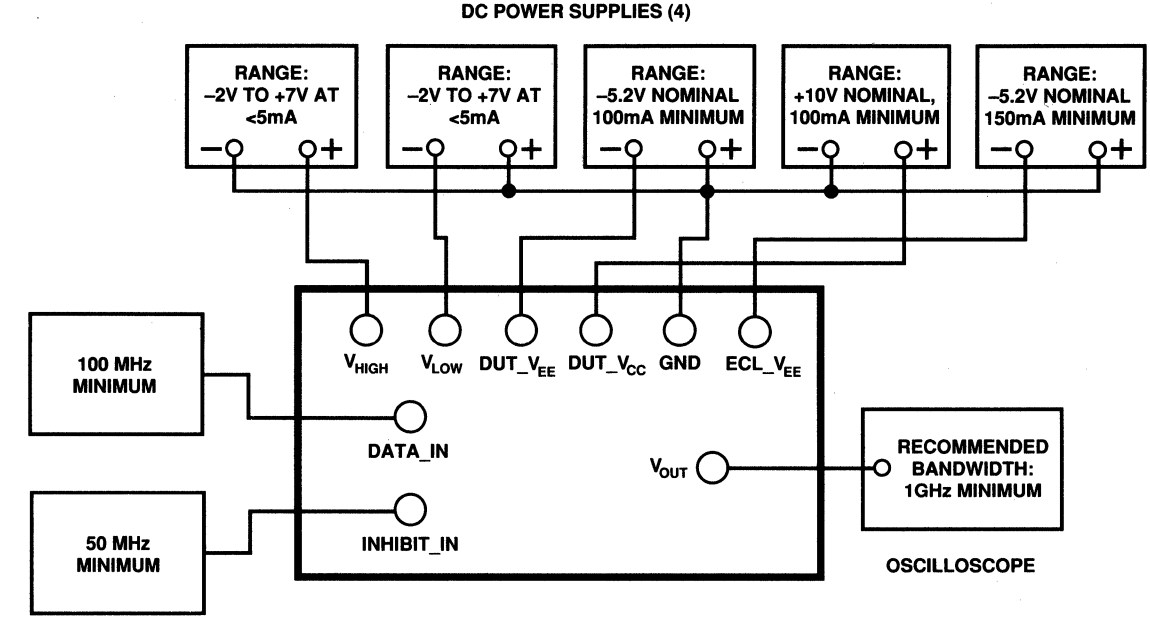
The Drive and Inhibit inputs should be driven with standard ECL levels. If the full performance of the AD1321 needs to be evaluated, the generator must be able to supply an ECL level at frequencies greater than 200 MHz. Motorola's MC10216 is used on the evaluation board to simulate the actual application. V_{BB} is used on the MC10216 as the logic reference and the outputs have 330 ohm pulldowns to V_{EE}.

Five power supplies are required: DUT_V_{CC}, DUT_V_{EE}, V_{HIGH}, V_{LOW} and ECL_V_{EE}. DUT_V_{CC} requires +10 V at 100 mA minimum; DUT_V_{EE} requires −5.2 V at 100 mA minimum; ECL_V_{EE} requires −5.2 V at 150 mA minimum. V_{HIGH} and V_{LOW} require −2 V to +7 V at 5 mA (each).

The output performance of the pin driver can only be measured properly with a scope which has the proper bandwidth for the required application. The input impedance and the bandwidth of the scope probe should be taken into consideration when evaluating the performance of the device. The resultant bandwidth of the system is the RMS value of the components in the system.

The characterizations performed by Analog Devices were performed using the following equipment: the scope equipment consists of the Tektronix 11402 mainframe (1 GHz BW), P6203 FET probe (1 GHz, 1.2 pF, 1 M ohm) and the 11A71 plug-in (1 GHz BW, 50 ohm).

The Hewlett-Packard 54120 and 54110 were also evaluated with the 500 ohm, 1.2 pF passive probes and the Data Precision 6100 with their model 640 FET probe (50 kΩ, 4 pF). When measuring the performance of waveforms close to or exceeding the bandwidth of a scope, it is not uncommon for the results between scopes to be different because of aberrations and slew rates.



CONNECTORS ON AD1321 EVALUATION BOARD:

1. **DC POWER SUPPLIES: FEMALE BANANA JACKS**
2. **PULSE GENERATORS: FEMALE BNC CONNECTORS**
3. **OSCILLOSCOPE: FEMALE PROBE SOCKET (TEKTRONIX p/n: 131–0258–00)**

Figure 20. AD1321 Evaluation Board Connections

Ultrahigh Speed Pin Driver with Inhibit Mode

AD1322

FEATURES
200 MHz Driver Operation
Driver Inhibit Function
200 ps Edge Matching
Guaranteed Industry Specifications
50 Ω Output Impedance
2 V/ns Slew Rate
Variable Output Voltages for ECL, TTL and CMOS
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation & Characterization Equipment

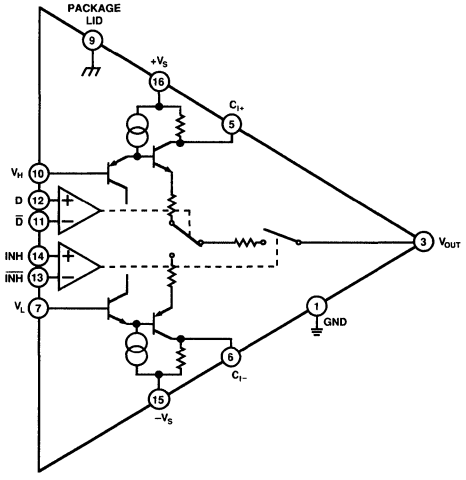
PRODUCT DESCRIPTION

The AD1322 is a complete high speed pin driver designed for use in digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities and long term reliability in an ultrasmall 16-lead, hermetically sealed (gull wing) package.

Featuring unity gain programmable output levels of −2 V to +7 V with output swing capability of less than 100 mV to 9 V, the AD1322 is designed to stimulate ECL, TTL and CMOS logic families. The 200 MHz (2.5 ns pulsewidth) data rate capacity, and matched output impedance allows for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (inhibit mode) electrically removing the driver from the path, through the inhibit mode feature. The pin driver leakage current in inhibit is typically 50 nA, and output charge transfer entering inhibit is typically less than 15 pC.

The AD1322 transition from HI/LO or to inhibit is controlled through the data and inhibit inputs. The input circuitry is implemented utilizing high speed differential inputs with a common-mode range of 3 volts. This allows for direct interface to

AD1322 FUNCTIONAL BLOCK DIAGRAM



the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic HI/LO inputs are equally easy to interface. Typically requiring 350 μA of bias current, the AD1322 can be directly coupled to the output of a digital-to-analog converter.

The 200 MHz analog bandwidth of the logic HI/LO inputs allows for four quadrant multiplying providing maximum flexibility as a standard pin driver and a waveform generator all in one package.

The AD1322 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0 to +70°C.

10

SPECIFICATIONS (All measurements made in free air at +25°C. Output load 10 kΩ/6 pF with $+V_S$ = +10 V, $-V_S$ = −5.2 V unless otherwise specified)

Parameter	AD1322KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Input Voltage	−2.0		+7.0	Volts	
Differential Input Range	0.4	ECL	3.0	Volts	
Bias Current		175	300	μA	
REFERENCE INPUTS					See Note 1
V_{HIGH} Range (V_H)	−2.5		+7.5	Volts	
V_{LOW} Range (V_L)	−2.5		+7.5	Volts	
V_{HIGH} Bias Currents (V_H)		0.5	1.2	mA	
V_{LOW} Bias Currents (V_L)		0.3	0.5	mA	
Input Bandwidth		200		MHz	See Figure 9
OUTPUT CHARACTERISTICS					See Notes 1, 2
Logic High Range	−2.0		+7.0	Volts	
Logic Low Range	−2.0		+7.0	Volts	
Amplitude [V_H−V_L]	0.1		+9.0	Volts	
Accuracy					See Figure 1
Initial Offset					See Note 3
V_H	+320	+350	+380	mV	
V_L	−180	−150	−120	mV	
Gain Error	−4.5	−2.5	−0.5	% of Set Level	See Note 4
Linearity Error					
0 V to +5.5 V	−0.5		+0.5	% of Set Level	
−2 V to +7 V	−1.0		+1.0	% of Set Level	
Output Voltage TC		0.5		mV/°C	See Figures 7 & 8
Current Drive					
Static	30.0			mA	
Dynamic	100.0			mA	See Note 5
Current Limit			85	mA	
Output Impedance	48.5	50.0	51.5	ohms	See Note 6
DYNAMIC PERFORMANCE					
Driver Mode					See Note 7
Delay Time	0.9	1.2	1.5	ns	See Figure 2
Prop Delay TC		2.0		ps/°C	See Figure 4
Delay Time Matching					
Edge-to-Edge	−200	±50	+200	ps	See Figure 5
Rise & Fall Times					See Figure 10
1 V Swing		0.5	0.9	ns	Measurement 20%–80%
3 V Swing		1.8	2.2	ns	Measurement 10%–90%
5 V Swing		3.1	3.5	ns	Measurement 10%–90%
Large Signal Slew	1.0	1.3		V/ns	Measurement 20%–80% at a 9 V Swing
Toggle Rate	200			MHz	ECL output
Minimum PW, V_{OUT} = 2 V		2.0		ns	See Figure 12
Overshoot & Preshoot	−(3% V_O +50)		+(3%V_O +50)	mV	See Figure 3, Note 8
Settling Time					See Figure 3, Note 8
to ±1% V_O			15	ns	
Delay Time vs. PW		100		ps	See Note 9, See Figure 6

Parameter	AD1322KZ Min	Typ	Max	Units	Comments
DYNAMIC PERFORMANCE					
Inhibit Mode					See Figure 2
Delay Time				ns	See Note 10
Drive-to-Inhibit	0.9		1.7	ns	
Inhibit-to-Drive	1.3		1.9	ns	
Delay Time Matching					
Edge-to-Edge	−200	±50	+200	ps	
Overshoot & Preshoot		40	80	mV	See Figure 3
Output Capacitance		8	10	pF	
Output Charge Going into Inhibit Mode		15		pC	See Figure 13
Leakage Current in Inhibit Mode					
−2 V to +5 V		50	200	nA	
+5 V to +7 V			1.0	μA	
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range			15.2	Volts	
Supply Range					See Note 11
Positive Supply	+8.0	+10.0	+12.0	Volts	
Negative Supply	−7.2	−5.2	−3.2	Volts	
Current					
Positive Supply	4.2	60	78	mA	
Negative Supply	−78	−60	−42	mA	
+PSRR V_{OH} = +7 V	0.5		0.5	%/%V_{OUT}	+V = ±2.5%
−PSRR V_{OL} = −2 V	0.5		0.5	%/%V_{OUT}	−V = ±2.5%

NOTES

[1]The output voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different values of V_{OUT} such as 0 V to +9 V as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

[2]V_H can be set to be as much as 4 volts below V_L without any harm to the driver with the restriction that neither level can go below −2 V with the typical power supply setting. In this condition the rise and fall times will approximately double.

[3]All pin drivers are pretrimmed at the factory to incorporate an offset error of +350 mV, ±30 mV for V_H and −150 mV, ±30 mV for V_L. For V_H and V_L the offset error remains constant within the specified range.

[4]The gain error of the driver is always in the negative direction with respect to the voltage set level.

[5]Transient output current can easily exceed the AD1322's steady-state current limit when driving capacitive loads. The transient output current capability can be increased by connecting 0.039 μF capacitors between Pin 5 and ground and Pin 6 and ground. This will prevent the driver from current limiting by providing the "edge" current necessary when driving capacitive loads. These capacitors will not affect the driver's dc current limit.

[6]Driver output impedance is 50 ohms, ±1.5 ohms for a 3 V swing into a 50 ohm cable.

[7]Delay times are measured from the crossing of differential ECL outputs at the inputs to the driver to the 50% point of a ±400 mV driver output.

[8]Due to uncontrolled inductances in the test socket, overshoot, preshoot and settling time cannot be fully tested. These characteristics are guaranteed by characterization data instead.

[9]Delay matching vs. PW is defined as the amount of change in propagation, with respect to the leading edge, due to change in pulsewidth of the input signal. The AD1322 is characterized over the pulsewidth range of 2 ns to 100 ns.

[10]Inhibit mode delay times are measured from the crossing of differential (ECL) INH inputs to a 200 mV transition at the pin driver output. V_{OUT} is connected to a 100 ohm/15 pF load terminated to ground. V_{OH} is set at +1 V and V_{OL} is set at −1 V for this test.

[11]A supply range of 15.2 V must be maintained to guarantee a 9 V output swing.

10

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- +Vs to GND . . . . . +13 V
- $-V_S$ to GND . . . . . −8.2 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from D to $\overline{D}$ . . . . . 5 V
- Difference from INH to $\overline{INH}$ . . . . . 5 V
- D, $\overline{D}$, INH, $\overline{INH}$ . . . . . $+V_S$ −12 V, $-V_S$ +11.5 V
- V_H to V_L . . . . . −4 V, +9 V
- V_H, V_L . . . . . $+V_S$ −13.0 V, $-V_S$ +13.2 V

Driver Output
- Voltage . . . . . $+V_S$ −13.0 V, $-V_S$ +13.2 V
- Short Circuit to GND . . . . . Indefinite

Operating Temperature Range . . . . . 0 to +70°C

Storage Temperature Range . . . . . −65°C to +125°C

Lead Temperature Range (Soldering 20 sec)† . . . . . +300°C

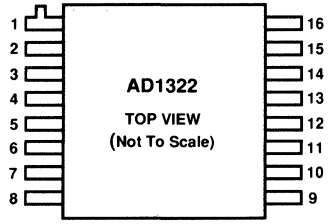
NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

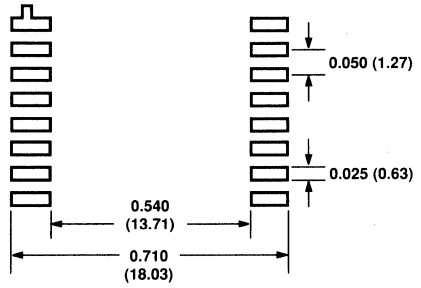
†To ensure lead coplanarity (±0.002 inches) and solderability handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).



SUGGESTED LANDING PADS LOCATION



PIN CONFIGURATION

PIN NO.	SYMBOL	FUNCTION
1	GND	CIRCUIT GROUND
2	N/C	NO CONNECTION
3	V_{OUT}	DRIVER OUTPUT
4	N/C	NO CONNECTION
5	C_{I+}	POSITIVE DECOUPLE
6	C_{I-}	NEGATIVE DECOUPLE
7	V_L	VOLTAGE LOGIC LOW
8	N/C	NO CONNECTION
9	LID	LID CONNECTION*
10	V_H	VOLTAGE LOGIC HIGH
11	$\overline{D}$	DRIVER INPUT
12	D	DRIVER INPUT
13	$\overline{INH}$	INHIBIT INPUT
14	INH	INHIBIT INPUT
15	$-V_S$	NEGATIVE SUPPLY
16	$+V_S$	POSITIVE SUPPLY

*IT IS RECOMMENDED TO CONNECT PIN 9 TO CIRCUIT GROUND.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD1322KZ	0 to +70°C	16-Lead Gull Wing	Z-16A

*See Section 20 for package outline information.

OFFSET ERROR

The offset error for logic high is determined by holding the output of the driver at logic high, and applying zero volts to the logic high reference input. The driver output value represents the offset "high" error. The same approach is used to identify offset "low" error. Refer to the Specification Table, Note 3.

$$V_{HIGH\ OFFSET} = V_{OUT}$$

where:

V_H = 0 V
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH

GAIN ERROR

Defined as the ratio of the driver's output voltage to its logic set level voltage and is expressed in terms of percent of set level. The gain error is typically seen as 2.5% and is always in the negative direction with respect to the logic set level.

$$V_{HIGH\ GAIN}\ (\%) = \frac{V_{OUT} - V_H - V_{HIGH\ OFFSET}}{V_H} \times 100$$

where:

V_H = 5.0 V+$V_{HIGH\ OFFSET}$
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH

LINEARITY ERROR

The deviation of the transfer function from a reference line. For the AD1322, the linearity error is calculated by subtracting the worst case gain error from the best case gain error (for the specified range) and divide the result by two. This method guarantees that the maximum linearity error for any set level within the specified range will be within the specified limits.

$$V_{HIGH\ LINEARITY}\ (\%) = \frac{V_{HIGH\ GAIN}\ (max) - V_{HIGH\ GAIN}\ (min)}{2} \times 100$$

DELAY TIME

The amount of time it takes the input signal to propagate through the driver and be converted to the desired logic levels. The measurement technique is defined in the notes and is shown in Figure 2.

EDGE-TO-EDGE MATCHING

Edge-to-edge matching is the difference, in time, between the delay time of the rising edge and the falling edge.

MINIMUM PULSEWIDTH

Defined as the smallest pulse applied to the input of the driver which can maintain an output signal amplitude of 2 V. The minimum pulsewidth is measured at the 50% point of the waveform.

OVERSHOOT AND PRESHOOT

The amount by which the driver's output voltage exceeds the desired set voltage. Preshoot is similar to overshoot but is the amount by which the driver's output goes below the initial voltage when driving to the new set level (or inhibit mode). See Figure 3.

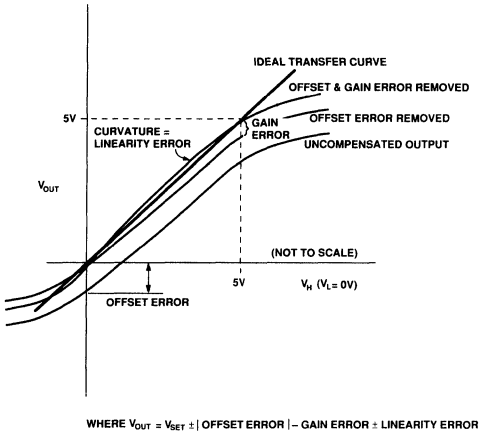


Figure 1. Definition of Terms

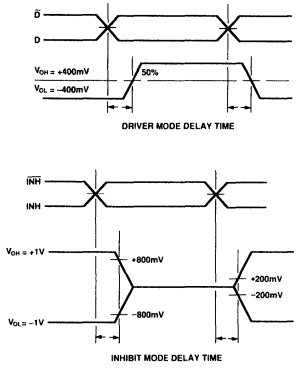


Figure 2. Timing Diagram for Driver and Inhibit Propagation Delay

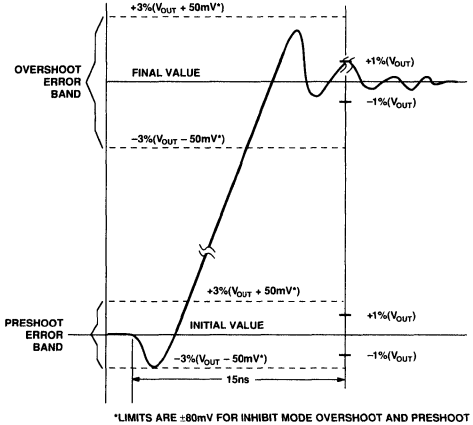


Figure 3. Definition of Waveform Abberrations

Typical Performance Characteristics

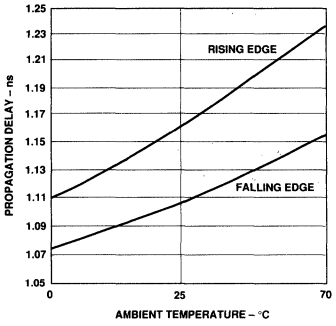


Figure 4. Driver Propagation Delay vs. Temperature

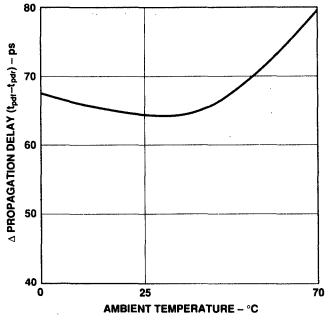


Figure 5. Propagation Delay Edge Matching vs. Temperature

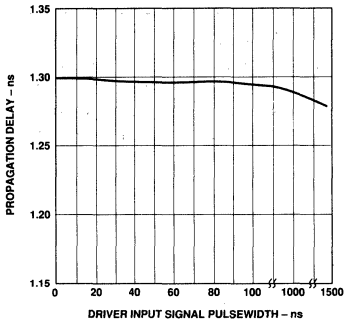


Figure 6. Propagation Delay vs. Input Signal Pulsewidth

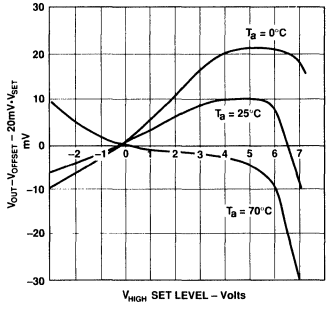


Figure 7. Change in V_{HIGH} over Temperature

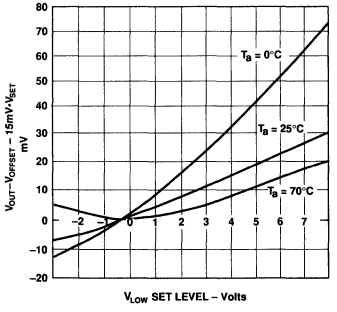


Figure 8. Change in V_{LOW} over Temperature

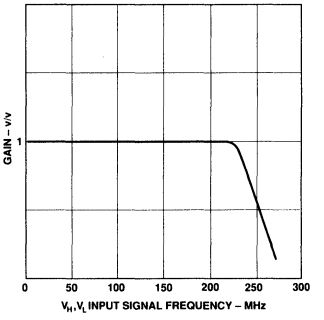


Figure 9. V_{HIGH} , V_{LOW} Input Bandwidth

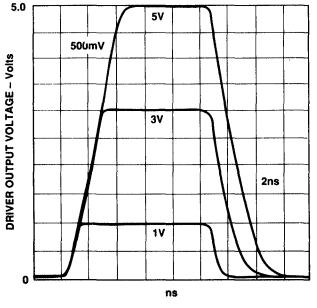


Figure 10. 10 ns Output Pulse at 1 V, 3 V and 5 V

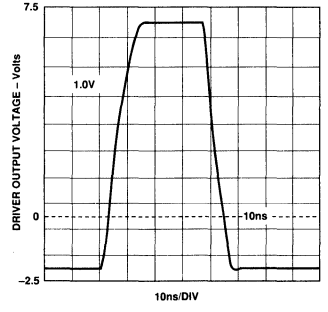


Figure 11. V_{OUT} = 9 V as Seen at the End of a 28", 50 Ω Cable

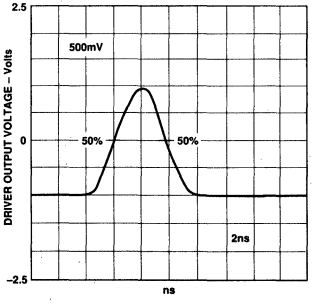


Figure 12. Minimum (Data) Pulsewidth as Defined by V_{OUT} = 2 V, 50% Crossing ≤ 2 ns

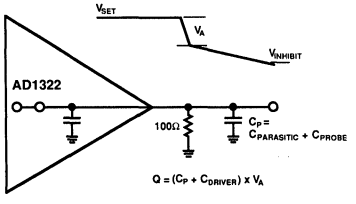


Figure 13. Charge into Inhibit Test Setup

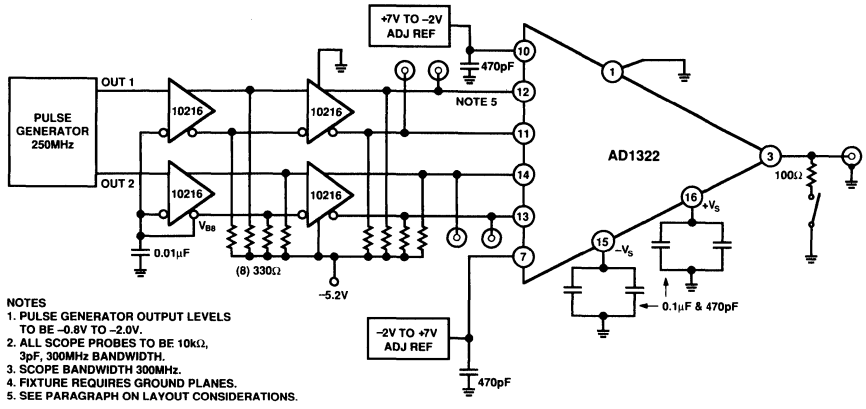


Figure 14. AD1322 Test Setup

FUNCTIONAL DESCRIPTION

The AD1322 is a complete high speed pin driver designed for use in general purpose instrumentation and digital functional test equipment. The purpose of a pin driver is to accept digital, analog and timing information from a system source and combine these to drive the device to be tested.

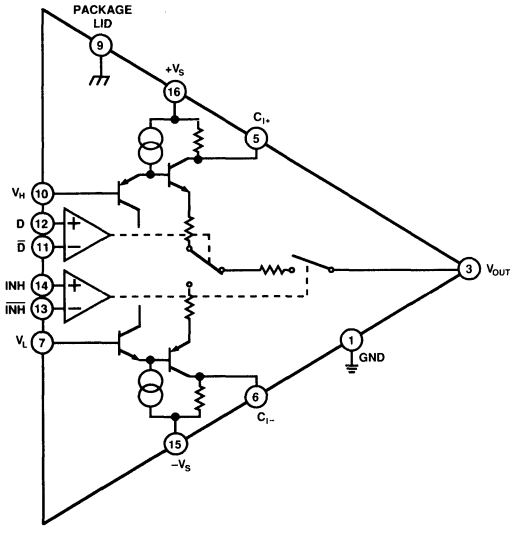


Figure 15. AD1322 Block Diagram

The circuit configuration for the AD1322 is outlined in Figure 15. Simply stated, a pin driver performs the function of a precise, high speed level translator with an output which can be disabled. The AD1322 accepts differential digital information utilizing a high speed differential design on the D and INH inputs providing precise timing at logic crossover and high noise immunity. The wide input voltage range allows for ECL operation with power supplies at 0 to −5.2 V, +2 V to −3.2 V or +5 V to 0 V. Where timing is less critical TTL or CMOS logic levels may be used to toggle the AD1322. By biasing the D and INH inputs to approximately +1.3 V for TTL and 1/2 V_{CC} for CMOS, the D and INH inputs can be directly driven from these single-ended output sources. The output of the pin driver will follow the logic state of the D input providing the INH input is low. When inhibit is asserted the output is disconnected and any activity on the input does not affect the output.

Analog information is provided to the pin driver through the V_H and V_L terminals as reference voltages. These analog voltages are buffered internally using unity gain followers. The resulting gain and linearity errors are provided in the specification table. System timing requirements are achieved through a specified 1.2 ns, ±200 ps driver propagation delay, 2.0 V/ns slew rate, defined preshoot and overshoot, and a dynamically trimmed 50 Ω output impedance.

LAYOUT CONSIDERATIONS

While it is generally considered good engineering practice to capacitively decouple the power supplies of an active device, it is absolutely essential for a high power, high speed device such as the AD1322. The engineer merely has to consider the current pulse demand from the power supply when a dynamic current change of −100 mA to +100 mA is required in only a few nanoseconds. Therefore, a 470 pF high frequency decoupling capacitor must be located within 0.25 inches of the $+V_S$ and $-V_S$ terminals to a low impedance ground. A 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor should also be situated between the power supplies and ground. However, the proximity to the device is less critical assuming low impedance power supply distribution techniques are employed. Circuit performance will be similarly enhanced and noise minimized by locating a 470 pF capacitor as close as possible to V_H, V_L and connected to ground. Bypass considerations have been summarized in Figure 16.

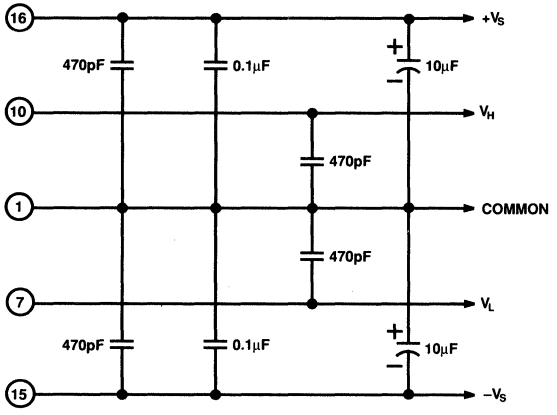


Figure 16. Basic Circuit Decoupling

An equally important consideration is the use of microwave stripline techniques on the output of the AD1322. Failure to preserve the 50 Ω output impedance of the pin driver will result in unwanted reflections, ringing and general corruption of the wave shape. Care should be exercised when selecting etch widths and routing, wire and cable to the device to be tested, and in choosing relays if they are required.

THERMAL CONSIDERATIONS

The AD1322 is provided in a 0.450″ × 0.450″, 16 lead (bottom brazed) gull wing, surface mount package with a typical junction-to-case thermal resistance of 5.6°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1322 in this package is shown in Figure 17. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1, 2].

NOTES
[1]lfm is air flow in Linear Feet/Minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

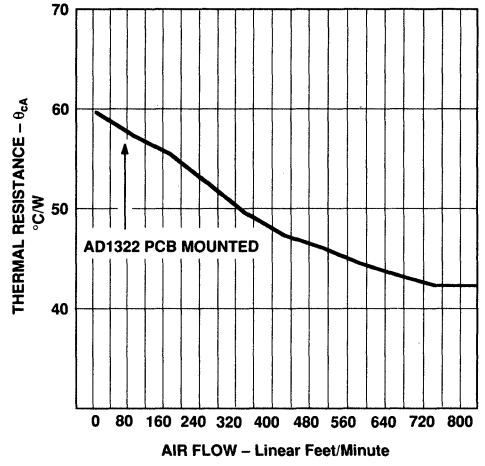


Figure 17. Case-to-Ambient Thermal Resistance vs. Air Flow

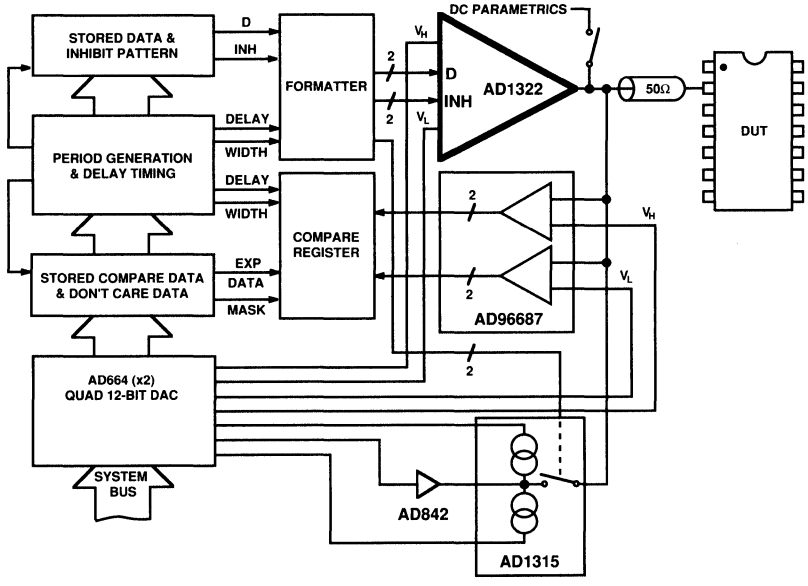
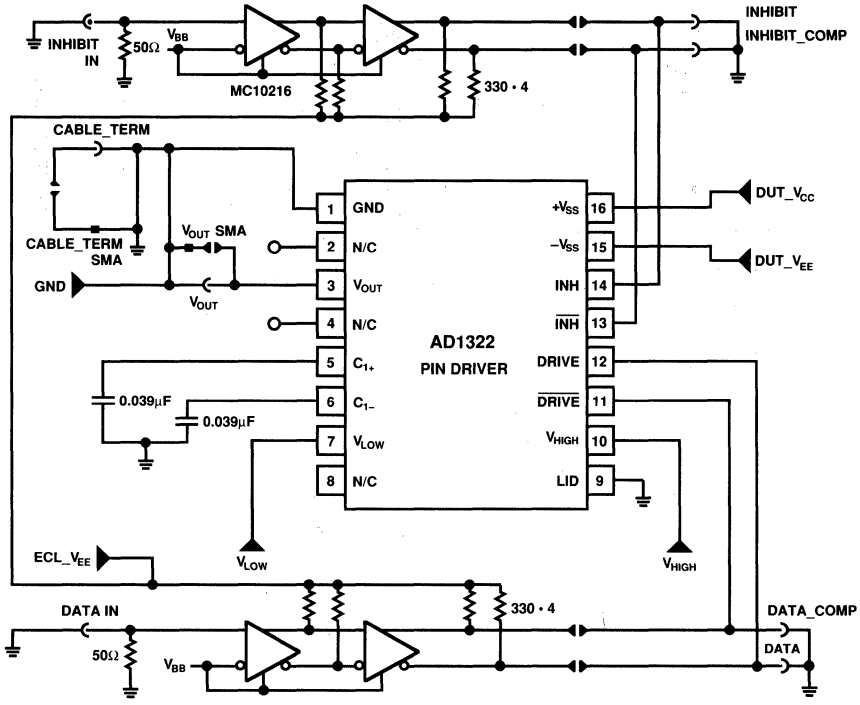


Figure 18. High Speed Digital Test System Block Diagram

10

APPLICATIONS

The AD1322 has been optimized to function as a pin driver in an ATE test system. Shown in Figure 18 is a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1322 pin driver, AD96687 high speed dual comparator, AD1315 active load, and the AD664 quad 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 200 MHz in a data mode or 100 MHz in the I/O mode, yet fit into a neat trim package.



NOTES:
"HALF-MOON" CONNECTORS CAN BE CONNECTED OR DISCONNECTED AS REQUIRED . . . ◀▶
DECOUPLING CAPS ARE NOT SHOWN ON THIS SCHEMATIC, BUT THE BOARD USES 0.1µF AND 470pF CAPS TO DECOUPLE THE V_{CC}, V_{EE}, V_{LOW} AND V_{HIGH} SUPPLIES.
SMA CONNECTORS ■
PROBE JACKS)
BNC CONNECTORS (

Figure 19. AD1322EB Evaluation Board Schematic

AD1322 EVALUATION BOARD

Introduction

The AD1322EB evaluation board was developed to aid the customer in quickly evaluating the performance of the AD1322. Included is complete documentation of the evaluation board along with suggestions on equipment to use and measurement limitations.

Overview

The AD1322 is a high speed pin driver used in automatic test equipment

The device has true differential inputs for both the drive and inhibit which can be driven from either TTL or ECL logic levels (ECL is recommended). Standard ECL design and layout techniques should be used.

The device runs from dual power supplies +10 V and −5.2 V. It is very important that these power supplies are decoupled properly at the device pin. (High frequency oscillations will couple through to the device output.)

The reference input pins are dc inputs; therefore they also should be decoupled properly. The reference input range is −2 V to +7 V.

The output slew rate is 1 V/ns for large signals and has a rep rate for an ECL level of 100 MHz minimum.

Equipment

The Drive and Inhibit inputs should be driven with standard ECL levels. If the full performance of the AD1322 needs to be evaluated, the generator must be able to supply an ECL level at frequencies greater than 200 MHz. Motorola's MC10216 is used on the evaluation board to simulate the actual application. V_{BB} is used on the MC10216 as the logic reference and the outputs have 330 ohm pulldowns to V_{EE}.

Five power supplies are required: DUT_V_{CC}, DUT_V_{EE}, V_{HIGH}, V_{LOW} and ECL_V_{EE}. DUT_V_{CC} requires +10 V at 100 mA minimum; DUT_V_{EE} requires −5.2 V at 100 mA minimum; ECL_V_{EE} requires −5.2 V at 150 mA minimum. V_{HIGH} and V_{LOW} require −2 V to +7 V at 5 mA (each).

The output performance of the pin driver can only be measured properly with a scope which has the proper bandwidth for the required application. The input impedance and the bandwidth of the scope probe should be taken into consideration when evaluating the performance of the device. The resultant bandwidth of the system is the RMS value of the components in the system.

The characterizations performed by Analog Devices were performed using the following equipment: the scope equipment consists of the Tektronix 11402 mainframe (1 GHz BW), P6203 FET probe (1 GHz, 1.2 pF, 1 M ohm) and the 11A71 plug-in (1 GHz BW, 50 ohm).

The Hewlett-Packard 54120 and 54110 were also evaluated with the 500 ohm, 1.2 pF passive probes and the Data Precision 6100 with their model 640 FET probe (50 kΩ, 4 pF). When measuring the performance of waveforms close to or exceeding the bandwidth of a scope, it is not uncommon for the results between scopes to be different because of aberrations and slew rates.

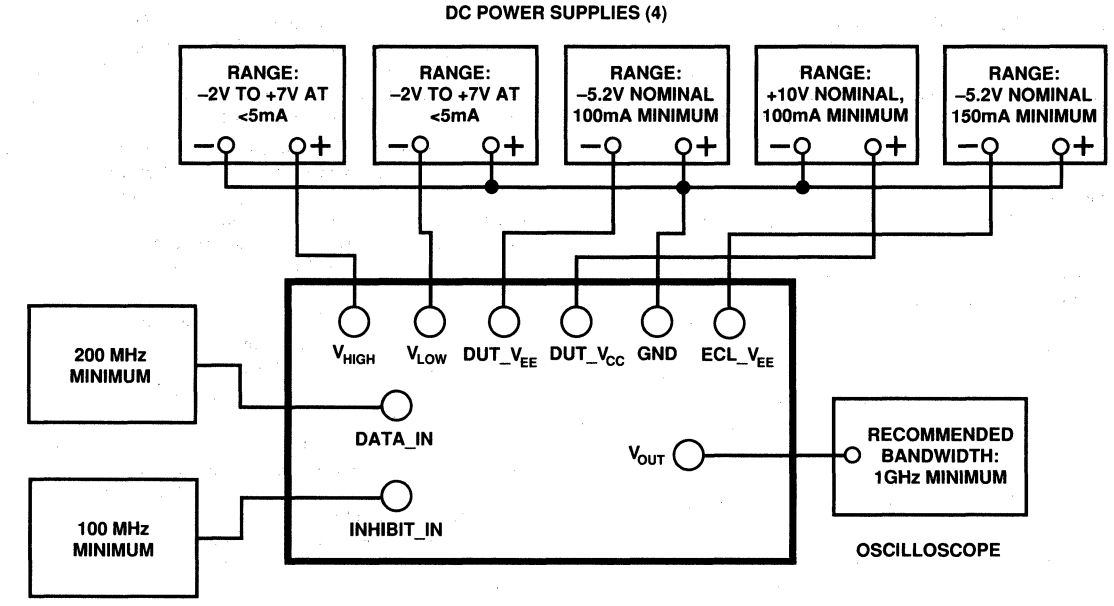


Figure 20. AD1322 Evaluation Board Connections

Ultrahigh Speed Pin Driver with Inhibit Mode

AD1322B

FEATURES
200 MHz Driver Operation
Driver Inhibit Function
200 ps Edge-to-Edge Matching
Guaranteed Industry Specifications
Trimmed 50 Ω Output Resistance
Variable Output Voltages for ECL, TTL and CMOS
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package

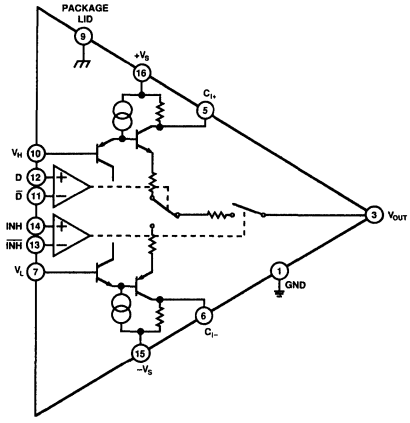
APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation & Characterization Equipment
Pulse Generator for High Speed Amplifiers
General Purpose Driver

PRODUCT DESCRIPTION

The AD1322B is a complete high speed pin driver designed for use in digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities and long-term reliability in an ultrasmall 16-lead, hermetically sealed gull wing package.

Featuring unity gain programmable output levels of −2 V to +7 V, with output swing capability of 400 mV to 9 V, the AD1322B is designed to stimulate ECL, TTL, and CMOS logic families. The 200 MHz (2.5 ns pulse width) data rate capacity, controlled slew rate, and matched 50 Ω output resistance allow for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (Inhibit mode) electrically removing the pin driver from the path. The typical Inhibit leakage current is 250 nA and the output charge transfer going into Inhibit is typically less than 5 pC.

AD1322B FUNCTIONAL BLOCK DIAGRAM



The AD1322B transition from HI/LOW or to Inhibit is controlled through the data and inhibit inputs. The input uses high speed differential circuitry with a common-mode range of 8 V. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic HI/LO inputs are equally easy to interface. Requiring typically 15 µA of bias current, the AD1322B can be directly coupled to the output of a DAC either alone or in parallel with several other drivers.

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SPECIFICATIONS (All measurements made in free air at +25°C. Output load 10 kΩ/6 pF with $+V_S$ = +10 V, $-V_S$ = −5.2 V unless otherwise specified.)

Parameter	AD1322BKZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Input Voltage	$-V_S$ +2.2		$+V_S$ −4.5	Volts	
Differential Input Range	0.4	ECL	3.0	Volts	
Bias Current	−300	175	300	μA	
REFERENCE INPUTS					See Note 1
V_{HIGH} Range (V_H)	$-V_S$ +2.7		$+V_S$ −2.5	Volts	
V_{LOW} Range (V_L)	$-V_S$ +2.7		$+V_S$ −2.5	Volts	
Bias Currents	−40	±15	40	μA	
Bias Current Change		2	10	μA	See Note 2
OUTPUT CHARACTERISTICS					See Notes 1, 3
Logic High Range	$-V_S$ +3.2		$+V_S$ −3.0	Volts	
Logic Low Range	$-V_S$ +3.2		$+V_S$ −3.0	Volts	
Amplitude [$V_H - V_L$]	0.4		+9.0	Volts	
Accuracy					
Initial Offset	−100		+100	mV	
Gain Error	−2.5	−1.0	−0.5	% of V_{SET}	See Notes 4, 5
Linearity Error					
$-V_S$ +5.2 V to $+V_S$ −4.5 V	−0.15		+0.15	% of V_{SET}	See Note 5
$-V_S$ +3.2 V to $+V_S$ −3 V	−0.6	±0.4	+0.6	% of V_{SET}	
$-V_S$ +4.2 V to $+V_S$ −4 V	−0.4	±0.2	+0.4	% of V_{SET}	
Output Voltage TC		0.5		mV/°C	
Current Drive					
Static	30.0			mA	See Note 5
Dynamic	100.0			mA	See Note 6
Current Limit			85	mA	Output to GND
Output Resistance	48.5	50.0	51.5	Ω	See Note 7
Leakage Current in Inhibit Mode					
−2 V to +7 V	−1	0.25	+1	μA	
DYNAMIC PERFORMANCE					See Note 8
Driver Mode					
Delay Time	1.0	1.3	1.6	ns	See Note 9
Prop Delay TC		1.0		ps/°C	
Delay Time Matching Edge-to-Edge		50	200	ps	
Rise & Fall Times					
1 V Swing	0.3	0.5	0.7	ns	Measurement 20%–80%
2 V Swing	1.0	1.2	1.4	ns	Measurement 10%–90%
3 V Swing	1.4	1.7	2.0	ns	Measurement 10%–90%
5 V Swing	2.5	2.8	3.1	ns	Measurement 10%–90%
9 V Swing	4.6	5.0	5.4	ns	Measurement 10%–90%
Toggle Rate	200			MHz	ECL Output
Overshoot & Preshoot					See Note 10
1 V to 7 V	−(3% +50)		+(3% +50)	mV	
Settling Time					See Note 10
1 V to 7 V, ±(1% × V_O)			15	ns	
Delay Time vs. PW		100		ps	See Note 11
DYNAMIC PERFORMANCE					
Inhibit Mode Delay Time					Note 12
Drive to Inhibit	1.1	1.4	1.7	ns	
Inhibit to Drive	1.1	1.4	1.7	ns	
Delay Time Matching					
Edge-to-Edge		50	200	ps	
Overshoot & Preshoot			150	mV	1 V Swing
Output Capacitance		3.5	5	pF	
Output Charge Going into Inhibit Mode		5		pC	

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter	AD1322BKZ Min	Typ	Max	Units	Comments
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range		15.2	15.6	Volts	
Supply Range					See Note 13
Positive Supply	+8.0	+10.0	+11.0	Volts	
Negative Supply	−7.2	−5.2	−3.2	Volts	
Current					
Positive Supply	4.2	60	78	mA	
Negative Supply	−78	−60	−42	mA	
+PSRR		5	20	mV/V	$+V_S$, $-V_S$ = ±2.5%
PACKAGE OPTION[14]					
Gull Wing (Z-16A)					

NOTES

[1]The output voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different values of V_{OUT} such as −1 V to +8 V or −4 V to + 5 V as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

[2]V_H and V_L inputs have internal buffers which reduce the input bias current requirements. These buffers also reduce the amount of bias current change when the output switches logic levels.

[3]V_H can be set to be as much as 4 V below V_L without any harm to the driver with the restriction that neither level can go below −2 V with the typical power supply setting.

[4]While in inhibit move, the output voltage must not go more than 6 V above V_{HIGH} or 6 V below V_{LOW}.

[5]Guaranteed with power supply conditions of: $+V_S$ = +11 V, $-V_S$ = −4.2 V; $+V_S$ = + 10 V, $-V_S$ = −5.2 V; $+V_S$ = +8 V, $-V_S$ = −7.2 V.

[6]Transient output current can easily exceed the AD1322B's steady state current limit when driving capacitive loads. The transient output current capability can be increased by connecting 0.039 μF capacitors between Pin 5 and ground and Pin 6 and ground. This will prevent the driver from current limiting by providing the "edge" current necessary when driving capacitive loads. These capacitors will not affect the driver's dc current limit.

[7]Driver output resistance is 50 Ω for a 3V p–p signal into a 50Ω load.

[8]The driver output has 2 ns length of 50 Ω coaxial cable attached with a 10 k/2 pF probe, 1 GHz bandwidth or equivalent at the other end.

[9]Delay times are measured from the crossing of the differential ECL levels at the input to the 50% point of an 800 mV driver output with V_H and V_L set at ±400 mV, respectively.

[10]Due to uncontrolled inductances in the test socket, overshoot, preshoot and settling time cannot be 100% tested. These characteristics are guaranteed by characterization data instead.

[11]Delay matching vs. PW is defined as the amount of change in propagation, with respect to the leading edge, due to change in pulsewidth of the input signal. This specification applies over the pulsewidth range of 2 ns to 100 ns.

[12]Inhibit mode delay times are measured from the crossing of differential (ECL) INH inputs to a 200 mV crossing at the pin driver's output connected to a 2 ns length of 50 Ω coaxial cable. The cable is terminated to ground through a 50 Ω resistor. The measurement is made between the end of the cable and the 50 Ω resistor to GND with a 10 kΩ/2 pF scope probe.

[13]A supply range of 15.2 V must be maintained to guarantee a 9 V output swing.

Specifications subject to change without notice.

10

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- +Vs to GND . . . . . +13 V
- $-V_S$ to GND . . . . . −8.2 V
- Difference from $+V_S$ to $-V_S$ . . . . . +16 V

Inputs
- Difference from D to $\overline{D}$ . . . . . 4.75 V
- Difference from INH to $\overline{INH}$ . . . . . 4.75 V
- D, $\overline{D}$, INH, $\overline{INH}$ . . . . . $+V_S$ −13 V, $-V_S$ +11.5 V
- V_H to V_L . . . . . −1 V, +9 V
- V_H, V_L . . . . . $+V_S$ −13.2 V, $-V_S$ +13.2 V

Driver Output
- Voltage . . . . . $+V_S$ −13.2 V, $-V_S$ +13.2 V
- Short Circuit to GND . . . . . Indefinite

Operating Temperature Range . . . . . 0 to +70°C

Storage Temperature Range . . . . . −65°C to +125°C

Lead Temperature Range (Soldering 20 sec)† . . . . . +300°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†To ensure lead coplanarity (±0.002 inches) and solderability handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

Special Function Components
Contents

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Orientation . . . . . 11 – 3
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AD7341/AD7371 – LC²MOS Voiceband Reconstruction and Antialiasing Filter Set . . . . . 11 – 17
AD9500 – Digitally Programmable Delay Generator . . . . . 11 – 33
AD9501 – Digitally Programmable Delay Generator . . . . . 11 – 43
AD9901 – Ultrahigh Speed Phase/Frequency Discriminator . . . . . 11 – 55

Selection Guide
Special Function Components

Model	Description	Package Options[1]	Temp Range[2]	Page
AD639	**Universal Trigonometric Function Converter**	**D**	**I**	**11–5**
AD7341	**Voiceband Transmission Filter for 14-Bit DAC**	**N, P**	**C**	**11–17**
AD7371	**Voiceband Receive Filter for 14-Bit ADC**	**N, P**	**C**	**11–17**
AD9500	**Digitally Programmable Delay Generator**	**E, P, Q**	**I, M**	**11–33**
AD9901	**Digital Phase/Frequency Discriminator**	**E, Q**	**C, M**	**11–55**
AD9501	**TTL/CMOS Digitally Programmable Delay Generator**	**N, P, Q**	**C, M**	**11–43**

[1]Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; N–Plastic Molded Dual-In-Line; P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip.
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
Special Function Components

This section contains technical data on integrated-circuit chips that could not be classified in any of the major sections of this databook without losing their identities. For example, the AD639 trigonometric function generator is a close relative of analog multiplier/dividers, in both function and circuitry; but if it were listed in that section, its unique trigonometric capabilities would be "buried".

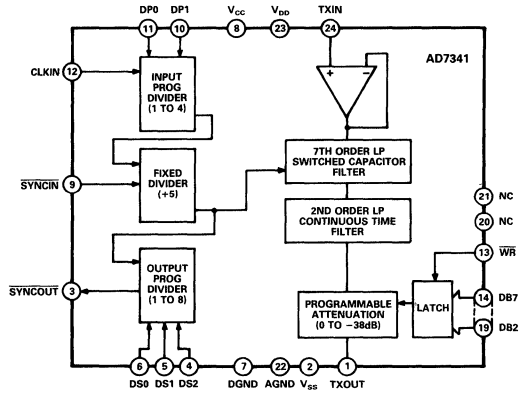
We describe briefly here the function and salient uses of these devices. For further information, consult the individual data sheets.

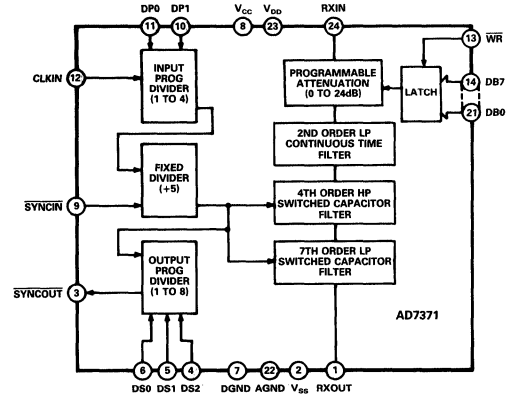
ANALOG FUNCTIONS

AD7341 and AD7371 Filters

These filters have been designed for use in high speed voice band modems, in particular those adhering to the CCITT V.32 and V.33 recommendations. The AD7371 is the antialiasing filter for the receive ADC, while the AD7341 is the reconstruction filter for the output DAC.

Both filters contain a 7th order low pass switched capacitor section with a cut-off frequency of 3.5kHz. This can be varied by changing the device CLKIN frequency. The AD7371 has an additional 4th order high pass section with a cut-off frequency of 180Hz to filter out mains interference.



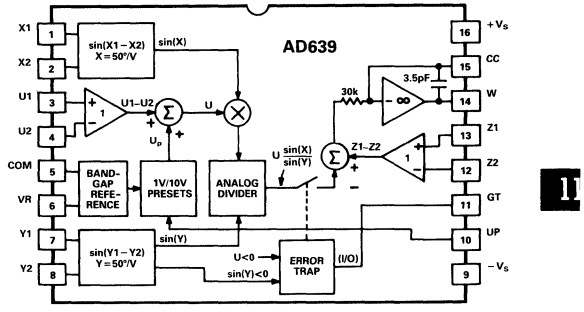


The key performance features of the parts are low noise and distortion and high stopband attenuation. In-band signal-to-noise ratio is 75dB, while THD is better than −75dB. The stopband attenation is 70dB minimum.

Additional features include programmable gain for the AD7371 and programmable attenuation for the AD7341. Both devices have signals which ease synchronization with accompanying DACs and ADCs.

AD639 Universal Trigonometric Function Generator

The AD639 is an analog "trigonometric microsystem" on a single silicon chip, packaged in a 16-pin DIP. From a differential input voltage, representing an angle (20mV/°), it can be pin programmed to generate a voltage output, accurately determined by any of the standard functions – sine, cosine, tangent, secant, cosecant and cotangent – as well as some lesser known variants, such as the versine and exsecant, plus a corresponding set of inverse functions. All inputs are differential, and either polarity of input or output can be generated.



Trigonometric functions play an important role in electronics. Inherent to many communications, measurement and display systems, they also find increasing application in control and robotics. Most familiar are the *sine* and the *cosine*, which find wide use as fundamental signal sources – both separately and in orthogonal pairs. In display systems, these functions are basic to graphical manipulations (axis rotation and polar-to-Cartesian conversion), and they also appear in many antenna-related signal transformations. The *tangent* is important in scanning systems, and the *arctangent* is used in Cartesian-to-polar conversion and in determining phase angle from the real and imaginary components of a complex signal.

With its large repertoire of functions, the AD639 makes it possible to include trigonometric transformations in the analog portion of a system with little added cost or board space, and with high accuracy, without the overhead in software, memory or time, which would accompany such computations in an associated digital system. It also makes it easy to generate low-distortion sine-wave signals, with voltage control of amplitude and frequency, up to 10V and 1MHz, respectively.

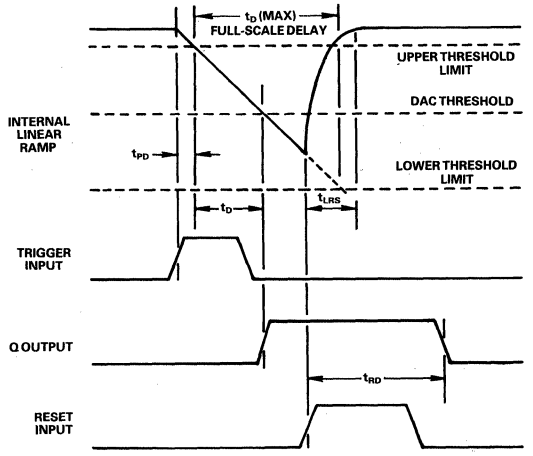
DIGITAL FUNCTIONS

AD9500/AD9501 Digitally Programmable Delay Generators
The AD9500 delays events by an interval selected by an 8-bit digital code, with settable time resolution as small as 10 picoseconds. The delay is initiated at the time a *Trigger* input goes *high*: an integrator generates a downgoing ramp, and when it crosses a preset level (established by an 8-bit DAC), a comparator output changes state to produce the delayed output, *Q*.

The delay is equal to the programmed delay – which depends on the integrator's selectable RC time constant and the precision threshold set by the DAC – plus a propagation delay. A pulse of appropriate width applied at the *Reset* input resets the integrator and the Q output to prepare the device for the next *Trigger*. The range of full-scale programmed delays is from 2.5ns to 10μs, depending on the choice of R and C. When $RC = 2.5$ns, the LSB (or one increment of delay) is 2,500 ps/256 ≈ 10 ps, which is also the typical jitter level.

The AD9500 is designed to delay ECL pulse patterns, while the AD9501 inputs and output are TTL compatible. The inputs to the AD9500 are differential for maximum noise immunity.

An important application is in equalizing skew in multichannel systems; with one line used as the standard, the programmed delays of the other AD9500s are adjusted to eliminate the timing skews. Other applications include multiple-phase clock generators, measuring unknown delays and time response of high-speed ac waveforms, and digitally programmable oscillators.



t_D (MAX) – PROGRAM DELAY (FULL SCALE)
t_{PD} – MINIMUM PROPAGATION DELAY
t_D – PROGRAM DELAY
t_{LRS} – LINEAR RAMP SETTLING TIME
t_{RD} – RESET PROPAGATION DELAY

AD9500 Internal Timing Diagram

ANALOG DEVICES

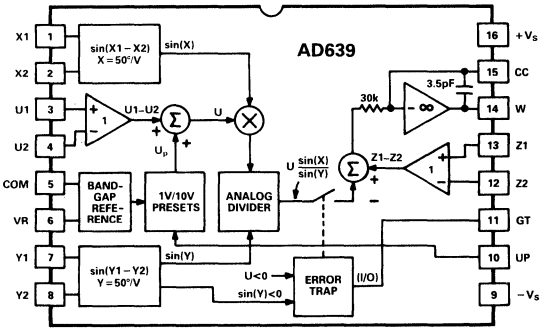
Universal Trigonometric Function Converter

AD639*

FEATURES
- Complete, Fully-Calibrated Synthesis System
- All Standard Functions: Sin, Cos, Tan, Cosec, Sec, Cot, Arcsin, Arccos, Arctan, etc.
- Accurate Law Conformance (Sine to 0.02%)
- Angular Range of ±500° (Sine Mode)
- Function Programmable by Pin Strapping
- 1.5MHz Bandwidth (Sine Mode)
- Multiplication via External Amplitude Input

APPLICATIONS
- Continuous Wave Sine Generators
- Synchro Sine/Cosine Multiplication
- Coordinate Conversion and Vector Resolution
- Imaging and Scanning Linearization Circuits
- Quadrature and Variable Phase Oscillators

AD639 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD639 is a high accuracy monolithic function converter which provides all the standard trigonometric functions and their inverses via pin-strapping. Law conformance and total harmonic distortion surpass that previously attained using analog shaping techniques. Speed also exceeds that possible using ROM look-up tables and a DAC; in the sine mode, bandwidth is typically 1.5MHz. Unlike other function synthesis circuits, the AD639 provides a smooth and continuous sine conformance over a range of −500° to +500°. A unique sine generation technique results in 0.02% law conformance errors and distortion levels of −74dB in triwave to sinewave conversion.

The AD639 is available in three performance grades. The A and B are specified from −25°C to +85°C and the S is guaranteed over the extended temperature range of −55°C to +125°C. All versions are packaged in a hermetic TO-116, 16-pin ceramic DIP. A-grade chips are also available.

PRODUCT HIGHLIGHTS

The AD639 generates a basic function which is the ratio of a pair of independent sines:

$$W = U\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)}$$

The differential angle arguments are proportional to the input voltages X and Y scaled by 50°/V. Using the 1.8V on-board reference any of the angular inputs can be preset to 90°. This provides the means to set up a fixed numerator or denominator (sin 90° = 1) or to convert either sine function to a cosine (cosθ = sin (90° − θ)). Using the ratio of sines, all trigonometric functions can be generated (see Table I).

The amplitude of the function is proportional to a voltage U, which is the sum of an external differential voltage ($U_1 - U_2$) and an optional internal preset voltage (U_p). The control pin UP selects a 0V, 1V or 10V laser-trimmed preset amplitude which may be used alone ($U_1 - U_2 = 0$) or internally added to the $U_1 - U_2$ analog input. At the output, a further differential voltage Z can be added to the ratio of sines to obtain the offset trigonometric functions versine (1 − cos θ), coversine (1 − sin θ) and exsecant (1 − sec θ). A gating input is available which may be used to enable or disable the analog output. This pin also acts as an error flag output in situations where a combination of inputs will cause the output to saturate or to be undefined.

In the inverse modes, the argument can be the ratio of two input signals. This allows the user to compute the phase angle between the real and imaginary components of a signal using the arctangent mode.

SPECIFICATIONS (typical @T_A = 25°C, V_S = ±15V, U or U_p = 10V unless otherwise specified)

Parameter	Conditions	AD639A Min	AD639A Typ	AD639A Max	AD639B Min	AD639B Typ	AD639B Max	AD639S Min	AD639S Typ	AD639S Max	Units
SYSTEM PERFORMANCE											
SINE AND COSINE MODE ACCURACY											
Law Conformance[1]	−90° to +90°, U = 10V		0.02			0.02			0.02		%
Total Harmonic Distortion[2]	@10kHz, U = 10V		−74			−74			−74		dB
Mismatch of Six Peaks	−540° to +540°		0.05			0.05			0.05		%
Output Noise	@10kHz, U = 10V		2.8			2.8			2.8		$\mu V/\sqrt{Hz}$
	@10kHz, U = 1V		0.5			0.5			0.5		$\mu V/\sqrt{Hz}$
PEAK ABSOLUTE ERROR											
Sine Mode	−90° to +90°, U_p = 10V		0.4	**0.8**		0.2	**0.4**		0.2	**0.8**	%FS
	T_{min} to T_{max}		1.0			0.8	**1.8**		1.2	**2.5**	%FS
Cosine Mode	−90° to +90°, U_p = 10V		0.6	**1.2**		0.4	**0.7**		0.5	**1.2**	%FS
	T_{min} to T_{max}		1.5			1.2	**2.0**		1.7	**2.7**	%FS
Sine or Cosine	−180° to +180°, U_p = 10V		0.8	**1.5**		0.5	**0.8**		0.6	**1.5**	%FS
	T_{min} to T_{max}		1.7			1.3	**2.5**		2.1	**3.0**	%FS
	−360° to +360°, U_p = 10V		1.2			1.0			0.9		%FS
	−90° to +90°, U_p = 1V		1.3	**2.5**		1.0	**1.7**		0.9	**2.5**	%FS
	T_{min} to T_{max}		1.5			1.0	**2.3**		∠.0	**3.5**	%FS
	−180° to +180°, U_p = 1V		1.5	**3.0**		1.2	**2.0**		1.1	**3.0**	%FS
	T_{min} to T_{max}		1.7			1.3	**2.5**		2.3	**4.0**	%FS
	−360° to +360°, U_p = 1V		2.0			1.8			1.5		%FS
vs Supply	−360° to +360°, U_p = 10V V_s = ±15V ±1V		0.02			0.02			0.02		%FS/V
	−360° to +360°, U_p = 1V V_s = ±15V ±1V		0.07			0.07			0.07		%FS/V
TANGENT MODE ACCURACY											
Peak Error[3]	−45° to +45°, U_p = 10V		0.5	**3.5**		0.5	**2.0**		0.5	**3.5**	%FS
	T_{min} to T_{max}		2.5			1.5	**2.8**		3.0		%FS
	−45° to +45°, U_p = 1V		0.9	**5.0**		0.9	**3.0**		0.9	**2.5**	%FS
	T_{min} to T_{max}		4.0			2.0	**5.0**		**1.5**	**3.0**	%FS
ARCTANGENT MODE ACCURACY											
Peak Angular Error											
Fixed Scale	U_p = 1V		0.5			0.5			0.5		Degrees
Variable Scale	U = 0.1V, −11V≤Z≤+11V		1.5			1.5			1.5		Degrees
	U = 10V, −11V≤Z≤+11V		0.2			0.2			0.2		Degrees
SECTIONAL SPECIFICATIONS											
ANGLE INPUTS (X1 & X2, Y1 & Y2)[4]											
Input Resistance to COM			3.6			3.6			3.6		kΩ
Nominal Scaling Factor			50			50			50		°/V
X1 & X2 Inputs											
Angular Range For Specified Error(X1 − X2)		−360		+360	−360		+360	−360		+360	Degrees
Scaling Error X1 or X2			0.2	**0.65**		0.2	**0.65**		0.2	**0.65**	%
Angular Offset X1 = X2 = 0			0.1	**0.3**		0.1	**0.3**		0.1	**0.3**	Degrees
Y1 & Y2 Inputs											
Angular Range For Specified Error (Y1 − Y2)		0		+180	0		+180	0		+180	Degrees
Scaling Error Y1 or Y2			0.2	**2.0**		0.2	**2.0**		0.2	**1.0**	%
Angular Offset Y1 = Y2 = 0			0.1	**1.0**		0.1	**1.0**		0.1	**0.5**	Degrees
AMPLITUDE INPUTS (U1 & U2)											
Input Resistance to COM			50			50			50		kΩ
Nominal Gain	X = Y = VR, W to Z1		1			1			1		V/V
Gain Error	U = 0.1 to 10V		0.01	**0.5**		0.01	**0.5**		0.01	**0.5**	%
	T_{min} to T_{max}		0.08			0.08			0.25		%
Voltage Offset	$U_1 = U_2 = 0V$		3.0	**10**		3.0	**10**		3.0	**10**	mV
	T_{min} to T_{max}		3.0			3.0			4.0		mV
Linearity Error	$0 \le U_1 - U_2 \le 10V$		0.1			0.1			0.1		%
AMPLITUDE PRESET (UP)											
1V Preset Enabled	UP tied to $-V_S$										
Amplitude Accuracy			0.4	**2.0**		0.4	**2.0**		0.4	**2.0**	%
	T_{min} to T_{max}		1.5			1.5			2.0		%
10V Preset Enabled	UP tied to $+V_S$										
Amplitude Accuracy			0.1	**0.55**		0.1	**0.55**		0.1	**0.55**	%
	T_{min} to T_{max}		1.0			1.0			1.5		%
INVERSE INPUTS (Z1 & Z2)											
Input Resistance to COM			50			50			50		kΩ

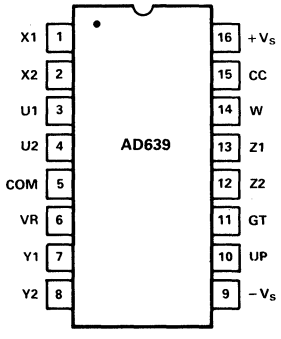
Parameter	Conditions	AD639A Min	AD639A Typ	AD639A Max	AD639B Min	AD639B Typ	AD639B Max	AD639S Min	AD639S Typ	AD639S Max	Units
SIGNAL OUTPUT (W)[5]	$R_L \geq 2k\Omega$, $C_L \leq 100pF$										
Small Signal Bandwidth W to Z1											
	Cc = 0		1.5			1.5			1.5		MHz
	Cc = 200pF		30			30			30		kHz
Slew Rate	Cc = 0		30			30			30		V/μs
Output Voltage Swing		**±11**	±13		**±11**	±13		**±11**	±13		V
Short Circuit Current		**20**	30	**45**	**20**	30	**45**	**20**	30	**45**	mA
Output Offset	$Z_1 = Z_2 = 0$, $U_p = 10$		5	**30**		5	**30**		5	**30**	mV
	T_{min} to T_{max}		10			10					mV
	$Z_1 = Z_2 = 0$, $U_p = 1V$			**20**			**20**			**20**	mV
	T_{min} to T_{max}		7			7					mV
VOLTAGE REFERENCE (VR)											
$R_L \geq = 1.8k\Omega$											
Nominal Output			+1.8			+1.8			+1.8		V
Output Voltage Tolerance			0.05	**0.45**		0.05	**0.45**		0.05	**0.45**	%
	T_{min} to T_{max}		0.08			0.08	**0.5**		0.2	**0.6**	%
Supply Regulation	$+V_S$ = 5V to 18V		150			150			150		μV/V
Maximum Output Current			4			4			4		mA
GATE I/O (GT)											
Switching Threshold as an Input	Output Valid		+1.5			+1.5			+1.5		V
	Output Invalid		0.1			0.1			0.1		V
Voltage Output	Error, $R_L = 5k\Omega$		+2.25			+2.25			+2.25		V
	No Error, $R_L = 5k\Omega$		−0.25			−0.25			−0.25		V
POWER SUPPLIES											
Operating Range		**±5.5**		**±18**	**±5.5**		**±18**	**±5.5**		**±18**	V
$+V_S$ Quiescent Current	U = X = 0V, Y = Vr		8.0	**11**		8.0	**11**		8.0	**11**	mA
$-V_S$, Quiescent Current	U = X = 0V, Y = Vr		5.5	7.5		5.5	7.5		5.5	7.5	mA
TEMPERATURE RANGE											
Operating, Rated Performance		−25		+85	−25		+85	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[6]											
16-Pin Ceramic Side Braze DIP (D)		AD639AD			AD639BD			AD639SD			
								AD639SD/883B			
Chips		AD639 A-Chips									

NOTES
[1]Intrinsic accuracy measured at an amplitude of 10V using external adjustments to absorb residual errors in angular scaling, angular offset, amplitude scaling and output offset.
[2]Using a time and amplitude symmetric triangular wave of +3.6V peak-to-peak and external adjustments to absorb residual errors in angular scaling and offset.
[3]Full scale is defined as the ideal output when the angle input is at either end of the limit specified.
[4]Specifications for the X inputs apply for range U = 1V to 10V, while the Y input errors are specifically given for U = 1V.
[5]When driving loads of less than 4kΩ, a 25pF capacitor from pin 15 to pin 9 avoids possible instability, although this is unnecessary when C_L is greater than 150pF.
[6]See Section 20 for package outline information.

Specifications subject to change without notice.

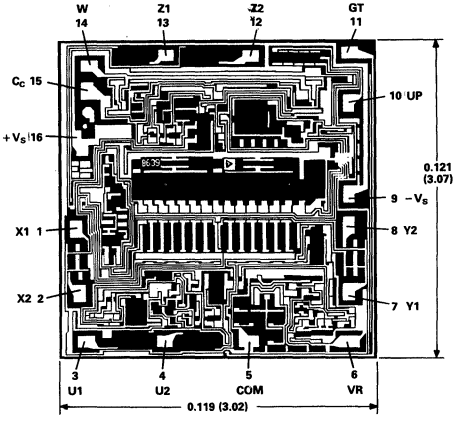
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units. Contact the factory for details.

PIN CONFIGURATION



METALIZATION PHOTO
CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Consult factory for latest dimensions.



ABSOLUTE MAXIMUM RATINGS

	AD639A,B	AD639S
Supply Voltage	±18V	*
Internal Power Dissipation	300mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages X_1, X_2, Y_1, Y_2[1]	±12V	*
Input Voltages U_p, U_1, U_2, Z_1, Z_2[1]	±25V	*
Operating Temperature Range	−25°C to +85°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, Soldering	60sec, +300°C	*
Thermal Resistance, θ_{JC}	22°C/W	*
Thermal Resistance, θ_{JA}	90°C/W	*

NOTES
*Same as AD639A,B Specifications
[1]These inputs are purely resistive and the maximum inputs are determined by resistor dissipation limits, not the supply voltages.

$\sin(\theta)$	$= \frac{\sin(\theta)}{1} = \frac{\sin(\theta-0)}{\sin(90°-0)}$		$\text{cosec}(\theta)$	$= \frac{1}{\sin(\theta)} = \frac{\sin(90°-0)}{\sin(\theta-0)}$	
$\cos(\theta)$	$= \frac{\cos(\theta)}{1} = \frac{\sin(90°-\theta)}{\sin(90°-0)}$		$\sec(\theta)$	$= \frac{1}{\cos(\theta)} = \frac{\sin(90°-0)}{\sin(90°-\theta)}$	
$\tan(\theta)$	$= \frac{\sin(\theta)}{\cos(\theta)} = \frac{\sin(\theta-0)}{\sin(90°-\theta)}$		$\text{cotan}(\theta)$	$= \frac{\cos(\theta)}{\sin(\theta)} = \frac{\sin(90°-\theta)}{\sin(\theta-0)}$	

Table I.

Principles Of Operation

Figure 1 is a functional equivalent of the AD639, intended to assist in understanding and utilizing the device: it is not a literal representation of the internal circuitry[1]. Two similar sine-shaping networks accept input voltages X_1, X_2, Y_1 and Y_2, proportional to the corresponding angles x_1, x_2, y_1 and y_2, with a scaling factor of 50°/V (20mV/°).

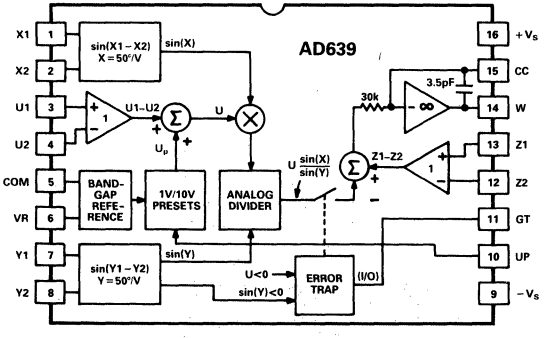


Figure 1. Equivalent Block Schematic of the AD639

The first of these networks generates an output proportional to the sine of $x = (x_1 - x_2)$ over a useful operating range in excess of −500° to +500° (see Figure 3). The accuracy of the function over the central ±180° is excellent, a consequence of the optimized network design, further enhanced by precision laser wafer trimming during manufacture. The output of the X-network is multiplied by the amplitude-control voltage, U. This may be provided by applying inputs to U1 or U2, or pre-selected to be 1V or 10V by a control input to UP, or in combination; that is, the function amplitude is $U = (U_1 - U_2) + U_p$.

The second network generates an output proportional to the sine of $y = (y_1 - y_2)$. Although the X and Y networks are similar, other design considerations result in a smaller angular range for the Y-input. The principal range is from 0° to +180°; in the adjacent ranges (+180° to +360° and 0° to −180°) the error trap is activated.

The ratio of the two sines is generated by *implicit* division, rather than by use of a separate analog divider as indicated in Figure 1, and is summed with the voltage $Z = (Z_1 - Z_2)$. The difference is applied to the high-gain output op-amp. In the *normal* modes (see below) Z1 is connected to the output W, and Z2 is grounded. Under these conditions, the function is

$$W = U \frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)}$$

Either sine function can be converted to the cosine by applying the input to X2 or Y2 and introducing a +90° offset, since

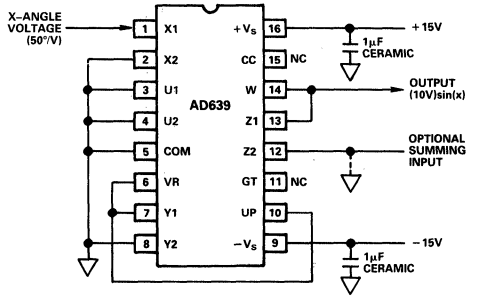


Figure 2. Connections for the Sine Mode with Amplitude Preset to 10V

[1]For details of the sine-network theory and design, see "A Monolithic Microsystem for Analog Synthesis of Trigonometric Functions and their Inverses," Barrie Gilbert, *IEEE Journal of Solid-State Circuits*, Vol. SC-17, No. 6, Dec. 1982, pp 1179-1191. Reprints available.

$\cos(\theta) = \sin(90° - \theta)$. For example, by connecting the +1.8V reference output at pin 6 (VR) to X1 and the angle voltage, V_θ, to X2 the numerator becomes the cosine of angle θ. Alternatively, by connecting VR to either X1 or Y1 and grounding X2 or Y2, the numerator or denominator, respectively, becomes unity, since $\sin(90° - 0) = 1$. By these means, the full set of *normal* functions shown in Table I can be generated. All functions can be sign-inverted by interchanging the X-inputs. The Z2 input can be used to sum another function to the output, W, with unity gain.

In addition to the *normal* modes providing sine, cosine, tangent, cosecant, secant and cotangent functions, the AD639 can generate the *offset* functions such as the versine, $1 - \cos(\theta)$, discussed below. The *inverse* functions such as arc-sine, arc-cosine and arc-tangent, are also supported by the AD639, by closing the feedback loop through the corresponding *normal* function. The output angle is limited to the principal range (for example, −90° to +90° for the arc-sine and arc-tangent, 0° to +180° or −180° to 0° for the arc-cosine).

TERMINOLOGY

When discussing a device having as many inputs and operating modes as the AD639, it is important to clarify the nomenclature and scaling conventions. In all cases *angles* are denoted by lower-case letters (x, y, θ) and have the dimension of angular degrees. Upper-case letters (A, V, U, W, X, Y and Z) refer to *voltages*; subscripts are used to refer to one or the other of a differential pair such as $X_1 - X_2$, or the preset value U_p. Numbered upper-case letters refer to the variable name or the package pin.

THE ANGLE INPUTS: X1, X2, Y1, Y2

The angles $x = (x_1 - x_2)$ and $y = (y_1 - y_2)$ are directly proportional to the differential voltages $X = (X_1 - X_2)$ and $Y = (Y_1 - Y_2)$ respectively, with a scaling factor of 50°/V. The X-inputs can be driven to ±12V pk, that is ±600°. The Y-input should be limited to 0 to +3.6V (0° to +180°) to satisfy certain internal requirements. The resistance at these inputs is nominally 3.6kΩ to COM.

The sine function exhibits odd-order symmetry: $\sin(-\theta) = -\sin(\theta)$. By simply interchanging the X-inputs, the overall sign of any function can be inverted. The Y-inputs can also be interchanged to allow operation with a negative input voltage (0 to −3.6V) while maintaining the correct angular range.

It may occasionally be desirable to reduce the angular scaling factor. For example, to convert a triwave of ±10V amplitude into a continuous sinewave requires a scaling factor of 9°/V (since ±10V corresponds to ±90°). This can be achieved by using a resistor (in this case, about 16.4kΩ) in series with the X1 input; a resistor of equal value must be inserted in series with the X2 input to minimize angular offset error. Note that the on-chip thin-film resistors are not trimmed to absolute value, so a scaling adjustment is needed; however, once set, scaling will be stable.

THE AMPLITUDE-CONTROL INPUTS: U1, U2, UP

The amplitude of the function can be determined either by the application of an external voltage to the U1 and U2 inputs, or by enabling the internal preset voltage U_p by taking the control pin UP low or high, or via a combination of these modes. The net amplitude is $U = (U_1 - U_2) + U_p$. This sum must be greater than zero and less than $|-V_s|$; voltages beyond these limits activate the error trap.

In the external mode, the differential voltage $(U_1 - U_2)$ will generally be in the range 10mV to 10V. Positive inputs are applied to U1 while U2 is grounded; for negative inputs, interchange U1 and U2. The input resistance at U1 and U2 is nominally 50kΩ to analog common. A nominal bias current of −50μA is needed at the U-inputs; zero-valued inputs must therefore be connected to common to prevent offset error. The gain from the U-interface to the output is trimmed to be unity for $\sin(x)/\sin(y) = 1$. The effective gain can be lowered using a series resistor; to avoid offset an equal resistor must be used in the zero-valued input.

The UP control pin may be left unconnected (or grounded) to disable the internal amplitude preset, connected to $+V_s$ to set $U_p = 10V$, or to $-V_s$ to set $U_p = 1V$. An external resistor of 75kΩ ($\pm V_s = 5V$) to 360kΩ ($\pm V_s = 15V$) can be inserted in series with UP (which also has an input resistance of typically 50kΩ) to minimize power dissipation. Alternatively, V_r can be used to enable $U_p = 10V$ for ambient temperatures below +60°C. The UP input can be used to switch the output on or off under logic control, but requires a relatively long response time. The GT interface is more suitable for this purpose and it allows gating to any amplitude, U not just to the preset values of 1V or 10V.

THE REFERENCE OUTPUT: VR

The voltage V_r is laser-trimmed to +1.8V with respect to analog common. It can be used to fix the angle x or y to 90° and thus set sin(x) or sin(y) to unity. It can also provide a 90° offset to convert the numerator or denominator to a cosine function. Stable offsets less than 90° may be introduced using a voltage-dividing series-resistor (nominally 3.6kΩ for 45°). V_r can also be used as the amplitude input voltage $U_1 - U_2$, or as a convenient control input to set $U_p = 10V$ for ambient temperatures below +60°C. This output is short-circuit protected and can provide up to 4mA total load current.

THE ERROR-TRAP AND GATE: GT

In some applications it may be useful to know that the output is severely in error due to a dynamic combination of inputs. For example, the tangent, cotangent, secant and cosecant all exhibit regions where the function increases sharply for small angular changes, and the output may easily saturate. Consider the case where (10V) tan (θ) is being generated. W is 10V for θ = 45°, and the theoretical output of 17.3V at θ = 60° cannot be achieved using ±15V supplies. Likewise, the output is invalid whenever the angle y is outside of a valid range (principally 0 to +180°), or when $U < 0$ or $U > |-V_s|$. Under such conditions the AD639 generates a HIGH output at pin 11 and simultaneously clamps the analog output to zero (in fact, to the voltage Z_2). Grounding GT disables the error trap.

The GT pin may also be used as an *input* to gate the function output. This is achieved by raising pin 11 to a voltage above +1.5V. Response time is typically 500ns for a logic drive of 0 to +2V, and the ON/OFF ratio is greater than 83dB when used as a continuous-wave sine converter with a single-sided ±1.8V triwave drive at frequencies up to 10kHz, or 63dB at 100kHz; the feedthrough is entirely capacitive, and is equivalent to 5pF between X1 or X2 and the op-amp summing node. Feedthrough can be minimized by using a balanced drive to X1 and X2.

Operation in Normal Modes

In *normal* modes, the Z-input establishes a feedback path around the output op-amp, by connecting Z1 to the output, W, and Z2 to the ground associated with the load circuit. For the highest accuracy Z1 can be used to sense the output at the load terminals. Similarly, zero-valued angle inputs and the angle common (pin 5) should be connected to the ground associated with the source circuitry.

SINE MODE

The AD639 can generate either (1) a low-distortion continuous sinewave from a repetitive triwave input or (2) a high-accuracy sine function for use in computational applications. In most cases, the choice of preset or externally-controlled amplitude will make little difference to distortion or accuracy, and both methods are used in this section. In all of the *normal* modes, the Z2 input can be used either to sum a further signal to the output (or introduce an optional output offset trim). The denominator is set to unity by making $y = 90°$, using the $+1.8V$ output. Figure 2 shows typical connections. The 10V preset is selected, using V_r as a control input to UP, and the ideal output is (10V)sin(x). In practice, five basic types of error arise:

1. *X-angle scaling error*: The amount by which the angle generated for each volt of X-input differs from 50°. In triwave-to-sinewave (CW) applications this introduces odd-order harmonic distortion, and is indistinguishable from an incorrect triwave amplitude.
2. *X-angle offset error*: The actual angle generated when $X = (X_1 - X_2) = 0$. In CW applications this introduces even-order harmonic distortion, as a non-zero mean in the triwave would.
3. *Amplitude scaling error*: The amount by which the peak-to-peak amplitude of the sinewave differs from the ideal value, U/sin(y). This error is usually critical only in computational applications. Errors associated with the Y-network also affect the amplitude in the sine mode.
4. *Output offset error*: The amount by which the *mean value* of the sinewave differs from zero (strictly, the voltage on Z2). This error is only important in computational applications. Note that the output may also be non-zero due to angular offset on the X-input. For example, the typical specified X-angle offset of 0.1° introduces an output error of 17.45mV when U/sin(y) = 10V, more than three times the specified mean offset component of 5mV.
5. *Law-conformance error*: The residual deviation between the output function and the ideal function when all of the above errors have been removed by trimming during manufacture or further external trimming, limiting the ultimate accuracy of the function.

Figure 3 shows the function when driven well beyond the specified angular range, using a differential X-input of ±18V peak. This also shows the AD639's ability to drive ±15V into a 600Ω load, with supplies of ±18V. Using an accurate data-acquisition system the output can be compared to a computer-generated sine function. When the first four types of errors are trimmed out, the peak error over the full input range is typically less than 0.5%. Over the central $-90°$ to $+90°$, the peak law-conformance error is typically only 0.02%. Figure 4 shows the law conformance for four typical samples of AD639. The differential signal interfaces simplify the inclusion of optional offset correction to any of the variables.

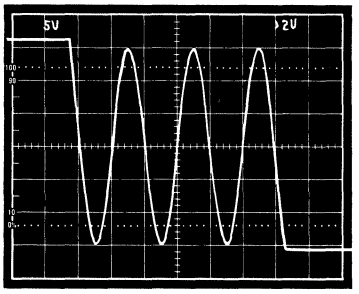


Figure 3. Output Function for Peak X-Input of ± 18V, with U = 15V, R_L = 600Ω ($\pm V_S$ = 18V)

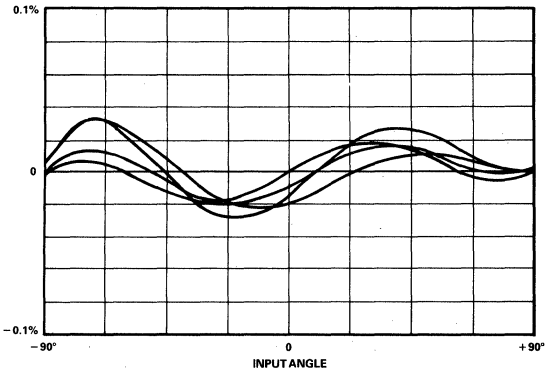


Figure 4. Residual Error Over Central 180° Using External Trimming

HARMONIC DISTORTION

The AD639 can generate continuous sinewaves of very low distortion using a linear, highly-symmetric triangle-wave of ±1.8V amplitude. Imperfections in the triwave will cause the following errors:

1. *Incorrect amplitude*: This causes odd-order distortion. Each 1% error (either too large or too small) generates 0.25% of HD3, 0.0833% of HD5 and a total harmonic distortion (THD) of 0.27% (−51.42dBs).
2. *Baseline offset*: This causes even-order distortion. Each millivolt of offset in a 1.8V triwave generates 0.037% of HD2, 0.0074% of HD4 and a THD of 0.038%, as well as a DC offset of 0.055% of the output amplitude.
3. *Time-asymmetry*: The run-up time, t_1, and run-down time, t_2, of the triwave may be unequal. This causes both odd- and even-order harmonics. Let the asymmetry in percent be $p = 100(t_1 - t_2)/(t_1 + t_2)$. The even-order terms are proportional to p; the odd-order terms increase as p^2. A 1% time-asymmetry generates 0.57% of HD2, 0.00625% of HD3, 0.043% of HD4 and 0.00167% of HD5, and a THD of −44dBs. There is no DC term.
4. *Amplitude-nonlinearity*: This can take on many forms, such as an exponential nonlinearity in the triwave, amplitude compression, and so on. Distortion can be calculated for various special cases. Fortunately, it is fairly easy to avoid these types of imperfections in the triwave generator using appropriate design methods.

When triwave errors are minimized, harmonic distortion can be as low as 0.01%. Figure 5 shows the output spectrum at 10kHz, with an output amplitude of 20V pk-pk and a load resistance of 10kΩ. An HP3325A synthesizer/function generator was used to produce the triwave. Distortion rises only slightly when using the minimum specified load of 2kΩ; in fact, the AD639 can drive loads down to 600Ω. At $\pm V_s = \pm 18V$, sine amplitudes of ±15V (10.6V rms, or 225mW of load power) can be generated, with typically 0.03% HD2 and HD3.

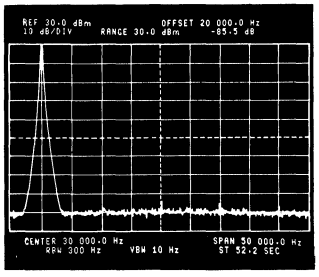


Figure 5. Spectrum of 10V Sine Output at 10kHz; HD2 = −88dBs, HD3 = −85.5dBs

COSINE MODE

The cosine function is generated by offsetting the sine by 90° using V_r. The X-input is connected to X2 and VR to X1; then

$$W = U \frac{\sin(90° - x)}{\sin(90° - 0)} = U \cos(x)$$

Connections for the cosine are shown in Figure 6; the amplitude in this case is determined externally, by way of illustration. The angular range now extends from −400° to +600°, with highest accuracy between 0° and +180°.

TANGENT AND COTANGENT MODES

The tangent function is provided by the connections shown in Figure 7. The angle voltage, corresponding to θ, is applied both to the numerator, set to the sine mode, and the denominator, set to the cosine of the same angle:

$$W = U \frac{\sin(\theta - 0)}{\sin(90° - \theta)} = U \frac{\sin(\theta)}{\cos(\theta)} = U \tan(\theta)$$

Most applications require accurate operation for angles up to nearly ±90° and accordingly U is preset to 1V (rather than 10V). Under these conditions, W = 1V when θ = 45° and 11.43V when θ = 85°. Using 15V supplies, the output op-amp will be unable to generate the tangent much beyond this point: at only 86° it would theoretically need to reach 14.3V. For an input exceeding 90° in either direction the denominator becomes negative, and the error trap is enabled. Figure 8 shows the function for inputs up to ±2.5V (±125°).

The errors associated with the sine mode, (see above) apply to the tangent mode also, but the total error in the tangent, cosecant, secant and cotangent modes (when the Y-input is also varied) are higher, since the Y network is not trimmed and the angular

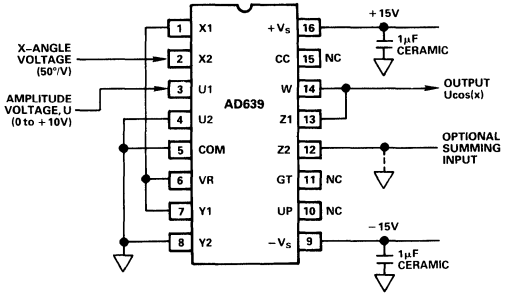


Figure 6. Connections for the Cosine Mode with External Amplitude Control

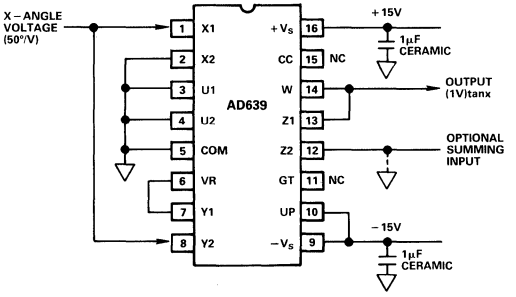


Figure 7. Connections for Tangent Mode with Amplitude Preset to 1V

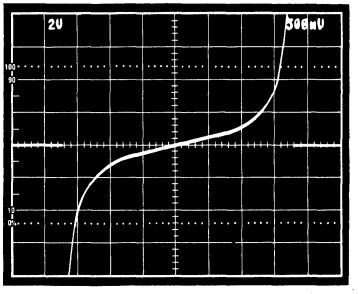


Figure 8. The Tangent Output for Angle Inputs Up to ±125° (Error Trap Activated Above 85°)

scaling and offset errors of this network are absorbed during trimming of the output in the sine mode.

The cotangent is generated by interchanging numerator and denominator. The principal range is now from 0 to +180°, and the output (1V)cot (θ) ranges from +11.43V at θ = 5°, through zero at θ = 90°, to −11.43V at θ = 175°.

SECANT AND COSECANT MODES

In secant and cosecant modes, the numerator is fixed to unity by connecting X1 to VR and X2 to analog common. For the secant, angle voltage A is connected to Y2 and Y1 is tied to VR; then

$$W = U\frac{\sin(90°-0)}{\sin(90°-\theta)} = U\frac{1}{\cos(\theta)} = U\sec(\theta)$$

The principal range is $-90°$ to $+90°$. The most practical amplitude scaling is provided using the U-preset of 1V, when the output ranges from $+11.47V$ at $\theta = -85°$ and $+85°$, to $+1V$ at $\theta = 0$. The cosecant differs only slightly: the angle input is connected to Y1 and Y2 is connected to analog common, making the denominator sin (θ). The principal range is now 0 to $+180°$. When $U = 1V$ the output is $+11.47V$ at $\theta = +5°$ and $+175°$, and $+1V$ at $\theta = 90°$.

OFFSET MODES

The versine, vers $(\theta) = 1 - \cos(\theta)$, coversine, covers $(\theta) = 1 - \sin(\theta)$, and exsecant, exsec $(\theta) = 1 - \sec(\theta)$ involve the addition of a constant term to one of the normal trigonometric functions. These can be generated with the AD639 using the Z2 input to add a voltage to the output proportional to the amplitude of the basic function. In the versine and coversine modes this is simply the same voltage as applied to U1 (U2 grounded) to set up the amplitude of the sign-inverted cosine or sine function, respectively:

$$W = U - Uf(\theta) = U(1 - f(\theta))$$

In these two modes the output starts at zero and has a peak value of twice the amplitude voltage, U.

For the exsecant a *negative* voltage is added at Z2 and this same voltage is applied to U2 with U1 grounded; this satisfies the requirement that the sign of $U_1 - U_2$ be positive. (See comments on the Amplitude Control Inputs). The angle inputs are set up for the secant; the principal range is still $-90°$ to $+90°$, but the output is now zero when the input angle is zero.

OPERATION AT LOW SUPPLY VOLTAGES

The signal ranges at the angle interfaces are essentially independent of the supply voltages. In almost all cases, the primary limitation to the function's range will arise at the output, W, which can swing to within approximately 2V of either supply. For example, the X-input may have a peak value of $\pm 12V$ ($\pm 600°$) even when using $\pm 5V$ supplies.

Inverse Function Modes

The AD639 generates the inverse trigonometric functions by closing the feedback loop around the output op-amp through the *angle* inputs, rather than through the Z-interface, resulting in a nonlinear feedback system. To understand this, note first that the *general* transfer function (with UP disabled) is

$$W = A_{OL}\left[(U_1 - U_2)\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} - (Z_1 - Z_2)\right]$$

where A_{OL} is the open-loop gain of the output op-amp (typically 85dB). Provided that the overall feedback remains negative, the loop can be closed in many ways, so as to force the quantity inside the brackets to a null, when

$$\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} = \frac{(Z_1 - Z_2)}{(U_1 - U_2)}$$

whatever combinations of variables are used to set up the feedback path. In particular, when the *angle* inputs are used the system will have one of the *normal* functions in the feedback path. The input to this system is now the *ratio* (Z/U), and the output is a voltage corresponding to the angle generated by the *inverse* of the function in the feedback path.

Since all of the normal functions are periodic, and the maximum value of the op-amp output can be equivalent to angles as large as $\pm 650°$, the closed-loop system could arrive at false "solutions" to the above equation, that is, at angles outside of the principal range. Also, the feedback can become positive in the wrong angular range, causing latch-up. Hence, it is essential to limit the magnitude of the feedback voltage. Ideally, this is done using precise active clamps, but the saturated value of the output at given supply voltages, in combination with a simple resistive divider to the angle inputs, is usually sufficient to limit operation to the principal range. The voltage at the angle inputs will be accurate, but the op-amp output will in general have inaccurate scaling and may show large offsets, due to the bias currents at the angle inputs. The error-trap should be disabled in the inverse modes by grounding GT.

ARCTANGENT MODE

The arctangent is the most useful of the inverse modes. With the connections shown in Figure 9 the loop solves the equation

$$\frac{\sin(0-\theta)}{\sin(90°-\theta)} = -\tan(\theta) = \frac{(Z_1 - Z_2)}{(U_1 - U_2)}$$

where θ is the angle corresponding to voltage A, scaled by 50°/V. It follows that

$$\theta = \tan^{-1}\frac{(Z_2 - Z_1)}{(U_1 - U_2)}$$

The reversal of Z_1 and Z_2 in the numerator is due to the negative sign in the tangent function. The numerator may be either positive or negative, and the connections can be interchanged to alter the overall sign of the function. The denominator must be positive, but U1 and U2 may be interchanged to accept a negative input voltage. The ability of the AD639 to form the ratio of two

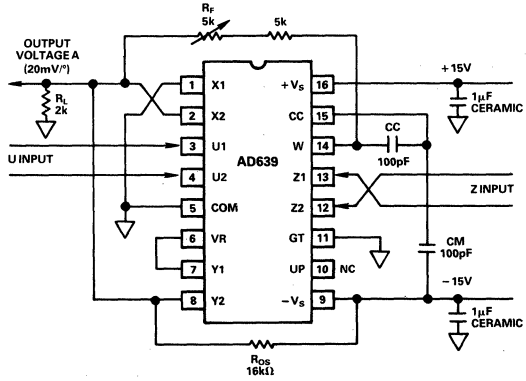


Figure 9. Connections for the General Arctangent Mode

variables prior to the arctangent operation is very useful in many applications, for example, in real-time Cartesian-to-polar conversion (see Applications section). The denominator can also be preset to 1V or 10V using the UP input; when U = 1V, the angle a is simply the arctangent of the voltage value of $Z_2 - Z_1$. Figure 10 shows an X-Y plot of the output for Z = −10V to +10V (horizontal axis of photograph) with four values of U (0.3V, 1V, 3V, 10V).

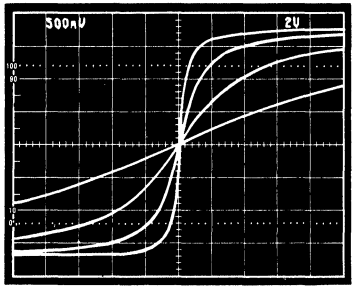


Figure 10. The Arctangent Output for Z = ± 10V and U = 0.3V, 1V, 3V and 10V

Range-Limiting and Loading

Resistor R_f in Figure 9 forms a divider with the parallel sum of the input resistance at X2 and Y2 and the load resistance, shown here as 2kΩ, which prevents the output angle voltage A from exceeding ±1.7V (θ = ±85°), using ±15V supplies. This voltage is not *directly* affected by the load resistance (that is, the output behaves as a low-impedance node) but the angular range limits are. Consequently, the nominal value of R_f should be calculated for specific values of load resistance, angular range and supply voltages, and a trim range of about ±10% included to set up the angle limits correctly. R_{os} is needed to compensate the input bias currents and thus equalize the clipping limits; it does not cause an offset in θ. The direct output at pin 14 is also the arctangent but with imprecise scaling. Although this can be trimmed by R_f there will also be a supply-dependent offset due to R_{os}. For these reasons, the direct output should not be used in this mode.

HF Compensation

The output op-amp is internally compensated to be stable in all the normal modes when feedback is via the unity-gain difference amplifier associated with the Z-interface. The dominant pole is determined by the 30kΩ resistor and on-chip 3.5pF capacitor (see Figure 1) for a closed-loop bandwidth of 1.5MHz. In the arc-tangent mode, however, the gain of the feedback path is much greater than unity for practical angle values and is theoretically unbounded. For example, if the forward path is set up to generate (1V)tan(θ), the incremental gain near θ = 0 is slightly less than unity (since a 20mV change in voltage A causes a change of (1V)tan(1°) or 17.5mV in output W) but at θ = 85° the gain is 115. While the resistive divider used to limit the angle voltage A will lower the loop gain, it can still exceed unity. The capacitors C_c and C_m in Figure 9 provide the HF compensation required for operation up to ±85°, with all values of U.

ARCSINE AND ARCCOSINE MODES

The basic principles for the arcsine and arccosine are similar to those described for the arctangent. As before, the argument of the function is the ratio (−Z/U), where U may be preset to 1V or 10V, the loop gain must be negative over the principal angular range of the output, and the feedback voltage must be limited to ensure that this range is not exceeded. The loop stability is easier to ensure, since the peak gain is bounded. With U = 10V the maximum incremental gain of the forward path (at 0° for the sine and +90° for the cosine) is 8.75 and the peak loop gain is much less than this because of the attenuation used to limit the angular range. Thus relatively little additional HF compensation is required.

Connections for the arcsine are similar to the arctangent (Figure 9) except that Y2 is grounded, and C_c and C_m can be reduced or even omitted. R_f is adjusted for a peak angular range of ±90° at the (attenuated) output; if too high, the function will still be correct, but the maximum angle will be less than 90°; if too low, the function will exhibit hysteresis near the peak output. Adjustments will be needed for other values of load resistance and supply voltages. Note that the general limitation on the amplitude input ($U <= |-V_s|$) must be observed. Figure 11 shows an X-Y plot of the arcsine output for Z = −10V to +10V (horizontal axis of photograph) with three values of U (2V, 5V and 10V). The arcsine can be inverted by reversing the Z-interface.

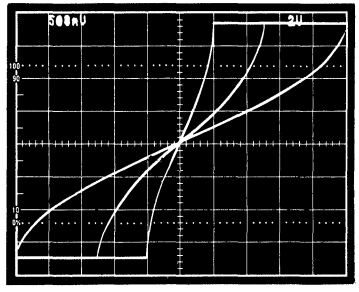


Figure 11. The Arcsine Output for Z = ± 10V and U = 2V, 5V and 10V

For the arccosine, use the arcsine connections with X1 tied to V_r and insert a small-signal diode in series with R_f, having its cathode on the angle-interface side. This allows the output to move only in a positive direction. Z1 now becomes the positive numerator input, and the principal range is from 0° (when Z/U = −1) to +180°. The function is similar in appearance to the arcsine, except for the +90° output pedestal and the reversal of phase along the horizontal axis. Note that

$$\cos^{-1}(Z/U) = 90° - \sin^{-1}(Z/U) = 90° + \sin^{-1}(-Z/U).$$

To generate the negative arccosine, reverse the X- and Z-interfaces and the polarity of the diode. The output now runs from −180° for an input of $Z = (Z_1 - Z_2) = -10V$ (with U = 10V) to 0° at Z = +10V.

It is strongly recommended that X-Y oscilloscope methods are used to investigate functional behavior during the development of any of these modes of operation: time-domain displays can easily become confusing.

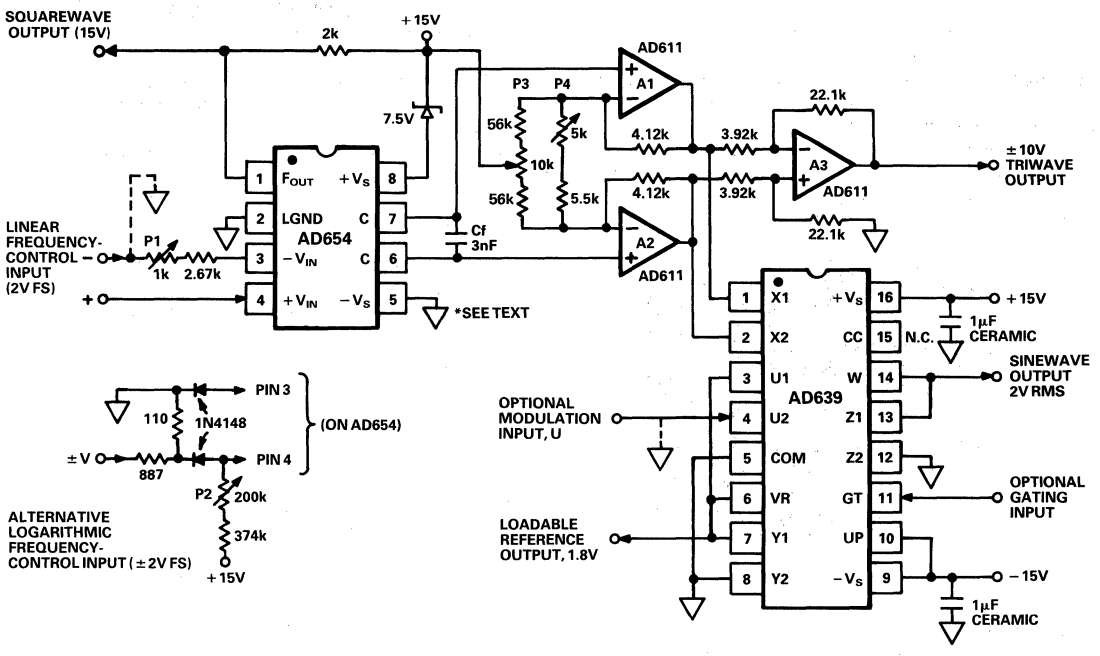


Figure 12. General-Purpose Function Generator

Applications

WIDE-RANGE WAVEFORM GENERATOR

Figure 12 shows an inexpensive signal generator, providing voltage control of frequency from 20Hz to 20kHz and a pre-set sine amplitude of 2.8V (within 0.1dB of 2V rms). This output may be further modulated by an input of up to ±2.8V to U2, or gated off by an input of +1.5V or more to GT; Figure 13 shows the gated response. If required, a further input can be summed into Z2. The sine output can be set to 10V amplitude by connecting UP to VR and grounding U1.

An AD654 is used to generate the triwave which appears across the timing capacitor C_f, and is buffered, amplified and level-shifted by A1 and A2. Using a spectrum analyzer, P3 and P4 are adjusted to minimize even- and odd-harmonic distortion, respectively. The triwave linearity is not good enough to realize the inherent capabilities of the AD639, but total harmonic distortion is in the −50dB to −60dB range. A3 provides further gain for a ±10V triwave output. The square-wave output is taken directly from the AD654 and is unbuffered. It swings between ground and +15V; if pins 2 and 5 of the AD654 are connected to −15V, this output is 30V pk-pk.

The frequency scaling with the linear input (shown) is 10kHz/V, calibrated using P1. The frequency can be controlled manually, using a potentiometer and the V_r output of the AD639. P1 has sufficient trim range to provide a full-scale frequency of 20kHz with the 1.8V peak input. The alternative input scheme provides a "log-sweep" response with an approximate scaling of 10^V kHZ (when V is in volts). The range is now from about 10Hz to 100kHz; the frequency should be set to 1kHz with V=0, using P2. The frequency is now sensitive to variations in both temperature and the +15V supply, but stability will be adequate for many applications.

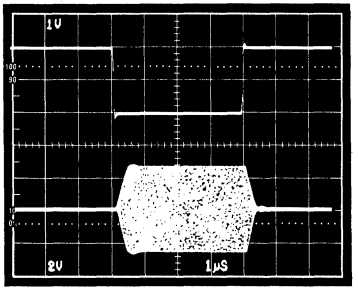


Figure 13. Gated Output. Top Trace: 0 to +2V Gate Input. Bottom Trace: 2V rms Gated Sine Output

Frequency Multiplication

Because of the exceptionally wide angular range of the numerator function of the AD639, it is possible to generate sinewave outputs with 2, 3, 4 or 5 times the triwave frequency using the cosine mode for even multiples or the sine mode for odd multiples.[2] For example, to multiply the output frequency by 3, use the sine function with the X-input driven to ±5.4V (±270°). Distortion remains low; all harmonics are typically under −50dBs, even for the frequency-quintupling mode.

[2]For full details see "A Remarkable Monolithic Microsystem Generates Trigonometric Functions," Barrie Gilbert, *Industrial Electronics Equipment Design*, September 1984, pp. 19-24. Reprints available.

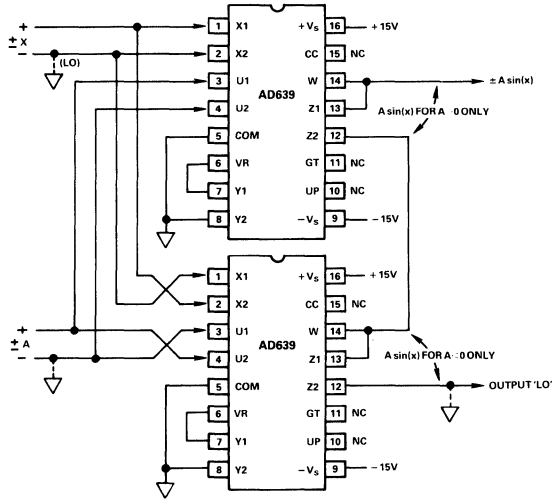


Figure 14. Four-Quadrant Sine Multiplier; for Cosine, Interchange X1 and X2 and Connect Angle 'Lo' Input to VR

FOUR-QUADRANT SINE/COSINE MULTIPLICATION

In synchro applications it is often necessary to multiply an AC sinusoidal 'carrier' by a further sine 'modulation' function. This can be achieved in two ways; the first is suitable only when there is a large ratio between the carrier frequency and the modulation frequency. Using a single AD639, the carrier input Asin(ωt) is applied to U2, and a DC bias voltage established on U1 (which can be provided by a series resistor connected to $+V_s$). The modulation input, x, is applied to angle inputs connected for $-\sin(x)$. The output is then $W = -\sin(x)(U_1 - A\sin(\omega t))$. Using AC-coupling to the load, the voltage Asin(x)sin(ωt) results. Since the peak value of W is $(U_1 + A)$, a maximum of about 6V amplitude can be achieved before output saturation. A further limitation of this approach is that the AC-coupling may allow excessive transmission of the sine modulation function. However, with typical values of 400Hz for the carrier and 10Hz for the upper modulation frequency, this simple approach is practical. Cosine modulation is similarly achieved.

An alternative method is DC-coupled and thus imposes no frequency-ratio limitations; it also allows an input/output amplitude of up to 12V. Two AD639s are used (Figure 14), the second having both the X- and U-interfaces phase-inverted relative to the first, and the two outputs are summed. The figure shows a general bipolar input, A, applied to the U-inputs. The first device generates Asin(x) when A is positive and zero when A is negative. The second device generates $-A\sin(x)$ (actually $A\sin(-x)$) when A is negative and zero when A is positive. The instantaneous sum of the two half-sines is Asin(x). The switching speed of the U-interface is adequate to handle a sinusoidal input $A = (10V)\sin(\omega t)$ at frequencies up to at least 1kHz, without significant crossover distortion. In synchro applications errors as small as 5 arc-minutes can be achieved.

Polar-to-Cartesian Conversion

Using a pair of AD639s connected as shown in Figure 14, and a second pair connected similarly for the cosine function, a vector of magnitude A and angle x can be resolved into its orthogonal components Asin(x) and Acos(x), with unrestricted operation in all quadrants and very high accuracy.

Cartesian-to-Polar Conversion

A point Z,U in a plane can be converted to a magnitude component, A, and an angle component, θ. A suitable vector summation circuit can be found in the AD637 data sheet. The AD639 in the arctangent mode can provide the angle output $\theta = \tan^{-1}(Z/U)$. If U is bipolar, an absolute-value circuit using an AD630 should be added.

11

Sine/Cosine (Quadrature) Oscillators

Quadrature oscillators generate a pair of sinusoudal outputs displaced by 90°, and invariably are based on a "state-variable" loop consisting of two integrators and a sign-inverter. Practical difficulties in this approach are (1) considerable additional circuitry is required to control the amplitude of the oscillation; (2) a trade-off arises between the settling-time of this control circuitry and the distortion level, particularly troublesome at low frequencies; (3) the amplitude balance of the two outputs is dependent on the matching of two time-constants; (4) two tracking analog multipliers or multiplying DACs are needed if the frequency is to be programmable.

These problems are avoided using a function-shaping technique based on a triwave oscillator, which requires only one time-constant, and whose frequency can thus be more easily controlled. The need for an amplitude control system is eliminated using the scheme shown in Figure 15. The two outputs have accurate amplitudes of 10V (without the need for an external reference source) or can be individually controlled by external voltages, without any effect on frequency. Variable-amplitude sine and cosine outputs can be added (using the Z-input discussed earlier) to provide continuously-variable phase-control of the output.

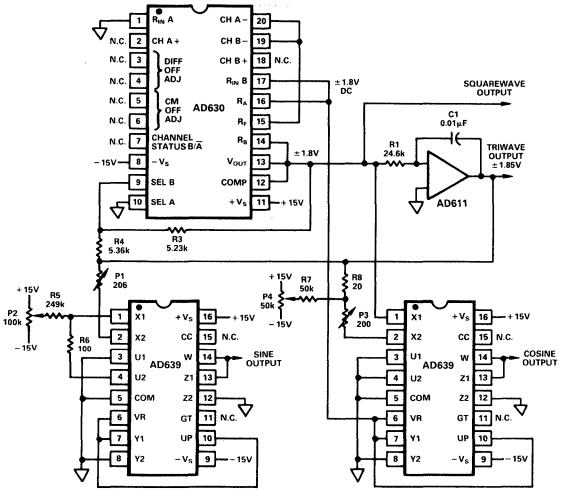


Figure 15. Quadrature Oscillator

The triwave oscillator comprises an AD630, which alternates the sign of the 1.8V reference from one of the AD639s to generate a square-wave output of ±1.8V amplitude, and an integrator formed by R1, C1 and the op-amp, which generates the triwave. The amplitude of the triwave is determined by the ratio of R3 and R4, and is nominally ±1.845V, 2.5% higher than needed at the inputs of the AD639s, providing the adjustment range needed to minimize distortion. In many applications, all adjustments can be eliminated; to do this, make R3 = R4 = 5kΩ, omit P2, P4, R5 and R7 and replace P1, P3, R6, and R8 with short circuits. The frequency is nominally $1/4C_1R_1$, and is 1kHz with the component values shown. A variety of methods may be used to provide external control of frequency, including the use of another AD630 in series with R1, or the use of a multiplying DAC.

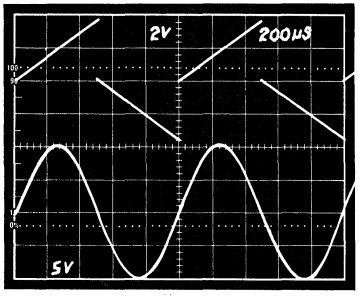


Figure 16. Top Waveform: Difference Voltage Between Triwave and Squarewave. Bottom Waveform: Resulting Output

The sine output is generated using the triwave directly. P1 and P2 should be adjusted using a spectrum analyzer for minimum odd-order and even-order harmonics, respectively. The cosine output is generated by using the *difference* between the triwave and the square-wave, shown in the upper waveform in Figure 16. This composite voltage first generates a sine-function over the range 0 to +180°, then over the range 0 to −180°, to produce the function shown in the lower waveform, which can be seen to be 90° out of phase with the triwave. The complete set of waveforms available from this generator are shown in Figure 17.

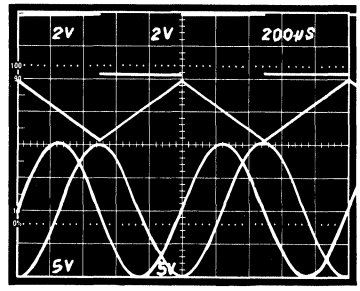


Figure 17. Timing Relationships Between All Outputs of the Quadrature Oscillator

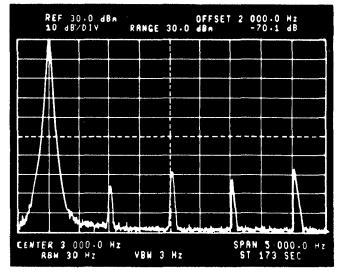


Figure 18. Spectrum of Cosine Output at 1kHz

P3 and P4 are adjusted for minimum odd-order and even-order cosine harmonics, respectively; Figure 18 shows the cosine spectrum for a well-adjusted circuit.

Due to the finite transition time back to the baseline in the drive voltage to the cosine generator, a brief spike occurs at the zero-crossing of this output. The frequency components will be beyond the bandwidth of the output amplifier in the AD639, and the energy contained in these spikes will not generally be troublesome. They may be further reduced, if necessary, by adding a capacitor between pins 14 and 15, to roll off the AD639 output response.

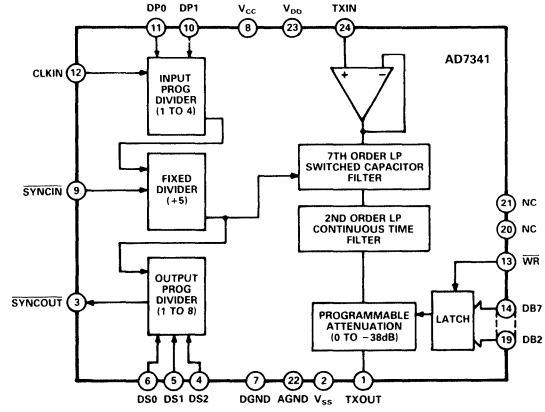
LC²MOS Voiceband Reconstruction and Antialiasing Filter Set

AD7341/AD7371

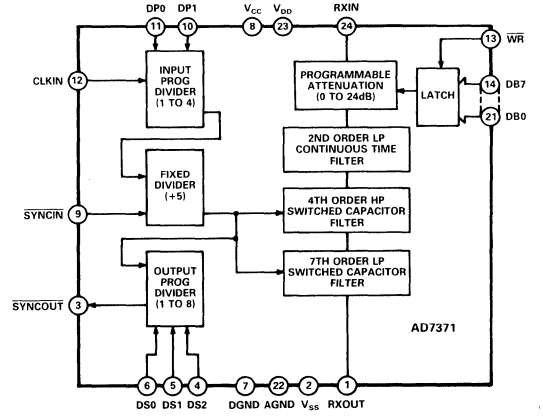
FEATURES

AD7341 – Transmit (Reconstruction) Filter for 14-Bit DAC (AD7840)
Programmable Attenuation (0dB to −38dB)
AD7371 – Receive Filter for 14-Bit ADC (AD7871)
Programmable Gain (0dB to 24dB)
70dB Stopband Attenuation
75dB In-Band Signal-to-Noise Ratio
Better Than −75dB Total Harmonic Distortion
CCITT V.32 and V.33 Compatible
Small, 0.3", 24-Pin Plastic Package and 28-Pin PLCC

AD7341 FUNCTIONAL BLOCK DIAGRAM



AD7371 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7341 and AD7371 are reconstruction and antialiasing filters designed for use in high speed voiceband modems with speeds up to 14.4 kbits/sec, in accordance with CCITT V.32 and V.33 recommendations. These filters, along with the AD7840 DAC, the AD7871 ADC and a digital signal processor (DSP) can be used to implement a complete modem.

The AD7341 is the transmit or reconstruction filter. It implements the filter function using a seventh order low pass switched capacitor filter and a second order low pass continuous time filter. The cutoff frequency is 3.5kHz.

The AD7371 is the receive filter. It is a high order bandpass filter with a lower cutoff frequency of 180Hz and an upper cutoff frequency of 3.5kHz. The filter function is implemented using a second order low pass continuous time filter, a fourth order high pass switched capacitor filter and a seventh order low pass switched capacitor filter.

11

SPECIFICATIONS

TRANSMIT FILTER[1] (V_{DD} = V_{CC} = 5V ±5%; V_{SS} = −5V ±5%; AGND = DGND = 0V; CLKIN = 288kHz (M/S Ratio = 40/60 to 60/40. T_A = +25°C. Attenuator set at 0dB, unless otherwise stated.)

Parameter	AD7341JN AD7341JP	Units	Test Conditions/Comments
INPUT CHARACTERISTICS			
Input Signal Range	±3	V max	
Input Impedance	100	MΩ typ	
FILTER CHARACTERISTICS[2,3]			
CLKIN Frequency	288	kHz	N1 = 1 (i.e., DP0 = 1, DP1 = 0)
Cutoff Frequency	3.5	kHz	0.1dB Down from the Lowest Point in the Passband
Second Harmonic	−80	dB typ	
Third and Higher Harmonics	−80	dB typ	
Passband Ripple	0.4	dB max	0≤f≤3.3kHz
Passband Gain Error	±0.5	dB max	Deviation from Nominal Setting on Programmable Attenuator
Signal-to-Noise Ratio	72	dB min	0≤f≤3.5kHz
	75	dB typ	SNR Includes Noise and Harmonics
	70	dB typ	Attenuator Set at −30dB, 0≤f≤3.5kHz
Stopband Rejection	70	dB min	f≥6.1kHz
Differential Group Delay	350	µs typ	0≤f≤3.3kHz and Referenced to the Absolute Group Delay at 1kHz
OUTPUT CHARACTERISTICS			
Output Voltage	±3	V max	R_L = 3kΩ, C_L = 100pF
Offset Voltage	±70	mV max	
Attenuation Range	0 to −38	dB	Determined by DB2–DB7, See Table III
Relative Accuracy[3,4]	±0.1	dB typ	
Output Resistance	0.2	Ω typ	
LOGIC INPUTS			
$\overline{WR}$, DB2–DB7, DP0, DP1, DS0–DS2, $\overline{SYNCIN}$, CLKIN			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
CLKIN Divider Range (N1)[5]	1 to 4		CLKIN Can Be Set to 288kHz, 576kHz, 864kHz or 1.152MHz. N1 Is Set by DP0, DP1.
LOGIC OUTPUTS $\overline{SYNCOUT}$[6]			
Divider Range (N2)	1 to 8		N2 Is Set by DS0–DS2.
Frequency	$f_{CLKIN}/(N1\times5\times N2)$	kHz	
Pulse Width	$1/f_{CLKIN}$	µs	
V_{OH}, Output High Voltage	2.4	V min	I_{SOURCE} = 400µA
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6mA
POWER SUPPLIES			
V_{DD}	4.75/5.25	V min/V max	
V_{CC}	4.75/5.25	V min/V max	
V_{SS}	−4.75/−5.25	V min/V max	
I_{DD} + I_{CC}	25	mA max	
I_{SS}	25	mA max	
Power Dissipation	265	mW max	

NOTES

[1]Operating temperature ranges as follows: J versions: 0 to +70°C.

[2]Specified for an input frequency of 288kHz. This is internally divided by 5 to produce a switched capacitor filter frequency of 57.6kHz. For input frequencies lower than 288kHz, the filter response is shifted down by the ratio of this input frequency to 288kHz.

[3]Measured using a ±3V, 1kHz sine wave.

[4]Measured over the full attenuation range.

[5]Required to derive internal frequency of 288kHz from CLKIN.

[6]Determined by data transmission rate.

Specifications subject to change without notice.

RECEIVE FILTER[1] ($V_{DD} = V_{CC} = 5V \pm 5\%$; $V_{SS} = -5V \pm 5\%$; AGND = DGND = 0V; CLKIN = 288kHz M/S Ratio = 40/60 to 60/40. $T_A = +25°C$. PGA set at 0dB, unless otherwise stated.)

Parameter	AD7371JN AD7371JP	Units	Test Conditions/Comments
INPUT CHARACTERISTICS			
Input Signal Range	±3	V max	
Input Impedance	10	kΩ typ	
FILTER CHARACTERISTICS[2,3]			
CLKIN Frequency	288	kHz	N1 = 1 (i.e., DP0 = 1, DP1 = 0)
Lower Cutoff Frequency	180	Hz	0.1dB Down from the Lowest Point in the Passband
Upper Cutoff Frequency	3.5	kHz	0.1dB Down from the Lowest Point in the Passband
Second Harmonic	−80	dB typ	
Third and Higher Harmonics	−80	dB typ	
Passband Ripple	0.4	dB max	200Hz≤f≤3.3kHz
Passband Gain Error	±0.5	dB max	Deviation from Nominal Setting on PGA
Signal-to-Noise Ratio	72	dB min	180Hz≤f≤3.5kHz
	75	dB typ	
	60	dB typ	Input Signal Level of −24dB; PGA Gain Set at +24dB
Stopband Rejection	66	dB min	f≥6.1kHz
	40	dB typ	f≥60kHz
Differential Group Delay	300	µs typ	500Hz≤f≤3.3kHz and Referenced to the Absolute Group Delay at 1kHz
OUTPUT CHARACTERISTICS			
Output Voltage	±3	V max	$R_L = 3k\Omega$, $C_L = 100pF$
Offset Voltage	±70	mV max	
Gain Range	0 to +24	dB	Determined by DB0–DB7, see Table VI
Relative Accuracy[3,4]	±0.1	dB typ	
Output Resistance	0.2	Ω typ	
LOGIC INPUTS			
$\overline{WR}$, DB0–DB7, DP0, DP1, DS0–DS2, $\overline{SYNCIN}$, CLKIN			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
CLKIN Divider Range (N1)[5]	1 to 4		CLKIN Can Be Set to 288kHz, 576kHz, 864kHz or 1.152MHz. N1 Is Set by DP0, DP1.
LOGIC OUTPUTS $\overline{SYNCOUT}$[6]			
Divider Range (N2)	1 to 8		N2 Is Set by DS0–DS2.
Frequency	$f_{CLKIN}/(N1 \times 5 \times N2)$	kHz	
Pulse Width	$1/f_{CLKIN}$	µs	
V_{OH}, Output High Voltage	2.4	V min	$I_{SOURCE} = 400\mu A$
V_{OL}, Output Low Voltage	0.4	V max	$I_{SINK} = 1.6mA$
POWER SUPPLIES			
V_{DD}	4.75/5.25	V min/V max	
V_{CC}	4.75/5.25	V min/V max	
V_{SS}	−4.75/−5.25	V min/V max	
$I_{DD} + I_{CC}$	25	mA max	
I_{SS}	25	mA max	
Power Dissipation	265	mW max	

NOTES

[1]Operating temperature ranges as follows: J versions: 0 to +70°C.

[2]Specified for an input frequency of 288kHz. This is internally divided by 5 to produce a switched capacitor filter frequency of 57.6kHz. For input frequencies lower than 288kHz, the filter response is shifted down by the ratio of this input frequency to 288kHz.

[3]Measured using a ±3V, 1kHz sine wave.

[4]Measured over the full attenuation range.

[5]Required to derive a switched capacitor filter frequency of 288kHz from CLKIN.

[6]Determined by data transmission rate.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

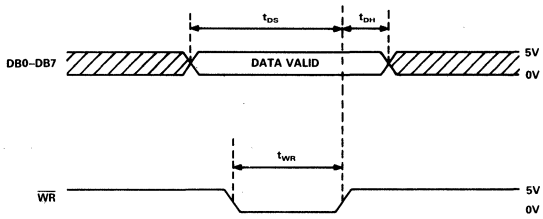
($V_{DD} = V_{CC} = +5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$)

Parameter	Limit at $T_A = +25°C$	Units	Comments
t_{WR}	80	ns min	Write Pulse Width
t_{DS}	60	ns min	Data Setup Time
t_{DH}	20	ns min	Data Hold Time
t_{SYNCIN}	80	ns min	$\overline{SYNCIN}$ Pulse Width

NOTE

[1]Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_R = t_F = 20ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.

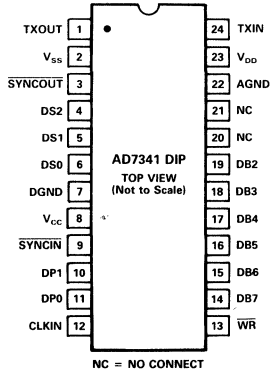
Specifications subject to change without notice.

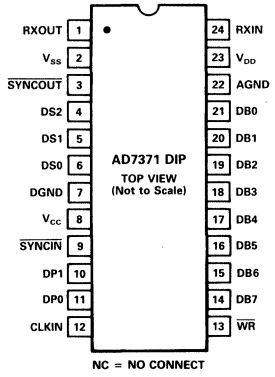


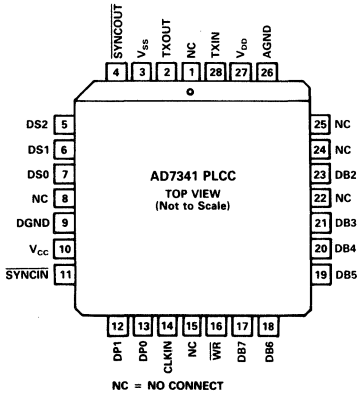
NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% to 90% of +5V. tr = tf = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $(V_{IH} + V_{IL})/2$.

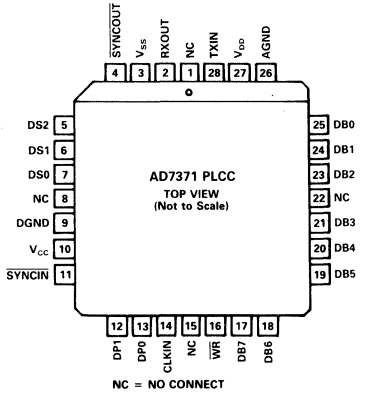
Figure 1. AD7341/AD7371 Timing Diagram

PIN CONFIGURATIONS









ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . −0.3V to +7V
V_{CC} to DGND . . . . . −0.3V to +7V
V_{DD} to V_{CC} . . . . . −0.6V to +0.6V
V_{SS} to DGND . . . . . +0.3V to −7V
AGND to DGND . . . . . −0.3V to V_{CC}
RXIN, TXIN to AGND . . . . . V_{SS} −0.3V to V_{DD} + 0.3V
RXOUT, TXOUT to AGND[1] . . . . V_{SS} −0.3V to V_{DD} + 0.3V
Digital Input Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Power Dissipation (Any Package) to +75°C 1000mW
Operating Temperature Range
J Versions. . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

NOTE
[1]RXOUT, TXOUT may be shorted to AGND, DGND, V_{DD}, V_{CC}, V_{SS} provided that the power dissipation of the package is not exceeded.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one absolute maximum rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION

Temperature Range and Package Options[1]

	Plastic DIP (N-24)	PLCC[2] (P-28A)
Transmit Filter	AD7341JN	AD7341JP
Receive Filter	AD7371JN	AD7371JP

NOTES
[1]See Section 20 for package outline information.
[2]PLCC: Plastic Leaded Chip Carrier.

11

TERMINOLOGY

Cutoff Frequency

The filter cutoff frequency is the point in the response where the amplitude begins to fall off. For the AD7341 and AD7371 it is defined as 0.1dB down from the lowest point in the passband. The AD7341 low pass filter has one cut off frequency at 3.5kHz while the AD7371 band pass filter has a lower cutoff frequency of 180Hz and an upper cutoff frequency of 3.5kHz.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the filter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals (including harmonics) up to 3.5kHz.

Second Harmonic

Second harmonic is the ratio of the second harmonic amplitude to the fundamental amplitude, expressed in dBs.

Third and Higher Harmonics

This is the amplitude ratio of the rms sum of the third and higher harmonics to the fundamental, expressed in dBs. Total harmonic distortion (THD) is the rms sum of the second harmonic and the third and higher harmonics.

Passband Ripple

This is the ripple in the passband section of the frequency response and is expressed in dBs. For the AD7341, it is measured in the band 0 to 3.3kHz, and for the AD7371 it is measured in the band 200Hz to 3.3kHz.

Passband Gain Error

Passband gain error is the deviation of the actual passband level from the ideal passband level. For the AD7341, it is measured with the attenuation set to 0dB (DB2–DB7 = 0); for the AD7371, it is measured with the gain set to 0dB (DB0–DB7 = 1).

Stopband Rejection

This is the magnitude of the stopband response relative to the passband magnitude. The stopband is specified for frequencies greater than 6.1kHz.

Differential Group Delay

Absolute group delay is the rate of change of phase versus frequency, d0/df. For the AD7341 and AD7371, differential group delay is the absolute group delay in a specified band relative to the absolute group delay at 1kHz. The specified band for the AD7341 is 0 to 3.3kHz and for the AD7371 it is 500Hz to 3.3kHz.

Offset Voltage

This is the amount of offset introduced into the input signal by the filter. For the AD7341 it is measured with the attenuation set at 0dB, and for the AD7371 it is measured with the gain set at 0dB.

Attenuation Range

For the AD7341, this is the amount by which the output can be attenuated, using the digital inputs DB7–DB2. Table I gives a selection of attenuations for various values of digital input.

Gain Range

For the AD7371, this is the amount by which the input can be amplified, using the digital inputs DB7–DB0. Table VI gives gain versus digital input code.

Relative Accuracy

This is a measure of the accuracy with which either the AD7341 attenuation or the AD7371 gain can be programmed, having allowed for the passband gain error. It is expressed in dBs relative to attenuation or gain setting with a digital input code of all 1s.

TYPICAL PERFORMANCE CURVES ($V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $f_{CLKIN} = 288kHz$, $T_A = +25°C$ unless otherwise stated)

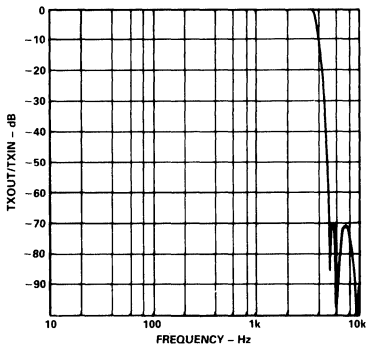


Figure 2. AD7341 Amplitude Response

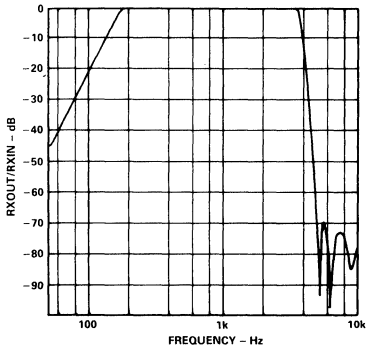


Figure 3. AD7371 Amplitude Response

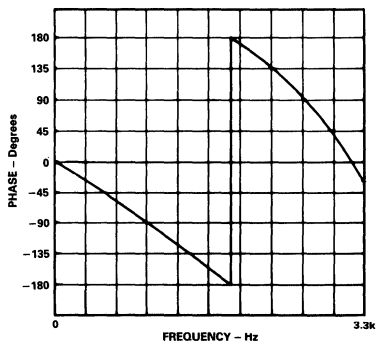


Figure 4. AD7341 Phase Response

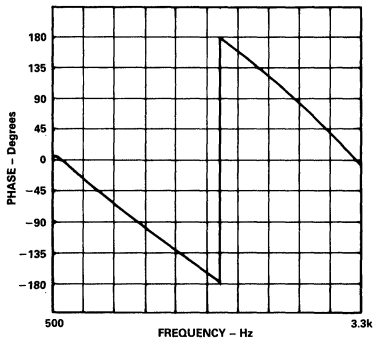


Figure 5. AD7371 Phase Response

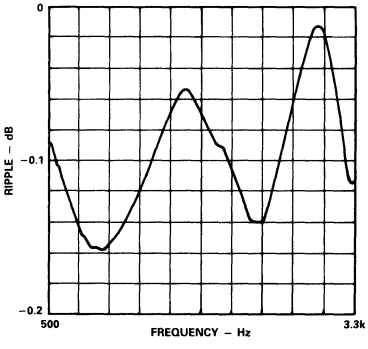


Figure 6. Passband Ripple in the AD7341/AD7371

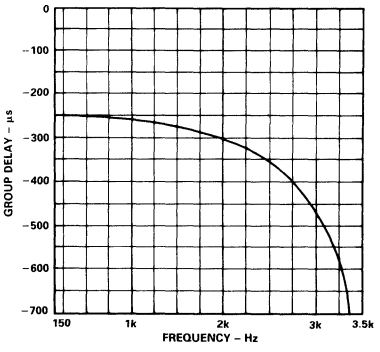


Figure 7. AD7341 Group Delay

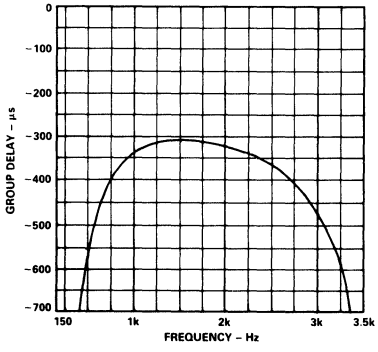


Figure 8. AD7371 Group Delay

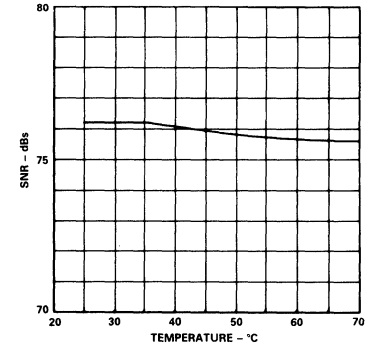


Figure 9. AD7341 SNR vs. Temperature

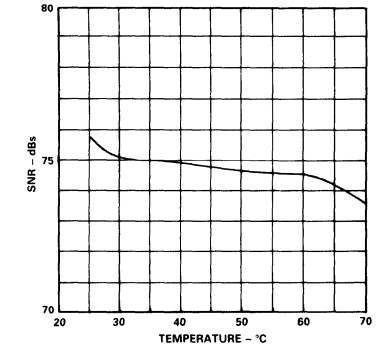


Figure 10. AD7371 SNR vs. Temperature

AD7341 DIP PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	TXOUT	Signal output pin from filter.
2	V_{SS}	Negative supply pin for the device. This is −5V ± 5%.
3	$\overline{\text{SYNCOUT}}$	This output pulse is derived from the SCF (Switched Capacitor Filter) clock and can be used in system synchronization. The pulse frequency is $f_{SYNCOUT} = f_{CLKIN} / (N1 \times 5 \times N2)$, where f_{CLKIN} is the input frequency at CLKIN, N1 is the value loaded to the input programmable divider and N2 is the value loaded to the output programmable divider. N1 is set by DP0 and DP1 (see Table II). N2 is set by DS0, DS1 and DS2 and varies from 1 to 8. Table I shows the typical $\overline{\text{SYNCOUT}}$ frequencies which can be set when f_{CLKIN} is 288kHz and N1 is 1.

DS2	DS1	DS0	$\overline{\text{SYNCOUT}}$ Frequency
0	0	0	7.2kHz
0	0	1	57.6kHz
0	1	0	28.8kHz
0	1	1	19.2kHz
1	0	0	14.4kHz
1	0	1	11.52kHz
1	1	0	9.6kHz
1	1	1	8.22kHz

Table I. Setting $\overline{\text{SYNCOUT}}$ Frequency Using DS2, DS1, DS0

DP1	DP0	CLKIN Divide Ratio, N1
0	0	4
0	1	1
1	0	2
1	1	3

Table II. Setting CLKIN Divide Ratio Using DP1, DP0

4	DS2	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table I.
5	DS1	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table I.
6	DS0	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table I.
7	DGND	Ground point for on chip digital circuitry.
8	V_{CC}	Positive supply pin for the on chip digital circuitry. This is +5V ± 5%.
9	$\overline{\text{SYNCIN}}$	This asynchronous digital input resets the internal clock circuitry from which $\overline{\text{SYNCOUT}}$ is derived. This allows $\overline{\text{SYNCOUT}}$ to be synchronized to an external signal.
10	DP1	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table II.
11	DP0	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table II.
12	CLKIN	Clock input for the device. This is internally divided to produce the SCF clock.
13	$\overline{\text{WR}}$	Active low digital input. Data for the on chip programmable attenuation is loaded to the input latch when this signal goes low and is latched when it goes high.
14–19	DB7–DB2	Six-bit data bus which sets the attenuation level on the output. See Table III.
20	NC	No connect.
21	NC	No connect.
22	AGND	Ground point for the on-chip analog circuitry.
23	V_{DD}	Positive supply pin for the on-chip analog circuitry. This is +5V ± 5%.
24	TXIN	Filter input.

DB7	DB6	DB5	DB4	DB3	DB2	Attenuation dB
1	1	1	1	1	1	0
0	1	1	1	1	1	−6
0	0	1	1	1	1	−12
0	0	0	1	1	1	−18
0	0	0	0	1	1	−24
0	0	0	0	0	1	−30
0	0	0	0	0	0	−38

Table III. Output Attenuation vs. Digital Input Code

AD7371 DIP PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	RXOUT	Signal output pin from filter.
2	V_{SS}	Negative supply pin for the device. This is −5V ± 5%.
3	$\overline{\text{SYNCOUT}}$	This output pulse is derived from the SCF (switched capacitor filter) clock and can be used in system synchronization. The pulse frequency is $f_{SYNCOUT} = f_{CLKIN} / (N1 \times 5 \times N2)$, where f_{CLKIN} is the input frequency at CLKIN, N1 is the value loaded to the input programmable divider and N2 is the value loaded to the output programmable divider. N1 is set by DP0 and DP1 (see Table V). N2 is set by DS0, DS1 and DS2 and varies from 1 to 8. Table IV shows the typical $\overline{\text{SYNCOUT}}$ frequencies which can be set when f_{CLKIN} is 288kHz and N1 is 1.

DS2	DS1	DS0	$\overline{\text{SYNCOUT}}$ Frequency
0	0	0	7.2kHz
0	0	1	57.6kHz
0	1	0	28.8kHz
0	1	1	19.2kHz
1	0	0	14.4kHz
1	0	1	11.52kHz
1	1	0	9.6kHz
1	1	1	8.22kHz

Table IV. Setting $\overline{\text{SYNCOUT}}$ Frequency Using DS2, DS1, DS0

DP1	DP0	CLKIN Divide Ratio, N1
0	0	4
0	1	1
1	0	2
1	1	3

Table V. Setting CLKIN Divide Ratio Using DP1, DP0

4	DS2	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table IV.
5	DS1	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table IV.
6	DS0	Unlatched digital input which is used to set $\overline{\text{SYNCOUT}}$ frequency. See Table IV.
7	DGND	Ground point for on chip digital circuitry.
8	V_{CC}	Positive supply pin for the on chip digital circuitry. This is +5V ± 5%.
9	$\overline{\text{SYNCIN}}$	This digital input resets the internal clock circuitry from which $\overline{\text{SYNCOUT}}$ is derived. This allows $\overline{\text{SYNCOUT}}$ to be synchronized to an external signal.
10	DP1	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table V.
11	DP0	Unlatched digital input pin which is used to set divide ratio on the CLKIN input. See Table V.
12	CLKIN	Clock input for the device. This is internally divided to produce the SCF clock.
13	$\overline{\text{WR}}$	Active low digital input. Data for the on chip programmable gain is loaded to the input latch when this signal goes low and is latched when it goes high.
14–21	DB7–DB0	Eight-bit data bus which sets the gain level on the input. See Table VI.
22	AGND	Ground point for the on-chip analog circuitry.
23	V_{DD}	Positive supply pin for the on-chip analog circuitry. This is +5V ± 5%.
24	RXIN	Filter input.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Gain dB
0	0	0	0	0	0	0	0	24
0	0	0	1	1	0	0	0	21
0	0	1	0	0	0	1	0	18
0	0	1	1	0	0	0	0	15
0	1	0	0	0	1	0	0	12
0	1	1	0	0	0	0	1	9
0	1	1	1	0	1	1	1	6
1	0	1	1	0	0	0	0	3
1	1	1	1	1	1	1	1	0

Table VI. Input Gain vs. Digital Input Code

CIRCUIT DESCRIPTION

AD7341 Filter

The AD7341 transmit filter performs the reconstruction or smoothing function for the transmit channel D/A converter. Figure 11 is the block diagram for the filter and programmable attenuation section.

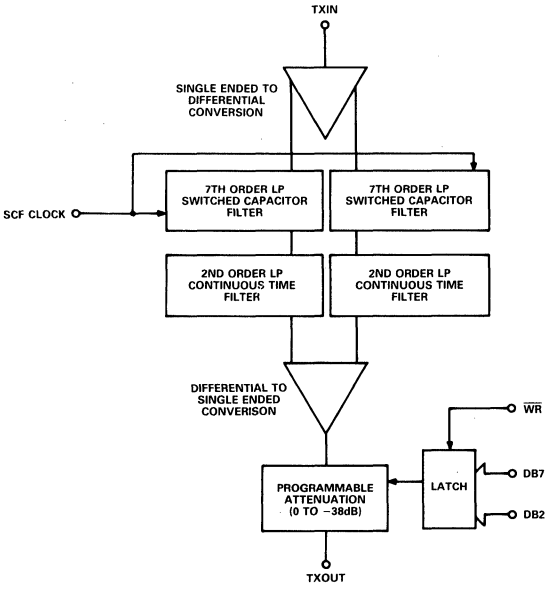


Figure 11. AD7341 Filter Section

The transmit channel signal is applied at TXIN and is converted to a differential signal. It then goes to the fully differential switched capacitor low pass section. This is a seventh order elliptical filter which gives a 3.5kHz cut off frequency and stopband attenuation of greater than 70dB at frequencies above 6.1kHz. The use of the differential filter structure ensures an excellent harmonic distortion figure and also gives improved rejection of common mode noise such as clock feedthrough in the switched capacitor switching transistors. The filter cut off frequency depends directly on the clock driving the switched capacitor section and upon the capacitor matching. Capacitor matching is typically better than 2% and this means that if the clock is constant, cut off frequency variation from device to device will be less than 2%. Since the switched capacitor filters are sampled data systems (analog data) with a sampling frequency of 57.6kHz, they must be followed by a smoothing filter to remove aliased components due to this clock. This smoothing filter is a second order low pass continuous time section. The differential outputs of the two smoothing filters are then recombined to a single ended signal. The level of SCF clock feedthrough at the output is typically −65dB. This can be further reduced by using a simple RC combination at the output (39kΩ and 1000pF reduce the feedthrough to −80dB). The second order filter shown in Figure 22 reduces it to below −90dB. After recombination of the differential signals, a programmable attenuation stage follows. The attenuator circuit diagram is shown in Figure 12. It

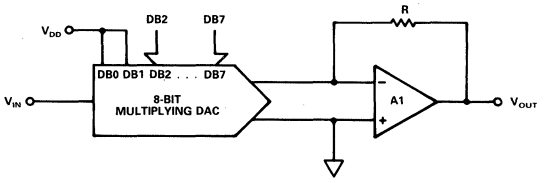


Figure 12. AD7341 Output Attenuator

consists of an 8-bit multiplying DAC with the two LSBs (DB1, DB0) tied high. The transfer function is given by:

$$A = 20 \log \frac{256}{4N+3}$$

where A is the attenuation in dBs and N is the 6-bit binary code loaded to the device. Expressing N in terms of A gives:

$$N = \frac{1}{4}\left[\frac{256}{10^{\frac{A}{20}}} - 3\right]$$

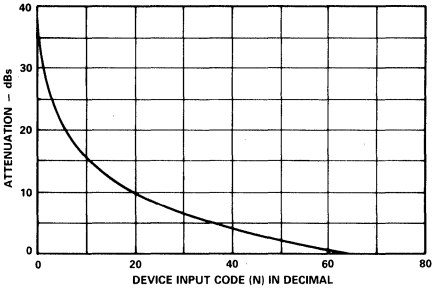


Figure 13. Programmable Attenuation vs. Input Code for the AD7341

This allows the calculation of the device input code for a given output attenuation. The attenuation range is 0 to 38dB and allows the user to adapt the output signal for different line specifications. Figure 13 shows how attenuation varies with input code, and Table III gives a selection of attenuations for specific codes.

AD7371 Filter

The receive filter performs the antialiasing function for the receive channel A/D converter. It provides rejection of high frequency out-of-band signals, attenuation of low frequency noise at both 50Hz and 60Hz line frequencies and programmable gain for the input signal. Figure 14 is the block diagram for the filter and programmable gain section.

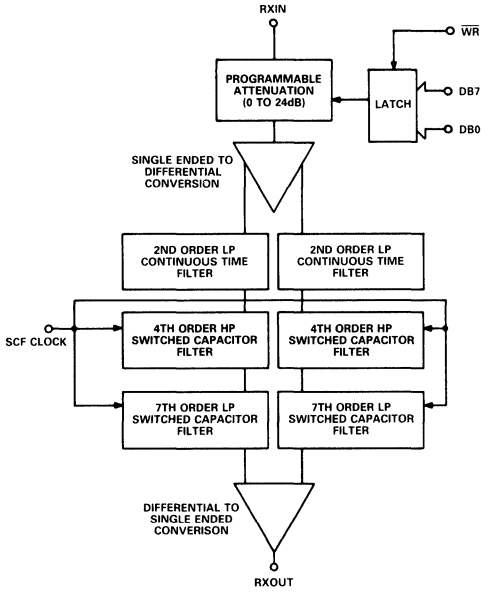


Figure 14. AD7371 Filter Section

The input signal is applied at RXIN and passes through the programmable gain stage. Figure 15 shows the circuit diagram for this. It consists of an 8-bit multiplying DAC and resistor combination in the feedback loop of an operational amplifier. The transfer function is given by:

$$G = 20 \log \frac{272.2}{N+17.2}$$

G is the gain in dBs and N is the 8-bit binary code loaded to the device. Varying this code between 0 and 255 gives a gain range of 24dB to 0dB. Expressing N in terms of G gives:

$$N = \frac{272.2}{10^{\frac{G}{20}}} - 17.2$$

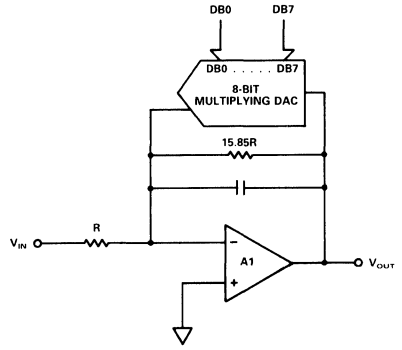


Figure 15. AD7371 Programmable Gain Amplifier

This equation can be used to calculate the code, N, needed to give the desired gain, G. Figure 16 is a graph of gain versus input code, and Table VI gives a selection of gains for specific codes.

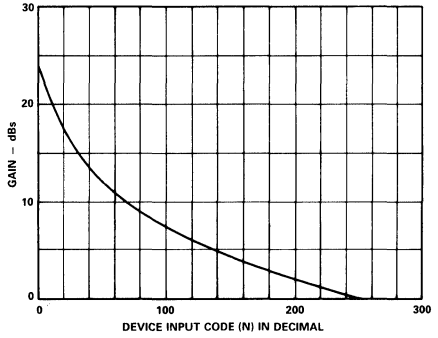


Figure 16. Programmable Gain vs. Input Code for the AD7371

After the PGA stage, the receive signal is converted to a fully differential signal before going to the differential filters. The first differential filter is a second order continuous time section. This is necessary to provide antialiasing for the sampling switched capacitor filter. The continuous time filter eliminates any high frequency components from the input signal which would be aliased back into the passband of the switched capacitor filter and appear as noise. Following the continuous time filter, the fourth order elliptical high pass switched capacitor section has a cutoff frequency of 180Hz, and the seventh

order elliptical low pass switched capacitor section has a cutoff frequency of 3.5kHz. As in the reconstruction filter, the cutoff frequency variation from device to device for fixed CLKIN is typically less than 2%. On recombination of the differential signals, the output goes to RXOUT.

SCF Clock and System Synchronization

The clock generation circuitry for both the AD7341 and the AD7371 is identical and is shown in Figure 17. For the specified filter response, the switched capacitor clock must be

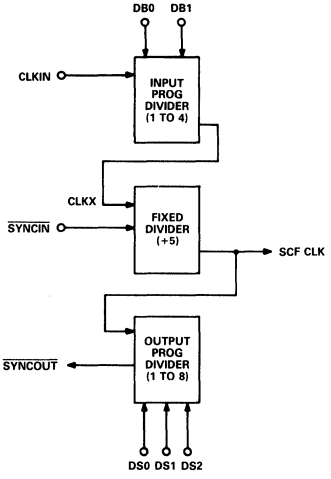


Figure 17. AD7341/AD7371 Clock Generation Circuitry

57.6kHz. This means that CLKX in Figure 17 must always be 288kHz (57.6kHz×5). The input programmable divider allows the user the option of four CLKIN frequencies (288kHz, 576kHz, 864kHz or 1152kHz). The input divider can then be programmed to ensure that CLKX is 288kHz.

The AD7341 and the AD7371 are always used with a DAC and ADC respectively. The DAC and ADC update and sample at a certain rate (9.6kHz or 7.2kHz, for example). The filters sample at 57.6kHz. In order to ensure that there is no low frequency aliasing, the DAC/ADC rate must be synchronized with the SCF clock. This means the SCF rate must be an integral multiple of the DAC/ADC rate. The AD7341/AD7371 actually generates this required synchronized clock on chip. The output programmable divider allows division of the SCF clock by 1 to 8. The divide ratio is determined by inputs DS0–DS2. The output of the programmable divider goes to $\overline{\text{SYNCOUT}}$ which is then used to drive either the $\overline{\text{CONVST}}$ input of an ADC or the $\overline{\text{LDAC}}$ input of a DAC. The output programmable divider also has a reset input ($\overline{\text{SYNCIN}}$). This is normally tied high. When it is brought low, the counter is reset. On returning high, the counter is reactivated. By using this $\overline{\text{SYNCIN}}$ facility, it is possible to adjust the point in time at which sampling occurs while maintaining the same rate. This is useful in modem applications and is known as cycle slipping. Figure 18 shows the complete timing waveforms for the AD7341/AD7371.

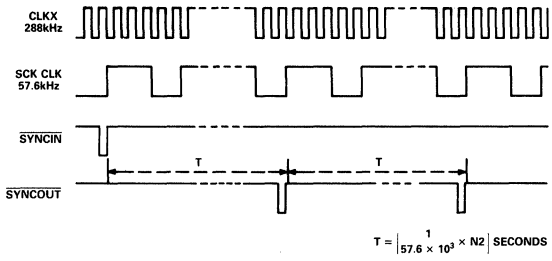


Figure 18. AD7341/AD7371 Timing Waveforms

APPLYING THE AD7341/7371

The prime application for the AD7341/7371 is in the analog front end for echo-cancelling modems. Here, the filters are combined with a high resolution DAC and ADC to provide the interface between the analog and the digital domain. The excellent noise performance of the AD7371 and the high resolution of the AD7871 (14-bit ADC) combine to allow the modem echo-cancelling loop to be implemented totally in the digital domain. This overcomes the disadvantage with lower resolution systems which need to do a digital approximation of the echo and reconstruct in analog form for an analog echo-cancelling loop.

Conversely, in the modem transmitter, the combination of AD7341 and high resolution DAC (14-bit AD7840) allows transmission of the signal with minimum impairments to the line.

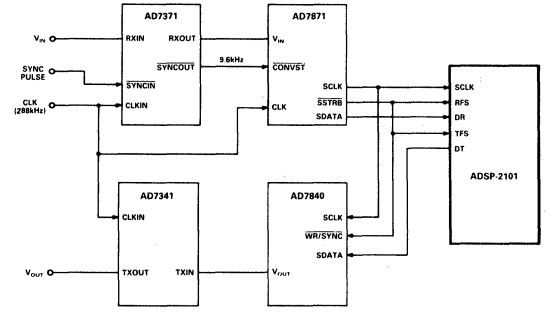


Figure 19. Modem Analog Front End and Interface to ADSP-2101 DSP

Figure 19 shows a typical hardware interface between the analog front end chipset and the ADSP-2101 in an echo-cancelling modem. The ADSP-2101 is the new DSP microcomputer from Analog Devices. It has program memory and data memory on chip and is code compatible with the ADSP-2100. It also has two serial ports. The particular configuration, shown in Figure 19, uses the serial interface on both the AD7840 and AD7871 to

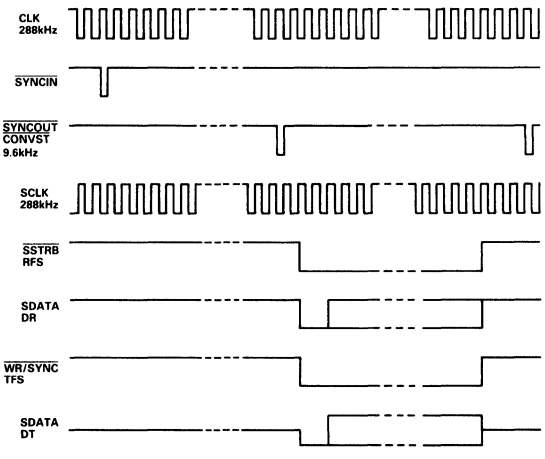


Figure 20 System Timing for Figure 19

talk to one of the ADSP-2101 serial ports. The system timing diagram is shown on Figure 20. The 288kHz clock drives the two filters and the ADC. The $\overline{\text{SYNCIN}}$ pulse may be used to set the absolute sampling instant. DS0, DS1 and DS2 on the AD7371 are programmed to give a 9.6kHz $\overline{\text{SYNCOUT}}$ signal. This drives the AD7871 $\overline{\text{CONVST}}$ input and is thus the sampling rate. SCLK on the AD7871 clocks out serial data on its rising edge. $\overline{\text{SSTRB}}$ is the framing pulse for the serial data. Within this framing pulse, a 16-bit data stream is output on the SDATA line. Each data bit is valid on the falling edge of SCLK. There are two leading zeros and the 14-bit conversion result appears after these. When RFS on the ADSP-2101 goes low, data appearing on DR is clocked into the receive shift register on each falling edge of SCLK. Once the 16 data bits have been received an internal interrupt is set and the processor can read the data.

The circuit of Figure 19 also uses the $\overline{\text{SSTRB}}$ signal to frame the transmit data from the DSP . Thus, when $\overline{\text{SSTRB}}$ goes low, data contained in the transmit shift register of the DSP is clocked out on each rising edge of SCLK. The AD7840, in turn, loads each data bit into its input register on the SCLK falling edges. The DAC output is updated when 16 data bits have been received.

Using the ADSP-2101 and the chipset, the modem hardware is simplified. The number of lines required to connect the chips is much less than a parallel interface structure would need and no external glue logic is required.

CHIPSET LAYOUT

Figure 23 is the circuit diagram for a modem analog front end based on the Analog Devices chip set. The component overlay is given in Figure 21, while the PCB layout is given in Figures 24 and 25.

The modem analog front end uses the AD7341, AD7371, AD7840 and AD7871. Total channel SNR performance is better than 72dB with a full scale input signal and unity gain on the filter chips. The 14-bit resolution of the converters gives an instantaneous dynamic range of 84dB. If greater dynamic range is required, then the AD7371 PGA can be used to give up to 24dB extra.

The evaluation board makes full use of the flexible interfaces on the AD7840 and the AD7871. J1 is a 96-way VME bus connector which carries the parallel interface for the board. This plugs directly into the connector on the evaluation board for the ADSP-2100, which is another in the Analog Devices family of Digital Signal Processors and is code compatible with the ADSP-2101. Thus, direct interfacing between the boards is possible. All the signals necessary for interfacing to other DSPs are available on J1. The 9-way D-Type connector, J2, carries the serial interface for the board. This allows DSPs with serial ports to interface directly to the chipset.

Power supplies used to operate the board are ±15V analog supplies and a single +5V digital supply. A ±5V analog supply is derived from the ±15V supply by using the 78L05/79L05 regulators. This supply is used for the AD7341, AD7371, AD7840 and AD7871. The supply grounds are tied together on the board so that there is no need to have them connected back at the supply source.

The analog input and output ranges are both ±10V. The analog input is attenuated by IC1 and associated circuitry to give the required ±3V input range for the filter and ADC. Likewise, the analog output from the reconstruction filter (±3V) is gained up by the output amplifier (IC6) to give a ±10V output. This output amplifier also contains a simple second order filter to further attenuate the switched capacitor clock noise at the output.

There are three digital inputs to the board. These are CLKIN, ADC SYNCIN and DAC SYNCIN. CLKIN provides the clock for the ADC and filters. The DIP switches on the board have been set up to accept a nominal clock of 288kHz for the filters. ADC SYNCIN and DAC SYNCIN can be used to resynchronize the filters/converters with an external synchronizing signal. If this is not required, then both of these inputs should be tied high.

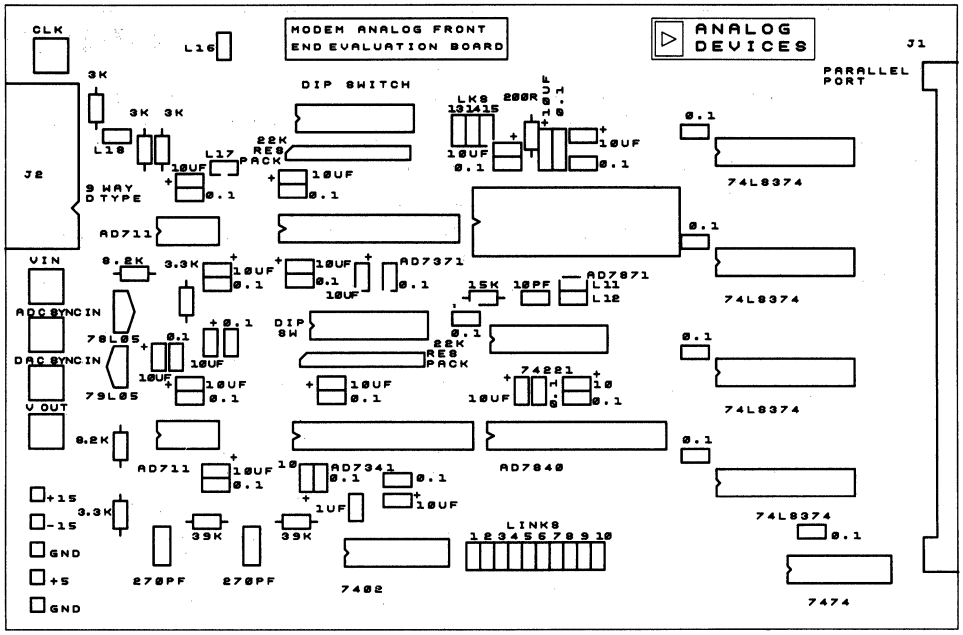


Figure 21. Component Overlay for Circuit of Figure 23

Parallel Interface

If the parallel interface is required, then the four latch chips (IC7 to IC10) should be inserted into the sockets provided. Links L16, L17, L18, L5 and L6 should be omitted. This isolates the serial port from bus activity. Link L15 should be inserted to choose 14-bit parallel operation for the ADC. Omit links L14 and L13. Internal or external clock operation for the ADC may be chosen by L11 and L12. L11 gives external clock operation, while L12 gives internal clock operation. AD7871 conversion is started by $\overline{\text{CONVST}}$ (pin 1) going low. When conversion is complete, $\overline{\text{INT/BUSY}}$ (pin 4) goes low. IC13 extends this pulse. This is then used to read the ADC result into the latches and to interrupt the processor. The processor interrupt service routine then reads the latch contents. Note that the data format is 14 bits with sign extension to 16 bits.

On the AD7840 insert L2 to tie the chip select low and omit L1. Insert L3 to use $\overline{\text{SYNCOUT}}$ of filter to write to the DAC and omit L4. Thus, the processor writes data to the latches and the DAC gets updated on every rising edge of $\overline{\text{WR/SYNC}}$. The data format is 14-bit right justified.

Serial Interface

If the serial interface is required, then omit the four latches (74LS374) and use the serial connector (J2). Links L5, L6, L16, L17 and L18 must be inserted. Omit L15 and insert L14. This places the AD7871 in serial mode of operation with continuously running SCLK. As in the parallel mode, conversion is started by $\overline{\text{CONVST}}$ going low. Serial data appears on Pin 9 (SDATA) as conversion is taking place, and it is latched into the processor shift register on each falling edge of SCLK. The frame synchronization pulse for the data is on Pin 7 ($\overline{\text{SSTRB}}$). The data format is 16-bit with the MSB first. The 16 bits of data are made up of two leading zeros and the 14-bit conversion result. For the DAC in the serial mode omit L3 and insert L4. This provides the necessary inversion of the $\overline{\text{SYNCOUT}}$ pulse from the filter so that it can be used as the frame synchronization for the DAC and the processor. When this goes low data in the processor shift register is clocked out on each rising edge of SCLK and latched into the DAC shift register on each falling edge of SCLK. Since $\overline{\text{LDAC}}$ (Pin 24) is tied permanently low, the DAC register is updated automatically when the 16-bit data stream has been received. The format of this data stream is set up by links L7 to L10. Consult Table I on the AD7840 data sheet for the appropriate settings. Figure 22, below, shows the pin designations for J2.

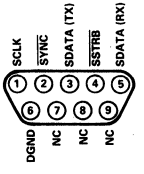


Figure 22. Pin Configuration for J2 (Front View)

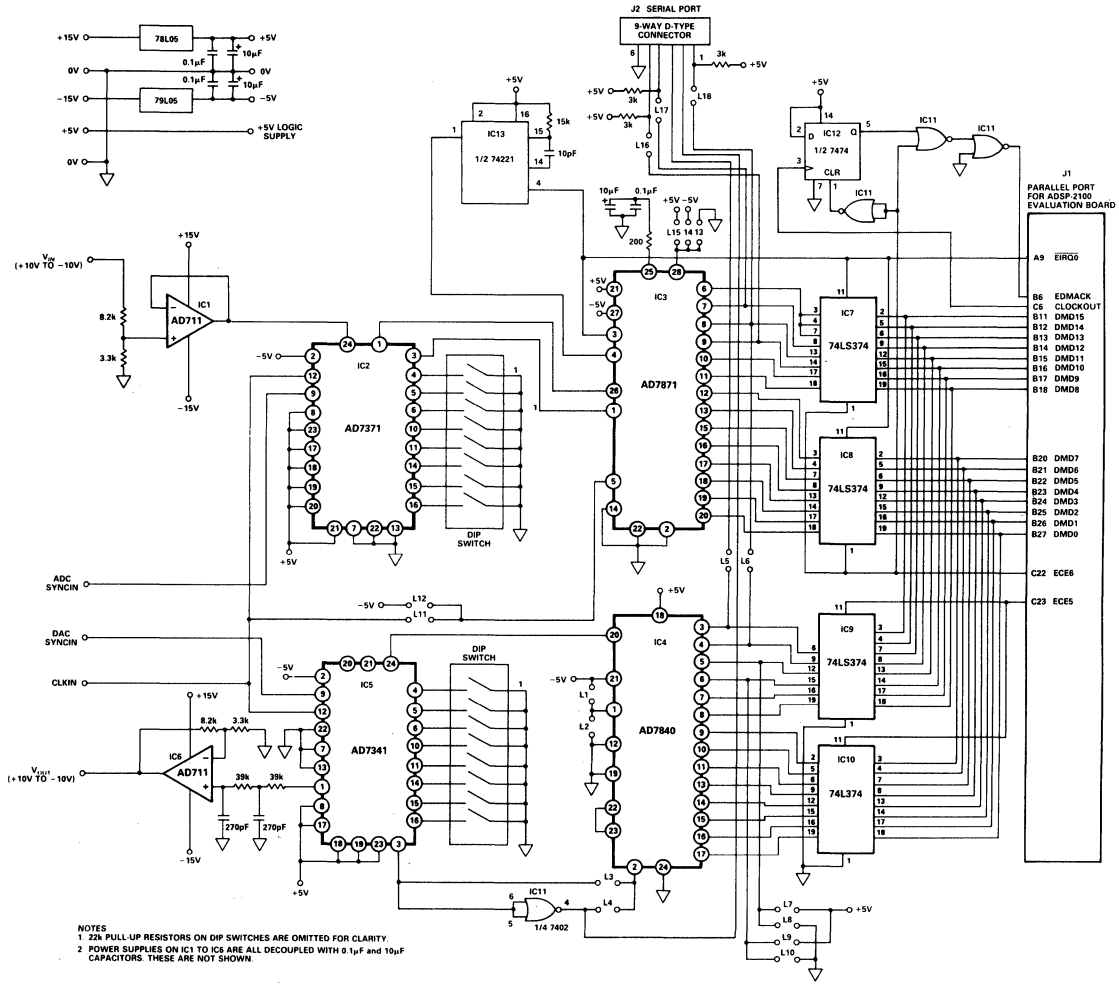


Figure 23. Circuit Diagram for Modem Analog Front End

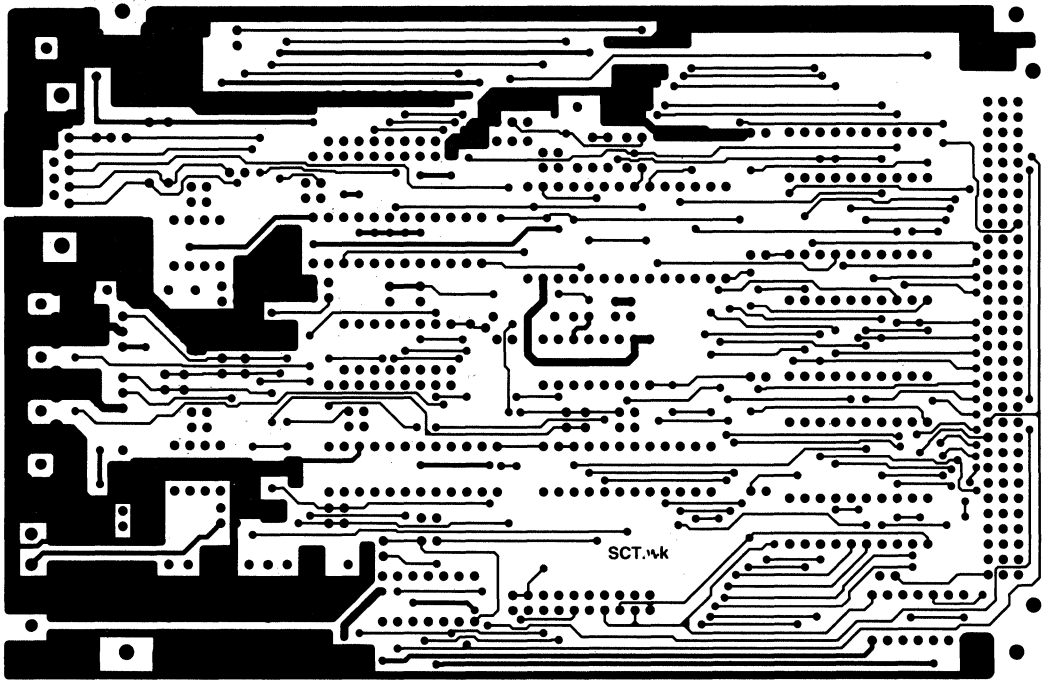


Figure 24. PCB Component Side Layout for Figure 23

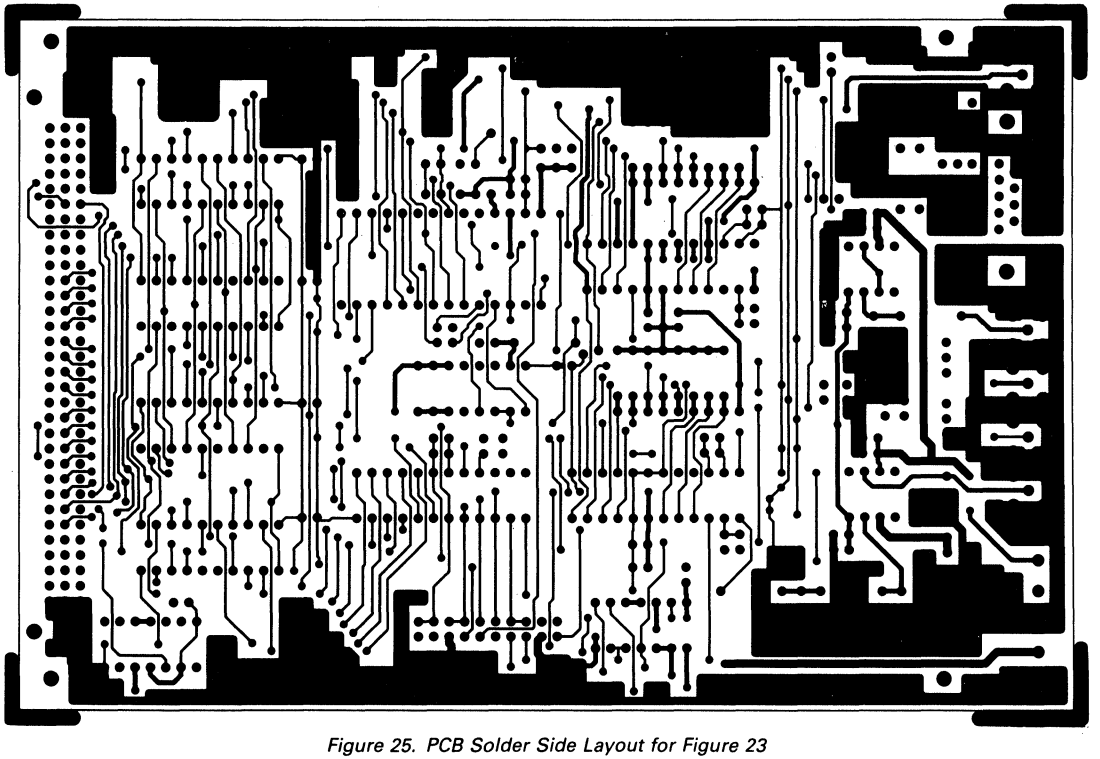


Figure 25. PCB Solder Side Layout for Figure 23

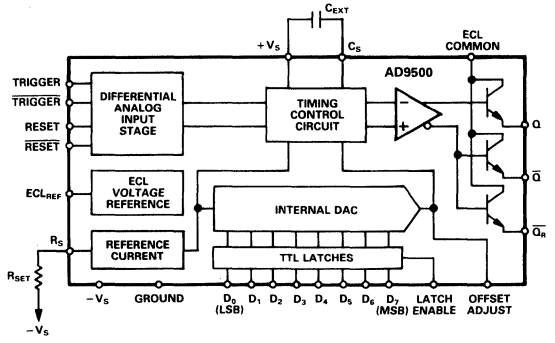
Digitally Programmable Delay Generator

AD9500

FEATURES
10ps Delay Resolution
2.5ns to 10μs Full-Scale Range
Fully Differential Inputs
Separate Trigger and Reset Inputs
Low Power Dissipation – 310mW

APPLICATIONS
ATE
Pulse Deskewing
Arbitrary Waveform Generators
High-Stability Timing Source
Multiple Phase Clock Generators

AD9500 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

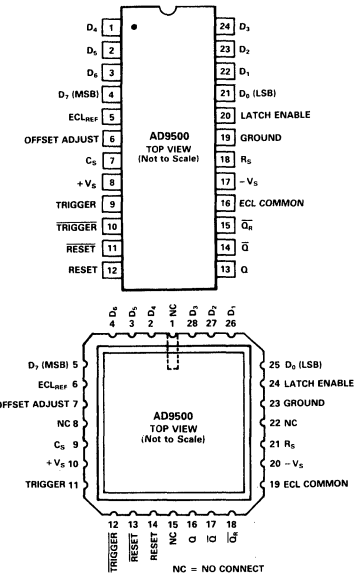
The AD9500 is a digitally programmable delay generator, which provides programmed delays, selected through an 8-bit digital code, in resolutions as small as 10ps. The AD9500 is constructed in a high-performance bipolar process, designed to provide high-speed operation for both digital and analog circuits.

The AD9500 employs differential TRIGGER and RESET inputs which are designed primarily for ECL signal levels but function with analog and TTL input levels. An on-board ECL reference midpoint allows both of the inputs to be driven by either single ended or differential ECL circuits. The AD9500 output is a complementary ECL stage, which also provides a parallel $\overline{Q_R}$ output circuit to facilitate reset timing implementations.

The digital control data is passed to the AD9500 through a transparent latch controlled by the LATCH ENABLE signal. In the transparent mode, the internal DAC of the AD9500 will attempt to follow changes at the inputs. The LATCH ENABLE is otherwise used to strobe the digital data into the AD9500 latches.

The AD9500 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades are packaged in a 24-pin ceramic "Skinny" DIP (0.3" package width), as well as 28-pin surface mount packages. Contact the factory for MIL-STD-883, revision C, qualified devices.

PIN CONFIGURATIONS



ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9500BP	−25°C to +85°C	28-Pin PLCC (Plastic), Industrial Temperature	P-28A
AD9500BQ	−25°C to +85°C	24-Pin "Skinny" DIP, Industrial Temperature	Q-24
AD9500TE	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9500TQ	−55°C to +125°C	24-Pin "Skinny" DIP, Extended Temperature	Q-24

*See Section 20 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$)	+7V
Negative Supply Voltage ($-V_S$)	−7V
ECL COMMON to Ground Differential	−2.0V to +5.0V
Digital Input Voltage Range	−3.5V to +5.0V
Trigger/Reset Input Voltage Range	±5.0V
Trigger/Reset Differential Voltage	5.0V
Minimum R_{SET}	220Ω
Digital Output Current (Q and $\overline{Q}$)	30mA
Digital Output Current ($\overline{Q_R}$)	2mA
Offset Adjust Current (Sinking)	4mA
Power Dissipation (+25°C Free Air)[2]	2.62W
Operating Temperature Range	
AD9500BP/BQ	−25°C to +85°C
AD9500TE/TQ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+175°C
Lead Soldering Temperature (10sec)	+300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages + V_S = +5.0V, $-V_S$ = −5.2V; C_{EXT} = 0pF; R_{SET} = 500Ω, unless otherwise stated)

Parameter	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY[4]									
Differential Linearity	7	+25°C			0.5			0.5	LSB
Integral Linearity	7	+25°C			1.0			1.0	LSB
Monotonicity	7	+25°C		Guaranteed			Guaranteed		
DIGITAL INPUT									
Logic "1" Voltage	7,8	Full	2.0			2.0			V
Logic "0" Voltage	7,8	Full			0.8			0.8	V
Logic "1" Current	1,2,3	Full			5			5	µA
Logic "0" Current	1,2,3	Full			5			5	µA
Digital Input Capacitance	12	+25°C			5.5			5.5	pF
Data Setup Time[5]	12	+25°C		0.4	0.75		0.4	0.75	ns
Data Hold Time[6]	12	+25°C		0.4	0.75		0.4	0.75	ns
Latch Pulse Width (t_{LPW})	12	+25°C	3.0			3.0			ns
RESET/TRIGGER INPUTS[7]									
TRIGGER Input Voltage Range		Full		−2.5;4.5			−2.5;4.5		V
RESET Input Voltage Range		Full		−2.5;2.0			−2.5;2.0		V
Differential Switching Voltage	7,8	Full		40	300		40	300	mV
Input Bias Current	1	+25°C		40	50		40	50	µA
	2,3	Full			75			75	µA
Input Resistance		+25°C		4			4		kΩ
Input Capacitance	12	+25°C		6.5	7.25		6.5	7.25	pF
Minimum Input Pulse Width (t_{TPW}, t_{RPW})		+25°C		2.0			2.0		ns
DYNAMIC PERFORMANCE[8]									
Maximum Trigger Rate	12	+25°C	100			100			MHz
Minimum Propagation Delay (t_{PD})[9]	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Minimum Propagation Delay TC[10]		Full		7.5			7.5		ps/°C
Full-Scale Range TC		Full		0.5			0.5		ps/°C
Delay Uncertainty (Jitter)		+25°C		10			10		ps
Reset Propagation Delay (t_{RD})[11]	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Reset-to-Trigger Holdoff (t_{THO})[12]	4	+25°C	0.2	0		0.2	0		ns
Trigger-to-Reset Holdoff (t_{RHO})[13]	4	+25°C	2.0	1.5		2.0	1.5		ns
Minimum Output Pulse Width		+25°C		3.3			3.3		ns
Output Rise Time	12	+25°C			2.0			2.0	ns
Output Fall Time	12	+25°C			2.0			2.0	ns
Delay Coefficient Settling Time (t_{DAC})[14]		+25°C		29			29		ns
Linear Ramp Settling Time (t_{LRS})		+25°C		22			22		ns

Parameter	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
SUPPORT FUNCTIONS									
ECL_{REF}	1	+25°C	−1.4	−1.3	−1.2	−1.4	−1.3	−1.2	V
ECL_{REF} Voltage Drift[15]		Full		1.1			1.1		mV/°C
Offset Adjust Range		Full		−2			−2		mA
DIGITAL OUTPUTS[8]									
Logic "1" Voltage	1,2,3	Full	−1.1			−1.1			V
Logic "0" Voltage	1,2,3	Full			−1.5			−1.5	V
POWER SUPPLY[16]									
Positive Supply Current (+5.0V)	1	+25°C		24	28		24	28	mA
	2,3	Full			30			30	mA
Negative Supply Current (−5.2V)	1	+25°C		37	42		37	42	mA
	2,3	Full			44			44	mA
Nominal Power Dissipation		+25°C		312			312		mW
Power Supply Rejection Ratio[17]									
Full-Scale Range Sensitivity	7	+25°C		70	300		70	300	ps/V
Minimum Propagation Delay Sensitivity	7	+25°		150	500		150	500	ps/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance

24-Pin Ceramic $\theta_{JA} = 56°C/W; \theta_{JC} = 16°C/W$
28-Pin PLCC (Plastic) $\theta_{JA} = 60°C/W; \theta_{JC} = 22°C/W$
28-Pin Ceramic LCC $\theta_{JA} = 69°C/W; \theta_{JC} = 25°C/W$

[3]Military subgroups apply to military qualified devices only.

[4]$R_{SET} = 10k\Omega$. (Full-scale delay = 100ns).

[5]The digital data inputs must remain stable for the specified time prior to the LATCH ENABLE signal.

[6]The digital data inputs must remain stable for the specified time after the LATCH ENABLE signal.

[7]The TRIGGER and RESET inputs are differential and must be driven relative to one another. Both of these inputs are ECL compatible, but can also be used with TTL logic families in a limited fashion.

[8]Outputs terminated through 50Ω resistors to −2.0V.

[9]Program Delay = 0.0ps (Digital Data = 00_H). In Operation, any programmed delays are in addition to the Minimum Propagation Delay.

[10]Measured from the 50% transition point of the reset signal input, to the 50% transition point of the resetting output.

[11]Minimum time from falling edge of RESET to triggering input, to insure a valid output event.

[12]Change in total delay through AD9500, exclusive of changes in minimum-propagation delay t_{PD}.

[13]Minimum time from triggering event to rising edge of RESET, to insure a valid output event.

[14]Measured from the LATCH ENABLE input to the point when the AD9500 becomes 8-bit accurate again, after a full-scale change in the programmed delay.

[15]Standard 10K and 10KH ECL families operate with a 1.1mV/°C drift by design.

[16]Supply voltages should remain stable within ±5% for normal operation.

[17]Measured at ±5% of $-V_S$ and $+V_S$.

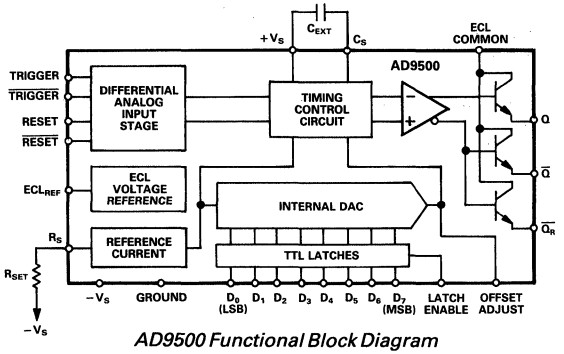
Specifications subject to change without notice.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

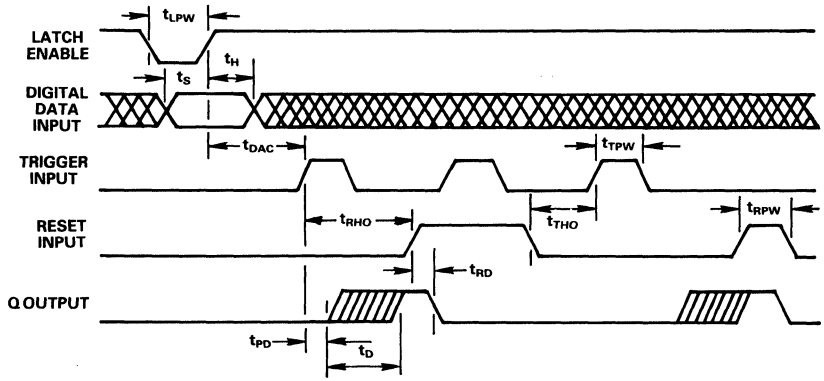
Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
D_4–D_6	– One of eight digital inputs used to set the programmed delay.
D_7 (MSB)	– One of eight digital inputs used to set the programmed delay. D_7 (MSB) is the most significant bit of the digital input word.
ECL_{REF}	– ECL midpoint reference, nominally −1.3V. Use of the ECL_{REF}, allows either of the TRIGGER or the RESET inputs to be configured for single-ended ECL inputs.
OFFSET ADJUST	– The OFFSET ADJUST is used to adjust the minimum propagation delay (t_{PD}), by pulling or pushing a small current out of or into the pin.
C_S	– C_S allows the full-scale range to be extended by using an external timing capacitor. The value of C_{EXT}, connected between C_S and $+V_S$, may range from no external capacitance to 0.1μF+. See R_S ($C_{INTERNAL}$ = 10pF).
$+V_S$	– Positive supply terminal, nominally +5.0V.
TRIGGER	– Noninverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The TRIGGER input must be driven in conjunction with the $\overline{\text{TRIGGER}}$ input.
$\overline{\text{TRIGGER}}$	– Inverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The $\overline{\text{TRIGGER}}$ input must be driven in conjunction with the TRIGGER input.
$\overline{\text{RESET}}$	– Inverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The RESET input must be driven in conjunction with the $\overline{\text{RESET}}$ input.
RESET	– Noninverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The $\overline{\text{RESET}}$ input must be driven in conjunction with the RESET input.
Q	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic HIGH on the Q output. A "resetting" event at the inputs will produce a logic LOW on the Q output
$\overline{Q}$	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q}$ output.
$\overline{Q_R}$	– $\overline{Q_R}$ output is parallel to the $\overline{Q}$ output. The $\overline{Q_R}$ output is typically used to drive delaying circuits for extending output pulse widths. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q_R}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q_R}$ output.
ECL COMMON	– The collector common for the ECL output stage. The collector common may be tied to +5.0V, but normally it is tied to the circuit ground for standard ECL outputs.
$-V_S$	– Negative supply terminal, nominally −5.2V.
R_S	– R_S is the reference current setting terminal. An external setting resistor, R_{SET}, connected between R_S and $-V_S$ determines the internal reference current. See C_S ($250\Omega \le R_{SET} \le 50k\Omega$).
GROUND	– The ground return for the TTL and analog inputs.
LATCH ENABLE	– Transparent TTL latch control line. A logic HIGH on the LATCH ENABLE freezes the digital code at the logic inputs. A logic LOW on the LATCH ENABLE allows the internal current levels to be continuously updated through the logic inputs D_0 thru D_7.
D_0 (LSB)	– One of eight digital inputs used to set the programmed delay. D_0 (LSB) is the least significant bit of the digital input word.
D_3–D_1	– One of eight digital inputs used to set the programmed delay.



AD9500 Functional Block Diagram

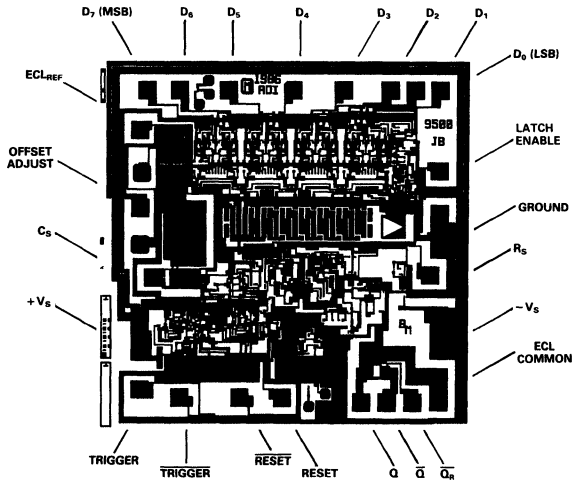


t_S – DIGITAL DATA SETUP TIME
t_H – DIGITAL DATA HOLD TIME
t_{LPW} – LATCH ENABLE PULSE WIDTH
t_{DAC} – INTERNAL DAC SETTLING TIME
t_{PD} – MINIMUM PROPAGATION DELAY
t_{RD} – RESET PROPAGATION DELAY
t_D – PROGRAMMED DELAY
t_{TPW} – TRIGGER PULSE WIDTH
t_{RPW} – RESET PULSE WIDTH
t_{THO} – RESET-TO-TRIGGER HOLDOFF
t_{RHO} – TRIGGER-TO-RESET HOLDOFF

NOTE
A TRIGGERING EVENT MAY OCCUR AT ANY TIME WHILE THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

System Timing Diagram

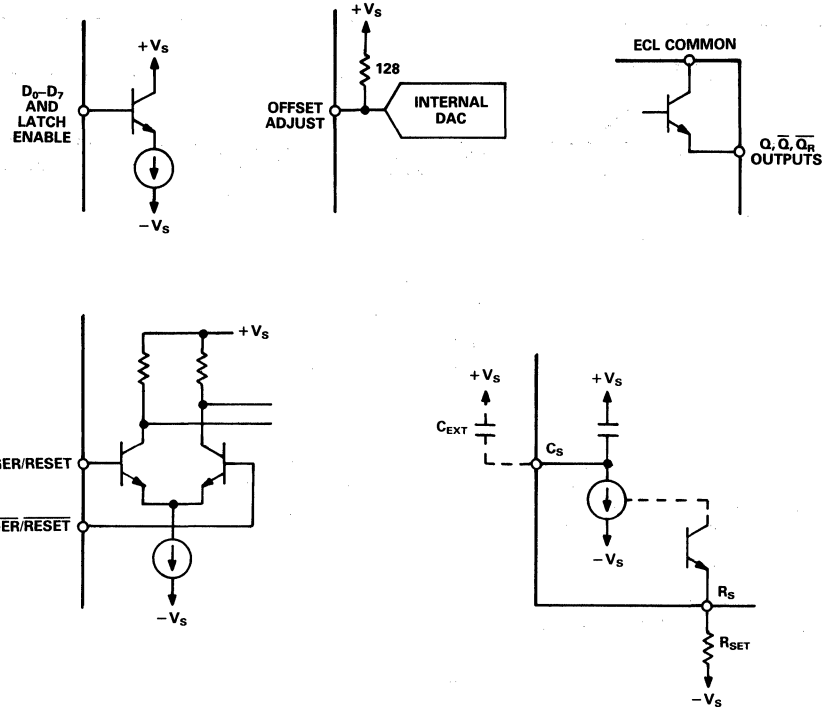
DIE LAYOUT



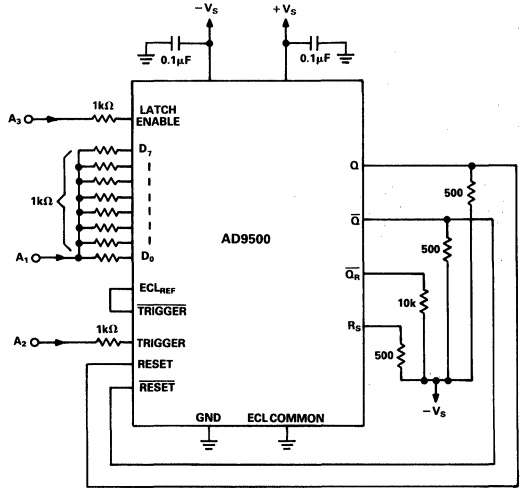
MECHANICAL INFORMATION

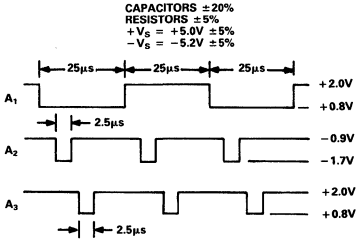
Die Dimensions	104 × 103 × 18 (max) mils
Pad Dimensions	4 × 4 (min)mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold; Gold Ball Bonding

Input/Output Circuits



Burn-In Circuit





INSIDE THE AD9500

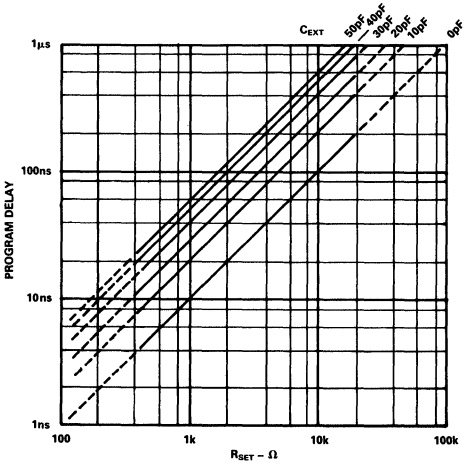
The heart of the AD9500 is the linear ramp generator. A triggering event at the input of the AD9500 initiates the ramp cycle. As the ramp voltage falls, it will eventualy go below the threshold set up by the internal DAC (digital-to-analog converter). A comparator monitors both the linear ramp voltage and the DAC threshold level. The output of the comparator serves as the output for the AD9500, and the interval from the trigger until the output switches is the total delay time of the AD9500.

The total delay through the AD9500 is made up of two components. The first is the full-scale programmed delay, $t_{D\ (max)}$, determined by R_{SET} and C_{EXT}. The second component of the total delay is the minimum propagation delay through the AD9500 (t_{PD}). The full-scale delay is variable from 2.5ns to greater than 1ms. The internal DAC is capable of generating 256 separate programmed delays within the full-scale range (this gives 10ps increments for a 2.5ns full-scale setting).

The actual programmed delay is directly related to both the digital control data (digital data to the internal DAC) and the RC time constant established by R_{SET} and C_{EXT}. The specific relationship is as follows:

Total Delay = Minimum Propagation Delay + Programmed Delay

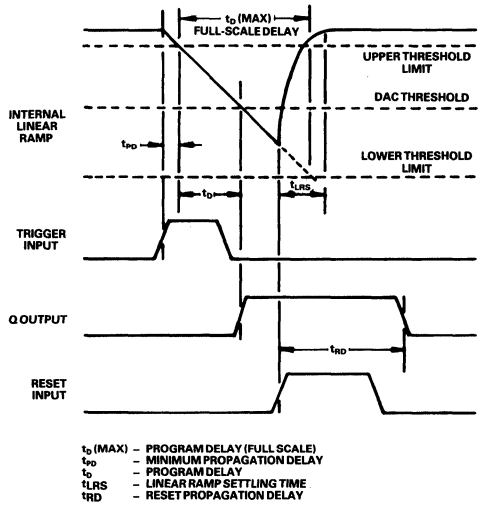
$= t_{PD} + (\text{digital value}/256)\ R_{SET}\ (C_{EXT} + 10pF)$



Typical Programmed Delay Ranges

The internal DAC determines the programmed delay by way of the threshold level at its output. The LATCH ENABLE control for the on-board latch is active (latches) logic "HIGH". In the logic "LOW" state, the latch is transparent, and the internal DAC will attempt to follow changes at the digital data inputs.

Both the LATCH ENABLE control and the data inputs are TTL compatible. The internal DAC may be updated at any time, but full timing accuracy may not be attained unless triggering events are held off until after the DAC settling time (t_{DAC}).



Internal Timing Diagram

On resetting, the ramp voltage held in the timing capacitor (C_{EXT} + 10pF) is discharged. The AD9500 discharges the bulk of the ramp voltage very quickly, but to maintain *absolute* accuracy, subsequent triggering events should be held off until after the linear ramp settling time (t_{LRS}). Applications which employ high frequency triggering at a constant rate will not be affected by the slight settling errors since they will be constant for fixed reset-to-trigger cycles.

The RESET and TRIGGER inputs of the AD9500 are differential and must be driven relative to one another. Accordingly, the TRIGGER and RESET inputs are ideally suited for analog or complementary input signals. Single-ended ECL input signals can be accommodated by using the ECL midpoint reference (ECL_{REF}) to drive one side of the differential inputs.

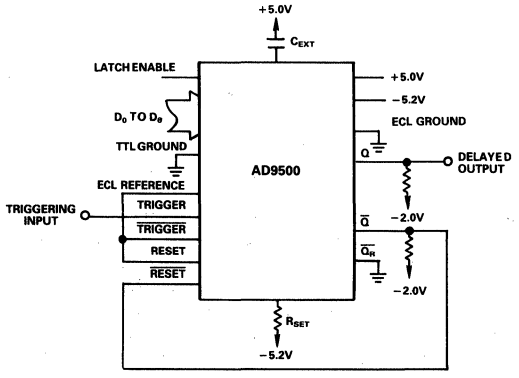
The output of the AD9500 consists of both Q and $\overline{Q}$ driver stages, as well as the $\overline{Q_R}$ output which is used primarily for extending the output pulse width. In the most direct reset configuration, either the Q or the $\overline{Q}$ output is tied to the respective RESET input. This generates a delayed output pulse with a duration equal to the reset delay time (t_{RD}) of approximately 6ns. Note that the reset delay time (t_{RD}) becomes extended for very small programmed delay settings. The duration of the output pulse can be extended by driving the reset inputs with the $\overline{Q_R}$ output through an RC network (see "Extended Output Pulse Width" application). Using the $\overline{Q_R}$ output to drive the reset circuit avoids loading the Q or $\overline{Q}$ outputs.

APPLICATIONS

The AD9500 is a very versatile device, but at the same time, it is not difficult to use. Essentially there are only a few basic configurations which can be extended into a number of applications. The TRIGGER and RESET inputs of the AD9500 can be treated as single ended, or as differential, which allows the AD9500 to operate with a wide range of signal sources. The output pulse from the AD9500 can be reset in one of two ways, either immediately by driving the RESET inputs with the output itself, or in a delayed mode.

MINIMUM CONFIGURATION

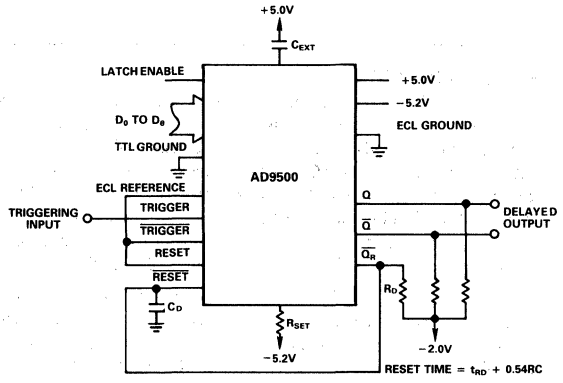
The minimum configuration uses only one of the TRIGGER inputs. The other is connected to the ECL reference midpoint, ECL_{REF}. This allows the AD9500 to be triggered with standard 10K or 10KH ECL signals. Once a triggering event occurs, the Q output will go into the logic HIGH state, and the $\overline{Q}$ output will go into the logic LOW state after the programmed delay. The Q output is then used to drive the RESET input, causing the AD9500 to reset itself. The result is a delayed output pulse which is only as wide as the reset propagation delay (t_{RD}).



Single Input – Minimum Timing Configuration

EXTENDED OUTPUT PULSE WIDTHS

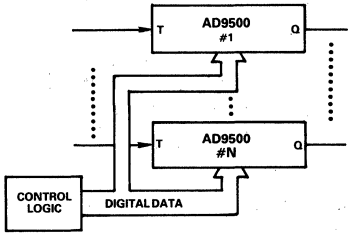
The extended pulse configuration is similar to the minimum configuration. The difference here is that the output pulse width has been extended. Operation is identical in terms of triggering the AD9500; the functional difference is in the resetting circuit. In this case the $\overline{Q_R}$ output is used to drive the $\overline{RESET}$ input through a resistor/capacitor charging network. The charging network will cause the signal at the $\overline{RESET}$ input to fall more slowly, which will extend the output pulse width. An added benefit of the extended pulse width configurations is that both the Q and the $\overline{Q}$ outputs are completely free for other uses.



Extended Output Pulse Width Configuration

MULTICHANNEL DESKEWING

Perhaps the most appropriate use of the AD9500 is in multiple delay matching applications. Slight differences in impedance and cable length can create large timing skews within a high-speed system. Much of this skew can be eliminated by running each signal through an AD9500. With one line used as a standard, the programmed delays of the other AD9500s are adjusted to eliminate the timing skews. With the very fine timing adjustments possible from the AD9500 (as small as 10ps), nearly any high-speed system should be able to automatically adjust itself to extremely tight tolerances.

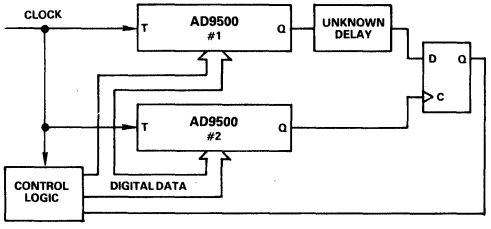


Multiple Delay Matching

MEASURING UNKNOWN DELAYS

Two AD9500s can be combined to measure delays with a high degree of precision. One AD9500 is set with little or no programmed delay, and its output is used to drive the unknown delay circuit, which in turn drives the input of a "D" type flipflop. The second AD9500 is triggered along with the first, and its output provides a clocking signal for the flipflop. The programmed delay of the second AD9500 is then varied to detect the output edge from the unknown delay circuit.

Detecting the output edge is relatively straightforward. If the programmed delay through the second AD9500 is too long, the flipflop output will be at logic HIGH. If, on the other hand, the programmed delay through the second AD9500 is too short, the flipflop output will be at logic LOW. When the programmed delay is properly adjusted, the flipflop will likely bounce between logic HIGH and logic LOW. The digital code value used to create the second programmed delay is a direct indication of the delay through the unknown circuit. The most accurate results can only be attained by calibrating the system without the unknown delay circuit in place.

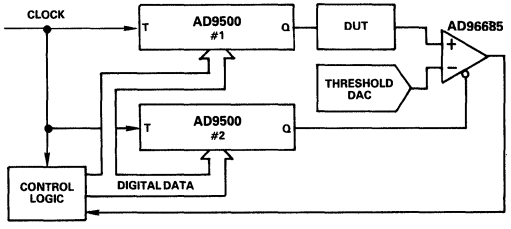


Measuring Unknown Delays

MEASURING HIGH-SPEED AC WAVEFORMS

The same circuitry used to measure unknown delays can be extended to measure the time response of high-speed ac waveforms. With the addition of a digital-to-analog converter and an analog comparator, the circuit functions very much like the previous application. The DAC sets a threshold level which drives one of the differential comparator inputs. The other comparator input is driven by the device under test (DUT). The output of the first AD9500 causes the DUT to produce an output. The second AD9500, which is also triggered along with the first AD9500, strobes the comparator latch enable.

If the DUT output is greater than the DAC threshold when the comparator is latched, the comparator output will be at logic HIGH. If the output is below the DAC threshold, the comparator will be at logic LOW. The programmed delay setting of the second AD9500 is adjusted to the point where the DUT output equals the DAC threshold. By varying the DAC threshold level and adjusting the second AD9500 programmed delay, a point by point reconstruction of the ac waveform can be created.

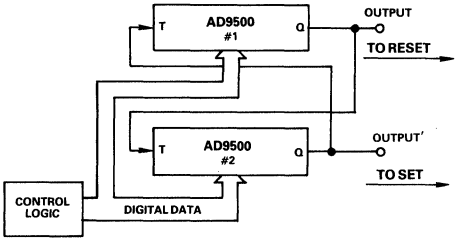


Measuring ac Waveforms

PROGRAMMABLE OSCILLATOR

Another interesting use of the AD9500 is in a digitally programmable oscillator. The highly accurate delays generated by the AD9500 can be exploited to create a ring oscillator with variable duty cycle. The delayed output of the first AD9500 is used to drive the TRIGGER input of the second AD9500. The output of the second AD9500, in turn, is used to drive the TRIGGER input of the first AD9500. Together the two devices will alternately trigger each other creating two pulse chains on the outputs.

The total delay through both AD9500s combined, determines the period of the oscillation frequency. The duty cycle can be controlled by using the outputs to drive the SET and RESET inputs of a flipflop. The total delay through the first AD9500 will control the flipflop logic LOW output pulse width, and the second AD9500 will control the flipflop logic HIGH output pulse width.



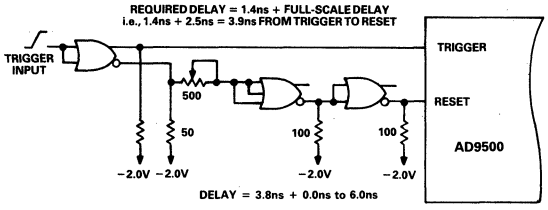
Ring Oscillator

LAYOUT CONSIDERATIONS

The AD9500 is a precision timing device, and as such high-frequency design techniques must be employed to achieve the best performance. The use of a low impedance ground plane is particularly important. Ideally the ground plane should be on the component side of the layout and extend under the AD9500, to shield it from system timing signals. Sockets pose a special problem for a circuit like the AD9500 because of the additional inter-lead capacitance they create. If sockets must be used, pin sockets are generally preferred. Power supply decoupling is also critical to a high-speed design; a 0.1μF ceramic capacitor and a 0.01μF mica capacitor for both power supplies should be very effective. DAC threshold stability can be improved by decoupling the OFFSET ADJUST pin to +5.0V (note that this will lengthen the DAC settling time, t_{DAC}).

100MHz TRIGGERING

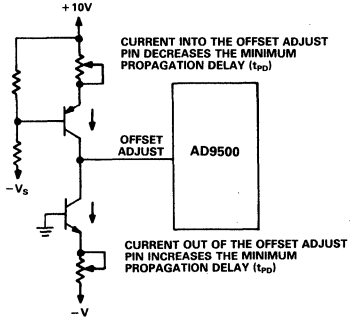
The AD9500 can be triggered at rates above 100MHz. This is accomplished by resetting the AD9500 shortly after it is triggered, which also tends to generate an extremely narrow output pulse. The delay circuit between the trigger input and the reset input provides the variable delay required for various configurations from 2.5ns full-scale to over 10ns full-scale (greater than 10ns total delay precludes 100MHz triggering).



Reset Holdoff for High-Speed Triggering

DELAY OFFSET ADJUSTMENTS

As the full-scale delay is increased, a component of the minimum propagation delay also increases. This is caused by the additional time required by the ramp (now with a much "flatter" slope) to fall below the DAC threshold corresponding to the minimum propagation delay (t_{PD}). One means of decreasing the minimum propagation delay (when the full-scale delay, set by R_{SET} and C_{EXT} is large) is to offset the internal DAC threshold toward the initial ramp levels, thus reducing the time for the internal ramp to cross the threshold once the AD9500 is triggered.



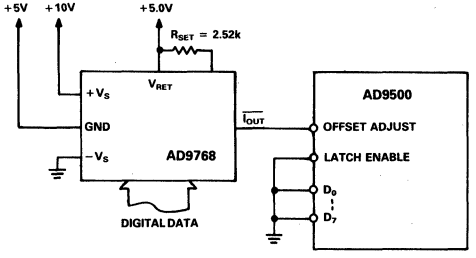
The Offset Adjust Pin Can Be Used to Match Several AD9500s

The DAC levels are offset toward the initial ramp level by injecting a small current into the offset adjust pin. Note, however, that the ramp start-up region is less linear than the later portions of the ramp, which is the primary reason for the built-in offset. If the minimum propagation delay is kept above 5ns (the linear portion of the ramp), no significant degradation in linearity should result. This concept can be extended to match the actual propagation delays of several AD9500s, by injecting or sinking a small current (<2mA) into or out of each of the OFFSET ADJUST pins.

GENERAL PERFORMANCE ENCHANCEMENTS

High-speed operation is generally more consistent if C_{EXT} is kept small (i.e., no external capacitor) to maintain small discharge time constants. Integral linearity, however, benefits from larger values of C_{EXT} by buffering small system spikes and surges. Another means of improving integral linearity is to draw a small current (≈200μA) out of the OFFSET ADJUST pin with a 47kΩ pull-down resistor. This has the effect of moving the internal DAC reference levels into a relatively more linear region of the ramp. This technique is generally only useful for small full-scale delay configurations. Its use with larger full-scale delays will extend the minimum propagation delay (t_{PD}). A pull-up resistor to +5.0V creates the opposite effect by reducing the minimum propagation delay (t_{PD}) at the expense of increased reset propagation delay (t_{RD}) and degraded linearity (see OFFSET matching circuit).

An external DAC can be used with the AD9500 for increased resolution and higher update rates. For the most part, a standard ECL DAC, operating between +5.0V and ground, should work with the AD9500. The output of the external DAC must be connected to the OFFSET ADJUST pin of the AD9500 with the internal DAC turned off (D_0 thru D_7 at logic LOW). For normal operation, the external DAC output should range from 0mA to −2mA (sinking).



Operation with External DAC

ANALOG DEVICES

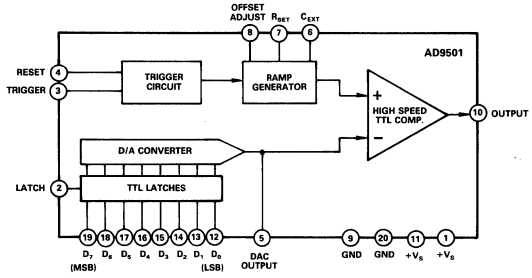
Digitally Programmable Delay Generator

AD9501

FEATURES
Single +5 V Supply
TTL and CMOS Compatible
10 ps Delay Resolution
2.5 ns to 10 μs Full-Scale Range
Maximum Trigger Rate 50 MHz

APPLICATIONS
Disk Drive Deskewing
Data Communications
Test Equipment
Radar I & Q Matching

AD9501 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9501 is a digitally programmable delay generator which provides programmed time delays of an input pulse. Operating from a single +5 V supply, the AD9501 is TTL- or CMOS-compatible, and is capable of providing accurate timing adjustments with resolutions as low as 10 ps. Its accuracy and programmability make it ideal for use in data deskewing and pulse delay applications, as well as clock timing adjustments.

Full-scale delay range is set by the combination of an external resistor and capacitor, and can range from 2.5 ns to 10 μs for a single AD9501. An eight-bit digital word selects a time delay within the full-scale range. When triggered by the rising edge of an input pulse, the output of the AD9501 will be delayed by an amount equal to the selected time delay (t_D) plus an inherent propagation delay (t_{PD}).

The AD9501 is available for a commercial temperature range of 0 to +70°C in a 20-pin plastic DIP, 20-pin ceramic DIP, and a 20-lead plastic leaded chip carrier (PLCC). Military temperature range devices for operation from −55°C to +125°C are available in ceramic DIPs.

11

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage . . . . . +7 V
Digital Input Voltage Range . . . . . −0.5 V to $+V_S$
Trigger/Reset Input Volt. Range . . . . . −0.5 V to $+V_S$
Minimum R_{SET} . . . . . 30 Ω
Digital Output Current (Sourcing) . . . . . 10 mA
Digital Output Current (Sinking) . . . . . 50 mA

Operating Temperature Range
AD9501JN/JP/JQ . . . . . 0 to +70°C
AD9501SQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[2] . . . . . +175°C
Lead Soldering Temperature (10 sec.) . . . . . +300°C

ELECTRICAL CHARACTERISTICS

[$+V_S = +5$ V; C_{EXT} = Open; $R_{SET} = 3090$ Ω (Full-scale range = 100 ns); Pin 8 grounded; and device output connected to Pin 4 RESET input unless otherwise noted]

Parameter	Temp	Test Level	COMMERCIAL 0 to +70°C AD9501JN/JP/JQ Min	Typ	Max	Mil Sub[3]	MILITARY −55°C to +125°C AD9501SQ Min	Typ	Max	Units
RESOLUTION			8				8			Bits
ACCURACY										
Differential Nonlinearity	+25°C	I			0.5	7			0.5	LSB
Integral Nonlinearity	+25°C	I			1	7			1	LSB
Monotonicity	+25°C	I		Guaranteed		7		Guaranteed		
DIGITAL INPUTS										
Logic "1" Voltage	Full	VI	2.0			7, 8	2.0			V
Logic "0" Voltage	Full	VI			0.8	7, 8			0.8	V
Logic "1" Current	Full	VI			60	1, 2, 3			60	μA
Logic "0" Current	Full	VI			3	1, 2, 3			3	μA
Digital Input Capacitance	+25°C	IV			5.5	12			5.5	pF
Data Setup Time (t_S)[4]	+25°C	V		2.5				2.5		ns
Data Hold Time (t_H)[5]	+25°C	V		2.5				2.5		ns
Latch Pulse Width (t_L)	+25°C	V		3.5				3.5		ns
Reset/Trigger Pulse Width (t_R, t_T)	+25°C	V		2				2		ns
DYNAMIC PERFORMANCE										
Maximum Trigger Rate[6]	+25°C	IV	18	22		12	18	22		MHz
Minimum Propagation Delay (t_{PD})[7]	+25°C	I		25	30	4		25	30	ns
Propagation Delay Tempco[8]	Full	V		25				25		ps/°C
Full-Scale Range Tempco	Full	V		36				36		ps/°C
Delay Uncertainty	+25°C	V		53				53		ps
Reset Propagation Delay (t_{RD})[9]	+25°C	I		14.5	17.5	4		14.5	17.5	ns
Reset-to-Trigger Holdoff (t_{THO})[10]	+25°C	V		4.5				4.5		ns
Trigger-to-Reset Holdoff (t_{RHO})[11]	+25°C	V		19				19		ns
Minimum Output Pulse Width[12]	+25°C	V		7.5				7.5		ns
Output Rise Time[13]	+25°C	I		2.3	3.5	9		2.3	3.5	ns
Output Fall Time[13]	+25°C	I		1.0	2.0	9		1.0	2.0	ns
DAC Settling Time (t_{LD})[14]	+25°C	V		30				30		ns
Linear Ramp Settling Time (t_{LRS})[15]	+25°C	V		20				20		ns
DIGITAL OUTPUT										
Logic "1" Voltage (Source 1 mA)	Full	VI	2.4			1, 2, 3	2.4			V
Logic "0" Voltage (Sink 4 mA)	Full	VI		0.24	0.4	1, 2, 3		0.24	0.4	V
POWER SUPPLY[16]										
Positive Supply Current (+5.0 V)	Full	VI		69.5	83	1, 2, 3		69.5	83	mA
Power Dissipation	Full	VI			415	1, 2, 3			415	mW
Power Supply Rejection Ratio[17]										
Full-Scale Range Sensitivity	+25°C	I		0.7	2.0	7		0.7	2.0	ns/V
Minimum Prop Delay Sensitivity	+25°C	I		0.45	1.7	7		0.45	1.7	ns/V

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: 20-lead plastic leaded chip carrier θ_{JA}=73°C/W; θ_{JC}=29°C/W. 20-pin ceramic DIP θ_{JA}=65°C/W; θ_{JC}=20°C/W. 20-pin plastic DIP θ_{JA}=65°C/W; θ_{JC}=26°C/W.
[3]Military subgroups apply only to military-qualified devices.
[4]Digital data inputs must remain stable for the specified time prior to the positive transition of the LATCH signal.
[5]Digital data inputs must remain stable for the specified time after the positive transition of the LATCH signal.
[6]Programmed delay (t_D)=0 ns. Maximum self-resetting trigger rate is limited to 6.9 MHz with 100 ns programmed delay. If t_D=0 ns and external RESET signal is used, maximum trigger rate is 23 MHz.
[7]Programmed delay (t_D)=0 ns. In operation, any programmed delays are in addition to the minimum propagation delay (t_{PD}).
[8]Programmed delay (t_D)=0 ns. [Minimum propagation delay (t_{PD})]
[9]Measured from 50% transition point of the RESET signal input to the 50% transition point of the falling edge of the output.
[10]Minimum time from the falling edge of RESET to the triggering input to insure valid output pulse, using external RESET pulse.
[11]Minimum time from triggering event to rising edge of RESET to insure valid output event, using external RESET pulse. Extends to 125 ns when programmed delay is 100 ns.
[12]When self-resetting with a full-scale programmed delay.
[13]Measured from +0.4 V to +2.4 V; source=1 mA; sink=4 mA..
[14]Measured from the data input to the time when the AD9501 becomes 8-bit accurate, after a full-scale change in the program delay data word.
[15]Measured from the RESET input to the time when the AD9501 becomes 8-bit accurate, after a full-scale programmed delay.
[16]Supply voltage should remain stable within ±5% for normal operation.
[17]Measured at $+V_S$=+5.0 V ±5%; specification shown is for worst case.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

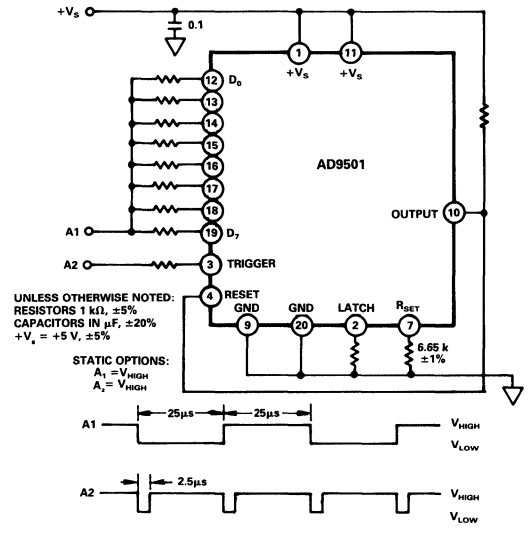
IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C. (5% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 – Static tests at maximum rated operating temperature.
Subgroup 3 – Static tests at minimum rated operating temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated operating temperature.
Subgroup 6 – Dynamic tests at minimum rated operating temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated operating temperature.
Subgroup 11 – Switching tests at minimum rated operating temperature.
Subgroup 12 – Periodically sample tested.



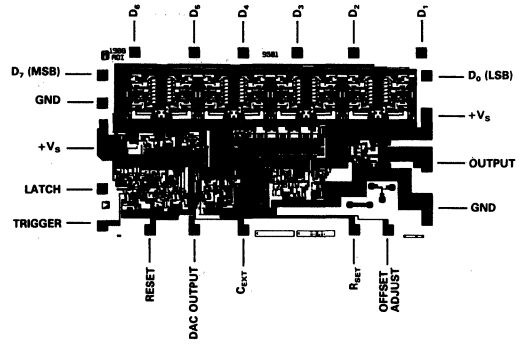
AD9501 Burn-In Circuit

MIL-STD-883 Compliance Information

The AD9501 is a time delay generator and is constructed in accordance with MIL-STD-883. The AD9501 is electrostatic sensitive and falls within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.

DIE LAYOUT AND MECHANICAL INFORMATION

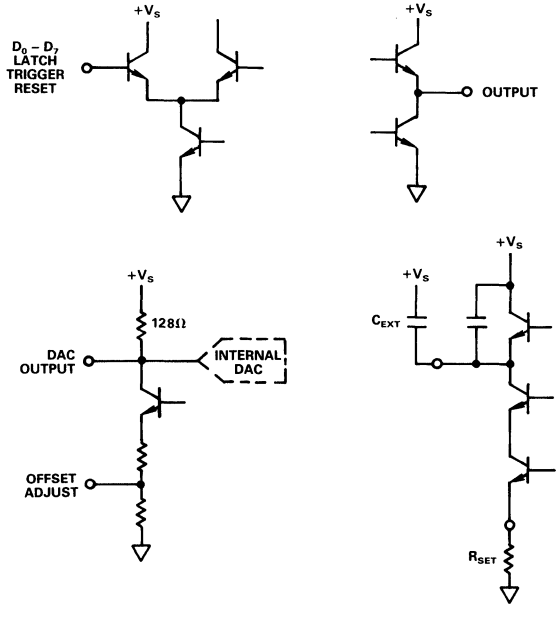


MECHANICAL INFORMATION

Die Dimensions	.89 × 153 × 15 (±2) mils
Pad Dimensions	.4 × 4 mils
Metalization	Aluminum
Backing	.None
Substrate Potential	.Ground
Passivation	.Oxynitride
Die Attach	.Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding

AD9501 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$+V_S$	Positive voltage supply; nominally +5 V.
2	LATCH	TTL/CMOS register control line. Logic HIGH latches input data D_0–D_7. Register is transparent for logic LOW.
3	TRIGGER	TTL/CMOS-compatible input. Rising edge triggers the internal ramp generator, and begins the delay cycle.
4	RESET	TTL/CMOS-compatible input. Logic HIGH resets the ramp voltage and OUTPUT.
5	DAC OUTPUT	Output voltage of the internal digital-to-analog converter.
6	C_{EXT}	Optional external capacitor connected to $+V_S$; used with R_{SET} and 8.5 pF internal capacitor to determine full-scale delay range (t_{DFS}).
7	R_{SET}	External resistor to ground, used to determine full-scale delay range (t_{DFS}).
8	OFFSET ADJUST	Normally connected to GROUND. Can be used to adjust minimum propagation delay (t_{PD}); see Theory of Operation text.
9	GROUND	Circuit ground return.
10	OUTPUT	TTL-compatible delayed output pulse.
11	$+V_S$	Positive voltage supply; nominally +5 V.
12–19	D_0–D_7	TTL/CMOS-compatible inputs, used to set the programmed delay of the AD9501 delayed ouput. D_0 is LSB and D_7 is MSB.
20	GROUND	Circuit ground return.



AD9501 Equivalent Circuits

THEORY OF OPERATION

The AD9501 is a digitally programmable delay device. Its function is to provide a precise incremental delay between input and output, proportional to an 8-bit digital word applied to its delay control port. Incremental delay resolution is 10 ps at the minimum full-scale range of 2.5 ns. Digital delay data inputs, latch, trigger and reset are all TTL/CMOS-compatible. Output is TTL-compatible.

Refer to the block diagram of the AD9501.

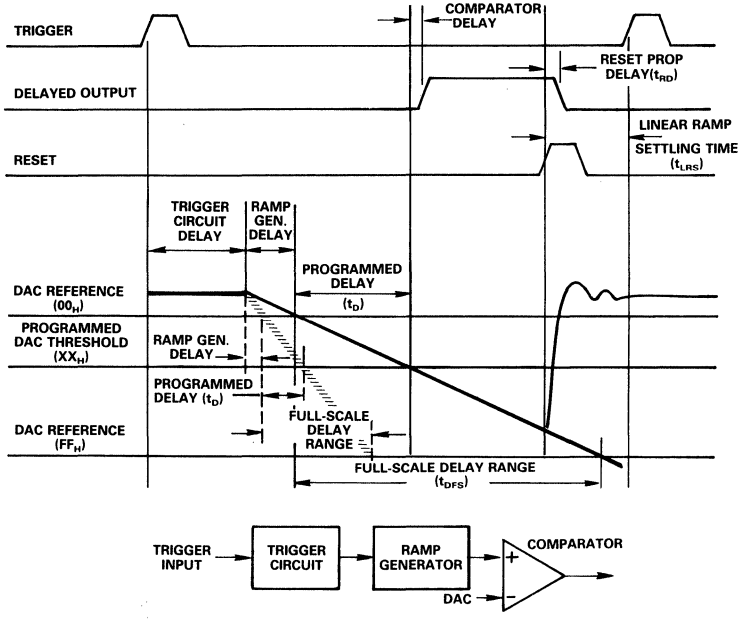
Inside the unit, there are three main subcircuits: a linear ramp generator, an 8-bit digital-to-analog converter (DAC) and a voltage comparator. The rising edge of the input (TRIGGER) pulse initiates the delay cycle by triggering the ramp generator. The voltage comparator monitors the ramp voltage and switches the delayed output (Pin 10) HIGH when the ramp voltage crosses the threshold set by the DAC output voltage. The DAC threshold voltage is programmed by the user with digital inputs.

Figure 1, the AD9501 Internal Timing diagram, illustrates in detail how the delay is determined. Minimum Delay (t_{PD}) is the sum of Trigger Circuit delay, Ramp Generator delay, and Comparator delay.

The Trigger Circuit delay and Comparator delay are fixed; Ramp Generator delay is a variable affected by the rate of change of the linear ramp and (to a lesser degree) the value of the offset voltage described below.

Maximum Delay is the sum of Minimum Delay (t_{PD}) and Full-Scale Program Delay (t_{DFS}).

Ramp Generator delay is the time required for the ramp to slew from its reset voltage to the most positive DAC reference voltage (00_H). The difference in these two voltages is nominally 18 mV (with OFFSET ADJUST open) or 34 mV (OFFSET ADJUST grounded).



MINIMUM PROPAGATION DELAY = (t_{PD}) = TRIGGER CIRCUIT DELAY + RAMP GENERATOR DELAY + COMPARATOR DELAY

MAXIMUM PROPAGATION DELAY = MINIMUM PROPAGATION DELAY(t_{PD}) + FULL-SCALE DELAY RANGE (t_{DFS})

$$\text{PROGRAMMED DELAY } (t_D) = \left(\frac{\text{DIGITALVALUE}}{256}\right) R_{SET} (C_{EXT} + 8.5\text{pF}) \quad (3.84)$$

TOTAL DELAY = (t_{PD}) + (t_D)

AD9501 TESTED WITH C_{EXT} = 0 pF; R_{SET} = 3.09 kΩ (100 ns PROGRAMMED DELAY)

Figure 1. AD9501 Internal Timing

Offset between the two levels is necessary for three reasons. First, offset allows the ramp to reset and settle without re-entering the voltage range of the DAC. Second, the DAC may overshoot as it switches to its most positive value (00_H); this could lead to false output pulses if there were no offset between the ramp reset voltage and the upper reference. Overshoot on the ramp could also lead to false outputs without the offset. Finally, the ramp is slightly nonlinear for a short interval when it is first started; the offset shifts the most positive DAC level below this nonlinear region and maintains ramp linearity for short programmed delay settings.

Pin 8 of the AD9501 is called OFFSET ADJUST (see block diagram) and allows the user to control the amount of offset separating the initial ramp voltage and the most positive DAC reference. This, in turn, causes the Ramp Generator delay to vary.

Figure 2 shows differences in timing which occur if OFFSET ADJUST Pin 8 is grounded or open. The variable Ramp Generator delay is the major component of the three components which comprise Minimum Delay (t_{PD}) and, therefore, is affected by the connection to Pin 8.

It is preferable to ground Pin 8 because the smaller offset that results from leaving it open increases the possibility of false output pulses. When grounding the pin, it should be grounded directly or connected to ground through a resistor or potentiometer with a value of 10 kΩ or less.

Caution is urged when using resistance in series with Pin 8. The possibility of false output pulses, as discussed above, is increased under these circumstances. Using resistance in series with Pin 8 is recommended only when matching minimum delays between two or more AD9501 devices; it is not recommended if using a single AD9501. Changing the resistance between Pin 8 and ground from zero to 10 kΩ varies the Ramp Generator Delay by approximately 35%.

The Full-Scale Delay Range (t_{DFS}) can be calculated from the equation:

$$(t_{DFS}) = R_{SET} \times (C_{EXT} + 8.5\ pF) \times 3.84$$

Whenever Full-Scale Delay Range is 326 ns or less, C_{EXT} should be left open. Additional capacitance and/or larger values of R_{SET} increase the Linear Ramp Settling Time, which reduces the maximum trigger rate. When delays longer than 326 ns are required, up to 500 pF can be connected from C_{EXT} to $+V_S$. R_{SET} should be selected in the range from 50 Ω to 10 kΩ. Graph 1 shows typical Full-Scale Delay Ranges for various values of R_{SET} and C_{EXT}.

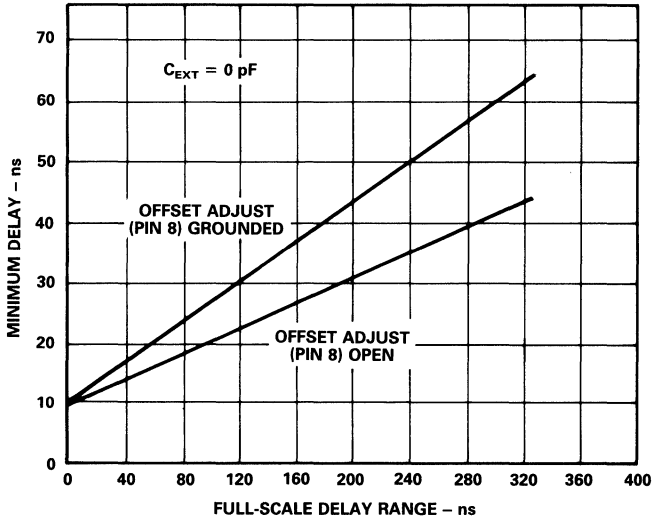
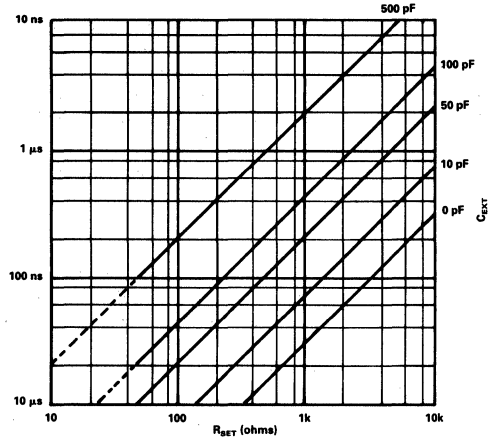


Figure 2. AD9501 Minimum Delay (t_{PD}) vs. Full-Scale Delay Range (t_{DFS})

Ramp charging current and DAC full-scale current are slaved together in the AD9501 to minimize delay drift over temperature. To preserve the unit's low drift performance, both R_{SET} and C_{EXT} should have low temperature coefficients. Resistors which are used should be 1% metal film types.

The programmed delay (t_D) is set by the DAC inputs, D_0–D_7.



Graph 1. RC Values vs. Full-Scale Delay Range (t_{DFS})

The minimum delay through the AD9501 corresponds to an input code of 00_H, and FF_H gives the full-scale delay. Any programmed delay can be approximated by:

$$t_D = (DAC\ code/256) \times t_{DFS}$$

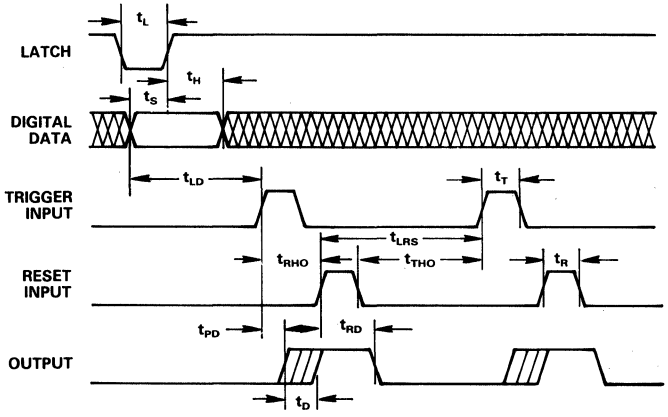
Total delay through the AD9501 for any given DAC code is equal to:

$$t_{TOTAL} = t_D + t_{PD}$$

As shown on the block diagram, TTL/CMOS latches are included to store the digital delay data. Data is latched when LATCH is HIGH. When LATCH is LOW, the latches are transparent, and the DAC will attempt to follow any changes on inputs D_0–D_7.

The System Timing Diagram, Figure 3, shows the timing relationship between the input data and the latch. The DAC settling time (t_{LD}) is approximately 30 ns. After the digital (Programmed Delay) data is updated, a minimum 30 ns must elapse between the time LATCH goes high and the arrival of a TRIGGER pulse to assure rated pulse delay accuracy.

When RESET goes HIGH, the ramp timing capacitor (C_{EXT} + 8.5 pF) is discharged. The RESET input is level-sensitive, and overrides the TRIGGER input. Therefore, any trigger pulse which occurs when RESET is HIGH will not produce an output pulse. As shown on the system timing diagram, Figure 3, the next trigger pulse should not occur before the Linear Ramp Settling Time (t_{LRS}) interval is completed to assure rated pulse delay accuracy.



NOTE: A TRIGGERING EVENT MAY OCCUR AT ANY TIME THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

t_L	– LATCH PULSE WIDTH	t_{RHO}	– TRIGGER-TO-RESET HOLD-OFF
t_H	– DIGITAL HOLD TIME	t_{THO}	– RESET-TO-TRIGGER HOLD-OFF
t_S	– DIGITAL DATA SETUP TIME	t_R	– RESET PULSE WIDTH
t_{LD}	– DAC SETTLING TIME	t_{PD}	– MINIMUM PROPAGATION DELAY
t_T	– TRIGGER PULSE WIDTH	t_{RD}	– RESET PROPAGATION DELAY
t_{LRS}	– LINEAR RAMP SETTLING TIME	t_D	– PROGRAMMED DELAY

Figure 3. AD9501 System Timing

For most applications, OUTPUT can be tied to RESET. This causes the output pulse to be narrow (equal to the Reset Propagation Delay t_{RD}). Alternatively, an external pulse can be applied to RESET. To assure a valid output pulse, however, the delay between TRIGGER and RESET should be equal to or greater than the total delay of $t_{PD} + t_D$ illustrated in the internal timing diagram Figure 1.

As shown in that figure, the capacitor voltage discharges very rapidly and includes a small amount of overshoot and ringing. Rated timing delay will not be realized unless subsequent trigger events are delayed until after the linear ramp settles to its reset voltage value.

The values for the various delay increments in the specification table are based on a Full-Scale Delay Range of 100 ns with OUTPUT tied to RESET (self-resetting operation).

When Full-Scale Delay Range is set for intervals shorter than 100 ns, the rate of change of the linear ramp is increased. This faster rate means the Maximum Trigger Rate shown in the specification table is increased because the Ramp Generator Delay and, consequently, Minimum Propagation Delay t_{PD} become smaller.

Linear Ramp Settling Time t_{LRS} also becomes shorter as Full-Scale Delay Range is decreased. Minimum Delays for various Full-Scale Delay Range values are shown in Figure 2.

APPLICATIONS

The AD9501 is useful in a wide variety of precision timing applications because of its ability to delay TTL/CMOS pulse edges by increments as small as 10 ps.

In Figure 4, the AD9501 typical circuit configuration, the delayed output is tied back to the RESET input. This will produce a narrow output pulse whose leading edge is delayed by an amount proportional to the 8-bit digital word stored in the on-board latches. For the configuration shown, the output pulse width will be equal to the Reset Propagation Delay (t_{RD}). If wider pulses are required, a delay can be inserted between OUTPUT and RESET. If preferred, an external pulse can be used as a reset input to control the timing of the falling edge (and consequently, the width) of the delayed output.

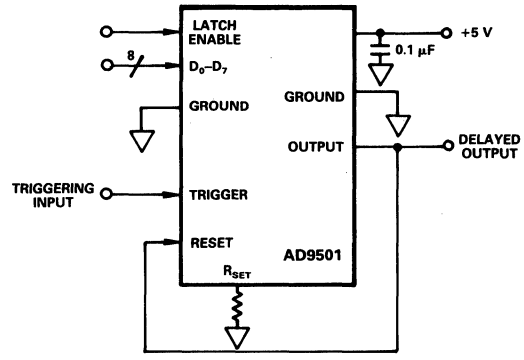


Figure 4. AD9501 Typical Circuit Configuration

Multiple Signal Path Deskewing

High speed electronic systems with parallel signal paths require that close delay matching be maintained. If delay mismatch (time skew) occurs, errors can occur during data transfer. For these situations, the matching of delays is generally accomplished by carefully matching lead lengths.

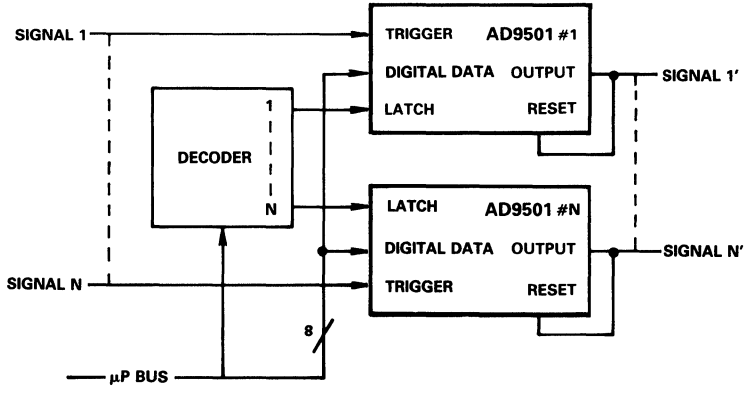


Figure 5. Multiple Signal Path Deskewing

This delay matching is often difficult when using high speed, high-pin-count testers because lead length and circuit impedance can change when the tester setup is changed for different types of devices. The skew which might result from these changes can be compensated by using AD9501 units as shown in Figure 5.

When deskewing multiple signal paths, a single stimulus pulse is applied to all inputs of the AD9501s which are used. The delay for each signal path is then measured by the tester's delay measurement circuit. Using a closed loop technique, all delays are equalized by changing the digital value held in the register of each AD9501. Once all delays have been matched to the desired tolerance, the calibration loop is opened; and the tester is ready to test the new type of device.

Digitally Programmable Oscillator

Two AD9501s can be configured as an astable oscillator, as shown in Figure 6.

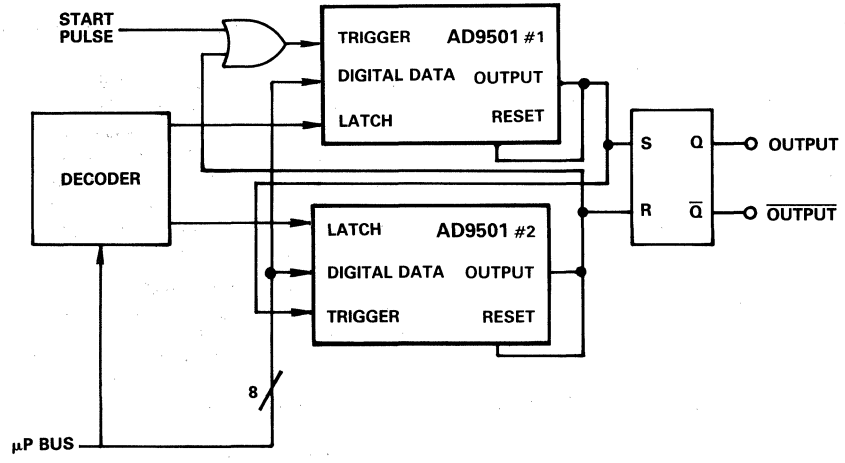


Figure 6. Digitally Programmable Oscillator

Delay through each side of the oscillator is determined by the programmed delay (t_D) of each AD9501 plus the minimum propagation delay (t_{PD}) of each. Increasing the digital value applied to either AD9501 decreases frequency, just as increasing RC decreases frequency in an analog ring oscillator.

Using a pair of AD9501 Delay Generators as shown allows the user great flexibility because both the frequency and the duty cycle of the oscillator are easily controlled.

Frequency of the oscillator output can be established with the equation:

$$f = 1/(2t_{PD} + t_{D1} + t_{D2})$$

when t_{D1} and t_{D2} are the programmed delays of AD9501 #1 and AD9502 #2, respectively.

Programmable Pulse Generator

In this application, shown in Figure 7, two AD9501 units are triggered from a common clock signal. Their outputs go to the inputs of an RS flip-flop. A digital delay value is applied as an input to each with AD9501 #2 typically having a larger value than AD9501 #1.

As shown by the timing portion of the diagram, changing the delay value from one clock cycle to the next generates a pseudo-random pulse whose leading and trailing edge delays are controlled relative to Clock In. The dashed lines illustrate how the programmed delays of the AD9501 components control both the timing and width of the generator output.

The frequency (f) and pulse width (t_{pw}) of the pulse generator can be determined as follows:

$$f = f_{CLOCK\ IN}$$

and:

$$t_{pw} = t_{TOT2} - t_{TOT1}$$

with T_{TOT} being equal to each AD9501's minimum propagation delay (t_{PD}) plus programmed delay (t_D). If both AD9501s are set for the same full-scale delay range, their minimum propagation delays will be approximately the same, and the pulse width will be approximately equal to the difference in programmed delays.

Digital Delay Detector

An unknown digital delay can be measured by applying a repetitive clock to the circuit shown in Figure 8.

The pictured delay detector works in a manner similar to a successive approximation ADC; in this circuit, however, a D-type flip-flop replaces the ADC's voltage comparator.

To calibrate the circuit, short out the unknown delay and apply the clock input to both AD9501 units.

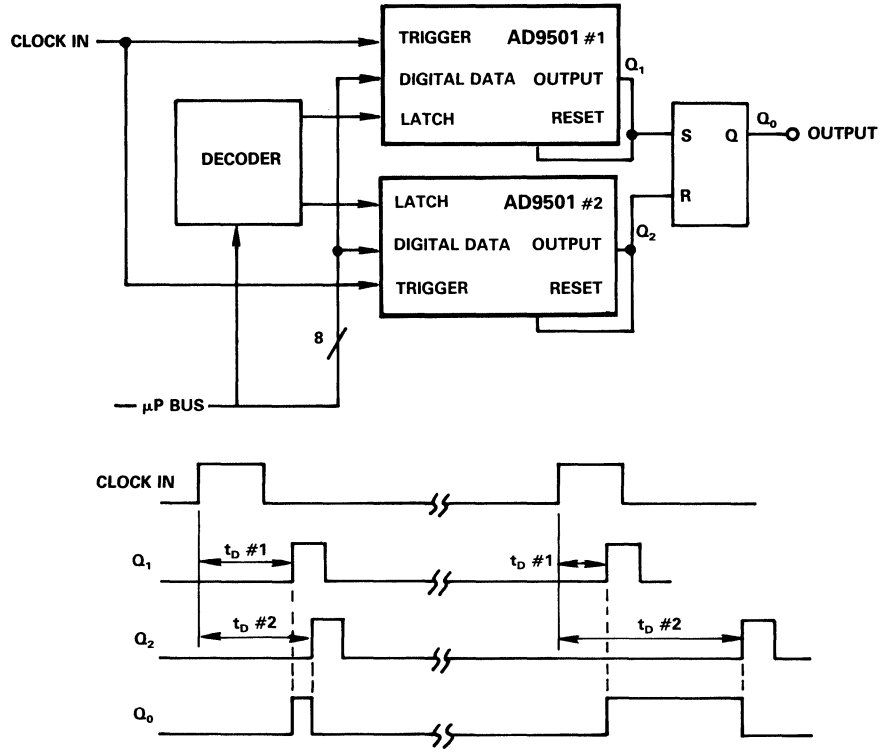


Figure 7. Programmable Pulse Delay Generator

AD9501 #1 should be programmed so its delay is greater than the zero-set programmed delay of AD9501 #2. To accomplish this, continue to apply clock pulses and increment the digital data into AD9501 #1 until the output of the successive approximation register (SAR) is 02H (00000010) or greater. At this point, the delay through AD9501 #1 is slightly longer than the delay through AD9501 #2, making it possible to use the SAR output as the zero reference point for measuring the unknown delay when it is reinserted into the circuit.

This calibration procedure compensates for the setup time of the flip-flop, stray circuit delays and other nonideal characteristics which are an inherent part of any circuit.

Eight cycles of the clock input are required to determine the value of the unknown delay.

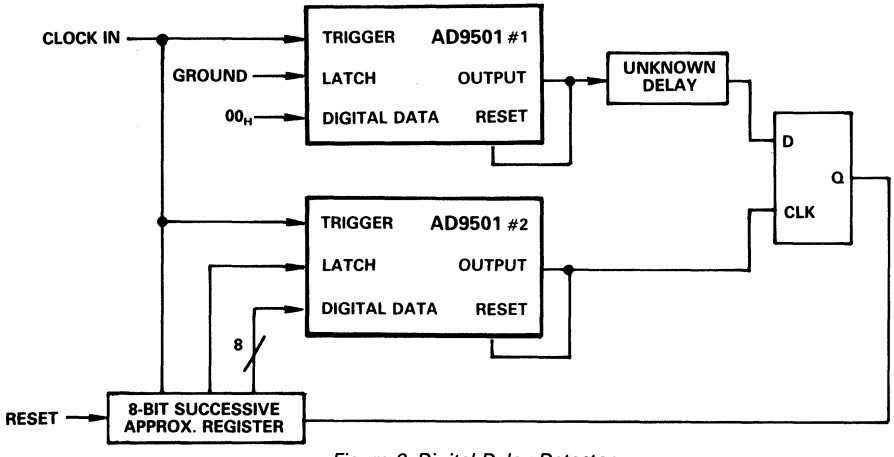


Figure 8. Digital Delay Detector

Analog Settling Time Measurement

This circuit, shown in Figure 9, functions in a manner similar to the digital delay detector; for this application, too, the clock must be repetitive. As in the delay detector, AD9501 #1 is used to cancel the propagation delay of AD9501 #2, propagation delay of the comparators, stray delays, etc. To accomplish this, use the calibration procedure described earlier for the digital delay generator.

The difference betwen the two circuits is in the detection method. The register of the digital delay is replaced by a window comparator for the analog settling measurement.

Threshold voltages V1 and V2 are set for the desired tolerance around the final value of the DUT output signal. As shown in the lower portion of the diagram, the output of the detector is high when the analog output signal of the converter is within the limits set by V_1 and V_2.

Therefore, the settling time can be measured by starting the delay of AD9501 #2 at its maximum setting and decrementing it until the window comparator goes low. The difference between the DAC codes applied to AD9501 #2 and AD9501 #1 is a measure of the settling time of the D/A converter being tested.

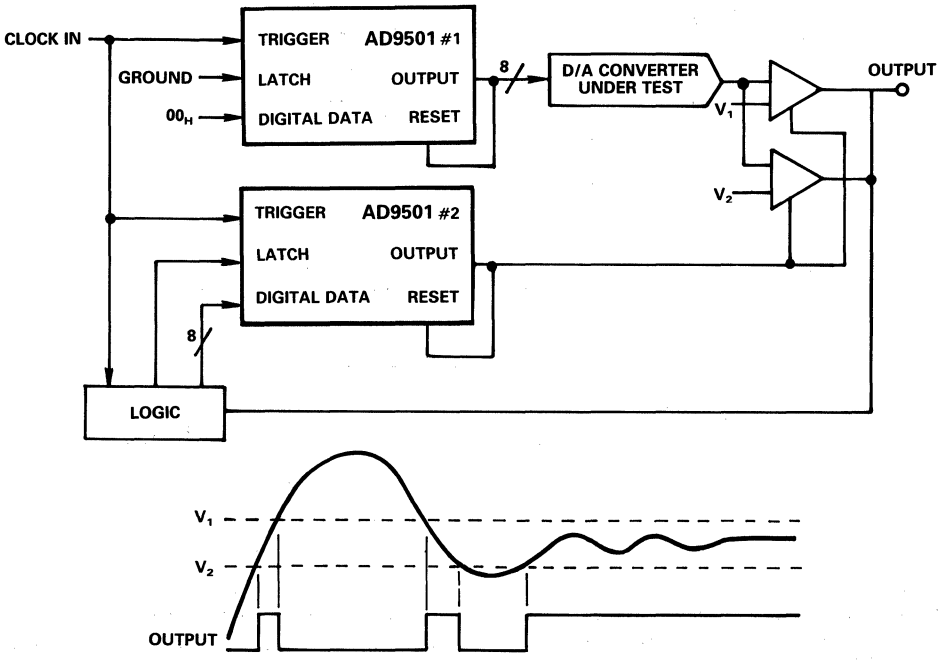


Figure 9. Analog Settling Time Measurement

Layout Considerations

Although the inputs and output of the AD9501 are digital, the delay is determined by analog circuits. This makes it critical to use high speed analog circuit layout techniques to achieve rated performance.

The ground plane should be on the component side of the board and extend under the AD9501 to shield it from digital switching signals. Most socket assemblies add significant inter-lead capacitance, and should be avoided whenever possible. If sockets must be used, individual pin sockets such as AMP part number 6-330808-0 (closed knock-out end) or 6-330808-3 (open end) should be used.

Power supply decoupling is also critical for high speed design; a 0.1 μF capacitor should be connected as close as possible to each supply pin.

ORDERING INFORMATION

Device	Temperature	Description	Package Options*
AD9501JN	0 to +70°C	20-Pin Plastic DIP	N-20
AD9501JP	0 to +70°C	20-Lead PLCC	P-20A
AD9501JQ	0 to +70°C	20-Pin Ceramic DIP	Q-20
AD9501SQ	−55°C to +125°C	20-Pin Ceramic DIP	Q-20

*See Section 20 for package outline information.

ANALOG DEVICES

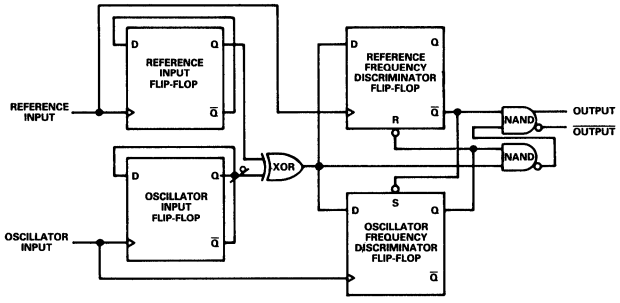
Ultrahigh Speed Phase/Frequency Discriminator

AD9901

FEATURES
Phase and Frequency Detection
ECL/TTL/CMOS Compatible
Linear Transfer Function
No "Dead Zone"

APPLICATIONS
Low Phase Noise Reference Loops
Fast-Tuning "Agile" IF Loops
Secure "Hopping" Communications
Coherent Radar Transmitter/Receiver Chains

AD9901 BLOCK DIAGRAM



GENERAL DESCRIPTION

THE AD9901 is a digital phase/frequency discriminator capable of directly comparing phase/frequency inputs up to 200MHz. Processing in a high speed trench-oxide isolated process, combined with an innovative design, gives the AD9901 a linear detection range, free of indeterminant phase detection zones common to other digital designs.

With a single +5V supply, the AD9901 can be configured to operate with TTL or CMOS logic levels; it can also operate with ECL inputs when operated with a −5.2V supply. The open-collector outputs allow the output swing to be matched to post-filtering input requirements. A simple current setting resistor controls the output stage current range, permitting a reduction in power when operated at lower frequencies.

A major feature of the AD9901 is its ability to compare phase-/frequency inputs at standard IF frequencies without prescalers. Excessive phase uncertainty which is common with standard PLL configurations is also eliminated. The AD9901 provides the locking speed of traditional phase/frequency discriminators, with the phase stability of analog mixers.

The AD9901 is available as a commercial temperature range device, 0 to +70°C, and as a military temperature device, −55°C to +125°C. The commercial version is packaged in a 14-pin ceramic DIP, and the military versions are available in both 14-pin ceramic DIPs and 20-contact ceramic LCC packages.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$ for TTL Operation) . . . . +7V
Negative Supply Voltage ($-V_S$ for ECL Operation) . . . . . −7V
Input Voltage Range (TTL Operation) . . . . . 0V to +5.5V
Differential Input Voltage (ECL Operation) 4.0V
I_{SET} Current 12mA
Output Current 30mA

Operating Temperature Range
AD9901KQ/KP . . . . . 0 to +70°C
AD9901TQ/TE . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[2] . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S = +5.0V$ [for TTL] or $-5.2V$ [for ECL], unless otherwise noted)

			Commercial Temperature 0 to +70°C AD9901KQ/KP				Military Temperature −55°C to +125°C AD9901/TQ/TE			
	Temp	Test Level	Min	Typ	Max	Mil. Sub[3]	Min	Typ	Max	Units
INPUT CHARACTERISTICS										
TTL Input Logic "1" Voltage	Full	VI	2.0			1, 2, 3	2.0			V
TTL Input Logic "0" Voltage	Full	VI			0.8	1, 2, 3			0.8	V
TTL Input Logic "1" Current[4]	Full	VI			0.6	1, 2, 3			0.6	mA
TTL Input Logic "0" Current[4]	Full	VI			1.6	1, 2, 3			1.6	mA
ECL Differential Switching Volt.	Full	VI	300			1, 2, 3	300			mV
ECL Input Current	Full	VI			20	1, 2, 3			20	μA
OUTPUT CHARACTERISTICS										
Peak-to-Peak Output Voltage Swing[5]	Full	VI	1.6	1.8	2.0	1, 2, 3	1.6	1.8	2.0	V
TTL Output Compliance Range	Full	V		3; 7				3; 7		V
ECL Output Compliance Range	Full	V		±2				±2		V
I_{OUT} Range	Full	V		0.9; 11				0.9; 11		mA
Internal Reference Voltage	Full	VI	0.42	0.47	0.52	1, 2, 3	0.42	0.47	0.52	V
PHASE CHARACTERISTICS										
Linear Phase Detection Range[5]										
40kHz	+25°C	V		360				360		Degrees
30MHz	+25°C	V		320				320		Degrees
70MHz	+25°C	V		270				270		Degrees
POWER SUPPLY CHARACTERISTICS										
TTL Supply Current (+5.0V)[6, 7]	+25°C	I		43.5	54.0	1		43.5	54.0	mA
	Full	I		43.5	54.0	2, 3		43.5	54.0	mA
ECL Supply Current (−5.2V)[6, 7]	+25°C	I		42.5	52.5	1		42.5	52.5	mA
	Full	I		42.5	52.5	2, 3		42.5	52.5	mA
Nominal Power Dissipation	+25°C	V		215				215		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Maximum junction temperature should not exceed +175°C. Junction temperature can be calculated by:

$t_J = PD\ (\theta_{JA}) + t_A = PD\ (\theta_{JC}) + t_C$

where:

PD = power dissipation
θ_{JA} = thermal impedance from junction to air (°C/W)
θ_{JC} = thermal impedance from junction to case (°C/W)
t_A = ambient temperature (°C)
t_C = case temperature (°C)
typical thermal impedances:
AD9901 Ceramic DIP = θ_{JA} = 74°C/W; θ_{JC} = 21°C/W
AD9901 LCC = θ_{JA} = 80°C/W; θ_{JC} = 19°C/W
AD9901 PLCC = θ_{JA} = 80°C/W; θ_{JC} = 30°C/W

[3]Military subgroups apply only to military-qualified devices.

[4]V_L = +0.4V; V_H = +2.4V.

[5]R_{SET} = 47.5Ω; R_L = 182Ω.

[6]Includes load current of 10mA (load resistors = 182Ω).

[7]Supply should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

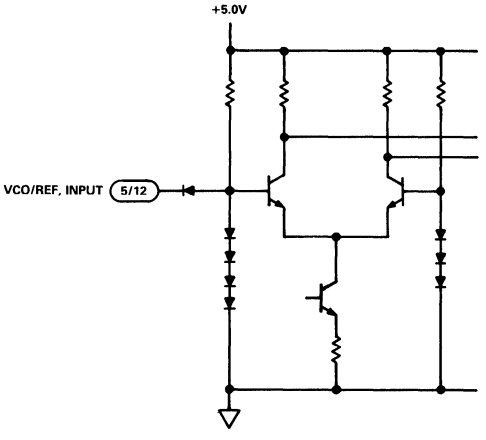
ORDERING INFORMATION

Model	Temperature	Description	Paclage Options*
AD9901KQ	0 to +70°C	14-Pin Ceramic DIP	Q-14
AD9901KP	0 to +70°C	20-Pin PLCC	P-20A
AD9901TQ	−55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD9901TE	−55°C to +125°C	20-Contact Ceramic LCC	E-20A

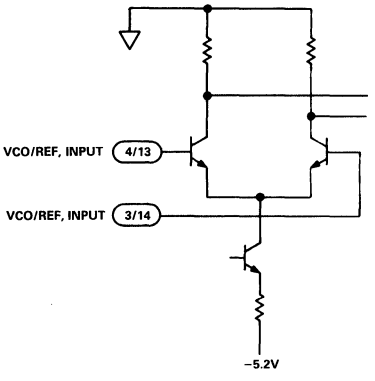
*See Section 20 for package outline information.

INPUT/OUTPUT EQUIVALENT CIRCUITS

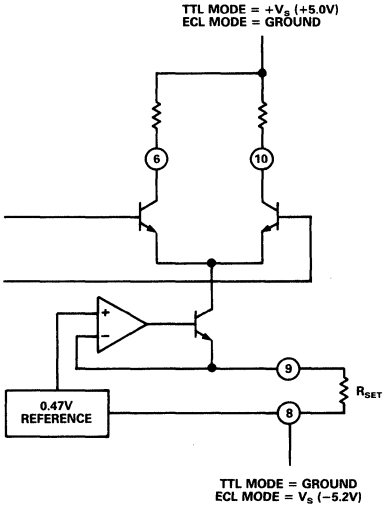
(Based on DIP pinouts)



TTL Input

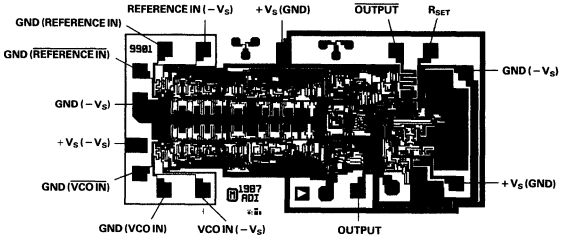


ECL Input



Output

DIE LAYOUT AND MECHANICAL INFORMATION



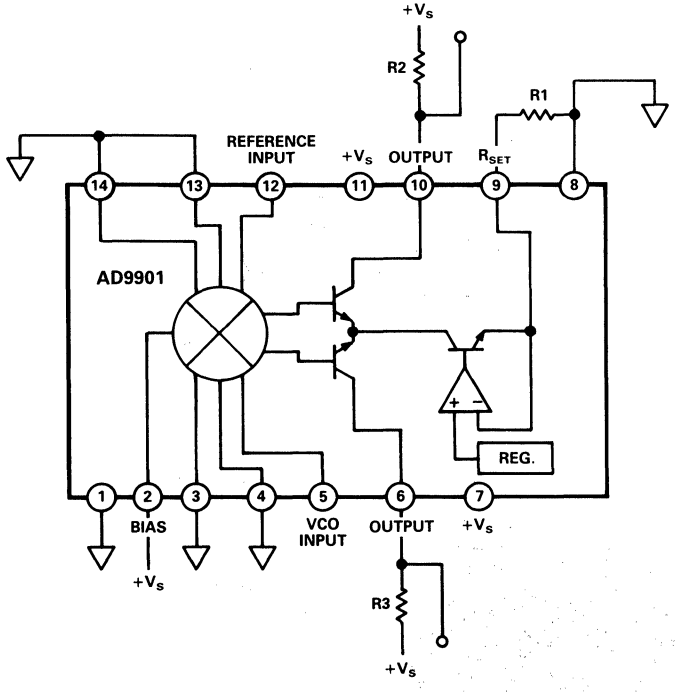
Die Dimensions	63 × 118 × 16(±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding

EXPLANATION OF MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
(5% PDA calculated against Subgroup 1 for high-rel versions)
Subgroup 2 – Static tests at maximum rated operating temperature.
Subgroup 3 – Static tests at minimum rated operating temperature.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at maximum rated operating temperature.
Subgroup 6 – Dynamic tests at minimum rated operating temperature.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at maximum rated operating temperature.
Subgroup 11 – Switching tests at minimum rated operating temperature.
Subgroup 12 – Periodically sample tested.

TTL/CMOS MODE FUNCTIONAL PIN DESCRIPTIONS

GROUND	Ground connections for AD9901. Connect all grounds together and to low-impedance ground plane as close to the device as possible.
$+V_S$	Positive supply connection; nominally +5.0V for TTL operation.
BIAS	Connect to $+V_S$ (+5V) for TTL operation.
VCO INPUT	TTL compatible input; normally connected to the VCO output signal. VCO INPUT and REFERENCE INPUT are equivalent to one another.
OUTPUT	The noninverted output. In TTL/CMOS mode, the output swing is approximately +3.2V to +5V.
R_{SET}	External R_{SET} connection. The current through the R_{SET} resistor is equal to the maximum full-scale output current. R_{SET} should be connected to ground through an external resistor in TTL mode. I_{SET} = 0.47V/R_{SET} = I_{LOAD} (max.)
$\overline{\text{OUTPUT}}$	The inverted output. In TTL/CMOS mode, the output swing is approximately +3.2V to +5V.
REFERENCE INPUT	TTL compatible input, normally connected to the reference input signal. The VCO INPUT and the REFERENCE INPUT are equivalent.



TTL Mode
(Based on DIP Pinouts)

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

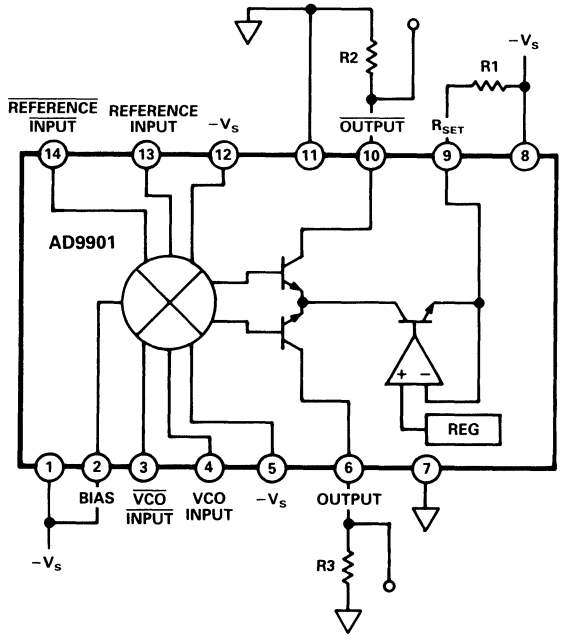
IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ECL MODE FUNCTIONAL PIN DESCRIPTIONS

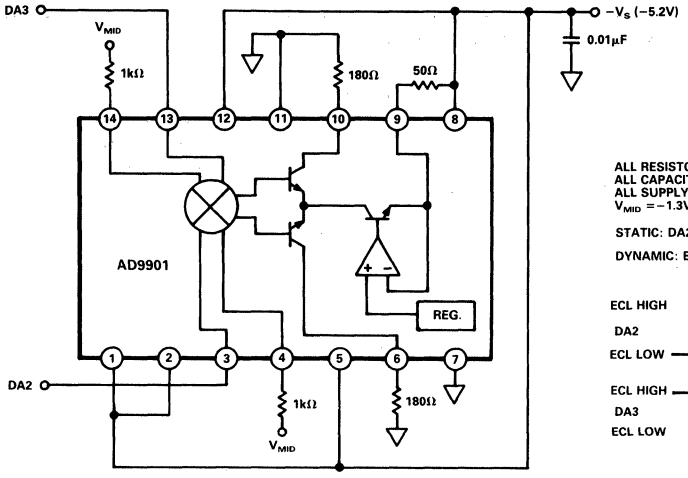
$-V_S$	Negative supply connection, nominally −5.2V for ECL operation.
BIAS	Connect to −5.2V for ECL operation.
$\overline{\text{VCO INPUT}}$	Inverted side of ECL compatible differential input, normally connected to the VCO output signal.
VCO INPUT	Noninverted side of ECL-compatible differential input, normally connected to the VCO output signal.
OUTPUT	The noninverted output. In ECL mode, the output swing is approximately 0V to −1.8V.
GROUND	Ground connections for AD9901. Connect all grounds together and to low-impedance ground plane as close to the device as possible.
R_{SET}	External R_{SET} connection. The current through the R_{SET} resistor is equal to the maximum full-scale output current. R_{SET} should be connected to $-V_S$ through an external resistor in ECL mode. $I_{SET} = 0.47V/R_{SET} = I_{LOAD}$ (max).
$\overline{\text{OUTPUT}}$	The inverted output. In ECL mode, the output swing is approximately 0V to −1.8V.
REFERENCE INPUT	Noninverted side of ECL-compatible differential input, normally connected to the reference input signal. The VCO INPUT and the REFERENCE INPUT are equivalent to one another.
$\overline{\text{REFERENCE INPUT}}$	Inverted side of ECL-compatible differential input, normally connected to the reference input signal. The $\overline{\text{VCO INPUT}}$ and the $\overline{\text{REFERENCE INPUT}}$ are equivalent.



ECL Mode
(Based on DIP Pinouts)

AD9901 BURN-IN CIRCUIT

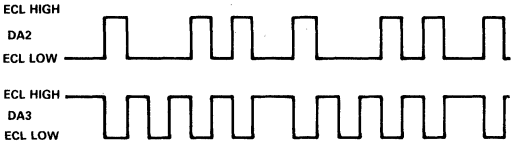
(Based on DIP ECL Pinouts)



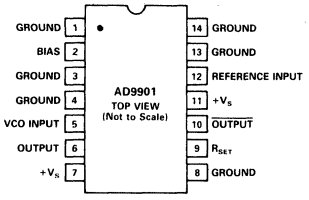
ALL RESISTORS ±5%
ALL CAPACITORS ±20%
ALL SUPPLY VOLTAGES ±5%
V_{MID} = −1.3V ±5%

STATIC: DA2=ECL HIGH; DA3=ECL LOW

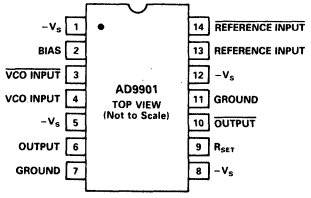
DYNAMIC: ECL HIGH



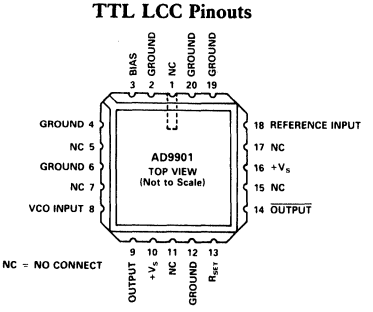
TTL DIP Pinouts



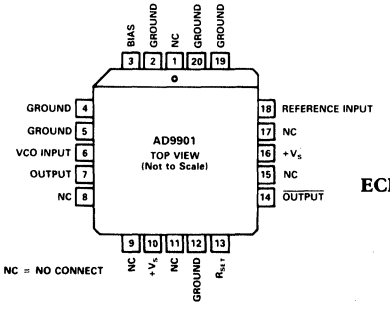
ECL DIP Pinouts



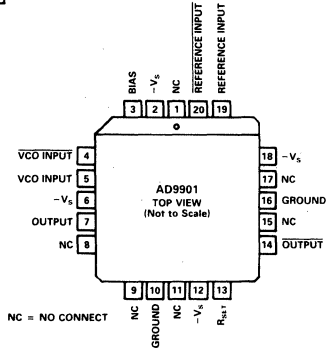
TTL LCC Pinouts



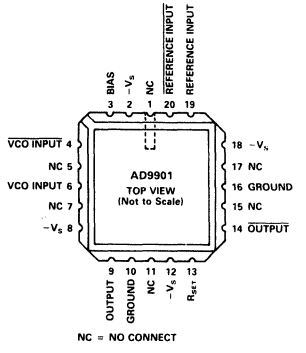
TTL PLCC Pinouts



ECL PLCC Pinouts



ECL LCC Pinouts



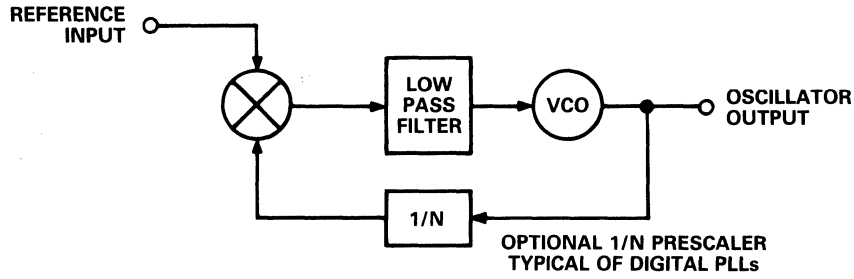


Figure 1. Phase-Locked Loop Control System

THEORY OF OPERATION

A phase detector is one of three basic components of a phase-locked loop (PLL); the other two are a filter and a tunable oscillator. A basic PLL control system is shown in Figure 1.

The function of the phase detector is to generate an error signal which is used to retune the oscillator frequency whenever its output deviates from a reference input signal. The two most common methods of implementing phase detectors are (1) an analog mixer and (2) a family of sequential logic circuits known as digital phase detectors.

The AD9901 is a digital phase detector. As illustrated in the block diagram of the unit, straightforward sequential logic design is used. The main components include four "D" flip-flops, an exclusive-OR gate (XOR) and some combinational output logic. The circuit operates in two distinct modes: as a linear phase detector and as a frequency discriminator.

When the reference and oscillator are very close in frequency, only the phase detection circuit is active. If the two inputs are substantially different in frequency, the frequency discrimination circuit overrides the phase detector portion to drive the oscillator frequency toward the reference frequency and put it within range of the phase detector.

Input signals to the AD9901 are pulse trains, and its output duty cycle is proportional to the phase difference of the oscillator and reference inputs. Figures 2, 3 and 4 illustrate, respectively, the input/output relationships at lock; with the oscillator leading the reference frequency; and with the oscillator lagging. This output pulse train is low-pass filtered to extract the dc mean value $[K_\phi (\phi_I - \phi_O)]$ where K_ϕ is a proportionality constant (phase gain).

At or near lock (Figures 2, 3 and 4), only the two input flip-flops and the exclusive-OR gate (the phase detection circuit) are active. The input flip-flops divide both the reference and oscillator frequencies by a factor of two. This insures that inputs to the exclusive-OR are square waves, regardless of the input duty cycles of the frequencies being compared. This division-by-two also moves the nonlinear detection range to the ends of the range rather than near lock, which is the case with conventional digital phase detectors.

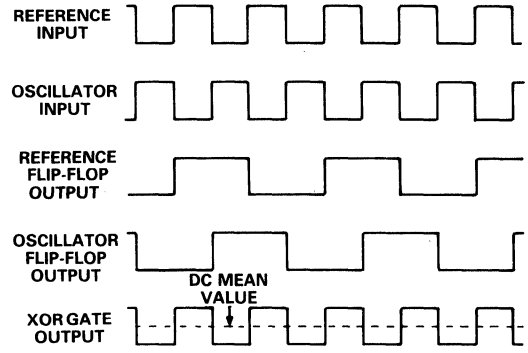


Figure 2. AD9901 Timing Waveforms at "Lock"

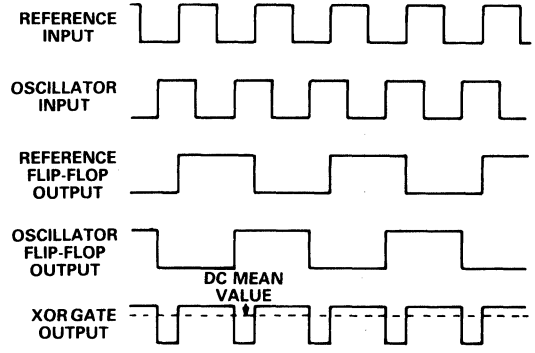


Figure 3. Timing Waveforms (ϕ_{OUT} Leads ϕ_{IN})

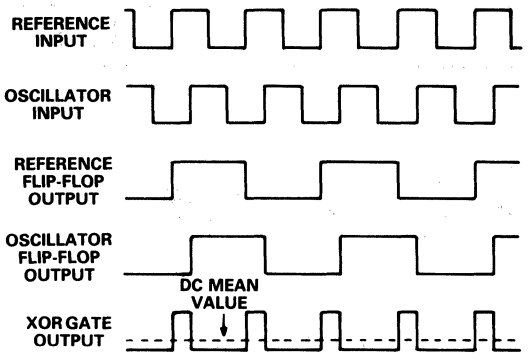


Figure 4. Timing Waveforms (ϕ_{OUT} Lags ϕ_{IN})

Figure 5 illustrates the constant gain near lock.

When the two square waves are combined by the XOR, the output has a 50% duty cycle if the reference and oscillator inputs are exactly 180° out of phase; under these conditions, the AD9901 is operating in a locked mode. Any shift in the phase relationship between these input signals causes a change in the output duty cycle. Near lock, the frequency discriminator flip-flops provide constant HIGH levels to gate the XOR output to the final output.

The duty cycle of the AD9901 is a direct measure of the phase difference between the two input signals when the unit is near lock. The transfer function can be stated as $[K_\phi(\phi_I - \phi_O)](V/RAD)$, where K_ϕ is the allowable output voltage range of the AD9901 divided by 2π.

For a typical output swing of 1.8V, the transfer function can be stated as ($1.8V/2\pi = 0.285V/RAD$). Figure 5 shows the relationship of the dc mean value of the AD9901 output as a function of the phase difference of the two inputs.

It is important to note that the slope of the transfer function is constant near its midpoint. Many digital phase comparators have an area near the lock point where their gain goes to zero, resulting in a "dead zone." This causes increased phase noise (jitter) at the lock point.

The AD9901 avoids this dead zone by shifting it to the endpoints of the transfer curve, as indicated in Figure 5. The increased gain at either end increases the effective error signal to pull the oscillator back into the linear region. This does not affect phase noise, which is far more dependent upon lock region characteristics.

It should be noted, however, that as frequency increases, the linear range is decreased. At the ends of the detection range, the reference and oscillator inputs approach phase alignment. At this point, slew rate limiting in the detector effectively increases phase gain. This decreases the linear detection by nominally 3.6ns. Therefore, the typical detection range can be found by calculating $[(1/F - 3.6ns)/(1/F)] \times 360°$. As an example, at 200MHz the linear phase detection range is ±50°.

Away from lock, the AD9901 becomes a frequency discriminator. Any time either the reference or oscillator input occurs twice before the other, the Frequency High or Frequency Low flip-flop is clocked to logic LOW. This overrides the XOR output and holds the output at the appropriate level to pull the oscillator toward the reference frequency. Once the frequencies are within the linear range, the phase detector circuit takes over again. Combining the frequency discriminator with the phase detector eliminates locking to a harmonic of the reference.

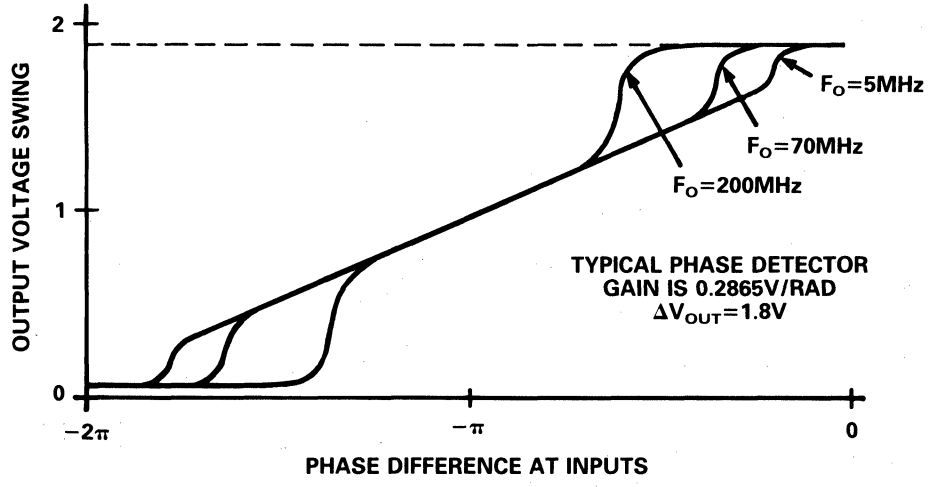
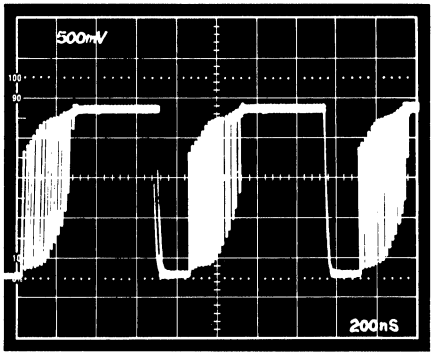


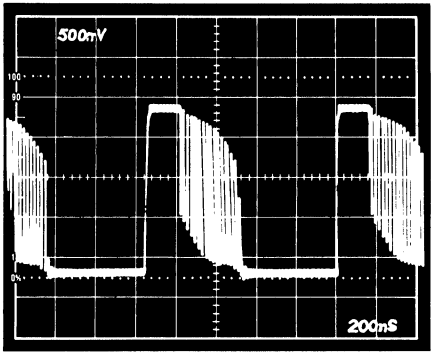
Figure 5. Phase Gain Plot

Photograph 1 shows the effect of the "Frequency Low" flip-flop when the oscillator frequency is much lower than the reference input. The narrow pulses, which result from cycles when two positive reference-input transitions occur before a positive VCO edge, increase the dc mean value. Photograph 2 illustrates the inverse effect when the "Frequency High" flip-flop reacts to a much higher VCO frequency.

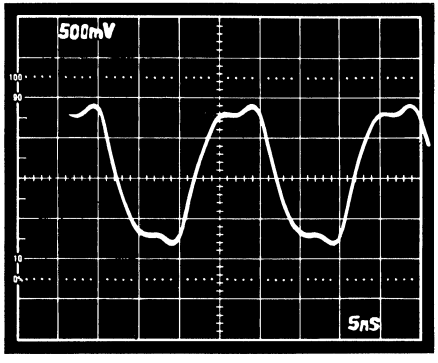
Photograph 3 shows the output waveform at lock for 50MHz operation. This output results when the phase difference between reference and oscillator is approximately $-\pi$Rad.



Photograph 1. AD9901 Output Waveform($F_O << F_I$)



Photograph 2. AD9901 Output Waveform ($F_O >> F_I$)



Photograph 3. AD9901 Output Waveform (F_O=F_I= 50MHz)

AD9901 APPLICATIONS

Page 10 of the data sheet illustrates a phase-locked loop (PLL) system utilizing the AD9901. The first step in designing this type of circuit is to characterize the VCO's output frequency as a function of tuning voltage. The transfer function of the oscillator in the diagram is shown in Figure 6.

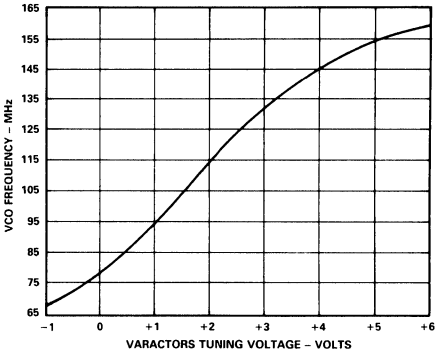


Figure 6. VCO Frequency vs. Voltage

Next, the range of frequencies over which the VCO is to operate is examined to assure that it lies on a linear portion of the transfer curve. In this case, frequencies from 100MHz to 120MHz result from tuning voltages of approximately +1.5V to +2.5V. Because the nominal output swing of the AD9901 is 0 to −1.8V, an inverting amplifier with a gain of 2 follows the loop filter.

As shown in the illustration, a simple passive RC low-pass filter made up of two resistors and a tantalum capacitor eliminates the need for an expensive high speed op amp active-filter design. In this passive-filter second-order-loop system, where n = 2, the damping factor is equal to:

$$\delta = 0.5\,[K_O K_d/n(\tau_1 + \tau_2)]^{1/2}\,[\tau_2 + (n/K_O K_d)]$$

and the values for τ_1 and τ_2 are the low-pass filter's time constants R_1C and R_2C. The gain of 2 of the inverting stage, when combined with the phase detector's gain, gives:

$$K_d = 0.572V/RAD$$

With K_O = 115.2RAD/s/V, τ_1 equals 1.715s, and τ_2 equals 3.11×10^{-4}s for the required damping factor of 0.7. The illustrated values of 30Ω (R_1), 160Ω (R_2), and 10μF (C) in the diagram approximate these time constants.

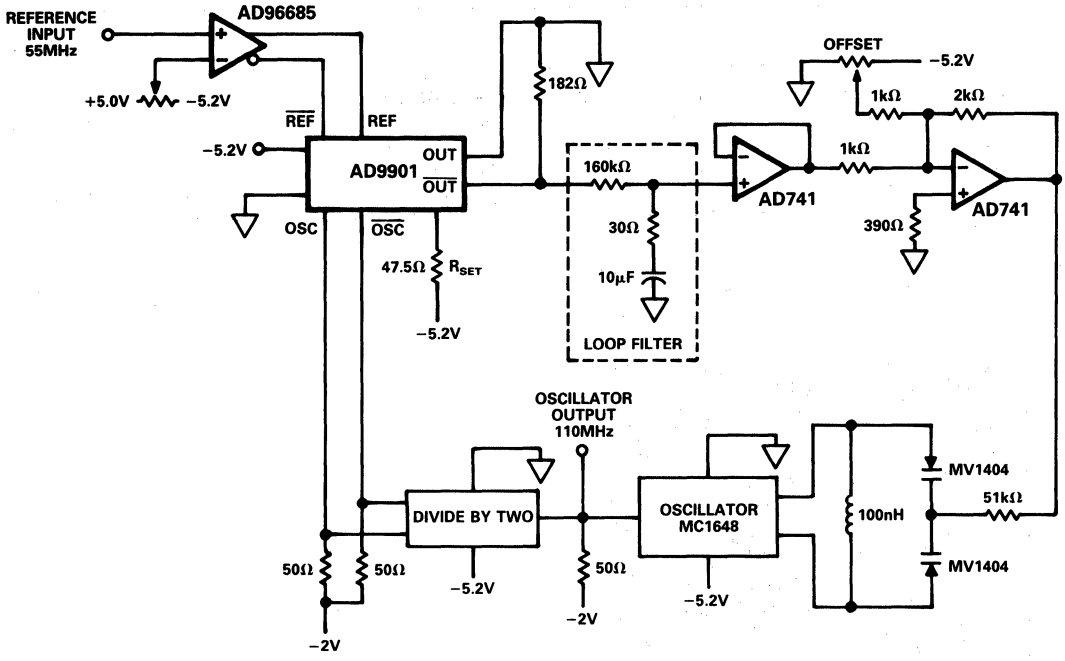
The gain of the RC filter is:

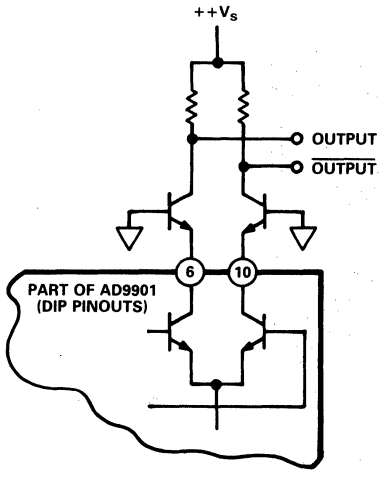
$$V_O/V_I = (1 + sR_2C)/[1 + s(R_1 + R_2)C].$$

Where $K_O K_d >> \omega_n$, the system's natural frequency:

$$\omega_n = [K_O K_d/n(\tau_1 + \tau_2)]^{1/2} = 4.5\text{kHz}.$$

For general information about phase-locked loop design, the user is advised to consult the following references: Gardner, *Phase-Lock Techniques* (Wiley); or Best, *Phase Locked Loops* (McGraw-Hill).





ALTERNATE HIGH LEVEL OUTPUT CIRCUIT
(++V_S TYPICALLY +15V TO +60V)

Phased Locked Loop Using AD9901

Temperature Transducers
Contents

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Selection Guide . . . . . 12 – 2
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AC2626 – General Purpose Temperature Probe . . . . . 12 – 5
AD590 – Two-Terminal IC Temperature Transducer . . . . . 12 – 7
AD592 – Low Cost, Precision IC Temperature Transducer . . . . . 12 – 17

Selection Guide
Temperature Transducers

Model	I_{OUT} µA/K	Cal Error °C max	Nonlin °C max	Package Options[1]	Temp Range[2]	Page	Comments
AC2626	**1**	**0.5–5**	**0.3–1.5**	**3/16″ Stainless Steel Sheath**	**C, M**	**12–5**	**General Purpose Temperature Probe 4″ and 6″ Length**
AD590	**1**	**0.5–5**	**0.3–1.5**	**F, H**	**M+**	**12–7**	**Wide Temperature Range, Accurate**
AD592	**1**	**0.5–2.5**	**0.15–0.35**	**N**	**I+**	**12–17**	**Low Cost, Accurate**

[1]Package Options: F–Flat Pack; H–Round Hermetic Metal Can (Header); N–Plastic Molded Dual-In-Line.
[2]Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.

Orientation
Temperature Transducers

The devices in this section are two-terminal monolithic integrated circuits designed to measure temperatures within the range −55°C to +150°C. When +4V to +30V of excitation voltage is applied, they act as current sources that provide an output proportional to absolute temperature, 1μA/K. Expressed in degrees Celsius (T_C),

$$I = 1\mu A/°C \cdot T_C + 273.2\mu A$$

Current sources have a number of advantages: they are based on a linear relationship and are highly repeatable; the current is independent of voltage drops, voltage noise and common-mode voltage – and practically independent of excitation voltage; the current can be translated to a voltage at a remote destination via an appropriate value of resistance (V = I R) – and simple offsetting circuitry (if necessary).

They are easy to use; they don't require linearization circuitry, high-precision voltage amplifiers, resistance-measuring circuitry or cold-junction compensation. Indeed, they are themselves widely used for cold-junction compensation of thermocouple circuitry.

There are many other applications, including appliance temperature sensing, automotive temperature measurement and control, HVAC (heating, ventilating and air conditioning) system monitoring, industrial temperature control, board-level electronics temperature diagnostics, temperature readout options in instrumentation and temperature-correction circuitry for precision electronics.

AD592 Low-Cost Precision IC Temperature Transducer
The AD592 is a low-cost, plastic packaged device with an operating temperature range of −25°C to +105°C and precalibrated accuracy (using laser wafer-trimming) to within 0.5°C (AD592CN) at +25°C. Its specified nonlinearity (maximum deviation from a best straight line) is 0.35°C maximum over temperature and less than 0.15°C from 0 to +70°C.

AD590 IC Temperature Transducer
The AD590 is similar in principle to the AD592 but is encased in a choice of a hermetically sealed metal can and a probe-compatible ceramic sensor package. Its maximum temperature range for rated performance is −55°C to +150°C, with maximum nonlinearity of 0.3°C over the temperature range (AD590M).

AC2626 General-Purpose Temperature Probe
The AC2626 is a stainless steel tubular probe containing an AD590 chip, with specifications generally similar to those of the AD590. The probe has an outside diameter of 3/16″ (4.76mm); it is available in 6″ (152.4mm) and 4″ (101.6mm) lengths and has 3-foot Teflon-coated lead wires.

The probe is designed for immersion in both liquids and gases and can also be used for temperature measurements in refrigeration and general temperature monitoring. Its applications include flow-rate measurement, level detection of fluids and anemometry.

For measurements in pipes or other closed vessels, a compression fitting (AC2629) is available. It may be applied anywhere along the probe and is available in a choice of brass and stainless steel.

RELATED PRODUCTS

A variety of digital panel instruments are available for use in temperature monitoring. They can be found in the section on Digital Panel Instruments. The AD2040* low-cost, 3-digit temperature indicator and the AD2038* 6-channel digital scanning thermometer may be of especial interest.

For interfacing temperature measurements to systems, signal-conditioning products in wide variety of architectures and physical forms can be found in the section on signal conditioning; for the circuit designer, suitable operational, instrumentation and isolation amplifiers can be found in the respective sections.

For background information, a valuable aid to understanding, design, and applications is the *Transducer Interfacing Handbook*, published by Analog Devices (1980). It is available for $14.50 (hard cover) from P. O. Box 796, Norwood, MA 02062.

***Data sheets available upon request.**

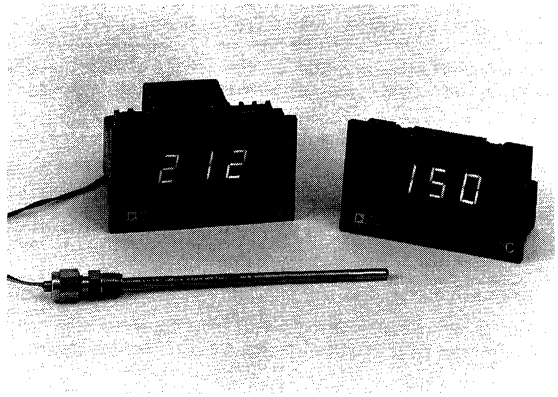
ANALOG DEVICES

General Purpose Temperature Probe

AC2626

FEATURES

- **Linear Current Output: 1μA/K**
- **Wide Range: -55°C to +150°C**
- **Laser Trimmed Sensor (AD590) to ±1.0°C Calibration Accuracy (AC2626L)**
- **Excellent Linearity: ±0.4°C Over Full Range (AC2626L)**
- **6 Inch or 4 Inch Standard, Stainless Steel Sheath**
- **3/16 Inch in Outside Diameter**
- **3 Feet Teflon Coated Lead Wire**
- **Wide Power Supply Range +4V to +30V**
- **Low Cost**
- **Fast Response: 2 Seconds (In Stirred Water)**
- **Sensor Isolated From Sheath**



PRODUCT DESCRIPTION

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4-inch (101.6mm) lengths. The probe is available in linearity grades of 0.3°C, 0.4°C, 0.8°C or 1.5°C.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AC2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

PRODUCT HIGHLIGHTS

The AC2626 is based on the AD590 temperature transducer, a two terminal integrated circuit which produces an output current linearly proportional to absolute temperature.

Costly linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AC2626.

Due to the high impedance current output of the AD590, the AC2626 is particularly useful in remote sensing applications, because of its insensitivity to voltage drops over lines. The output characteristics also make the AC2626 easy to multiplex.

In addition to temperature measurement, applications include temperature compensation, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry.

DIRECT INTERFACE PRODUCTS

For display and/or control applications, two companion products are available. The AD2038, 6 channel digital thermometer, and the AD2040, low cost temperature indicator, were designed to be used in conjunction with the AC2626.

1. The AD2038 is a low cost, ac line powered 6 channel digital scanning thermometer designed to interface to printers, computers, serial data transmitters, etc., for display, control, logging or transmission of multi-point temperature data. Channel selection is made via three methods: manual, using the switch provided on the front; auto/scan, where the AD2038 cycling on an internal clock can continually scan the six input channels or external selection, where control inputs provided on the rear connector enable channel selection via external BCD coding.
2. The AD2040 is a low cost, 3 digit temperature indicator. An internal precision voltage reference, resistor network and span and zero adjusts allow the AD2040 to read out directly in °C, °F, K or R. User selectable readout as well as all other connections, i.e., +5V dc power and AC2626 interface are all made via the terminal block on the rear.

APPLICATION HINTS

1. Under all operating conditions, a minimum 4V dc must be present across the AC2626.
2. Use of twisted pair wiring is recommended, particularly for remote applications or in high noise environments. Shielded wire is desirable in severe noise environments.
3. For the lowest cost, the J and K grades are recommended. Where probe interchangeability is desired, grade L is recommended.

SPECIFICATIONS (typical @ +25°C and +5V unless otherwise specified)

MODEL	AC2626J	AC2626K	AC2626L	AC2626M
ABSOLUTE MAXIMUM RATINGS[1]				
Forward Voltage (V_S)	+44V	*	*	*
Reverse Voltage (V_S)	-20V	*	*	*
Breakdown Voltage (Case to Leads)	±200V	*	*	*
Rated Performance Temp. Range	-55°C to +150°C	*	*	*
Storage Temperature Range	-60°C to +160°C	*	*	*
POWER SUPPLY				
Operating Voltage Range	+4V to +30V	*	*	*
OUTPUT				
Nominal Current Output @ +25°C (298.2°K)	298.2μA	*	*	*
Nominal Temperature Coefficient	1μA/°C	*	*	*
Calibration Error @ +25°C	±5.0°C max	±2.5°C max	±1.0°C max	±0.5°C max
Absolute Error (over rated performance temperature range)				
Without External Calibration Adjustment	±10.0°C max	±5.5°C max	±3.0°C max	±1.7°C max
With +25°C Calibration Error Set to Zero	±3.0°C max	±2.0°C max	±1.6°C max	±1.0°C max
Nonlinearity	±1.5°C max	±0.8°C max	±0.4°C max	±0.3°C max
Repeatability[2]	0.1°C	*	*	*
Long Term Drift[3]	0.1°C max/month	*	*	*
Time Constant[4] (in stirred water)	2 sec.	*	*	*
Current Noise	40pA$\sqrt{Hz}$	*	*	*
Power Supply Rejection				
+4V≤V_S≤+5V	0.5μA/V	*	*	*
+5V≤V_S≤+15V	0.2μA/V	*	*	*
+15V≤V_S≤+30V	0.1μA/V	*	*	*
Electrical Turn-On Time	20μs	*	*	*
+ Lead Color	yellow	orange	blue	green

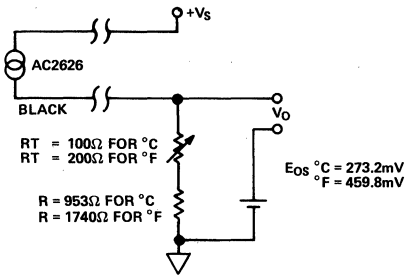
ORDERING GUIDE

AC2626
- GRADE: J, K, L — ENTER
- LENGTH: 4, 6 — ENTER

AC2629
- BRASS: B
- TYPE 316 STAINLESS: SS — ENTER

NOTES
[1] Maximum safe recommended pressure: 7500psi (5.17 × 10^4 Kpa).
[2] Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed, not tested.
[3] Conditions: constant +5V, constant +125°C; guaranteed, not tested.
[4] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.
*Specifications same as AC2626J.
Specifications subject to change without notice.

CALIBRATION



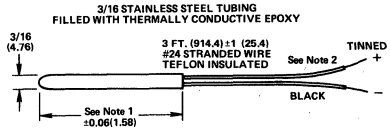
For most applications, a single point calibration is sufficient. With the probe at a known temperature, adjust R_T so that V_O corresponds to the known temperature.

If more detailed information is desired, see the AD590 data sheet and application note.

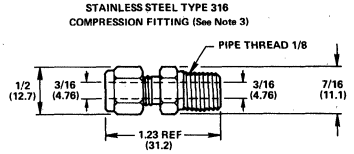
MECHANICAL OUTLINE

Dimensions shown in inches and (mm).

AC2626



AC2629



NOTE 1 Probes are available in 4-inch or 6-inch lengths.
NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue.
NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

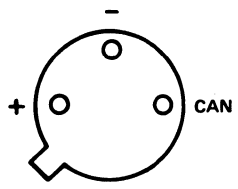
ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590*

FEATURES
Linear Current Output: 1μA/K
Wide Range: -55°C to +150°C
Probe Compatible Ceramic Sensor Package
Two-Terminal Device: Voltage In/Current Out
Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
Excellent Linearity: ±0.3°C Over Full Range (AD590M)
Wide Power Supply Range: +4V to +30V
Sensor Isolation from Case
Low Cost

AD590 PIN DESIGNATIONS



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

***Covered by Patent No. 4,123,698.**

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.

SPECIFICATIONS (@ +25°C and V_S = 5V unless otherwise noted)

Model	AD590J			AD590K			
	Min	Typ	Max	Min	Typ	Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			**±5.0**			**±2.5**	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			**±10**			**±5.5**	°C
With +25°C Calibration Error Set to Zero			**±3.0**			**±2.0**	°C
Nonlinearity			**±1.5**			**±0.8**	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA/$\sqrt{\text{Hz}}$
Power Supply Rejection							
$+4V \leq V_S \leq +5V$		0.5			0.5		μA/V
$+5V \leq V_S \leq +15V$		0.2			0.2		μA/V
$+15V \leq V_S \leq +30V$		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTIONS[5]							
TO-52 (H-03A)		AD590JH			AD590KH		
Flat Pack (F-2A)		AD590JF			AD590KF		

NOTES

[1]The AD590 has been used at −100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2]Maximum deviation between +25°C readings after temperature cycling between −55°C and +150°C; guaranteed not tested.

[3]Conditions: constant +5V, constant +125°C; guaranteed, not tested.

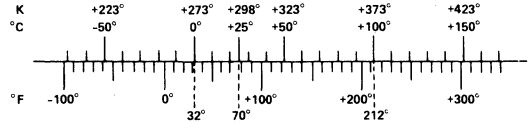
[4]Leakage current doubles every 10°C.

[5]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Model	AD590L Min	AD590L Typ	AD590L Max	AD590M Min	AD590M Typ	AD590M Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			**±1.0**			**±0.5**	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			**±3.0**			**±1.7**	°C
With +25°C Calibration Error Set to Zero			**±1.6**			**±1.0**	°C
Nonlinearity			**±0.4**			**±0.3**	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA$\sqrt{\text{Hz}}$
Power Supply Rejection							
$+4V \leq V_S \leq +5V$		0.5			0.5		μA/V
$+5V \leq V_S \leq +15V$		0.2			0.2		μA/V
$+15V \leq V_S \leq +30V$		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTION[5]							
TO-52 (H-03A)		AD590LH			AD590MH		
Flat Pack (F-2A)		AD590LF			AD590MF		



TEMPERATURE SCALE CONVERSION EQUATIONS

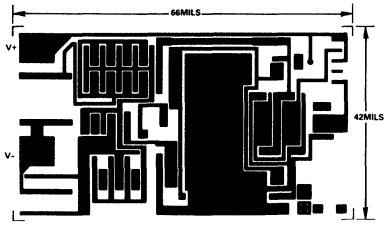
$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

The 590H has 60μ inches of gold plating on its Kovar leads and Kovar header. A resistance welder is used to seal the nickel cap to the header. The AD590 chip is eutectically mounted to the header and ultrasonically bonded to with 1 MIL aluminum wire. Kovar composition: 53% iron nominal; 29% ±1% nickel; 17% ±1% cobalt; 0.65% manganese max; 0.20% silicon max; 0.10% aluminum max; 0.10% magnesium max; 0.10% zirconium max; 0.10% titanium max; 0.06% carbon max.

The 590F is a ceramic package with gold plating on its Kovar leads, Kovar lid, and chip cavity. Solder of 80/20 Au/Sn composition is used for the 1.5 mil thick solder ring under the lid. The chip cavity has a nickel underlay between the metalization and the gold plating. The AD590 chip is eutectically mounted in the chip cavity at 410°C and ultrasonically bonded to with 1 mil aluminum wire. Note that the chip is in direct contact with the ceramic base, not the metal lid. When using the AD590 in die form, the chip substrate must be kept electrically isolated, (floating), for correct circuit operation.

METALIZATION DIAGRAM



CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(In r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly proportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

Figure 2 shows the typical V–I characteristic of the circuit at +25°C and the temperature extremes.

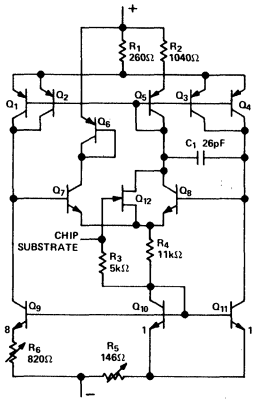


Figure 1. Schematic Diagram

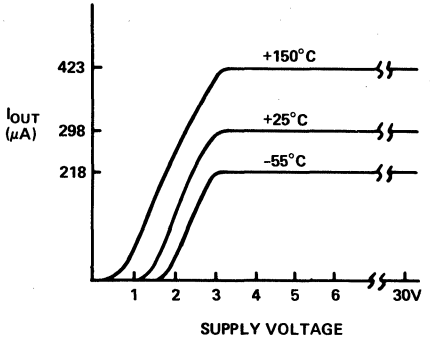


Figure 2. V–I Plot

[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at -55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

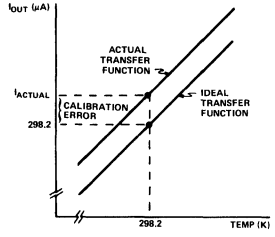


Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

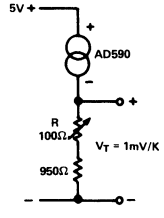


Figure 4. One Temperature Trim

[1] T(°C) = T(K) -273.2; Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

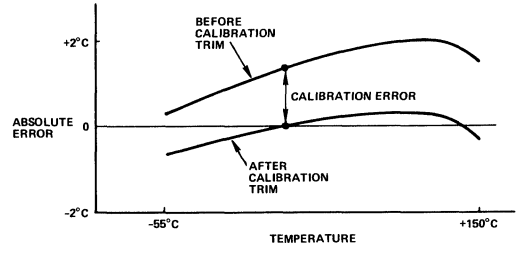


Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 2.33°C at -55°C to 3.02°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the -55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

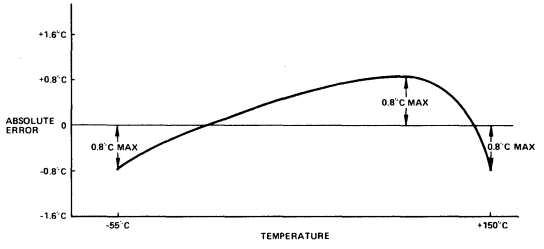


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V. Also note that V- should be at least -4V: if V- is ground there is no voltage applied across the device.

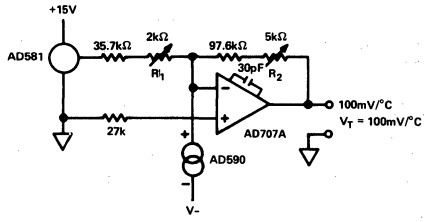


Figure 7A. Two Temperature Trim

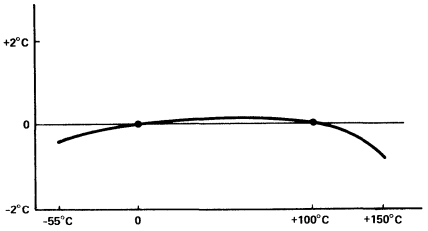


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

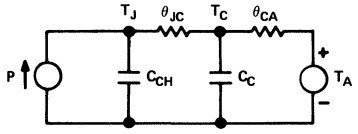


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package, θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table I gives the sum of θ_{JC} and θ_{CA} for several common thermal media for both the "H" and "F" packages. The heatsink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at +25°C, when driven with a 5V supply, will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

MEDIUM	$\theta_{JC} + \theta_{CA}$ (°C/watt)		τ (sec) (Note 3)	
	H	F	H	F
Aluminum Block	30	10	0.6	0.1
Stirred Oil[1]	42	60	1.4	0.6
Moving Air[2]				
With Heat Sink	45	—	5.0	—
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	—	108	—
Without Heat Sink	480	650	60	30

[1] Note: τ is dependent upon velocity of oil; average of several velocities listed above.
[2] Air velocity ≅ 9ft/sec.
[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table I. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T(t). Table I shows the effective time constant, τ, for several media.

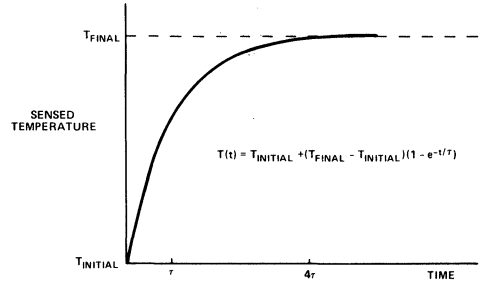


Figure 9. Time Response Curve

GENERAL APPLICATIONS

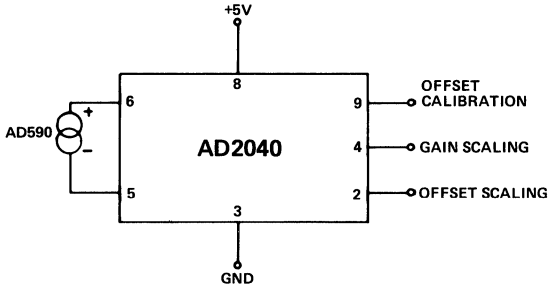


Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded; and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with 1°C or 1°F resolution, in addition to an absolute accuracy of ±2.0°C over the -55°C to +125°C temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

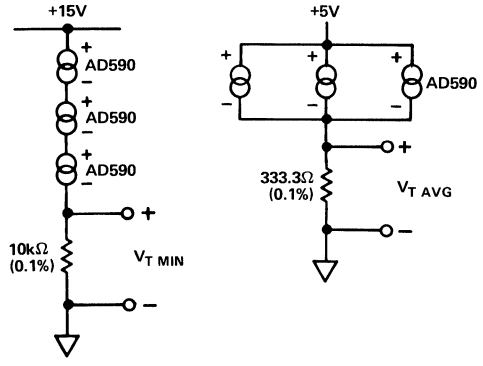


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate

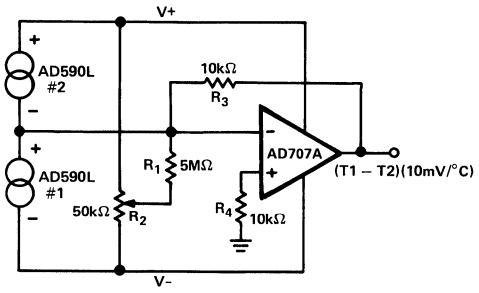


Figure 12. Differential Measurements

a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V- are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

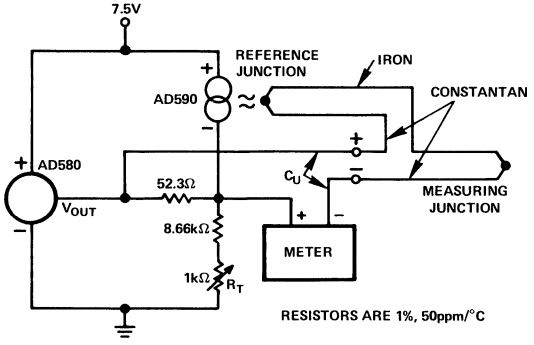


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

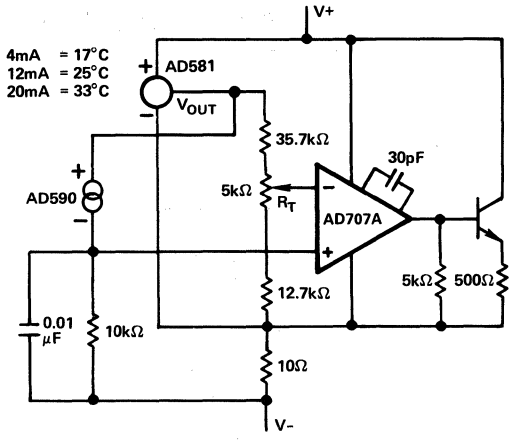


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1μA/K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

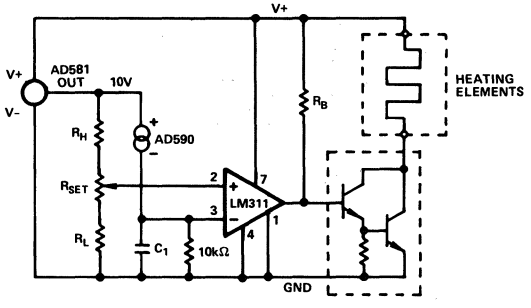


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8-bit DAC to produce a digitally controlled set point. This

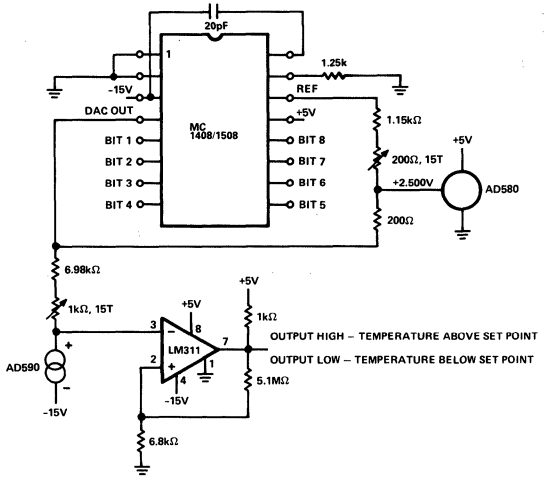


Figure 16. DAC Set Point

particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

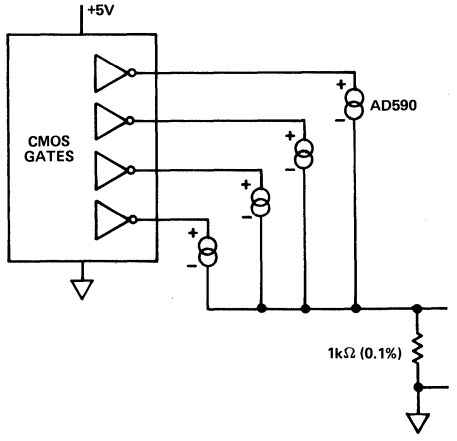


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

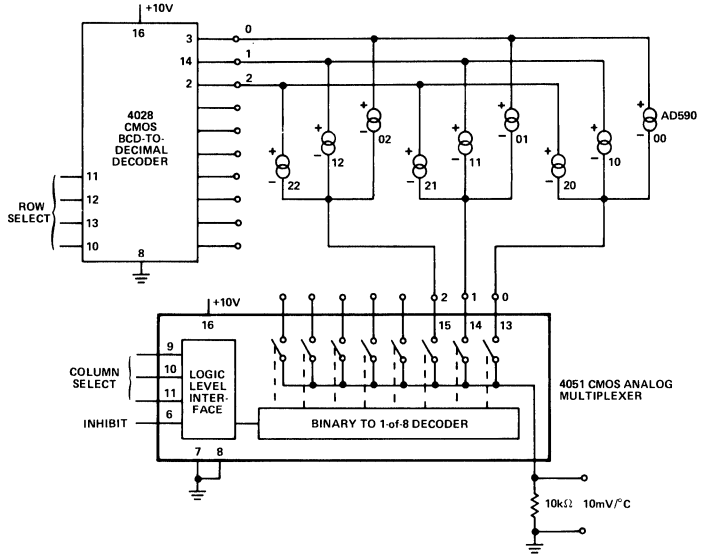


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

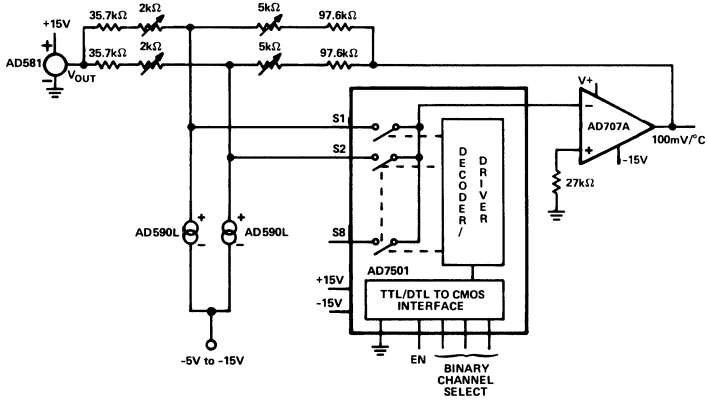


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of -55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.

ANALOG DEVICES

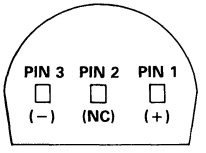
Low Cost, Precision IC Temperature Transducer

AD592*

FEATURES

High Precalibrated Accuracy: 0.5°C max @ 25°C
Excellent Linearity: 0.15°C max (0 to +70°C)
Wide Operating Temperature Range: −25°C to +105°C
Single Supply Operation: +4V to +30V
Excellent Repeatability and Stability
High Level Output: 1μA/K
Two Terminal Monolithic IC: Temperature In/ Current Out
Minimal Self-Heating Errors

AD592 CONNECTING DIAGRAM



*PIN 2 CAN BE EITHER ATTACHED OR UNCONNECTED

BOTTOM VIEW

PRODUCT DESCRIPTION

The AD592 is a two terminal monolithic integrated circuit temperature transducer that provides an output current proportional to absolute temperature. For a wide range of supply voltages the transducer acts as a high impedance temperature dependent current source of 1μA/K. Improved design and laser wafer trimming of the IC's thin film resistors allows the AD592 to achieve absolute accuracy levels and nonlinearity errors previously unattainable at a comparable price.

The AD592 can be employed in applications between −25°C and +105°C where conventional temperature sensors (i.e., thermistor, RTD, thermocouple, diode) are currently being used. The inherent low cost of a monolithic integrated circuit in a plastic package, combined with a low total parts count in any given application, make the AD592 the most cost effective temperature transducer currently available. Expensive linearization circuitry, precision voltage references, bridge components, resistance measuring circuitry and cold junction compensation are not required with the AD592.

Typical application areas include; appliance temperature sensing, automotive temperature measurement and control, HVAC (heating/ventilating/air conditioning) system monitoring, industrial temperature control, thermocouple cold junction compensation, board-level electronics temperature diagnostics, temperature readout options in instrumentation, and temperature correction circuitry for precision electronics. Particularly useful in remote sensing applications, the AD592 is immune to voltage drops and voltage noise over long lines due to its high impedance current output. AD592s can easily be multiplexed; the signal current can be switched by a CMOS multiplexer or the supply voltage can be enabled with a tri-state logic gate.

***Covered by Patent No. 4,123,698.**

The AD592 is available in three performance grades; the AD592AN, AD592BN and AD592CN. All devices are packaged in a plastic TO-92 case rated from −45°C to +125°C. Performance is specified from −25°C to +105°C. AD592 chips are also available, contact the factory for details.

PRODUCT HIGHLIGHTS

1. With a single supply (4V to 30V) the AD592 offers 0.5°C temperature measurement accuracy.
2. A wide operating temperature range (−25°C to +105°C) and highly linear output make the AD592 an ideal substitute for older, more limited sensor technologies (i.e., thermistors, RTDs, diodes, thermocouples).
3. The AD592 is electrically rugged; supply irregularities and variations or reverse voltages up to 20V will not damage the device.
4. Because the AD592 is a temperature dependent current source, it is immune to voltage noise pickup and IR drops in the signal leads when used remotely.
5. The high output impedance of the AD592 provides greater than 0.5°C/V rejection of supply voltage drift and ripple.
6. Laser wafer trimming and temperature testing insures that AD592 units are easily interchangeable.
7. Initial system accuracy will not degrade significantly over time. The AD592 has proven long term performance and repeatability advantages inherent in integrated circuit design and construction.

SPECIFICATIONS (typical @ 25°C, V_S = 5V, unless otherwise noted)

Model	AD592AN Min	AD592AN Typ	AD592AN Max	AD592BN Min	AD592BN Typ	AD592BN Max	AD592CN Min	AD592CN Typ	AD592CN Max	Units
ACCURACY										
Calibration Error @25°C[1]		1.5	2.5		0.7	1.0		0.3	0.5	°C
T_A = 0 to +70°C										
Error over Temperature		1.8	3.0		0.8	1.5		0.4	0.8	°C
Nonlinearity[2]		0.15	0.35		0.1	0.25		0.05	0.15	°C
T_A = −25 to +105°C										
Error over Temperature[3]		2.0	3.5		0.9	2.0		0.5	1.0	°C
Nonlinearity[2]		0.25	0.5		0.2	0.4		0.1	0.35	°C
OUTPUT CHARACTERISTICS										
Nominal Current Output @25°C (298.2K)		298.2			298.2			298.2		µA
Temperature Coefficient		1			1			1		µA/°C
Repeatability[4]			0.1			0.1			0.1	°C
Long Term Stability[5]			0.1			0.1			0.1	°C/month
ABSOLUTE MAXIMUM RATINGS										
Operating Temperature	−25		+105	−25		+105	−25		+105	°C
Package Temperature[6]	−45		+125	−45		+125	−45		+125	°C
Forward Voltage (+ to −)			44			44			44	V
Reverse Voltage (− to +)			20			20			20	V
Lead Temperature (Soldering 10 sec)			300			300			300	°C
POWER SUPPLY										
Operating Voltage Range	4		30	4		30	4		30	V
Power Supply Rejection										
+4V<V_S<+5V			0.5			0.5			0.5	°C/V
+5V<V_S<+15V			0.2			0.2			0.2	°C/V
+15V<V_S<+30V			0.1			0.1			0.1	°C/V

NOTES

[1]An external calibration trim can be used to zero the error @25°C.

[2]Defined as the maximum deviation from a mathematically best fit line.

[3]Parameter tested on all production units at +105°C only. C grade at −25°C also.

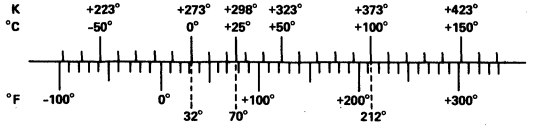
[4]Maximum deviation between +25°C readings after a temperature cycle between −45°C and +125°C. Errors of this type are noncummulative.

[5]Operation @125°C, error over time is noncummulative.

[6]Although performance is not specified beyond the operating temperature range, temperature excursions within the package temperature range will not damage the device.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

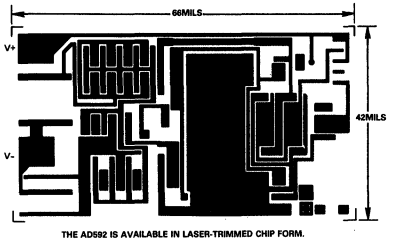


TEMPERATURE SCALE CONVERSION EQUATIONS

$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

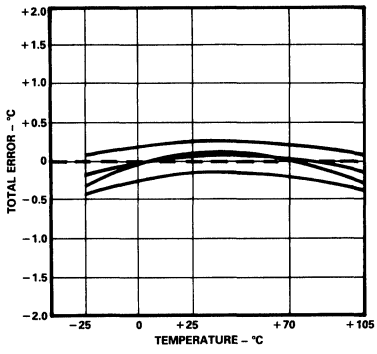
$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

METALIZATION DIAGRAM

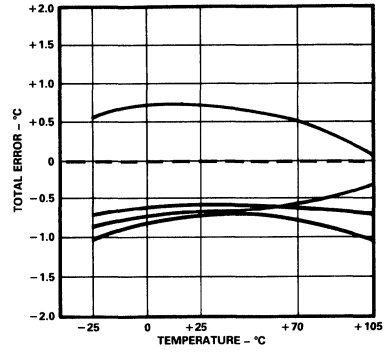


THE AD592 IS AVAILABLE IN LASER-TRIMMED CHIP FORM.

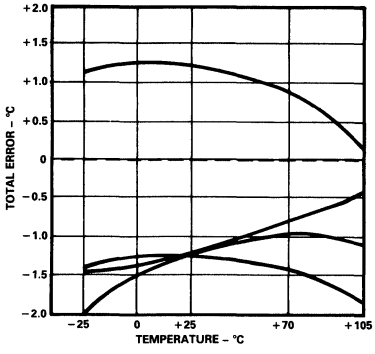
Typical @ V_S = +5V



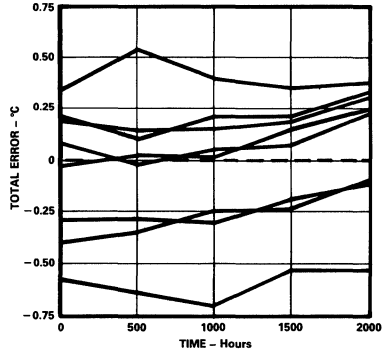
AD592CN Accuracy Over Temperature



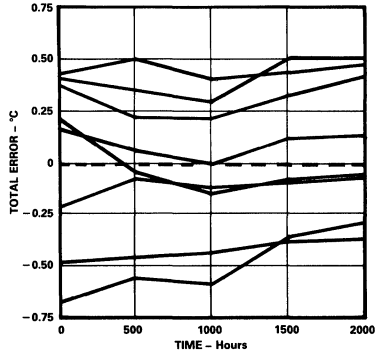
AD592BN Accuracy Over Temperature



AD592AN Accuracy Over Temperature



Long-Term Stability @ 85°C and 85% Relative Humidity



Long-Term Stability @ 125°C

AD592 ORDERING GUIDE

Model	Package Option[1]	Max Cal Error @ 25°C	Max Error −25°C to +105°C	Max Nonlinearity −25°C to +105°C
AD592CN	TO-92	0.5°C	1.0°C	0.35°C
AD592BN	TO-92	1.0°C	2.0°C	0.4°C
AD592AN	TO-92	2.5°C	3.5°C	0.5°C

NOTE
[1]See Section 20 for package outline information.

THEORY OF OPERATION

The AD592 uses a fundamental property of silicon transistors to realize its temperature proportional output. If two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in base-emitter voltages will be (kT/q)(ln r). Since both k, Boltzman's constant and q, the charge of an electron are constant, the resulting voltage is directly Proportional To Absolute Temperature (PTAT). In the AD592 this difference voltage is converted to a PTAT current by low temperature coefficient thin film resistors. This PTAT current is then used to force the total output current to be proportional to degrees Kelvin. The result is a current source with an output equal to a scale factor times the temperature (K) of the sensor. A typical V-I plot of the circuit at +25°C and the temperature extremes is shown in Figure 1.

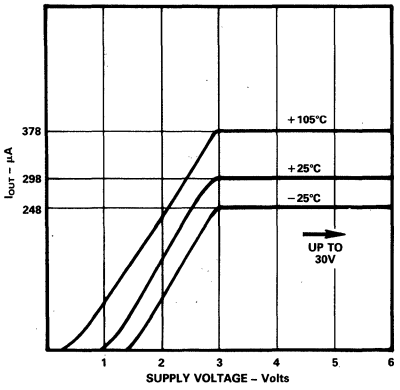


Figure 1. V–I Characteristics

Factory trimming of the scale factor to 1µA/K is accomplished at the wafer level by adjusting the AD592's temperature reading so it corresponds to the actual temperature. During laser trimming the IC is at a temperature within a few degrees of 25°C and is powered by a 5V supply. The device is then packaged and automatically temperature tested to specification.

FACTORS AFFECTING AD592 SYSTEM PRECISION

The accuracy limits given on the Specifications page for the AD592 makes it easy to apply in a variety of diverse applications. To calculate a total error budget in a given system it is important to correctly interpret the accuracy specifications, nonlinearity errors, the response of the circuit to supply voltage variations and the effect of the surrounding thermal environment. As with other electronic designs external component selection will have a major effect on accuracy.

CALIBRATION ERROR, ABSOLUTE ACCURACY AND NONLINEARITY SPECIFICATIONS

Three primary limits of error are given for the AD592 such that the correct grade for any given application can easily be chosen for the overall level of accuracy required. They are the calibration accuracy at 25°C, and the error over temperature from 0 to 70°C and −25°C to +105°C. These specifications correspond to the actual error the user would see if the current output of a AD592 were converted to a voltage with a precision resistor. Note that the maximum error at room temperature, over the commercial IC temperature range, or an extended range including the boiling point of water, can be directly read from the Specifications Table. All three error limits are a combination of initial error, scale factor variation and nonlinearity deviation from the ideal 1µA/K output. Figure 2 graphically depicts the guaranteed limits of accuracy for an AD592CN.

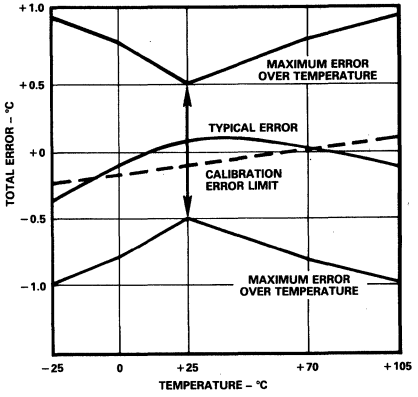


Figure 2. Error Specifications (AD592CN)

The AD592 has a highly linear output in comparison to older technology sensors (i.e., thermistors, RTDs and thermocouples), thus a nonlinearity error specification is separated from the absolute accuracy given over temperature. As a maximum deviation from a best-fit straight line this specification represents the only error which cannot be trimmed out. Figure 3 is a plot of typical AD592CN nonlinearity over the full rated temperature range.

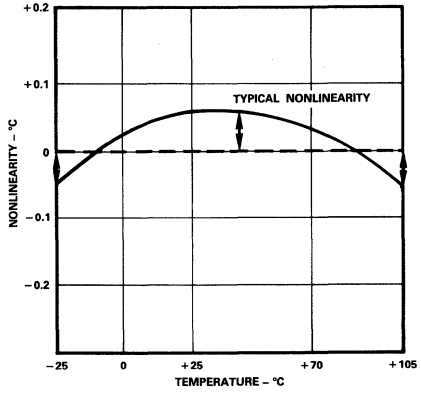


Figure 3. Nonlinearity Error (AD592CN)

TRIMMING FOR HIGHER ACCURACY

Calibration error at 25°C can be removed with a single temperature trim. Figure 4 shows how to adjust the AD592's scale factor in the basic voltage output circuit.

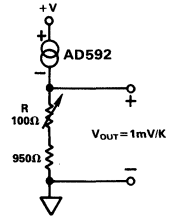


Figure 4. Basic Voltage Output (Single Temperature Trim)

To trim the circuit the temperature must be measured by a reference sensor and the value of R should be adjusted so the output (V_{OUT}) corresponds to 1mV/K. Note that the trim procedure should be implemented as close as possible to the temperature highest accuracy is desired for. In most applications if a single temperature trim is desired it can be implemented where the AD592 current-to-output voltage conversion takes place (e.g., output resistor, offset to an op amp). Figure 5 illustrates the effect on total error when using this technique.

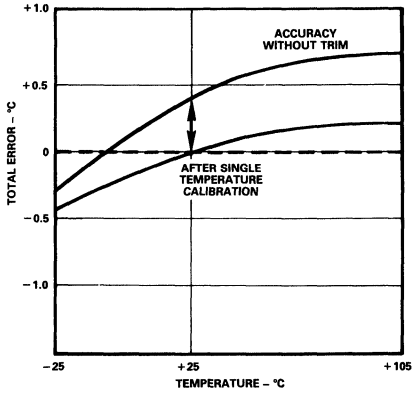


Figure 5. Effect of Scale Factor Trim on Accuracy

If greater accuracy is desired, initial calibration and scale factor errors can be removed by using the AD592 in the circuit of Figure 6.

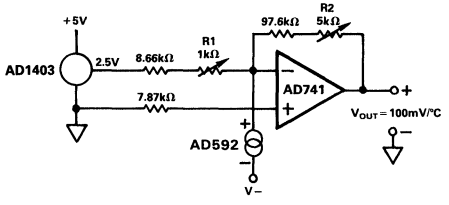


Figure 6. Two Temperature Trim Circuit

With the transducer at 0°C adjustment of R1 for a 0V output nulls the initial calibration error and shifts the output from K to °C. Tweaking the gain of the circuit at an elevated temperature by adjusting R2 trims out scale factor error. The only error remaining over the temperature range being trimmed for is nonlinearity. A typical plot of two trim accuracy is given in Figure 7.

SUPPLY VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection characteristics of the AD592 minimizes errors due to voltage irregularity, ripple and noise. If a supply is used other than 5V (used in factory trimming), the power supply error can be removed with a single temperature trim. The PTAT nature of the AD592 will remain unchanged. The general insensitivity of the output allows the use of lower cost unregulated supplies and means that a series resistance of several hundred ohms (e.g., CMOS multiplexer, meter coil resistance) will not degrade the overall performance.

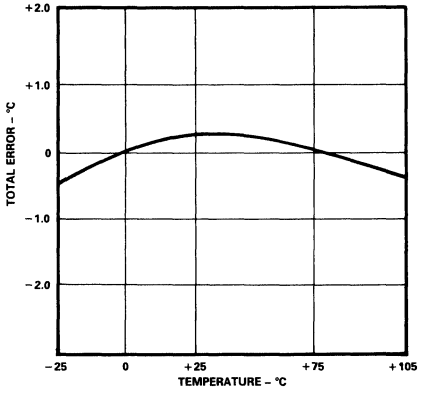


Figure 7. Typical Two Trim Accuracy

The thermal environment in which the AD592 is used determines two performance traits: the effect of self-heating on accuracy and the response time of the sensor to rapid changes in temperature. In the first case, a rise in the IC junction temperature above the ambient temperature is a function of two variables; the power consumption level of the circuit and the thermal resistance between the chip and the ambient environment (θ_{JA}). Self-heating error in °C can be derived by multiplying the power dissipation by θ_{JA}. Because errors of this type can vary widely for surroundings with different heat sinking capacities it is necessary to specify θ_{JA} under several conditions. Table I shows how the magnitude of self-heating error varies relative to the environment. In typical free air applications at 25°C with a 5V supply the magnitude of the error is 0.2°C or less. A common clip-on heat sink will reduce the error by 25% or more in critical high temperature, large supply voltage situations.

Medium	θ_{JA} (°C/watt)	τ (sec)*
Still Air		
Without Heat Sink	175	60
With Heat Sink	130	55
Moving Air		
Without Heat Sink	60	12
With Heat Sink	40	10
Fluorinert Liquid	35	5
Aluminum Block**	30	2.4

*τ is an average of five time constants (99.3% of final value). In cases where the thermal response is not a simple exponential function, the actual thermal response may be better than indicated.
**With thermal grease.

Table I. Thermal Characteristics

Response of the AD592 output to abrupt changes in ambient temperature can be modeled by a single time constant τ exponential function. Figure 8 shows typical response time plots for several media of interest.

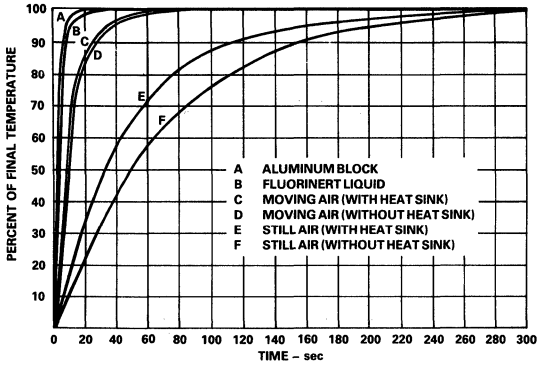


Figure 8. Thermal Response Curves

The time constant, τ, is dependent on θ_{JA} and the thermal capacities of the chip and the package. Table I lists the effective τ (time to reach 63.2% of the final value) for several different media. Copper printed circuit board connections where neglected in the analysis, however, they will sink or conduct heat directly through the AD592's solder dipped Kovar leads. When faster response is required a thermally conductive grease or glue between the AD592 and the surface temperature being measured should be used. In free air applications a clip-on heat sink will decrease output stabilization time by 10–20%.

MOUNTING CONSIDERATIONS

If the AD592 is thermally attached and properly protected, it can be used in any temperature measuring situation where the maximum range of temperatures encountered is between −25°C and +105°C. Because plastic IC packaging technology is employed, excessive mechanical stress must be safeguarded against when fastening the device with a clamp or screw-on heat tab. Thermally conductive epoxy or glue is recommended under typical mounting conditions. In wet or corrosive environments any electrically isolated metal or ceramic well can be used to shield the AD592. Condensation at cold temperatures can cause leakage current related errors and should be avoided by sealing the device in nonconductive epoxy paint or dips.

APPLICATIONS

Connecting several AD592 devices in parallel adds the currents through them and produces a reading proportional to the average temperature. Series AD592s will indicate the lowest temperature because the coldest device limits the series current flowing through the sensors. Both of these circuits are depicted in Figure 9.

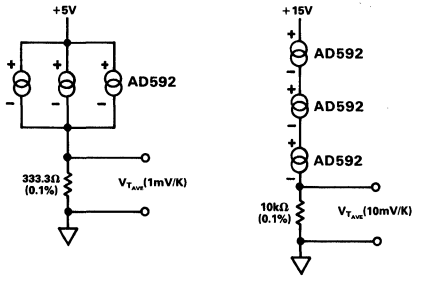


Figure 9. Average and Minimum Temperature Connections

The circuit of Figure 10 demonstrates a method in which a voltage output can be derived in a differential temperature measurement.

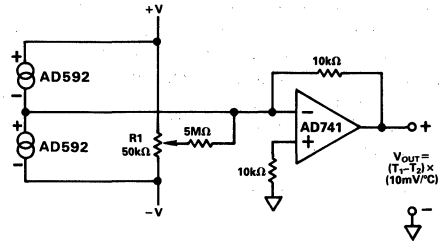


Figure 10. Differential Measurements

R1 can be used to trim out the inherent offset between the two devices. By increasing the gain resistor (10kΩ) temperature measurements can be made with higher resolution. If the magnitude of V+ and V− is not the same, the difference in power consumption between the two devices can cause a differential self-heating error.

Cold junction compensation (CJC) used in thermocouple signal conditioning can be implemented using an AD592 in the circuit configuration of Figure 11. Expensive simulated ice baths or hard to trim, inaccurate bridge circuits are no longer required.

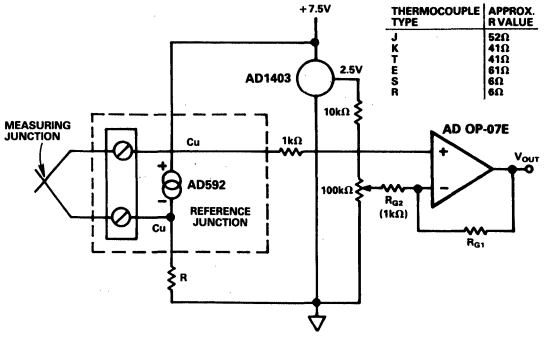


Figure 11. Thermocouple Cold Junction Compensation

The circuit shown can be optimized for any ambient temperature range or thermocouple type by simply selecting the correct value for the scaling resistor – R. The AD592 output (1μA/K) times R should approximate the line best fit to the thermocouple curve (slope in V/°C) over the most likely ambient temperature range. Additionally, the output sensitivity can be chosen by selecting the resistors R_{G1} and R_{G2} for the desired noninverting gain. The offset adjustment shown simply references the AD592 to °C. Note that the TC's of the reference and the resistors are the primary contributors to error. Temperature rejection of 40 to 1 can be easily achieved using the above technique.

Although the AD592 offers a noise immune current output, it is not compatible with process control/industrial automation current loop standards. Figure 12 is an example of a temperature to 4-20mA transmitter for use with 40V, 1kΩ systems.

In this circuit the 1μA/K output of the AD592 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. Rt is trimmed for proper reading at an

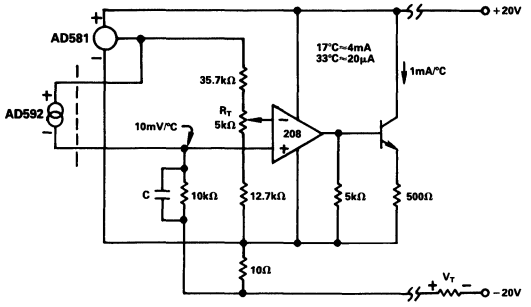


Figure 12. Temperature to 4–20mA Current Transmitter

intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD592 may be chosen.

Reading temperature with an AD592 in a microprocessor based system can be implemented with the circuit shown in Figure 13.

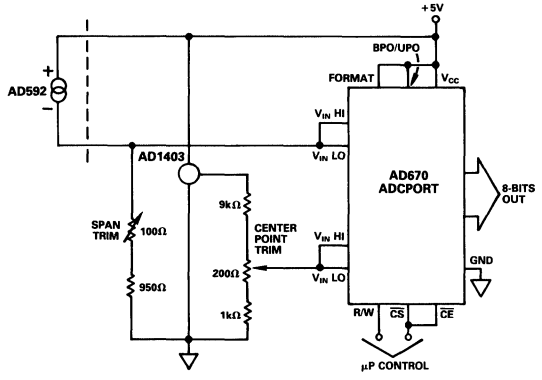


Figure 13. Temperature to Digital Output

By using a differential input A/D converter and choosing the current to voltage conversion resistor correctly any range of temperatures (up to the 130°C span the AD592 is rated for) centered at any point can be measured using a minimal number of components. In this configuration the system will resolve up to 1°C.

A variable temperature controlling thermostat can easily be built using the AD592 in the circuit of Figure 14.

R_{HIGH} and R_{LOW} determine the limits of temperature controlled by the potentiometer R_{SET}. The circuit shown operates over the full temperature range (−25°C to +105°C) the AD592 is rated for. The reference maintains a constant set point voltage and insures that approximately 7V appears across the sensor. If it is necessary to guardband for extraneous noise hysteresis can be added by tying a resistor from the output to the ungrounded end of R_{LOW}.

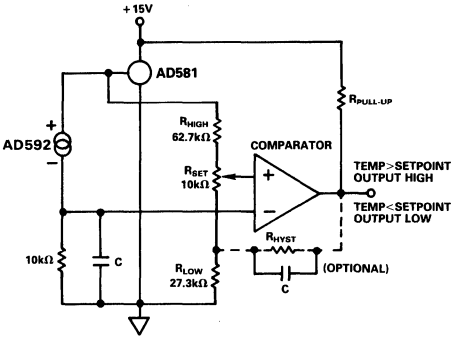


Figure 14. Variable Temperature Thermostat

Multiple remote temperatures can be measured using several AD592s with a CMOS multiplexer or a series of 5V logic gates because of the device's current-mode output and supply-voltage compliance range. The on-resistance of a FET switch or output impedance of a gate will not effect the accuracy, as long as 4V is maintained across the transducer. MUXs and logic driving circuits should be chosen to minimize leakage current related errors. Figure 15 illustrates a locally controlled MUX switching the signal current from several remote AD592s. CMOS or TTL gates can also be used to switch the AD592 supply voltages, with the multiplexed signal being transmitted over a single twisted pair to the load.

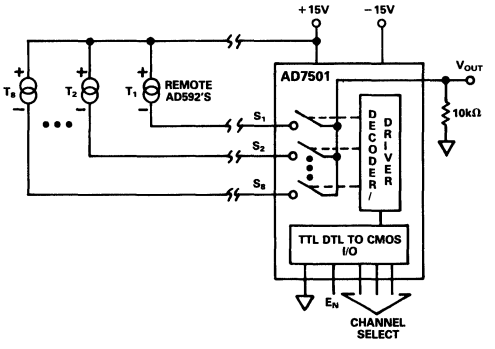


Figure 15. Remote Temperature Multiplexing

To minimize the number of MUXs required when a large number of AD592s are being used, the circuit can be configured in a matrix. That is, a decoder can be used to switch the supply voltage to a column of AD592s while a MUX is used to control which row of sensors are being measured. The maximum number of AD592s which can be used is the product of the number of channels of the decoder and MUX.

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An example circuit controlling 80 AD592s is shown in Figure 16. A 7-bit digital word is all that is required to select one of the sensors. The enable input of the multiplexer turns all the sensors off for minimum dissipation while idling.

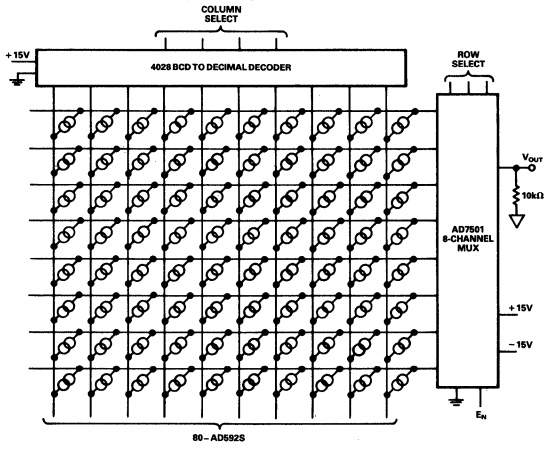

Figure 16. Matrix Multiplexer

To convert the AD592 output to °C or °F a single inexpensive reference and op amp can be used as shown in Figure 17. Although this circuit is similar to the two temperature trim circuit shown in Figure 6, two important differences exist. First, the gain resistor is fixed alleviating the need for an elevated temperature trim. Acceptable accuracy can be achieved by choosing an inexpensive resistor with the correct tolerance. Second, the AD592 calibration error can be trimmed out at a known convenient temperature (i.e., room temperature) with a single pot adjustment. This step is independent of the gain selection.

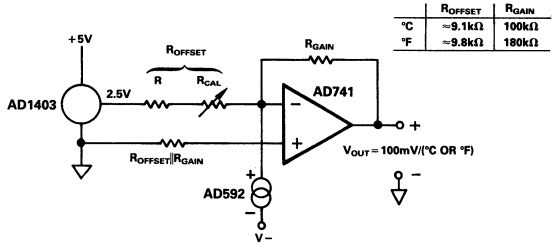

Figure 17. Celsius or Fahrenheit Thermometer

Signal Conditioning Components & Subsystems
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Selection Guide
Signal Conditioning Components & Subsystems

Model	V/I Transmitters: Loop Power	V/I Transmitters: Local Power	Isolated	Sensor Excitation	Sensor Type(s)	IC	Hybrid Package	Hybrid Module	Page
AD594/AD595					**TC**	**X**			**13–9**
AD596/AD597					**TC**	**X**			**13–17**
AD598		X		X	**LVDT**	**X**			**13–23**
AD693	**X**	**X**		**X**	**mV: All**	X			**13–39**
AD694		**X**		**X**	**0–2 or 10 V Input Range**	X			**13–51**
1B21	**X**		**X**					**X**	**13–63**
1B22		**X**	**X**					**X**	**13–67**
1B31				**X**	**Strain Gage**		X		**13–71**
1B32				**X**	**Strain Gage**		**X**		**13–79**
1B41			**X**	**X**	**RTD**			**X**	**13–87**
1B51			**X**		**TC, mV**			**X**	**13–91**
AC1226			**Thermocouple Cold Junction Compensator**					X	**13–5**
2B20		X						X	13–95
2B22		X	X					X	13–99
2B23		X	X					X	13–103
2B24	X		X					X	21–4
2B30					Strain Gage, RTD			X	13–107
2B31				X	Strain Gage, RTD			X	13–107
2B50			X		TC, mV			X	13–113
2B52	X		X		TC, mV			X	21–4
2B53	X				TC, mV			X	21–4
2B54/2B55			**X**		**mV, 4-Channel**			**X**	**13–117**
2B57	X			X	Solid State (AD590)			X	21–4
2B58				X	3-Wire RTD			X	21–4
2B59	X			X	2-Wire RTD			X	21–4
3B Series	**Modular Signal Conditioning Subsystem, Flexible, User Configurable**								**13–123**
4B Series	Alarm Limit Subsystem								21–4
5B Series	**Modular Signal Conditioning Subsystem; System Applications**								**13–127**
6B Series	**Software Configurable, Digitizing Signal Conditioning Subsystem**								**13–135**
7B Series	**Low Cost, Modular Process Control Signal Conditioners**								**13–143**

Boldface Type: Product recommended for new design.

Orientation
Signal Conditioning Components & Subsystems

Signal conditioners provide an analog interface between sensors and the systems they serve. They amplify signals, provide zero suppression where necessary, introduce electrical isolation, furnish excitation for passive transducers and provide analog outputs in the form required by the system – either voltage or current – at appropriate levels.

The most popular sensors are thermocouples, RTDs (resistance temperature detectors) and strain gages; they are low-level devices requiring precision amplification with low drift and noise. A useful discussion of their properties and signal-conditioning requirements can be found in the Analog Devices *Transducer Interfacing Handbook* (1980, $14.50 postpaid), available from P.O.Box 9106, Norwood MA 02062-9106.

Signal-conditioning circuits can be assembled using many of the precision products to be found in this databook, such as operational amplifiers, instrumentation amplifiers, and isolation amplifiers, along with other electronic circuit elements and appropriate hardware. However, many system designers have found that, with less expenditure of valuable engineering talent, excellent and reliable results can be achieved at lower cost by purchasing complete dedicated signal conditioners with fully specified performance in standard packages.

The general requirements for signal conditioners include the usual precision electrical characteristics, such as high gain, low drift and noise, accurate scale factors and fast – or filtered – response. Quite often, electrical isolation must be provided between the point of measurement and the system; besides maximizing common-mode rejection, this can provide protection of people and equipment. Where ruggedness and safety are involved, it may be useful to choose products, when available, that meet appropriate standards developed by such entities as CSA and Factory Mutual Research Company.

Many sensors require auxiliary circuitry; for example, thermocouples require a constant-temperature reference junction or an equivalent "ice-point" reference circuit, and strain gages and RTDs are passive devices that need excitation. Although the results of a measurement may be produced – and are ultimately needed – in the form of voltage, they may have to be transmitted as a varying current with a standard span, such as 4 to 20mA; often the power for such current loops is furnished to the sensor and its conditioner from the remote destination.

Another requirement arises from the fact that systems often involve many diverse channels of measurement. Such systems need a *family* of signal conditioners to meet the multiplicity of functional needs, yet it is desirable that they be compactly and ruggedly housed, modular, provided with a power supply and capable of being interchanged as system needs change. It is for such applications that the 3B, 5B, 6B and 7B families and their housings were designed.

The *selection guide* lists the available devices that are recommended for new system designs, along with their salient features; detailed information will be found in the data sheets. Examples of such devices include conditioners for thermocouples, RTDs, strain gages, and low (mV)-level signal sources and current transmitters that convert the signal information to 4-20mA or 0-20mA currents for loops requiring analog information in that form. If a modular subsystem is desired, selection information for choosing specific modules within the 3B, 5B, 6B and 7B families will be found in the family data sheets.

The individually listed devices are manufactured in various forms, ranging from monolithic integrated circuits (AD594/595/596/597 and AD693/AD694) to devices in dual in-line packages – using hybrid and surface-mount technologies – to modules with either pins for chassis wiring or screw terminals for field wiring.

The *3B Series* is an integrated modular signal-conditioning subsystem consisting of a series of color-coded functionally complete plug-in mix-and-match input and output modules on a universal backplane available for mounting in either rugged industrial chassis or a standard rack. The backplane connects directly to field wiring via screw terminals and to the system destination via connectors. A standard 19″ relay rack mount will hold 16 modules; 8- and 4-module units are also available. Among the characteristics of the modules are input protection, low-pass filtering, ±1μV/°C zero drift, and galvanic isolation to ±1,500 volts peak. The output modules translate high-level voltage inputs to standard process-current levels (0-20mA or 4-20mA) with accuracy to within 0.1%.

The *5B Series* of modules comprises a family of plug-in single-channel signal conditioners for sensors that perform complete signal conditioning functions optimized for the nature of each device's specified input. Characterized by high performance, small size and low price, they are ideal for monitoring such analog quantities as temperature, pressure and flow in industrial data-acquisition applications.

They are isolated (1,500 volts rms), operate from single 5-volt supplies and have ±0.05% calibration accuracy; they are identical in size (2.25″×2.25″×0.60″) and pinout. Physically compatible backplanes will hold as many as 16 units in a 19″ rack-mount space 3 1/2″ high. Signal-conditioning functions include input protection, filtering, chopper-stabilized low-drift amplification, isolation, linearization for RTD and thermocouple inputs and excitation for strain gages and RTDs.

5B Series modules have 240-volt protection for all field terminations. All feature excellent common-mode rejection, meet IEEE 472-1974 surge-withstand specs and operate over the −40°C to +85°C ambient temperature range. They are physically rugged, with sturdy 0.04′ pin connections and no adjustment potentiometers to compromise accuracy and system integrity; they are secured with a single self-contained mounting screw.

The *6B Series* of modules represents a new level of integration in modulator signal conditioners. Each module performs signal conditioning, isolation, ranging, 16-bit A/D conversion and digital communications (RS-485) for thermocouples, RTDs, millivolt, volt and process current signals. An on-board microcontroller autocalibrates the A/D converter and controls all channel parameters such as address, baud rate, sensor type, etc., which are stored in nonvolatile memory in the module.

The 6B Series modules are ideal for remote monitoring and data gathering applications in harsh environments. The module configurability also reduces inventory that is needed for an application interfacing with a variety of sensors.

The *7B Series* of Process Control Signal Conditioners is a family of isolation-based, plug-in, signal-channel signal conditioners that accept inputs from a wide range of process control sensors and low level signals while providing high level output signals. Characterized by high performance, compact size and low cost, these modules have been optimized for use in process control applications.

The 7B modules are isolated (1.5kV rms), operate from a single +24V dc supply and have a ±0.1%, max calibrated accuracy; they are identical in size (1.7″ × 2.11″ × 0.60″) and are footprint compatible with standard solid-state relays. Signal conditioning functions include input protection, filtering, isolation, linearization for RTD and thermocouple inputs, excitation for remote transmitters and an output current module. User-specified custom ranges, that are technically feasible, can be supplied.

The 7B modules have 240 volt protection (−25°C to +85°C) for all field wiring terminations. All modules feature high common-mode rejection and operate over the extended industrial temperature range of −40°C to +85°C. The modules are packaged in a rugged, compact plastic case, and they utilize sturdy 0.04″ pin connections. No external adjustment potentiometers are provided, thus minimizing the possibility of mechanical or human errors in the field that may adversely affect the system integrity. The 7B modules are secured with a single self-contained mounting screw.

ANALOG DEVICES

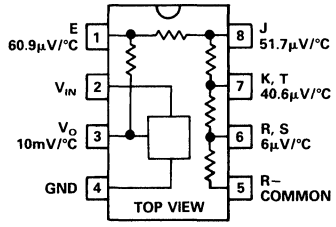
Micropower Thermocouple Cold Junction Compensator

AC1226

FEATURES
- 80μA Supply Current
- 4V to 36V Operation
- 0.5°C Typical Initial Accuracy
- Compatible with Standard Thermocouples (E, J, K, R, S, T)
- Auxiliary 10mV/°C Output
- Bow Corrected

APPLICATIONS
- Thermocouple Cold Junction Compensator
- Centigrade Thermometer
- Temperature Compensation Network

AC1226 PIN CONFIGURATION

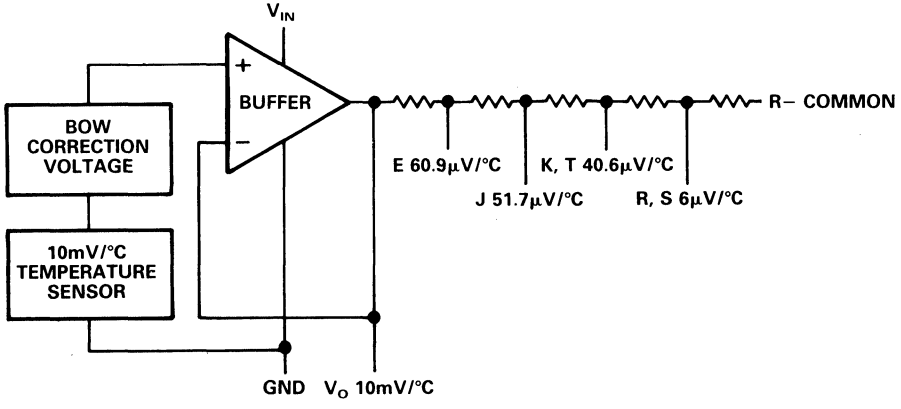


PRODUCT DESCRIPTION

The AC1226 is a micropower thermocouple cold junction compensator for use with type E, J, K, R, S and T thermocouples. It utilizes wafer level and post-package trimming to achieve typical 0.5°C initial accuracy. Special curvature correction circuitry is used to match the "bow" found in all thermocouples so that accurate cold junction compensation is maintained over a wider temperature range.

The AC1226 will operate with a supply voltage from 4V to 36V. Typical supply current is 80μA, resulting in less than 0.1°C internal temperature rise for supply voltages under 10V. A 10mV/°C output is available at low impedance in addition to the direct thermocouple voltages of 60.9μV/°C (E), 51.7μV/°C (J), 40.3μV/°C (K, T) and 5.95μV/°C (R, S). All outputs are essentially independent of power supply voltage.

The AC1226 is available in an 8-pin plastic mini-DIP for temperatures between 0 and +70°C.



AC1226 Block Diagram

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SPECIFICATIONS

Electrical Characteristics (V_S=5V, T_A=+25°C, Pin 5 tied to Pin 4, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Units
TEMPERATURE ERROR AT 10mV/°C OUTPUT[1,2]	T_J=+25°C Full Temperature Span*		0.5 See Curve	2.0	°C
RESISTOR DIVIDER ACCURACY[1,3]	V_{OUT}=10mV/°C				
	E	60.4	60.9	61.6	µV/°C
	J	51.2	51.7	52.3	
	K, T	40.2	40.6	41.2	
	R, S	5.75	5.95	6.3	
SUPPLY CURRENT	4V≤V_{IN}≤36V	50	80	100	µA
	*	50		150	
LINE REGULATION[4]	4V≤V_{IN}≤36V*		0.003	0.02	°C/V
LOAD REGULATION[4]	0≤I_O≤1mA*		0.04	0.2	°C
DIVIDER IMPEDANCE	E		2.5		kΩ
	J		2.1		
	K, T		4.4		
	R, S		3.8		
CHANGE IN SUPPLY CURRENT	4V≤V_{IN}≤36V		0.01	0.05	µA/V
PACKAGE OPTION[5] Plastic DIP (N-8)					

NOTES

[1]To calculate total temperature error at individual thermocouple outputs, add 10mV/°C output error to the resistor divider error. Total error for type K output at +25°C with an AC1226 is 2.0°C plus (0.6µV/°C) (25°C)/(40.6µV/°C=2.0°C+0.37°C=2.37°C.

[2]Temperature error is defined as the deviation from the following formula: V_{OUT}=10mV(T) + (10mV)(5.5×10^{-4})(T−25°C)^2. The second term is a built-in nonlinearity designed to help compensate the nonlinearity of the cold junction. This "bow" is ≈0.34°C for a 25°C temperature change.

[3]Divider accuracy is measured by applying a 10.000V signal to the output divider and measuring the individual outputs.

[4]Regulation does not include the effects of self-heating. See "Internal Temperature Rise" in Application Guide. Load regulation is 30µA≤I_O≤1mA for T_A≤0°C.

[5]See Section 20 for package outline information.

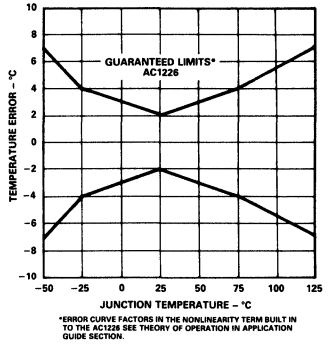
*Denotes the specifications which apply over the full operating temperature range.

Specifications subject to change without notice.

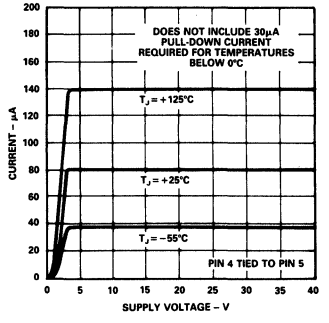
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage 36V
Output Voltage (Forced) 5V
Output Short Circuit Duration . . . . . .Indefinite
Operating Temperature Range . . . . . .0 to +70°C
Storage Temperature Range . . . . . .−55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . .+300°C

Typical Performance Characteristics



10mV/°C Output Temperature Error



Supply Current

APPLICATION GUIDE

The AC1226 was designed to be extremely easy to use, but the following ideas and suggestions should be helpful in obtaining the best possible performance and versatility from this new cold junction compensator.

THEORY OF OPERATION

A thermocouple consists of two dissimilar metals joined together. A voltage (Seebeck EMF) will be generated if the two ends of the thermocouple are at different temperatures. In Figure 1, iron and constantan are joined at the temperature measuring point T1. Two additional thermocouple junctions are formed where the iron and constantan connect to ordinary copper wire. For the purposes of this discussion it is assumed that these two junctions are at the same temperature, T2. The Seebeck voltage, V_S, is the product of the Seebeck coefficient α, and the temperature difference, T1–T2; $V_S = \alpha$ (T1–T2). The junctions at T2 are commonly called the cold junction because a common practice is to immerse the T2 junction in 0°C ice/water slurry to make T2 independent of room temperature variations. Thermocouple tables are based on a cold junction temperature of 0°C.

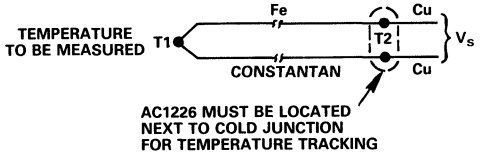


Figure 1.

For most applications an electronically simulated cold junction is required. The idea is basically to add a temperature dependent voltage to V_S such that the voltage sum is the same as if the T2 junction were at a constant 0°C instead of at room temperature. This voltage source is called a cold junction compensator. Its output is designed to be 0V at 0°C and have a slope equal to the Seebeck coefficient over the expected range of T2 temperatures.

To operate properly, a cold junction compensator must be at exactly the same temperature as the cold junction of the thermocouple (T2). *Therefore, it is important to locate the AC1226 physically close to the cold junction with local temperature gradients minimized.* If this is not possible, an extender made of matching thermocouple wire can be used. This shifts the cold junction from the user termination to the end of the extender so that the AC1226 can be located remotely from the user termination as shown in Figure 2.

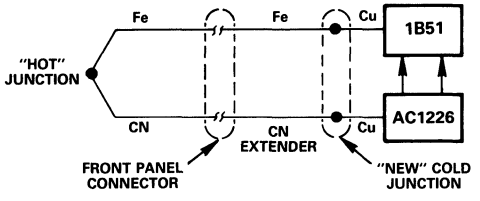


Figure 2.

The four thermocouple outputs on the AC1226 are 60.9μV/°C (E), 51.7μV/°C (J), 40.6μV/°C (K and T) and 6μV/°C (R and S). These particular coefficients are chosen to match the room temperature (+25°C) slope of the thermocouples. Over wide temperature ranges, however, the slope of thermocouples changes, yielding a quasi-parabolic error compared to a constant slope. The AC1226 outputs have a deliberate parabolic "bow" to help compensate for this effect. The outputs can be mathematically described as the sum of a linear term equal to room temperature slope plus a quadratic term proportional to temperature deviation from +25°C *squared*. The coefficient (β) of the quadratic term is a compromise value chosen to offer improvement in all the outputs.

$$V_{OUT} = \alpha T + \beta(T - 25°C)^2$$
$$\beta \approx 5.5 \times 10^{-4}$$

The actual β term which would be required to best compensate each thermocouple type in the temperature range of 0 to +50°C is: E, 6.6×10^{-4}; J, 4.8×10^{-4}; K, 4.3×10^{-4}; R, 1.9×10^{-3}; S, 1.9×10^{-3}; T, 1×10^{-3}.

The temperature error specification for the AC1226 (shown as a graph) assumes a β of 5.5×10^{-4}. For example, an AC1226 is considered "perfect" if its 10mV/°C output fits the equation $V_O = 10mV(T) + 5.5 \times 10^{-4}(T-25)^2$.

OPERATING AT NEGATIVE TEMPERATURES

The AC1226 is designed to operate with a single positive supply. It therefore cannot deliver proper outputs for temperatures below zero unless an external pull-down resistor is added to the V_O output. This resistor can be connected to any convenient negative supply. It should be selected to sink at least 30μA of current. Suggested value for a −5V supply is 150kΩ, and for a −15V supply, 470kΩ. Smaller resistors must be used if an external load is connected to the 10mV/°C output. The AC1226 can source up to 1mA of current, but there is a trade-off with internal temperature rise.

INTERNAL TEMPERATURE RISE

The AC1226 is specified for temperature accuracy assuming no internal temperature rise. At low supply voltages this rise is usually negligible (≈0.05°C @ 5V), but at higher supply voltages or with external loads or pull-down current, internal rise could become significant. This effect can be calculated from a simple thermal formula, $\Delta T = (\theta J_A)(V^+)(I_Q + I_L)$, where θJ_A is thermal resistance from junction to ambient (≈130°C/W), V^+ is the AC1226 supply voltage, I_Q, is the AC1226 supply current (≈80μA), and I_L is the total load current including actual load to ground and any pull-down current needed to generate negative outputs. A sample calculation with a 15V supply and 50μA pull-down current would yield, (130°C/W) (15V) (80+50μA) = 0.32°C. This is a significant rise in some applications. It can be reduced by lowering supply voltage (a simple fix is to insert a 10V Zener in the V_{IN} lead) or the system can be calibrated and specified after an initial warm-up period of several minutes.

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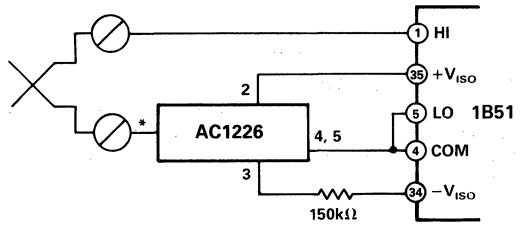
THERMOCOUPLE EFFECTS IN LEADS

Thermocouple voltages are generated whenever dissimilar materials are joined. *This includes the leads of IC packages,* which may be kovar in TO-5 cans, alloy 42 or copper in dual-in-line packages, and a variety of other materials in plating finishes and solders. The net effect of these thermocouples is "zero" if all are at exactly the same temperature, but temperature gradients exist within IC packages and across PC boards whenever power is dissipated. For this reason, extreme care must be used to ensure that no temperature gradients exist in the vicinity of thermocouple terminations, the AC1226, or the thermocouple amplifier. If a gradient cannot be eliminated, leads should be positioned isothermally, especially the AC1226 R^- and appropriate output pins, the amplifier input pins and the gain setting resistor leads. An effect to watch for is amplifier offset voltage warm-up drift caused by mismatched thermocouple materials in the wire bond/lead system of the package. This effect can be as high as tens of microvolts in TO-5 cans with kovar leads. It has nothing to do with the actual offset drift specification of the amplifier and can occur in amplifiers with measured "zero" drift. Warm-up drift is directly proportional to amplifier power dissipation. It can be minimized by avoiding TO-5 cans, using low supply current amplifiers and by using the lowest possible supply voltages. Finally, it can be accommodated by calibrating and specifying the system after a five minute warm-up period.

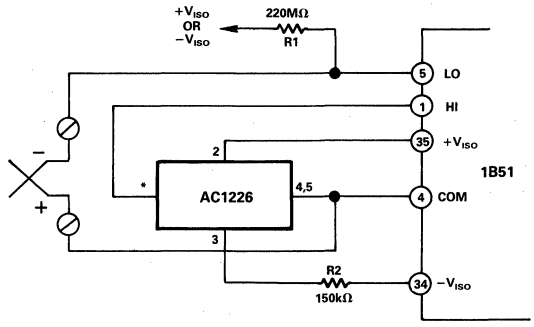
Figure 3 shows how to connect the AC1226 to the IB51 to compensate for the cold junction. This circuit is a conditioned and isolated channel for E, J, K, R, S or T thermocouples.

Figure 4 shows optional AC1226/1B51 connections with open input detection. This circuit minimizes input offset error generated by the pull up (or pull down) resistor, by eliminating the AC1226's divider impedance as seen by theresistor R1.



*PIN NUMBER DEPENDS ON THERMOCOUPLE TYPE.

Figure 3. Using the AC21226 with the 1B51, Isolated mV/Thermocouple Signal Conditioner



*PIN NUMBER DEPENDS ON THERMOCOUPLE TYPE.

Figure 4. Optional AC1226/1B51 Connections for Thermocouple Input with Open Detection Circuit

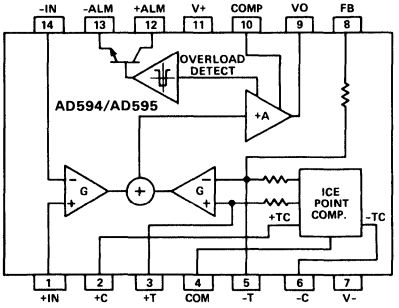
Monolithic Thermocouple Amplifiers with Cold Junction Compensation

AD594*/AD595*

FEATURES

- **Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples**
- **Can Be Used with Type T Thermocouple Inputs**
- **Low Impedance Voltage Output: 10mV/°C**
- **Built-in Ice Point Compensation**
- **Wide Power Supply Range: +5V to ±15V**
- **Low Power: <1mW typical**
- **Thermocouple Failure Alarm**
- **Laser Wafer Trimmed to 1°C Calibration Accuracy**
- **Set-Point Mode Operation**
- **Self-Contained Celsius Thermometer Operation**
- **High Impedance Differential Input**
- **Side-Brazed DIP or Low Cost Cerdip**

AD594/AD595 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD594/AD595 can be powered from a single ended supply (including +5V) and by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristic of type J (iron-constantan) thermocouples and the AD595 is laser trimmed for type K (chromel-alumel) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications.

***Protected by U.S. Patent No. 4,029,974.**

The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used from 0 to +50°C, and are available in 14-pin, hermetically sealed, side-brazed ceramic DIPs as well as low cost cerdip packages.

PRODUCT HIGHLIGHTS

1. The AD594/AD595 provides cold junction compensation, amplification, and an output buffer in a single IC package.
2. Compensation, zero, and scale factor are all precalibrated by laser wafer trimming (LWT) of each IC chip.
3. Flexible pin-out provides for operation as a set-point controller or a stand-alone temperature transducer calibrated in degrees Celsius.
4. Operation at remote application sites is facilitated by low quiescent current and a wide supply voltage range of +5V to dual supplies spanning 30V.
5. Differential input rejects common-mode noise voltage on the thermocouple leads.

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SPECIFICATIONS (@ +25°C and V_S = 5 V, Type J (AD594), Type K (AD595) Thermocouple, unless otherwise noted)

Model	AD594A			AD594C			AD595A			AD595C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS													
$+V_S$ to $-V_S$			36			36			36			36	Volts
Common-Mode Input Voltage	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages													
+ALM	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	−55		+125	−55		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT													
(Specified Temperature Range 0 to +50°C)													
Calibration Error at +25°C[1]			**±3**			**±1**			**±3**			**±1**	°C
Stability vs. Temperature[2]			**±0.05**			**±0.025**			**±0.05**			**±0.025**	°C/°C
Gain Error			**±1.5**			**±0.75**			**±1.5**			**±0.75**	%
Nominal Transfer Function			10			10			10			10	mV/°C
AMPLIFIER CHARACTERISTICS													
Closed Loop Gain[3]		**193.4**			**193.4**			**247.3**			**247.3**		
Input Offset Voltage	(Temperature in °C)×51.70 µV/°C			(Temperature in °C)×51.70 µV/°C			(Temperature in °C)×40.44 µV/°C			(Temperature in °C)×40.44 µV/°C			µV
Input Bias Current		0.1			0.1			0.1			0.1		µA
Differential Input Range	−10		+50				−10		+50	−10		+50	mV
Common-Mode Range	**$-V_S$ −0.15**		**$+V_S$ −4**	**$-V_S$ −0.15**		**$+V_S$ −4**	**$-V_S$ −0.15**		**$+V_S$ −4**	**$-V_S$ −0.15**		**$+V_S$ −4**	Volts
Common-Mode Sensitivity – RTO		**10**			**10**			**10**			**10**		mV/V
Power Supply Sensitivity – RTO		**10**			**10**			**10**			**10**		mV/V
Output Voltage Range													
Dual Supplies	**$-V_S$ +2.5**		**$+V_S$ −2**	**$-V_S$ +2.5**		**$+V_S$ −2**	**$-V_S$ +2.5**		**$+V_S$ −2**	**$-V_S$ +2.5**		**$+V_S$ −2**	Volts
Single Supply	0		$+V_S$ −2	0		$+V_S$ −2	0		$+V_S$ +2	0		$+V_S$ −2	Volts
Usable Output Current[4]		±5			±5			±5			±5		mA
3 dB Bandwidth		15			15			15			15		kHz
ALARM CHARACTERISTICS													
$V_{CE(SAT)}$ at 2 mA		0.3			0.3			0.3			0.3		Volts
Leakage Current			**±1**			**±1**			**±1**			**±1**	µA max
Operating Voltage at – ALM			**$+V_S$ −4**			**$+V_S$ −4**			**$+V_S$ −4**			**$+V_S$ −4**	Volts
Short Circuit Current		20			20			20			20		mA
POWER REQUIREMENTS													
Specified Performance	$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0			Volts
Operating[5]	$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30			Volts
Quiescent Current (No Load)													
$+V_S$		160	300		160	300		160	300		160	300	µA
$-V_S$		100			100			100			100		µA
PACKAGE OPTIONS[6]													
TO-116 (D-14)	AD594AD			AD594CD			AD595AD			AD595CD			
Cerdip (Q-14A)	AD594AQ			AD594CQ			AD595AQ			AD595CQ			

Notes
[1]Calibrated for minimum error at +25°C using a thermocouple sensitivity of 51.7 µV/°C. Since a J type thermocouple deviates from this straight line approximation, the AD594 will normally read 3.1 mV when the measuring junction is at 0°C. The AD595 will similarly read 2.7 mV at 0°C.
[2]Defined as the slope of the line connecting the AD594/AD595 errors measured at 0°C and 50°C ambient temperature.
[3]Pin 8 shorted to Pin 9.
[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50 kΩ resistor at output voltages below 2.5 V.
[5]$-V_S$ must not exceed −16.5 V.
[6]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Thermocouple Temperature °C	Type J Voltage mV	AD594 Output mV	Type K Voltage mV	AD595 Output mV
− 200	− 7.890	−1523	− 5.891	−1454
− 180	− 7.402	−1428	− 5.550	−1370
− 160	− 6.821	−1316	− 5.141	−1269
− 140	− 6.159	−1188	− 4.669	−1152
− 120	− 5.426	−1046	− 4.138	−1021
− 100	− 4.632	− 893	− 3.553	− 876
− 80	− 3.785	− 729	− 2.920	− 719
− 60	− 2.892	− 556	− 2.243	− 552
− 40	− 1.960	− 376	− 1.527	− 375
− 20	− .995	− 189	− .777	− 189
− 10	− .501	− 94	− .392	− 94
0	0	3.1	0	2.7
10	.507	101	.397	101
20	1.019	200	.798	200
25	1.277	250	1.000	250
30	1.536	300	1.203	300
40	2.058	401	1.611	401
50	2.585	503	2.022	503
60	3.115	606	2.436	605
80	4.186	813	3.266	810
100	5.268	1022	4.095	1015
120	6.359	1233	4.919	1219
140	7.457	1445	5.733	1420
160	8.560	1659	6.539	1620
180	9.667	1873	7.338	1817
200	10.777	2087	8.137	2015
220	11.887	2302	8.938	2213
240	12.998	2517	9.745	2413
260	14.108	2732	10.560	2614
280	15.217	2946	11.381	2817
300	16.325	3160	12.207	3022
320	17.432	3374	13.039	3327
340	18.537	3588	13.874	3434
360	19.640	3801	14.712	3641
380	20.743	4015	15.552	3849
400	21.846	4228	16.395	4057
420	22.949	4441	17.241	4266
440	24.054	4655	18.088	4476
460	25.161	4869	18.938	4686
480	26.272	5084	19.788	4896
500	27.388	5300	20.640	5107
520	28.511	5517	21.493	5318
540	29.642	5736	22.346	5529
560	30.782	5956	23.198	5740
580	31.933	6179	24.050	5950
600	33.096	6404	24.902	6161
620	34.273	6632	25.751	6371
640	35.464	6862	26.599	6581
660	36.671	7095	27.445	6790
680	37.893	7332	28.288	6998
700	39.130	7571	28.128	7206
720	40.382	7813	29.965	7413
740	41.647	8058	30.799	7619
750	42.283	8181	31.214	7722
760	–	–	31.629	7825
780	–	–	32.455	8029
800	–	–	33.277	8232
820	–	–	34.095	8434
840	–	–	34.909	8636
860	–	–	35.718	8836
880	–	–	36.524	9035
900	–	–	37.325	9233
920	–	–	38.122	9430
940	–	–	38.915	9626
960	–	–	39.703	9821
980	–	–	40.488	10015
1000	–	–	41.269	10209
1020	–	–	42.045	10400
1040	–	–	42.817	10591
1060	–	–	43.585	10781
1080	–	–	44.349	10970
1100	–	–	45.108	11158
1120	–	–	45.863	11345
1140	–	–	46.612	11530
1160	–	–	47.356	11714
1180	–	–	48.095	11897
1200	–	–	48.828	12078
1220	–	–	49.555	12258
1240	–	–	50.276	12436
1250	–	–	50.633	12524

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +25°C, V_S = −5V, +15V)

INTERPRETING AD594/AD595 OUTPUT VOLTAGES

To achieve a temperature proportional output of 10mV/°C and accurately compensate for the reference junction over the rated operating range of the circuit, the AD594/AD595 is gain trimmed to match the transfer characteristic of J and K type thermocouples at 25°C. For a type J output in this temperature range the TC is 51.70μV/°C, while for a type K it is 40.44μV/°C. The resulting gain for the AD594 is 193.4 (10mV/°C divided by 51.7μV/°C) and for the AD595 is 247.3 (10mV/°C divided by 40.44μV/°C). In addition, an absolute accuracy trim induces an input offset to the output amplifier characteristic of 16μV for the AD594 and 11μV for the AD595. This offset arises because the AD594/AD595 is trimmed for a 250mV output while applying a 25°C thermocouple input.

Because a thermocouple output voltage is nonlinear with respect to temperature, and the AD594/AD595 linearly amplifies the compensated signal, the following transfer functions should be used to determine the actual output voltages:

AD594 output = (Type J Voltage + 16μV) × 193.4

AD595 output = (Type K Voltage + 11μV) × 247.3

or conversely:

Type J voltage = (AD594 output / 193.4) − 16μV

Type K voltage = (AD595 output / 247.3) − 11μV

Table I above lists the ideal AD594/AD595 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples, with the package and reference junction at 25°C. As is normally the case, these outputs are subject to calibration, gain and temperature sensitivity errors. Output values for intermediate temperatures can be interpolated, or calculated using the output equations and ANSI thermocouple voltage tables referred to zero degrees Celsius. Due to a slight variation in alloy content between ANSI type J and DIN FE–CUNI thermocouples Table I should not be used in conjunction with European standard thermocouples. Instead the transfer function given previously and a DIN thermocouple table should be used. ANSI type K and DIN NICR–NI thermocouples are composed of identical alloys and exhibit similar behavior. The upper temperature limits in Table I are those recommended for type J and type K thermocouples by the majority of vendors.

SINGLE AND DUAL SUPPLY CONNECTIONS

The AD594/AD595 is a completely self-contained thermocouple conditioner. Using a single +5V supply the interconnections shown in Figure 1 will provide a direct output from a type J thermocouple (AD594) or type K thermocouple (AD595) measuring from 0 to +300°C.

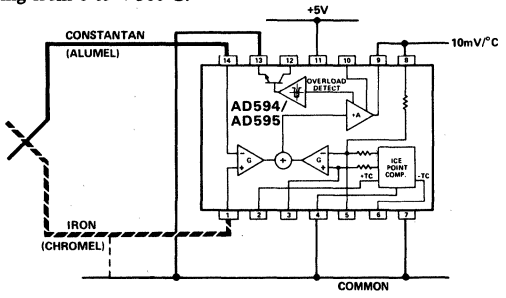


Figure 1. Basic Connection, Single Supply Operation

Any convenient supply voltage from +5V to +30V may be used, with self-heating errors being minimized at lower supply levels. In the single supply configuration the +5V supply connects to pin 11 with the V− connection at pin 7 strapped to power and signal common at pin 4. The thermocouple wire inputs connect to pins 1 and 14 either directly from the measuring point or through intervening connections of similar thermocouple wire type. When the alarm output at pin 13 is not used it should be connected to common or −V. The precalibrated feedback network at pin 8 is tied to the output at pin 9 to provide a 10mV/°C nominal temperature transfer characteristic.

By using a wider ranging dual supply, as shown in Figure 2, the AD594/AD595 can be interfaced to thermocouples measuring both negative and extended positive temperatures.

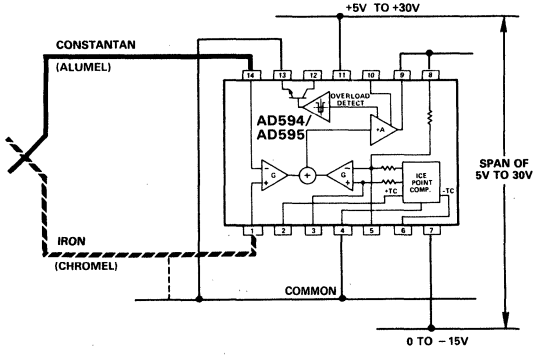


Figure 2. Dual Supply Operation

With a negative supply the output can indicate negative temperatures and drive grounded loads or loads returned to positive voltages. Increasing the positive supply from 5V to 15V extends the output voltage range well beyond the 750°C temperature limit recommended for type J thermocouples (AD594) and the 1250°C for type K thermocouples (AD595).

Common-mode voltages on the thermocouple inputs must remain within the common-mode range of the AD594/AD595, with a return path provided for the bias currents. If the thermocouple is not remotely grounded, then the dotted line connections in Figures 1 and 2 are recommended. A resistor may be needed in this connection to assure that common mode voltages induced in the thermocouple loop are not converted to normal mode.

THERMOCOUPLE CONNECTIONS

The isothermal terminating connections of a pair of themocouple wires forms an effective reference junction. This junction must be kept at the same temperature as the AD594/AD595 for the internal cold junction compensation to be effective.

A method that provides for thermal equilibrium is the printed circuit board connection layout illustrated in Figure 3.

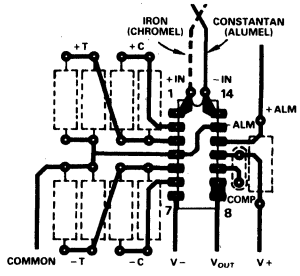


Figure 3. PCB Connections

Here the AD594/AD595 package temperature and circuit board are thermally contacted in the copper printed circuit board tracks under pins 1 and 14. The reference junction is now composed of a copper-constantan (or copper-alumel) connection and copper-iron (or copper-chromel) connection, both of which are at the same temperature as the AD594/AD595.

The printed circuit board layout shown also provides for placement of optional alarm load resistors, recalibration resistors and a compensation capacitor to limit bandwidth.

To ensure secure bonding the thermocouple wire should be cleaned to remove oxidation prior to soldering. Noncorrosive rosin flux is effective with iron, constantan, chromel and alumel and the following solders: 95% tin-5% antimony, 95% tin-5% silver or 90% tin-10% lead.

FUNCTIONAL DESCRIPTION

The AD594 behaves like two differential amplifiers. The outputs are summed and used to control a high-gain amplifier, as shown in Figure 4.

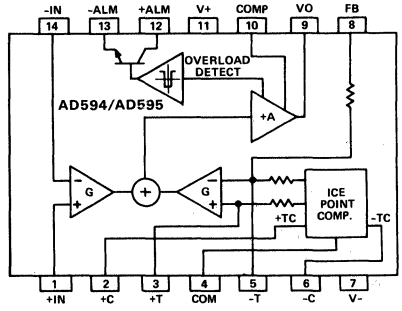


Figure 4. AD594/AD595 Block Diagram

In normal operation the main amplifier output, at pin 9, is connected to the feedback network, at pin 8. Thermocouple signals applied to the floating input stage, at pins 1 and 14, are amplified by gain G of the differential amplifier and are then further amplified by gain A in the main amplifier. The output of the main amplifier is fed back to a second differential stage in an inverting connection. The feedback signal is amplified by this stage and is also applied to the main amplifier input through a summing circuit. Because of the inversion, the amplifier causes

the feedback to be driven to reduce this difference signal to a small value. The two differential amplifiers are made to match and have identical gains, G. As a result, the feedback signal that must be applied to the right-hand differential amplifier will precisely match the thermocouple input signal when the difference signal has been reduced to zero. The feedback network is trimmed so that the effective gain to the output, at pins 8 and 9, results in a voltage of 10mV/°C of thermocouple excitation.

In addition to the feedback signal, a cold junction compensation voltage is applied to the right-hand differential amplifier. The compensation is a differential voltage proportional to the Celsius temperature of the AD594/AD595. This signal disturbs the differential input so that the amplifier output must adjust to restore the input to equal the applied thermocouple voltage.

The compensation is applied through the gain scaling resistors so that its effect on the main output is also 10mV/°C. As a result, the compensation voltage adds to the effect of the thermocouple voltage a signal directly proportional to the difference between 0°C and the AD594/AD595 temperature. If the thermocouple reference junction is maintained at the AD594/AD595 temperature, the output of the AD594/AD595 will correspond to the reading that would have been obtained from amplification of a signal from a thermocouple referenced to an ice bath.

The AD594/AD595 also includes an input open circuit detector that switches on an alarm transistor. This transistor is actually a current-limited output buffer, but can be used up to the limit as a switch transistor for either pull-up or pull-down operation of external alarms.

The ice point compensation network has voltages available with positive and negative temperature coefficients. These voltages may be used with external resistors to modify the ice point compensation and recalibrate the AD594/AD595 as described in the next column.

The feedback resistor is separately pinned out so that its value can be padded with a series resistor, or replaced with an external resistor between pins 5 and 9. External availability of the feedback resistor allows gain to be adjusted, and also permits the AD594/AD595 to operate in a switching mode for set-point operation.

CAUTIONS:

The temperature compensation terminals (+C and −C) at pins 2 and 6 are provided to supply small calibration currents only. The AD594/AD595 may be permanently damaged if they are grounded or connected to a low impedance.

The AD594/AD595 is internally frequency compensated for feedback ratios (corresponding to normal signal gain) of 75 or more. If a lower gain is desired, additional frequency compensation should be added in the form of a 300pF capacitor from pin 10 to the output at pin 9. As shown in Figure 5 an additional 0.01μF capacitor between pins 10 and 11 is recommended.

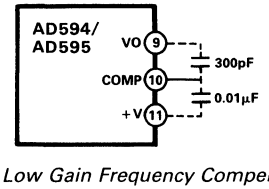


Figure 5. Low Gain Frequency Compensation

RECALIBRATION PRINCIPLES AND LIMITATIONS

The ice point compensation network of the AD594/AD595 produces a differential signal which is zero at 0°C and corresponds to the output of an ice referenced thermocouple at the temperature of the chip. The positive TC output of the circuit is proportional to Kelvin temperature and appears as a voltage at +T. It is possible to decrease this signal by loading it with a resistor from +T to COM, or increase it with a pull-up resistor from +T to the larger positive TC voltage at +C. Note that adjustments to +T should be made by measuring the voltage which tracks it at −T. To avoid destabilizing the feedback amplifier the measuring instrument should be isolated by a few thousand ohms in series with the lead connected to −T.

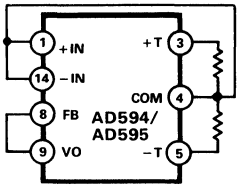


Figure 6. Decreased Sensitivity Adjustment

Changing the positive TC half of the differential output of the compensation scheme shifts the zero point away from 0°C. The zero can be restored by adjusting the current flow into the negative input of the feedback amplifier, the −T pin. A current into this terminal can be produced with a resistor between −C and −T to balance an increase in +T, or a resistor from −T to COM to offset a decrease in +T.

If the compensation is adjusted substantially to accommodate a different thermocouple type, its effect on the final output voltage will increase or decrease in proportion. To restore the nominal output to 10mV/°C the gain may be adjusted to match the new compensation and thermocouple input characteristics. When reducing the compensation the resistance between −T and COM automatically increases the gain to within 0.5% of the correct value. If a smaller gain is required, however, the nominal 47kΩ internal feedback resistor can be paralleled or replaced with an external resistor.

Fine calibration adjustments will require temperature response measurements of individual devices to assure accuracy. Major reconfigurations for other thermocouple types can be achieved without seriously compromising initial calibration accuracy, so long as the procedure is done at a fixed temperature using the factory calibration as a reference. It should be noted that intermediate recalibration conditions may require the use of a negative supply. An example using a type E thermocouple and an AD594 is given on the next page.

EXAMPLE: TYPE E RECALIBRATION – AD594/AD595

Both the AD594 and AD595 can be configured to condition the output of a type E (chromel-constantan) thermocouple. Temperature characteristics of type E thermocouples differ less from type J, than from type K, therefore the AD594 is preferred for recalibration.

While maintaining the device at a constant temperature follow the recalibration steps given here. First, measure the device temperature by tying both inputs to common (or a selected common mode potential) and connecting FB to V_O. The AD594 is now in the stand alone Celsius thermometer mode. For this example assume the ambient is 24°C and the initial output V_O is 240mV. Check the output at V_O to verify that it corresponds to the temperature of the device.

Next, measure the voltage $-T$ at pin 5 with a high impedance DVM (capacitance should be isolated by a few thousand ohms of resistance at the measured terminals). At 24°C the $-T$ voltage will be about 8.3mV. To adjust the compensation of an AD594 to a type E thermocouple a resistor, R1, should be connected between $+T$ and $+C$, pins 2 and 3, to raise the voltage at $-T$ by the ratio of thermocouple sensitivities. The ratio for converting a type J device to a type E characteristic is:

$$r\,(AD594) = (60.9\mu V/°C)/(51.7\mu V/°C) = 1.18$$

Thus, multiply the initial voltage measured at $-T$ by r and experimentally determine the R1 value required to raise $-T$ to that level. For the example the new $-T$ voltage should be about 9.8mV. The resistance value should be approximately 1.8kΩ.

The zero differential point must now be shifted back to 0°C. This is accomplished by multiplying the original output voltage V_O by r and adjusting the measured output voltage to this value by experimentally adding a resistor, R2, between $-C$ and $-T$, pins 5 and 6. The target output value in this case should be about 283mV. The resistance value of R2 should be approximately 240kΩ.

Finally, the gain must be recalibrated such that the output V_O indicates the device's temperature once again. Do this by adding a third resistor, R3, between FB and $-T$, pins 8 and 5. V_O should now be back to the initial 240mV reading. The resistance value of R3 should be approximately 280kΩ. The final connection diagram is shown in Figure 7. An approximate verification of the effectiveness of recalibration is to measure the differential gain to the output. For type E it should be 164.2.

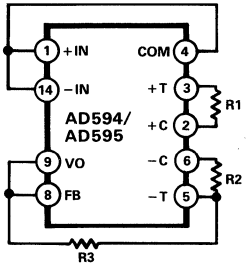


Figure 7. Type E Recalibration

When implementing a similar recalibration procedure for the AD595 the values for R1, R2, R3 and r will be approximately 650Ω, 84kΩ, 93kΩ and 1.51, respectively. Power consumption will increase by about 50% when using the AD595 with type E inputs.

Note that during this procedure it is crucial to maintain the AD594/AD595 at a stable temperature because it is used as the temperature reference. Contact with fingers or any tools not at ambient temperature will quickly produce errors. Radiational heating from a change in lighting or approach of a soldering iron must also be guarded against.

USING TYPE T THERMOCOUPLES WITH THE AD595

Because of the similarity of thermal EMFs in the 0 to 50°C range between type K and type T thermocouples, the AD595 can be directly used with both types of inputs. Within this ambient temperature range the AD595 should exhibit no more than an additional 0.2°C output calibration error when used with type T inputs. The error arises because the ice point compensator is trimmed to type K characteristics at 25°C. To calculate the AD595 output values over the recommended -200 to 350°C range for type T thermocouples, simply use the ANSI thermocouple voltages referred to 0°C and the output equation given on page 3 for the AD595. Because of the relatively large nonlinearities associated with type T thermocouples the output will deviate widely from the nominal 10mV/°C. However, cold junction compensation over the rated 0 to 50°C ambient will remain accurate.

STABILITY OVER TEMPERATURE

Each AD594/AD595 is tested for error over temperature with the measuring thermocouple at 0°C. The combined effects of cold junction compensation error, amplifier offset drift and gain error determine the stability of the AD594/AD595 output over the rated ambient temperature range. Figure 8 shows an AD594/AD595 drift error envelope. The slope of this figure has units of °C/°C.

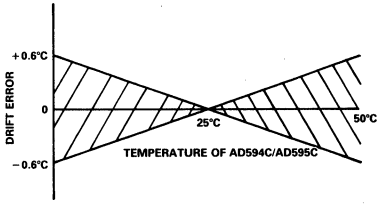


Figure 8. Drift Error vs. Temperature

THERMAL ENVIRONMENT EFFECTS

The inherent low power dissipation of the AD594/AD595 and the low thermal resistance of the package make self-heating errors almost negligible. For example, in still air the chip to ambient thermal resistance is about 80°C/watt (for the D package). At the nominal dissipation of 800μW the self-heating in free air is less than 0.065°C. Submerged in fluorinert liquid (unstirred) the thermal resistance is about 40°C/watt, resulting in a self-heating error of about 0.032°C.

SET-POINT CONTROLLER

The AD594/AD595 can readily be connected as a set-point controller as shown in Figure 9.

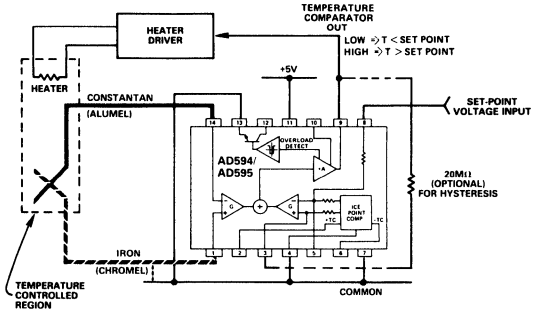


Figure 9. Set-Point Controller

The thermocouple is used to sense the unknown temperature and provide a thermal EMF to the input of the AD594/AD595. The signal is cold junction compensated, amplified to 10mV/°C and compared to an external set-point voltage applied by the user to the feedback at pin 8. Table I lists the correspondence between set-point voltage and temperature, accounting for the nonlinearity of the measurement thermocouple. If the set-point temperature range is within the operating range (−55°C to +125°C) of the AD594/AD595, the chip can be used as the transducer for the circuit by shorting the inputs together and utilizing the nominal calibration of 10mV/°C. This is the centigrade thermometer configuration as shown in Figure 13.

In operation if the set-point voltage is above the voltage corresponding to the temperature being measured the output swings low to approximately zero volts. Conversely, when the temperature rises above the set-point voltage the output switches to the positive limit of about 4 volts with a +5V supply. Figure 9 shows the set-point comparator configuration complete with a heater element driver circuit being controlled by the AD594/AD595 toggled output. Hysteresis can be introduced by injecting a current into the positive input of the feedback amplifier when the output is toggled high. With an AD594 about 200nA into the +T terminal provides 1°C of hysteresis. When using a single 5V supply with an AD594, a 20MΩ resistor from V_O to +T will supply the 200nA of current when the output is forced high (about 4V). To widen the hysteresis band decrease the resistance connected from V_O to +T.

ALARM CIRCUIT

In all applications of the AD594/AD595 the −ALM connection, pin 13, should be constrained so that it is not more positive than (V+) − 4V. This can be most easily achieved by connecting pin 13 to either common at pin 4 or V− at pin 7. For most applications that use the alarm signal, pin 13 will be grounded and the signal will be taken from +ALM on pin 12. A typical application is shown in Figure 10.

In this configuration the alarm transistor will be off in normal operation and the 20k pull up will cause the +ALM output on pin 12 to go high. If one or both of the thermocouple leads are interrupted, the +ALM pin will be driven low. As shown in Figure 10 this signal is compatible with the input of a TTL gate which can be used as a buffer and/or inverter.

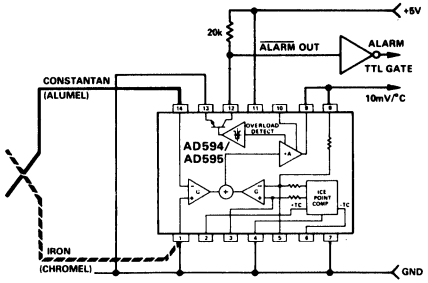


Figure 10. Using the Alarm to Drive a TTL Gate ("Grounded" Emitter Configuration)

Since the alarm is a high level output it may be used to directly drive an LED or other indicator as shown in Figure 11.

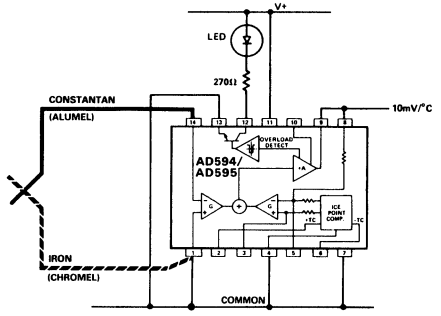


Figure 11. Alarm Directly Drives LED

A 270Ω series resistor will limit current in the LED to 10mA, but may be omitted since the alarm output transistor is current limited at about 20mA. The transistor, however, will operate in a high dissipation mode and the temperature of the circuit will rise well above ambient. Note that the cold junction compensation will be affected whenever the alarm circuit is activated. The time required for the chip to return to ambient temperature will depend on the power dissipation of the alarm circuit, the nature of the thermal path to the environment and the alarm duration.

The alarm can be used with both single and dual supplies. It can be operated above or below ground. The collector and emitter of the output transistor can be used in any normal switch configuration. As an example a negative referenced load can be driven from −ALM as shown in Figure 12.

The collector (+ALM) should not be allowed to become more positive than (V−) +36V, however, it may be permitted to be more positive than V+. The emitter voltage (−ALM) should be constrained so that it does not become more positive than 4 volts below the V+ applied to the circuit.

Additionally, the AD594/AD595 can be configured to produce an extreme upscale or downscale output in applications where an extra signal line for an alarm is inappropriate. By tying either of the thermocouple inputs to common most runaway control conditions can be automatically avoided. A +IN to common connection creates a downscale output if the thermocouple opens, while connecting −IN to common provides an upscale output.

13

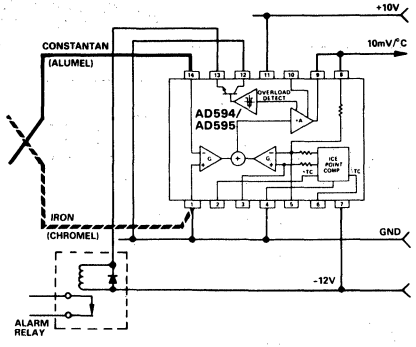


Figure 12. –ALM Driving A Negative Referenced Load

CELSIUS THERMOMETER

The AD594/AD595 may be configured as a stand-alone celsius thermometer as shown in Figure 13.

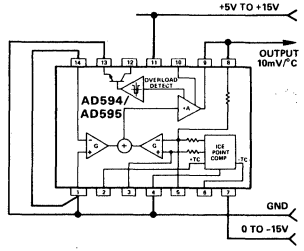


Figure 13. AD594/AD595 as a Stand-Alone Celsius Thermometer

Simply omit the thermocouple and connect the inputs (pins 1 and 14) to common. The output now will reflect the compensation voltage and hence will indicate the AD594/AD595 temperature with a scale factor of 10mV/°C. In this three terminal, voltage output, temperature sensing mode, the AD594/AD595 will operate over the full military −55°C to +125°C temperature range.

THERMOCOUPLE BASICS

Thermocouples are economical and rugged; they have reasonably good long-term stability. Because of their small size, they respond quickly and are good choices where fast response is important. They function over temperature ranges from cryogenics to jet-engine exhaust and have reasonable linearity and accuracy.

Because the number of free electrons in a piece of metal depends on both temperature and composition of the metal, two pieces of dissimilar metal in isothermal contact will exhibit a potential difference that is a repeatable function of temperature, as shown in Figure 14. The resulting voltage depends on the temperatures, T1 and T2, in a repeatable way.

Since the thermocouple is basically a differential rather than absolute measuring device, a known reference temperature is required for one of the junctions if the temperature of the other is to be inferred from the output voltage. Thermocouples made of specially selected materials have been exhaustively characterized in terms of voltage versus temperature compared to primary temperature standards. Most notably the water-ice point of 0°C is used for tables of standard thermocouple performance.

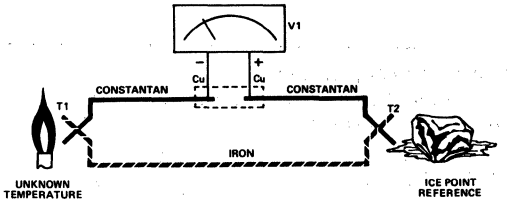


Figure 14. Thermocouple Voltage with 0°C Reference

An alternative measurement technique, illustrated in Figure 15, is used in most practical applications where accuracy requirements do not warrant maintenance of primary standards. The reference junction temperature is allowed to change with the environment

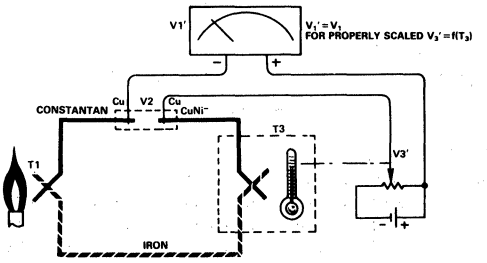


Figure 15. Substitution of Measured Reference Temperature for Ice Point Reference

of the measurement system, but it is carefully measured by some type of absolute thermometer. A measurement of the thermocouple voltage combined with a knowledge of the reference temperature can be used to calculate the measurement junction temperature. Usual practice, however, is to use a convenient thermoelectric method to measure the reference temperature and to arrange its output voltage so that it corresponds to a thermocouple referred to 0°C. This voltage is simply added to the thermocouple voltage and the sum then corresponds to the standard voltage tabulated for an ice-point referenced thermocouple.

The temperature sensitivity of silicon integrated circuit transistors is quite predictable and repeatable. This sensitivity is exploited in the AD594/AD595 to produce a temperature related voltage to compensate the reference or "cold" junction of a thermocouple as shown in Figure 16.

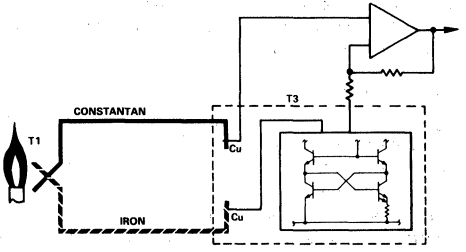


Figure 16. Connecting Isothermal Junctions

Since the compensation is at the reference junction temperature, it is often convenient to form the reference "junction" by connecting directly to the circuit wiring. So long as these connections and the compensation are at the same temperature no error will result.

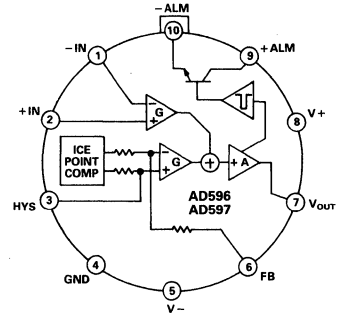
ANALOG DEVICES

Thermocouple Conditioners and Set-Point Controllers

AD596*/AD597*

FEATURES
Low Cost
Operates with Type J (AD596) or Type K (AD597) Thermocouples
Built-in Ice Point Compensation
Temperature Proportional Operation – 10mV/°C
Temperature Set-Point Operation – ON/OFF
Programmable Switching Hysteresis
High Impedance Differential Input

AD596/AD597 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD596/AD597 is a monolithic temperature set-point controller which has been optimized for use at elevated temperatures such as those found in oven control applications. The device cold junction compensates and amplifies a type J or K thermocouple input to derive an internal signal proportional to temperature. The internal signal is then compared with an externally applied set-point voltage to yield a low impedance switched output voltage. Dead-Band or switching hysteresis can be programmed using a single external resistor. Alternately, the AD596/AD597 can be configured to provide a voltage output (10mV/°C) directly from a type J or K thermocouple signal. It can also be used as a stand-alone voltage output temperature sensor.

The AD596/AD597 can be powered with a single supply from +5V to +30V, or dual supplies up to a total span of 36V. Typical quiescent supply current is 160μA which minimizes self-heating errors.

The AD596/AD597 includes a thermocouple failure alarm that indicates an open thermocouple lead when operated in the temperature proportional measurement mode. The alarm output has a flexible format which can be used to drive relays, LEDs or TTL logic.

The device is packaged in a reliability qualified, cost effective 10-pin metal can and is trimmed to operate over an ambient temperature range from +25°C to +100°C. Operation over an extended ambient temperature range is possible with slightly reduced accuracy. The AD596 will amplify thermocouple signals covering the entire −200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate −200°C to +1250°C type K inputs.

The AD596/AD597 has a calibration accuracy of ±4°C at an ambient temperature of 60°C and an ambient temperature stability specification of 0.05°C/°C from +25°C to +100°C. If higher accuracy, or a lower ambient operating temperature is required, either the AD594 (J thermocouple) or AD595 (K thermocouple) should be considered.

PRODUCT HIGHLIGHTS

1. The AD596/AD597 provides cold junction compensation and a high gain amplifier which can be used as a set-point comparator.
2. The input stage of the AD596/AD597 is a high quality instrumentation amplifier that allows the thermocouple to float over most of the supply voltage range.
3. Linearization not required for thermocouple temperatures close to 175°C (+100°C to +540°C for AD596).
4. Cold junction compensation is optimized for ambient temperatures ranging from +25°C to +100°C.
5. In the stand-alone mode, the AD596/AD597 produces an output voltage that indicates its own temperature.

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***Protected by U.S. Patent No. 4,029,974.**

SPECIFICATIONS (@ +60°C and V_S = 10V, Type J (AD596), Type K (AD597) Thermocouple, unless otherwise noted)

Model	AD596AH			AD597AH			Units
	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS							
$+V_S$ to $-V_S$			36			36	Volts
Common-Mode Input Voltage	$(-V_S-0.15)$		$+V_S$	$(-V_S-0.15)$		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages							
+ALM	$-V_S$		$(-V_S+36)$	$-V_S$		$(-V_S+36)$	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			
TEMPERATURE MEASUREMENT							
(Specified Temperature Range							
+25°C to +100°C)							
Calibration Error[1]	**−4**		**+4**	**−4**		**+4**	°C
Stability vs. Temperature[2]		±0.02	±0.05		±0.02	±0.05	°C/°C
Gain Error	**−1.5**		**+1.5**	**−1.5**		**+1.5**	%
Nominal Transfer Function		10			10		mV/°C
AMPLIFIER CHARACTERISTICS							
Closed Loop Gain[3]		180.6			245.5		V/V
Input Offset Voltage		°C×53.21+235			°C×41.27−37		µV
Input Bias Current		0.1			0.1		µA
Differential Input Range	−10		+50	−10		+50	mV
Common-Mode Range	$(-V_S-0.15)$		$(+V_S-4)$	$(-V_S-0.15)$		$(+V_S-4)$	Volts
Common-Mode Sensitivity–RTO			**10**			**10**	mV/V
Power Supply Sensitivity–RTO		1	**10**		1	**10**	mV/V
Output Voltage Range							
Dual Supplies	$(-V_S+2.5)$		$(+V_S-2)$	$(-V_S+2.5)$		$(+V_S-2)$	Volts
Single Supply	**0**		$(+V_S-2)$	**0**		$(+V_S-2)$	Volts
Usable Output Current[4]	±5			±5			mA
3dB Bandwidth		15			15		kHz
ALARM CHARACTERISTICS							
$V_{CE(SAT)}$ at 2mA		0.3			0.3		Volts
Leakage Current			**±1**			**±1**	µA
Operating Voltage at −ALM			$(+V_S-4)$			$(+V_S-4)$	Volts
Short Circuit Current		20			20		mA
POWER REQUIREMENTS							
Operating[5]		$(+V_S$ to $-V_S)\leq 30$			$(+V_S$ to $-V_S)\leq 30$		Volts
Quiescent Current							
$+V_S$		160	**300**		160	**300**	µA
$-V_S$		100	**200**		100	**200**	µA
PACKAGE OPTION[6]							
TO-100 (H-10A)		AD596AH			AD597AH		

NOTES

[1]This is a measure of the deviation from ideal with a measuring thermocouple junction of 175°C and a chip temperature of 60°C. The ideal transfer function is given by:

AD596: $V_{OUT} = 180.57\times(V_m - V_a +$ (ambient in °C)$\times 53.21\mu V/°C + 235\mu V)$

AD597: $V_{OUT} = 245.46\times(V_m - V_a +$ (ambient in °C)$\times 41.27\mu V/°C - 37\mu V)$.

Where V_m and V_a represent the measuring and ambient temperatures and are taken from the appropriate J or K thermocouple table. The ideal transfer function minimizes the error over the ambient temperature range of 25°C to 100°C with a thermocouple temperature of approximately 175°C.

[2]Defined as the slope of the line connecting the AD596/AD597 CJC errors measured at 25°C and 100°C ambient temperature.

[3]Pin 6 shorted to pin 7.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50kΩ resistor at output voltages below 2.5V.

[5]$-V_S$ must not exceed −16.5V.

[6]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Thermocouple Temperature °C	Type J Voltage mV	AD596 Output mV	Type K Voltage mV	AD597 Output mV
− 200	− 7.890	−1370	− 5.891	−1446
− 180	− 7.402	−1282	− 5.550	−1362
− 160	− 6.821	−1177	− 5.141	−1262
− 140	− 6.159	−1058	− 4.669	−1146
− 120	− 5.426	− 925	− 4.138	−1016
− 100	− 4.632	− 782	− 3.553	− 872
− 80	− 3.785	− 629	− 2.920	− 717
− 60	− 2.892	− 468	− 2.243	− 551
− 40	− 1.960	− 299	− 1.527	− 375
− 20	− .995	− 125	− .777	− 191
− 10	− .501	− 36	− .392	− 96
0	0	54	0	0
10	.507	146	.397	97
20	1.019	238	.798	196
25	1.277	285	1.000	245
30	1.536	332	1.203	295
40	2.058	426	1.611	395
50	2.585	521	2.022	496
60	3.115	617	2.436	598
80	4.186	810	3.266	802
100	5.268	1006	4.095	1005
120	6.359	1203	4.919	1207
140	7.457	1401	5.733	1407
160	8.560	1600	6.539	1605
180	9.667	1800	7.338	1801
200	10.777	2000	8.137	1997
220	11.887	2201	8.938	2194
240	12.998	2401	9.745	2392
260	14.108	2602	10.560	2592
280	15.217	2802	11.381	2794
300	16.325	3002	12.207	2996
320	17.432	3202	13.039	3201
340	18.537	3402	13.874	3406
360	19.640	3601	14.712	3611
380	20.743	3800	15.552	3817
400	21.846	3999	16.395	4024
420	22.949	4198	17.241	4232
440	24.054	4398	18.088	4440
460	25.161	4598	18.938	4649
480	26.272	4798	19.788	4857
500	27.388	5000	20.640	5066
520	28.511	5203	21.493	5276
540	29.642	5407	22.346	5485
560	30.782	5613	23.198	5694
580	31.933	5821	24.050	5903
600	33.096	6031	24.902	6112
620	34.273	6243	25.751	6321
640	35.464	6458	26.599	6529
660	36.671	6676	27.445	6737
680	37.893	6897	28.288	6944
700	39.130	7120	29.128	7150
720	40.382	7346	29.965	7355
740	41.647	7575	30.799	7560
750	42.283	7689	31.214	7662
760	–	–	31.629	7764
780	–	–	32.455	7966
800	–	–	33.277	8168
820	–	–	34.095	8369
840	–	–	34.909	8569
860	–	–	35.718	8767
880	–	–	36.524	8965
900	–	–	37.325	9162
920	–	–	38.122	9357
940	–	–	38.915	9552
960	–	–	39.703	9745
980	–	–	40.488	9938
1000	–	–	41.269	10130
1020	–	–	42.045	10320
1040	–	–	42.817	10510
1060	–	–	43.585	10698
1080	–	–	44.439	10908
1100	–	–	45.108	11072
1120	–	–	45.863	11258
1140	–	–	46.612	11441
1160	–	–	47.356	11624
1180	–	–	48.095	11805
1200	–	–	48.828	11985
1220	–	–	49.555	12164
1240	–	–	50.276	12341
1250	–	–	50.633	12428

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +60°C, V_S = −5V, +15V)

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TEMPERATURE PROPORTIONAL OUTPUT MODE

The AD596/AD597 can be used to generate a temperature proportional output of 10mV/°C when operated with J and K type thermocouples as shown in Figure 1. Thermocouples produce low level output voltages which are a function of both the temperature being measured and the reference or cold junction temperature. The AD596/AD597 compensates for the cold junction temperature and amplifies the thermocouple signal to produce a high level 10mV/°C voltage output which is a function only of the temperature being measured. The temperature stability of the part indicates the sensitivity of the output voltage to changes in ambient or device temperatures. This is typically 0.02°C/°C over the +25°C to +100°C recommended ambient temperature range. The parts will operate over the extended ambient temperature ranges from −55°C to +125°C, but thermocouple nonlinearity at the reference junction will degrade the temperature stability over this extended range. Table I is a list of ideal AD596/AD597 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples with package and reference junction at 60°C. As is normally the case, these outputs

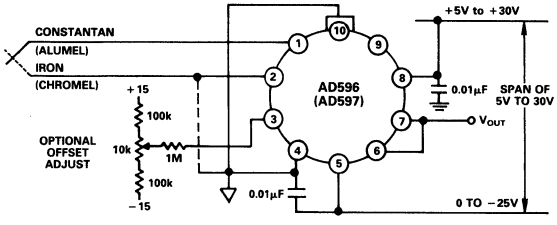


Figure 1. Temperature Proportional Output Connection

are subject to calibration and temperature sensitivity errors. These tables are derived using the ideal transfer functions:

AD596 output = (Type J voltage +301.5µV) × 180.57
AD597 output = (Type K voltage) × 245.46

The offsets and gains of these devices have been laser trimmed to closely approximate thermocouple characteristics over measurement temperature ranges centered around 175°C with the

AD596/AD597 at an ambient temperature between 25°C and 100°C. This eliminates the need for additional gain or offset adjustments to make the output voltage read:

V_{OUT} = 10mV/°C × (thermocouple temperature in °C) (within specified tolerances).

Excluding calibration errors, the above transfer function is accurate to within 1°C from +80°C to +550°C for the AD596 and −20°C to +350°C for the AD597. The different temperature ranges are due to the differences in J and K type thermocouple curves.

European DIN FE-CuNi thermocouple vary slightly from ANSI type J thermocouples. Table I does not apply when these types of thermocouples are used. The transfer functions given previously and a thermocouple table should be used instead.

Figure 1 also shows an optional trimming network which can be used to change the device's offset voltage. Injecting or sinking 200nA from Pin 3 will offset the output aproximately 10mV (1°C).

The AD596/AD597 can operate from a single supply from 5V to 36V or from split supplies totalling 36V or less as shown. Since the output can only swing to within 2V of the positive supply, the usable measurement temperature range will be restricted when positive supplies less than 15V for the AD597 and 10V for the AD596 are used. If the AD596/AD597 is to be used to indicate negative Celsius temperatures, then a negative supply is required.

Common-mode voltages on the thermocouple inputs must remain within the common-mode voltage range of the AD596/AD597, with a return path provided for the bias currents. If the thermocouple is not remotely grounded, then the dotted line connection shown in Figure 1 must be made to one of the thermocouple inputs. If there is no return path for the bias currents, the input stage will saturate, causing erroneous output voltages.

In this configuration, the AD596/AD597 has circuitry which detects the presence of an open thermocouple. If the thermocouple loop becomes open, one or both of the inputs to the device will be deprived of bias current causing the output to saturate. It is this saturation which is detected internally and used to activate the alarm circuitry. The output of this feature has a flexible format which can be used to source or sink up to 20mA of current. The collector (+ALM) should not be allowed to become more positive than ($-V_S$ +36V), however, it may be permitted to be more positive than $+V_S$. The emitter voltage (−ALM) should be constrained such that it does not become more positive than 4V below $+V_S$. If the alarm feature is not used, this pin should be connected to Pins 4 or 5 as shown in Figure 1.

SET-POINT CONTROL MODE

The AD596/AD597 can be connected as a set-point controller as shown in Figure 2. The thermocouple voltage is cold junction compensated, amplified, and compared to an external set-point voltage. The relationship between set-point voltage and temperature is given in Table I. If the temperature to be controlled is within the operating range (−55°C to +125°C) of the device, it can monitor its own temperature by shorting the inputs to ground. The set-point voltage with the thermocouple inputs grounded is given by the expressions:

AD596 Set-Point Voltage = °C × 9.6mV/°C +42mV
AD597 Set-Point Voltage = °C × 10.1mV/°C −9.1mV

The input impedance of the set-point pin of the AD596/AD597 is approximately 50kΩ. The temperature coefficient of this resistance is ±15ppm/°C. Therefore, the 100ppm/°C 5kΩ pot

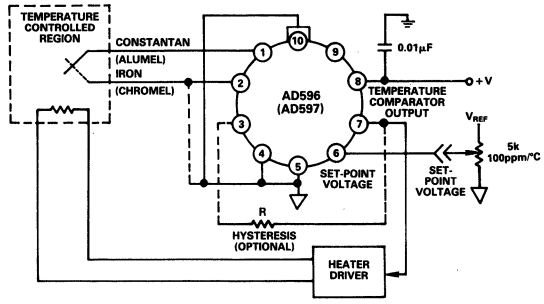


Figure 2. Set-Point Control Mode

shown in Figure 2 will only introduce an additional ±1°C degradation of temperature stability over the +25°C to +100°C ambient temperature range.

Switching hysteresis is often used in set-point systems of this type to provide noise immunity and increase system reliability. By reducing the frequency of on-off cycling, mechanical component wear is reduced leading to enhanced system reliability. This can easily be implemented with a single external resistor between Pins 7 and 3 of the AD596/AD597. Each 200nA of current injected into Pin 3 when the output switches will cause about 1°C of hysteresis; that is: $R_{HYST}\ (\Omega) = \frac{V_{OUT}}{200nA} \times \frac{1}{°C_{HYST}}$.

In the set-point configuration, the AD596/AD597 output is saturated at all times, so the alarm transistor will be ON regardless of whether there is an open circuit or not. However, −ALM must be tied to a voltage below ($+V_S$ −4V) for proper operation of the rest of the circuit.

STAND-ALONE TEMPERATURE TRANSDUCER

The AD596/AD597 may be configured as a stand-alone Celsius thermometer as shown in Figure 3.

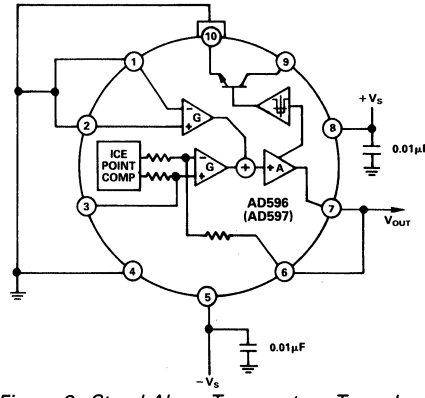


Figure 3. Stand-Alone Temperature Transducer Temperature Proportional Output Connection

Simply omit the thermocouple and connect the inputs (Pins 1 and 2) to common. The output will now reflect the compensation voltage and hence will indicate the AD596/AD597 temperature. In this three terminal, voltage output, temperature sensing mode, the AD596/AD597 will operate over the full extended −55°C to +125°C temperature range. The output scaling will be 9.6mV per °C with the AD596 and 10.1mV per °C with the AD597. Additionally there will be a 42mV offset with the AD596 causing it to read slightly high when used in this mode.

THERMOCOUPLE CONNECTIONS

The connection of the thermocouple wire and the normal wire or printed circuit board traces going to the AD596/AD597 forms an effective reference junction as shown in Figure 4. This junction must be kept at the same temperature as the AD596/AD597 for the internal cold junction compensation to work properly. Unless the AD596/AD597 is in a thermally stable enclosure, the thermocouple leads should be brought in directly to Pins 1 and 2.

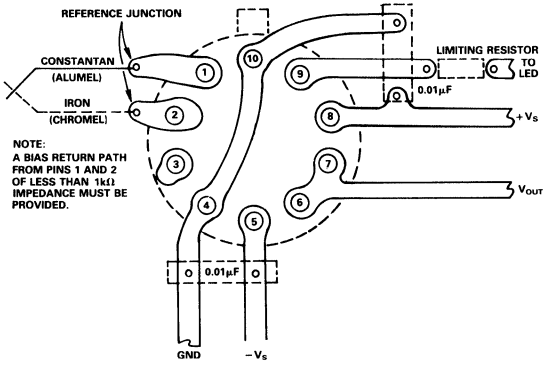


Figure 4. PCB Connections

To ensure secure bonding, the thermocouple wire should be cleaned to remove oxidization prior to soldering. Noncorrosive resin flux is effective with iron, constantan, chromel, and alumel, and the following solders: 95% tin–5% silver, or 90% tin–10% lead.

SINGLE AND DUAL SUPPLY CONNECTIONS

In the single supply configuration as used in the set-point controller of Figure 2, any convenient voltage from +5V to +36V may be used, with self-heating errors being minimized at lower supply levels. In this configuration, the $-V_S$ connection at Pin 5 is tied to ground. Temperatures below zero can be accommodated in the single supply set-point mode, but not in the single supply temperature measuring mode (Figure 1 reconnected for single supply). Temperatures below zero can only be indicated by a negative output voltage, which is impossible in the single supply mode.

Common-mode voltages on the thermocouple inputs must remain below the positive supply, and not more than 0.15V more negative than the minus supply. In addition, a return path for the input bias currents must be provided. If the thermocouple is not remotely grounded, then the dotted line connections in Figures 1 and 2 are mandatory.

STABILITY OVER TEMPERATURE

The AD596/AD597 is specified for a maximum error of ±4°C at an ambient temperature of 60°C and a measuring junction temperature at 175°C. The ambient temperature stability is specified to be a maximum of 0.05°C/°C. In other words, for every degree change in the ambient temperature, the output will change no more than 0.05 degrees. So, at 25°C the maximum deviation from the temperature-voltage characteristic of Table I is ±5.75°C, and at 100°C it is ±6°C maximum (see Figure 5). If the offset error of ±4°C is removed with a single offset adjustment, these errors will be be reduced to ±1.75°C and ±2°C max. The optional trim circuit shown in Figure 1 demonstrates how the ambient offset error can be adjusted to zero.

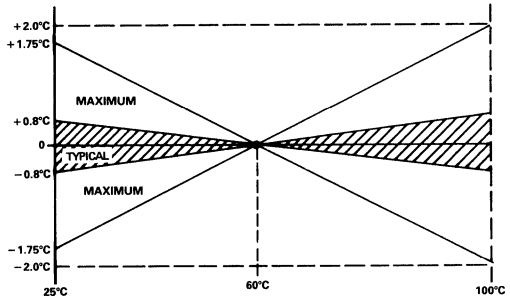


Figure 5. Drift Error vs. Temperature

THERMAL ENVIRONMENTAL EFFECTS

The inherent low power dissipation of the AD596/AD597 keeps self-heating errors to a minimum. However, device output is capable of delivering ±5mA to an external load and the alarm circuitry can supply up to 20mA. Since the typical junction to ambient thermal resistance in free air is 150°C/W, significant temperature difference between the package pins (where the reference junction is located) and the chip (where the cold junction temperature is measured and then compensated) can exist when the device is operated in a high dissipation mode. These temperature differences will result in a direct error at the output. In the temperature proportional mode, the alarm feature will only activate in the event of an open thermocouple or system transient which causes the device output to saturate. Self-Heating errors will not effect the operation of the alarm but two cases do need to be considered. First, after a fault is corrected and the alarm is reset, the AD596/AD597 must be allowed to cool before readings can again be accurate. This can take 5 minutes or more depending upon the thermal environment seen by the device. Second, the junction temperature of the part should not be allowed to exceed 150°C. If the alarm circuit of the AD596/AD597 is made to source or sink 20mA with 30V across it, the junction temperature will be 90°C above ambient causing the die temperature to exceed 150°C when ambient is above 60°C. In this case, either the load must be reduced, or a heat sink used to lower the thermal resistance.

TEMPERATURE READOUT AND CONTROL

Figure 6 shows a complete temperature indication and control system based on the AD596/AD597. Here the AD596/AD597 is being used as a closed-loop thermocouple signal conditioner and an external op-amp is used to implement set point. This has two important advantages. It provides a high level (10mV/°C) output for the A/D panel meter and also preserves the alarm function for open thermocouples.

The A/D panel meter can easily be offset and scaled as shown to read directly in degrees Fahrenheit. If a two temperature calibration scheme is used, the dominant residual errors will arise from two sources; the ambient temperature rejection (typically ±2°C over a 25°C to 100°C range) and thermocouple nonlinearity typical +1°C from 80°C to 550°C for type J and +1°C from −20°C to 350°C for type K.

An external voltage reference is used both to increase the stability of the A/D converter and supply a stable reference for the set-point voltage.

A traditional requirement for the design of set-point control thermocouple systems has been to configure the system such that the appropriate action is taken in the event of an open thermocouple. The open thermocouple alarm pin with its flexible current-limited output format supports this function when the part operates in the temperature proportional mode. In addition, if the thermocouple is not remotely grounded, it is possible to program the device for either a positive or negative full scale output in the event of an open thermocouple. This is done by connecting the bias return resistor directly to Pin 1 if a high output voltage is desired to indicate a fault condition. Alternately, if the bias return is provided on the thermocouple lead connected to Pin 2, an open circuit will result in an output low reading. Figure 6 shows the ground return connected to Pin 1 so that if the thermocouple fails, the heater will remain off. At the same time, the alarm circuit lights the LED signalling the need to service the thermocouple. Grounding Pin 2 would lead to low output voltage saturation, and in this circuit would result in a potentially dangerous thermal runaway under fault conditions.

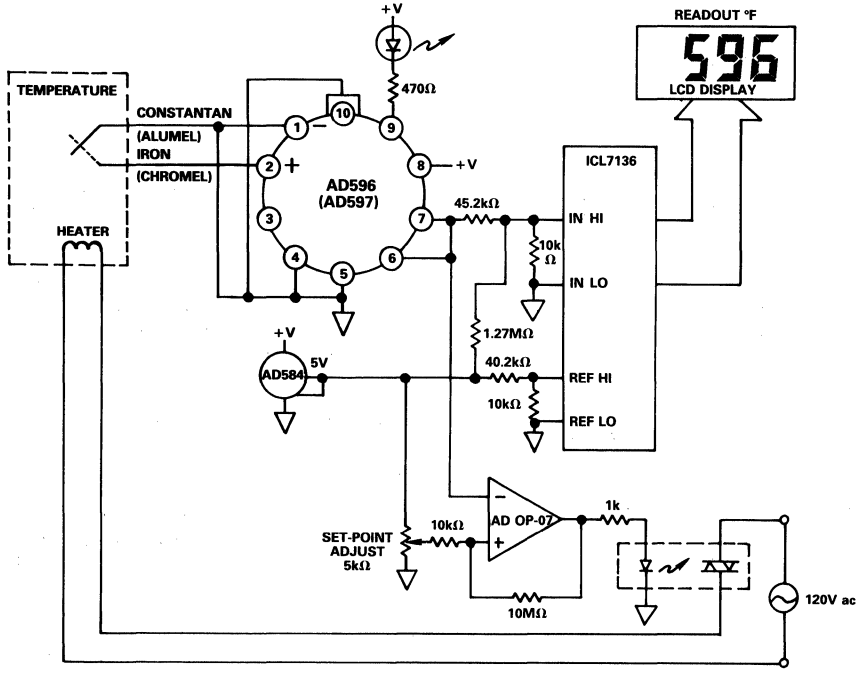


Figure 6. Temperature Measurement and Control

LVDT Signal Conditioner

AD598

FEATURES

Single Chip Solution, Contains Internal Oscillator and Voltage Reference
No Adjustments Required
Insensitive to Transducer Null Voltage
Insensitive to Primary to Secondary Phase Shifts
DC Output Proportional to Position
20 Hz to 20 kHz Frequency Range
Single or Dual Supply Operation
Unipolar or Bipolar Output
Will Operate a Remote LVDT at Up to 300 Feet
Position Output Can Drive Up to 1000 Feet of Cable
Will Also Interface to an RVDT
Outstanding Performance
Linearity: 0.05% of FS max
Output Voltage: ±11 V min
Gain Drift: 50 ppm/°C of FS max
Offset Drift: 50 ppm/°C of FS max

PRODUCT DESCRIPTION

The AD598 is a complete, monolithic Linear Variable Differential Transformer (LVDT) signal conditioning subsystem. It is used in conjunction with LVDTs to convert transducer mechanical position to a unipolar or bipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passive components to set frequency and gain, the AD598 converts the raw LVDT secondary output to a scaled dc signal. The device can also be used with RVDT transducers.

The AD598 contains a low distortion sine wave oscillator to drive the LVDT primary. The LVDT secondary output consists of two sine waves that drive the AD598 directly. The AD598 operates upon the two signals, dividing their difference by their sum, producing a scaled unipolar or bipolar dc output.

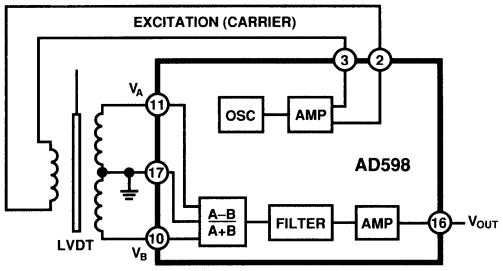
The AD598 uses a unique ratiometric architecture (patent pending) to eliminate several of the disadvantages associated with traditional approaches to LVDT interfacing. The benefits of this new circuit are: no adjustments are necessary, transformer null voltage and primary to secondary phase shift does not affect system accuracy, temperature stability is improved, and transducer interchangeinterchangeabilityability is improved.

The AD598 is available in two performance grades:

Grade	Temperature Range	Package
AD598JR	0 to +70°C	20-Pin Small Outline (SOIC)
AD598AD	−40°C to +85°C	20-Pin Ceramic DIP

It is also available processed to MIL-STD-883B, for the military range of −55°C to +125°C.

AD598 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD598 offers a monolithic solution to LVDT and RVDT signal conditioning problems; few extra passive components are required to complete the conversion from mechanical position to dc voltage and no adjustments are required.
2. The AD598 can be used with many different types of LVDTs because the circuit accommodates a wide range of input and output voltages and frequencies; the AD598 can drive an LVDT primary with up to 24 V rms and accept secondary input levels as low as 100 mV rms.
3. The 20 Hz to 20 kHz LVDT excitation frequency is determined by a single external capacitor. The AD598 input signal need not be synchronous with the LVDT primary drive. This means that an external primary excitation, such as the 400 Hz power mains in aircraft, can be used.
4. The AD598 uses a ratiometric decoding scheme such that primary to secondary phase shifts and transducer null voltage have absolutely no effect on overall circuit performance.
5. Multiple LVDTs can be driven by a single AD598, either in series or parallel as long as power dissipation limits are not exceeded. The excitation output is thermally protected.
6. The AD598 may be used in telemetry applications or in hostile environments where the interface electronics may be remote from the LVDT. The AD598 can drive an LVDT at the end of 300 feet of cable, since the circuit is not affected by phase shifts or absolute signal magnitudes. The position output can drive as much as 1000 feet of cable.
7. The AD598 may be used as a loop integrator in the design of simple electromechanical servo loops.

SPECIFICATIONS (typical @ +25°C and ±15 V dc, C1 = 0.015 μF, R2 = 80 kΩ, R_L = 2 kΩ, unless otherwise noted. See Figure 7.)

Model	AD598J Min	AD598J Typ	AD598J Max	AD598A Min	AD598A Typ	AD598A Max	Unit
TRANSFER FUNCTION[1]	$V_{OUT} = \frac{V_A - V_B}{V_A + V_B} \times 500\ \mu A \times R2$						V
OVERALL ERROR[2]							
T_{min} to T_{max}		0.6	2.35		0.6	1.65	% of FS
SIGNAL OUTPUT CHARACTERISTICS							
Output Voltage Range (T_{min} to T_{max})	**±11**			**±11**			V
Output Current (T_{min} to T_{max})	**8**			**6**			mA
Short Circuit Current		20			20		mA
Nonlinearity[3] (T_{min} to T_{max})		75	**±500**		75	**±500**	ppm of FS
Gain Error[4]		0.4	**±1**		0.4	**±1**	% of FS
Gain Drift		20	**±100**		20	**±50**	ppm/°C of FS
Offset[5]		0.3	**±1**		0.3	**±1**	% of FS
Offset Drift		7	**±200**		7	**±50**	ppm/°C of FS
Excitation Voltage Rejection[6]		100			100		ppm/dB
Power Supply Rejection (±12 V to ±18 V)							
PSRR Gain (T_{min} to T_{max})	**300**	100		**400**	100		ppm/V
PSRR Offset (T_{min} to T_{max})	**100**	15		**200**	15		ppm/V
Common Mode Rejection (±3 V)							
CMRR Gain (T_{min} to T_{max})	**100**	25		**200**	25		ppm/V
CMRR Offset (T_{min} to T_{max})	**100**	6		**200**	6		ppm/V
Output Ripple[7]		4			4		mV rms
EXCITATION OUTPUT CHARACTERISTICS (@ 2.5 kHz)							
Excitation Voltage Range	2.1		24	2.1		24	V rms
Excitation Voltage							
(R1 = Open)[8]	**1.2**		**2.1**	**1.2**		**2.1**	V rms
(R1 = 12.7 kΩ)[8]	**2.6**		**4.1**	**2.6**		**4.1**	V rms
(R1 = 487 Ω)[8]	**14**		**20**	**14**		**20**	V rms
Excitation Voltage TC[9]		600			600		ppm/°C
Output Current	**30**			**30**			mA rms
T_{min} to T_{max}	12			12			mA rms
Short Circuit Current		60			60		mA
DC Offset Voltage (Differential, R1 = 12.7 kΩ)							
T_{min} to T_{max}		30	**±100**		30	**±100**	mV
Frequency	20		20k	20		20k	Hz
Frequency TC, (R1 = 12.7 kΩ)		200			200		ppm/°C
Total Harmonic Distortion		−50			−50		dB
SIGNAL INPUT CHARACTERISTICS							
Signal Voltage	0.1		3.5	0.1		3.5	V rms
Input Impedance		200			200		kΩ
Input Bias Current (AIN and BIN)		1	**5**		1	**5**	μA
Signal Reference Bias Current		2	**10**		2	**10**	μA
Excitation Frequency	0		20	0		20	kHz
POWER SUPPLY REQUIREMENTS							
Operating Range	13		36	13		36	V
Dual Supply Operation (±10 V Output)	±13			±13			V
Single Supply Operation							
0 to +10 V Output	17.5			17.5			V
0 to −10 V Output	17.5			17.5			V
Current (No Load at Signal and Excitation Outputs)		12	**15**		12	**15**	mA
T_{min} to T_{max}			**16**			**18**	mA
TEMPERATURE RANGE							
JR (SOIC)	0		70				°C
AD (DIP)				−40		+85	°C
PACKAGE OPTION[10]							
SOIC (R-20)		AD598JR					
Side Brazed DIP (D-20)					AD598AD		

NOTES

[1]V_A and V_B represent the Mean Average Deviation (MAD) of the detected sine waves. Note that for this Transfer Function to linearly represent positive displacement, the sum of V_A and V_B of the LVDT must remain constant with stroke length. See "Theory of Operation." Also see Figures 7 and 12 for R2.

[2]From T_{min} to T_{max} the overall error due to the AD598 alone is determined by combining gain error, gain drift and offset drift. For example, the worst case overall error for the AD598AD from T_{min} to T_{max} is calculated as follows: overall error = gain error at +25°C (±1% full scale) + gain drift from −40°C to +25°C (50 ppm/°C of FS × +65°C) + offset drift from −40°C to +25°C (50 ppm/°C of FS× 65°C) = ±1.65% of full scale. Note that 1000 ppm of full scale equals 0.1% of full scale. Full scale is defined as the voltage difference between the maximum positive and maximum negative output.

[3]Nonlinearity of the AD598 only, in units of ppm of full scale. Nonlinearity is defined as the maximum measured deviation of the AD598 output voltage from a straight line. The straight line is determined by connecting the maximum produced full-scale negative voltage with the maximum produced full-scale positive voltage.

[4]See Transfer Function.

[5]This offset refers to the $(V_A-V_B)/(V_A+V_B)$ input spanning a full-scale range of ±1. [For $(V_A-V_B)/(V_A+V_B)$ to equal +1, V_B must equal zero volts; and correspondingly for $(V_A-V_B)/(V_A+V_B)$ to equal −1, V_A must equal zero volts. Note that offset errors do not allow accurate use of zero magnitude inputs; practical inputs are limited to 100 mV rms.] The ±1 span is a convenient reference point to define offset referred to input. For example, with this input span a value of R2 = 20 kΩ would give V_{OUT} span a value of ±10 volts. Caution, most LVDTs will typically exercise less of the $(V_A-V_B)/(V_A+V_B)$ input span and thus require a larger value of R2 to produce the ±10 V output span. In this case the offset is correspondingly magnified when referred to the output voltage. For example, a Schaevitz E100 LVDT requires 80.2 kΩ for R2 to produce a ±10.69 V output and $(V_A-V_B)/(V_A+V_B)$ equals 0.27. This ratio may be determined from the graph shown in Figure 18, $(V_A-V_B)/(V_A+V_B)$ = (1.71 V rms−0.99 V rms)/(1.71 V rms+0.99 V rms). The maximum offset value referred to the ±10.69 V output may be determined by multiplying the maximum value shown in the data sheet (±1% of FS by 1/0.27 which equals ±3.7% maximum. Similarly, to determine the maximum values of offset drift, offset CMRR and offset PSRR when referred to the ±10.69 V output, these data sheet values should also be multiplied by (1/0.27). For this example, for the AD598AD the maximum values of offset drift, PSRR offset and CMRR offset would be: 185 ppm/°C of FS; 741 ppm/V and 741 ppm/V respectively when referred to the ±10.69 V output.

[6]For example, if the excitation to the primary changes by 1 dB, the gain of the system will change by typically 100 ppm.

[7]Output ripple is a function of the AD598 bandwidth determined by C2, C3 and C4. See Figures 16 and 17.

[8]R1 is shown in Figures 7 and 12.

[9]Excitation voltage drift is not an important specification because of the ratiometric operation of the AD598.

[10]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tested are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

THERMAL CHARACTERISTICS

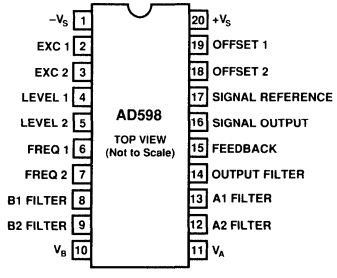
	θ_{JC}	θ_{JA}
SOIC Package	22°C/W	80°C/W
Side Brazed Package	25°C/W	85°C/W

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ . . . . . 36 V
Storage Temperature Range
R Package . . . . . −65°C to +150°C
D Package . . . . . −65°C to +150°C
Operating Temperature Range
AD598JR . . . . . 0 to +70°C
AD598AD . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 Seconds) . . . . +300°C
Power Dissipation Up to +65°C . . . . . 1.2 W
Derates Above +65°C . . . . . 12 mW/°C

CONNECTION DIAGRAM

Plastic SOIC (R) Package
and
Side Brazed Ceramic DIP (D) Package



13

Typical Characteristics (at +25°C and V_S = ±15 V unless otherwise noted)

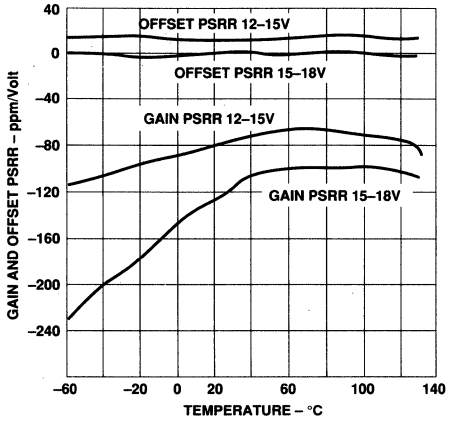


Figure 1. Gain and Offset PSRR vs. Temperature

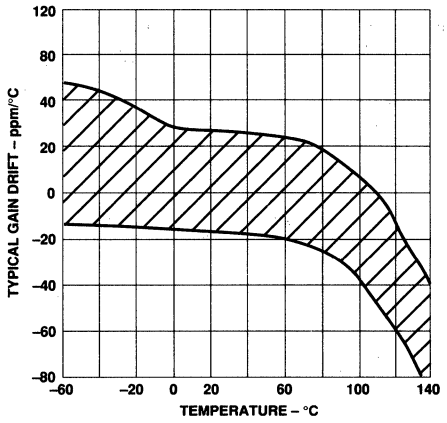


Figure 2. Typical Gain Drift vs. Temperature

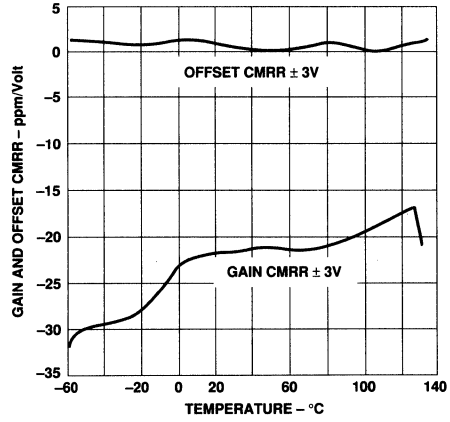


Figure 3. Gain and Offset CMRR vs. Temperature

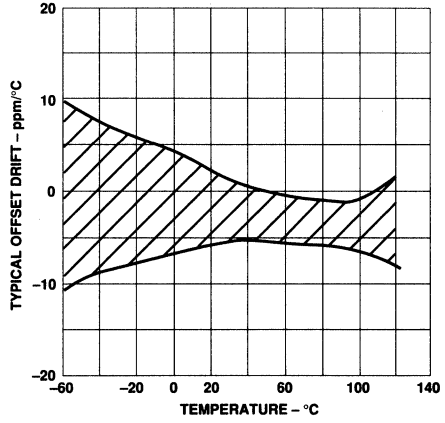


Figure 4. Typical Offset Drift vs. Temperature

THEORY OF OPERATION

A block diagram of the AD598 along with an LVDT (Linear Variable Differential Transformer) connected to its input is shown in Figure 5. The LVDT is an electromechanical transducer whose input is the mechanical displacement of a core and whose output is a pair of ac voltages proportional to core position. The transducer consists of a primary winding energized by an external sine wave reference source, two secondary windings connected in series, and the moveable core to couple flux between the primary and secondary windings.

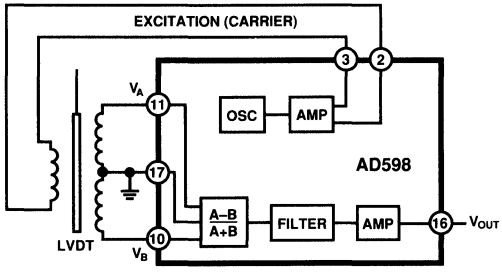


Figure 5. AD598 Functional Block Diagram

The AD598 energizes the LVDT primary, senses the LVDT secondary output voltages and produces a dc output voltage proportional to core position. The AD598 consists of a sine wave oscillator and power amplifier to drive the primary, a decoder which determines the ratio of the difference between the LVDT secondary voltages divided by their sum, a filter and an output amplifier.

The oscillator comprises a multivibrator which produces a triwave output. The triwave drives a sine shaper, which produces a low distortion sine wave whose frequency is determined by a single capacitor. Output frequency can range from 20 Hz to 20 kHz and amplitude from 2 V rms to 24 V rms. Total harmonic distortion is typically −50 dB.

The output from the LVDT secondaries consists of a pair of sine waves whose amplitude difference, $(V_A–V_B)$, is proportional to core position. Previous LVDT conditioners synchronously detect this amplitude difference and convert its absolute value to a voltage proportional to position. This technique uses the primary excitation voltage as a phase reference to determine the polarity of the output voltage. There are a number of problems associated with this technique such as (1) producing a constant amplitude, constant frequency excitation signal, (2) compensating for LVDT primary to secondary phase shifts, and (3) compensating for these shifts as a function of temperature and frequency.

The AD598 eliminates all of these problems. The AD598 does not require a constant amplitude because it works on the ratio of the difference and sum of the LVDT output signals. A constant frequency signal is not necessary because the inputs are rectified and only the sine wave carrier magnitude is processed. There is no sensitivity to phase shift between the primary excitation and the LVDT outputs because synchronous detection is not employed. The ratiometric principle upon which the AD598 operates requires that the sum of the LVDT secondary voltages remains constant with LVDT stroke length. Although LVDT manufacturers generally do not specify the relationship between V_A+V_B and stroke length, it is recognized that some LVDTs do not meet this requirement. In these cases a nonlinearity will result. However, the majority of available LVDTs do in fact meet these requirements.

The AD598 utilizes a special decoder circuit. Referring to the block diagram and Figure 6 below, an implicit analog computing loop is employed. After rectification, the A and B signals are multiplied by complementary duty cycle signals, d and (1–d) respectively. The difference of these processed signals is integrated and sampled by a comparator. It is the output of this comparator that defines the original duty cycle, d, which is fed back to the multipliers.

As shown in Figure 6, the input to the integrator is [(A+B)d]-B. Since the integrator input is forced to 0, the duty cycle $d = B/(A+B)$.

The output comparator which produces $d = B/(A+B)$ also controls an output amplifier driven by a reference current. Duty cycle signals d and (1–d) perform separate modulations on the reference current as shown in Figure 6, which are summed. The summed current, which is the output current, is $I_{REF} \times (1–2d)$.

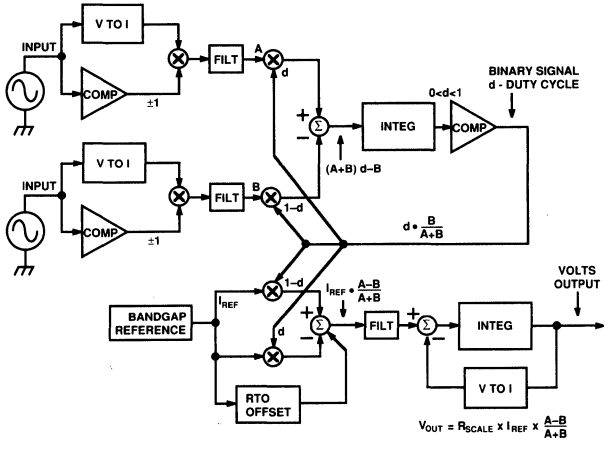


Figure 6. Block Diagram of Decoder

Since d = B/(A+B), by substitution the output current equals $I_{REF} \times (A-B)/(A+B)$. This output current is then filtered and converted to a voltage since it is forced to flow through the scaling resistor R2 such that:

$$V_{OUT} = I_{REF} \times (A-B)/(A+B) \times R2$$

CONNECTING THE AD598

The AD598 can easily be connected for dual or single supply operation as shown in Figures 7 and 12. The following general design procedures demonstrate how external component values are selected and can be used for any LVDT which meets AD598 input/output criteria.

Parameters which are set with external passive components include: excitation frequency and amplitude, AD598 system bandwidth, and the scale factor (V/inch). Additionally, there are optional features, offset null adjustment, filtering, and signal integration which can be used by adding external components.

DESIGN PROCEDURE
DUAL SUPPLY OPERATION

Figure 7 shows the connection method with dual ±15 volt power supplies and a Schaevitz E100 LVDT. This design procedure can be used to select component values for other LVDTs as well. The procedure is outlined in Steps 1 through 10 as follows:

1. Determine the mechanical bandwidth required for LVDT position measurement subsystem, $f_{SUBSYSTEM}$. For this example, assume $f_{SUBSYSTEM}$ = 250 Hz.
2. Select minimum LVDT excitation frequency, approximately 10 × $f_{SUBSYSTEM}$. Therefore, let excitation frequency = 2.5 kHz.
3. Select a suitable LVDT that will operate with an excitation frequency of 2.5 kHz. The Schaevitz E100, for instance, will operate over a range of 50 Hz to 10 kHz and is an eligible candidate for this example.
4. Determine the sum of LVDT secondary voltages V_A and V_B. Energize the LVDT at its typical drive level V_{PRI} as shown in the manufacturer's data sheet (3 V rms for the E100). Set the core displacement to its center position where $V_A = V_B$. Measure these values and compute their sum V_A+V_B. For the E100, V_A+V_B = 2.70 V rms. This calculation will be used later in determining AD598 output voltage.
5. Determine optimum LVDT excitation voltage, V_{EXC}. With the LVDT energized at its typical drive level V_{PRI}, set the core displacement to its mechanical full-scale position and measure the output V_{SEC} of whichever secondary produces the largest signal. Compute LVDT voltage transformation ratio, VTR.

   $$VTR = V_{PRI}/V_{SEC}$$

   For the E100, V_{SEC} = 1.71 V rms for V_{PRI} = 3 V rms. VTR = 1.75

   The AD598 signal input, V_{SEC}, should be in the range of 1 V rms to 3.5 V rms for maximum AD598 linearity and minimum noise susceptibility. Select V_{SEC} = 3 V rms. Therefore, LVDT excitation voltage V_{EXC} should be:

   $$V_{EXC} = V_{SEC} \times VTR = 3 \times 1.75 = 5.25\ Vrms$$

   Check the power supply voltages by verifying that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.
6. Referring to Figure 7, for V_S = ±15 V, select the value of the amplitude determining component R1 as shown by the curve in Figure 8.
7. Select excitation frequency determining component C1.

   $$C1 = 35\ \mu F\ Hz/f_{EXCITATION}$$

8. C2, C3 and C4 are a function of the desired bandwidth of the AD598 position measurement subsystem. They should be nominally equal values.

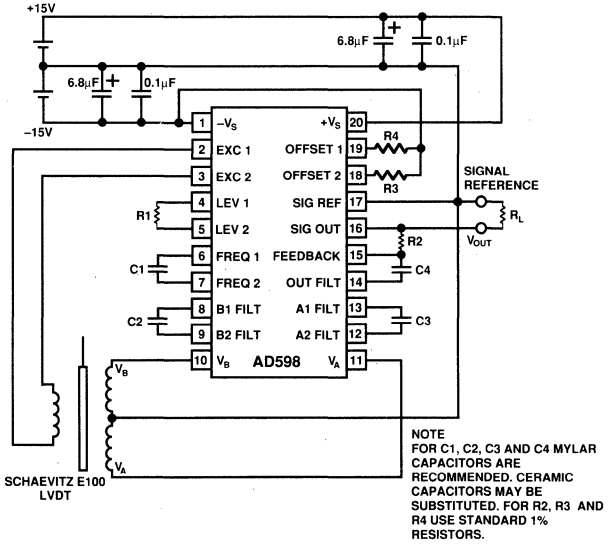


Figure 7. Interconnection Diagram for Dual Supply Operation

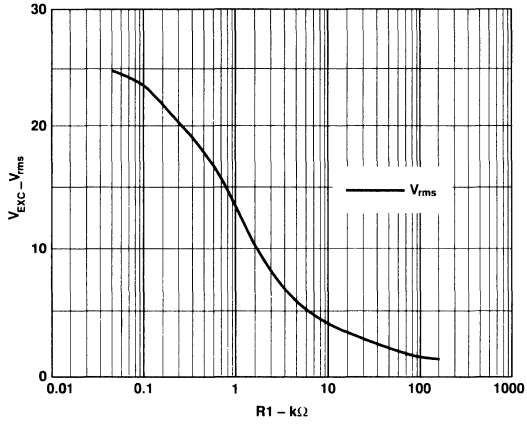


Figure 8. Excitation Voltage V_{EXC} vs. R1

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/f_{SUBSYSTEM}\ (Hz)$$

If the desired system bandwidth is 250 Hz, then

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/250\ Hz = 0.4\ \mu F$$

See Figures 13, 14 and 15 for more information about AD598 bandwidth and phase characterization.

9. In order to Compute R2, which sets the AD598 gain or full-scale output range, several pieces of information are needed:
   a. LVDT sensitivity, S
   b. Full-scale core displacement, d
   c. Ratio of manufacturer recommended primary drive level, V_{PRI}, to (V_A + V_B) computed in Step 4.

   LVDT sensitivity is listed in the LVDT manufacturer's catalog and has units of millivolts output per volts input per inch displacement. The E100 has a sensitivity of 2.4 mV/V/mil. In the event that LVDT sensitivity is not given by the manufacturer, it can be computed. See section on Determining LVDT Sensitivity.

   For a full-scale displacement of d inches, voltage out of the AD598 is computed as

$$V_{OUT} = S \times \left[\frac{V_{PRI}}{(V_A + V_B)}\right] \times 500\mu A \times R2 \times d.$$

   V_{OUT} is measured with respect to the signal reference, Pin 17 shown in Figure 7.

   Solving for R2,

$$R2 = \frac{V_{OUT} \times (V_A + V_B)}{S \times V_{PRI} \times 500\ \mu A \times d} \qquad (1)$$

   Note that V_{PRI} is the same signal level used in Step 4 to determine (V_A + V_B)

   For V_{OUT} = 20 V full-scale range (±10 V) and d = 0.2 inch full-scale displacement (±0.1 inch),

$$R2 = \frac{20\ V \times 2.70\ V}{2.4 \times 3 \times 500\ \mu A \times 0.2} = 75.3\ k\Omega$$

   V_{OUT} as a function of displacement for the above example is shown in Figure 9.

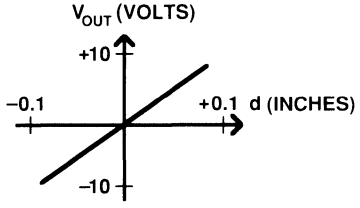


Figure 9. V_{OUT} (±10 V Full Scale) vs. Core Displacement (±0.1 Inch)

10. Selections of R3 and R4 permit a positive or negative output voltage offset adjustment.

$$V_{OS} = 1.2\ V \times R2 \times \left(\frac{1}{R3 + 5\ k\Omega^*} - \frac{1}{R4 + 5\ k\Omega^*}\right) \qquad (2)$$

*These values have a ±20% tolerance.

For no offset adjustment R3 and R4 should be open circuit.

To design a circuit producing a 0 to +10 V output for a displacement of ±0.1 inch, set V_{OUT} to +10 V, d = 0.2 inch and solve Equation (1) for R2.

$$R2 = 37.6\ k\Omega$$

This will produce a response shown in Figure 10.

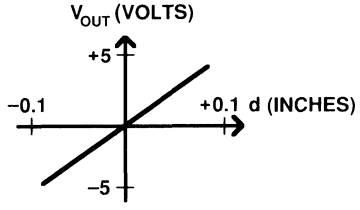


Figure 10. V_{OUT} (±5 V Full Scale) vs. Core Displacement (±0.1 Inch)

In Equation (2) set V_{OS} = 5 V and solve for R3 and R4. Since a positive offset is desired, let R4 be open circuit.

Rearranging Equation (2) and solving for R3

$$R3 = \frac{1.2 \times R2}{V_{OS}} - 5\ k\Omega = 4.02\ k\Omega$$

Figure 11 shows the desired response.

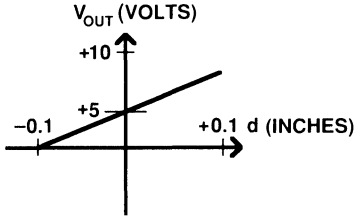


Figure 11. V_{OUT} (0–10 V Full Scale) vs. Displacement (±0.1 Inch)

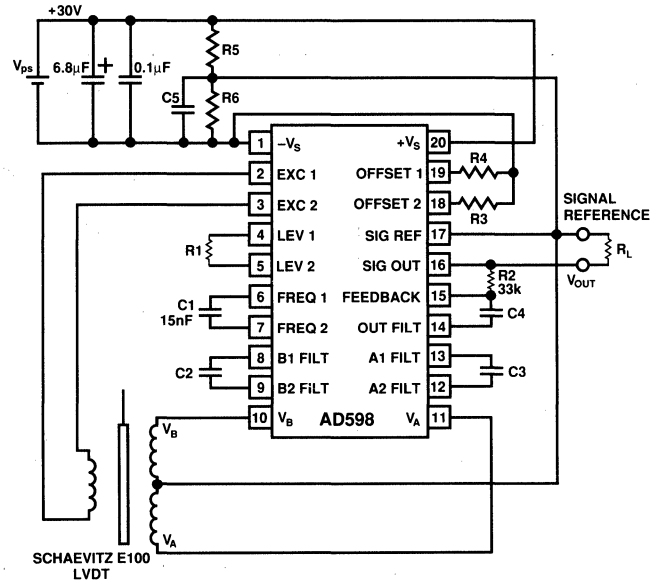


Figure 12. Interconnection Diagram for Single Supply Operation

DESIGN PROCEDURE
SINGLE SUPPLY OPERATION

Figure 12 shows the single supply connection method.

For single supply operation, repeat Steps 1 through 10 of the design procedure for dual supply operation, then complete the additional Steps 11 through 14 below. R5, R6 and C5 are additional component values to be determined. V_{OUT} is measured with respect to SIGNAL REFERENCE.

11. Compute a maximum value of R5 and R6 based upon the relationship

$$R5 + R6 \leq V_{PS}/100\ \mu A$$

12. The voltage drop across R5 must be greater than

$$2 + 10\ k\Omega^* \left(\frac{1.2\ V}{R4 + 5\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2} \right) Volts$$

Therefore

$$R5 \geq \frac{2 + 10\ k\Omega^* \left(\frac{1.2\ V}{R4 + 5\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2} \right)}{100\ \mu A}\ Ohms$$

*These values have ±20% tolerance.

Based upon the constraints of R5 + R6 (Step 11) and R5 (Step 12), select an interim value of R6.

13. Load current through R_L returns to the junction of R5 and R6, and flows back to V_{PS}. Under maximum load conditions, make sure the voltage drop across R5 is met as defined in Step 12.

    As a final check on the power supply voltages, verify that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.

14. C5 is a bypass capacitor in the range of 0.1 μF to 1 μF.

Gain Phase Characteristics

To use an LVDT in a closed loop mechanical servo application, it is necessary to know the dynamic characteristics of the transducer and interface elements. The transducer itself is very quick to respond once the core is moved. The dynamics arise primarily from the interface electronics. Figures 13, 14 and 15 show the frequency response of the AD598 LVDT Signal Conditioner. Note that Figures 14 and 15 are basically the same; the difference is frequency range covered. Figure 14 shows a wider range of mechanical input frequencies at the expense of accuracy. Figure 15 shows a more limited frequency range with

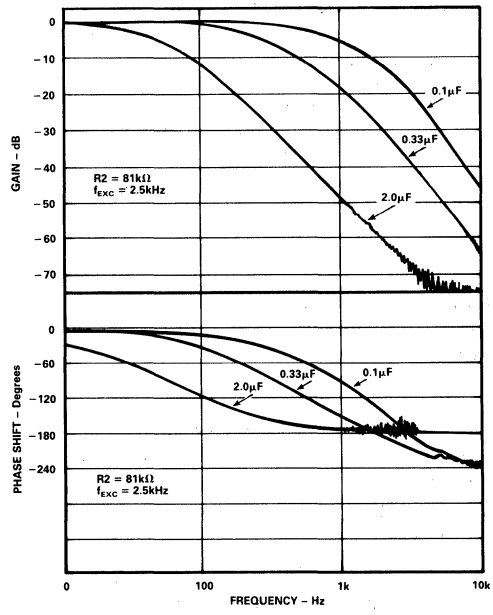


Figure 13. Gain and Phase Characteristics vs. Frequency (0–10 kHz)

enhanced accuracy. The figures are transfer functions with the input to be considered as a sinusoidally varying mechanical position and the output as the voltage from the AD598; the units of the transfer function are volts per inch. The value of C2, C3 and C4, from Figure 7, are all equal and designated as a parameter in the figures. The response is approximately that of two real poles. However, there is appreciable excess phase at higher frequencies. An additional pole of filtering can be introduced with a shunt capacitor across R2, (see Figure 7); this will also increase phase lag.

When selecting values of C2, C3 and C4 to set the bandwidth of the system, a trade-off is involved. There is ripple on the "dc" position output voltage, and the magnitude is determined by the filter capacitors. Generally, smaller capacitors will give higher system bandwidth and larger ripple. Figures 16 and 17 show the magnitude of ripple as a function of C2, C3 and C4, again all equal in value. Note also a shunt capacitor across R2 shown as a parameter (see Figure 7). The value of R2 used was 81 kΩ with a Schaevitz E100 LVDT.

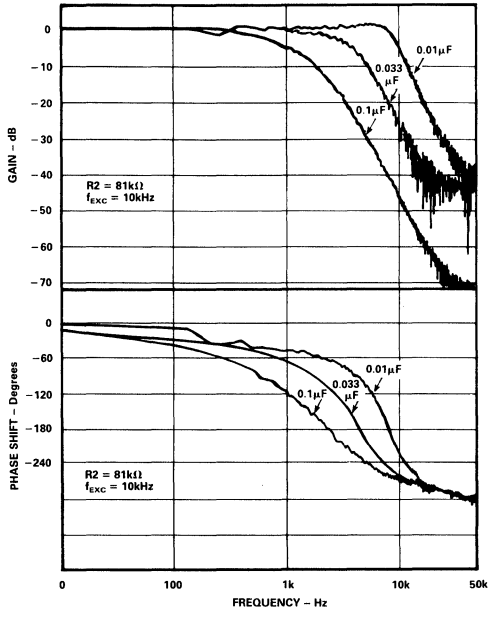


Figure 14. Gain and Phase Characteristics vs. Frequency (0–50 kHz)

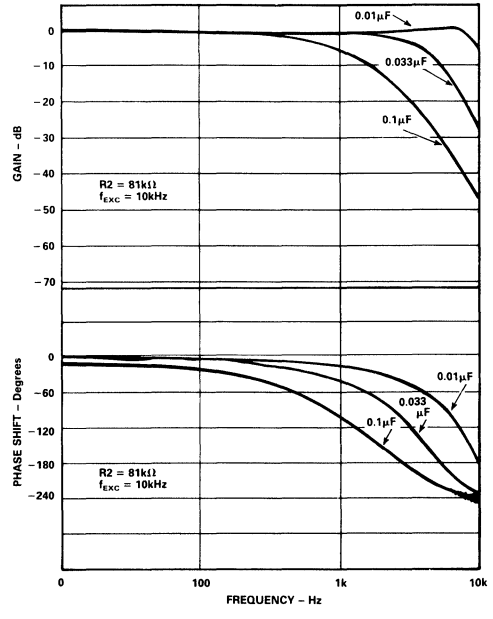


Figure 15. Gain and Phase Characteristics vs. Frequency (0–10 kHz)

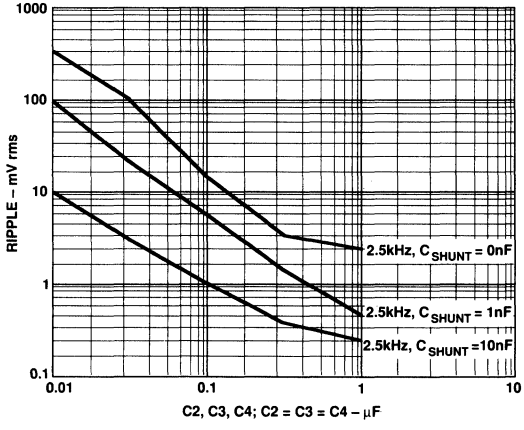


Figure 16. Output Voltage Ripple vs. Filter Capacitance

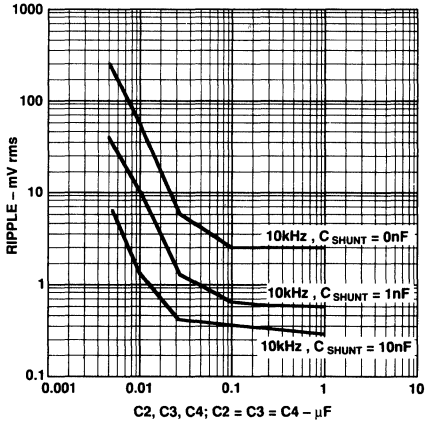


Figure 17. Output Voltage Ripple vs. Filter Capacitance

Determining LVDT Sensitivity

LVDT sensitivity can be determined by measuring the LVDT secondary voltages as a function of primary drive and core position, and performing a simple computation.

Energize the LVDT at its recommended primary drive level, V_{PRI} (3 V rms for the E100). Set the core to midpoint where $V_A = V_B$. Set the core displacement to its mechanical full-scale position and measure secondary voltages V_A and V_B.

$$Sensitivity = \frac{V_A\ (at\ Full\ Scale) - V_B\ (at\ Full\ Scale)}{V_{PRI} \times d}$$

From Figure 18,

$$Sensitivity = \frac{1.71 - 0.99}{3 \times 100\ mils} = 2.4\ mV/V/mil$$

Thermal Shutdown and Loading Considerations.

The AD598 is protected by a thermal overload circuit.If the die temperature reaches 165°C, the sine wave excitation amplitude gradually reduces, thereby lowering the internal power dissipation and temperature.

Due to the ratiometric operation of the decoder circuit, only small errors result from the reduction of the excitation amplitude. Under these conditions the signal-processing section of the AD598 continues to meet its output specifications.

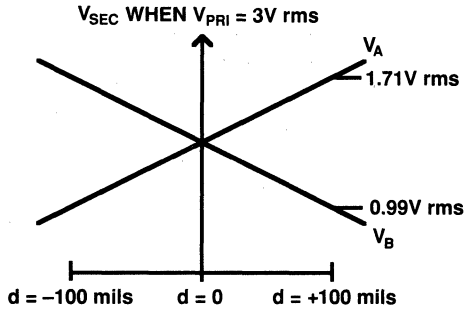


Figure 18. LVDT Secondary Voltage vs. Core Displacement

The thermal load depends upon the voltage and current delivered to the load as well as the power supply potentials. An LVDT Primary will present an inductive load to the sine wave excitation. The phase angle between the excitation voltage and current must also be considered, further complicating thermal calculations.

APPLICATIONS

PROVING RING-WEIGH SCALE

Figure 20 shows an elastic member (steel proving ring) combined with an LVDT to provide a means of measuring very small loads. Figure 19 shows the electrical circuit details.

The advantage of using a Proving Ring in combination with an LVDT is that no friction is involved between the core and the coils of the LVDT. This means that weights can be measured without confusion from frictional forces. This is especially important for very low full-scale weight applications.

Although it is recognized that this type of measurement system may best be applied to weigh very small weights, this circuit was designed to give a full-scale output of 10 V for a 500 lb weight, using a Morehouse Instruments model 5BT Proving Ring. The LVDT is a Schaevitz type HR050 (±50 mil full

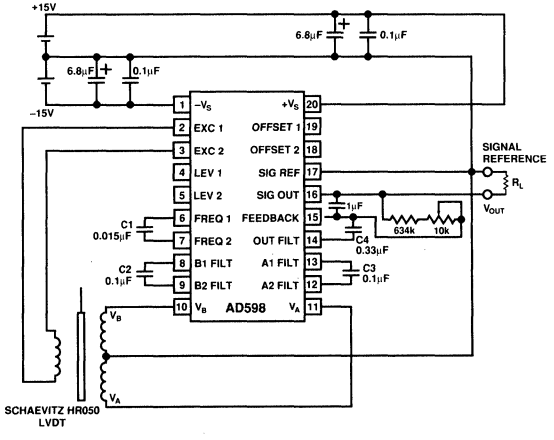


Figure 19. Proving Ring-Weigh Scale Circuit

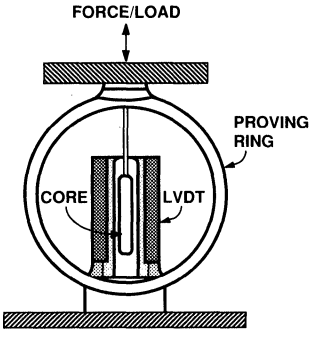


Figure 20. Proving Ring-Weigh Scale Cross Section

scale). Although this LVDT provides ± 50 mil full scale, the value of R2 was calculated for d = ±30 mil and V_{OUT} equal to 10 V as in Step 9 of the design procedures.

The 1 µF capacitor provides extra filtering, which reduces noise induced by mechanical vibrations. The other circuit values were calculated in the usual manner using the design procedures.

This weigh-scale can be designed to measure tare weight simply by putting in an offset voltage by selecting either R3 or R4 (as shown in Figures 7 and 12). Tare weight is the weight of a container that is deducted from the gross weight to obtain the net weight.

The value of R3 or R4 can be calculated using one of two separate methods. First, a potentiometer may be connected between Pins 18 and 19 of the AD598, with the wiper connected to $-V_{SUPPLY}$. This gives a small offset of either polarity; and the value can be calculated using Step 10 of the design procedures. For a large offset in one direction, replace either R3 or R4 with a potentiometer with its wiper connected to $-V_{SUPPLY}$.

The resolution of this weigh-scale was checked by placing a 100 gram weight on the scale and observing the AD598 output signal deflection on an oscilloscope. The deflection was 4.8 mV.

The smallest signal deflection which could be measured on the oscilloscope was 450 μV which corresponds to a 10 gram weight. This 450 μV signal corresponds to an LVDT displacement of 1.32 microinches which is equivalent to one tenth of the wave length of blue light.

The Proving Ring used in this circuit has a temperature coefficient of 250 ppm/°C due to Young's Modulus of steel. By putting a resistor with a temperature coefficient in place of R2 it is possible to temperature compensate the weigh-scale. Since the steel of the Proving Ring gets softer at higher temperatures, the deflection for a given force is larger, so a resistor with a negative temperature coefficient is required.

SYNCHRONOUS OPERATION OF MULTIPLE LVDTS

In many applications, such as multiple gaging measurement, a large number of LVDTs are used in close physical proximity. If these LVDTs are operated at similar carrier frequencies, stray magnetic coupling could cause beat notes to be generated. The resulting beat notes would interfere with the accuracy of measurements made under these conditions. To avoid this situation all the LVDTs are operated synchronously.

The circuit shown in Figure 21 has one master oscillator and any number of slaves. The master AD598 oscillator has its frequency and amplitude programmed in the usual manner via R1 and C2 using Steps 6 and 7 in the design procedures. The slave AD598s all have Pins 6 and 7 connected together to disable their internal oscillators. Pins 4 and 5 of each slave are connected to Pins 2 and 3 of the master via 15 kΩ resistors, thus setting the amplitudes of the slaves equal to the amplitude of the master. If a different amplitude is required the 15 kΩ resistor values should be changed. Note that the amplitude scales linearly with the resistor value.The 15 kΩ value was selected because it matches the nominal value of resistors internal to the circuit. Tolerances of 20% between the slave amplitudes arise due to differing internal resistors values, but this does not affect the operation of the circuit.

Note that each LVDT primary is driven from its own power amplifier and thus the thermal load is shared between the AD598s. There is virtually no limit on the number of slaves in this circuit, since each slave presents a 30 kΩ load to the master AD598 power amplifier. For a very large number of slaves (say 100 or more) one may need to consider the maximum output current drawn from the master AD598 power amplifier.

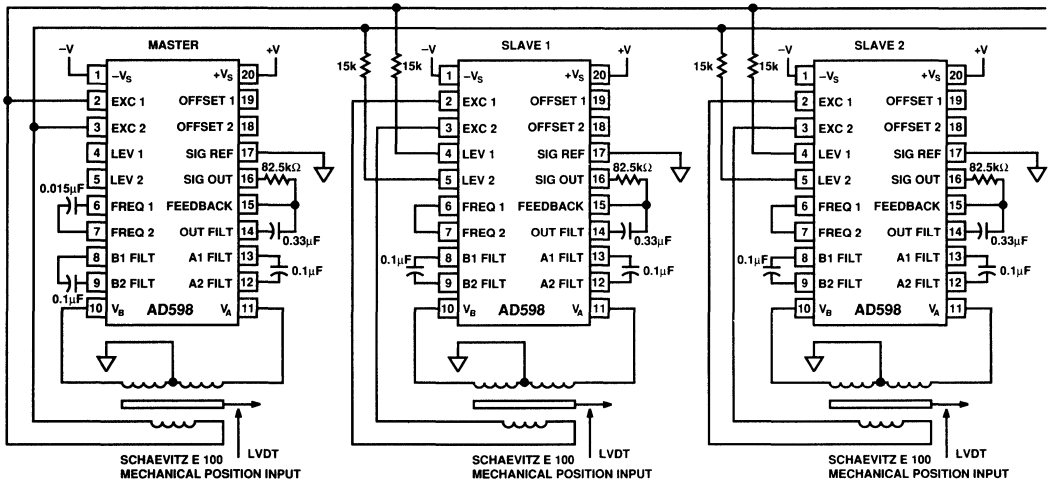


Figure 21. Multiple LVDTs – Synchronous Operation

HIGH RESOLUTION POSITION-TO-FREQUENCY CIRCUIT

In the circuit shown in Figure 22, the AD598 is combined with an AD652 voltage-to-frequency (V/F) converter to produce an effective, simple data converter which can make high resolution measurements.

This circuit transfers the signal from the LVDT to the V/F converter in the form of a current, thus eliminating the errors normally caused by the offset voltage of the V/F converter. The V/F converter offset voltage is normally the largest source of error in such circuits. The analog input signal to the AD652 is converted to digital frequency output pulses which can be counted by simple digital means.

This circuit is particularly useful if there is a large degree of mechanical vibration (hum) on the position to be measured. The hum may be completely rejected by counting the digital frequency pulses over a gate time (fixed period) equal to a multiple of the hum period. For the effects of the hum to be completely rejected, the hum must be a periodic signal.

The V/F converter is currently set up for unipolar operation. The AD652 data sheet explains how to set up for bipolar operation. Note that when the LVDT core is centered, the output frequency is zero. When the LVDT core is positioned off center, and to one side, the frequency increases to a full-scale value. To introduce bipolar operation to this circuit, an offset must be introduced at the LVDT as shown in Step 10 of the design procedures.

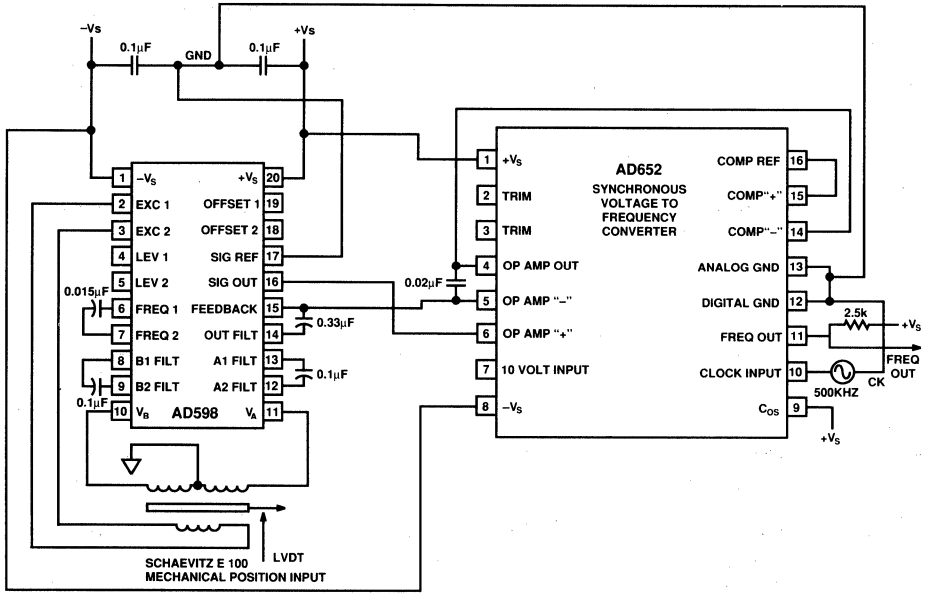


Figure 22. High Resolution Position-to-Frequency Converter

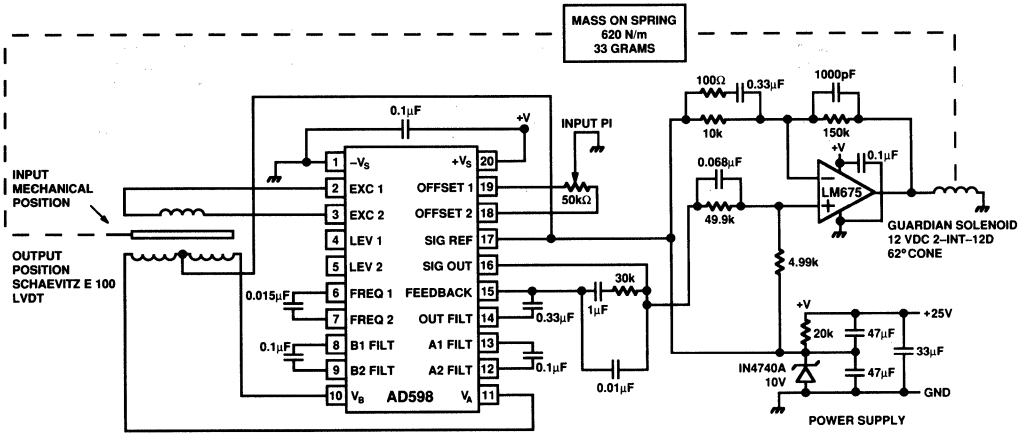


Figure 23. Low Cost Set-Point Controller

LOW COST SET-POINT CONTROLLER

A low cost set-point controller can be implemented with the circuit shown in Figure 23. Such a circuit could possibly be used in automobile fuel control systems. The potentiometer, P1, is attached to the gas pedal, and the LVDT is attached to the butterfly valve of the fuel injection system or carburetor. The position of the butterfly valve is electronically controlled by the position of the gas pedal, without mechanical linkage.

This circuit is a simple two IC closed loop servo-controller. It is simple because the LVDT circuit is functioning as the loop integrator. By putting a capacitor in the feedback path (normally occupied by R2), the output signal from the AD598 corresponds to the time integral of the position being measured by the LVDT. The LVDT position signal is summed with the offset signal introduced by the potentiometer, P1. Since this sum is integrated, it must be forced to zero. Thus the LVDT position is forced to follow the value of the input potentiometer, P1. The output signal from the AD598 drives the LM675 power amplifier, which in turn drives the solenoid.

This circuit has dual advantages of being both low cost and high accuracy. The high accuracy results from avoiding the offset errors normally associated with converting the LVDT signal to a voltage and then subsequently integrating that voltage.

MECHANICAL FOLLOWER SERVO-LOOP

Figure 24 shows how two Schaevitz E100 LVDTs may be combined with two AD598s in a mechanical follower servo-loop configuration. One of the LVDTs provides the mechanical input position signal, while the other LVDT mimics the motion.

The signal from the input position circuit is fed to the output as a current so that voltage offset errors are avoided. This current signal is summed with the signal from the output position LVDT; this summed signal is integrated such that the output position is now equal to the input position. This circuit is an efficient means of implementing a mechanical servo-loop since only three ICs are required.

This circuit is similar to the previous circuit (Figure 23) with one exception: the previous circuit uses a potentiometer instead of an LVDT to provide the input position signal. Replacing the potentiometer with an LVDT offers two advantages. First, the increased reliability and robustness of the LVDT can be exploited in applications where the position input sensor is located in a hostile environment. Second, the mechanical motions of the input and output LVDTs are guaranteed to be identical to within the matching of their individual scale factors. These particular advantages make this circuit ideal for application as a hydraulic actuator controller.

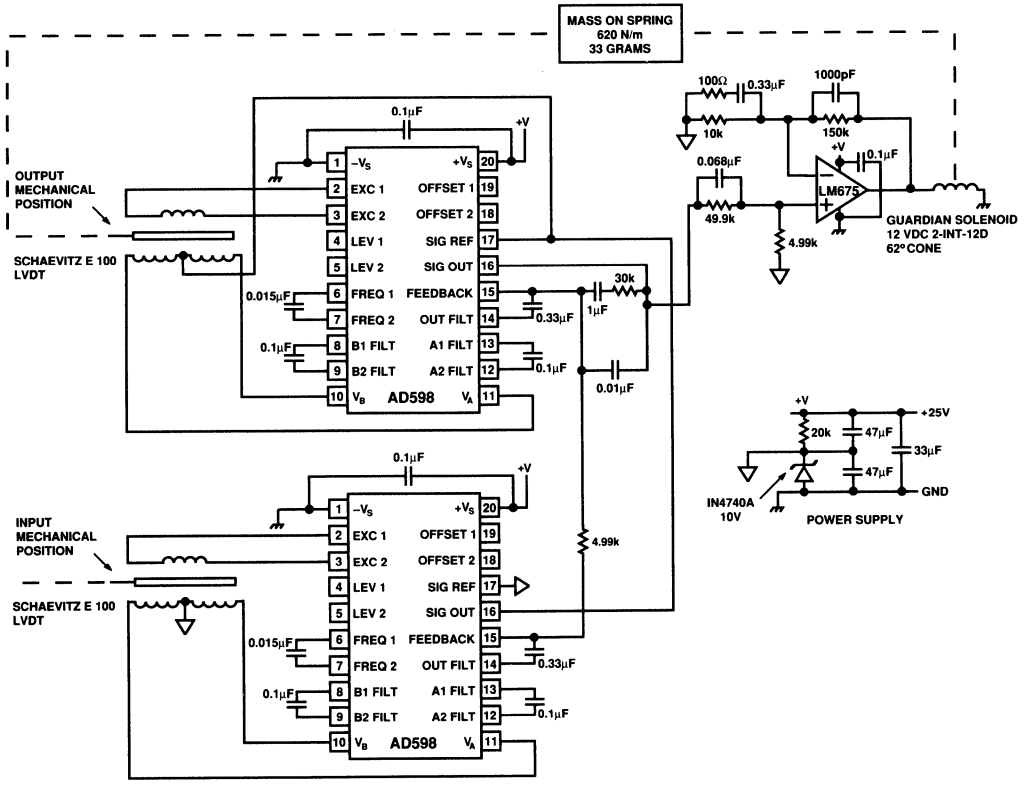


Figure 24. Mechanical Follower Servo-Loop

DIFFERENTIAL GAGING

LVDTs are commonly used in gaging systems. Two LVDTs can be used to measure the thickness or taper of an object. To measure thickness, the LVDTs are placed on either side of the object to be measured. The LVDTs are positioned such that there is a known maximum distance between them in the fully retracted position.

This circuit is both simple and inexpensive. It has the advantage that two LVDTs may be driven from one AD598, but the disadvantage is that the scale factor of each LVDT may not match exactly. This causes the workpiece thickness measurement to vary depending upon its absolute position in the differential gage head.

This circuit was designed to produce a ±10 V signal output swing, composed of the sum of the two independent ±5 V swings from each LVDT. The output voltage swing is set with an 80.9 kΩ resistor. The output voltage Vout for this circuit is given by:

$$V_{OUT} = \left[\frac{(V_A - V_B)}{(V_A + V_B)} + \frac{(V_C - V_D)}{(V_C + V_D)}\right] \times 500\ \mu A \times R2.$$

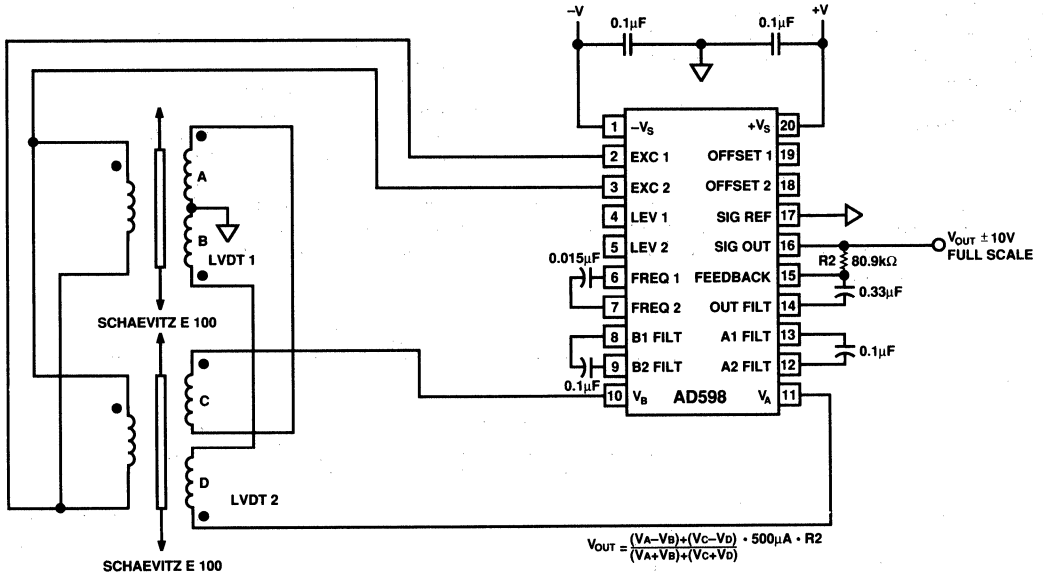


Figure 25. Differential Gaging

PRECISION DIFFERENTIAL GAGING

The circuit shown in Figure 26 is functionally similar to the differential gaging circuit shown in Figure 25. In contrast to Figure 25, it provides a means of independently adjusting the scale factor of each LVDT so that both scale factors may be matched.

The two LVDTs are driven in a master-slave arrangement where the output signal from the slave LVDT is summed with the output signal from the master LVDT. The scale factor of the slave LVDT only is adjusted with R1 and R2. The summed scale factor of the master LVDT and the slave LVDT is adjusted with R3.

R1 and R2 are chosen to be 80.9 kΩ resistors to give a ±10 V full-scale output signal for a single Schaevitz E100 LVDT. R3 is chosen to be 40.2 kΩ to give a ±10 V output signal when the two E100 LVDT output signals are summed. The output voltage for this circuit is given by:

$$V_{OUT} = \left[\frac{(V_A - V_B)}{(V_A + V_B)} + \frac{(V_C - V_D)}{(V_C + V_D)} \times \frac{R2}{R1}\right] \times 500\ \mu A \times R3.$$

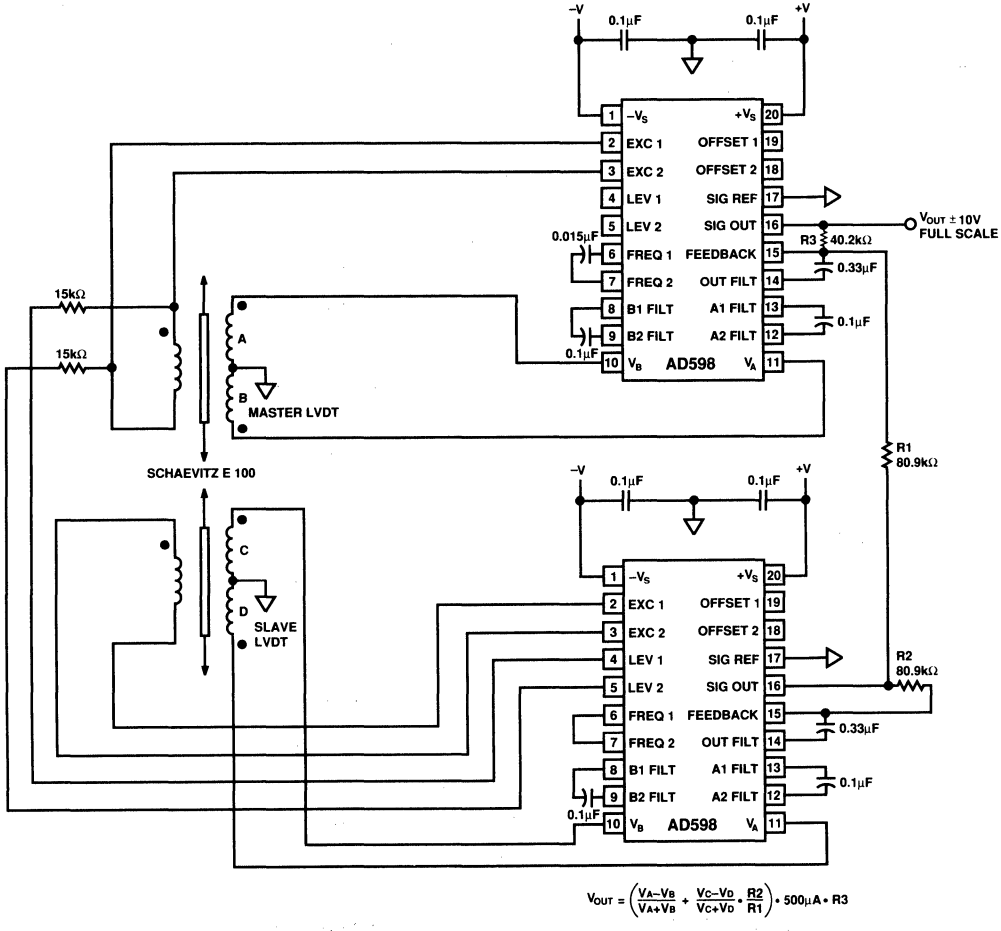


Figure 26. Precision Differential Gaging

OPERATION WITH A HALF-BRIDGE TRANSDUCER

Although the AD598 is not intended for use with a half-bridge type transducer, it may be made to function with degraded performance.

A half-bridge type transducer is a popular transducer. It works in a similar manner to the LVDT in that two coils are wound around a moveable core and the inductance of each coil is a function of core position.

In the circuit shown in Figure 27 the V_A and V_B input voltages are developed as two resistive-inductor dividers. If the inductors are equal (i.e., the core is centered), the V_A and V_B input voltages to the AD598 are equal and the output voltage V_{OUT} is zero. When the core is positioned off center, the inductors are unequal and an output voltage V_{OUT} is developed.

The linearity of this circuit is dependent upon the value of the resistors in the resistive-inductor dividers. The optimum value may be transducer dependent and therefore must be selected by trial and error. The 300 Ω resistors in this circuit optimize the nonlinearity of the transfer function to within several tenths of 1%. This circuit uses a Sangamo AGH1 half-bridge transducer. The 1 μF capacitor blocks the dc offset of the excitation output signal. The 4 nF capacitor sets the transducer excitation frequency to 10 kHz as recommended by the manufacturer.

ALTERNATE HALF-BRIDGE TRANSDUCER CIRCUIT

This circuit suffers from similar accuracy problems to those mentioned in the previous circuit description. In this circuit the V_A input signal to the AD598 really and truly is a linear function of core position, and the input signal V_B, is one half of the excitation voltage level. However, a nonlinearity is introduced by the A−B/A+B transfer function.

The 500 Ω resistors in this circuit are chosen to minimize errors caused by dc bias currents from the V_A and V_B inputs. Note that in the previous circuit these bias currents see very low resistance paths to ground through the coils.

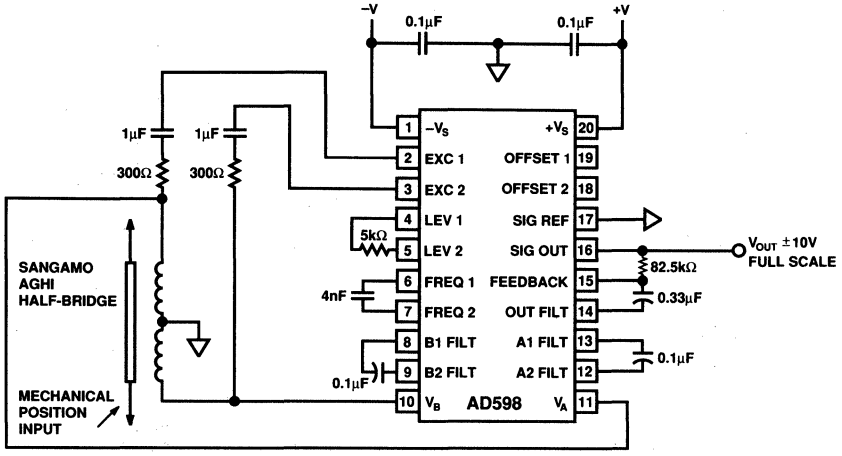


Figure 27. Half-Bridge Operation

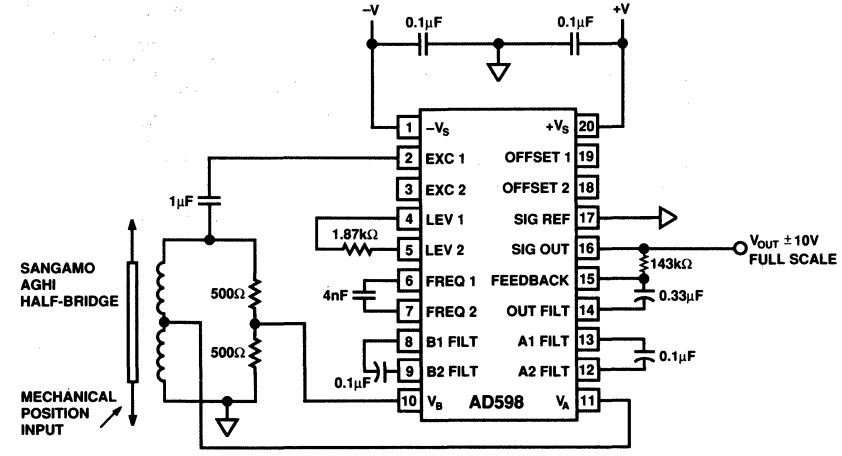


Figure 28. Alternate Half-Bridge Circuit

ANALOG DEVICES

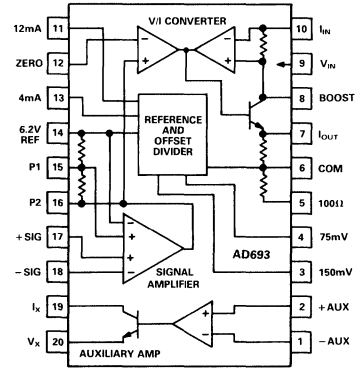
Loop-Powered, 4–20mA Sensor Transmitter

AD693

FEATURES

Instrumentation Amplifier Front End
Loop-Powered Operation
Precalibrated 30mV or 60mV Input Spans
Independently Adjustable Output Span and Zero
Precalibrated Output Spans: 4–20mA Unipolar
0–20mA Unipolar
12 ± 8mA Bipolar
Precalibrated 100Ω RTD Interface
6.2V Reference with Up to 3.5mA of Current Available
Uncommitted Auxiliary Amp for Extra Flexibility
Optional External Pass Transistor to Reduce Self-Heating Errors

AD693 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD693 is a monolithic signal conditioning circuit which accepts low-level inputs from a variety of transducers to control a standard 4-20mA, two-wire current loop. An on-chip voltage reference and auxiliary amplifier are provided for transducer excitation; up to 3.5mA of excitation current is available when the device is operated in the loop-powered mode. Alternatively, the device may be locally powered for three-wire applications when 0-20mA operation is desired.

Precalibrated 30mV and 60mV input spans may be set by simple pin strapping. Other spans from 1mV to 100mV may be realized with the addition of external resistors. The auxiliary amplifier may be used in combination with on-chip voltages to provide six precalibrated ranges for 100Ω RTDs. Output span and zero are also determined by pin strapping to obtain the standard ranges: 4-20mA, 12 ± 8mA and 0-20mA.

Active laser trimming of the AD693's thin-film resistors result in high levels of accuracy without the need for additional adjustments and calibration. Total unadjusted error is tested on every device to be less than 0.5% of full scale at +25°C, and less than 0.75% over the industrial temperature range. Residual nonlinearity is under 0.05%. The AD693 also allows for the use of an external pass transistor to further reduce errors caused by self-heating.

For transmission of low-level signals from RTDs, bridges and pressure transducers, the AD693 offers a cost-effective signal conditioning solution. It is recommended as a replacement for discrete designs in a variety of applications in process control, factory automation and system monitoring.

The AD693 is packaged in an 20-pin ceramic side-brazed DIP and is specified over the −40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD693 is a complete monolithic low-level voltage-to-current loop signal conditioner.
2. Precalibrated output zero and span options include 4-20mA, 0-20mA, and 12 ± 8mA in two- and three-wire configurations.
3. Simple resistor programming adds a continuum of ranges to the basic 30mV and 60mV input spans.
4. The common-mode range of the signal amplifier input extends from ground to near the device's operating voltage.
5. Provision for transducer excitation includes a 6.2V reference output and an auxiliary amplifier which may be configured for voltage or current output and signal amplification.
6. The circuit configuration permits simple linearization of bridge, RTD, and other transducer signals.
7. A monitored output is provided to drive an external pass transistor. This feature off-loads power dissipation to extend the temperature range of operation, enhance reliability, and minimize self-heating errors.
8. Laser-wafer trimming results in low unadjusted errors and affords precalibrated input and output spans.
9. Zero and span are independently adjustable and noninteractive to accommodate transducers or user defined ranges.
10. Six precalibrated temperature ranges are available with a 100Ω RTD via pin strapping.

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SPECIFICATIONS (@ +25°C and V_S = +24V, Input Span = 30mV or 60mV, Output Span = 4-20mA, R_L = 250Ω, V_{CM} = 3.1V, with external pass transistor unless otherwise specified)

Model	Conditions	AD693AD Min	Typ	Max	Units
LOOP-POWERED OPERATION					
TOTAL UNADJUSTED ERROR[1,2]			±0.25	**±0.5**	% Full Scale
T_{min} to T_{max}			±0.4	**±0,75**	% Full Scale
100Ω RTD CALIBRATION ERROR[3]	(See Fig. 17)		±0.5	±2.0	°C
LOOP POWERED OPERATION[2]					
Zero Current Error[4]	Zero = 4mA		±25	**±80**	μA
	Zero = 12mA		±40	**±120**	μA
	Zero = 0mA[5]	+7	+35	**+100**	μA
vs. Temp.	Zero = 4mA		±0.5	±1.5	μA/°C
Power Supply Rejection (RTI)	12V ≤ V_{OP} ≤ 36V[6]		±3.0	**±5.6**	μV/V
	0V ≤ V_{CM} ≤ 6.2V				
Common-Mode Input Range	(See Fig. 3)	0		$+V_{OP}-4V$[6]	V
Common-Mode Rejection (RTI)	0V ≤ V_{CM} ≤ 6.2V		±10	**±30**	μV/V
Input Bias Current[7]			+5	**+20**	nA
T_{min} to T_{max}			+7	**+25**	nA
Input Offset Current[7]	V_{SIG} = 0		±0.5	**±3.0**	nA
Transconductance					
Nominal	30mV Input Span		0.5333		A/V
	60mV Input Span		0.2666		A/V
Unadjusted Error			±0.05	**±0.2**	%
vs. Common-Mode	0V ≤ V_{CM} ≤ 6.2V				
	30mV Input Span		±0.03	±0.04	%/V
	60mV Input Span		±0.05	±0.06	%/V
Error vs. Temp.			±20	±50	ppm/°C
Nonlinearity[8]	30mV Input Span		±0.01	**±0.05**	% of Span
	60mV Input Span		±0.02	**±0.07**	% of Span
OPERATIONAL VOLTAGE RANGE					
Operational Voltage, V_{OP}[6]		**+12**		**+36**	V
Quiescent Current	Into Pin 9		+500	**+700**	μA
OUTPUT CURRENT LIMIT		**+21**	+25	**+32**	mA
COMPONENTS OF ERROR					
SIGNAL AMPLIFIER[9]					
Input Voltage Offset			±40	**±200**	μV
vs. Temp			±1.0	±2.5	μV/°C
Power Supply Rejection	12V ≤ V_{OP} ≤ 36V[6]		±3.0	**±5.6**	μV/V
	0V ≤ V_{CM} ≤ 6.2V				
V/I CONVERTER[9,10]					
Zero Current Error	Output Span = 4-20mA		±30	±80	μA
Power Supply Rejection	12V ≤ V_{OP} ≤ 36V[6]		±1.0	±3.0	μA/V
Transconductance					
Nominal			0.2666		A/V
Unadjusted Error			±0.05	±0.2	%
6.200V REFERENCE[9,12]					
Output Voltage Tolerance			±3	**±12**	mV
vs. Temp.			±20	±50	ppm/°C
Line Regulation	12V ≤ V_{OP} ≤ 36V[6]		±200	**±300**	μV/V
Load Regulation[11]	0mA ≤ I_{REF} ≤ 3mA		±0.3	**±0.75**	mV/mA
Output Current[13]	Loop Powered, (Fig. 10)	**+3.0**	+3.5		mA
	3-Wire Mode, (Fig. 15)		+5.0		mA
AUXILIARY AMPLIFIER					
Common-Mode Range		0		$+V_{OP}-4V$[6]	V
Input Offset Voltage			±50	±200	μV
Input Bias Current			+5	+20	nA
Input Offset Current			+0.5	±3.0	nA
Common-Mode Rejection			90		dB
Power Supply Rejection			105		dB

Model	Conditions	AD693AD Min	Typ	Max	Units
Output Current Range	Pin I_X OUT	+0.01		+5	mA
Output Current Error	Pin V_X – Pin I_X		±0.005		%
TEMPERATURE RANGE					
Case Operating[14]	T_{min} to T_{max}	–40		+85	°C
Storage		–65		+150	°C
PACKAGE OPTION[15]			D-20		

NOTES

[1]Total error can be significantly reduced (typically less than 0.1%) by trimming the zero current. The remaining unadjusted error sources are transconductance and nonlinearity.

[2]The AD693 is tested as a loop powered device with the signal amp, V/I converter, voltage reference, and application voltages operating together. Specifications are valid for preset spans and spans between 30mV and 60mV.

[3]Error from ideal output assuming a perfect 100Ω RTD at 0 and +100°C.

[4]Refer to the Error Analysis to calculate zero current error for input spans less than 30mV.

[5]By forcing the differential signal amplifier input sufficiently negative the 7μA zero current can always be achieved.

[6]The operational voltage (V_{OP}) is the voltage directly across the AD693 (Pin 10 to 6 in two-wire mode, Pin 9 to 6 in local power mode). For example, $V_{OP} = V_S - (I_{LOOP} \times R_L)$ in two-wire mode (refer to Figure 10).

[7]Bias currents are not symmetrical with input signal level and flow out of the input pins. The input bias current of the inverting input increases with input signal voltage, see Figure 2.

[8]Nonlinearity is defined as the deviation of the output from a straight line connecting the endpoints as the input is swept over a 30mV and 60mV input span.

[9]Specifications for the individual functional blocks are components of error that contribute to, and that are included in, the Loop Powered Operation specifications.

[10]Includes error contributions of V/I converter and Application Voltages.

[11]Changes in the reference output voltage due to load will affect the Zero Current. A 1% change in the voltage reference output will result in an error of 1% in the value of the Zero Current.

[12]If not used for external excitation, the reference should be loaded by approximately 1mA (6.2kΩ to common).

[13]In the loop powered mode up to 5mA can be drawn from the reference, however, the lower limit of the output span will be increased accordingly. 3.5mA is the maximum current the reference can source while still maintaining a 4mA zero.

[14]The AD693 is tested with a pass transistor so $T_A \cong T_C$.

[15]See Section 20 for package outline information.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+36V
Reverse Loop Current	200mA
Signal Amp Input Range	–0.3V to V_{OP}
Reference Short Circuit to Common	Indefinite
Auxiliary Amp Input Voltage Range	–0.3V to V_{OP}
Auxiliary Amp Current Output	10mA
Storage Temperature	–65°C to +150°C
Lead Temperature, 10sec Soldering	+300°C
Max Junction Temperature	+150°C

Typical Characteristics

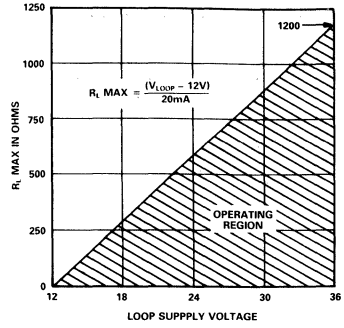


Figure 1. Maximum Load Resistance vs. Power Supply

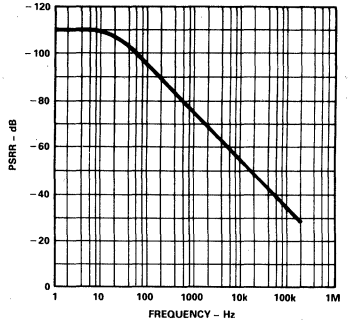


Figure 5. Signal Amplifier PSRR vs. Frequency

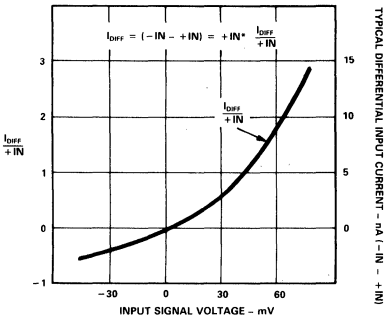


Figure 2. Differential Input Current vs. Input Signal Voltage Normalized to +IN

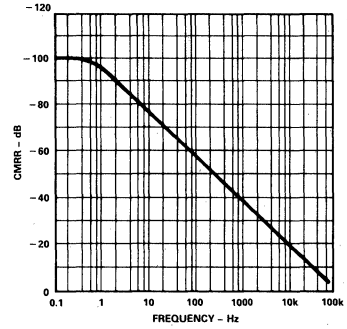


Figure 6. CMRR (RTI) vs. Frequency

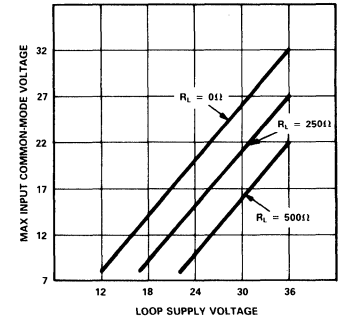


Figure 3. Maximum Common-Mode Voltage vs. Supply

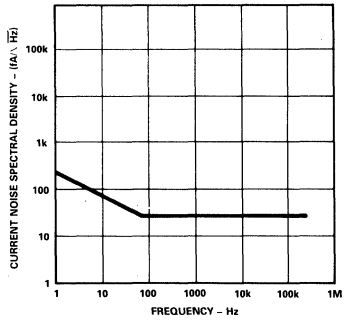


Figure 7. Input Current Noise vs. Frequency

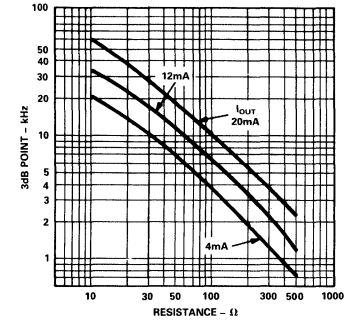


Figure 4. Bandwidth vs. Series Load Resistance

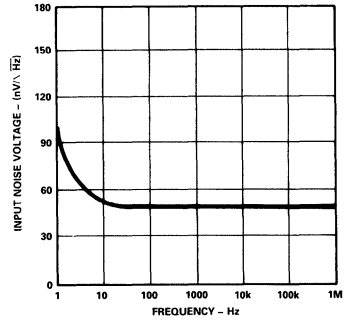


Figure 8. Input Voltage Noise vs. Frequency

FUNCTIONAL DESCRIPTION

The operation of the AD693 can be understood by dividing the circuit into three functional parts (see Figure 9). First, an instrumentation amplifier front-end buffers and scales the low-level input signal. This amplifier drives the second section, a V/I converter, which provides the 4-to-20mA loop current. The third section, a voltage reference and resistance divider, provides application voltages for setting the various "live zero" currents. In addition to these three main sections, there is an on-chip auxiliary amplifier which can be used for transducer excitation.

VOLTAGE-TO-CURRENT (V/I) CONVERTER

The output NPN transistor for the V/I section sinks loop current when driven on by a high gain amplifier at its base. The input for this amplifier is derived from the difference in the outputs of the matched preamplifiers having gains, G2. This difference is caused to be small by the large gain, +A, and the negative feedback through the NPN transistor and the loop current sampling resistor between I_{IN} and Boost. The signal across this resistor is compared to the input of the left preamp and servos the loop current until both signals are equal. Accurate voltage-to-current transformation is thereby assured. The preamplifiers employ a special design which allows the active feedback amplifier to operate from the most positive point in the circuit, I_{IN}.

The V/I stage is designed to have a nominal transconductance of 0.2666 A/V. Thus, a 75mV signal applied to the inputs of the V/I (Pin 16, noninverting; Pin 12, inverting) results in a full-scale output current of 20mA.

The current limiter operates as follows: the output of the feedback preamp is an accurate indication of the loop current. This output is compared to an internal setpoint which backs off the drive to the NPN transistor when the loop current approaches 25mA. As a result, the loop and the AD693 are protected from the consequences of voltage overdrive at the V/I input.

VOLTAGE REFERENCE AND DIVIDER

A stabilized bandgap voltage reference and laser-trimmed resistor divider provide for both transducer excitation as well as precalibrated offsets for the V/I converter. When not used for external excitation, the reference should be loaded by approximately 1mA (6.2kΩ to common).

The 4mA and 12mA taps on the resistor divider correspond to −15mV and −45mV, respectively, and result in a live zero of 4mA or 12mA of loop current when connected to the V/I converter's inverting input (Pin 12). Arranging the zero offset in this way makes the zero signal output current independent of input span. When the input to the signal amp is zero, the noninverting input of the V/I is at 6.2V.

Since the standard offsets are laser trimmed at the factory, adjustment is seldom necessary except to accommodate the zero offset of the actual source. (See "Adjusting Zero".)

SIGNAL AMPLIFIER

The Signal Amplifier is an instrumentation amplifier used to buffer and scale the input to match the desired span. Inputs applied to the Signal Amplifier (at Pins 17 and 18) are amplified and referred to the 6.2V reference output in much the same way as the level translation occurs in the V/I converter. Signals from the two preamplifiers are subtracted, the difference is amplified, and the result is fed back to the upper preamp to minimize the difference. Since the two preamps are identical, this minimum will occur when the voltage at the upper preamp just matches the differential input applied to the Signal Amplifier at the left.

Since the signal which is applied to the V/I is attenuated across the two 800Ω resistors before driving the upper preamp, it will necessarily be an amplified version of the signal applied between Pins 17 and 18. By changing this attenuation, you can control the span referred to the Signal Amplifier. To illustrate: a 75mV signal applied to the V/I results in a 20mA loop current. Nominally, 15mV is applied to offset the zero to 4mA leaving a 60mV range to correspond to the span. And, since the nominal attenuation of the resistors connected to Pins 16, 15 and 14 is 2.00, a 30mV input signal will be doubled to result in 20mA of loop current. Shorting Pins 15 and 16 results in unity gain and permits a 60mV input span. Other choices of span may be implemented with user supplied resistors to modify the attenuation. (See section "Adjusting Input Span".)

The Signal Amplifier is specially designed to accommodate a large common-mode range. Common-mode signals anywhere up to and beyond the 6.2V reference are easily handled as long as V_{IN} is sufficiently positive. The Signal Amplifier is biased with respect to V_{IN} and requires about 3.5 volts of headroom. The extended range will be useful when measuring sensors driven, for example, by the auxiliary amplifier which may go above the 6.2V potential. In addition, the PNP input stage will continue to operate normally with common-mode voltages of several hundred mV, negative, with respect to common. This feature accommodates self-generating sensors, such as thermocouples,

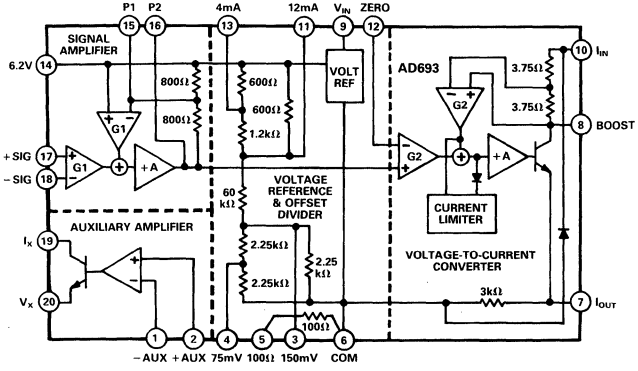


Figure 9. Functional Block Diagram

which may produce small negative normal-mode signals as well as common-mode noise on "grounded" signal sources.

AUXILIARY AMPLIFIER

The Auxiliary Amplifier is included in the AD693 as a signal conditioning aid. It can be used as an op amp in noninverting applications and has special provisions to provide a controlled current output. Designed with a differential input stage and an unbiased Class A output stage, the amplifier can be resistively loaded to common with the self-contained 100Ω resistor or with a user supplied resistor.

As a functional element, the Auxiliary Amplifier can be used in dynamic bridges and arrangements such as the RTD signal conditioner shown in Figure 17. It can be used to buffer, amplify and combine other signals with the main Signal Amplifier. The Auxiliary Amplifier can also provide other voltages for excitation if the 6.2V of the reference is unsuitable. Configured as a simple follower, it can be driven from a user supplied voltage divider or the precalibrated outputs of the AD693 divider (Pins 3 and 4) to provide a stiff voltage output at less than the 6.2 level, or by incorporating a voltage divider as feedback around the amplifier, one can gain-up the reference to levels higher than 6.2V. If large positive outputs are desired, I_X, the Auxiliary Amplifier output current supply, should be strapped to either V_{IN} or Boost. Like the Signal Amplifier, the Auxiliary requires about 3.5V of headroom with respect to V_{IN} at its input and about 2V of difference between I_X and the voltage to which V_X is required to swing.

The output stage of the Auxiliary Amplifier is actually a high gain Darlington transistor where I_X is the collector and V_X is the emitter. Thus, the Auxiliary Amplifier can be used as a V/I converter when configured as a follower and resistively loaded. I_X functions as a high-impedance current source whose current is equal to the voltage at V_X divided by the load resistance. For example, using the onboard 100Ω resistor and the 75mV or 150mV application voltages, either a 750μA or 1.5mA current source can be set up for transducer excitation.

The I_X terminal has voltage compliance within 2V of V_X. If the Auxiliary Amplifier is not to be used, then Pin 2, the noninverting input, should be grounded.

REVERSE VOLTAGE PROTECTION FEATURE

In the event of a reverse voltage being applied to the AD693 through a current-limited loop (limited to 200mA), an internal shunt diode protects the device from damage. This protection mode avoids the compliance voltage penalty which results from a series diode that must be added if reversal protection is required in high-current loops.

Applying the AD693

CONNECTIONS FOR BASIC OPERATION

Figure 10 shows the minimal connections for basic operation: 0-30mV input span, 4-20mA output span in the two-wire, loop-powered mode. If not used for external excitation, the 6.2V reference should be loaded by approximately 1mA (6.2kΩ to common).

USING AN EXTERNAL PASS TRANSISTOR

The emitter of the NPN output section, I_{OUT}, of the AD693 is usually connected to common and the negative loop connection (Pins 7 to 6). Provision has been made to reconnect I_{OUT} to the base of a user supplied NPN transistor as shown in Figure 11. This permits the majority of the power dissipation to be moved off chip to enhance performance, improve reliability, and extend the operating temperature range. An internal hold-down resistor of about 3k is connected across the base emitter of the external transistor.

The external pass transistor selected should have a BV_{CEO} greater than the intended supply voltage with a sufficient power rating for continuous operation with 25mA current at the supply voltage. Ft should be in the 10MHz to 100MHz range and β should be greater than 10 at a 20mA emitter current. Some transistors that meet this criteria are the 2N1711 and 2N2219A. Heat sinking the external pass transistor is suggested.

The pass transistor option may also be employed for other applications as well. For example, I_{OUT} can be used to drive an LED connected to Common, thus providing a local monitor of loop fault conditions without reducing the minimum compliance voltage.

ADJUSTING ZERO

In general, the desired zero offset value is obtained by connecting an appropriate tap of the precision reference/voltage divider network to the inverting terminal of the V/I converter. As shown in Figure 9, precalibrated taps at Pins 14, 13 and 11 result in zero offsets of 0mA, 4mA and 12mA, respectively, when connected to Pin 12. The voltages which set the 4mA and 12mA zero operating points are 15mV and 45mV negative with respect to

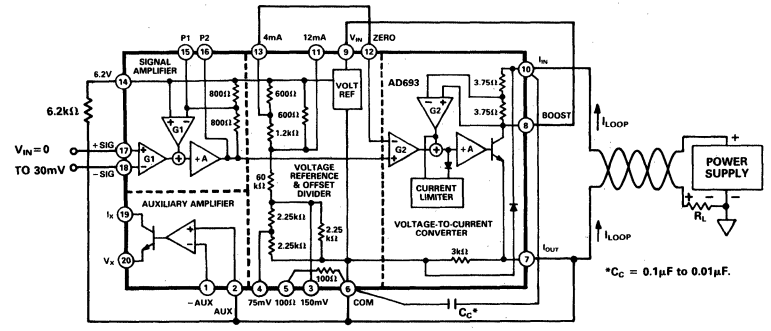


Figure 10. Minimal Connection for 0–30mV Unipolar Input, 4–20mA Output

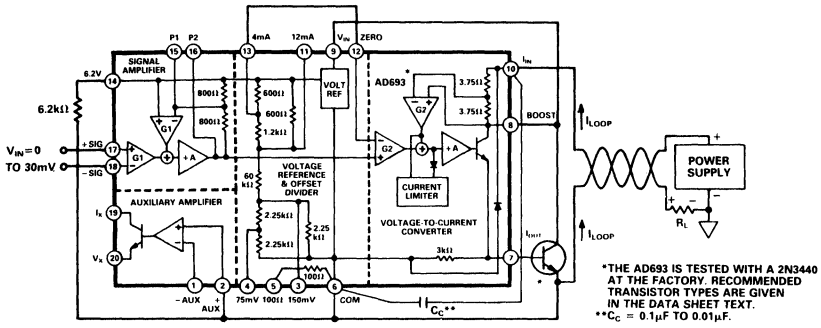


Figure 11. Using an External Pass Transistor to Minimize Self-Heating Errors

6.2V, and they each have a nominal source resistance of 450Ω. While these voltages are laser trimmed to high accuracy, they may require some adjustment to accommodate variability between sensors or to provide additional ranges. You can adjust zero by pulling up or down on the selected zero tap, or by making a separate voltage divider to drive the zero pin.

The arrangement of Figure 12 will give an approximately linear adjustment of the precalibrated options with fixed limits. To find the proper resistor values, first select I_A, the desired range of adjustment of the output current from nominal. Substitute this value in the appropriate formula below for adjustment at the 4mA tap.

$R_{Z1} = (1.6V/I_A) - 400\Omega$ and

$R_{Z2} = R_{Z1} \times 3.1V/(15mV + I_A \times 3.75\Omega)$

Use a similar connection with the following resistances for adjustments at the 12mA tap.

$R_{Z1} = (4.8V/I_A) - 400\Omega$ and

$R_{Z2} = R_{Z1} \times 3.1V/(45mV + I_A \times 3.75\Omega)$

These formulae take into account the ±10% tolerance of tap resistance and insure a minimum adjustment range of I_A. For example, choosing I_A = 200μA will give a zero adjustment range of ±1% of the 20mA full-scale output. At the 4mA tap the maximum value of:

$R_{Z1} = 1.6V/200\mu A - 400\Omega = 7.6k\Omega$ and

$R_{Z2} = 7.6k\Omega \times 3.1V/(15mV + 200\mu A \times 3.75\Omega) = 1.49M\Omega$

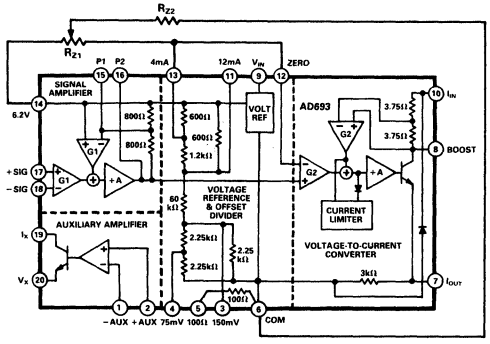


Figure 12. Optional 4mA Zero Adjustment (12mA Trim Available Also)

These can be rounded down to more convenient values of 7.5kΩ and 1.3MΩ, which will result in an adjustment range comfortably greater than ±200μA.

ADJUSTING INPUT SPAN

Input Span is adjusted by changing the gain of the Signal Amplifier. This amplifier provides a 0-to-60mV signal to the V/I section to produce the 4-to-20mA output span (or a 0-to-75mV signal in the 0-to-20mA mode). The gain of this amplifier is trimmed to 2.00 so that an input signal ranging from 0-to-30mV will drive the V/I section to produce 4-to-20mA. Joining P1 and P2 (Pins 15 and 16) will reduce the Signal Amplifier gain to one, thereby requiring a 60mV signal to drive the V/I to a full 20mA span.

To produce spans less than 30mV, an external resistor, R_{S1}, can be connected between P1 and 6.2V. The nominal value is given by:

$$R_{S1} = \frac{400\Omega}{\frac{30mV}{S} - 1}$$

where S is the desired span. For example, to change the span to 6mV a value of:

$$R_{S1} = \frac{400\Omega}{\frac{30mV}{6mV} - 1} = 100\Omega$$

is required. Since the internal, 800Ω gain setting resistors exhibit an absolute tolerance of 10%, R_{S1} should be provided with up to ±10% range of adjustment if the span must be well controlled.

For spans between 30mV and 60mV a resistor R_{S2} should be connected between P1 and P2. The nominal value is given by:

$$R_{S2} = \frac{400\Omega\,(1 - \frac{60mV}{S})}{\frac{30mV}{S} - 1}$$

For example, to change the span to 40mV, a value of:

$$R_{S2} = \frac{400\Omega\,(1 - \frac{60mV}{40mV})}{\frac{30mV}{40mV} - 1} = 800\Omega$$

is required. Remember that this is a nominal value and may require adjustment up to ±10%. In many applications the span must be adjusted to accommodate *individual* variations in the sensor as well as the AD693. The span changing resistor should, therefore, include enough adjustment range to handle both the

sensor uncertainty and the absolute resistance tolerance of P1 and P2. Note that the temperature coefficient of the internal resistors is nominally −17ppm/°C, and that the external resistors should be comparably stable to insure good temperature performance.

An alternative arrangement, allowing wide range span adjustment between two set ranges, is shown in Figure 13. R_{S1} and R_{S2} are calculated to be 90% of the values determined from the previous formulae. The smallest value is then placed in series with the wiper of the 1.5kΩ potentiometer shown in the figure. For example, to adjust the span between 25mV and 40mV, R_{S1} and R_{S2} are calculated to be 2000Ω and 800Ω, respectively. The smaller value, 800Ω, is then reduced by 10% to cover the possible ranges of resistance in the AD693 and that value is put in place.

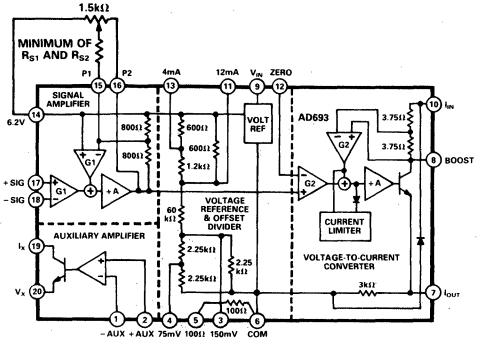


Figure 13. Wide Range Span Adjustment

A number of other arrangements can be used to set the span as long as they are compatible with the pretrimmed noninverting gain of two. The span adjustment can even include thermistors or other sensitive elements to compensate the span of a sensor.

In devising your own adjustment scheme, remember that you should adjust the gain such that the desired span voltage at the Signal Amplifier input translates to 60mV at the output. Note also that the full differential voltage applied to the V/I converter is 75mV; in the 4-20mA mode, −15mV is applied to the inverting input (zero pin) by the Divider Network and +60mV is applied to the noninverting input by the Signal Amplifier. In the 0-to-20mA mode, the total 75mV must be applied by the Signal Amplifier. As a result, the total span voltage will be 25% larger than that calculated for a 4-20mA output.

Finally, the external resistance from P2 to 6.2V should not be made less than 1kΩ unless the voltage reference is loaded to at least 1.0mA. (A simple load resistor can be used to meet this requirement if a low value potentiometer is desired.) In no case should the resistance from P2 to 6.2V be less than 200Ω.

Input Spans Between 60 and 100mV

Input spans of up to 100mV can be obtained by adding an offset proportional to the output signal into the zero pin of the V/I converter. This can be accomplished with two resistors and adjusted via the optional trim scheme shown in Figure 14. The resistor divider formed by R_{E1} and R_{E2} from the output of the Signal Amplifier modifies the differential input voltage range applied to the V/I converter.

In order to determine the fixed resistor values, R_{E1} and R_{E2}, first measure the source resistance (R_D) of the internal divider network. This can be accomplished (power supply disconnected) by measuring the resistance between the 4mA of offset (Pin 13) and common (Pin 6) with the 6.2V reference (Pin 14) connected to common. The measured value, R_D, is then used to calculate R_{E1} and R_{E2} via the following formula:

$$R_{E2} = R_D\left(\frac{S}{S - 60mV} - 1.0024\right)$$

and $R_{E1} = 412R_{E2}$

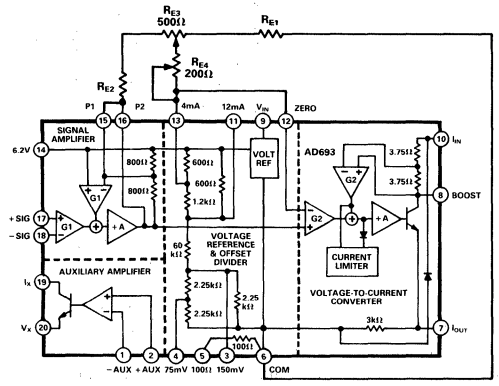


Figure 14. Adjusting for Spans between 60mV and 100mV (R_{E1} and R_{E2}) with Fine-Scale Adjust (R_{E3} and R_{E4})

Figure 14 shows a scheme for adjusting the modified span and 4mA offset via R_{E3} and R_{E4}. The trim procedure is to first connect both signal inputs to the 6.2V Reference, set R_{E4} to zero and then adjust R_{E3} so that 4mA flows in the current loop. This in effect, creates a divider with the same ratio as the internal divider that sets the 4mA zero level (−15mV with respect to 6.2V). As long as the input signal remains zero the voltage at Pin 12, the zero adjust, will remain at −15mV with respect to 6.2V.

After adjusting R_{E3} place the desired full scale (S) across the signal inputs and adjust R_{E4} so that 20mA flows in the current loop. An attenuated portion of the input signal is now added into the V/I zero to maintain the 75mV maximum differential. If there is some small offset at the input to the Signal Amplifier, it may be necessary to repeat the two adjustments.

LOCAL-POWERED OPERATION FOR 0-20mA OUTPUT

The AD693 is designed for local-powered, three-wire systems as well as two-wire loops. All its usual ranges are available in three-wire operation, and in addition, the 0-to-20mA range can be used. The 0-20mA convention offers slightly more resolution and may simplify the loop receiver, two reasons why it is sometimes preferred.

The arrangement, illustrated in Figure 15, results in a 0-20mA transmitter where the precalibrated span is 37.5mV. Connecting P1 to P2 will double the span to 75mV. Sensor input and excitation is unchanged from the two-wire mode except for the 25% increase in span. Many sensors are ratiometric so that an increase in excitation can be used instead of a span adjustment.

In the local-powered mode, increases in excitation are made easier. Voltage compliance at the I_{IN} terminal is also improved; the loop voltage may be permitted to fall to 6 volts at the AD693, easing the trade-off between loop voltage and loop resistance. Note that the load resistor, R_L, should meter the current into Pin 10, I_{IN}, so as not to confuse the loop current with the local power supply current.

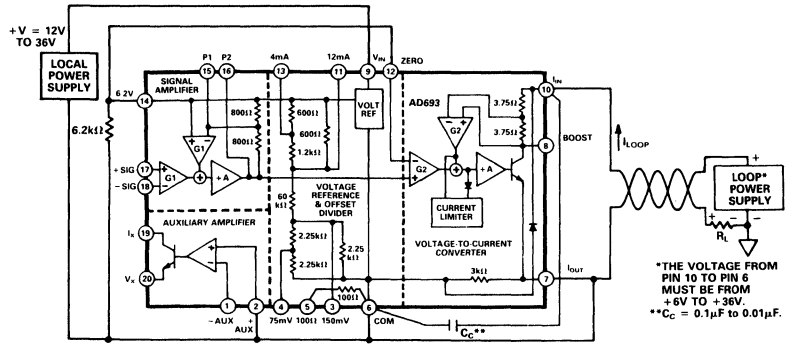


Figure 15. Local Powered Operation with 0–20mA Output

OPTIONAL INPUT FILTERING

Input filtering is recommended for all applications of the AD693 due to its low input signal range. An RC filter network at each input of the signal amplifier is sufficient, as shown in Figure 16. In the case of a resistive signal source it may be necessary only to add the capacitors, as shown in Figure 18. The capacitors should be placed as close to the AD693 as possible. The value of the filter resistors should be kept low to minimize errors due to input bias current. Choose the 3dB point of the filter high enough so as not to compromise the bandwidth of the desired signal. The RC time constant of the filter should be matched to preserve the ac common-mode rejection.

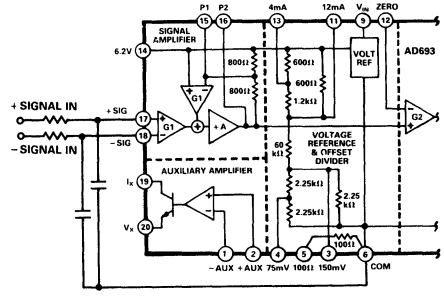


Figure 16. Optional Input Filtering

INTERFACING PLATINUM RTDs

The AD693 has been specially configured to accept inputs from 100Ω Platinum RTDs (Resistance Temperature Detectors). Referring to Figure 17, the RTD and the temperature stable 100Ω resistor form a feedback network around the Auxiliary Amplifier resulting in a noninverting gain of $(1+R_T/100\Omega)$, where R_T is the temperature dependent resistance of the RTD. The noninverting input of the Auxiliary Amplifier (Pin 2) is then driven by the 75mV signal from the Voltage Divider (Pin 4). When the RTD is at 0, its 100Ω resistance results in an amplifier gain of +2 causing V_X to be 150mV. The Signal Amplifier compares this voltage to the 150mV output (Pin 3) so that zero differential signal results. As the temperature (and therefore, the resistance) of the RTD increases, V_X will likewise increase according to the gain relationship. The difference between this voltage and the zero degree value of 150mV drives the Signal Amp to modulate the loop current. The AD693 is pre-calibrated such that the full 4-20mA output span corresponds to a 0 to 104°C range in the RTD. (This assumes the European Standard of $\alpha = 0.00385$.) A total of 6 precalibrated ranges for three-wire (or two-wire) RTDs are available using only the pin strapping options as shown in Table I.

A variety of other temperature ranges can be realized by using different application voltages. For example, loading the Voltage Divider with a 1.5kΩ resistor from Pin 3 to Pin 6 (common) will approximately halve the original application voltages and

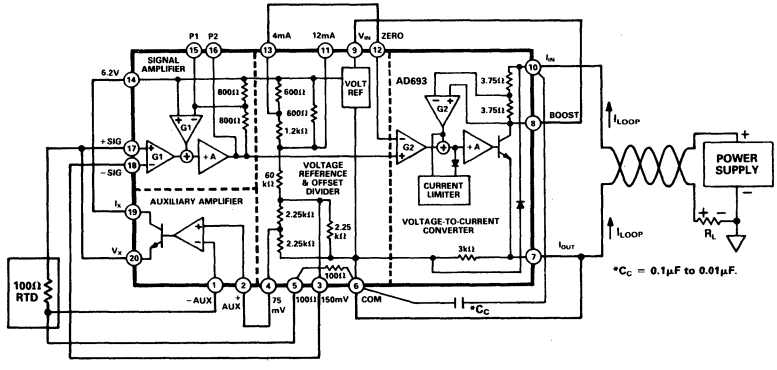


Figure 17. 0-to-104 C Direct Three-Wire 100Ω RTD Interface, 4–20mA Output

Temperature Range	Pin Connections
0 to +104°C	12 to 13
0 to +211°C	12 to 13, and 15 to 16
+25°C to +130°C	12 to 14
+51°C to +266°C	12 to 14, and 15 to 16
−50°C to +51°C	12 to 11
−100°C to +104°C	12 to 11 and 15 to 16

Table I. Precalibrated Temperature Range Options Using a European Standard 100Ω RTD and the AD693

allow for a doubling of the range of resistance (and therefore, temperature) required to fill the two standard spans. Likewise, increasing the application voltages by adding resistance between Pins 14 and 3 will decrease the temperature span.

An external voltage divider may also be used in conjunction with the circuit shown to produce any range of temperature spans as well as providing zero output (4mA) for a non 0 temperature input. For example, measuring V_X with respect to a voltage 2.385 times the excitation (rather than 2 times) will result in zero input to the Signal Amplifier when the RTD is at 100°C (or 138.5Ω).

As suggested in Table I, the temperature span may also be adjusted by changing the voltage span of the Signal Amplifier. Changing the gain from 2 to 4, for example, will halve the temperature span to about 52°C on the 4-20mA output configuration. (See section "Adjusting Input Span".)

The configuration for a three-wire RTD shown in Figure 17 can accommodate two-wire sensors by simply joining Pins 1 and 5 of the AD693.

INTERFACING LOAD CELLS AND METAL FOIL STRAIN GAGES

The availability of the on-chip Voltage Reference, Auxiliary Amplifier and 3mA of excitation current make it easy to adapt the AD693 to a variety of load cells and strain gages.

The circuit shown in Figure 18 illustrates a generalized approach in which the full flexibility of the AD693 is required to interface to a low resistance bridge. For a high impedance transducer the bridge can be directly powered from the 6.2V Reference.

Component values in this example have been selected to match the popular standard of 2mV/V sensitivity and 350Ω bridge resistance. Load cells are generally made for either tension and compression, or compression only; use of the 12mA zero tap allows for operation in the tension and compression mode. An optional zero adjustment is provided with values selected for ±2% FS adjustment range.

Because of the low resistance of most foil bridges, the excitation voltage must be low so as not to exceed the available 4mA zero current. About 1V is derived from the 6.2V Reference and an external voltage divider; the Aux-Amp is then used as a follower to make a stiff drive for the bridge. Similar applications with higher resistance sensors can use proportionally higher voltage.

Finally, to accommodate the 2mV/V sensitivity of the bridge, the full-scale span of the Signal Amplifier must be reduced. Using the load cell in both tension and compression with 1V of excitation, therefore, dictates that the span be adjusted to 4mV. By substituting in the expression, $R_{S1} = 400\Omega/[(30mV/S) - 1]$, the nominal resistance required to achieve this span is found to be 61.54Ω. Calculate the minimum resistance required by subtracting 10% from 61.54Ω to allow for the internal resistor tolerance of the AD693, leaving 55.38Ω (See "Adjusting Input Span".) The standard value of 54.9Ω is used with a 20Ω potentiometer for full-scale adjustment.

If a load cell with a precalibrated sensitivity constant is to be used, the resultant full-scale span applied to the Signal Amplifier is found by multiplying that sensitivity by the excitation voltage. (In Figure 18, the excitation voltage is actually (10kΩ/62.3kΩ) (6.2V) = 0.995V).

THERMOCOUPLE MEASUREMENTS

The AD693 can be used with several types of thermocouple inputs to provide a 4-20mA current loop output corresponding to a variety of measurement temperature ranges. Cold junction compensation (CJC) can be implemented using an AD592 or AD590 and a few external resistors as shown in Figure 19.

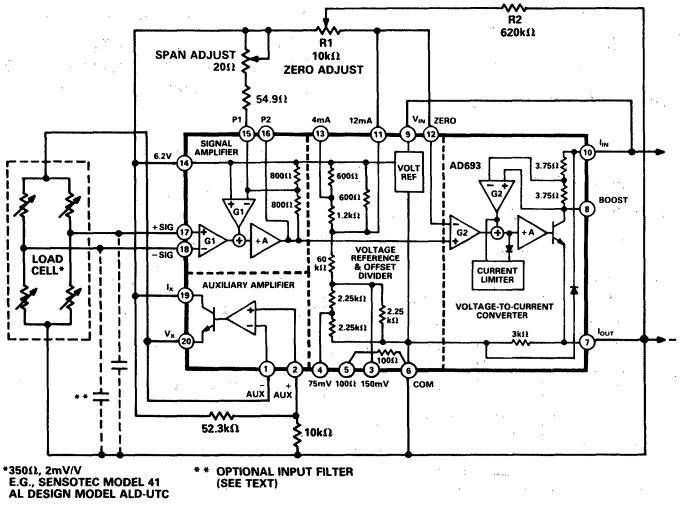


Figure 18. Utilizing the Auxiliary Amplifier to Drive a Load Cell, 12mA ±8mA Output

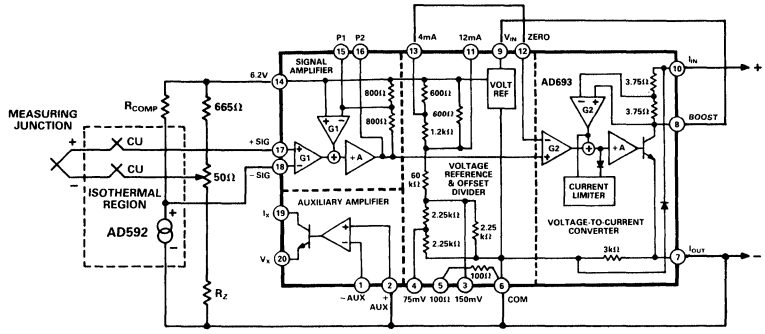


Figure 19. Thermocouple Inputs with Cold Junction Compensation

POLARITY	MATERIAL	TYPE	AMBIENT TEMP	RCOMP	RZ	30mV TEMP RANGE	60mV TEMP RANGE
+	IRON	J	25°	51.7Ω	301K	546°C	1035°C
−	CONSTANTAN		75°	53.6Ω	294K		
+	NICKEL-CHROME	K	25°	40.2Ω	392K	721°C	—
−	NICKEL-ALUMINUM		75°	42.2Ω	374K		
+	NICKEL-CHROME	E	25°	60.4Ω	261K	413°C	787°C
−	COPPER-NICKEL		75°	64.9Ω	243K		
+	COPPER	T	25°	40.2Ω	392K	USE WITH GAIN>2	
−	COPPER-NICKEL		75°	45.3Ω	340K		

Table II. Thermocouple Application – Cold Junction Compensation Table

From Table II simply choose the type of thermocouple and the appropriate average reference junction temperature to select values for R_{COMP} and R_Z. The CJC voltage is developed across R_{COMP} as a result of the AD592 1μA/K output and is added to the thermocouple loop voltage. The 50Ω potentiometer is biased by R_Z to provide the correct zero adjustment range appropriate for the divider and also translates the Kelvin scale of the AD592 to °Celsius. To calibrate the circuit, put the thermocouple in an ice bath (or use a thermocouple simulator set to 0) and adjust the potentiometer for a 4mA loop current.

The span of the circuit in °C is determined by matching the signal amplifier input voltage range to it's temperature equivalent via a set of thermocouple tables referenced to °C. For example, the output of a properly referenced type J thermocouple is 60mV when the hot junction is at 1035°C. Table II lists the maximum measurement temperature for several thermocouple types using the preadjusted 30mV and 60mV input ranges.

More convenient temperature ranges can be selected by determining the full-scale input voltages via standard thermocouple tables and adjusting the AD693 span. For example, suppose only a 300°C span is to be measured with a type K thermocouple. From a standard table, the thermocouple output is 12.207mV; since 60mV at the signal amplifier corresponds to a 16mA span at the output a gain of 5, or more precisely 60mV/12.207mV = 4.915 will be needed. Using a 12.207mV span in the gain resistor formula given in "Adjusting Input Span" yields a value of about 270Ω as the minimum from P1 to 6.2V. Adding a 50Ω potentiometer will allow ample adjustment range.

With the connection illustrated, the AD693 will give a full-scale indication with an open thermocouple.

ERROR BUDGET ANALYSIS

Loop-Powered Operation specifications refer to parameters tested with the AD693 operating as a loop-powered transmitter. The specifications are valid for the preset spans of 30mV, 60mV and those spans in between. The section, "Components of Error", refers to parameters tested on the individual functional blocks, (Signal Amplifier, V/I Converter, Voltage Reference, and Auxiliary Amplifier). These can be used to get an indication of device performance when the AD693 is used in local power mode or when it is adjusted to spans of less than 30mV.

Table III lists the expressions required to calculate the total error. The AD693 is tested with a 250Ω load, a 24V loop supply and an input common-mode voltage of 3.1V. The expressions below calculate errors due to deviations from these nominal conditions.

The total error at zero consists only of offset errors. The total error at full scale consists of the offset errors plus the span errors. Adding the above errors in this manner may result in an error as large as 0.8% of full scale, however, as a rule, the AD693 performs better as the span and offset errors do not tend to add worst case. The specification "Total Unadjusted Error", (TUE), reflects this and gives the maximum error as a % of full scale for any point in the transfer function when the device is operated in one of its preset spans, with no external trims. The TUE is less than the error you would get by adding the span and offset errors worst case.

Thus, an alternative way of calculating the total error is to start with the TUE and add to it those errors that result from operation of the AD693 with a load resistance, loop supply voltage, or common-mode input voltage different than specified. (See Example 1 below.)

ERROR BUDGET FOR SPANS LESS THAN 30mV

An accommodation must be made to include the input voltage offset of the signal amplifier when the span is adjusted to less than 30mV. The TUE and the Zero Current Error include the input offset voltage contribution of the signal amplifier in a gain of 2. As the input offset voltage is multiplied by the gain of the signal amplifier, one must include the additional error when the signal amplifier is set to gains greater than 2.

For example, the 300 °K span thermocouple application discussed previously requires a 12.207mV input span; the signal amplifier must be adjusted to a gain of approximately 5. The loop transconductance is now 1.333 A/V, (5 × 0.2666 A/V). Calculate the total error by substituting the new values for the transconductance and span into the equations in Table III as was done in Example I. The error contribution due to V_{OS} is $5 \times V_{OS}$, however, since $2 \times V_{OS}$ is already included in the TUE and the Zero Current Error it is necessary to add an error of only $(5-2) \times V_{OS}$ to the error budget. Note that span error may by reduced to zero with the span trim, leaving only the offset and nonlinearity of the AD693.

RTI Contributions to Offset Error

	Error Source	Expression for RTI Error at Zero
I_{ZE}	Zero Current Error	I_{ZE}/X_S
PSRR	Power Supply Rejection Ratio	$(\lvert V_{LOOP} - 24V\rvert + [\lvert R_L - 250\Omega\rvert \times I_Z]) \times PSRR$
CMRR	Common-Mode Rejection Ratio	$\lvert V_{CM} - 3.1V\rvert \times CMRR$
IOS	Input Offset Current	$R_S \times IOS$

RTI Contributions to Span Error

	Error Source	Expression for RTI Error at Full Scale
X_{SE}	Transconductance Error	$V_{SPAN} \times X_{SE}$
X_{PSRR}	Transconductance PSRR[1]	$\lvert R_L - 250\Omega\rvert \times I_S \times PSRR$
X_{CMRR}	Transconductance CMRR	$\lvert V_{CM} - 3.1V\rvert \times V_{SPAN} \times X_{CMRR}$
X_{NL}	Nonlinearity	$V_{SPAN} \times X_{NL}$
I_{DIFF}	Differential Input Current[2]	$R_S \times I_{DIFF}$

Abbreviations

I_Z	Zero Current (usually 4mA)
I_S	Output span (usually 16mA)
R_S	Input source impedance
R_L	Load resistance
V_{LOOP}	Loop supply voltage
V_{CM}	Input common-mode voltage
V_{SPAN}	Input span
X_S	Nominal transconductance in A/V

[1]The 4-20mA signal, flowing through the metering resistor, modulates the power supply voltage seen by the AD693. The change in voltage causes a power supply rejection error that varies with the output current, thus it appears as a span error.

[2]The input bias current of the inverting input increases with input signal voltage. The differential input current, I_{DIFF}, equals the inverting input current minus the noninverting input current; see Figure 2. I_{DIFF}, flowing into an input source inpedance, will cause an input voltage error that varies with signal. If the change in differential input current with input signal is approximated as a linear function, then any error due to source impedance may be approximated as a span error. To calculate I_{DIFF}, refer to Figure 2 and find the value for $I_{DIFF}/+In$ corresponding to the full-scale input voltage for your application. Multiply by +In max to get I_{DIFF}. Multiply I_{DIFF} by the source impedance to get the input voltage error at full scale.

Table III. RTI Contributions to Span and Offset Error

EXAMPLE I

The AD693 is configured as a 4-20mA loop powered transmitter with a 60mV FS input. The inputs are driven by a differential voltage at 2V common mode with a 300Ω balanced source resistance. A 24V loop supply is used with a 500Ω metering resistance. (See Table IV below.)

Trimming the offset and span for your application will remove all span and offset errors except the nonlinearity of the AD693.

OFFSET ERRORS			
I_Z	Already included in the TUE spec.	0.0μV	
PSRR	PSRR = 5.6μV/V; (|24V − 24V| + [|500Ω − 250Ω| × 4mA]) × 5.6μV/V = V_{LOOP} = 24V, R_L = 500Ω I_Z = 4mA	5.6μV	
CMRR	CMRR = 30μV/V; |2V − 3.1V| × 30μV/V = V_{CM} = 2V	33.0μV	
IOS	IOS = 3nA, R_S = 300Ω; 300Ω × 3nA =	0.9μV	
Total Additional Error at 4mA			**39.5μV**
As % of full scale; (39.5μV × 0.2666 A/V)/20mA × 100% =		0.053% of FS	
SPAN ERRORS			
X_{SE}	Already included in the TUE spec.	0.0μV	
X_{PSRR}	PSRR = 5.6μV/V; (|500Ω − 250Ω| × 16mA) × 5.6μV/V = R_L = 500Ω, I_S = 16mA	22.4μV	
X_{CMRR}	X_{CMRR} = 0.06%/V; |2V − 3.1V| × 60mV × 0.06%/V = V_{CM} = 2V, V_{SPAN} = 60mV	39.6μV	
I_{DIFF}	V_{SPAN} = +60mV; 300Ω × 2 × 20nA $I_{DIFF}/+In$ = 2 from Figure 2)	12.0μV	
X_{NL}	Already included in the TUE	0.0μV	
Total Additional Span Error at Full Scale			**74.0μV**
Total Additional Error at Full Scale; $\epsilon_{OFFSET} + \epsilon_{SPAN}$ = 39.5μV + 74.0μV =		113.5μV	
As % of Full Scale; (113.5μV × 0.2666 A/V)/20mA × 100% =		0.151% of FS	
New Total Unadjusted Error @ FS; $\epsilon_{TUE} + \epsilon_{ADDITIONAL}$ = 0.5% + 0.151% =			**0.651% of FS**

Table IV. Example 1

ANALOG DEVICES

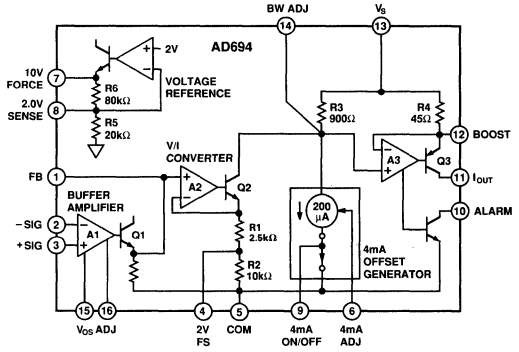
4–20 mA Transmitter

AD694*

FEATURES

4–20 mA, 0–20 mA Output Ranges
Precalibrated Input Ranges:
0 V to 2 V, 0 V to 10 V
Precision Voltage Reference
Programmable to 2.000 V or 10.000 V
Single or Dual Supply Operation
Wide Power Supply Range: +4.5 V to +36 V
Wide Output Compliance
Input Buffer Amplifier
Open-Loop Alarm
Optional External Pass Transistor to Reduce Self-Heating Errors
0.002% typ Nonlinearity

AD694 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD694 is a monolithic current transmitter that accepts high level signal inputs to drive a standard 4–20 mA current loop for the control of valves, actuators, and other devices commonly used in process control. The input signal is buffered by an input amplifier that can be used to scale the input signal or buffer the output from a current mode DAC. Precalibrated input spans of 0 V to 2 V and 0 V to 10 V are selected by simple pin strapping; other spans may be programmed with external resistor.

The output stage compliance extends to within 2 V of V_S and its special design allows the output voltage to extend below common in dual supply operation. An alarm warns of an open 4 to 20 mA loop or noncompliance of the output stage.

Active laser trimming of the AD694's thin film resistors results in high levels of accuracy without the need for additional adjustments and calibration. An external pass transistor may be used with the AD694 to off-load power dissipation, extending the temperature range of operation.

The AD694 is the ideal building block for systems requiring noise immune 4–20 mA signal transmission to operate valves, actuators, and other control devices, as well as for the transmission of process parameters such as pressure, temperature, or flow. It is recommended as a replacement for discrete designs in a variety of applications in industrial process control, factory automation, and system monitoring.

The AD694 is available in hermetically sealed, 16-pin cerdip, specified over the −40°C to +85°C industrial temperature range and in a 16-pin plastic DIP specified over the 0 to +70°C temperature range.

***Protected by U.S. Patents: 30,586; 4,250,445; 4,857,862.**

PRODUCT HIGHLIGHTS

1. The AD694 is a complete voltage in to 4–20 mA out current transmitter.
2. Pin programmable input ranges are pre-calibrated at 0 V to 2 V and 0 V to 10 V.
3. The input amplifier may be configured to buffer and scale the input voltage, or to serve as an output amplifier for current output DACs.
4. The output voltage compliance extends to within 2 V of the positive supply and below common. When operated with a 5 V supply, the output voltage compliance extends 30 V below common.
5. The AD694 interfaces directly to 8-, 10-, and 12-bit single supply CMOS and bipolar DACs.
6. The 4 mA zero current may be switched on and off with a TTL control pin, allowing 0–20 mA operation.
7. An open collector alarm warns of loop failure due to open wires or noncompliance of the output stage.
8. A monitored output is provided to drive an external pass transistor. The feature off-loads power dissipation to extend the temperature range of operation and minimize self-heating error.

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SPECIFICATIONS (@ +25°C, R_L = 250 Ω and V_S = +24 V, unless otherwise noted)

Model	AD694JN/AQ			AD694BQ			
	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS							
Input Voltage Range	−0.2	V_S−2.0V	**V_S−2.5 V**	−0.2	V_S−2.0 V	**V_S−2.5 V**	V
Input Bias Current							
Either Input, T_{min} to T_{max}		1.5	**5**		1.5	**5**	nA
Offset Current, T_{min} to T_{max}		±0.1	**±1**		±0.1	**±1**	nA
Offset Current Drift		±1.0	±5.0		±1.0	±5.0	pA/°C
Input Impedance	5			5			MΩ
OUTPUT CHARACTERISTICS							
Operating Current Range	0		23	0		23	mA
Specified Performance	4		20	4		20	mA
Output Voltage Compliance	**V_S−36 V**		**V_S−2 V**	**V_S−36 V**		**V_S−2 V**	V
Output Impedance, 4–20 mA	40.0	50.0		40.0	50.0		MΩ
Current Limit @ 2× FS Overdrive	**24**		**44**	**24**		**44**	mA
Slew Rate		1.3			1.3		mA/μs
SPAN AND ZERO ACCURACY[1]							
4 mA Offset Error @ 0 V Input[2]							
Error from 4.000 mA, 4 mA On		±10	**±20**		±5	**±10**	μA
Error from 0.000 mA, 4 mA Off	0	+10	**+20**	0	+5	**+10**	μA
T_{min} to T_{max}		±10	**±40**		±5	**±20**	μA
vs. Supply (2 V Span/10 V Span)		0.3/0.05	**0.8/0.4**		0.3/0.05	**0.8/0.4**	μA/V
Trim Range, 4 mA Zero	2.0		4.8	2.0		4.8	mA
Span							
Nominal Transfer Function							
Input FS = 2 V		8.0			8.0		mA/V
Input FS = 10 V		1.6			1.6		mA/V
Transfer Function Error from Nom,							
Input FS = 2 V, 10 V		±0.1	**±0.3**		±0.05	**±0.15**	% of Span
T_{min} to T_{max}		±0.002	±0.005		±0.001	**±0.0025**	% of Span/°C
vs. Supply		±0.001	**±0.005**		±0.001	**±0.005**	% of Span/V
Nonlinearity[3]		±0.005	**±0.015**		±0.001	**±0.005**	% of Span
4 mA On: Max Pin 9 Voltage			0.8			0.8	V
4 mA Off: Min Pin 9 Voltage	2.0			2.0			V
VOLTAGE REFERENCE							
Output Voltage: 10 V Reference	**9.960**	10.000	**10.040**	**9.980**	10.000	**10.020**	V
Output Voltage: 2 V Reference	**1.992**	2.000	**2.008**	**1.996**	2.000	**2.004**	V
T_{min} to T_{max}[4]		30	**50**		20	**30**	ppm/°C
vs. Output Current, V_{REF} = 2 V, 10 V		0.15	**0.50**		0.15	**0.50**	mV/mA
vs. Supply, V_{REF} = 2 V, 10 V		±0.001	**±0.005**		±0.001	**±0.005**	%/V
Output Current							
Source	5			5			mA
Sink		0.2			0.2		mA
ALARM CHARACTERISTICS							
$V_{CE(SAT)}$ @ 2.5 mA		0.35			0.35		V
Leakage Current			**±1**			**±1**	μA
Alarm Pin Current		20			20		mA
POWER REQUIREMENTS							
Specified Performance		24			24		V
Operating Range							
2 V FS, V_{REF} = 2 V	**4.5**		**36**	**4.5**		**36**	V
2 V, 10 V FS, V_{REF} = 2 V, 10 V	**12.5**		**36**	**12.5**		**36**	V
Quiescent Current, 4 mA Off		1.5	**2.0**		1.5	**2.0**	mA
TEMPERATURE RANGE							
Specified Performance[5] AD694AQ/BQ	−40		+85	−40		+85	°C
AD694JN	0		+70	0		+70	°C
Operating AD694AQ/BQ	−55		+125	−55		+125	°C
AD694JN	−40		+85	−40		+85	°C

Model	AD694JN/AQ Min	AD694JN/AQ Typ	AD694JN/AQ Max	AD694BQ Min	AD694BQ Typ	AD694BQ Max	Units
BUFFER AMPLIFIER[6]							
Input Offset Voltage							
Initial Offset		±150	**±500**		±50	**±500**	μV
T_{min} to T_{max}		±2	±3		±2	±3	μV/°C
vs. Supply	80	90		80	90		dB
vs. Common Mode	80	90		80	90		dB
Trim Range	**±2.5**	±4.0		**±2.5**	±4.0		mV
Frequency Response							
Unity Gain, Small Signal		300			300		kHz
Input Voltage Noise (0.1 to 10 Hz)		2			2		μV p-p
Open-Loop Gain							
V_O = +10 V, RL ≥ 10 kΩ		50			50		V/mV
Output Voltage @ Pin 1, FB[1]							
V_{OL}		1.0	10		1.0	10	mV
V_{OH}	V_S−2.5 V	V_S−2 V		V_S−2.5 V	V_S−2 V		V

NOTES

[1]The single supply op amps of the AD694, lacking pull down current, may not reach 0.000 V at their outputs. For this reason, span, offset, and nonlinearity are specified with the input amplifiers operating in their linear range. The input voltage used for the tests is 5 mV to 2 V and 5 mV to 10 V for the two pre-calibrated input ranges. Span and zero accuracy are tested with the buffer amplifier configured as a follower.

[2]Offset at 4 mA out and 0 mA out are extrapolated to 0.000 V input from measurements made at 5 mV and at full scale. See Note 1.

[3]Nonlinearity is specified as the maximum deviation of the output, as a % of span, from a straight line drawn through the endpoints of the transfer function.

[4]Voltage reference drift guaranteed by the Box Method. The voltage reference output over temperature will fall inside of a box whose length is determined by the temperature range and whose height is determined by the maximum temperature coefficient multiplied by the temperature span in degrees C.

[5]Devices tested at these temperatures with a pass transistor. Allowable temperature range of operation is dependent upon internal power dissipation. Absolute maximum junction and case temperature should not be exceeded. See section: "Power Dissipation Considerations."

[6]Buffer amplifier specs for reference. Buffer amplifier offset and drift already included in Span and Zero accuracy specs above.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +36 V
V_S to I_{OUT} . . . . . +36 V
Input Voltage, (Either Input Pin 2 or 3) . . . . −0.3 V to +36 V
Reference Short Circuit to Common . . . . . Indefinite
Alarm Voltage, Pin 10 . . . . . +36 V
4 mA Adj, Pin 6 . . . . . +1 V
4 mA On/Off, Pin 9 . . . . . 0 V to 36 V

Storage Temperature Range
AD694Q . . . . . −65°C to +150°C
AD694N . . . . . −65°C to +125°C
Lead Temperature, 10 sec Soldering . . . . . +300°C
Maximum Junction Temperature . . . . . +150°C
Maximum Case Temperature
Plastic Package (N) . . . . . +125°C
Cerdip Package (Q) . . . . . +125°C

Transistor Count: . . . . . 75 Active Devices
Substrate Connection: . . . . . to Com, Pin 5

Thermal Characteristics:
Plastic (N) Package: θ_{JC} = 50°C/Watt
θ_{CA} (Still Air) = 85°C/Watt
Cerdip (Q) Package: θ_{JC} = 30°C/Watt
θ_{CA} (Still Air) = 70°C/Watt

ESD Susceptibility
All pins are rated for a minimum of 4000 V protection, except for Pins 2, 3 and 9 which are rated to survive a minimum of 1500 V. ESD testing conforms to Human Body Model. Always practice ESD prevention.

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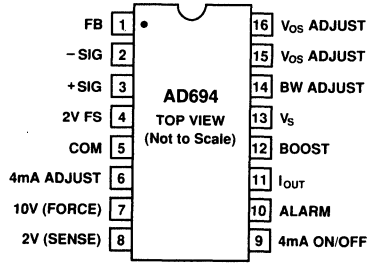
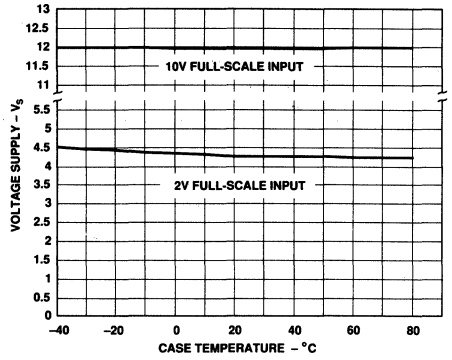
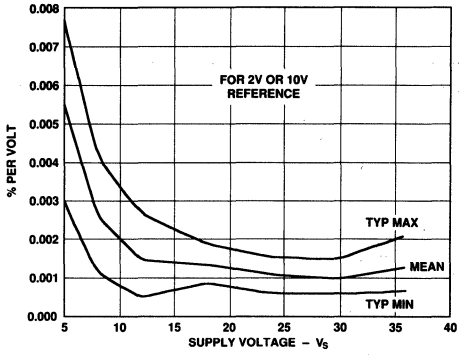
No pin, other than I_{OUT} (11) and ±Sig (2), (3) as noted, may be permitted to become more negative than Com (5). No pin may be permitted to become more positive than V_S (13).

PIN CONFIGURATION

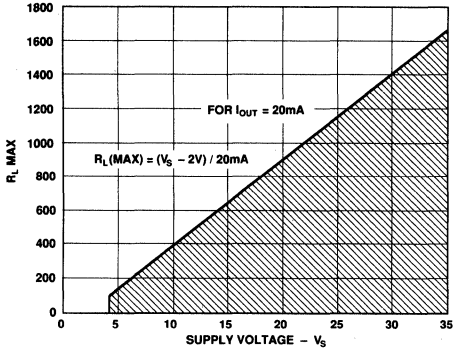




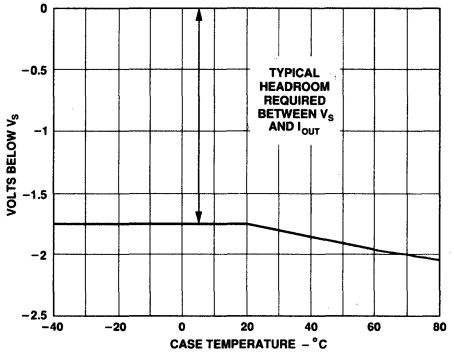
Typical Minimum Supply Voltage vs. Temperature for 2 V & 10 V Full Scale



Voltage Reference Power Supply Rejection



Maximum R_L vs. Supply Voltage



I_{OUT}: Voltage Compliance vs. Temperature

ORDERING GUIDE

Model	Package Option*
AD694JN	Plastic DIP (N-16)
AD694AQ	Cerdip (Q-16)
AD694BQ	Cerdip (Q-16)

*See Section 20 for package outline information.

FUNCTIONAL DESCRIPTION

The operation of the AD694 can best be understood by dividing the circuit into three functional parts (see Figure 1). First, a single supply input amplifier buffers the high level, single-ended input signal. The buffer amplifier drives the second section, a voltage to current (V/I) converter, that makes a 0 to 16 mA signal dependent current.

The third section, a voltage reference and offset generator, is responsible for providing the 4 mA offset current signal.

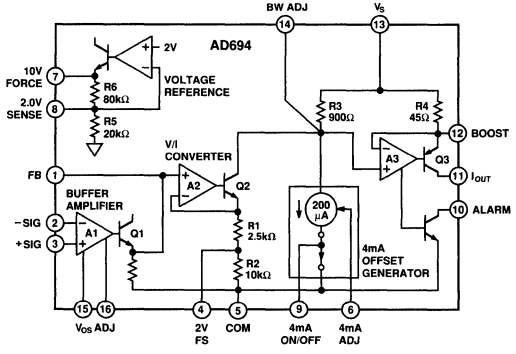


Figure 1. Functional Block Diagram

BUFFER AMPLIFIER

The buffer amplifier is a single supply amplifier that may be used as a unity gain buffer, an output amplifier for a current output D/A converter, or as a gain block to amplify low level signals. The amplifier's PNP input stage has a common-mode range that extends from a few hundred mV below ground to within 2.5 V of V_S. The Class A output of the amplifier appears at Pin 1 (FB). The output range extends from about 1 mV above common to within 2.5 V of V_S when the amplifier is operated as a follower. The amplifier can source a maximum load of 5 kΩ, but can sink only as much as its internal 10 kΩ pull-down resistor allows.

V/I CONVERTER

The ground referenced, input signal from the buffer amplifier is converted to a 0 to 0.8 mA current by A2 and level shifted to the positive supply. A current mirror then multiplies this signal by a factor of 20 to make the signal current of 0 to 16 mA. This technique allows the output stage to drive a load to within 2 V of the positive supply (V_S). Amplifier A2 forces the voltage at Pin 1 across resistors R1 and R2 by driving the Darlington transistor, Q2. The high gain Darlington transmits the resistor current to its collector and to R3 (900 Ω). A3 forces the level shifted signal across the 45 Ω resistor to get a current gain of 20. The transfer function of the V/I stage is therefore:

$$I_{OUT} = (20 \times V_{(PIN1)}) / (R1 + R2)$$

resulting in a 0–16 mA output swing for a 0–10 V input. Tying Pin 4 (2 V FS) to ground shorts out R2 and results in a 2 V full-scale input for a 16 mA output span.

The output stage of the V/I converter is of a unique design that allows the I_{OUT} pin to drive a load below the common (substrate) potential of the device. The output transistor can always drive a load to a point 36 V below the positive supply (V_S). An optional NPN pass transistor can be added to transfer most of the power dissipation off-chip, to extend the temperature range of operation.

The output stage is current-limited at approximately 38 mA to protect the output from an overdrive at its inputs. The V/I will allow linear operation to approximately 24 mA. The V/I converter also has an open collector alarm (Pin 10) which warns of open-circuit condition at the I_{OUT} pin or of attempts to drive the output to a voltage greater than V_S −2 V.

4 mA OFFSET GENERATOR

This circuit converts a constant voltage from the voltage reference to a constant current of approximately 200 µA. This current is summed with the signal current at Pin 14 (BW Adjust), to result in a constant 4 mA offset current at I_{OUT}. The 4 mA Adj (Pin 6) allows the offset current to be adjusted to any current in the range of 2 mA to 4.8 mA. Pin 9 (4 mA On/Off) can shut off the offset current completely if it is lifted to 2.0 V or more, allowing 0 to 20 mA operation of the AD694. In normal 4–20 mA operation, Pin 9 is connected to ground.

VOLTAGE REFERENCE

A 2 V or 10 V voltage reference is available for user applications, selectable by pin-strapping. The 10 V option is available for supply voltages greater than 12.5 V, the 2 V output is available over the whole 4.5 V – 36 V power supply range. The reference can source up to 5 mA for user applications. A boost transistor can be added to increase the current drive capability of the 2 V mode.

APPLYING THE AD694

The AD694 can easily be connected for either dual or single supply operation, to operate from supplies as low as 4.5 V and as high as 36 V. The following sections describe the different connection configuration, as well as adjustment methods. Table I shows possible connection options.

Input Range	Output Range	Voltage Reference	Min V_S	Pin 9	Pin 4	Pin 8
0–2 V	4–20 mA	2 V	4.5 V	Pin 5	Pin 5	Pin 7
0–10 V	4–20 mA	2 V	12.5 V	Pin 5	Open	Pin 7
0–2.5 V	0–20 mA	2 V	5.0 V	≥2 V	Pin 5	Pin 7
0–12.5 V	0–20 mA	2 V	13.0 V	≥2 V	Open	Pin 7
0–2 V	4–20 mA	10 V	12.5 V	Pin 5	Pin 5	Open
0–10 V	4–20 mA	10 V	12.5 V	Pin 5	Open	Open
0–2.5 V	0–20 mA	10 V	12.5 V	≥2 V	Pin 5	Open
0–12.5 V	0–20 mA	10 V	13.0 V	≥2 V	Open	Open

Table I. Precalibrated Ranges for the AD694

BASIC CONNECTIONS: 12.5 V SINGLE SUPPLY OPERATION WITH 10 V FS

Figure 2 shows the minimal connections required for basic operation with a +12.5 V power supply, 10 V input span, 4–20 mA output span, and a 10 V voltage reference. The buffer amplifier is connected as a voltage follower to drive the V/I converter by connecting FB (Pin 1) to −Sig (Pin 2). 4 mA On/Off (Pin 9) is tied to ground (Pin 5) to enable the 4 mA offset current. The AD694 can drive a maximum load $R_L = [V_S - 2\ V] / 20\ mA$, thus the maximum load with a 12.5 V supply is 525 Ω.

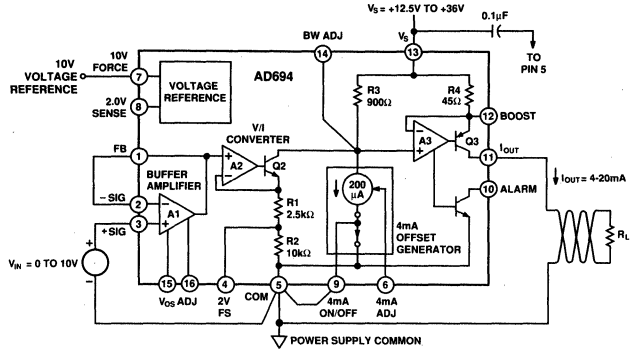


Figure 2. Minimal Connections for 0–10 V Single-Ended Input, 4–20 mA Output, 10 V Reference Output

SELECTING A 2 V FULL-SCALE INPUT

The 2 V full-scale option is selected by shorting Pin 4 (2 V FS) to Pin 5 (Common). The connection should be as short as possible; any parasitic resistance will affect the precalibrated span accuracy.

SELECTING THE 2 V VOLTAGE REFERENCE

The voltage reference is set to a 2 V output by shorting Pin 7 to Pin 8 (10 V Force to 2 V Sense). If desired, the 2 V reference can be set up for remote force and sense connection. Keep in mind that the 2 V Sense line carries a constant current of 100 μA that could cause an offset error over long wire runs. The 2 V reference option can be used with all supply voltages greater than 4.5 V.

An NPN boost transistor can be added in the 2 V mode to increase the current drive capability of the 2 V reference. The 10 V force pin is connected to the base of the NPN, and the NPN emitter is connected to the 2 V sense pin. The minimum V_S of the part increases by approximately 0.7 V.

4.5 V SINGLE SUPPLY OPERATION

For operation with a +4.5 V power supply, the input span and the voltage reference output must be reduced to give the amplifiers their required 2.5 V of head room for operation. This is done by adjusting the AD694 for 2 V full-scale input, and a voltage reference output of 2 V as described above.

GENERAL DESIGN GUIDELINES

A 0.1 μF decoupling capacitor is recommended in all applications from V_S (Pin 13) to Com (Pin 5). Additional components may be required if the output load is nonresistive, see section on driving nonresistive loads. The buffer amplifier PNP inputs should not be brought more than −0.3 V of common, or they will begin to source large amounts of current. Input protection resistors must be added to the inputs if there is a danger of this occurring. The output of the buffer amplifier, Pin 1 (FB), is not short circuit protected. Shorting this pin to ground or V_S with a signal present on the amplifier may damage it. Input signals should not drive Pin 1 (FB) directly; always use the buffer amplifier to buffer input signals.

DRIVING NONRESISTIVE LOADS

The AD694 is designed to be stable when driving resistive loads. Adding a 0.01 μF capacitor from I_{OUT} (Pin 11) to Com (Pin 5), as shown in Figure 3, insures the stability of the AD694 when driving inductive or poorly defined loads. This capacitor is recommended when there is any uncertainty as to the characteristics of the load.

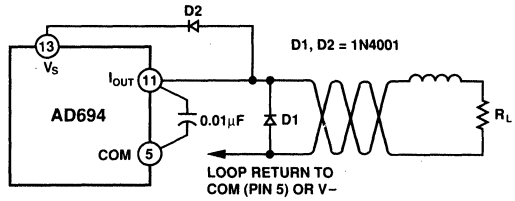


Figure 3. Capacitor Utilized When Driving Nonresistive Loads; Protection Diodes Used When Driving Inductive Loads

Additional protection is recommended when driving inductive loads. Figure 3 shows two protective diodes, D1 and D2, added to protect against voltage spikes that may extend above V_S or below common that could damage the AD694. These diodes should be used in addition to the 0.01 μF capacitor. When the optional NPN transistor is used, the capacitor and diodes should connect to the NPN emitter instead of Pin 11.

0–20 mA OPERATION

A 0–20 mA output range is available with the AD694 by removing the 4 mA offset current with the 4 mA On/Off pin. In normal 4–20 mA operation 4 mA On/Off (Pin 9) is tied to ground, enabling the 4 mA offset current. Tying Pin 9 to a potential of 2 V or greater turns off the 4 mA offset current; connecting Pin 9 to the voltage reference, 2 V or 10 V, is a convenient way to do this. In 0–20 mA mode the input span is increased by 20%, thus the precalibrated input spans of 2 V and 10 V become 2.5 V and 12.5 V. Minimum supply voltages for the two spans increase to 5 V and 13 V.

The 4 mA On/Off pin may also be used as a "jiggle pin" to unstick valves or actuators, or as a way to shut off a 4–20 mA loop entirely. Note that the pin only removes the 4 mA offset and not the signal current.

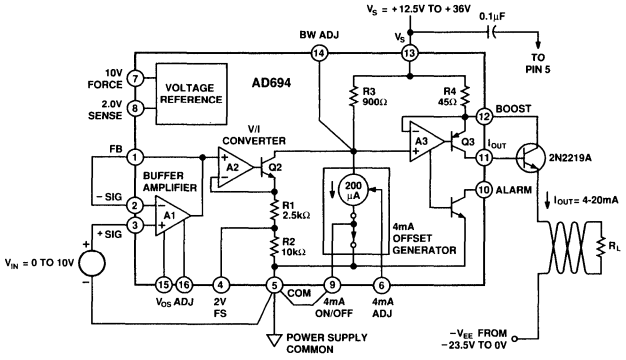


Figure 4. Using Optional Pass Transistor to Minimize Self-Heating Errors; Dual Supply Operation Shown

DUAL SUPPLY OPERATION

Figure 4 shows the AD694 operated in dual supply mode. (Note that the pass transistor is shown for illustration and is not required for dual supply operation.) The device is powered completely by the positive supply which may be as low as 4.5 V. The unique design of the output stage allows the I_{OUT} pin to extend below common to a negative supply. The output stage can source a current to a point 36 V below the positive supply. For example, when operated with a +12.5 V supply, the AD694 can source a current to a point as low as 23.5 V below common. This feature can simplify the interface to dual supply D/A converters by eliminating grounding and level-shifting problems while increasing the load that the transmitter is able to drive. Note that the I_{OUT} pin is the only pin that should be allowed to extend lower than −0.3 V of common.

OPERATION WITH A PASS TRANSISTOR

The AD694 can operate as a stand-alone 4–20 mA converter with no additional active components. However, provisions have been made to connect I_{OUT} to the base of an external NPN pass transistor as shown in Figure 4. This permits a majority of the power dissipation to be moved off-chip to enhance performance and extend the temperature range of operation. Note that the positive output voltage compliance is reduced by approximately 0.7 V, the V_{BE} of the pass device.

The external pass transistor selected should have a BV_{CEO} greater than the intended supply voltage with a sufficient power rating for continuous operation with 25 mA current at the supply voltage. Ft should be in the 10 MHz to 100 MHz range and β should be greater than 10 at a 20 mA emitter current. Heat sinking the external pass transistor is suggested.

POWER DISSIPATION CONSIDERATIONS

The AD694 is rated for operation over its specified temperature without the use of an external pass transistor. However, it is possible to exceed the absolute maximum power dissipation, with some combinations of power supply voltage and voltage reference load. The internal dissipation of the part can be calculated to determine there is a chance that the absolute maximum dissipation may be exceeded. The die temperature must never exceed 150°C.

Total power dissipation (P_{TOT}), is the sum of power dissipated by the internal amplifiers, P (Standing), the voltage reference, P (V_{REF}) and the current output stage, P(I_{OUT}) as follows:

$$P_{TOT} = P\ (Standing) + P\ (V_{REF}) + P\ (I_{OUT})$$

where:

$P\ (Standing)$ = 2 mA (max) × V_S
$P\ (V_{REF})$ = (V_S − V_{REF})× I_{VREF}
$P\ (I_{OUT})$ = (V_S − V_{OUT}) × I_{OUT} (max):

I_{OUT} *(max)* may be the max expected operating current, or the overdriven current of the device.

$P\ (I_{OUT})$ drops to (2 Volts × I_{OUT}) if a pass transistor is used.

Definitions:

V_{REF} = output voltage of reference
I_{VREF} = output current of reference
V_S = supply voltage
V_{OUT} = voltage at I_{OUT} pin.

An appropriate safety factor should be added to P_{TOT}.

The junction temperature may be calculated with the following formula:

$$T_J = P_{TOT}\ (\theta_{JC} + \theta_{CA}) + T_{AMBIENT}$$

θ_{JC} is the thermal resistance between the chip and the package (case), θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection of the case to ambient.

For example, assume that the part is operating with a V_S of 24 V in the cerdip package at 50°C, with a 1 mA load on the 10 V reference. Assume that I_{OUT} is grounded and that the max I_{OUT} would be 20 mA. The internal dissipation would be:

$$P_{(TOT)} = 2\ mA \times 24\ V + (24\ V - 10\ V) \times 1\ mA + (24\ V - 0\ V) \times 20\ mA$$
$$= 48\ mW + 14\ mW + 480\ mW = 542\ mW$$

Using θ_{JC} of 30°C/Watt and θ_{CA} of 70°C/Watt, (from spec page) the junction temperature is:

$$T_J = 542\ mW\ (30°C/W + 70°C/W) + 50°C = 104.2°C$$

The junction temperature is in the safe region.

13

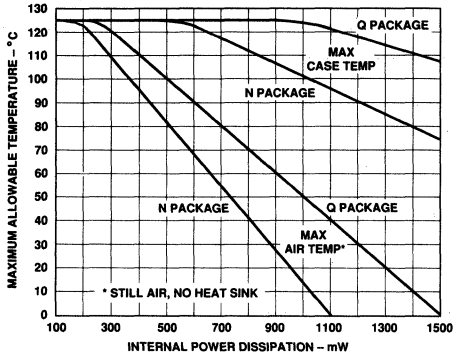


Figure 5. Internal Power Dissipation in mW

Internal power dissipation can be reduced either by reducing the value of θ_{CA} through the use of air flow or heat sinks, or by reducing $P_{(TOT)}$ of the AD694 through the use of an external pass transistor. Figure 5 shows the maximum case and still air temperatures for a given level of power dissipation.

ADJUSTMENT PROCEDURES

The following sections describe methods for trimming the output current offset, the span and the voltage reference.

ADJUSTING 4 mA ZERO

The 4 mA zero current may be adjusted over the range of 2 mA to 4.8 mA to accommodate large input signal offsets, or to allow small adjustment in the zero current. The zero may be adjusted by pulling up or down on Pin 6 (4 mA Adj) to increase or decrease the nominal offset current. The 4 mA Adj. (Pin 6) should not be driven to a voltage greater than 1 V. The arrangement of Figure 6 will give an approximately linear adjustment of the 4 mA offset within fixed limits. To find the proper resistor values, first select X, the desired range of adjustment as a fraction of 4 mA. Substitute this value in the appropriate formula below along with the chosen reference output voltage (V_{REF} = 2 V or 10 V usually), to determine the resistor values required.

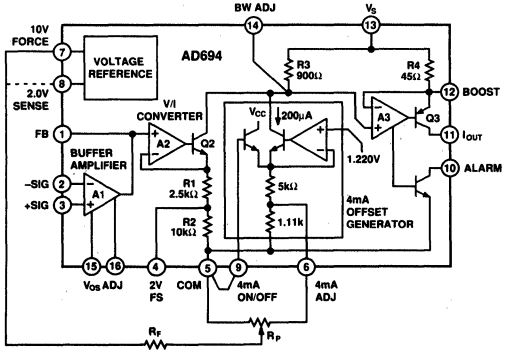


Figure 6. Optional 4 mA Zero Adjustment

$$R_P = 180\ \Omega\ (1/X - 4.5)$$

$$R_F = 500\ \Omega\ [(V_{REF} / 1.22\ V) - 0.18 - 0.82X][1/X - 4.5]$$

These formulae take into account the ±10% internal resistor tolerance and ensure a minimum adjustment range for the 4 mA offset. For example, assume the 2 V reference option has been selected. Choosing X = 0.05; gives an adjustment range of ±5% of the 4 mA offset.

$$R_P = 180\ \Omega\ (1/0.05 - 4.5) = 2.79\ k\Omega$$

$$R_F = 500\ \Omega\ [(2\ V / 1.22) - 0.18 - 0.82 \times 0.05][1/0.05 - 4.5] = 10.99\ k\Omega$$

These can be rounded down to more convenient values of 2.5 kΩ and 9.76 kΩ. In general, if the value of R_P is rounded down slightly, the value of R_F should be rounded down proportionately and vice versa. This helps to keep the adjustment range symmetrical.

ADJUSTING SPAN FOR 10 V FS

When the AD694 is configured with a 10 V input full-scale the span maybe adjusted using the network shown in Figure 7. This scheme allows an approximately linear adjustment of the span above or below the nominal value. The span adjustment does not interact with the 4 mA offset. To select R_S and R_T, choose X, the desired adjustment range as a fraction of the span. Substitute this value in the appropriate formula below.

$$R_T = 1.8\ k\Omega\ ((1 - X) / X)$$

$$R_S = 9\ k\Omega[\ 1 - 0.2\ (1 + X)(\ 1 - X\ )] / 2X$$

These formulae take into account the ±10% absolute resistor tolerance of the internal span resistors and ensures a minimum adjustment range of the span. For example, choosing the adjustment range to be ±2%, or 0.02 gives:

$$R_T = 1.8\ k\Omega((1 - 0.02) / 0.02) = 88.2\ k\Omega$$

$$R_S = 9\ k\Omega\ [\ 1 - 0.2\ (1 + 0.02)(\ 1 - 0.02\ )] / (2 \times 0.02) = 175.5\ k\Omega$$

These values can be rounded up to the more convenient values of 100 kΩ and 198 kΩ. In general, if R_T is rounded up, then the value of R_S should be rounded up proportionally and vice versa.

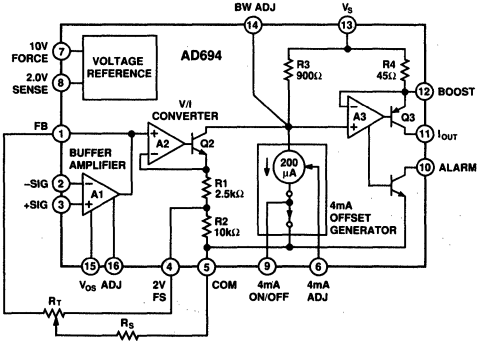


Figure 7. Span Adjustment, 10 V Full Scale

ADJUSTING SPAN FOR 2 V FS

The precalibrated 2 V full-scale range requires a different adjustment scheme due to the single supply nature of the AD694. Figure 8 shows an adjustment scheme that allows an approximately linear adjustment of the 2 V span plus or minus the nominal value. The span adjustment does not affect the value of the 4 mA offset current.

To find the proper resistor values first select X, the desired range of adjustment as a fraction of the output span. Substitute this value into the following formulae:

$$R_A = 2 \times R_B \text{ where } R_B \text{ is greater than 5 K}$$
$$R_C = (2.75\ k\Omega \times X) / (1 - 0.275X)$$

These formulae take into account the ±10% absolute tolerance of the internal span resistors and ensure a minimum adjustment range.

For example, choosing the adjustment range to be ±320 μA of FS or, ±2%, let X = 0.02. Thus:

Setting R_B = 10 K, then $R_A = 2(.02) \times 10\ k\Omega = 400\ \Omega$

$R_C = (2.75\ k\Omega \times 0.02) / (1 - 0.275 \times (0.02)) = 55.3\ \Omega$

The value of R_C can be rounded to the more convenient values of 49.9 Ω. In general, if R_A is rounded up, then R_C should be rounded up proportionally and vice versa; rounding up will increase the range of adjustment.

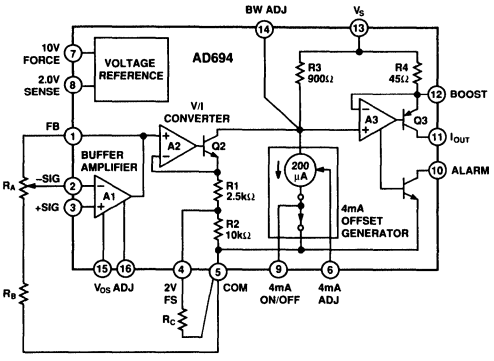


Figure 8. Span Adjustment, 2 V Full Scale

PROGRAMMING OTHER SPANS

There are two methods for programming input spans less than 10 V. The first decreases the input span by programming a noninverting gain into the buffer amplifier. For example, to achieve an input span of 0–5 V, the AD694 is set in its 10 V full-scale mode and the buffer amplifier is configured with a noninverting gain of 2 by adding 2 resistors. Now a 5 V signal at +Sig results in a 10 V full-scale signal at FB (Pin 1), the input to the V/I. This method requires that the V/I be programmed to a 10 V full scale for input spans between 2 V to 10 V. It should be programmed to a 2 V full scale if input spans of less than 2 V are required. This adjustment scheme makes the accuracy of the span adjustment dependent upon the ratio accuracy of the required gain resistors. Thus, it is possible to accurately configure spans other than 2 V or 10 V without using trimming potentiometers, given that the resistor ratios are sufficiently accurate. A supply voltage of 12.5 V is required for spans between 2 V and 10 V. Spans below 2 V require a V_S of 4.5 V or greater.

A second method, allows other spans of less than 10 V to be programmed when supply voltage is less than 12.5 V. Since the AD694 amplifiers require 2.5 V of headroom for operation, a 5 V full-scale input is possible with a 7.5 V supply. This is achieved by placing a resistor, in parallel with R2, (2 V FS (Pin 4) to Com (Pin 5)), to adjust the transconductance of the V/I converter without a headroom penalty. A disadvantage of this method is that the external resistor must match the internal resistor in a precise manner, thus a span trim will be required. The value should be chosen to allow for the ±10% uncertainty in the absolute value of the internal resistor R2.

ADJUSTING REFERENCE OUTPUT

Figure 9 shows one method of making small adjustments to the 10 V reference output. This circuit allows a linear adjustment range of ±200 mV. The 2 V reference may also be adjusted but only in the positive direction.

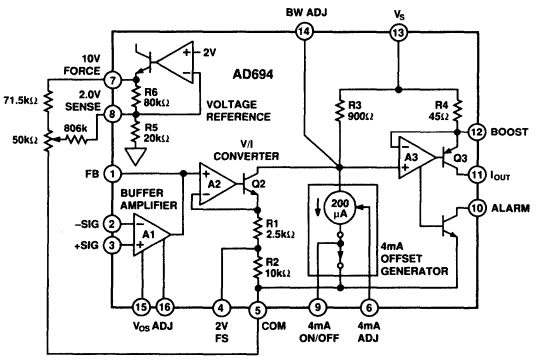


Figure 9. 10 V Reference Output Adjustment

Other reference voltages can be programmed by adding external resistors. For example, a resistor placed in parallel with R5 can be added to boost the reference output as high as 20 V. Conversely, a resistor in parallel with R6 can be used to set the reference voltage to a value between 2 V and 10 V. The output voltage V_{REF} = 2 V (R6 + R5) / R5. In choosing external adjustment resistors remember that the internal resistors, while ratio matched to a high degree of accuracy, have an absolute resistor tolerance of only ±10%. Be prepared to compensate for this if a precise voltage other than the precalibrated values of 2 V or 10 V is required.

BANDWIDTH CONTROL

The bandwidth of the AD694 can be limited to provide noise filtering. This is achieved by connecting an external capacitor from BW ADJ (Pin 14) to V_S (Pin 13) as shown in Figure 10. To program the bandwidth, substitute the desired bandwidth in Hz, into the formula below to determine the required capacitor.

$$C = 1 \text{ farad Hz } \Omega / (2 \pi 900 \Omega BW)$$

The bandwidth chosen will vary ±10% due to internal resistor tolerance, plus an additional amount due to capacitor tolerance.

This method of bandwidth control is not recommended as a way to filter large high frequency transients in the input signal. It is recommended that frequencies greater than the BW of the buffer amplifier be eliminated with an input filter to avoid rectification of noise by the input amplifiers.

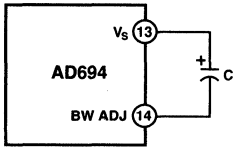


Figure 10. Noise Filtering with an External Capacitor

BUFFER AMPLIFIER OFFSET ADJUST

The buffer amplifier input voltage offset has been laser trimmed to a high degree of accuracy; however, there may be occasions when an offset trim is desired. Figure 11 shows the adjustment method; a trim range of greater than ±2.5 mV is available with this scheme. It is not recommended that this adjustment method be used to affect the 4 mA offset current as the trim will induce offset drift into the buffer amplifier. The buffer amplifier will drift approximately 1μV/°C for each 300 μV of induced offset. To adjust the 4 mA offset current refer to the section "ADJUSTING ZERO."

ALARM CIRCUIT

The AD694 has an alarm circuit which warns of open circuit conditions at I_{OUT} (Pin 11), or of attempts to drive the voltage at I_{OUT} higher than V_S-2 V. The alarm transistor will pull down if an out of control condition is sensed. The alarm current is limited to about 20 mA.

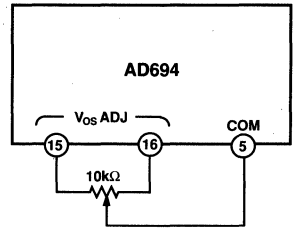


Figure 11. Buffer Amplifier V_{OS} Adjustment

Figure 12 shows a typical application. In a digital/analog system the alarm can provide a TTL signal to a controller. The collector of the alarm transistor is tied to the system logic supply through a 20 kΩ pull-up resistor. The alarm is off in normal operation and the voltage at the alarm pin is high. In the event that the wire from I_{OUT} (Pin 11) is opened, or if a large input overdrive forces I_{OUT} too close to V_S, then the alarm pin is driven low. This configuration is compatible with CMOS or TTL logic levels. The alarm transistor can also be used to directly drive an LED or other indicators.

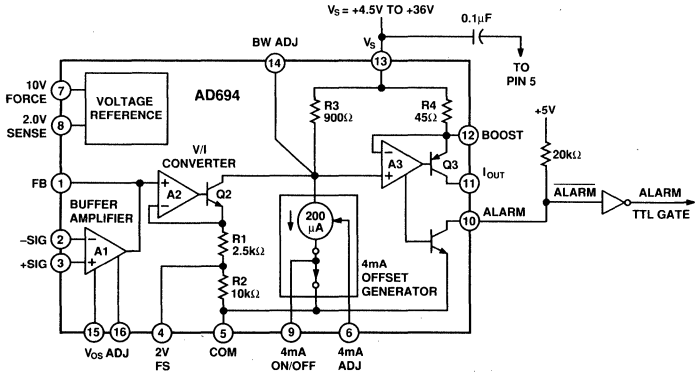


Figure 12. Using the Alarm to Drive a TTL Gate

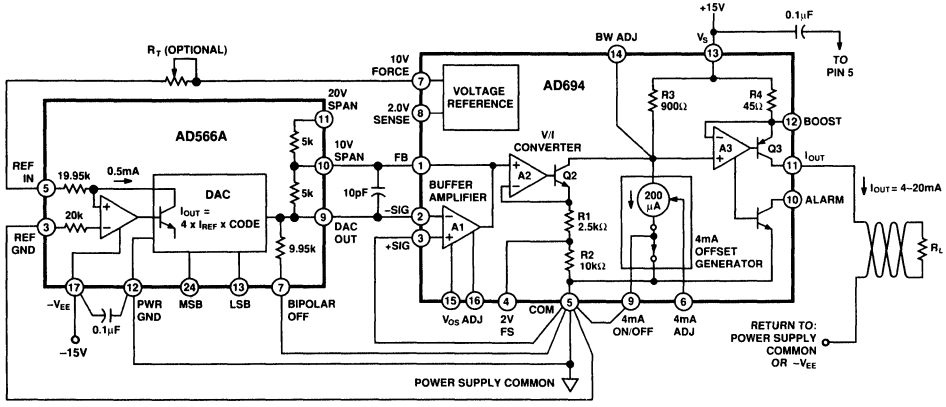


Figure 13. Digital to 4–20 mA Interface Using a Current Steering DAC

APPLICATIONS

CURRENT OUTPUT DAC INTERFACE

The AD694 can be easily interfaced to current output DACs such as the AD566A to construct a digital to 4–20 mA interface as shown in Figure 13. The AD694 provides the voltage reference and the buffer amplifier necessary to operate the DAC. Only simple connections are necessary to construct the circuit. The 10 V reference of the AD694 supplies reference input of the AD566. The buffer amplifier converts the full-scale current to +10 V utilizing the internal resistors in the DAC; therefore the AD694 is configured for a 10 V full-scale input. A 10 pF capacitor compensates for the 25 pF output capacitance of the DAC. An optional 100 Ω trim resistor, (R_T), allows the full-scale to be trimmed, a 50 Ω resistor may be substituted if a trim is not required; accuracy will be typically ±1 LSB and the trim does not affect the 4 mA offset. Care should be taken in managing the circuit grounds. Connections from AD694 Pins 9, 3 and AD566 Pins 3 and 7 should be as short as possible and to a single point close to Pin 5 of the AD694. Best practice would have separate connections to the star ground from each pin; this is essential for the AD566 power ground from Pin 12. The 4–20 mA output (Pin 11) must have a return path to the power ground. The return line from the load may be connected to the power ground, or to the −15 V supply based upon the size of the load to be driven, and on power dissipation considerations.

SINGLE SUPPLY DIGITAL TO 4–20 mA INTERFACE

A 12 bit input to 4–20 mA output interface can be constructed that operates on a single 15 V supply. The DAC is operated in its voltage switching mode; this allows the DAC, when supplied with a voltage reference of less than 2.5 V, to provide an output voltage that is proportional to the digital input code and ranges from 0 V to V_{REF}. The AD694 voltage reference is connected to supply 2 V and the input stage is set to a 2 V full scale; the input buffer amplifier serves to buffer the voltage output from the DAC. Connected in this manner a full-scale DAC input code will result in a 20 mA output and an all 0 code will result in a 4 mA output. The loading on the AD694 voltage reference is

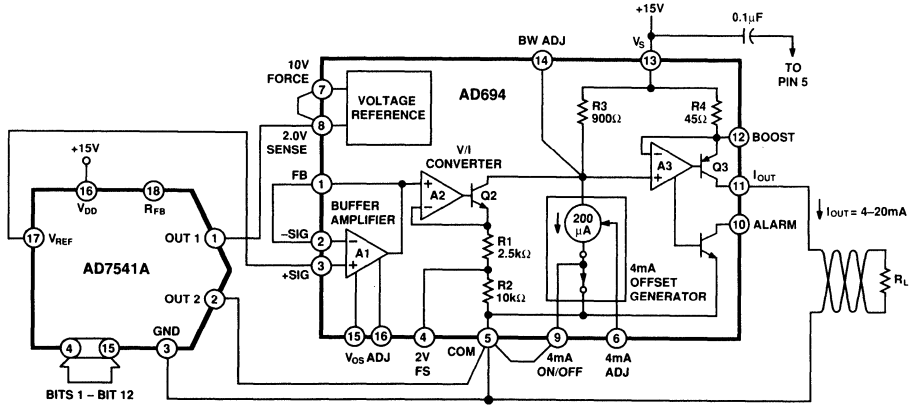


Figure 14. Single Supply Digital Input to 4–20 mA Output

code dependent, and the response time of the circuit will be determined by the reaction of the voltage reference. The supply voltage to the AD7541A should be kept close to 15 V. If V_S is reduced significantly from 15 V the differential nonlinearity of the DAC will increase and the linearity will be degraded.

In some applications it is desirable to have some under-range and over-range in the 4–20 mA output. For example, assume an over and under range capability of ±5% of span is needed, then the output current range corresponding to the full scale of the DAC is 3.2 mA to 20.8 mA. To accomplish this, the span of the AD694 would be increased 10% to 17.6 mA by adding a noninverting gain of 1.1 to the buffer amplifier. The 4 mA offset would then be reduced by 0.8 mA, by utilizing the adjustment scheme explained in "Adjusting 4 mA Zero." Then a digital input from all zero code to full scale would result in an output current of 3.2 mA to 20.8 mA.

LOW COST SENSOR TRANSMITTER

Sensor bridges typically output differential signals in the 10 mV to 100 mV full-scale range. With an AD694, a dual op amp, and some resistors, an instrumentation amplifier front end can be added which easily handles these types of low level signals.

The traditional 3 op amp instrumentation amplifier is built using an AD708, dual op amp for the front end, and the AD694's buffer amplifier is used for the subtractor circuit, as shown in Figure 15. The AD694's 2 V reference is used to provide a "ground" of 2 V that insures proper operation of the in amp over a wide common mode range. The reference pin of the subtractor circuit is tied to the 2 V reference (point C). A 2 kΩ pull-down resistor insures that the voltage reference will be able to sink any subtractor current. The 2 V FS (Pin 4) is attached to the 2 V reference; this offsets the input range of the V/I converter 2 volts positive, to match the "ground" of the in amp. The AD694 will now output a 4–20 mA output current for a 0 to 2 V differential swing across V_A. The gain of the in amp front end is adjusted so that the desired full-scale input signal at V_{IN} results in a V_A of 2 V. For example a sensor that has a 100 mV full scale will require a gain of 20 in the front end. The gain is determined according to the equation:

$$G = [2R_S / Rg] + 1$$

The circuit shown, will convert a positive differential signal at V_{IN} to a 4–20 mA current. The circuit has common-mode range of 3 V to 8 V. The low end of the common-mode range is limited by the AD708's ability to pull down on R_S. A single supply amplifier could be used instead to extend the common-mode range down to about 1.5 V.

As shown, the circuit handles positive differential signals, (V_{IN} positive). To handle bipolar differential signals (V_{IN} is positive or negative), the reference pin of the in amp (point C) must be offset positively from the 2 V reference. For example, disconnected point C from the 2 V reference and connecting it to a 3 V source would result in a V_A of 1 V, (or half scale) for a zero volt differential input from the sensor.

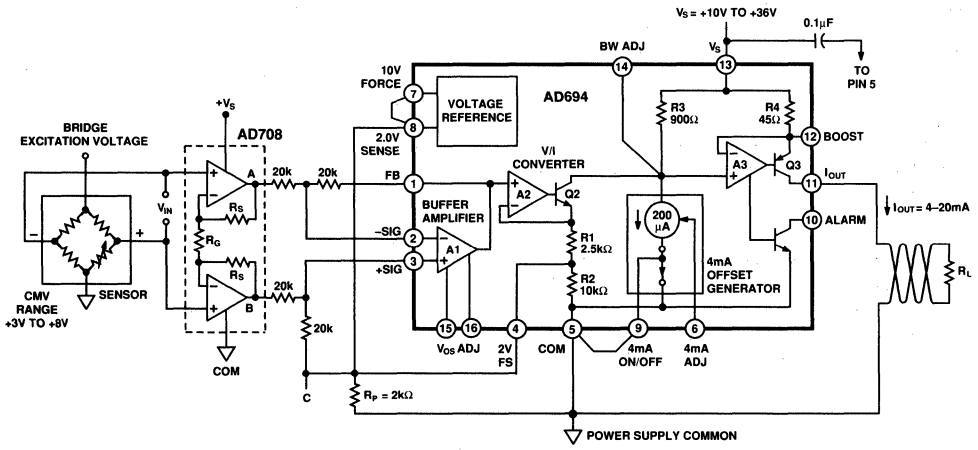


Figure 15. Low Cost, Single Supply, 3-Wire Sensor Transmitter

ANALOG DEVICES

Isolated, Loop-Powered Voltage-to-Current Converter

1B21

FEATURES
- **Wide Input Range: 0-1V to 0-10V**
- **High CMV Isolation: 1500V rms**
- **Programmable Output Ranges: 4mA to 20mA**
  0 to 20mA
- **Load Resistance Range: 0 to 1.35kΩ max**
- **High Accuracy**
  - **Low Offset Tempco: ±300nA/°C**
  - **Low Gain Tempco: ±50ppm/°C**
  - **Low Nonlinearity: ±0.02%**
  - **High CMR: 90dB min**
- **Small Package: 0.7″ × 2.1″ × 0.35″**
- **Meets IEEE Std. 472: Transient Protection (SWC)**

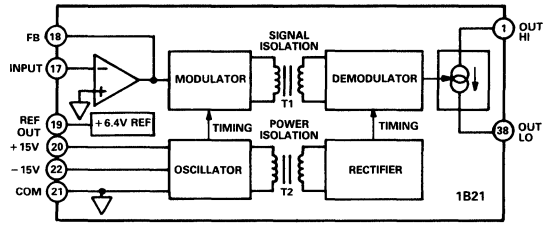
APPLICATIONS
- **Multichannel Process Control**
- **D/A Converter – Current Loop Interface**
- **Analog Transmitters and Controllers**
- **Remote Data Acquisition Systems**

GENERAL DESCRIPTION

The 1B21 is an isolated voltage-to-current converter that incorporates a unique circuit design utilizing transformer based isolation and automated surface mount manufacturing technology. It provides an unbeatable combination of versatility and performance in a compact plastic package. Designed for industrial applications, it is especially suited for harsh environments with extremely high common-mode interference.

Functionally, the V/I converter consists of four basic sections: input conditioning, modulator, demodulator and current source (1B21 Functional Block Diagram). The input is a resistor programmable gain stage that accepts a 0-1V to 0-10V voltage input. This maps into a 0 to 20mA output or can be offset by 20% using the internal reference for 4mA to 20mA operation. The high level signal is modulated and passed across the barrier which provides complete input to output galvanic isolation of 1500V rms continuous by the use of transformer coupling techniques. Nonlinearity is an excellent ±0.05% max.

1B21 FUNCTIONAL BLOCK DIAGRAM



Designed for multichannel applications, the 1B21 requires an external loop supply and can accept up to 30V max. This would provide a loop compliance of 27V, which is sufficient to drive a 1.35kΩ load resistance.

The 1B21 is fully specified over −25°C to +85°C and operates over the industrial (−40°C to +85°C) temperature range.

DESIGN FEATURES AND USER BENEFITS

High CMV Isolation: The 1B21 features high input to output galvanic isolation to eliminate ground loops and offer protection against damage from transients and fault voltages. The isolation barrier will withstand continuous CMV of 1500V rms and meets the IEEE Standard for Transient Voltage Protection (Std. 472-SWC).

Small Size: The 1B21 package size (0.7″ × 2.1″ DIP) makes it an excellent choice in multichannel systems for maximum channel density. The 0.35″ height also facilitates applications with limited board clearance.

Ease of Use: Complete isolated voltage-to-current conversion with minimum external parts required to get a conditioned current signal. No external buffers or drivers are required.

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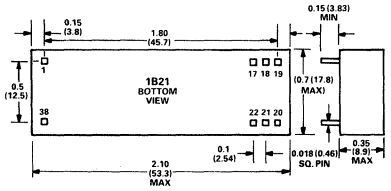
SPECIFICATIONS (typical at +25°C and V_S = ±15V unless otherwise noted)

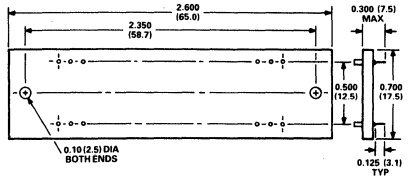
Model	1B21AN
INPUT SPECIFICATIONS	
Input Range	0 to +10V
Full-Scale Input	+1V min to +10V max
Input Bias Current	±30pA (±400pA max)
OUTPUT SPECIFICATIONS	
Current Output Range	4mA to 20mA, 0 to 20mA
Load Compliance at V_{LOOP} = 30V	27V min
Max Output Current @ Input Overload	25mA
Output Noise, 100Hz Bandwidth	1μA p-p
NONLINEARITY (% of Span)	±0.02% (±0.05% max)
ISOLATION	
CMV, Input to Output Continuous	1500V rms
CMR, @ 60Hz	90dB min
Transient Protection	IEEE-STD 472 (SWC)
ACCURACY	
Warm-Up Time to Rated Performance	5 min
Total Output Error @ +25°C (Untrimmed)	
Offset (V_{IN} = 0V)[1]	±100μA
Span (V_{IN} = +10V)	±0.6% FSR
vs. Temperature (−25°C to +85°C)	
Offset[2]	±300nA/°C
Span	±50ppm/°C
REFERENCE OUTPUT	
Voltage	+6.4V dc
Output Error	±1.5% max
Temperature Coefficient	±20ppm/°C max
DYNAMIC RESPONSE	
Settling Time to 0.1% of F.S. for 10V Step	9ms
Small Signal Bandwidth	100Hz
POWER SUPPLY	
Input Side	
Operating Voltage	±15V ±5%
Quiescent Current	
+15V Supply	10mA
−15V Supply	5mA
Power Supply Rejection	±0.01%/V
Loop Side	
Operating Voltage	+15V to +30V
Maximum Current	25mA
ENVIRONMENTAL	
Temperature Range	
Rated Performance	−25°C to +85°C
Operating	−40°C to +85°C
Storage	−40°C to +85°C
Relative Humidity, Noncondensing	0 to 95% @ +60°C
CASE SIZE	0.7" × 2.1" × 0.35" (17.8 × 53.3 × 8.9)mm

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1060 MATING SOCKET



PIN DESIGNATIONS

PIN	FUNCTION
1	OUT HI
17	IN
18	FB
19	REF
20	+15V
21	COM
22	−15V
38	OUT LOW

NOTES

[1]For 0-20mA mode. For 4-20mA mode an additional 60μA is contributed by the ±1.5% reference error on the 4mA output.

[2]For a complete discussion of the temperature effects of the offset resistor and reference refer to "Using the 1B21" section.

Specifications subject to change without notice.

INSIDE THE 1B21

Referring to the functional block diagram, the ±15V power inputs provide power to both the input side circuitry and the power oscillator. The 25kHz power oscillator provides both the timing information for the signal modulator and drives transformer T2 for the output side power supplies. The secondary winding of T2 is full wave rectified and filtered to create the output side power.

The input stage is configured as an inverting amplifier with three user supplied resistors for gain, offset and feedback. The conditioned signal is modulated to generate a square wave with a peak-to-peak amplitude proportional to V_{IN}. This signal drives the signal transformer T1. An internal reference with a nominal output voltage of +6.4V and tempco of ±20ppm/°C is provided to develop a 4mA offset for 4mA to 20mA current loop applications.

After passing through signal transformer T1, the amplitude modulated signal is demodulated and filtered by a single pole filter. Timing information for the output side is derived from the power transformer T2. The filtered output provides the control signal for the voltage-to-current converter stage. An external power supply is required in series with the load to complete the current loop.

USING THE 1B21

Input Configurations: The 1B21 has been designed with a flexible input stage for a variety of input and output ranges. The basic interconnection for setting gain and offset is shown in Figure 1. The output of the internal amplifier is constrained to 0 to −5V, which maps into 0 to 20mA across the isolation barrier. Thus to create a 4mA offset at the output, the input amplifier has to be offset by 1V.

For example, for 0 to 20mA operation the transfer function for the input stage is:

$$5/V_{IN} = R_F/R_I$$

and no offset resistor is needed. For 4mA to 20mA operation we get:

$$4/V_{IN} = R_F/R_I$$

which maps the input voltage into a 4V span. To create a 1V offset at the output of the internal amplifier (4mA at the output of the 1B21) a current derived from the reference can be fed into the summing node. The offset resistor (for a 1V output offset) will be given by the equation: $R_O = 6.4R_F$. For most applications it is recommended that R_F be in the 25kΩ ±20% range. Resistor values for typical input and output ranges are shown in Table I.

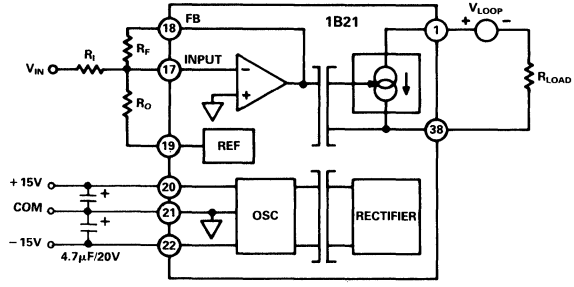


Figure 1. Basic Interconnections

Input Volts	Output mA	R_I kΩ	R_F kΩ	R_O kΩ
0-5	0-20	25	25	Open
0-10	0-20	50	25	Open
0-5	4-20	25	20	128
0-10	4-20	50	20	128
1-5	4-20	25	25	Open

Table I. Resistor Values for Typical Ranges

Adjustments: Figure 2 is an example of using potentiometers for trimming gain and offset for a 0-5V input and 0 to 20mA output. The network for offset adjustment keeps the resistors relatively small to minimize noise effects while giving a sensitivity of ±1% of span. For more adjustment range, resistors smaller than 274k can be used. Resistor values from Table I can be substituted for other input and output ranges.

In general, any bipolar voltage can be input to the 1B21 as long as it is offset to meet the 0 to −5V constraint of the modulator and the input signal range is 1V minimum.

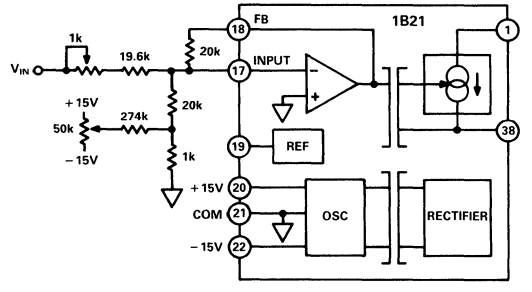


Figure 2. Offset and Span Adjustment

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TC Considerations of External Resistors: The specifications for gain and offset temperature coefficient (TC) for the 1B21 exclude the effects of external components. The total gain TC for the circuit in Figure 1 is:

Gain TC = 1B21 Gain TC + (Tracking TC of R_F and R_I)

The offset TC is also affected by the thermal stability of the internal voltage reference and its contribution is:

Ref TC = $(V_{REF})(R_F/R_O)(4mA/V)$(TC of V_{REF} + Tracking TC of R_F and R_O)$/1 \times 10^6$

Total Offset TC = 1B21 Offset TC + Ref TC

Specifically using R_F, R_I and R_O from Case 3 in Table I, with absolute TCs of ±25ppm/°C we get:

Gain TC = 50 + (25 + 25) = 100ppm/°C

Offset TC = $300 + (6.4V)(20k/128k)(4mA/V)(20 + 25 + 25)/1 \times 10^6$

= ±580nA/°C

Similarly, when using a resistor network with a tracking spec of ±5ppm/°C, the total gain TC would be ±55ppm/°C and the total offset TC would be ±400nA/°C.

APPLICATIONS

Output Protection: In many industrial applications it may be necessary to protect the current output from accidental shorts to ac line voltages in addition to high common-mode voltages and short circuits to ground. The circuit shown in Figure 3 can be used for this purpose. The maximum permissible load resistance will be lowered by the fuse resistance (typically 8Ω) when protection circuitry is utilized.

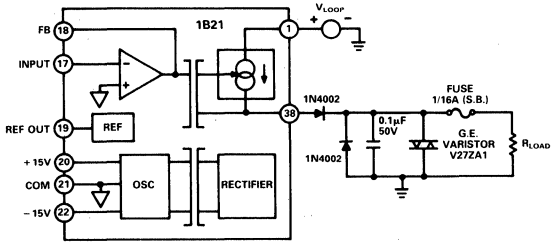


Figure 3. Output Protection Circuitry

Low Drift Input Network: Figure 4 shows a configuration suitable for applications where errors have to be minimized over a wide temperature range. A temperature tracking network such as a 50k Beckman (PN 698-3R50KD) can be used to implement both offset and gain for either 0 to 20mA or 4mA to 20mA current loops. For 0-10V signals either IN1 or IN2 can be used for input. For 0-5V signals, jumper IN1 to IN2. Similarly, for 4mA to 20mA operation the 4mA node should be jumpered to OFFSET, while for 0 to 20mA it should be tied to COM.

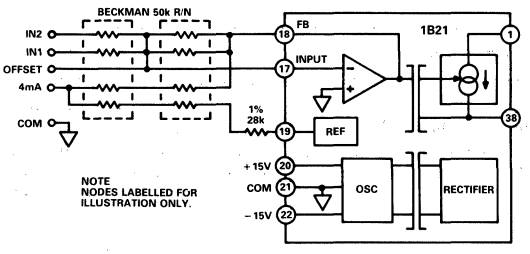


Figure 4. Low Tempco Resistor Network Configuration

Multiloop Isolation: Multiple 1B21s can be connected to a single loop supply in parallel as shown in Figure 5. The amperage of the loop supply should be sufficient to drive all the loops at full-scale output.

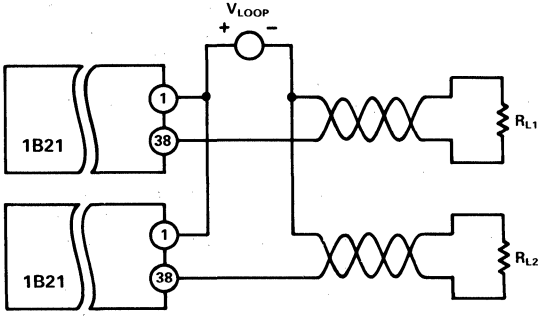


Figure 5. Multiple 1B21s with Single Loop Supply

ANALOG DEVICES

Programmable, Isolated Voltage-to-Current Converter

1B22

FEATURES

Internal Isolated Loop Supply Drives 1000 Ω Load
Pin Programmable Inputs: 0 to +5 V or 0 to +10 V
Pin Programmable Outputs: 4 to 20 mA or 0 to 20 mA
High CMV Isolation: 1500 V RMS
Normal Mode Output Protection: 240 V RMS
High Accuracy
Low Offset Tempco: ±300 nA/°C
Low Gain Tempco: ±50 ppm/°C
Low Nonlinearity: ±0.02%
High CMR: 90 dB min
Small Package: 1.0″×2.10″×0.35″
Meets IEEE STD 472: CMV Transient Protection (SWC)

APPLICATIONS

Multichannel Process Control
D/A Converter – Current Loop Interface
Analog Transmitters and Controllers
Remote Data Acquisition Systems

GENERAL DESCRIPTION

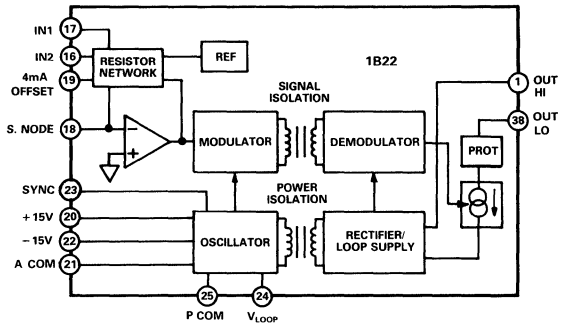
The 1B22 is an isolated voltage-to-current converter that incorporates transformer isolation to achieve high performance and automated surface mount manufacturing for low cost and increased reliability. Designed for industrial applications, it is especially suited for harsh environments with extremely high common mode interference. With programmable inputs and outputs, the 1B22 provides an unbeatable combination of versatility and performance in a compact plastic package.

Functionally, the V/I converter consists of four basic sections: input conditioning, modulator/demodulator, isolated loop supply and current source (Figure 1). The 1B22 is pin programmable for 0 to +5 V or 0 to +10 V inputs and 0 to 20 mA or 4 to 20 mA outputs using an internal resistor network. It can also be set by an external resistor to accept 0 to +1 V to 0 to +10 V inputs. Transformer coupling provides 1500 V rms galvanic isolation between the inputs and the current loop. Nonlinearity is an excellent ±0.05% max.

Loop power is generated internally through a dc/dc converter and is also isolated from the input side (1500 V rms). Loop compliance voltage is dependent on the voltage supplied to the 1B22, and with V_{LOOP} = 28 V, it is sufficient to drive a 1000 Ω load.

The 1B22 is fully specified over −25°C to +85°C and operates over the industrial (−40°C to +85°C) temperature range.

1B22 FUNCTIONAL BLOCK DIAGRAM



DESIGN FEATURES AND USER BENEFITS

Isolated Loop Power: Internal loop supply completely isolates the loop from the input terminals (1500 V rms) and provides the capability to drive 0 to 1000 Ω loads. This eliminates the need for an external dc/dc converter.

Ease of Use: The 1B22 offers complete isolated voltage-to-current conversion with minimum external parts required to get a conditioned current signal. No external buffers or drivers are required.

High CMV Isolation: The 1B22 features high input to output galvanic isolation to eliminate ground loops and offer protection against damage from transients and fault voltages. The isolation barrier will withstand continuous CMV of 1500 V rms and meets the IEEE Standard for Common Mode Voltage Transient Protection (STD 472-SWC).

Small Size: The 1B22 package size (1.0″×2.1″ DIP) makes it an excellent choice in multichannel systems for maximum channel density. The 0.35″ height also facilitates applications with limited board clearance.

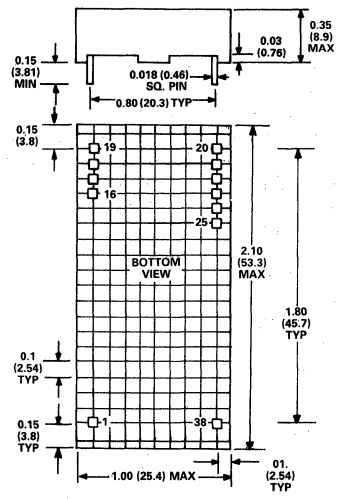
SPECIFICATIONS (typical @ +25°C and V_S = ±15 V, V_{LOOP} = +24 V, unless otherwise noted)

Model	1B22AN
INPUT SPECIFICATIONS	
Factory Calibrated, User Selectable	0 to +5 V, 0 to +10 V
Input Impedance	
0 to +10 V Input Range	50 kΩ
0 to +5 V Input Range	25 kΩ
OUTPUT SPECIFICATIONS	
Current Output Range, User Selectable	4 to 20 mA, 0 to 20 mA
Load Compliance Range, V_{LOOP}=+15 V	8 V min
V_{LOOP}=+28 V	20 V min
Maximum Output Current @ Input Overload	30 mA
Output Noise, 100 Hz Bandwidth	300 nA p–p
NONLINEARITY (% OF SPAN)	±0.02% (±0.05% max)
ISOLATION	
CMV, Input to Output Continuous	1500 V rms max
CMR, @ 60 Hz	90 dB min
Normal-Mode Output Protection	240 V rms continuous
CMV Transient Protection	IEEE - STD 472 (SWC)
ACCURACY	
Warm-Up Time to Rated Performance	5 min
Total Output Error @ +25°C	
Offset (V_{IN} = 0 V)	±60 µA
Span (V_{IN} = +10 V)	±0.7% Full Scale
vs. Temperature (−25°C to +85°C)	
Offset	±300 nA/°C
Span	±50 ppm/°C
DYNAMIC RESPONSE	
Settling Time to 0.1% of FS for 10 V Step	9 ms
Small Signal Bandwidth	400 Hz
POWER SUPPLY	
Bipolar Input Supplies	
Operating Voltage	±15 V ±5%
Quiescent Current	±7.5 mA
Power Supply Rejection	±0.01%/V
Loop Supply	
Operating Voltage	+14 V to +30 V
Operating Current, at Full-Scale Output	25 mA
Loop Supply Rejection	±0.005%/V
ENVIRONMENTAL	
Temperature Range	
Rated Performance	−25°C to +85°C
Operating	−40°C to +85°C
Storage	−40°C to +85°C
Relative Humidity, Noncondensing	0 to 95% @ 60°C
CASE SIZE	1.0″×2.1″×0.35″

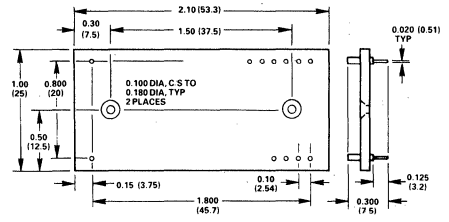
NOTE
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1225 MATING SOCKET



PIN DESIGNATIONS

PIN	FUNCTION
1	OUT HI
16	IN2
17	IN1
18	S. NODE
19	4mA OFFSET
20	+15V
21	ANA COM
22	−15V
23	SYNC
24	V_{LOOP}
25	POWER COM
38	OUT LOW

INSIDE THE 1B22

The 1B22 produces an isolated 4 to 20 mA or 0 to 20 mA output current which is proportional to the input voltage and independent of the output load resistance (Figure 1). The input stage is configured as an inverting amplifier with a resistor network to provide pin-strappable input ranges of 0 to +5 V and 0 to +10 V and output ranges of 0 to 20 mA and 4 to 20 mA. The conditioned signal is modulated to generate a square wave that drives transformer T1. The peak-to-peak amplitude of the signal is proportional to V_{IN}. An internal, high stability reference with a nominal output voltage of +6.4 V is used to develop a 4 mA offset for the 4 to 20 mA current loop output.

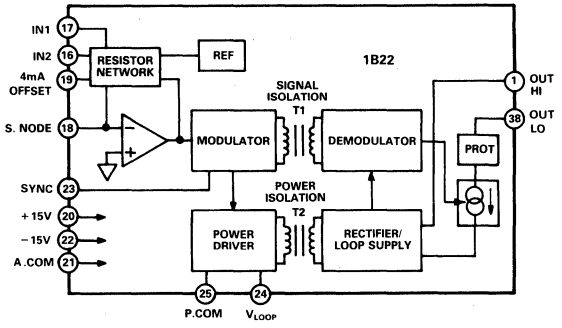


Figure 1. 1B22 Functional Block Diagram

After passing through signal transformer T1, the amplitude modulated signal is demodulated and filtered by a single pole filter. This filtered output is the control signal for the voltage-to-current converter stage. Timing information for the demodulator is derived from the power transformer T2. The 1B22 outputs are protected from accidental shorts to ac line voltages up to 240 V rms. Combined with 1500 V input to output isolation, the 1B22 provides unbeatable protection against transients, wiring errors and current loop short circuits to power lines.

The dc-dc converter consists of a power driver, power transformer T2, a full wave rectifier and a filter. The dc-dc converter provides the power for the output circuitry as well as the isolated compliance voltage for the loop. This voltage is proportional to V_{LOOP} on the input side. The 1B22 requires ±15 V supplies to power the input side circuitry and a +14 V to +30 V supply for the dc-dc converter.

USING THE 1B22

Basic Interconnections: The 1B22 may be applied to achieve rated performance as shown in Figure 2. For 0 to 10 V signals either IN1 or IN2 can be used for input; for 0 to +5 V signals jumper IN1 to IN2. Similarly, for 4 to 20 mA operation the 4 mA OFFSET node should be jumpered to the S. NODE, while for 0 to 20 mA it should be tied to COM. Figure 3 shows the functional diagram of the resistor network used in the 1B22.

For applications where a separate loop supply is not available, the ±15 V supplies can be used by connecting +15 V to V_{LOOP} (Pin 24) and COM to P.COM (Pin 25). For additional compliance voltage, P.COM can be connected to −15 V to drive higher loads.

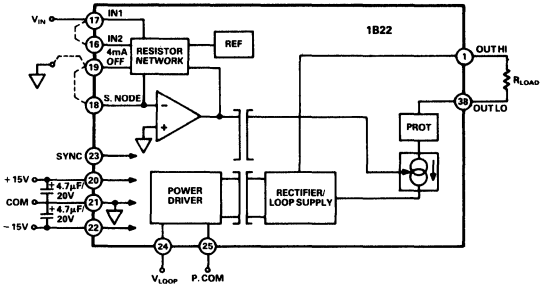


Figure 2. Basic Interconnections

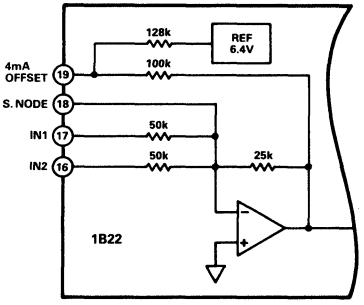


Figure 3. Internal Resistor Network

Optional Trim Adjustments: Figure 4 is an example of using potentiometers for trimming gain and offset for a 0 to +10 V input and 4 to 20 mA output. The network for offset adjustment keeps the resistors relatively small to minimize noise effects while giving a sensitivity of ±1% of span. For more adjustment range, resistors smaller than 274 kΩ can be used.

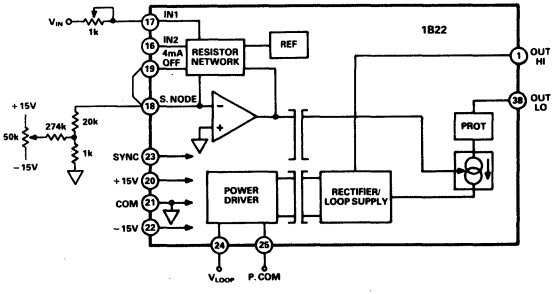


Figure 4. Optional Offset and Span Adjustment

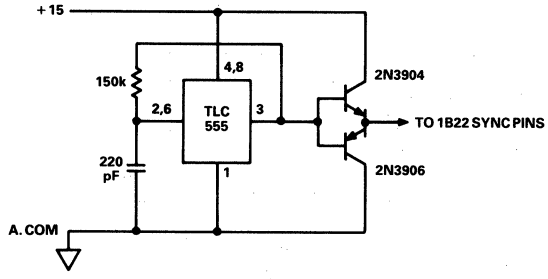


Figure 5. Multiple 1B22s' Synchronization

Synchronizing Multiple 1B22s: In applications where multiple 1B22s are used in close proximity, radiated individual oscillator frequencies may cause "beat frequency" related output errors. These errors can be eliminated by driving the SYNC pins of all the units with a 40 kHz clock circuit at 50% duty cycle (Figure 5). The SYNC input typically has an input impedance of 150 kΩ‖180 pF.

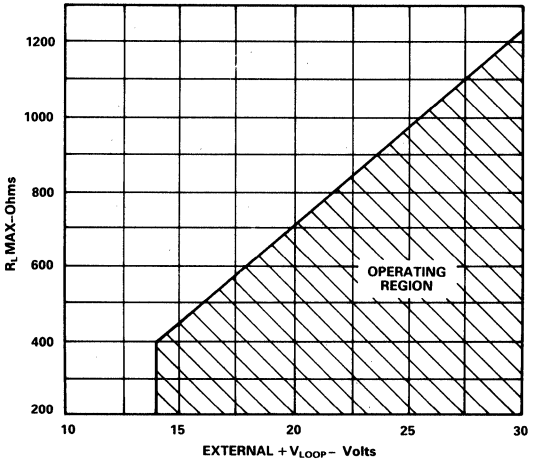


Figure 6. Loop Supply vs. Load

Loop Supply Requirements: The 1B22 design allows flexible loop supply options. The loop supply voltage required for any value of load resistance can be calculated from the following equation:

$$V_{LOOP} = \frac{2R_L + 780}{106}$$

This value allows for approximately 10% overrange capability. The graph in Figure 6 shows the relationship between supply voltage and load resistance.

APPLICATIONS

Isolated D/A Converter: The 1B22 offers total ground isolation and protection from high voltage transients in interfacing D/A converters to standard 4 to 20 mA current loops. The D/A converter, such as the Analog Devices' 12-bit AD7245 DACPORT™, should be connected for operation on the unipolar 0 to +10 V output range. This is shown in Figure 7.

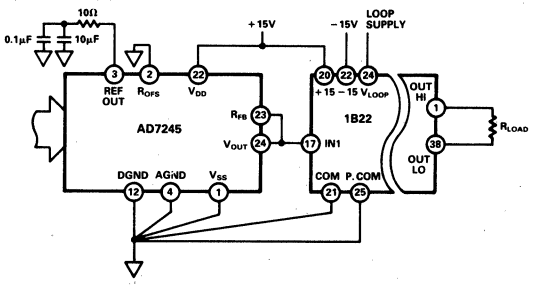


Figure 7. D/A Converter – Isolated 4–20 mA Interface

Pressure Transmitter: In Figure 8, the 1B22 is used in a pressure transmitter application to provide complete input-output isolation and avoid signal errors due to ground loop currents. The process pressure is monitored with a strain gage type pressure transducer interfaced by the Analog Devices' 1B32 transducer signal conditioner. The high level voltage output of the 1B32 is converted to the isolated 4 to 20 mA current for transmission to a remote recorder or indicator.

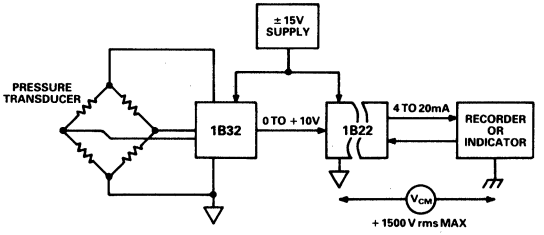


Figure 8. Isolated Pressure Transmitter

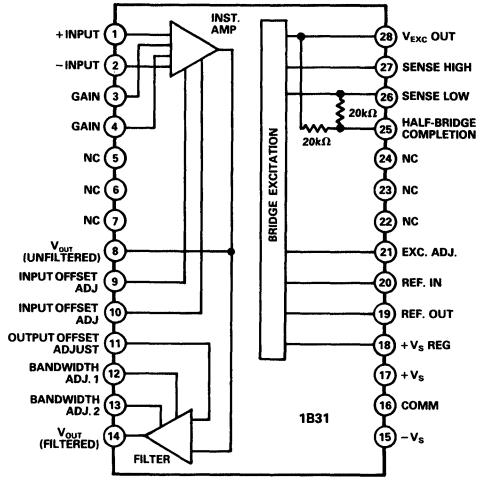
Wide Bandwidth Strain Gage Signal Conditioner

1B31

FEATURES
- **Low Cost**
- **Complete Signal-Conditioning Solution**
- **Small Package: 28-Pin Double DIP**
- **Internal Half-Bridge Completion Resistors**
- **Remote Sensing**
- **High Accuracy**
  - **Low Drift: ±0.25μV/°C**
  - **Low Noise: 0.3μV p-p**
  - **Low Nonlinearity: ±0.005% max**
  - **High CMR: 140dB min (60Hz, G = 1000V/V)**
- **Programmable Bridge Excitation: +4V to +15V**
- **Adjustable Low Pass Filter: f_C = 10Hz to 20kHz**

APPLICATIONS
- **Measurement of: Strain, Torque, Force, Pressure**
- **Instrumentation: Indicators, Recorders, Controllers**
- **Data Acquisition Systems**
- **Microcomputer Analog I/O**

1B31 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 1B31 is a high performance strain gage signal-conditioning component that offers the industry's best price/performance solution for applications involving high-accuracy interface to strain gage transducers and load cells. Packaged in a 28-pin double DIP using hybrid technology, the 1B31 is a compact and highly reliable product. Functionally, the signal conditioner consists of three sections: a precision instrumentation amplifier, a two-pole low pass filter, and an adjustable transducer excitation.

The instrumentation amplifier (IA) section features low input offset drift of ±0.25μV/°C (RTI, G = 1000V/V) and excellent nonlinearity of ±0.005% max. In addition, the IA exhibits low noise of 0.3μV p-p typ (0.1Hz-10Hz), and outstanding 140dB min common-mode rejection (G = 1000V/V, 60Hz). The gain is programmable from 2V/V up to 5000V/V by one external resistor.

The two-pole low pass filter offers a 40dB/decade roll-off from 1kHz to reduce high frequency noise and improve system signal-to-noise ratio. The corner frequency is adjustable downwards by external capacitors and upwards to 20kHz by three resistors. The output voltage can also be offset by ±10V with an external potentiometer to null out dead weight.

The 1B31's regulated transducer excitation stage features low output drift (±0.004%/°C typ) and can drive 120Ω or higher resistance load cells. The excitation is preset at +10V and is adjustable from +4V and +15V. This section also has remote sensing capability to allow for lead-wire compensation in 6-wire bridge configurations. For half-bridge strain gages, a matched pair of thin-film 20kΩ resistors is connected across the excitation outputs. This assures temperature tracking of ±5ppm/°C max and reduces part count.

The 1B31 is available in a plastic package specified over the industrial (−40°C to +85°C) temperature range and will be available soon in a bottom-brazed ceramic package specified over the military (−55°C to +125°C) temperature range.

DESIGN FEATURES AND USER BENEFITS

Ease of Use: Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

Half-Bridge Completion: Matched resistor pair tracking to ±5ppm/°C max for half-bridge strain gage applications.

Remote Sensing: Voltage drops across the excitation lead-wires are compensated by the regulated supply, making 6-wire load-cell interfacing straightforward.

Programmable Transducer Excitation: Excitation source preset for +10V dc operation without external components. User-programmable from a +4V to +15V dc to optimize transducer performance.

Adjustable Low Pass Filter: The two-pole active filter (f_C = 1kHz) reduces noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency (10Hz to 20kHz).

13

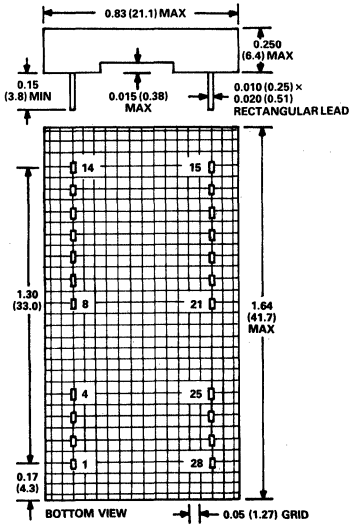
SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

Model	1B31AN	1B31SD†
GAIN[1]		
Gain Range	2 to 5000V/V	*
Gain Equation	$R_G = \frac{80k\Omega}{G-2}$	*
Gain Equation Accuracy, G≤1000V/V	±3%	*
Gain Temperature Coefficient[2]	±15ppm/°C (±25ppm/°C max)	*
Nonlinearity	±0.005% max	*
OFFSET VOLTAGES[1]		
Total Offset Voltage, Referred to Input		
Initial, @ +25°C (Adjustable to Zero)		
G = 2V/V	±2mV (±10mV max)	*
G = 1000V/V	±50μV (±200μV max)	*
Warm-Up Drift, 5 min., G = 1000V/V	Within ±1μV of final value	*
vs. Temperature		
G = 2V/V	±25μV/°C (±50μV/°C max)	*
G = 1000V/V	±0.25μV/°C (±2μV/°C max)	*
At Other Gains	$\left(\pm 2 \pm \frac{100}{G}\right)\mu V/°C$	*
vs. Supply		
G = 2V/V	±50μV/V	*
G = 1000V/V	±0.5μV/V	*
Output Offset Adjust Range	±10V min	*
INPUT BIAS CURRENT		
Initial @25°C	±10nA (±50nA max)	*
vs. Temperature	±25pA/°C	*
INPUT DIFFERENCE CURRENT		
Initial @ +25°C	±5nA (±20nA max)	*
vs. Temperature	±10pA/°C	*
INPUT IMPEDANCE		
Differential	1GΩ‖4pF	*
Common Mode	1GΩ‖4pF	*
INPUT VOLTAGE RANGE		
Linear Differential Input (V_D)	±5V	*
Maximum CMV Input	$\pm\left(12 - \frac{G \times V_D}{4}\right)V$ max	*
CMR, 1kΩ Source Imbalance		
G = 2V/V, dc to 60Hz	86dB	*
G = 100V/V to 5000V/V		
1kHz Bandwidth[3]		
@ dc to 60Hz	110dB min	*
10Hz Bandwidth[4]		
@ dc	110dB min	*
@ 60Hz	140dB min	*
INPUT NOISE		
Voltage, G = 1000V/V		
0.1Hz to 10Hz	0.3μV p-p	*
10Hz to 100Hz	1μV p-p	*
Current, G = 1000V/V		
0.1Hz to 10Hz	60pA p-p	*
10Hz to 100Hz	100pA p-p	*
RATED OUTPUT[1]		
Voltage, 2kΩ Load, min	±10V	*
Current	±5mA	*
Impedance, dc to 2Hz, G = 2V/V to 1000V/V	0.5Ω	*
Load Capacitance	1000pF	*
Output Short-Circuit Duration	Indefinite	*
DYNAMIC RESPONSE[1]		
Small Signal Bandwidth −3dB, G = 2V/V to 1000V/V	1kHz	*
Slew Rate	0.05V/μs	*
Full Power	350Hz	*
Settling Time, G = 2V/V to 1000V/V, ±10V Output, Step to ±0.1%	2ms	*
LOW PASS FILTER		
Number of Poles	2	*
Gain (Pass Band)	−2V/V	*
Cutoff Frequency (−3dB Point)	1kHz	*
Roll-Off	40dB/decade	*

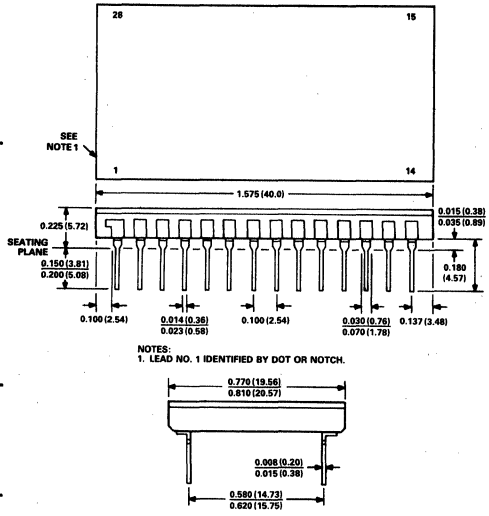
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic Package (N)



Ceramic Package (D)



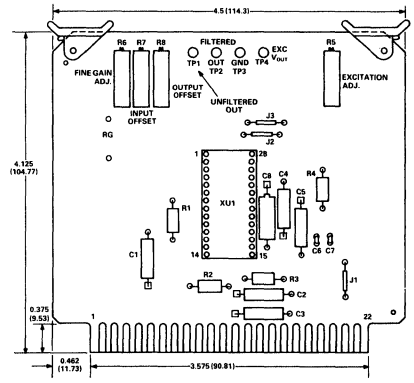
PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+INPUT	15	$-V_S$
2	−INPUT	16	COMMON
3	GAIN	17	$+V_S$
4	GAIN	18	$+V_S$ REGULATOR
8	V_{OUT} (UNFILTERED)	19	REF OUT
9	INPUT OFFSET ADJ.	20	REF IN
10	INPUT OFFSET ADJ.	21	EXCITATION ADJ.
11	OUTPUT OFFSET ADJ.	25	HALF-BRIDGE COMP.
12	BANDWIDTH ADJ. 1	26	SENSE LOW
13	BANDWIDTH ADJ. 2	27	SENSE HIGH
14	V_{OUT} (FILTERED)	28	V_{EXC} OUT

Model	1B31AN	1B31SD†
BRIDGE EXCITATION		
Regulator Input Voltage Range	+9.5V to +28V	*
Output Voltage Range	+4V to +15V	*
Regulator Input/Output Voltage Differential	+3V to +24V	*
Output Current[5]	100mA max	*
Regulation, Output Voltage vs. Supply	±0.05%/V	*
Load Regulation, I_L = 1mA to 50mA	±0.1%	*
Output Voltage vs. Temperature	±0.004%/°C	*
Output Noise, 10Hz to 1kHz[6]	200μV p-p	*
Reference Voltage (Internal)	+6.8V ±5%	*
Internal Half-Bridge Completion		
Nominal Resistor Value	20kΩ ±1%	*
Temperature Tracking	±5ppm/°C max	*
POWER SUPPLY		
Voltage, Rated Performance	±15V dc	*
Voltage, Operating	±12V to ±18V dc	*
Current, Quiescent[7]	+10mA	*
ENVIRONMENTAL		
Temperature Range		
Rated Performance	−40°C to +85°C	−55°C to +125°C
Operating	−40°C to +85°C	−55°C to +125°C
Storage	−40°C to +100°C	−65°C to +150°C
Relative Humidity	0 to 95% @ +60°C	*
CASE SIZE	0.83" × 1.64" × 0.25" (21.1 × 41.7 × 6.350mm) max	0.81" × 1.57" × 0.23" (20.6 × 40.0 × 5.72mm)

NOTES
*Specifications same as 1B31AN.
†SD grade available in Spring 1988.
[1]Specifications referred to the filtered output at Pin 14.
[2]Exclusive of external gain setting resistor.
[3]Unadjusted filter setting.
[4]Filter cutoff frequency set with external capacitors.
[5]Derate from +50°C as shown in Figure 14.
[6]4.7μF capacitor from $V_{REF\ IN}$ (Pin 20) to COMM.
[7]Excluding bridge excitation's current, and with no loading on the output.
Specifications subject to change without notice.

AC1222 MOUNTING CARD



AC1222 CONNECTOR DESIGNATION

PIN	FUNCTION	PIN	FUNCTION
1	+INPUT	T	V_{EXC} OUT
2	−INPUT	U	SENSE HIGH
3	N/C	V	SENSE LOW
4	GAIN (3)	W	HALF-BRIDGE COMP.
5	GAIN (4)	X	REF OUT
6	V_{OUT} (UNFILTERED)	Y	REF IN
7	INPUT OFFSET ADJ. (9)	Z	EXC. ADJ.
8	INPUT OFFSET ADJ. (10)		
9	OUTPUT OFFSET ADJ.		
10	BANDWIDTH ADJ. 1		
11	BANDWIDTH ADJ. 2		
12	V_{OUT} (FILTERED)		
19	$-V_S$		
20	COMMON		
21	$+V_S$		
22	$+V_S$ REG		

The AC1222 mounting card is available for the 1B31. The AC1222 is an edge connector card with a 28-pin socket for plugging in the 1B31. In addition, it has provisions for installing the gain resistor and adjusting the bridge excitation voltage and cutoff frequency. Adjustment potentiometers for offset, fine gain and excitation are also provided. The AC1222 comes with a Cinch 251-22-30-160 (or equivalent) edge connector.

APPLICATIONS

The 1B31 can be interfaced easily and directly to a wide variety of transducers for precise measurement of strain, torque, force and pressure. For applications in harsh industrial environments, such characteristics as high CMR, low noise and excellent temperature stability make the 1B31 unsurpassed for use in indicators, recorders and controllers.

The combination of low cost, small size and high performance of the 1B31 allows the system designer to use one conditioner per channel. The advantages include significantly lower system noise and high resolution, and elimination of crosstalk and aliasing errors.

FUNCTIONAL DESCRIPTION

Model 1B31 is based on a two-stage amplifier design and an adjustable voltage regulator section, as shown in Figure 1. The front end is a low noise, low drift, instrumentation amplifier (IA) that is optimized to amplify low level transducer signals (from 2mV full scale) riding on high common-mode voltage (±9.5V). The gain of the IA is programmed by a single resistor (1V/V to 2500V/V) and the input offset nulled out by an external potentiometer across the offset adjust Pins 9 and 10. The inverted signal ($V_{-INPUT} - V_{+INPUT}$) is brought out to Pin 8 for applications such as vibration and torque testing where the unfiltered output is required.

The signal is also fed to an inverting Butterworth filter with a fixed gain of −2V/V. This two-pole filter is preset with a 1kHz

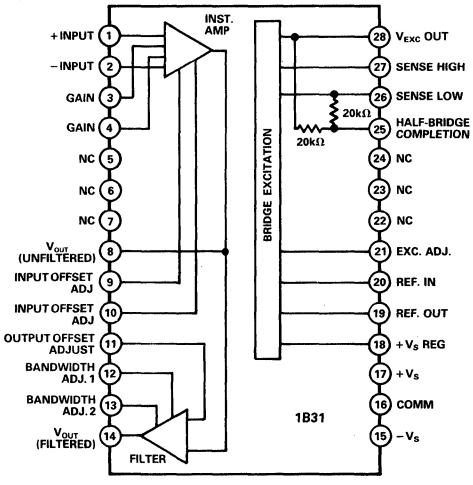


Figure 1. Block Diagram and Pinout

corner frequency which can be adjusted downwards to 10Hz by using two external capacitors or upwards to 20kHz by three resistors. This stage also provides a convenient means of adjusting output offset voltage (±10V) by connecting a 50kΩ potentiometer to Pin 11.

13

The bridge excitation section is an adjustable output, regulated supply with an internally provided reference voltage (+6.8V). It is configured as a gain stage with the output preset at +10V. The excitation voltage is increased by connecting a resistor between Pins 21 and 26, and decreased by connecting a resistor between Pins 19 and 20. Sense lines are provided to compensate for lead-wire resistance by effectively bringing the leads into the feedback loop.

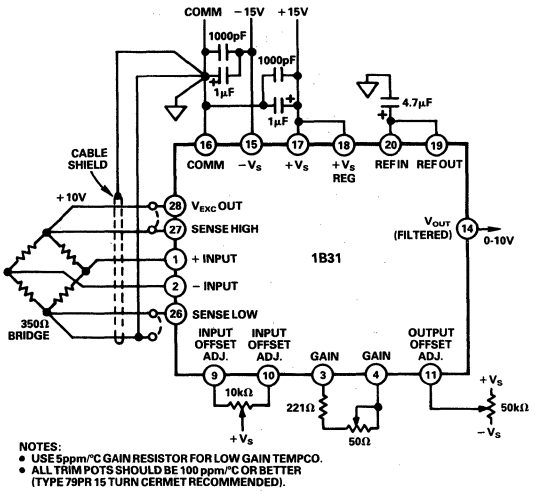
For half-bridge applications, two tracking thin-film resistors (20kΩ), ±5ppm/°C max) are connected from V_{EXC} OUT (Pin 28) to SENSE LOW (Pin 26).

OPERATING INSTRUCTIONS

Gain Setting: The differential gain, G, is determined by the equation:

$$G = 2 + \frac{80k\Omega}{R_G}$$

where R_G is connected between the GAIN terminals (Pins 3 and 4) of the IB31, as shown in Figure 2. For best performance, a low temperature coefficient (5ppm/°C) R_G is recommended. For fine span adjustment, a 50Ω potentiometer may be connected in series with R_G.



NOTES:
- USE 5ppm/°C GAIN RESISTOR FOR LOW GAIN TEMPCO.
- ALL TRIM POTS SHOULD BE 100 ppm/°C OR BETTER (TYPE 79PR 15 TURN CERMET RECOMMENDED).

Figure 2. Typical Application

Input Offset Adjustment: To null input offset voltage, an optional 10kΩ potentiometer may be connected across the INPUT OFFSET ADJ. terminals (Pins 9 and 10 in Figure 2). With gain set at the desired value, connect both inputs (Pins 1 and 2) to COMMON (Pin 16), and adjust the 10kΩ potentiometer for zero volts at Pin 14. For applications using software nulling, Pins 9 and 10 should be left unconnected.

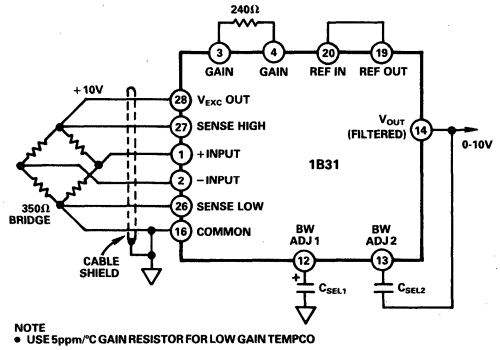
Output Offset Adjustment: The output can be offset over the ±10V range to compensate for dead load or bridge imbalance by using a 50kΩ potentiometer connected to Pin 11 as shown in Figure 2. Pin 11 is normally grounded if output offsetting is not desired.

Filter Cutoff Frequency Programming: The low pass filter cutoff frequency is internally set at 1kHz. It may be decreased from 1kHz by the addition of two external capacitors connected as shown in Figure 3 (from Pin 12 to common and between Pins 13 and 14). The values of capacitors required for a desired cutoff frequency, f_C, below 1kHz are obtained by the equations below:

$$C_{SEL1} = 0.015\mu F \left[\frac{1kHz}{f_C} - 1\right]$$

$$C_{SEL2} = 0.0022\mu F \left[\frac{1kHz}{f_C} - 1\right]$$

C_{SEL1} can be polarized for large values.



NOTE
- USE 5ppm/°C GAIN RESISTOR FOR LOW GAIN TEMPCO

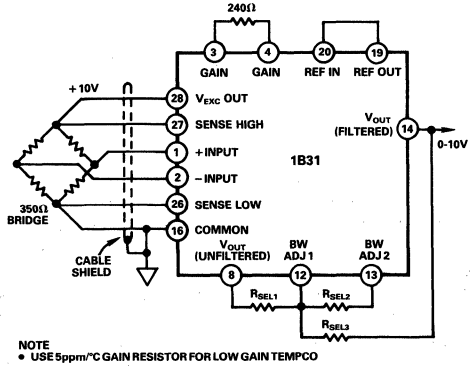
Figure 3. Narrow Bandwidth Application

The cutoff frequency may also be increased from 1kHz to 20kHz by the addition of three external resistors, connected as shown in Figure 4. The equations for determining the resistor values are:

$$R_{SEL1} = 20k\Omega / \left[\frac{f_C}{1kHz} - 1\right]$$

$$R_{SEL2} = 16k\Omega / \left[\frac{f_C}{1kHz} - 1\right]$$

$$R_{SEL3} = 40k\Omega / \left[\frac{f_C}{1kHz} - 1\right]$$



NOTE
- USE 5ppm/°C GAIN RESISTOR FOR LOW GAIN TEMPCO

Figure 4. Wide Bandwidth Application

Table I gives the nearest resistor and capacitor values for several common filter cutoff frequencies.

f_C(Hz)	C_{SEL1}(μF)	C_{SEL2}(μF)	
10	1.5	0.2	
50	0.27	0.039	
100	0.15	0.02	
200	0.056	0.0082	
500	0.015	0.0022	
	R_{SEL1}(kΩ)	R_{SEL2}(kΩ)	R_{SEL3}(kΩ)
2000	20	16.2	40.2
5000	4.99	4.12	10.0
10000	2.21	1.78	4.42
20000	1.05	0.866	2.21

Table I. Filter Cutoff Frequency vs. R_{SEL} and C_{SEL}

Note: The 25MHz gain bandwidth product of the IA should be considered in high-gain, wide bandwidth configurations.

Voltage Excitation Programming: The excitation voltage is preset to +10V. To increase V_{EXC} up to +15V a resistor must be connected between EXC. ADJ. and SENSE LOW (Pins 21 and 26) as shown in Figure 5. For a desired V_{EXC} the resistor value, R_{EXT}, is determined by the following equations:

$$R_T = \frac{10k\Omega \times V_{REF\ OUT}}{V_{EXC} - V_{REF\ OUT}} \quad ; \quad V_{REF\ OUT} = +6.8V$$

$$R_{EXT} = \frac{20k\Omega \times R_T}{20k\Omega - R_T}$$

The +10V to +15V range can be covered by a 20kΩ potentiometer between the reference terminals.

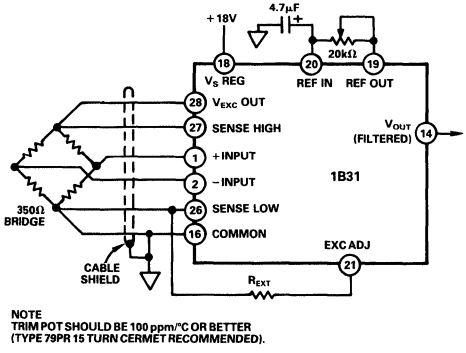


Figure 5. Constant Voltage Excitation: +10V to +15V Range

To decrease V_{EXC} down to +4V, a resistor has to be connected between REF IN and REF OUT (Pins 19 and 20) as shown in Figure 6. The equations to determine the value of R_{EXT} are:

$$V_{REF\ IN} = 0.68V_{EXC}$$

$$R_{EXT} = 10k\Omega \left[\frac{V_{REF\ OUT}}{V_{REF\ IN}} - 1\right] ; \quad V_{REF\ OUT} = +6.8V$$

A 20kΩ potentiometer between the REF IN and REF OUT pins will span the +4V to +10V excitation range. A 4.7μF tantalum capacitor from REF IN (Pin 20) to COMMON (Pin 16) is recommended in all cases to lower the voltage noise at the reference input.

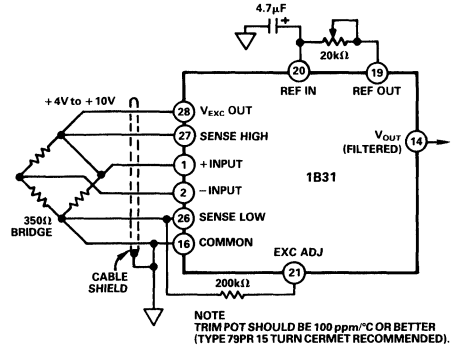


Figure 6. Constant Voltage Excitation: +4V to +10V Range

The remote sensing inputs should be connected to the transducer separately from the excitation leads or jumpered as shown in Figure 2.

Power Supply Decoupling: The power supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the 1B31 as possible (Figure 2).

Input Protection: The differential inputs of the 1B31 can be protected from accidental shorts to power line voltages (115V rms) by the circuit shown in Figure 7. The back-to-back diodes clamp the inputs to a maximum of ±12.5V and were selected for low leakage current. The 15kΩ resistors in series with the inputs will degrade the noise performance of the 1B31 to 4.2μV p-p in a bandwidth of 0.1Hz to 1kHz. For six-wire load cells in harsh environments the additional protection for the sense inputs shown in Figure 7 is recommended.

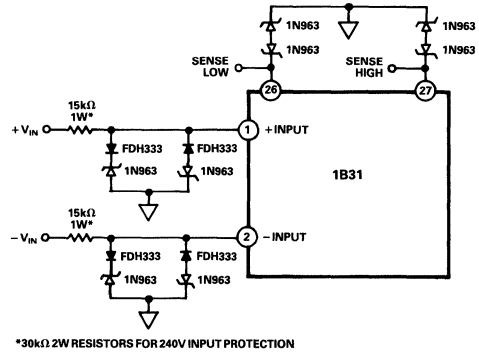


Figure 7. 115V Input Protection for 1B31

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Total offset voltage drift is composed of input and output drifts and is a function of gain. The 1B31 typically exhibits ±0.25μV/°C RTI drift at a gain of 1000V/V over the full temperature range. The RTI voltage offset drift vs. gain is graphed in Figure 8.

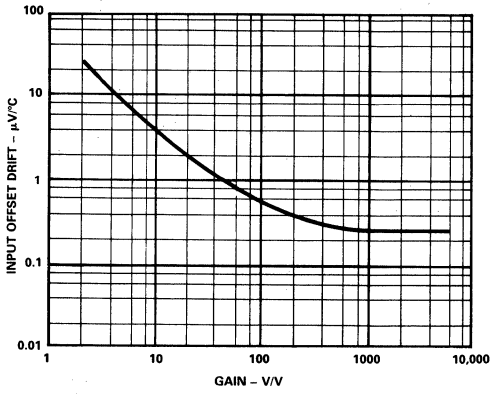


Figure 8. Total Input Offset Drift vs. Gain

Low Pass Filter: The two pole Butterworth filter is a multiple feedback design with a gain of −2V/V. It is preset at a cutoff frequency of 1kHz (−3dB) with a 40dB/decade roll-off. The step response at 1kHz is 1.5ms settling time to 0.1% of final value with less than 5% overshoot. The frequency response of the filter is shown graphically in Figure 9.

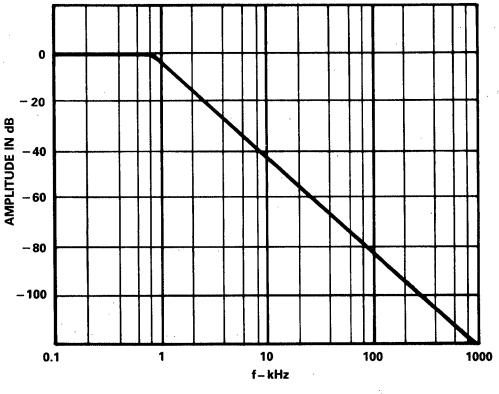
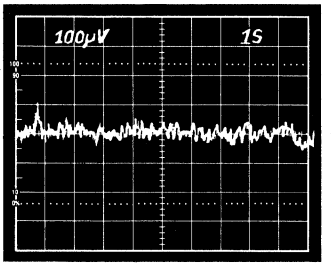
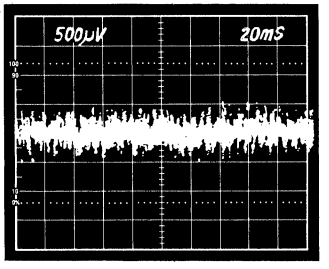


Figure 9. Filter Amplitude Response vs. Frequency

Gain Nonlinearity and Noise: Gain Nonlinearity is specified as a percent of full-scale output, and for the 1B31 it is ±0.005% maximum over the full-gain range. The IA design also offers exceptionally quiet performance with typical input noise of 0.3μV p-p for a 10Hz bandwidth (Figure 10a) and 1μV p-p for a 1kHz bandwidth (Figure 10b).



a. Bandwidth = 0.1Hz to 10Hz



b. Bandwidth = 0.1Hz to 1kHz

Figure 10. Voltage Noise, RTO @ G = 1000V/V

Common-Mode Rejection: CMR as a function of gain and frequency is shown in Figure 11. The best results (140dB @ 60Hz) are obtained by programming the low pass filter with a 10Hz cutoff frequency, which contributes an additional 30dB to the 1kHz specification where 60Hz noise is not attenuated by the filter.

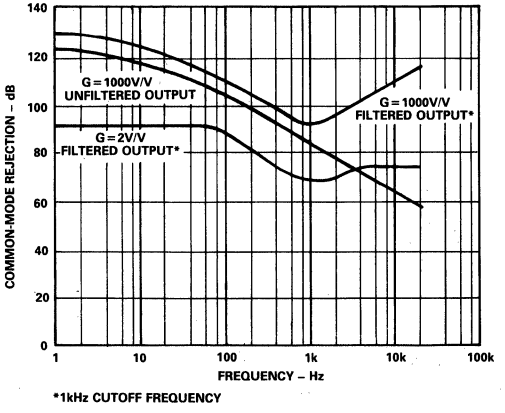


Figure 11. Common-Mode Rejection vs. Frequency and Gain

Turn On Drift: The input offset of the 1B31 stabilizes to within 1μV of final value in 5 minutes (Figure 12). The test conditions are: 350Ω bridge with +10V excitation and ambient temperature of +25°C.

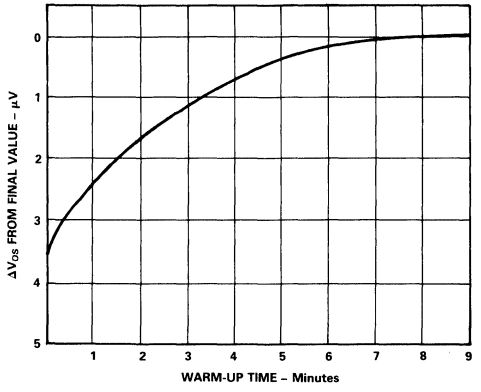


Figure 12. Offset Voltage, RTI, Turn-On Drift

Bridge Excitation: The adjustable bridge excitation is specified over a wide regulator input voltage range (+9.5V to +28V). Maximum load current I_L as a function of regulator input-output differential voltage is shown in Figure 13. The maximum output current also depends on ambient temperature and above 50°C a derating factor should be derived from Figure 14.

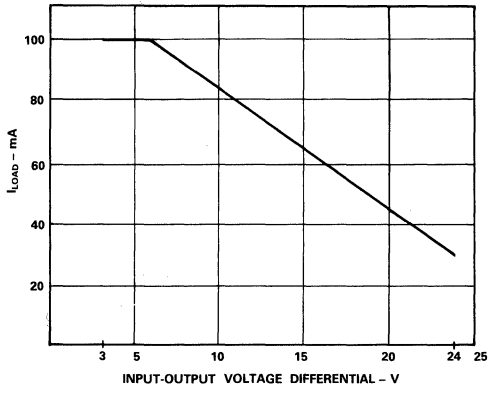


Figure 13. Excitation Source Input – Output Voltage Differential vs. Load Current; Ambient Temperature ≤25°C.

APPLYING THE 1B31

Strain Measurement: The 1B31 is shown in a strain measurement system in Figure 15. A single active gage (120Ω, Gage Factor = 2) is used in a bridge configuration to detect fractional changes in gage resistance caused by strain. An equivalent resistance

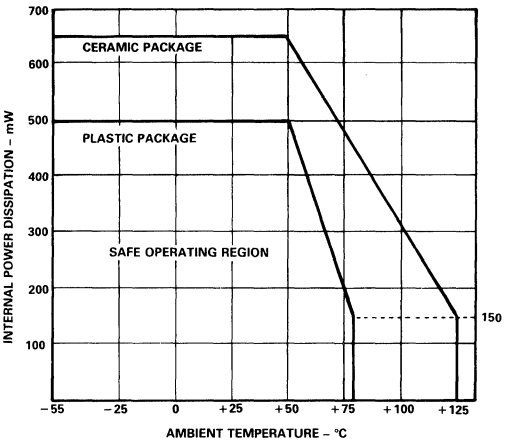


Figure 14. Excitation Source Internal Power Dissipation vs. Temperature

dummy gage mounted adjacent to the active gage provides temperature compensation. The rest of the bridge is completed by the 1B31 internal half-bridge network which consists of two 20kΩ, 1% thin-film resistors tracking to within ±5ppm/°C max. Bridge excitation is set at +4V to avoid self-heating errors from the strain gage. System calibration produces a +1V output for an input of 1000 microstrains. The filter cutoff frequency is set at approximately 100Hz.

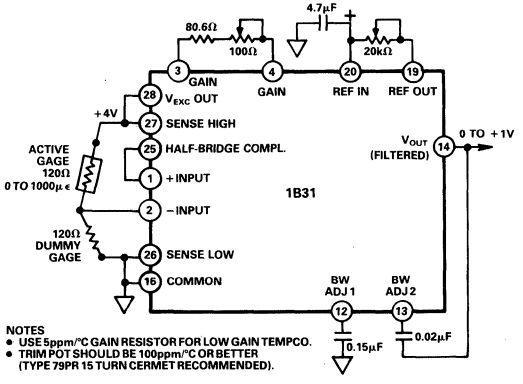


Figure 15. Strain Gage Application Using Internal Half-Bridge

Pressure Transducer Inferface: A strain gage type pressure transducer (Dynisco 800 series) is interfaced to a 1B31 in Figure 16. Regulated excitation of +10V dc is provided for a 30mV full-scale output. The gain is sett at 333.3 to achieve a 0-10V output for a 0-10,000 psi range of the transducer. A shunt calibration resistor is built into the transducer for easy verification of the 80% point of its full-scale output. A typical shielding scheme to preserve the excellent performance characteristics of the 1B31 is also shown. To avoid ground loops, signal return or cable shield should be grounded only at one point.

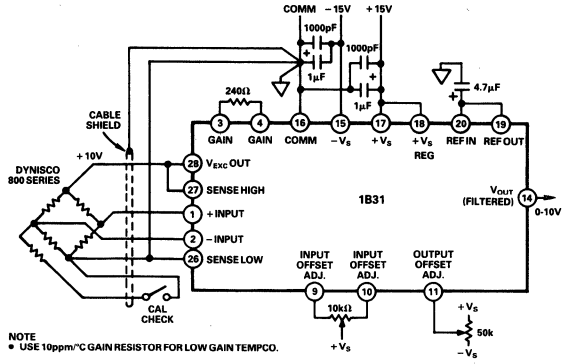


Figure 16. Pressure Transducer Application

Multiple Load-Cells: For transducer configurations where the maximum load current of 100mA of the 1B31 is not sufficient, a buffer and a power transistor such as a TIP31 can be used as shown in Figure 17. This design can supply 300mA at +10V excitation over the full industrial temperature range (−25°C to +85°C). In a multiple 1B31 system an added advantage is that ratiometric operation can be preserved by using one excitation source which also serves as the reference voltage for the system A/D converter.

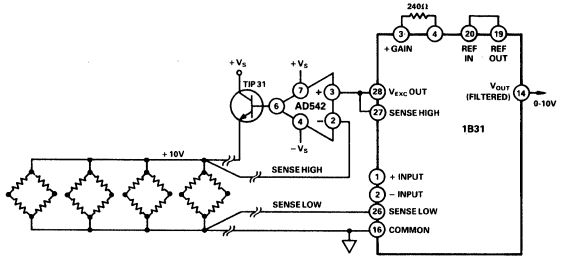


Figure 17. Multiple Load-Cell Application

Mobile Transducer Application: The small size and reliability of the 1B31 make it an ideal choice for mobile applications. Since the 1B31 requires a negative supply, one possible solution for its generation is shown in Figure 18. The positive voltage of a +12V battery is used to drive a CMOS TLC555 oscillator with a typical supply current of 360µA. The output is a square wave that is rectified by the diodes and filtered to provide a −9V supply. Excitation voltage should be equal to or less than +9V for adequate headroom for the 1B31 voltage regulator.

Pressure Transducer Data Acquisition System: Figure 19 shows a two module solution for microcomputer based data acquisition using a 1B31 and an AD1170 18-bit A/D converter. A 3mV/V pressure transducer (e.g. Dynisco 800 series) is interfaced to a 1B31 set up with a gain of 333.3 to give a 0 – 5V output. The regulated excitation is +5V, and for ratiometric operation it is also used as the voltage reference input for the AD1170. An initial ECAL command establishes the voltage excitation as the full-scale input of the AD1170 and periodic calibration cycles keep the converter tracking the reference input. This configuration yields very high CMR (168dB @ 60Hz) enhanced by the 1B31 low pass filter and the integrating conversion scheme of the

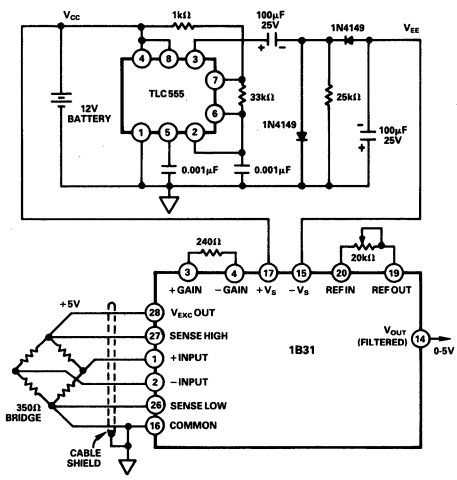


Figure 18. Negative Supply Generation for 1B31

AD1170. In addition, fixed offsets caused by bridge imbalance can be nulled out by the AD1170 with a power-up initialization command from the microcomputer. This eliminates a potentiometer or software overhead which might otherwise be needed.

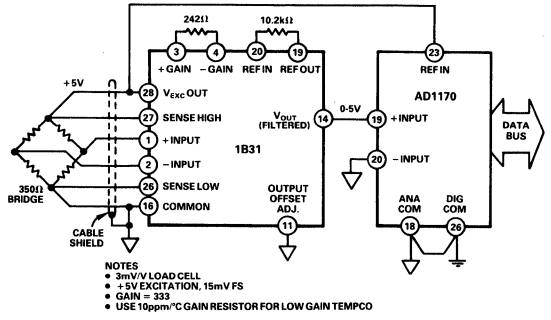


Figure 19. Pressure Transducer Data Acquisition Using 1B31 and AD1170

Isolated Current Loop Interface: The output of the 1B31 can be interfaced to a process loop as shown in Figure 20. The 2B23 module produces an isolated 4-to-20mA output current which is proportional to the input voltage and independent of the output load resistance. Common-mode input/output isolation is ±1500V pk continuous.

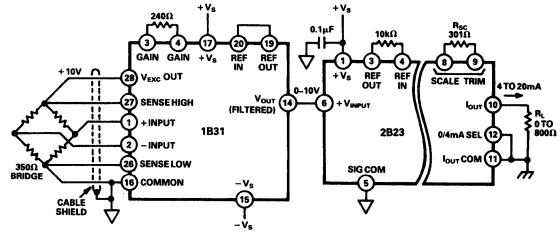


Figure 20. Isolated 4-20mA Transmitter

ANALOG DEVICES

Bridge Transducer Signal Conditioner

1B32

FEATURES
- **Low Cost**
- **Complete Signal-Conditioning Solution**
- **Small Package: 28-Pin Double DIP**
- **Internal Thin-Film Gain Network**
- **High Accuracy**
  - **Low Input Offset Tempco: ±0.07μV/°C**
  - **Low Gain Tempco: ±2ppm/°C**
  - **Low Nonlinearity: ±0.005% max**
  - **High CMR: 140dB min (60Hz, G=1000V/V)**
- **Programmable Bridge Excitation: +4V to +15V**
- **Remote Sensing**
- **Low Pass Filter (f_C=4Hz)**

APPLICATIONS
- **Weigh Scales**
- **Instrumentation: Indicators, Recorders, Controllers**
- **Data Acquisition Systems**
- **Microcomputer Analog I/O**

GENERAL DESCRIPTION

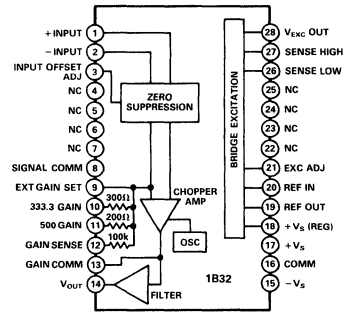
Model 1B32 is a precision, chopper-based, signal-conditioning component ideally suited for high-accuracy applications of load cells and bridge transducers. Packaged in a compact 28-pin plastic double DIP, the 1B32 takes advantage of hybrid technology for high reliability as well as higher channel density. Functionally, the signal conditioner consists of three basic parts: a high performance chopper-based amplifier, a low-pass filter and an adjustable transducer excitation source.

The chopper-based amplifier features extremely low input offset tempco of ±0.07μV/°C (RTI, G=500V/V) and excellent nonlinearity of ±0.005% max over its full gain range of 100 to 5000V/V. The 1B32 has a thin-film resistor network for pin-strapping the gain to 500V/V or 333.3V/V (for 2mV/V and 3mV/V load cells). The gain tempco for these fixed gains is a highly stable ±2ppm/°C. Additionally, the gain can be set to any value in the gain range with two external resistors. The amplifier also has a wide-range input referred zero suppression capability (±10V), which can easily be interfaced to a D/A converter. The bandwidth of the chopper is 4Hz at G=100V/V.

The integral three-pole, low-pass filter offers a 60dB/decade roll-off from 4Hz to reduce common-mode noise and improve system signal-to-noise ratio.

The 1B32's regulated transducer excitation stage features low output drift (±40ppm/°C typ) and can drive 120Ω or higher resistance load cells. The excitation is preset at +10V with other voltages between +4V and +15V programmable with external resistors. This section also has remote sensing capability to allow for lead-wire compensation in 6-wire load cells and other bridge configurations.

1B32 FUNCTIONAL BLOCK DIAGRAM



The 1B32 is fully specified over the industrial (−25°C to +85°C) temperature range.

DESIGN FEATURES AND USER BENEFITS

Pin-Strappable Gain: The internal resistor network can be pin-strapped for gains of 500V/V and 333.3V/V for 2mV/V and 3mV/V load cells. The tracking network guarantees a gain tempco of ±6ppm/°C max.

Custom Trimmable Network: For volume applications, the 1B32 can be supplied with a custom laser trimmed gain network. Contact factory for further information.

Wide Range Zero Suppression: The output can be offset by ±10V for nulling out a dead load or to do a tare adjustment.

Remote Sensing: Voltage drops across the excitation lead-wires are compensated by the regulated supply, making 6-wire load-cell interfacing straightforward.

Programmable Transducer Excitation: The excitation source is preset for +10V dc operation without external components. It is user-programmable for a +4V to +15V dc range (@ 100mA) to optimize transducer performance.

Low-Pass Filter: The three-pole active filter (f_C=4Hz) reduces 60Hz line noise and improves system signal-to-noise ratio.

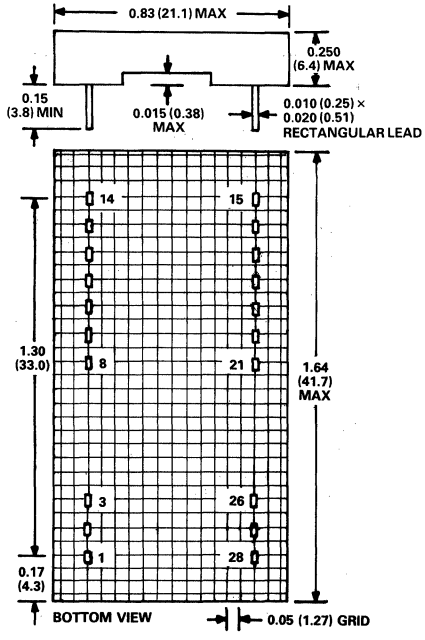
SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

Model	1B32AN
GAIN	
Gain Range	100V/V to 5000V/V
Internal Gain Setting	333.3V/V and 500V/V
Gain Equation	$1 + \frac{R_F}{R_I}$
Gain Equation Accuracy[1]	±0.1%
Gain Temperature Coefficient[2]	±2ppm/°C (±6ppm/°C max)
Gain Nonlinearity	±0.005% max
OFFSET VOLTAGES	
Total Offset Voltage, RTI	
Initial, @ +25°C, G = 1000V/V	±40μV
Warm-Up Drift, G = 1000V/V, 10 min	Within ±1μV
vs. Temperature (−25°C to +85°C)	
G = 1000V/V	±0.07μV/°C (±0.2μV/°C max)
At Other Gains	$\pm\left(0.06 + \frac{15}{G}\right)\mu V/°C$
Output Offset Adjust Range	±10V
INPUT BIAS CURRENT	
Initial @25°C	±3nA
vs. Temperature (−25°C to +85°C)	±50pA/°C
INPUT DIFFERENCE CURRENT	
Initial @ +25°C	±3nA
vs. Temperature (−25°C to +85°C)	±10pA/°C
INPUT RESISTANCE	
Differential	100MΩ
Common Mode	100MΩ
INPUT VOLTAGE RANGE	
Linear Differential Input	±0.1V
Maximum Differential Input	+5V
CMV Input Range	0 to +7.5V
CMR, 1kΩ Source Imbalance[3]	
G = 100V/V to 5000V/V @ dc	86dB
G = 100V/V, @ 60Hz	120dB
G = 1000V/V, @ 60Hz	140dB min
INPUT NOISE	
Voltage, G = 1000V/V	
0.1Hz to 10Hz	1μV p-p
Current, G = 1000V/V	
0.1Hz to 10Hz	3pA p-p
RATED OUTPUT	
Voltage, 2kΩLoad, min	±10V
Current	±5mA
Impedance, dc to 2Hz, G = 100V/V	0.6Ω
Load Capacitance	500pF
Output Short Circuit Duration (to Ground)	Indefinite
DYNAMIC RESPONSE	
Small Signal Bandwidth	
−3dB Gain Accuracy, G = 100V/V	4Hz
G = 1000V/V	3.5Hz
Slew Rate	20V/sec
Full Power	0.5Hz
Settling Time, G = 100V/V, ±10V Output Step to ±0.1%	2sec
LOW PASS FILTER	
Number of Poles	3
Cutoff Frequency (−3dB Point)	4Hz
Roll-Off	60dB/decade

(Continued on next page)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



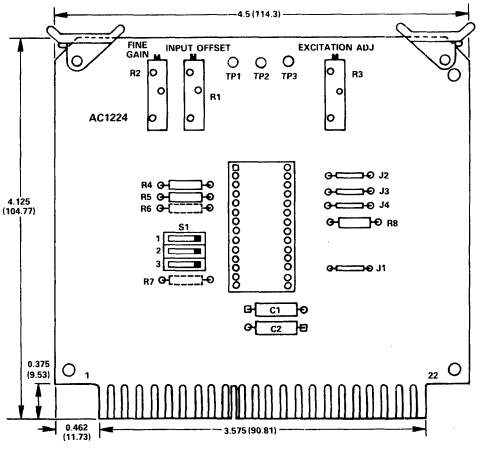
PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+INPUT	15	$-V_S$
2	−INPUT	16	COMM
3	INPUT OFFSET ADJ	17	$+V_S$
4	NC	18	$+V_S$ REG
5	NC	19	REF OUT
6	NC	20	REF IN
7	NC	21	EXC ADJ
8	SIGNAL COMM	22	NC
9	EXT GAIN SET	23	NC
10	333.3 GAIN	24	NC
11	500 GAIN	25	NC
12	GAIN SENSE	26	SENSE LOW
13	GAIN COMM	27	SENSE HIGH
14	V_{OUT}	28	V_{EXC} OUT

BRIDGE EXCITATION	
Regulator Input Voltage Range	+9.5V to +28V
Output Voltage Range	+4V to +15V
Regulator Input/Output Voltage Differential	+3V to +24V
Output Current[4]	100mA max
Regulation, Output Voltage vs. Supply	±0.05%/V
Load Regulation, I_L = 1mA to 50mA	±0.1%
Output Voltage vs. Temperature (−25°C to +85°C)	±40ppm/°C
Output Noise, 0.1Hz to 10Hz[5]	300μV p-p
Reference Voltage (Internal)	+6.8V ±5%
Sense & Excitation Lead Resistance	10Ω max
POWER SUPPLY	
Voltage, Rated Performance	±15V dc
Voltage, Operating	±12V to ±18V dc
Current, Quiescent[6]	+4mA, −1mA
ENVIRONMENTAL	
Temperature Range	
Rated Performance	−25°C to +85°C
Operating	−40°C to +85°C
Storage	−40°C to +100°C
Relative Humidity	0 to 95%, Noncondensing, @ +60°C
CASE SIZE	0.83" × 1.64" × 0.25" (21.1 × 41.7 × 6.35mm) max

NOTES
[1]Using internal network for gain.
[2]For pin-strapped gain. The tempco of the individual thin-film resistors is ±50ppm/°C max.
[3]3V p-p 60Hz common-mode signal used in test setup.
[4]Derate 2mA/°C from +50°C.
[5]4.7μF capacitor from REF IN (Pin 20) to COMM.
[6]Excluding bridge excitation current and with no loading on the output.
Specifications subject to change without notice.

AC1224 MOUNTING CARD



AC1224 GAIN SETTINGS VIA SWITCH S1

GAIN	S1-1	S1-2	S1-3
333	CLOSED	OPEN	CLOSED
500	OPEN	CLOSED	CLOSED
EXTERNAL	OPEN	OPEN	OPEN

AC1224 CONNECTOR DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
T	V_{EXC} OUT	1	+INPUT
U	SENSE HIGH	2	−INPUT
V	SENSE LOW	12	V_{OUT}
X	REF OUT	19	$-V_S$
Y	REF IN	20	COMM
Z	EXC ADJ	21	$+V_S$
		22	$+V_S$ REG

The AC1224 mounting card is available for the 1B32. The AC1224 is an edge connector card with a socket for plugging in the 1B32. In addition it has provisions for switch selecting internal gains as well as installing gain resistors. Adjustment pots for offset, fine gain and excitation are also provided. The AC1224 comes with a Cinch 251-22-30-160 (or equivalent) edge connector.

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FUNCTIONAL DESCRIPTION

Model 1B32 is based on a switched capacitor, chopper stabilized amplifier followed by an active filter and an adjustable voltage regulator section for excitation. The ultralow drift chopper samples the difference between the +INPUT and −INPUT at 190Hz. The signal is modulated, amplified and then demodulated. This stage introduces a pole with a 20dB/decade rolloff from 4Hz. The high-level signal is then filtered by a two-pole active filter with a 4Hz cutoff frequency to give a ±10V output. The clock signal for the chopper is generated by an on-board oscillator.

As shown in Figure 1, the gain can be pin-strapped by an internal resistor network. Standard gains of 333.3 and 500 can be achieved by this method with gain tempco of ±6ppm/°C max. Finally, the offset adjust of the amplifier is input referred, and requires a voltage input similar to the differential input voltage to implement wide range suppression.

The bridge excitation section is an adjustable ouput, regulated supply with an internally provided reference voltage (+6.8V). It is configured as a gain stage with the output preset at +10V. The excitation voltage is increased by connecting a resistor between Pins 19 and 20. Sense lines are provided to compensate for lead-wire resistance by bringing the leads into the feedback loop.

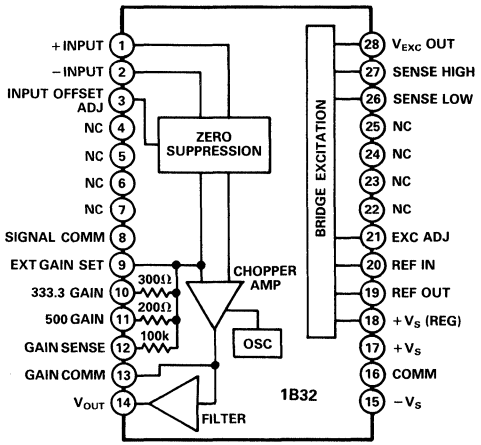


Figure 1. 1B32 Block Diagram and Pinout

OPERATING INSTRUCTIONS

Ground Connections: Signal common (Pin 8) and power common (Pin 16) are not internally connected within the 1B32. These pins must be connected together externally or excessive current will be drawn.

Gain Setting: The differential gain of the 1B32 can be either pin-strapped or programmed externally with two resistors. The internal thin-film gain network (Figure 1) provides gains of 500 and 333.3 for standard load-cell sensitivities of 2mV/V and 3mV/V. This is achieved by connecting GAIN SENSE (Pin 12) to GAIN COMM (Pin 13) and grounding Pin 10 or Pin 11 (Figure 2). The gain tempco using the internal network is an excellent ±2ppm/°C typ (±6ppm/°C max).

To program the gain externally, two resistors are connected as shown in Figure 3. The gain equation is:

$$G = 1 + \frac{R_F}{R_I}$$

The gain-strapping Pins (10 and 11) and GAIN SENSE (Pin 12) are left unconnected, effectively floating the internal network.

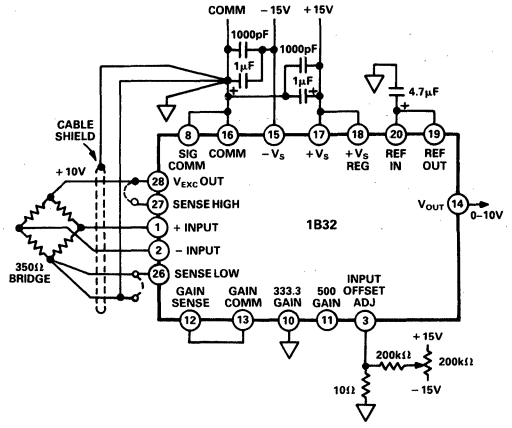


Figure 2. Internal Gain Strapping

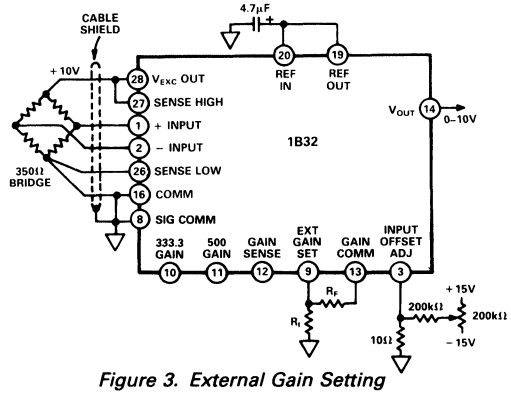


Figure 3. External Gain Setting

Offset Adjustment: The input-referred offset adjust has the same sensitivity as the inputs of the 1B32. The voltage level at INPUT OFFSET ADJ (Pin 3) is gained by the same factor as the input signal to provide a ±10V output adjust. Figure 2 shows an external network and potentiometer set up for a ±7.5mV span at the input, which gives a ±2.5V (7.5mV × 333.3) output adjust capability. Wider ranges can be chosen with the appropriate resistor and potentiometer values.

Note: If offset adjustment is not required, Pin 3 must be grounded.

Voltage Excitation Programming: The excitation voltage is preset to +10V. To increase V_{EXC} up to +15V a resistor must be connected between EXC ADJ and SENSE LOW (Pins 21 and 26) as shown in Figure 4.

The V_S (REG) input (Pin 18) must be raised to +18V to satisfy the +3V min input-output voltage differential of the regulator. Consult the Performance Characteristics section for safe operating conditions of the regulator. For a desired V_{EXC} the resistor value, R_{EXT}, is determined by the following equations:

$$R_T = \frac{10k\Omega \times V_{REF\ OUT}}{V_{EXC} - V_{REF\ OUT}} \quad ; \quad V_{REF\ OUT} = +6.8V$$

$$R_{EXT} = \frac{20k\Omega \times R_T}{20k\Omega - R_T}$$

The +10V to +15V range can be covered by a 20kΩ potentiometer between REF IN (Pin 20) and REF OUT (Pin 19). R_{EXT} of

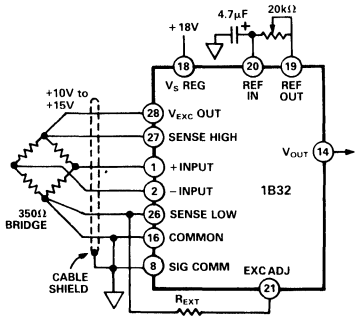


Figure 4. Constant Voltage Excitation: +10V to +15V Range

200kΩ is recommended for fine adjustment at +10V excitation voltage.

Similarly to decrease V_{EXC} down to +4V, connect a 20kΩ potentiometer between Pins 19 and 20, as shown in Figure 5.

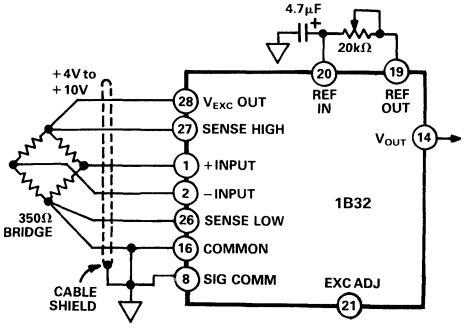


Figure 5. Constant Voltage Excitation: +4V to +10V Range

A 4.7µF tantalum capacitor from REF IN (Pin 20) to COMMON (16) is recommended in all cases to lower the voltage noise at the reference input.

The remote sensing inputs should be connected to the transducer separately from the excitation leads or jumpered as shown in Figure 2. The resistance of the excitation and sense lines should not exceed 10Ω.

Power Supply: The V_S REG input (Pin 18) should be connected to $+V_S$ (Pin 17) even if the bridge excitation section is not used. Also the power supplies should be decoupled with 1µF tantalum and 1000pF ceramic capacitors as close to the 1B32 as possible (Figure 2).

Input Protection: The 1B32 differential inputs can be protected from accidental shorts to power line voltages (115V rms) by the circuit shown in Figure 6. The back-to-back diodes clamp the inputs to a maximum of ±12.5V and were selected for low leakage current. The 15kΩ resistors in series with the inputs will degrade the noise performance of the 1B32 to 4µV p-p (0.1Hz to 10Hz). When interfacing with six-wire load cells in harsh environments, input protection for the sense inputs is also recommended (Figure 6).

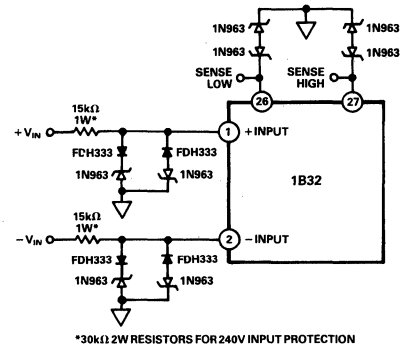


Figure 6. 115V Input Protection

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: The chopper front end of the 1B32 gives it excellent input offset stability. As shown in Figure 7, it typically exhibits drift of ±0.07µV/°C RTI at a gain of 1000V/V (±75µV/°C RTO). The measurement is two-point, and is taken at −25°C and +85°C, which covers the specified temperature range of the 1B32.

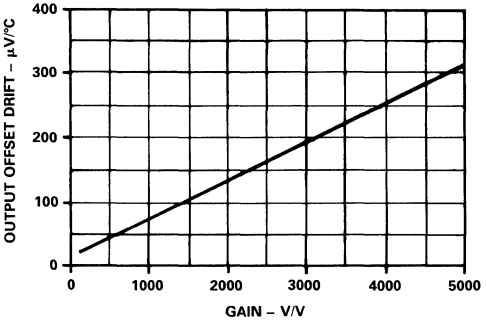


Figure 7. Total Output Offset Drift vs. Gain

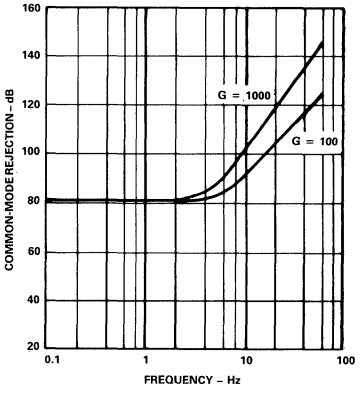


Figure 8. Common-Mode Rejection vs. Frequency

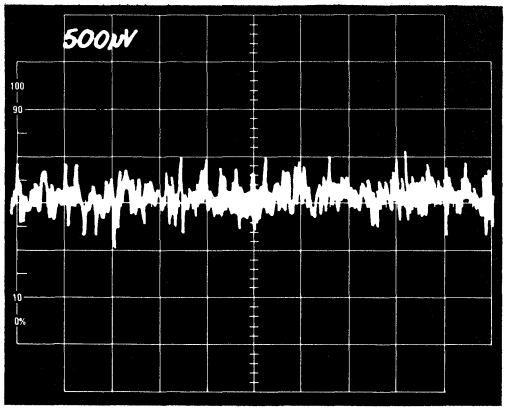


Figure 9. Voltage Noise, 0.1Hz to 10Hz, G = 1000

Common-Mode Rejection: CMR as a function of frequency is shown in Figure 8. Test conditions are a 3V p-p common-mode signal and 1kΩ source imbalance. The CMR improves with increasing gain. Note that the 4Hz filter enhances the CMR performance above the corner frequency by attenuating the normal-mode signal at 60dB/decade.

Gain Nonlinearity and Noise: Gain Nonlinearity is specified as a percent of full-scale output, and for the 1B32 it is ±0.005% max over the full span. The chopper design also offers exceptional low-noise performance, with typical input noise of 1μV p-p in the 0.1Hz to 10Hz bandwidth (Figure 9).

Low-Pass Filter: The 1B32 has three poles at 4Hz in its design. One is introduced in the amplifier, while the other two are provided by an active Butterworth filter following the amplifier. Total roll-off is 60dB/decade from 4Hz. The frequency response of the filter is shown in Figure 10.

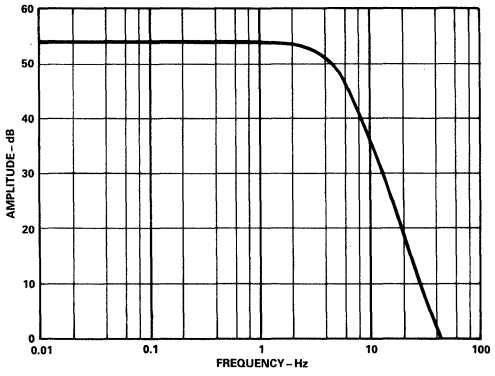


Figure 10. Filter Amplitude Response vs. Frequency, G = 500

Turn-On Drift: The 1B32 offset voltage stabilizes to within 1μV of its final value in 10 minutes (Figure 11). The test conditions are: 350Ω bridge with a +10V excitation and ambient temperature of +25°C.

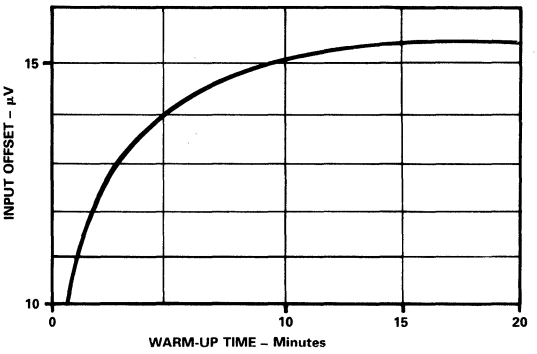


Figure 11. Offset Voltage RTI, Turn-On Drift

Bridge Excitation: The adjustable bridge excitation is specified over a wide regulator input voltage range (+9.5V to +28V). Maximum load current I_L as a function of regulator input-output differential voltage is shown in Figure 12. The maximum output current also depends on ambient temperature, and above +50°C a derating factor of 2mA/°C must be applied. The safe operating region for internal power dissipation vs. temperature is graphed in Figure 13.

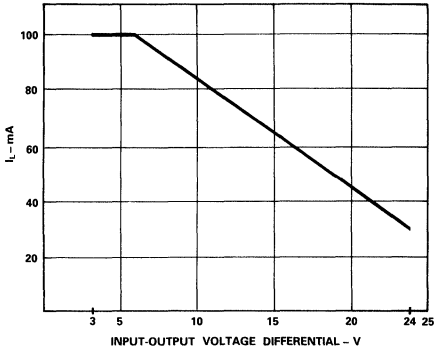


Figure 12. Excitation Source Load Current vs. Input-Output Voltage Differential, ≤25°C

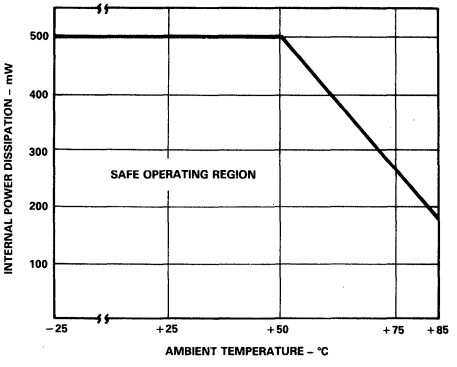


Figure 13. Excitation Source Internal Power Dissipation vs. Temperature

APPLYING THE 1B32

Pressure Transducer Interface: A strain gage type pressure transducer (Dynisco 800 series) is interfaced to a 1B32 in Figure 14. Regulated excitation of +10V dc is provided for a 30mV full-scale output for a 0-10,000 psi range of the transducer. A shunt calibration resistor is built into the transducer for easy verification of the 80% point of its full-scale output. A typical shielding scheme to preserve the excellent performance characteristics of the 1B32 is also shown. To avoid ground loops, signal return and cable shield should be grounded only at one point.

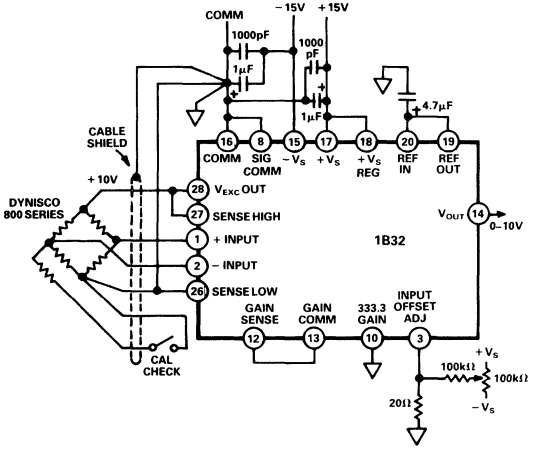


Figure 14. Pressure Transducer Interface

Pressure Transducer Data Acquisition System: A two module solution for microcomputer based data acquisition using a 1B32 and an AD1170 18-bit A/D converter is shown in Figure 15. A 3mV/V pressure transducer (e.g. Dynisco 800 series) is interfaced to a 1B32 configured with a gain of 333.3, to provide a 0 to 5V output. The regulated excitation is +5V, and is used as the reference input for the AD1170 to produce ratiometric operation. This configuration yields very high CMR enhanced by the 1B32 low pass filter and the integrating conversion scheme of the AD1170.

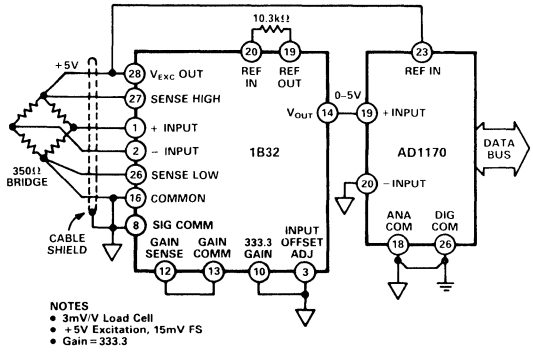


Figure 15. Auto-Calibrating Data Acquisition Using 1B32 and AD1170

In addition, fixed offsets caused by bridge imbalance can be nulled out by the AD1170 with a power-up initialization command from the microcomputer. The full-scale output of the 1B32 and transducer can be normalized to the AD1170 full scale through the electronic calibration command ECAL. Both the offset and full-scale correction data will then be stored in nonvolatile memory to eliminate the need for the trim process after each power-up. The AD1170 eliminates a potentiometer or software overhead which might otherwise be needed for these functions.

Multiple Load-Cells: For transducer configurations where the maximum load current of the 1B32 is not sufficient, a buffer and a power transistor such as a TIP31 can be used as shown in Figure 16. This approach will supply 300mA at +10V excitation over −25°C to +85°C temperature range. In a multiple 1B32 system an added advantage is that ratiometric operation can be preserved by using the excitation voltage as the reference for the system A/D converter.

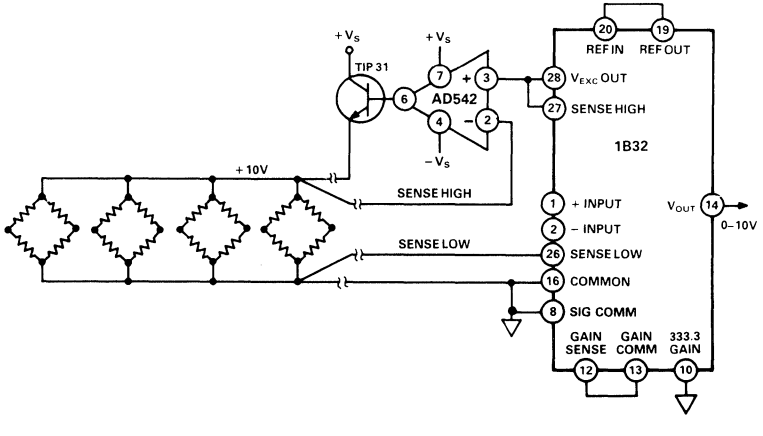


Figure 16. Multiple Load-Cell Application

Mobile Transducer Applications: The small size and reliability of the 1B32 make it an excellent choice for mobile applications. Since the 1B32 requires bipolar supplies, a possible circuit to provide the negative voltage is shown in Figure 17. The CMOS TLC555 is powered by a +12V battery, and typically draws 360μA. The output is a square wave that is rectified by the diodes and filtered to provide a −9V supply. Excitation voltage should be equal to or less than +9V for adequate headroom for the 1B32 voltage regulator. Note that the 1B32 will operate with ±9V supplies as long as the excitation voltage and the output range are less than 5V.

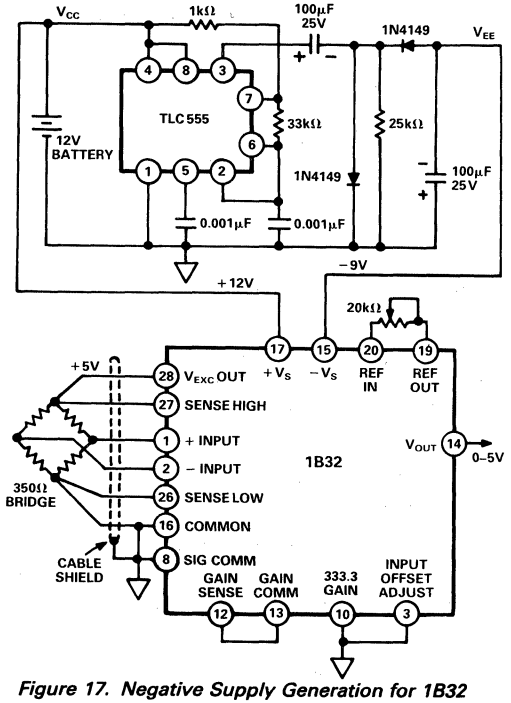


Figure 17. Negative Supply Generation for 1B32

Digital Output Offset Adjust: A 10-bit multiplying DAC such as the AD7533 can be used to control the output offset of the 1B32 as shown in Figure 18. The DAC is configured for unipolar operation with an AD OP-07 generating a voltage output. This 0-10V output is attenuated by R_1 and R_{SEL} and superposed on another fixed voltage derived from V_{EXC}. Thus the voltage at Pin 3 (INPUT OFFSET ADJUST) is insensitive to the tempco of the excitation voltage since it is also used as the reference of the DAC. For best performance R_1 and R_2 should track to ±5ppm/°C. As an example, a ±5V output adjustment can be obtained by using R_{SEL} = 200Ω for G = 500 and V_{EXC} = 10V.

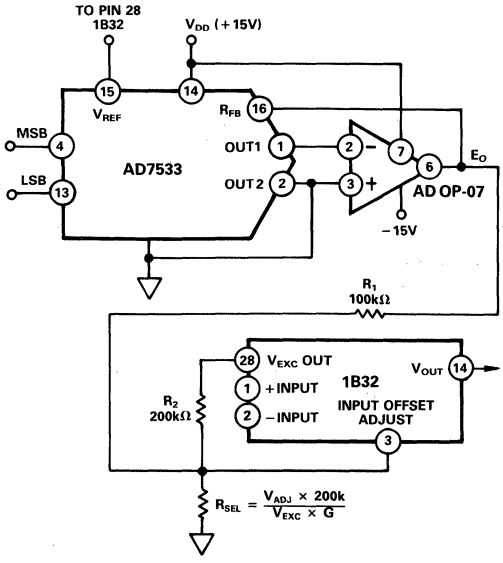


Figure 18. Output Offset Adjust Using a 10-Bit DAC

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (E_O as shown in Figure 18)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right)=\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right)=0$

Table I. Unipolar Binary Code Table

ANALOG DEVICES

Isolated RTD Signal Conditioner

1B41

FEATURES

Complete RTD Signal Conditioning Solution
Resistor Programmable Linearization
Lead Resistance Compensation
High CMV Isolation: 1500 V rms Continuous
High Accuracy
Low Input Offset Tempco: 0.002 Ω/°C
Linearization Conformance: ±0.1% FSR
High CMR: 160 dB (60 Hz, G = 1000 V/V)
Small Package: 1.0″×2.1″×0.35″ DIP
Low Pass Filter (f_C = 3 Hz)
Pin Compatible with 1B51 Isolated mV/Thermocouple Conditioner

APPLICATIONS

Multichannel RTD Temperature Measurement
Industrial Measurement and Control Systems
Data Acquisition Systems

GENERAL DESCRIPTION

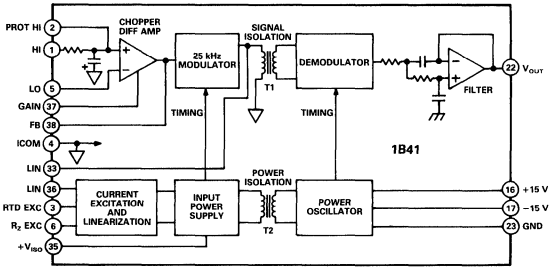
The 1B41 is a precision, isolated, RTD signal conditioner that incorporates a circuit design utilizing transformer based isolation and automated surface mount manufacturing technology. It provides an unbeatable combination of versatility and performance in a compact plastic package. Designed for measurement and control applications, it is especially suited for harsh environments with extremely high common mode interference. Unlike expensive solutions that require separate dc/dc converters, each 1B41 generates its own floating current excitation, providing true low cost channel-to-channel isolation.

Functionally, the signal conditioner consists of four basic sections: chopper stabilized amplifier, isolation, current excitation and output filter. The amplifier section allows an RTD resistance range of 20 Ω to 5 kΩ. Wide range zero suppression can be implemented at this stage.

The isolation section has complete input to output galvanic isolation of 1500 V rms continuous by the use of transformer coupling techniques. A stable sensor excitation provides 0.25 mA for most RTD applications. For platinum RTDs the excitation is internally compensated to provide an output that is linear with temperature. Filtering at 3 Hz is implemented by a passive antialiasing filter at the input and a two-pole active filter at the output. Overall NMR is 60 dB and CMR is 160 dB min @ 60 Hz.

The 1B41 is fully specified over −25°C to +85°C and operates over the industrial (−40°C to +85°C) temperature range.

1B41 FUNCTIONAL BLOCK DIAGRAM



DESIGN FEATURES AND USER BENEFITS

Ease of Use: The 1B41 has direct RTD interface with minimum external parts required to get a high-level, conditioned signal.

Lead Resistance Compensation: Voltage drops in RTD lead wires are compensated by the use of matching current sources in the 1B41.

High Noise Rejection: The combination of a chopper stabilized front end with a low pass filter provides high system accuracy in harsh industrial environments as well as good rejection of 50/60 Hz noise.

Small Size: The 1B41 package size (1.00″×2.1″×0.35″) and functional completeness makes it an excellent choice in systems with limited board space and clearance.

Wide Range Zero Suppression: This input referred function is a convenient way to null large input offsets. A single resistor value sets the RTD resistance for which the output is zero volts.

Low Pass Filter: The three-pole active filter (f_C = 3 Hz) reduces 50/60 Hz noise and aliasing errors.

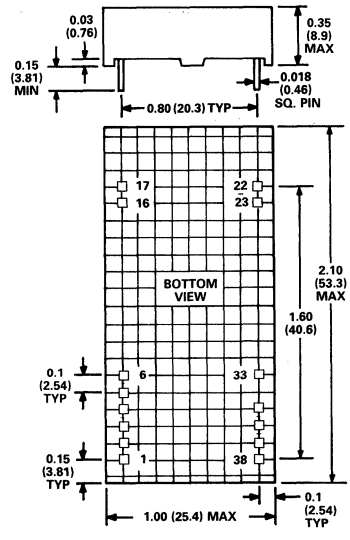
SPECIFICATIONS[1] (typical @ +25°C and V_S = +15 V unless otherwise noted)

Model	1B41AN	1B41BN
INPUT SPECIFICATIONS		
Sensor Type	Pt 100 Ω @ 0°C, α = 0.00385, 0.00392	*
Linear Input Resistance Range	20 Ω to 5 kΩ Full Scale	*
Max InputVoltage Range	+1 V to −5 V	*
Input Offset	0.5 Ω (2 Ω max)	*
Input Offset Tempco	0.002 Ω/°C (0.01 Ω/°C max)	*
Max CMV, Input to Output		
ac, 60 Hz, Continuous	1500 V rms	*
Continuous, dc	±2000 V peak	*
CMR, @ 60 Hz, 1 kΩ Source Imbalance	160 dB min	*
NMR, @ 60 Hz	60 dB min	*
Common Mode Transient Protection	IEEE-STD 472 (SWC)	*
Sensor Current Excitation	0.25 mA	*
Current Source Matching	1.5 μA	*
OUTPUT SPECIFICATIONS		
Voltage, 2 kΩ Load, min	±10 V	*
Current	±5 mA	*
Output Offset Voltage		
Initial	50 mV typ	25 mV typ
vs. Temperature	175 μV/°C	50 μV/°C
Output Noise, dc to 100 kHz	1 mV pk-pk	*
Impedance, dc	0.1 Ω	*
ACCURACY		
Gain Accuracy[2]	2% FSR (5% FSR max)	*
Gain Tempco (0 to +70°C)	±50 ppm/°C	*
(−25°C to +85°C)	±75 ppm/°C	*
Gain Nonlinearity	±0.035%	±0.025%
Linearization Conformance		
Pt 100 Ω	0.1% FSR	*
0 to +600°C	0.09% FSR	*
0 to +200°C	0.06% FSR	*
0 to +100°C	0.06% FSR	*
−100°C to +100°C	0.06% FSR	*
Lead Wire Compensation	0.01 Ω/Ω	*
DYNAMIC RESPONSE		
Bandwidth, −3 dB	dc to 3 Hz	*
POWER SUPPLY		
Voltage, Rated Performance	±15 V dc	*
Voltage, Operating	±13.5 V to ±18 V	*
Current, Quiescent	+12 mA, −4 mA	*
ENVIRONMENTAL		
Temperature Range		
Rated Performance	−25°C to +85°C	*
Operating	−40°C to +85°C	*
Storage	−40°C to +85°C	*
Relative Humidity	0 to 95% @ 60°C	*
CASE SIZE	1.0″×2.1″×0.35″	*
	(25.4×53.3×8.9) mm	*

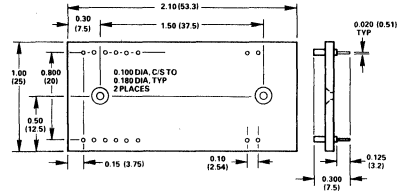
NOTES
*Specifications same as 1B41AN.
[1]All specifications use the test circuit of Figure 1.
[2]Excluding external ranging resistor errors.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC 1227 MATING SOCKET

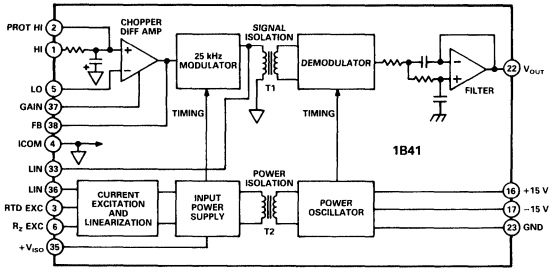


PIN DESIGNATIONS

PIN	DESIGNATION
1	HI
2	PROT HI
3	RTD EXC
4	ICOM
5	LO
6	R_Z EXC
16	+15 V
17	−15 V
22	V_O
23	GND
33	LIN
35	$+V_{ISO}$
36	LIN
37	GAIN
38	FB

INSIDE THE 1B41

Referring to the functional block diagram, the ±15 V power inputs provide power to both the output side circuitry and the power oscillator. The 25 kHz power oscillator provides both the timing information for the signal demodulator and drives transformer T2 for the input side power supplies. The secondary winding of T2 is half wave rectified and filtered to create the input side power.



1B41 Functional Block Diagram

Dual current sources of 0.25 mA are derived from the floating power supply and accomplish 3-wire compensation as well. This creates a voltage difference between the RTD and R_Z. This voltage is applied to the chopper stabilized differential amplifier. Linearization can be implemented at this stage by a simple jumper option. This creates a bow in the current source that nulls out the nonlinearity of Pt 100 RTDs.

The signal input (HI) is single pole filtered for noise rejection and antialiasing. PROT HI is the output node of the filter, and is used only for special input applications as described in the applications section of this data sheet.

The chopper stabilized gain stage amplifies the differential input voltage with a gain set by external resistors.

The signal is amplitude modulated onto a 25 kHz carrier and passed through the signal transformer T1. The synchronous demodulator restores the signal to the baseband. A two-pole active low pass stage filters out clock noise and completes a three-pole Butterworth filter formed with the input pole.

USING THE 1B41

Range Setting: The gain of the 1B41 is controlled on the input side by a pair of user provided resistors (see Figure 1). A feedback resistor of 20 kΩ ±1% is required between the feedback pin (Pin 38) and the gain pin (Pin 37). The gain setting resistor is connected between the gain pin (Pin 37) and input side common (Pin 4).

In the equations below R_Z is the value of the RTD resistance at the temperature at which zero volts ouptut is desired, R_{HS} is the resistance of the RTD when the temperature is the average of the zero ouput temperature and the full-scale temperature, and R_{FS} is the resistance of the RTD at the full-scale temperature.

$$R_G = 20\ k\Omega/(G-1)$$

$$R_{LIN} = 6.1\ k\Omega(2Q-3)/(2-Q)$$

where $Q \equiv \Delta R_{FS}/\Delta R_{HS}$

$G \equiv (20\ k\Omega/\Delta R_{FS})(Q-1)$

$\Delta R_{FS} = R_{FS} - R_Z$

$\Delta R_{HS} = R_{HS} - R_Z$

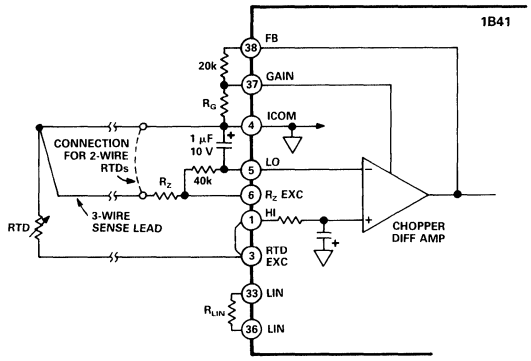


Figure 1. 1B41 Basic Hookup

Since gain and linearization are interactive, it is recommended that any offset and span errors be removed in software or at a later stage in the data acquisition circuitry.

The accuracy of the resistor values must be taken into account when calculating the initial gain accuracy of an application. The initial accuracy of the 1B41 must then be added to the resistor errors to predict the total accuracy. Likewise, the ratiometric temperature coefficient of the gain and feedback resistors must be added to the temperature coefficient of the 1B41 to predict the total resulting thermal drift.

3-Wire Compensation: The 1B41 accomplishes 3-wire compensation by using matched current sources on both RTD EXC (Pin 3) and R_Z EXC (Pin 6). Figure 2 shows lead wires with resistances of R_{L1}, R_{L2} and R_{L3}. The following equation describes the error voltage caused by lead resistance and the current source mismatch.

$$V_{ERROR} = I_1R_{L3} - I_2R_{L2}$$

This equation depends upon the matching of the wire resistance and the matching of the 1B41 current sources. When all leads have the same resistance and the current sources are matched, no error is introduced.

For 2-wire RTDs, ICOM (Pin 4) can be connected as shown in Figure 1. This does not compensate for lead wire resistance.

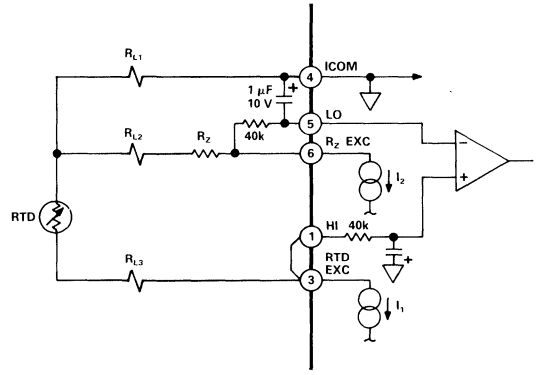


Figure 2. 3-Wire Compensation

Note that since the current sources are in fact *current sinks*, as the RTD resistance increases, the voltage at HI (Pin 1) gets more negative. This causes the output of the 1B41 to get more positive.

Example: A 100 Ω platinum RTD, α = 0.00385, is 100 Ω at 0°C, 138.50 Ω at 100°C, and 175.84 Ω at 200°C.

$$R_Z = 100\ \Omega,\ R_{HS} = 138.50\ \Omega,\ R_{FS} = 175.84\ \Omega$$

$$Q = \frac{175.84 - 100}{138.50 - 100} = 1.9699$$

$$R_{LIN} = \frac{6.1\ k\Omega(2 \times 1.9699 - 3)}{(2 - 1.9699)} = 190.46\ k\Omega$$

$$R_G = \frac{20\ k\Omega}{255.78 - 1} = 78.5\ \Omega$$

PERFORMANCE

CMR and NMR: Common mode rejection is a result of both isolation and filtering, and is dependent on signal frequency, conditioner gain and source impedance imbalance.

The CMR performance is also enhanced by low pass filtering, giving an effective CMR of 160 dB at 60 Hz (f_C = 3 Hz) at the output of the filter.

Gain Nonlinearity: 1B41 gain nonlinearity is defined as the deviation of the output voltage from the best straight line and is specified as % peak-to-peak of a ±10 V output span.

APPLICATION EXAMPLES

Input Protection: Although the 1B41 provides ±1500 V of common mode protection, it is sometimes desirable to have some level of normal mode protection as well. The signal input of the 1B41 is normally less than 500 mV but could be very large under a fault condition.

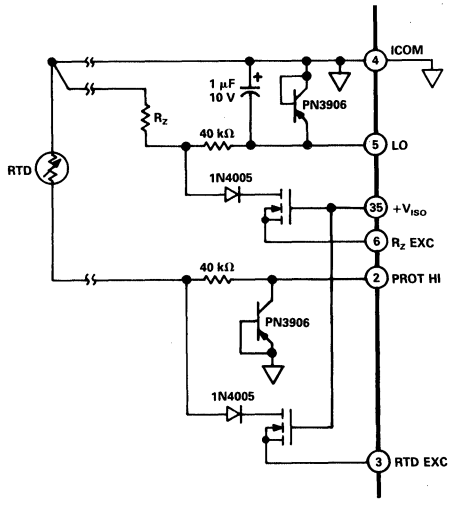


Figure 3. 120 V/240 V AC Normal Mode Input Protection

Referring to Figure 3, the inputs and current sources show 240 V rms protection. The PN3906 pnp transistors are used for the diode properties of the base emitter junction. When the emitter is more positive than the base, the transistor functions as a forward biased diode. When the emitter is negative with respect to the base, the junction is a very low leakage Zener diode with a breakdown voltage of about −8 V. This serves as a voltage clamp for LO and PROT HI. A fault voltage applied between ICOM and either of the two inputs will appear mostly across the 40 kΩ resistor. The power dissipated in the resistor is approximately 1.44W for a 240 V fault.

Each current source is protected by a MOSFET and a diode. The MOSFET is an n-channel enhancement mode device. The RTD EXC and R_Z EXC pins are normally about −3.5 V with respect to ICOM. The voltage at $+V_{ISO}$ is about +6.5 V, yielding a V_{GS} of about 10 V. For normal operation, the FET must be saturated on. A device with a threshold voltage of less than 5 V at 1 mA I_{DS} guarantees saturation.

The V_{DS} breakdown voltage must be greater than the expected fault voltage. At 240 V rms, the peak voltage is 339V, so the FET must have a breakdown voltage of at least 350 V. The power dissipation requirements are minimal, however. The power dissipated in the FET under fault mode is 240 V×0.25 mA×0.5 = 30 mW. The factor of 0.5 is due to the 50% duty cycle. This allows a compact TO-92 packaged device, such as the VN0650.

During the other half of the cycle, the fault voltage is applied across the series diode. The diode must have a reverse breakdown voltage of at least 350 V.

Other RTD Measurements. The 1B41 can be configured for making differential measurements using 2-wire RTDs. As shown in Figure 4, the two RTDs are connected between ICOM and HI and LO. The current sources at R_Z EXC and RTD EXC create a differential signal across HI and LO that is proportional to the difference in resistance of the two RTDs. The following equation shows how to calculate R_G for applications where hardware linearization is not desired.

$$R_G = \frac{40\ k\Omega}{G - 2}$$

The LIN pins (Pins 33 and 36) must be left unconnected to maintain a constant current source.

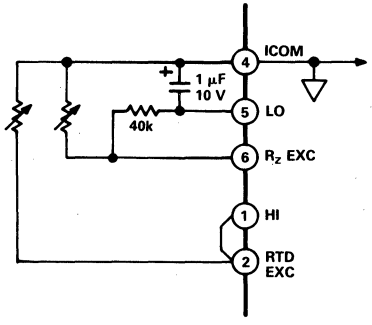


Figure 4. Differential RTD Measurement

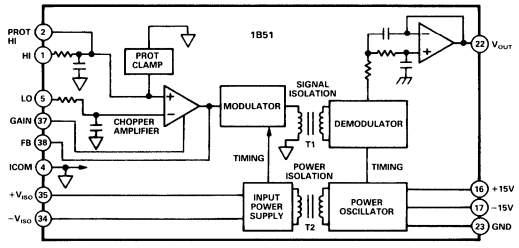
Isolated mV/Thermocouple Signal Conditioner

1B51

FEATURES
- **Functionally Complete Precision Conditioner**
- **High Accuracy**
  - **Low Input Offset Tempco: ±0.1μV/°C**
  - **Low Nonlinearity: ±0.025%**
  - **High CMR: 160dB (60Hz, G=1000V/V)**
- **High CMV Isolation: 1500V rms Continuous**
- **240V rms Input Protection**
- **Small Package: 1.0″×2.1″×0.35″ DIP**
- **Isolated Power**
- **Low Pass Filter (f_C=3Hz)**
- **Pin Compatible with 1B41 Isolated RTD Conditioner**

APPLICATIONS
- **Multichannel Thermocouple Temperature Measurement**
- **Low Level Data Acquisition Systems**
- **Industrial Measurement & Control Systems**

1B51 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 1B51 is a precision, mV/thermocouple signal conditioner that incorporates a circuit design utilizing transformer based isolation and automated surface mount manufacturing technology. It provides an unbeatable combination of versatility and performance in a compact plastic package. Designed for measurement and control applications, it is specially suited for harsh environments with extremely high common-mode interference. Unlike costlier solutions that require separate dc/dc converters, each 1B51 generates its own input side power, providing true, low cost channel-to-channel isolation.

Functionally, the signal conditioner consists of three basic sections: chopper stabilized amplifier, isolation and output filter. The chopper amplifier features a highly stable offset tempco of ±0.1μV/°C and resistor programmable gains from 2 to 1000. Wide range zero suppression can be implemented at this stage.

The isolation section has complete input to output galvanic isolation of 1500V rms continuous using transformer coupling techniques. Isolated power of 2mA at ±6.2V is provided for ancillary circuits such as zero suppression and open-input detection. Filtering at 3Hz is implemented by a passive antialiasing filter at the front end and a two-pole active filter at the output. Overall NMR is 60dB and CMR is 160dB min @ 60Hz, G=1000.

The 1B51 is specified over −25°C to +85°C and operates over the industrial (−40°C to +85°C) temperature range.

DESIGN FEATURES AND USER BENEFITS

High Noise Rejection: The combination of a chopper stabilized front end with a low pass filter provides high system accuracy in harsh industrial environments as well as excellent rejection of 50/60Hz noise.

Input Protection: The input is internally protected against continuous application of 240V rms.

Low Cost: The 1B51 offers a very low cost per channel for high performance, isolated, low level signal conditioners.

Wide Range Zero Suppression: This input referred function is a convenient way to null large input offsets.

Low Pass Filter: The three pole active filter (f_C=3Hz) reduces 60Hz noise and aliasing errors.

Small Size: The 1B51 package size (1.0″×2.1″×0.35″) and functional completeness make it an excellent choice in systems with limited board space and clearance.

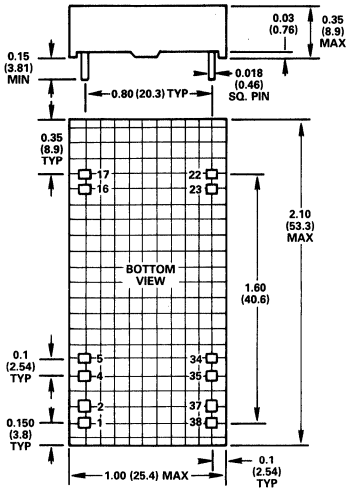
SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

Model	1B51AN	1B51BN
GAIN		
Gain Equation	$G=\left[1+\frac{R_{FB}}{R_G}\right] \times 2$	*
Gain Error	1% max	*
Gain Temperature Coefficient[1]	50ppm/°C	*
Gain Nonlinearity	±0.035% (±0.05% max)	±0.025% (±0.04% max)
OFFSET VOLTAGES		
Input Offset Voltage		
Initial, @ +25°C (Adjustable to Zero)	25µV (100µV max)	*
vs. Temperature	±0.1µV/°C (±0.5µV/°C max)	*
vs. Time, Noncumulative	±1µV/month max	*
Output Offset Voltage		
Initial	−50mV	−25mV
vs. Temperature	−175µV/°C	−50µV/°C
INPUT OFFSET CURRENT		
Initial	0.6nA (2.5nA max)	*
vs. Temperature	±2.5pA/°C (12.5pA/°C max)	*
INPUT BIAS CURRENT		
Initial @ +25°C	10nA	*
vs. Temperature	10pA/°C	*
INPUT IMPEDANCE		
Power On	50MΩ	*
Power Off	40kΩ min	*
INPUT VOLTAGE RANGE		
Linear Differential Input	±10mV to ±5V	*
Max CMV, Input to Output		
ac, 60Hz, Continuous	1500V rms	*
Continuous, dc	±2000V	*
CMR @ 60Hz, 1kΩ Source Imbalance, G = 1000	160dB min	*
NMR @ 60Hz	60dB min	*
Transient Protection	IEEE-STD 472 (SWC)	*
INPUT NOISE		
Voltage, 0.1Hz to 10Hz, 1kΩ Source Imbalance	1µV p-p	*
RATED OUTPUT		
Voltage, 2kΩ Load, min	±10V	*
Current	±5mA	*
Output Noise, dc to 100kHz	1mV p-p	*
Impedance, dc	0.1Ω	*
FREQUENCY RESPONSE		
Bandwidth, −3dB	dc to 3Hz	*
ISOLATED POWER		
Voltage, No Load	±6.2V±5%	*
Current	2mA	*
Regulation, No Load to Full Load	7.5%	*
Ripple	250mV p-p	*
POWER SUPPLY		
Voltage, Rated Performance	±15V dc	*
Voltage, Operating	±13.5V to ±18V	*
Current, Quiescent	+12mA @ +15V, −4mA @ −15V	*
PSRR	0.1%/V	*
ENVIRONMENTAL		
Temperature Range		
Rated Performance	−25°C to +85°C	*
Operating	−40°C to +85°C	*
Storage	−40°C to +85°C	*
Relative Humidity	0 to 95% @ +60°C	*
CASE SIZE	1.00″×2.10″×0.35″ (25.4×53.3×8.9)mm	*

NOTES
*Specifications same as 1B51AN.
[1]See graph in text.
Specifications subject to change without notice.

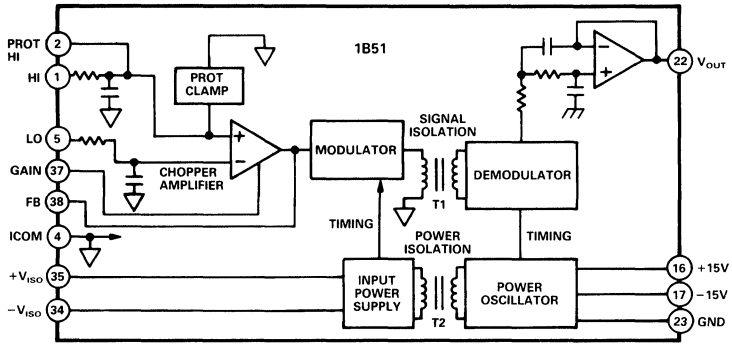
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	DESIGNATION
1	HI
2	PROT HI
4	ICOM
5	LO
16	+15V
17	−15V
22	V_O
23	GND
34	$-V_{ISO}$
35	$+V_{ISO}$
37	GAIN
38	FB



Functional Block Diagram

INSIDE THE 1B51

Referring to the functional block diagram, the ±15V power inputs provide power to both the output side circuitry and the power oscillator. The 25kHz power oscillator provides the timing information for the signal demodulator and drives power transformer T2 for the input side power supplies. The secondary winding of T2 is half wave rectified and filtered to create the input side bipolar unregulated supplies.

The signal input (HI) is single-pole filtered for noise rejection and antialiasing. The protection clamps limit the voltage at PROT HI to ±8V. Thus, a large voltage applied between HI and input common (I COM) appears mostly across the input resistor.

The chopper stabilized gain stage amplifies the differential input voltage with a gain set by external resistors. The voltage at the inverting input of the chopper stabilized amplifier (LO) should be equal to the input voltage at which the desired output voltage is zero. This is a true input referred zero suppression function.

The signal is amplitude modulated onto a 25kHz carrier and passed through the signal transformer T1. The synchronous demodulator restores the signal to the baseband. A two-pole active low pass stage filters out clock noise and completes a three-pole Butterworth filter formed with the input pole.

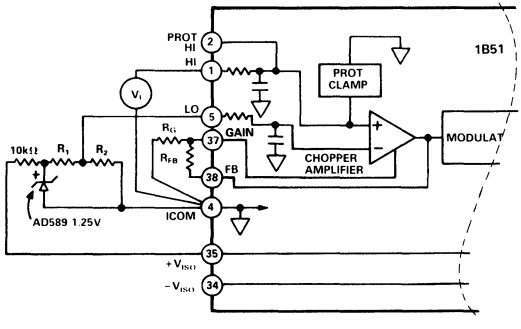


Figure 1. Input Gain Setting and Zero Supression

USING THE 1B51

Gain Setting:

The gain of the 1B51 is controlled on the input side by a pair of user provided resistors (see Figure 1). A feedback resistor of between 10kΩ and 20kΩ is required between the feedback pin (FB) and the gain pin. The gain setting resistor is connected between the gain pin and input side common (ICOM). The gain equation is

$$G = \left[1 + \frac{R_{FB}}{R_G}\right] \times 2$$

Gains of 2–1000 can be achieved by adjusting this ratio.

The accuracy of the resistor values must be taken into account when calculating the initial gain accuracy of an application. The initial accuracy of the 1B51 must then be added to the resistor errors to predict the total accuracy. Likewise, the ratiometric temperature coefficient of the gain and feedback resistors must be added to the temperature coefficient of the 1B51 to predict the total resulting thermal drift.

It is possible to use a trimming potentiometer to correct for initial gain and system gain errors. The feedback resistor can be comprised of a resistor in series with a trimming potentiometer, as long as the total resistance remains between 10kΩ and 20kΩ. Alternatively, the gain resistor can also be an adjustable resistor. In general, the greater the trim range, the coarser the resolution.

Zero Suppression:

Since the 1B51 is a differential input device, true input referred zero suppression can be accomplished (see Figure 1). A voltage reference powered by the input side power supplies is applied to the LO terminal. Since the transfer function is

$$V_O = (V(HI) - V(LO)) \times GAIN$$

the input voltage for which the desired output is zero should be applied to the LO pin. The equation is

$$V_Z = 1.25(R_2/(R_1 + R_2))$$

Any drift of this input zero suppression voltage appears as offset drift, so a temperature stable reference should be used. The source impedance at the LO terminal should be kept below 1kΩ.

Open Input Detection:
The 1B51 can sense an open thermocouple or broken input line with the addition of an external resistor. By connecting a 220MΩ resistor between the HI pin and the positive or negative isolated supply, an open input will cause a positive or negative full scale output, respectively.

To preserve the normal mode input protection capability of the 1B51, the resistor must be able to withstand 220Vac. A high voltage rating can be obtained by connecting lower value resistors in series.

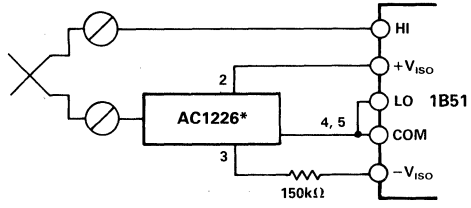
Cold Junction Compensation:
When using a thermocouple as an input to the 1B51, a second thermocouple junction is formed at the terminations of the thermocouple wires, commonly referred to as the cold junction. The measured output voltage of the sensor is the voltage generated by the thermocouple minus the voltage generated by the cold junction.

Since thermocouples are specified with 0V representing 0°C, it would be ideal to maintain the cold junction at 0°C. A more practical approach involves adding a temperature dependent voltage to the thermocouple signal so as to oppose the cold junction effects. This type of correction is known as cold junction compensation.

Many different methods are commonly used to implement cold junction compensation. Usually a thermistor or a semiconductor sensor is used to generate the cold junction voltage. The slope of the cold junction voltage must be the same as that of the thermocouple. Therefore, the cold junction compensation depends on the thermocouple type.

Sometimes, one cold junction compensation sensor is used by a number of thermocouple channels. This is accomplished by measuring the temperature of the connection block directly, and adding the appropriate voltage to each uncompensated thermocouple channel after the gain has been taken. *In all cases, the cold junction sensor must be in the thermal proximity with the connection block.*

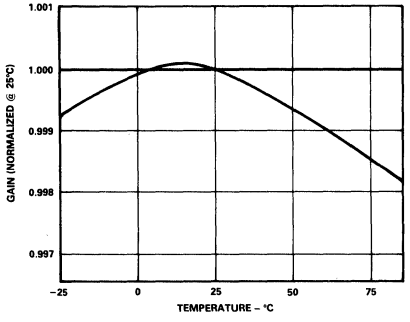
Figure 2 shows a monolithic cold junction compensation device used with the 1B51. The Analog Devices AC1226 measures the ambient temperature and generates the appropriate cold junction voltage for several different thermocouple types.



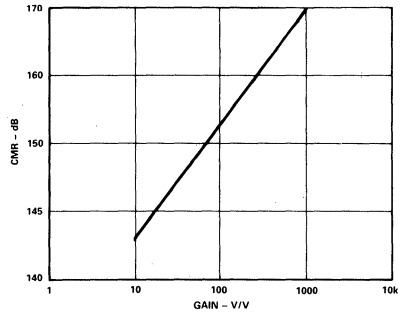
*PIN NUMBER DEPENDS ON THERMOCOUPLE TYPE. SEE AC1226 DATA SHEET FOR DETAILS.

Figure 2. 1B51 Cold Junction Compensation

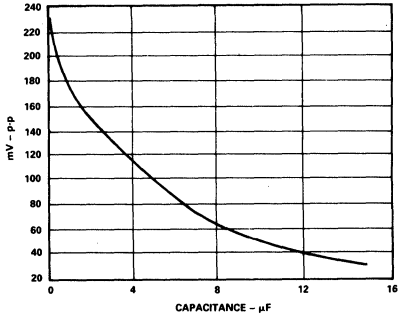
TYPICAL PERFORMANCE CURVES (@T_A = +25°C, V_S = ±15V)



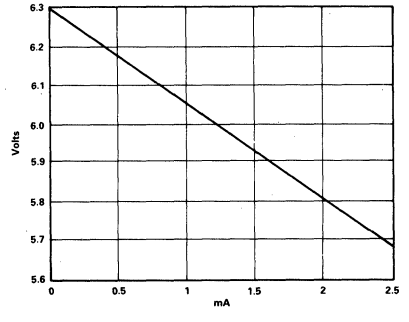
Gain vs. Temperature



CMR vs. Gain



+V_{ISO} Ripple vs. Capacitance



+V_{ISO} vs. Load

High Performance, 4–20mA Output Voltage-to-Current Converter

2B20

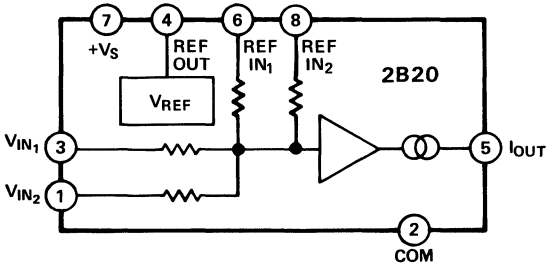
FEATURES

- Complete, No External Components Needed
- Small Size: 1.1″ x 1.1″ x 0.4″ Module
- Input: 0 to +10V; Output: 4 to 20mA
- Low Drift: 0.005%/°C max; Nonlinearity: 0.005% max (2B20B)
- Wide Temperature Range: -25°C to +85°C
- Single Supply: +10V to +32V
- Meets ISA Std 50.1 for Type 3, Class L and U, Nonisolated Current Loop Transmitters
- Economical

APPLICATIONS

- Industrial Instrumentation and Control Systems
- D/A Converter – Current Loop Interface
- Analog Transmitters and Controllers
- Remote Data Acquisition Systems

2B20 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 2B20 is a complete, modular voltage-to-current converter providing the user with a convenient way to produce a current output signal which is proportional to the voltage input. The nominal input voltage range is 0 to +10V. The output current range is 4 to 20mA into a grounded load.

Featuring low drift (0.005%/°C max, 2B20B) over the -25°C to +85°C temperature range and single supply operation (+10V to +32V), model 2B20 is available in two accuracy grades. The 2B20B offers precision performance with nonlinearity error of 0.005% (max) and guaranteed low offset error of ±0.1% max and span error of ±0.2% max, without external trims. The 2B20A is an economical solution for applications with lesser accuracy requirements, featuring nonlinearity error of 0.025% (max), offset error of ±0.4% (max), span error of ±0.6% (max), and span stability of 0.01%/°C max.

The 2B20 is contained in a small (1.1″ x 1.1″ x 0.4″), rugged, epoxy encapsulated package. For maximum versatility, two signal input (V_{IN1} and V_{IN2}) and two reference input (REF_{IN1} and REF_{IN2}) terminals are provided. Utilizing terminals V_{IN1} and REF_{IN1} eliminates the need for any external components, since offset and span are internally calibrated. If higher accuracy (up to ±0.01%) is required, inputs V_{IN2} and REF_{IN2} with series trim potentiometers may be utilized.

APPLICATIONS

Model 2B20 has been designed for applications in process control and monitoring systems to transmit information between subsystems or separated system elements. The 2B20 can serve as a transmission link between such elements of process control system as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners.

In a typical application, model 2B20 may act as an interface between the D/A converter output of a microcomputer based system and a process control device such as a variable position valve. Another typical application of the 2B20 may be as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-to-pneumatic transducers.

DESIGN FEATURES AND USER BENEFITS

Process Signal Compatibility: To provide output signal compatibility, the 2B20 meets the requirements of the Instrument Society of America Standard S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 3, Class L and U, nonisolated current loop transmitters.

External Reference Use: For increased flexibility, when ratiometric operation is desired, the 2B20 offers a capability of connecting an external reference (i.e., from multiplying D/A converter) to the REF_{IN2} terminal.

Wide Power Supply Range: A wide power supply range (+10V to +32V dc) allows for operation with either a +12V battery, a +15V powered data acquisition system, or a +24V powered process control instrumentation.

SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

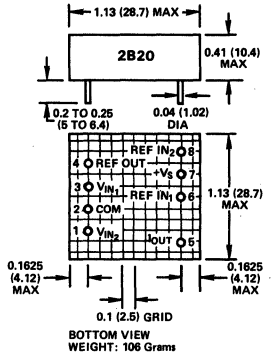
Model	2B20A	2B20B
INPUT SPECIFICATIONS		
Voltage Signal Range	0 to +10V	*
Input Impedance	10kΩ	*
OUTPUT SPECIFICATIONS		
Current Output Range[1]	4 to 20mA	*
Load Resistance Range[2]		
V_S = +12V	0 to 350Ω max	*
V_S = +15V	0 to 500Ω max	*
V_S = +24V	0 to 950Ω max	*
NONLINEARITY (% of Span)	±0.025% max	±0.005% max
ACCURACY[3]		
Warm-Up Time to Rated Specs	1 minute	*
Total Output Error @ +25°C[3,4]		
Offset (V_{IN} = 0 volts)	±0.4% max	±0.1% max
Span (V_{IN} = +10 volts)	±0.6% max	±0.2% max
vs. Temperature (-25°C to +85°C)		
Offset (V_{IN} = 0 volts)	±0.01%/°C max	±0.005%/°C max
Span (V_{IN} = +10 volts)	±0.01%/°C max	±0.005%/°C max
DYNAMIC RESPONSE		
Settling Time – to 0.1% of F.S.		
for 10V Step	25μs	*
Slew Rate	2.5mA/μs	*
REFERENCE INPUT[5]		
Voltage	+2.5V dc	*
Input Impedance	10kΩ	*
POWER SUPPLY		
Voltage, Rated Performance	+15V dc	*
Voltage, Operating	+10V to +32V dc max	*
Supply Change Effect (% of Span)[6]		
on Offset	±0.005%/V	*
on Span	±0.005%/V	*
Supply Current	6mA + I_{LOAD}	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Storage	-55°C to +125°C	*
CASE SIZE	1.125" X 1.125" X 0.4"	*

NOTES
*Specifications same as 2B20A.
[1] Current output sourced into a grounded load over a supply voltage range of +10V to +32V.
[2] See Figure 1 for the maximum load resistance value over the power supply range.
[3] Accuracy is guaranteed with no external trim adjustments when REF_{IN} is connected to REF_{OUT}.
[4] All accuracy is specified as % of output span where output span is 16mA (±0.1% = ±0.016mA output error).
[5] Reference input is normally connected to the reference output (+2.5V dc).
[6] Optional trim pots may be used for calibration at each supply voltage.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1016

LOAD RESISTANCE RANGE

The load resistance is the sum of the resistances of all connected receivers and the connection lines. The 2B20 operating load resistance is power supply dependent and will decrease by 50 ohms for each 1 volt reduction in the power supply. Similarly, it will increase by 50 ohms per volt increase in the power supply, but must not exceed the safe voltage capability of the unit.

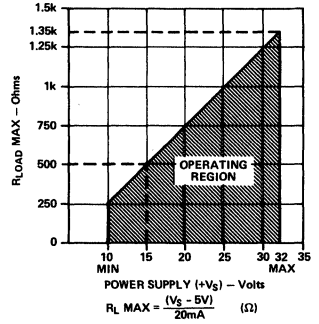


Figure 1. Maximum Load Resistance vs. Power Supply

PRINCIPLE OF OPERATION

The design of the 2B20 is comprised of high performance op amps, precision resistors and a high stability voltage reference to develop biasing and output drive capability. The 2B20 is designed to operate from a single positive power supply over a wide range of +10V to +32V dc and accepts a single ended, 0 to +10V voltage input. The internal reference has nominal output voltage of +2.5V (REF_{OUT}) and is used to develop 4mA output current for a zero volts input when REF_{IN} is connected to REF_{OUT}.

The output stage of the 2B20 utilizes a sensing resistor in the feedback loop, so the output current is linearly related to the voltage input and independent of the load resistance. There is no minimum resistance for the loads driven by the 2B20; it can drive even a short circuit with no damage to the unit. The maximum resistance of the load as seen by the unit (resistance of the load plus the resistance of the connecting wire) is limited. The maximum external loop resistance, R_L, is given by:

$$R_L\ (\Omega)\ max = \left(\frac{+V_S - 5V}{20mA}\right)$$

Figure 1 shows the operating region of the 2B20. The load must be returned to power supply common. The voltage appearing between I_{OUT} (pin 5) and COM (pin 2) should not exceed $V_{max} = +V_S - 5V$. Exceeding this value (up to +32V dc) will not damage the unit, but it will result in a loss of linearity.

The basic connections of the 2B20 are shown in Figure 2.

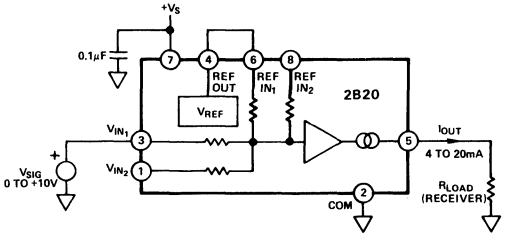


Figure 2. Basic Connections Diagram

OPTIONAL CALIBRATION AND TRIM PROCEDURE

Model 2B20's factory trimmed offset error is ±0.1% max and span error is ±0.2% max (2B20B). In most applications, further trimming will not be required. If it is necessary to obtain calibrated accuracy of up to ±0.01%, or, if a high signal source resistance (with respect to 10kΩ) introduces calibration error, inputs V_{IN2} and REF_{IN2} and optional trim pots should be used with V_{IN1} and REF_{IN1} open. To perform external trims, connect 500Ω potentiometers in series with V_{IN2} (span trim) and REF_{IN2} (offset trim) as shown in Figure 3. Adjust span pot, monitoring voltage drop across R_{LOAD}, to obtain an output voltage of 5.000V (I_{OUT}=20mA) for a +10V input. Next, with 0 volts input, adjust offset pot to obtain 1.000V output (I_{OUT}=4mA). Check both offset and span and retrim if necessary after each adjustment.

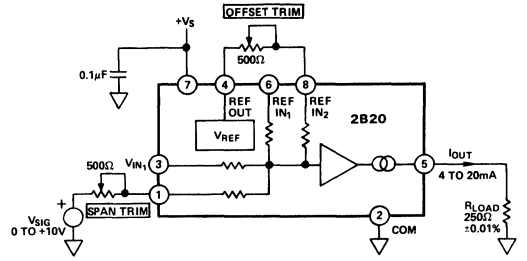


Figure 3. Model 2B20 Connections Using Optional Offset and Span Trims

CONNECTING THE 2B20 FOR 0 TO 10mA OUTPUT

The 2B20 may be utilized in applications requiring 0 to 10mA current output for a 0 to +10V input voltage range as shown in Figure 4a. To obtain 0mA output for 0V input, adjust the offset potentiometer until there is no current flowing in the output. The 2B20 span calibration may be adjusted by a 2kΩ gain potentiometer in series with the V_{SIG} input.

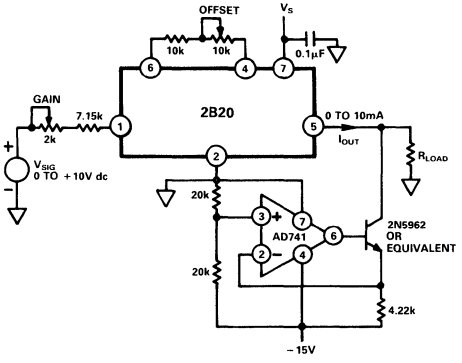


Figure 4a. 2B20 Configuration for 0 to 10mA Operation

CONNECTING THE 2B20 FOR 0 TO 20mA OUTPUT

The 2B20 may also be configured for use in applications requiring 0 to 20mA output for a 0 to +10V input range as shown in Figure 4b. To obtain 0mA output for 0V input, adjust the offset potentiometer. The 2B20 span calibration may be adjusted by a 2kΩ gain potentiometer in series with the V_{SIG} input.

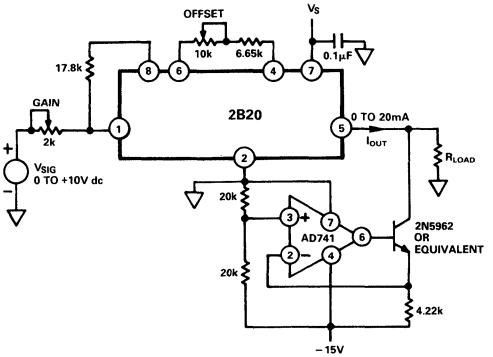


Figure 4b. 2B20 Configuration for 0 to 20mA Operation

OUTPUT PROTECTION

In many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 5 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

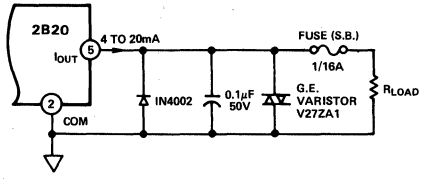


Figure 5. Output Protection Circuitry Connections

APPLICATIONS

Interfacing Voltage Output D/A Converters: The 2B20 is well suited in applications requiring 4 to 20mA output from D/A converters. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 6. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B20 (or the AD DAC80). First, a digital input code of all ones is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all 0s is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA -1LSB = 19.9961mA.

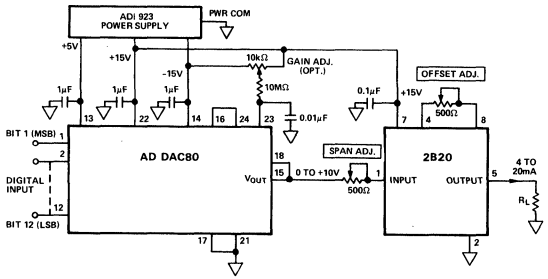


Figure 6. AD DAC80 – 4 to 20mA Current Loop Interface

Interfacing Current Output D/A Converters: To interface current output D/A converters, such as the AD562, a circuit configuration illustrated in Figure 7 should be used. Since the AD562 is designed to operate with an external +10V reference, the same external reference may be utilized by the 2B20 for ratiometric operation. The output of the AD562 is used to drive the summing junction of an operational amplifier to produce an output voltage. Using the internal feedback resistor of the AD562 provides a 0 to +10V output voltage range suitable to drive the 2B20.

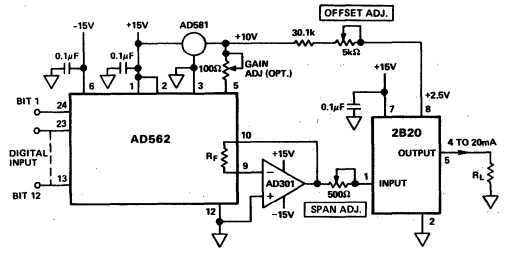


Figure 7. 12-Bit – 4 to 20mA Current Loop Interface

Microcomputer – Current Loop Interface: Figure 8 shows a typical application of the 2B20 in a multichannel microcomputer analog output system. When a microcomputer is to control a final control element, such as a valve positioner, servomechanism or motor, an analog output board with 4 to 20mA outputs is often necessary. The output boards typically have from one to eight channels, each with its own D/A converter. The 2B20, in a compact package, allows for an easy installation without any additional components and offers a 12-bit system compatible performance.

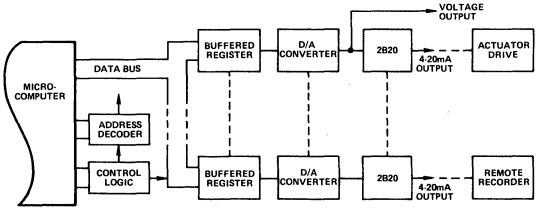


Figure 8. Microcomputer Analog Output Subsystem

Pressure Control System: In Figure 9, model 2B20 is used in a proportional pressure control system. The 3-15psi working pressure of a system is monitored with a pressure transducer interfaced by the model 2B31 signal conditioner. The high level voltage output of the 2B31 is converted to a 4 to 20mA to provide signal to the limit alarm and proportional control circuitry. A current-to-position converter controlling a motorized valve completes the pressure-control loop.

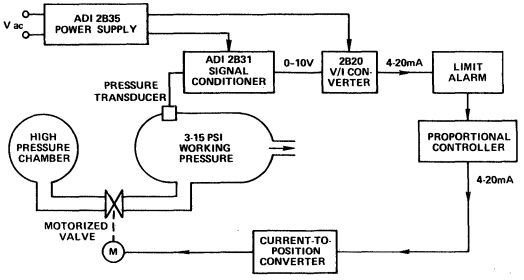


Figure 9. Proportional Pressure Control System

Isolated 4 to 20mA Output: For applications requiring up to ±1500V dc input to output isolation, consider using Analog Devices' model 2B22 isolated voltage-to-current converter.

ANALOG DEVICES

High Performance, Isolated Voltage-to-Current Converter

2B22

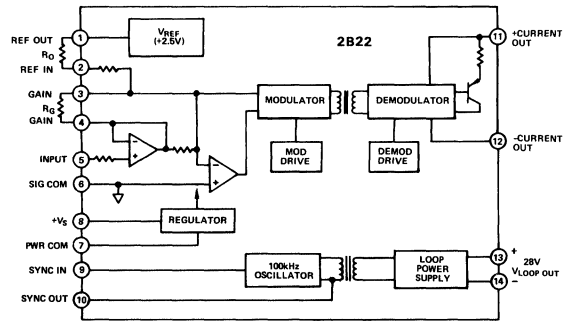
FEATURES

Wide Input Range: 0 to +1V to 0 to +10V
Standard Output Range: 4 to 20mA
High CMV Input/Output Isolation: 1500V dc Continuous
Low Nonlinearity: 0.05% max, 2B22L
Low Span Drift: 0.005%/°C max, 2B22L
Single Supply: +14V to +32V
Meets IEEE Std 472: Transient Protection (SWC)
Meets ISA Std 50.1: Isolated Current Loop Transmitters

APPLICATIONS

Industrial Instrumentation and Process Control
Ground Loop Elimination
High Voltage Transient Protection
D/A Converter – Current Loop Interface
Analog Transmitters and Controllers
Remote Data Acquisition Systems

2B22 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 2B22 is a high performance, compact voltage-to-current converter offering 1500V dc input to output isolation in interfacing standard process signals. The input stage of the model 2B22 is single resistor programmable to accept voltage ranges from 0 to +1V to 0 to +10V. The isolated output current range is 4 to 20mA, and the 2B22 can be operated with 0 to 1000Ω grounded or floating loads.

Using modulation techniques with transformer isolation for reliable performance, the 2B22 is available in three accuracy selections offering guaranteed nonlinearity error (2B22L: ±0.05% max, 2B22K: ±0.1% max, and 2B22J: ±0.2% max) and guaranteed low span drift: ±0.005%/°C max, ±0.01%/°C max, and ±0.015%/°C max, respectively. The internally trimmed span and offset errors are ±0.1% max for the 2B22L and ±0.25% max for the 2B22J/2B22K. Both span and offset are adjustable by the optional external potentiometers.

Featuring a wide range, single supply operation (+14V to +32V), the 2B22 provides isolated +28V loop power and is capable of delivering rated current into an external 0 to 1000Ω load resistance. The unique output stage configuration also allows the user to utilize an optional external loop power supply to interface systems designed for a two-wire operation.

APPLICATIONS

Model 2B22 has been specifically designed for high accuracy applications in process control and monitoring systems to offer complete galvanic isolation and protection against damage from transients and fault voltages in transmitting information between subsystems or separated system elements. The 2B22 meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 4, Class U isolated current loop transmitters.

In the industrial environment, model 2B22 can serve as a transmission link between such system elements as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners. In data acquisition and control systems, the 2B22 may act as an isolated interface between the D/A converter output of a microcomputer and standard 4 to 20mA analog loops.

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 2B22 is a conservatively designed, compact module capable of reliable operation in harsh environments. To assure high reliability, the 2B22 has a calculated MTBF of over 270,000 hours and has been designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

Process Signal Compatibility: The versatile input stage design with a single resistor gain adjustment enables the 2B22 to accept any one of the standard inputs—0-1V, 0-10V, 1-5V; or 1-5mA, 4-20mA, 10-50mA; and provide standard, isolated 4-20mA output.

Isolated Loop Power: Internal 28V dc loop supply, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to drive 0 to 1000Ω loads and eliminates the need for an external dc/dc converter.

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SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

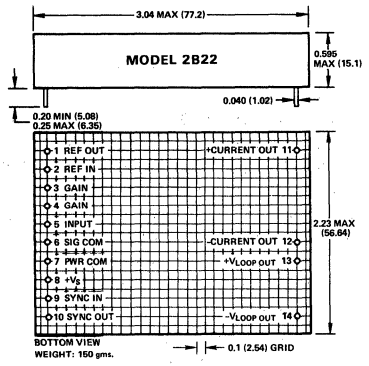
Model	2B22J	2B22K	2B22L
INPUT SPECIFICATIONS			
Voltage Signal Range, G = 1.6mA/V	0 to +10V	*	*
G = 16mA/V	0 to +1V	*	*
Gain Range	1.6 to 16mA/V	*	*
Maximum Safe Input	+15V	*	*
Input Impedance	10MΩ	*	*
OUTPUT SPECIFICATIONS			
Current Output Range	4 to 20mA	*	*
Load Resistance Range, V_S = +14V to +32V, Internal Loop Power	0 to 1000Ω max	*	*
Maximum Output Current, @ Input Overload	25mA	*	*
Output Ripple, 100Hz Bandwidth G = 1.6mA/V	60μA pk-pk	*	*
NONLINEARITY (% of Span)	±0.2% max	±0.1% max	±0.05% max
CMV, INPUT TO OUTPUT			
ac, 60Hz, 1 Minute Duration	1500V rms	*	*
Continuous, ac or dc	±1500V pk max	*	*
CMR, INPUT TO OUTPUT			
60Hz, 1kΩ Source Imbalance	90dB	*	*
ACCURACY[1]			
Warm Up Time to Rated Performance 5 Minutes			
Total Output Error @ +25°C[1,2]			
Offset (V_{IN} = 0V)	±0.25% max	±0.25% max	±0.1% max
Span (V_{IN} = +10V)	±0.25% max	±0.25% max	±0.1% max
vs. Temperature (0 to +70°C, G = 1.6mA/V)			
Offset (V_{IN} = 0V)	±0.01%/°C max	±0.005%/°C max	±0.0025%/°C max
Span (V_{IN} = +10V)	±0.015%/°C max	±0.01%/°C max	±0.005%/°C max
vs. Temperature (0 to +70°C)			
Offset (V_{IN} = 0V, G = 1.6mA/V to 16mA/V)	±0.01%/°C	±0.005%/°C	±0.0025%/°C
Span (G = 1.6mA/V to 16mA/V)[3]	±0.015%/°C	±0.01%/°C	±0.005%/°C
DYNAMIC RESPONSE			
Settling Time – to 0.1% of F.S. for 10V Step	300μs	*	*
Slew Rate	0.06mA/μs	*	*
REFERENCE INPUT			
Voltage	+2.5V dc	*	*
Input Impedance	6kΩ	*	*
OSCILLATOR			
Frequency, Internal Oscillator	100kHz ± 10%	*	*
External Sync Input			
Frequency	100kHz ± 10% max	*	*
Waveform	Square wave, 50% duty cycle	*	*
Voltage	20V p-p	*	*
POWER SUPPLY			
Voltage, Rated Performance	+15V dc	*	*
Voltage, Operating	+14V to +32V dc	*	*
Supply Current (at Full Scale Output)			
Using Internal Loop Power	100mA	*	*
Using External Loop Power	50mA	*	*
Supply Change Effect (% of Span)			
on Offset (V_{IN} = 0V)	±0.0005%/V	*	*
on Span (V_{IN} = +10V)	±0.0005%/V	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +75°C	*	*
Storage	-55°C to +85°C	*	*
CASE SIZE	2.2" X 3" X 0.6"	*	*

NOTES
[1] Accuracy is guaranteed at G = 1.6mA/V with no external trim adjustments when connected as shown in Figure 1.
[2] All accuracy is % of span where span is 16mA (±0.1% = ±0.016mA error).
[3] Span T.C. for gains higher than 1.6mA/V is R_G dependent – a low T.C. (±10ppm/°C) R_G is recommended for best performance.
*Specifications same as 2B22J.

Specifications subject to change without notice.

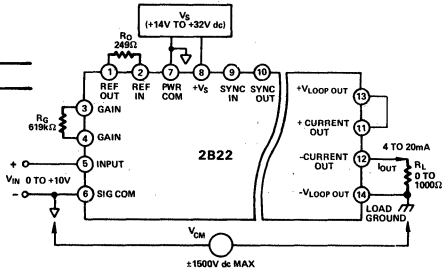
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



INTERCONNECTION DIAGRAM

Model 2B22 can be applied directly to achieve rated performance as shown in Figure 1 below. The input stage gain of 1.6mA/V, to convert a 0 to +10V signal into a 4 to 20mA output current, is obtained with the values shown. A single polarity power supply (+14V to +32V dc) should be connected to pin 8. To eliminate ground loops, the user should ensure that the signal return (common) lead does not carry the power supply current. Power common (pin 7) and signal common (pin 6) should be tied at the power supply common terminal. The voltage difference between pins 6 and 7 should not exceed 0.2V. An internal dc-dc converter provides isolated output loop power (pins 13 and 14), which is connected externally to the current output terminals (pins 11 and 12) and a load resistance. The standard 4 to 20mA current output signal is delivered into any external load between zero and 1000Ω.



NOTE: Resistors R_O and R_G are 1%, 50ppm/°C Metal Film Type. Values shown are for G = 1.6mA/V. For G = 16mA/V, use 10ppm/°C R_G and 50ppm/°C R_O.

Figure 1. Basic Connections

FUNCTIONAL DESCRIPTION

The high performance of model 2B22 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier, modulator section and the current output circuitry. The block diagram for model 2B22 is shown in Figure 2 below.

The 2B22 produces an isolated 4 to 20mA output current which is proportional to the voltage input and independent of the load resistance. The input amplifier operates single-ended and accepts a positive voltage within 0 to +10V range. Gain can be set from 1.6mA/V to 16mA/V by changing the gain resistor R_G to accommodate input ranges from 0 to +1V (G = 16mA/V) to 0 to +10V (G = 1.6mA/V). The transfer function is $I_{OUT} = (4mA + G \times V_{IN})$.

An internal, high stability reference has nominal output voltage of +2.5V (REF OUT) and is used to develop a 4mA output current for a 0 volts input. The terminals REF OUT (pin 1) and REF IN (pin 2) should be connected via the offset setting resistor R_O. For ratiometric operation, an external reference voltage can be connected to the REF IN terminal.

The 2B22 is designed to operate from a single positive power supply over a wide range of +14V to +32V dc. An internal dc-dc converter provides isolated +28V loop power which is independent of $+V_S$. The maximum resistance of the load R_L (resistance of the receivers plus the resistance of the connecting wire) is 1000Ω. Since the loop power is derived from the input side, the current capability of the power supply ($+V_S$) must be 100mA min to supply full output signal current.

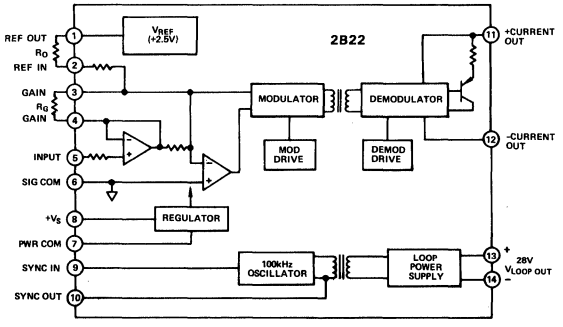


Figure 2. Block Diagram — 2B22

OPTIONAL TRIM ADJUSTMENTS

Model 2B22 is factory calibrated for a 0 to +10V input range (G = 1.6mA/V). As shipped, the 2B22 meets its listed specifications without use of any external trim potentiometers. Additional trim adjustment capability, to reduce span and offset errors to ±0.05% max, is easily provided as shown in Figure 3. The span and offset trim pots are adjusted while monitoring the voltage drop across a precision (or known) load resistor. The following trim procedure is recommended:

1. Connect model 2B22 as shown in Figure 3.
2. Apply V_{IN} = 0 volts and adjust R_O (Offset Adjust) for V_{OUT} = +2V ± 4mV.
3. Apply V_{IN} = +10.00V and adjust R_G (Span Adjust) for V_{OUT} = +10V ± 4mV.

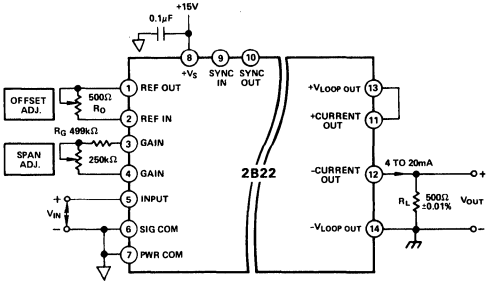


Figure 3. Optional Span and Offset Adjustment

GAIN AND OFFSET SETTING

The gain of the 2B22 is a scale factor setting that establishes the nominal conversion relationship to accommodate +1V to +10V full scale inputs (V_{IN}). The value of the gain setting resistor R_G is determined by: $R_G(k\Omega) = 6.314SF/(10.1 - SF)$ where SF is a scale factor equal to the value of V_{IN} F.S. Example: to convert a 0 to +1V input to the 4 to 20mA output, SF = 1 and R_G = 693Ω. Due to device tolerances, allowance should be made to vary R_G by ±5% using the potentiometer.

The value of the offset resistor R_O is independent from the gain setting and given by the relationship: $R_O(k\Omega) = 2.5 (V_{REF} - 2.4)$ where V_{REF} is the reference voltage applied. For example, the reference provided by the 2B22 is +2.5V and therefore R_O = 250Ω. The accuracy of the R_O calculation from from the above formula is ±5%. When an external reference operation is desired (i.e. for ratiometric operation), connect the reference voltage via R_O to pin 2 and leave pin 1 open.

EXTERNAL LOOP POWER OPERATION

For maximum versatility, the 2B22's output stage is designed to operate from the optional, isolated external loop power supply. This feature allows the user to interface systems wired for a two-wire operation. As shown in Figure 4, the same wiring is used for loop power and output. The load resistance is connected in series with an external dc power supply (+6V to +32V), and the current drawn from the supply is the 4 to 20mA output signal. The input stage of the 2B22 still requires $+V_S$ power, but the current drain from $+V_S$ is limited to 50mA. Use of an external loop power may require gain and offset trimming to obtain specified accuracy. The maximum series load resistance depends on the loop supply voltage as shown in Figure 4.

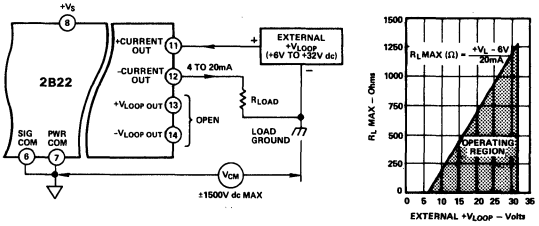


Figure 4. Optional External Loop Power Operation

SYNCHRONIZING MULTIPLE 2B22'S

In applications where multiple 2B22's are used in close proximity, radiated individual oscillator frequencies may cause "beat frequency" related output errors. These errors can be eliminated by synchronizing multiple units by connecting the SYNC OUT (pin 10) terminal to the SYNC IN (pin 9) terminal of the adjacent 2B22. The SYNC OUT terminal of this "slaved" unit can be used to drive another adjacent 2B22 (Figure 5). For best accuracy, each 2B22 should be retrimmed when synchronizing connections are used.

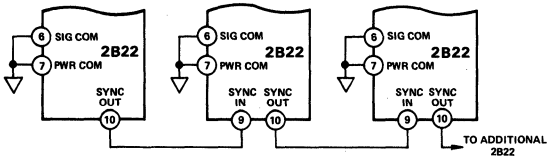


Figure 5. Multiple 2B22's Synchronization

OUTPUT PROTECTION

The current output terminals (pins 11 and 12) are protected from shorts up to +32V dc but in many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages in addition to back EMF induced from long output connections. The circuit shown in Figure 6 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

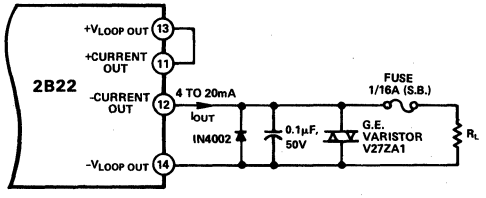


Figure 6. Output Protection Circuitry Connections

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Process Signal Isolator: In process control applications, model 2B22 can be applied to interface standard process signals (e.g. 1 to 5mA, 4 to 20mA, 10 to 50mA, 1 to 5V) and convert them to isolated 4 to 20mA output. A typical hook-up of model 2B22 is illustrated in Figure 7, showing input resistor R_C converting the current from a remote loop to a voltage input, and a span adjustment resistor R_G. A value of R_C should be selected to develop a minimum of +1V signal with full scale input current applied. For example, a 50Ω resistor converts the 4 to 20mA current input to a 200mV to 1V voltage input, which the 2B22 isolates and converts to a 4 to 20mA output. The reference input (pin 2) is not connected since the process signal provides a desired offset.

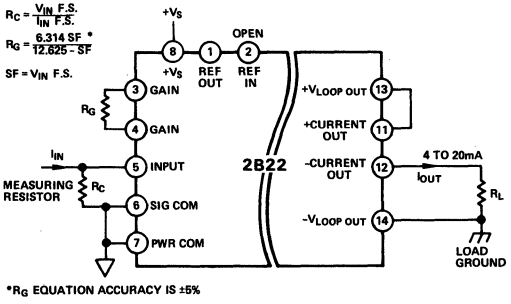


Figure 7. Process Signal Current Isolator

Isolated D/A Converter: Model 2B22 offers total ground isolation and protection from high voltage transients in interfacing D/A converters to standard 4 to 20mA current loops. This requirement is common in a microcomputer-based control system. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the D/A converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 8. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B22. First, a digital input code of all one's is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all zero's is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA less 1LSB (19.9961mA).

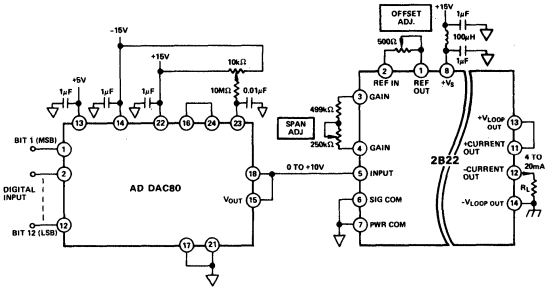


Figure 8. D/A Converter – Isolated 4 to 20mA Interface

Pressure Transmitter: In Figure 9, model 2B22 is used in a pressure transmitter application to provide complete input-output isolation and avoid signal errors due to ground loop currents. The process pressure is monitored with a strain gage type pressure transducer interfaced by the Analog Devices' model 2B30 transducer conditioner. The bridge excitation and system power is provided by the model 2B35 triple output power supply. The high level voltage output of the 2B30 is converted to the isolated 4 to 20mA current for transmission to a remote recorder or indicator.

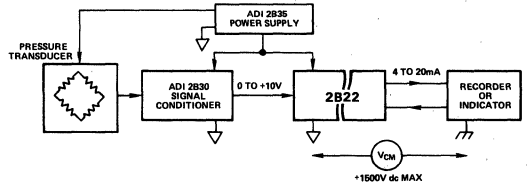


Figure 9. Isolated Pressure Transmitter

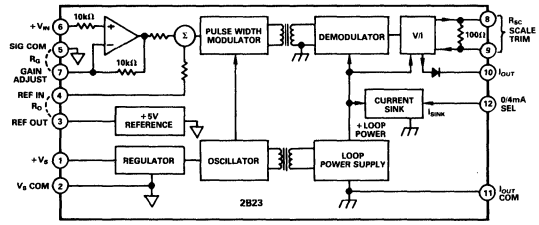
Programmable Output, Isolated Voltage-to-Current Converter

2B23

FEATURES
- **Wide Input Range, Resistor Programmable**
- **Pin Programmable Output: 4 to 20mA or 0 to 20mA**
- **High CMV Input/Output Isolation: ±1500V pk Continuous**
- **Low Nonlinearity: ±0.05% max (2B23K)**
- **Low Span Drift: ±0.005%/°C max (2B23K)**
- **Single Supply Operation: +14V to +28V**
- **Small Size: 1.8″ × 2.4″ × 0.6″**
- **Meets IEEE Std. 472: Transient Protection (SWC)**
- **Meets ISA Std. 50.1: Isolated Current Loop Transmitters**

APPLICATIONS
- **Industrial Instrumentation and Process Control**
  - **Ground Loop Elimination**
  - **Transient Voltage Protection**
- **Analog Transmitters and Controllers**
- **Remote Data Acquisition Systems**

2B23 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The model 2B23 is a high performance, low cost voltage to current converter featuring ±1500V pk input to output isolation for interfacing with standard process signals. The input stage of the 2B23 may be single resistor programmed to accept voltages within a 0 to +10V range (+0.1V to +10V full scale). The isolated output is pin programmable to provide current in the range of 4 to 20mA or 0 to 20mA and can be operated with 0 to 800Ω grounded or floating loads.

The 2B23 uses reliable transformer isolation techniques and is available in two accuracy selections offering guaranteed nonlinearity error (2B23K: ±0.05% max, 2B23J: ±0.1% max) and guaranteed low span drift (2B23K: ±0.005%/°C max, 2B23J: ±0.01%/°C max). The internally trimmed span and offset errors are ±0.1% for the 2B23K and ±0.25% for the 2B23J. Both span and offset may be adjusted using optional external potentiometers.

Featuring wide range, single supply operation (+14V to +28V dc), the 2B23 provides isolated loop power, thus eliminating the need for an external dc/dc converter.

APPLICATIONS

Model 2B23 has been designed to provide high accuracy, versatility and low cost in industrial and laboratory system applications requiring isolated current transmission. The 2B23 meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" and may serve as a transmission link between such system elements as computers, controllers, actuators, recorders and indicators.

In data acquisition and control systems, the 2B23 may act as an isolated interface between the D/A converter output of a microcomputer analog I/O and standard 4 to 20mA or 0 to 20mA analog loops. In process control systems, the 2B23 may be used as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-to-pneumatic transducers.

DESIGN FEATURES AND USER BENEFITS

High CMV Isolation: The 2B23 features high input to output galvanic isolation to eliminate ground loops and offer protection against damage from transients and fault voltages. Its isolation barrier will withstand continuous CMV of ±1500V pk and 1500V rms @ 60Hz for 60 seconds.

High Reliability: To assure high reliability in harsh industrial environments, reliable magnetic isolation is used. The 2B23 meets the IEEE Standard for Transient Voltage Protection (472–1974: Surge Withstand Capability) and offers reliable operation over −25°C to +85°C temperature range.

Versatility: The 2B23 can be easily tailored to the user's application, accommodating a wide range of input voltages, providing pin programmable, standard current outputs and offering wide range, single supply operation.

Small Size: To conserve board space, the 2B23 is packaged in a compact, 1.8″ × 2.4″ × 0.6″ module.

SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

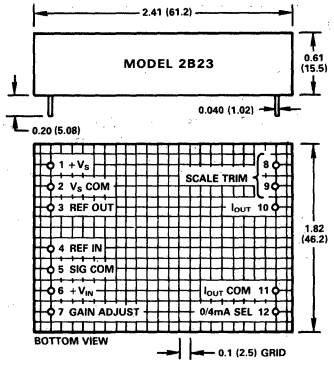
Model	2B23J	2B23K
INPUT SPECIFICATIONS		
Input Voltage Range		
Factory Calibrated	0 to +10V	*
Full Scale Input	+0.1V min to +10V max	*
Transfer Function (TF)		
Factory Calibrated	1.6mA/V	*
User Programmable	1.6mA/V to 200mA/V	*
Maximum Safe Input	±15V	*
Input Impedance	10MΩ	*
OUTPUT SPECIFICATIONS		
Current Output Range		
User Selectable	4 to 20mA, 0 to 20mA	*
Load Resistance Range		
Internal Loop Power	0 to 800Ω max	*
Maximum Output Current		
@ Input Overload	22mA typ	*
Output Noise		
100Hz Bandwidth	1.5μA pk-pk	*
NONLINEARITY	±0.1% max	±0.05% max (±0.02% typ)
ISOLATION		
CMV, Input to Output		
ac, 60Hz, 1 min	1500V rms	*
Continuous, ac or dc	±1500V pk	*
Transient Protection	IEEE Std. 472 (SWC)	*
CMR		
@ 60Hz, 1kΩ Source Imbalance	86dB	*
ACCURACY[1]		
Warm Up Time to Rated Performance	5 Minutes	*
Total Output Error @ +25°C[2,3]		
Offset (V_{IN} = 0V)	±0.25% max	±0.1% max
Span (V_{IN} = +10V)	±0.25% max	±0.1% max
vs. Temperature (0 to +70°C)		
Offset, 4-20mA Mode	±0.01%/°C max	±0.005%/°C max
0-20mA Mode	±0.01%/°C typ	±0.005%/°C typ
Span, Both Modes	±0.01%/°C max	±0.005%/°C max
DYNAMIC RESPONSE		
Settling Time to 0.1% of FS for 10V Step	5ms	*
Small Signal Bandwidth	400Hz	*
POWER SUPPLY		
Voltage, Rated Performance (+V_S)	+15V dc	*
Voltage, Operating	+14V min to +28V max	*
Supply Current (@ 20mA Output)	75mA	*
Supply Change Effect		
on Offset and Span	±0.0015%/V	*
ENVIRONMENTAL		
Temperature Range		
Rated Performance	0 to +70°C	*
Operating	−25°C to +85°C	*
Relative Humidity		
per MIL-STD 202, Method 103B	±0.2% Error	*
RFI Immunity		
27MHz @ 5W @ 3ft	±0.1% Error	*
CASE SIZE	1.8" × 2.4" × 0.6"	*

NOTES
[1]Accuracy is guaranteed @ TF = 1.6mA/V with no external trim adjustments when connected in the basic configuration.
[2]All accuracy is % of span where span is 16mA (i.e., ±0.1% = 0.016mA error).
[3]Span T.C. for transfer functions higher than 1.6mA/V is R_G dependent – low T.C. (±10ppm/°C)
R_G recommended for best performance.

*Specifications same as 2B23J.
Specifications subject to change without notice.

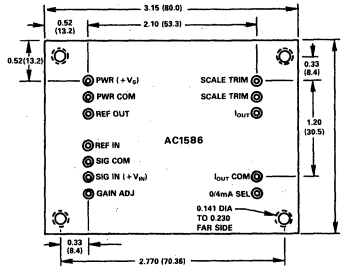
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1586

Dimensions shown in inches and (mm).



FUNCTIONAL DESCRIPTION

The high performance of model 2B23 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier stage, modulator, and current output circuitry. A block diagram of the 2B23 is shown in Figure 1.

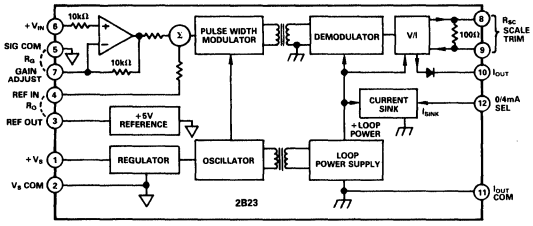


Figure 1. 2B23 Functional Block Diagram

The model 2B23 produces an isolated 4 to 20mA or 0 to 20mA output current which is proportional to the input voltage and independent of the output load resistance. The input amplifier accepts a positive voltage within the range of 0 to +10V. The transfer function of the input stage may be set from 1.6mA/V to 200mA/V (dependent upon the output current range desired) by changing the gain resistor R_G connected between pins 5 and 7.

An internal, high stability reference having a nominal output voltage of +5V (REF OUT) is used to develop a 4mA output current for a 0 volts input. REF OUT (Pin 3) and REF IN (Pin 4) should be connected via the offset scaling resistor R_O. An output current bypass section allows scaling of the nominal 4 to 20mA output current to a range of 0 to 20mA. This is accomplished by connecting the output range select pin (Pin 12) to the I_{OUT} pin (Pin 10) thereby providing a bypass for the 4mA. For 4-20mA operation, the bypass pin is connected to I_{OUT} COMMON (Pin 11).

The 2B23 is designed to operate from a single positive power supply ($+V_S$) over a range of +14V to +28V dc. The power supply section consists of an input voltage regulator, a dc/dc converter, plus associated rectifying and filtering circuitry. The dc/dc converter generates isolated loop power which is independent of V_S and capable of driving the maximum load resistance (resistance of receivers plus the resistance of connecting wire) of 800Ω. The current capability of the power supply ($+V_S$) must be 75mA minimum to supply full output signal current.

BASIC INTERCONNECTIONS

The 2B23 may be applied to achieve rated performance as shown in Figure 2. The transfer function of 1.6mA/V, for conversion of the 0 to +10V input signal into a 4 to 20mA output current, is obtained using the values shown (R_O = 10kΩ, R_{SC} = 301Ω, R_G open). For best performance, R_{SC} should be a metal film, ±0.1% tolerance, 25ppm/°C resistor and R_O should be ±1%, 100ppm/°C.

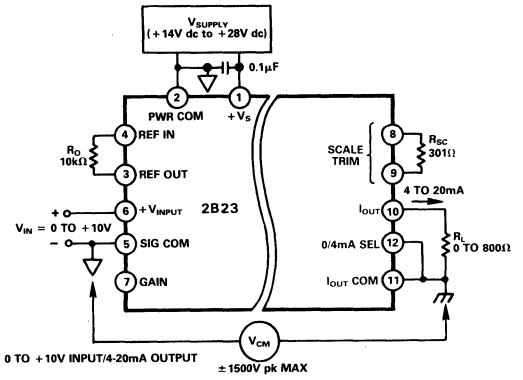


Figure 2. Basic Interconnections

A power supply ($+V_S$) is connected to Pin 1. To avoid ground loops, the user should ensure that the input signal return (SIG COM) does not carry the power supply return current. Power common (Pin 2) and signal common (Pin 5) should be tied at the power supply common terminal.

OPTIONAL TRIM ADJUSTMENTS

Model 2B23 is factory calibrated for a 0 to +10V input range and an output of 4 to 20mA, meeting its listed specifications without use of any external trim potentiometers. If desired, optional span and zero trim adjustments may be easily accomplished as described in the following sections.

Input Gain Adjustment: The input gain of the 2B23 is a scale factor setting that establishes the nominal conversion relationship to accommodate +1V to +10V full scale inputs (V_{IN}). In addition, full scale inputs as low as 100mV may be accommodated.

The value of the gain setting resistor R_G is determined by: R_G (kΩ) = 10kΩ/(G − 1) where G represents a ratio of 10V/V_{IN}(V) F.S. For example, to convert a 0 to +1V input to 4 to 20mA output, V_{IN} F.S. = +1V and G = 10V/1V = 10, therefore R_G = 10kΩ/9 = 1.1kΩ. Due to resistor tolerances, allowance should be made to vary R_G by using a series cermet type potentiometer (Figure 3). For best performance, R_G should be a metal film, 1% tolerance, 25ppm/°C resistor.

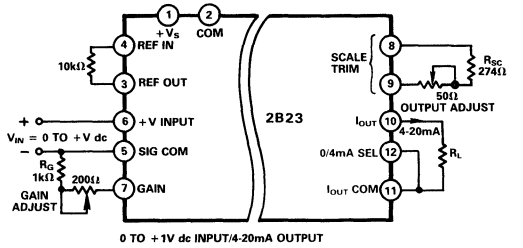
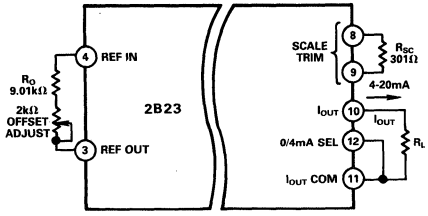


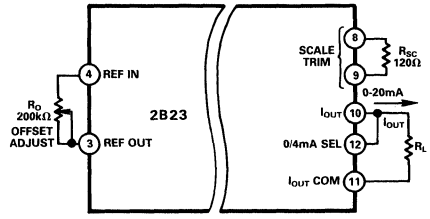
Figure 3. Input Gain Adjustment

Offset and Output Scaling Adjustments: After selecting the required input stage gain, the 2B23 must then be configured for either 4 to 20mA or 0 to 20mA output current range. Figures 4a and 4b illustrate the respective methods for each. The value of the offset resistor R_O is independent from the gain setting and may be adjusted by a series cermet pot.

For fine adjustment of the output current, R_{SC} value should be trimmed as shown in Figure 3.



4a. 4–20mA Output Connections



4b. 0–20mA Output Connections

Figure 4. 4–20mA/0–20mA Scaling Connections

USING MULTIPLE 2B23s

Unlike other transformer-based isolators, the 2B23 does not require any synchronizing circuits to eliminate beat frequency related output errors in multichannel applications. This is due to the use of pulse-width modulation technique in the 2B23. Radiated individual oscillator frequencies will have no effect upon performance, even in situations requiring multiple 2B23s to be located in close proximity to one another. For this reason, no provisions for external synchronization are necessary.

OUTPUT PROTECTION

The current output terminals (Pins 10 and 11) are protected for reverse voltage and shorts up to +32V dc but in many industrial applications it may be necessary to protect the 4 to 20mA from accidental shorts to ac line voltages. The circuit shown in Figure 5 may be employed for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

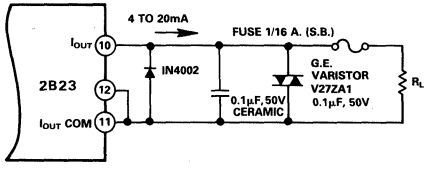


Figure 5. Output Protection Circuitry

APPLICATIONS

In Figure 6, model 2B23 is used in multiloop application of the data acquisition and control system to provide isolated current interface to a recorder, indicator and a valve positioner.

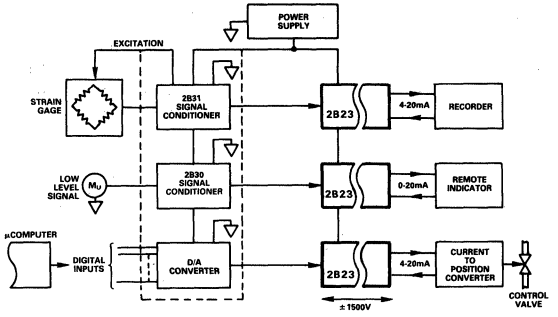


Figure 6. Multiloop Isolation

In applications requiring current to voltage conversion, the 2B23 may be used as shown in Figure 7. An external −10V reference is used to provide necessary input offset. This circuit will provide ±1500V isolation in converting 4-20mA into a 0 to +10V output. The output measurement device must have a high input impedance to avoid loading errors.

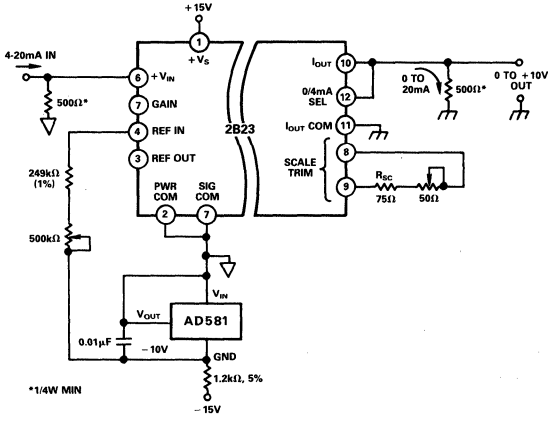


Figure 7. 4–20mA to 0 to +10V Isolated Converter

High Performance, Economy Strain Gage/RTD Conditioners

2B30/2B31

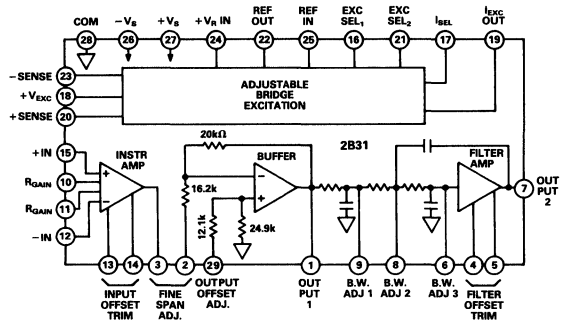
FEATURES

- Low Cost
- Complete Signal Conditioning Function
- Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max
- Wide Gain Range: 1 to 2000V/V
- Low Nonlinearity: 0.0025% max ("L")
- High CMR: 140dB min (60Hz, G = 1000V/V)
- Input Protected to 130V rms
- Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)
- Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100μA to 10mA)

APPLICATIONS

- Measurement and Control of:
  - Pressure, Temperature, Strain/Stress, Force, Torque
- Instrumentation: Indicators, Recorders, Controllers
- Data Acquisition Systems
- Microcomputer Analog I/O

2B31 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Models 2B30 and 2B31 are high performance, low cost, compact signal conditioning modules designed specifically for high accuracy interface to strain gage-type transducers and RTD's (resistance temperature detectors). The 2B31 consists of three basic sections: a high quality instrumentation amplifier; a three-pole low pass filter, and an adjustable transducer excitation. The 2B30 has the same amplifier and filter as the 2B31, but no excitation capability.

Available with low offset drift of 0.5μV/°C max (RTI, G = 1000V/V) and excellent linearity of 0.0025% max, both models feature guaranteed low noise performance (1μV p-p max) and outstanding 140dB common mode rejection (60Hz, CMV = ±10V, G = 1000V/V) enabling the 2B30/2B31 to maintain total amplifier errors below 0.1% over a 20°C temperature range. The low pass filter offers 60dB/decade roll-off from 2Hz to reduce normal-mode noise bandwidth and improve system signal-to-noise ratio. The 2B31's regulated transducer excitation stage features a low output drift (0.015%/°C max) and a capability of either constant voltage or constant current operation.

Gain, filter cutoff frequency, output offset level and bridge excitation (2B31) are all adjustable, making the 2B30/2B31 the industry's most versatile high-accuracy transducer-interface modules. Both models are offered in three accuracy selections, J/K/L, differing only in maximum nonlinearity and offset drift specifications.

APPLICATIONS

The 2B30/2B31 may be easily and directly interfaced to a wide variety of transducers for precise measurement and control of pressure, temperature, stress, force and torque. For applications in harsh industrial environments, such characteristics as high CMR, input protection, low noise, and excellent temperature stability make 2B30/2B31 ideally suited for use in indicators, recorders, and controllers.

The combination of low cost, small size and high performance of the 2B30/2B31 offers also exceptional quality and value to the data acquisition system designer, allowing him to assign a conditioner to each transducer channel. The advantages of this approach over low level multiplexers include significant improvements in system noise and resolution, and elimination of crosstalk and aliasing errors.

DESIGN FEATURES AND USER BENEFITS

High Noise Rejection: The true differential input circuitry with high CMR (140dB) eliminating common-mode noise pickup errors, input filtering minimizing RFI/EMI effects, output low pass filtering (f_c=2Hz) rejecting 50/60Hz line frequency pickup and series-mode noise.

Input and Output Protection: Input protected for shorts to power lines (130V rms), output protected for shorts to ground and either supply.

Ease of Use: Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

Programmable Transducer Excitation: User-programmable adjustable excitation source-constant voltage (4V to 15V @ 100mA) or constant current (100μA to 10mA) to optimize transducer performance.

Adjustable Low Pass Filter: The three-pole active filter (f_c=2Hz) reducing noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

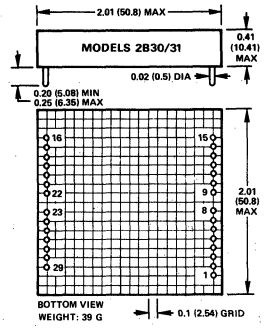
MODEL	2B30J 2B31J	2B30K 2B31K	2B30L 2B31L
GAIN[1]			
Gain Range	1 to 2000V/V	*	*
Gain Equation	$G = (1 + 94k\Omega/R_G)$ [$20k\Omega/(R_F + 16.2k\Omega)$]	*	*
Gain Equation Accuracy	±2%	*	*
Fine Gain (Span) Adjust. Range	±20%	*	*
Gain Temperature Coefficient	±25ppm/°C max (±10ppm/°C typ)	*	*
Gain Nonlinearity,	±0.01% max	±0.005% max	±0.0025% max
OFFSET VOLTAGES[1]			
Total Offset Voltage, Referred to Input			
Initial, @ +25°C	Adjustable to Zero (±0.5mV typ)	*	*
Warm-Up Drift, 10 Min., G = 1000	Within ±5µV (RTI) of Final Value	*	*
vs. Temperature			
G = 1V/V	±150µV/°C max	±75µV/°C max	±50µV/°C max
G = 1000V/V	±3µV/°C max	±1µV/°C max	±0.5µV/°C max
At Other Gains	±(3 ± 150/G)µV/°C max	±(1 ± 75/G)µV/°C max	±(0.5 ± 50/G)µV/°C max
vs. Supply, G = 1000V/V[5]	±25µV/V	*	*
vs. Time, G = 1000V/V	±5µV/month	*	*
Output Offset Adjust. Range	±10V	*	*
INPUT BIAS CURRENT			
Initial @ +25°C	+200nA max (100nA typ)	*	*
vs. Temperature (0 to +70°C)	-0.6nA/°C	*	*
INPUT DIFFERENCE CURRENT			
Initial @ +25°C	±5nA	*	*
vs. Temperature (0 to +70°C)	±40pA/°C	*	*
INPUT IMPEDANCE			
Differential	100MΩ‖47pF	*	*
Common Mode	100MΩ‖47pF	*	*
INPUT VOLTAGE RANGE			
Linear Differential Input	±10V	*	*
Maximum Differential or CMV Input			
Without Damage	130V rms	*	*
Common Mode Voltage	±10V	*	*
CMR, 1kΩ Source Imbalance			
G = 1V/V, dc to 60Hz[1]	90dB	*	*
G = 100V/V to 2000V/V, 60Hz[1]	140dB min	*	*
dc[2]	90dB min (112 typ.)	*	*
INPUT NOISE			
Voltage, G = 1000V/V			
0.01Hz to 2Hz	1µV p-p max	*	*
10Hz to 100Hz[2]	1µV p-p	*	*
Current, G = 1000			
0.01Hz to 2Hz	70pA p-p	*	*
10Hz to 100Hz[2]	30pA rms	*	*
RATED OUTPUT[1]			
Voltage, 2kΩ Load[3]	±10V min	*	*
Current	±5mA min	*	*
Impedance, dc to 2Hz, G = 100V/V	0.1Ω	*	*
Load Capacitance	0.01µF max	*	*
DYNAMIC RESPONSE (Unfiltered)[2]			
Small Signal Bandwidth			
-3dB Gain Accuracy, G = 100V/V	30kHz	*	*
G = 1000V/V	5kHz	*	*
Slew Rate	1V/µs	*	*
Full Power	15kHz	*	*
Settling Time, G = 100, ±10V Output			
Step to ±0.1%	30µs	*	*
LOW PASS FILTER (Bessel)			
Number of Poles	3	*	*
Gain (Pass Band)	+1	*	*
Cutoff Frequency (-3dB Point)	2Hz	*	*
Roll-Off	60dB/decade	*	*
Offset (at 25°C)	±5mV	*	*
Settling Time, G = 100V/V, ±10V			
Output Step to ±0.1%	600ms	*	*
BRIDGE EXCITATION (See Table 1)			
POWER SUPPLY[4]			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(12 to 18)V dc	*	*
Current, Quiescent[6]	±15mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +125°C	*	*
CASE SIZE	2" x 2" x 0.4" (51 x 51 x 10.2mm)	*	*

NOTES

*Specifications same as 2B30J/2B31J.
[1] Specifications referred to output at pin 7 with 3.75k, 1%, 25ppm/°C fine span resistor installed and internally set 2Hz filter cutoff frequency.
[2] Specifications referred to the unfiltered output at pin 1.
[3] Protected for shorts to ground and/or either supply voltage.
[4] Recommended power supply ADI model 902-2 or model 2B35
[5] Tracking power supplies.
[6] Does not include bridge excitation and load currents.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

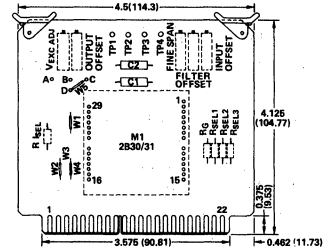


PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT 1 (UNFILTERED)	16	EXC SEL 1
2	FINE GAIN (SPAN) ADJ.	17	I SEL
3	FINE GAIN (SPAN) ADJ.	18	$V_{EXC\ OUT}$
4	FILTER OFFSET TRIM	19	$I_{EXC\ OUT}$
5	FILTER OFFSET TRIM	20	SENSE HIGH (+)
6	BANDWIDTH ADJ. 3	21	EXC SEL 2
7	OUTPUT 2 (FILTERED)	22	REF OUT
8	BANDWIDTH ADJ. 2	23	SENSE LOW (-)
9	BANDWIDTH ADJ. 1	24	REGULATOR $+V_{R\ IN}$
10	R_{GAIN}	25	REF IN
11	R_{GAIN}	26	$-V_S$
12	-INPUT	27	$+V_S$
13	INPUT OFFSET TRIM	28	COMMON
14	INPUT OFFSET TRIM	29	OUTPUT OFFSET TRIM
15	+ INPUT		

Note: Pins 16 thru 25 are not connected in Model 2B30

AC1211/AC1213 MOUNTING CARDS



AC1211/AC1213 CONNECTOR DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
A	REGULATOR $+V_{R\ IN}$	1	EXC SEL 1
B	SENSE LOW (-)	2	I SEL
C	REF OUT	3	$V_{EXC\ OUT}$
D	REF IN	4	$I_{EXC\ OUT}$
E		5	SENSE HIGH (+)
F		6	EXC SEL 2
H		7	OUTPUT OFFSET TRIM
J		8	
K	$-V_S$	9	$-V_S$
L	$+V_S$	10	$+V_S$
M		11	
N	COMMON	12	COMMON
P		13	
R	FINE GAIN ADJ.	14	
S	FINE GAIN ADJ.	15	
T	FILTER OFFSET TRIM	16	
U	FILTER OFFSET TRIM	17	R_{GAIN}
V	OUTPUT 2 (FILTERED)	18	R_{GAIN}
W	- INPUT	19	OUTPUT 1 (UNFILTERED)
X	INPUT OFFSET TRIM	20	BANDWIDTH ADJ. 1
Y	INPUT OFFSET TRIM	21	BANDWIDTH ADJ. 3
Z	+ INPUT	22	BANDWIDTH ADJ. 2

The AC1211/AC1213 mounting card is available for the 2B30/2B31. The AC1211/AC1213 is an edge connector card with pin receptacles for plugging in the 2B30/2B31. In addition, it has provisions for installing the gain resistors and the bridge excitation, offset adjustment and filter cutoff programming components. The AC1211/AC1213 is provided with a Cinch 251-22-30-160 (or equivalent) edge connector. The AC1213 includes the adjustment pots; no pots are provided with the AC1211.

FUNCTIONAL DESCRIPTION

Models 2B30 and 2B31 accept inputs from a variety of full bridge strain gage-type transducers or RTD sensors and convert the inputs to conditioned high level analog outputs. The primary transducers providing direct inputs may be 60Ω to 1000Ω strain gage bridges, four-wire RTD's or two- or three-wire RTD's in the bridge configuration.

The 2B30 and 2B31 employ a multi-stage design, shown in Figure 1, to provide excellent performance and maximum versatility. The input stage is a high input impedance (10^8 Ω), low offset and drift, low noise differential instrumentation amplifier. The design is optimized to accurately amplify low level (mV) transducer signals riding on high common mode voltages (±10V), with wide (1-2000V/V), single resistor (R_G), programmable gain to accommodate 0.5mV/V to 36mV/V transducer spans and 5Ω to 2000Ω RTD spans. The input stage contains protection circuitry for accidental shorts to power line voltage (130V rms) and RFI filtering circuitry.

The inverting buffer amplifier stage provides a convenient means of fine gain trim (0.8 to 1.2) by using a 10kΩ potentiometer (R_F); the buffer also allows the output to be offset by up to ±10V by applying a voltage to the noninverting input (pin 29). For dynamic, high bandwidth measurements—the buffer output (pin 1) should be used.

The three-pole active filter uses a unity-gain configuration and provides low-pass Bessel-type characteristics-minimum overshoot response to step inputs and a fast rise time. The cutoff frequency (-3dB) is factory set at 2Hz, but may be increased up to 5kHz by addition of three external resistors (R_{SEL_1} - R_{SEL_3}).

INTERCONNECTION DIAGRAM AND SHIELDING TECHNIQUES

Figure 1 illustrates the 2B31 wiring configuration when used in a typical bridge transducer signal conditioning application. A recommended shielding and grounding technique for preserving the excellent performance characteristics of the 2B30/2B31 is shown.

Because models 2B30/2B31 are direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and conditioner common (pin 28). The sensitive input and gain setting terminals should be shielded from noise sources for best performance, especially at high gains. To avoid ground loops, signal return or cable shield should never be grounded at more than one point.

The power supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS

Models 2B30/2B31 have been conservatively specified using min-max values as well as typicals to allow the designer to develop accurate error budgets for predictable performance. The error calculations for a typical transducer application, shown in Figure 1 (350Ω bridge, 1mV/V F.S., 10V excitation), are illustrated below.

Assumptions: 2B31L is used, G = 1000, ΔT = ±10°C, source imbalance is 100Ω, common mode noise is 0.25V (60Hz) on the ground return.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources and their effect on system accuracy (worst case) as a % of Full Scale (10V) are listed:

Error Source	Effect on Absolute Accuracy % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.0025	±0.0025
Gain Drift	±0.025	
Voltage Offset Drift	±0.05	
Offset Current Drift	±0.004	
CMR	±0.00025	±0.00025
Noise (0.01 to 2Hz)	±0.01	±0.01
Total Amplifier Error	±0.09175 max	±0.01275 max
Excitation Drift	±0.15 (±0.03 typ)	
Total Output Error (Worst Case)	±0.24175 max (±0.1 typ)	±0.0127 max

The total worst case effect on absolute accuracy over ±10°C is less than ±0.25% and the 2B31 is capable of 1/2 LSB resolution in a 12 bit, low input level system. Since the 2B31 is conservatively specified, a typical overall accuracy error would be lower than ±0.1% of F.S.

In a computer or microprocessor based system, automatic recalibration can nullify gain and offset drifts leaving noise, nonlinearity and CMR as the only error sources. A transducer excitation drift error is frequently eliminated by a ratiometric operation with the system's A/D converter.

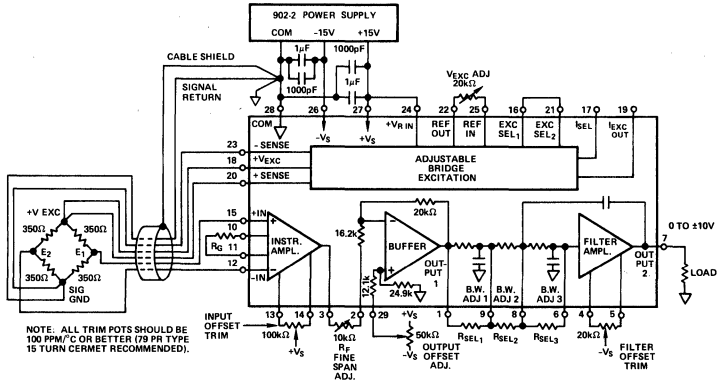


Figure 1. Typical Bridge Transducer Application Using 2B31

BRIDGE EXCITATION (2B31)

The bridge excitation stage of the model 2B31 is an adjustable output, short circuit protected, regulated supply with internally provided reference voltage (+7.15V). The remote sensing inputs are used in the voltage output mode to compensate for the voltage drop variations in long leads to the transducer. The regulator circuitry input (pin 24) may be connected to $+V_S$ or some other positive dc voltage (pin 28 referenced) within specified voltage level and load current range. User-programmable constant voltage or constant current excitation mode may be used. Specifications are listed below in Table I.

MODEL	2B31J	2B31K	2B31L
Constant Voltage Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	*	*
Output Voltage Range	+4V to +15V	*	*
Regulator Input/Output Voltage Differential	3V to 24V	*	*
Output Current[1]	0 to 100mA max	*	*
Regulation, Output Voltage vs. Supply	0.05%/V	*	*
Load Regulation, I_L = 1mA to I_L = 50mA	0.1%	*	
Output Voltage vs. Temperature (0 to +70°C)	0.015%/°C max 0.003%/°C typ	*	*
Output Noise	1mV rms	*	*
Reference Voltage (Internal)	7.15V ±3%	*	*
Constant Current Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	*	*
Output Current Range	100μA to 10mA	*	*
Compliance Voltage	0 to 10V	*	*
Load Regulation	0.1%	*	*
Temperature Coefficient (0 to +70°C)	0.003%/°C	*	*
Output Noise	1μA rms	*	*

[1] Output Current derated to 33mA max for 24V regulator input/output voltage differential.

Table I. Bridge Excitation Specifications

OPERATING INSTRUCTIONS

Gain Setting: The differential gain, G, is determined according to the equation:

$$G = (1 + 94k\Omega/R_G)\ [20k\Omega/(R_F + 16.2k\Omega)]$$

where R_G is the input stage resistor shown in Figure 1 and R_F is the variable 10kΩ resistor in the output stage. For best performance, the input stage gain should be made as large as possible, using a low temperature coefficient (10ppm/°C) R_G, and the output stage gain can then be used to make a ±20% linear gain adjustment by varying R_F.

Input Offset Adjustment: To null input offset voltage, an optional 100kΩ potentiometer connected between pins 13 and 14 (Figure 1) can be used. With gain set at the desired value, connect both inputs (pins 12 and 15) to the system common (pin 28), and adjust the 100kΩ potentiometer for zero volts at pin 3. The purpose of this adjustment is to null the internal amplifier offset and it is not intended to compensate for the transducer bridge unbalance.

Output Offset Adjustment: The output of the 2B30/2B31 can be intentionally offset from zero over the ±10V range by applying a voltage to pin 29, e.g., by using an external potentiometer or a fixed resistor. Pin 29 is normally grounded if output offsetting is not desired. The optional filter amplifier offset null capability is also provided as illustrated in Figure 1.

Filter Cutoff Frequency Programming: The low pass filter cutoff frequency may be increased from the internally set 2Hz by the addition of three external resistors connected as shown in Figure 1. The values of resistors required for a desired cutoff frequency, f_c, above 5Hz are obtained by the equation below:

$$R_{SEL_1} = 11.6 \times 10^6/(2.67f_c - 4.34);$$

$$R_{SEL_2} = 27.6 \times 10^6/(4.12f_c - 7)$$

$$R_{SEL_3} = 1.05 \times 10^6/(0.806f_c - 1.3)$$

where R_{SEL} is in ohms and f_c in Hz. Table II gives the nearest 1% R_{SEL} for several common filter cutoff (-3dB) frequencies.

f_c (Hz)	R_{SEL1} (kΩ) (Pin 1 to 9)	R_{SEL2} (kΩ) (Pin 9 to 8)	R_{SEL3} (kΩ) (Pin 8 to 6)
2	Open	Open	Open
5	1270.000	2050.00	383.000
10	523.000	806.00	154.000
50	90.000	137.00	26.700
100	44.200	68.10	13.300
500	8.660	13.30	2.610
1000	4.320	6.65	1.300
5000	0.866	1.33	0.261

Table II. Filter Cutoff Frequency vs. R_{SEL}

Voltage Excitation Programming: Pin connections for a constant voltage output operation are shown in Figure 2. The bridge excitation voltage, V_{EXC}, is adjusted between +4V to +15V by the 20kΩ (50ppm/°C) R_{VSEL} potentiometer. For ratiometric operation, the bridge excitation can be adjusted by applying an external positive reference to pin 25 of the 2B31. The output voltage is given by: $V_{EXC\ OUT} = 3.265V_{REF\ IN}$. The remote sensing leads should be externally connected to the excitation leads at the transducer or jumpered as shown in Figure 2 if sensing is not required.

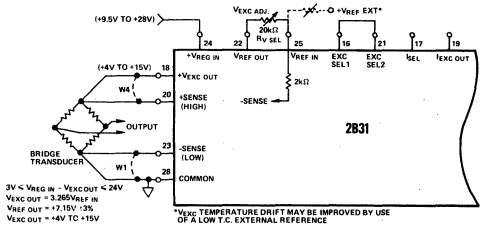


Figure 2. Constant Voltage Excitation Connections

Current Excitation Programming: The constant current excitation output can be adjusted between 100μA to 10mA by two methods with the 2B31. Figure 3 shows circuit configuration for a current output with the maximum voltage developed across the sensor (compliance voltage) constrained to +5V. The value of programming resistor R_{ISEL} may be calculated from the relationship: $R_{ISEL} = (V_{REG\ IN} - V_{REF\ IN})/I_{EXC\ OUT}$. This application requires a stable power supply because any variation of the input supply voltage will result in a change in the excitation current output.

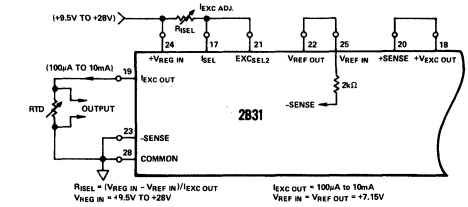


Figure 3. Constant Current Excitation Connections (V_{COMPL} = 0 to +5V)

A compliance voltage range of 0 to +10V can be obtained by connecting the 2B31 as shown in Figure 4. The 2kΩ potentiometer R_{ISEL} is adjusted for desired constant current excitation output.

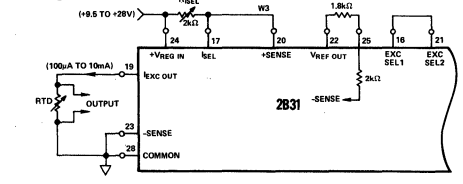


Figure 4. Constant Current Excitation Connections (V_{COMPL} = 0 to +10V)

APPLICATIONS

Strain Measurement: The 2B30 is shown in Figure 5 in a strain measurement system. A single active gage (120Ω, GF = 2) is used in a bridge configuration to detect small changes in gage resistance caused by strain. The temperature compensation is provided by an equivalent dummy gage and two high precision 120Ω resistors complete the bridge. The 2B35 adjustable power supply is set to a low +3V excitation voltage to avoid the self-heating error effects of the gage and bridge elements. System calibration produces a 1V output for an input of 1000 microstrains. The filter cutoff frequency is set at 100Hz.

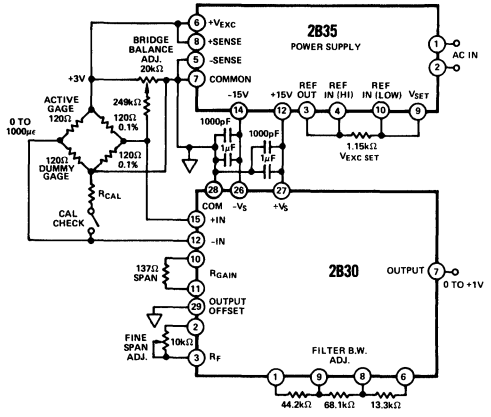


Figure 5. Interfacing Half-Bridge Strain Gage Circuit

Pressure Transducer Interface: A strain gage type pressure transducer (BLH Electronics, DHF Series) is interfaced by the 2B31 in Figure 6. The 2B31 supplies regulated excitation (+10V) to the transducer and operates at a gain of 333.3 to achieve 0-10V output for 0-10,000 p.s.i. at the pressure transducer. Bridge Balance potentiometer is used to cancel out any offset which may be present and the Fine Span potentiometer adjustment accurately sets the full scale output. Depressing the calibration check pushbutton switch shunts a system calibration resistor (R_{CAL}) across the transducer bridge to give an instant check on system calibration.

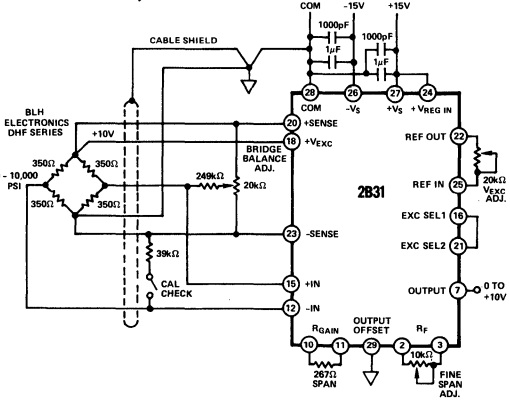


Figure 6. Pressure Transducer Interface Application

Platinum RTD Temperature Measurement: In Figure 7 model 2B31 provides complete convenient signal conditioning in a wide range (-100°C to +600°C) RTD temperature measurement system. YSI - Sostman four-wire, 100Ω platinum RTD (PT139AX) is used. The four wire sensor configuration, combined with a constant current excitation and a high input impedance offered by the 2B31, eliminates measurement errors resulting from voltage drops in the lead wires. Offsetting may be provided via the 2B31's offset terminal. The gain is set by the gain resistor for a +10V output at +600°C. This application requires a stable power supply.

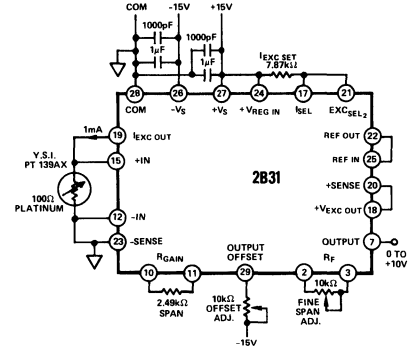


Figure 7. Platinum RTD Temperature Measurement

Interfacing Three-Wire Sensors: A bridge configuration is particularly useful to provide offset in interfacing to a platinum RTD and to detect small, fractional sensor resistance changes. Lead compensation is employed, as shown in Figure 8, to maintain high measurement accuracy when the lead lengths are so long that thermal gradients along the RTD leg may cause changes in line resistance. The two completion resistors (R1, R2) in the bridge should have a good ratio tracking (±5ppm/°C) to eliminate bridge error due to drift. The single resistor (R3) in series with the platinum sensor must, however, be of very high absolute stability. The adjustable excitation in the 2B31 controls the power dissipated by the RTD itself to avoid self-heating errors.

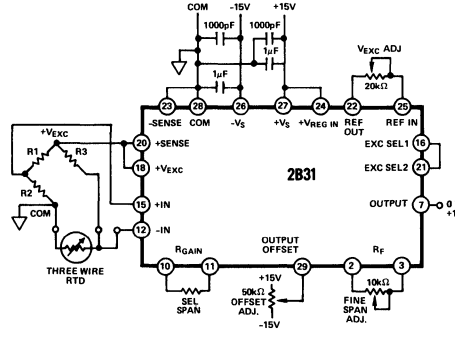


Figure 8. Three-Wire RTD Interface

Linearizing Transducer Output: To maximize overall system linearity and accuracy, some strain gage-type and RTD transducer analog outputs may require linearization. A simple circuit may be used with the 2B31 to correct for the curvature in the input signal as shown in Figure 9. The addition of feedback in the excitation stage will allow for the correction of

nonlinearity by the addition of two components. The sense of the feedback is determined by whether the nonlinearity is concave upward or concave downward (jumper A to pin 21, or to pin 25). The magnitude of the correction is determined by the resistor, R_{SEL}, and the *linearity adjust* pot provides a fine trim.

If an RTD is to be used, the adjustment can be made efficiently, without actually changing the temperature, by simulating the RTD with a precision resistance decade. The offset is adjusted at the low end of the resistance range, the fine span is adjusted at about one third of the range, and the linearity is adjusted at a resistance corresponding to full-scale temperature. One or two iterations of the adjustments will probably be found necessary because of the interaction of linearity error and scale-factor error. This circuit's applications are not restricted to RTD's; it will work in most cases where bridges are used – e.g., load cells and pressure transducers.

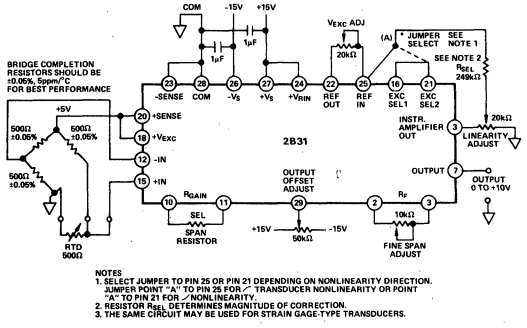


Figure 9. Transducer Nonlinearity Correction

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Models 2B30/2B31 are available in three drift selections: ±0.5, ±1 and ±3µV/°C (max, RTI, G = 1000V/V). Total input drift is composed of two sources (input and output stage drifts) and is gain dependent. Figure 10 is a graph of the worst case total voltage offset drift vs. gain for all versions.

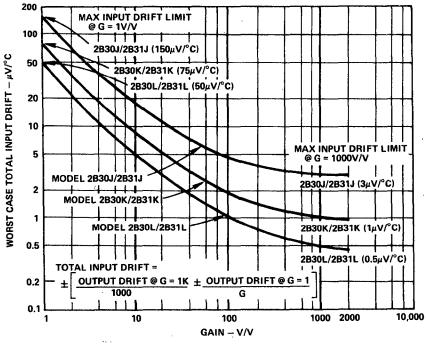


Figure 10. Total Input Offset Drift (Worst Case) vs. Gain

Gain Nonlinearity and Noise: Nonlinearity is specified as a percent of full scale (10V), e.g. 0.25mV RTO for 0.0025%. Three maximum nonlinearity selections offered are: ±0.0025%, ±0.005% and ±0.01% (G = 1 to 2000V/V). Models 2B30/2B31 offer also an excellent voltage noise performance by guaranteeing maximum RTI noise of 1µV p-p (G = 1000V/V, $R_S \leq 5k\Omega$) with noise bandwidth reduced to 2Hz by the LPF.

Common Mode Rejection: CMR is rated at ±10V CMV and 1kΩ source imbalance. The CMR improves with increasing gain. As a function of frequency, the CMR performance is enhanced by the incorporation of low pass filtering, adding to the 90dB minimum rejection ratio of the instrumentation amplifier. The effective CMR at 60Hz at the output of the filter (f_c = 2Hz) is 140dB min. Figure 11 illustrates a typical CMR vs. Frequency and Gain.

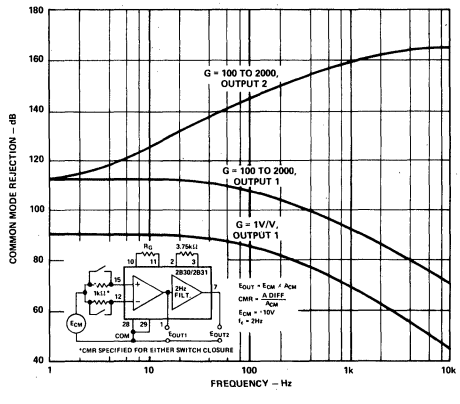


Figure 11. Common-Mode Rejection vs. Frequency and Gain

Low Pass Filter: The three pole Bessel-type active filter attenuates unwanted high-frequency components of the input signal above its cutoff frequency (-3dB) with 60dB/decade rolloff. With a 2Hz filter, attenuation of 70dB at 60Hz is obtained, settling time is 600ms to 0.1% of final value with less than 1% overshoot response to step inputs. Figure 12 shows the filter response.

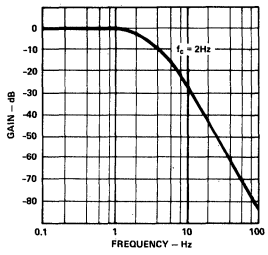


Figure 12. Filter Amplitude Response vs. Frequency

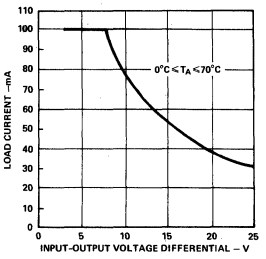


Figure 13. Maximum Load Current vs. Regulator Input-Output Voltage Differential

Bridge Excitation (2B31): The adjustable bridge excitation is specified to operate over a wide regulator input voltage range (+9.5V to +28V). However, the maximum load current is a function of the regulator circuit input-output differential voltage, as shown in Figure 13. Voltage output is short circuit protected and its temperature coefficient is ±0.015% V_{OUT}/°C max (±0.003%/°C typ). Output temperature stability is directly dependent on a temperature coefficient of a reference and for higher stability requirements, a precision external reference may be used.

ANALOG DEVICES

Isolated, Thermocouple Signal Conditioner

2B50

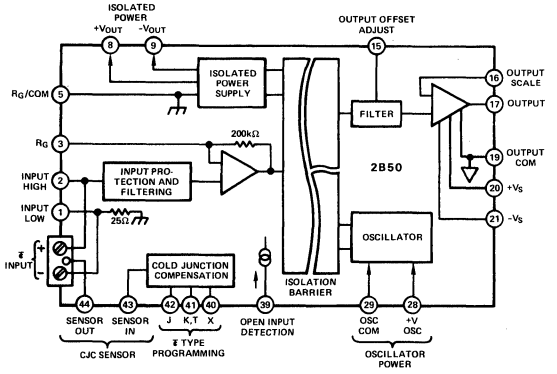
FEATURES

Accepts J, K, T, E, R, S or B Thermocouple Types
Internally Provided Cold Junction Compensation
High CMV Isolation: ±1500V pk
High CMR: 160dB min @ 60Hz
Low Drift: ±1μV/°C max (2B50B)
High Linearity: ±0.01% max (2B50B)
Input Protection and Filtering
Screw Terminal Input Connections

APPLICATIONS

Precision Thermocouple Signal Conditioning for:
Process Control and Monitoring
Industrial Automation
Energy Management
Data Acquisition Systems

2B50 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The model 2B50 is a high performance thermocouple signal conditioner providing input protection, isolation and common mode rejection, amplification, filtering and integral cold junction compensation in a single, compact package.

The 2B50 has been designed to condition low level analog signals, such as those produced by thermocouples, in the presence of high common mode voltages. Featuring direct thermocouple connection via screw terminals and internally provided reference junction temperature sensor, the 2B50 may be jumper programmed to provide cold junction compensation for thermocouple types J, K, T, and B, or resistor programmed for types E, R, and S.

The high performance of the 2B50 is accomplished by the use of reliable transformer isolation techniques. This assures complete input to output galvanic isolation (±1500V pk) and excellent common mode rejection (160dB @ 60Hz).

Other key features include: input protection (220V rms), filtering (NMR of 70dB @ 60Hz), low drift amplification (±1μV/°C max - 2B50B), and high linearity (±0.01% max - 2B50B).

APPLICATIONS

The 2B50 has been designed to provide thermocouple signal conditioning in data acquisition systems, computer interface systems, and temperature measurement and control instrumentation.

In thermocouple temperature measurement applications, outstanding features such as low drift, high noise rejection, and 1500V isolation make the 2B50 an ideal choice for systems used in harsh industrial environments.

DESIGN FEATURES AND USER BENEFITS

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, the 2B50 has been conservatively designed to meet the IEEE Standard for transient voltage protection (472-1974: SWC) and provide 220V rms differential input protection.

High Noise Rejection: The 2B50 features internal filtering circuitry for elimination of errors caused by RFI/EMI, series mode noise, and 50Hz/60Hz pickup.

Ease of Use: Internal compensation enables the 2B50 to be used with seven different thermocouple types. Unique circuitry offers a choice of internal or remote reference junction temperature sensing. Thermocouple connections may be made either by screw terminals or, in applications requiring PC Board connections, by terminal pins.

Small Package: 1.5″ X 2.5″ X 0.6″ size conserves board space.

13

SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

MODEL	2B50A	2B50B
INPUT SPECIFICATIONS		
Thermocouple Types		
Jumper Configurable Compensation	J, K, T, or B	*
Resistor Configurable Compensation	R, S, or E	*
Input Span Range	±5mV to ±100mV	*
Gain Range	50V/V to 1000V/V	*
Gain Equation	$1 + (200k\Omega/R_G)$	*
Gain Error	±0.25%	*
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max
Gain Nonlinearity[1]	±0.025% max	±0.01% max
Offset Voltage		
Input Offset (Adjustable to Zero)	±50μV	*
vs. Temperature	±2.5μV/°C max	±1μV/°C max
vs. Time	±1.5μV/month	*
Output Offset (Adjustable to Zero)	±10mV	*
vs. Temperature	±30μV/°C	*
Total Offset Drift	$\pm\left(2.5 + \frac{30}{G}\right)$ μV/°C	$\pm\left(1 + \frac{30}{G}\right)$ μV/°C
Input Noise Voltage		
0.01Hz to 100Hz, R_S = 1kΩ	1μV p-p	*
Maximum Safe Differential Input Voltage	220V rms, Continuous	*
CMV, Input to Output		
Continuous, ac or dc	±1500V pk max	*
Common Mode Rejection		
@ 60Hz, 1kΩ Source Unbalance	160dB min	*
Normal Mode Rejection @ 60Hz	70dB min	*
Bandwidth	dc to 2.5Hz (–3dB)	*
Input Impedance	100MΩ	*
Input Bias Current[2]	±5nA	*
Open Input Detection	Downscale	*
Response Time[3], G = 250	1.4sec	*
Cold Junction Compensation		
Initial Accuracy[4]	±0.5°C	*
vs. Temperature[5] (+5°C to +45°C)	±0.01°C/°C	*
OUTPUT SPECIFICATIONS		
Output Voltage Range[6]	±5V @ ±2mA	*
Output Resistance	0.1Ω	*
Output Protection	Continuous Short to Ground	*
POWER SUPPLY		
Voltage		
Output ±V_S (Rated Performance)	±15V dc ±10% @ ±0.5mA	*
(Operating)	±12V to ±18V dc max	*
Oscillator +V_{OSC} (Rated Performance)	+13V to +18V @ 15mA	*
ENVIRONMENTAL		
Temperature Range, Rated Performance	0 to +70°C	*
Operating	–25°C to +85°C	*
Storage Temperature Range	–55°C to +85°C	*
RFI Effect (5W @ 470MHz @ 3ft)		
Error	±0.5% of Span	*
PHYSICAL		
Case Size	1.5" X 2.5" X 0.6"	*

NOTES

*Specifications same as 2B50A.

[1] Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line; e.g., nonlinearity at an output span of 10V pk-pk (±5V) is ±0.01% or ±1mV.

[2] Does not include open circuit detection current of 20nA (optional by jumper connection).

[3] Open input response time is dependent upon gain.

[4] When used with internally provided CJC sensor.

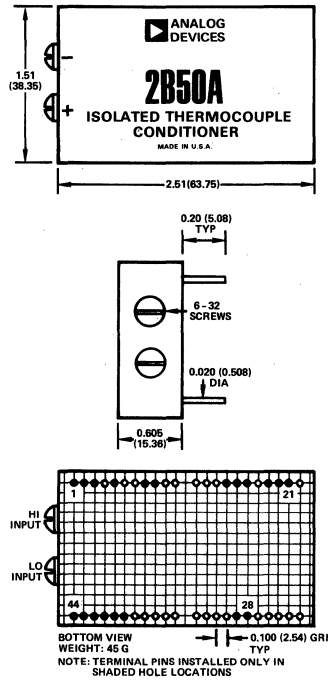
[5] Compensation error contributed by ambient temperature changes at the module.

[6] Output swing of ±10V may be obtained through output scaling (Figure 5).

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	INPUT LO	23	
2	INPUT HI	24	
3	R_G	25	
4		26	
5	R_G/COM	27	
6		28	+V OSC
7		29	OSC COM
8	+V ISO OUT	30	
9	-V ISO OUT	31	
10		32	
11		33	
12		34	
13		35	
14		36	
15	OUTPUT OFFSET ADJUST	37	
		38	
16	OUTPUT SCALE	39	OPEN INPUT DET.
17	OUTPUT	40	X
18		41	K, T ‡ TYPE PROGRAMMING
19	OUTPUT COM	42	J
20	+V_S	43	CJC SENSOR IN
21	-V_S	44	CJC SENSOR OUT
22			

MATING SOCKET: AC1218

FUNCTIONAL DESCRIPTION

The internal structure of the 2B50 is shown in Figure 1. An input filtering and protection network precedes a low drift, high performance amplifier whose gain is set by a user supplied resistor (R_G) for gains of 50 to 1000V/V. Isolated power is brought out to permit convenient adjustment of the input offset voltage, if desired.

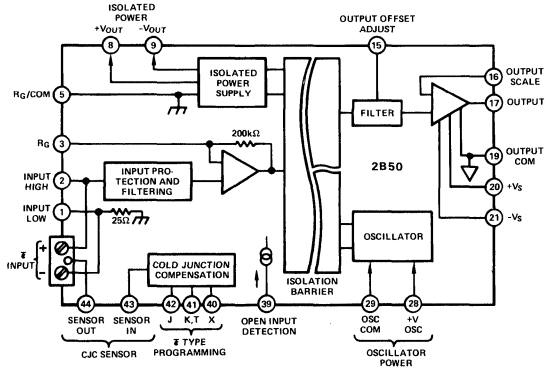


Figure 1. 2B50 Functional Block Diagram

Internal circuitry provides reference junction compensation. An integral reference junction sensor is provided for direct thermocouple connections, or an external reference sensor (2N2222 transistor) may be used in applications having remote thermocouple termination. Compensating networks for thermocouple types J, K, and T are built into the 2B50. A fourth compensation (X) may be programmed with a single resistor for any other thermocouple type. The 2B50 can be programmed for uncompensated output when used with inputs other than thermocouples.

Transformer coupling is used to achieve stable, reliable input to output galvanic isolation, as well as elimination of ground loop error effects.

Normally, the full scale output of the 2B50 is ±5V. However, with the addition of an external resistive divider, the output buffer amplifier may be scaled for a gain of up to 2, providing a full scale output swing of ±10V.

OPERATING INSTRUCTIONS

The connections shown in Figure 2 are common to most applications using the 2B50, and, in many cases, will be all that is required.

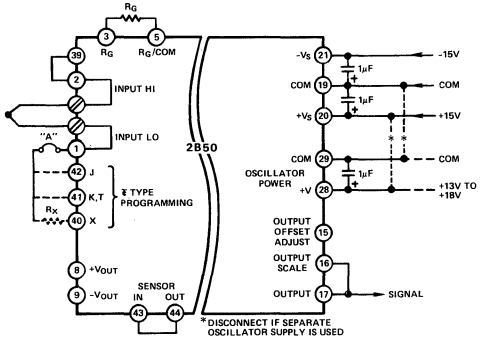


Figure 2. Basic 2B50 Application

Two sets of parallel thermocouple input connections are provided. The thermocouple input may be connected by screw terminals (input +, Input -) or to terminal Pins 1 (-) and 2 (+) in cases where thermocouples are to be remotely terminated. The following sections describe a basic thermocouple application, as well as detail some optional connections to enhance performance in more demanding applications. Jumper A (Figure 2) is used to disconnect cold junction compensation circuitry during offset adjustments.

INTERCONNECTION GUIDELINES

All power supply inputs should be decoupled with 1μF capacitors as close to the unit as possible. Any jumpers installed for programming purposes should also be installed as close as possible to minimize noise pickup effects.

Since the oscillator section of the 2B50 accounts for most of the power consumption but can accept a wide range of voltages (+13V to +18V), it may be desirable to power this section from a convenient source of unregulated power.

If the same supply is to be used for both amplifier and oscillator circuitry, the power supply returns should be brought out separately so that oscillator power supply currents do not flow in the low lead of the signal output. In either case, a 1μF capacitor must be connected from $+V_{OSC}$ (Pin 28) to Oscillator COM (Pin 29).

The oscillator and amplifier sections are completely isolated; therefore, a dc power return path is not required between the two power supply commons.

GAIN SETTING

The gain of the 2B50 is set by a user-supplied resistor (R_G) connected as shown in Figure 2. Gain will normally be selected so that the maximum output of the signal source will result in a plus full scale output swing. The resistor value required is determined by the equation: $R_G = 200k\Omega/(G-1)$.

A series trim on the gain setting resistor can be used to trim out the resistor tolerance and module gain error (Figure 3). Since addition of a series resistance will always decrease gain, the value of the gain-setting resistor should be selected to provide a gain somewhat higher than the desired trimmed gain. A good quality (e.g., 10ppm/°C), metal-film resistor should be used for R_G, since drift of R_G will add to the overall gain drift of the 2B50. A cermet pot is suitable for the trim. Note that a minimum gain of 50 is required for guaranteed operation.

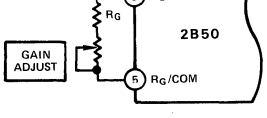


Figure 3. Gain Adjustment

INPUT AND OUTPUT OFFSET ADJUSTMENTS

The 2B50 has provisions for adjusting input and output offset errors of the module. None of the offset adjustments will affect drift performance, and adjustments need not be used unless the particular application calls for lower offsets than those specified.

Connections for offset adjustments are shown in Figure 4. Isolated supply voltages are brought out for input trimming convenience only and are not for use as a power supply for external components.

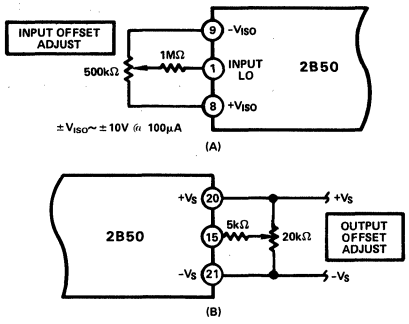


Figure 4. (A) Input and (B) Output Offset Adjustment

OFFSET CALIBRATION

1. Short Input + and Input - together.
2. Disconnect cold junction compensation circuitry by removing Jumper "A" (Figure 2).
3. Adjust input offset trim pot (±250μV range, RTI) to zero output while operating at the desired gain. In most applications, adjustment of the input offset alone will be sufficient. Output offset adjustment (±30mV range) may be performed if it is desired to adjust output offset on the nonisolated side.

OPEN INPUT DETECTION

Connecting the open input detection pin (Pin 39) to Input High (Pin 2) creates a 20nA bias current which will provide a negative overscale response if the input is opened, or in case of thermocouple "burn out". The speed at which this occurs is dependent on gain, with a typical response time of 1.4sec @ G = 250. For positive upscale response, connect a 500MΩ resistor between $+V_{ISO}$ (Pin 8) and Input Hi (Pin 2).

OUTPUT SCALING

With the output scale (Pin 16) connected to the output (Pin 17), the full scale output range is ±5V and the total gain is equal to the gain set by R_G. For applications requiring a full scale output of ±10V, a resistive divider may be connected to provide a gain of 2 at the output amplifier (see Figure 5). In this configuration, total gain will be twice the gain set by R_G. Output gains greater than 2 cannot be used.

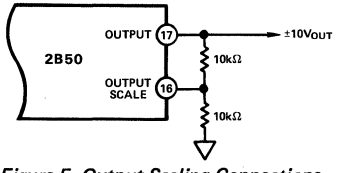


Figure 5. Output Scaling Connections

COLD JUNCTION COMPENSATION

The 2B50 may be programmed to provide cold junction compensation for types J, K and T thermocouples by connecting a jumper from Input Low (Pin 1) to the appropriate programming points (Pin 42 for J, Pin 41 for K or T). To compensate other themocouple types, a resistor (R_X) is connected from the "X" programming point (Pin 40) to Input Low (Pin 1). Table I shows the appropriate R_X values for types E, R, and S. R_X should be a 50ppm/°C, 1% tolerance resistor.

Type B thermocouples are unique, in that they have almost no output in the +5°C to +45°C range, and, therefore, do not require cold junction compensation at all. To accommodate a type B thermocouple, resistor R_X must be left open. Error due to cold junction temperature will be less than ±1°C for any measurement above 260°C. In the measurement range above 1000°C (where type B thermocouples are normally used) the error will be less than ±0.3°C.

T/C Type	R_X (kΩ)
E	1.87
R,S	19.6
B	Open

Table I. Compensation Values for Thermocouple Types E, R, S and B

REMOTE REFERENCE SENSING

In applications requiring termination of thermocouple leads at a point located remotely from the 2B50, with connections brought to the 2B50 (Pins 1, 2) by copper wires, reference temperature sensing at the remote location will be necessary. The 2B50 has provisions for connection of a 2N2222 transistor (metal can version) for use as a reference junction sensor. The connections are shown in Figure 6. The remote sensing transistor is calibrated by adjusting R_{CAL} to obtain the value of V_{CAL} as specified in Table II.

(Example: V_{CAL} = 570.0mV @ 25°C)

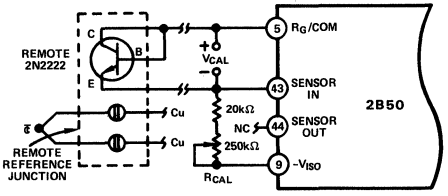


Figure 6. Remote Reference Junction Sensing

Sensor Temp (°C)	V_{CAL} (mV)
5	616.5
10	604.9
15	593.3
20	581.6
25	570.0
30	558.4
35	546.8
40	535.1
45	523.5

(Values may be interpolated)

Table II. Calibration Voltages vs. Sensor Temperature

Proper sensor placement is important. Close thermal contact of the sensor and thermocouple termination point (reference junction) is essential for accurate operation of the 2B50. The sensor may be placed any distance from the 2B50. When the sensor leads are more than ten feet long, or in the presence of strong noise signal sources, shielded cable should be used.

ANALOG DEVICES

Four-Channel, Isolated Thermocouple/mV Conditioners

2B54/2B55

FEATURES

Low Cost Per Channel
Wide Input Span Range: ±5mV to ±100mV (2B54)
±50mV to ±5V (2B55)
Pin Compatible with 2B34 RTD Conditioner
High CMV Isolation: ±1000V dc; CMR = 156dB min @ 60Hz
Low Input Offset Voltage Drift: ±1μV/°C max (2B54B)
Low Gain Drift: ±25ppm/°C max (2B54B)
Low Nonlinearity: ±0.02% max (±0.012% typ)
Normal Mode Input Protection (130V rms) and Filtering
Channel Multiplexing: 400 chan/sec Scanning Speed
Solid State Reliability

APPLICATIONS

Multichannel Thermocouple Temperature Measurements
Low and High Level Data Acquisition Systems
Industrial Measurement and Control Systems

GENERAL DESCRIPTION

Models 2B54 and 2B55 are low cost, high performance, four-channel signal conditioners. Both models are functionally complete, providing input protection, isolation and common mode rejection, multiplexing, filtering and amplification.

The 2B54 has been designed to condition low level signals (±5mV to ±100mV), like those generated by thermocouples or strain gages, in the presence of high common mode voltages. The 2B55 is optimized to condition ±50mV to ±5V or 4 to 20mA transmitter signals as inputs. The four-channel structure of both models results in significant cost and size reduction.

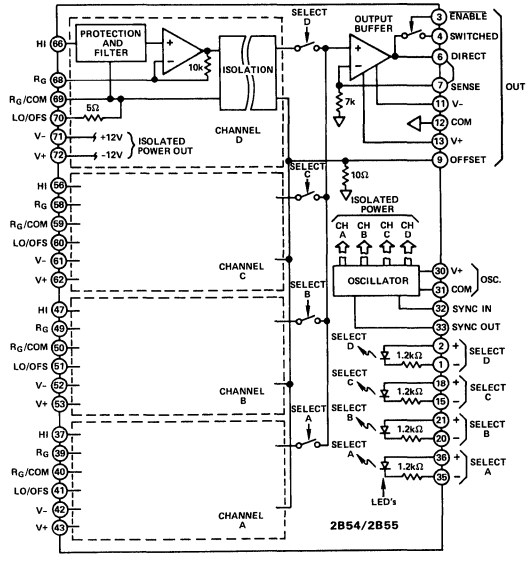
The high performance of the 2B54 and 2B55 is accomplished by the use of reliable transformer isolation techniques and an amplifier-per-channel architecture. Each of the input channels is galvanically isolated (±1000V dc) from the other input channels and from output ground. The amplifier-per-channel structure is used to obtain low input drift (±1μV/°C max, 2B54B), high common mode rejection (156dB @ 60Hz), and very stable gain (±25ppm/°C max). Other key features include low input noise (1μV p-p), low nonlinearity (±0.02% max) and open-thermocouple detection (2B54).

APPLICATIONS

Models 2B54 and 2B55 were designed to serve as a superior alternative to the relay multiplexing circuits used in multi-channel data acquisition systems, computer interface systems, process signal isolators, and temperature measurement and control instrumentation. Advantages over relay circuits include functional versatility, superior performance, and solid state reliability. Both models are also pin compatible with the 2B34, four-channel RTD/strain gage conditioner.

In thermocouple temperature measurement applications, outstanding low drift, high noise rejection, high throughput and 1000V isolation make the 2B54 a natural choice over flying

2B54/2B55 FUNCTIONAL BLOCK DIAGRAM



capacitor multiplexers in conditioning any thermocouple type. When cold junction compensation is required in measurement of temperature with thermocouples, the 2B54 may be used directly with the model 2B56 Universal Cold Junction Compensator.

DESIGN FEATURES AND USER BENEFITS

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, reliable transformer isolation and solid state switching are used. Both models have been conservatively designed to meet the IEEE standard for Transient Voltage Protection (472-1974:SWC) and offer 130V rms normal mode input protection.

High Noise Rejection: To preserve high system accuracy in electrically noisy industrial environments, the 2B54 and 2B55 provide excellent common mode noise rejection, RFI/EMI immunity, and low pass filtering for rejection of series mode noise and 50Hz/60Hz pickup.

Ease of Use: The multichannel, functionally complete design in a compact (2" X 4" X 0.4") module, assures ease of use, conserves board space and eliminates the need for a number of discrete components necessary in relay multiplexing circuits.

Low Cost: The 2B54 and 2B55 offer the lowest cost per channel for isolated, solid state, low level signal conditioners.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V and V_{OSC} = +15V, unless otherwise noted)

Model	2B54A	2B54B	2B55A
ANALOG INPUTS			
Number of Channels	4	*	*
Input Span Range	±5mV to ±100mV	*	±50mV to ±5V
Gain Equation	$G = 1 + 10k\Omega/R_G$	*	*
Gain Error	±0.2% max (G = 50 to 300)	*	±0.2% max (G = 1 to 100)
	±1% max (G = 1000)	*	NA
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max	±25ppm/°C max
Gain Nonlinearity[1]	±0.03% max (G = 50 to 300)	±0.02% max(±0.012% typ)	±0.02% max (G = 1 to 100)
	±0.03% (G = 1000)	*	NA
Offset Voltage			
Input Offset, Initial (Adj. to Zero)	±20µV max	*	±50µV max
vs. Temperature	±2.5µV/°C max	±1µV/°C max(±0.5µV/°C typ)	±5µV/°C max
vs. Time	±1.5µV/month	*	*
Output Offset (Adjustable to Zero)	±12mV max	*	*
vs. Temperature	±50µV/°C max	*	*
Total Offset Drift (RTI), max	$\pm\left(2.5+\frac{50}{G}\right)\mu V/°C$	$\pm\left(1+\frac{50}{G}\right)\mu V/°C$	$\pm\left(5\mu V+\frac{50}{G}\right)\mu V/°C$
Input Noise Voltage			
0.01Hz -100Hz, R_S = 1kΩ	1µV p-p	*	*
CMV, Channel-to-Channel or Channel-to-Ground			
Continuous, ac, 60Hz	750V rms	*	*
Continuous, ac or dc	±1000V pk max	*	*
Common Mode Rejection			
$R_S \leq 100\Omega$, $f \geq 50Hz$	156dB min (G = 1000)	*	145dB min (G = 100)
$R_S \leq 100\Omega$, $f \geq 50Hz$	128dB min (G = 50)	*	110dB min (G = 1)
Normal Mode Input, Without Damage	130V rms, 60Hz	*	*
Normal Mode Rejection, @ 60Hz	55dB min (G = 1000)	*	55dB min (G = 100)
Input Resistance, Power On	100MΩ	*	*
Power Off	35kΩ min	*	74kΩ min
Input Bias Current	+8nA max	*	*
ANALOG OUPUT			
Output Voltage Swing[2]	±5V @ ±5mA	*	*
Output Noise, dc - 100kHz	0.8mV p-p	*	*
Output Resistance			
Direct Output	0.1Ω	*	*
Switched Output	35Ω	*	*
CHANNEL SELECTION			
Channel Selection Time to ±0.01% FS	2.5ms max	*	*
Channel Scanning Speed	400 chan/sec min	*	*
Channel Select Input Reverse Voltage Rating	3V max	*	*
POWER SUPPLY			
Voltage			
Output ±V_S (Rated Performance)	±15V dc ±10%	*	*
(Operating)	±12V to ±18V dc max	*	*
Oscillator +V_{OSC} (Rated Performance)	+13.5V to +24V	*	*
Absolute max +V_{OSC}	+26V	*	*
Current			
Output ±V_S = ±15V	±4mA max	*	*
Oscillator +V_{OSC} = +15V	40mA max	*	*
Supply Effect on Offset			
Output ±V_S	100µV/V RTO	*	*
Oscillator +V_{OSC}	1µV/V RTI	*	*
ENVIRONMENTAL			
Temperature			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +85°C	*	*
Relative Humidity			
Non-Condensing to +40°C	0 to 85%	*	*
CASE SIZE	2" X 4" X 0.4"	*	*

NOTES

*Specifications same as 2B54A.

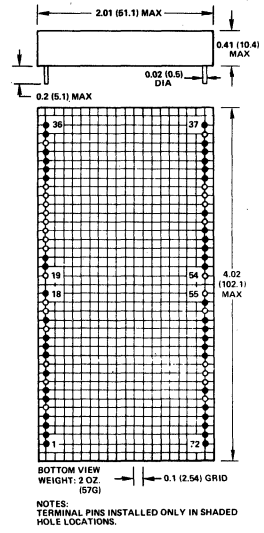
[1] Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line; e.g. nonlinearity at an output span of 10V pk-pk (±5V) is ±0.02% or ±2mV.

[2] Protected for shorts to ground and/or either supply voltage.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

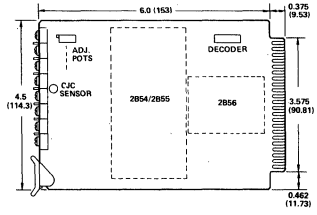


2B54/2B55 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	- SELECT CH. D	37	HI
2	+ SELECT CH. D	38	
3	SW'D OUTPUT ENABLE	39	R_G
4	SWITCHED OUTPUT	40	R_G/COM CHANNEL A
5		41	LO/OFS
6	DIRECT OUTPUT	42	V- OUT
7	SENSE	43	V+ OUT
8		44	
9	OFS. ADJ.	45	
10		46	
11	-V_S	47	HI
12	COM	48	
13	+V_S	49	R_G
14		50	R_G/COM CHANNEL B
15	- SELECT CH. C	51	LO/OFS
16		52	V- OUT
17		53	V+ OUT
18	+ SELECT CH. C	54	
19		55	
20	- SELECT CH. B	56	HI
21	+ SELECT CH. B	57	
22		58	R_G
23		59	R_G/COM CHANNEL C
24		60	LO/OFS
25		61	V- OUT
26		62	V+ OUT
27		63	
28		64	
29		65	
30	+V_{OSC} OSC. POWER	66	HI
31	COM OSC. POWER	67	
32	IN SYNC	68	R_G
33	OUT SYNC	69	R_G/COM CHANNEL D
34		70	LO/OFS
35	- SELECT CH. A	71	V- OUT
36	+ SELECT CH. A	72	V+ OUT

AC1215 OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MOUNTING CARDS AC1215, AC1216

The AC1215 and AC1216 mounting cards are available to assist in evaluation of the 2B54 and 2B55. These 4 1/2" X 6" printed circuit edge connector cards have sockets that allow a 2B54/2B55 and 2B56 to be plugged directly onto them, as well as offset adjustment pots, and address decoding circuitry. The AC1215 and AC1216 differ only in input signal connections: the AC1215 includes a screw terminal block and AC1216 has an edge connector.

Mating Connector:
Cinch 251-22-30-160 or equivalent.

FUNCTIONAL DESCRIPTION

The internal structure of the 2B54/2B55 is shown in Figure 1. Four individually isolated input channels are multiplexed into a single output buffer, with the desired channel selected by control inputs SELECT A through SELECT D. Isolated power and timing signals for the input channels are provided by an internal oscillator.

Each channel contains an input protection and filtering network and a low-drift amplifier whose gain is set by a user-supplied resistor (R_G). Additional filtering is provided in the amplifier circuit. This structure preserves signal integrity by taking all signal gain ahead of the isolation and multiplexing circuits. The isolated power supply for each channel is brought out to permit convenient fine adjustment of the input offset voltage if desired.

Transformer coupling is used to achieve stable, reliable galvanic isolation of each channel from all other channels and from output ground. Although the bandwidth of the input channels is small (<2Hz at high gains) to provide immunity to normal-mode noise, the multiplexing technique allows the channels to be scanned at a high rate (400 channels/sec). Thus a high revisitation rate is maintained even in systems with a large number of input channels.

The output buffer amplifier operates at unity gain with feedback provided by an external connection from the DIRECT output to the SENSE input. The DIRECT output provides a ±5V swing with low source resistance to permit error-free operation with heavy loads. In addition, a separate series-switched output with an active-low enable control is provided so that multiple modules may be combined without the use of external analog multiplexers. An offset trim point which does not affect drift is also provided on the output channel.

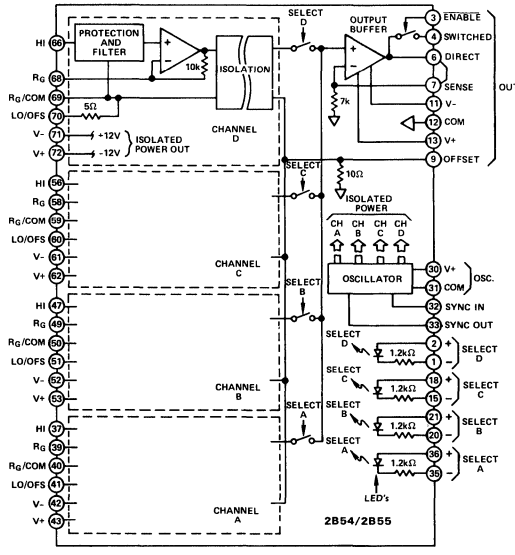


Figure 1. 2B54/2B55 Functional Block Diagram

The internal oscillator has its own power supply pins for enhanced application flexibility, and a sync mechanism is provided to eliminate beat-frequency errors when multiple 2B54/2B55's are used or when a system clock is present.

The 2B54 and 2B55 share the same design, differing only in input specifications and filter characteristics.

OPERATING INSTRUCTIONS

The connections shown in Figure 2 are common to most applications of the 2B54/2B55, and in many cases will be all that is required. The following sections describe this basic application and also detail some optional connections which enhance the module's utility in more complex applications.

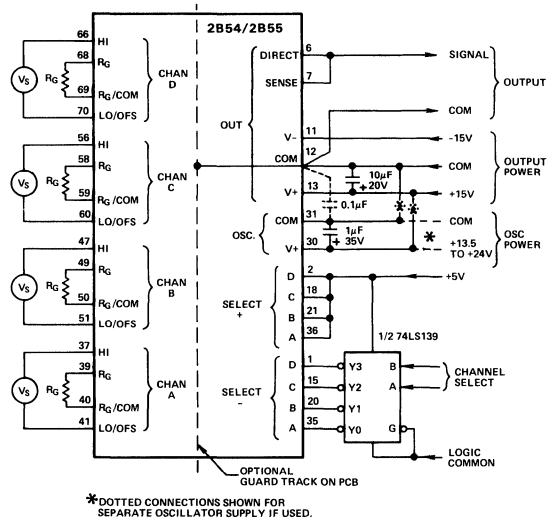


Figure 2. Basic 2B54/2B55 Application

Interconnection Guidelines

In any high accuracy isolator application it is important to minimize coupling between input and output, and the 2B54/2B55 pinout has been designed to make this easy to do. For best results, keep all leads associated with signals on the input edge as far as possible from signals on the output edge. This will minimize the effects of board leakage and capacitance. The use of a guard track on both sides of the board (Figure 2) can also be helpful.

The power supplies should be decoupled with tantalum capacitors as close to the unit as possible. For lowest noise, the output grounding scheme should be as shown in Figure 2. The output signal common is connected directly to pin 12, with power supply returns brought separately to that pin so that power supply currents do not flow in the low lead of the signal output.

Since most of the power taken by the 2B54/2B55 is supplied to the internal oscillator which requires only a positive supply and can accommodate a wide range of supply voltages, it is sometimes desirable to power the oscillator from a convenient source of unregulated power (such as +24V — Figure 2). A 0.1µF capacitor should be then connected directly from pin 12 to pin 31. Since the output and oscillator circuits are not fully isolated, a dc path must exist between the two power supply commons. A small (one or two volts) potential difference between OUT COM and OSC COM will not affect operation.

Gain Setting

The gain of each channel is independently set by a user-supplied resistor (R_G) connected as shown in Figure 2. Channel gain will normally be selected so that the maximum output of the signal source will result in a plus or minus full scale (±5V) output swing. The resistor value required is $R_G = 10k\Omega/(G-1)$. Thus if $R_G = 101\Omega$, the gain will be 100, and an input signal swing of ±50mV will yield an output span of ±5V.

A parallel trim on the gain-setting resistor can be used to trim out the resistor's tolerance and the module's gain error (Figure 3). Since a parallel trim will always increase the gain, the value of the gain-setting resistor should be chosen to give an untrimmed gain somewhat lower than the desired trimmed gain. Good quality metal-film resistors should be used for R_G since gain accuracy and drift are a direct function of R_G's characteristics. Cermet pots are suitable for the trim.

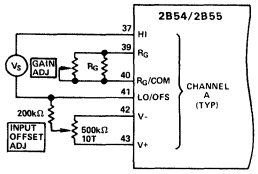


Figure 3. Input Offset and Gain Adjustments

Optional Offset Adjustment

The 2B54/2B55 has provision for fine adjustment of the input offset of each channel and the output offset of the entire module. None of the offset adjustments affect offset drift, and there is no need to make any adjustment unless the application calls for tighter offsets than those specified for the module type.

Connections for input offset adjustment are shown in Figure 3. This is a fine trim with a limited range (±250μV – 2B54 and ±1mV – 2B55, RTI), used to adjust each channel for zero offset while operating at the desired gain. Since the range of the input offset trim is small, it will usually be necessary to adjust output offset first. This can be conveniently done by operating one channel with zero input at unity gain (by disconnecting the gain resistor) and adjusting the output offset control for zero output. Connections for output offset adjustment are shown in Figure 4.

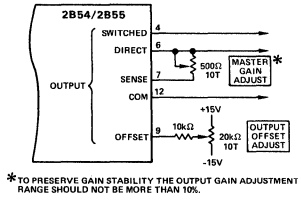


Figure 4. Output Offset and Master Gain Adjustments

An alternative offset adjustment procedure is appropriate in applications where the channel gains are field-selected by switching the gain-setting resistor. Here it is desirable to set the input offset so that there is no zero shift at the output when the gain is changed. To make the adjustment, switch back and forth from low to high gain with zero input and adjust the input offset control until no shift occurs at the output when changing gains. Then adjust the output offset control for zero output at the lower gain.

Stable components (a metal film resistor and a cermet pot) should be used for the input offset adjustment to avoid compromising drift. Output offset adjustment components are not critical and may be omitted altogether when a single 2B54/2B55 is followed by an A to D Converter that has a zero adjustment.

Channel Selection

Each channel in the 2B54/2B55 is turned on and off by a SELECT input. As indicated in Figure 1, each SELECT input consists of an LED in series with a resistor, and is not connected to any other circuits in the module. Turning the LED on (I≥2.5mA) turns the channel on, and turning the LED off (I≤50μA) turns the channel off. This allows considerable flexibility of connection, but the easiest way to use the SELECT inputs is to tie all four SELECT + pins to +5V and drive the SELECT–inputs from TTL logic (either open-collector or totem-pole outputs can be used), as shown in Figure 2.

It is also possible to use CMOS logic to drive the SELECT inputs (Figure 5). With a +15V logic supply a standard CMOS decoder or gate can supply enough current to drive the SELECT inputs directly, but at lower supply voltages it is advisable to use a buffer such as that shown in Figure 5b. The power taken by the SELECT inputs is small, since only one is on at a time, but at the higher CMOS supply voltages more current than the required 2.5mA will flow. This does not affect operation, but if desired the current can be brought back to the minimum value with series resistors as shown in Figure 5. Use 2kΩ for 10V operation, and 3.9kΩ at 15V.

The maximum reverse voltage applied to any SELECT input must be limited to 3V to avoid damage to the LED. Maximum forward current should be kept below 25mA. Each SELECT input is isolated from all other circuits in the module and may be operated up to ±50V away from output and power ground.

Channels may be selected in any order, and there are no restrictions on rate or duty cycle except the 2.5ms settling time for access to a channel. It should be noted, however, that selecting two or more channels simultaneously for more than a few microseconds will result in a very long settling time when the conflict is resolved. Timing overlaps should therefore be avoided.

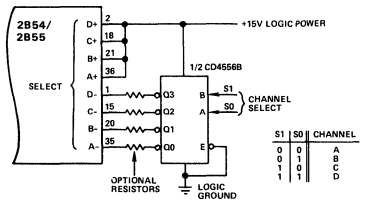


Figure 5a.

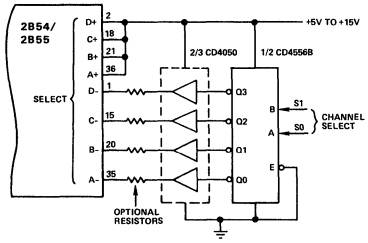


Figure 5b.

Figure 5. CMOS Channel Selection

Channel Expansion

The 2B54/2B55 has provision for directly interconnecting several modules when more than four channels are needed. The series-switched outputs of a group of modules are connected together, the SELECT inputs are driven in parallel, and the output of the desired module is selected using the Output Enable pin. This is shown in Figure 6. A single 74LS139 decoder is used to drive the SELECT inputs of up to four modules, and also provides address expansion so that the binary coded channel address word selects the appropriate module output via the Output Enable pins. The overall operation of the series-switched outputs is analogous to three-state logic, and the output rail is thus an analog bus.

It is possible to operate up to sixteen modules in parallel, for a total of 64 input channels. Note that it will be necessary to break up the SELECT inputs into several groups to avoid overloading the decoder when many modules are used. The settling time of the output switches is <50μs to ±0.01% and is thus negligible in comparison to the channel selection times.

The Output Enable signal is active low, and is compatible with both TTL and CMOS logic. The switching threshold is +1.8V; input current at 0V is typically -0.4mA.

The output resistance of the Switched Output (typically 35Ω +0.5%/°C) is low enough to provide fast switching times but will cause gain errors when driving a heavy load. A single buffer isolating the Switched Outputs from the load will solve this problem in an "analog bus" application (Figure 6). In single-module applications the DIRECT (low impedance) output should be used. Note that in all cases the SENSE pin *must* be connected to the DIRECT output to provide feedback for the output amplifier.

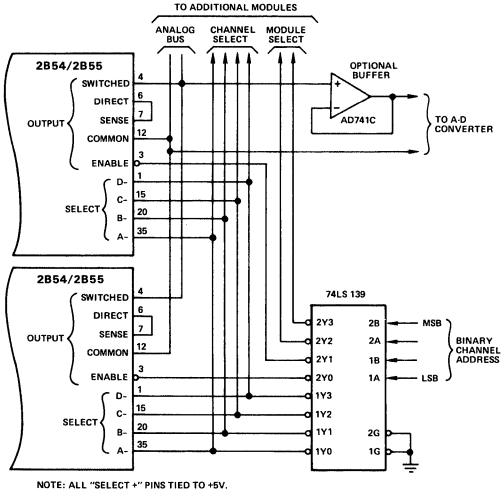


Figure 6. Expansion to More than Four Channels

Synchronization

In applications where multiple 2B54/2B55's are used in close proximity or when system clock signals are present near the isolator, differences in individual oscillator frequencies may cause "beat frequency" related output errors. To eliminate these errors, multiple units may be synchronized by connecting the SYNC OUT (pin 33) terminal to the SYNC IN (pin 32) terminal of the adjacent 2B54/2B55 (Figure 7). The first of a group of modules may be synchronized to an external source via the SYNC IN pin. To minimize noise pickup, sync wiring should be separated from analog signal runs.

The frequency of the external sync source, when used, will have a small effect on the gain and output offset of the 2B54/2B55. Thus any adjustments should be made with the module synchronized.

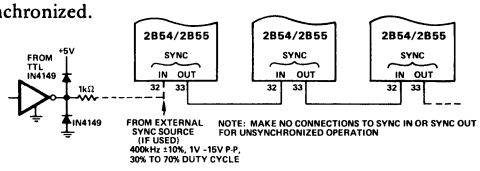


Figure 7. Synchronization

Open Input Detection

The 2B54 can be programmed to respond to an open-circuit condition on a channel input with either an upscale or downscale response when the affected channel is selected. The response time to detect an open input can be in the tens of seconds, since only a few nA of input bias current are available to charge the input filter. The circuits in Figure 8 indicate the selection of either downscale or upscale response and can be used to provide shorter open-circuit response times. Either circuit will produce a bias current of approximately 20nA which can be used to aid or oppose the 3nA typically supplied by the module, as shown. The circuit of Figure 8A has the advantage of simplicity, but the high-value resistor may not be readily available. Figure 8B shows how to solve the problem at the expense of complexity. The values shown may be modified to give an optimum trade of bias current for response time in a given application. A 2 to 5 second response is typical for the values shown.

If a downscale response is desired, a resistor divider circuit like Figure 8B may be desired to prevent a negative overscale. If a negative overscale condition occurs (typically -7V), the output will saturate on all channels.

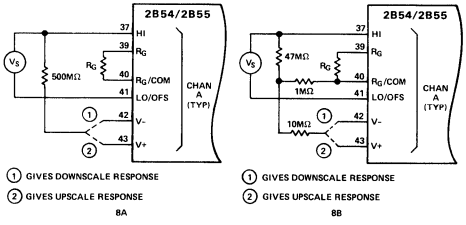


Figure 8. High Speed or Reversed Open Input Detection

Output Filtering

In most applications, no output filtering will be required since the effect of the small carrier-related noise spikes on the output (<1mV p-p, 100kHz B.W.) drops off rapidly as bandwidth decreases and in many cases will be negligible. In some applications (e.g., when driving a successive-approximation A to D) the effective system bandwidth may be large enough to pass the noise. To eliminate the carrier noise (without any effect on switching times), a simple R-C filter may be used at the output (Figure 9A). Only one filter is needed even when multiple modules are used, as shown in Figure 9B. If the load to be driven has an input resistance of less than 10MΩ, a buffer will be needed.

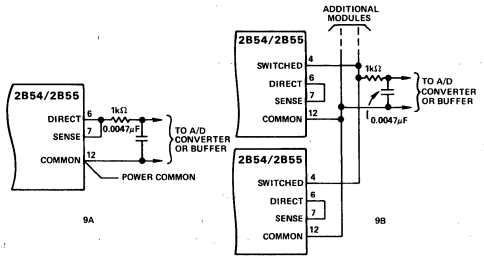


Figure 9. Output Filtering

CMR AND NMR PERFORMANCE

Common mode rejection is a result of both isolation and filtering and indicates ability to reject common mode inputs while amplifying differential signal inputs. CMR is dependent on source impedance imbalance, signal frequency and conditioner gain.

Normal mode rejection is also a function of the 2B54/2B55 gain. Figures 10 and 11 illustrate typical CMR and NMR performance. Note that any additional low pass filtering (e.g., an integrating A to D converter) at the output of the 2B54/2B55 will further improve both CMR and NMR performance.

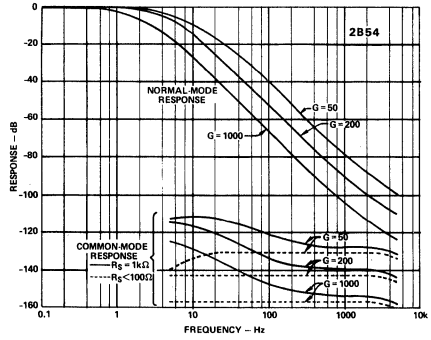


Figure 10. Common Mode and Normal Mode Response – 2B54

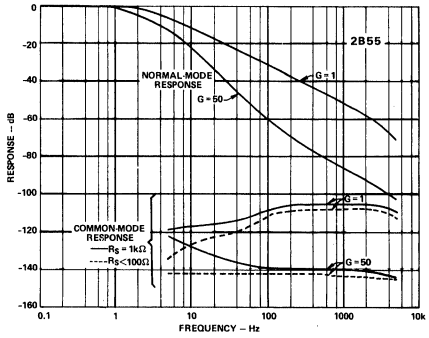


Figure 11. Common Mode and Normal Mode Response – 2B55

APPLICATIONS

Thermocouple Temperature Measurement: Figure 12 shows a four-channel thermocouple input system with isolation, amplification, and multiplexing provided by the 2B54. Several different thermocouple types are used, and the gain-setting resistors on each channel have been chosen to take the standard ANSI range for each type to a 5V output span. Since thermocouples must be compensated for the temperature of the reference junction which is formed where the thermocouple leads are terminated, the 2B56 Universal Cold Junction Compensator is used. The 2B56 monitors the temperature of the reference junction (terminal block) via an external sensor and corrects the signal at the output of the 2B54 for reference temperature. Compensation for several thermocouple types is selectable via digital control inputs. Thermocouple linearization, if needed, would be typically performed in system's software.

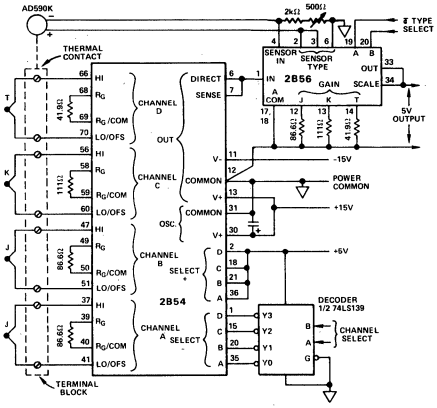


Figure 12. Four-Channel Thermocouple Temperature Measurement with Cold Junction Compensation

Process Signals Interface: In Figure 13, the 2B55 is used to provide floating inputs for four 4-20mA process signal loops. The use of floating inputs in this type of application gives protection from common-mode voltages and greatly simplifies system configuration, since additional loads in series with the loop can be connected on either side of the isolator input.

Each current input is converted into a 1 to 5 volt signal by a 250Ω resistor. The 2B55 is operated at unity gain (no gain-setting resistors) so that a 1 to 5 volt signal appears at the output. Since no gain-setting resistors are used, gain adjustment, if required, is done by connecting trims directly across the input resistors. Other current ranges can be accommodated by changing the value of the input resistors.

When there are several loads on the loop, compliance voltage at the transmitter may be at a premium. In this case it will be advantageous to reduce the voltage swing at the isolator inputs by using smaller resistors (perhaps 25Ω) and scaling the output back to a 5V span by taking an appropriate gain in the isolator.

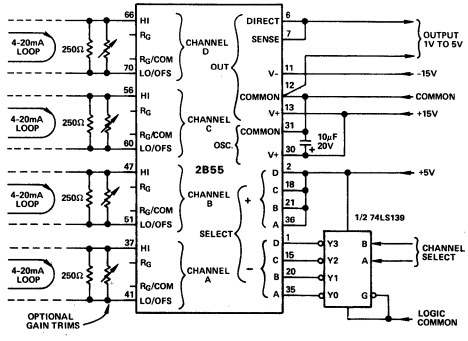


Figure 13. Isolated 4–20mA Loop Signals Interface

Complete Signal Conditioning I/O Subsystem

3B Series

FEATURES/BENEFITS

Low Cost, Completely Integrated 16-Channel Modular Signal Conditioning Subsystem
- **Wide Selection of Functionally Complete Input and Output Plug-In Modules**
- **Rugged Industrial Chassis, Rack or Surface Mounted**
- **On-Board Power Supplies Available**

Analog Input Modules Available for Direct Interface to a Wide Variety of Signal Sources
- **Thermocouples, RTDs, AC and DC Strain Gages, Torque Transducers, LVDTs**
- **Millivolt, Voltage and Frequency Sources, 4-20mA/0-20mA Process Current Inputs**

Current Output Modules
- **4-20mA/0-20mA Outputs**

Complete Signal Conditioning Function
- **Input Protection, Filtering, Amplification, Galvanic Isolation to ±1500V,**
- **Wide-Range Zero Suppression,**
- **High Noise Rejection and RFI/EMI Immunity,**
- **Simultaneous Voltage and Current Outputs**

FM Approved for Use in Class I, Division 2, Groups A, B, C and D Locations

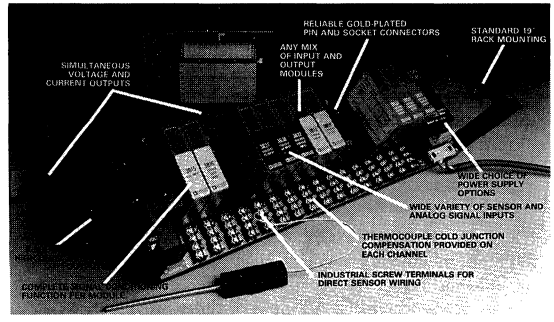
GENERAL DESCRIPTION

The 3B Series Signal Conditioning I/O Subsystem provides a low cost, versatile method of interconnecting real-world analog signals to a data acquisition, monitoring or control system. It is designed to interface directly to analog signals such as thermocouple, RTD, ac and dc strain gage, torque transducer, or AD590/AC2626 solid state temperature sensor outputs or millivolt or process current signals and convert the inputs to standardized analog outputs compatible with high level analog I/O subsystems.

The 3B Series Subsystem consists of a 19″ relay rack compatible universal mounting backplane and a family of plug in (up to 16 per rack) input and output signal conditioning modules. Eight and four channel backplanes are also available. Each backplane incorporates screw terminals for sensor inputs and current outputs and a connector for high level single ended outputs to the user's equipment.

The input and output modules are offered in both isolated (±1500V peak) and nonisolated versions. The input modules feature complete signal conditioning circuitry optimized for specific sensors or analog signals and provide high level analog outputs. Each input module provides two simultaneous outputs: 0 to 10V (or ±10V) and 4-20mA (or 0-20mA). Output modules accept high level single ended signals and provide an isolated or nonisolated 4-20mA (or 0-20mA) process signal. All modules feature a universal pin-out and may be readily "mixed and matched" and interchanged without disrupting field wiring.

Each backplane contains the provision for a subsystem power supply. The 3B Series Subsystem can operate from a dc/dc converter or ac power supply mounted on each backplane or from externally provided dc power. Two LEDs are used to indicate that power is being applied.



APPLICATIONS

The Analog Devices 3B Series Signal Conditioning Subsystem is designed to provide an easy and convenient solution to signal conditioning problems in measurement and control applications. Some typical uses are in mini- and microcomputer based systems, standard data acquisition systems, programmable controllers, analog recorders, dedicated control systems, and any other applications where monitoring and control of temperature, pressure, flow, and analog signals are required. Since each input module features two simultaneous outputs, the voltage output can be used to provide an input to a microprocessor based data acquisition or control system while the current output can be used for analog transmission, operator interface, or an analog backup system.

DESIGN FEATURES AND USER BENEFITS

Ease of Use: Direct sensor interface via screw terminals, standardized high level outputs, factory precalibration of each unit and the modular design make the 3B Series Subsystem extremely easy to use. The subsystem features rugged packaging for the industrial environment and can be easily installed and maintained.

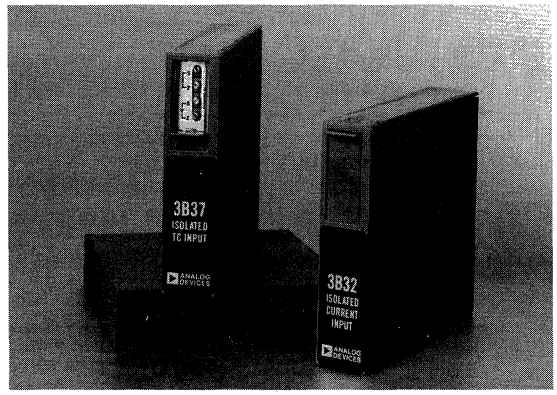
High Protection and Reliability: All field wired terminations offer 130V or 220V rms normal-mode protection. To assure connection reliability, gold plated pin and socket connections are used throughout the system. The isolated modules offer protection against high common-mode voltages and are designed to meet the IEEE Standard for Transient Voltage Protection (472–1974: SWC).

High Performance: The high quality signal conditioning features ±0.1% calibration accuracy and chopper-based amplification which assures low drift (±1μV/°C) and excellent long-term stability. For thermocouple applications, high accuracy cold junction sensing is provided in the backplane on each channel. Low drift sensor excitation is provided for RTD, strain gage, LVDT and AD590 models. RTD models and the 3B47 thermocouple model linearize the input signal to provide an output which is linear with temperature.

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

FEATURES

Wide Variety of Sensor Inputs
Thermocouples, RTDs, AC and DC Strain Gages, Torque Transducers, LVDTs, AD590/AC2626
Dual High Level Outputs
Voltage: 0 to +10V or ±10V
Current: 4-20mA/0-20mA
Mix and Match Input Capability
Sensor Signals, mV, V, 4-20mA, 0-20mA
High Accuracy: ±0.1%
Low Drift: ±1μV/°C
Reliable Transformer Isolation:
±1500V CMV, CMR =160dB
Meets IEEE-STD 472: Transient Protection (SWC)
Input Protection: 130V or 220V rms Continuous
Low Cost Per Channel



GENERAL DESCRIPTION

Each input module is a single channel signal conditioner that plugs into sockets on the backplane and accepts its signal from the input screw terminals. All input modules provide input protection, amplification and filtering of the input signal, accuracy of ±0.1%, low drift of 1μV/°C (low level input modules), and feature two high level analog outputs that are compatible with most process instrumentation. The isolated input modules also provide ±1500V isolation.

The choice of specific 3B module depends on the type of input signal and also whether an isolated or nonisolated interface is required. Input modules are available to accept millivolt, volt, process current, thermocouple, RTD, ac and dc strain gage, torque transducers and AD590 inputs. The voltage output of each module is available from the voltage I/O connector while the current output is available on the output screw terminals.

THERMOCOUPLE INPUT MODELS 3B37, 3B47

The isolated thermocouple models incorporate cold junction compensation circuitry which provides an accuracy of ±0.5°C over the +5°C to +45°C ambient temperature range. Open thermocouple detection (upscale) is also provided. Standard models are available for thermocouple types J, K, T, E, R, S and B. Factory configured custom ranges are also available. The 3B37-X-00 can be user configured with the AC1310 ranging card. The 3B47 internally linearizes the thermocouple signal. All screw terminals have a 220V rms protection.

RTD INPUT MODELS 3B14, 3B15, 3B34

Each RTD model provides a sensor excitation current and produces an output signal that is linear with temperature with a conformity error of ±0.05% of span and accuracy of ±0.1% span. The lead resistance effect for the three models is ±0.02°C/Ω for the 3B14 and the 3B34, and ±.00001°C/Ω for the 3B15. All excitation input and output screw terminal connections have at least 130V rms protection.

STRAIN GAGE INPUT MODEL 3B16

Models 3B16 accepts inputs from full four arm bridge strain gage-type transducers. It provides a constant +10V bridge excitation and can be used with a bridge resistance of 300Ω or greater. All excitation input and output screw terminal connections have 130V rms protection.

WIDEBAND STRAIN GAGE MODEL 3B18

Model 3B18 accepts inputs from full four arm bridge strain gage-type transducers. It provies a switch selectable excitation of +3.3V or +10.0V and can be used with 100Ω to 1000Ω strain gage bridges. The module has a 20kHz bandwidth to interface to dynamic signals.

AC STRAIN GAGE/TORQUE TRANSDUCER INPUT MODEL 3B20

Model 3B20 is a nonisolated wideband input module that is designed to interface to four arm bridge transducers or transformer coupled torque transducers. The 3B20 provides an ac excitation of 2-10V rms at frequencies ranging from 1kHz to 10kHz. This module can accept inputs from 1.5mV rms to 150mV rms.

MILLIVOLT AND VOLTAGE INPUT MODELS 3B10, 3B11, 3B30, 3B31

Models 3B10 and 3B11 are nonisolated modules that accept mV and V signals respectively. Models 3B30 and 3B31 are isolated modules that accept mV and V signals respectively. All screw terminal connections have at least 130V rms protection.

WIDEBAND MILLIVOLT AND VOLT INPUT MODELS 3B40, 3B41

Models 3B40 and 3B41 are isolated modules that accept mV and V signals respectively. The modules have a 10kHz bandwidth to interface to dynamic signals. All screw terminal connections have at least 130V rms protection.

CURRENT INPUT MODELS 3B12, 3B32

Models 3B12 (nonisolated) and 3B32 (isolated) accept process current signals. Both models use a 100Ω sensing resistor that is mounted on backplane terminals 2 and 3. All screw terminal connections have at least 130V rms protection.

AD590 INPUT MODEL 3B13

Model 3B13 accepts an AD590 as its input signal. Sensor excitation is provided and a 2kΩ sensing resistor is mounted on backplane terminals 2 and 3. All excitation input and output screw terminal connections have 130V rms protection.

LVDT OR RVDT INPUT MODEL 3B17

Model 3B17 accepts signals from 4, 5 and 6 wire LVDT or RVDT transducers. It provides an ac excitation of 1-5V rms at frequencies ranging from 1kHz to 10kHz and has a 100Hz bandwidth. All screw terminal connections have 130V rms protection.

AC INPUT MODELS 3B42, 3B43 AND 3B44

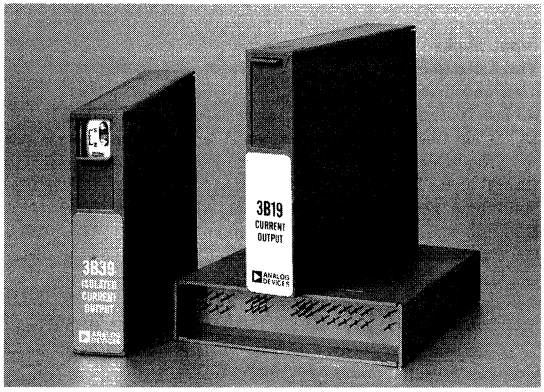
Models 3B42, 3B43, and 3B44 accept ac signals from 20mV to 450V rms. The modules are rms calibrated for sinusoidal inputs, such as ac power lines. All screw terminal connections have at least 130V rms protection.

FREQUENCY INPUT MODELS 3B45, 3B46

Models 3B45 and 3B46 accept frequency input signals from 25Hz to 25kHz. User selectable thresholds of 1.6V and 0V (for zero crossing) are available. All screw terminal connections have at least 130V rms protection.

Output Modules – 3B Series

FEATURES
High Level Voltage Input (0 to +10V, ±10V)
Process Current Output (4-20mA/0-20mA)
High Accuracy: ±0.1%
Reliable Transformer Isolation: ±1500V CMV, CMR = 90dB
Meets IEEE-STD 472: Transient Protection (SWC)
Output Protection: 130V or 220V rms Continuous
Reliable Pin and Socket Connections
Low Cost Per Channel



GENERAL DESCRIPTION

Each output module accepts a high level analog signal from the system connector and provides a current output on the output screw terminals. When a +24V loop supply is used, loads up to 850Ω can be driven. If desired, +15V can be used to power the output modules with a smaller load (up to 400Ω). Each output module features high accuracy of ±1%. If isolation is required, the 3B39 provides ±1500V peak common-mode voltage isolation protection.

NONISOLATED OUTOUT MODEL 3B19

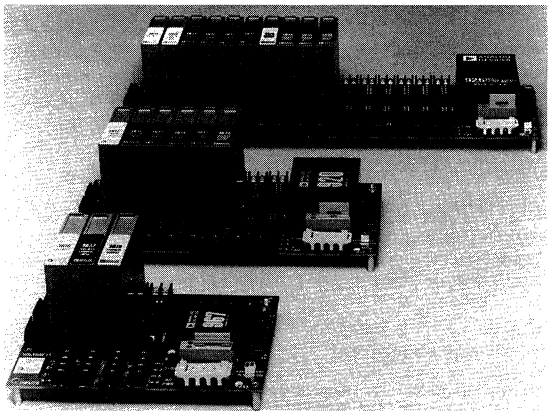
The 3B19 output module accepts a 0 to +10V or ±10V input signal and converts it to a proportional current output. Output ranges are jumper selectable for either 0-to 20mA or 4-to-20mA. The current output is protected to 130V rms continuous.

ISOLATED OUTPUT MODEL 3B39

Model 3B39 is an isolated module that accepts a 0 to +10V or ±10V input signal and converts it to a proportional current output. Output ranges are jumper selectable for either 0-to-20mA or 4-to-20mA. Input to output isolation is rated to 1500V pk continuous.

Backplanes

FEATURES
4-, 8-, or 16-Channel Versions Available
ac or dc Power Supply Options



GENERAL DESCRIPTION

The three backplane models, 3B01, 3B02 and 3B03 are designed for 16, 8 and 4 channels, respectively, to give users the flexibility to match the size of a system to specific applications. The 16-channel backplane can be mounted in a 19″×5.25″ panel space. The backplanes can be surface mounted, mounted on a rack or mounted in a NEMA enclosure.

POWER SUPPLY

The 3B Series Subsystem can operate from a common ac power supply or dc/dc (+24V input) power supply mounted on the backplane or an externally provided ±15V and +24V supply. The power supply is bussed to all signal conditioners in the system. The current consumption is a function of the modules that are actually used.

3B Series Subsystem Specifications

INPUT MODULES

Input Types
Thermocouples: J, K, T, E, R, S, B
Thermocouples: J, K, T, E, R, S, B (Linearized)
RTDs: 100Ω Platinum, 10Ω Copper, 120ΩNickel (Linearized)
DC Strain Gage Transducers: ±30mV and ±100mV spans
AC Strain Gage/Torque Transducers: 1.5mV to 150mV rms
LVDT or RVDT: 4, 5, 6 Wire
Solid State Temperature Transducers: AD590 or AC2626
DC Voltage: ±10mV, ±50mV, ±100mV ±1V, ±5V, ±10V
DC Current: 4-to-20mA, 0-to-20mA
AC Voltage: 0-50mV rms, 0-100mV rms, 0-10V rms, 0-150V rms, 0-250V rms
Frequency: 0-25Hz, 0-300Hz, 0-1500Hz, 0-3000Hz, 0-25kHz

Outputs (Simultaneous)
0 to +10V or ±10V and
4-to-20mA or 0-to-20mA*

Performance
Accuracy: ±0.1% of span
Nonlinearity: ±0.01% of span
Bandwidth: 3Hz (−3dB)

Isolated Modules
Common-Mode Voltage, Input to Output: ±1500V pk continuous
Transient Protection: Meets IEEE-Std 472 (SWC)
Normal-Mode Input Protection: 220V rms continuous
Current Output Protection: 130V rms continuous
Common-Mode Rejection @ 50Hz or 60Hz: 160dB
Normal-Mode Rejection @ 50Hz or 60Hz: 60dB

Nonisolated Modules
Common-Mode Voltage: ±6.5V
Normal-Mode Input Protection: 130V rms continuous
Current Output Protection: 130V rms continuous
Common-Mode Rejection @ 50Hz or 60Hz: 90dB
Normal-Mode Rejection @ 50Hz or 60Hz: 60dB

OUTPUT MODULES

Input
0 to +10V or ±10V

Output
4-to-20mA or 0-to-20mA

Performance
Accuracy: ±0.1% of span
Nonlinearity: ±0.01% of span

Isolated Module
Common-Mode Voltage,
Input to Output: ±1500V pk continuous
Current Output Protection
Transient: Meets IEEE-Std 472 (SWC)
Continuous: 220V rms

Nonisolated Module
Current Output Protection: 130V rms continuous

*There is no current output on the 3B47.
Specifications subject to change without notice.

BACKPLANES

Channel Capacity
3B01: 16 channels
3B02: 8 channels
3B03: 4 channels

POWER SUPPLIES

Backplane Mounted:
100, 115, 220, 240V ac, 50/60Hz
or +24V dc
External Power Option
±15V dc and +24V dc

MECHANICAL

Input or Output Modules:
3.150″ × 0.775″ ×3.395″
(80.0mm × 19.7mm × 86.2mm)
Backplanes:
3B01: 17.40″ × 5.20″ × 4.37″
(442.0mm × 132.1mm × 111.1mm)
3B02: 11.00″ × 5.20″ × 4.37″
(279.4mm × 132.1mm × 111.1mm)
3B03: 7.80″ × 5.20″ × 4.37″
(198.1mm × 132.1mm × 111.1mm)

ENVIRONMENTAL

Temperature Range, Rated Performance:
−25°C to +85°C
Storage Temperature Range:
−55°C to +85°C
Relative Humidity: Conforms to MIL-STD 202, Method 103
RFI Susceptibility: ±0.5% span error, 5W @ 400MHz @ 3 ft.

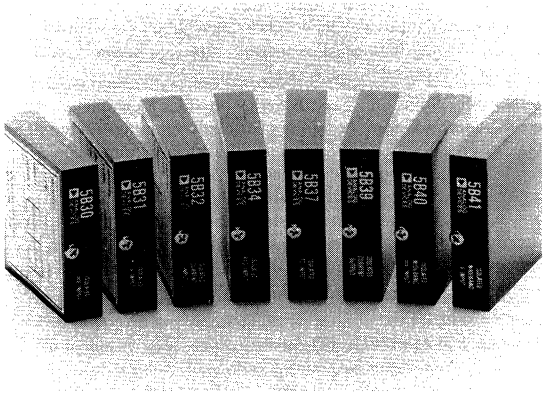
ANALOG DEVICES

Compact, Low Cost Modular Signal Conditioners

5B Series

FEATURES

- **Rugged, Compact, Low Cost Signal Conditioners**
- **Analog Input Modules for Direct Interface to**
  Sensors: Thermocouples, RTDs, and Strain Gages
  Millivolt and Voltage Sources
  4-20mA or 0-20mA Process Current Inputs
- **Analog Output Module**
  4-20mA or 0-20mA Process Current Output
- **Complete Signal Conditioning Function**
  240V rms Field Wiring Protection, Filtering, Amplification, 1500V rms CMV Isolation, High Noise Rejection, RFI/EMI Immunity, and Wide Range Zero Suppression
- **High Accuracy: ±0.05%**
- **Low Drift: ±1μV/°C**
- **−25°C to +85°C Temperature Range**
- **Mix and Match Module Capability**
- **Convenient Connection to User's Equipment**
- **Simplified Designer Application**
- **Custom Ranged Modules Available**
- **FM Approved**
  Approved for Use in Class I, Division 2, Groups A, B, C and D Locations



The 5B Series provides system designers with an easy to use solution for analog I/O in a minimum of board space. The modules' simple pinout and easy mechanical application simplify design.

There are also a number of backplanes which provide a complete signal conditioning solution for end users. Each backplane incorporates screw terminals for field wiring inputs and outputs and cold junction compensation sensors for thermocouple applications. Nineteen-inch relay rack compatible units that can hold up to sixteen modules are available.

GENERAL DESCRIPTION

The 5B Series represents an innovative generation of low cost, high performance plug-in signal conditioners. Designed for industrial applications, these modules incorporate a new circuit design utilizing transformer-based isolation and automated surface mount manufacturing technology. They are compact, economical components whose performance exceeds that available from more expensive devices. Combining 1500V rms continuous CMV isolation, ±0.05% calibrated accuracy, small size and low cost, the 5B Series is an attractive alternative to expensive signal conditioners and in-house designs.

All modules are hard potted and identical in pinout and size (2.25″ × 2.25″ × 0.60″). They can be mixed and matched, permitting users to address their exact needs, and may be changed without disturbing field wiring. The isolated input modules provide 0 to +5V or ±5V outputs and accept J, K, T, E, R, S and B thermocouples; 100Ω platinum, 10Ω copper and 120Ω nickel RTDs, full or half bridge strain gages; mV, V, 4-20mA or 0-20mA, and wide bandwidth (10kHz) mV and V signals. These modules feature complete signal conditioning functions including 240V rms input protection, filtering, chopper stabilized low drift (±1μV/°C), amplification, 1500V rms isolation, linearization for RTD and thermocouple (with 5B47) inputs and sensor excitation when required. The output module converts a 0 to +5V input to an isolated 4-20mA or 0-20mA process current signal. All modules feature excellent common mode rejection and meet IEEE 472-1974 surge withstand specs.

APPLICATIONS

These signal conditioners are designed to provide an easy and convenient solution to signal conditioning problems of both designers and end users in measurement and control applications. Typical uses include mini- and microcomputer-based measurement systems, standard data acquisition systems, programmable controllers, analog recorders and dedicated control systems. The 5B Series modules are ideally suited to applications where monitoring and control of temperature, pressure, flow and other analog signals are required.

FM APPROVAL/THE 5B SERIES

The 5B Series Signal Conditioners are approved by Factory Mutual for use in Class I, Division 2, Groups A, B, C and D locations. This approval certifies that the 5B Series is suitable for use in locations where a hazardous concentration of flammable gas exists only under unlikely conditions of operation. Equipment of this type is called "nonincendive" and needs no special enclosure or other physical safeguards.

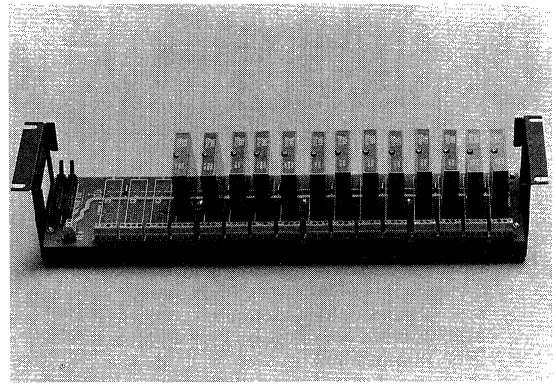
DESIGN FEATURES AND USER BENEFITS

System Design: It is easy for system designers to apply the functionally complete 5B Series modules in their own circuit board or backplane. These modules feature a simple pinout, plug into widely available sockets and are secured with self-contained mounting screws. Other features, which can be used to minimize system interface cost, have also been incorporated in the 5B Series design. Each input module has an output switch which is controlled by a TTL-compatible enable input, eliminating the need for an external multiplexer. Each output module has a track and hold input which permits a single DAC to serve numerous current output channels. For thermocouple applications, cold junction compensation sensors are available.

Subsystem Solution: The 5B Series provides a complete signal conditioning solution. A family of backplanes, plug-in modules, factory precalibration of each unit, direct sensor interface via screw terminal connections, standardized high level outputs, and ribbon cable system interface result in easy integration into any system. For thermocouple applications, high accuracy cold junction compensation sensing is provided on each channel. A general susbsystem application is outlined in Figure 1.

Flexibility: The 5B Series can be easily tailored to meet each user's needs. These plug-in signal conditioners can be mixed and matched to provide I/O for various process sensors and actuators. Many standard configurations of each module are available, and, for added flexibility, factory laser trimmed custom units can be supplied. A wide zero suppression capability allows a user to map any portion of the input signal into the full ouput span permitting improved system resolution within a selected measurement range.

High Reliability: The 5B Series was designed to assure maximum reliability under real-world conditions. The modules are specified over the −25°C to +85°C temperature range. Each module is hard potted; there are no adjustment potentiometers which could introduce mechanical and human errors that impair system integrity. All field wired terminations, including sensor inputs, excitations and current outputs, are protected against continuous 240V rms line voltage. This prevents a fault from damaging the module, the backplane or other devices connected to the system. The modules also provide protection against high common-mode



voltages and are designed to meet the IEEE standard for transient voltage protection (472-1974: SWC). Gold plated pin and socket connections are used throughout the system to assure connection reliability.

High Performance: The high quality signal conditioning features ±0.05% calibration accuracy, nonlinearity of only ±0.02% span and chopper-based amplification which assures low drift (±1μV/°C) and excellent long-term stability. Low drift sensor excitation is provided when required, and the RTD and thermocouple modules provide an output which is linear with temperature.

High Noise Rejection: The 5B Series modules were designed to accurately process low level signals in electrically noisy environments by providing 1500V rms continuous transformer isolation which eliminates ground loops, protects against transients and solves common-mode voltage problems. To further preserve signal integrity, 160dB common-mode rejection, 60dB normal-mode rejection and excellent RFI/EMI immunity are provided.

Small Size: Each 5B Series module measures only 2.25″ × 2.25″ × 0.60″ resulting in space savings for both system designers and end users: each module occupies 1.35 square inches of board space and a 16-channel backplane occupies only 3.5 inches in a rack.

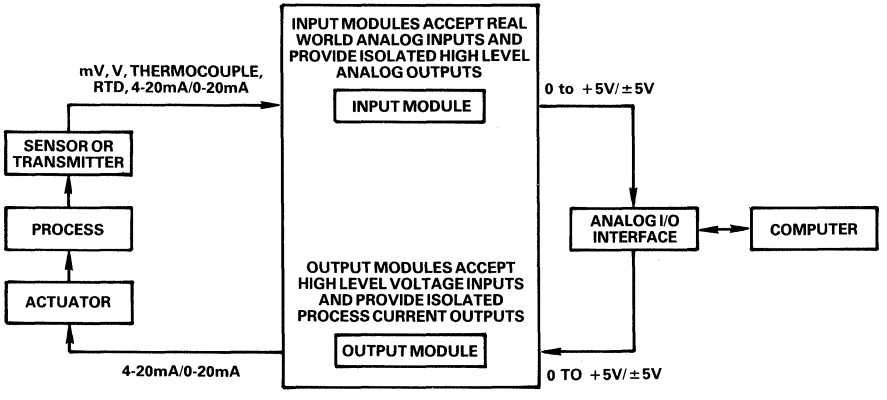
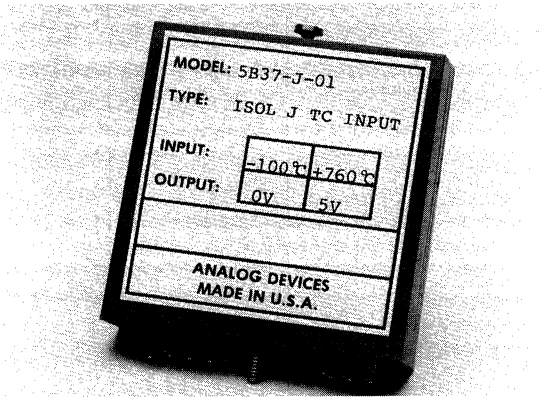


Figure 1. Functional Block Diagram of a General Measurement and Control Application Using the 5B Series

INPUT MODULE FEATURES

- **Variety of Signal Source Inputs**
  Sensors: Thermocouples, RTDs, and Strain Gages
  Millivolt and Voltage Sources
  4-20mA or 0-20mA Process Current Inputs
- **Mix and Match Input Capability**
- **High Level Voltage Output: ±5V or 0 to +5V**
- **High Accuracy: ±0.05%**
- **Low Drift: ±1μV/°C**
- **Reliable Transformer Isolation: 1500V rms CMV, 160dB CMR, Meets IEEE-STD 472: Transient Protection (SWC)**
- **Input Protection: 240V rms Continuous**
- **Factory Ranged and Trimmed, Custom Ranges Available**



GENERAL DESCRIPTION

The galvanically isolated 5B Series input modules are single channel, plug-in signal conditioners that provide input protection, amplification and filtering, series output switching, and a high level analog output. Key specifications include: 1500V rms isolation, accuracy of ±0.05%, ±0.02% span nonlinearity and low drift of ±1μV/°C. All modules operate from a single +5V supply with typical power consumption of 0.15W. The modules are hard potted.

The transfer function provided by each input module is:
Input – specified sensor measurement range
Output – 0 to +5V or ±5V.

Each 5B Series input module is available in a number of standard ranges, and special ranges can be factory configured. Analog Devices will provide a special function when a model 5B__ __ -CUSTOM is ordered with the desired range.

5B37 FUNCTIONAL DESCRIPTION

Figure 2 shows a functional diagram for a typical input module, the 5B37 thermocouple conditioner. The module provides cold junction compensation for the associated screw terminals as well as a bias current to give a predictable (upscale) response to an open thermocouple. Input protection allows safe operation even in the event of a 240V rms power line being connected to the signal terminals. (In modules designed to work with sensors requiring excitation, low drift sensor excitation is provided and is protected at the same level.)

A three-pole filter with a 4Hz cutoff provides 60dB of normal-mode rejection and CMR enhancement at 60Hz. One pole of this filter is located at the module input while the other two poles are in the output stage for optimum noise performance. A chopper-stabilized input amplifier provides all of the module's gain for ultralow drift. This amplifier operates on the input signal after subtraction of a stable, laser trimmed zero-suppression signal which sets the zero-scale input value. It is, therefore, possible to suppress a zero-scale input which is many times the total span to provide precise expanded scale measurements.

Signal isolation is provided by transformer coupling, using a proprietary modulation technique for exceptionally linear, stable performance at low cost. A demodulator on the output side of the signal transformer recovers the original signal, which is then filtered and buffered to provide a clean, low impedance output. A series output switch is included to eliminate the need for external multiplexing in many applications. This switch has a low output resistance (50Ω) and is controlled by an active-low enable input which is compatible with CMOS and LSTTL signals. In cases where the output switch is not used, such as single-channel and conventionally multiplexed applications, the enable input should be grounded to power common to turn on the switch.

A single +5V power supply input (as used for all 5B Series modules) operates a clock oscillator which drives power transformers for the input and output circuits. The input circuit is, of course, fully floating. In addition, the output section acts as a third floating port, eliminating many problems that might be created by ground loops and supply noise. The common-mode range of the output circuit is limited; however, output common must be kept within ±3V of power common, and a current path must exist between the two commons at some point for proper operation of the demodulator and output switch.

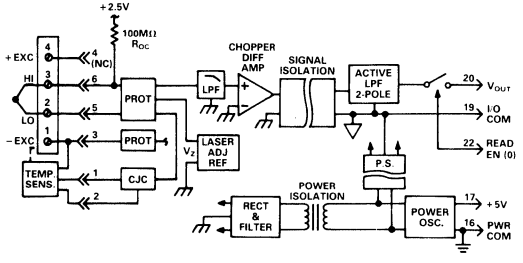


Figure 2. 5B37 Block Diagram

INPUT MODULE SPECIFICATIONS (typical @ +25°C and +5V power)

Model	5B30/5B31	5B32	5B34	5B37/5B47	5B40/5B41	5B38
Input Ranges	dc mV/dc V	Process Current	RTD	Thermocouple	Wideband dc mV/V	300Ω to 10kΩ Bridges
Output Ranges	±5V or 0 to +5V	0 to +5V	0 to +5V	0 to +5V	*	±5V
Accuracy[1]	±0.05% Span	*	*	*/0.10% Span	*	*
Nonlinearity	±0.02% Span	*	0.05% Span Conformity	*/NA	*	*
Stability vs. Ambient Temperature						
Input Offset	±1μV/°C/20μV/°C	±0.0025% Span/°C	±0.02°C/°C	±1μV/°C	±2μV/°C/±40μV/°C	*
Output Offset	±20μV/°C	*	*	*/NA	*	*
Span	±25ppm of rdg/°C	±35ppm of rdg/°C	±50ppm of rdg/°C	*	*	*
Common-Mode Voltage, Input to Output	1500V rms Continuous	*	*	*	*	*
Common-Mode Rejection@ 50Hz to 60Hz						
1kΩ Source Unbalance	160dB/150dB	*	*	*	100dB/90dB	100dB
Normal-Mode Rejection @ 50Hz or 60Hz	60dB	*	*	*	N/A	N/A
Differential Input Protection	240V rms Continuous	*	*	*	*	*
Output Resistance	50Ω	*	*	*	*	*
Voltage Output Protection	Continuous Short to Ground	*	*	*	*	*
Input Transient Protection	Meets IEEE-STD 472 (SWC)	*	*	*	*	*
Input Resistance	5MΩ/650kΩ	*	*	*	200MΩ/650kΩ	>20MΩ
Bandwidth	4Hz	*	*	*	10kHz	10kHz
Output Selection Time	20μs	*	*	*	*	*
Power Supply	+5V ±5%	*	*	*	*	*
Power Consumption	0.15W	*	*	*	*	1W
Size	2.25" × 2.25" × 0.6"	*	*	*	*	*
Environmental						
Temperature Range, Rated Performance	−25°C to +85°C	*	*	*	*	*
Temperature Range, Operation	−40°C to +85°C	*	*	*	*	*
Storage Temperature Range	−40°C to +85°C	*	*	*	*	*
Relative Humidity Conforms to	0 to 95% @ 60°C					
MIL Spec 202	Noncondensing	*	*	*	*	*
RFI Susceptibility	±0.5% Span Error, 5W					
	@ 400MHz @ 3'	*	*	*	*	*

NOTES
*Specifications same as 5B30.
[1]Accuracy specification includes the combined effects of repeatability, hysteresis and linearity and does not include sensor or signal source error.
This specification is for the 5B Series family and may not apply to all ranges of all modules. Consult the *5B Series User's Manual* for detailed specifications.
Specifications subject to change without notice.

Input Type/Span	Output	Model
dc, ±5mV to ±500mV	±5V	5B30, 5B40
dc, ±500mV to ±10V	±5V	5B31, 5B41
Process Current, 4-20mA or 0-20mA	0-5V	5B32
Thermocouple Types J, K, T, E, R, S, B	0-5V	5B37/5B47
Linearized Thermocouple Types J, K, T, E, R, S, B	0-5V	5B47
2, 3, 4 Wire RTDs – 100Ω Platinum, 10Ω Copper, 120Ω Nickel	0-5V	5B34
Full and Half Bridge Strain Gages	±5V	5B38

Table I. Input Selection

ISOLATED MILLIVOLT AND VOLTAGE INPUT MODELS 5B30 AND 5B31
Models 5B30 and 5B31 accept millivolt and voltage signals respectively and have a 4Hz bandwidth.

ISOLATED CURRENT INPUT MODEL 5B32
Model 5B32 accepts process current signals. A resistor is supplied to convert the signal current to a voltage, and, since that resistor cannot be protected against destruction in the event of inadvertent connection of the power line, it is provided in the form of a separate pluggable resistor carrier assembly. Extra current conversion resistors are available as accessories.

ISOLATED RTD INPUT MODEL 5B34
This RTD input module provides 3 wire lead resistance compensation and can be connected to 2, 3 or 4 wire RTDs. The lead resistance effect is ±0.02°C/Ω. It provides a low drift sensor excitation current of 0.25mA for the 5B34 or 5B34-N or 1.0mA for the 5B34-C and produces an output signal that is linear with temperature with a conformity error of ±0.05% of span and accuracy of ±0.05% of span.

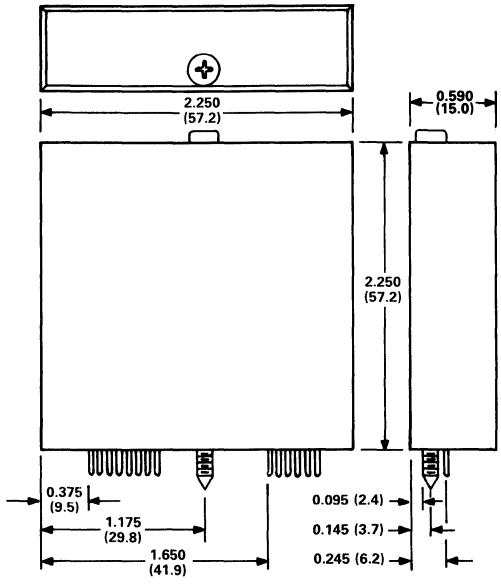
ISOLATED THERMOCOUPLE INPUT MODELS 5B37 AND 5B47
The isolated thermocouple models incorporate cold junction compensation circuitry which provides an accuracy of ±0.5°C over the +5°C to +45°C ambient temperature range. Open thermocouple detection (upscale) is also provided. Standard models are available for thermocouple types J, K, T, E, R, S and B. Model 5B47 provides a linearized 0-5V output signal for all thermocouple types.

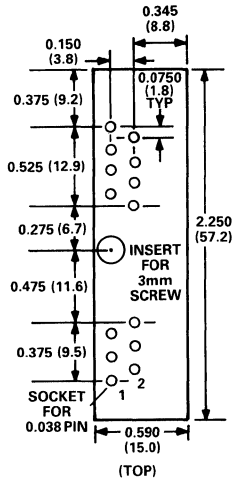
ISOLATED WIDEBAND MILLIVOLT AND VOLTAGE INPUT MODELS 5B40 AND 5B41
Models 5B40 and 5B41 accept millivolt and voltage signals respectively and have a 10kHz bandwidth for interface to dynamic signals.

ISOLATED WIDEBAND STRAIN GAGE INPUT MODEL 5B38
The 5B38 accepts signals from full and half bridge 300Ω to 10kΩ transducers. The 5B38 provides +10.0V excitation and provides a −5V to +5V output. This module features a 10kHz bandwidth.

5B SERIES MODULE OUTLINE

Dimensions shown in inches and (mm).





PIN DESIGNATIONS

WRITE EN (0)	23	22	READ EN (0)
RESERVED	21	20	V_{OUT}
I/O COM	19	18	V_{IN}
+5V	17	16	POWER COM
		6	IN HI
IN LO	5	4	+EXC
−EXC	3	2	SENSOR +
SENSOR −	1		

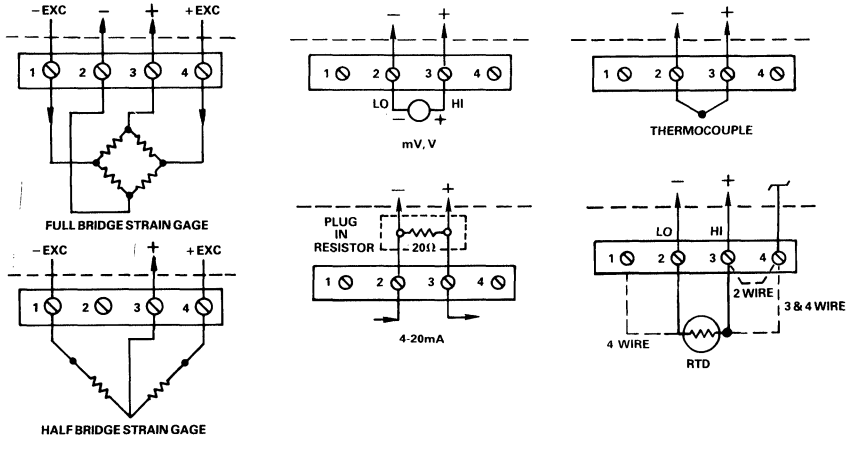


Figure 3. 5B Series Input Connections

OUTPUT MODULE FEATURES

- **Voltage Input Ranges: 0 to +5V or ±5V**
- **Process Current Output: 4-20mA or 0-20mA**
- **High Accuracy: ±0.05%**
- **Reliable Transformer Isolation: 1500V rms CMV, CMR=90dB**
- **Meets IEEE-STD 472: Transient Protection (SWC)**
- **Output Protection: 240V rms Continuous**

GENERAL DESCRIPTION

The 5B39 Current Output Module accepts a high level analog signal at its input and provides a 4-20mA or 0-20mA process current signal at its output. The module features high accuracy of ±0.05% and 1500V rms common-mode voltage isolation protection.

The transfer function provided by this module is:

Input – 0 to +5V or ±5V
Output – 4-20mA or 0-20mA.

To provide this range of functions four varieties of the 5B39 are available; unipolar or bipolar input and output range must be specified when ordering.

5B39 FUNCTIONAL DESCRIPTION

Figure 4 is a functional block diagram of the 5B39 current output module. The voltage input, usually from a digital-to-analog converter, is buffered and a quarter scale offset is added if a 4-20mA output is specified.

The signal is latched in a track-and-hold circuit. This track-and-hold allows 1 DAC to serve numerous output channels. The output droop rate is 80μA/s which corresponds to a refresh interval for 0.01% FS droop of 25ms. The track-and-hold is controlled by an active-low enable input which is compatible with CMOS and LSTTL signals. In conventional applications where one DAC is used per channel and the track-and-hold is not used, the enable input should be grounded to power common. This keeps the module in tracking mode.

The signal is sent through an isolation barrier to the current output (V-to-I converter) stage. Signal isolation is provided by transformer coupling using a proprietary modulation technique for linear, stable performance at low cost. A demodulator on the output side of the signal transformer recovers the original signal, which is then filtered and converted to a current output. Output protection allows safe operation even in the event of a 240V rms power line being connected to the signal terminals.

A single +5V supply powers a clock oscillator which drives power transformers for the input circuit and the output's high compliance, current loop supply. The output current loop is, of course, fully floating. In addition, the input section acts as a third floating port, eliminating many problems that might be created by ground loops and supply noise. The common-mode range of the input circuit is limited; however, input common must be kept with ±1V of power common, and a current path must exist between the two commons at some point for proper operation of the track-and-hold control input.

OUTPUT MODULE SPECIFICATIONS

(typical @ +25°C and +5V power)

Input Ranges	0 to +5V or ±5V
Output Ranges	4-20mA or 0-20mA
Load Resistance Range[1]	0 to 650Ω
Accuracy[2]	±0.05% Span
Nonlinearity	±0.02% Span
Stability vs. Ambient Temperature	
Zero	±0.5μA
Span	20ppm of Span/°C
Common-Mode Voltage, Output to Input and Power Supply	1500V rms Continuous
Common-Mode Rejection	90dB
Normal-Mode Output Protection	240V rms Continuous
Output Transient Protection	Meets IEEE-STD 472 (SWC)
Sample & Hold:	
Output Droop Rate	80μA/s
Acquisition Time	50μs
Over Range Capability	10%
Maximum Output Under Fault	26mA
Input Resistance	10MΩ
Bandwidth	400Hz
Power Supply	+5V dc ±5%
Power Consumption	0.85W (170mA)
Maximum Input Voltage Without Damage	±10V
Size	2.25" × 2.25" × 0.6"
Environmental	
Temperature Range, Rated Performance	−25°C to +85°C
Storage Temperature Range	−40°C to +85°C
Relative Humidity Conforms to MIL Spec 202	0 to 95% @ 60°C Noncondensing
RFI Susceptibility	±0.5% span error, 5W @ 400MHz @ 3 ft.

NOTES
[1]With a minimum power supply voltage of 4.95V, R_L can be up to 750Ω.
[2]Accuracy specification includes the combined effects of repeatability, hysteresis and linearity. Does not include signal source error.
Specifications subject to change without notice.

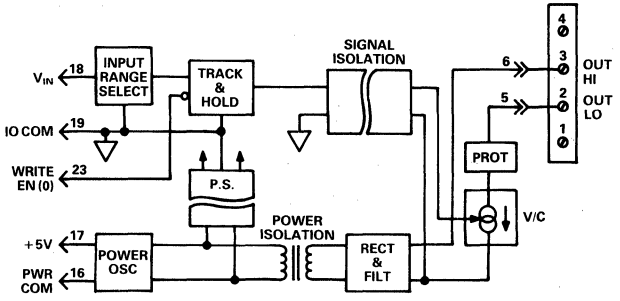


Figure 4. 5B39 Block Diagram

DESIGNER APPLICATION FEATURES

- **Module Pins Fit Widely Available Sockets**
- **Single Threaded Insert for Module Hold Down**
- **Cold Junction Compensation Sensors Available**
- **Input Modules Have Internal Series Output Switches**
- **Output Modules Have Track-and-Hold Inputs**

DESIGNER APPLICATION INFORMATION

The 5B Series was designed to facilitate integration by a system designer into his own circuit board or backplane. Only a single 3.0mm threaded insert is required for module hold down. Module pins are accommodated by widely available sockets, and temperature sensors for thermocouple cold junction compensation are available as one-piece precalibrated units.

The 5B Series was also designed to minimize system interface space and cost. Each input module has an internal series output switch which can be controlled by a TTL-compatible enable input eliminating the need for external multiplexers. Each output module has a track-and-hold input which allows a single digital-to-analog converter to serve numerous channels. In applications where it is desirable to do so, the module enable lines can be grounded, and the 5B Series input modules can be used with a conventional external mux and the output modules with a DAC per channel.

Ease of system application of these modules is enhanced by the fact that the output modules have enable and signal input pin assignments which do not coincide with the enable and signal output pins of the input modules, see Figure 5. This means that in a single mix-and-match backplane environment the reading of inputs and the writing and refreshing of outputs are completely independent and occur simultaneously. For example, the input system may dwell for a long time on a single channel to collect thousands of samples without having to interrupt the process to do an output refresh or set a new output value. Similarly, a "dumb" refresh circuit can be built which can maintain outputs without even knowing which channels have output modules; it can refresh all channels, and those that are really inputs will ignore the operation.

BASIC DESIGN GUIDELINES

Modules may be mounted in any position and will normally be placed next to the screw terminals connecting to the associated field wiring. The temperature sensor is only used by thermocouple modules, but it is normally installed in all channel locations in a "mix-and-match" application. This sensor must be physically close to the terminals where the thermocouple wire connects to copper. Because the low power dissipation of the 5B Series minimizes temperature gradients on the backplane, no special precautions are needed to get accurate temperature sensing. Provision must be made on each channel for the 5B32's current conversion resistor.

The width of the modules is intended to permit installation on 0.6" centers where required, but consideration must be given in each application to the required distance between backplane conductors where large interchannel voltages exist or where code requirements apply. The nature of the screw terminals used for field wiring will also factor in determining practical interchannel spacing.

The *5B Series User's Manual* includes an extensive discussion of system design issues. Design of backplanes which take full advantage of the 5B Series' capabilities by maintaining isolation is emphasized.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

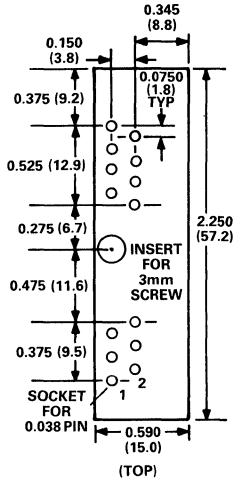


Figure 5. Module Footprint and Pinout

PIN DESIGNATIONS

WRITE EN (0)	23	22	READ EN (0)
RESERVED	21	20	V_{OUT}
I/O COM	19	18	V_{IN}
+5V	17	16	POWER COM
		6	IN HI
IN LO	5	4	+EXC
−EXC	3	2	SENSOR +
SENSOR −	1		

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BACKPLANE FUNCTIONAL DESCRIPTION

To address diverse applications, the 5B Series includes an expanding family of backplanes. Two 16-channel backplanes which can be mounted in a 19" × 3.5" panel space are available. Each channel has four screw terminals for field connections. These connections satisfy all transducer inputs, process current outputs, and provide transducer excitation when necessary. A cold junction sensor is supplied on each channel to accommodate thermocouple modules. A system interface connector provides high level voltage I/O for all channels. Both 5B Series backplanes require a +5V external power source. Other backplanes with integral power supplies are under development.

The 5B Series offers high density packaging to conserve mounting space and can be easily tailored to fit the user's needs. All modules feature universal pin out which assures interchangeability. The screw down design allows easy reconfiguration.

The 5B01, diagrammed in Figure 6, provides sixteen single ended input/output pins on the system connector. It is pin compatible with Analog Devices' 3B Series applications. (Note, however, that 5B Series modules provide a ±5V output swing rather than the ±10V swing provided by 3B Series modules).

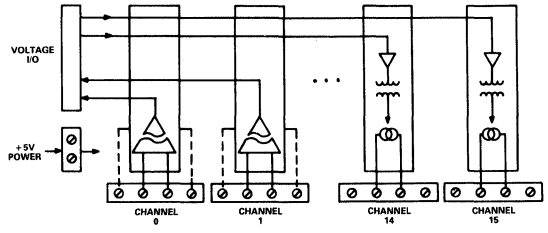


Figure 6. 5B01 Block Diagram

The 5B02, diagrammed in Figure 7, incorporates an input and an output bus which take advantage of the internal series output switches in the input modules and the track-and-holds in the output modules. Designers integrating the 5B02 into a measurement and control system do not need external multiplexers and can use a single digital to analog or analog to digital converter to serve numerous output or input channels.

For smaller applications, the 5B03 and 5B04 module sockets are available for one and two 5B Series modules, respectively. These module sockets may be clustered for groups of three or more signals, and they are DIN rail compatible using Phoenix Universal Module UM elements.

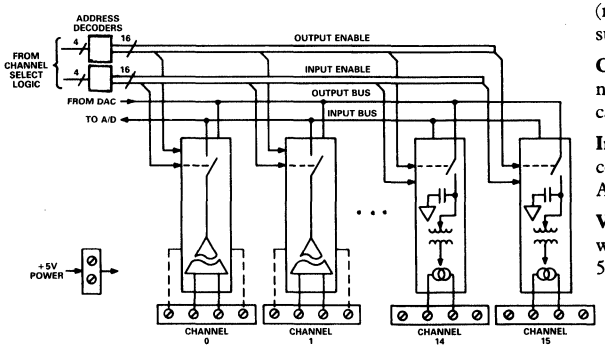


Figure 7. 5B02 Block Diagram

BACKPLANE SPECIFICATIONS

	5B01, 5B02	5B03/5B04
Channels	16	1, 2
External Power Requirement	+5V	*
Cold Junction Sensor	On Each Channel	*
Physical Size	3.5" × 17.4" 88.9mm × 442mm	4.25" × 1.37" 108mm × 34.7mm

*Same as 5B01, 5B02.

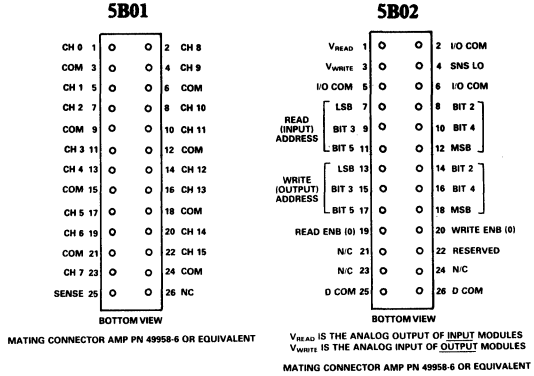


Figure 8. System Connector Pinout

ACCESSORIES

To ease the board design process for designers and to complete the 5B Series subsystem solution, the following accessories are available.

CJC Sensors. SIP temperature sensors are available to provide cold junction temperature measurement for thermocouple applications on user designed backplanes. These sensors are provided on each channel of all backplanes. Model number AC1361.

Current Conversion Resistors. Supplied with each 5B32 Current Input Module, a replacement pluggable resistor (20Ω) assembly. Model number AC1362.

Single Channel Socket. A single channel test socket with screw terminals and cold junction compensation for module evaluation. DIN rail compatible. Model number AC1360.

Rack Mount. A single piece metal chassis for mounting 5B Series backplanes in a 19" rack. Model number AC1363.

Power Supplies. Chassis mounted 1A (model number 955), 3A (model number 976) and 5A (model number 977) 5V power supplies are available.

Cables. A 2' (60cm) 26-pin cable with two connectors, model number AC1315. For daisy chaining 5B02 backplanes, a 26-pin cable with three connectors, model number CAB-01.

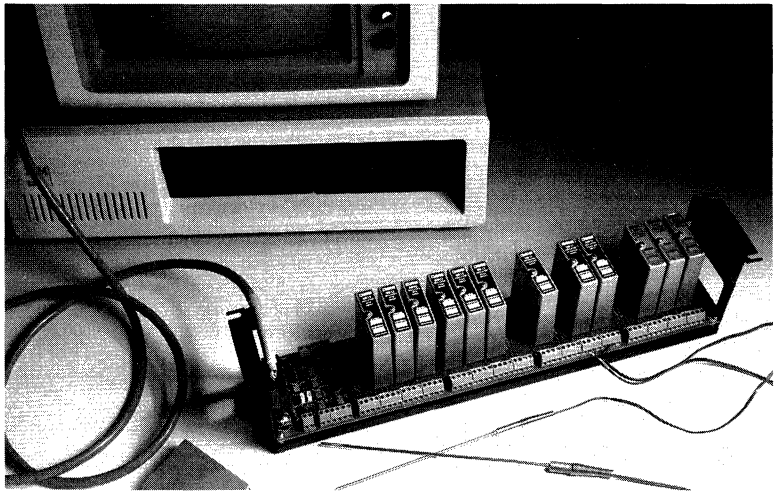
Interface Board. A universal interface board with a 26-pin connector in and 26 screw terminals out. Model number AC1324.

Voltage Switch Input Module. A nonisolated, unity gain module which allows a preconditioned signal to be connected into the 5B Series backplane. Model number AC1367.

ANALOG DEVICES

Configurable, Analog and Digital I/O Signal Conditioners

6B Series



ANALOG I/O FEATURES
- Sensor-to-Computer Conditioning and Digitizing
- Inputs/Outputs: Thermocouples, RTDs, Millivolt, Volt, Process Current
- Communication Interface: RS-485
  Backplane Option of RS-232 or RS-485
- Field Configurable via Software
  - 6B11: J, K, T, E, R, S and B Thermocouple, ±15 mV to ±5 V, 4-20 mA, 0-20 mA
  - 6B12: ±150 mV to ±50 V, 4-20 mA, 0-20 mA
  - 6B13: 100 Ω Pt, 120 Ω Ni and 10 Ω Cu
  - 6B21: 0-20 mA or 4-20 mA Output
- Configurable Parameters Stored in Module's EEPROM
- Autocalibrating, High Performance Integrating Converter, No Potentiometers Required
- Linearized Outputs in Engineering Units
- Input to Output Isolation: 1500 V rms
  Meets IEEE Standard for CMV Transient Voltage Protection (IEEE-STD 472)
- Small Package: 2.3″×3.1″×0.75″
  Modules Plug into Backplane for High Channel Density
- Specifications Valid Over the −25°C to +85°C Temperature Range

DIGITAL I/O FEATURES
- 24 Channels of Digital I/O
- Interfaces with Industry Standard Solid-State Relay Panels
- Readback for Output Monitoring
- Bit or Byte Addressable
- Communication Compatible with Analog I/O Backplanes

APPLICATIONS
Distributed Data Acquisition and Control
Test Stand Automation
Machine Monitoring
Material Testing
Energy Management

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This eight-page data summary contains key specifications to speed your selections of the proper solution for your application. Additional information on this product can be obtained by from your local sales office.

GENERAL DESCRIPTION

The 6B Series of modules and boards provide the hardware needed to implement a flexible, distributed monitoring and control application. By selecting only the modules and interfaces needed and connecting them via RS-485, the data acquisition and control strategy can be designed for optimum location of the I/O as well as minimizing sensor runs. The modularity and configurability of the 6B Series also makes them very cost effective.

Analog I/O

The 6B Series analog I/O modules represent a complete sensor-to-RS-485 solution. Each module performs signal conditioning, isolation, ranging, A/D or D/A conversion and digital communications. The sensors and inputs supported include thermocouples, RTDs, millivolt, volt and current signals. The output module can drive 0-20 mA or 4-20 mA interface valves or actuators. All calibration, address and linearizing parameters are stored in nonvolatile memory in the module.

Designed for industrial applications, the 6B Series modules incorporate transformer based isolation with automated surface mount manufacturing technology for increased reliability at low cost. These compact, rugged modules can be mixed and matched on a 16 channel backplane for high density, remote data acquisition and control.

Unlike conventional signal conditioners, each 6B module is a complete microcomputer based data acquisition system. A big advantage of an onboard microcontroller is the ability to reconfigure each module for various sensor types and input ranges. This reduces the number of different models that have to be used in a given application and carried in inventory. Also, by distributing the processing needs down to the node level, the host is off-loaded for supervisory and higher level control functions.

Interconnection between modules is via an RS-485 bidirectional serial bus standard. Communications between modules and host is in ASCII over an RS-232 or RS-485 link. Interface circuitry to convert RS-232 to RS-485 is built into the backplane. Baud rates are software programmable, and speeds up to 19.2 K baud can be selected.

All modules are fully encapsulated and identical in pinout and size (2.3″×3.1″×0.75″). The 6B Series is fully specified over the industrial temperature range of −25°C to +85°C.

Digital I/O

Digital signals can be monitored and controlled in a 6B Series RS-485 network by a 24-channel digital I/O interface board. This subsystem is completely compatible with the 6B Series protocol. Connections to 16 and 24 channel solid-state relay backplanes is via a 50 conductor ribbon cable. This allows interfacing with inputs and outputs from 4 to 240 V. Power control modules are also available that can switch up to three amps and come with a variety of ratings for low voltage dc to 280 V ac.

Similar to the analog modules, the digital I/O subsystem has an onboard microcontroller as well as nonvolatile memory. All the digital channels are addressable on a byte or bit-by-bit basis. In addition, the board can easily be configured for its address, baud rate and checksum status.

DESIGN FEATURES AND USER BENEFITS

Digitizing and Conditioning: By combining the signal conditioning and isolation functions with the A/D or D/A converter, the task of designing a computer based data acquisition system is greatly simplified. Since the RS-485 standard is a party line configuration, multiple 6B modules can be daisy chained onto the same bus.

Configurable: Each 6B Series module is configurable through software for many parameters including sensor type, output format, baud rate and checksum status. This can be very useful in pilot plant environments where the temperature ranges are not known beforehand. An additional benefit is that inventory can be greatly reduced for an application.

High Performance: The high quality signal conditioning combined with a precision A/D or D/A converter delivers ±0.05% accuracy including all temperature effects. For input modules, the auto-zeroing feature of the A/D converter assure excellent zero drift and long term stability.

Small Size and Remotely Mountable: A 16-channel backplane can be mounted on a 19″ rack and occupies only 3.5″ of rack space. Each backplane has a RS-485 interface on screw terminals and an optional converter to RS-232. This allows easy hookup to a computer over distances up to 4000 ft (RS-485).

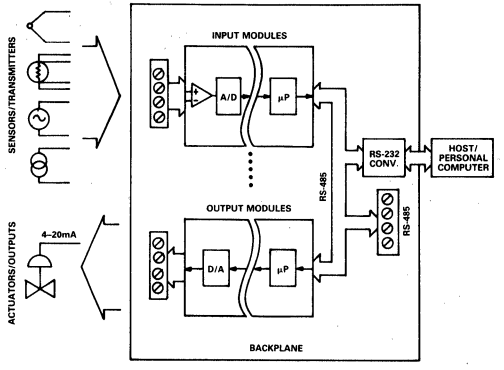


Figure 1. 6B Series Analog I/O Block Diagram

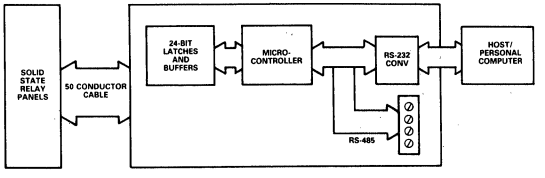
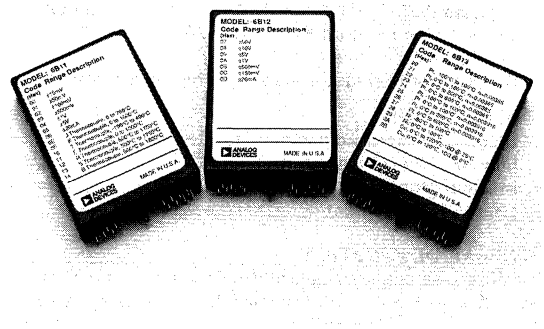


Figure 2. 6B Series Digital I/O Block Diagram

FEATURES

- **Variety of Signal Source Inputs**
  Sensors: Thermocouples and RTDs
  Millivolt and Voltage Sources
  4-20 mA and 0-20 mA Process Current Inputs
- **RS-485 Output**
- **Software Configurable for Ranges and Sensors**
- **All Configurable Parameters Stored in EEPROM**
- **Linearized Output in Engineering Units**
- **Mix and Match Input Capability**
- **Reliable Transformer Isolation: 1500 V CMV, 160 dB CMR, Meets IEEE-472: CMV Transient Protection**
- **Input Protection: 240 V rms Continuous**



DESCRIPTION

The 6B Series input modules cover all signal ranges from ±15 mV to ±50 V and all thermocouple and RTD types. The input signal is conditioned and scaled by the programmable gain amplifier and digitized by a 16-bit integrating converter under microprocessor control. The conversion rate is 9 samples/sec which gives a Nyquist bandwidth of 4.5 Hz.

The digitized value is passed serially across a magnetically isolated barrier (1500 V rms) and clocked in by a custom controller chip. The onboard microcontroller then converts the data into engineering units as determined by the channel parameters, i.e., whether the input signal was from a thermocouple, an RTD or a process current. In between conversions the microcontroller auto-zeros the offset and gain by monitoring the onboard temperature and reference drift. CJC compensation is also performed at this stage.

The 6B11 linearizes and compensates J, K, T, E, R, S and B thermocouples and digitizes millivolt and volt ranges from ±15 mV to ±5 V. The 6B12 interfaces with high level signals ranging from ±150 mV to ±50 V and the 6B13 linearizes 100 Ω Pt (alphas of 0.00385 and 0.003916), 120 Ω Ni RTDs and 10 Ω Cu RTDs.

The 6B Series modules have a simple master-slave relationship with the host and respond only when spoken to. Each module has a unique ID number stored in nonvolatile memory for addressing. The format is ASCII, and all standard baud rates up to 19.2 K baud are possible. Refer to the communication section of the data sheet for a summary of the command set.

Each 6B Series module can be recalibrated in the field or lab to an external reference. Similarly it can be reconfigured in the field for a different transfer function. All user configured parameters are stored in the nonvolatile memory (EEPROM) of the module.

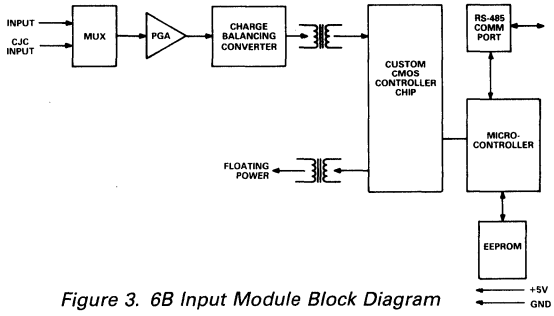


Figure 3. 6B Input Module Block Diagram

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FEATURES
Digitally Controlled Current Loop Output (12-Bits)
Programmable Output Ranges: 0-20 mA or 4-20 mA
Active Current Output; External Loop Power Supply Not Required
Common Mode Isolation: 1500 V
Meets IEEE-Std 472 for CMV Transient Protection
Normal Mode Output Protection: 240 V rms
Programmable Slew Rate Limiting
Output Monitoring and Readback for Fault Detection

APPLICATIONS
Distributed Data Acquisition and Control
Industrial Pilot Plant Control
Machine Control
Energy Management

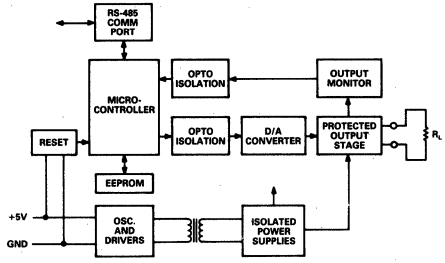

Figure 4. 6B21 Block Diagram

GENERAL DESCRIPTION

The 6B21 is an output module in the 6B Series that provides 0-20 mA or 4-20 mA process currents. It is electrically and mechanically compatible with the existing modules and backplanes. It takes a command from the host and converts it into an isolated process current suitable for interfacing with valves and actuators. The 6B21 was designed with fault protection as a key objective. In addition, the actual current flowing in the current loop can be read back by an on-board isolated A/D converter. The module will revert to a preset output stored in EEPROM in case of a brown-out.

The block diagram for the 6B21 is shown in Figure 4. An on-board microprocessor communicates with the host through a RS-485 port to exchange command and status information. An EEPROM is used to store calibration constants as well as configuration information. The microprocessor also controls the output DAC through an optically isolated serial interface. The D/A converter drives the current loop through a protected V/I converter.

The output monitor is a V/F converter whose frequency is proportional to the loop current. This variable signal frequency is fed back to the microprocessor through an optical isolator. The microprocessor then scales the frequency signal and returns the current readback data to the host. A DC/DC converter generates 25 V @ 25 mA to power the current loop and output circuitry from the +5 V power supply.

The 6B21 is encapsualted and packaged in a 2.3″×3.1″×0.75″ module. It is fully specified over the industrial (−25°C to +85°C) temperature range.

Output Module Specifications (typical @ 25°C and +5 V power unless otherwise noted)

Model	6B21
OUTPUT SPECIFICATIONS	
Range	0-20 mA + 10% Overange 4-20 mA +10% Overrange
Initial Accuracy	
Output Offset	±5 μA (±15 μA max)
Span	±0.02% FSR (±0.05% FSR max)
Accuracy vs. Temperature	
Output Offset TC	±1 μA/°C
Gain TC	±50 ppm/°C
Resolution	±0.02% FSR
Nonlinearity	±0.02% FSR
Bandwidth	100 samples/sec
Settling Time	1 ms to 0.1% FSR
Noise (100 Hz Bandwidth)	1 μA pk-pk
Load Resistor	0 to 750 Ω
Normal Mode Protection	240 V rms
Slew Rate	Step Response Plus 0.125 – 128 mA/sec in Eleven Binary Ranges
READBACK SPECIFICATIONS	
Initial Accuracy	
Output Offset	±100 μA
Span	±0.5% FSR
Accuracy vs. Temperature	
Output Offset TC	±5 μA/°C
Gain TC	±200 ppm/°C
Resolution	0.5% FSR
Nonlinearity	0.5% FSR
ISOLATION SPECIFICATIONS	
Common Mode Voltage Input to Output	1500 V rms
CMR @ 60 Hz	90 dB min
Transient Protection	IEEE-Std 472 (SWC)
POWER CONSUMPTION	1.2 W

NOTES
†See table for specific accuracy by range.
*Specifications same as 6B11.
Specifications subject to change without notice.

FEATURES
24 Channels of Digital I/O
Interfaces with Industry Standard Digital I/O Panels
High Output Current Capability
RS-232 Interface to Host (6B50-2)
RS-485 Interface to Other 6B Series Backplanes
Instruction Set Compatible with 6B Series
Readback for Output Monitoring

APPLICATIONS
Distributed Data Acquisition and Control
Industrial Pilot Plant Control
Machine Control
Energy Management

GENERAL DESCRIPTION

The 6B50 is a digital I/O board that is compatible with the 6B Series at the network level. It takes a command from the host and converts it into logic levels suitable for interfacing with industry standard optoisolated digital I/O panels. All I/O channels can be configured for input or output, using bit or byte addressing. In addition, the status of the port can be read back by the host to confirm the I/O configuration.

The block diagram for the 6B50 is shown below. An onboard microprocessor communicates with the host to exchange command and status information. An EEPROM is used to store system parameters (address, baud rate, etc.) as well as I/O configuration information. The microcontroller is interfaced to 8-bit latches and buffers for a maximum of 24 digital I/O channels. Each channel can be set individually as an input or output.

Similar to other 6B Series backplanes, the 6B50 is available with only an RS-485 interface (6B50-1), or with an additional RS-485/RS-232 converter (6B50-2). The 6B50 is a 3.47" × 6.5" open board that can be panel or rack mounted. It is fully specified over the commercial (0 to +70°C) temperature range.

INTERFACING

The 6B50 interfaces with industry standard single and quad solid-state relay modules. These are available for use with inputs and outputs from 4 V to 240 V. Power control modules can switch up to three amps and are available in a variety of ratings for low voltage dc to 280 V ac. Analog Devices also supplies 16- and 24-channel digital subsystems (DB-16 and DB-24) that interface with the 6B50 through a 50 conductor flat ribbon cable.

The single channel modules listed below plug into the DB-16 board.

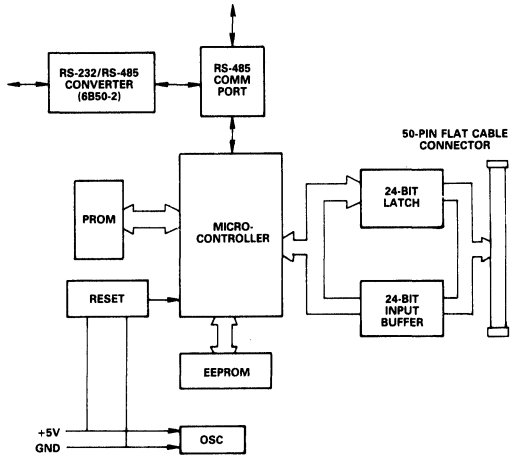

Figure 5. 6B50 Block Diagram

Model	Range
IA140A	AC Input, 140 V
IA280A	AC Input, 280 V
OA140A	AC Output, 140 V
OA280A	AC Output, 280 V
ID016	DC Input, 16 V
ID032	DC Input, 32 V
OD060	DC Output, 60 V
OD200	DC Output, 200 V

The quad modules listed below plug into the DB-24 board.

Model	Range
OA240QA	4 Channels Output, 120 V/240 V AC
OD60Q	4 Channels Output, 60 V DC
IA120QA	Input, 120 V AC
IA240QA	4 Channels Input, 240 V AC or DC
ID32Q	4 Channels Input, 10–32 V DC
ID16FQ	4 Channels Fast Input, 16 V DC
	50 μs Turn-on Time, 100 μs Turn-off Time

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BACKPLANES

Backplane Description

The 6B Series backplanes, combined with modules, provide a complete data acquisition system for end users. Each backplane incorporates screw terminals for field wiring inputs and outputs and cold junction compensation for thermocouple applications. The communication interface is RS-232 or RS-485 depending on the option.

For flexibility in application, one, four and sixteen channel backplanes are provided. These can be ordered either with the standard RS-485 interface, or with the optional RS-485 to RS-232 converter. The RS-232 interface allows easy hookup to most serial ports, while the standard RS-485 interface can be used for daisy chaining additional backplanes. The RS-485 interface can drive a twisted pair cable upto a maximum of 4000 ft.

BACKPLANE SPECIFICATIONS

	Channels	Interface[1]	Dimensions	Power Consumption
6BP01-1	1	RS-485	4.25″×1.37″	Passive
6BP01-2	1	RS-232	4.25″×2.85″	200 mA
6BP04-1	4	RS-485	3.47″×6.5″	200 mA
6BP04-2	4	RS-232	3.47″×6.5″	200 mA
6BP16-1	16	RS-485	3.47″×17.4″	200 mA
6BP16-2	16	RS-232	3.47″×17.4″	200 mA

[1]All backplanes have the RS-485 interface.

All 6B Series backplanes require a +5 V ± 5% power supply for the backplane circuitry as well as the modules. Backplanes and power supplies can be easily mounted on a rack mount kit described below.

SOFTWARE SUPPORT

Utility Disk: A test program to evaluate the 6B Series is part of the *6B Series User's Manual*. This allows for functionality of the modules to be tested on the bench as well as for programming all parameters, i.e., address, range, output format, checksum enable, etc.

Drivers: Drivers for popular software packages are also available as accessories. These drivers provide transparent access to the 6B Series modules from the serial port, and maintain a user friendly interface. Drivers are currently available for: Control EG*, LABTECH NOTEBOOK† and THE FIX‡.

LABTECH† ACQUIRE: Bundled with every 6B Series order at no extra charge, ACQUIRE is a basic software package that simplifies the data acquisition and recording process. It provides a menu driven software interface for the 6B Series and is very easy to learn. ACQUIRE features data logging and triggering options, as well as several ways to display data graphically.

***Control EG is a trademark of Quinn-Curtis.**
†LABTECH and LABTECH NOTEBOOK are registered trademarks of Laboratory Technologies Corporation.
‡THE FIX is a registered trademark of Intellution, Inc.

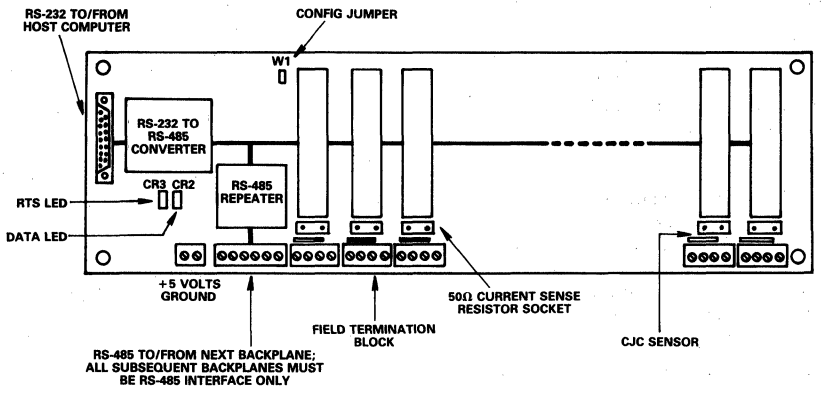


Figure 6. 6BP16-2 Block Diagram

Input Module Specifications (typical @ 25°C and +5 V power)

Model	6B11	6B12	6B13
Input Ranges	Thermocouple, mV, V, mA	mV, V, mA	Pt, Ni, Cu RTD
Output	RS-485	*	*
Accuracy†	±0.05% or better[1]	*	±0.03°C (Pt, Ni)
Zero Drift	±0.3 µV/°C	*	} Combined Effect: ±0.005°C/°C
Span Drift	±25 ppm/°C max	±50 ppm/°C max	
Common Mode Voltage, Input to Output	1500 V rms Continuous	*	*
Common Mode Rejection @ 50 Hz or 60 Hz 1 kΩ Source Imbalance	160 dB	108 dB	*
Normal Mode Rejection @ 50 Hz or 60 Hz	58 dB	56 dB	*
Differential Input Protection	240 V rms Continuous	*	*
Input Transient Protection (CMV)	IEEE-Std 472 (SWC)	*	*
Input Resistance	100 MΩ	1 MΩ	N/A
Bandwidth	4 Hz	*	*
Conversion Rate	9 samples/sec	*	*
Power Consumption	1.2 W	*	*

Range Accuracy (typical @ 25°C and +5 V power)

Hex Code	Range Description	Typical Accuracy	Maximum Error	Peak-to-Peak Noise	Units
	6B11				
00	±15 mV	±0.03	±0.06	±0.02	% of FS
01	±50 mV	±0.015	±0.04	±0.01	% of FS
02	±100 mV	±0.0055	±0.03	±0.005	% of FS
03	±500 mV	±0.005	±0.03	±0.002	% of FS
04	±1 V	±0.005	±0.03	±0.005	% of FS
05	±5 V	±0.005	±0.03	±0.0015	% of FS
06	±20 mA[1]	±0.008	±0.03	±0.005	% of FS
0E	J Thermocouple, 0 to 760°C	±0.4	±0.75	±0.14	°C
0F	K Thermocouple, 0 to 1000°C	±0.5	±0.75	±0.22	°C
10	T Thermocouple, −100°C to 400°C	±0.5	±0.75	±0.2	°C
11	E Thermocouple, 0 to 1000°C	±0.5	±0.75	±0.2	°C
12	R Thermocouple, 500°C to 1750°C	±0.63	±1.5	±0.3	°C
13	S Thermocouple, 500°C to 1750°C	±0.62	±1.5	±0.4	°C
14	B Thermocouple, 500°C to 1800°C	±1.2	±2.0	±0.7	°C
	6B12				
07	±50 V	±0.006	±0.03	±0.004	% of FS
08	±10 V	±0.006	±0.03	±0.005	% of FS
09	±5 V	±0.006	±0.03	±0.006	% of FS
0A	±1 V	±0.006	±0.03	±0.007	% of FS
0B	±500 mV	±0.01	±0.04	±0.008	% of FS
0C	±150 mV	±0.03	±0.06	±0.02	% of FS
0D	±20 mA[1]	±0.006	±0.03	±0.007	% of FS
	6B13				
20	Pt, −100°C to +100°C, α = 0.00385	0.02	0.15	0.03	°C
21	Pt, 0°C to +100°C, α = 0.00385	0.03	0.15	0.04	°C
22	Pt, 0°C to +200°C, α = 0.00385	0.03	0.15	0.04	°C
23	Pt, 0°C to +600°C, α = 0.00385	0.05	0.15	0.05	°C
24	Pt, −100°C to +100°C, α = 0.003916	0.03	0.15	0.03	°C
25	Pt, 0°C to +100°C, α = 0.003916	0.05	0.15	0.03	°C
26	Pt, 0°C to +200°C, α = 0.003916	0.03	0.15	0.04	°C
27	Pt, 0°C to +600°C, α = 0.003916	0.04	0.15	0.05	°C
28	Ni, −80°C to +100°C	0.05	0.15	0.02	°C
29	Ni, 0°C to +100°C	0.03	0.15	0.02	°C
2A	Cu, 0°C to +120°C, =0 Ω @ 25°C	0.13	0.5	0.04	°C
2B	Cu, 0°C to +120°C, 10 Ω @ 25°C	0.11	0.5	0.04	°C

NOTE
[1]Excluding error contribution from current sense resistor.

Common Module Specifications

POWER SUPPLY	
Voltage, Operating	+5 V ± 5%
ENVIRONMENTAL	
Temperature Range	
Rated Performance	−25°C to +85°C
Storage	−40°C to +85°C
Relative Humidity (MIL Spec 202)	0 to 95% @ 60°C

Digital I/O Specifications (typical @ 25°C and +5 V power unless otherwise noted)

Model	6B50
DIGITAL I/O	
Number of I/O	24 (Configurable for Input or Output)
I/O Circuit Configuration	Open Collector Outputs with 47 kΩ Pullups to +5 V
Digital Inputs	
High Level Input	3.5 V min, 5.25 V max
Low Level Input	0.8 V max
Digital Outputs	
High Level Output Current	50 µA @ 5 V
Low Level Output Current	100 mA @ 1.1 V
High Level Output Voltage	5.25 V max
COMMUNICATIONS	
RS-232C	
Baud Rates	300, 600, 1200, 2400, 4800, 9600, 19.2 K
Maximum Distance	50 ft
RS-485	
Baud Rates	300, 600, 1200, 2400, 4800, 9600, 19.2 K
Maximum Distance	4000 ft
POWER SUPPLY	
Voltage, Operating	+5 V ± 5%
Current, Quiescent	225 mA[1]
SIZE	3.47" × 6.5" (90.68 mm x 165.1 mm)
ENVIRONMENTAL	
Temperature Range	
Rated Performance	0 to +70°C
Storage	−40°C to +85°C
Relative Humidity	0 to 90% Noncondensing

NOTE
[1]Excluding load current.
Specifications subject to change without notice.

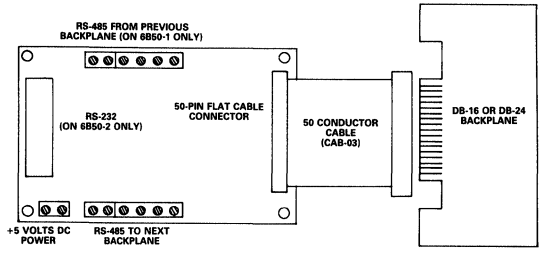


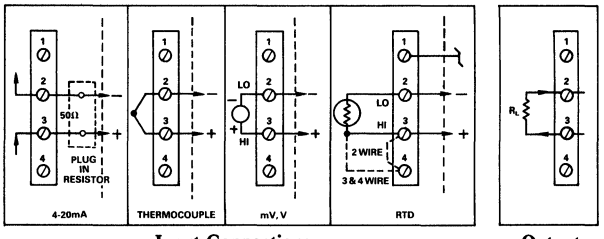
Figure 7. 6B50 Digital I/O Board Block Diagram

Input Module Pin Designations

N/C	25	24	XCV+
XCV−	23	22	RTS+
RTS−	21	20	+5V PWR
PWR COM	19	18	CONFIG
IN LO	7	6	IN HI
−EXC	5	4	+EXC
CJC EXC	3	2	+SNS
−SNS	1		

Output Module Pin Designations

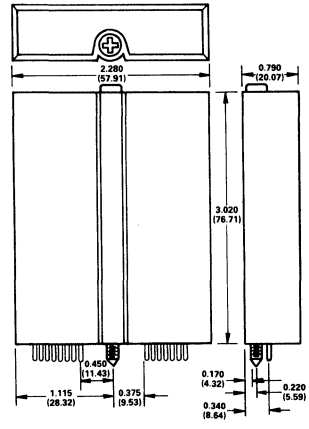
N/C	25	24	XCV+
XCV−	23	22	RTS+
RTS−	21	20	+5V PWR
PWR COM	19	18	CONFIG
LO	7	6	HI
N/C	5	4	N/C
N/C	3	2	N/C
N/C	1		



Input Connections **Output Connections**

Figure 8. 6B Series Connections

6B Module Outline



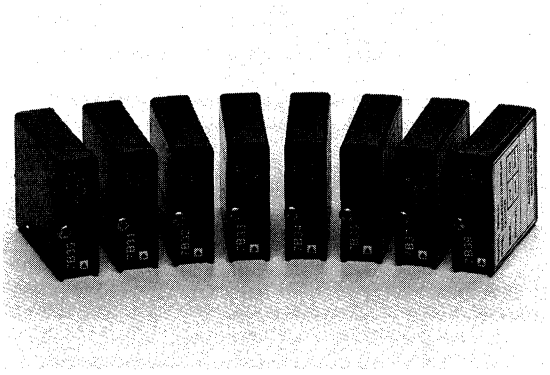
ANALOG DEVICES

Low Cost, Modular Process Control Signal Conditioners

7B Series

FEATURES

- **Accepts Process Control Input Signals: Thermocouples, RTDs, Current, Millivolt and Voltage Inputs**
- **Powered Current Input Provides Isolated +24 V for a Transmitter**
- **Analog Current Output Module**
- **Complete Signal Conditioning Function: 120 V RMS Field Wiring Protection, Filtering, Amplification, 1500 V RMS Transformer Based Isolation**
- **Operates From +14 V DC to +35 V DC Power**
- **Factory Calibrated Accuracy**
- **Mix and Match Modularity**
- **Custom Ranges Available**



GENERAL DESCRIPTION

The 7B Series of signal conditioners represents a new level of price versus performance for the process control industry. These modular, plug-in conditioners accept inputs from the most common process control transducers and signals and provide a high level isolated output voltage. Galvanic isolation of 1500 volts rms is achieved by transformer based circuitry. Both the signal path and the power supply are isolated enabling true channel-to-channel isolation.

The modules accept a nominal power supply input of +24 volts dc with a range of +14 volts to +35 volts. The small size of 1.7″ × 2.1″ × 0.60″ allows large point count applications without taking up a lot of space. All specifications are valid over −40°C to +85°C.

Isolated input modules are available for J, K, T, E, R, S and B thermocouples; platinum, copper and nickel RTDs; and current, voltage and millivolt signals. The isolated powered loop input module provides +24 volts for a transmitter and accepts a 4–20 mA current input. All input modules provide a high level 1–5 volt output signal, with additional output ranges available. An isolated current output module provides a 0–20 mA or 4–20 mA signal to the field for control applications. A compact sensor for cold junction compensation reduces the space required on the backplane.

A variety of backplanes are available to provide a complete solution for the end user or systems integrator. Each backplane contains screw terminals for the field wiring connections. A cold junction compensation thermistor is installed under the terminal blocks on each channel. Only the thermocouple input module receives this input signal. This flexibility allows any module type, input or output, to be used in any channel on the backplane. A 25-pin D style connector is used for system hookup. Provisions are made for redundant power connections as well as an LED to indicate power on. Nineteen-inch rack mount kits are available.

APPLICATIONS

The 7B Series of signal conditioners is designed to provide an easy and cost effective solution to interfacing to transducers in process monitoring and control systems. These modules can be designed into a system as a component or used with Analog Devices' backplanes to provide a higher level solution. The +24 volt power supply requirement and a simple pinout eases the integration of the 7B Series into a user designed backplane. Applications requiring monitoring and control of large numbers of analog signals are a perfect fit for the 7B Series.

SPECIFICATIONS

Input Modules (All specifications are at +25°C, +24 V power.)

Model	7B30/7B31	7B32	7B33	7B34	7B35	7B37
Input Ranges	DC mV/DC V	Current	dc V	RTD	Current	Thermocouples
Output Ranges	1–5 V, 0–10 V	1–5 V, 2–10 V	1–5 V, 2–10 V	*	1–5 V, 2–10 V	*
Accuracy[1]	±0.1% Span max	*	*	±0.13%–±0.25% Span max[2]	*	±0.10%–±0.15% Span Max[2]
Nonlinearity	±0.02% max	±0.025%	*	±0.05% Span Conformance	±0.025%	*
Stability vs. Ambient Temperature						
Input Offset (max)	±1 μV/°C / ±5 μV/°C	±35 ppm/°C	±35 ppm/°C	±0.02°C/°C	±25 ppm/°C	*
Output Offset	±10 ppm/°C	*	*	*	*	*
Span	60 ppm/°C max/80 ppm/°C max	*	*	*	*	*
CMV, Input to Output	1500 V RMS Continuous	*	*	*	*	*
CMR @ 50 or 60 Hz, 1 kΩ, Source Unbalance	140 dB/120 dB min	105 dB min	105 dB min	160 dB min	105 dB min	160 dB min
NMR @ 60 Hz	60 dB min	NA	NA	*	NA	*
NMR @ 50 Hz	56 dB min	NA	NA	*	NA	*
Input Protection, Continuous	120 V AC Continuous	*	*	*	*	*
Voltage Output Protection	Continuous Short to Gnd	*	*	*	*	*
Input Transient Protection	Meets IEEE-STD472	*	*	*	*	*
Input Resistance	10 MΩ/100 kΩ	250 Ω	1 MΩ min	NA	250 Ω	10 MΩ min
Bandwidth	3 Hz	100 Hz	100 Hz	3 Hz	100 Hz	3 Hz
Response Time, 0 to 90%	200 ms max	10 ms max	10 ms max	500 ms max	10 ms max	200 ms max
Minimum Output Voltage	−1.2 V[3]/−30 V[4]	*	*	*	*	*
Maximum Output Voltage	+7.4 V[3]/+13.5 V[4]	*	*	*	*	*
Open Input Response	NA	Downscale	Downscale	Upscale	Downscale	Upscale
Open Input Detection Time	NA	2 s max	2 s max	10 s max	2 s max	10 s max
Power Supply	+14 V to +35 V	*	*	*	+18 V to +30 V	*
Power Supply Sensitivity	±0.01% Span/V, max	*	*	*	±0.025%	*
Power Consumption	25 mA max	*	*	*	60 mA max	*
Size (H)(W)(D)	2.13″×1.705″×0.605″, max	*	*	*	*	
Environmental						
Rated Temperature Range	−40°C to +85°C	*	*	*	*	*
Operating Temperature Range	−40°C to +85°C	*	*	*	*	*
Storage Temperature Range	−40°C to +85°C	*	*	*	*	*
Relative Humidity	0 to 90%, Noncondensing	*	*	*	*	*

NOTES
[1]Accuracy specification includes the combined effects of repeatability, hysteresis and linearity and does not include sensor or signal source error.
[2]Accuracy specification is dependent on input range, consult factory.
[3]1–5 V output.
[4]0–10 V output.

*Specifications same as 7B30.

Specifications subject to change without notice.

Input Type / Span		Output	Model
VOLTAGE			
mV DC:	0–10 mV, 0–50 mV, 0–100 mV	1–5 V, 0–10 V	7B30
V DC:	0–1 V, 0–5 V, 1–5 V	1–5 V, 0–10 V	7B30
V DC:	0–10 V	1–5 V, 0–10 V	7B31
V:	1–5 V	1–5 V	7B33
PROCESS CURRENT			
4–20 mA		1–5 V	7B32
4–20 mA, External 250 Ω Resistor		1–5 V	7B33
0–20 mA dc/4–20 mA dc, External 250 ΩResistor		1–5 V, 0–10 V	7B30
4–20 mA Powered Loop Current		1–5 V	7B35
RTDs			
100 Ω Pt, 10 Ω Cu, 120 Ω Ni		1–5 V, 0–10 V	7B34
THERMOCOUPLES			
J, K, T, E, R, S, B		1–5 V, 0–10 V	7B37

Table I. Input Selection

PIN DESIGNATIONS

I/O & POWER COM	5
V_{OUT}	4
+24 VOLTS	3
INPUT LOW	2
INPUT HIGH	1
SENSOR	0

NOTE
PIN 0 IS ONLY USED ON THE 7B34 RTD INPUT AND THE 7B37 THERMOCOUPLE INPUT MODULES.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Output Module (All specifications are at +25°C ±5°C, +24 V power.)

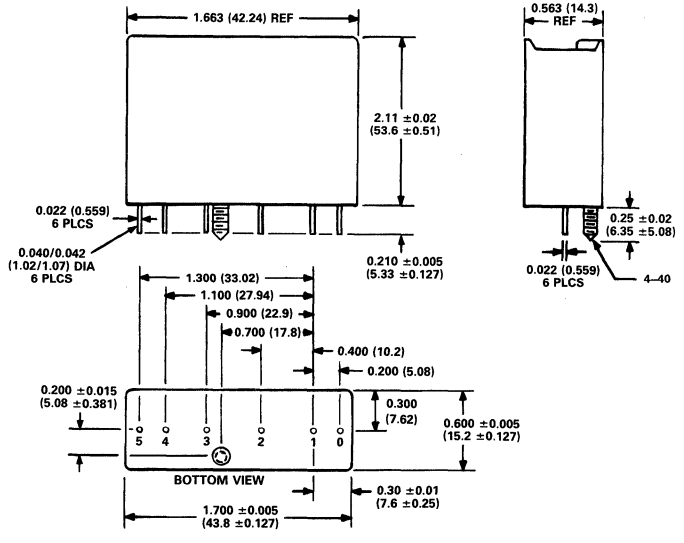
Model	7B39
Input Range	1–5 V, 0–10 V
Output Range	4–20 mA, 0–20 mA
Load Resistance Range	0 to 750 Ω
Accuracy[1]	±0.1% max
Nonlinearity	±0.02% max
Stability vs. Ambient Temperature	±0.01%/°C max
CMV, Input To Output	1500 V RMS Continuous
Normal Mode Output Protection	120 V RMS Continuous
Output Transient Protection	Meets IEEE-STD472 (SWC)
Input Resistance	10 MΩ
Open Input Response	Downscale
Open Input Detection Time	2 s max
Response Time 0 to 90%	10 ms max
Output Range	
Minimum Output Current	0 mA
Maximum Output Current	32 mA
Bandwidth	100 Hz
Power Supply	+14 V dc to +35 V dc
Power Supply Sensitivity	±0.012%/V
Power Consumption	65 mA max
Maximum Input Voltage	
Size	2.13″×1.705″×0.605″ max
Environmental	
Rated Temperature Range	−40°C to +85°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +85°C
Relative Humidity	0 to 90% Noncondensing

NOTES
[1]Accuracy specification includes the combined effects of repeatability, hysteresis and linearity. Does not include signal source error.
Specifications subject to change without notice.

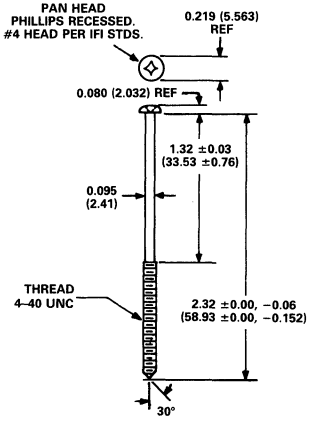
7B SERIES MODULE OUTLINE

Dimensions shown in inches and (mm).

Module



Fastening Screw



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This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SYSTEM DESIGN FEATURES

- **Power Supply Range of +14 Volts to +35 Volts**
- **Single Threaded Insert for Module Hold Down**
- **Accepts Thermistor for Cold Junction Compensation**

SYSTEM DESIGN INFORMATION

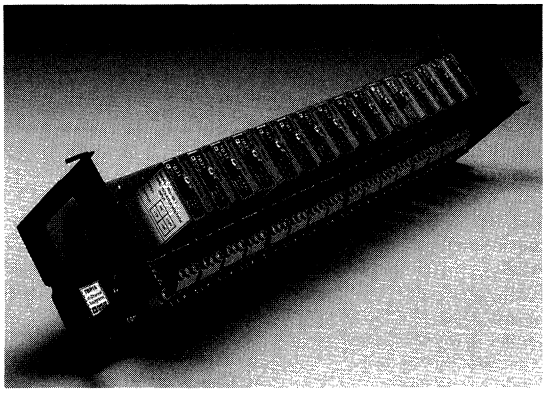
The 7B Series was designed to be easily integrated into a process control system. The pins and the hold down screw fit into the same sockets as those used with the solid-state relays. The thermistor recommended for cold junction compensation is commercially available. The pins are 0.040″ in diameter and 0.210″ extending from the bottom of the case. The millivolt, volt and current input modules and the current output module have five pins and the thermocouple and RTD modules have six pins each. The RTD module requires three field wiring connections, all others need two.

BASIC DESIGN GUIDELINES

Modules may be mounted in any position and will normally be placed next to the screw terminals connecting to the associated field wiring. The temperature sensor is used only by the thermocouple modules; but if it is installed in each channel, then modules can be inserted in any channel depending upon the application. The operation of the non-thermocouple modules is not affected by the temperature sensor. This sensor must be physically close to the terminals where the thermocouple wire connects to copper. Because the low power dissipation of the 7B Series modules minimizes temperature gradients on the backplane, no special precautions are needed to get accurate temperature sensing.

Provisions must be made for a current sense resistor if there are current inputs and the 7B32 with the internal sense resistor is not being used. The the screw terminals for the field wiring connections are large enough the resistor can be connected directly on the terminals. Provisions can also be made to use the pluggable current sense resistor offered as an accessory.

The width of the modules permits installation on 0.625″ centers where required, but consideration must be given in each application to the required distance between backplane conductors where large interchannel voltages exist or code requirements apply. The isolation specification may be downrated due to the module spacings.



MODULE DESCRIPTIONS

7B30 and 7B31: Isolated Millivolt and Voltage Input

The 7B30 and 7B31 accept millivolt and volt signals, respectively. They each provide an isolated +1 to +5 volt or 0 to +10 volt output signal. Both modules have standard ranges from ±10m volts up to ±10 V or a custom range can be specified within these limits. The 7B31 can be used with the AC1372 current sense resistor to provide a current input module with a 0 to +10 volt output. These modules have a 3 Hz bandwidth.

Figure 1 shows a block diagram of the 7B30/7B31. The high and low input terminals are protected for up to 120 V rms. The high level signals of the 7B31 are attenuated and both modules have a one pole low pass filter on the input. A low drift amplifier provides the gain of the module. The signal is modulated and passed across a transformer supplying 1500 volts of isolation. The signal is then demodulated so the original signal is recovered. The two pole output filter and buffer ensure a clean low noise signal on the output. The power supply section of the module is also isolated allowing channel-to-channel isolation.

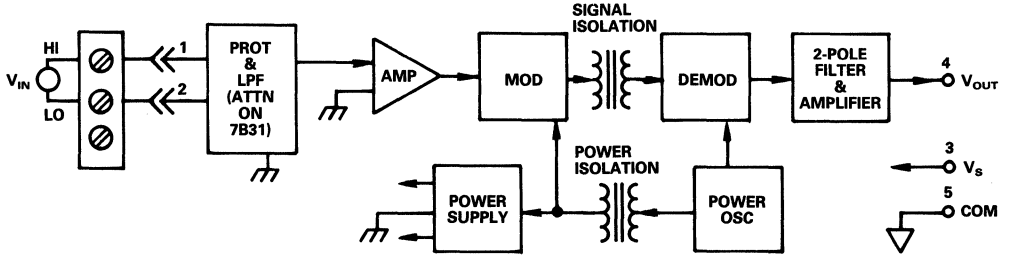


Figure 1. 7B30/7B31 Block Diagram

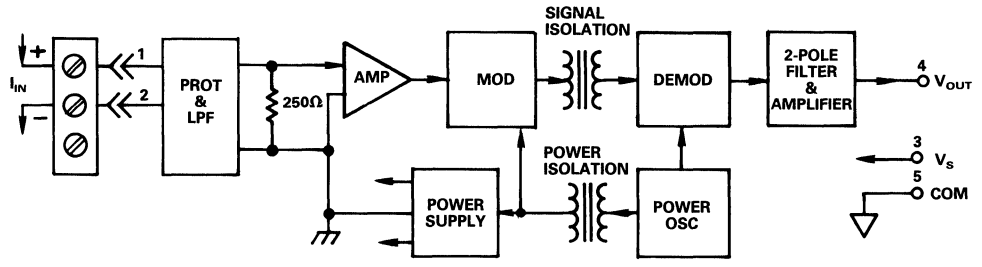


Figure 2. 7B32 Block Diagram

7B32: Isolated Current Input

The 7B32 accepts a 4–20 mA current input and provides a +1 to +5 volt output. The 7B32 incorporates an internal protected current conversion resistor allowing the process current to be directly connected to the module without compromising system integrity. The internal resistor allows the module calibration to include the current sense resistor. Downscale open input detection and a bandwidth of 100 Hz is featured.

Figure 2 is a functional block diagram of the 7B32. The module features input protection of 120 V rms in addition to a low pass filter on the input. The input current is converted to a voltage signal and then modulated to pass across the transformer barrier. The isolated signal is then demodulated and buffered and filtered to provide a clean output voltage proportional to the input current.

The 7B32 is available with a +1 to +5 volt output. If a current input module with a 0 to +10 volt output is desired, a standard 7B31 with a +1 to + 5 volt input and a 250 Ω current conversion resistor (model AC1372) can be used. In applications where an external current sense resistor is preferred, the 7B33 voltage input module and the current sense resistor can be used to allow a +1 to +5 volt output.

7B33: Isolated High Level Voltage Input

The 7B33 accepts a +1 to +5 volt input signal and provides a +1 to +5 volt output with a signal bandwidth of 100 Hz.

Figure 3 is a functional block diagram of the 7B33. The two input terminals are protected for the hookup of 120 V rms. A 2.2 MΩ resistor on the input provides downscale open input detection within 2 seconds of a break on the input. A low pass filter combined with a low drift amplifier insure a clean signal into the modulator stage. The signal is modulated and passed across the transformer to provide 1500 V rms common mode isolation. The signal is recovered by the demodulator and fed through a 2-pole filter and buffered to provide a clean, low impedance output signal.

The +24 volt power input to the 7B33 provides power for the output stage and is passed across a second transformer in order to provide isolated power for the input circuitry. This ensures channel-to-channel isolation of the modules.

The 7B33 is available with a +1 to +5 volt input and a +1 to +5 volt output, this module has no provisions for gain or attenuation or custom ranges. The 7B30 and 7B31 mV and V input modules should be used for custom ranges or different input or output ranges.

The 7B33 can be used with a 250 Ω resistor as a current input module. This external current sense resistor allows the current loop to be maintained if the module has to be removed.

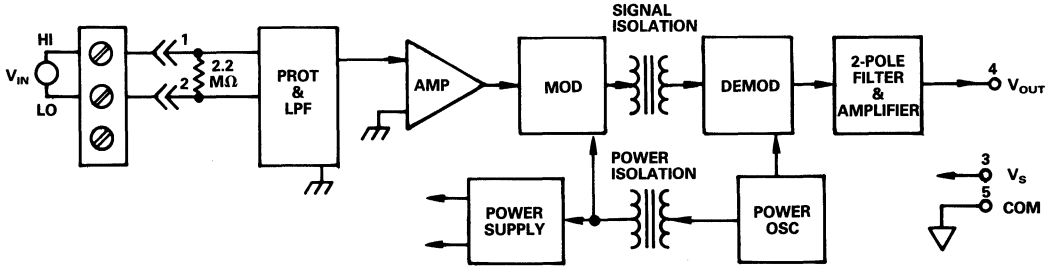


Figure 3. 7B33 Block Diagram

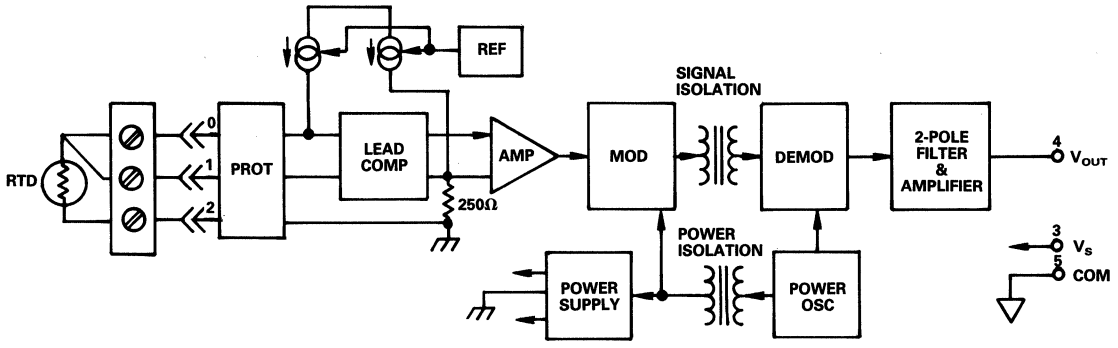


Figure 4. 7B34 Functional Block Diagram

7B34: Isolated Linearized RTD Input

The 7B34 accepts inputs from 100 Ω platinum (DIN and JIS alphas), 120 Ω nickel and 10Ω copper RTDs and provides a linear voltage output. The 7B34 is available with a +1 to +5 volt or a 0 to +10 volt output range, all ranges feature a 3 Hz bandwidth. Three wire lead compensation is provided, and 2, 3 or 4 wire RTDs may be used. Upscale open input protection is provided on the signal leads.

Figure 4 is a functional block diagram of the 7B34. The 7B34 uses three pins for the RTD input, two for the sensor and a third for the excitation. All three input terminals are protected for up to 120 V rms. Low drift sensor excitation current of 0.25 mA is provided for platinum and nickel RTDs and 1.0 mA current for copper RTDs. A current source identical to the excitation current source is connected to the third lead of the RTD to cancel the effects of lead resistance. This current also flows through Rz, chosen to represent the RTD value of the zero output to voltage of the module. This signal is then amplified and modulated to be passed across the isolation barrier. The original signal is recovered in the demodulator stage. A two pole filter and a buffer ensure a clean low noise output voltage is provided.

The +24 volt power is also isolated by transformer coupling to provide channel-to-channel isolation and signal to power isolation. The 7B34 will accept power supply inputs from +14 volts to +35 volts.

7B35: Isolated Powered Current Loop Input

The 7B35 accepts a 4–20 mA current input and provides the loop power for a transmitter. This module features downscale open input detection and a bandwidth of 100 Hz. The module incorporates a protected 250 Ω current sense resistor eliminating the need for external resistors. A +1 to +5 volt output range is standard.

The functional block diagram is shown in Figure 5. The two input terminals are protected for 120 V rms. A one-pole input filter eliminates high frequency noise. A 250 Ω current conversion resistor converts the signal to a voltage to be amplified. The signal is then modulated and passed across the galvanic isolation of the transformer to provide 1500 volts of common mode isolation. The demodulator reclaims the original signal, which is filtered and buffered to give a clean, low noise output voltage.

The power supply for the module is also isolated and the module will accept power inputs from +18 volts to +30 volts.

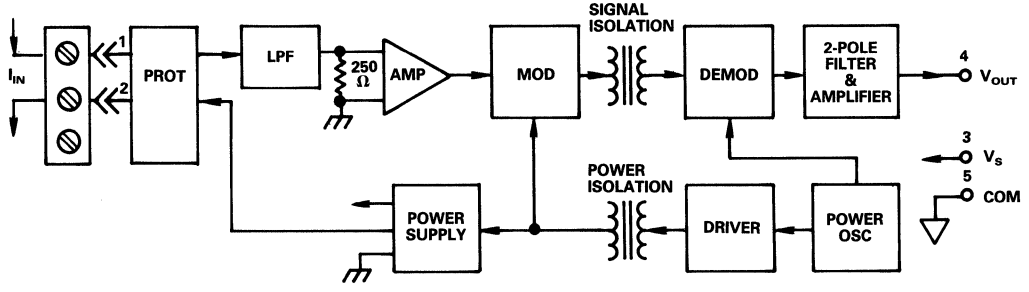


Figure 5. 7B35 Functional Block Diagram

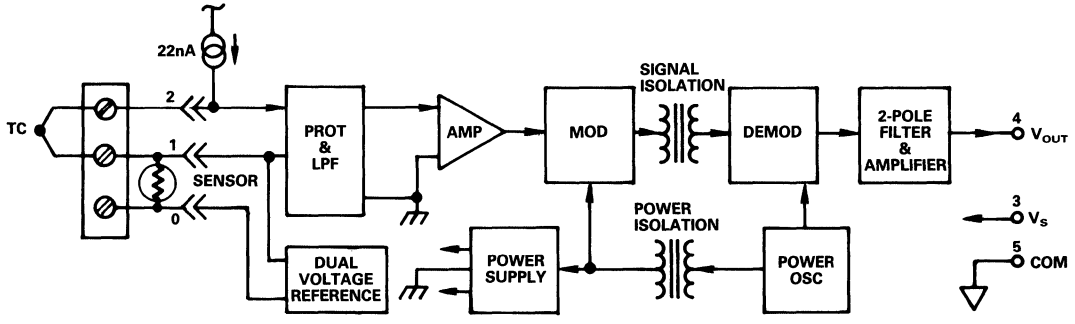


Figure 6. 7B37 Block Diagram

7B37: Isolated Thermocouple Input

The 7B37 accepts inputs from J, K, T, E, R, S and B type thermocouples and provides a nonlinearized +1 to +5 volt or 0 to +10 volt output. Upscale open thermocouple detection is featured within 10 seconds of a break in in the thermocouple wiring. This module is designed to accept cold junction compensation from a thermistor mounted on the backplane adjacent to the field wiring terminals.

There are standard ranges available for each thermocouple type and custom ranging is available to map a specific input range to the full output span.

Figure 6 is a functional block diagram of the 7B37. In order to accommodate the CJC input, the 7B37 uses three input pins. Cold junction compensation circuitry corrects for the effects of connecting the thermocouple wires to the screw terminals on the backplane. Upscale open input detection is provided through the 22 nA current source. The input terminals are protected for the inadvertent connection of 120 V rms. A one-pole low pass filter on the input rejects high frequency noise. The input signal is offset to set the zero scale input value. A low drift amplifier provides a stable signal into the modulator; 1500 volt signal isolation is provided by transformer coupling. A demodulator on the output side recovers the original, which is buffered and filtered to provide a clean output signal.

7B39: Isolated Current Output

This module accepts a +1 to +5 volt or 0 to +10 volt input from the user's system and provides a galvanically isolated 4–20 mA or 0–20 mA current output to the field wiring capable of driving a 750 Ω load at +24 volt power. The bandwidth is 100 Hz.

The functional block diagram is shown in Figure 7. The module accepts its input signal from the user's system, typically a D/A. The signal is buffered and then modulated to be passed across the transformer isolation barrier. After the signal is demodulated, it is converted to an output current. The output current loop is floating. The output terminals are protected even if a 120 V rms signal is connected.

A single +24 volt power supply drives the module's power transformer and the clock oscillator. The power is isolated from the input signal.

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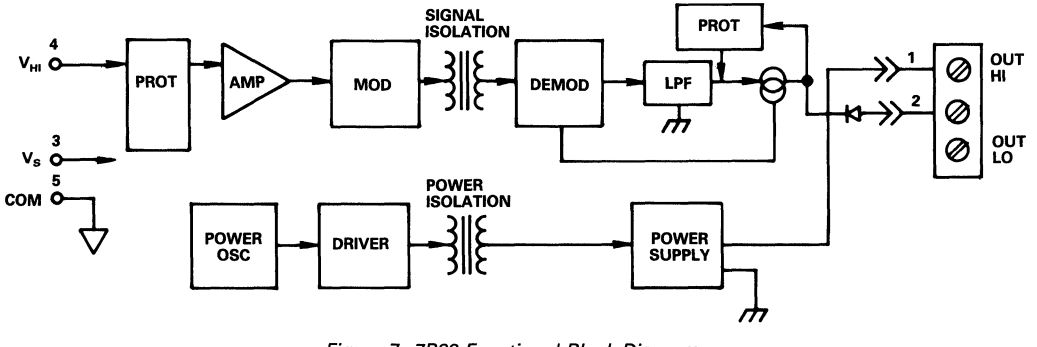

Figure 7. 7B39 Functional Block Diagram

BACKPLANE FUNCTIONAL DESCRIPTION

The 7B Series includes a variety of backplanes to address end user and evaluation needs. Backplanes are available in 16-, 8- and 4-channel sizes. The 16- and 8-channel backplanes can be mounted in a 19″ by 3.5″ panel space. The 4-channel backplane is ideal for evaluation purposes or small point count applications.

Each backplane channel has three screw terminals for field connections. The field connections accept transducer or signal inputs and provide excitation and current outputs when needed. A cold junction compensation sensor is mounted underneath the screw terminal block on each channel to accommodate thermocouple modules. Each I/O channel has six pin sockets to ensure interchangeability of the modules. A standard D type 25-pin connector is used for system interface on the 16-channel backplane. The connector provides 16 single ended input and/or output signals.

All 7B Series backplanes have three power supply connections. The modules can accept power supply levels from +14 to +35 volts. Two connections are used for a primary +24 volt power input and a backup power supply. A series diode is used to sense the power supply. If one supply fails, the other supply can take over. The diode also provides reverse power connection protection. The third power connection can be used for a +15 volt power supply since there is no diode drop in the line to affect the power supply level. A LED on each backplane indicates the power status.

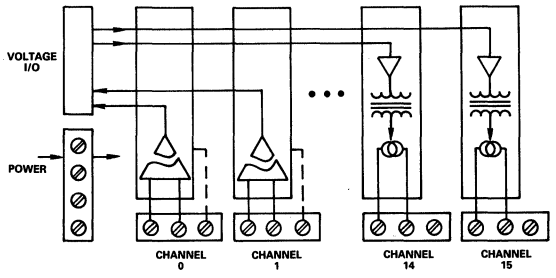

Figure 8. 7BP16 Block Diagram

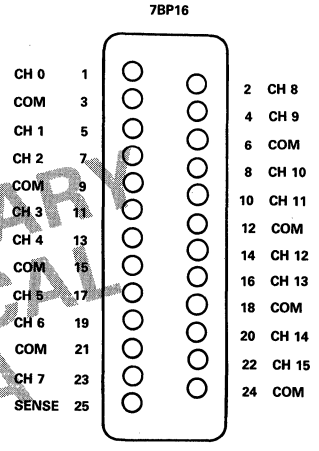

Figure 9. System Connector Pinout Bottom View

BACKPLANE SPECIFICATIONS

	7BP16	7BP08	7BP04
Channels	16	8	4
External Power Requirement	+14 V to +35 V	*	*
Cold Junction Sensor	On Each Channel	*	*
Size	3.5″×17.4″		

*Specifications same as 7BP16

ACCESSORIES

To facilitate system design with the 7B Series the following accessories are available:

CJC Sensor. The thermistor used for cold junction compensation is available for integration into a custom designed backplane. This sensor is installed on each channel of the backplane.

Current Conversion Resistor. This encapsulated, precision 250 Ω resistor can be used with the 7B33 Isolated Voltage Input Module to convert a 4–20 mA current input to the 1–5 volt input for the module.

Rack Mount. A single piece metal chassis for mounting a 7B Series backplane in a 19″ rack. Model number AC1363.

Power Supply. Chassis mounted +24 volts at 1 amp power supply, capable of supplying a 16-channel backplane.

Cables. A 2 foot cable with a 25-pin D type connector and a 26-pin connector is available to connect the 7B Series backplane to systems compatible with the 3B and 5B Series families.

Digital Panel Instruments
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Selection Guide
Digital Panel Instruments

Digital Panel Meters

Model	Digits	FS Range	Data Output	Display Type	Page	Comments
AD2026-1	3	−99 mV to +999 mV	N/A	LED	14–11	+5 V Power
AD2010	3 1/2	±199.9 mV	BCD	LED	14–7	+5 V Power
AD2021	3 1/2	±199.9 mV, ±1.999 V, ±19.99 V	Serial	LED	14–9	+5 V Power
AD2026-2	3	−99 mV to +999 mV	N/A	LED	14–11	Line Power

Digital Temperature/Transducer Meters

Model	Interface	Readout	Digital Data Output	Page	Comments
AD2050	Thermocouple	LED 3 1/2 Digits	7-Bit Character Serial ASCII	14–13	Self-Calibrated, User Specified Thermocouple
AD2051	Thermocouple	LED 3 1/2 Digits	7-Bit Character Serial ASCII	14–13	Self-Calibrated, Switch Selected Thermocouple
AD2060	RTD/Thermister	LED 3 1/2 Digits	7-Bit Character Serial ASCII	14–15	Self-Calibrated, User Specified RTD/Thermister
AD2061	RTD/Thermister	LED 3 1/2 Digits	7-Bit Character Serial ASCII	14–15	Self-Calibrated, Switch Selected RTD/Thermister
AD2070	Thermocouple	LED 4 1/2 Digits	7-Bit Character Serial ASCII	14–17	Self-Calibrated, Autoranging Thermocouple
AD2071	Thermocouple	LED 4 1/2 Digits	7-Bit Character Serial ASCII	14–17	Self-Calibrated, Autoranging Thermocouple

Orientation
Digital Panel Instruments

A digital panel instrument is a self-contained instrument designed for panel mounting. It contains circuitry for measuring analog quantities, converting them to digital and providing a numeric readout. In addition, it usually provides data outputs for interfacing with a printer and/or a computer system.

Digital panel instruments manufactured by Analog Devices fall into two classes: digital panel meters for voltage measurements and microprocessor-based digital thermometers to read out temperature measurements from user-chosen sensors. A *digital panel meter* measures voltage, generally with fractional-millivolt resolution. A *temperature meter* accepts inputs from standard thermocouples, RTDs, and thermistors, and provides readouts directly in temperature, to 3 1/2 or 4 1/2 digits; thermocouple meters provide reference-junction compensation and linearization, while RTD/thermistor meters also provide current excitation for RTDs and thermistors.

Two useful publications from Analog Devices may be helpful in understanding the issues involved in signal conditioning and data conversion: *Analog-Digital Conversion Handbook*, third edition (1986, $32.95) and *Transducer Interfacing Handbook* (1980, $14.50). Both are available from the Analog Devices Literature Center at P.O. Box 9106, Norwood MA 02062-9106.

A DPM samples the input voltage periodically, converts that voltage to digital, and displays the corresponding reading visually. A digital panel meter, then, consists of four basic functional sections: the input section, including signal conditioning and analog to digital conversion circuitry; the display; the data outputs and the power supply.

Processing the Input Signal
The primary function of the input section is to convert an analog input voltage into a digital signal for display. Besides this basic function, the input section also buffers the input to provide a high input impedance, prevent circuit damage in overvoltage conditions, reject both normal-mode and common-mode noise on the input signal, compensate for large variations in operating temperature and sometimes even measure the ratio of two separate input voltages.

The analog to digital conversion scheme used on most DPMs is the dual-slope type due to its inherent stability and normal-mode noise rejection. The dual-slope converter can also be used to measure the ratio of two input voltages in some DPM designs. Lower-resolution DPMs sometimes use staircase or single slope converters which require RC filtering of the input signal for a normal-mode-noise rejection.

The input of the DPM may be single-ended, differential or floating. Single-ended inputs measure the input voltage with respect to input common and may require some care in application to avoid ground loop problems. To prevent ground loops, some of Analog Devices' DPMs use a "limited differential input," where a resistor separates analog and digital grounds allowing up to 200mV of common-mode voltage and providing up to 60dB of common-mode rejection.

AC-powered DPMs can be floated on the power-supply transformer to provide isolation and CMR. For example, the line-powered AD2026-2 has floating inputs with 116dB of CMR and a 1,000-volt common-mode rating.

Displaying the Data – Digital Outputs
Once the input signal is digitized, it is decoded and displayed on a digital readout. Analog Devices DPMs use large seven-segment light-emitting diode (LED) displays.

DPM full-scale range, including *overrange*, is defined by the number of digits and polarity. In mixed-fraction designations (e.g., 3 1/2 digits), a full digit is one capable of displaying any numeral from 0 through 9. The fraction generally means the ratio of the display's maximum leading digit to the power of two that corresponds to the number of overrange bits; for example, a 3 1/2-digit meter's maximum reading is 1999, a 4 3/4-digit meter's maximum reading is 39999.

Since the visual display of a DPM must be in a decimal format, counter chips used in DPM conversion circuitry are generally binary-coded decimal (BCD) types. The data output format depends on the circuit design of the meter; for example, the AD2010 has parallel BCD data outputs with all BCD bits available simultaneously, while the AD2021 has character-serial outputs – each BCD digit is gated onto a single set of parallel output lines in sequence. The latter technique requires fewer connections and simplifies data interfacing.

Digital data outputs from DPMs are generally compatible with DTL or TTL logic systems; many DPMs are also compatible with CMOS logic.

Control
The kinds and number of control inputs and outputs – and their interpretation – may differ from one model to another, but they are well defined on the data sheets. Examples of typical control functions that may be found in DPMs include triggering of conversions, external *hold*, decimal points (jumper or logic-programmable), display blanking and *status* output.

DIGITAL TEMPERATURE METERS
Microprocessor-based devices in this class include the AD2050/AD2051 Thermocouple Meters, the AD2060/AD2061 Autoranging RTD/Thermistor Meters and the AD2070/AD2071 Autoranging Thermocouple Meters.

In addition to the basic panel-meter circuitry, these instruments have signal-conditioning front ends with overvoltage protection and open-sensor detection, automatic self-calibration and sophisticated output options. Besides linearization, their functions include cold-junction compensation for thermocouples and excitation for RTDs and thermistors. They read out in degrees Fahrenheit or Celsius, and the autoranging types choose between 0.1° and 1° resolution, depending on range.

The AD2050, AD2060, and AD2070 are dedicated instruments for optional specific sensor types (e.g., type K thermocouple), while the AD2051, AD2061, and AD2071 are "universal instruments" for any one of a set of specified sensors, programmable by the user to meet the needs of the application.

Communication options simplify temperature recording with computers, strip-chart recorders or printers. In addition to 7-bit character-serial ASCII outputs, the user has the option of a linearized analog output for strip-chart recorders, and serial ASCII output in two forms: isolated 20mA digital current-loop and/or nonisolated TTL. The AD2070/AD2071 has optional isolation for all data outputs, including RS-232.

Understanding Performance Specifications

Resolution, Accuracy and Stability – these three specs are very important in the selection of a DPM. Although more digits may mean more resolution, the digits themselves are useless unless the accuracy is sufficient for the digits to have real meaning. Therefore, accuracy and resolution should be comparable.

Besides temperature variations, there are three components of DPM inaccuracy: *zero offset error, gain error* and *quantization error*. In any device using a counter and clock to determine a digital output, there is always a potential ±1 count error in the output. This is caused by the timing of the input gate of the counter; when the gate closes asynchronously with the clock, a clock pulse that occurs just as the gate closes may or may not be counted, hence the fixed ±1 digit inaccuracy.

Zero-level offsets in the analog circuitry cause errors specified as a percentage of full-scale reading. These errors can be corrected by a zero-calibration potentiometer requiring periodic resetting, or by internal calibration circuits that set the zero level automatically between each pair of readings, assuring no zero-level contribution to the error.

Gain variations occur as a function of signal level in the analog circuitry and produce errors which are specified as a percentage of the reading. These are the hardest errors to design out of a DPM circuit, but they can be minimized by component specification and selection. A range potentiometer is used for periodic adjustment of the gain. Gain errors may also be calibrated out in "smart" instruments having an automatic internal calibration facility (e.g. AD2070).

Since all the electronic components used in the design of a DPM have some temperature dependence, one can expect the accuracy of the DPM to be affected by changes in operating temperature. If automatic zero correction circuitry is not used, the zero level may drift with temperature. Variations in the reference voltage circuitry and its associated switches will cause changes in the gain of the DPM, but careful selection and matching of components can minimize this error.

To illustrate these specifications, consider a 3 1/2 digit DPM (1999 counts full scale). The resolution of the unit is the value of one digit, 1 part in 2000 or 0.05% of full scale. If the accuracy is comparable to the resolution (exclusive of digital indecision), the DPM should have a maximum error of ±0.05% ±1 digit.

Temperature coefficient specifications for a DPM should be very good to maintain the accuracy. A tempco of only 50ppm/°C (0.005%/°C) will produce an additional error of ±0.05% over a range of only ±10°C.

Since each manufacturer tends to use a different method of specifying accuracy and temperature coefficients, specifications must be expressed in common terms to be comparable.

DEFINITIONS – DPM TERMS & SPECIFICATIONS

Accuracy (Absolute): DPMs are calibrated with respect to a reference voltage which is in turn calibrated to a recognized voltage standard. The absolute accuracy error of the DPM is the tolerance of the full-scale set point referred to the absolute voltage standard.

Accuracy (Relative): Relative accuracy error is the difference between the nominal and actual ratios to full scale of the digital output corresponding to a given analog input. See also: *Linearity*.

Automatic Zero: To achieve zero stability, a time interval during each conversion is provided to allow the circuitry to compensate for drift errors, thereby providing virtually no zero drift error.

Bias Current: The current required from the source at zero signal input by the input circuit of the DPM. Bias current is normally specified at typical and maximum values. Analog Devices' DPMs using transistor input circuitry are biased current sinks.

Binary Coded Decimal (BCD): Data coding where each decimal digit is represented by a group of 4 binary coded digits (called "quads"). Each quad has bits corresponding to 8, 4, 2 and 1 and 10 permissible levels with weights 0-9. BCD is normally used where a decimal display is needed.

Bipolar: A bipolar DPM measures inputs which may be of either positive or negative polarity and automatically displays the polarity as well as the magnitude of the input voltage on the readout.

Character Serial BCD: Multiplexed BCD data outputs, where each digit is gated sequentially onto four common output lines.

Common-Mode Rejection: A differential-input DPM will reject any input signals present at both input terminals simultaneously if they are within the common-mode voltage range. Common-mode rejection is expressed as a ratio and usually given in dB. (CMR = 20 log CMRR 120dB of common-mode rejection.) (CMRR = 10^6) means that a 10V common-mode voltage is processed as though it were an additive differential input signal of 10μV magnitude.

Common-Mode Voltage: A voltage that appears in common at both input terminals of a device, with respect to its ground.

Conversion Rate: The frequency at which readings may be processed by the DPM. Specifications are typically given for internally clocked rates and maximum permissible externally-triggered rates.

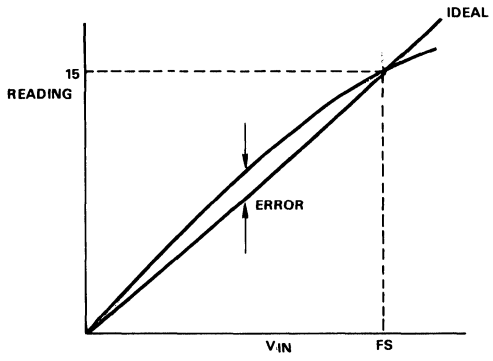
Conversion Time: The maximum time required for a DPM to complete a reading cycle, specified for the full-scale reading.

Dual-Slope Conversion: An integrating A/D conversion technique in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time.

Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown, until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period.

Input Impedance: The complex ratio of signal voltage to signal current at the input terminals. For dc measuring DPMs, the input is measured at dc. For ac measuring DPMs, it is expressed as a dc resistance shunted by a specified capacitance.

Linearity: The conventional definition for nonlinearity of a DPM is the deviation from a "best" straight line which has been fitted to a calibration curve. Analog Devices defines nonlinearity as the deviation from a straight line drawn between the zero and full-scale end points. Not only is this an easier method for customer calibration, it is also a more conservative method of specifying nonlinearity.



Linearity

Normal-Mode Rejection: Filtering or integrating the input signal improves noise rejection of undesired signals present at the analog *high* input. Normal-mode rejection is expressed as the ratio of the actual value of the undesired signal to its measured value over a specified frequency range. (NMR (dB) = 20 log NMRR, e.g. NMR = 40dB means an attenuation of 100:1.)

Overload: An input voltage exceeding the full-scale range of the DPM produces an overload condition. An overload condition is usually indicated by conspicuous manipulation of the display such as all dashes, flashing zeros, etc. On a 3 1/2 digit DPM with a range of 199.9mV, a ≥200mV, signal will produce an overload condition.

Overrange: An input signal that exceeds all nines on a DPM, but is less than an overload. On a 3 1/2 digit DPM with a full-scale range of 199.9mV, the all-nines range is 0-99.9mV, and signals from 100-199.9mV are said to fall in the 100% overrange region. Some DPMs have higher overrange capability. A 3 3/4 digit DPM has a full-scale range of 3.999 or 300% overrange.

Overvoltage Protection: The input section of the DPM must provide protection from large overloads. Specifications are given for sustained dc voltages that can be tolerated.

Parallel BCD: A data output format where all digital outputs are available simultaneously.

Range (Temperature Operating): The range of temperatures over which the DPM will meet or exceed its performance specifications.

Range (Full Scale): The range of input signals that can be measured by a DPM before reaching an overload condition. A 3 1/2 digit DPM's full-scale range consists of three digits (all-nines range) and 100 percent overrange capability.

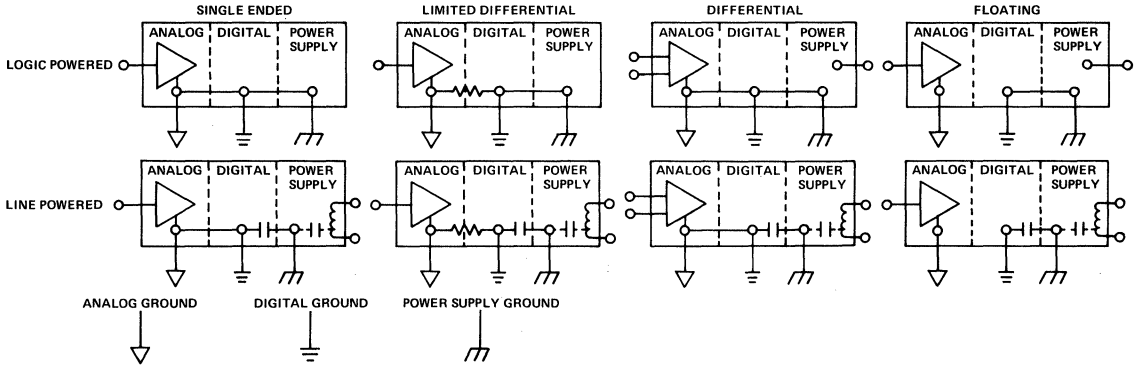
Ratiometric: Dual Slope DPMs compare voltage inputs to a stable internal reference voltage. In some systems, the voltage being measured is a function of another voltage, and accurate measurements should be made as the ratio of the two voltages. Some DPMs provide inputs for external reference voltages for ratiometric measurements.

Resolution: The smallest voltage increment that can be measured by a DPM. It is a function of the full-scale range and number of digits of a DPM. For example, if a 3 1/2 digit DPM has a resolution of 1 part in 2000 (0.05%) over a full-scale range of 199.9mV, the DPM can resolve 0.1mV.

Digits	Counts (F.S.)	Resolution (% F.S.)
2 1/2	199	0.5%
3	999	0.1%
3 1/2	1999	0.05%
3 3/4	3999	0.025%
4	9999	0.01%
4 1/2	19999	0.005%
4 3/4	39999	0.0025%

Temperature Coefficient: The additive error term (ppm/°C or % Reading/°C) caused by effects of variations in operating temperature on the electronic characteristics of the DPM.

Unipolar Input DPM: A DPM designed to measure input voltages of only one polarity.



Grounding Configurations of DPMs

ANALOG DEVICES

Low Cost, 3 1/2 Digit DPM for OEM Applications

AD2010

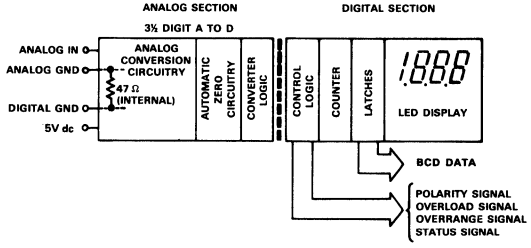
FEATURES

LED Display with Latched Digital Outputs
Small Size, Lightweight
Automatic Zero Correction; Max Error: 0.05% ±1 Digit
High Normal Mode Rejection: 40dB @ 50 or 60Hz
Optional Ratiometric Operation
Leading "0" Display Blanking
5V dc Powered

APPLICATIONS

Medical/Scientific/Analytic Instruments
Data Acquisition Systems
Industrial Weighing Systems
Readouts in Engineering Units
Digital Thermometers

AD2010 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Analog Devices' model AD2010 represents an advance in price/performance capabilities of 3½ digit digital panel meters. The AD2010 offers 0.05% ±1 digit maximum error with bipolar, single ended input, resolution of 100μV, and a common mode rejection ratio of 60dB (CMRR) at ±200mV (CMV).

The AD2010 features a light-emitting-diode (LED) display with a full scale range of 0 to ±199.9 millivolts, latched digital data outputs and control interface signals, and leading zero display blanking. Automatic-zero correction circuitry measures and compensates for offset and offset drift errors, thereby providing virtually no error. Another useful feature of the AD2010 is its 5V dc operation. The AD2010 can operate from the users' 5V dc system supply, thereby eliminating the shielding and decoupling needed for line powered units when the ac line must be routed near signal leads.

To satisfy most application requirements, the conversion rate of the AD2010 is normally 4 readings per second. However, an external trigger may be applied to vary the sampling rates from a maximum of 24 readings per second down to an indefinite hold time. The AD2010 can also be connected for automatic conversion at its maximum conversion rate. During conversion, the previous reading is held by the latched logic. The numeric readout is available as BCD data. Application of the metering system in a computer or data logging system is made easy with the availability of the "overrange," "polarity," "overload," and "status" signals.

A simplified block diagram of the AD2010, illustrating the features described above is shown in Figure 1.

IMPROVED NOISE IMMUNITY, ACCURACY AND ZERO STABILITY

Dual-slope integration, as used in the AD2010 and as described in the theory of operation section, offers several design benefits.

- Conversion accuracy, for example, is independent of both the timing capacitor value and the clock frequency, since they affect both the up ramp and down ramp integration in the same ratio.
- Normal mode noise at line frequencies or its harmonics is rejected since the average value of this noise is zero over the integration period.
- To achieve zero stability, a time interval during each conversion is provided to allow the automatic-zero correction circuitry to measure and compensate for offset and offset drift errors, thereby, providing virtually no zero error.

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For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and +5VDC unless otherwise noted)

DISPLAY OUTPUT
- Display consists of four LED's (0.27" (6.9mm) high). for data digits plus 100% overrange and polarity indication.
- Overload – three data digits display zeros and flashes.
- Decimal Points – selectable at input connector.
- Leading "0" Display Blanking – controlled externally.

INPUT
- Full Scale Range – 0 to ±199.9 millivolts
- Automatic Zero
- Automatic Polarity
- Bias Current – 3nA
- DC Impedance – 100MΩ
- Overvoltage Protection – 20V sustained, 50V momentary without damage.
- Decimal Points (3) – illuminate with logic "1", extinguish with logic "0".

ACCURACY
- Maximum Error – 0.05% of reading ±1 digit
- Resolution – 0.1 millivolt
- Temperature Range – 0 to +50°C operating
  -30°C to +85°C storage
- Temperature Coefficient – ±50ppm/°C

NORMAL MODE REJECTION
- 40dB @ 60Hz

COMMON MODE REJECTION
- 60dB @ ±200mV

CONVERSION RATE
- External Trigger – up to 24 conversions per second
- Internal Trigger – 4 conversions per second
- Automatic – A new conversion is initiated automatically upon completion of conversion in process; conversion rate will vary from 24/sec to 40/sec depending on input magnitude.
- Hold and Read upon command.

CONVERSION TIME
- Normal Conversion – 42ms max (full scale input)
- Overload Conversion – 62ms max

INTERFACE SIGNALS
- DTL/TTL Compatible

	IN	OUT
logic "0"	<0.8V	<0.4V
logic "1"	>2.0V	>2.4V

- Inputs

External Trigger – Operation in the "External Trigger" mode requires that the "External Hold" input be a logic "0" or ground.

Negative Trigger Pulses – Applying a logical "low" to the "HOLD" input disables the internal trigger. A negative trigger pulse (logic "1" to logic "0") of 1.0μs minimum applied to the "EXT TRIGGER" input will initiate conversion in the same manner as the internal oscillator. The external trigger should not be repeated, however, until the "status" indicates completion of the conversion in process.

Positive Trigger Pulses – The "HOLD" input can be used to trigger the AD2010 from a "normally low" signal with the "EXT TRIGGER" input open or logic "1". Following a "hold" a new reading will be initiated on the leading edge of the "hold" signal. Thus, a momentary positive pulse on the "HOLD" input can be used to trigger the AD2010. The drift correct interval, however, begins on the trailing edge of the positive pulse, so if the pulse width exceeds 1ms, the conversion will actually be initiated by the internal trigger.

Specifications subject to change without notice.

Maximum Conversion Rate - Automatic – The AD2010 can also be connected for automatic conversion at its maximum conversion rate by connecting the "status" output back into the "hold" input. In this manner the status signal going high at the end of one conversion immediately initiates a new conversion. The pulses appearing on the status line can be used to step a multiplexer directly, since the built-in drift-correct delay of 8.33ms will allow settling of the input prior to conversion. A logic "0" applied to the "EXT TRIGGER" will inhibit the automatic trigger mode.

External Hold – Logic "0" or ground applied to this input disables the internal trigger and the last conversion is held and displayed. For a new conversion under internal control the input must be opened or at logic "1". For a new conversion under external control, a positive pulse of less than 1.0ms can be applied (as previously explained).

OUTPUTS
- 3 BCD Digits (8421 Positive True) - latched - 3TTL loads
- Overrange - logic "1" - latched - 6TTL loads, indicates overrange.
- Overload - logic "0" indicates overload (>199.9mV) logic "1" - latched - 6TTL loads, indicates data valid.
- Polarity - logic "1" - latched - 6TTL loads, indicates positive polarity input.
- Status - logic "0" - conversion in process logic "1" - latched - 6TTL loads, indicates conversion complete.

POWER
- +5V dc ±5%, 500mA

WARM UP
- Essentially none to specified accuracy

ADJUSTMENTS
- Range potentiometer for full scale calibration. Calibration recommended every six months.

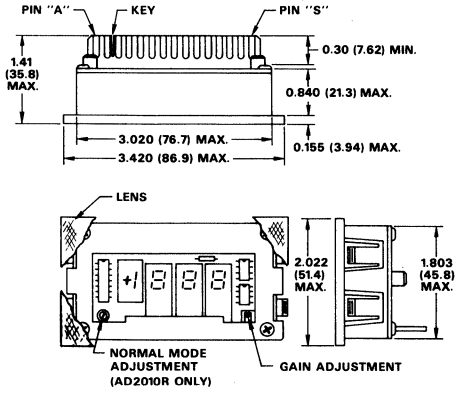
SIZE
- 3"W x 1.8"H x 0.84"D (76.2 x 45.7 x 21.3mm) (overall depth for case and printed circuit board extension is 1.40" (35.6mm)).

ORDERING GUIDE
- AD2010 - Standard AD2010 as described above - tuned for peak normal mode rejection at 60Hz and its harmonics.

WEIGHT
- 4 oz. (113.5gm)

OVERALL DIMENSIONS

All dimensions are given in inches and (mm).



Low Cost, 3 1/2 Digit Logic Powered DPM with LED Displays

AD2021

FEATURES
"Second Generation" MOS-LSI Design
Large 0.5" (13mm) LED Displays
+5VDC Logic Powered
±1.999V, ±199.9mV or ±19.99V Full Scale Ranges
Limited Differential Input
Low Power Consumption: 2.0 Watts
Small Size, Industry Standard Case Design

APPLICATIONS
General Purpose Logic Powered DPM Applications
Portable Applications Requiring Low Power Consumption

GENERAL DESCRIPTION

The AD2021 is a low cost, 3½ digit, +5V dc logic powered digital panel meter with large LED displays. While designed for general purpose DPM applications, the small size, light weight and low power consumption of the AD2021 make it an ideal digital readout for modern, compact instrument designs.

THE BENEFITS OF "SECOND GENERATION" DESIGN

The AD2021 is designed around MOS-LSI (Metal-Oxide-Semiconductor, Large Scale Integration) integrated circuits, which greatly reduce the number of components, and thereby the size, and reduce power consumption to 2.0 watts. Both the lower power consumption and fewer interconnections between components promise greatly increased reliability, and the circuit design maintains the performance and features of earlier DPMs. Large 0.5 inch (13mm) LED displays offer the visual appeal of gas discharge displays with the ruggedness and lifetime of all solid state devices.

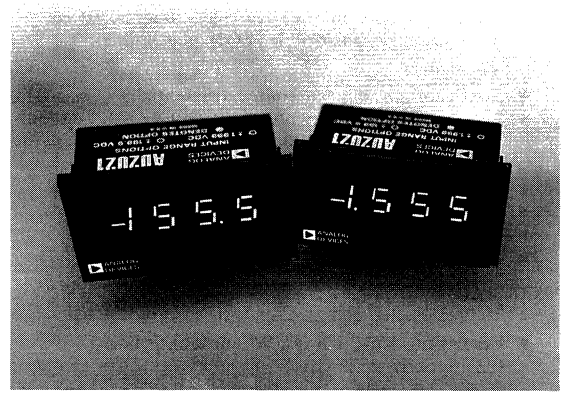
EXCELLENT PERFORMANCE AND EASY APPLICATION

The AD2021 measures input voltage over a full scale range of ±1.999V dc or ±199.9mV dc ("S" option) with an accuracy of ±0.05% reading ±0.025% full scale ±1 digit. Using the "limited differential" input first used on Analog Devices' AD2010, the AD2021 prevents ground loop problems and provides 35 to 50dB of common mode rejection at common mode voltages up to ±200mV. Normal mode rejection is 40dB at 50Hz to 60Hz.

BCD data outputs are provided in a bit parallel, character serial format compatible to CMOS logic systems. For those applications requiring parallel BCD data, schemes for making the serial to parallel conversion are available. Controls to hold readings, select decimal points and blank the display are provided.

DESIGNED AND BUILT FOR RELIABILITY

The AD2021 is packaged in Analog Devices' logic powered DPM case size, only 1.25 inches (32mm) deep. The small size of this DPM makes it easy to accommodate in any instrument design, and since several other manufacturers now use the same panel cutout for logic powered DPMs, this industry standardization allows mechanical second sourcing. In addition, the



AD2021 uses the same pin connections as the AD2010 (except in BCD outputs, of course) as a convenience to allow updating designs to take advantage of the second generation design and larger display of the AD2021. Each AD2021 receives a full one week failure free burn-in before shipment.

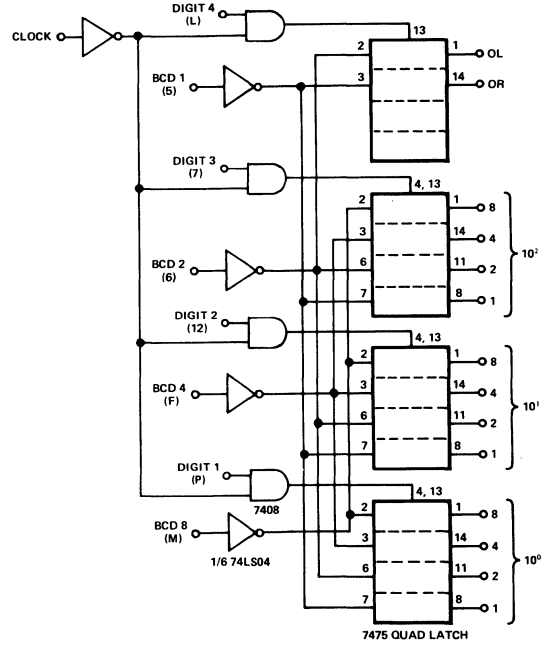


Figure 1. AD2021 Bit Parallel Character Serial to Full Parallel Data Conversion. AD2021 Pin Connections Are Shown in Parentheses.

For detailed information, contact factory.

SPECIFICATIONS (typical at +25°C and nominal power supply voltage)

DISPLAY OUTPUT
- Light emitting diode, planar seven segment display readouts, 0.5" (13mm) high for three data digits, 100% overrange and negative polarity indication. Overload indicated by flashing display, polarity remains valid.
- Decimal points selectable at input connector.
- Display blanking on three data digits (does not affect overrange digit, polarity sign of decimal points).

ANALOG INPUT
- Configuration: bipolar, limited differential
- Full Scale Range: ±1.999V or ±199.9mV ("S" option) ±19.99V ("V" option)
- Automatic Polarity
- Auto Zero
- Input Impedance: 100MΩ (1MΩ – "V" option)
- Bias Current: 50pA
- Overvoltage Protection: ±50V dc, sustained

ACCURACY
- ±0.05% reading ±0.025% full scale ±1 digit[1]
- Resolution: 1mV, 10mV ("V" option) or 100μV ("S" option)
- Temperature Range[2]: 0 to +50°C operating; -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: auto zero
- Warm-Up Time to Rated Accuracy: less than one minute
- Settling Time to Rated Accuracy: 0.4 second

NORMAL MODE REJECTION
- 40dB at 50–60Hz

COMMON MODE REJECTION
- AD2021: 35dB (dc -10kHz)
- AD2021/S: 50dB (dc -10kHz)
- AD2021/V: 15dB (dc -10kHz)

COMMON MODE VOLTAGE
- ±200mV

CONVERSION RATE
- 5 conversions per second
- Hold and read on command

CONTROL INPUTS
- Display Blanking: (TTL, DTL compatible, 2 TTL loads). Logic "0" or grounding blanks the three data digits only, not the decimal points, overrange digit (if on) and polarity sign. Logic "1" or open circuit for normal operation. Display blanking has no effect on output data and the display reading is valid immediately upon removal of a blanking signal.
- Hold: (CMOS, DTL, TTL compatible, 1LP TTL load). Logic "0" or grounding causes the DPM to cease conversions and display the data from the last conversion. Logic "1" or open circuit for normal operation. After the "Hold" input is removed, one to two conversions are needed before the reading is valid.
- Decimal Points: Grounding or Logic "0" will illuminate the desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle when the decimal points are illuminated.

DATA OUTPUTS (See Application Section for details on data outputs)
- BCD Data Outputs: (CMOS, LP TTL or LP Schottky compatible), bit parallel, character serial format.
- Digit Strobe Outputs: (CMOS, DTL, TTL compatible, one TTL load). Logic "1" on any of these lines indicates the output data is valid for that digit.
- Polarity Output: (CMOS, TTL, DTL compatible, one TTL load). Logic "1" indicates positive polarity input, logic "0" indicates negative polarity.
- Status: (CMOS or LP TTL compatible). When this signal is at Logic "1", the output data is valid.
- Clock: (CMOS, DTL, TTL compatible, one TTL load). The clock signal is brought out to facilitate conversion from character serial to parallel data.
- INTERFACING DATA OUTPUTS. The BCD data outputs are in a bit parallel, character serial format. There are four BCD bit outputs (1, 2, 4, 8) and four digit outputs (10^0, 10^1, 10^2, 10^3). The BCD digits are gated onto the output lines sequentially, and the BCD bits are valid for the digit whose digit line is high. The data is valid except when being updated which occurs within 2 milliseconds after the status line goes low.

REFERENCE OUTPUT
- A 6.4V ±5% analog reference output is made available. This reference should be buffered and filtered if use in external circuitry is desired.

POWER INPUT
- +5V dc ±5%, 1.45 watts

CALIBRATION ADJUSTMENTS (See Application Section for calibration instructions)
- Gain
- Zero
- Recommended recalibration interval: six months

SIZE
- 3"W x 1.8"H x 1.33"D (76 x 46 x 34mm)
- 1.90" (48mm) overall depth to rear of card edge connector.
- Panel cutout required: 3.175" x 1.810" (80.65 x 45.97mm).

WEIGHT
- 4 ounces, (115 grams)

OPTIONS – ORDERING GUIDE
- Input Voltage Range: AD2021 – 1.999V dc Full Scale
  AD2021/S – 199.9mV dc Full Scale
  AD2021/V – 19.99V dc Full Scale

CONNECTOR
- 30 pin, 0.156" spacing card edge connector. Viking 2VK15D/1-2 or equivalent.
- Optional: Order AC1501

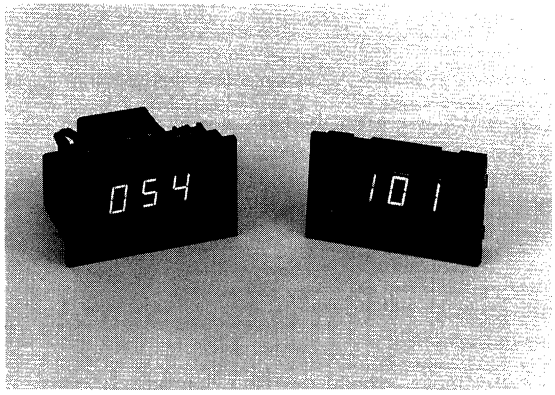
NOTES
[1] Guaranteed at 25°C and nominal supply voltage
[2] Guaranteed

Specifications subject to change without notice.

Low Cost, 3 Digit AC Line or Logic Powered DPM

AD2026*

FEATURES
Third Generation I^2L LSI Design
Either Line Powered or Logic Powered
Large 0.56″ Red Orange LEDs
Balanced Differential Input/Floating 1000V, CMV
Terminal Block Interface (ac Version)
High Reliability: >250,000 Hour MTBF
Small Size and Weight
Low Cost



GENERAL DESCRIPTION

The AD2026 is specifically designed to provide a digital alternative to analog panel meters. The AD2026 is available either logic powered (+5V dc) or ac line powered. Most of the analog and digital circuitry is implemented on a single I^2L LSI chip, the AD2020. Only 13 additional components are required to complete the AD2026 +5V dc version. The entire dc version is mounted on a single 3″ X 1 5/8″ PCB. AC line power is achieved with the addition of a second PCB containing the ac power transformer and power supply circuitry.

The AD2026, on both the ac line and logic powered versions, offers as a standard feature, 0.56″ high LED Displays. Brightness is enhanced on both versions due to the Red Orange lens. In addition to the Red Orange lens, the AD2026 is also available with a dark red lens for applications where maximum brightness is not required and minimum backlighting is desired.

A unique patented case design utilizes molded-in fingers, both to capture the PCB in the case and to provide snap-in mounting of the DPM in a standard panel cutout. No mounting hardware of any kind is used. The dc version occupies less than 1″ of space behind the panel. The line powered version offers the same mounting features but occupies 2 1/2″ of behind-panel space.

EXCELLENT PERFORMANCE

The AD2026 offers the instrument designer digital accuracy, resolution and use of readout while occupying less space than its analog counterpart. Other features of analog meters such as reliability and instantaneous response are retained in the AD2026.

The AD2026 measures and displays inputs from -99mV to +999mV, with an accuracy of 0.1% of reading ±1 digit. Zero shift is less than one bit over the full operating temperature range, resulting in the same performance as a DPM with auto zero. The balanced differential input of the dc powered AD2026 rejects common mode voltages up to 200mV, enough to eliminate most ground loop problems. The floating differential input inherent in the ac line powered version offers 1000V of common mode voltage rejection.

*Covered by patent numbers: 4,092,698; 29,992; 3,872,466; and 3,887,863.

Optional 10.0V full scale (F.S.) range is available on the ac line version that will accept inputs from -0.99V to 9.99V.

WIRING CONNECTIONS

For Balanced Differential operation with the AD2026 dc version, connect input as shown in Figure 1. The common mode loop must provide a return path for the bias currents internal to the AD2026. The resistance of this path must be less than 100kΩ and total common mode voltages must not exceed 200mV.

For applications where attenuation is required, scaling resistors can be connected between pins 6 and 7 and between pins F and H. Pin 5 must be used as the High Analog Input when scaling resistors are used and pin 4 when they are not. Pin E is the Analog Low Input.

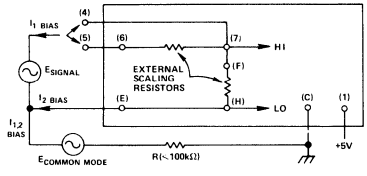


Figure 1.

Connection to the ac line powered AD2026 is via the terminal strip on the rear. AC line power is connected to terminals 4 and 5 and the signal input is connected to terminal 1 (Analog HI) and 2 (Analog Ground).

SPECIFICATIONS (typical at +25°C and nominal supply voltage unless otherwise noted)

DISPLAY OUTPUT
- Light emitting diode, planar seven segment display readouts, 0.56" (14.6mm) high (orange)
- Overload Indication: EEE
- Negative Indication: -XX
- Negative Overload Indication: ---
- Decimal Points: three (3) selectable at input connector (dc version); internally on ac version

ANALOG INPUT
- Configuration: balanced differential input (dc version) single ended isolated (ac version)
- Full Scale Range: -99mV to +999mV
  -0.99V to +9.99V (10V option on ac version)
- Automatic Polarity
- Input Impedance: 100MΩ; 100kΩ (10V option)
- Bias Current: 100nA
- Overvoltage Production: ±15V dc, sustained

ACCURACY
- ±0.1% ±1 digit[1]
- Resolution: 1mV or 10mV
- Temperature Range[2]: -10°C to +60°C operating; -25°C to +80°C storage
- Temperature Coefficient: Gain: 50ppm/°C
  Zero: 10μV/°C (essentially auto zero)
- Warm-Up Time to Rated Accuracy: Instantaneous
- Settling Time to Rated Accuracy: 0.3 second for full input voltage swing (dc version); 0.75 second for full input voltage swing (ac version)

COMMON MODE REJECTION (1kΩ source imbalance, dc to 1kHz)
- 50dB, ±200mV common mode voltage (dc version)
- 116dB (96dB on 10V range); 1000V rms max CMV (ac version)

NORMAL MODE REJECTION
- 30dB at 50-60Hz (ac version)

CONVERSION RATE
- 4 conversions per second
- Hold and read on command (dc version only)

CONTROL INPUTS

Display Blanking/Display Power Input, (dc version only): The display of the AD2026 can be blanked by removal of power to the display power input, with no effect on conversion circuitry. If external logic switching is used, the display requires 110mA peak (85mA average) when illuminated.

Hold (dc version only): When the Hold input is at Logic "0", grounded or open circuit, the AD2026 will convert at 4 conversions per second. If a voltage of 0.6V to 2.4V is applied to this input, the DPM will stop converting and hold the last reading. A 12kΩ resistor in series with this input to +5V will provide the proper voltage input. (Consult factory for "HOLD" on ac version.)

DECIMAL POINT
- To illuminate decimal points on dc version, ground appropriate pin (A, B or 3).
- To illuminate decimal points on ac version, remove shroud and bridge appropriate solder pad (A, B or 3).

POWER INPUT LOGIC POWER[3]
- Converter: +5V ±5%, 0.2 watts typ; 0.33 watts max
- Display: +5V ±40%, 0.45 watts typ; 0.75 watts max

POWER INPUT AC LINE POWER
- AC line, 50-60Hz, 1.5 watts

CALIBRATION ADJUSTMENTS
- Gain
- Zero
- Recommended recalibration interval: six months

SIZE[4]
- 3.43"W X 2.0"H X 0.85"D (87 X 52 X 22mm)
- 0.88" (22mm) overall depth to rear of connector
- Panel cutout required: 3.175 ±0.015" X 1.810 ±0.015" (80.65 ±0.38 X 45.97 ±0.38mm)

WEIGHT
- 1.8 ounces (53 grams) (dc version)
- 7 ounces (198 grams) (ac version)

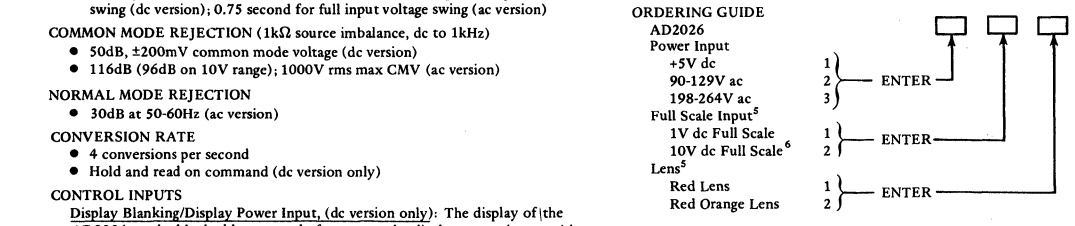
CONNECTIONS

A 10-pin T&B/Ansley 609-1000M with two feet of 10 conductor ribbon cable is available. Order AC2618 (dc version, only).

Conductor to pin A is color coded. Sequence of ribbon connections is A, 1, B, 2, C, 3, etc.

The AD2026 ac version is complete with terminal strip for easy interface.

ORDERING GUIDE

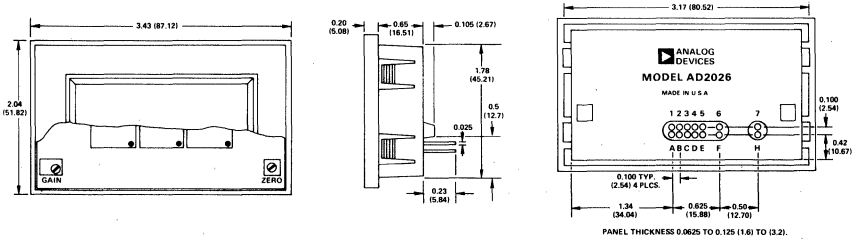


NOTES:
[1] Guaranteed at +25°C and nominal supply voltage.
[2] Guaranteed.
[3] When the same power supply is used to power both display and converter, +5V, ±5%, 0.65 watts typical, 0.9 watts max is required.
[4] Dimensions for ac line powered version: 3.43"W X 2.0"H X 2.44"D (87mm X 52mm X 63mm)
[5] No Charge Options
[6] 10V dc full scale option is available on ac power only

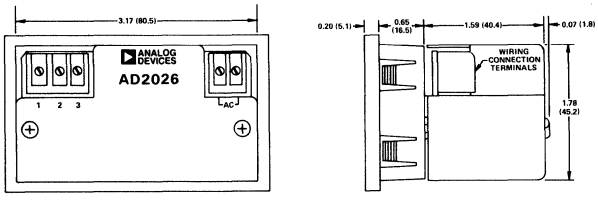
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC VERSION



PIN CONNECTIONS

AC VERSION

PIN	FUNCTION
1	Input
2	Analog Ground
3	NC
4	AC HI
5	AC LO

DC VERSION

PIN	FUNCTION
1	+5V Power
2	+5V Display Power
3	Decimal Point X.XX
4	Input (When Scaling Resistors Not Used)
5*	Input (When Scaling Resistors Are Used)
6*	Series Arm of Scaling Resistor Divider
7*	Series Arm of Scaling Resistor Divider

PIN	FUNCTION
A	Decimal Point XX.X
B	Decimal Point XXX.
C	Power Ground
D	Hold
E	Analog Ground
F*	Shunt Arm of Scaling Resistor Divider
H*	Shunt Arm of Scaling Resistor Divider

*NOT NORMALLY USED. ALLOWS CONVENIENT MOUNTING OF SCALING RESISTORS.

Microprocessor-Based Thermocouple Meters

AD2050/AD2051

FEATURES

Automatic Self-Calibration for Gain, Offset, Cold Junction Compensation and Thermocouple Linearization
J, K, T, E, R, S Thermocouple Selections (AD2050) Universal Meter (AD2051), User Programmable
Character Serial ASCII Digital Output
Optional Linearized Analog Output: 1mV/degree
Optional Isolated 20mA Loop/TTL Serial Outputs
Meets DIN/NEMA Dimension Specifications
Temperature Ranges: −265°F to +1999°F
−165°C to +1760°C
Power Options: 120V ac, 240V ac, +7.5V dc to +28V dc

APPLICATIONS

Temperature Monitoring in Laboratory, Manufacturing, and Quality Control Environments
Process Control Temperature Measurements
Remote Data Logging

GENERAL DESCRIPTION

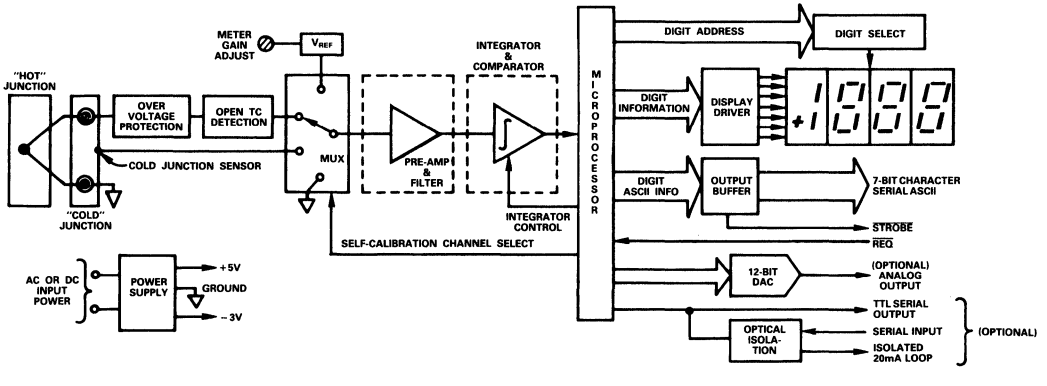
The AD2050 and AD2051 are high performance single channel 3½ digit thermocouple meters that can measure temperatures accurately between −265 and +1999 in degrees Celsius or Fahrenheit. The AD2050 is supplied factory programmed to interface directly with any of the following six thermocouple types: J, K, T, E, R and S. The AD2051 is a universal instrument in which the user selects one of the six thermocouple types via switch programming. Being microprocessor based, all gain and offset error correction, cold junction compensation, thermocouple linearization, and °C/°F scaling are automatically performed in firmware.

The AD2050 and AD2051 display temperature information on large 0.56″ (14.3mm) high LEDs. Digital information is provided in standard ASCII character serial format with rate selection for easy interface to printers, terminals, and other peripherals. For remote data acquisition applications, an optional isolated 20mA serial loop/TTL compatible interface is available. Also an optional analog output linearized to 1mV/degree is provided for driving recorders and other analog instruments. Selection of °C or °F scaling is accessed by removing the front panel lens and setting the selector switch to its proper position.

The AD2050 and AD2051 can also be ordered with any of the following power versions: 120V ac, 240V ac, or +7.5V dc to +28V dc. Input overvoltage protection for 300V peak (thermocouple to ac line shorts) and common mode voltages as high as 1400V peak (ac version) with overrange and open thermocouple detection are provided. These instruments are rated for operation over the +10°C to +40°C temperature range. Testing is performed per MIL-STD-202E Method 103B to insure specified operation over various relative humidity conditions. The AD2050 and AD2051 are supplied in rugged high impact plastic cases that meet DIN/NEMA standard dimensions.

14

AD2050/AD2051 FUNCTIONAL BLOCK DIAGRAM



For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and rated supply voltages unless otherwise specified)

THERMOCOUPLE INPUTS
- Thermocouple Types: J, K, T, E, S, R
- Input Impedance: >100MΩ
- External (Lead) Resistance Effect: <20μV per 350Ω of Lead Resistance
- Cold Junction Compensation Error: ±0.5°C max (+10°C to +40°C)
- Open Thermocouple: +EEE Display; +EEEE ASCII Digital Output; +2.048V Analog Output
- Thermocouple Short to ac Line: Internal Protection Provided to 300V peak (200V ac rms)
- Common Mode Voltage: 1400V peak (dc or ac), between Input and Power Line Ground (ac Versions)
- Common Mode Rejection Ratio: >130dB with 250Ω Source Imbalance (ac Versions); (dc to 60Hz)
- Normal Mode Rejection Ratio: >80dB @ 50/60Hz

DIGITAL OUTPUTS
- Character Serial ASCII
  Data: Nine transmitted characters, (each 7 bits plus strobe)
  Drive Capability: 2TTL loads, CMOS/TTL compatible
  Strobe: Negative transition determines when character serial data is valid. CMOS/TTL compatible.
  Character Rate: Selectable on P1 (pin 32)
  Grounded: 25 characters/sec. (SLOW)
  Open: 100 characters/sec. (FAST)
- Isolated Serial Output (Optional)
  Data: Asynchronous ASCII 20mA current loop
  (Optically isolated to ±600V peak)
  Baud Rate: Selectable on P1 (Pin 32)
  Grounded: 300 baud (SLOW)
  Open: 1200 baud (FAST)
  Distance: 10,000 ft. max
- Serial Output (Nonisolated, Optional)
  Data: Serial ASCII
  Drive Capability: 2TTL Loads, CMOS/TTL compatible
  Baud Rate: (same as Isolated Serial Output)
- Overrange: ±EEEE
- Minimum Time Between New Data Update: 150ms

DIGITAL INPUTS
- $\overline{\text{REQ}}$: Low-Level Triggered: Must go low at any time other than during data transmission to be recognized. $\overline{\text{REQ}}$ line taken low during data transmission will not be acknowledged and the ASCII digital output transmission will not occur. Display readings are not effected by $\overline{\text{REQ}}$.
- SERIAL INPUT (Optional): Edge Triggered, Current On to Current Off: Must be triggered at any time other than during data transmission to be recognized. Serial Input triggered during data transmission will not be acknowledged and the 20mA isolated/TTL compatible serial output transmission will not occur. Display readings are not effected by Serial Input.

ANALOG OUTPUT (OPTIONAL)
- Voltage: 1mV/degree, linearized
- Current: ±2mA max drive
- CMV: 1400V peak (ac or dc) Peak between Analog Output Ground & ac Power Line Ground
- Overrange: +2.048V, −0.512V

ACCURACY
- Temperature Resolution: 1°C/1°F
- All Ranges are Guaranteed Monotonic
- Range Temperature Coefficient: ±25ppm/°C typ, ±60ppm/°C max
- Readout Accuracy @25°C:

Sensor Type	Range	Accuracy	
J	−165°C to 760°C	±0.7°C	±1/2LSD
J	−265°F to 1400°F	±1.3°F	±1/2LSD
K	−50°C to 1250°C	±0.9°C	±1/2LSD
K	−58°F to 1999°F	±1.6°F	±1/2LSD
T	−150°C to 400°C	±0.8°C	±1/2LSD
T	−238°F to 752°F	±1.4°F	±1/2LSD
E	−100°C to 870°C	±1.0°C	±1/2LSD
E	−148°F to 1598°F	±2.0°F	±1/2LSD
S, R	+300°C to 1760°C	±1.5°C	±1/2LSD
	0° to 299°C	±6.0°C	± 1/2LSD
S, R	+572°F to 1999°F	±3.0°F	±1/2LSD
	+32°F to 571°F	±12.0°F	±1/2LSD

ANALOG TO DIGITAL CONVERSION
- Technique: Offset Dual Slope with Gain and Offset Error Correction
- Rate: 2.5 Conversions/Second Typical
- Input Integration Period: 100ms for 50/60Hz Noise Rejection

POWER REQUIREMENTS (Choice of Three Supply Ranges)
- ac: 90V ac to 132V ac @ 25mA (47Hz to 500Hz)
  198V ac to 264V ac @ 12.5mA (47Hz to 500Hz)
- dc: +7.5V to +28V dc @ 200mA (Protected Against Supply Reversals)

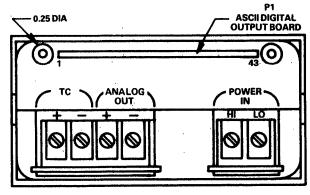
DISPLAY
- Type: Seven Segment Orange LED 0.56" (14.3mm) high
- Polarity Indication: "+" or "−" displayed
- Overrange Indication: ±EEE
- Display Test: At Power Turn-On, 3 Second Display of "+1888" Tests all Segments of Display

ENVIRONMENTAL
- Rated Temperature Range: +10°C to +40°C
- Operating Temperature Range: −10°C to +50°C
- Storage Temperature Range: −40°C to +85°C
- Relative Humidity: Meets MIL-STD-202E, Method 103B

DIMENSIONS
- Case: 3.78" × 1.89" × 5.13" (96.8mm × 48.9mm × 131.3mm), high impact molded plastic case. DIN/NEMA Standard
- Weight: 15.2 oz (431 grams) max, ac powered
  12.0 oz (341 grams) max, dc powered.

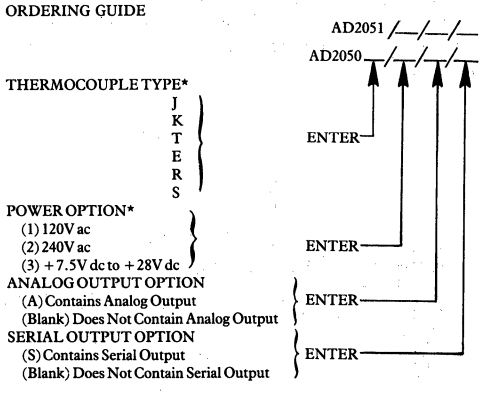
RELIABILITY
- Burn In: 168 Hours at +50°C and Power ON/OFF Cycles.
- Calibration: NBS Traceable
- Recalibration: Recommended 15-Month Intervals
- Warranty: 12 months

CONNECTOR
One 44 pin 0.1" (2.54mm) spacing card edge connector
Viking 3VH22/1 JN5 or equivalent
Optional: Order AC2630



Rear Panel View

ORDERING GUIDE



*Only one option can be ordered. The thermocouple type does not need to be specified when ordering the AD2051 since it is user programmable.

Specifications subject to change without notice.

Microprocessor-Based Autoranging RTD/Thermistor Meters

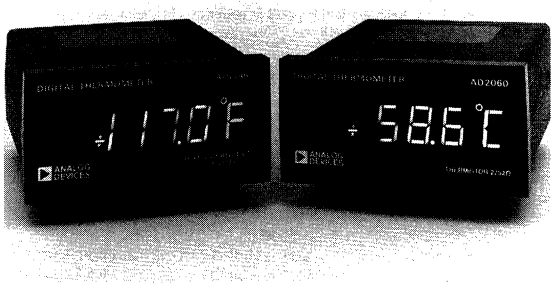
AD2060/AD2061

FEATURES

Temperature Ranges: −328°F to +1562°F
−200°C to +850°C
Autoranging: 0.1° from −199.9° to +199.9°; 1°≥200°
Sensor Selection (AD2060): RTD 100Ω Platinum
α = 0.00385, 0.00390, 0.00392 or 2252Ω Thermistor
Universal Meter (AD2061) Sensor User Programmable
Switch Selectable Sensor Configuration: 2, 3 or 4-Wire
7-Bit ASCII Character Serial Data Output
Automatic Self-Calibration for Gain, Offset, Excitation and Sensor Linearization
Optional Linearized Analog Voltage Output: 1mV/Degree
Optional Isolated 20mA ASCII Loop/TTL Serial Outputs

APPLICATIONS

Temperature Monitoring in Laboratory, Manufacturing and Quality Control Environments
Process Control Temperature Measurements
Remote Data Logging



GENERAL DESCRIPTION

The AD2060/AD2061 are high performance single channel 3½ digit RTD/Thermistor meters that can measure temperature accurately between −328°F and +1562°F (−200°C and +850°C). Both meters offer autoranging from 0.1°C/F to 1°C/F. The AD2060 is supplied factory programmed for one of four sensor types: 100Ω Platinum RTDs: α = 0.00385, 0.00390, 0.00392 or a 2252Ω Thermistor. The AD2061 is a universal meter in which the user selects one of the four sensor types via switch programming. The microprocessor based AD2060/AD2061 provides gain, offset and excitation error correction, linearization and °C/°F scaling in firmware. The AD2060/AD2061 display temperature information on large 0.56″(14.3mm) high LEDs. Digital information is provided in 7-bit standard ASCII character serial format with baud rate selection for easy interface to printers, terminals and other peripherals. For remote data acquisition applications, an optional isolated 2-wire 20mA ASCII serial loop/TTL compatible interface is available. For driving recorders or other analog instruments, an optional linearized analog voltage output of 1mV/degree is available. Selection of °C or °F scaling is accessed by removing the front panel lens and setting the selector switch to its proper position.

The AD2060/AD2061 can be ordered in one of the following power versions: 120V ac, 240V ac or +7.5V dc to +28.0V dc. Input voltage protection of 180V peak (RTD short to ac line), common-mode voltage to 1400V peak (ac version) with overrange and open sensor detection is provided. These meters are rated for operation over the 0 to +40°C temperature range. Each AD2060/AD2061 is burned-in for 168 hours @ 50°C with on/off power cycles for increased reliability.The AD2060/AD2061 are supplied in rugged molded plastic cases that meet UL94V-0 and DIN/NEMA standard dimensions.

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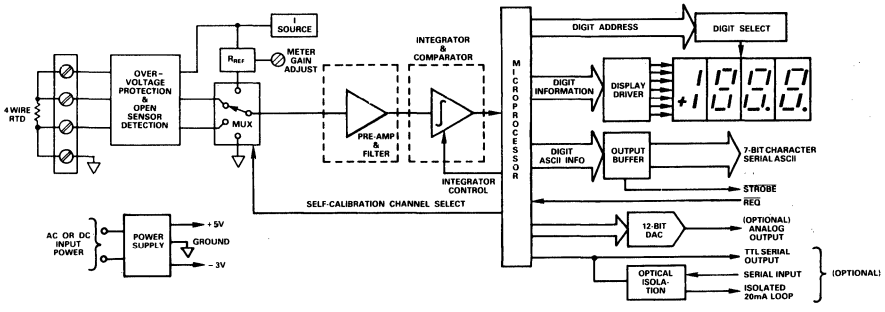
AD2060/AD2061 FUNCTIONAL BLOCK DIAGRAM



For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and rated supply voltages unless otherwise specified)

RTD INPUTS
- RTD Types: 100Ω Platinum
  α = 0.00385 (Per DIN 43760)
  α = 0.00390
  α = 0.00392
- Configuration: 2, 3 or 4 Wire
- Excitation Current: 0.25mA nominal
- External Lead
  Resistance Effect: Automatically Compensated for 3 & 4 wire configurations
- Lead Resistance: 50Ω/Lead max; RTD + Lead Resistance must be less than 400Ω
- 3 Wire Error: 2.8°C/Ω of impedance imbalance
- Open Sensor: DISPLAY +EEE
- RTD Short to ac Line: Internal protection provided to 180V peak (130V rms)
- Maximum Common-Mode Voltage: 1400V peak (ac or dc) between input and power line ground (ac version)
- Common-Mode Rejection Ratio: 100dB ac power to RTD input
- Normal Mode Rejection: 60dB @ 50/60Hz

THERMISTOR INPUTS
- Thermistor Type: Series 400 R = 2252Ω
- Configuration: 2 Wire
- Open Sensor: DISPLAY -EEE

ACCURACY
- Temperature Resolution: Autoranging (0.1° from −199.9° to +199.9°, 1°≥200°)
- All Ranges Guaranteed Monotonic
- Range Temperature Coefficient: 20ppm/°C typ, 30ppm/°C max
- Readout Accuracy* @ +25°C

Sensor	Range	Accuracy
100Ω RTD α = 0.00385	−200°C to +850°C	±0.3°C ± 1/2LSD
	−328°F to +1562°F	±0.6°F ± 1/2LSD
100Ω RTD α = 0.00392	−200°C to +640°C	±0.3°C ± 1/2LSD
	−328°F to +1184°F	±0.6°F ± 1/2LSD
100Ω RTD α = 0.00390	−200°C to +640°C	±0.3°C ± 1/2LSD
	−328°F to +1184°F	±0.6°F ± 1/2LSD
Thermistor R = 2252Ω	−30°C to +100°C	±0.4°C ± 1/2LSD
	−22°F to +212°F	±0.8°F ± 1/2LSD

*Readout Accuracy: Includes Gain and Offset Errors. Recommended Recalibration Interval 15-MONTHS.

DIGITAL OUTPUTS
- Character Serial ASCII
  Data: Eleven transmitted characters, (each 7 bits plus strobe)
  Drive Capability: 2TTL loads, CMOS/TTL compatible
  $\overline{\text{Strobe}}$: Negative transition determines when character serial data is valid. CMOS/TTL compatible.
  Character Rate: Selectable on P1 (Pin 32)
  Grounded: 25 characters/sec. (SLOW)
  Open: 100 characters/sec. (FAST)
- Isolated Serial Output (Optional)
  Data: Asynchronous ASCII 20mA current loop (Optically isolated to ±600V peak)
  Baud Rate: Selectable on J1 (Pin 32)
  Grounded: 300 baud (SLOW)
  Open: 1200 baud (FAST)
  Distance: 10,000 ft. max
- Nonisolated Serial Output (Optional)
  Data: Serial ASCII
  Drive Capability: 2TTL Loads, CMOS/TTL compatible
  Baud Rate: (same as Isolated Serial Output)
- Overrange: ±EEE.E
- Minimum Time Between New Data Update: 150ms

DIGITAL INPUTS
- $\overline{\text{REQ}}$: Low-Level Triggered: Must go low at any time other than during data transmission to be recognized. $\overline{\text{REQ}}$ line taken low during data transmission will not be acknowledged and the ASCII digital output transmission will not occur. Display readings are not effected by $\overline{\text{REQ}}$.
- $\overline{\text{SERIAL INPUT}}$ (Optional): Edge Triggered, Current On to Current Off: Must be triggered at any time other than during data transmission to be recognized. $\overline{\text{Serial Input}}$ triggered during data transmission will not be acknowledged and the 20mA isolated/TTL compatible serial output transmission will not occur. Display readings are not effected by $\overline{\text{Serial Input}}$.

ANALOG OUTPUT (OPTIONAL)
- Voltage: 1mV/degree, linearized
- Current: ±2mA max drive
- CMV: 1400V peak (ac or dc) between Analog Output Ground & ac Power Line Ground
- Overrange: +2.048V, −0.512V
- Accuracy: ±2mV from Display Reading

ANALOG TO DIGITAL CONVERSION
- Technique: Offset Dual Slope with Gain and Offset Error Correction
- Rate: 2.5 Conversions/Second Typical
- Input Integration Period: 100ms for 50/60Hz Noise Rejection

POWER REQUIREMENTS (Choice of Three Supply Ranges)
- ac: 90V ac to 132V ac @ 25mA (47Hz to 500Hz)
  198V ac to 264V ac @ 12.5mA (47Hz to 500Hz)
- dc: +7.5V to +28V dc @ 200mA (Protected Against Supply Reversals)

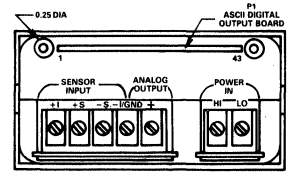
DISPLAY
- Type: Seven Segment Orange LED 0.56" (14.3mm) high
- Polarity Indication: "+" or "−" displayed
- Overrange Indication: ±EEE
- Display Test: At Power Turn-On, 3 Second Display of "+188.8." Tests all Segments of Display

ENVIRONMENTAL
- Rated Temperature Range: 0 to +40°C
- Operating Temperature Range: −10°C to +50°C
- Storage Temperature Range: −40°C to +85°C
- Relative Humidity: Meets MIL-STD-202E, Method 103B (0 to 90%, Noncondensing)

DIMENSIONS
- Case: 3.78" × 1.89" × 5.13" (96.8mm × 48.9mm × 131.3mm), rugged molded plastic case. Meets UL94V-0 and DIN/NEMA Standard dimensions
- Weight: 15.2 oz (431 grams) max, ac powered
  12.0 oz (341 grams) max, dc powered.

RELIABILITY
- MTBF: >55,000 hours calculated
- Burn In: 168 Hours at +50°C and Power ON/OFF Cycles.
- Calibration: NBS Traceable
- Recalibration: Recommended 15-Month Intervals
- Warranty: 12 months

CONNECTOR
One 44 pin 0.1" (2.54mm) spacing card edge connector Viking 3VH22/1 JN5 or equivalent
Optional: Order AC2630



Rear Panel View

ORDERING GUIDE

AD2061 /_/_/_

AD2060 /_/_/_/_/_

SENSOR TYPE*
- (385) 100Ω Platinum RTD α = 0.00385
- (390) 100Ω Platinum RTD α = 0.00390
- (392) 100Ω Platinum RTD α = 0.00392

} ENTER

- (2252) Thermistor R = 2252Ω

POWER OPTION*
- (1) 120V ac
- (2) 240V ac
- (3) +7.5V dc to +28V dc

} ENTER

ANALOG OUTPUT OPTION
- (A) Contains Analog Output
- (Blank) Does Not Contain Analog Output

} ENTER

SERIAL OUTPUT OPTION
- (S) Contains Serial Output
- (Blank) Does Not Contain Serial Output

} ENTER

*Only one option can be ordered. The sensor type does not need to be specified when ordering the AD2061 since it is user programmable.

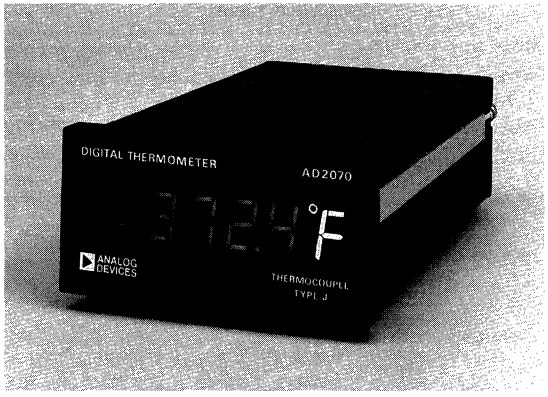
Specifications subject to change without notice.

Microprocessor-Based Autoranging Thermocouple Meters

AD2070/AD2071

FEATURES

- **Autoranging (0.1° – 1°)**
- **4 1/2 Digit Resolution**
- **Automatic Self-Calibration for Gain, Offset, Cold Junction Compensation and Thermocouple Linearization**
- **J, K, T, E, R, S, C, B, J DIN, and T DIN Thermocouple Selection**
- **Universal Meter (AD2071), User Programmable for All Thermocouple Types**
- **Four Port Isolation: Input, Power, Digital Output and Analog Output**
- **Optional Isolated and Linearized Analog Voltage Output 1mV/Degree**
- **Optional Isolated 20mA Loop/TTL Serial Data Output**
- **Optional Isolated RS-232/TTL Serial Data Output**
- **Heavy Gauge Rugged Metal Case**



GENERAL DESCRIPTION

The AD2070/AD2071 are high performance, microprocessor based, autoranging, single channel thermocouple meters that can measure temperature accurately from −328°F to +4200°F (−200°C to +2315°C). The AD2070 is supplied factory programmed for any of the following ten thermocouple types: J, K, T, E, R, S, C, B, J DIN, and T DIN. The AD2071 is a universal meter in which the user selects one of the ten thermocouple types via switch programming. Both meters offer autoranging from 0.1°C/°F to 1°C/°F. The microprocessor based AD2070/AD2071 provides gain and offset error correction, cold junction compensation, thermocouple linearization and °C/°F scaling in firmware.

The AD2070/AD2071 display temperature information on large 0.56″ (14.3mm) high LEDs. Digital information is provided in standard ASCII character serial format with rate selection for easy interface to printers. For remote data acquisition applications, an optional isolated 20mA serial loop or RS-232 compatible interface is available. For driving recorders or other analog instruments, an optional isolated and linearized analog voltage output of 1mV/degree is available. Selection of °C or °F scaling is accessed by removing the front panel lens and setting a selector switch.

The AD2070/AD2071 can be ordered in one of the following power versions: 120V ac, 240V ac or +7.5V dc to +28.0V dc. Input overvoltage protection rating is 300V peak (thermocouple to ac line shorts). The common-mode voltage rating is 1400V peak. Overrange and open thermocouple detection are provided in all models. Analog output and digital outputs are isolated to 500V peak from power, input and output sections. Each meter is burned-in for 168 hours at 50°C with on/off power cycles for increased reliability. These meters are rated for operation over a +10°C to +40°C range. The AD2070/AD2071 are supplied in a heavy gauge, rugged metal case that meets DIN/NEMA standard dimensions.

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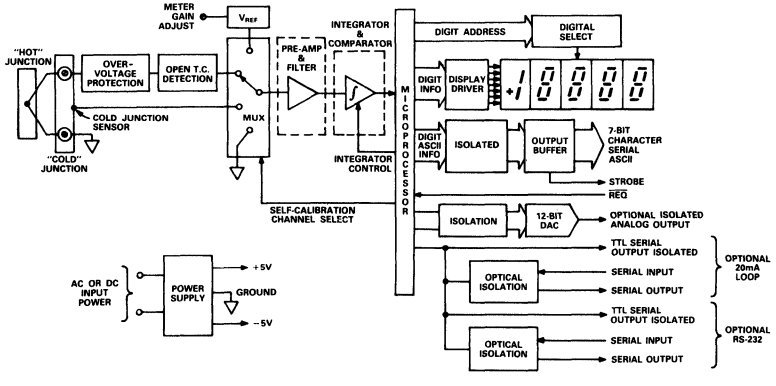
AD2070/AD2071 FUNCTIONAL BLOCK DIAGRAM



For detailed information, contact factory.

SPECIFICATIONS (typical @ +25°C and rated supply voltages unless otherwise specified)

THERMOCOUPLE INPUTS

THERMOCOUPLE TYPES:
J, K, T, E, R, S, B, C, J DIN and T DIN
INPUT IMPEDANCE:
100MΩ
EXTERNAL LEAD RESISTANCE EFFECT:
<20μV per 350Ω of Lead resistance
COLD JUNCTION COMPENSATION ERROR:
±0.3°C max (+10°C to +40°C)
OPEN THERMOCOUPLE:
+EEEE Display; +EEEE.E ASCII DIGITAL OUTPUT: +3.500V
ANALOG OUTPUT
THERMOCOUPLE SHORT TO AC LINE:
Internal Protection Provided to 300V peak, (200V ac rms)
COMMON-MODE VOLTAGE:
1400V peak (dc or ac), Between Input and Power Line Ground
COMMON-MODE REJECTION RATIO:
>130dB with 250Ω Source Imbalance (dc to 60Hz)
NORMAL-MODE REJECTION RATIO:
>80dB @ 50/60Hz

DIGITAL OUTPUTS

ISOLATED CHARACTER SERIAL ASCII (Standard)
DATA:
Eleven transmitted characters, each 7 bits plus strobe
DRIVE CAPABILITY:
2TTL Loads, CMOS/TTL compatible
OVERRANGE: ±EEEE.E
STROBE:
Positive transition determines when character serial data is valid. CMOS/TTL compatible.
ISOLATION:
500V Between Input, Analog Output and Power Input
CHARACTER RATE:
Selectable on P1 (Pin 20)
Grounded: 25 Characters/sec. (SLOW)
Open: 100 Characters/sec. (FAST)

ISOLATED SERIAL OUTPUT (Optional)
DATA:
Asynchronous ASCII 20mA current loop or RS-232
BAUD RATE:
Selectable on P1 (Pin 20)
Grounded: 300 baud (SLOW)
Open: 1200 baud (FAST)
OVERRANGE:
±EEEE.E
DISTANCE:
50 ft. (RS-232), 10,000 ft. (20mA loop)
ISOLATION:
500V Between Input, Analog Output and Power Input

ISOLATED SERIAL OUTPUT
DATA:
Serial ASCII TTL
DRIVE CAPABILITY:
2TTL Loads, CMOS/TTL Compatible
BAUD RATE:
(same as above)
OVERRANGE:
±EEEE.E
ISOLATION:
500V Between Input, Analog Output and Power Input
MINIMUM TIME BETWEEN NEW DATA UPDATE:
100ms

DIGITAL INPUTS

$\overline{\text{REQ}}$: LOW-LEVEL TRIGGERED:
Must go low at any time other than during data transmission to be recognized. $\overline{\text{REQ}}$ line taken low during data transmission will not be acknowledged and the ASCII digital output transmission will not occur. Display readings are not effected by $\overline{\text{REQ}}$.

$\overline{\text{SERIAL INPUT}}$: EDGE TRIGGERED, CURRENT ON TO CURRENT OFF
Must be triggered at any time other than during data transmission to be recognized. $\overline{\text{Serial Input}}$ triggered during data transmission will not be acknowledged and the isolated 20mA loop/TTL or isolated RS-232/TTL compatible serial output transmission will not occur. Display readings are not effected by $\overline{\text{Serial Input}}$.

ISOLATED ANALOG OUTPUT (OPTIONAL)

VOLTAGE:
1mV/degree, Fahrenheit or Celsius linearized
CURRENT:
±2mA max
OVERRANGE:
+3.500V, −0.328V
ACCURACY:
±2mV from Display Reading
ISOLATION:
500V Between Input, Digital Output and Power Input

ACCURACY

TEMPERATURE RESOLUTION:
Autoranging 0.1°C/°F – 1°C/°F
RANGE TEMPERATURE COEFFICIENT:
20ppm/°C typ, ±40ppm/°C max (of Reading)
All Ranges are Guaranteed Monotonic.

POWER REQUIREMENTS (Choice of Three Supply Ranges)

ac:
90V ac to 132V ac @ 25mA (dc to 1kHz)
198V ac to 264V ac @ 12.5mA (dc to 1kHz)
dc:
+7.5V to +28V dc @ 600mA (Protected Against Supply Reversals)

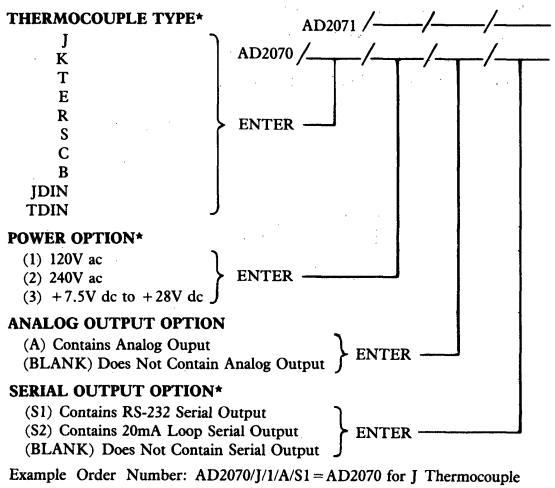
DISPLAY

TYPE:
Seven Segment Orange LED 0.56" (14.3mm) high
POLARITY INDICATION:
"+" or "−" displayed
OVERRANGE INDICATION:
±EEEE
DISPLAY TEST:
At Power Turn-On, 3 Second Display of "+1888.8." Tests All Segments of Display

DIMENSIONS

CASE:
3.78" × 1.89" × 6.75" (96.8mm × 48.0mm × 171.0mm), rugged aluminum case. DIN/NEMA Standard.
PANEL CUT OUT: $3.622^{+0.031}_{-0.000}$" $(92^{+,8}_{-,0})$mm × $1.771^{+0.024}_{-0.000}$ $(45^{+,6}_{-,0})$mm
PANEL THICKNESS:
1/16" (1.5mm) to 3/16" (4.8mm)
WEIGHT:
23 oz. (650 grams) typ

ORDERING GUIDE



Example Order Number: AD2070/J/1/A/S1 = AD2070 for J Thermocouple Type, 120V ac Power, Analog Voltage Output and RS-232 Serial Output.

*Only one option can be ordered. The thermocouple type does not need to be specified when ordering the AD2071 since it is user programmable.

Specifications subject to change without notice.

Bus Interface & Serial I/O Products

THE μMAC® SERIES

The μMAC product line consists of data acquisition and control front ends designed for use in industrial applications. The systems provide signal conditioning, A/D and D/A conversion and control capabilities in front of a supervisory computer or in a stand-alone configuration. Two general groups of systems are available: intelligent, fixed function systems and programmable stand-alone systems.

Fixed-Function Front Ends

The fixed function systems are the μMAC-4000 and the μMAC-1050. The μMAC-4000 system provides isolation and conditioning of signals, A/D and D/A conversion, and storage of data (in engineering units) that is transferred to any host computer upon command (via RS-232 link). The μMAC-1050 offers additional levels of functionality such as minimum/maximum recording, local alarming, CAM sequence emulation, configuration storage in EEPROM, ramping of analog outputs, and other features that minimize host computer interaction. The unit also supports an RS-422/485 port for multidrop configurations.

Software driver options are available for both the μMAC-4000 and μMAC-1050 to provide a high level language interface to the units. Refer to the chart for more detailed information.

Programmable Units

The programmable μMAC units are the μMAC-1060, μMAC-5000, μMAC-6000, and the μDCS-6000. The μMAC-5000 and μMAC-6000 are fully programmable in μMACBASIC® or C (μMAC-6000 only) and support battery-backed data and program storage, hardware watchdog timers, and serial communications for stand alone operation or custom host interface.

The μMAC-1060 is a single board controller that offers unprecedented price/performance levels. The unit is programmable in a fast, space efficient version of C, and also provides a watchdog timer, battery-backed memory, and up to three serial ports.

The μDCS-6000 provides a complete solution for distributed process monitoring and control applications. Based on the μMAC-6000 hardware, the system becomes a powerful controller with embedded FIX DMACS* software from Intellution.

THE RTI® SERIES

The RTI Series consists of analog and digital input/output boards that are compatible with popular microcomputer bus standards including:

- RTI-800 Series, IBM PC/XT/AT*
- RTI-200 Series, IBM PS/2,* Micro Channel* Architecture
- RTI-1200 Series, STD
- RTI-600 Series, VMEbus
- RTI-700 Series, MULTIBUS*

The RTI Series are families of boards that provide a wide range of functionality. Each board can operate independently or can be used with other RTI Series boards to solve an application. Different analog-to-digital conversion speeds, resolutions, input and output channel capacities are available, allowing customization of the systems. The RTI Series are typically used in applications where the computer is close to the sensors being measured.

RTI Software

The RTI-200 Series, RTI-800 Series and some of the RTI-1200 Series boards are supported by MS-DOS* driver software that provides easy-to-use, high-level routines for user written software programs. The routines can be called from popular languages like Microsoft* BASIC (Interpreted and Compiled), C, QuickBASIC,* Borland International TURBO Pascal* and TURBO C.*

Industry standard data acquisition and control software products like LABTECH NOTEBOOK,* LABTECH CONTROL,* SNAPSHOT STORAGE SCOPE,* Control EG,* THE FIX,* and UnkelScope* support many of the RTI Series boards.

Signal Conditioners

The μMAC and RTI products can be used with signal conditioners in applications that require conditioning for isolated or nonisolated signals. The 3B and 5B Series of signal conditioning modules and the STB family of analog signal conditioning panels can be used with most RTI and μMAC products.

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Selection Guide
Bus Interface & Serial I/O Products

IBM PC/XT/AX I/O Boards

		Analog Input				Analog Output		Digital I/O		
Model	Function	Analog Input Channels	Resolution	Max Throughput XT	Max Throughput AT	Analog Output Channels	Resolution	Channels	Time-Related	Other Features
RTI-800 RTI-800-A RTI-800-F	Analog Input and Digital I/O	16 SE/8 DI 16 SE/8 DI 16 SE/8 DI	12-Bit 12-Bit 12-Bit	31 kHz 58 kHz 91 kHz	27 kHz 58 kHz 58 kHz			8 In/8 Out 8 In/8 Out 8 In/8 Out	3 Counter/Timers 3 Counter/Timers 3 Counter/Timers	Analog Input Expandable to 32 SE/16 DI PGA External Digital Trigger
RTI-802-4 RTI-802-8	Analog Output					4 8	12-Bit 12-Bit			Remote Sensing
RTI-815 RTI-815-A RTI-815-F	Multifunction Analog and Digital I/O	16 SE/8 DI 16 SE/8 DI 16 SE/8 DI	12-Bit 12-Bit 12-Bit	31 kHz 58 kHz 91 kHz	27 kHz 58 kHz 58 kHz	2 2 2	12-Bit 12-Bit 12-Bit	8 In/8 Out 8 In/8 Out 8 In/8 Out	3 Counter/Timers 3 Counter/Timers 3 Counter/Timers	Analog Input Expandable to 32 SE/16 DI PGA External Digital Trigger
RTI-817	Digital I/O							Three 8-Bit Ports		External Strobing Interrupts on Change of State
RTI-820	Modular Analog and Digital I/O	Up to 64	12-Bit	19 kHz	19 kHz	Up to 16	12-Bit	Three 8-Bit Ports		Interfaces Directly to Analog Signal Conditioning Panels; Slave Microprocessor Controls Analog Outputs
RTI-827	Frequency Input, Event Counting, Pulse Output							Three Outputs One 4-Bit Port	5 Counter/Timers	Debounce Circuitry on on Inputs External Interrupts
RTI-850-F	High Resolution Analog Input	8 DI	16-Bit 15-Bit 14-Bit	N/A N/A N/A	71 kHz 76 kHz 76 kHz					On-Board Memory Extensive Analog and Digital Triggering
RTI-860	High Speed Simultaneous Analog Input	16 SE	12-Bit 8-Bit	N/A N/A	250 kHz 330 kHz					On Board Memory Extensive Analog and Digital Triggering
RTI-870	Ultrahigh Resolution	4 DI	22-Bit	20 Hz				Two 4-Bit Ports		

Selection Guide
Bus Interface & Serial I/O Products

STD BUS Compatible I/O Boards

		STD BUS (NMOS)								STD BUS (CMOS)			
	Analog Devices Part Number	**RTI-1226**	**RTI-1225**	**RTI-1260**	**RTI-1262**	**RTI-1265**	**RTI-1266**	**RTI-1267**	**RTI-1270**	**RTI-1280**	**RTI-1281**	**RTI-1282**	**RTI-1287**
Board Type	Input	•		•		•			•	•			
	Input/Output		•				•	•			•		•
	Output				•							•	
Channel Capacity	Input (Single Ended/ Differential)	16/8	16/8	32/16		64	64	24 Digital I/O	16/16	16/8	16/8		24 Digital I/O
	Output		2		4		16				2	4 or 8	
Input Resolution	10 Bits	•	•										
	12 Bits			•		•	•		•	•	•		
Output Resolution	8 Bits		•										
	12 Bits				•		•				•	•	
Additional Features													
Programmable Gain Amplification				•						•	•		
Single +5 V Operation		•	•	•	•	•	•	•	•	•	•	•	•
4–20 mA Output					•							•	
Direct Sensor Interface													
Thermocouples, RTDs						•	•		•				
IBM PC Software Compatible						•	•	•					

IBM PS/2 Micro Channel I/O Boards

		Analog Input			Analog Output		Digital I/O		
Model	Function	Analog Input Channels	Resolution	Max Throughput	Analog Output Channels	Resolution	Channels	Time Related	Other Features
RTI-204	Low Cost Analog Input and Digital I/O	8 SE	12-Bit	19 kHz	0	N/A	8 Bits	2 Counter/Timers	Digital Pattern Recognition
RTI-205	Low Cost Multifunction Analog and Digital I/O	8 SE	12-Bit	19 kHz	2	12-Bit	8 Bits	2 Counter/Timers	Digital Pattern Recognition
RTI-817	Digital I/O	0	N/A	N/A	0	N/A	Four 8-Bit Ports	0	Interrupt on Change of State; External Strobing and Interrupt Support
RTI-220	Analog I/O	Up to 64	12-Bit	21 kHz	Up to 16	12-Bit	0	0	Interfaces Directly to Analog Signal Conditioning Panels; Slave Microprocessor Controls Analog Outputs
RTI-222	Analog Output	0	N/A	N/A	Up to 16	12-Bit	0	0	Interfaces Directly to Analog Signal Conditioning Panels; Slave Microprocessor Controls Analog Outputs

Selection Guide
Bus Interface & Serial I/O Products

VMEbus Compatible I/O Boards

	Analog Devices Part Number	VMEbus RTI-600	VMEbus RTI-602
Board Type	Input	•	
	Input/Output		
	Output		•
Channel Capacity	Input (Single Ended/ Differential)	32/16	
	Output		4
Input Resolution	10 Bits		
	12 Bits	•	
Output Resolution	8 Bits		
	12 Bits		•
Additional Features			
Programmable Gain Amplification		•	
Single +5 V Operation		•	•
4–20 mA Output			•
Direct Sensor Interface Thermocouples, RTDs			

Multibus Compatible I/O Boards

	Analog Devices Part Number	MULTIBUS RTI-711	MULTIBUS RTI-724	MULTIBUS RTI-732
Board Type	Input	•		
	Input/Output			•
	Output		•	
Channel Capacity	Input (Single Ended/ Differential)	32/16		32/16
	Output		4	2
Input Resolution	10 Bits			
	12 Bits	•		•
Output Resolution	8 Bits			
	12 Bits		•	•
Additional Features				
Programmable Gain Amplification		•		•
Single +5 V Operation		•	•	•
4–20 mA Output				•
Direct Sensor Interface Thermocouples, RTDs				

µMAC Series

	µMAC-1050	µMAC-4000	µMAC-5000	µMAC-6000	µMAC-1060	µDCS-6000
Programming	Fixed Function (PC Programming in C, Basic Pascal, 3rd Party Packages)	Fixed Function	µMACBASIC	µMACBASIC, C	C	FIX DMACS
Max RAM	N/A	N/A	128K	256K		256K
# Comm Ports						
Serial	1	1	2	3		3
IEEE-488	None	None	None	1		None
Max I/O Points						
AIO	48 AIN, 10 AOT	48 AIN, 32 AOT	100+*	350+*		350+*
DIO	64	272	304	1024		1024
Resolution (Bits)	18 Bits	13 Bits	11/14 Bits	12/14 Bits	13–18 Bits	12/14 Bits
Data Acquisition Rate per Channel	15	15	50/25	2800/1400 (C)	400–44	10

*Input/Output capability depends on configuration.

Automotive Components

This section contains solid-state sensors and sensor signal conditioners designed specifically for automotive applications. The solid-state sensors integrate one or more sensors with signal conditioning circuitry and a complete output interface onto a single monolithic IC. The ability to work from typical automotive voltage supplies over wide temperature ranges, together with the benefits of advanced signal conditioning, make the products inherently user friendly.

The devices in this section represent several years of market research and product development in a cooperative effort with major customers in the automotive industry. While ideally suited for automotive applications, many of the products are attractive for nonautomotive applications as well. All products are available as described or can be modified for custom volume applications.

SOLID-STATE SENSOR PRODUCT CONCEPT

In order to achieve significant improvement in automotive sensors, Analog Devices utilizes its knowledge and expertise in process technology, signal conditioning circuitry, and laser trimmable on-chip thin film resistors. This allows the sensor and signal conditioning circuitry to be brought onto one and the same IC resulting in the following benefits:

1. *Higher signal resolution* is achieved by combining the sensor and signal conditioner to get a high level output (for example linear 0 V to 5 V) which can be transferred with high noise immunity to the microcontroller.

   This is an improvement over traditional sensors which transfer low level outputs (for example 100 mV) across long transfer lines between the sensor and microcontroller with significant loss of resolution.

2. *Increased accuracy and linearity* are attained by using on-chip smart compensation circuitry and linear signal processing to compensate for all major sensor errors and unwanted drifts over temperature and time.

3. *Standard signal interfaces* include voltage (for example 0 V to 5 V), current, or digital signal outputs. This increases the possibility of sharing the solid-state sensor with more than one controller unit.

AUTOMOTIVE POWER SUPPLY CONSIDERATIONS

Many of Analog Devices' solid-state sensors are designed to operate directly from the car battery, and thus withstand the inherent harsh conditions present from an unregulated and unprotected power supply. Other members of the sensor family are designed to use the existing +5 V regulated power supply from the microcontroller PC board.

The car battery voltage, nominally +12 V, is a dc voltage which varies between +8.5 V and +14.6 V during normal operating conditions. However, in some cases, the battery voltage can drop far below +8.5 V (for example, during engine start in winter) or can go above +14.6 V (for example, when the alternator charge controller fails). Some systems must remain operative even under these harsh conditions, and all systems should remain undamaged.

Other situations which need to be considered are:
- reversed power supply (incorrectly installed battery)
- double battery voltage (jump start)
- voltage transients in the range of ±60 V to ±100 V
- load dump
- EMI (electromagnetic interference)

OPERATING TEMPERATURE RANGE

Automotive sensors must operate over a wide temperature range. Typical requirement include:

Passenger Compartment The minimum temperature rises above 0°C almost immediately after the car has been started.	−40°C to +85°C
Engine Compartment Temperatures may exceed 150°C or even 180°C depending on ventilation.	−40°C to +125°C
Trunk and Chassis	−40°C to +110°C
Brake Systems This may extend to +250°C depending on location and ventilation.	−40°C to +180°C

All of the devices in this section meet the temperature range of −40°C to +125°C. Many of the products extend to +150°C, and Analog Devices is continuing developments to increase the temperature range to +180°C and beyond.

FUTURE DEVELOPMENTS

Analog Devices is continuing to develop new solid-state sensors and signal conditioning circuits, both general purpose and application specific (ASIC). We will continue to seek direction from key automotive system designers to develop and produce products that will enhance the next generation of automobiles.

AD22001* – 5-Channel Monolithic Comparator for Lamp Monitoring

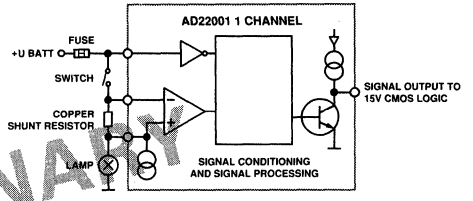
FEATURES
Continuous Status Checks of Five Bulbs
Lamp Status Check In "On" and "Off" State
Status Checks of Two In-Line Fuses
Very Low Voltage Drop at Sensor Shunt Resistor (Nominal 1.75 mV at 22°C)
Temperature and Supply Voltage Compensated
Can Be Powered Directly from Car Battery
Operating Temperature Range: −40°C to +125°C
15 V CMOS Compatible Digital Outputs Signals
Voltage Limited Power Supply Output for 15 V CMOS Logic ICs

The AD22001 is a monolithic, five channel comparator circuit for monitoring the functionality of various lamps in automotive applications.

The basic function of the IC is to test the series circuit leading to the lamp to determine if the circuit is intact and a functional lamp is in the socket. The AD22001 continuously checks the status of four to five bulbs in either their "on" or "off" state, and also tests for the presence of an in-line fuse in two of the series circuits.

Patents pending.

Digital outputs indicate the status of each channel. Additionally, the AD22001 provides a voltage limited power supply output to supply 15 V CMOS circuits that may interface to the AD22001.



Typical Application Circuit For a Single Channel Lamp Monitor

AD22100* – Monolithic Temperature Sensor with Signal Conditioning

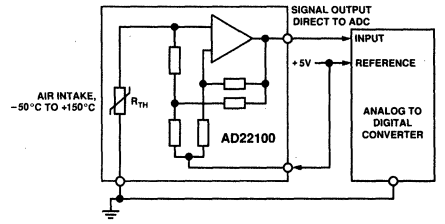
FEATURES
200°C Temperature Span
Accuracy Better Than 2% of Full Scale
Linearity Better Than ±2°C
Ratiometric Output Voltage – Output Proportional to Temperature × Supply Voltage
Reverse Voltage Protection
Low Quiescent Current – Minimal Self-Heating
High Level, Low Impedance Output
22.5 mV/°C from +5.000 V Supply
Wide Power Supply Range

The AD22100 is a monolithic temperature sensor with on-chip signal conditioning. It covers the range −50°C to +150°C making it ideal for use in a wide range of automotive applications, including both liquid and air temperature measurement.

The signal conditioning obviates the need for any trimming, buffering or linearization circuitry, greatly simplifying the overall system design.

Patents pending.

The output voltage, which is proportional to the temperature times the supply voltage, can be input directly to an analog-to-digital converter, which can use the AD22100 supply voltage as its reference.



Typical Application Circuit

This information applies to products under development. Their characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD22050* – Single-Supply Sensor Interface Circuit

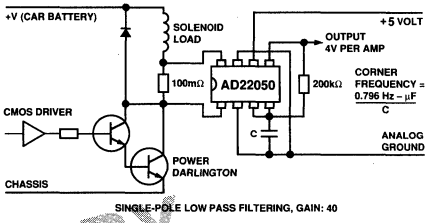
FEATURES
Gain of ×20 Alterable from ×1 to ×160
Input CMR from Ground to 6× (V_S −1 V)
Output Span 10 mV to (V_S −0.2) V
1-, 2-, 3-Pole Low Pass Filtering Available
Accurate Midscale Offset Capability
Differential Input Resistance 400 kΩ
Drives 1 kΩ Load to +4 V Using V_S = +5 V
Transient Spike Protection & RFI Filters Included
Operating Temperate Range −40°C to +125°C

APPLICATIONS
Current Sensing
Motor Control
Interface for Pressure Transducers, Position Indicators, Strain Gages, and Other Low Level Signal Sources

The AD22050 is a single supply difference amplifier for amplifying and low pass filtering small differential voltages (typically 100 mV FS at a gain of 40) from sources having a large common-mode voltage.

Supply voltage of between +3.0 V and +36 V can be used. The input common-mode range extends from ground to over +24 V using a +5 V supply with excellent rejection of this common-mode voltage. This is achieved by the use of a special resistive attenuator at the input, laser trimmed to a very high differential balance.

Provisions are included for optional low pass filtering and gain adjustments. An accurate mid-scale offset feature allows bipolar signals to be amplified.



Typical Application Circuit for a Current Sensor Interface

*Patents pending.

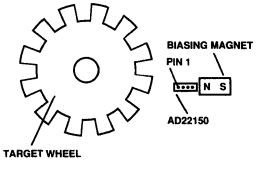
AD22150* – Monolithic Hall Effect Sensor with Signal Conditioning

FEATURES
Sensitive to Small Changes in Field: Operate and Release Points at −12 G and +12 G Respectively
Switch Points Moved in Presence of Large Dynamic Fields (Up to ±200 G)
Open Collector Output
Stable Over −40°C to +150°C Temperature Range
Hysteresis Built Into the Output
Maximum Frequency 50 kHz
Minimum Frequency User Selectable with One External Capacitor
Powered Directly by Automobile Battery

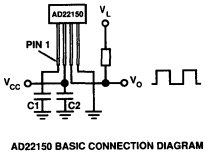
The AD22150 is a monolithic Hall effect sensor complete with signal conditioning circuitry, which is sensitive to changes in magnetic field provided, for example, by teeth on a moving ferrous wheel.

When used in a biasing magnetic field, the ac coupling rejects the steady state field to provide precisely controlled switch points, while hysteresis of the output ensures bounce free transitions between states.

The AD22150 is stable over a wide temperature range and has a broad frequency response. Its tolerance of assembly inaccuracies and its immunity to surface roughness combine to give a part ideal for use in diverse applications.



Typical Application Circuit



AD22150 Basic Connection Diagram

*Patents pending.

AD22180* – Automotive Battery Monitor Circuit

FEATURES
Measures Automotive Battery Temperature & Voltage
Built-In Battery Charging Characteristic
Provides a Signal to Maximize the Battery Charging Without Exceeding the Battery Gassing Voltage at Any Given Temperature
Signals "Charge Battery" for Battery Voltage Below the Battery Voltage Characteristics of the Figure: 13.35 V @ 40°C +35 mV/°C for Temperatures Below 40°C and −11 mV/°C Above 40°C
TTL Compatible Open Collector Output
Output Short Circuit Protected
No External Components Required
Powered Directly by Automobile Battery with Transient and Reverse Voltage Protection
Operating Temperature Range −55°C to +125°C

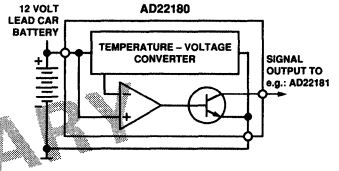
The AD22180 is a three-terminal, monolithic monitor circuit for 12 V, lead based, automotive batteries.

The basic function of this IC is to measure the battery voltage and temperature. The measured voltage and temperature will then be compared with the internal battery charging curve. This IC should be mounted in thermal contact with the battery case.

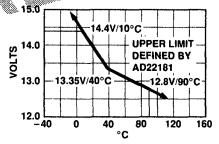
***Protected by U.S. Patent Re30,586; others pending.**

The digital open collector output indicates when the battery can be further charged without damaging or reducing its lifetime (digital state: high), and when to stop charging (digital state: low).

The digital output of the AD22180 can be directly connected to the Alternator Controller Circuit AD22181.



Typical Application Circuit



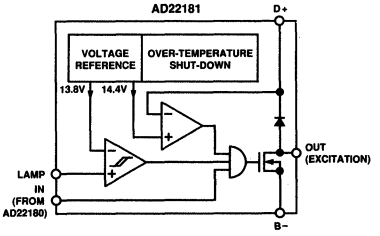
Temperature-Voltage Characteristics

AD22181* – Alternator Control Circuit

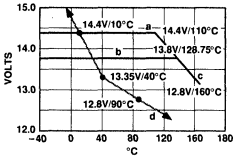
FEATURES
Directly Controls Alternator Excitation
Temperature Invariant Charging Voltage Limiter
Over-Temperature Protective Shutdown
Remote Sensed Headlamp Voltage Charging Limit
Interface for Battery Temperature – Voltage Charge Control Using AD22180
Fail-Safe Operation
Acceleration Cut-Off Mode

The AD22181 is a 4-pin hybrid device to control an automobile alternator. The AD22181 and AD22180 work together to provide a complete charging control system designed to maximize battery charge without damaging the battery, alternator, headlamps, or electrical system, due to overvoltage or extreme temperature.

The AD22181 contains sensors, control circuitry, and a power transistor to control the excitation to the alternator based on the following input parameters: AD22180 output (car battery voltage and temperature control), alternator temperature (to avoid extreme temperatures), headlamp voltage (to avoid overvoltage to headlamps when they are in "on" condition), and alternator voltage (fail-safe mechanism to avoid overvoltage to the electrical system in case the signal from the AD22180 is lost).



Typical Application Circuit



a) FIXED UPPER LIMIT FOR BATTERY VOLTAGE
b) FIXED CHARGING LIMIT HEADLAMP VOLTAGE
c) OVER-TEMPERATURE SHUT-DOWN
d) BATTERY VOLTAGE vs TEMPERATURE CHARGING LIMIT FROM AD22180

Temperature-Voltage Characteristics

***Protected by U.S. Patent Re30,586; others pending.**

Application Specific Integrated Circuits

Analog Devices offers a full spectrum of capabilities in mixed-signal application specific integrated circuits (ASICs). These chip-level systems can implement combined analog/digital designs with 12-bit accuracy and 16-bit resolution that formerly required board-level solutions.

Analog Devices can incorporate most of the functions of its standard monolithic parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a predefined system-on-a-chip known as a Linear System Macro to your application.

Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, England and Ireland.

Multiple locations for fabrication, assembly and testing ensure a ready supply of production parts. Products can be processed in full MIL-38510 certified facilities.

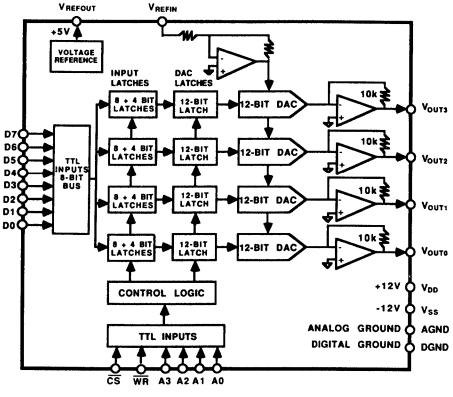
DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASIC parts. Described here are three Linear System Macros, a custom chipset and a semicustom chip.

AD75004 Quad DAC

This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously.

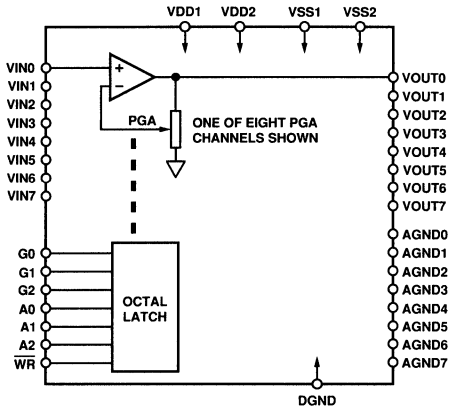
AD75004 QUAD DAC



AD75068 Octal Programmable Gain Amplifier

The AD75068 contains eight programmable gain amplifiers (PGAs). Each is complete, including switch/resistor network and gain programming latch, and requires no external components. Each channel may be independently programmed for gains from 1 to 128. A unique circuit design maintains constant 2 MHz bandwidth at all gains and offers very low phase shift; the PGAs also feature low input bias current (<10 pA).

AD75068 OCTAL PROGRAMMABLE GAIN AMPLIFIER



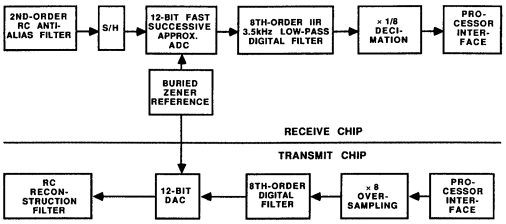
Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. For example, the AD75004 quad DAC could be expanded to 6 channels, each of which may have separate reference inputs. The AD75068 could be configured to include filtering. These modifications, if based on standard library cells, can provide the fastest, most cost effective semicustom solution.

Modem Chipset

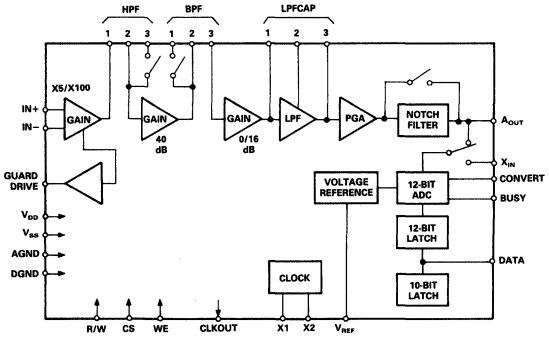
Library cells can be combined to form macro building blocks for high speed modems. This two-chip design concept filters and converts data to interface a digital signal processor with the analog circuitry of a 9600-baud modem. On one chip, the received signal passes through an antialiasing filter, sample-and-hold, 12-bit A/D converter, 8th-order digital filter and decimation. On the other chip, transmit data is 8 × oversampled, then goes to an 8th-order filter, a 12-bit DAC and an active reconstruction filter.

HIGH SPEED MODEM CHIPSET



AD79015 LOW LEVEL DAS

This circuit is a complete data acquisition system for low level signals (e.g., ECG and EEG) with a throughput of 10,000 samples per second. It provides high accuracy, high stability and functional completeness in a small 28-pin PLCC package. It includes a high performance instrumentation amp, bandpass and 50/60 Hz notch filters, and a 12-bit ADC with on-chip reference. It also includes a fast 8/12-bit serial port to interface to most microprocessor systems.



HIGH PERFORMANCE PROCESSES

Analog Devices' semicustom and custom circuits are fabricated using the same high performance processes as our standard ICs. These technologies include two mixed bipolar-CMOS processes and a high voltage CMOS process. These processes include thin-film resistors which may be laser trimmed for precise matching and stable performance over a wide temperature range.

The BiMOS II and Linear Compatible CMOS (LC^2MOS) processes combine bipolar and CMOS devices on one chip. Functional density is an order of magnitude greater than previous mixed-signal processes; over 20,000 devices can be placed on a single chip. Bipolar transistors provide low noise, low offset input stages and high power output stages. The CMOS devices offer high input impedance, and make dense logic and good switches for data converters, multiplexers and switched-capacitor filters. LC^2MOS also provides a JFET for very low input noise.

The bipolar-CMOS processes operate on supply voltages ranging from single +5 volts to split ±15 V, with signal levels ranging from single-ended +3 V to ±10 V. These processes are ideally suited for applications in data acquisition, instrumentation, industrial automation and telecommunications.

The High Voltage Switch (HVS) process provides quality analog switches that can operate with supply voltages up to ±22 volts. It can combine switches and multiplexers with CMOS logic.

The following table summarizes the processes available for designing ASICs. Other processes in development offer even higher speed, denser logic and higher integration of analog and digital functions.

ANALOG DEVICES HIGH PERFORMANCE PROCESSES FOR ASICS

Process	Power	Signal	Features
BiMOS II	±12 V	±8 V	Wide Variety of Precision Linear and Digital Functions
LC^2MOS	+5 V to ±15 V	+3 V to ±10 V	Wide Variety of Precision Linear and Digital Functions
HVS	+5 V to ±22 V	+2 V to ±18 V	High Voltage Switches, Muxes and Logic Functions

CELL LIBRARIES

Cell libraries for the bipolar CMOS processes are described below. These libraries are growing with the development of new processes, macrocells and cells. Many new catalog parts will also be available as cells. Your local sales office can give you current information on the cell libraries and available Linear System Macros.

Operational amplifiers are available in bipolar, JFET and CMOS configurations. Representative bipolar op amp cells have performance characteristics similar to an AD OP-27 and a slew-enhanced AD741. The LC^{2}MOS process offers JFET op amps, including an AD711 equivalent.

Instrumentation amplifiers with performance comparable to the AD521 and AD524 are available. Linear comparators have response times down to 100 nanoseconds and strobed comparators have setup/access times down to 50 nanoseconds.

Digital-to-analog converters range in resolution from 8 to 16 bits, and include cells similar to the AD667 and AD1856. Analog-to-digital converters vary from 8 to 16 bits in resolution, and include cells equivalent to the AD7572 and AD674. One half-flash ADC cell converts to 8-bit accuracy in 500 nanoseconds, and one successive approximation cell converts to 12 bits in less than 5 microseconds.

Support cells include sample-and-hold amplifiers with performance comparable to the AD585, low voltage bandgap references comparable to the AD584, and low noise buried Zener references.

RC active filters and programmable switched-capacitor filters are available with specifications in these ranges:

Topology: all classical filter types

Frequency Range: 200 Hz to 20 kHz (switched-cap) or 100 Hz to 1 MHz (RC)

Number of Sections: up to 10th-order (switched-cap) or 4th-order (RC)

Signal/Noise and THD: >72 dB, compatible with 12-bit data acquisition.

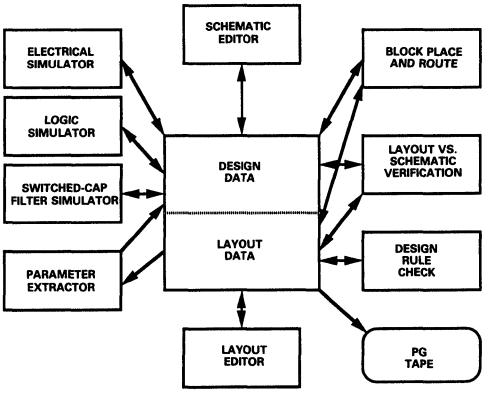
Logic cells include gates, counters, registers, microsequencer, PLA, RAM and ROM. Interface cells include 8-bit and 16-bit parallel I/O ports as well as synchronous serial ports and UARTS.

COMPUTER-AIDED DESIGN TOOLS

Designing a high performance mixed-signal IC is inherently more difficult than designing a gate array. The variety of analog and digital functions requires a cell-based approach. However, the use of powerful tools gives high confidence of functionality at first silicon through thorough simulation and layout verification. Complete computer-generated documentation of all schematics and analog and logic simulation waveforms permits thorough evaluation of Analog's design by your design staff before signoff for final layout and fabrication.

The overall work flow through the CAD environment is shown below. Key to meeting the special challenges of mixed analog-/digital circuitry are the simulation and auto-layout tools, and the unification of design and layout information in a single database. Analog Devices has developed a suite of proprietary computer-aided design tools, called JANUS™, to address these issues and to implement turn-key designs.

Computer-Aided Design Flow



The JANUS schematic editor offers numerous time-saving techniques and provides for specification of such data as wire widths, routing layers and routing priorities. It automatically generates a netlist used by subsequent tools.

Analog uses several simulators, including electrical, logic and behavioral types. ADICE, a proprietary enhanced version of the SPICE electrical simulator, gives precision simulation of critical analog sections. It uses Newton-Raphson methods to iteratively solve nonlinear time-dependent simultaneous differential equations. It is efficient for circuits up to about 250 active devices and is used for the frequency domain or transient analysis of analog cells such as op amps, or sensitive digital cells such as dynamic RAM.

Event-driven simulators handle larger circuits, with thousands of devices, and are typically used to simulate logic. The JANUS mixed-signal simulator combines an event-driven simulator with Newton-Raphson methods. It dynamically partitions the circuit to apply the faster event-driven techniques where possible, and the matrix methods where necessary. It also dynamically sizes the matrix and time steps to speed simulation further. The simulator can operate at the transistor level or use behavioral models, or both at the same time, allowing trade-offs between accuracy and speed.

JANUS is a trademark of Analog Devices, Inc.

For layout, the challenge is to increase automation while accommodating the layout sensitivity of analog circuitry. Device generators exist for the full range of active and passive devices available in the technology to automatically create a physical representation of the circuit schematic. This layout may be optimized through conventional interactive polygon-pushing.

The JANUS placement editor starts with a topological placement based on the schematic, and uses simulated annealing to automatically place devices and cells. The user may define the cost function for the annealer; the default version comprehends such analog concerns as thermal and electrical matching and device and cell grouping, as well as cell overlap, net length, and die area.

The JANUS routing editor is driven by the connectivity of the schematics, but allows great freedom to manually control the routing of critical analog signal paths or power/ground lines while autorouting noncritical nets and spacing the layout to achieve automatic enforcement of layout rules. The JANUS routing editor uses up to three interconnect levels, and will automatically expand and compact placement as necessary to achieve 100% routing.

Finally, industry-standard layout verification tools assure conformance of the layout to both the schematic and design rules to give high confidence of functionality in first silicon. The CAD tool suite communicates via industry-standard stream formats to external databases and pattern generators.

TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, H-P, Teradyne and LTX test equipment. The design, wafer probe and test areas share data on the network for statistical analysis and device modeling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

PACKAGING

Analog Devices ICs are available in most modern package types, including high pin-count and surface mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below. This list is constantly expanded and other packages may be used if they are suitable for high performance applications.

Available Packages

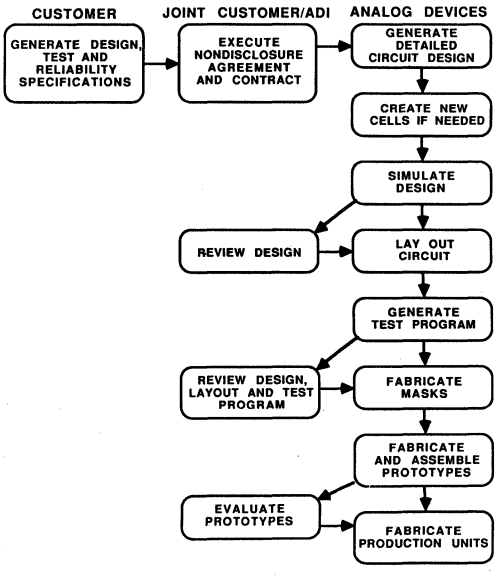
Pin-grid array (PGA): 68 to 144 pins
Leaded ceramic chip carrier (LDCC): 44 pins
Leadless ceramic chip carrier (LCC): 20 to 68 I/Os
Plastic quad flat pack (PQFP): 100 pins
Plastic leaded chip carrier (PLCC): 20 to 68 pins
Plastic dual in-line package (DIP): 14 to 64 pins
Side-brazed DIP: 14 to 64 pins
Frit-seal DIP (Cerdip): 14 to 40 pins
Small outline (SO): 14 to 28 pins

PROGRAM RESPONSIBILITIES AND INTERFACES

The following figure shows the major phases in developing an ASIC and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices Sales Engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.

PROGRAM RESPONSIBILITIES AND INTERFACES



Power Supplies
Modular AC/DC Power Supplies

GENERAL DESCRIPTION

Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low-cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 25 mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES

- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5 V), Dual (±12 V, ±15 V), and Triple (±15 V/+5 V, ±15 V/+1 V to +15 V) Output Supplies
- Current Outputs:
  25 mA to 1000 mA for Dual and Triple Output Supplies
  250 mA to 5000 mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

GENERAL SPECIFICATIONS

Power Requirements

Input Voltage Range:	105 V ac to 125 V ac
Frequency:	50 Hz to 250 Hz

Electrical Specifications

Temperature Coefficient:	0.02%/°C
Output Voltage Accuracy:	±2%, max See Specifications Table
Breakdown Voltage:	500 V rms, min
Isolation Resistance:	50 MΩ
Short Circuit Protection:	All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.

Environmental Requirements

Operating Temperature Range:	−25°C to +71°C
Storage Temperature Range:	−25°C to +85°C

SPECIFICATIONS – Typical @ +25°C and 115 V ac 60 Hz unless otherwise noted*

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. max %	Load Reg. max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	904	±15	±50	0.02	0.02	±200 mV −0 mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
	Single Output	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
		928	5	3000	0.05	0.10	±2%	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1%	0.5	
		927	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2%	1.0 (typ)	
		2B35J	±15	±65	0.08	0.1	(−0, +300 mV)	0.5	3.5×2.5×1.25
			+1 to +15**	125	0.08	0.1		0.25	
		2B35K	±15	±65	0.01	0.02	(−0, +300 mV)	0.5	3.5×2.5×1.25
			+1 to +15**	125	0.01	0.02		0.25	
Chassis Mounted	Dual Output	952	±15	±100	0.05	0.05	±2%	1	4.4×2.7×1.45
		970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.45
		973	±15	±350	0.05	0.05	±2%	1	4.4×2.7×2.00
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.45
		976	5	3000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
		977	5	5000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
	Triple Output	972	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	300	0.02	0.10	±2%	1.0 (typ)	
		974	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2%	1.0 (typ)	

*Consult Analog Devices Power Supplies Catalog for additional information.
**Resistor programmable.
Specifications subject to change without notice.

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Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offers system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Fourteen models are offered in five power levels of 1 watt, 1.8 watts, 4.5 watts, 6 watts and 12 watts. Input voltage versions include 5 volt, 12 volt, 24 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±60 mA to 1000 mA output current capability.

Most models are high efficiency (typicaly over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20 kHz) Converter Switching Frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (Either Output to Common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free Air Convection Cooling
  No external heat sink or specification derating is required over the operating temperature range.

GENERAL SPECIFICATIONS FOR 1 W AND 1.8 W MODELS

Line Regulation – Full Range: ±0.3% (±1% max, 949)
Load Regulation – No Load to Full Load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20 mV p-p (with 15 μF tantalum capacitor across each output) 2 mV rms max, 949)
Breakdown Voltage: 300 V dc min (500 V dc min, 949)
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5 W, 6 W AND 12 W MODELS

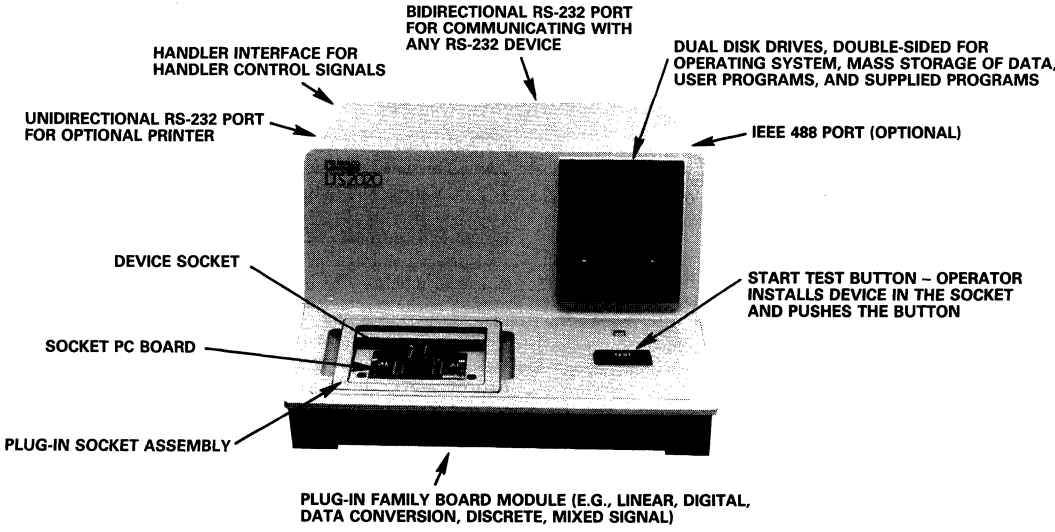
Line Regulation – Full Range: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Load Regulation – No Load to Full Load: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Output Noise and Ripple: 1 mV rms max
Breakdown Voltage: 500 V dc min
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

SPECIFICATIONS – Typical @ +25°C at nominal input voltage unless otherwise noted*

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	2.0×2.0×0.38
958	5	100	5	4.5/5.5	200 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17A	±1%	±0.01%	58%	2.0×2.0×0.38
960	±12	±40	5	4.5/5.5	384 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
964	±15	±33	12	10.8/13.2	165 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
965	±15	±190	5	4.65/5.5	1.7 A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
966	±15	±190	12	11.2/13.2	710 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
967	±15	±190	24	22.3/26.4	350 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6 A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35 A	±1%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6 A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250 mA	±0.5%	±0.01%	61%	2.0×2.0×0.38
951	±15	±410	5	4.65/5.5	3.7 A	±0.5%	±0.01%	62%	3.5×2.5×0.88

NOTES
[1]Models 940 and 941 will deliver up to 120 mA output current (and Model 943 will deliver up to 600 mA) over an input voltage range of 4.65 V dc and 5.5 V dc.
*Consult Analog Devices Power Suppies Catalog for additional information.
**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120 mA.
Specifications subject to change without notice.

LTS-2020 Component Test Systems



THE LTS CONCEPT

The LTS-2020 is a versatile component test system which tests a multitude of components to the manufacturer's specifications (linear, digital, data conversion, and discrete devices). The system offers such features as RS-232 ports for networking, IEEE for compatibility with handlers and probers, dual disk drives for mass storage of data, automatic self-calibration, and a full statistical analysis software package.

The LTS-2020 provides several data output formats – datalog, yield analysis, and statistical analysis. The console provides the primary measurement and control functions to test a specific class of devices. The socket assembly is the mechanical and electronic interface for the family board and the DUT board. The DUT board plugs directly into the socket assembly and contains the circuitry and socket, specific to the actual device under test.

Analog Devices' component test systems are the first benchtop testers that are programmable in BASIC and fill-in-the-blanks CREATE. CREATE is menu-driven software which prompts the user for data sheet limits and conditions, then builds a completed test program for the specified device. Turnkey program libraries are available for each of the device families.

Far more than just comprehensive production testers, these test systems can handle complex engineering analysis and incoming inspection. They are the first systems that can provide all the capabilities of today's large centralized test systems at a price that is approximately one-third the cost. The LTS-2020 not only provides the flexibility of distributed or decentralized testing, it allows for cost effective multiple system purchases. They increase overall test reliability since the threat of a single big failure is eliminated in a distributed testing environment.

MIXED SIGNAL TEST CAPABILITY

The LTS-2800 Mixed Signal Family Board and LTS-0680 Test Head perform a wide variety of ac and dc parametric tests on devices such as complex hybrids, octal DACs, ASICs, converters, and pulse width modulators. The family board supplies the dc pin drivers, the dc force and measure system, a V_{CC} buffer, an rms-to-dc conversion circuit, voltage and current sources, and a 24 × 5 switching matrix. With its 24 programmable pin drivers, the system can provide high and low digital voltages, a three-state (high impedance) output mode, and accurate voltages and currents (V/I source).

The family board incorporates a series of 12-bit calibrated sources, used for programming V_{IL} and V_{IH} voltage levels at the digital inputs of the device under test. A threshold source for programming voltage levels on a comparator is used to detect digital output voltage levels accurately. For forcing and measuring currents, a V/I source provides and measures 10 μA to 400 mA and voltages to ±20 V.

A switching matrix provides system flexibility by allowing any one of several capabilities to be switched to any of the pin drivers. These include the measure system, V/I source, V_{IH} and V_{IL} sources, the rms-to-dc circuit, and BNC input and output connectors for interconnection with external instruments using the IEEE-488 bus.

The LTS-0680 Mixed Signal Test Head contains a precise and versatile time measure unit which provides accurate ac measurement of propagation delays, slew rates, pulse widths, and rise and fall times. It also incorporates a 16-bit user data bus, 16-bit relay driver bus, four 12-bit programmable sources, and a user's expansion board. A square wave source to the DUT provides up to ±10 volt signals, from 1.22 kHz to 2.5 MHz.

LINEAR DEVICE TEST CAPABILITY

The LTS-2101 Operational Amplifier Family Board tests today's very demanding high precision op amps, comparators, and regulators. This board houses the test loop used in testing op amps and comparators and the pulse load circuitry used in developing the high currents needed for voltage regulator testing.

For testing devices under 100 μV, the LTS-2101 offers a tight offset spec of ±(0.25% + 5 μV). Use of low thermal Emf relays and a test loop gain of 10,045 ensures superior low level V_{OS} measurement performance for optimum repeatability of low level signals.

Testing of low current devices is achieved with the LTS-0614 Socket Assembly which is designed to test bias and offset currents with an accuracy of ±(5% + 25 fA) for any FET amplifier, including quad devices. Program libraries containing prewritten test programs for many standard op amps, comparators and regulators are available on disk.

ANALOG-TO-DIGITAL TEST CAPABILITY

The LTS-2200 ADC Family Board provides the test circuitry required for testing monolithic, hybrid, or modular ADCs. An on-board 16-bit microprocessor with 8K bytes of memory acts as a slave for the system console and executes preprogrammed test routines such as linearity, all codes existence, transition noise measurements, and conversion time measurements at high speed. Absolute accuracy can be measured within 200 μV. Linearity, differential nonlinearity, offset, gain, and PSSR are tested to ±0.05 DUT LSB +200 μV. Turnkey test packages are available for many of the standard ADCs currently in use.

DIGITAL-TO-ANALOG TEST CAPABILITY

The LTS-2302 DAC Family Board utilizes advanced state-of-the-art test techniques to provide comprehensive test capabilities for a wide variety of D/A converters. It will test both voltage and current output DACs, DACs with and without buffer registers, and serial or parallel input DACs to 16-bit accuracy.

High repeatability on low level signals is achieved because of the grounding scheme on the LTS-2302. The incorporation of high level components in the V/I circuits ensures true accuracy. In addition, the methodology for measuring low bit currents allows appropriate testing of this parameter on CMOS DACs.

Output leakage current on the LTS-2302 is measured with the bit drivers to the DAC set to logic 0. Current is measured using the I to V converter. A 1 MΩ resistor within the I to V circuitry ensures sensitivity, thereby measuring current down to ±1 μA full scale.

DIGITAL DEVICE TEST CAPABILITY

The LTS-2510 Digital Device Family Board provides 24-pin driver/detectors and a precision, four quadrant V/I source for testing SSI/MSI TTL and CMOS digital devices. This board contains four programmable device supplies and switching circuitry necessary for performing accurate parametric measurements on all device pins.

Together with the LTS-0655 remote ac test fixture, dynamic parametric testing of 24-pin SSI/MSI TTL digital devices can be achieved. Accuracies are achieved down to ±4% + 1.5 ns at a resolution of 500 ps. Dynamic parameters tested are propagation delay, setup, and hold times.

DISCRETE DEVICE TEST CAPABILITY

The LTS-2600 Transistor Family Board tests bipolar transistors, JFETs, diodes, and optocouplers. An on-board 16-bit microprocessor with 4K bytes of memory acts as a slave for the LTS system and coordinates the timing and pulse width control of the stimulus and measurement signals. In addition, the microprocessor monitors the interlock circuitry to insure safe handling of high power test signals.

MOSFET software packages support the testing of N and P channel enhancement mode and N channel depletion mode devices. Tests which may be performed on MOSFET devices include Idss, Igss, Igssf, Igssr, Id (off), Id (on), B Vdss, B Vgss, B Vgssf, B Vgssr, Vds (on), Vgs (th), Vgsoff, Vsd, Rds (on), and Gsf.

The Smartpower Test Fixture will support fast, accurate testing of devices such as Darlington Arrays, Differential Line Drivers/Receivers, and Transceivers/Repeaters. It contains a matrix board which facilitates the muxing of High Voltage/High Current V/Is, a nonometer, diffamp, 16-bit measure system, and mecca ground reference to any one of eight matrix points at the DUT site and eight dc pin drivers programmable to any one of four modes – V/I, V_{IH}, V_{IL} or Tristate. This configuration allows true digital dc parametric testing of the front end of smartpower devices while providing the high voltage and high current capability to test the discrete output stage.

ANALOG SWITCH TEST CAPABILITY

The LTS-2700 Analog Switch Family Board adds switch and multiplexer testing capability to the LTS-2020. This test capability, with CREATE software, allows datalogged device testing at the incoming inspection and semiconductor manufacturing levels and includes software power for use in component evaluation applications.

The LTS-2700 tests on and off drain to source leakage currents with an accuracy of 250 pA while forcing differential voltages up to 50 V (± 25 V from GND). Other tests performed are drain to source on resistance, greatest change in drain-source on resistance between channels, digital input current and supply current.

Twenty high integrity analog lines are provided – four to be used as drain connections and sixteen for source connections. Also provided are eight programmable digital drivers, four digital control bits, six variable power supplies, and one fixed +5 V supply. These combinations of sources provide testing of devices such as 4-channel switches, 16 to 1 multiplexers, and other combinations of switches and multiplexers.

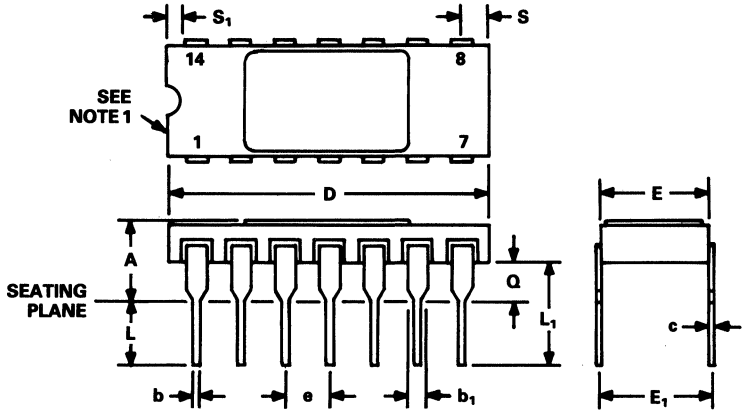
Package Information
Contents

ADI LETTER DESIGNATOR	DESCRIPTION	PAGE
Side Brazed DIP (Ceramic)		
D-14	14 Lead	20 – 2
D-16	16 Lead	20 – 3
D-18	18 Lead	20 – 4
D-20	20 Lead	20 – 5
Bottom Brazed DIP (Ceramic)		
DH-14A	14 Lead	20 – 6
DH-14B	14 Lead	20 – 7
Metal Platform DIP		
DH-16B	16 Lead	20 – 8
Leadless Chip Carrier (Ceramic)		
E-20A	20 Terminal	20 – 9
E-28A	28 Terminal	20 – 10
Flat Pack (Ceramic)		
F-2A	2 Lead	20 – 11
Metal Can		
H-03A	3 Lead (TO-52)	20 – 12
H-03B	3 Lead (TO-5 Style)	20 – 13
H-08A	8 Lead (TO-99)	20 – 14
H-08B	8 Lead (TO-99 Style)	20 – 15
H-10A	10 Lead (TO-100)	20 – 16
H-12A	12 Lead (TO-8 Style)	20 – 17
Plastic DIP		
N-8	8 Lead	20 – 18
N-14	14 Lead	20 – 19
N-16	16 Lead	20 – 20
N-18	18 Lead	20 – 21
N-20	20 Lead	20 – 22
N-24	24 Lead	20 – 23

ADI LETTER DESIGNATOR	DESCRIPTION	PAGE
Plastic Leaded Chip Carrier (PLCC)		
P-20A	20 Lead	20 – 24
P-28A	28 Lead	20 – 25
Cerdip		
Q-8	8 Lead	20 – 26
Q-14	14 Lead	20 – 27
Q-16	16 Lead	20 – 28
Q-18	18 Lead	20 – 29
Q-24	24 Lead	20 – 30
Small Outline (SOIC)		
R-8	8 Lead	20 – 31
R-16	16 Lead	20 – 32
R-20	20 Lead	20 – 33
Plastic Quad Flat Pack		
S-52	52 Lead	20 – 34
Plastic		
TO-92	3 Lead	20 – 35
Single In-Line Package (SIP)		
Y-10	10 Lead	20 – 36
Leaded Chip Carrier (Gull Wing)		
Z-8	8 Lead	20 – 37
Z-16A	16 Lead	20 – 38
Z-16B	16 Lead (Wide)	20 – 39

Package Outline Dimensions

D-14
14-Lead Side Brazed Ceramic DIP

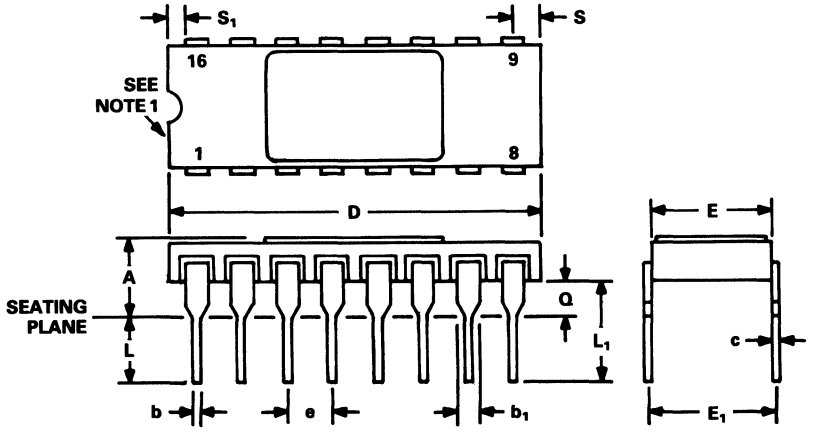


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twelve spaces.

D-16

16-Lead Side Brazed Ceramic DIP



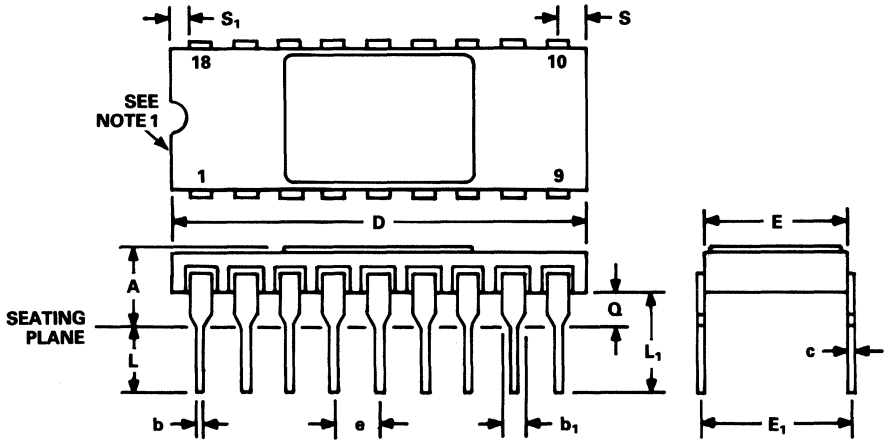
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Fourteen spaces.

D-18

18-Lead Side Brazed Ceramic DIP

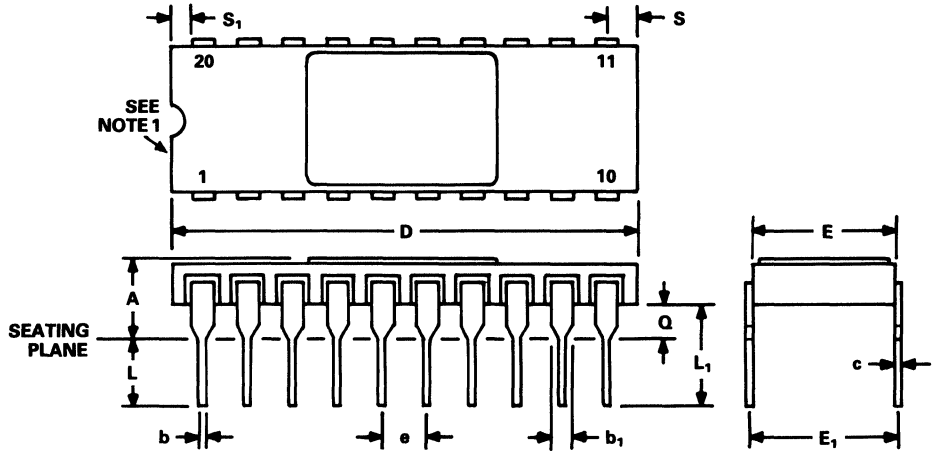


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Sixteen spaces.

D-20
20-Lead Side Brazed Ceramic DIP

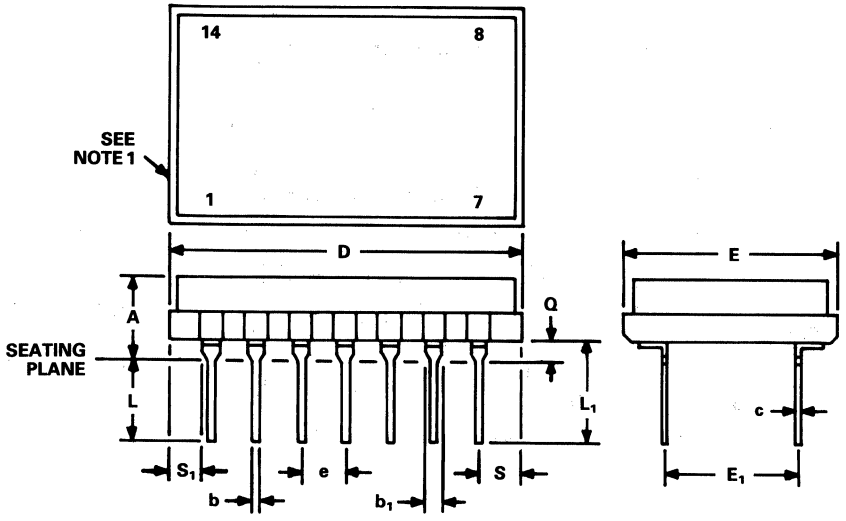


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.090	0.110	2.29	2.79	7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Eighteen spaces.

DH-14A

14-Lead Bottom Brazed Ceramic DIP



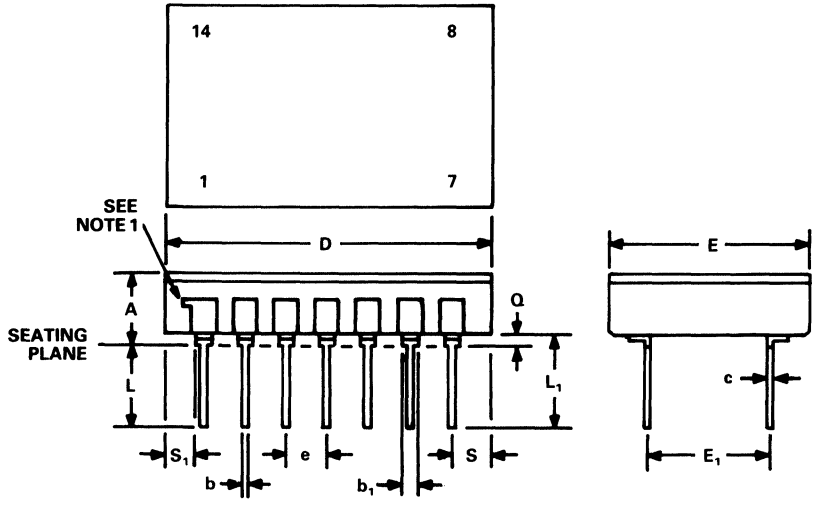
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.220		5.59	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		0.805		20.45	
E	0.480	0.505	12.19	12.83	
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		4,7
L	0.125	0.200	3.18	5.08	
L_1	0.180		4.57		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twelve spaces.

DH-14B

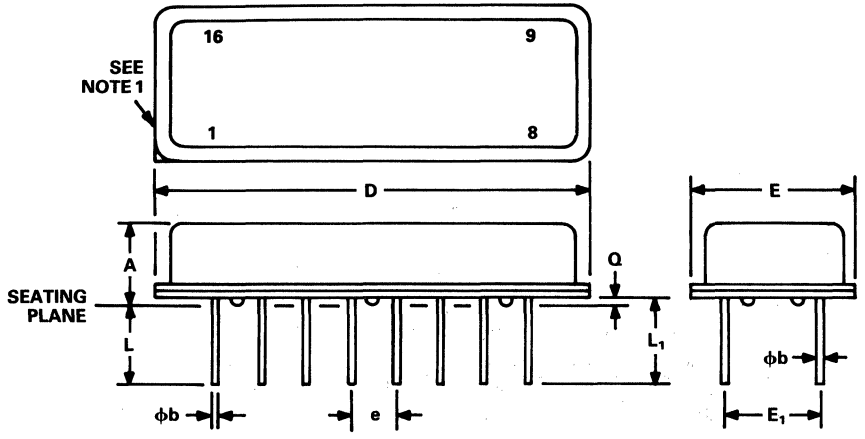
14-Pin Bottom Brazed Ceramic (Large Capacity)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.140	0.220	3.56	5.59	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	
c	0.008	0.015	0.20	0.38	
D	0.835	0.875	21.21	22.23	
E	0.480	0.510	12.19	12.95	
E_1	0.295	0.305	7.49	7.75	5
e	0.100 BSC		2.54 BSC		3, 6
L	0.150	0.200	3.05	5.08	
L_1	0.180		4.57		
Q	0.015	0.035	0.38	1.91	2
S		0.137		3.48	4
S_1	0.060		1.52		4

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Dimension Q shall be measured from the seating plane to the base plane.
3. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
4. Applies to all four corners.
5. E_1 shall be measured at the centerline of the leads.
6. Twelve spaces.

DH-16B
16-Lead Metal Platform DIP

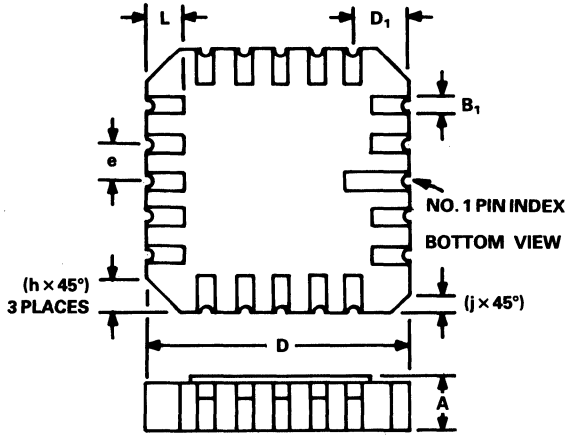


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.175	0.215	4.45	5.46	
ϕb	0.016	0.020	0.41	0.51	
D	0.960	0.985	24.4	25.0	
E	0.490	0.520	12.45	13.21	
E_1	0.295	0.305	7.49	7.75	4
e	0.095	0.105	2.41	2.67	5
L_1	0.160	0.255	4.06	6.48	

NOTES
1. Index area; a square corner or a lead one identification mark is located adjacent to lead one.
2. Pin 6 is electrically connected to the case.
3. Case has metal bottom surface.
4. E_1 shall be measured at the centerline of the leads.
5. Fourteen spaces.

E-20A

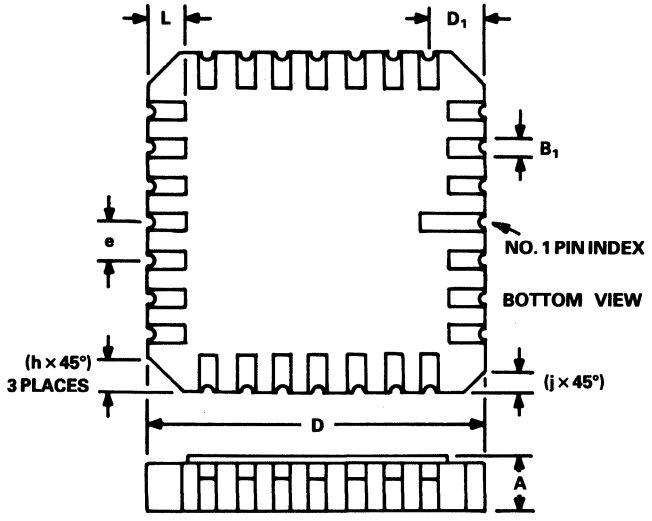
20-Terminal Leadless Ceramic Chip Carrier



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.342	0.358	8.69	9.09	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

E-28A
28-Terminal Leadless Ceramic Chip Carrier

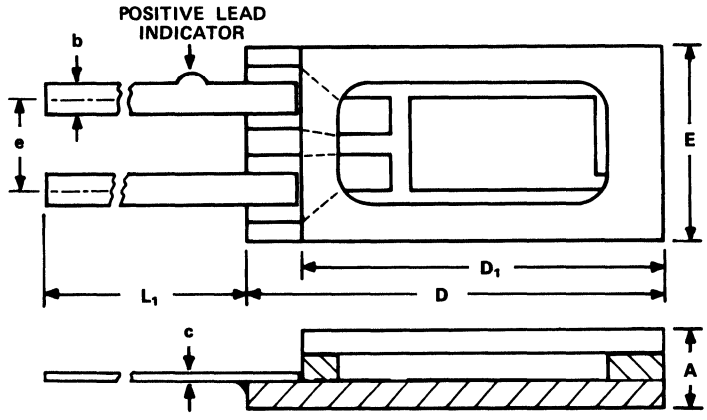


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	1
B_1	0.022	0.028	0.56	0.71	
D	0.442	0.458	11.23	11.63	2
D_1	0.075 REF		1.91 REF		
e	0.050 BSC		1.27 BSC		
j	0.020 REF		0.51		
h	0.040 REF		1.02		
L	0.045	0.055	1.14	1.40	

NOTES
1. Dimension A controls the overall package thickness.
2. Applies to all 4 sides.
3. All terminals are gold plated.

F-2A

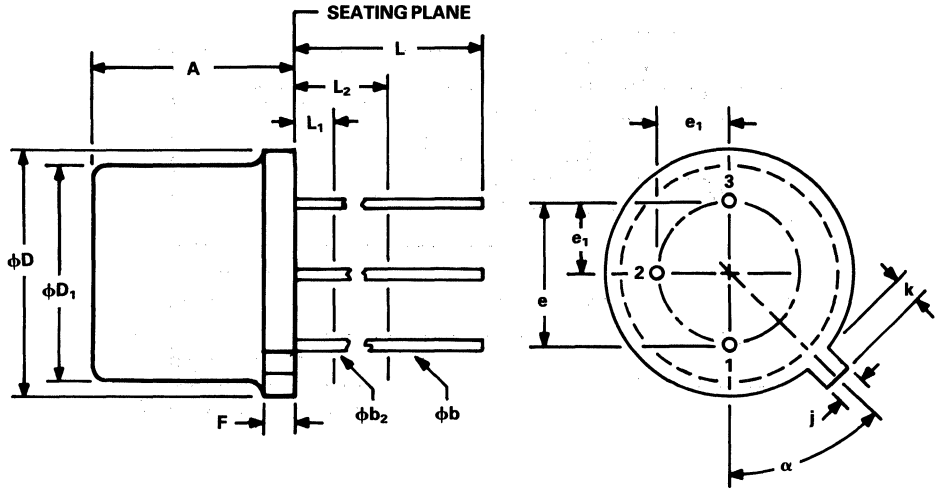
2-Lead Flat Pack



	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.044	0.066	1.12	1.67	
b	0.015	0.019	0.38	0.48	2
c	0.0045	0.0065	0.12	0.17	2
D		0.250		6.35	1
D_1		0.220		5.59	
E	0.081	0.093	2.06	2.36	1
e	0.045	0.055	1.14	1.40	
L_1	0.750		19.05		

NOTES
1. This dimension allows for off-center lid, meniscus and solder overrun.
2. All leads – increase maximum limit by 0.003" (0.08 mm) when hot solder dip finish is applied.

H-03A
3-Lead Metal Can (TO-52)

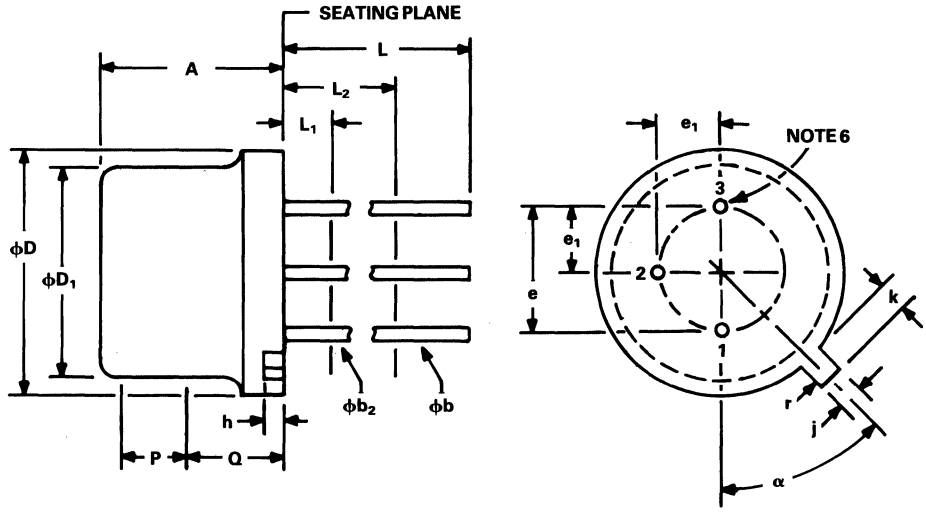


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.115	0.150	2.92	3.81	
ϕb		0.021		0.53	1,4
ϕb_2	0.016	0.019	0.41	0.48	1,4
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		2
e_1	0.050 T.P.		1.27 T.P.		2
F		0.030		0.76	
j	0.036	0.046	0.91	1.17	
k	0.028	0.048	0.71	1.22	3
L	0.500		12.70		1
L_1		0.050		1.27	1
L_2	0.250		6.35		
α	45° T.P.				

NOTES
1. (Three Leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.5" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.054" (1.4mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

H-03B

3-Lead Metal Can (TO-5 Style)

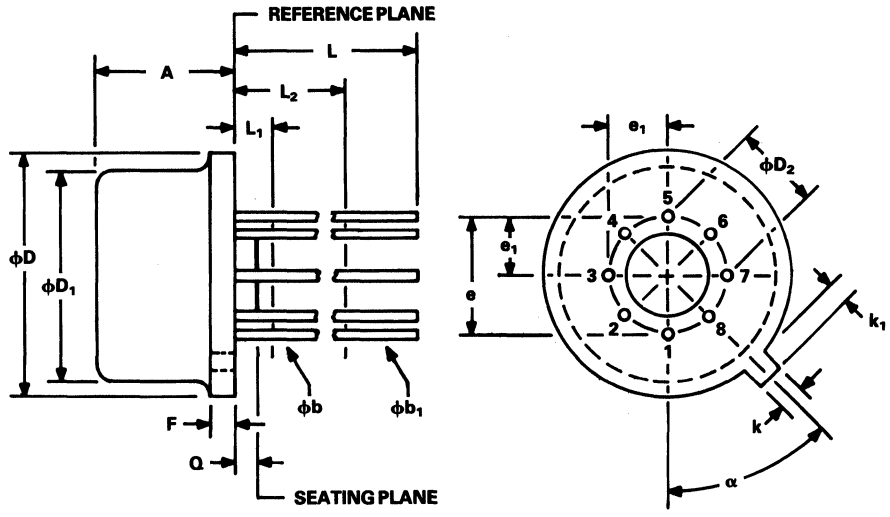


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
φb	0.016	0.021	0.41	0.53	2, 7
ϕb_2	0.016	0.019	0.41	0.48	2, 7
φD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
e	0.200 T.P.		5.08 T.P.		4
e_1	0.100 T.P.		2.54 T.P.		
h	0.015	0.035	0.38	0.89	
j	0.028	0.034	0.71	0.86	
k	0.029	0.045	0.74	1.14	3
L	0.500		12.70		2
L_1		0.050		1.27	2
L_2	0.250		6.35		2
P	0.100		2.54		1
Q					5
r		0.007		0.18	
α	45° T.P.				

NOTES

1. This zone is controlled for automatic handling. The variation in actual diameter within the zone shall not exceed 0.010" (0.25mm).
2. (Three leads) ϕb_2 applies between L_1 and L_2. φb applies between L_2 and 0.500" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from seating plane.
3. Measured from maximum diameter of the actual device.
4. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.54" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to the maximum-width tab.
5. Details of outline in this zone optional.
6. Lead #3 connected to case.
7. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

H-08A
8-Lead Metal Can (TO-99)

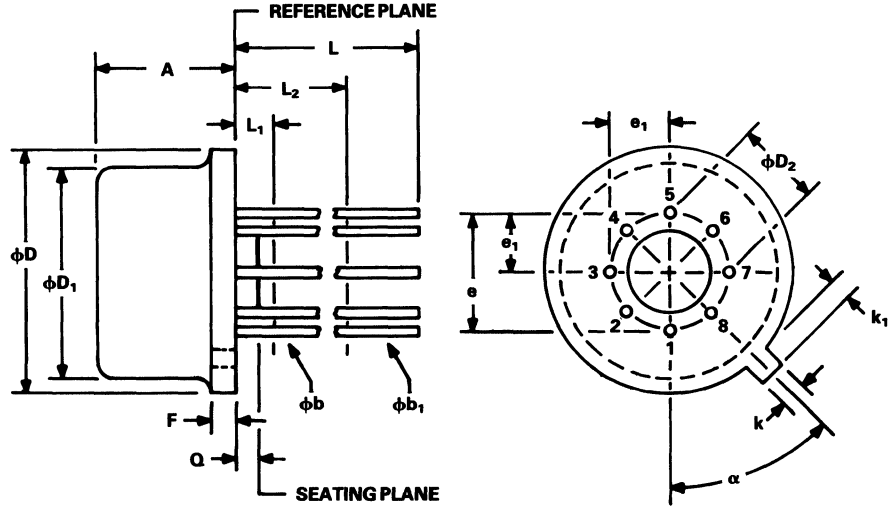


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1, 4
ϕb_1	0.016	0.021	0.41	0.53	1, 4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	
L	0.500	0.750	12.70	19.05	
L_1		0.050		1.27	
L_2	0.250		6.35		
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES
1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500" (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product are within 0.007" (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003" (0.08mm) when hot solder dip finish is applied.

H-08B

8-Lead Metal Can (TO-99 Style)

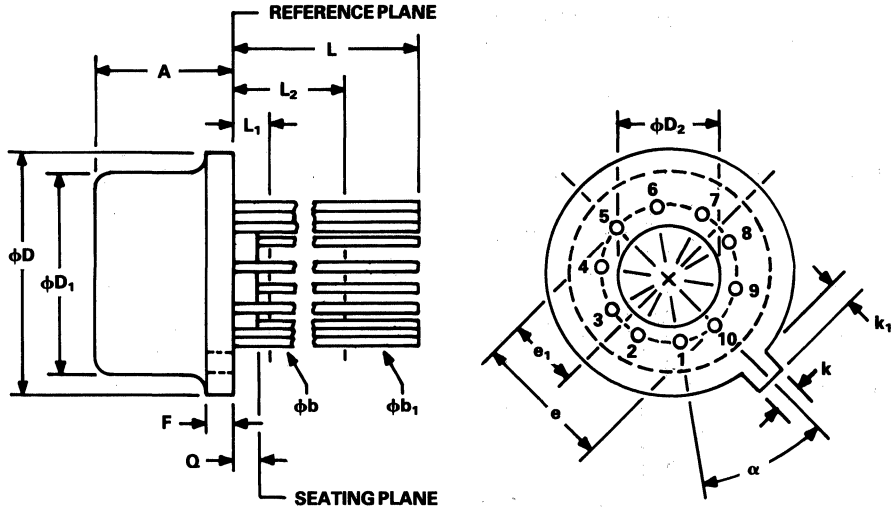


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500″ (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500″ (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019″ (0.48mm) measued in gauging plane 0.054″ (1.37mm) + 0.001″ (0.03mm) – 0.000″ (0.00mm) below the base plane of the product are within 0.007″ (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003″ (0.08mm) when hot solder dip finish is applied.

H-10A
10-Lead Metal Can (TO-100)

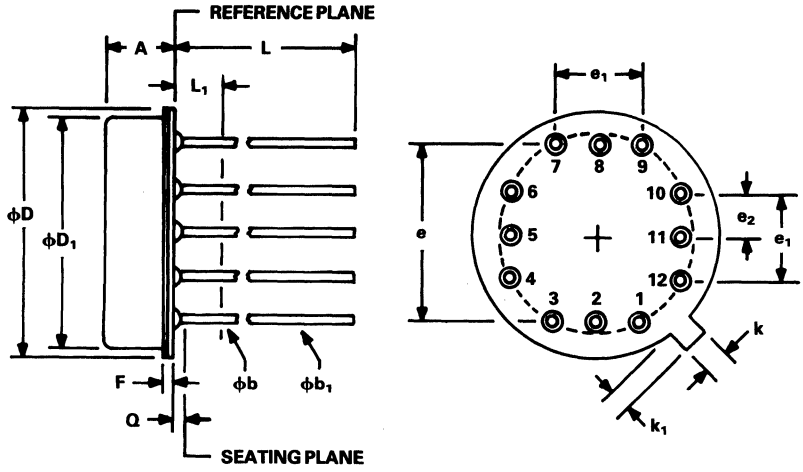


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	36° BSC		36° BSC		3

NOTES
1. (Three Leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.5" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.054" (1.4mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

H-12A

12-Lead Metal Can (TO-8 Style)

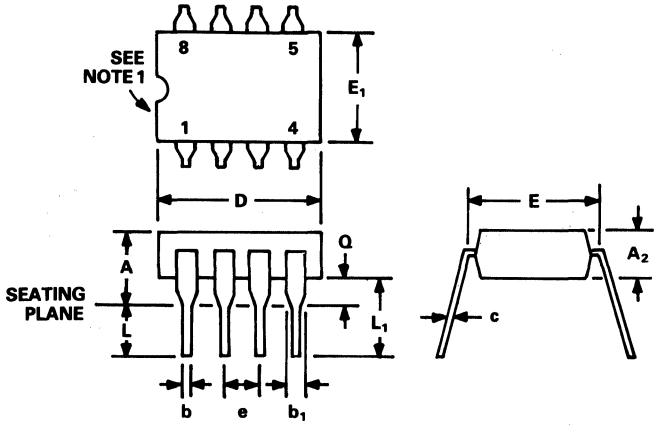


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.148	0.181	3.76	4.60	
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.592	0.610	15.04	15.44	
ϕD_1	0.545	0.555	13.84	14.10	
e	0.400 BSC				3
e_1	0.200 BSC				3
e_2	0.100 BSC				3
F		0.040		1.02	
k	0.026	0.036	0.66	0.91	
k_1	0.026	0.036	0.66	0.91	2
L	0.375		9.50		1
L_1		0.050		1.27	1
Q	0.010	0.045	0.25	1.14	

NOTES

1. (All leads) ϕb applies between L and L_1. ϕb_1 applies between L_1 and 0.375" (9.50mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.375" (9.50mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product is within 0.007" (0.18mm) of their true position relative to the maximum width tab.

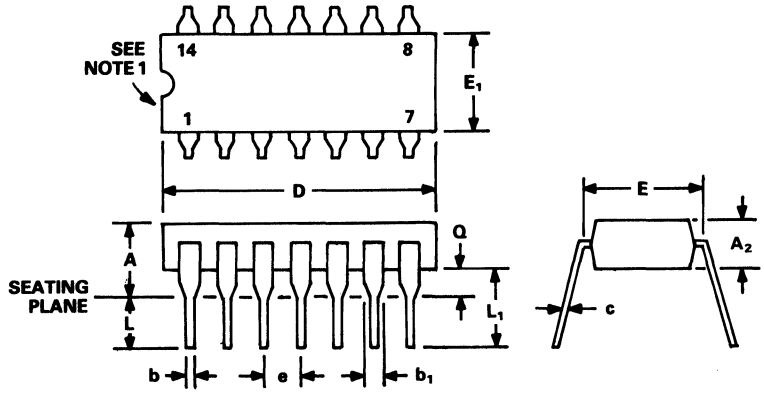
N-8
8-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

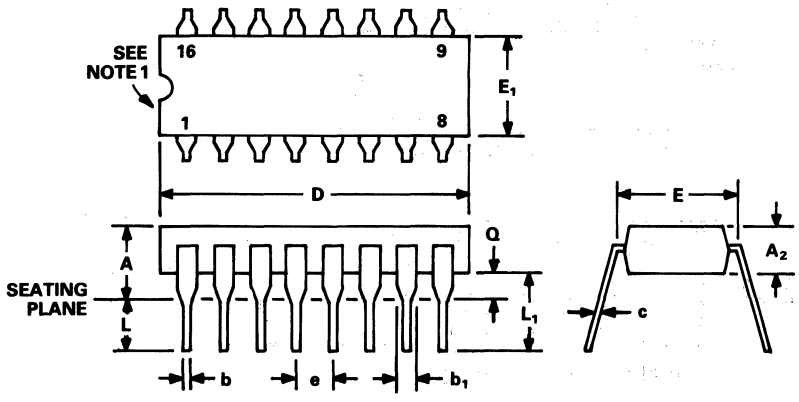
N-14
14-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

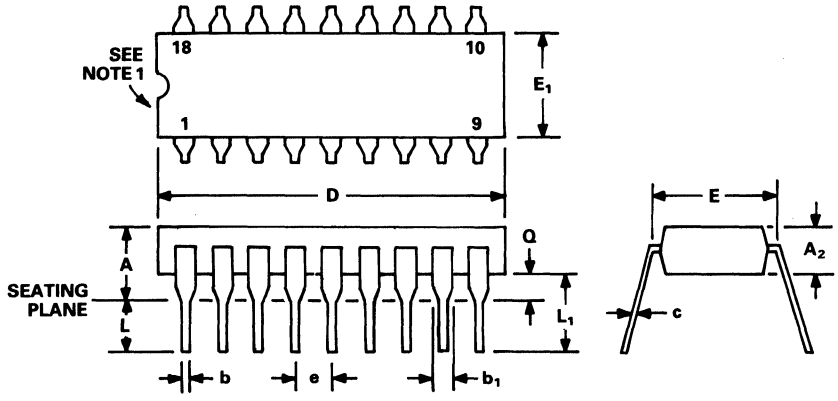
N-16
16-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

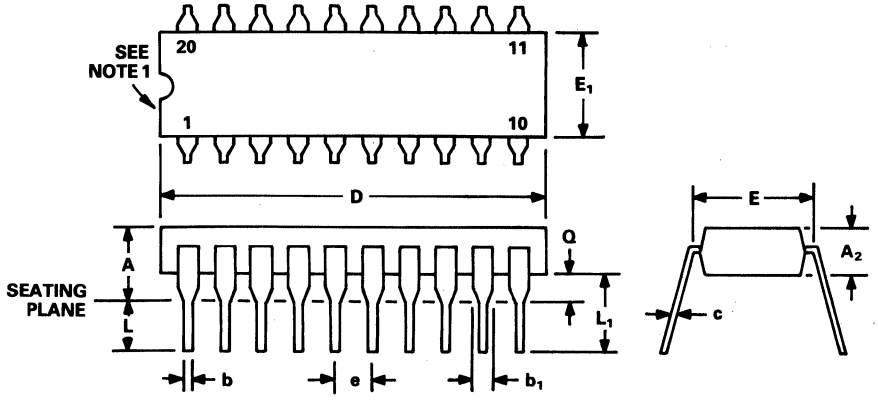
N-18
18-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.845	0.925	21.47	23.49	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

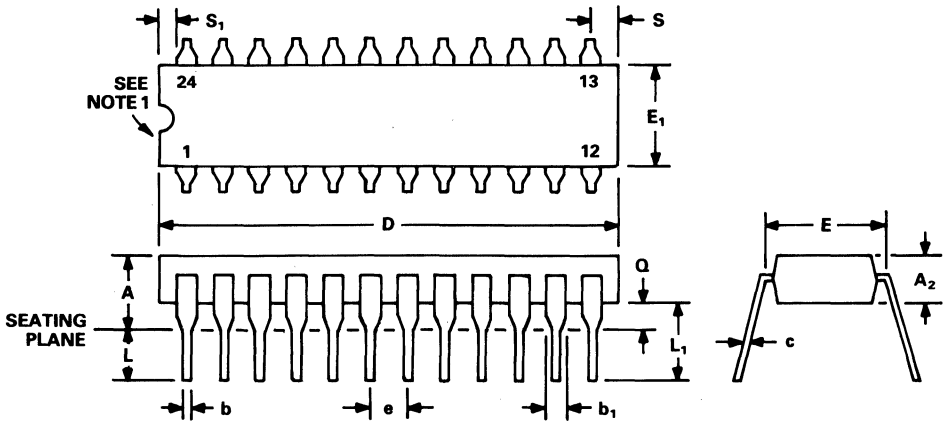
N-20
20-Lead Plastic DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.50	26.90	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-24
24-Lead Plastic DIP

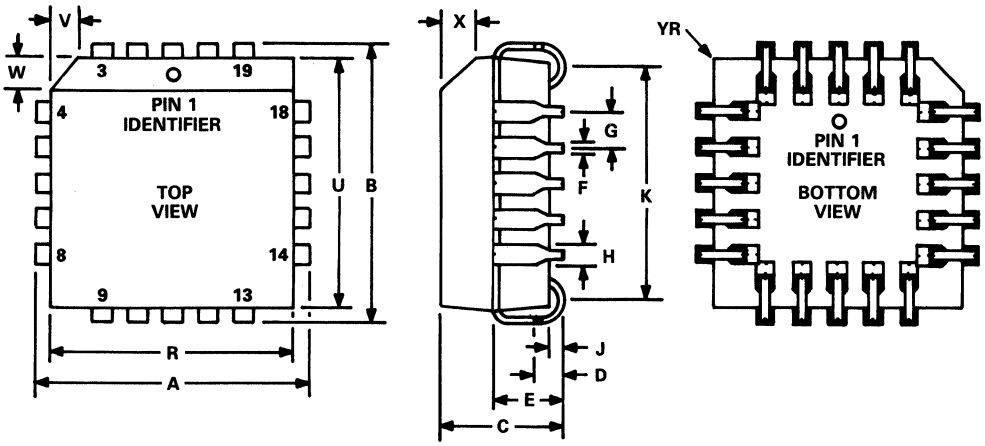


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.60	32.30	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.125	0.200	3.18	5.05	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

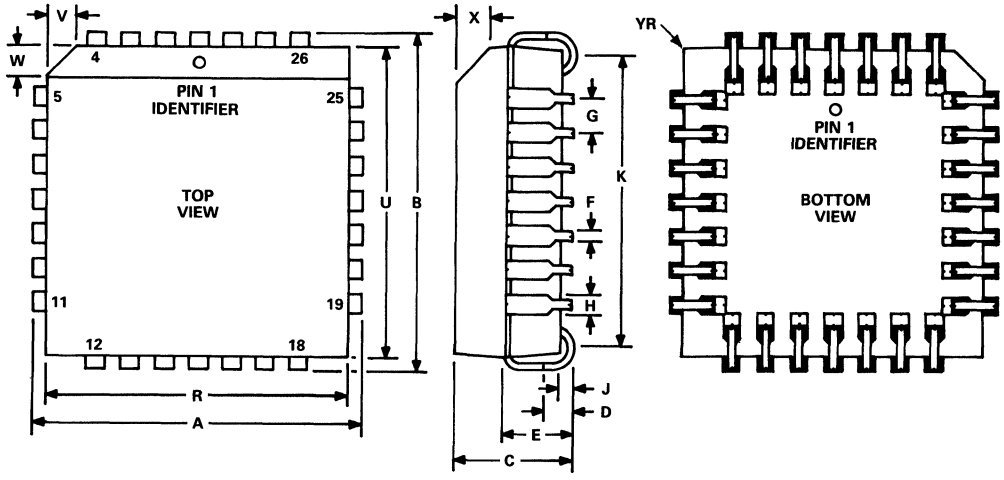
P-20A

20-Lead Plastic Leaded Chip Carrier (PLCC)



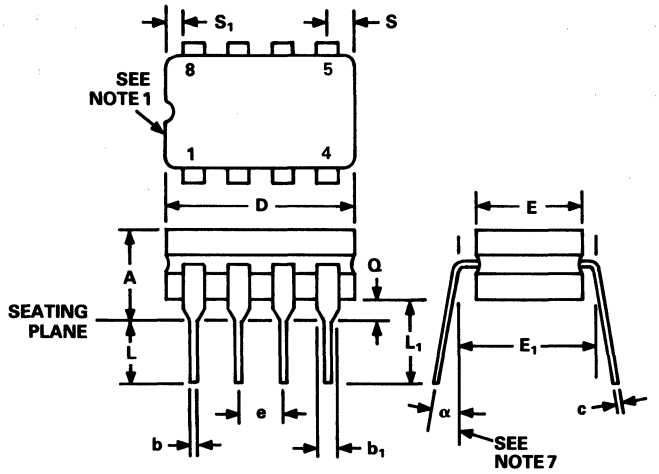
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.02
B	0.385	0.395	9.78	10.02
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.290	0.330	7.37	8.38
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-28A
28-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.390	0.430	9.91	10.92
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

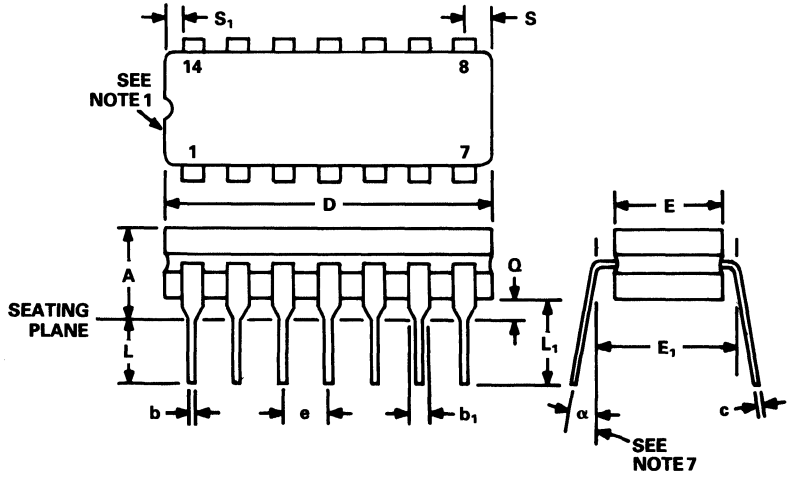
Q-8
8-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.35	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

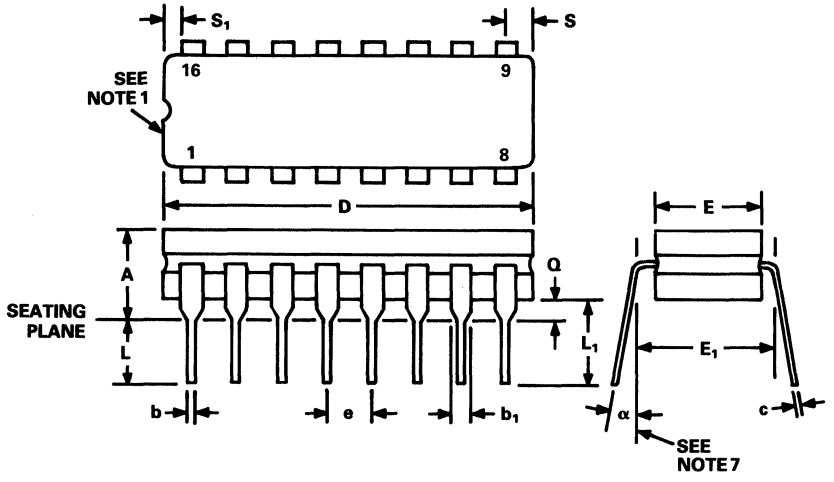
Q-14
14-Lead Cerdip



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twelve spaces.

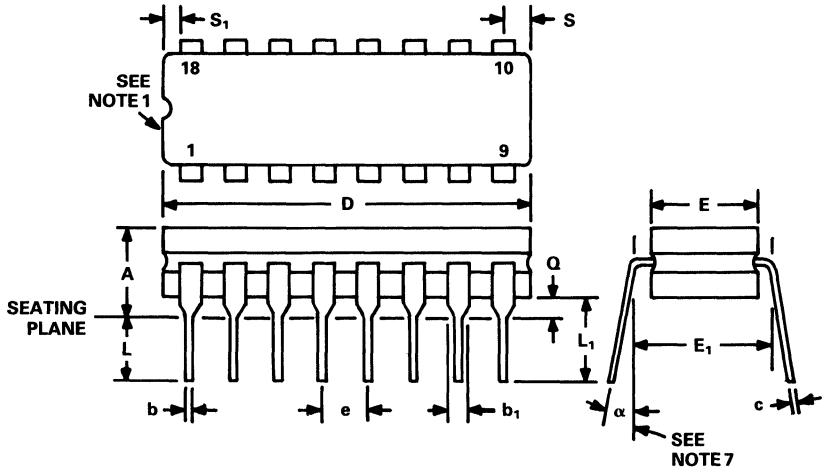
Q-16
16-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003"(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Fourteen spaces.

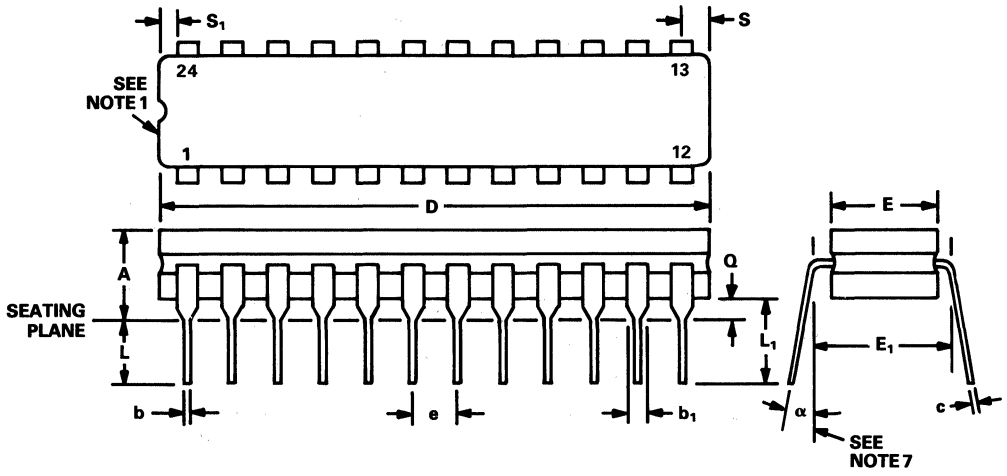
Q-18
18-Lead Cerdip



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2,7
c	0.008	0.015	0.20	0.38	7
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003″(0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Sixteen spaces.

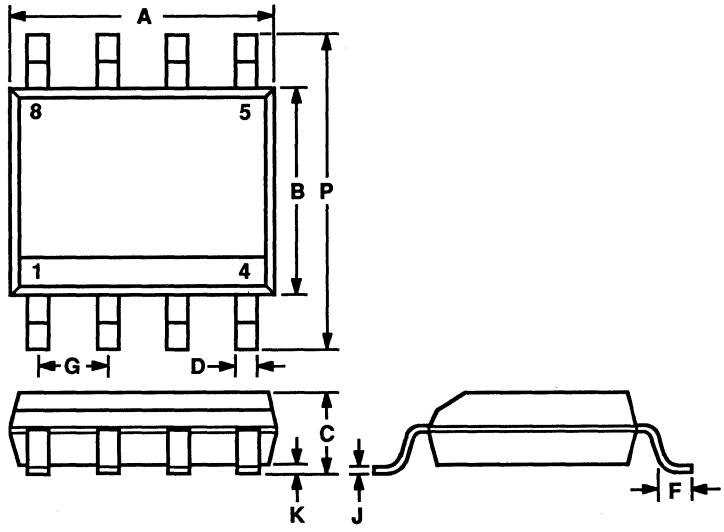
Q-24
24-Lead Cerdip



	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A		0.225		5.715	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" 0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°, E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Twenty-two spaces.

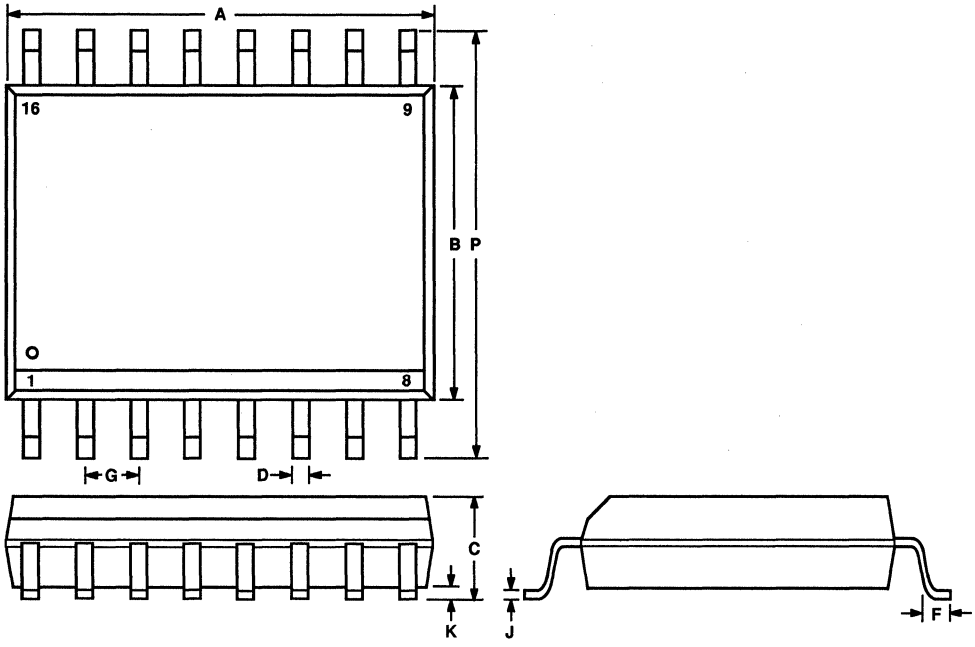
R-8
8-Lead Small Outline (SOIC)



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.189	0.196	4.80	4.98
B	0.150	0.157	3.81	3.99
C	0.094	0.102	2.39	2.59
D	0.014	0.019	0.36	0.48
F	0.016	0.050	0.41	1.27
G	0.050 BSC		1.27 BSC	
J	0.0075	0.0098	0.19	0.25
K	0.004	0.010	0.10	0.25
P	0.229	0.244	5.82	6.20

R-16

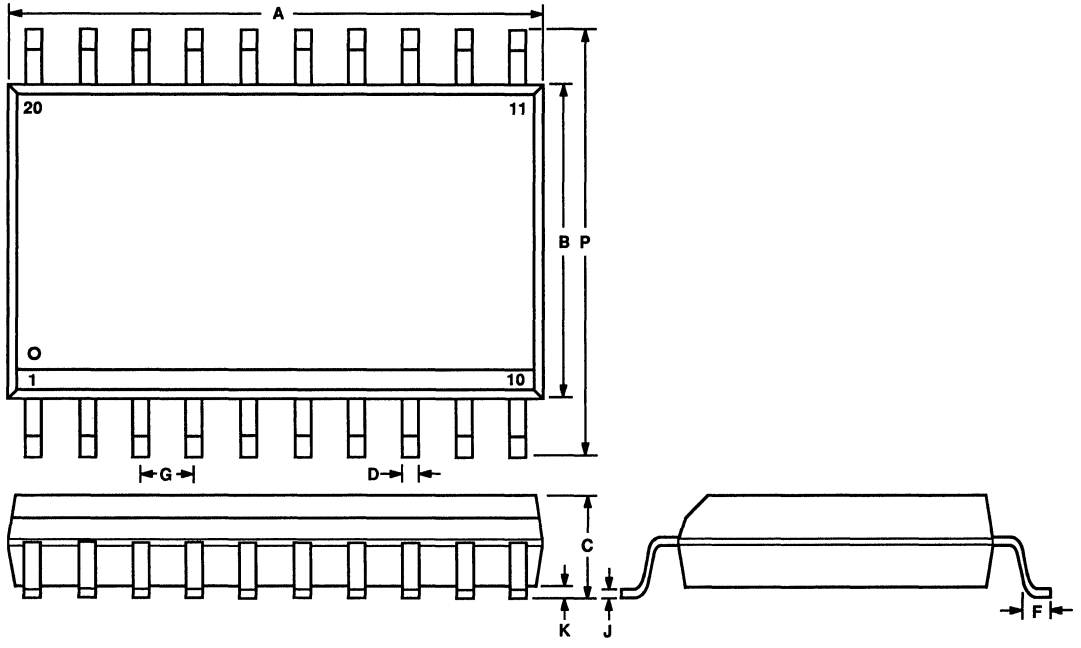
16-Lead Small Outline SOIC



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.398	0.413	10.10	10.50
B	0.291	0.299	7.40	7.60
C	0.089	0.104	2.26	2.64
D	0.014	0.022	0.36	0.56
F	0.018	0.034	0.46	0.86
G	0.50 BSC		1.27 BSC	
J	0.007	0.015	0.18	0.38
K	0.005	0.011	0.125	0.275
P	0.404	0.419	10.26	10.65

R-20

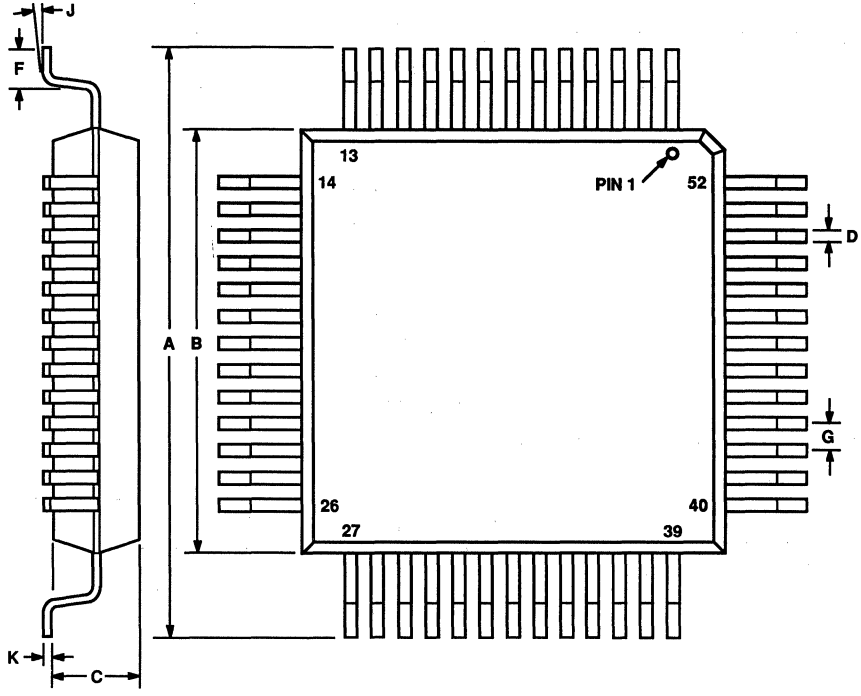
20-Lead Wide Body Plastic SOIC



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.496	0.512	12.60	13.00
B	0.292	0.300	7.40	7.60
C	0.093	0.104	2.36	2.64
D	0.014	0.019	0.36	0.48
F	0.016	0.050	0.40	1.27
G	0.50 BSC		1.27 BSC	
J	0.007	0.015	0.18	0.38
K	0.004	0.011	0.10	0.28
P	0.394	0.419	10.00	10.65

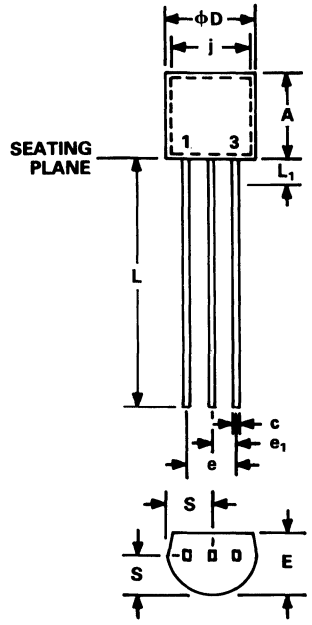
S-52

52-Lead Plastic Quad Flat Pack



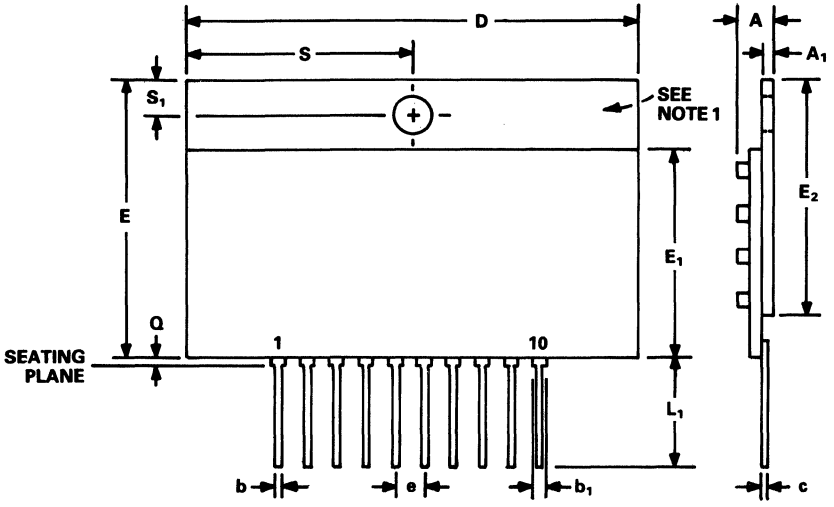
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.537	0.557	13.65	14.15
B	0.390	0.398	9.9	10.10
C	0.078	0.082	1.97	2.09
D	0.010	0.014	0.25	0.35
F	0.026	0.037	0.65	0.95
G	0.0256 BSC		0.65 BSC	
J	0.006	0.008	0.15	0.20
K	0.006	0.012	0.15	0.30

TO-92
3-Lead Plastic



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.170	0.210	4.58	5.33
c	0.016	0.019	0.407	0.482
ϕD	0.175	0.205	4.96	5.20
e	0.095	0.105	2.42	2.66
e_1	0.045	0.055	1.15	1.39
E	0.125	0.165	3.94	4.19
J	0.175	0.205	4.96	5.20
L	0.500		12.70	
L_1		0.050		1.27
S	0.080	0.105	2.42	2.66

Y-10
10-Lead Single In-Line Package (SIP)

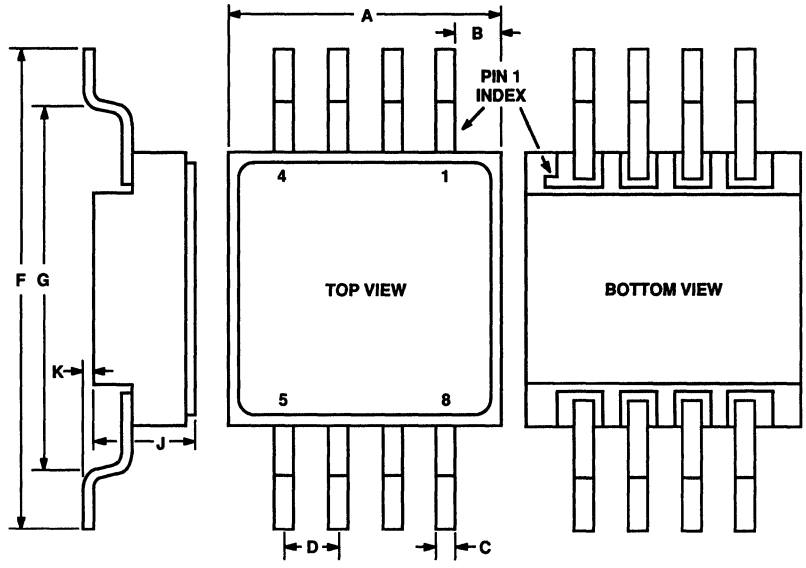


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.123	0.150	3.12	3.81
A_1	0.038	0.042	0.97	1.07
b	0.016	0.020	0.41	0.51
b_1	0.040	0.070	1.02	1.78
c	0.009	0.012	0.23	0.31
D	1.566	1.586	39.78	40.28
E	0.990	1.050	25.15	26.67
E_1	0.750 REF		19.05 REF	
E_2	0.810 REF		20.57 REF	
e	0.100 BSC		2.54 BSC	
L_1	0.150	0.350	3.81	8.89
Q	0.060	0.080	1.52	2.03
S	0.780 REF		19.51 REF	
S_1	0.115 REF		2.92 REF	

NOTE
1. Metal tab is electrically insulated from circuitry.

Z-8

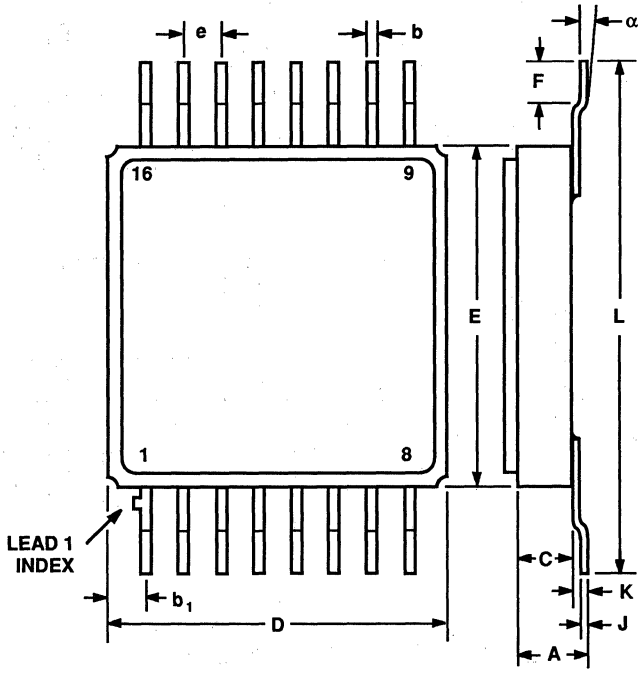
8-Lead Leaded Chip Carrier (Gull Wing)



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.250	0.260	6.35	6.61
B	0.028	0.049	0.711	1.25
C	0.015	0.019	0.38	0.48
D	0.045	0.055	1.14	1.40
F	0.433	0.457	10.90	11.60
G	0.323	0.347	8.20	8.81
J	0.083	0.103	23.37	23.87
K	0.015		0.381	

Z-16A

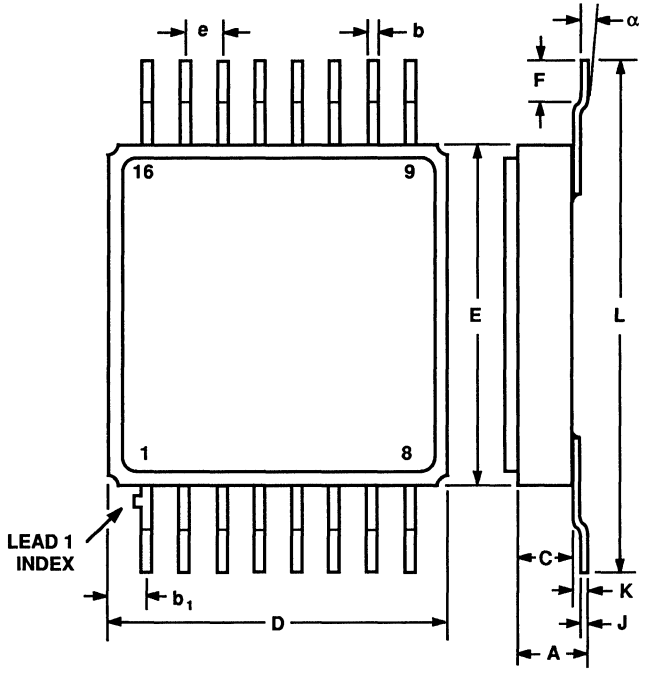
16-Lead Leaded Chip Carrier (Gull Wing)



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.103	0.133	2.61	3.38
b	0.013	0.017	0.33	0.43
b_1	0.040	0.060	1.02	1.52
C	0.080	0.100	2.03	2.54
D	0.442	0.458	11.23	11.63
E	0.442	0.458	11.23	11.63
e	0.045	0.055	1.14	1.40
J	0.007	0.010	0.18	0.25
K	0.023	0.033	0.58	0.84
L	0.675	0.685	17.15	17.40
α	−5°	+5°	−5°	+5°

Z-16B

16-Lead Leaded Chip Carrier (Gull Wing-Wide)



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.113	0.143	2.87	3.63
b	0.013	0.017	0.33	0.43
b_1	0.090	0.110	2.29	2.79
C	0.090	0.110	2.29	2.79
D	0.542	0.558	13.77	14.17
E	0.542	0.558	13.77	14.17
e	0.045	0.055	1.14	1.40
J	0.007	0.010	0.18	0.25
K	0.023	0.033	0.58	0.84
L	0.775	0.785	16.69	19.94
α	−5°	+5°	−5°	+5°

Appendix Contents

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Worldwide Sales Directory . . . . . 21 – 10

Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Massachusetts, U.S.A. (617-329-4700).

MODEL NUMBERING

Many of the data sheets in the Databook for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. IC and hybrid part numbers are created using one of these two systems:

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit model number, for some models, the combination [digit][letter][two or three digits] is used instead of ADXXXX, e.g., 2S80 an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows the somewhat different numbering scheme used by our Computer Labs Division for some hybrid circuits. The number starts with a three-character alphabetic prefix, followed by a hyphen, a three- or four-digit number, and alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

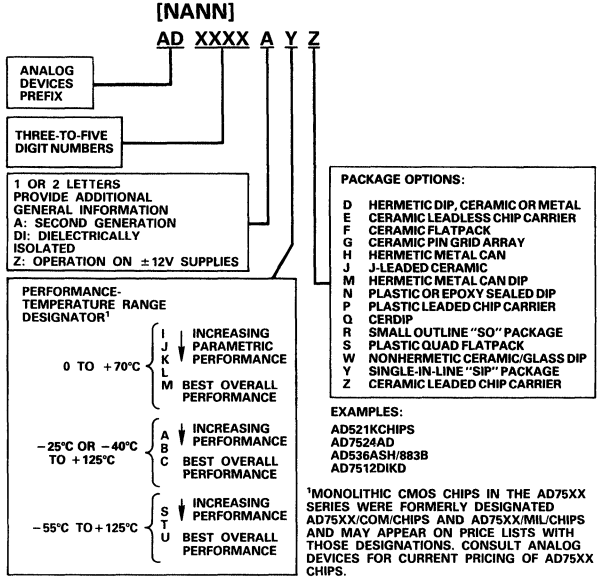

Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades have the Added Suffix, /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

***For some models, the combination [digit][letter][two or three digits] is used instead of ADXXXX, e.g., 2S80.**

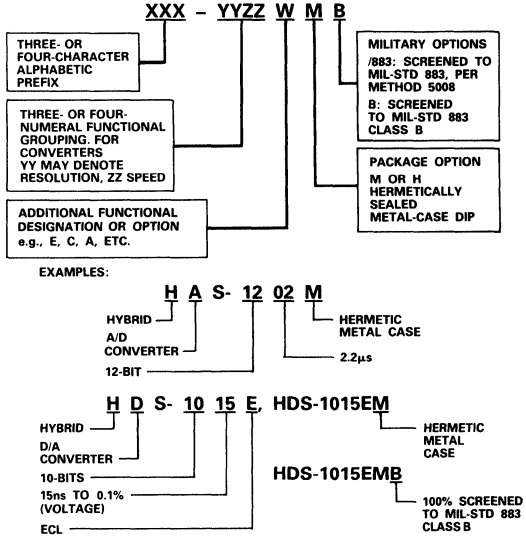

Figure 2. Computer Labs Video Hybrid Product Designations

SECOND SOURCE

In addition to our many proprietary products, we also manufacture devices that are fit-, form-, and function-compatible (and often superior in performance and reliability) to popular products that originated elsewhere. For such products, we usually add the prefix "AD" to the familiar model number (example: ADDAC85C-CBI-V).

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via TWX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. On all orders under fifty dollars ($50.00), a five-dollar ($5.00) processing charge is required.

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and µMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Not Included in the Databook (But Still Available)

The information published in this Databook is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs or in designs for which they are uniquely suitable. Data sheets on these products are available upon request.

Model	Model	Model	Model
AD101	AD7541	HOS-050/050A/050C	148
AD201	AD7546	HOS-060	171
AD293	AD7550	HOS-200	184
AD294	AD7552	RDC-1700	234
AD301	AD7574	RDC-1702	235
AD301AL	AD9611	RDC-1704	260
AD370/371	AD9686	RDC-1725	261
AD503	ADC-14I/17I	RDC-1726	272
AD504	ADC1111	RDC-1768	273
AD506	ADC1143	RTM Series	275
AD510	AD DAC-08	SDC1700	276
AD515	ADEB770	SDC1702	277
AD518	CAV-1210	SDC1704	285
AD533	DAC-QS	SDC1725	288
AD535	DAC-QZ	SDC1726	310
AD545	DAC-10Z	SDC1768	428
AD567	DAC-12M	SHA-2A	429
AD611	DAC-12QS	SHA-5	433
AD651	DAC-12QZ	SHA-1134	434
AD1403	DAC1009	SHA-1144	435
AD2004	DAC1108	STM Series	436
AD2006	DAC1132	2B24	440
AD2008	DAC1146	2B34	442
AD2009	DAC1420	2B35	450
AD2016	DAC1422	2B50	451
AD2020	DAC1423	2B52	452
AD2033	DAS1128	2B53	453
AD2040	DAS1150	2B56	458
AD3554	DAS1151	2B57	460
AD3860	DAS1152	2B58	603
AD7110	DAS1153	2B59	606
AD7118	DAS1155	4B Series	610
AD7240	DAS1156	40	756
AD7506	DAS1157	44	903
AD7507	DAS1158	45	906
AD7520	DRC1705	46	915
AD7521	DRC1706	48	926
AD7522	DSC1705	50	947
AD7523	DSC1706	51	948
AD7525	HDH-1205	52	950
AD7530	HDS-1240E	118	959
AD7531			968

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but – as a rule — they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
AD108/208/308	AD705	AD2038	None	DAC-10DF	AD568
AD108A/208A/308A	AD705	AD5010/6020	AD9000	DAC-10H	DAC-10Z
AD111/211/311	AD790	AD6012	AD565A	DAC-14QM	DAC1136
AD345	AD1321/1322	AD7115	AD7111	DAC-16QM	DAC1136
AD351	AD790	AD7513	ADG201A	DAC1009	AD767
AD362	AD1362	AD7516	AD7510DI	DAC1106	AD568
AD376	AD1376	AD7519	None	DAC1112	DAC12QS
AD501	AD711	AD7527	AD7548	DAC1118	AD767
AD502	AD711	AD7544	AD7548	DAC1122	AD7541A
AD505	AD509	AD7555	AD1175K	DAC1125	AD7533
AD508	AD517	AD7560	None	DRC1605/06	DRC1705/06; SDC1740
AD511	AD711	AD7570	AD7579/AD7580	DRC1765/66	AD2S65/66
AD512	AD711	AD7571	AD7579/AD7580	DSC1605/06	DSC1705/06; SDC1740
AD513	AD711	AD7583	AD7880+MUX	DSC1765/66	AD2S65/66
AD514	AD711	AD9011	AD9002	DTM1716/17	Consult ADI
AD516	AD711	AD9615	AD9611/AD9617	HAS-0802	HAS1202A
AD520	AD524	AD9685	AD96685	HAS-1002	HAS1202A
AD523	AD549	AD9687	AD96686	HAS-1202	HAS1202A
AD528	AD711/744	AD9688	AD9002/AD9028	HDD-1015	AD9712A
AD530	AD533	ADADC-816	AD7820/AD7821	HDD-1409	None
AD531	AD532	ADC-8S	AD673	HDH-0802	AD9713A
AD540	AD544	ADC-10Z	AD574A	HDH-1003	AD9713A
AD559	AD557/AD558	ADC-12QL	AD7578	HDL-3805	ADV453/ADV478
AD565	AD565A	ADC-12QZ	AD574A/AD674A	HDL-3806	ADV453/ADV478
AD566	AD566A	ADC-1100	AD7550/AD7552	HDM-1210	AD668/AD9713A
AD612	AD524	ADC1102	AD7870	HDS-0810E	AD9712A
AD614	AD524	ADC1103	AD7572A	HDS-0820	AD9713A
AD801	AD711	ADC1105	AD7550/AD7552	HDS-1015E	AD9712A
AD810-813	None	ADC1109	AD7572A	HDS-1025	AD9713A
AD814-816	None	ADC1111	AD574A	HDS-1250	AD668/AD9713A
AD818	None	ADC1121	AD7880	HOS-100AH/SH	None
AD820-822	None	ADC1123	AD7880	HTC-0300	HTC-0300A
AD830-833	None	ADC1133	AD574A	HTC-0500	HTC-0300A
AD835-839	None	ADC-QM	AD574A/AD674A	IPA-1751	IPA-1764
AD1145	AD7846	ADC-QU	AD574A/AD674A	IRDC1730-33	2S80
AD1408	AD558	AD DAC100	AD561	MAH-0801	AD9005
AD1508	AD558	ADG200	None	MAH-1001	AD9005
AD1678	AD678	ADG201	ADG201A	MAS-0801	AD9005
AD1679	AD679	ADLH0032G/CG	AD843	MAS-1001	AD9005
AD1779	AD779	ADLH0033G/CG	AD9620/AD9630	MAS-1202	AD9005
AD2003	AD2021	ADM501	None	MATV0811	AD9012/48
AD2022	None	ADP501	None	MATV-0816	AD9012/48
AD2023	None	ADSHC-85	AD585	MATV-0820	AD9012/48
AD2024	None	ADSHM-5	HTC-0300A	MCI-1794	2S80 + CCT
AD2025	None	API1620/1718	Consult ADI	MDA Family	AD9712A/13A
AD2027	None	BDM1615/16/17	SDC1740 Series+CCT	MDH Family	AD9712A/13A
AD2028	None	CAV-0920/1020	AD9020/9060	MDMS Family	AD9712A/13A
AD2036	None	CAV-1202	AD9005	MDS Family	AD9712A/13A
AD2037	None	CAV-1205	AD9005	MDSL Family	AD9712A/13A

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
MOD-1005/20	AD9020/60	THC-Family	HTC-0300A	287	None
OSC-1754	OSC-1758	THS-Family	HTC-0300A	301 (Module)	52
RAC1763	Consult ADI	TSL1612	Consult ADI	302	310 (Module)
RDC1602/03	RDC1702/03	1S10/20	1S40; 2S80/82	311	AD549
RDC1711/21	2S80	1S14/24/44/64	1S74	350	None
RDC1767	RDC1768	1S61	1S60; 2S80/82	424	435/AD534
RSCT1621	2S80	2S20	None	426	AD534
RTI-1200	RTI-711 Series	9S70/71/72	None	427	None
RTI-1201	RTI-711 Series	9S75/76/79	None	432	None
RTI-1202	RTI-711 Series	41	AD515A	454	AD537
RTM1630-34	RTM1680/83	42	AD549	456	AD537
RTM1636	Consult ADI	43	AD549	602J10	AD524
RTM1660/63/71/72	Consult ADI	47	48	602J100	AD524
RTM1679	None	102	48	602K100	AD524
RTM1681/86/87/89	Consult ADI	106	118	603	AD524
RTM1690/96	Consult ADI	107	118	605	AD524
RTM1697	None	108	52	751	AD640
RTM1736/37	RDC1740 + CCT	110	48	752	759
SAC1763	Consult ADI	120	50	901	904
SBCD1752/53/56/57	SDC1740 + CCT	141	40	907	921
SCDX1623	None	142	48	908	921
SCM1677	None	143	52	909	921
SDC1602/3/4	SDC1702/03/04/40	146	AD382	931	None
SDC1711/21	2S80	149	50	932	None
SDC1767	SDC1768	153	AD517	933	None
SERDEX	μMAC-5000	161	None	935	None
SHA-1A	AD585	163	None	942	None
SHA-3	AD585	165	None	944	None
SHA-4	AD585	170	None	946	None
SHA-6	AD1154	180	AD OP-07	948	947
*SHA1114	AD585	183	184	950	None
SPA-1695	None	220	234	956	None
SSCT1621	2S80	230	235	971	921
STM1630-34	STM1680/83	231	233		
STM1636	Consult ADI	232	235		
STM1660/63/71/72	Consult ADI	233	None		
STM1679	None	274J	284J		
STM1681/86/87/89	Consult ADI	279	286J		
STM1690/96	Consult ADI	280	281		
STM1697	None	282J	292A		
STM1736/37	SDC1740 + CCT	283J	292A		

Analog Devices provides a wide array of FREE technical publications. These include Data Sheets for all products, Catalogs, Application Notes and Guides and four serial publications: *Analog Productlog*, a digest of new-production information; *DSPatch,*™ a newsletter about digital signal-processing (applications); *Analog Briefings,*® current information about products for military/avionics and the status of reliability at ADI; and *Analog Dialogue,* our technical magazine, with in-depth discussions of products, technologies and applications.

In addition to the free publications, seven technical reference books are available at reasonable cost. Subsystem products are supported with hardware, software, and user documentation, at prices related to content.

Brief descriptions of typical publications appear below. For copies of any items, to subscribe to any of our free serials or to request any other publications, please get in touch with Analog Devices or the nearest sales office.

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Data Acquisition Products Databooks. Contain selection guides, data sheets and other useful information about all Analog Devices ICs, hybrids, modules and subsystem components recommended for new designs. The 1989/90 series consists of:

DATA CONVERSION PRODUCTS DATABOOK—1989/90. Data Sheets and Selection Guides on D/A, A/D, V/F, and F/V Converters, Sample-Track/Hold Amplifiers, Voltage References, Multiplexers & Switches, Synchro-Resolver Converters, Data Acquisition Subsystems, Application-Specific ICs. (Available FREE.)

DSP PRODUCTS DATABOOK—1989. Data Sheets, Selection Guides and Application Notes on DSP Microprocessor, Microcoded Support Components, Floating-Point Components and Fixed-Point Components. (Available FREE.)

LINEAR PRODUCTS DATABOOK—1990. Data Sheets and Selection Guides on Op Amps, Instrumentation Amplifiers, Isolators, RMS-to-DC Converters, Multipliers/Dividers, Log/Antilog Amplifiers, Comparators, Temperature-Measuring Components and Transducers, Special Function Components, Digital Panel Instruments, Signal-Conditioning Components and Subsystems, Mass Storage Components, ATE Components, Automotive Components, Bus Interface and Serial I/O Products, Application Specific ICs. (Available FREE.)

MILITARY PRODUCTS DATABOOK. Information and data on products processed in accordance with MIL-STD-883 Class B.

DATA-ACQUISITION AND CONTROL CATALOG—1990. Tutorial and Configuration Guide, with Product Reference and Index. Bus-Compatible I/O Boards for: IBM PS/2,* IBM PC/XT/AT,* STD Bus, VMEbus, MULTIBUS.† Distributed I/O Subsystems—fixed-function front ends, programmable units, and distributed control systems. Modular Signal Conditioners—analog and digitizing. Analog Signal-Conditioning Panels—isolated and non-isolated. Digital Subsystems—16- and 24/32-channel. Software—DOS drivers and applications packages.

POWER SUPPLIES–Linear Supplies•DC-DC Converters. 12-page Short-Form Catalog listing AC/DC Power Supplies, Modular DC/DC Converters, Power-Supply Test Procedures, Transients, Thermal Derating, Mechanical Outlines of Packages and Sockets.

APPLICATION NOTES AND GUIDES

All are available upon request.

Application Notes.

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- "FIFO Operation and Boundary Conditions in the AD1332 and AD1334."
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- "Implement Infinite Sample-and-Hold Circuits Using Analog Input/Output Ports."
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- "Simultaneous and Independent Sampling of Analog Signals with the AD1334."
- "The AD7574 Analog-to-Microprocessor Interface."

Amplifiers:
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- "CMOS DACs and Operational Amplifiers Combine to Build Programmable-Gain Amplifiers" (in 2 parts: *I and II*).
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D/A Converters:
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"Three-Phase Sine-Wave Generation Using the AD7226 Quad DAC."

Digital Signal-Processing: (Note: Seven additional DSP Application Notes are incorporated in the *1989 DSP Products Databook*.)
"A Guide to Designing Microcoded Circuits."
"Considerations for Selecting a DSP Processor" (ADSP-2100A vs. TMS320C25).
"Implement a Cache Memory in Your Word-Slice® System."
"Interfacing the AD7572 to High-Speed DSP Processors."
"Sharing the Output Bus of the ADSP-1401 Microprogram Sequencer."
"Variable-Width Bit Reversing with the ADSP-1410 Address Generator."
"Wait-State Generation on the ADSP-2100 and ADSP-2100A."

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"Using the 2S80 Series Resolver-to-Digital Converters with Synchros: Solid-State Scott-T Circuit."
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Application Guides.

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Applications Guide for Isolation Amplifiers and Signal Conditioners. A 20-page guide to specifications and applications of galvanically isolated amplifiers and signal conditioners for industrial, instrumentation and medical applications.

CMOS DAC Application Guide 3rd Edition by Phil Burton (1989—64 pages). Introduction to CMOS DACs, Inside CMOS DACs, Basic Application Circuits in Current-Steering Mode, Single-Supply Operation Using Voltage-Switching Mode, The Logic Interface, Applications.

ESD Prevention Manual – Protecting ICs from electrostatic discharges. Thirty pages of information that will assist the reader in implementing an appropriate and effective program to assure protection against electrostatic discharge (ESD) failures.

High-Speed Data Conversion – A 24-page short-form guide to video and other high-speed A/D and D/A converters and accessories, in forms ranging from monolithic ICs to card-level products.

RMS-to-DC Conversion Application Guide 2nd Edition by C. Kitchin and L. Counts (1986—61 pages). RMS-DC Conversion: Theory, Basic Design Considerations; RMS Application Circuits; Testing Critical Parameters; Input Buffer Amplifier Requirements; Programs for Computing Errors, Ripple and Settling Time.

Surface Mount IC—A 28 page guide to ICs in SO and PLCC packages. Products include op amps, rms-to-dc converters, DACs, ADCs, VFCs, sample-holds and CMOS switches.

DSP MANUALS

Available at no charge for single copies; write on letterhead.

ADSP-2100 Family Support Publications—for the ADSP-2100 and ADSP-2101 single-chip signal processors.

ADSP-2100 USER'S MANUAL. Introduction, Computational Units, Data Moves, Program Control, System Interface, Instruction Set Overview, Appendixes. 162 pages.

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ADSP-2101 USER'S MANUAL—Architecture. Introduction, Computational Units, Data Moves, Program Control, Timer, Serial Ports, System Interface, Memory Interface, Instruction Set Overview, Appendixes. 184 pages.

TECHNICAL REFERENCE BOOKS—Can be purchased from Analog Devices, Inc.; send check for indicated amount to One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. If more than one book is ordered, deduct a discount of $1 from the price of each book. Price of the entire set of seven books is $129 (in effect, the synchro, transducer, and nonlinear circuits books are free). VISA or MasterCard accepted; phone (617) 461-3392.

ANALOG-DIGITAL CONVERSION HANDBOOK: Third Edition, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice Hall (1986). A comprehensive guide to A/D and D/A converters and their applications. This third edition of our classic is in hardcover and has more than 700 pages, an Index, a Bibliography, and much new material, including: video-speed, synchro-resolver, V/F, high-resolution, and logarithmic converters, ICs for DSP, and a "Guide for the Troubled." Seven of its 22 chapters are totally new. $32.95

NEW—*DIGITAL SIGNAL-PROCESSING APPLICATIONS USING THE ADSP-2100 FAMILY*, by the Applications Staff of Analog Devices, DSP Division; edited by Amy Mar (628 pages). Englewood Cliffs NJ: Prentice Hall (1990). Bridge the gap between DSP algorithms and their real-world implementation on state-of-the-art signal processors. Each chapter tackles a specific application topic, briefly describing the algorithm and discussing its implementation on the ADSP-2100 family of DSP chips. Comprehensive source-code listings are complete with comments and accompanied by explanatory text. Programs are listed on a pair of supplementary diskettes—furnished with the book. Application areas include fixed- and floating-point arithmetic, function approximation, digital filters, one- and two-dimensional FFTs, image processing, graphics, LP speech coding, PCM, ADPCM, high-speed modem algorithms, DTMF coding, sonar beamforming. Additional topics include memory interface, multiprocessing, and host interface. The book can serve as a companion to *Digital Signal Processing in VLSI*. Price includes diskettes. $38.00

NEW—*DIGITAL SIGNAL PROCESSING IN VLSI*, by Richard J. Higgins. Englewood Cliffs NJ: Prentice Hall (1990). An introductory 614-page guide for the engineer and scientist who needs to understand and use DSP algorithms and special-purpose DSP hardware ICs—and the software tools developed to carry them out efficiently. Real-World Signal Processing; Sampled Signals and Systems; The DFT and the FFT Algorithm; Digital Filters; The Bridge to VLSI; Real DSP Hardware; Software Development for the DSP System; DSP Applications; plus Bibliography and Index. $38.00

NEW—*HIGH-SPEED DESIGN SEMINAR*, published by Analog Devices (1990). A 496-page guide to the practical application of high-speed semiconductor devices in processing of analog signals. Topics include: data conversion, digital video applications, high-speed sample-holds and operational amplifiers, nonlinear signal processors (including log amps), comparators and pin electronics, time-delay generators, phase-locked loops, direct digital synthesis, computer graphics and RAM-DACs, and high-speed techniques. $20.00

NONLINEAR CIRCUITS HANDBOOK: Designing with Analog Function Modules and ICs, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1974). A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction devices. Principles, circuitry, performance, specifications, testing, and application of these devices–contains 325 illustrations. $5.95

SYNCHRO & RESOLVER CONVERSION, edited by Geoff Boyes. Norwood, MA; Analog Devices, Inc. (1980). Principles and practice of interfacing synchros, resolvers, and Inductosyns* to digital and analog circuitry. $11.50

TRANSDUCER INTERFACING HANDBOOK: A Guide to Analog Signal Conditioning, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1980). A book for the electronic engineer who must interface transducers for temperature, pressure, force, level, or flow to electronics, these 260 pages tell how transducers work—as circuit elements—and how to connect them to electronic circuits for effective processing of their signals. $14.50

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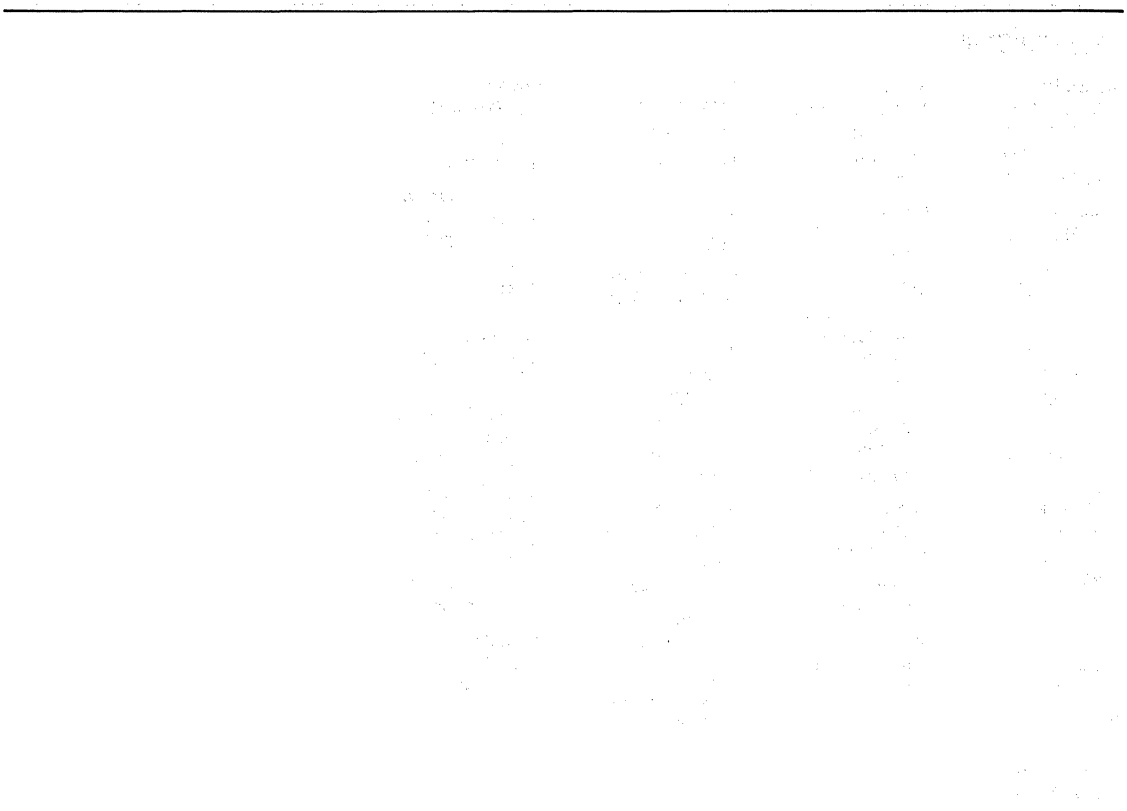

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